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MOS BRIEF 5

MOS CLOCK SAVERS

Extra effort in the design of MOS clock-drive networks can pay large dividends in power savings and lower component costs. Compared with straightforward designs, component counts and power dissipation often can be cut in half or more by reorganizing the MOS subsystem to reduce operating frequency and duty cycle, by redistributing the clock power with buffers, or by combining these approaches.

The larger the drive network, the more opportunities the designer has to economize if he appreciates the power-frequency-load tradeoffs of MOS devices. For openers, consider the 20,000-bit serial memory in Figure 1. It could be built with 100

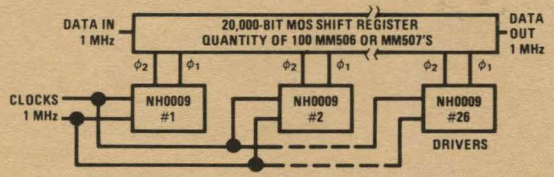

FIGURE 1. Straightforward Drive Network Can Be Costly

MM506 dual 100-bit dynamic shift registers and 26 NH0009 two-phase clock drivers at 70°C. Each MM506 presents a capacitive load of about 80 pF and takes a voltage swing of 16V. At 1 MHz, an NH0009 can drive four MM506's. (If single-phase clocks were preferred, NH0007 or NH0012 drivers could be used.)

A designer could cut the cost and power of the Figure 1 design by reducing operating frequency and data rates. The energy needed to charge and discharge load capacitance is, in any driver,

$$P_{transient} = CV^2 f$$

where C is the load, V the voltage change, and f the repetition rate. If the frequency is halved, for instance, each driver can handle twice the number of MOS devices. At a frequency of 200 kHz, our drivers can handle 80 complex MOS devices in well-designed systems. The savings can be greater than 1:1 because reductions in duty cycle and internal power consumption of the drivers and registers can be made at lower frequencies. Total power dissipation is the sum of load and internal power consumption.

Suppose, though, that a reduced data rate is not acceptable. If the shift registers are rearranged and the data multiplexed as in Figure 2, the operating frequency of the registers can be cut to 250 kHz and each NH0009 can drive many additional MM506's. A suitable clock format can be provided by only two drivers, 24 drivers being replaced by a few bipolar binaries and seven gates, for a considerable savings in power and component costs. The registers will also dissipate much less power. As an alternative, we could keep the drivers (26) and raise the data rate to 4 MHz.

It would be difficult to find a more economical drive network for a large system than Figure 3. Here, a single NH0009 drives remote pnp-npn switches that buffer and distribute the clock signals. If each buffer is made with 2N4142 and 2N4140 transistors, each could do the work of two NH0009's. Transient power would remain the same as in Figure 1, since the load is not changed, but each transistor would dissipate only one-fourth the average DC power of an NH0009. Such a network can synchronously operate a very large MOS memory assembly, whether it is a serial system like Figure 1 or a multiplexed configuration like Figure 2.

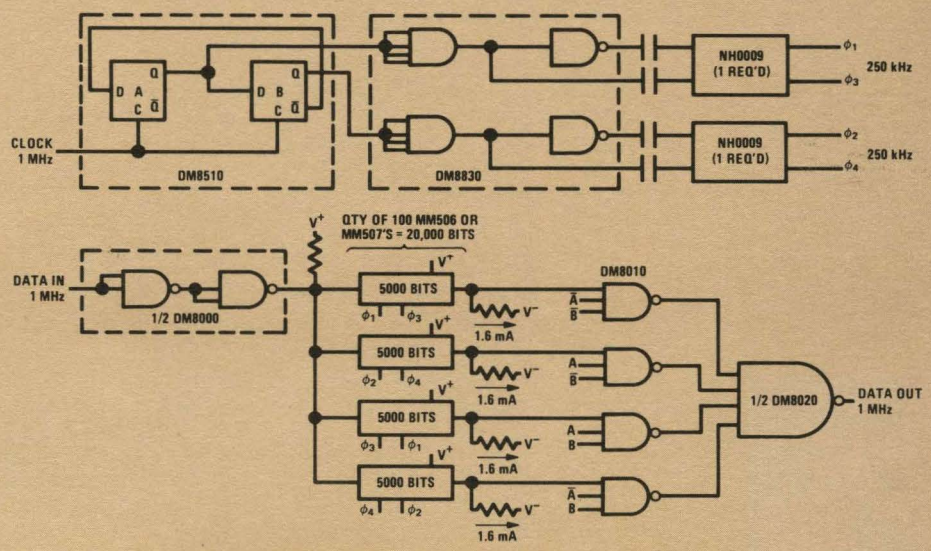

FIGURE 2. Parallel Organization Eliminates 17 Drivers

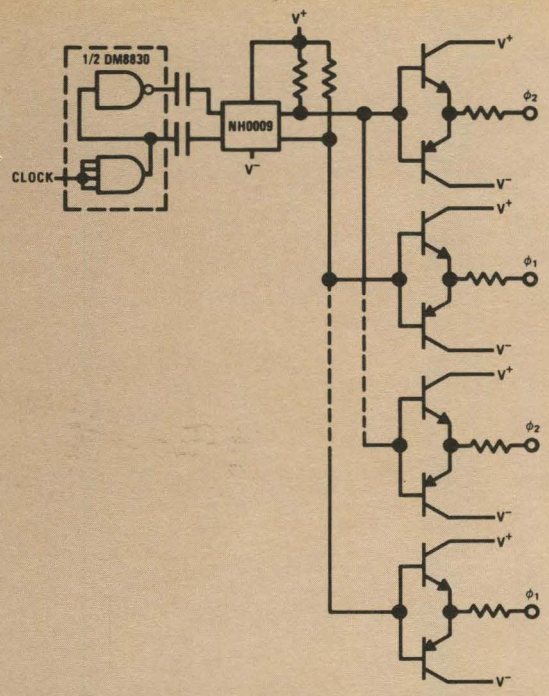

FIGURE 3. Remote Buffers Redistribute Clock Signals

The NH0009 simplifies these examples because it adapts to any practical variation in C, V and f. Discrete-component drivers such as Figure 4 can also do a good job, but clutter up a diagram (as well as PC boards). Figure 5 is a neater subassembly because a voltage translator interfaces the TTL control lines and the buffers. Either of these circuits can drive several MOS devices.

Whatever technique the designer prefers, he must take certain precautions. Since the drivers source and sink large currents into their capacitive loads,

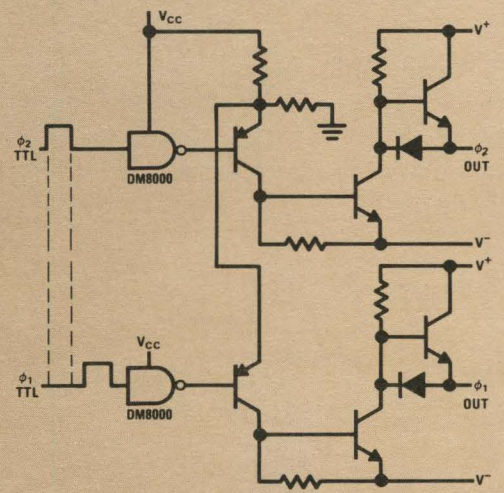

FIGURE 4. Typical Discrete-Component MOS Driver

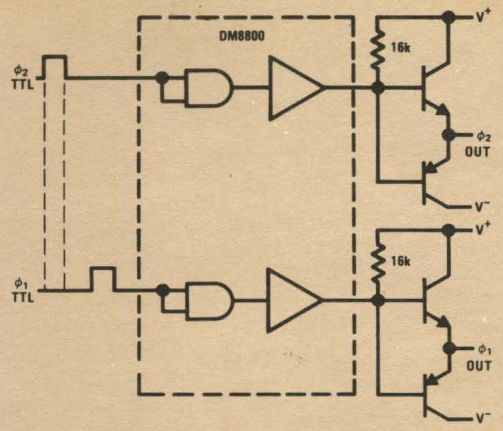

FIGURE 5. Voltage Translator Simplifies Driver Design

they require adequate power-supply decoupling. In large systems, clock-line layouts should be adjusted to avoid excessive clock swinging, of course. Clock lines may have to be terminated to prevent oscillations and noise generation. During positive logic transitions, no clock line should swing more than 0.5V more positive than the most positive bias on the MOS device driven. To avoid malfunctions due to excessive overshoot, the transitions may have to be clamped with a germanium diode, or other low-impedance terminations such as the remote buffer driver shown in Figure 3.

Problems like those are overcome nicely in Figure 3. The long lines between the NH0009 and the buffers carry relatively small currents. The collector-base junctions in the transistors act as clamps and terminations, while the emitter resistors control clock transition time and minimize overshoot. A pullup resistor was added to the NH0009 to maintain the required DC margin and to keep impedance low during the logic "0" state of the buffers.

Overall system costs can be further reduced by techniques—such as a one-resistor TTL/MOS signal interface—that are described in other National Semiconductor literature. Finally, to keep this discussion of savings in perspective, it should be remembered that merely using MOS shift registers, read-only memories, character generators and other large-scale MOS circuits in a digital system will usually make the cost considerably less than an all-bipolar design. No other process is as stingy with valuable silicon "real estate". The register in these examples, the MM506, contains 1240 elements in a 92-by-78-mil chip. And it consumes less than a milliwatt per storage cell.

Data sheets and additional application information on the MOS devices are available upon request.

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