Voltage Measurement with the PC87365/6

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The PC87365 and PC87366 are the latest additions to National's PC8736x family of SuperI/O devices. These devices integrate most of the commonly found SuperI/O peripheral functions, and analog functions including voltage and temperature measurement.

This application note describes in detail the new voltage measurement module integrated in the PC87365 and PC87366 SuperI/O devices, the Voltage Level Monitor (VLM). The VLM, which incorporates an A/D converter (ADC), monitors various voltages in the system, reports their values to system monitoring software and can set an alarm when any of these voltages is outside a specified range.

ARCHITECTURE

The VLM, along with the ADC, has a set of Control, Configuration and Status registers and digital circuitry that control its operation. Access to the VLM Configuration registers is through the PC87365/6 Index and Data registers, located at I/O addresses 2Eh, 2Fh (when BADDR strap is set to 0), or 4Eh, 4Fh (when BADDR strap is set to 1). Logical device number 0D has been assigned to the module. To enable the device, 01h should be written to the logical device Activate register at location 30h. See the *BIOS Porting Guide for LPC SuperI/O PC8736X* for more details.

User-supplied external V_{REF} can be selected. V_{REF} is internally scaled. Refer to the PC87365/6 datasheets for recommended V_{REF} values.

Once enabled, the VLM continuously monitors all enabled channels and stores the results. Conversions are disabled when a power loss condition is indicated by $\overline{SLPS3}$ becoming active (for ACPI compliant devices). VLM register contents are maintained by V_{SB} power.

Figure 1 shows a block diagram of the VLM. An analog MUX selects one of the enabled voltage channels. Voltage sampled is measured by an 8-bit ADC using a successive approximation technique. The measured result is stored in the Read Channel Voltage (RDCHV) register corresponding to the selected input channel. The voltage reading is compared to two user-set limits: V_{HIGH} and V_{LOW}. If the voltage reading is outside either of these limits, the respective status bit (Channel High Limit Exceeded or Channel Low Limit Exceeded) in the Voltage Channel Configuration and Status (VCHCFST) register is set. The Status bit stays active until it is cleared by software. An ALARM Status bit in the Voltage Event Status 0/1 (VEVSTS0/1) register is set when the Channel High Limit Exceeded or the Channel Low Limit Exceeded bit is set for the respective channel.

The $\overline{SMI}$ output generates an interrupt if any enabled $\overline{SMI}$ event occurs. Each bit in the VEVSTS0/1 register has a corresponding $\overline{SMI}$ Enable bit in the Voltage Event to $\overline{SMI}$ 0/1 (VEVSMI0/1) register. When any Status bit and its corresponding $\overline{SMI}$ Enable bit are set, the $\overline{SMI}$ output is active.

The IRQ output generates an interrupt if any enabled IRQ event occurs. Each bit in the VEVSTS0/1 register has a corresponding IRQ Enable bit in the Voltage Event to IRQ 0/1 (VEVIRQ0/1) register. When any Status bit and its corresponding IRQ Enable bit are set, the IRQ output is active.

The VLM can monitor up to seven external system voltages. In addition, it internally monitors V_{SB}, V_{DD}, AV_{DD} and V_{BAT} power supplies.

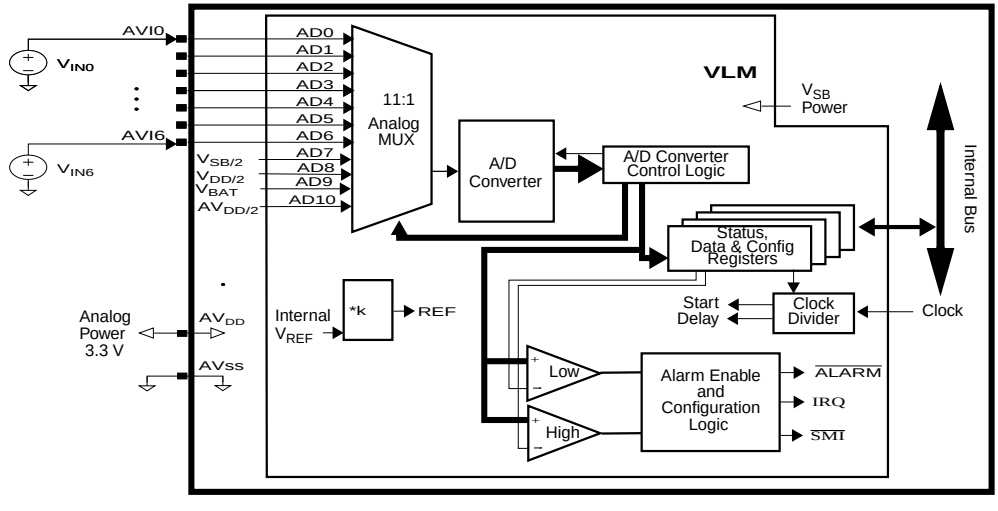

Figure 1. VLM Block Diagram

MEASURING VOLTAGE

The VLM incorporates an 8-bit, successive approximation ADC. It has approximately 12 mV LSB, yielding a 0V to 3.00V input range determined by $K*V_{REF}$, where K is a scale factor that scales a reference voltage (V_{REF}) applied to the VLM to approximately 3V. V_{REF} can be either from an external or an internal reference supply, as shown in Figure 1.

Figure 2 shows analog input examples of the VLM. Voltages in the range of 0V to 2.5V can be directly connected to the inputs. The 3.3V, 5V and 12V inputs should be attenuated with external resistors to any desired value within the input range. In a typical application, the input voltage divider can be selected to provide 2.6V at the analog inputs of the VLM. This is sufficiently high for good voltage resolution, while providing a margin of about 15% on the upper end for voltage fluctuations that can be tracked by the VLM. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 between 10 KΩ and 100 KΩ. This is low enough to avoid errors due to leakage currents. Then select R1 so that the value of V_{IN} is less than 2.6V. The following equation demonstrates the relationship between these variables:

$$R_1 = R_2\left(\frac{V_S}{V_{IN}} - 1\right) \qquad (1)$$

Calculate the measured voltage value according to the equation below:

$$V_S = (K_M + 1)*V_{IN} \qquad (2)$$

$$\text{where: } K_M = \frac{R_1}{R_2} \qquad (3)$$

For the negative inputs, first select a value for R2 between 2 KΩ and 20 KΩ. This is low enough to avoid errors due to leakage currents. Then select R1 to provide 2.6V input according to the equation below:

$$R_1 = R_2\left(\frac{V_{IN} - V_S}{AV_{DD(MAX)} - V_{IN}}\right) \qquad (4)$$

Calculate the measured voltage value according to the equation below (where V_M is the same as in equation 3 above):

$$V_S = (1 + K_M)*V_{IN} - K_M*AV_{DD} \qquad (5)$$

Table 1 shows examples of R1 and R2 values for various input voltages.

Table 1. Selecting R1 and R2 Values Based on Input Voltages

Voltage Source (V_S)	R1 or R_{IN} Value (KΩ)	R2 Value (KΩ)	Voltage at Analog Input (V)	Voltage Multiplier (K_M)
+1.0	10	None	+1.0	1
+2.5	10	None	+2.5	1
+3.3	2.7	10	+2.6	0.27
+5	9.2	10	+2.6	0.92
+12	36	10	+2.61	3.6
-12	73	5	+2.6	14.6
-5	38	5	+2.6	7.6

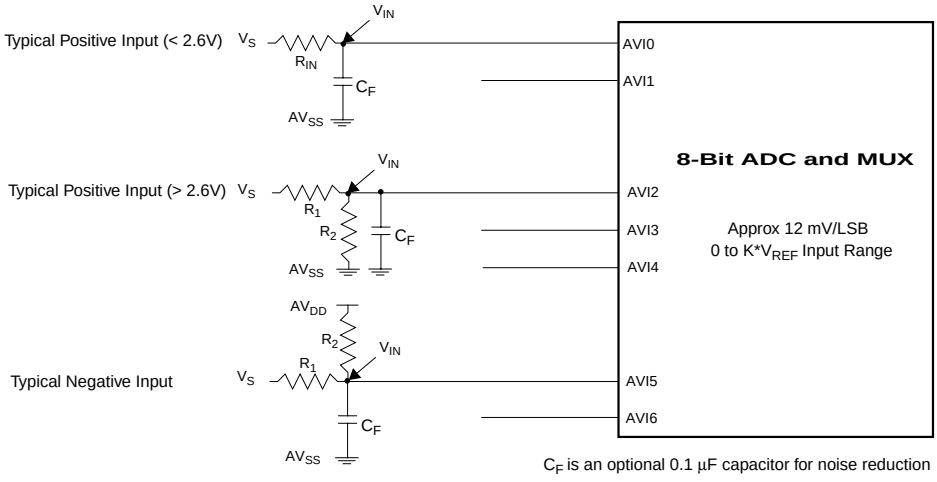

Figure 2. Analog Input Examples

AV_{DD} can be measured using Channel 10 of the VLM. Use the computed value of AV_{DD} (see below) in equation 5 for improved accuracy.

Measured voltage is stored in channel registers in the form of an integer between 0 and 255. Measured V_i can be calculated using the equation $V_i = K*V_{REF}$ *$RDCHV_i/256$, where $RDCHV_i$ is the value stored in the channel register. Channels 7, 8 and 10 are internally divided by 2. Calculate V_i for these channels using the following equation: $V_i = K*V_{REF}*RDCHV_i/128$. Note that the scale factor K has been set to 2.45.

MEASUREMENT ACCURACY

The obvious advantage of such a resistive network is that a larger voltage range can be measured.

By not dividing down the voltage using external resistive networks, the following advantages apply:

1. Current drawn from the source is minimized.
2. Resolution of measurement is maximized.

If a channel is not divided down, 1 LSB of measured data gives 2.97/256 = 11.5mV. Measuring 12V with dividers, 1 LSB of measured data gives 12/256 = 46.9mV. Assuming perfect resistors, the supply can be measured with an accuracy of ±.4%; however, measurement resolution is lower for higher supply voltages.

A source of error in voltage measurement, using resistor ratio-basd voltage dividers, is the degree of precision of the dividers. Resistors with ±1% precision result in up to 2% error in the measured value of Vs, if equal values of R1 and R2 are used in the divider. Hence, it is recommended to use precision resistors (R1 and R2) in order to maintain measurement accuracy.

Accuracy of the VLM is specified in the datasheet as ±2 LSB, which translates to ±.8% error when measuring voltages below 3V. For 5V and 12V supply measurements with ±1% precision resistor dividers, total accuracy would be about ±2%, assuming worst case numbers for errors.

INTERNAL VOLTAGE MEASUREMENT

System supply voltages V_{SB}, V_{DD} and AV_{DD} are internally measured by the VLM on channels 7, 8 and 10, respectively. The specification for these supplies is 3.3V ±10%. In order to detect voltage outside both specification limits; i.e., 3V and 3.6V, the supply voltages must be divided. The device includes internal matching precision resistors, as shown in Figure 3, to divide supply voltages by 2 to approximately 1.65V (nominal).

Note: When setting the Channel High and Low limits for channels 7, 8 and 10, bear in mind the divided voltage.

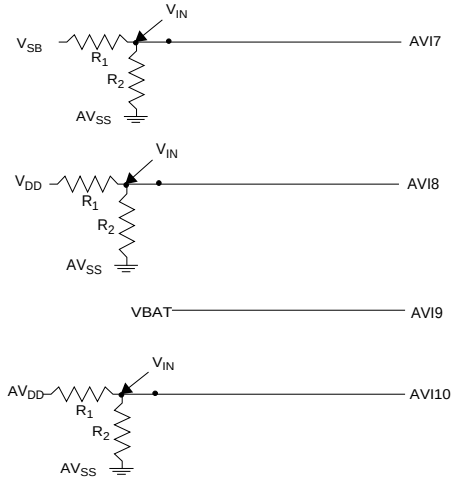

Figure 3. Internal Voltage Measurement

BATTERY VOLTAGE MEASUREMENT

The VLM can monitor internal SuperI/O battery voltage. V_{BAT} is measured using channel 9 of the VLM. A typical battery used in PC systems has a voltage of up to 3.6V. In the PC87365/6, the internal channel for V_{BAT} measurement does not use a resistive network divider before feeding the voltage into the actual VLM circuit (see Figure 3). This prevents a constant drain current and the significant reduction of battery life, while resulting in the negligible side effect of the inability to distinguish between a full and almost full battery. (See MEASUREMENT ACCURACY for other reasons for not dividing down V_{BAT}.) Therefore, the maximum range is 0 to 2.97V ($K*V_{REF}$). A measured voltage from a perfectly good and new battery is FFh. Based on this level, it is recommended to set Channel High Limit for channel 9 to FFh. Only when the voltage starts dropping below 2.97V do measured voltages drop below FFh.

Increased resolution of battery voltage measurement is an essential advantage in better voltage tracking over time. A typical Lithium battery has a voltage-over-time curve as shown in Figure 4 (if loaded with a constant current drain). A system that monitors the voltage-over-time is partially able to predict the remaining lifetime. If measurements can be made with a higher resolution, better slope calculations can be made, as well as improved battery lifetime predictions.

When the battery voltage is at its virgin voltage level, FFh or 2.97V, it cannot be tracked. This inability could be perceived as a disadvantage. However, a battery voltage higher than this is well within the specifications of any battery-backed block within the PC system. Therefore, although tracking cannot be performed, it can be presumed that the battery voltage level is good. When the battery starts dropping below FFh values, the increased resolution enables the system management software to make much better predictions as to the expected lifetime of the battery. When voltage levels of FFh are valid levels, as is the case with the measured V_{BAT} voltage level, it not possible to use the VLM High Limit alarm function. This is not a real system issue, since a voltage higher than 2.97V is no reason for alarm. Because the voltage only declines during a battery's normal lifetime, monitoring is only required for V_{BAT} that falls below a lower limit.

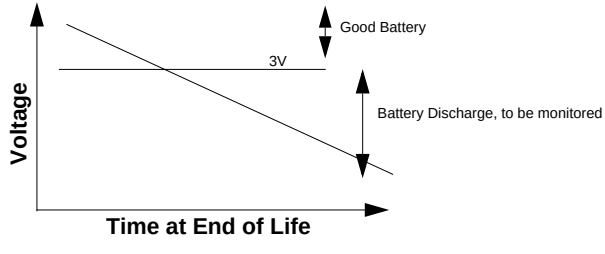

Figure 4. Typical Lithium Voltage vs. Time, Using Constant Current Drain

VLM CONFIGURATION

The VLM must be enabled in order to start measuring and monitoring the system voltages. Before enabling it, select the required channels and configure each one for options such as ALARM generation.

Refer to the PC87365/6 datasheets for details on VLM configuration and channel specific registers.

The VLM Bank Selection (VLMBS) register, located at offset 09 and common to all banks, selects the active bank. Each bank corresponds to one input channel. The default bank selection after system reset is 0.

Designate the reference voltage to be used in the system. Then enable the VLM by writing 1 into bit 0 of the VLM Configuration (VLMCFG) register. The default reference voltage is the external reference voltage generator. To select the internal reference source, write 0 to bit 1 of the VLMCFG register.

Once enabled, the VLM continuously measures the voltages of all the enabled channels periodically, as defined by the conversion rate setting. To guarantee the stability of the signal at the input of the ADC, a delay is added between the end of each conversion and the beginning of the next.

Select the conversion rate and delay suitable for the number of channels selected and the input source resistance of the power supplies through the Voltage Conversion Rate (VCNVR) register located at offset 07h. Refer to the PC87365/6 datasheets for more details on channel delay calculation and conversion rate settings.

Voltage measurements are made on all selected channels. Reading bit 7 of the Voltage Channel Configuration and Status (VCHCFST) register, located at offset 0Ah, for the corresponding channel indicates if the conversion is complete. The RDCHV register at offset 0Bh contains the measurement results.

Refer to the *BIOS Porting Guide for LPC SuperI/O PC8736X*, April 1999, Section 3 for more details on VLM configuration.

USING THE ALARM

The VLM can detect constant drift in power supply due to wear, changes in input conditions or temperature, and power fail conditions. It can also detect power supply overload if the overload period exceeds 10 msec. The VLM cannot detect short noise spikes in the power supply.

To use the ALARM feature, the Channel Voltage High Limit and Low Limit (CHVH and CHVL) registers, at offset 0Ch and 0Dh, must contain the high and low limits set for correct system operation. Bit 4 of the VCHCFST register must also be enabled. If the measured value exceeds user-defined limits, bits 1 and/or 2 of the VCHCFST register is/are set, depending on which limit has been exceeded. The relevant bits of VEVSTS0 and VEVSTS1, at offsets 00h and 01h, are also set to 1 if the high /low limit has been exceeded.

Enabling bits of the Voltage Event to IRQ 0 and 1 registers (VEVIRQ0 and VEVIRQ1), located at offsets 05h and 04h, enables IRQ events for the corresponding channel. Similarly, enabling bits of the Voltage Event to $\overline{\text{SMI}}$ 0 and 1 registers (VEV$\overline{\text{SMI}}$0 and VEV$\overline{\text{SMI}}$1), located at offsets 03h and 02h, enables generation of SMI event.

Before using the ALARM feature, it is advisable to clear all pending flags in the VCHCFST register.

SAMPLE PROGRAM TO MEASURE VOLTAGE

Following is a sample program that enables the VLM to measure input voltage. For the purposes of this example, internal voltage reference is selected, Channel 0 is enabled, and ALARM/$\overline{\text{SMI}}$/IRQ events are enabled, to indicate if the measured value exceeds the user-defined high/low limits.

```
//***********
Select VLM Device from PnP
//***********
wr  2E 07          -- Writes 07h to location 2E. This writes 07h (which is address of
                   -- " LOGICAL DEVICE NUM" register) to INDEX register

wr 2F 0D           -- Writes 0D to location 2F. This writes 0D to Config Data register.
                     -- 0D is logical device number for VLM

wr 2E 60           -- Selects I/O Base address descriptor bits 15-8

wr 2F 09           -- Selects address[15:8] = 09

wr 2E 61           -- Selects I/O Base address descriptor bits 7-0

wr 2F 50           -- Selects address[7:0] = 50

wr 2E 30           -- Selects Device Activate register

wr 2F 01           -- Enables VLM

//***********
Configure VLM Module
//***********
wr 02 01           -- Writes Voltage Event to SMI 0 register, enables SMI routing for channel 0

wr 07 05           -- 07 is Voltage Conversion Rate (VCNVR) register
                    -- VCNVR[2:0] = 5 selects 10 ms conversion period
                    -- VCNVR[5:3] = 0 selects 40 µs sampling delay

wr 09 00           -- Writes 00 to VLM Bank Select register (selects channel 0)

wr 0A 11           -- Writes to Voltage Channel Configuration and Status register
                    -- VCHCFST[4] = 1, enables Alarm
                    -- VCHCFST[0] = 1, enables channel

wr 0C aa           -- Writes to Channel Voltage High Limit register. This sets high limit = aa

wr 0D a0           -- Writes to Channel Voltage Low Limit register. This sets low limit = a0

wr 08 00           -- Writes to VLM Config register
                    -- VLMCFG[1] = 0, selects internal V_REF for measurement
                    -- VLMCFG[0] = 0, deasserts standby operation for VLM
                    -- Samples all enabled channels when VLM comes out of standby


delay              -- Waits for end of conversion

rd 0a              -- Reads Voltage Channel Configuration and Status register
                    -- VCHCFST[7] should be set to 1 to indicate end of conversion
```

RECOMMENDATIONS FOR TOP PERFORMANCE

Power is supplied to the analog parts of the ADC through two, dedicated analog power pins: AV_{DD} and AV_{SS}. This ensures effective isolation of the analog parts from noise caused by the digital parts. The digital parts of the VLM are supplied via V_{SB}. The following recommendations reduce noise and improve accuracy of the voltage measurements.

- Connect the supply and ground of the input attenuator (see Figure 2) to the AV_{SS} or AV_{DD} pin for the highest accuracy.
- A separate, low-impedance ground plane for analog ground (see Figure 5), which provides a ground point for the voltage dividers and analog components, enhances performance but is not mandatory.
- Place analog components, such as voltage dividers, as close as possible physically to the PC87365/6 inputs.
- Provide analog supply AV_{DD} through an external RC or an LC filter.
- Position the power supply bypass, the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors as close as possible physically to the AV_{DD} and AV_{SS} pins of the PC87365/6.
- Place a low-leakage, non-polarized, 0.47 µF capacitor as close as possible physically to the V_{REF} pin.
- Shield analog input traces from noisy digital signals on the board.
- Connect any unused analog input pins to AV_{SS} on the board.

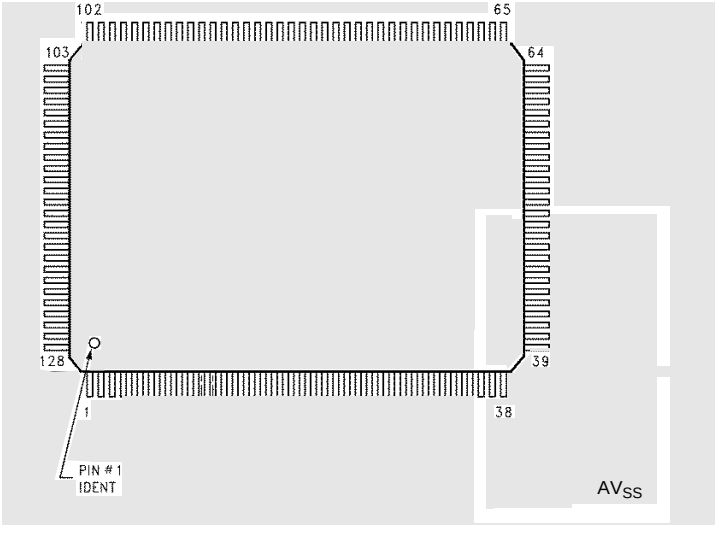

Figure 5. AV_{SS} Plane Layout Example

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