Functional Description and Specifications of the PCM16C02 PC Card Interface Device in Rev 3 DMA Mode

National Semiconductor
Application Note 998
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- DMA INTERFACE PIN DESCRIPTION AND BLOCK DIAGRAM
- ATTRIBUTE MEMORY MAP
- HOST-SIDE DMA REGISTER (0x3FA)
- FUNCTION CONFIGURATION OPTION REGISTER 1 (0x1040)
- DMA READ TIMING DIAGRAM AND SPECIFICATIONS
- DMA WRITE TIMING DIAGRAM AND SPECIFICATIONS

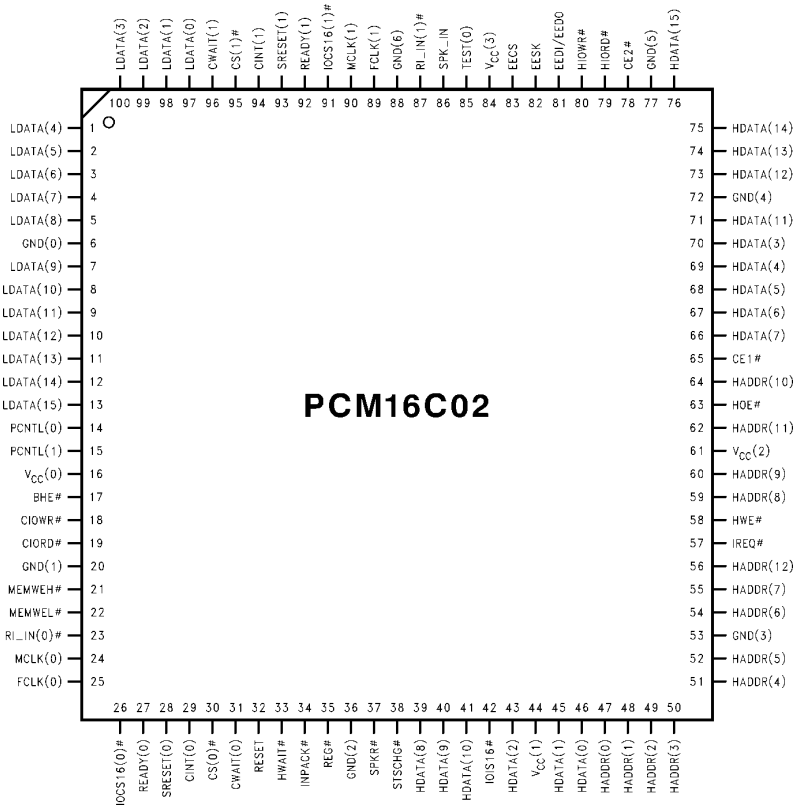
OVERVIEW

This note provides the functional description and details of register settings necessary to configure Function 1 of the PCM16C02 to support the DMA extension to the PC Card Standard, February 1995 (i.e, Rev 3 DMA Mode). Also, included in this note are performance specifications necessary for DMA designs. Note, the implementation of a specific PC Card design using DMA is outside of the scope of this note.

1.0 DMA INTERFACE PIN DESCRIPTION

During DMA Mode, nine device pins for Function 1 are configured to support the PC Card Standard DMA interface. Two of the nine device pins support the TC__IN pin of the PC Card Standard DMA interface. The HOE# pin is configured as TC__IN during DMA Writes, and the HWE# pin is configured as TC__IN during DMA Reads.

Refer to the Connection Diagram in *Figure 1-1* and the Block Diagram in *Figure 1-2* while reviewing the DMA Mode Pins described in Table 1-1.



TL/F/12118–1

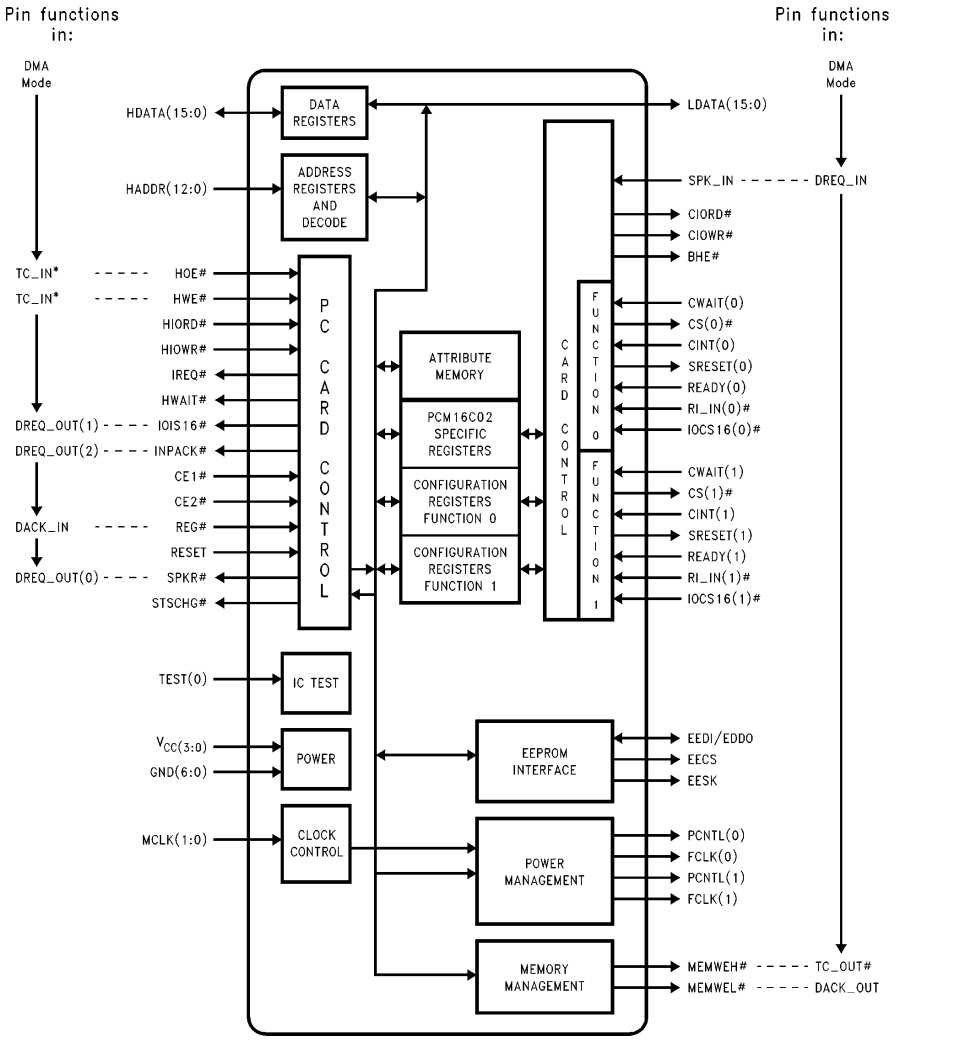
Order Number PCM16C02VJG
See NS Package Number VJG100A

FIGURE 1-1. Connection Diagram

RRD-B30M105/Printed in U. S. A.

TABLE 1-1. DMA Mode Pins

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
TC__IN	I	58, 63	TTL	>100k to V_{CC}	Terminal Count Output from the Host
TC__OUT#	O Tri	21	CMOS 6 mA	>10k to V_{CC}	Terminal Count Output to Function
DACK__IN	I	35	TTL	>100k to V_{CC}	DMA Acknowledge from the Host
DACK__OUT	O Tri	22	CMOS 6 mA	>10k to V_{CC}	DMA Acknowledge Output to Function
DREQ__IN	I	86	TTL Schmitt		DMA Request Input from Function
DREQ__OUT (0)	O	37	CMOS 6 mA		DMA Request Output to Host
DREQ__OUT (1)	O	42	CMOS 6 mA		DMA Request Output to Host
DREQ__OUT (2)	O	34	CMOS 6 mA		DMA Request Output to Host



TL/F/12118–2

Note: TC__IN is HOE# for DMA Writes and HWE# for DMA Reads.

FIGURE 1-2. Block Diagram

2.0 ATTRIBUTE MEMORY MAP

The Attribute Memory Map remains the same except for the Reserved for Future Use Register at location (0x3FA) is defined as the Host-Side DMA Register. See Attribute Memory Map in Table 2-1.

TABLE 2-1. Attribute Memory Map

Register Description	Register Type	Address (Hex)	EEPROM
Card Information Structure	PC Card CIS	0x000−0x03E2	Yes
Pin Polarity Register	PCM16C02 Specific	0x03E4	Yes
PMGR and Clock Register	PCM16C02 Specific	0x03E6	Yes
CTERM0 Register	PCM16C02 Specific	0x03E8	Yes
CTERM1 Register	PCM16C02 Specific	0x03EA	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03EC−0x03EE	Yes
Miscellaneous Register	PCM16C02 Specific	0x03F0	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03F2−0x03F4	Yes
Wait State Timer Registers	PCM16C02 Specific	0x03F6	Yes
NAND Flash (NM29N16) Config Register	PCM16C02 Specific	0x03F8	Yes
Host-Side DMA Register	PCM16C02 Specific	0x03FA	Yes
Watchdog Timer Register	PCM16C02 Specific	0x03FC	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03FE	Yes
Card Information Structure	PC Card CIS	0x0400−0x07FE	Optional
ID Register	PCM16C02 Specific	0x1000	No
EEPROM Control Register	PCM16C02 Specific	0x1002	No
EEPROM Security Register	PCM16C02 Specific	0x1004	No
Reserved for Future Use Registers	PCM16C02 Specific	0x1006−0x101E	No
Function 0 Configuration Option Register	PC Card	0x1020	No
Function 0 Configuration Status Register	PC Card	0x1022	No
Function 0 Pin Replacement Register	PC Card	0x1024	No
Unused	PC Card	0x1026	No
Function 0 I/O Event Register	PC Card	0x1028	No
Function 0 Base A Register	PC Card Extension	0x102A	No
Function 0 Base B Register	PC Card Extension	0x102C	No
Unused	PC Card Extension	0x102E−0x1030	No
Function 0 Limit Register	PC Card Extension	0x1032	No
Reserved for Future Use Registers	PC Card Extension	0x1034−0x103E	No
Function 1 Configuration Option Register	PC Card	0x1040	No
Function 1 Configuration Status Register	PC Card	0x1042	No
Function 1 Pin Replacement Register	PC Card	0x1044	No
Unused	PC Card	0x1046	No
Function 1 I/O Event Register	PC Card	0x1048	No

3.0 HOST-SIDE DMA REGISTER (0x3FA)

If enabled for DMA mode, the PCM16C02 will properly meet all of the PC Card Standard requirements for DMA operation including the generation of DACK and TC signals to the card function, and the passing of DREQ from the function to the host.

D7–D6	D5	D4	D3	D2	D1	D0
RFU	Dreq__sel(1)	Dreq__sel(0)	TC__ppol	Dack__ppol	Dreq__ppol	RFU

Dreq__sel—Selects which host-side output will become Dreq__out when configured for DMA mode.

If: Dreq__sel(1)	Dreq__sel(0)	Dreq__out is:
0	0	Spkr
0	1	IOIS16
1	0	Inpack
1	1	Reserved

TC__ppol—Sets the polarity for the TC output in DMA mode. If set to zero (0), TC will go low when HOE# or HWE# are asserted (low) with REG# de-asserted (high). If set to one (1), TC will go high when HOE# or HWE# are asserted (low) with REG# de-asserted (high). Default value for TC__ppol is zero.

Dack__ppol—Sets the polarity for the DACK output in DMA mode. If set to zero (0), DACK will go low when HIORD# or HIOWR# are asserted (low) with REG# de-asserted (high). If set to one (1), DACK will go high when HIORD# or HIOWR# are asserted (low) with REG# de-asserted (high). Default value for Dack__ppol is zero.

Dreq__ppol—sets the polarity for the DREQ__OUT output in DMA mode. If set to zero (0), DREQ__OUT will go low when DREQ__IN is taken (low). If set to one (1), DREQ__OUT will go high when DREQ__IN is taken (low). Default value for Dreq__ppol is zero.

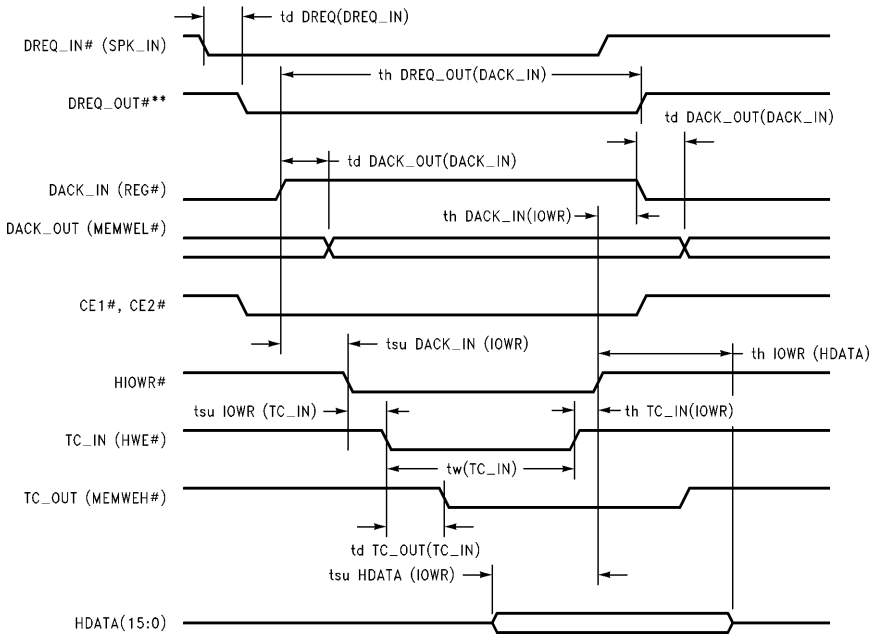
4.0 FUNCTION CONFIGURATION OPTION REGISTER 1 (0x1040)

D7	D6	D5–D0
SREST	LevIREQ	Function Configuration Index

DMA__EN(D4) (For Function 1 ONLY)—If set to a one (1), function 1 is configured for DMA mode. If set to zero (0), function 1 is configured for normal I/O mode (default state).

Thus Function 1 can be configured as either a standard I/O or DMA interface, however Function 0 cannot be configured as a DMA interface. Note, Function 0 can be configured as either a standard I/O or NAND Flash (NM29N16) interface.

5.0 DMA READ TIMING DIAGRAM AND SPECIFICATIONS



TL/F/12118–3

**SPKR, IOIS16 or INPACK may be selected to function as DREQ__OUT.

FIGURE 5-1. DMA Read Timing (I/O Write)

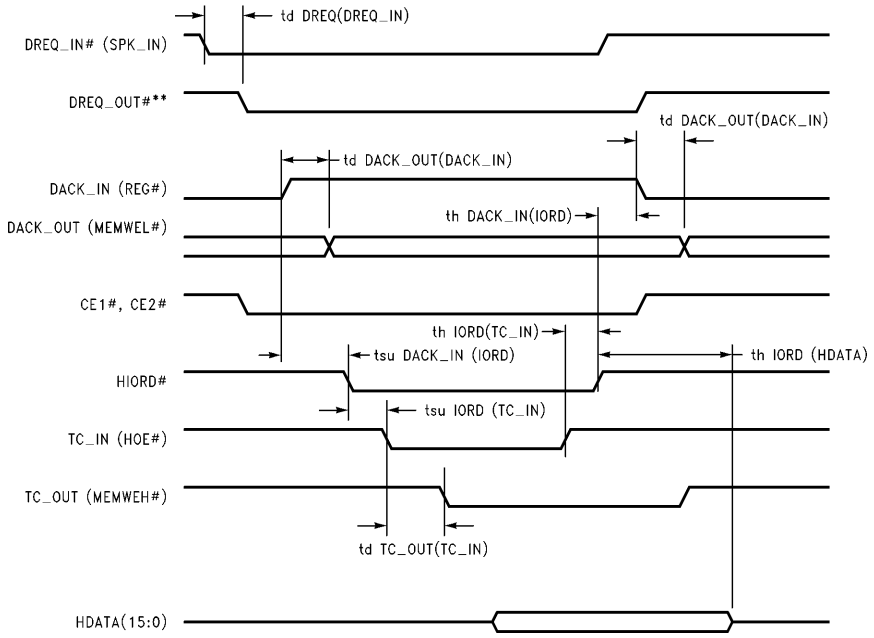
DMA Read Timing (I/O Write) Specification (See *Figure 5-1*)

Symbol	Path	V_{CC} (V)	Commercial $T_A = 0°C$ to $+70°C$		Units
			Min	Max	
td DREQ(DREQ__IN)	DREQ__OUT* Delay from DREQ__IN	4.75		15	ns
		3.0		20	
td DACK__OUT(DACK__IN)	DACK__OUT Delay from DACK__IN(REG)	4.75		18	ns
		3.0		22	
tsu DACK__IN(IOWR)	DACK__IN(REG) Setup to HIOWR Falling	4.75	5		ns
		3.0	5		
tsu IOWR(TC__IN)	HIOWR Setup to TC__IN(HWE) Falling	4.75	10		ns
		3.0	10		
td TC__OUT(TC__IN)	TC__OUT Delay from TC__IN(HWE)	4.75		15	ns
		3.0		20	
tsu HDATA(IOWR)	HDATA Setup to HIOWR Rising	4.75	100		ns
		3.0	100		
th IOWR(HDATA)	HDATA Hold from HIOWR Rising	4.75	30		ns
		3.0	30		
th TC__IN(IOWR)	HIOWR Hold from TC__IN Rising	4.75	10		ns
		3.0	10		
tw (TC__IN)	TC__IN Pulse Width	4.75	40		ns
		3.0	40		
th DREQ__OUT(DACK__IN)	DREQ__OUT Hold from DACK__IN Rising	4.75	0		ns
		3.0	0		
th DACK__IN(IOWR)	DACK__IN Hold from HIOWR Rising	4.75	5		ns
		3.0	5		

*SPKR, IOIS16 or INPACK may be selected to function as DREQ__OUT.

**Parameter guaranteed by design.

6.0 DMA WRITE TIMING DIAGRAM AND SPECIFICATIONS



TL/F/12118–4

**SPKR, IOIS16 or INPACK may be selected to function as DREQ__OUT.

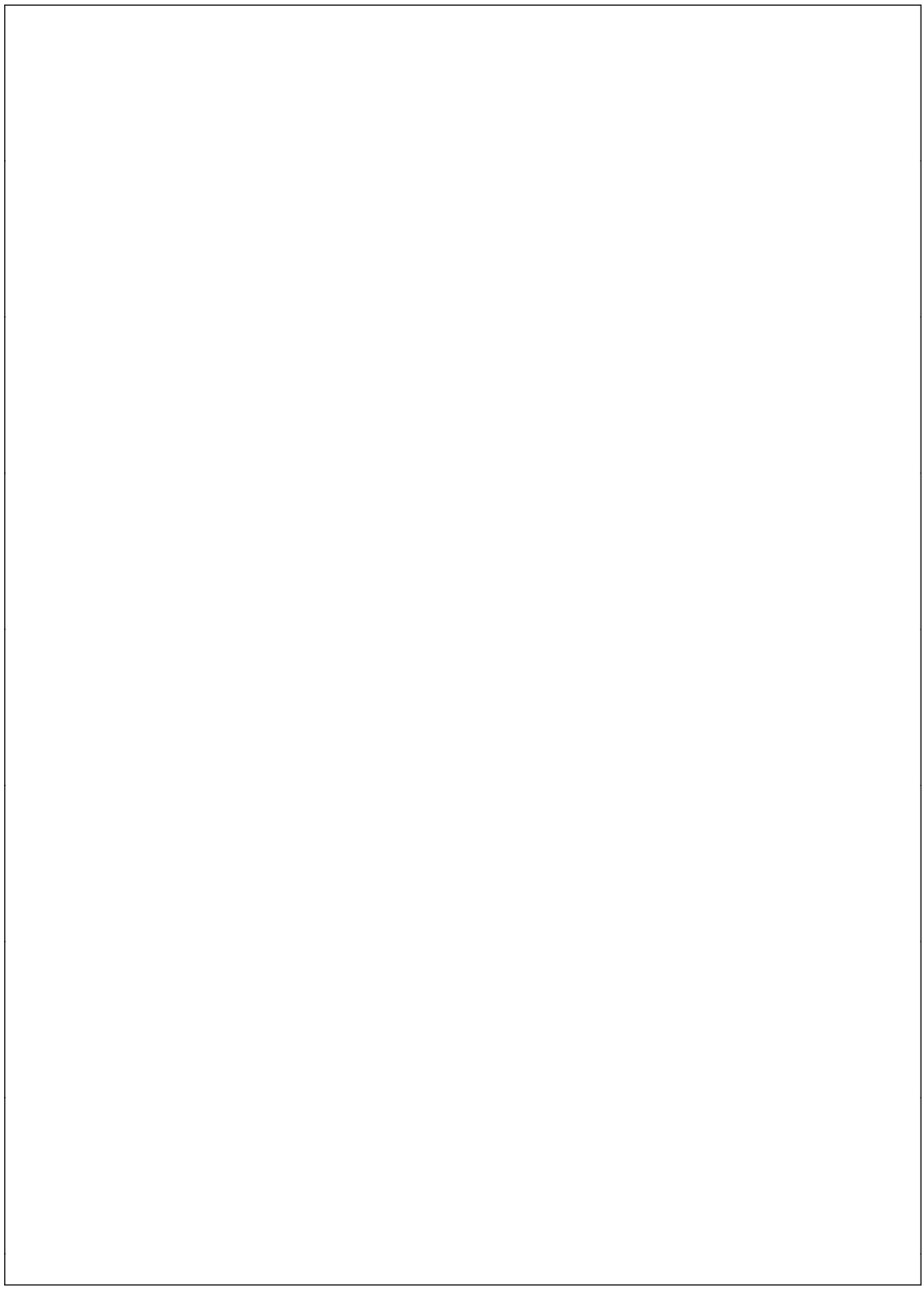
FIGURE 6-1. DMA Write Timing (I/O Read)

DMA Write Timing (I/O Read) Specification (See *Figure 6-1*)

Symbol	Path	V_{CC} (V)	Commercial $T_A = 0°C$ to $+70°C$		Units
			Min	Max	
td DREQ(DREQ__IN)	DREQ__OUT* Delay from DREQ__IN	4.75		15	ns
		3.0		20	
td DACK__OUT(DACK__IN)	DACK Delay from DACK__IN(REG)	4.75		18	ns
		3.0		22	
tsu DACK__IN(IORD)	DACK__IN(REG) Setup to HIORD Falling	4.75	5		ns
		3.0	5		
tsu IORD(TC__IN)	HIORD Setup to TC__IN(HOE) Falling	4.75	10		ns
		3.0	10		
td TC__OUT(TC__IN)	TC__OUT Delay from TC__IN(HOE)	4.75		15	ns
		3.0		20	
th IORD(HDATA)	HDATA Hold to HIORD Rising	4.75	0		ns
		3.0	0		
th DACK__IN(IORD)	DACK__IN Hold from HIORD Rising	4.75	5		ns
		3.0	5		
th IORD(TC__IN)	HIORD Hold from TC__IN Rising	4.75	10		ns
		3.0	10		

*SPKR, IOIS16 or INPACK may be selected to function as DREQ__OUT.

**Parameter guaranteed by design.



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