CGS410 Programmable Video Pixel Clock Generator

National Semiconductor
Application Note 923
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March 1994

INTRODUCTION

As system clock frequencies reach 100 MHz and beyond, maintaining control over clock timing becomes very important and difficult. Besides microprocessors, other video circuits such as RAMDAC, Video graphics processors, etc., require precise clock timing. Furthermore, system requirements dictate that clock distribution to synchronous system components have minimal skew (the time difference between signals that are intended to switch simultaneously).

There are four major types of low skew clock drivers available. These are gate, divider, PLL (Phase Lock Loop), and programmable delay.

The gate drivers *(*see *Figure 1*) are simple drivers with single-ended or differential inputs and outputs. These distribute clock signal to several different loads. The disadvantage of these simple drivers is that they transmit jitter and duty cycle distortions. The skew between the drivers may be of the order of 100 ps.

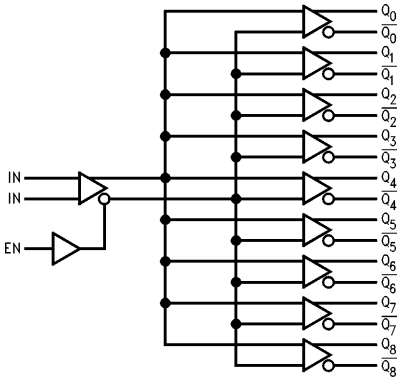

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FIGURE 1. Gate Type Driver

The divider type of drivers use flip flops (as frequency dividers) for providing outputs the frequency (or lower with other structures) of the input. The advantages of this technique are: the duty cycle distortion is minimum (outputs provide 50% duty cycle) and they provide both complementary and true outputs (see *Figure 2*). The disadvantage is that duty cycle can not be adjusted in a system.

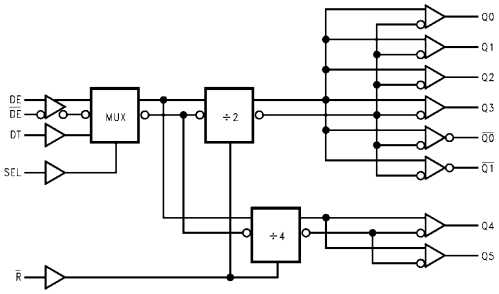

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FIGURE 2. Divider Type Driver

The programmable clock drivers (see *Figure 3*) are in reality a variation of the other drivers. In here, the delay between different outputs is programmable.

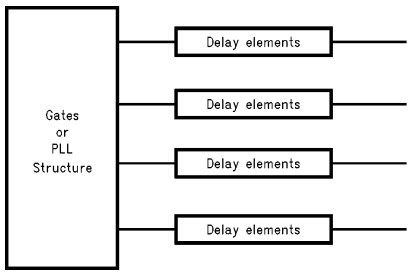

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FIGURE 3. Programmable Delays

The PLL type of driver contains a multiplexer at the front end which will accept more than one frequency input. A phase or frequency detector compares the phase of this multiplexer output signal to a feedback signal. Depending on whether the detected phase is leading or lagging, the phase/frequency detector output causes the charge pump to decrease or increase the frequency of the voltage-controlled oscillator (VCO). The output of the VCO is then connected through Multiplexers to a divider clock driver to provide many output frequencies and phases (see *Figure 4*). The CGS410 belongs to this category.

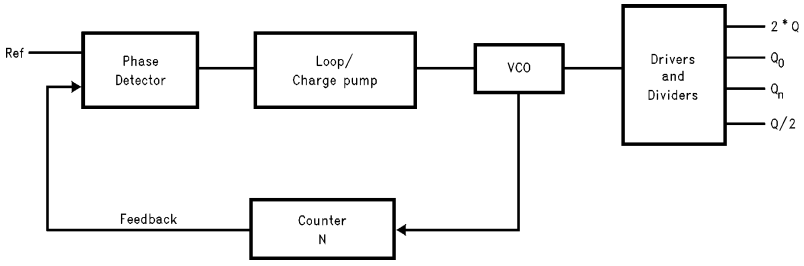

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FIGURE 4. PLL-Based Clock Driver

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Some of the features of the PLL type of clock drivers are:

1. Ability to lock on to any frequency that is lower than the desired output frequency. This allows for frequency multiplication.
2. Reduction of the input clock jitter.
3. Ability to include other driver types in the closed loop.

In all these approaches, the output skew is determined by the circuit design, physical layout, and process variation. These variations are predictable and can be controlled by specifying the MIN and MAX limits of the delay. In some applications, it is required to offset one output from another by a certain amount of delay. This can be accomplished by introducing specific delays in the output paths. These delays are programmable.

The CGS410 utilizes the PLL and it can be directly programmed by software to generate any desired frequency. Other features include:

1. Output frequencies to 135 KHz
2. Internal VCO running at 80 MHz to 135 MHz
3. On-chip loop filters
4. External filter support
5. CMOS output clocks
6. Configurable high-speed complementary clock outputs
7. Glitch-free transitions for clock changes
8. Single supply operation

The CGS410 is a CMOS programmable clock generator device capable of generating synthesized output clock with frequency of up to 135 MHz. The device achieves programmability by serially clocking data into an internal shift register. Upon receiving the last bit of information, the data is automatically transferred and mapped into the internal divider circuits.

At the heart of the CGS410 is an internal modulated ring oscillator which comprises the VCO. This VCO is different from external VCO implementations because, instead of using an L-C tank ratio to characterize the resonant frequency; an internal time delay through the ring is modulated in direct response to a voltage present on the FREQCTL input. The FREQCTL voltage is the response of the low pass filter driven by the charge pump.

The inherent advantage of running a ''ring-oscillator'' is its ability to create wide frequency variations as dictated by the gain of the VCO. This is in contrast to the L-C VCO implementations, where the tuning range is much narrower and the VCO gain (generally) much lower.

In order to reduce the internal die noise coupling, specific functions are powered from separate external source and ground return points. These paired pins are: BV_{DD}/BGND, DV_{DD}/DGND, XV_{CC}/XGND, and AV_{DD}/AGND. All pins can be grouped together with little increase in phase noise, with the exception of AV_{DD}/AGND.

What drives the ring-VCO approach is determined by the amount of jitter (instability) present on the VCO output. The jitter can be understood as minute frequency variations present on the VCO output in comparison to an ideal VCO. The jitter is a measure of how much the output clock period varies over time. The CGS410 has extremely low jitter. The low frequency (cycle-to-cycle) jitter is 2 ns to 3 ns. The high frequency jitter (over 1000 samples) is 300 ps to 500 ps.

CGS410 IN MULTIMEDIA APPLICATION

The *Figure 5* shows the block diagram of a typical video system. The NTSC color signal is converted into digital signal by a video A-to-D converter. The Field storage (memory) contains information on field bits (such as: starting address of the field and the size of the field) which are software configurable. The 3-way frame buffer shown in this example is sophisticated enough so that it can interface with the CPU, graphics processor and CRT processor. The output of the frame buffer is multiplexed with the output of the field store registers and fed to the RAMDAC. The CGS410 is used here to generate the load clock for the frame buffer and the Pixel clock for the RAMDAC. The Load clock for the frame buffer is generated by the CMOS compatible output on the CGS410 and it is programmable in order to produce the lower output frequencies synchronous to the Pixel clock. The Pixel clock for the RAMDAC can be derived either from the high frequency differential outputs PCLK and PCLKB on the CGS410 for higher pixel rates (as shown in *Figure 5*) or from the single ended, CMOS compatible PCLK output for average pixel rate. Proper termination should be used when using the differential clocks.

Image Capture and Display

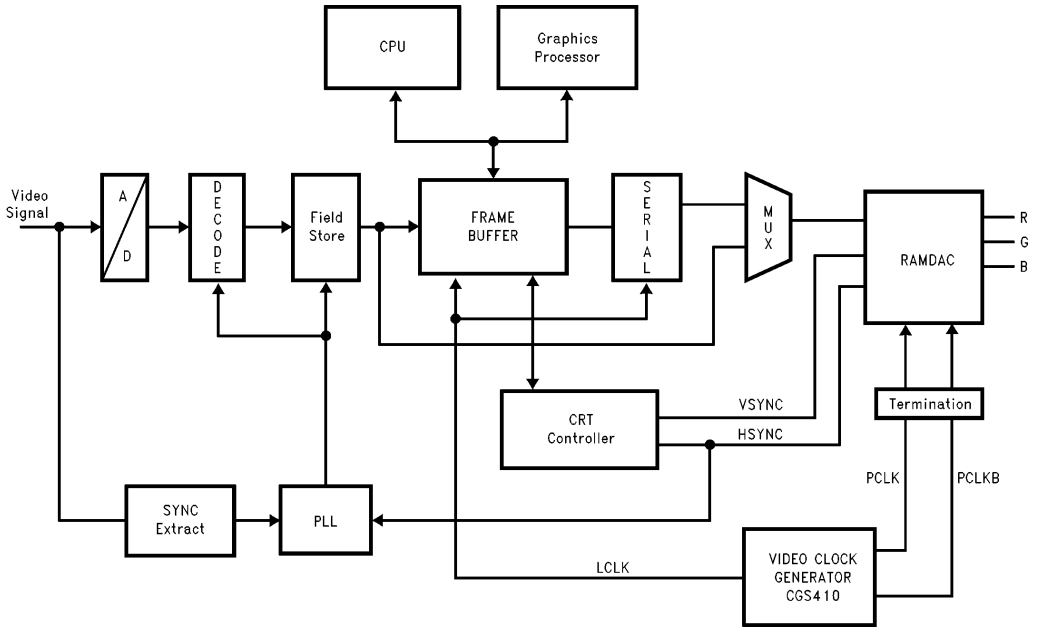

FIGURE 5

GRAPHICS ACCELERATOR BOARD FOR AT

The CGS410 Pixel Clock Generator can also be used in the Graphics Accelerator board for a PC AT. *Figure 6* shows the graphics frame buffer as an array in the CPU memory map. With 4 bits per pixel in this example, the images can be drawn at rates of up to 64 bits (16 pixels) per memory access cycle. The 4-plane memory is dual-ported to allow memory access to both the CPU and the graphics processor.

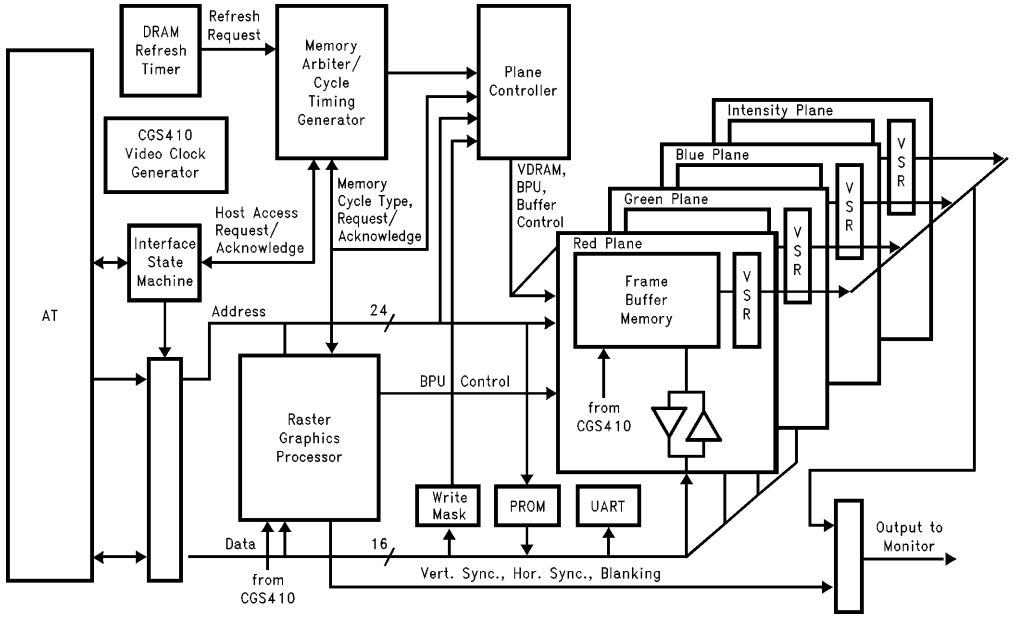

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FIGURE 6

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