DP83905EB-AT AT/LANTIC™ Evaluation Board

National Semiconductor
Application Note 875
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1.0 OVERVIEW

The DP83905EB-AT AT/LANTIC Demonstration board provides system designers with complete 16-bit 10BASE-T, 10BASE2 and 10BASE5 Ethernet Solutions in a half-size, jumperless, ISA adapter card. The board uses only four ICs and can be configured as either a shared memory or an I/O port adapter card. All of the bus interface logic is implemented in the DP83905, AT Local Area Network Twisted Pair Interface Controller (AT/LANTIC). The AT/LANTIC uses an E^2PROM to store the board's IEEE node address and it's own configuration information. It uses two 8k x 8 SRAMs for buffering packets to and from the network.

The DP83905 has a built in Manchester Encoder/Decoder and Twisted Pair Transceiver. This allows the AT/LANTIC to transmit and receive packets on a 10BASE-T network with the addition of only a filter and some discrete components. An AUI interface on the AT/LANTIC can also be used to run a 10BASE5 or 10BASE2 network with the addition of two 1:1 pulse transformers, a DC-DC Converter and the DP8392 Coaxial Transceiver Interface (CTI). Refer to the schematic at the end of this Application Note.

2.0 ARCHITECTURAL FEATURES

- Designed with the DP8390 Network Interface Controller, NIC
- Complete Ethernet solution with only 4 ICs
- Board options are configurable in software
- Half-size PC-AT® adapter card
- 2 Modes for ISA interface—Shared Memory or I/O Port (NE2000*plus*™ compatible)
- 10BASE-T, 10BASE2 or 10BASE5 connectivity
- Serial EEPROM stores IEEE address and AT/LANTIC configuration while using less power than a typical bipolar PROM
- Surface mount technology on most parts
- Boot PROM socket to allow diskless boot from NetWare™, LANManager and other network operating systems
- Able to select one of eight interrupts

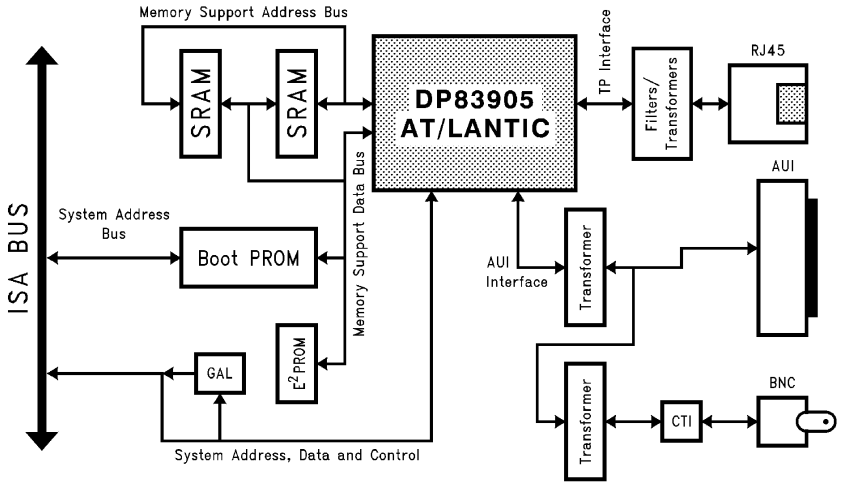

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FIGURE 1. DP83905EB-AT Block Diagram

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3.0 BOARD DESIGN AND LAYOUT

Figure 2 shows the part placement and power plane layout for the DP83905EB-AT Demonstration Board. The design is straight forward because all of the bus interface logic, including the 24 mA ISA bus drivers, is internal to the AT/LANTIC. The Twisted Pair interface is simple as the TPI transceiver is also internal to the AT/LANTIC. Thin Ethernet (10BASE2) is acheived with the addition of a DP8392CV CTI device and a DC-DC converter.

3.1 ISA Bus Interface

All of the ISA Bus interconnects of the AT/LANTIC can be directly routed to the ISA Bus connector. Changing the physical placement of the AT/LANTIC may make these traces easier to route, but in order to keep the Twisted Pair Interface traces as short as possible, the AT/LANTIC should be placed as close as possible to the card's metal bracket. This makes the routing of the ISA Bus traces longer and hence noisier. To filter low frequency noise (kHz range) on the bus a 22 μF decoupling capacitor was placed near the bus connector between power and ground.

The Boot PROM address lines also come directly from the ISA Bus connector. The reason for this is that the AT/LANTIC's Memory Support Address Bus does not buffer address bit A0 which is needed by the boot PROM (the AT/LANTIC only does word aligned transfers when in 16-bit mode). Boot PROM addresses must come directly off the ISA Bus where byte or word aligned transfers may be used by software. The physical location of the PROM is not critical.

3.2 Memory Support Bus Interface

The Memory Support Interface is that part of the design which is used by the AT/LANTIC's Local DMA and Auto-Configuration. This includes the SRAMs and the E^{2}PROM. *Figure 1* shows how both SRAMs and the E^{2}PROM are connected to the Memory Support Bus of the AT/LANTIC. The AT/LANTIC uses the SRAM (8k x 16) for buffering transmit and receive packets and it uses the E^{2}PROM to store the IEEE Node Address, a checksum, a board type, Configuration Registers A, B and C and codes which determine the data width in which the board is to run. Primarily the E^{2}PROM is used on start up; once the AT/LANTIC reads the configuration data and the IEEE node address out of the E^{2}PROM, this information is stored in the AT/LANTIC and made accessible by software.

In order to change the boot configuration of the board, the current configuration is changed in software and the AT/LANTIC downloads the new configuration to the E^{2}PROM. The new configuration will be stored so that when the board is powered up again, the new configuration will be loaded. (See Section 4.0—older designs required hardware jumpers to do this). The E^{2}PROM that the AT/LANTIC uses (NM93C06) is a serial device. The AT/LANTIC uses its MSD0–2 pins for Serial Data Out, Serial Data In and Clock to the E^{2}PROM when reading or writing it.

The two RAMs provide 16 kbytes of memory for the AT/LANTIC to use for buffering received packets and for the system to use for buffering transmit packets. In Shared RAM mode the RAM logically resides in system memory, but it must still be connected to the AT/LANTIC's Memory Support Bus. The AT/LANTIC buffers the data and address from the ISA Bus, decodes the address and drives chip select and the read or write strobe to the RAM. Note that the board was designed to accommodate either DIP or SOP SRAMs.

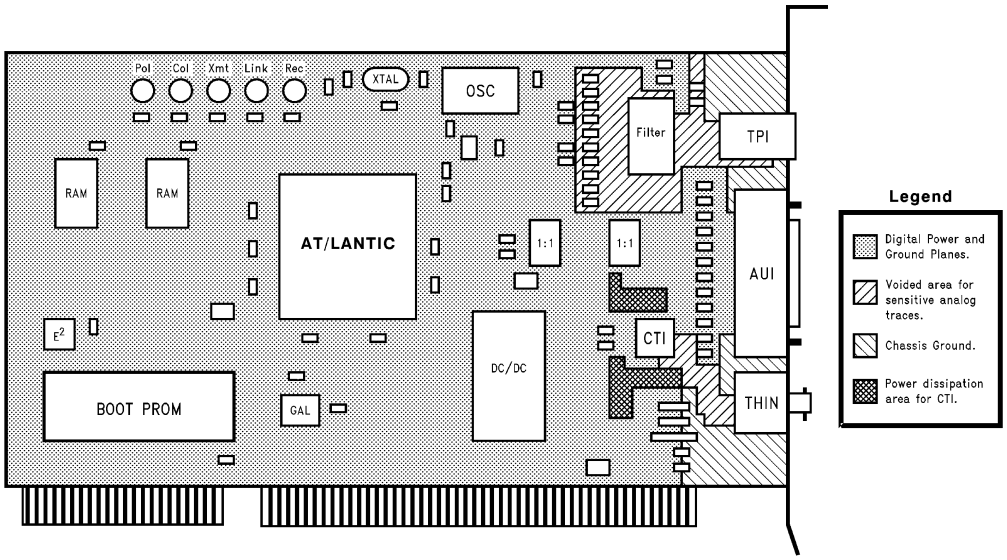

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FIGURE 2. DP83905EB-AT Board Layout and Component Placement

3.3 AT/LANTIC

Some design and layout considerations were made with respect to the DP83905. These are described in the following three sections.

3.3.1 Crystal and Oscillator Design

The AT/LANTIC has been designed to operate with either a crystal or an oscillator module. The DP83905EB-AT comes assembled with the crystal option. If an oscillator module is used, the crystal and the load capacitors C1 and C2 must be removed from the board. If the capacitors are not removed, they will create excessive loading on the clock which may stop the card from working. When mounting an oscillator, it should be raised slightly off the board so that it is not touching the metal pads for the capacitors C1 and C2 (some oscillator modules have built-in insulating raisers).

There are two layout considerations with respect to the clock. First, the traces for the clock should be short and the crystal or oscillator should be placed close to the AT/LANTIC (see *Figure 2*). Second, if a standard size crystal is being used and it must lie flat on the PC board, the power planes should be voided in that area. Note that on the DP83905EB-AT a low-profile crystal is being used that is not laying down. In this situation, it is not critical that the power planes be removed

3.3.2 Decoupling for the AT/LANTIC

The AT/LANTIC, like any other VLSI device, is composed of multiple functional/logic blocks. In some cases, these blocks run off of separate power rails internal to the part. Some of these blocks (such as the Twisted Pair Transceiver) can be quite susceptible to noise. Not only can the input signals couple noise from the board and environment, but output signals can transmit noise to the environment. Also, since the separate power pins are all connected to the same 5V supply in the PC, other noisy power signals can affect power supplies that need to be kept noise free. By separately decoupling the supply pins to the AT/LANTIC, the internal supplies are reasonably isolated from each other. Instead of placing decoupling capacitors near the AT/LANTIC, place the decoupling capacitors directly to the power pins. Each of the seven blocks within the AT/LANTIC should be decoupled by at least one 0.01 μF capacitor. Thus, each of the power rails in the chip has independant decoupling. This minimizes EMI and reduces power supply noise.

Another area of concern is the AT/LANTIC's ISA bus interface. This section is driving the ISA bus with 24 mA bus drivers. Not only is the current high, but the rise and fall times of the bus signals are fast. By decoupling the ISA interface supply, noise produced by these drivers is reduced.

Decoupling of noise from the PC bus is acheived using 0.01 μF and 22 μF capacitors (used to filter out lower frequency noise in the order of a few kHz). One 22 μF is placed near the media end of the board and the other near the ISA bus connector.

3.3.3 PLL Power Supply Noise

The VCO (Voltage Controlled Oscillator) block of the receive PLL (Phase-Lock Loop) within the AT/LANTIC is sensitive to noise in the frequency range of 10 kHz to 400 kHz. As little as 100 mV of noise in this range can cause the PLL to lose lock on an incoming packet. In order to improve the performance of the PLL, a single pole filter should be used on the PLL power supply pin. This is shown below in *Figure 3*.

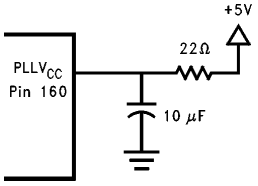

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FIGURE 3. PLL V_{CC} Noise Filter

3.4 Twisted Pair Interface (TPI)

This section refers to the layout diagram in *Figure 2,* of this Application Note.

The Twisted Pair Interface of the DP83905EB-AT is simple: the only components needed external to the AT/LANTIC are the pre-emphasis resistors, some capacitors, a transformer/filter module and, of course, the RJ45 modular connector. Resistors R19–22 (refer to the schematic at the end of this application note) provide the preemphasis for the TXO± output as described in the AT/LANTIC datasheet. R23 damps the TXO± output undershoot. Resistors R24 and R25 terminate the receive Twisted Pair line. C9, C43–C45 filter out the common mode noise in the transformer/filter. C46 and C47 filter out the high frequency noise harmonics on the TXO± output. All these components together with the transformer/filter module should be placed as close to the AT/LANTIC's twisted pair interface pins as possible. The traces should be kept straight and should not run near any other traces. The traces on the cable side of the transformer/filter module to the RJ45 connector should be kept short and straight too. Additionally, make sure that all differential traces are tracked in parallel so they are equilength and will pick up the same amount of common mode noise.

The entire area under all of these signals should be voided of signal traces and power planes, as these could couple noise into the Tx/Rx signals. This is shown in *Figure 2.* This part of the circuit is very critical and will affect FCC test results directly. Precaution should be taken during layout to ensure that noise is reduced as much as possible.

3.5 Attachment Unit Interface (AUI)

The DP83905EB-AT can be used with an external Medium Attachment Unit (MAU) so that connectivity to 10BASE5 or another medium can be acheived. This interface is via the 15-pin D-type connector and is a direct interface to the AT/LANTIC's ENDEC. The AT/LANTIC's ENDEC requires two 270Ω pull-down resistors on the transmit outputs and 78Ω terminations on the receive and collision inputs. Also, the RX, TX and CD lines must be AC coupled using a standard 1:1 pulse transformer. This is the only design requirement for the AUI interface: it is needed to isolate the AT/LANTIC from DC fault conditions. Although these differential signals are not as noise sensitive as the Twisted Pair inputs, care should still be taken when laying out this section of the board. It is not necessary to void the power planes under them.

3.6 Coaxial Transceiver Interface (CTI)

This section refers to the layout diagram in *Figure 2* of this application note.

The Coax Transceiver Interface (DP8392CV) should be placed very close to the BNC connector. This will allow the TXO/RXI trace to be short and straight. The area under this trace should be voided of all other signals and power planes (as shown in *Figure 2*) in order to meet the IEEE 802.3 input capacitance requirement. The BNC connector on the demonstration board is a standard part, however, ''quiet'' connectors are readily available to reduce noise for performance and FCC qualification. The CTI requires an area of copper on the top of the board for heat dissipation. This is also shown in *Figure 2* and is documented in the DP8392CV datasheet. The ground shield of the BNC connector (and of the coax cable) is resistively and capacitively decoupled to chassis ground. There is a chassis ground strip on each layer of the board running from the top to the bottom of the PC board. This is connected to the chassis of the PC through the 15-pin AUI connector's body metal. Chassis ground is then capacitively decoupled to digital ground. The chassis ground trace along the front of the board forms a ''shield'' so that noise is not emitted into or received from the environment.

In order to provide a jumperless solution, a 1:1 transformer is required between the CTI and the 15-pin AUI connector. This provides 500V isolation between the CTI and the DTE ground as required by the IEEE 802.3 specification.

3.6.1 DC-DC Converter Solution

The DP83905EB-AT has been designed to use a standard DC-DC converter which operates from a 12V supply and meets the specifications of the DP8392CV. When the AT/LANTIC is programmed for Thin Ethernet, the THIN output is driven high to turn on the DC-DC converter. For Thick Ethernet and Twisted Pair (10BASE5/T) the AT/LANTIC drives the THIN output low, turning off the DC-DC converter.

Table I shows the possible settings for bits PHYS1 and PHYS0, the Physical Layer Interface selection bits in Configuration Register B. When programmed as [0 1] the THIN output of the AT/LANTIC will go high which will turn on the DC-DC converter. When programmed to any other combination the THIN output will go low, turning the DC-DC converter off.

TABLE I. Physical Medium Selection

PHYS1–0	Media
0 0	10BASE-T
0 1	10BASE2
1 0	AUI (10BASE5)
1 1	TPI (RSL)

3.7 Interrupt Scheme

The DP83905EB-AT will support the selection of one of eight host interrupts. (Encoded mode.)

To program the AT/LANTIC to use the encoded mode interrupt scheme, set the INTMODE bit in Configuration Register C HIGH (logic 1)—see Section 4.3 for details. INT3 is the active interrupt output and INT0, 1, 2 are programmable outputs containing the values in bits 3–5 of configuration register A.

The DP83905EB-AT connects the AT/LANTIC's INT0–3 pins to the inputs of a 16V8 GAL. The GAL maps the INT0–2 inputs to the host's interrupts, as shown in *Figure 4* and Table II. This interrupt scheme is Novell NE2000*plus* compatible. The INT3 pin from the AT/LANTIC strobes true when an interrupt is generated by the AT/LANTIC's internal circuitry. The selected interrupt is output on the GAL (strobes LOW) for the duration of the INT3 strobe.

This means that the interrupt outputs are intended for use in an edge triggered interrupt environment. They will not function correctly in a machine with level triggered interrupts—interrupts may be missed.

By definition the ISA bus uses edge triggered interrupts, however, in an EISA machine, interrupts can be system selected to be either edge or level triggered.

```
IRQ3.OE = !INT3 & !INT2 & !INTl & !INT0;
IRQ3 = 0;
IRQ4.OE = !INT3 & !INT2 & !INTI & INT0;
IRQ4 = 0;
IRQ5.OE = !INT3 & !INT2 & INTl & !INT0;
IRQS = 0;
IRQ9.OE = !INT3 & !INT2 & INTl & INT0;
IRQ9 = 0;
IRQ10.OE = !INT3 & INT2 & !INTl & !INT0;
IRQ10 = 0;
IRQ11.OE = !INT3 & INT2 & !INTl & INT0;
IRQ11 = 0;
IRQ12.OE = !INT3 & INT2 & INTl & !INT0;
IRQ12 = 0;
IRQ15.OE = !INT3 & INT2 & INTl & INT0;
IRQI5 = 0;
```

FIGURE 4. GAL Contents

TABLE II. Interrupt Selection

INT 2, 1, 0	Interrupt Level
0 0 0	IRQ 3
0 0 1	IRQ 4
0 1 0	IRQ 5
0 1 1	IRQ 9
1 0 0	IRQ 10
1 0 1	IRQ 11
1 1 0	IRQ 12
1 1 1	IRQ 15

3.8 Status LEDs

Five LEDs are located at the top of the board to indicate network status. The LEDs from left to right are: POLARITY (POL), COLLISION (COL), TRANSMIT (XMT), LINK (LNK) and RECEIVE (REC).

The POL LED is lit when the TPI module detects seven consecutive link pulses or three consecutive receive packets with reversed polarity.

The COL LED is lit for approximately 50 ms whenever a collision is detected.

The XMT LED is lit for approximately 50 ms whenever the AT/LANTIC controller transmits data.

In TPI mode, the LNK LED is lit while link pulses are being received. This indicates that the twisted-pair connection is active.

The REC LED is lit for approximately 50 ms whenever received data is detected.

3.9 Bed-of-Nails Testing

The DP83905EB-AT supports in-circuit testing to ensure that the board has been assembled correctly with working parts. The schematic for the board shows each of these points (TPxx) as test points. Physically, they are holes on the board or surface mount pads. Every node on the board that does not include a through hole part has an associated test point. The AT bus signals are also brought out to test points. This allows a bed-of-nails tester to probe every node of the board.

4.0 CONFIGURATION OPTIONS

Please refer to the AT/LANTIC hardware and software design guides for a more detailed explanation of this section.

The DP83905EB-AT does not require jumpers because all the configuration options for the board can be programmed by software. The serial E^{2}PROM can also be written to by the AT/LANTIC, allowing the configuration to be changed and saved. The memory map of the E^{2}PROM is shown in Table III.

TABLE III. E^{2}PROM Contents

	D15–D8	D7–D0
0FH	73H	Config. Reg. C
0EH	Config. Reg. B	Config. Reg. A
0DH	Not used	Not used
0CH	Not used	Not used
0BH	Not used	Not used
0AH	Not used	Not used
09H	Not used	Not used
08H	42H	42H
07H	57H	57H
06H	Not used	Not used
05H	Not used	Not used
04H	Not used	Not used
03H	Checksum	Board Type
02H	E'Net Address 5	E'Net Address 4
01H	E'Net Address 3	E'Net Address 2
00H	E'Net Address 1	E'Net Address 0

The fields in the E^{2}PROM are defined as:

CONFIG REG. A—Stores base I/O Address and Interrupt number that the board is currently using. The AT/LANTIC has write access to this location. See bit description in Section 4.1.

CONFIG REG. B—Stores Physical Layer Interface and programmable bus options. The AT/LANTIC has write access to this location. See bit description in Section 4.2.

CONFIG REG. C—Stores Boot PROM address and other hardware specific configuration options. The AT/LANTIC cannot write to this location. See bit description in Section 4.3.

42H—This location (08H) must contain 42H (ASCII ''B''). When DWID is low, the software will read this location in the PROM Store of the AT/LANTIC and determine that the board is in an 8-bit slot. The AT/LANTIC cannot write to this location.

57H—This location (07H) must contain 57H (ASCII ''W''). When DWID is high, the software will read this location in the PROM Store of the AT/LANTIC and determine that the board is in a 16-bit slot. The AT/LANTIC cannot write to this location.

CHECKSUM—This location is only used in Shared RAM mode. The checksum is used to verify the Ethernet Address and the board type. The two's compliment addition of the last eight bytes (03H–00H) must equal FFH, otherwise there is an error. The value of the checksum is determined from this. The AT/LANTIC cannot write to this location.

BOARD TYPE—This location is only used in Shared RAM mode. The Board Type indicator tells the network driver what hardware is being used. The AT/LANTIC cannot write to this location. When the board is configured to operate in WD8013EBT compatible Shared RAM mode, the Board Type should be 05H.

ETHERNET ADDRESS—The last six bytes of the E^{2}PROM contain the Ethernet Address which is issued by the IEEE. These bytes must be programmed uniquely prior to fitting the device onto the board, as the AT/LANTIC is unable to write to these locations.

4.1 Configuration Register A

Please refer to the AT/LANTIC datasheet for a detailed description of the bits in Configuration Register A. The following descriptions show the bit definitions and their default settings.

IOAD2–0 (D2–D0)—The Base I/O Address for the DP83905EB-AT is programmed by these three bits. When programmed to [0 0 1], the AT/LANTIC will power up in software mode and not respond to any I/O Address. However, it will monitor the parallel port (278H) for four consecutive writes. On the fourth write to 278H, bus data will be loaded into Configuration Register A, setting the I/O address for the board. This is done so that the board will not conflict with other I/O slaves in the PC. The method the AT/LANTIC uses for monitoring the parallel port and activating configuration load is unique; no other device/software is likely to perform four consecutive writes to this location. Note that the DP83905EB-AT is shipped in this mode. When run the first time, the base I/O address must be changed using the ATLES software package.

INT2–0 (D5–D3)—Based on Configuration Register C, these three bits select which Interrupt line is directly driven or which decode is used for coded interrupts. The DP83905EB-AT comes programmed to drive coded interrupt 3. [INT2–0 = 0 0 0].

FREAD (D6)—This enables the Fast Read option of the AT/LANTIC's Remote DMA Read operation. The DP83905EB-AT is shipped with the FREAD function disabled. [FREAD = 0].

MEMIO (D7)—Selects either I/O Port mode or Shared RAM mode. The DP83905EB-AT comes configured to run in I/O Port mode. [MEMIO = 0].

4.2 Configuration Register B

Please refer to the AT/LANTIC Datasheet for a detailed description of the bits in Configuration Register B. The following descriptions show the bit definitions and their default settings.

PHYS1–0 (D1–D0)—The Physical Layer Interface bits select the type of physical layer being used on the board. This could be 10BASE-T, 10BASE2, AUI (10BASE5) or Reduced Squelch Twisted Pair. The DP83905EB-AT comes configured to use 10BASE2. [PHYS1,0 = 0 1].

GDLNK (D2)—This bit enables link test pulse generation and integrity checking when using twisted pair. It can also be read to indicate status. Link pulse generation and checking is disabled by writing a 1 to this bit. The DP83905EB-AT is shipped with link testing enabled.

IO16CON (D3)—One of two methods of generating $\overline{IO16}$ is chosen using this bit. In normal operation, $\overline{IO16}$ is driven off of the address decode. $\overline{IO16}$ can be configured to be driven from the slave read or write strobe by this bit. The DP83905EB-AT, as shipped, will generate $\overline{IO16}$ from address decode. [IO16CON = 0].

CHRDY (D4)—The way the AT/LANTIC drives $\overline{IOCHRDY}$ can be selected by programming this bit. When low, the AT/LANTIC will drive $\overline{IOCHRDY}$ after a slave strobe is asserted. When high, the AT/LANTIC will drive $\overline{IOCHRDY}$ on BALE being asserted; this may be required when being used with some AT bus chipsets that sample $\overline{IOCHRDY}$ early. The DP83905EB-AT, as shipped, will drive $\overline{IOCHRDY}$ after slave strobe is asserted.

BE (D5)—This bit can be read by software to determine if there was a Bus Error. A bus error will occur if the AT/LANTIC attempts to insert wait states into a system access and the system terminates the cycle without inserting wait states.

BPWR (D6)—This bit protects Boot PROM write cycles. When high, the AT/LANTIC can generate write cycles to the Boot PROM. This feature is intended for use with writeable Boot storage devices. The DP83905-AT is not shipped with a Boot PROM, so this is programmed low.

EELOAD (D7)—The EELOAD bit enables/disables the AT/LANTIC from writing the configuration information into the E^2PROM. This bit must be set before running the E^2PROM load algorithm documented in the AT/LANTIC datasheet.

4.3 Configuration Register C

Please refer to the AT/LANTIC Datasheet for a detailed description of all the bits in Configuration Register C. The following descriptions show the bit definitions and their default settings.

BPS3–0 (D3–D0)—These four bits select the memory address and size of the Boot PROM. If BPS3–0 is equal to [0 0 0 X], the Boot PROM is disabled. The DP83905EB-AT comes configured to operate without the boot PROM.

COMP—When this bit is programmed high, the AT/LANTIC's memory uses the full 64 kbytes of RAM. When low, the memory map is compatible with either the NE2000*plus* or the WD8013EBT (16 kbytes of RAM). The DP83905EB-AT is configured to run in compatible mode.

INTMODE—This bit selects which mode the AT/LANTIC's interrupt will run. When low, direct drive interrupts are used. When high, coded interrupts are used. The DP83905 is configured to use coded interrupts.

CLKSEL—When low, the NIC core of the AT/LANTIC is clocked by the 20 MHz clock on the X1 input. When high, an external clock other than 20 MHz can be used to clock BSCK. The DP83905EB-AT is configured to run on the internal 20 MHz clock.

SOFEN—This bit enables the software to update configuration registers A and B. When high, the configuration registers are not accessible by software. The DP83905EB-AT is configured to allow software to update the configuration registers.

5.0 FUNCTIONAL OPERATION

The DP83905EB-AT takes advantage of the AT/LANTIC's ability to function in either Shared RAM mode or I/O Port mode. When in Shared RAM mode, the AT/LANTIC's bus interface is configured such that the local RAM on the board is mapped into system memory as well as the AT/LANTIC's memory. This allows the driver to have direct access to the AT/LANTIC's local memory. In I/O Port mode, the local RAM on the board is only mapped in the AT/LANTIC's address space. This permits the AT/LANTIC to have sole ownership of the RAM. The network driver has access to the RAM through a data latch, which is in I/O space.

In both architectures, the AT/LANTIC uses the local RAM to buffer both transmit and receive packets. During transmissions, the driver will write Ethernet packets into a designated block in the RAM, typically called the Transmit Buffer. In most cases, the transmit buffer is large enough for only one packet, and although they can be, packets are not queued for transmission. When the entire packet is written to memory and the AT/LANTIC is programmed to perform a transmission, the AT/LANTIC will begin reading the packet and storing it in blocks of bytes or words into its FIFO. From the FIFO, the data is serialized, encoded and transmitted to the network.

In a like manner, the AT/LANTIC uses the local RAM to store packets as they are received from the network. The AT/LANTIC's Receive Buffer is organized as a ring (or FIFO) so that multiple packets can be buffered and at the same time the network driver can read packets that have already been received. As packets are received into the AT/LANTIC's FIFO from the network, the AT/LANTIC's DMA puts the packet data into the local RAM. After packets have been buffered by the AT/LANTIC, the network driver will read the packets out of the buffer ring. Sections 5.1 and 5.2 describe how the AT/LANTIC operates in each of its bus modes. Sections 5.3 and 5.4 briefly describe the transmit and receive operations.

5.1 Shared RAM Mode

With the AT/LANTIC configured to operate in Shared RAM Mode, the DP83905EB-AT is hardware compatible with a WD8013EBT card. Changes to the EEPROM contents are needed for the WD8013EBT drivers to run.

While operating in Shared RAM mode, the local RAM on the DP83905EB-AT can be mapped into system memory at one of several different locations. The upper and lower address decode and memory width can be selected by the Shared Memory Control Registers of the AT/LANTIC. The depth of the memory can be selected in Configuration Register C by setting the compatible (COMP) bit. This will configure the RAM to be either 16 kbytes (compatible with the NE2000*plus* and WD8013EBT) or 64 kbytes. The local buffer RAM is then accessible to both the AT/LANTIC and the ISA bus. An arbiter, internal to the AT/LANTIC, will determine which device currently has access to the RAM. The AT/LANTIC will only access the RAM during local DMA burst cycles for transmit and receive operations, however, it is critical that the AT/LANTIC is granted the bus within a short time after requesting it. For this reason, the arbiter will grant access to the internal NIC core in the event that both the AT/LANTIC and the host request the local bus at the same time. This arbitration is transparent to both the hardware and the network driver.

5.2 I/O Port Mode

If the AT/LANTIC is configured for I/O Port Mode, the DP83905EB-AT will be hardware compatible with an NE2000*plus* card. The NE2000*plus* network drivers will then run on the DP83905EB-AT.

In I/O Port mode, the AT/LANTIC is configured to use the Remote DMA function of the NIC core. In this mode of operation, the local RAM of the DP83905EB-AT is accessible only by the AT/LANTIC. In order for the driver to read any packets from the buffer ring or write any packets into the transmit buffer, the AT/LANTIC must be programmed to perform a remote DMA cycle. To execute a Remote DMA, the bus interface logic of the AT/LANTIC performs a simple handshake between the ISA bus and the NIC core through a D-type data latch (internal to the AT/LANTIC). For a remote DMA read, the AT/LANTIC will read a byte/word of data from the local memory and write it to the data latch. At the same time an I/O read cycle is executed by the host and the data is read from the latch. The handshake logic will wait state the ISA bus if the data is not ready when the read strobe becomes active. In a like manner, the AT/LANTIC will read data from the latch and write it to the local RAM during a remote DMA write.

As in Shared RAM mode, the AT/LANTIC's registers are accessible in I/O space. There is the addition of a hardware $\overline{\text{RESET}}$ port which can be driven by reading and writing to I/O location BASE + 18H, where BASE is the I/O base address chosen in Configuration Register A. The registers, data latches and reset port occupy 16 bytes of I/O space. Unlike Shared RAM mode, the Ethernet Address PROM is not located in I/O space. It is accessible only by the AT/LANTIC, so a remote DMA read is used to obtain its contents. In both I/O mode and Shared RAM mode, the Ethernet Address PROM is not a physical device, but a dynamic copy of the Ethernet address and other information (from the E^2PROM) held in the AT/LANTIC.

5.3 Transmit

The DP83905EB-AT can transmit and receive Ethernet packets on the three basic types of media available today. A twisted pair transceiver internal to the AT/LANTIC allows easy connectivity to a 10BASE-T network. The transceiver provides link integrity checking, polarity detection and correction and pre-emphasis of the transmit output. The AT/LANTIC can also be configured to use its AUI interface for connection to a MAU (10BASE2/5/F/T) or on board 10BASE2 transceiver.

To transmit a packet, there are three basic steps that need to be taken. Please refer to *Figure 1* of this Application Note. First, the packet that is to be transmitted is loaded into the AT/LANTIC's buffer RAM by the host. The packet must consist of a destination address, a source address, length and data. If the data is less than 48 bytes, it must be padded with arbitrary data so that the entire packet is 64 bytes as required by the IEEE 802.3 standard. (This is not a requirement of the AT/LANTIC.) Next, once the packet is in RAM, the host programs the local DMA registers with the location and length of the packet to be transmitted. Lastly, the host issues the transmit command to the AT/LANTIC and the AT/LANTIC will start transmitting the packet.

The first activity the AT/LANTIC does is a prefetch to load the FIFO with data. Next, the NIC core of the AT/LANTIC will start sending preamble in NRZ format to the ENDEC. The ENDEC, in turn, encodes the data with the transmit clock in Manchester format and drives a differential transmit pair to either the internal twisted pair transceiver or to the AUI port of the AT/LANTIC. The twisted pair transceiver then drives the TXO outputs while pre-emphasizing the signal to eliminate inter-symbol jitter. If 10BASE2 is being used, the DP8392CV receives the differential transmit data from the AT/LANTIC and drives the coax line with a single-ended signal. Both transceivers will monitor the network for collisions.

In the event that there is a collision, the transceiver will drive a 10 MHz signal on the Collision Detect differential pair. The ENDEC will then drive a collision signal to the NIC core so that the Ethernet MAC control section of the NIC will implement the collision backoff algorithm and attempt re-transmission.

After the preamble and start-of-frame delimiter have been transmitted, the AT/LANTIC will serialize bytes from the FIFO and transmit them in the manner described above. When the FIFO empties to a pre-set threshold, the AT/LANTIC will fetch more data from the local RAM using its local DMA function. As the data is being transmitted, a Cyclic Redundancy Check (CRC) is continuously being calculated. After all the data has been transmitted, the 4 byte CRC value is transmitted. This allows receiving stations to check the received packet for data integrity.

5.4 Receive

Receiving a packet is almost the exact opposite of transmitting a packet. The functional blocks discussed above remain the same, however there are some differences which will be discussed. The transceiver will sit idle until a valid signal is received on the media, indicating the start of a packet. This causes the transceiver's RX squelch to turn off. Both the twisted pair transceiver (internal to the AT/LANTIC) and the DP8392CV CTI have squelch circuitry which filter out noise on the network, however, they are implemented differently. The TPI transceiver checks an incoming signal for both amplitude and frequency (sometimes referred to as smart squelch).

The CTI only checks for valid amplitude. Once the CTI has turned its RX squelch off it starts driving the receive differential pair of the AUI. The ENDEC (internal to the AT/LANTIC) recovers a 10 MHz clock and receive data in NRZ format from the receive pair with its analog PLL. The NRZ data is clocked into the NIC core, de-serialized, and loaded into the FIFO. When the number of bytes in the FIFO reaches the programmed threshold, the AT/LANTIC requests the local bus and writes the received data into the receive buffer memory using its local DMA. After the packet is received, the AT/LANTIC writes four bytes of status information into the buffer and interrupts the host to inform it that the packet can be removed by software.

6.0 CONCLUSION

The DP83905EB-AT Demonstration board provides system developers with an easy to understand and use example of how to design an industry standard Ethernet adapter card. The DP83905EB-AT design can readily be adapted for PC® motherboard designs too.

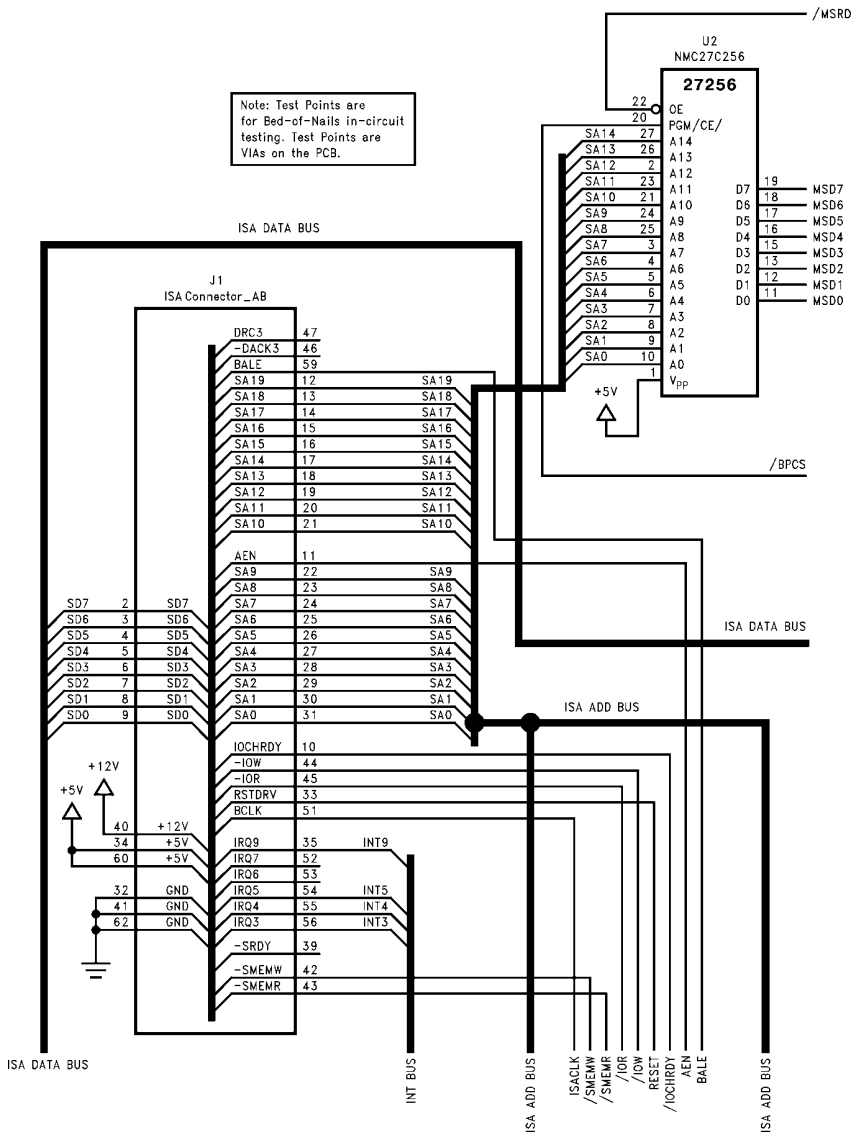
By using the DP83905 AT/LANTIC, jumperless Ethernet boards can be made extremely cost effective and simple to design and use.

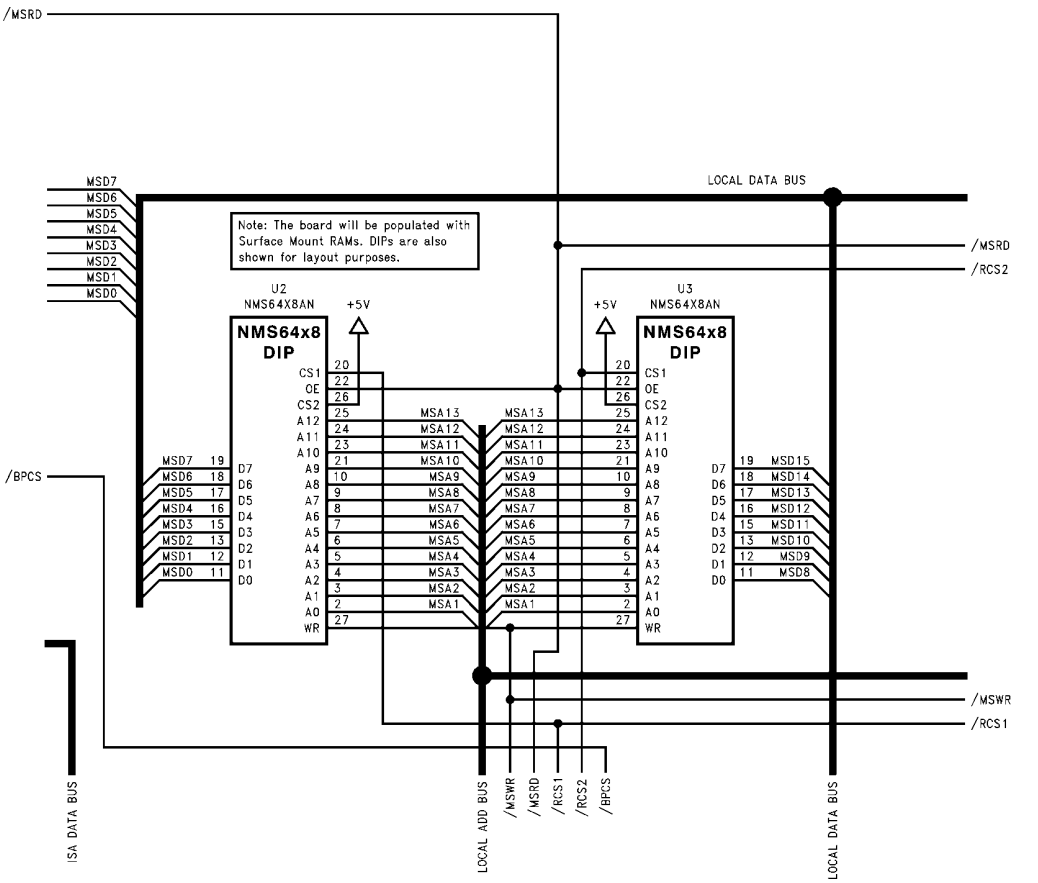
Parts List for DP83905EB-AT

Capacitors		
C1	27 pF	10% Ceramic, SMT 0805
C2	27 pF	10% Ceramic, SMT 0805
C3–C4	0.01 μF/50V	20% Ceramic, SMT 1206
C5	22 μF/16V	20% Tantalum, SMT 7343
C6	0.01 μF/50V	20% Ceramic, SMT 1206
C7	0.01 μF/1 kV	20% Ceramic Disk, TH
C8–C9	0.01 μF/50V	20% Ceramic, SMT 1206
C10	10 μF/16V	10% Ceramic, SMT 7343
C11–C20	0.01 μF/50V	20% Ceramic, SMT 1206
C21–C22	22 μF/16V	20% Tantalum, SMT 7343
C23–C27	0.01 μF/50V	20% Ceramic, SMT 1206
C28–C31	0.01 μF/50V	20% Ceramic, SMT 1206
C42, C44	0.01 μF/50V	20% Ceramic, SMT 1206
C43, C45	0.001 μF/50V	20% Ceramic, SMT 1206
C46–C47	33 pF/50V	10% Ceramic, SMT 0805
SP1	0.75 pF/1 kV	Spark Gap, TH
Resistors		
R2–R5	270Ω	5%, 1/8W, SMT 1206
R6–R9	39.2Ω	1%, 1/8W, SMT 1206
R10–R13	1.5 kΩ	5%, 1/8W, SMT 1206
R14	1 kΩ	1%, 1/8W, SMT 1206
R15	150Ω	1%, 1/8W, SMT 1206
R17	1 MΩ	5%, 1/2W, TH
R18	10 kΩ	1%, 1/8W, SMT 1206
R19	274Ω	1%, 1/8W, SMT 1206
R20	66.5Ω	1%, 1/8W, SMT 1206
R21	66.5Ω	1%, 1/8W, SMT 1206
R22	274Ω	1%, 1/8W, SMT 1206
R23	806Ω	1%, 1/8W, SMT 1206
R24–R25	49.9Ω	1%, 1/8W, SMT 1206
R26	22Ω	1%, 1/8W, SMT 1206
R39–R41	270Ω	5%, 1/8W, SMT 1206
R42	1 kΩ	1%, 1/8W, SMT 1206

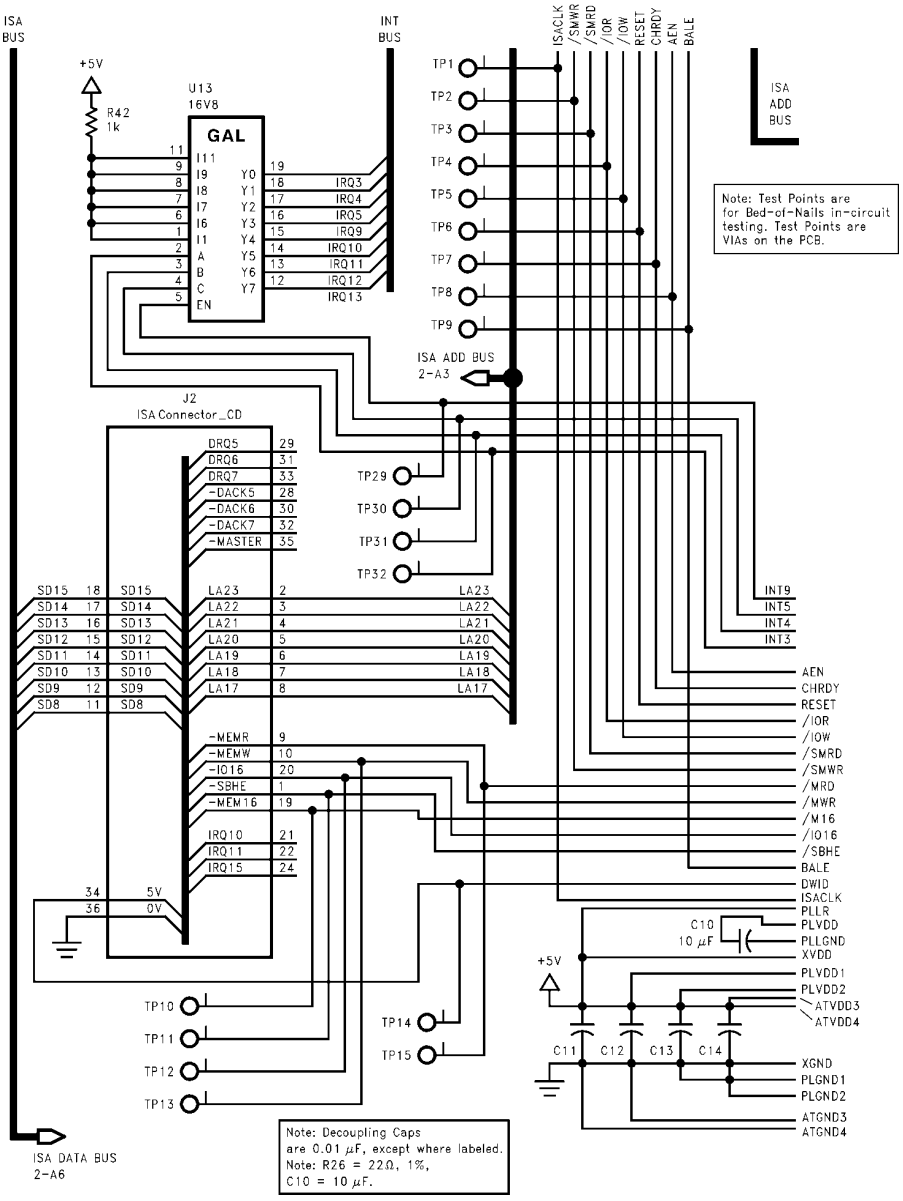
Parts List for DP83905EB-AT (Continued)

Integrated Circuits				
U1	AT/LANTIC	DP83905		
U4	EEPROM	NM93C06		
U5	EPROM	NM27C256		Do not populate
U6	FILTER	FL1012	VALOR	
U7	CTI	DP8392CV		
U9	8k x 8 SRAM	NMS64X8M70		
U10	8k x 8 SRAM	NMS64X8M70		
U13	GAL16V8	16V8-25LVC		
Connectors				
J3	15-Pin D Connector, Female (AMP # 745782-4)			AMP
J4	BNC Connector, Female (AMP #227161-7)			AMP
J5	RJ45 Modular Phone Jack, 8-Pin (AMP #555164-1)			AMP
Magnetics				
U8	DC-DC CONVERTER	PM6077	VALOR	
Y1	PULSE TRANSFORMER	23Z91SM	FIL-MAG	
Y2	PULSE TRANSFORMER	23Z91SM	FIL-MAG	
Socket				
S1	28-Pin Dual-in-Line Socket for EPROM, U5			
Diodes				
D1	MMBD1201			
D2	3mm Green LED			
D3	3mm Orange LED			
D6	3mm Green LED			
D7	3mm Hi-Efficiency Red LED			
D8	3mm Yellow LED			
Clocks				
X1	HC49S, 20 MHz Crystal (low profile) (Refer to AT/LANTIC datasheet for crystal specifications).			
X2	20 MHz Oscillator, 45-55 Duty cycle, 0.001% Tolerance Oscillator module should be raised off of board when mounting.			Do not populate

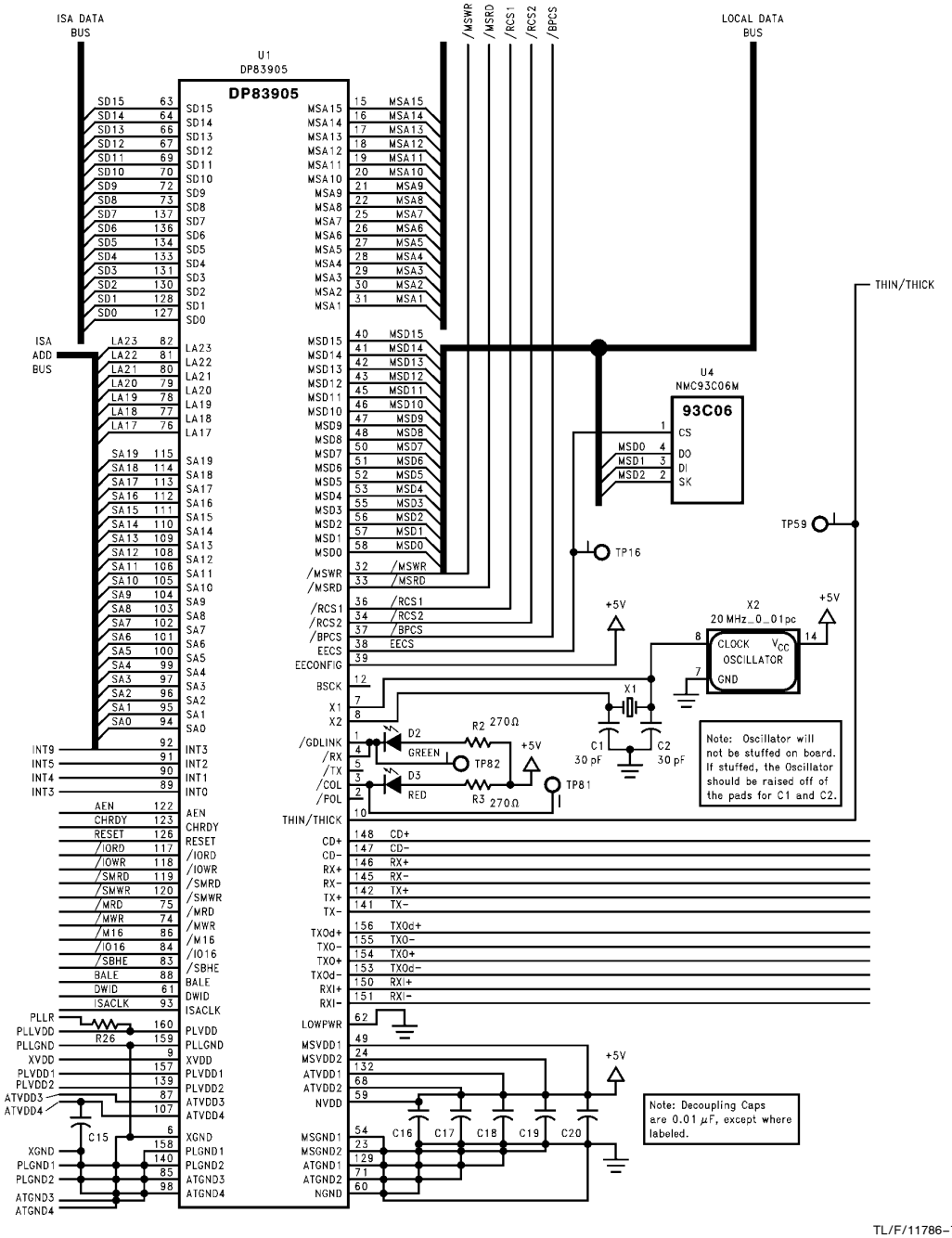

/MSRD
U2
NMC27C256
27256
Note: Test Points are for Bed-of-Nails in-circuit testing. Test Points are VIAs on the PCB.
ISA DATA BUS
J1
ISA Connector_AB
/BPCS
ISA ADD BUS
+12V
+5V
GND
INT BUS
ISACLK
/SMEMW
/SMEMR
/IOR
/IOW
RESET
/IOCHRDY
AEN
BALE
TL/F/11786–4


/MSRD
MSD7
MSD6
MSD5
MSD4
MSD3
MSD2
MSD1
MSD0
LOCAL DATA BUS
Note: The board will be populated with Surface Mount RAMs. DIPs are also shown for layout purposes.
/MSRD
/RCS2
U2
NMS64X8AN
+5V
NMS64x8 DIP
U3
NMS64X8AN
+5V
NMS64x8 DIP
CS1
OE
CS2
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WR
D7
D6
D5
D4
D3
D2
D1
D0
MSA13
MSA12
MSA11
MSA10
MSA9
MSA8
MSA7
MSA6
MSA5
MSA4
MSA3
MSA2
MSA1
MSD15
MSD14
MSD13
MSD12
MSD11
MSD10
MSD9
MSD8
/BPCS
/MSWR
/RCS1
ISA DATA BUS
LOCAL ADD BUS
/MSWR
/MSRD
/RCS1
/RCS2
/BPCS
LOCAL DATA BUS

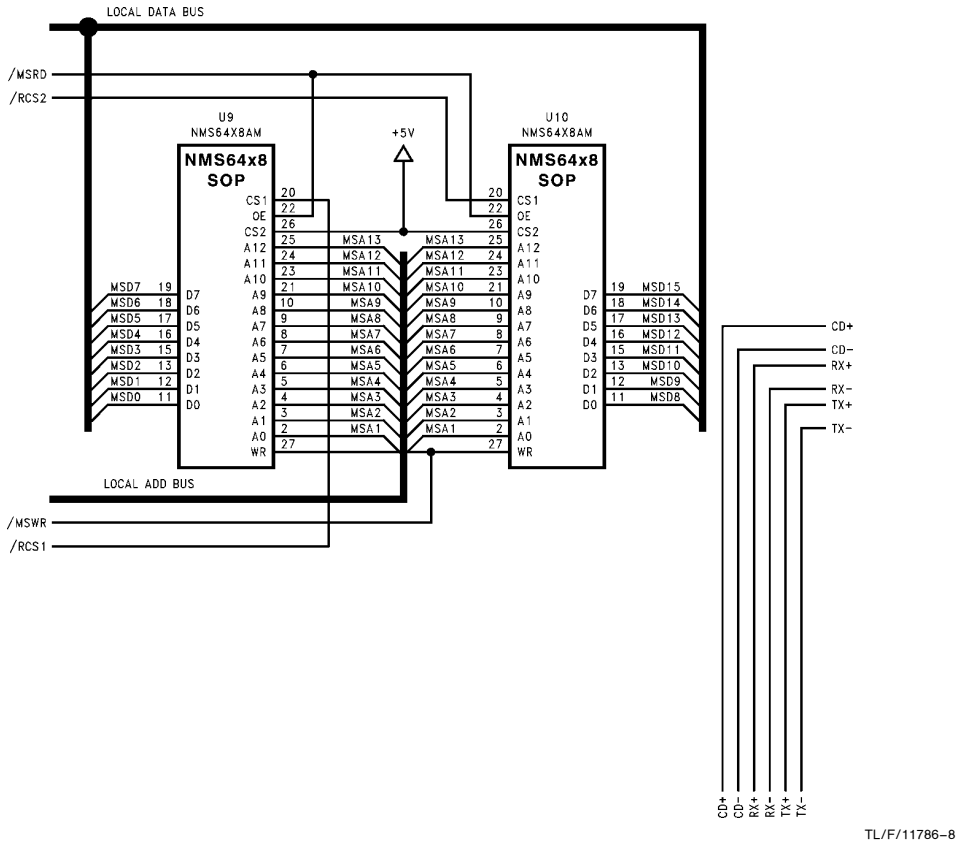
TL/F/11786–5


ISA BUS
INT BUS
ISACLK
/SMWR
/SMRD
/IOR
/IOW
RESET
CHRDY
AEN
BALE
+5V
R42
1k
U13
16V8
GAL
I11
I9
I8
I7
I6
I1
A
B
C
EN
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
IRQ3
IRQ4
IRQ5
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
ISA ADD BUS
ISA ADD BUS 2-A3
Note: Test Points are for Bed-of-Nails in-circuit testing. Test Points are VIAs on the PCB.
J2
ISA Connector_CD
DRQ5
DRQ6
DRQ7
-DACK5
-DACK6
-DACK7
-MASTER
TP29
TP30
TP31
TP32
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
LA23
LA22
LA21
LA20
LA19
LA18
LA17
INT9
INT5
INT4
INT3
AEN
CHRDY
RESET
/IOR
/IOW
/SMRD
/SMWR
/MRD
/MWR
/M16
/IO16
/SBHE
BALE
DWID
ISACLK
-MEMR
-MEMW
-IO16
-SBHE
-MEM16
IRQ10
IRQ11
IRQ15
5V
0V
PLLR
PLVDD
PLLGND
XVDD
PLVDD1
PLVDD2
ATVDD3
ATVDD4
C10
10 µF
C11
C12
C13
C14
XGND
PLGND1
PLGND2
ATGND3
ATGND4
TP10
TP11
TP12
TP13
TP14
TP15
ISA DATA BUS 2-A6
Note: Decoupling Caps are 0.01 µF, except where labeled.
Note: R26 = 22Ω, 1%,
C10 = 10 µF.

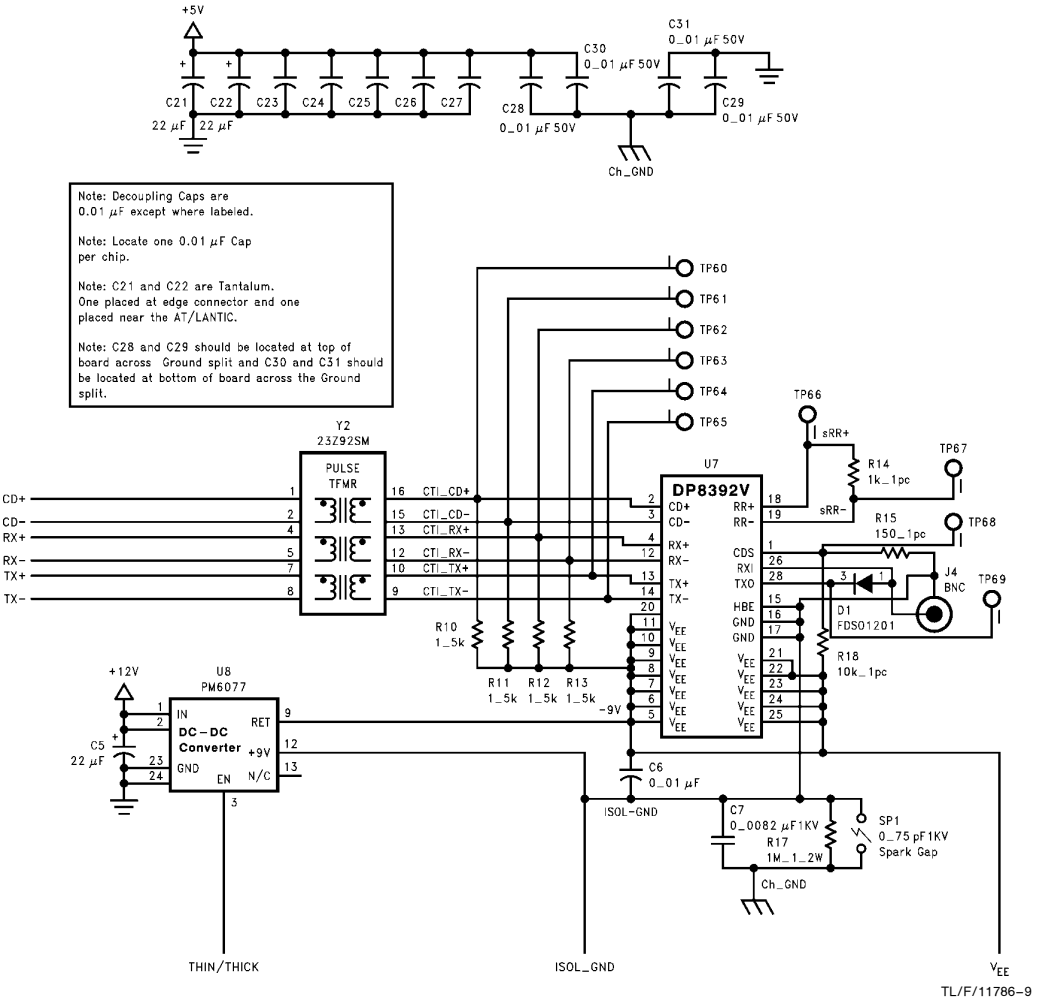
TL/F/11786–6


ISA DATA BUS
LOCAL DATA BUS
/MSWR
/MSRD
/RCS1
/RCS2
/BPCS
U1
DP83905
U4
NMC93C06M
93C06
CS
DO
DI
SK
MSD0
MSD1
MSD2
THIN/THICK
TP59
TP16
TP82
TP81
+5V
X1
X2
20 MHz_0_01pc
CLOCK OSCILLATOR
GND
D2
GREEN
D3
RED
R2 270Ω
R3 270Ω
C1 30 pF
C2 30 pF
Note: Oscillator will not be stuffed on board. If stuffed, the Oscillator should be raised off of the pads for C1 and C2.
Note: Decoupling Caps are 0.01 µF, except where labeled.
C15
C16
C17
C18
C19
C20
ISA ADD BUS
INT9
INT5
INT4
INT3
PLLR
R26
PLLVDD
PLLGND
XVDD
PLVDD1
PLVDD2
ATVDD3
ATVDD4
XGND
PLGND1
PLGND2
ATGND3
ATGND4
LOWPWR
NVDD
NGND

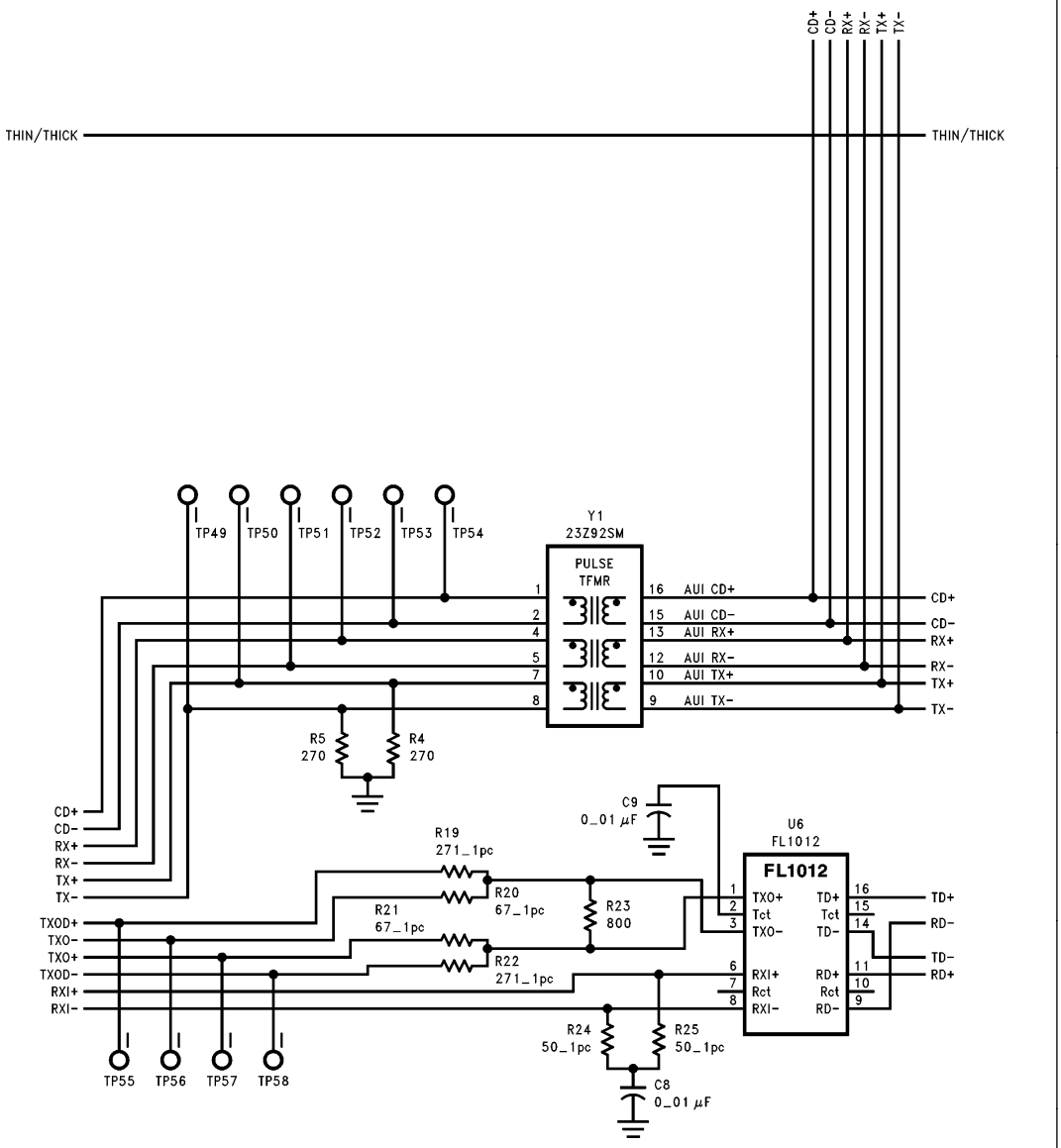
TL/F/11786–7


LOCAL DATA BUS
/MSRD
/RCS2
U9
NMS64X8AM
NMS64x8
SOP
+5V
U10
NMS64X8AM
NMS64x8
SOP
CS1
OE
CS2
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WR
D7
D6
D5
D4
D3
D2
D1
D0
MSD7 19
MSD6 18
MSD5 17
MSD4 16
MSD3 15
MSD2 13
MSD1 12
MSD0 11
MSD15 19
MSD14 18
MSD13 17
MSD12 16
MSD11 15
MSD10 13
MSD9 12
MSD8 11
MSA13
MSA12
MSA11
MSA10
MSA9
MSA8
MSA7
MSA6
MSA5
MSA4
MSA3
MSA2
MSA1
LOCAL ADD BUS
/MSWR
/RCS1
CD+
CD-
RX+
RX-
TX+
TX-

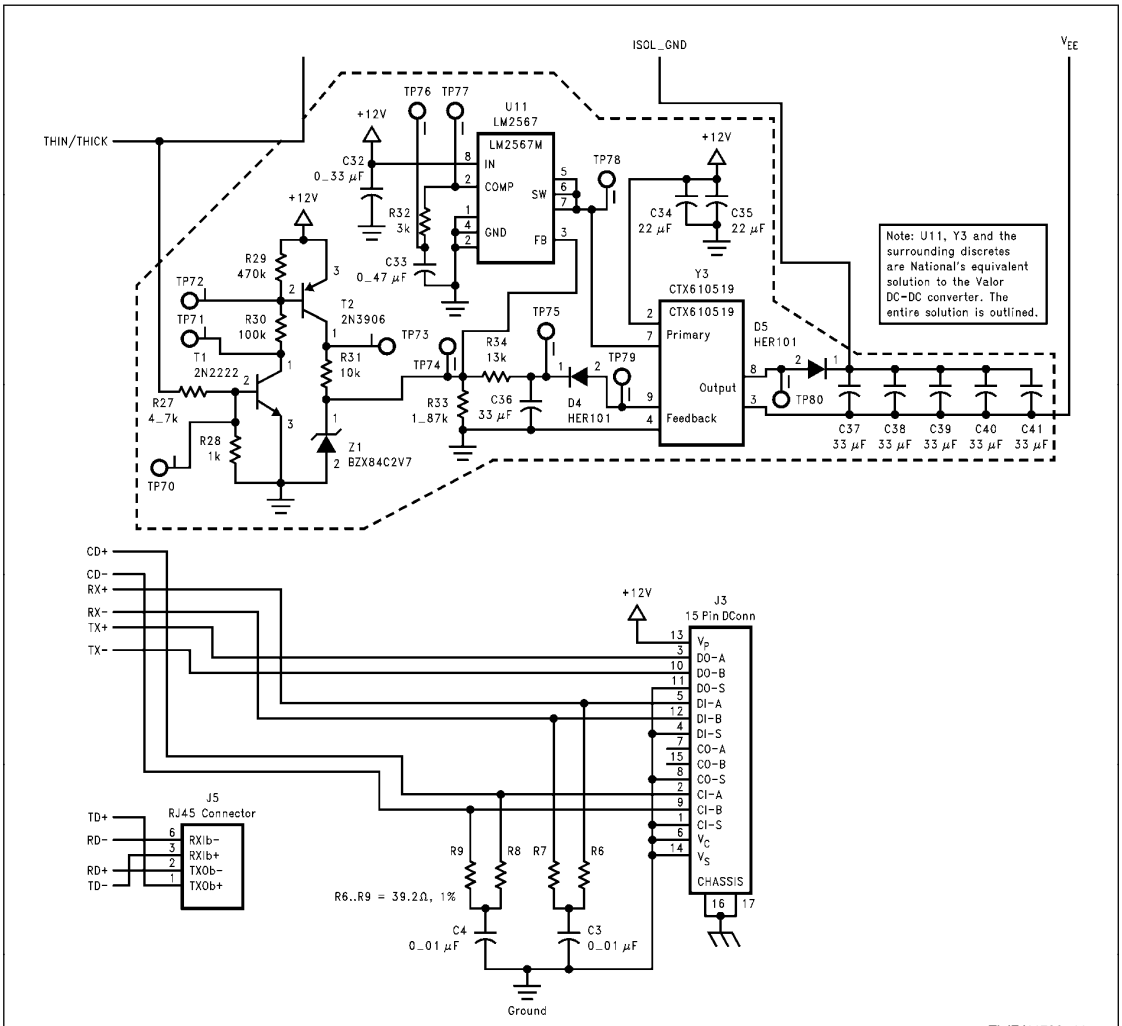
TL/F/11786–8


+5V
C21
22 µF
C22
22 µF
C23
C24
C25
C26
C27
C28
0_01 µF 50V
C30
0_01 µF 50V
C31
0_01 µF 50V
C29
0_01 µF 50V
Ch_GND
Note: Decoupling Caps are 0.01 µF except where labeled.
Note: Locate one 0.01 µF Cap per chip.
Note: C21 and C22 are Tantalum. One placed at edge connector and one placed near the AT/LANTIC.
Note: C28 and C29 should be located at top of board across Ground split and C30 and C31 should be located at bottom of board across the Ground split.
TP60
TP61
TP62
TP63
TP64
TP65
TP66
sRR+
TP67
R14
1k_1pc
sRR−
R15
150_1pc
TP68
J4
BNC
TP69
D1
FDSO1201
Y2
23Z92SM
PULSE
TFMR
CD+
CD−
RX+
RX−
TX+
TX−
CTI_CD+
CTI_CD−
CTI_RX+
CTI_RX−
CTI_TX+
CTI_TX−
U7
DP8392V
CD+
CD−
RX+
RX−
TX+
TX−
RR+
RR−
CDS
RXI
TXO
HBE
GND
GND
VEE
R10
1_5k
R11
1_5k
R12
1_5k
R13
1_5k
R18
10k_1pc
−9V
+12V
U8
PM6077
IN
GND
DC−DC
Converter
RET
+9V
EN
N/C
C5
22 µF
C6
0_01 µF
ISOL−GND
C7
0_0082 µF1KV
R17
1M_1_2W
SP1
0_75 pF1KV
Spark Gap
Ch_GND
THIN/THICK
ISOL_GND
VEE

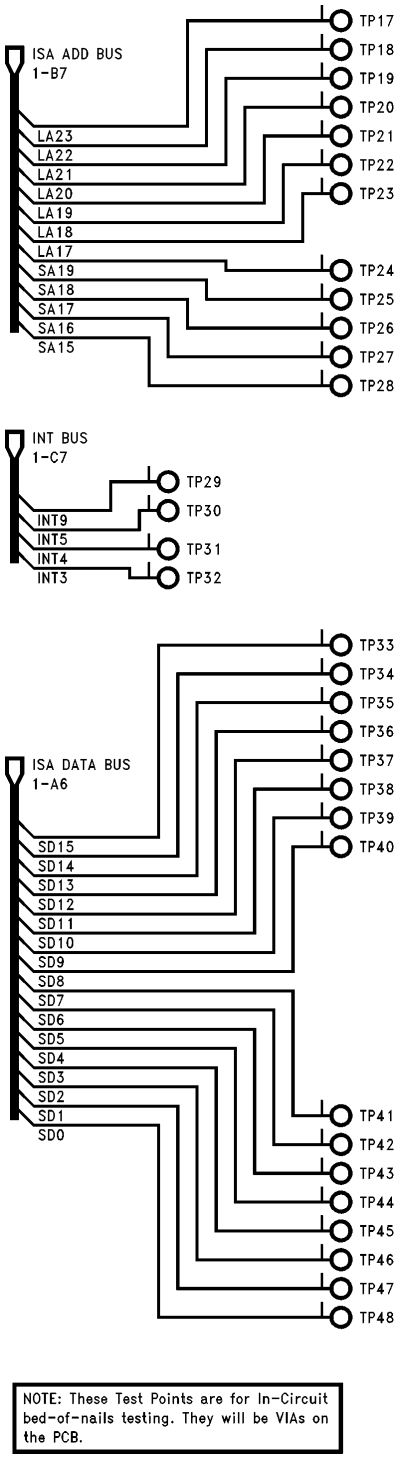
TL/F/11786–9


CD+
CD−
RX+
RX−
TX+
TX−
THIN/THICK
THIN/THICK
TP49
TP50
TP51
TP52
TP53
TP54
Y1
23Z92SM
PULSE
TFMR
1
2
4
5
7
8
16 AUI CD+
15 AUI CD−
13 AUI RX+
12 AUI RX−
10 AUI TX+
9 AUI TX−
CD+
CD−
RX+
RX−
TX+
TX−
R5
270
R4
270
C9
0_01 µF
U6
FL1012
FL1012
TXO+
Tct
TXO−
RXI+
Rct
RXI−
TD+
Tct
TD−
RD+
Rct
RD−
1
2
3
6
7
8
16
15
14
11
10
9
TD+
RD−
TD−
RD+
R19
271_1pc
R20
67_1pc
R21
67_1pc
R22
271_1pc
R23
800
R24
50_1pc
R25
50_1pc
C8
0_01 µF
TXOD+
TXO−
TXO+
TXOD−
RXI+
RXI−
TP55
TP56
TP57
TP58

TL/F/11786–10

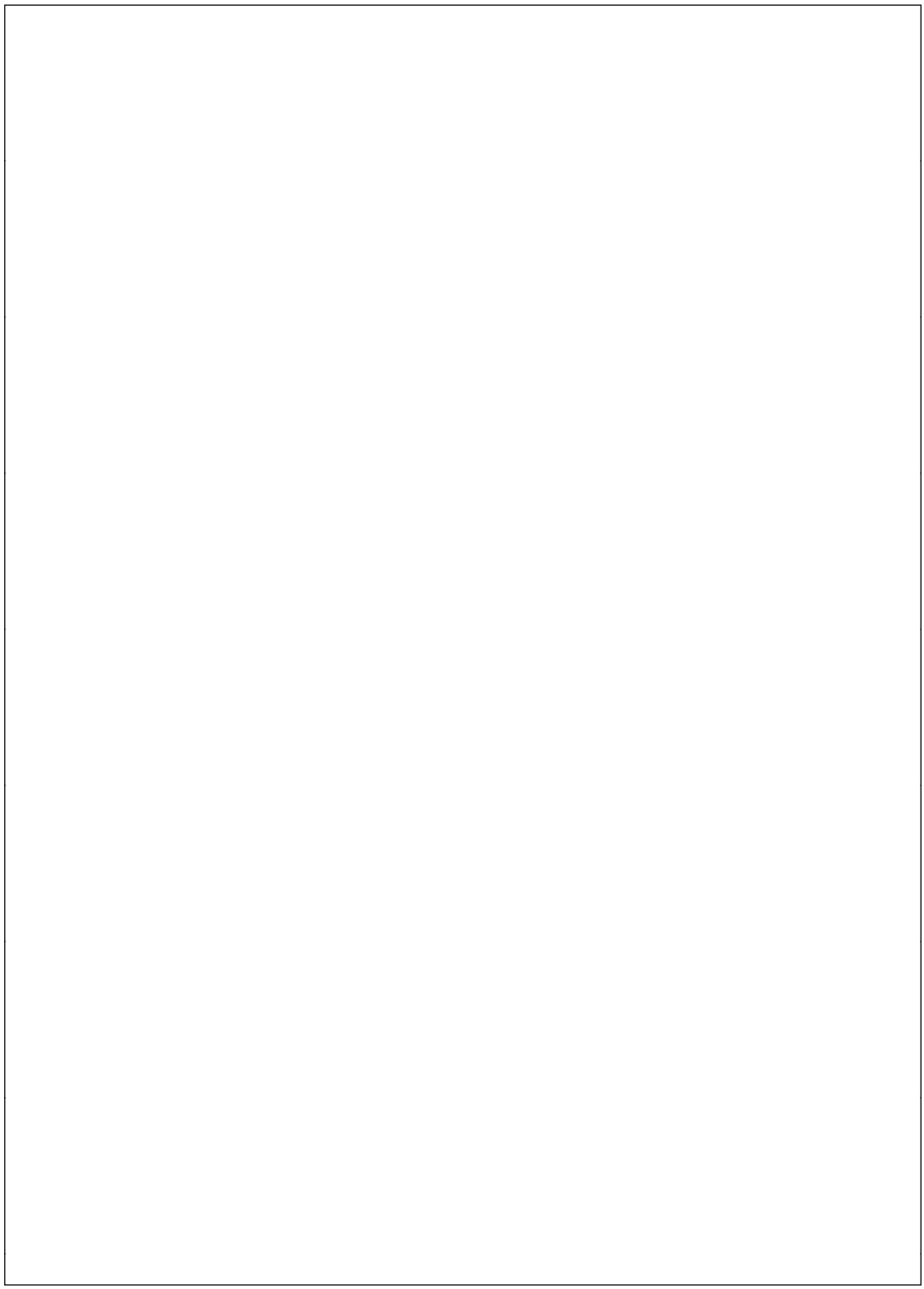

ISOL_GND
V_{EE}
THIN/THICK
TP76
TP77
+12V
U11
LM2567
LM2567M
IN
COMP
GND
SW
FB
C32
0_33 µF
R32
3k
C33
0_47 µF
TP78
+12V
C34
22 µF
C35
22 µF
Y3
CTX610519
CTX610519
Primary
Output
Feedback
D5
HER101
Note: U11, Y3 and the surrounding discretes are National's equivalent solution to the Valor DC-DC converter. The entire solution is outlined.
TP72
TP71
R29
470k
R30
100k
T2
2N3906
T1
2N2222
R31
10k
TP73
TP74
TP75
R34
13k
TP79
R33
1_87k
C36
33 µF
D4
HER101
TP80
C37
33 µF
C38
33 µF
C39
33 µF
C40
33 µF
C41
33 µF
R27
4_7k
R28
1k
TP70
Z1
BZX84C2V7
CD+
CD-
RX+
RX-
TX+
TX-
+12V
J3
15 Pin DConn
V_P
DO-A
DO-B
DO-S
DI-A
DI-B
DI-S
CO-A
CO-B
CO-S
CI-A
CI-B
CI-S
V_C
V_S
CHASSIS
J5
RJ45 Connector
TD+
RD-
RD+
TD-
RXIb-
RXIb+
TXOb-
TXOb+
R9
R8
R7
R6
R6..R9 = 39.2Ω, 1%
C4
0_01 µF
C3
0_01 µF
Ground

TL/F/11786–11



NOTE: These Test Points are for In-Circuit bed-of-nails testing. They will be VIAs on the PCB.

TL/F/11786–12



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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