Interfacing the HPC46064 to the DP83200 FDDI Chip Set

National Semiconductor
Application Note 736
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1.0 INTRODUCTION

Fiber Distributed Data Interface (FDDI) is a high bandwidth (100 Mbits per second) local area network (LAN) which uses a dual redundant ring architecture. The network consists of a number of point to point links connected to form a ring. The physical and electrical characteristics of the ring protocol are covered by the Physical Media Dependent (PMD), Physical (PHY) and Media Access Control (MAC) Standards as defined by the American National Standards Institute (ANSI) X3T9.5 committee, and can be implemented using the DP83200 FDDI chipset from National Semiconductor. The on-line verification of these point to point links, and the formation of a ring is covered by the FDDI Station Management (SMT) Standard.

This application note covers the use of the HPC46064 High Performance Microcontroller from National Semiconductor to provide the local processing power required within a Fiber Distributed Data Interface (FDDI) node for Station Management (SMT). The note covers the interface between the HPC and the FDDI chipset from National Semiconductor and a possible system architecture.

2.0 FDDI INTELLIGENT STATION ARCHITECTURE

In FDDI, the Station Management (SMT) service is split into three main sections, SMT Frame Services, Ring Management (RMT) and Connection Management (CMT). Within the National Semiconductor implementation of FDDI, any controller handling RMT and CMT services need only access the Control Bus directly, although a communications channel to the host is also required. An architecture using the HPC from National Semiconductor is shown in *Figure 1*. This can be implemented directly using the interface shown in *Figure 2*. Using this architecture, the SMT frame services are provided by the host.

The architecture shown is one of several that could be implemented with the HPC and the National FDDI chipset. This architecture connects the HPC multiplexed address/data bus to the control bus of the FDDI devices, allowing the HPC to access these devices directly with single instructions. The 16 Kbyte ROM of the HPC46064 is used to minimize chip count, though this architecture allows external ROM or RAM to be used if additional functions are implemented.

The HPC has sufficient performance to handle all of SMT, including frame based management, but this would require that the HPC have access to the frame buffer memory. This requires an arbitration scheme to resolve conflicts between the host and the HPC in accessing the buffer RAM. The arbitration scheme could be simply implemented using the HOLD and HLDA (Hold Acknowledge) pins of the HPC.

An advantage of putting all of SMT on the board is that the SMT function need not be resident in the host memory. The removal of TSRs or daemons from host memory leaves more room for applications.

An alternative architecture would run the HPC in single chip mode, reducing the chip count and allowing the Universal Peripheral Interface (UPI) port to be used as the host interface. This would require software drivers to simulate the FDDI control bus signals using the I/O ports of the HPC.

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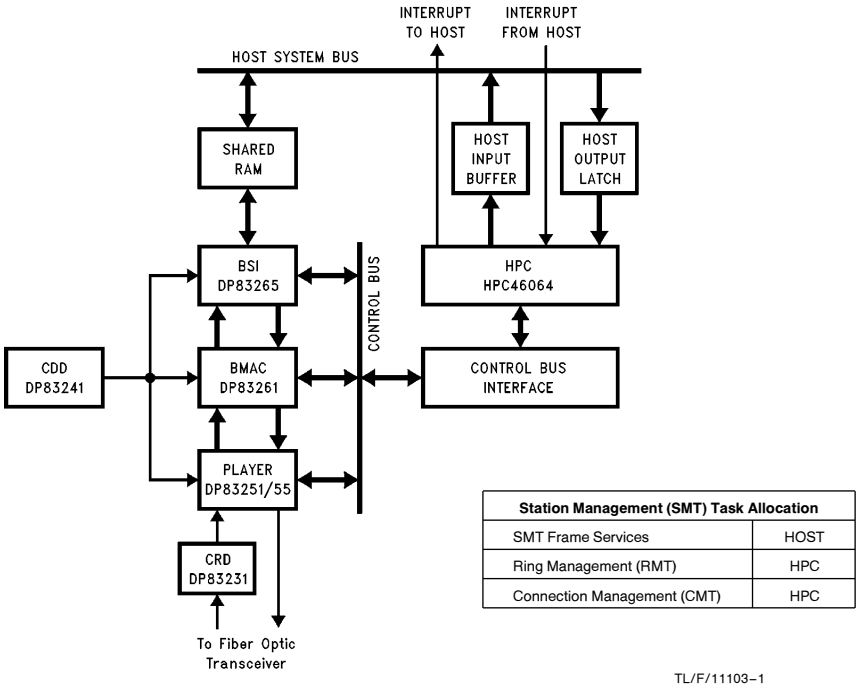

Station Management (SMT) Task Allocation	
SMT Frame Services	HOST
Ring Management (RMT)	HPC
Connection Management (CMT)	HPC

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FIGURE 1. FDDI Station Architecture Using HPC for Partial Station Management

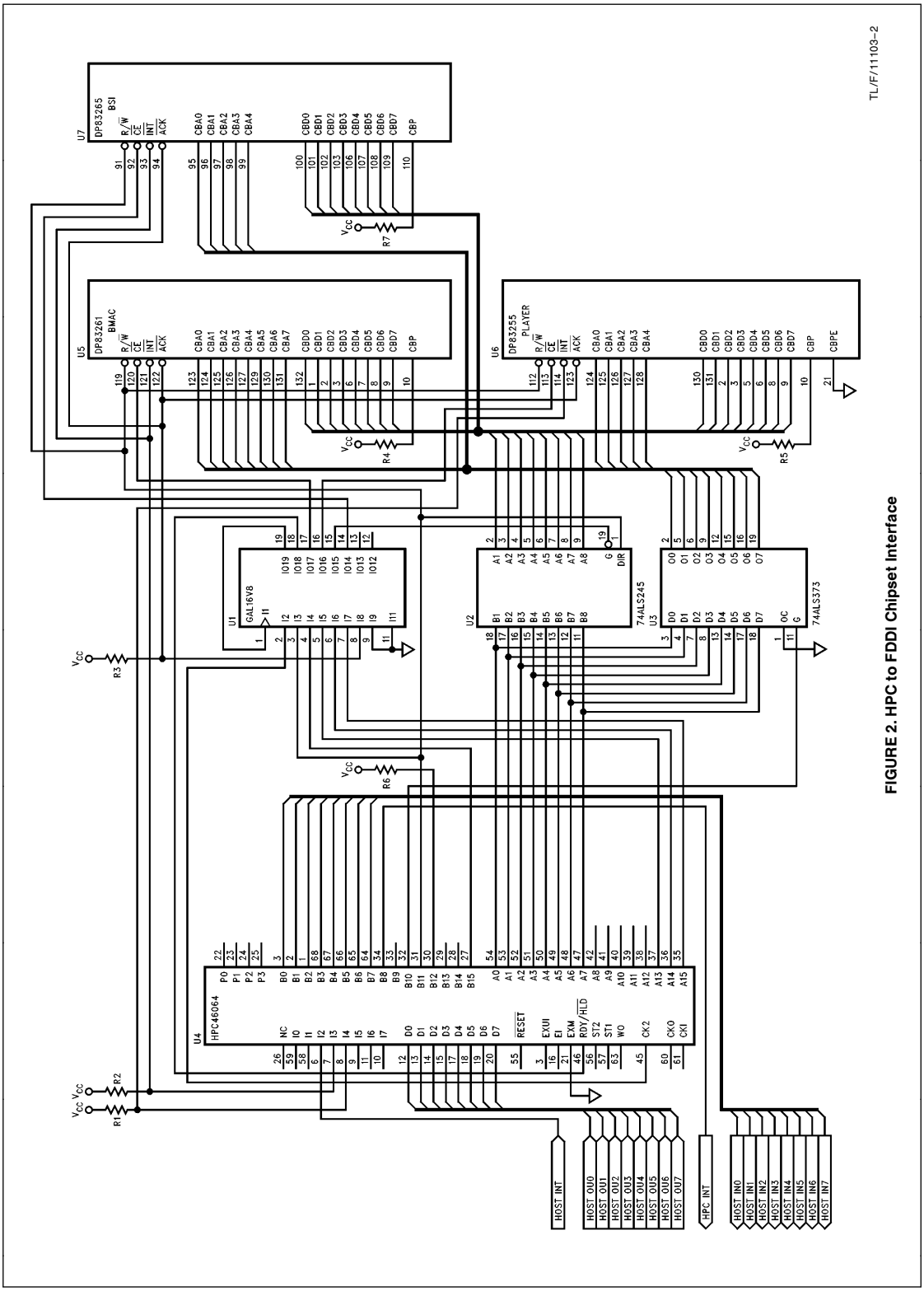

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FIGURE 2. HPC to FDDI Chipset Interface

3.0 DP83200 FDDI CHIPSET

The DP83200 FDDI chipset from National Semiconductor implements the PHY and MAC Standards as defined by the American National Standards Institute (ANSI) X3T9.5 committee. The chipset includes the following devices.

DP83231 Clock Recovery Device (CRD™ DEVICE)

The Clock Recovery Device extracts a 125 MHz clock from the incoming data of the upstream station. Its features include on-chip loopback control, on-chip PLL, ability to lock to a Master Line State in less than 100 μs, and a single +5V supply.

DP83241 Clock Distribution Device (CDD™ DEVICE)

From a 12.5 MHz reference, the CDD generates the 125 MHz, 25 MHz and 12.5 MHz clocks required by the PLAYER™ and BMAC™ devices.

DP83251/DP83255 Physical Layer Controller (PLAYER™ DEVICE)

The PLAYER device converts the BMAC 12.5 Mbyte/s stream into a 125 Mbaud 4B/5B encoded bit stream as specified in the FDDI PHY Standard. It synchronizes the received bit stream to the local 12.5 MHz clock and decodes the 4B/5B data into internal code. The DP83255 PLAYER device also contains a configuration switch for use in dual attachment stations and concentrators.

DP83261 Basic Media Access Controller (BMAC™ DEVICE)

The BMAC implements the functions defined by ANSI X3T9.5 FDDI Media Access Control Standard. The BMAC consists of the transmit and receive state machines, an address magnitude compare unit, a CRC checker, a CRC generator, protocol timers and diagnostic counters.

DP83265 BMAC System Interface (BSI™ DEVICE)

The BSI device provides a multiframe, multiple channel interface between the BMAC device and a host system. The BSI device interfaces directly to the system bus or through low-cost DRAMs. The efficient data structures employed provide high throughput with minimal host intervention.

For more information on these and other devices in the chipset please consult the appropriate data sheets and application notes.

4.0 HPC46064 High Performance Microcontroller (HPC DEVICE)

The HPC46064 is a member of the HPC family of High Performance Microcontrollers. Each member of the family has the same core CPU with a unique memory and I/O configuration to suit specific applications. The HPC46064 has 16 Kbytes of on-chip ROM and is fabricated in National's microCMOS technology. This process combined with the advanced architecture provides fast, flexible I/O, efficient data manipulation, and high speed computation.

The HPC46064 features include 16 bit internal architecture, 16- or 8-bit external data bus, 16 bit address and up to 52 general purpose I/O lines. The HPC46064 also includes a full duplex UART, four 16-bit timers, 16 Kbytes of ROM and 512 bytes of RAM.

The HPC46064 is used in this design because its 16 Kbytes of on-chip ROM remove the need for an external EPROM.

For prototyping or small production runs the pin compatible HPC467064 may be used, which has 16 Kbytes of on-chip EPROM.

Devices in the HPC family can directly address 64 Kbytes of external memory. This address range can be expanded to over 500 Kbytes without additional devices by using I/O pins to implement a simple bank switching technique.

This additional addressing range may be needed if the HPC implements the whole SMT function. The HPC development tools support this bank switching technique, allowing this low-cost microcontroller to handle the whole SMT function while minimizing the software development effort.

The performance of the system will not be affected by using this bank switching approach because many of the SMT functions are never performed simultaneously. The HPC could, for example, run the Physical Connection Management (PCM) from one memory bank, then switch to the bank containing the frame-based management functions at its leisure.

5.0 CONTROL BUS INTERFACE

The FDDI chipset from National Semiconductor provides the PHY and MAC services as detailed in the FDDI Standard. The chipset does not provide the Station Management (SMT) services, but does provide access to all the necessary data through a large array of 8-bit registers located onboard the PLAYER, BMAC, and BSI devices. The interface to these registers is via the Control Bus defined in the data sheet for the BMAC Device (Media Access Controller). The interface consists of an 8-bit address bus, 8-bit data bus and several control lines. The control lines consist of a read/write signal, a chip enable signal and an acknowledge signal. There is also an interrupt signal and a parity bit, which for this application, has been disabled. The interrupt signal and the acknowledge signal are open drain signals and can be wire-ORed.

A transfer cycle on the bus is started when the processor drives the Chip Enable ($\overline{CE}$) signal low. Within 20 ns, the data (write cycle only), address and read/write signals must all be valid. The device being accessed will respond by driving the Acknowledge ($\overline{ACK}$) signal low when data is valid (read cycle) or when the data has been clocked in (write cycle). The processor can now end the transfer by driving $\overline{CE}$ high and the device will complete the cycle by driving $\overline{ACK}$ TRI-STATE®.

The HPC provides a multiplexed 16 bit bus for interfacing to external memory. As only 8 bits are required for the Control Bus, the interface can be achieved with minimal components (see *Figure 2*). The multiplexed address is latched by the flow-through latch, U3. The data bus is buffered by the bi-directional buffer, U2, which is enabled whenever either read or write signals is asserted by the HPC. The direction is controlled by the Write (WR) signal. Two chip enables are provided (PCE and BCE) by decoding the read, write and upper address bits. The chip enables are delayed until the next Clock (CK2) falling edge so that during a write cycle, the data is available within 20 ns of the chip enable. The Ready (RDY) signal forces the HPC to insert wait states until an $\overline{ACK}$ is received from the Control Bus. (See *Figures 3* and *4* for interface waveforms.)

No polling of the Control Bus is required as the interrupt signals for each device are brought into the HPC separately. A simple host interface is provided consisting of two interrupt signals and two eight bit ports, one for read and one for write.

Device U1 is a GAL16V8 (a programmable logic device) and performs all of the logic functions required to generate the control signals used by this system. The programming of this device using the ABEL language is straightforward, as shown by *Figure 5*.

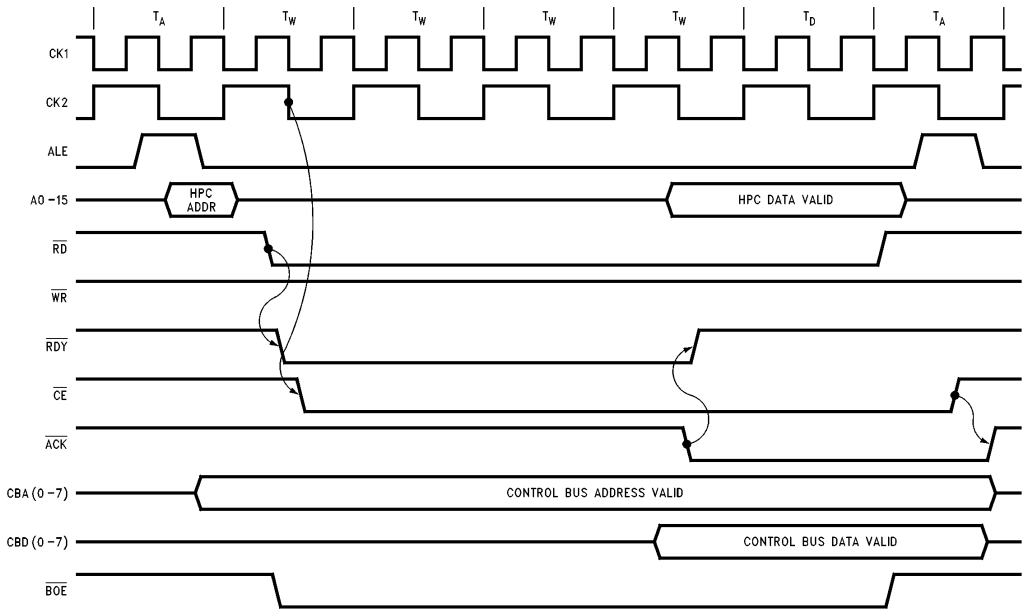

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FIGURE 3. Control Bus Interface READ Cycle

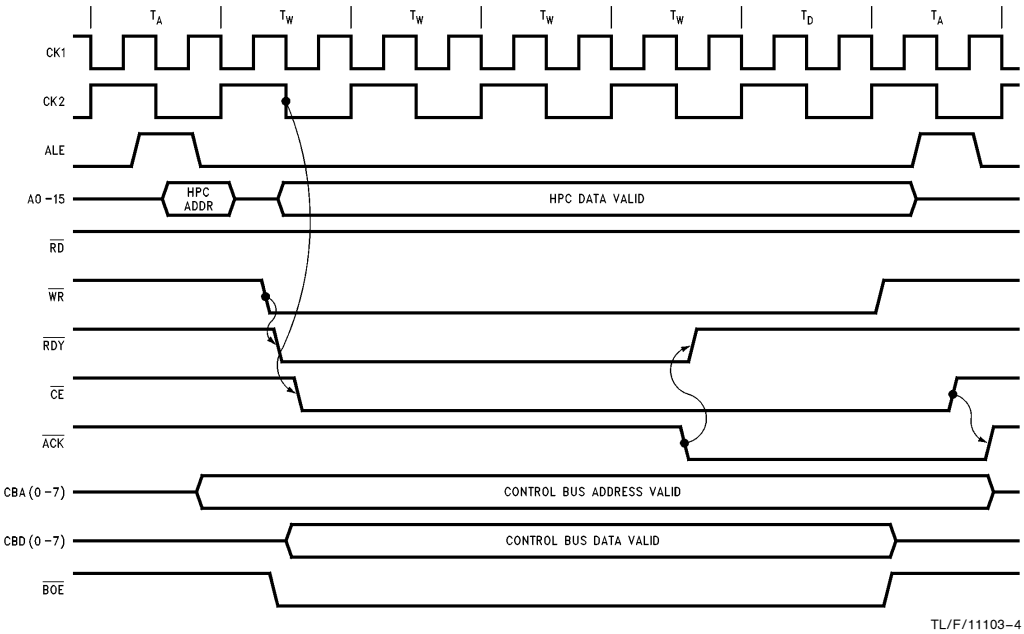

FIGURE 4. Control Bus Interface WRITE Cycle

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Title 'HPC to C Bus Interface
Simon Stanley                    National Semiconductor 12 Dec. 1990

U01                              device 'GAL16V8';
CK2,WR,RD,ACK                    pin 2,3,4,8;
A15,A14,A13                      pin 5,6,7;
RDY,NCK2,PCE,BCE, BSICE, BOE     pin 18,19,16,17,14,15;
Address = [A15,A14,A13,x,x,x,x,x,x,x,x,x,x,x,x,x];

equations
!PCE := (!RD# !WR) & (Address >= h8000) & (Address <= h9FFF);
!BCE := (!RD# !WR) & (Address >= hA000) & (Address <= hBFFF);
RDY = (WR & RD)# !ACK;
!BOE = !WR# !RD;
NCK2 = !CK2;
```

FIGURE 5. ABEL Source File for HPC FDDI Interface PAL

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