LM78S40 Switching Voltage Regulator Applications

National Semiconductor
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CONTENTS

INTRODUCTION

In modern electronic systems, voltage regulation is a basic function required by the system for optimal performance. The regulator provides a constant output voltage irrespective of changes in line voltage, load requirements, or ambient temperature.

For years, monolithic regulators have simplified power-supply design by reducing design complexity, improving reliability, and increasing the ease of maintenance. In the past, monolithic regulator systems have been dominated by linear regulators because of relatively low cost, low external component count, excellent performance, and high reliability. However, limitations to applicability and performance of linear regulators can force the user to other more complex regulator systems, such as the switching regulator.

Because of improvements in components made especially for them, switching-regulated power supplies have proliferated during the past few years. The emergence of inexpensive, high-speed switching power transistors, low-loss ferrites for inductor cores, and low-cost LSI circuits containing all necessary control circuitry has significantly expanded the range of switching regulator application.

This application note describes a new integrated subsystem that contains the control circuitry, as well as the switching elements, required for constructing switching regulator systems (*Figure 1*). The principle of operation is discussed, a complete system description provided, and the analysis and design of the basic configurations developed. Additional information concerning selection of external switching elements and design of the inductor is provided.

PRINCIPLE OF OPERATION

A D.C. power supply is usually regulated by some type of feedback circuit that senses any change in the D.C. output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

In a monolithic regulator, the output voltage is sampled and a high-gain differential amplifier compares a portion of this voltage with a reference voltage. The output of the amplifier is then used to modulate the control element, a transistor, by varying its operating point within the linear region or between the two operating extremes, cutoff and saturation. When the pass transistor is operated at a point between cutoff and saturation, the regulator circuit is referred to as *linear* voltage regulator. When the pass transistor is operated only at cutoff or at saturation, the circuit is referred to as a *switching* regulator.

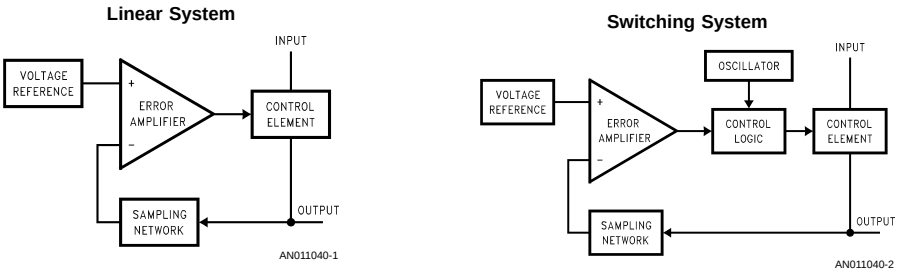


FIGURE 1. Regulator System Block Diagrams

One advantage of the switching regulator over the more conventional linear regulator is greater efficiency, since cutoff and saturation modes are the two most efficient modes of operation. In the cutoff mode, there is a large voltage across the transistor but little current through it; in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, most of the input power is transferred to the output, and efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

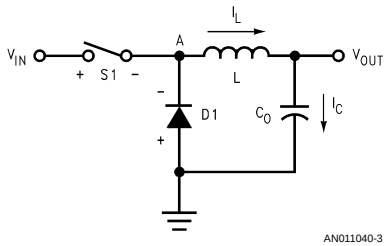
Besides high efficiency operation, another advantage of the switching regulator is increased application flexibility offered by output voltages that are less than, greater than, or of opposite polarity to the input voltage. *Figure 2* illustrates these three basic operating modes.

ARCHITECTURE

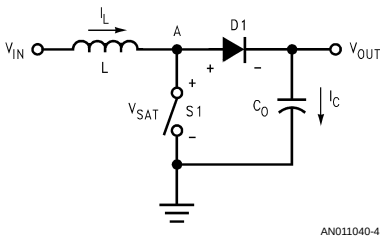
Each of the fundamental operating modes is built from the same set of functional blocks (*Figure 3*). Additional functions are required for control and protection, but again, these func-

tional blocks are common to each of the operational modes. The different modes are obtained by proper arrangement of these basic blocks.

Step-Down Configuration



Step-Up Configuration



Inverting Configuration

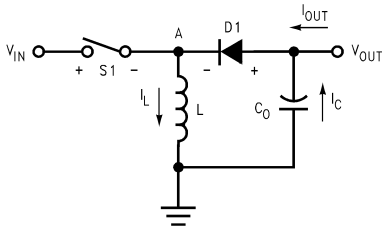


FIGURE 2. Basic Operating Modes

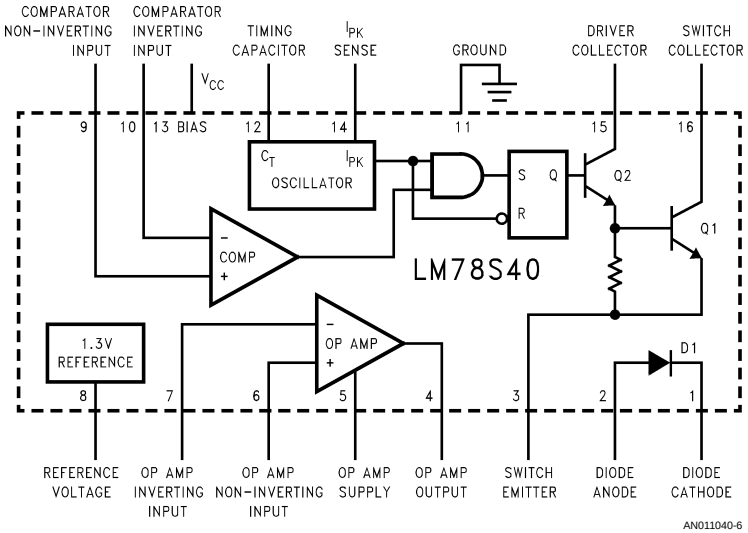


FIGURE 3. Functional Block Diagram

For maximum design flexibility and minimum external part count, the LM78S40 was designed to include all of the fundamental building blocks in an uncommitted arrangement. This provides for a simple, cost-effective design of any switching regulator mode.

The functional blocks of the regulator, illustrated in *Figure 3*, are:

- Current-controlled oscillator
- Temperature-compensated current-limiting circuit
- Temperature-compensated voltage reference
- High-gain differential comparator
- Power switching circuit
- High-gain amplifier

The current-controlled oscillator generates the gating signals used to control the on/off condition of the transistor power switch. The oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to

100 kHz. Most applications require an oscillator frequency from 20 kHz to 30 kHz. The oscillator duty cycle (t_{on}/t_{off}) is internally fixed at 6:1, but may be modified by the current-limiting circuit.

The temperature-compensated, current-limiting circuitry senses the switching transistor current across an external resistor and may modify the oscillator on-time, which in turn limits the peak current. This provides protection for the switching transistor and power diode. The nominal activation voltage is 300 mV, and the peak current can be programmed by a single resistor R_{SC}.

A 1.3V temperature-compensated, band-gap voltage source provides a stable reference to which the sampled portion of the output is compared. The reference is capable of providing up to 10 mA of current without an external pass transistor.

A high-gain ifferential comparator with a common-mode input range extending from ground to 1.5V less than V_{CC} is used to inhibit the basic gating signal generated by the oscillator turning on the transistor switch when the output voltage is too high.

The transistor switch, in a Darlington configuration with the collectors and emitter brought out externally for maximum design flexibility, is capable of handling up to 1.5A peak current and up to 40V collector-emitter voltage. The power switching diode is rated for the same current and voltage capabilities as the transistor switch; both have switching times that are normally 300 ns–500 ns.

Although not required by the basic operating modes, an independent operational amplifier has been included to increase flexibility. The characteristics of this amplifier are similar to the LM741, except that a power output stage has been provided, capable of sourcing up to 150 mA and sinking 35 mA. The input has also been modified to include ground as part of the common-mode range. This amplifier may be connected to provide series pass regulation or a second output voltage, or configured to provide special functions for some of the more advanced applications.

The switching regulator can be operated over a wide range of power conditions, from battery power to high-voltage, high-current supplies. Low voltage operation down to 2.4V and low standby current, less than 2.5 mA at 5V, make it ideal for battery-powered systems. On the other end, high-voltage capability, up to 40V, and high-current capability, up to 1.5A peak current, offer an operating range unmatched by other switching systems.

ANALYSIS — STEP-DOWN OPERATION

Figure 2 illustrates the basic configuration for a step-down switching voltage regulator system. The waveforms for this system are shown in *Figure 4*.

Assume, for analysis, that the following condition is true: before the switch is turned on,

$$i_L = 0$$

When switch S1 is closed, the voltage at point A becomes:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor i_L is increasing at a rate equal to:

$$\frac{di}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT} - V_{OUT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. Assuming that the output voltage over a full cycle does not change significantly, this rate may be considered to be constant, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. Since the inductor current cannot change instantaneously, it generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = -V_D$$

where V_D is the forward voltage of the diode.

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D + V_{OUT}}{L}\right)$$

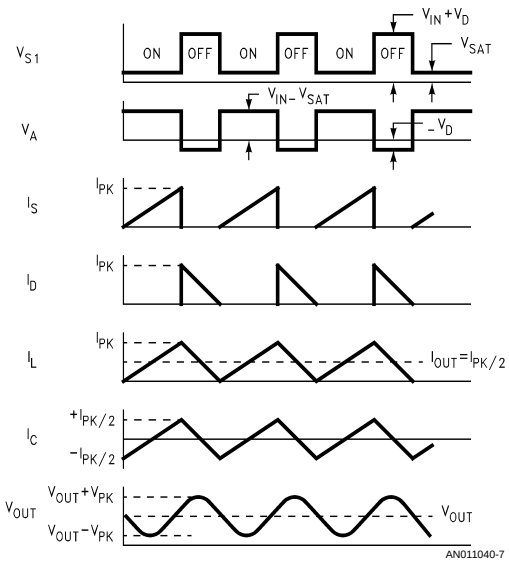


FIGURE 4. Waveforms for Step-Down Mode

The current through the inductor at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D + V_{OUT}}{L}\right) t$$

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D + V_{OUT}}{L}\right) t_{off}$$

which results in the following relationship between t_{on} and t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

In the above analysis, a number of assumptions were made. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 4* (i_L waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{on} + \left(\frac{I_{pk}}{2}\right) t_{off} = I_{OUT}\,(t_{on} + t_{off}),$$

$$\text{or } I_{pk} = 2\,I_{OUT}$$

For the average output voltage to remain constant, the average current through the inductor must equal the output current.

It was also assumed that the change (ripple) in the output voltage was small in comparison to the output voltage. The ripple voltage can be calculated from a knowledge of switching times, peak current and output capacitor size. *Figure 4* (i_C waveform) shows that:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{\frac{1}{2}\left(t_{on}\frac{I_{pk}}{4} + t_{off}\frac{I_{pk}}{4}\right)}{C_O} = \frac{I_{pk}\,(t_{on}/t_{off})}{8\,C_O}$$

The ripple voltage will be increased by the product of the output capacitor's equivalent series resistance (ESR) and i_C (though the two ripple terms do not directly add). Using large-value, low-ESR capacitors will minimize the ripple voltage, so the previous analysis will remain valid.

To calculate the efficiency of the system, n:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\,V_{IN}$$

The average input current can be calculated from the i_S waveform of *Figure 4*:

$$I_{IN(avg)} = \frac{t_{on}\left(\frac{I_{pk}}{2}\right)}{t_{on} + t_{off}} = I_{OUT}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

The output power is given by:

$$P_{OUT} = I_{OUT}\,V_{OUT}$$

Combining the above equations gives an expression for efficiency:

$$n = \left(\frac{V_{OUT}}{V_{OUT} + V_D}\right)\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right)$$

As the forward drops in the diode and switch decrease, the efficiency of the system is improved. With variations in input voltage, the efficiency remains relatively constant.

The above calculation for efficiency did not take into account quiescent power dissipation, which decreases efficiency at low current levels when the average input current is of the same magnitude as the quiescent current. It also did not take into account switching losses in the switch and diode or losses in the inductor that tend to reduce efficiency. It does, however, give a good approximation for efficiency, providing a close match with what is asured for the system.

ANALYSIS — STEP-UP OPERATION

Figure 2 illustrates the basic configuration for step-up switching voltage regulator system. The waveforms for this system are shown in *Figure 5*.

To analyze, first assume that just prior to closing S1:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A, which is also the voltage across the switch, is:

$$V_A = V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor i_L is increasing at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch remains closed and the inductor does not saturate. This rate will be constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{PK} = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. The inductor generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = V_{OUT} + V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\frac{V_{OUT} + V_D - V_{IN}}{L}$$

The current through the inductor and diode at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t$$

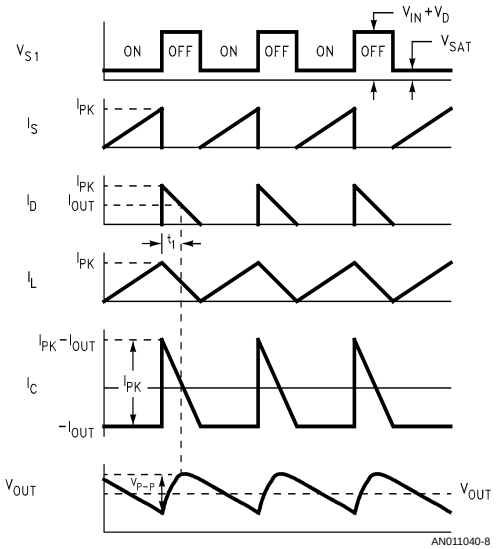


FIGURE 5. Waveforms for Step-Up Mode

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t_{off}$$

Thus, the relationship between t_{on} and t_{off} is given by:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$$

The above analysis assumes that the output voltage remains relatively constant. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 5* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$$

Also for the average output voltage to remain constant, the average current through the diode must equal the output current. The ripple voltage can be calculated using *Figure 5* (i_D waveform) where:

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}}\right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its minimum value to its maximum value. Therefore:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\frac{I_{pk} + I_{OUT}}{2}\right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P\text{-}P} = \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}} \left(\frac{t_{off}}{C_O}\right)$$

As with the step-down regulator, this ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\, V_{IN}$$

The average input current can be calculated from the i_L waveform of *Figure 5*:

$$I_{IN(avg)} = \frac{I_{pk}}{2}$$

The output power is given by:

$$P_{OUT} = I_{OUT}\, V_{OUT}$$

Combining and simplifying the above equations gives an expression for efficiency:

$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{OUT} + V_D - V_{SAT}}\right)$$

As the forward drops in the diode and switch are reduced, the efficiency of the system improves.

The above calculation did not take into account quiescent power dissipation or switching losses, which will reduce efficiency from the calculated value; it does, however, give a good approximation for efficiency.

ANALYSIS — INVERTING OPERATION

Figure 2 illustrates the basic configuration for an inverting regulator system. The waveforms for this system are shown in *Figure 6*.

To analyze, assume that the following condition is true just prior to turning on the switch:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A is:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch. At this time, diode D1 is reverse biased and the current through the inductor increases at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. This rate is constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1 is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened and the inductor generates a voltage that forward biases D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A \text{ s; } V_{OUT} - V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D - V_{OUT}}{L}\right)$$

The current through the inductor and diode at any given instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D - V_{OUT}}{L}\right) t$$

Assuming that the current through the inductor reaches zero after a time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D - V_{OUT}}{L}\right) t_{off}$$

Analysis shows the relationship between t_{on} and t_{off} to be:

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

The previous analysis assumes that the output voltage remains relatively constant. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 6* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}}\right)$$

For average output voltage to remain constant, the average current through the diode must equal the output current.

The ripple voltage can be calculated using *Figure 6* (i_D waveform):

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}}\right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its most positive value to its most negative value; therefore:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\frac{I_{pk} + I_{OUT}}{2}\right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P\text{-}P} = \frac{t_{off}}{C_O} \times \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}}$$

This ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT}\, V_{OUT}}{I_{IN}\, V_{IN}}$$

Average input current can be calculated from *Figure 6* (i_S waveform):

$$I_{IN(avg)} = \frac{I_{pk}}{2}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

Combining and simplifying the previous equations gives an expression for the system efficiency:

$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}}\left(\frac{|V_{OUT}|}{V_D + |V_{OUT}|}\right)$$

Again, as the forward drops in the diode and switch are reduced, the efficiency of the system improves. Also, since switching losses and quiescent current power dissipation are not included in the calculations, efficiency will be somewhat lower than predicted by the above equation.

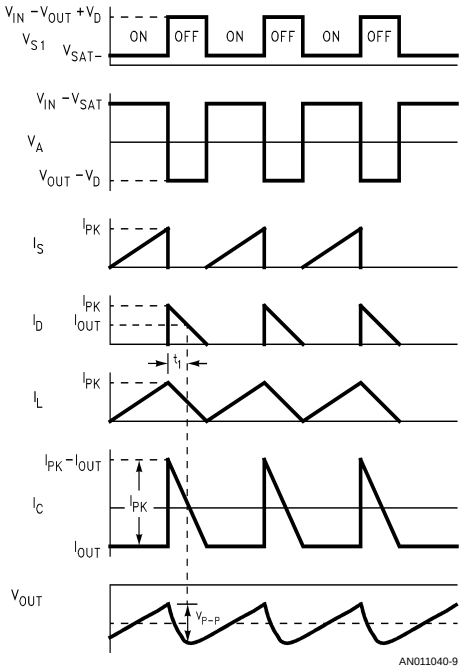


FIGURE 6. Voltage Inverter Waveforms

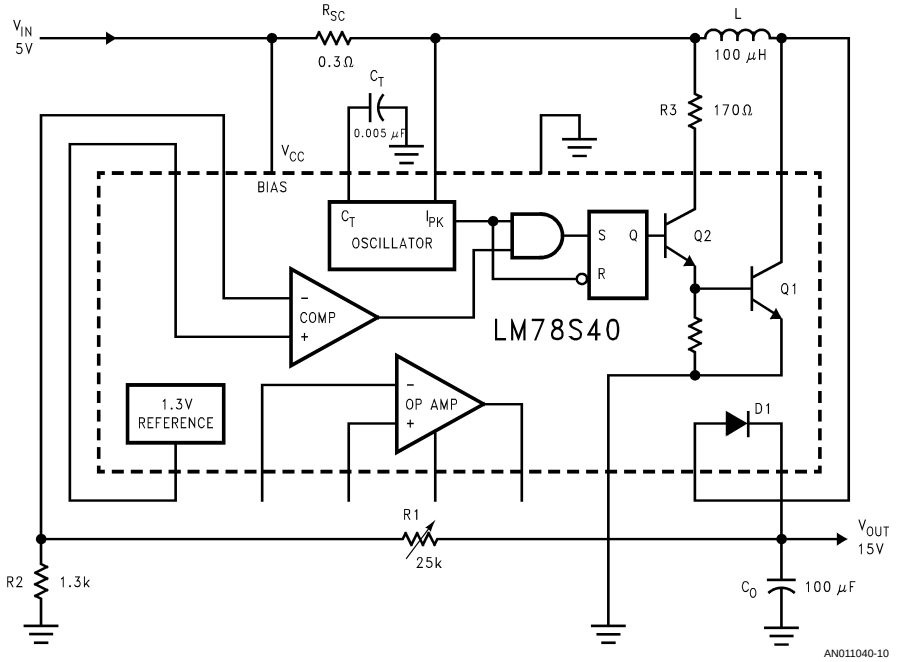


FIGURE 7. Step-Up Voltage Regulator

DESIGN — STEP-UP REGULATOR

A schematic of the basic step-up regulator is shown in *Figure 7*.

Conditions:

V_{IN} = 5V I_{OUT} = 150 mA

V_{OUT} = 15V $V_{RIPPLE} \leq 1\%$

Calculations:

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

$$I_{pk} = 2\,(0.15) \left(\frac{15 + 1.25 - 0.45}{5 - 0.45} \right) \approx 1\ A$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.3\Omega$$

To calculate the ratio of t_{on}/t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}} = \frac{15 + 1.25 - 5}{5 - 0.45} \approx 1.9$$

$$t_{on} = 1.9\, t_{off}$$

At this point, a value is selected for t_{off}, which in turn defines t_{on}. In making the selection, two constraints must be considered. The first constraint comes from efforts to maintain high efficiency. Rise and fall times should be kept small in comparison to the total period ($t_{on} + t_{off}$) so that only a small portion of the total time is spent in the linear mode of operation, where losses are high. This can be achieved if both t_{on} and t_{off} are made greater than or equal to 10 μs.

The second constraint is due to the techniques used to reduce the effects of the switching mode of operation on external systems. Filtering requirements can be made less stringent by maintaining a high switching frequency, i.e., above 15 or 20 kHz. This condition can be met by specifying the total period, $t_{on} + t_{off}$, to be less than 50 μs.

Therefore, the two design constraints are:

$$t_{on} \geq 10\ \mu s;\ t_{off} \geq 10\ \mu s$$

$$(t_{on} + t_{off}) \leq 50\ \mu s$$

In some cases, both constraints cannot be met and some trade-offs will be necessary.

Following these constraints, value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

It is now possible to calculate values for the timing capacitor C_T and the inductor L.

The timing capacitor is related (by design) to the off-time by the equation:

$C_T = (45 \times 10^{-5})\, t_{off}$

$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500$ pF

Therefore, set C_T = 5000 pF, which results in:

$$t_{off} \approx 11\ \mu s \text{ and } t_{on} \approx 21\ \mu s$$

For the inductor

$$L = t_{off}\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right)$$

$$L = (11 \times 10^{-6})\left(\frac{15 + 1.25 - 5}{1}\right) \approx 96\ \mu H$$

The inductor may be designed, using the equations in Appendix A, or purchased. An inductor such as a Delevan 3443-48, rated at 100 µH, is close enough in value for this application.

The output capacitor C_O value can be calculated using the ripple requirement specified:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\ V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(21 + 11)\,10^{-6}}{(8)\,(150 \times 10^{-3})} \geq 26.6\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

to allow for the additional ripple voltage caused by the ESR of the capacitor.

The sampling network, R1 and R2, can be calculated as follows. Assume the sampling network current is 1 mA. Then:

$$R1 + R2 = 15\ k\Omega$$

$$R2 = (R1 + R2)\left(\frac{V_{REF}}{V_{OUT}}\right)$$

$$R2 = (15 \times 10^3)\,\frac{1.3}{15} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 25 kΩ pot that can be used for adjustments in the output voltage.

Note: Sampling current as low as 100 µA can be used without affecting the performance of the system.

R3 is selected to provide enough base drive for transistor Q1. Assume a forced β of 20:

$$I_{C2} \approx I_{B1} = \frac{I_{pk}}{\beta} = \frac{1}{20} = 50\ mA$$

$$R3 \approx \frac{V_{IN} - 1.3}{I_B} = \frac{10 - 1.3}{0.05} = 174\Omega$$

Let R3 = 170Ω.

Using Q1 and Q2 with the external resistor R3 makes it possible to reduce the total power dissipation and improve the efficiency of this system over a system using Q1 and Q2 tied together as the control element. Each application should be checked to see which configuration yields the best performance.

An optional capacitor can be placed at the input to reduce transients that may be fed back to the main supply. The capacitor value is normally in the range of 100 µF to 500 µF, bypassed by a 0.01 µF capacitor.

Applications with peak operating currents greater than 1.5A or higher than 40V require an external transistor and diode as shown in *Figure 8*. This circuit assumes a 15V input and a 70V output.

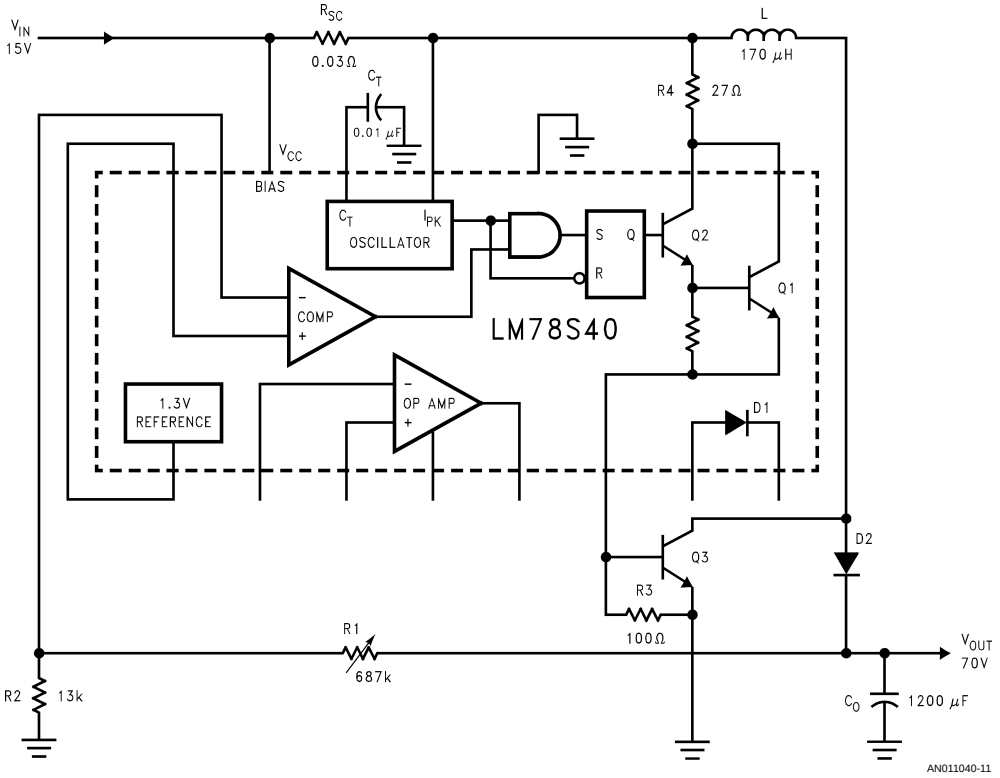


FIGURE 8. Switching Regulator with 15V Input, 70V Output

DESIGN — STEP-DOWN REGULATOR

A schematic of the basic step-down regulator is shown in *Figure 9*.

Conditions:

V_{IN} = 25V $I_{OUT(max)}$ = 500 mA

V_{OUT} = 10V V_{RIPPLE} < 1%

Calculations:

$I_{pk} = 2\ I_{OUT(max)}$

$I_{pk} = 2\ (0.5) = 1A$

Therefore:

$$R_{SC} = \frac{0.33}{I_{pk}} = 0.33\Omega$$

Next, calculate the ratio of t_{on} to t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{10 + 1.25}{25 - 1.1 - 10} \approx 0.8$$

$$t_{on} = 0.8\ t_{off}$$

Following design constraints previously discussed, a value is selected for t_{off}:

$$t_{off} = 22\ \mu s$$

$$t_{on} = 18.6\ \mu s$$

Then calculate C_T and L:

$$C_T = (45 \times 10^{-5})\ t_{off}$$

$$C_T = (45 \times 10^{-5})\ (22 \times 10^{-6}) \approx 0.1\ \mu F$$

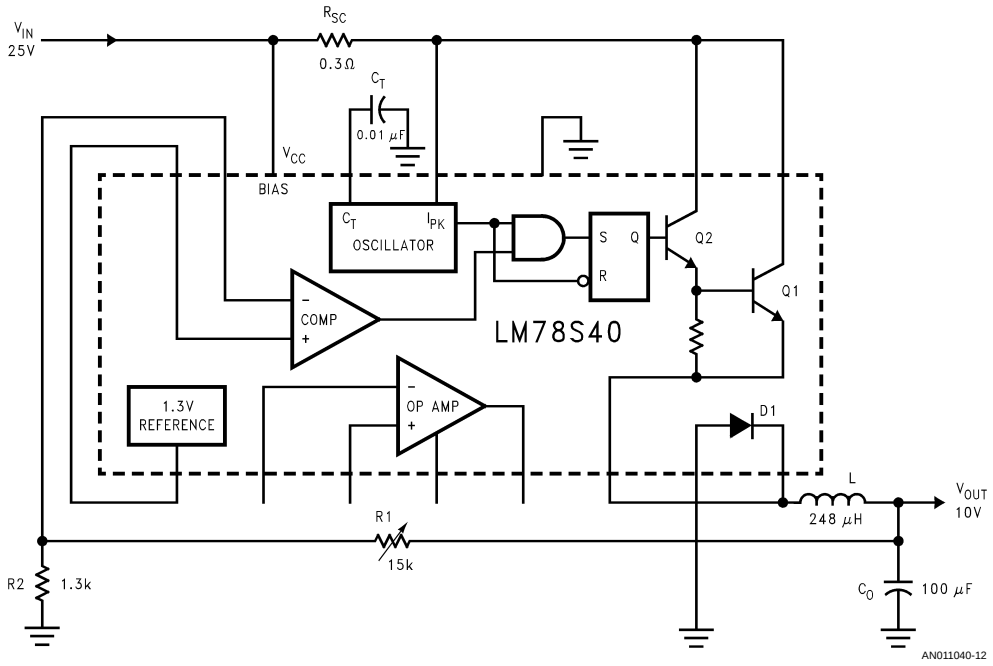


FIGURE 9. Step-Down Voltage Regulator

$$L = \left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$$

$$L = \frac{10 + 1.25}{1} (22 \times 10^{-6}) = 248\ \mu H$$

Output capacitor C_O can be calculated from ripple requirements:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(18.6 + 22)\,10^{-6}}{(8)\,(0.1)} = 50\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

Assuming that the sampling network current is 1 mA, then:

$$R1 + R2 = 10\ k\Omega$$

$$R2 = (R1 + R2)\frac{V_{REF}}{V_{OUT}} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 15 kΩ pot that can be used for adjustments in output voltage.

If $I_{pk} \geq 300$ mA, during the off-time when the diode is forward biased, the negative voltage generated at pin 1 causes a parasitic transistor to turn on, dissipating excess power. Replacing the internal diode with an external diode eliminates this condition and allows normal operation.

For applications with peak currents greater than 1A or voltages greater than 40V, an external transistor and diode are required, as shown in *Figure 10*, which assumes a 30V input and a 5V output at 5A.

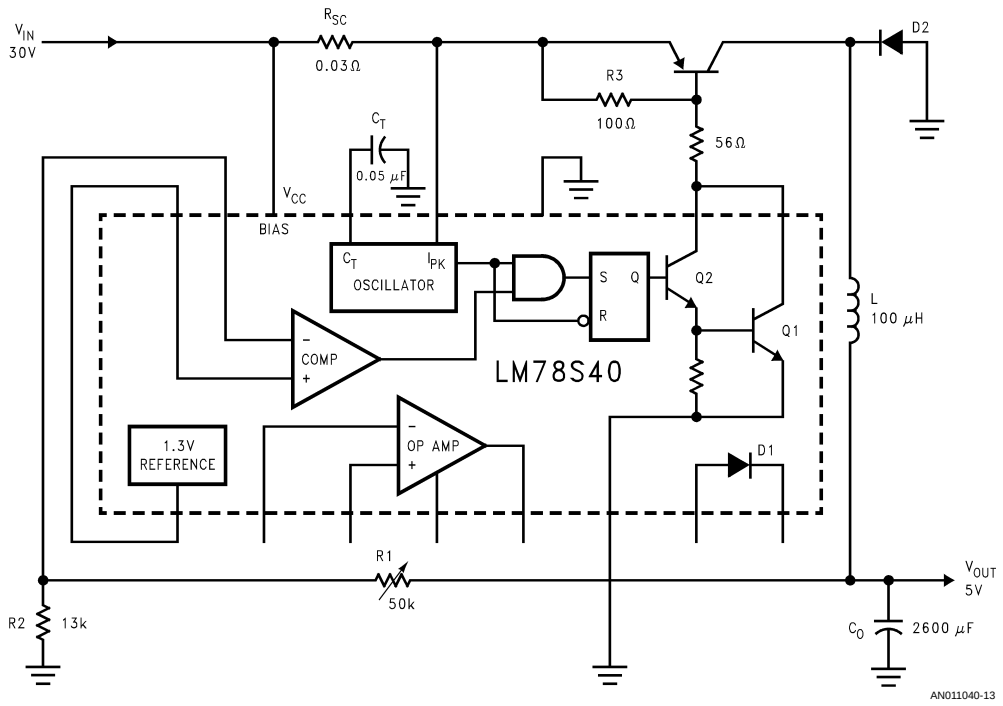


FIGURE 10. Modified Step-Down Regulator with 5A, 5V Output

DESIGN — INVERTING REGULATOR

A schematic of the basic inverting regulator is shown in *Figure 11*.

Conditions:

V_{IN} = 12V $I_{OUT(max)}$ = 500 mA

V_{OUT} = −15V $V_{RIPPLE} \leq 1\%$

Calculations:

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

For 2N6051 $V_{SAT} \leq 2V$

$$I_{pk} = 2\,(0.5) \left(\frac{12 + 1.25 + 15 - 2)}{12 - 2} \right) \cong 2.57$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.1\Omega$$

Calculating the ratio of t_{on} to t_{off},

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{1.25 + 15}{10 - 2} \approx 2$$

$$t_{on} = 2\, t_{off}$$

Following design constraints, a value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

Now, calculate C_T and L:

$C_T = (45 \times 10^{-5})\, t_{off}$

$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500$ pF

Setting C_T = 5000 pF makes $t_{off} \approx 11\ \mu s$ and $t_{on} \approx 22\ \mu s$.

$$L = \left(\frac{V_D - V_{OUT}}{I_{pk}} \right) t_{off}$$

$$L = \left(\frac{1.25 + 15}{2.57} \right) (11 \times 10^{-6}) \approx 70\ \mu H$$

The output capacitor C_O again is calculated:

$$C_O \geq \frac{(I_{pk} - I_O)^2\, t_{off}}{2\, I_{pk} \times V_{RIPPLE}}$$

$$C_O \geq \frac{(2.57 - 0.5)^2\, (11 \times 10^{-6})}{(2)\,(2.57)\,(0.1)} = 97\ \mu F$$

C_O is selected to be 200 μF.

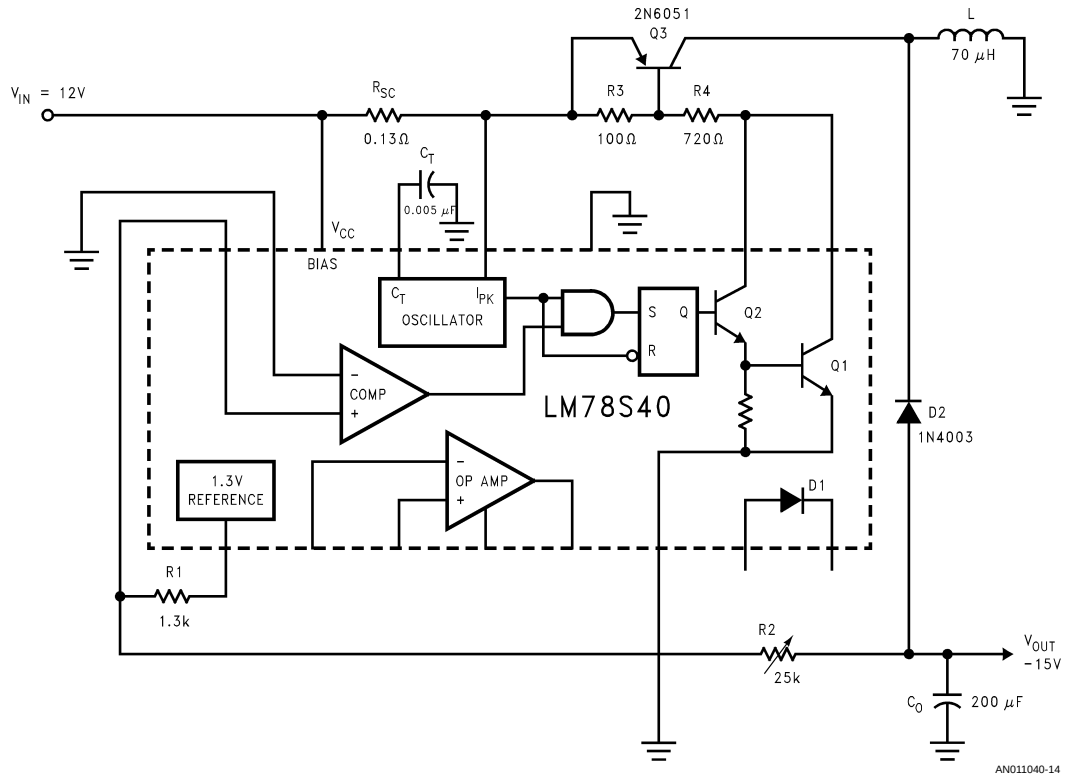


FIGURE 11. Inverting Regulator

The sampling network, R1 and R2, can easily be calculated. Assuming the sampling network current I_S is 1 mA:

$$R_1 = \frac{V_{REF}}{I_S} = 1.3\ k\Omega$$

$$R_2 = \frac{-V_{OUT}}{I_S} = 15\ k\Omega$$

Set R1 = 1.3 kΩ and use a 25 kΩ pot for R2 so that output voltage can be adjusted.

This application requires an external diode and transistor since the substrate of the or is referenced to ground and a negative voltage is present on the output. The external diode and transistor prevent the substrate diodes from a forward-biased condition. See Appendix B for selection of the diode and transistor.

R3 is provided for quick turn-off on the external transistor and is usually in the range of 100Ω to 300Ω. R4 can be calculated as follows:

$$R_4 \approx \frac{V_{IN} - V_{SAT} - V_T - V_{BE}}{I_{pk}/\beta}$$

where:

V_T = threshold voltage = 300 mV

V_{BE} = base emitter drop across the external transistor

$\beta \approx$ ¼ h_{FE} of the external transistor

If the 2N6051 is used, the value for R4 is:

$$R_4 = \frac{12 - 1.3 - 0.3 - 0.7}{(2.57/190)} \approx 720\Omega$$

Again, an optional capacitor can be placed at the input to reduce transients.

APPENDIX A
ANALYSIS AND DESIGN OF THE INDUCTOR

To select the proper core for a specific application, two factors must be considered.

The core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability LI^2SAT.

The window area for the core winding must permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable D.C. losses in the winding at maximum peak current. Each core has a specific dissipation capability LI^2 that will result in a specific power loss or temperature rise. This temperature rise plus the ambient temperature must not exceed the Curie temperature of the core.

The design of any magnetic circuit is based on certain equations for formulae. Equation 1 defines the value of inductance L in terms of basic core parameters and the total number of turns N wound on the core:

$$L = N^2 \times 0.4\pi\ \mu\ A_e\ \ell_e \times 10^{-5} \quad (1)$$

where:

μ= effective permeability of core

ℓ_e= effective magnetic path length (cm)

A_e= effective magnetic cross section (cm^2)

Equation 2 defines a compound parameter called the inductor index A_L:

$$A_L = 0.4\pi\ \mu A_e\ \ell_e \times 10\ (mH/1000\ turns) \quad (2)$$

Combining Equations 1 and 2 and multiplying by I^2 gives:

$$LI^2 = (NI)^2\ (A_L \times 10^{-6})\ (millijoules) \quad (3)$$

Any specific core has a maximum ampere-turn NI capability limited by magnetic saturation of the core material. The maximum LI^2SAT of the core can then be calculated from Equation 3 or, if the saturation flux density B_{SAT} is given, from Equation 4:

$$LI^2 = \frac{(B_{SAT})^2\ (A_e^2 \times 10^{-4})}{A_L}\ (millijoules) \quad (4)$$

The core selected for an application must have an LI^2SAT value greater than calculated to insure that the core does not saturate under maximum peak current conditions.

In switching regulator applications, power dissipation in the inductor is almost entirely due to D.C. losses in the winding. The dc resistance of the winding R_w can be calculated from Equation 5:

$$R_w = P(\ell_w/A_w)\ N \quad (5)$$

where

P= resistivity of wire (Ω/cm)

ℓ_w= length of turn (cm)

A_w= effective area of wire (cm^2)

Core geometry provides a certain window area A_c for the winding. The effective area A'_c is 0.5 A_c for toroids and 0.65 A_c for pot cores. Equation 6 relates the number of turns, area of wire, and effective window area of a fully wound core.

$$A_w = A'_c/N\ (cm^2) \quad (6)$$

By combining Equations 5 and 6 and multiplying each side by I^2, the power dissipation in the winding P_w can be calculated:

$$P_w = I^2R_w = I^2P\left(\frac{\ell_w}{A'_c}\right)N^2 \quad (7)$$

Substituting for N and rearranging:

$$LI^2 = P_w\left(\frac{A_L A'_c}{P\ell_w}\right) \times 10^{-6}\ (millijoules) \quad (8)$$

Equation 8 shows that the LI^2 capability is directly related to and limited by the maximum permissible power dissipation. One procedure for designing the inductor is as follows:

1. Calculate the inductance L and the peak current I_{pk} for the application. The required energy storage capability of the inductor $LI_{pk}2$ can now be defined.
2. Next, from Equation 3 or 4, calculate the maximum LI^2SAT capability of the selected core, where
$$LI^2SAT > LI_{pk}2$$
3. From Equation 1, calculate the number of turns N required for the specified inductance L, and finally, from Equation 7, the power dissipation P_w. P_w should be less than the maximum permissible power dissipation of the core.
4. If the power losses are unacceptable, a larger core or one with a higher permeability is required and steps 1 through 3 will have to be repeated.

Several design cycles are usually required to optimize the inductor design. With a little experience, educated guesses as to core material and size come close to requirements.

APPENDIX B
SELECTION OF SWITCHING COMPONENTS

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point; whereas in switching applications operation is fully on or fully off. Transistors must be selected and tested to withstand the unique stress caused by this mode of operation. Parameters such as current and voltage ratings, secondary breakdown ratings, power dissipation, saturation voltage and switching times critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage, including any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage $V_{CE(SAT)}$ and diode forward voltage V_D at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors. Transistor switching losses become significant when the combined rise t_r plus fall time t_f exceeds:

$$0.05\ (t_{on} + t_{off})$$

For 20 kHz operation, $t_r + t_f$ should be less than 2.5 μs for maximum efficiency. While transistor delay and storage times do not affect efficiency, delays in turn-on and turn-off can result in increased output voltage ripple. For optimal operation combined delay time t_d plus storage time t_s should be less than:

$$0.05\ (t_{on} + t_{off})$$

APPENDIX C
SELECTION OF OUTPUT FILTER CAPACITORS

In general, output capacitors used in switching regulators are large (>100 μF), must operate at high frequencies (>20 kHz), and require low ESR and ESL. An excellent trade-off between cost and performance is the solid-tantalum capacitor, constructed of sintered tantalum powder particles packed around a tantalum anode, which makes a rigid assembly or slug. Compared to aluminum electrolytic capacitors, solid-tantalum capacitors have higher CV product-per-unit volume, are more stable, and have hermetic seals to eliminate effects of humidity.

APPENDIX D
EMI

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = L\frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = 1/2\ LI^2$$

Interference and voltage spiking are easier to filter if the energy in the spikes is low and the components predominantly high frequency.

The following precautions will reduce EMI:

- Keep loop inductance to a minimum by utilizing appropriate layout and interconnect geometry.
- Keep loop area as small as possible and lead lengths small and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.
- Select an external diode that can hold peak recovery current as low as possible. This reduces the energy content of the voltage spikes.

APPENDIX E
DESIGN EQUATIONS

LM78S40 Design Formulae

Characteristic	Step Down	Step Up	Inverting
I_{pk}	$2\ I_{OUT(max)}$	$2\ I_{OUT(max)} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$	$2\ I_{OUT(max)} \left(\frac{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$
R_{SC}	$0.33\ I_{pk}$	$0.33\ I_{pk}$	$0.33\ I_{pk}$
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_{SAT}}$
L	$\left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$	$\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right) t_{off}$	$\left(\frac{\lvert V_{OUT}\rvert + V_D}{I_{pk}}\right) t_{off}$
t_{off}	$\frac{I_{pk} L}{V_{OUT} + V_D}$	$\frac{I_{pk} L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_{pk} L}{\lvert V_{OUT}\rvert + V_D}$
$C_{T\ (\mu F)}$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$
C_O	$\frac{I_{pk}\ (t_{on} + t_{off})}{8\ V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\ t_{off}}{2\ I_{pk}\ V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\ t_{off}}{2\ I_{pk}\ V_{RIPPLE}}$
Efficiency	$\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right) \frac{V_{OUT}}{V_{OUT} + V_D}$	$\frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{OUT} + V_D - V_S}\right)$	$\left(\frac{\lvert V_{OUT}\rvert}{V_D + \lvert V_{OUT}\rvert}\right)$
$I_{IN(avg)}$ (Max load condition)	$\frac{I_{pk}}{2} \left(\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} + V_D}\right)$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \left(\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}\right)$

Note 1: V_{SAT} — Saturation voltage of the switching element
V_D — Forward voltage of the flyback diode

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