Interfacing the DP8422A to an Asynchronous Port B in a Dual 68020 System

National Semiconductor
Application Note 617
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INTRODUCTION

This application note explains interfacing the DP8422A DRAM controller to two 68020 microprocessors that are running at the same frequency, but asynchronously to each other. This application note is a supplement to AN-539 (Interfacing the DP8420A/21A/22A to the 68020) and is intended to show synchronization logic and timing requirements for a Port B CPU that is running asynchronous to the DP8422A. It is assumed that the reader is already familiar with the 68020 access cycles and the DP8422A modes of operation.

DESIGN DESCRIPTION

This design shows all of the logic necessary to interface an asynchronous 20 MHz 68020 to the DP8422A Port B control inputs. This design is a worst case example and includes some logic that would not be needed in slower systems (i.e., 68000 @ 10 MHz). In our example, a Port B access begins when the asynchronous 68020 places a valid address on the address bus and asserts the address strobe, $\overline{AS}$. In order to synchronize this signal to the DP8422A, it is run through two DQ flip-flops, which are clocked by Port A's input clock. The first DQ is run by an inverted clock in order to reduce the synchronization delay time by ½T. Once $\overline{AREQB}$ is asserted, the access request is latched on the DP8422A and an access will start. If GRANTB is asserted, signaling Port B control of the access port, and a refresh is not in progress, the DP8422A will assert an access $\overline{RAS}$.

The transfer acknowledge signal, $\overline{ATACKB}$ is also asserted from $\overline{AREQB}$ asserting (or from the same edge of clock that starts $\overline{RAS}$ for a delayed access). $\overline{AREQB}$ also runs through two DQ flip-flops before being input as $\overline{DSACK}$ to the 68020B. These two flip-flops serve a dual purpose, one being to synchronize the $\overline{ATACKB}$ signal to the 68020B clock, and the other is to provide 1T of delay for the $\overline{ATACKB}$ signal.

Once $\overline{DSACK}$ is sampled as asserted by the 68020, $\overline{AS}$ is negated, signifying an end to the present access. $\overline{AS}$ negating is used to negate the $\overline{DSACK}$ input by presetting the two flip-flops connected to this input. This is done to guarantee that the 68020B $\overline{DSACK}$ signal is negated prior to the next access request being valid. The "Q" output that is connected to the $\overline{DSACK}$ input on the 68020 is also run through 1½T of delay (2DQ's) before it is used to preset the flip-flop that drives $\overline{AREQB}$. The preset is used to negate the $\overline{AREQB}$ signal and to hold it negated for the required $\overline{AREQB}$ negated pulse width as specified by the DP8422A. $\overline{AS}$ is also used to preset this signal so $\overline{AREQB}$ does not get asserted in instances where there are not back-to-back accesses. The 1½T delay is used so that the $\overline{AREQB}$ signal is negated after data is sampled by the 68020. In addition to the parameters calculated in AN-539, these additional parameters are included to show how the synchronizing logic still meets the necessary setup times required by the system (the "$" symbol refers to a DP8422A parameter, and the "#" symbol refers to a 68020 parameter).

$101 $\overline{AREQB}$ Asserted Setup to CLK High
(The DP8422A-25 needs 7 ns)
$= 1\ T_{CP} - t_{PHL}$ (74F74 DQ Flip-Flop)
$= 50$ ns $- 8$ ns
$= 42$ ns

#47a $\overline{DSACK}$ Asserted Setup Time
(68020 needs 5 ns)
$\frac{1}{2}\ T_{CP} - t_{PHL}$ (74F74)
25 ns $-$ 8 ns
17 ns

$\overline{AS}$ negated pulse width guarantees the DP8422A meets $\overline{AREQB}$ negated pulse width ($117) through the preset of DQ flip-flop which is connected to $\overline{AREQB}$ input.

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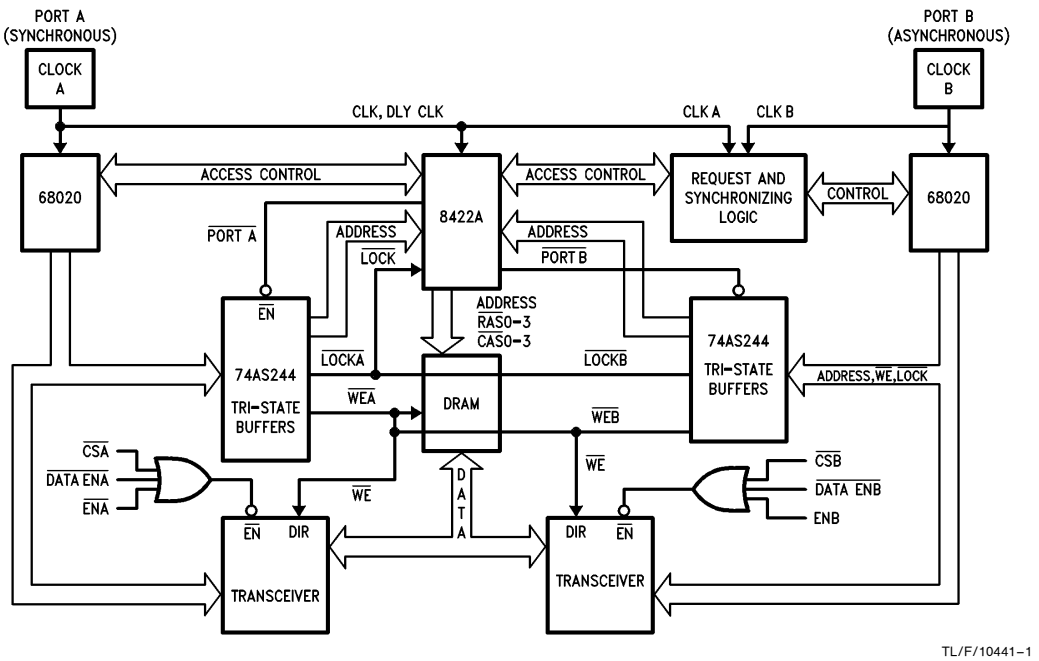

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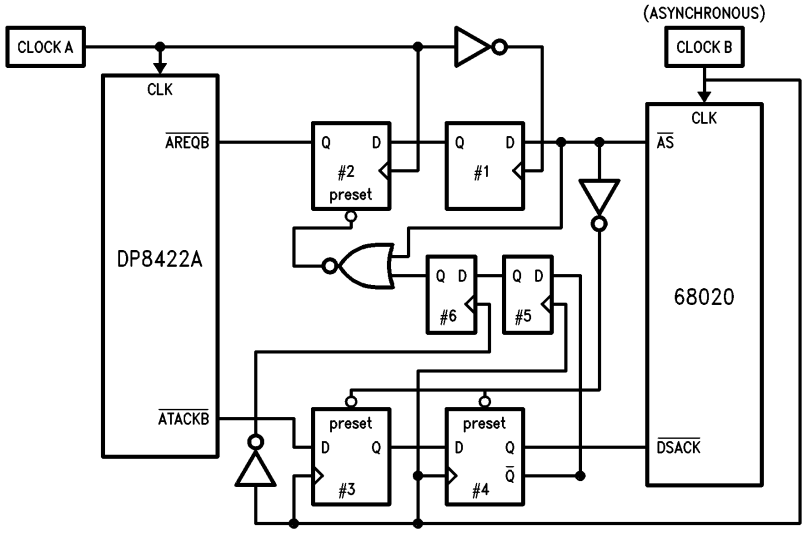
FIGURE 1. Dual Porting with the DP8422A with an Asynchronous Port B

Synchronizing Logic for a Dual 68020 Asynchronous System



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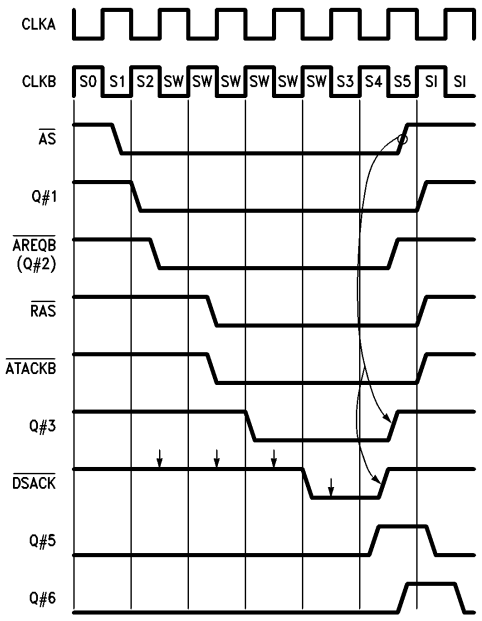
68020 Asynchronous Port B—Single Access



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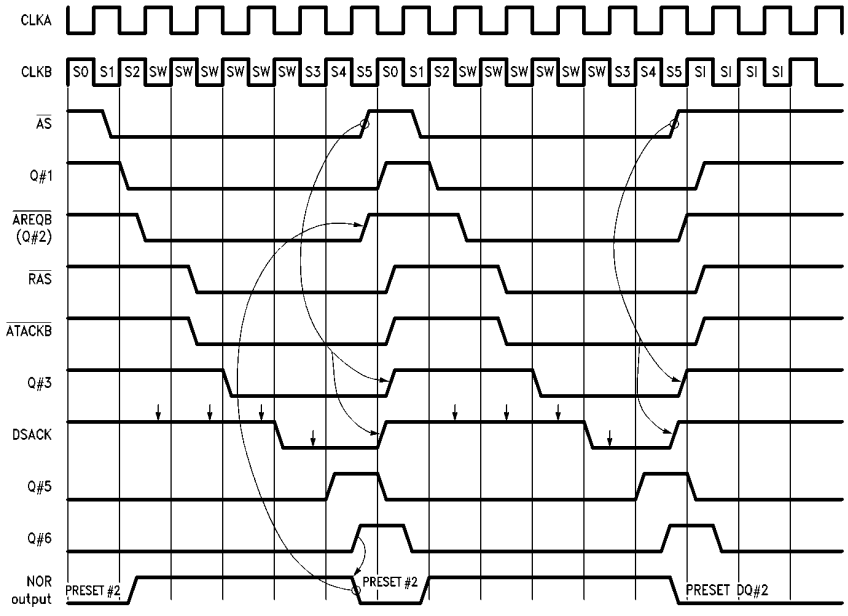
Back to Back Accesses where DQ Catches AS Negated Pulse in between Accesses



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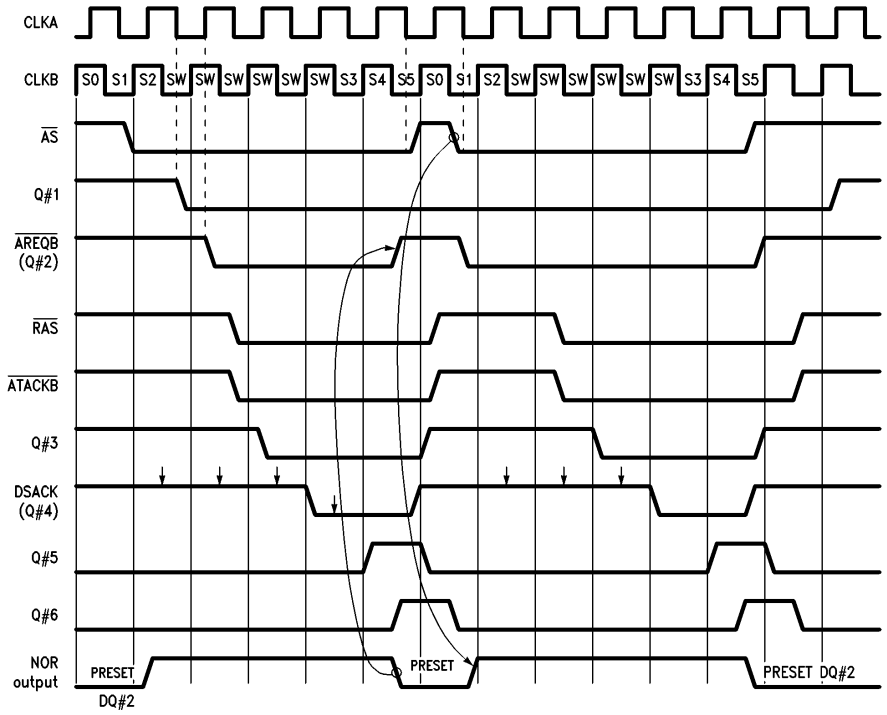
Back-to-Back Accesses where DQ # 1 Does Not Catch $\overline{AS}$ Negated Pulse in between Accesses



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