Realize the Speed of Asynchronous SCSI

National Semiconductor
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National Semiconductor's new SCSI Interface devices raise the standard of low cost SCSI.

National Semiconductor has two new low cost, high performance Small Computer Systems Interface (SCSI) devices; the DP5380 and DP8490. The DP5380 Asynchronous SCSI Interface (ASI) is pin and program compatible with the NMOS NCR5380 type device, but since it is manufactured in CMOS it offers speed and power advantages. The DP8490 Enhanced Asynchronous SCSI Interface (EASI) is pin compatible with the ASI, and program compatible until its enhanced mode is set. This mode offers features and architectural improvements which can greatly increase a system's throughput. However a major factor in favor of both devices is the improvement in their achievable data transfer rate.

Users who have replaced their NMOS 5380 type devices for National devices, in an existing application, have found improvements of between 10 and 15 percent in data transfer speeds. That is with no other changes to their application. For new designs, or performance upgrades, the gains possible can be much more dramatic.

In many applications the limiting factor in a data transfer is the DMA controller. This presented a problem to users i.e., ''How fast **can** the National devices transfer data?'' To determine this National designed an asynchronous DMA controller, using a programmable gate array, which can go as quickly as the SCSI device will allow it. **In these tests the National devices were up to 140% faster than the NCR5380 equivalent.**

SYSTEM OVERVIEW

A general SCSI application is shown in *Figure 1*. This shows the hardware required to interface a SCSI bus to a peripheral controller, without the devices to control the peripheral itself. The Central Processing Unit (CPU), the only ''intelligent'' device, controls all operations. It communicates with the SCSI bus through the EASI or ASI, which both support selection, reselection, arbitration and all other bus phases detailed in the ANS X3.131-1986 SCSI standard defined by the ANSI X3T9.2 committee. Since these devices can act as both target and initiator this could be the core of a peripheral controller or a host adaptor.

For optimum performance a DMA controller is used to transfer data between the SCSI device and memory. This memory is used as a cache for the final destination, which could be main system memory, a hard disk, floppy disk, printer, etc. By adding the appropriate interface the core shown in *Figure 1* can be adapted for the particular application.

TEST SYSTEM

To fully test the achievable DMA rate National built two boards of the form shown in *Figure 1*. The first board configures itself as an initiator, the second acts as a target. The initiator arbitrates for the SCSI bus, until successful, then selects the target and sends a Write command. This causes a DMA transfer from the initiator to the target.

The initiator arbitrates for the bus again, selects the target and sends a Read command. The data sent to the target is returned to the initiator, under DMA control, and checked. This process is constantly repeated, with the transmitted data varying between ''01,FF,00,01 etc.'' and ''FF,01,00,FF etc.'' This checks every data bit and varies the parity bit.

The two boards continually transmit blocks of data, alternating between Initiator Send/Target Receive and Initiator Receive/Target Send modes.

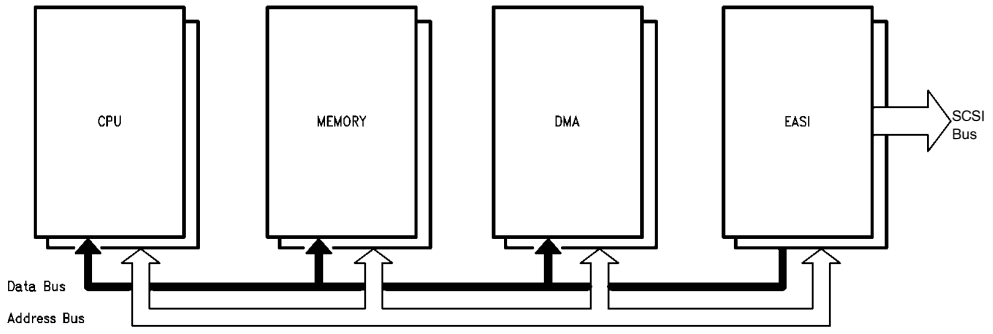

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FIGURE 1. Core of a SCSI Controller

RRD-B30M105/Printed in U. S. A.

TEST CIRCUIT

The two boards have identical circuitry, shown in *Figure 2*. The CPU is an NSC800™ 8-bit CMOS microprocessor, which requires an octal latch to demultiplex the address and data bus. The boards configuration, initiator or target, depends on the system software stored in the EPROM. Fast static RAM is required for the cache, CMOS RAM with an access time of 45 ns was selected. A PAL® is used to decode the chip selects. The SCSI controller can be either a 5380 or a DP8490.

The DMA controller was implemented in a Xilinx Programmable Gate Array. These devices offer a quick, easily adaptable method of prototyping. The design is entered as a schematic, then converted to the gate array format by a software package. Routing is largely automatic, but complex designs require a certain amount of interaction. In a speed critical design, such as the DMA controller, manual control of routing delays is vital.

The Xilinx device can automatically load its configuration from an EPROM on power-up. This could be the same EPROM that contains the boards software, but for simplicity during prototyping a separate device was used.

DMA DESIGN

The DMA controller required was highly application specific and could therefore be relatively simple. It basically consists of a counter, a register and control logic *(Figure 3)*. The counter is loaded with the start address of the DMA block and the register with the end address. On a subsequent DMA request the controller has to take control of the microprocessor bus and transfer data until the address in the counter equals the address in the end register.

The DMA is enabled by setting a bit in the control register. The other control bit determines whether the transfer is a memory read or a memory write.

Once enabled, a subsequent DMA request (DRQ) will cause the device to issue a bus request ($\overline{BRQ}$). When it receives a bus acknowledge ($\overline{BACK}$) from the processor it asserts the counter output onto the address bus and issues a DMA acknowledge ($\overline{DACK}$). The DMA controller also takes control of the I/O and memory read and write strobes. This device only operates in block mode, so $\overline{DACK}$ is asserted throughout the transfer. The SCSI device deasserts DRQ when $\overline{DACK}$ goes active. This is used to start the first transfer. Subsequent transfers are triggered by the throttle control, READY, going high.

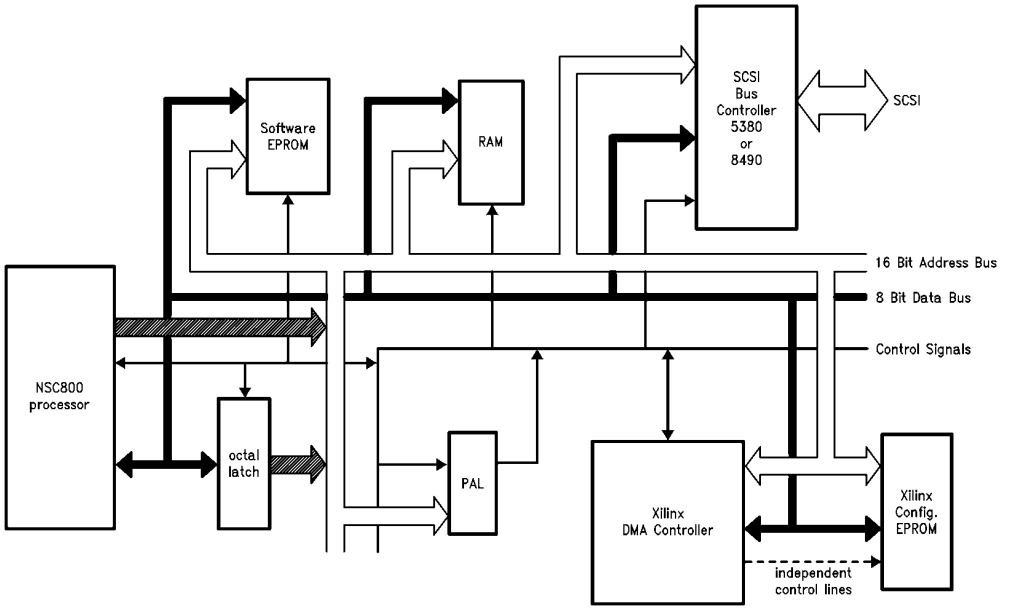

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FIGURE 2. Circuit of SCSI Test Board

For a memory read, $\overline{RD}$ is held active throughout the transfer and $\overline{IOW}$ is strobed. For a memory write, both $\overline{IOR}$ and $\overline{WR}$ are strobed. The basis of the control logic is shown in *Figure 4*.

Figure 5 shows the timings of the circuit in *Figure 4*. The I/O or memory strobe pulses low for the time difference between READY going high and the STROBEIN input causing CLOCK to go high. Thus the external delay line controls the strobe signals pulse widths. The back edge of CLOCK is used to increment the address counter.

The controller continues as in *Figure 5*, until the $\overline{EOP}$ (End of Process) signal is asserted. This is either asserted externally, to prematurely end a transfer, or by the DMA controller itself, once the current address counter equals the end address register.

The speed that the DMA controller transfers data is determined by the READY line. The SCSI controller deasserts READY after an $\overline{IOW}$ or $\overline{IOR}$, then asserts it when it is ready to transfer the next byte. This high transition triggers the next transfer of the DMA controller. Varying delay line time varies the $\overline{IOR}$, $\overline{IOW}$ and $\overline{WR}$ pulse widths, so different speeds of devices can be accommodated by this controller.

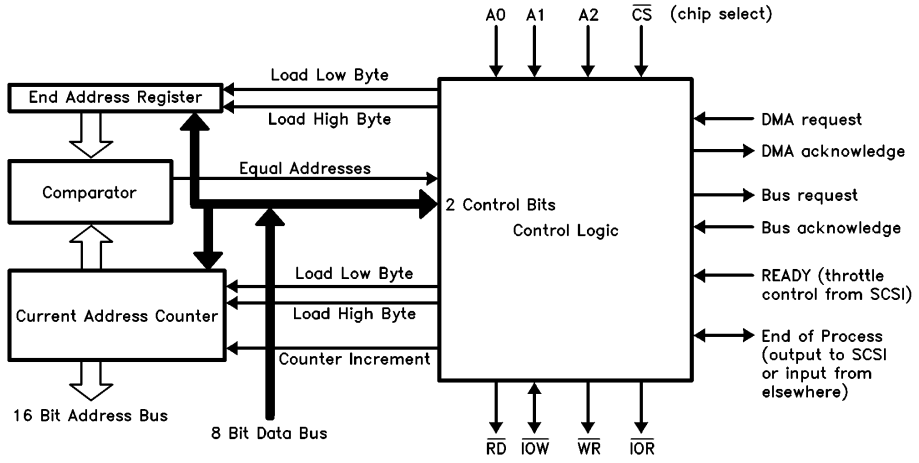

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FIGURE 3. Block Diagram of DMA Controller

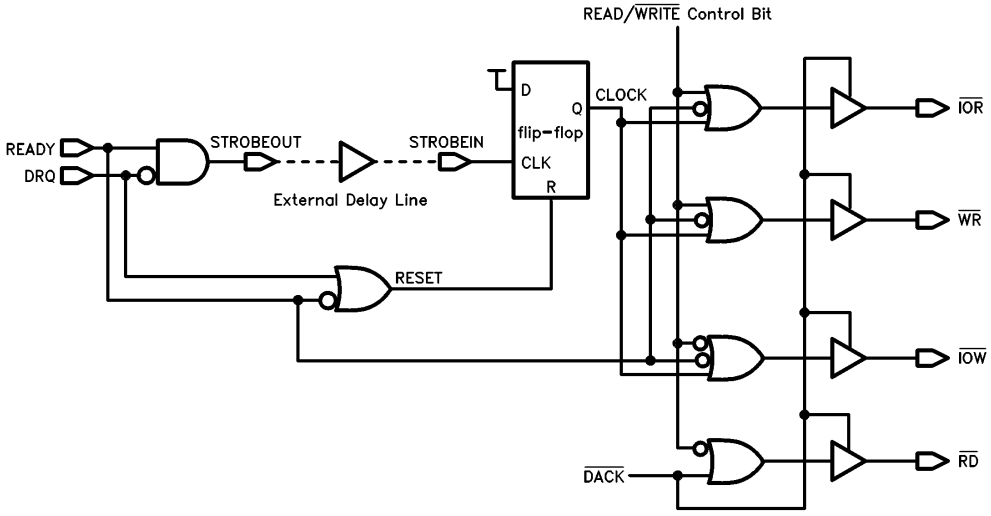

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FIGURE 4. DMA Control Logic

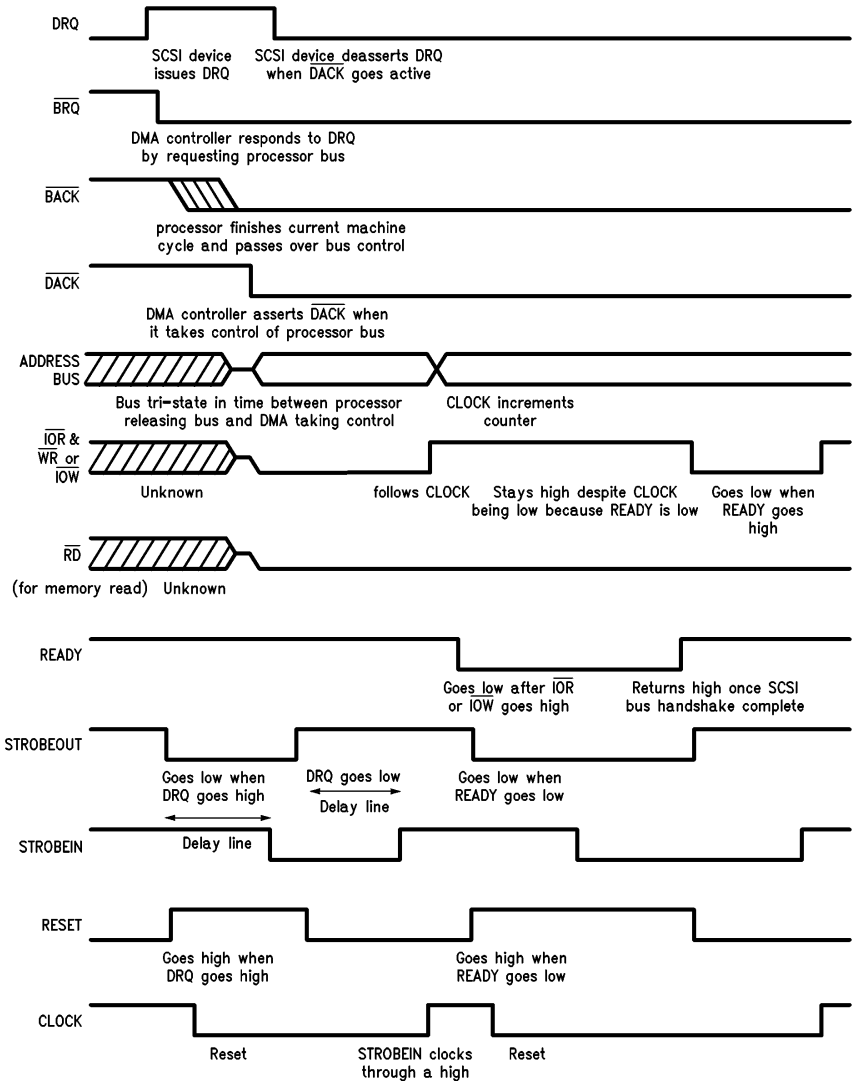

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FIGURE 5. DMA Controller Timings

BENCHMARKING

The system used for the benchmarking is shown in *Figure 6*.

The two boards were connected by three different lengths of cable; 50 cm, 3m and 6m (the maximum length of single ended cable allowed). 50-way STD IDC ribbon cable was used, wired as per SCSI specification with every second line grounded. All SCSI signal lines were terminated on both boards, with a 330Ω resistor to ground and a 220Ω resistor to V_{CC}.

A Hewlett Packard 16500A Logic Analysis system was used to monitor the control signals and measure the burst DMA rate. The 10 ns sampling rate gave sufficient accuracy to measure handshaking speeds which were all below 5 Mbytes/s.

The first byte of a transfer is delayed, as the initiator takes time to follow the phase set by the target. After this the DMA controller reaches its peak transfer rate, which is maintained until the end of the transfer. The frequency of the SCSI bus handshaking signal, REQ, was measured, to give the data transfer rate.

BENCHMARKED DEVICES

Initially it was planned to benchmark three manufacturers devices, that is National Semiconductor, NCR and Logic Devices.

However it was found that the Logic Devices part caused problems in the test board and would not function in conjunction with any other manufacturers device. The DMA controller uses DRQ to generate the first read and write strobes (see DMA Design section), but expects the signal to stay inactive for the rest of the transfer. The Logic Devices 5380 produces a spurious DRQ during a block mode transfer. This corrupts the read and write strobes produced by the DMA controller. The Logic Devices 5380 would not interface to other manufacturers devices because of its parity checking method. National and NCR only check the bus parity as they load their input data register. Logic Devices check parity when $\overline{ACK}$ is active, for Target Receive or when REQ is active for Initiator Receive. However, the National and NCR devices write the next byte of data before the $\overline{REQ}/\overline{ACK}$ handshake for the previous byte is complete. As parity is decoded through logic the data will be on the bus before the parity bit is valid. Logic Devices detect this as a parity error, which causes the transfer to be terminated.

The National and NCR devices were fully interchangeable.

Different Lengths of SCSI Bus

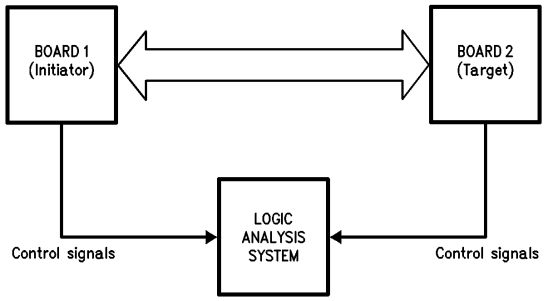

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FIGURE 6. Benchmarking System

BENCHMARK RESULTS

The transfer rate during a data phase was measured for a sample of National and NCR devices, over three lengths of cable. Measurements were made for Initiator Send/Target Receive mode and for Initiator Receive/Target Send mode. When a NCR device was used the delay line time was increased, to allow for its slower reading and writing times. *Figures 7a, b* and *c* show the results.

These tables show the dramatic speed advantages of the National device over NCR. The National device maintains a significant advantage over all three lengths of cable. It may appear that the NCR device maintains its speed better over longer lengths of cable, but only because the added propagation delays of the cable are a smaller percentage of the transfer time.

The Initiator Receive/Target Send mode is inherently faster, which makes the specification of one DMA rate for the device a highly debatable subject, even if the length of cable for the measurement is agreed. However, customers using the SCSI device for a disk application will appreciate the fact that this mode is faster, since approximately 80% of disk accesses are reads, while running most software.

Even if only one National device is used there is a significant improvement in performance, but to fully realize the potential of the SCSI interface two National devices are required. *Figure 8* shows just how much of an improvement this is.

a. 10cm Cable

Initiator / Target	Speed in Mbytes/second	
	National	NCR
National	**3.5** **4.9**	2.6 2.7
NCR	1.8 2.3	**1.5** **2.0**

b. 3m Cable

Initiator / Target	Speed in Mbytes/second	
	National	NCR
National	**3.1** **3.9**	2.3 2.5
NCR	1.6 2.2	**1.4** **1.9**

c. 6m Cable

Initiator / Target	Speed in Mbytes/second	
	National	NCR
National	**2.5** **3.0**	2.0 2.2
NCR	1.4 2.0	**1.3** **1.8**

Note: The upper value shows Initiator Send/Target Receive while the lower shows Initiator Receive/Target Send.

FIGURE 7. Measured DMA Transfer Rate

Percentage Improvement by Changing to National

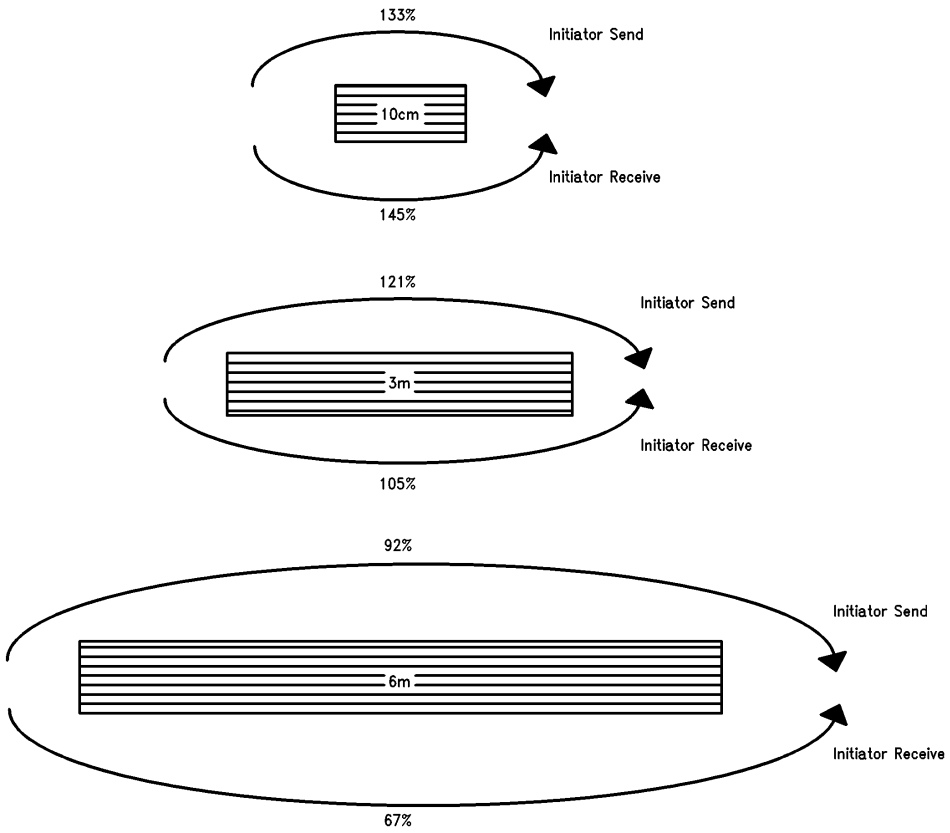

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FIGURE 8

CONCLUSIONS

The new asynchronous SCSI interface devices from National offer an instant improvement to old designs. By changing over to National devices the user can upgrade an existing SCSI interface by upwards of 10%, with no further effort. For greater performance improvements a fast DMA controller is required, at which point the asynchronous SCSI approaches synchronous SCSI speeds.

For new designs the DP8490 EASI is the ideal choice. In addition to the fast DMA transfer rate, this device offers architectural improvements which can greatly boost a systems throughput. In a 5380 the arbitration time is dead to the system, as the device must be polled to determine when this phase has started. By interrupt driving arbitration the DP8490 EASI frees many milliseconds, or even seconds, to be used at the system designers discretion. This time may be utilized for disk cacheing, overlapped seeks, printing etc. depending on the particular application. The entire interrupt structure has been revamped, making software for this device quicker to develop and quicker to run. To further ease software overheads the troublesome bugs of the 5380 have been fixed.

By improving the speed of data transfers, lowering the power consumption and offering new additions to a familiar SCSI interface device, National have rejuvenated asynchronous SCSI.

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