Using the TP3401/2/3 ISDN PBX Transceivers

National Semiconductor
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INTRODUCTION

The TP3401 Digital Adapter for Subscriber Loops (DASL) is a low-cost burst-mode transceiver for 144 kb/s full-duplex on single twisted-pair PBX and private network loops up to 1.8 km in length. Scrambled alternate mark inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. A multiplexed interface for two 64 kb/s "B" channels and one 16 kb/s "D" channel is provided. This application note, together with the TP3401 datasheet, provides the system designer with a thorough understanding of the device's operation as well as some sections that are useful to the terminal equipment designer. It covers the following topics:

1. Typical Application at the Terminal End
2. Activation/Deactivation Procedures
3. Repeater Mode Application
4. Transformer Design Guide
5. Surge Protection Methods at the Line Interface
6. Bit Error Rate Performance

1. TYPICAL APPLICATION AT THE TERMINAL END

a. System Description

For the purpose of this application note, a terminal which is designed to offer one PCM voice channel and one data channel will be discussed, although many other combinations can easily be configured.

As shown in *Figure 1*, the HPC16400 Microcontroller and TP3054/7 COMBO™ directly interface to DASL at the terminal end of the loop.

b. Main Controller HPC16400

The HPC16400 is a 16-bit highly integrated microcomputer which supports a wide range of communication application, this chip includes two HDLC channels, a DMA controller, programmable serial interface, UART and MICROWIRE/PLUS™ serial interface. This set of features makes the HPC16400 an ideal processor for running all the functions of an ISDN Terminal Adapter, TE or Telephone.

In a typical application as shown in *Figure 1*, one of the HDLC channels is dedicated to handle the LAPD protocol in the "D" channel, while the other provides packet-mode access to one of the "B" channels. The MICROWIRE/PLUS serial interface is used to transmit/receive the TP3401 control/status register byte for handling its activation/deactivation. The UART would serve as an RS232 interface running at any of the standard synchronous or asynchronous rates up to 128 kbaud. The DMA controller provides several register sets for packet RAM management with minimal CPU intervention, including "chaining" of successive packets.

c. COMBO TP3054 Interface Description

The TP3054 is a μ-law serial interface PCM Codec/Filter COMBO. When power is first applied, power-on reset circuitry initializes the chip and places it into a power-down state. All non-essential circuits are deactivated and the Dx, VFr0 output pins are put in high impedance states. To power-up the device a logical low level, which is controlled by an HPC16400 I/O pin, must be applied to the MCLKr/PDN pin. For synchronous operation, this application uses the same master clock and bit clock which come from the TP3401 for both the transmit and receive directions. In this mode, a clock must be applied to MCLKx/BCLKx pins and the MCLKr/PDN pin is used as a power-down control; also the BCLKr/CLKSEL pin is tied to ground for selecting master clock frequency 2.048 MHz. Both the FSr and FSx frame sync pulses come from the TP3401 for long frame sync operation.

The analog transmit input is an operational amplifier with provision for gain adjustment using two external resistors, R1 and R2. The analog receive output is added with side tone into the LM747 input, and the LM747 output drives the earphone.

d. Activation

The line signal detect output or hook switch, applied to the NMI pin, wakes up the HPC16400. After the HPC16400 wakes up, it starts to read DASL status register bits through MICROWIRE™ to decide which end is initiating the call. The state of the C0 bit indicates whether the far end or the near end is activating the call; C0 is one ($\overline{LSD} = 0$) for far-end activation and C0 is zero (off-hook) for near-end activation.

The HPC16400 powers up DASL by writing control register bit C6 = 1 through MICROWIRE. DASL starts sending a 2 kHz burst rate of scrambled 1s in the B and D channels to the line. Now HPC16400 is waiting for a MICROWIRE interrupt to check when DASL is in sync. If DASL status bit C1 changes to one (loop-in-sync), first the HPC16400 enables the HDLC 1 port which starts to handle the D channel at the Tx1 output pin, continuously sending FLAGs (01111110) to the far end and at Rx1 input pin looking for FLAGs. Then the HPC16400 powers up the COMBO for B1 channel communication and enables HDLC 2 port for B2 channel communication.

I/O port R3 is connected to $\overline{\text{on-hook}}$ signal as an input port. The HPC16400 polls this input port every 50 ms after the B1 channel is activated to monitor the hook-switch status. If the logic level of R3 pin changes from high to low, this means the terminal end disconnected the call by hook-switch during the B1 channel activation state, so the HPC16400 passes the B1 channel disconnection message to the network through the D channel. (See Section 2).

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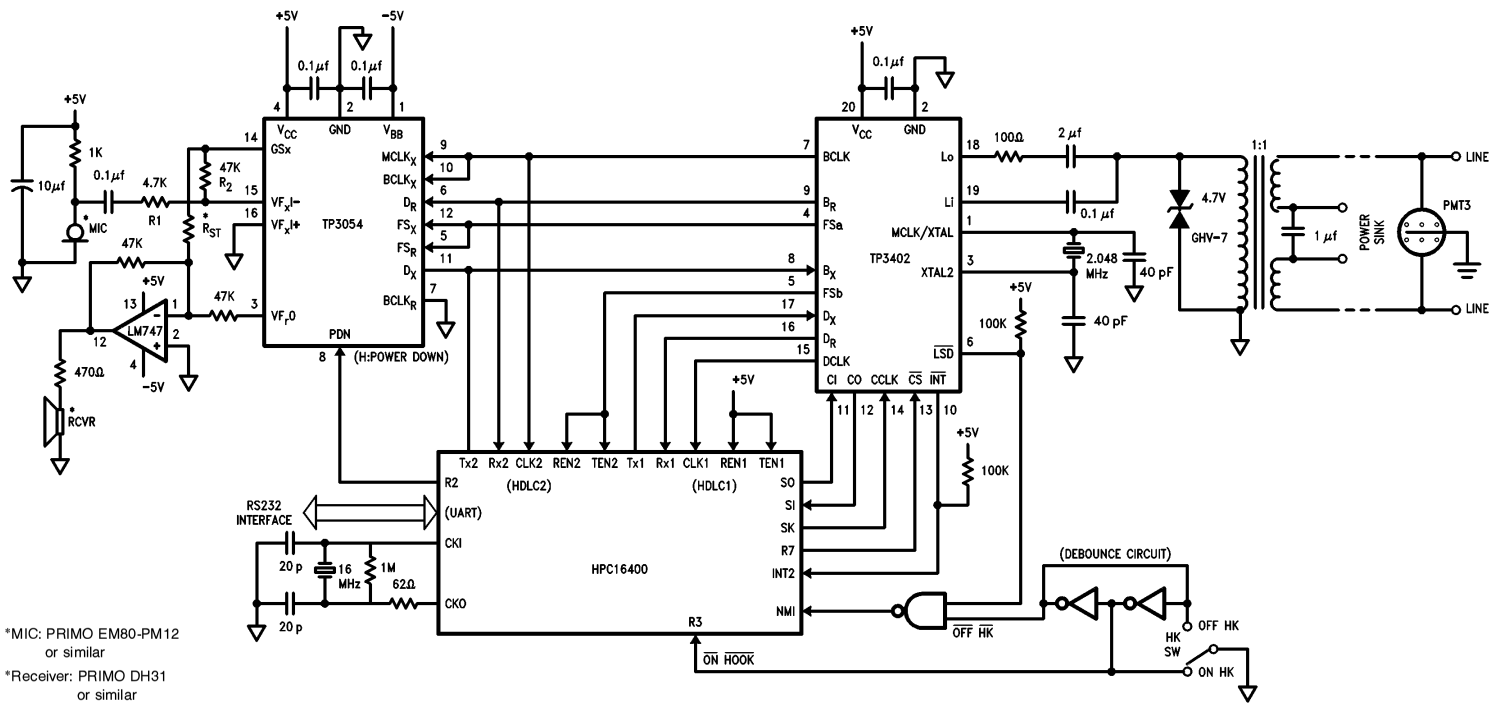

*MIC: PRIMO EM80-PM12
or similar

*Receiver: PRIMO DH31
or similar

*RST for side tone gain adjustment.
Typical R = 47k

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FIGURE 1. Typical Application for Terminal End

2. ACTIVATION/DEACTIVATION PROCEDURES

a. General Outline of the User-Network Interface

As shown in *Figure 2*, the user-network interface is based on peer-to-peer protocols from layer 1 to layer 3. All signaling messages on the D channel are used to exchange control information between the user and the network for call establishment and termination, and access to network facilities. The main functions in the three protocol layers involving network and terminal are listed below.

Layer 1, physical layer, includes functions for transmission, power feeding, activation/deactivation and maintenance.

Layer 2, data link layer. All data link layer messages in the peer-to-peer protocol are transmitted in frames which are delimited by flags. The denomination of the protocol procedure is LAPD, Link Access Procedures on the D Channel. LAPD includes functions for the provision of one or more logical link connections on the D channel, sequence control of messages, detection of errors and flow control.

Layer 3, network layer, includes functions for establishing, maintaining, and terminating circuit-switched connections, user-to-user signaling connections and packet-switched connections.

b. The Recommended Activation Procedure (Layer 1) from the NETWORK, i.e. TP3401 on a line card, is illustrated in Table I.

c. The Recommended Activation Procedure (Layer 1) from the TERMINAL is illustrated in Table II.

d. A Software Control Flow Chart for USER End Activation/Deactivation (Layer 1) is illustrated in Table III.

e. Call Clearing Procedure (Layer 3) is usually initiated by the user or the network sending signaling messages on the D channel across the user-network interface.

Clearing by the user: The terminal sends a DISConnect message. Following the receipt of a DISConnect message, the network considers the call to be in the disconnect-request state and disconnects the B channel that is used in the call, then the network returns a RELease message to the terminal. On receipt of the RELease message the terminal releases the B channel and the call reference, then sends a RELease COMplete message to the network.

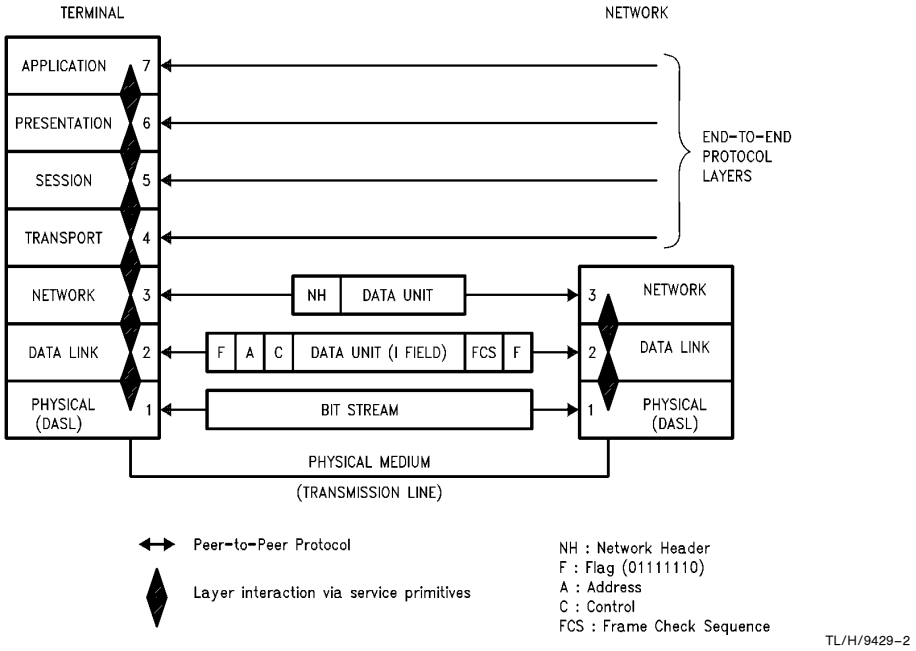

FIGURE 2. Protocol for the Signaling Procedure on the D Channel

Clearing by the network: The network sends a DISConnect message across the user-network interface and disconnects the B channel that was used in the call. Following the receipt of a DISConnect message, the user sends a RELease message to the network. On receipt of the RELease message, the network returns a RELease COMplete message to the terminal and releases the B channel and call reference for future use.

Note 1: Before loop-in-sync (C1 = 1) at the SLAVE (terminal) end, Fsa/Fsb and Fsc (TP3401 only) output pins are zero, the Br data output pin is tri-stated, Dr data output pin is high, BCLK and DCLK are free running outputs at 2.048 MHz and 16 kHz respectively, Bx and Dx data input pins are ignored, Lo output pin is sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.

Note 2: Before loop-in-sync (C1 = 1) at the MASTER (network) end, the Br data output pin is high during Fsb enable, otherwise that pin is tri-stated; Dr data output pin is high, $\overline{TS_r}$ output pin is low during B1/B2 received time slot, Bx and Dx data input pins are ignored, Lo output pin is sending 4 kHz burst rate of scrambled 1s in the B and D channels to the line.

Note 3: After the bit C1 = 1 (loop-in-sync) at the SLAVE (terminal) end, the HPC can start a timer and wait 2 ms to allow the network end to acquire loop-in-sync before attempting to enable B and D channels.

TABLE I. Activation from the Network End

Terminal End		Line	Network End	
HPC or μP	**DASL (SLAVE)**		**DASL (MASTER)**	**HPC or μP**
				1. Powers up DASL by writing control register bit C6 = 1 through MICROWIRE. Also starts the Default Timer.
	3. $\overline{LSD}$ pin goes low to wake up HPC, DASL status bit C0 changes to one and generates a MICROWIRE interrupt to the HPC.	← Tx 4 kHz burst	2. Starts sending 4 kHz burst rate of scrambled 1s in B and D channels to the line.	
4. Reads DASL status register and writes control register bit C6 = 1 through MICROWIRE to power up DASL. Also starts the Default Timer.				
	5. Starts sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.	→ Tx 2 kHz burst	6. The line signal detect circuit changes status bits C0 to one and generates a MICROWIRE interrupt to the HPC.	7. Reads DASL status register through the MICROWIRE interface.
	8. Flywheel circuit searches for 4 consecutive correctly formatted bursts, then sets status bit C1 = 1 (loop-in-sync) and generates a MICROWIRE interrupt. DASL starts to send 4 kHz burst data. (Note 1)	→ Tx 4 kHz burst (loop-in-sync)	10. Same as step 8. C1 = 1, loop-in-sync. (Note 2)	11. Same as step 9.
9. Reads DASL status register. If C1 = 1, the HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data. (Note 3)		← Tx 4 kHz burst (loop-in-sync)		

TABLE II. Activation from the Terminal End

Terminal End		Line	Network End	
HPC or μP	**DASL (SLAVE)**		**DASL (MASTER)**	**HPC or μP**
1. Powers up DASL by writing control register bit C6 = 1 through MICROWIRE. Also starts Default Timer.	2. Starts sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.	→ Tx 2 kHz burst	3. The line signal detect circuit changes status bit C0 to one and generates a MICROWIRE interrupt to the HPC.	4. Reads DASL status register and writes control register bit C6 = 1 through MICROWIRE to power up DASL. Also starts the Default Timer.
	6. $\overline{\text{LSD}}$ pin goes low, DASL status bit C0 changes to one and generates a MICROWIRE interrupt to the HPC.	← Tx 4 kHz burst	5. Starts sending 4 kHz burst rate of scrambled 1s in the B and D channels to the line.	
7. Reads DASL status register through the MICROWIRE interface.	8. Flywheel circuit searches for 4 consecutive correctly formatted bursts, then sets status bit C1 = 1 (loop-in-sync) and generates a MICROWIRE interrupt.			
9. Reads DASL status register. If C1 = 1, the HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data. (Note 3)	DASL starts to send 4 kHz burst data. (Note 1)	→ Tx 4 kHz burst (loop-in-sync)	10. Same as step 8. C1 = 1 loop-in-sync. (Note 2)	11. Same as step 9.
		← Tx 4 kHz burst (loop-in-sync)		

TABLE III. Activation/Deactivation Flow Chart at Terminal (Slave) End

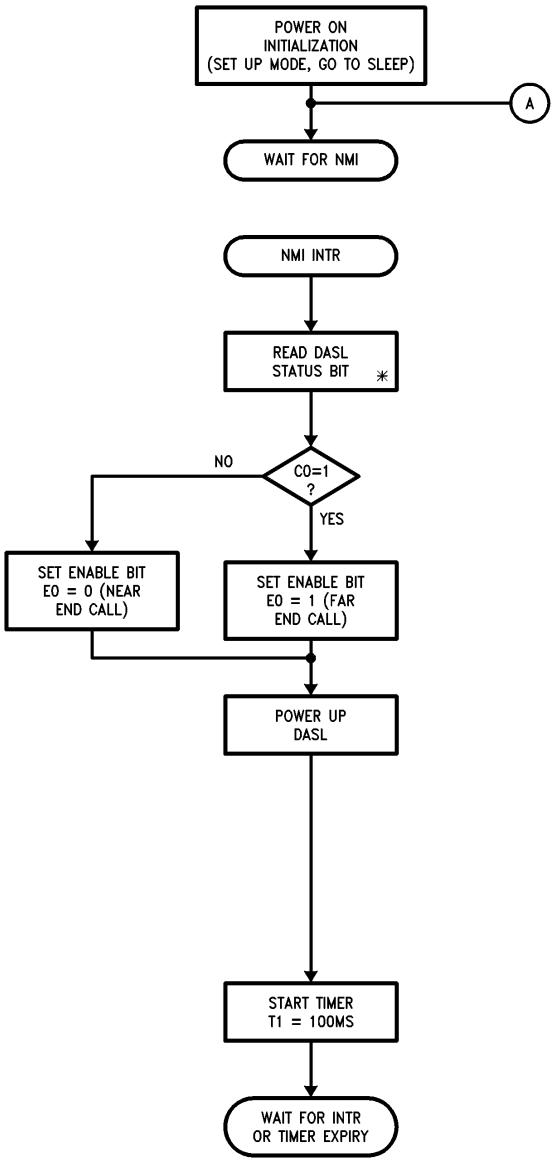

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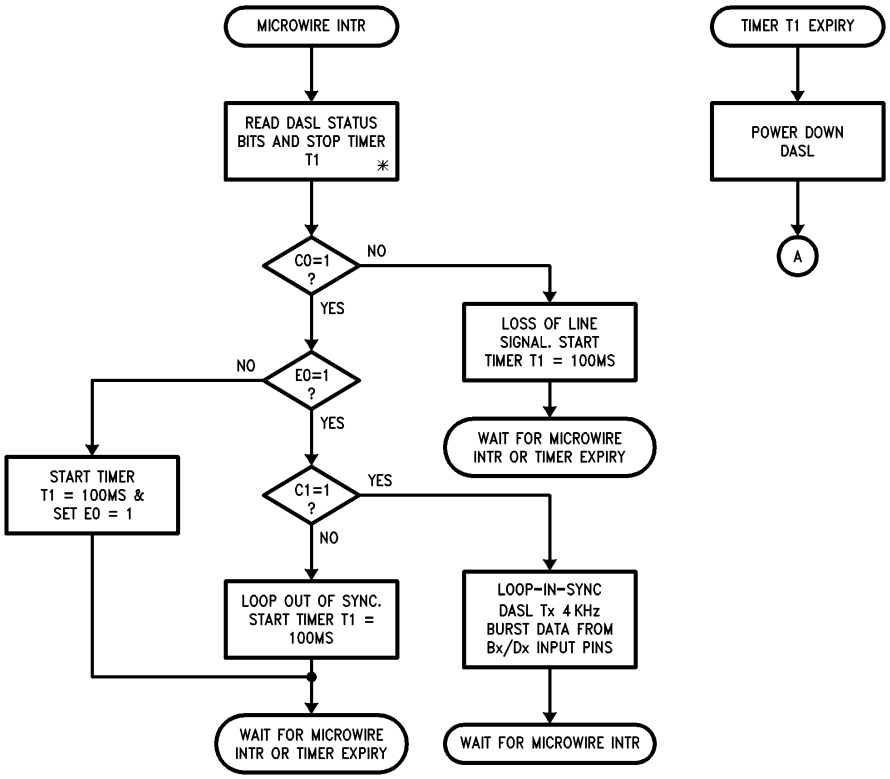
TABLE III. Activation/Deactivation Flow Chart at Terminal (Slave) End (Continued)



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*When reading the CO pin, data is always clocked into the CI pin, therefore the CI data word should be set to repeat the previous data word if no change in device mode is intended.

3. REPEATER MODE APPLICATION

a. System Description

In applications where a range beyond 1.8 km is required, a simple back-to-back connection of two DASLs provides a range extension capability out to 3.6 km. A low-cost microcontroller manages the activation and deactivation of the two loops, and B and D channel data passes transparently through between the two loops. Power for the REPEATER can be sourced from either end of the system.

As shown in *Figure 3*, two DASLs, which are connected back to back as master and slave to form a REPEATER, are directly controlled by a COP426C. The COP426C (Controller Oriented Processor) is a 4-bit complete microcomputer containing all system timing, MICROWIRE serial interface, 1k × 8 ROM and 64 × 4 RAM, 15 I/O lines, programmable read/write 8-bit timer/event counter, a true vectored interrupt and three-level subroutine stack.

In a typical application, the $\overline{INT}$ output pins of the two DASLs connect to L6 and L7 input pins of the COP426C. Also the G2 and G3 output pins of COP426C provide a chip select ($\overline{CS}$) signal to each DASL to enable the MICROWIRE serial interface. The COP426C, running on a slow R-C controlled clock, polls the input ports L6 and L7 every 4 ms. If either of these inputs changes to zero, the COP426C starts to run its activation/deactivation program as shown in the flow chart in Table VI; otherwise the COP426C goes to the idle mode, which takes only about 1 mA current for power saving. During activation, the loop at the Network end will always fully synchronize before the loop at the terminal end can synchronize. Network timing is thus passed on to the terminal. Only the Slave-mode DASL on the network side requires a 2.048 MHz clock oscillator; the Master-mode DASL on the terminal side uses the Slave's BCLK output as its MCLK timing source.

b. The Recommended Activation Procedure (Layer 1) from the NETWORK is illustrated in Table IV.

c. The Recommended Activation Procedure (Layer 1) from the TERMINAL is illustrated in Table V.

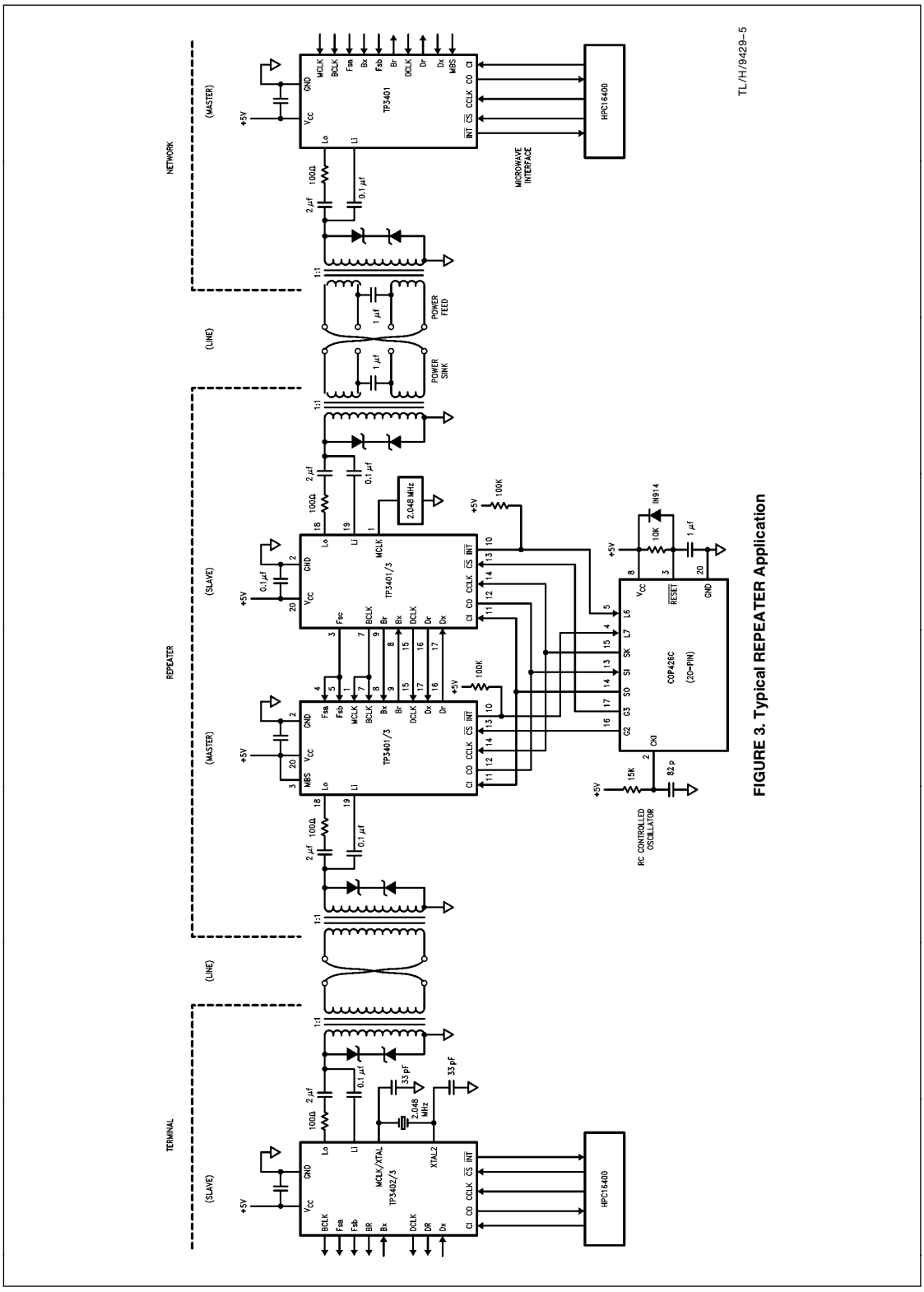


FIGURE 3. Typical REPEATER Application

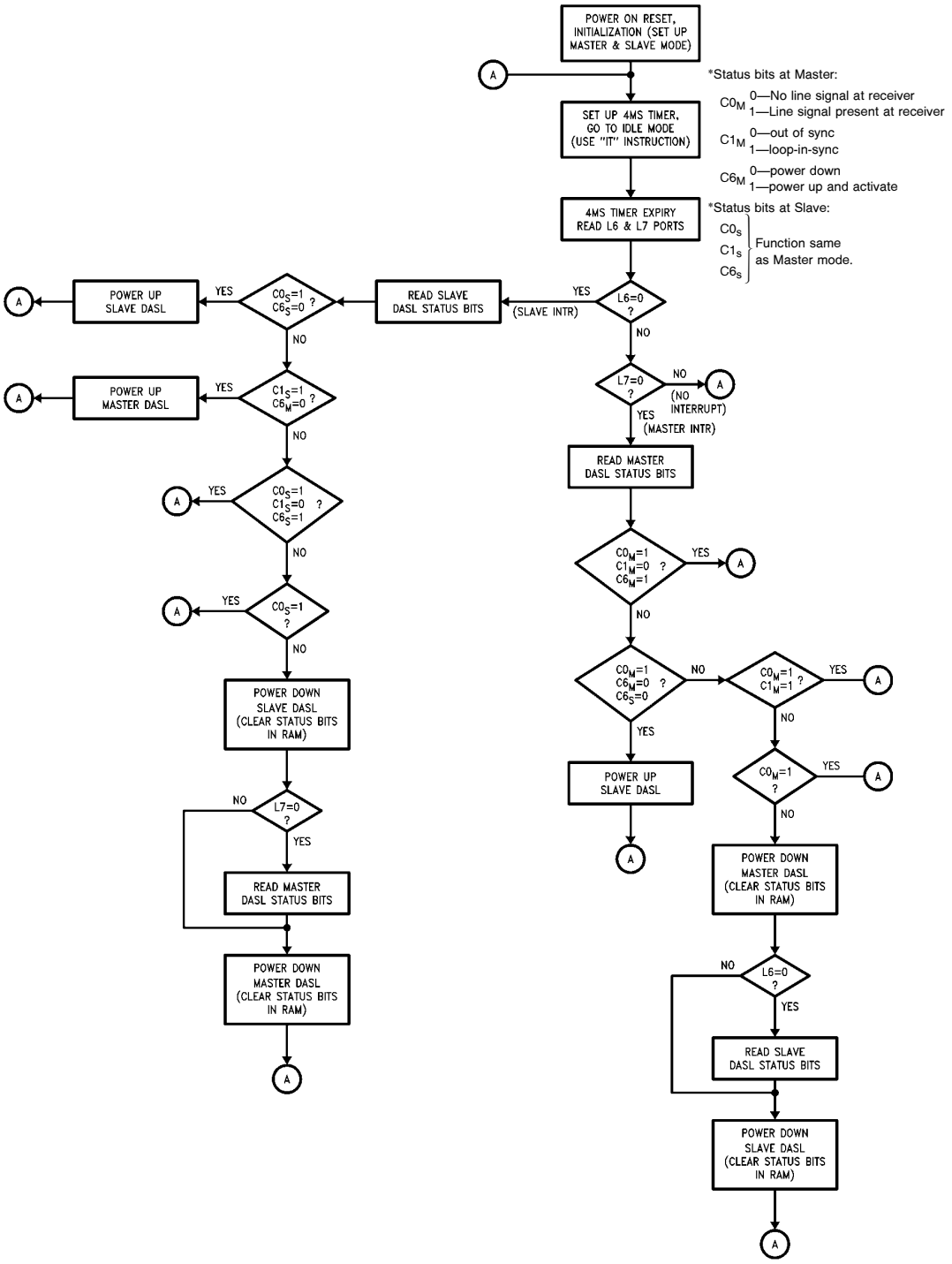
TABLE IV. Activation from Network for Repeater

Terminal End	Line	Repeater		Line	Network End
DASL (SLAVE)		DASL (MASTER)	DASL (SLAVE)		DASL (MASTER)
					1. HPC powers up DASL by writing control bit C6 = 1 through MICROWIRE and also starts the Default Timer. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.
			2. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to COP. COP reads DASL status register and writes control bit C6 = 1 through MICROWIRE to power up the DASL. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	← Transmit 4 kHz burst	
				→ Transmit 2 kHz burst	3. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL status register through the MICROWIRE interface.
			4. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates MICROWIRE interrupt and sends 4 kHz burst data from digital interface Bx and Dx to the line. COP reads DASL status register through MICROWIRE.		
		5. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.			
6. $\overline{\text{LSD}}$ pin goes low to wake up HPC, DASL status bit C0 changes to 1 and generates MICROWIRE interrupt to HPC. HPC reads DASL status register and writes control bit C6 = 1 through MICROWIRE to power up the DASL. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	← Transmit 4 kHz burst			→ Transmit 4 kHz burst (loop-in-sync)	7. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt and sends 4 kHz burst data that comes from digital interface Bx/Dx to the line. HPC reads DASL status register. If C1 = 1, HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables B channel. for voice data
	→ Transmit 2 kHz burst	8. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the COP. COP reads DASL status register through MICROWIRE interface.			
	→ Transmit 4 kHz burst (loop-in-sync)			← Transmit 4 kHz burst (loop-in-sync)	
9. Same as step 7. C1 = 1, loop-in-sync.	← Transmit 4 kHz burst loop-in-sync)	10. Same as step 4. C1 = 1, loop-in-sync.			
		ACTIVATION COMPLETION			

TABLE V. Activation From Terminal for Repeater

Terminal End	Line	Repeater		Line	Network End
DASL (SLAVE)		DASL (MASTER)	DASL (SLAVE)		DASL (MASTER)
1. HPC powers up DASL by writing control bit C6 = 1 through MICROWIRE and starts the Default Timer. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	→ transmit 2 kHz burst	2. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the COP. COP reads DASL status register through MICROWIRE interface.	3. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	→ Transmit 2 kHz burst	4. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL status register starts the Default Timer, writes control bit C6 = 1 through MICROWIRE to power up DASL. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.
			5. Same as step 2.	← Transmit 4 kHz burst	
		7. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.	6. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt and sends 4 kHz burst data from digital interface Bx and Dx to the line. COP reads DASL status register through MICROWIRE.		
8. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL MICROWIRE interface.	← transmit 4 kHz burst			→ Transmit 4 kHz burst (loop-in-sync)	9. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt, sends 4 kHz burst data that comes from digital interface Bx/Dx to the line. HPC reads DASL status register. If C1 = 1, HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data.
10. Same as step 9. C1 = 1, loop-in-sync.	→ transmit 4 kHz burst (loop-in-sync)	11. Same as step 6. C1 = 1, loop-in-sync.		← Transmit 4 kHz burst (loop-in-sync)	
	← transmit 4 kHz burst (loop-in-sync)				
		ACTIVATION COMPLETION			

TABLE VI. Activation/Deactivation Flow Chart for REPEATER Mode



4. TRANSFORMER DESIGN GUIDE

Two different transformer designs are described here, one for ''DRY'' loops, in which no D.C. current is flowing, and one for ''WET'' loops in which power feed current is supplied to the terminal via split windings. A 1:1 turns ratio is used, with a 100Ω termination impedance for good line impedance matching over the bandwidth of the line signal.

a. Dry transformer: no D.C. current through the transformer.

Dry transformer specification:

1. Ferrite core
   Siemens EP13-T38 or equivalent
   AL = 7000 nH/T-2 (ungapped)
2. Windings

Np	1–2	50T(AWG #34)
Ns1	3–4	25T(AWG #34)
Ns2	5–6	25T(AWG #34)

3. Inductance
   16 mH (ungapped) at 1 kHz
4. D.C. resistance
   Np = 0.52Ω (max)
   Ns1 = Ns2 = 0.26Ω (max)
5. Impedance
   100Ω
6. Frequency response
   Bandwidth: −3 dB down at 1 kHz and 1 MHz
   Return loss: More than 20 dB from 48 kHz to 192 kHz

b. Wet transformer: designed for ≤50 mA current through the transformer.

Wet transformer specification:

1. Ferrite core
   Siemens EP13-T38 or equivalent
   AL = 500 nH/T-2 (with 1-mil paper gapped)
2. Windings

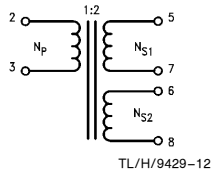
Np	1–2	130T(AWG #34)
Ns1	3–4	65T(AWG #34)
Ns2	5–6	65T(AWG #34)

3. Inductance
   8.7 mH (with 1-mil paper gapped) at 1 kHz
4. D.C. resistance
   Np = 3.0Ω (max)
   Ns1 = Ns2 = 2.0Ω (max)
5. Impedance
   100Ω
6. Frequency response
   Bandwidth: −3 dB down at 1.3 kHz and 900 kHz
   Return loss: More than 20 dB from 48 kHz to 192 kHz

Following is a list of vendors of 1:1 and 1:2 transformers which have been designed for use with the TP3401 DASL.

U.S.

1. AIE Magnetics (Florida); phone 813-347-2181.
   Part Number: 1:1 (center tapped) 325-0244 (EP10 core);
2. Schott Corporation (Nashville); phone 615-889-8800.
   Part Numbers: 1:1 (center tapped) 11085; (dry)
   1:1 (center tapped) 11086 (50 mA DC)



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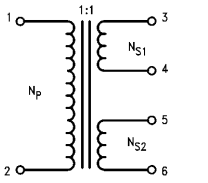

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5. SURGE PROTECTION METHODS AT THE LINE INTERFACE

There are two main sources of transient high voltages, lightning and short circuit wiring faults to commercial power systems. The induced overvoltage can seriously damage voltage sensitive components, so at least two levels of protection are required on the line interface as shown in *Figure 4*.

a. Protection at Secondary of Transformer

The protector at the secondary of the transformer is usually placed on the line at a distance greater than 25 meters from the linecard; the impedance of the line will ensure that this protector always operates first. A suitable protector is a gas discharge tube, which has high insulation resistance, low capacitance and high current capability, such as a three electrode gas discharge surge arrester PTM3(310).

PMT3(310) Specifications:
Manufacturer: General Instrument Corp.
D.C. breakdown voltage: 250V
Pulse breakdown voltage: Less than 1600V at a ramp speed of 10,000 V/μs
Peak surge current: 10,000 A
Holdover voltage: 100V and 150V minimum
Surge life: 400 surges average (500A, 10/1000 μs)
Capacitance: Less than 5 pF

b. Protection at Primary of Transformer

The protection at the primary of the transformer can be provided by either a Zener diode or Varister; in the application shown in *Figure 4* is one GHV-7 Varister.

GHV-7 Specifications:
Manufacturer: General Semiconductor Industries, Inc.
Breakdown voltage Bv: 4.7V
Max surge current: 30 A (8.4 ms), 100 A (1.0 ms)
Capacitance: Less than 150 pF

6. BIT ERROR RATE PERFORMANCE

a. General Description

On the receiver side of DASL, data detection is accomplished by threshold comparison synchronized to the received signal timing. A first-order adaptive equalizer has been computer optimized and field tested on a variety of PBX and short range subscriber networks. Performance objectives are based on standard twisted pair cable characteristics. The equalized signal is processed by a wave-difference time-extractor and loop filter circuit followed by level data-detection. A novel design of an early-late DPLL with effective 30 ns step increments guarantees timing precision and stability.

b. Test Set-Up

The following BER measurements for DASL have been taken in burst mode at 144 kb/s full duplex two wire transmission, using 1:1 transformers.

Loop lengths of up to 2 km of 22 AWG, 24 AWG and 26 AWG cable have been used.

For the measurements on the 22 AWG and 26 AWG cable, a TAS 2100 loop emulator was used.

A white noise signal, band-limited to 500 kHz, was inserted at the receiver's input.

Bit error rates were measured by transmitting 100 million bits using pseudo random patterns.

1 km/24 AWG, input signal level 295 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
14.1	0.0 E-7
17.7	1.0 E-7
21.2	1.3 E-5

2 km/24 AWG, input level 95 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
3.5	0.0 E-7
5.3	9.7 E-7
7	8.8 E-5

1 km/22 AWG, input level 440 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
22.1	0.0 E-7
28.3	2.0 E-6
35.4	9.1 E-5

1.8 km/26 AWG, input level 75 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
3.5	0.0 E-7
5.3	4.3 E-7
7	8.4 E-6

In addition to the above mentioned test method, BE rates have also been measured in the presence of a single tone interference signal at approximately twice the frequency of the main spectral lobe (in this case 400 kHz).

Range 1 km/24 AWG cable, 295 mV_{PP} input level:

BER = 0.0 E7 for a 53 mV_{PP} sine wave at 400 kHz.

Range 2 km/24 AWG cable, 95 mV_{PP} input level:

BER = 0.0 E-7 for a 14.4 mV_{PP} sine wave at 400 kHz.

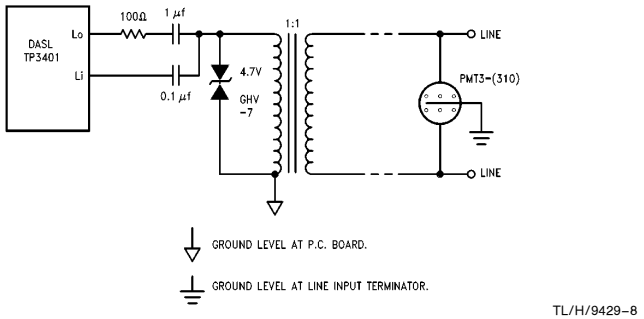

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FIGURE 4. Typical Protection Arrangement

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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