A Monolithic Power Op Amp

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Abstract: *The standard, junction-isolated power process has been modified by the addition of polycrystalline-film resistors to solve the topological problems encountered in making 90W, 80V, 10A power transistors and connecting them together for a push-pull output.*

An all-NPN output stage has been developed that holds cross-over distortion to 0.01-percent while driving a 4Ω load, even with the quiescent current below 20 mA. It is stable with all reactive loads and does not have the spurious-oscillation problems observed with the familiar quasi-complementary amplifier.

These innovations are described along with the design of a complete power op amp. The all-important safe-area protection is covered in a companion article [1]. Preventing failures from substrate currents arising when the output is driven outside the supply by inductive loads is discussed here.

introduction

Early interest in IC power amplifiers [2]–[3] equaled that of voltage regulators. Although standard regulators have enjoyed widespread commercial acceptance, no true industry standards have emerged with power amplifiers. Their application has been largely restricted to audio amplifiers in low-end, consumer-grade equipment.

The lack of suitable multi-lead power packages initially inhibited development. Unlike regulators, amplifiers cannot use three-terminal transistor packages. But limited output power and the inability to cope with the reactive loadlines commonly encountered with practical power amplifiers were the most serious shortcomings of the older designs.

The techniques developed for low-voltage IC regulators [4] are not adequate for the demands of high-power amplifiers even as refined [5]–[10]. The largest transistor structures used for regulators [8]–[10] are not suited topologically or structurally for connecting together two transistors as is required for push-pull amplifiers; and attempts at increasing peak power ratings [8]–[9] have fallen far short of theoretical capabilities. This has left the state of the art for power amplifiers much as summarized by Murari [11].

New techniques [12] have been applied to develop a linear power transistor that uses polysilicon resistors for ballasting, avoiding problems due to thermal destabilization [13] and avalanche injection [14] even with 80V collector voltage. More efficient use of silicon area is a feature of the design.

Protection circuitry that allows the power transistor to operate near its theoretical safe-area limits for both transient and steady-state conditions increases guaranteed power ratings by several times when compared to older techniques. At the same time, it dramatically lowers the peak junction temperature with worst-case fault conditions.

Still another modification of the ubiquitous quasi-complementary output stage [15] is described. Although avoided where possible, improved versions have evolved [16]–[17]. This latest has been tried with both power amplifiers and 20 MHz op amps. The frequency compensation, capacitive loading, asymmetrical response and cross-over distortion problems often encountered with the configuration are conspicuously absent.

These new methods are combined in a power operational amplifier that not only has increased voltage and current ratings but also is able to handle the high peak power associated with reactive loads. Output swings of ±35V at ±10A can be specified, and the continous dissipation rating is 90W. Peak dissipation above 800W is allowed. A photograph of the IC in the hermetic TO-3 prior to sealing is given in *Figure 1*. The performance and applications of the op amp are described in the references [18]–[19].

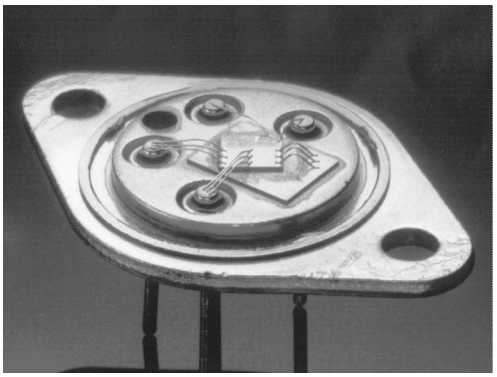

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FIGURE 1. Photograph of the LM12 power op amp mounted in a modified TO-3 package. Three, five-mil bond wires are required to handle the rated output current.

the op amp

A simplified schematic of the power op amp is provided in *Figure 2*. Input buffers, Q_1 and Q_2, drive the differential gain stage, Q_3 and Q_4. A current mirror, Q_5 and Q_6, converts the differential signal to single ended and drives Q_8, an integrating inverter that shapes the response of the amplifier. The output driver is a quasi-complementary amplifier that has been modified by providing a high-frequency signal path

around the inverting PNP, Q_{15}, through Q_9. A boost circuit, Q_{12}–Q_{14}, increases the low-frequency gain of the output follower, Q_{16}, to equalize the gain for bi-directional loads.

One reason for using input buffers is to limit the base drive to Q_3 and Q_4 when the negative common-mode limit is exceeded. Excessive base drive after saturation of the inverter causes a sense reversal on the input. This reversal can give severe distortion with overloads, rather than simple clipping.

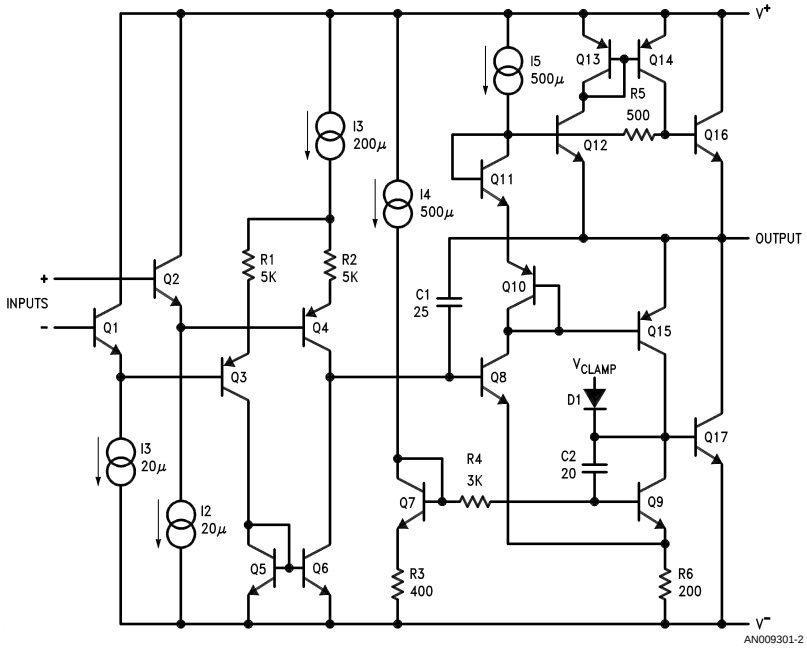


FIGURE 2. Simplified schematic of the op amp. The high-frequency path around the PNP in the quasicomplementary output stage causes it to behave like a true complementary amplifier.

Degeneration resistors, R_1 and R_2, lower the transconductance of the input transistors. This allows the op amp to be frequency compensated with smaller C_1. Since the current available to drive C_1 is undiminished, slew rate is increased.

The biasing circuitry for Q_9 cause it to operate at the same current as Q_8, with about 200 mV across R_6. The clamp diode, D_1 keeps Q_9 out of saturation and Q_{17} at the threshold of conduction when the output is sourcing current. Keeping Q_{17} from turning off completely reduces high-frequency cross-over distortion.

When sinking load current, the signal path is through the lateral PNP, Q_{15}, at low frequencies. As the f_T of the lateral PNP is approached, the path through Q_9 takes over. Above 2.5 MHz, Q_9 begins to look like a diode because of the R_4C_2 compensation. At higher frequencies where the loop stability of the integrating inverter is affected, the signal path for positive load is through the inverter, Q_8, and the follower, Q_{16}. With a negative load, the path is through the follower, Q_8, and the inverter, Q_{17}. The ac equivalent circuits are about the same for the two paths.

With careful design, R_5 in the boost circuit can be made low enough that the boost is effectively bypassed at high frequencies. The boost is, in fact, more stable than an extra follower.

Connecting C_1 to the output rather than the emitters of Q_{10} and Q_{11} reduces high frequency crossover distortion. If C_1 is connected to the emitters of Q_{10} and Q_{11}, the distortion components in the voltage-gain error of the output transistors appear across C_1. The resulting current must be supplied by the input stage. This causes closed-loop distortion. With C_1 connected to the output, only the distortion components in the base voltage of Q_8 generate current in C_1; so distortion is reduced by the inverter gain.

Compensating directly from the output requires well-controlled response in the output inverter out to nearly 100 MHz if spurious oscillations in the integrator loop are to be avoided. This is not easily accomplished over the full range of dc and ac loading conditions that a power op amp can encounter (including capacitors resonating with lead inductance). Controlled high-frequency response is a significant advantage of this design especially when compared to standard quasi-complementary.

Figure 3 shows additional details of the op amp design. Resistors and clamp diodes have been added to the input to prevent damage should the inputs be driven beyond the supplies. The current sources for the input stage are biased from an internal source, V_B. The voltage is about 1.3V, referred to V^-. A second, internal bias, V_Z = 12.3V, is available for circuitry that does not require the full supply voltage.

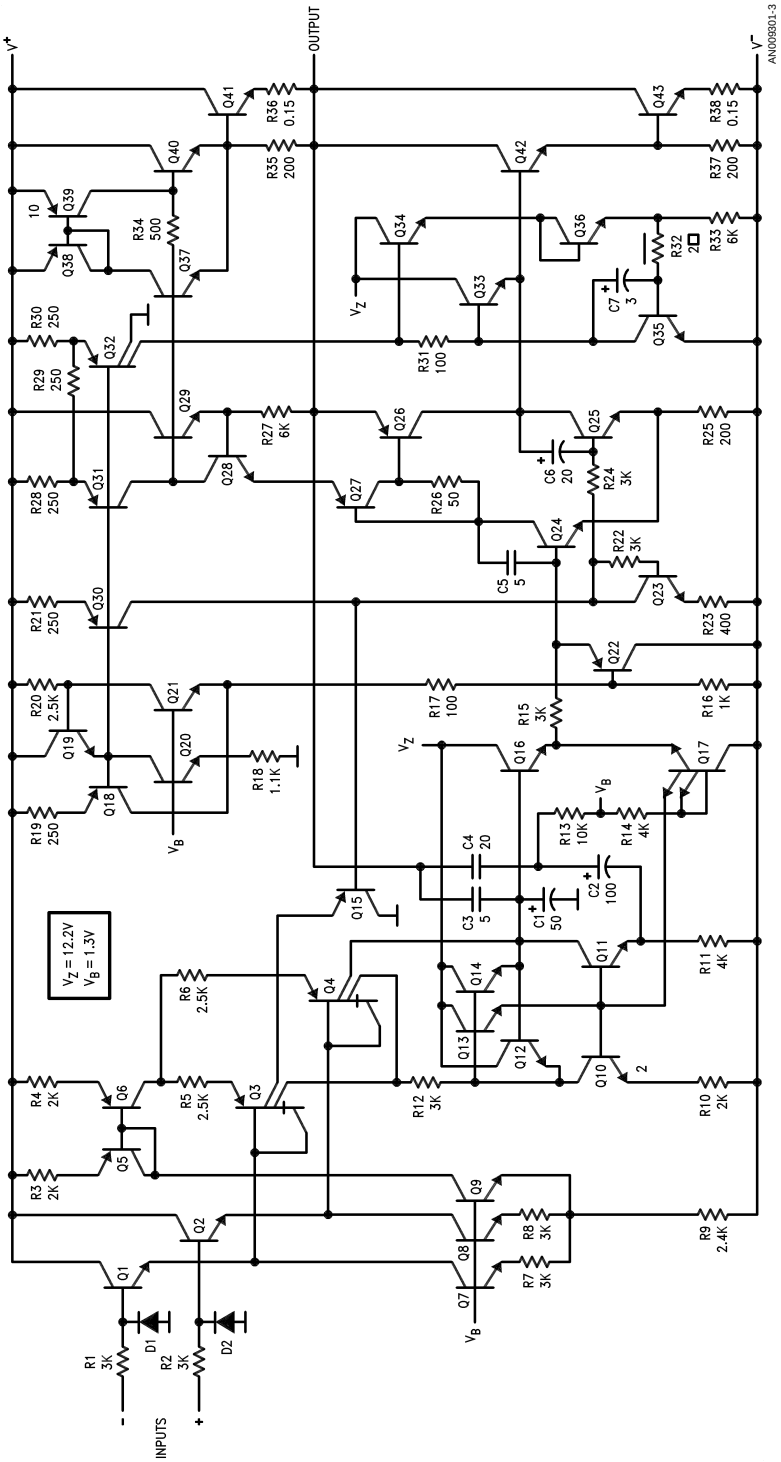


FIGURE 3. Details of the power op amp. Unusual frequency compensation boosts slew rate and lowers distortion. It is stable with capacitive loads, and no RC snubber is required on output.

The lateral PNPs in the differential stage have their collectors split into two equal segments. The current mirror is fed from one collector on each transistor making its operating current independent of the input voltage. This takes the phase shift of the mirror out of the signal path. Signal is taken from the second collector on Q_4. The other collector of Q_3 is returned to a point near the same voltage as the signal collector.

The lower collector on Q_3 and Q_4 is formed outside the active collectors. When the active collectors saturate, they re-inject the emitter current to the outside collector. Connecting this collector to the base prevents sense reversal as long as the base drive is less than the emitter current.

The mirror is buffered with followers Q_{13} and Q_{16}. Q_{12} and Q_{14} act as clamps to limit output swing. A multi-emitter inverted transistor supplies bleed current for the followers.

One feature of this input-stage design is that the common-mode range equals the output swing. This allows clean saturation characteristics when used as a follower.

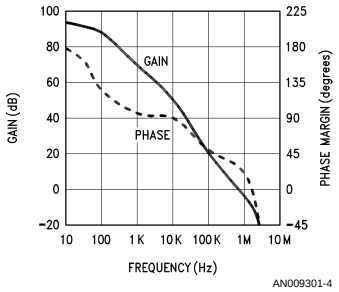
Bias voltage for the output stage current sources, Q_{30}–Q_{32}, is provided by Q_{18}–Q_{21}. The base drive to Q_{24} is limited by Q_{22} to control the maximum output current of Q_{24}.

The clamp on the collector of Q_{25} is provided by Q_{33}–Q_{36}. Darlington output transistors are accommodated by adding Q_{29} and R_{27} to the output stage bias circuitry. The quiescent current is stabilized with output swing by the action of R_{29}.

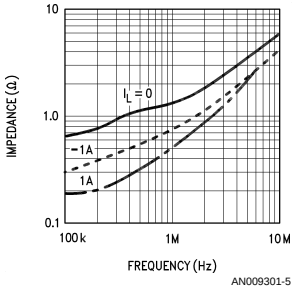
The op amp frequency compensation was designed to optimize capacitive-load stability, slew rate and cross-over distortion. The effective slew rate was increased from 2V/µs to 9V/µs by using two-pole compensation. The gain, phase and output impedance plots in *Figure 4* characterize performance.

Near the unity-gain crossover frequency (700 kHz) the output integrator is compensated by C_3 plus the series combination of C_2 and C_4. This gives an effective compensation capacitance of 22 pF. Below approximately 100 kHz, the feedback from the C_2/C_4 path is diverted by R_{13}, reducing the compensation capacitance to about 5 pF at audio frequencies. Thus, power bandwidth is increased and slew distortion is reduced at frequencies below 100 kHz.

Distortion components appearing on the base of Q_{16} generate currents in C_1 and C_3. These currents are supplied by the input stage, causing distortion. Returning C_2 to the emitter of Q_{11} rather than the base of Q_{16} prevents distortion currents from being generated in C_2.



a) Gain and Phase



b) Output Impedance

FIGURE 4. Gain-phase characteristics of the two-pole compensation (a) and ac output impedance (b) determine loop stability with capacitive loads. The op amp is free of spurious oscillations.

Stabilizing the integrator loop for all loading requires C_1 and C_5 when the main compensation is connected to the output. Both these capacitors increase distortion but do not negate the advantage of compensating to the output when signals are in the audio range.

Although the design is entirely empirical, it has been thoroughly tested over a wide range of applications and operating conditions [18]–[19]. No problems with spurious oscillations were encountered, and an output RC snubber was not required.

bias controller

A single voltage (V_B) is distributed to bias the IC. If this voltage is down, the op amp is shut off with its output open. Because of this, the bias supply can include the undervoltage lockout ($V_S < 14V$), the overvoltage shut-down ($V_S > 0.9\ BV_{CEO}$) and the control-circuit thermal limit ($T_C > 150^{\circ}C$).

A schematic of the bias controller is shown in *Figure 5*. Initial turn-on current is provided by a collector FET, Q_{11}. As supply voltage rises, Q_{10}, will conduct first through R_{15}; and saturate the collector of Q_9 connected to the base of Q_{12}. Saturated, this collector injects to the collector on the base of Q_4. When Q_4 conducts, it turns on Q_{14} which holds the bias bus low. As the total supply voltage approaches 14V,

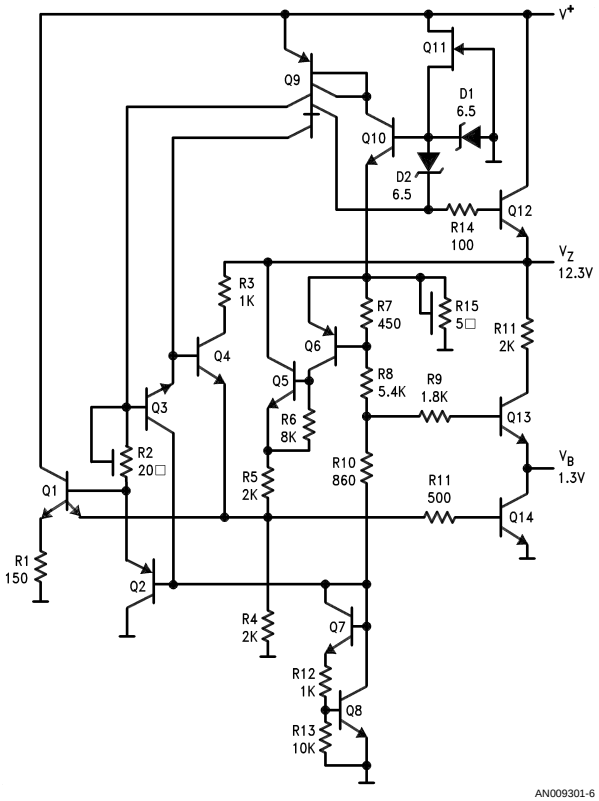


FIGURE 5. This bias controller provides undervoltage lockout, overvoltage shut-down and control-circuit thermal limit in addition to supplying a temperature-compensating bias.

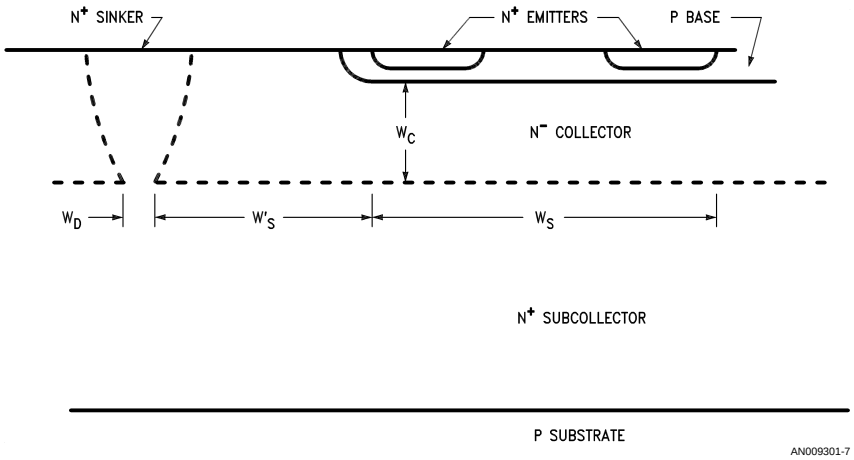


FIGURE 6. Cross section of the IC power transistor. Collector saturation resistance is determined solely by subcollector resistance, so getting emitters close to the sinker is important.

D_2 will conduct, pull the collector out of saturation, removing base drive from Q_4 and allowing V_B to come up to voltage.

The resistive divider off the emitter of Q_{10} works with Q_7, Q_8 and Q_{13} to supply a voltage, V_B, that will give a constant output current from an NPN current source biased from it, compensating for temperature variations of diffused-base resistors. This voltage can be routed through the IC using N^+ cross-unders diffused into the isolation wall to simplify layout. A second voltage, V_Z, powers internal circuitry that does not require the full supply voltage.

Thermal limiting is provided by Q_5 and Q_6. When Q_6 reaches 150˚C, the voltage across R_7 is large enough to turn on Q_6, Q_5 and Q_{14}. This shuts down V_B, causing positive feedback through R_9. The feedback generates a thermal hysteresis of about 5˚C. Since Q_6 is located at some distance from the power transistor, it responds mostly to case temperature.

Overvoltage shut-down is effected by Q_1. R_2 is a pinched-base resistor. Its resistance tracks the low voltage h_{FE} over the required range of temperature and production variables. When the h_{FE} of Q_1 rises to four times its low-voltage value, Q_1 turns on Q_{14}. This happens for $V_S \sim 0.9\ BV_{CEO}$. The operation is described elsewhere in greater detail [1].

power transistor design

Figure 6 shows a cross section of an IC power transistor. It is drawn to scale with the vertical dimensions expanded by a factor of three. The subcollector, with a sheet resistance in the range of 10–30Ω/□, is diffused into a 5–15Ω•cm P-type substrate. A N− film is then grown epitaxially. This is followed by isolation, sinker, base and emitter diffusions.

The voltage rating, BV_{CEO}, is determined by the collector doping and thickness (W_C). It is also influenced to a lesser degree by the peak ac current gain [20].

Current flow is from the emitter, across the base and collector, to the subcollector. It then flows to the left along the subcollector back up to the surface through the sinker.

In the limit, the collector saturation resistance in *Figure 6* is determined by the effective subcollector resistance. This is

$$R_{SUB} = \frac{R_{\square}}{\ell}\left[W_S' + \frac{W_S}{2}\right], \qquad (1)$$

where $R_{\square}$ is the subcollector sheet resistivity and ℓ is the length of the structure perpendicular to the drawing.

The resistance contributed by the collector contact through the sinker can be made negligible by insuring a minimum donor concentration at the sinker-subcollector interface around 10^{16} cm^{-3}. The concentration near the surface is well above 10^{19} cm^{-3}.

A bound for sinker resistance can be computed from spreading resistance plots for the sinker and subcollector. This is done by converting the logarithmic concentration profile into a linear plot of resistivity. Graphical integration will then provide

$$R_{SINK} \leq \frac{1}{W_D\ \ell}\int_o^{x_j} \rho dx. \qquad (2)$$

As a NPvN transistor enters quasi-saturation, a base extention forms expanding the effective base into the N− collector [21]. Once this extended base reaches the subcollector, carrier transport from the emitter is by diffusion, producing a small voltage drop (<200 mV) that is essentially independent of current density.

The base extension is accompanied by a decrease in transistor f_T that is also largely unaffected by current density. With IC transistors, the initial f_T is typically 200 MHz, dropping to 10 MHz as saturation is approached.

The dc current gain (h_{FE}) also drops with base extension. The drop is not directly related to the effective base width, except at high current densities. Maximizing the active emitter area will provide the best h_{FE} at high currents.

Figures 7, 8 show the cell structure used to make the power transistors. After emitter diffusion, an oxide is formed over the emitter. Contact holes are made and a 5000 Å polycrystalline-silicon film is deposited. The film is doped for a sheet resistivity of 30Ω/□ and etched to delineate the resistors. Another oxide is formed, after which contact holes for metal contact are cut. Metal is then deposited, etched and alloyed.

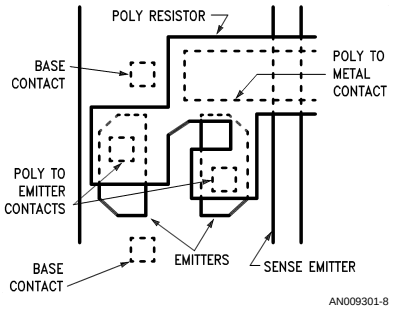


FIGURE 7. Details of the power transistor ballasting. The poly resistors contact down to the emitters and up to the metal. A narrow thermal-sense emitter runs alongside the active emitters.

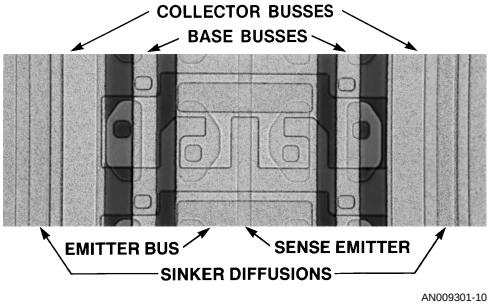


FIGURE 8. Photomicrograph of a power transistor cell. Developing ballast on a second level allows the metal to be optimized and the active emitter to extend beyond the base lead to minimize saturation resistance.

IC transistors require ballasting to avoid severe safe-area restrictions at higher voltages [13]. With 80Ω on each emitter, the high-voltage characteristics shown in *Figure 9* were obtained for the power transistor. The ballast resistors require no additional surface area, being formed over the active transistor and under the metal. The second-level connection of the emitters to the emitter bus allows the design of the emitters and the metal to be optimized independently without wasting silicon.

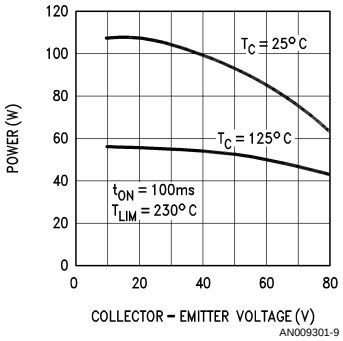


FIGURE 9. Continuous power rating of the IC power transistor as a function of collector voltage. High-voltage falloff is less at elevated temperatures because thermal gradients are reduced.

Base contacts are made small to maximize active emitter area and reduce lateral distance to the collector sinker, more than offsetting the moderate increase in base-spreading resistance in reducing saturation voltage and base drive at high currents. Base current is distributed around the emitter peripheries through the 110Ω/□ base diffusion. The emitters are shaped to minimize debiasing around the edge.

A temperature-sensing emitter runs through the hot zone of the center of the cell. This placement allows near-instantaneous limiting of peak junction temperature [1].

The power array was generated with nine columns, each formed by stacking fifteen of the cells shown in *Figure 8.* To this stack was added Darlington drivers, as shown in *Figure 10.* The base bus equalizes the base voltage for all columns so that temperature gradients among the column drivers do not cause unequal conduction. Individual column drivers hold down the drop along the base bus at maximum current. The driver bases and the temperature-sense emitters are brought out of the power array to metal busses with poly-silicon cross-unders.

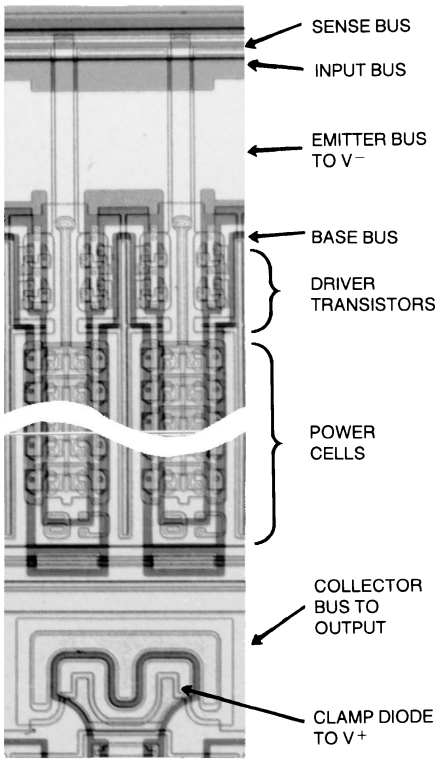


FIGURE 10. The location of the column drivers are shown here. Connections to the base of the driver transistors and the sense emitters are routed under the emitter bus using poly.

The main output transistor has zener clamps between the base and emitter busses to provide a path for the removal of stored base charge and work with the ballast resistance to limit the peak current when an instantaneous short forces voltage across a saturated output transistor.

A photomicrograph of the IC chip in *Figure 11* shows the overall design of the power array. Each power transistor is capable of handling 10A continuously with a dc current gain of 3000 at a saturation threshold of 3V. The current rating is established by the width of the emitter and collector busses coming out of the columns. Half the saturation voltage is developed across the ballast resistors with the other half across the subcollector resistance.

safe-area protection

Dynamic safe-area protection is obtained in this IC by limiting the peak junction temperature within the power transistor. The technique is discussed at length in a companion article [1], although the schematic in *Figure 12* gives additional details on its implementation. The power array is represented in the figure by Q_1 and Q_2. R_1 is the parallel combination of all the ballast resistors; the left emitter on Q_1 is the thermal-sense emitter.

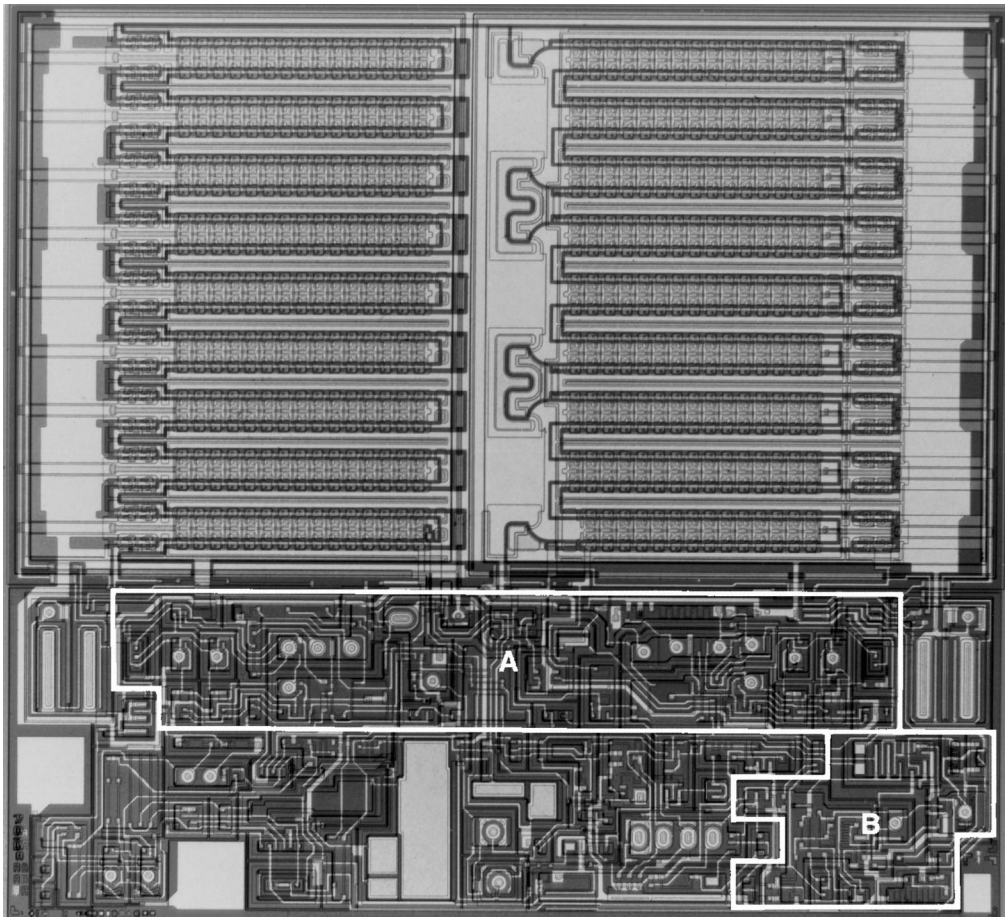


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FIGURE 11. Photomicrograph of the LM12 shows overall power array design. The safe-area protection (a) and bias-control (b) circuitry are identified to show the cost in silicon area. Die size is 164 x 179 mils.

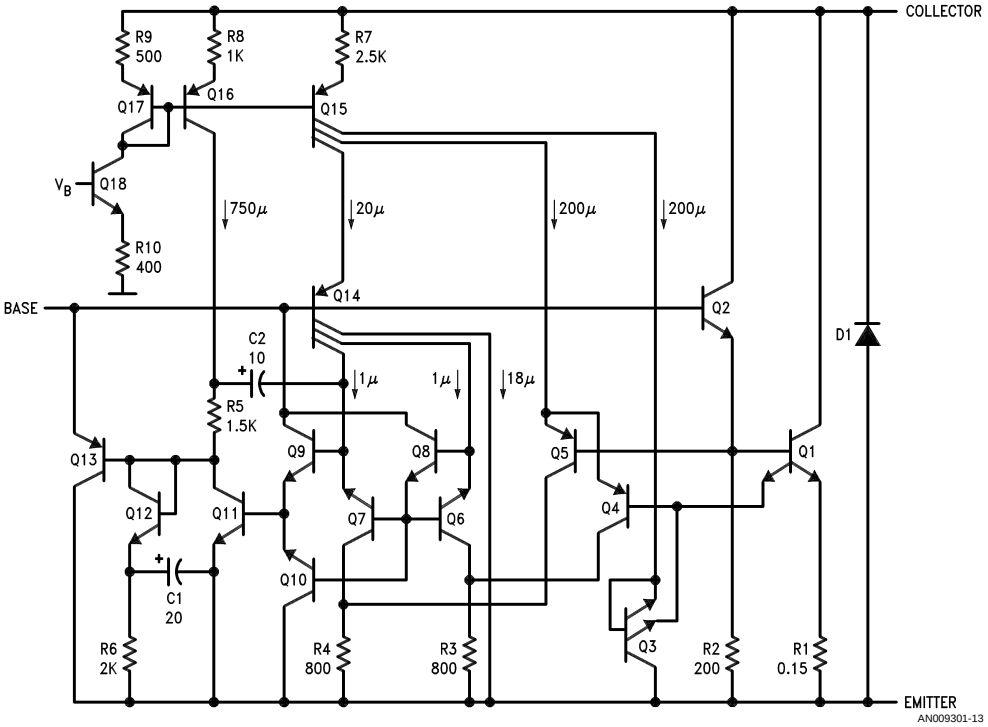


FIGURE 12. Schematic of the circuitry providing current limit and dynamic safe-area protection. The latter is accomplished by limiting the peak junction temperature near 230˚C.

As temperature is raised, the emitter-base voltage of the thermal-sense emitter drops and will ultimately reverse polarity. This will occur near 230˚C for the bias conditions used here. A frequency-compensated op amp is formed by Q_4–Q_{13}. As the sense-emitter voltage approaches zero, Q_{13} will turn on taking over in controlling the base of Q_2. In doing this, it will regulate the peak temperature.

Electrical current limit is provided by R_6, Q_{12} and Q_{13} working in conjunction with R_1. The collector current of Q_{16} is largely independent of temperature, being derived from a current source biased by V_B. This current is passed through a poly-silicon resistor, R_6. When the voltage drop across R_1 is roughly equal to the drop across R_6, base drive is shunted through Q_{13}, effecting limit.

The circuitry providing safe-area protection consumes considerable silicon, as can be seen in *Figure 11*. This expenditure is justified considering that it more than doubles the ratings that can be guaranteed for the power transistors.

substrate current

Figure 13 shows the output waveform of an op amp that has an inductive overload. Inductor current continues to flow even though the output transistor cannot handle it, and the output must be clamped to the supplies to limit the voltage across the transistors.

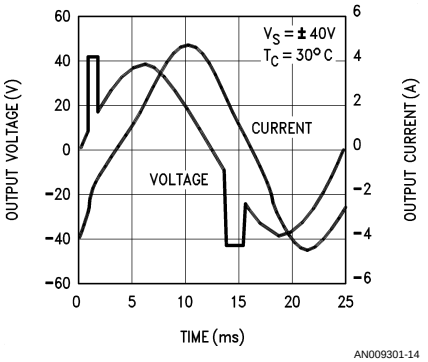
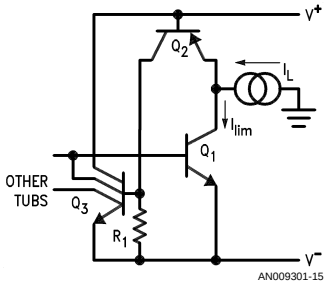


FIGURE 13. When safe-area protection activates with an inductive load, continuing load current causes the output to swing beyond supplies. A clamp is required to limit transistor voltage.

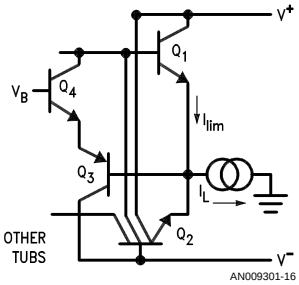
A diode that keeps the output from rising above V^+ is shown in *Figure 10*. The structure is the same as that in *Figure 6*. The sinker contact is the cathode; the base and emitter form

the anode. The diode is actually a low-gain PNP transistor with the substrate acting as a collector. A composite anode made with emitter and base shorted together reduces the current gain, but the reduction diminishes as operating current is increased [11].

Electron injection can occur at the die-attach interface. This is represented by Q_3 in *Figure 14a*, where Q_2 is the clamp diode. It increases the effective current gain of the clamp. The injected electrons can also diffuse laterally where they can be collected by tubs in the control circuitry. Should this interfere with the power-limiting circuitry, turning the output transistor back on, failure can result.



a) Clamping to V^+



b) Clamping to V^-

FIGURE 14. Equivalent circuits showing internal clamp activated by an inductive overload. The internal clamp diodes have a parasitic current that flows between supplies.

The substrate injection can be used to shut down the output transistor completely, as is indicated in *Figure 14a*. Even so, overheating can occur in the parasitic transistor, Q_2. It must dissipate a fraction (typically half) the overload current across the full supply voltage.

The region adjacent to the clamp diode is pre-heated by the initial overload. And the clamp has a higher thermal resistance than the power transistor because of its smaller size. This suggests that the energy that can be handled by the clamp diodes is strictly limited.

Since no practical method of reducing the parasitic current of clamp diodes in junction-isolated IC's has been found, external diodes must be used when the inductive energy is excessive. The diode in *Figure 10* can be designed with sufficient series impedance that an external clamp diode is effective when connected in parallel even if the IC is hot and the diode cold.

The collector tub of one output transistor will clamp the output to the substrate, which is connected to V^-. This diode injects electrons into the substrate that diffuse laterally to other tubs as represented by Q_2 in the equivalent circuit of *Figure 14b*. The power transistor with its collector connected to the output is ringed by a separate tub that is connected to V^-. Its purpose is to collect these electrons [22], but the effectiveness of the ring is limited. About half the injected electrons reach the power-transistor tub that is connected to V^+.

The electrons are collected and dissipate energy in the high-field region on the edge of the V^+ tub adjacent to the clamp. This region has been pre-heated by the initial overload and it is of limited area. Again, little energy can be handled safely.

The tub is not a low impedance diode, and its impedance is not easily tailored. An external clamp can divert considerable current under worst-case conditions. The situation has been found satisfactory for lighter inductive loads like loudspeakers. However, some motors can deliver enough sustained current to cause failures. This can be avoided by inserting another diode in series with the V^- lead of the op amp.

The substrate injection from forward-biased tubs can also affect the control circuitry. Again, it is necessary to insure that the overloaded power transistor is not turned back on. A positive method of accomplishing this is shown in *Figure 14b*. The overloaded transistor is shut off by Q_3 and Q_4 as the output approaches V^-.

performance

The major electrical specifications of the power op amp are summarized in *Table 1*. The input common mode range extends to within a volt of the positive supply and to 3V above the negative supply. No input-polarity reversal is experienced should the input voltage range be exceeded, and no damage results should the inputs be driven beyond the supplies. Recovery from output clipping at 20 kHz is clean, even when operated as a follower. Controlled turn-on is provided by the undervoltage shut-down that forces an open output until the supply voltage is sufficient to properly operate the circuit. Complete specifications, including guaranteed limits, have been published [23].

TABLE 1. Some typical characteristics of the LM12 for V_s = ±40V and T_C = 25˚C.

parameter	conditions	value
Input Offset Voltage	V_{CM} = 0	2 mV
Input Bias Current	V_{CM} = 0	150 nA
Voltage Gain	R_L = 4Ω	50V/mV
Output Voltage Swing	I_{OUT} = ±1.5A	±38V
	±10A	±35V
Peak Output Current	V_{OUT} = 0	±13A
Continuous dc Dissipation	T_C = 25˚C	90W
	100˚C	55W
Pulse Dissipation	t_{ON} = 10 ms	120W
	1 ms	240W
	0.2 ms	600W
Power Output	R_L = 4Ω	150W
Total Harmonic Distortion	R_L = 4Ω	0.01%
Bandwidth	A_V = 1	700 kHz
Slew Rate	R_L = 4Ω	9V/µs
Supply Current	I_{OUT} = 0	60 mA

conclusions

Limitations of monolithic ICs have delayed realization of high-performance push-pull power amplifiers. But, as shown here, the difficulties can be overcome. The intricacies of IC design can be applied to greatly reduce the silicon area required to guarantee a given level of performance. At the same time, many features can be incorporated with a negligible increase in cost. The die size of this op amp is about the same as that of one output transistor in equivalent discrete or hybrid designs.

Although development costs for achieving optimum performance can be high, they are insignificant when amortized over the lifetime of an industry-standard IC. There are many linear ICs that are still in volume production after more than eighteen years.

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