The MM58274C Adds Reliable Real-Time Keeping to Any Microprocessor System

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INTRODUCTION

When a Real-Time Clock (RTC) is to be added into a digital system, the designer will face a number of design constraints and problems that do not usually occur in normal systems. Attention to detail in both hardware and software design is necessary to ensure that a reliable and trouble free product is implemented.

The extra circuitry required for an RTC falls into three main groups: a precise oscillator to control real-time couting; a backup power source to maintain time-keeping when the main system power is removed; power failure detection and write protection circuitry. The MM58274C in common with most RTC devices uses an on-chip oscillator circuit and an external watch crystal (frequency 32.768 kHz) as the time reference. A battery is the usual source of backup power, along with circuitry to isolate the battery-backed clock from the rest of the system. Like any CMOS component, the RTC must be protected against data corruption when the main system power fails; a problem that is very often not fully appreciated.

Rather than dealing strictly with any one particular application, this applications note discusses all of the aspects involved in adding a reliable RTC function to a microprocessor system, with descriptions of suitable circuitry to achieve this. Hardware problems, component selection, and physical board layout are examined. The software examples given in the data sheet are explained and clarified, and some other software suggestions are presented. Finally a number of otherwise unrelated topics are lumped together under ''Miscellany''; including a discussion on how the MM58274C may be used directly to upgrade an existing MM58174A installation.

CONTENTS

1.0 HARDWARE

Selecting the correct components for the job and implementing a good board layout is crucial to developing an accurate and reliable Real-Time Clock function. The range of component choices available is large and the suitability of different types depends on the demands of the system.

1.1 COMPONENT SELECTION

With reference to *Figure 1*, the oscillator components and the battery are examined and the suitability of different types is discussed.

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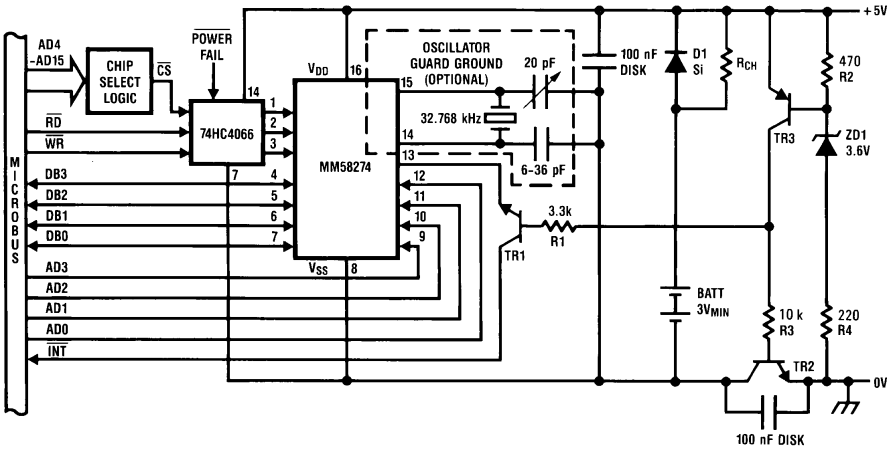

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FIGURE 1. MM58274C System Installation

1.1.1 Crystal

The oscillator is designed to work with a standard low power NT cut or XY Bar clock crystal of 32.768 kHz frequency. The circuit is a Pierce oscillator and is shown complete in *Figure 2*. The 20 MΩ resistor biases the oscillator into its linear region and ensures oscillator start-up. The 200 kΩ resistor prevents the oscillator amplifier from overdriving the crystal. If very low power crystals are used (i.e., less than 1 μW) an external resistor of around 200 kΩ may have to be added to reduce the drive to the crystal.

The oscillator will drive most normal watch crystals, with up to 20 μW drive available from the on-chip oscillator.

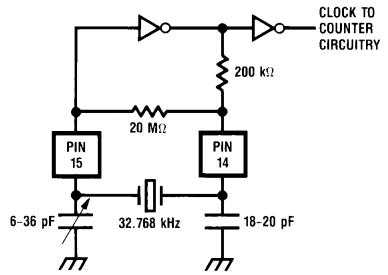

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FIGURE 2. Complete Oscillator Diagram

1.1.2 Loading Capacitors

Two capacitors are used to provide the correct output loading for the crystal. One is a fixed value capacitor in the range 18 pF–20 pF and the other is a variable 6 pF–36 pF trimmer capacitor. Adjusting the trimmer allows the crystal loading (and hence the oscillator frequency) to be fine tuned for optimal results.

The capacitors are the components most likely to affect the overall accuracy of the oscillator and care must be exercised in selection. Ceramic capacitors offer good operating temperature range with close tolerance and low temperature coefficients (typically ±3 ppm/K, for good quality examples). If trimming is undesirable a pair of close tolerance (±5% or better) capacitors in the range 18 pF–20 pF may be used. The average time-keeping accuracy for this configuration is within ±20 seconds per month.

1.1.3 Backup Battery

There are a number of different cell types available that can be used for time-keeping retention. Some cells are more suitable than others, and the way in which the system is used also influences the choice of cell. Ideally the standby voltage of the RTC should be kept as low as possible, as the supply current increases with increasing voltage *(Figure 3)*. Four different power sources are discussed: capacitors, nickel-cadmium rechargeable cells, alkaline and lithium primary cells.

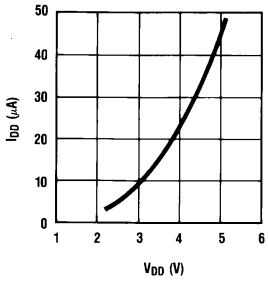

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FIGURE 3. Typical I_{DD} (μA) vs V_{DD} (V) for MM58274C in Standby Mode (T_A = 25°C)

Capacitors

When the system is permanently powered, and any long term removal of system power (i.e., more than a few hours) requires complete restarting, then a 1–2 Farad capacitor may be sufficient to run the clock during the power down. This can keep the clock running for 48–72 hours.

Nickel-Cadmium Cells

Nickel-cadmium (Ni-Cad) cells can be trickle-charged from the system power supply using a resistor as shown in *Figure 1*. The exact value of resistor used depends on the capacity and number of cells in the battery. Consult the manufacturers data for information on charging rates and times.

A 3- or 4-cell battery should be used to power the clock (the nominal battery voltages are 3.6V for 3 cells in series and 4.8V for 4 cells), with 3 cells preferable. PCB mounting batteries of 100 mAh capacity are available and these will give around 6 months data retention (at normal room temperature). For this cell type to be used the system must spend a large proportion of its time turned on to keep the battery charged (i.e., used daily).

Alkaline

Alkaline cells are among the least expensive primary cells which are suitable for use in real-time clock applications. They are available in a large range of capacities and shapes and have a very good storage (shelf) life.

Two cells in series will provide a nominal 3V, which is adequate to power the clock (via the isolating diode). The main problem with the alkaline system is that the cell terminal voltage drops slowly over the life of the cell. When the voltage at the clock supply pin drops to 2.2V, the cells must be replaced (battery voltage around 2.6V–2.7V). With present alkaline cells, this point is usually reached when the cells are only ½ to ⅔ discharged.

Provisions must be made either to check the battery voltage at regular intervals or to replace the cells regularly enough to avoid the danger of using discharged cells. Once again the manufacturers data regarding capacity and cell voltage against time must be examined to determine a suitable cell selection. A good alkaline system will supply 1–2 years continuous time-keeping.

Lithium

Lithium cells are the most suitable for real-time clock applications. A single cell with 3V potential is sufficient to power the system. The cell potential is very stable over use and the storage life is excellent. The energy density of lithium cells is very high, giving enough capacity in a physically small cell to power the clock continuously for at least 5 years (at room temperature using a 1,000 mAh cell).

Several cells which are recommended for RTC use are D2/3A*, D2A*, and 1/6DEL/P*. Each have 1,000 mAh capacity. These cells are available with solder pin connections for PCB mounting, giving a reliable backup supply.

Other Cells and Notes

There are many other types of cells, both primary and secondary, which may be adapted for RTC use. When selecting a cell type, attention must be paid to:

a. Cell capacity and physical size.
b. Storage (shelf) life.
c. Voltage variation over use.
d. Operating temperature range.
e. The method of battery connection and mounting.

In general, soldered cells are preferable to connector mounted cells. With replaceable batteries, the battery and connector contacts must be kept thoroughly clean. Dirty or corroded contacts can cause the clock to be starved of power, giving erratic and unreliable performance. The ease of operator access for cell replacement should also be considered.

Temperature Range

The performance of any cell will be satisfactory for most office or domestic environments. When ''ruggedized'' equipment is to be used (i.e., field portable equipment, automotive, etc.) the temperature specification of different cell types should be taken into account when selecting a cell. Lithium cells offer good performance over 0°C–70°C with little loss in capacity. Once again, the manufacturer's data should be examined to determine suitability, especially since different cells of the same type can have markedly different characteristics.

Few types of cells will offer any useful capacity at temperatures in or below the range 0°C–10°C, and fewer still will operate over the full military temperature range (−55°C to +125°C). Solid lithium cells and mercury-cadmium cells are two systems which can cover this range.

1.2 BOARD LAYOUT

1.2.1 Oscillator Connection

The oscillator components must be built as close to the pins of the clock chip as is physically possible. The ideal configuration is shown in *Figure 4*. From *Figure 2*, the oscillator circuit, it can be seen that both Osc In and Osc Out are high impedance nodes, susceptible to noise coupling from adjacent lines. Hence the oscillator should, as far as is practicable, be surrounded by a guard ground. The absolute maximum length of PCB tracking on either pin is 2.5 cm (1 inch). Longer tracks increase the parasitic track to track capacitances, increasing the risk of noise coupling and hence reducing the overall oscillator stability.

Where the system operates in humid or very cold environments (below 5°C), condensation or ice may form on the PCB. This has the effect of adding parasitic resistances and capacitances between pins 14 and 15, and also to ground. This variation in loading adversely affects the stability of the oscillator and in extreme cases may cause the oscillator to stop.

*Duracell Trade Number.
**Tadiran Trade Number.

Keeping the PCB tracks as short as possible will help to minimize the problem, and on its own this may be sufficient. Where the operating conditions are particularly severe, the PCB and oscillator components should be coated with a suitable water repellent material, such as lacquer or silicon grease (suitability being determined by the electrical properties of the materials—high impedance and low dielectric constant).

Figures 2 and *4* show the trimmer placed on Osc Out. The placement of the trimmer capacitor on either Osc In or Osc Out is not critical. Placing the trimmer on Osc Out yields a smaller trim range, but less susceptibility to changes in trimmer capacitance. Placement of the trimmer capacitor on Osc In gives a wider trim span, but slightly greater susceptibility to capacitance changes.

1.2.2 Battery Placement

For the battery, placement is less critical than with the oscillator components. Practical considerations are of greater importance now; i.e., accessibility. The battery should be placed where it is unlikely to be accidentally shorted or disconnected during routine operation and servicing of the equipment.

When replaceable cells are used, connecting a 100 μF capacitor across the RTC supply lines will keep the clock operating for 30–40 seconds with the battery disconnected *(Figure 5)*. This allows the battery to be replaced regardless of whether or not the main supply is active.

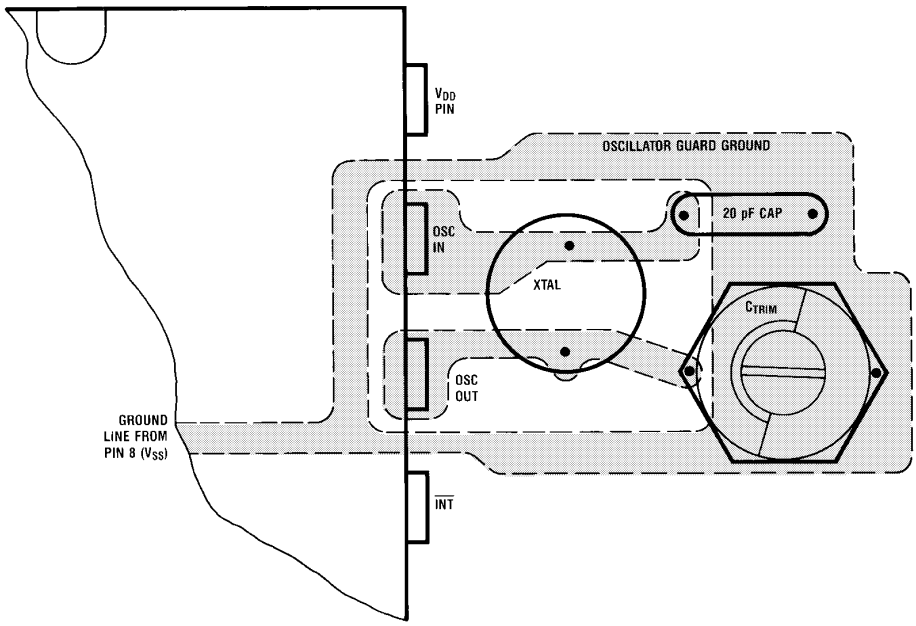

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FIGURE 4. Oscillator Board Layout

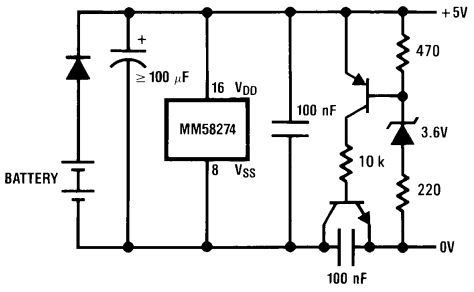

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FIGURE 5. Simplified Power Supply Diagram with 100 μF Capacitor Added

1.2.3 Other Components

The placement of the other RTC dedicated components (e.g., supply disconnection and power failure protection components) is not particularly critical. However, the same guidelines as applied to the battery should be followed when the PCB layout is designed.

1.3 POWER SUPPLY ISOLATION SCHEMES

1.3.1 The Need for Isolation

There are two reasons for disconnecting the clock circuit from the rest of the system:

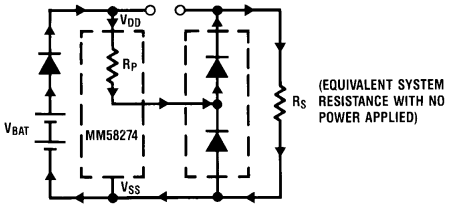
1. To prevent the backup battery from trying to power the whole system when the main power fails.
2. To minimize the battery current (and extend battery life) by preventing current leakage out of the RTC input pins.

The MM58274C inputs have internal pull-up devices which pull the inputs to V_{DD} in power down mode. This turns off the internal TTL input buffers and causes the μP interface functions of the clock to go to full CMOS logic levels, drawing no supply current (except for the unavoidable leakage current of the internal MOS transistors). For the MM58274C this is achieved by isolating the ground (V_{SS}) supply line from the rest of the system.

Figures 6a and *6b* show the two cases where first V_{DD} *(6a)* and then V_{SS} *(6b)* are open-circuited. The line out from the MM58274C represents any of the Control, Address, or Data lines on the RTC, with the internal pull-up resistor shown. The two diodes and resistor R_S represent the logic device connected to the RTC input and the resistance of the rest of the system with no power applied.

When V_{DD} is open-circuit as in *Figure 6a*, there is a complete current path, shown by the arrows, out of the RTC input and through the external circuitry. This battery current is a complete waste and serves only to reduce the cell life. Depending on the value of R_S, the voltage level at the pin may fall low enough to turn on the internal TTL level buffer, wasting further current as the buffer is no longer fully CMOS.

With V_{SS} disconnected *(Figure 6b)*, there is no return path to the battery and the pin is pulled completely up to V_{DD}. The TTL buffer is switched off and no power is lost.



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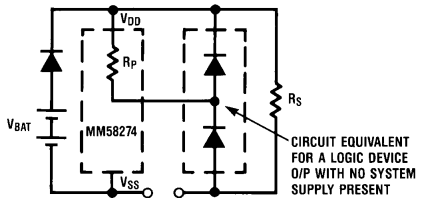
a) V_{DD} Disconnection



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b) V_{SS} Disconnection

FIGURE 6. Current Leakage Prevention by Proper Supply Disconnection

1.3.2 Isolation Techniques I—5V Supply Only

Figure 7 shows the isolation circuit suggested in the MM58274C data sheet. This circuit provides complete disconnection where only the system +5V is available for switching control.

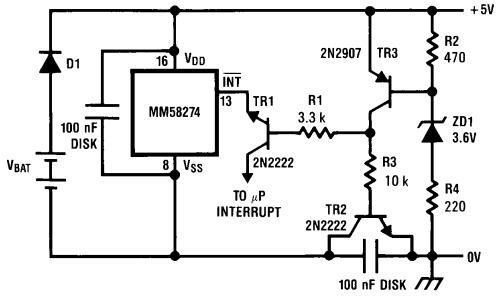

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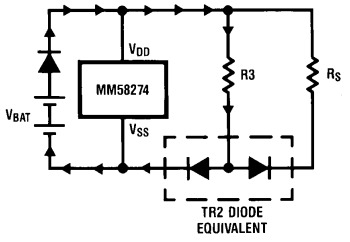
FIGURE 7. 5V Isolation Circuit

TR2 is the disconnecting device, which is controlled by TR3 and its associated circuitry. TR3 is turned on by its bias chain R2, ZD1, R4 as the system supply rises up to 4.2V. TR3 and R3 then turn on TR2 to connect the clock to the system supply. D1 isolates the backup battery when the system supply is active. The 100 nF disk capacitors decouple the supply during R/W operations and should be included in any disconnection scheme.

TR3 is necessary to prevent R3 and TR2 from leaking battery current in the power down condition. The circuit without TR3 is shown in *Figure 8* where TR2 has been replaced by equivalent diodes to clearly show the problem. The circuitry could be simplified by replacing TR3 with a Zener diode *(Figure 9)*. There will be a small loss of current down through TR2 however, as the Zener will pass a small leakage current at below its ''knee'' voltage. Thus the Zener should be selected for its low current capability.



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R_S = System Resistance with No Power Applied

FIGURE 8. Current Leakage in Simplified Disconnection Schemes

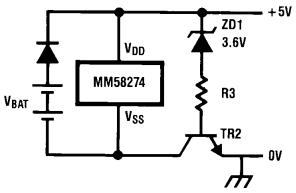

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FIGURE 9. Alternative Supply Disconnection Scheme Sensing 5V (Decoupling Capacitors Omitted for Clarity)

Finally TR1 and R1 *(Figure 7)* are optional components which are only required when the interrupt output is used. If interrupts are left programmed when the power fails, the interrupt timer will still time-out setting the interrupt output. Since this is an active low pull-down transistor it effectively shorts directly across TR2, destroying the RTC isolation and discharging the battery into the rest of the system *(Figure 10)*. In order to prevent this from occurring, TR1 and R1 are added.

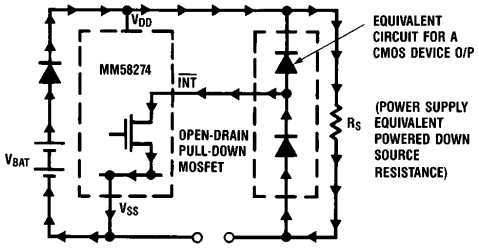

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FIGURE 10. Battery Discharge Path via Unisolated Interrupt Output

None of the disconnection components are at all critical, with general purpose transistors being completely adequate for the task. D1 should be a small-signal silicon or germanium diode.

1.3.3 Isolation Techniques II— Negative Supply Switched

Where a negative voltage supply is available (either regulated or unregulated) the circuit of *Figure 11* may be used. This is similar in operation to its diode equivalent shown in *Figure 12*, where the voltage drops across the diodes provide the correct potential to the clock. *Figure 11* has the advantage, however, that the clock power is supplied from the ground line by transistor action, rather than via the resistor as in *Figure 12*. Less lower is dissipated in the resistor as only transistor bias current need be drawn.

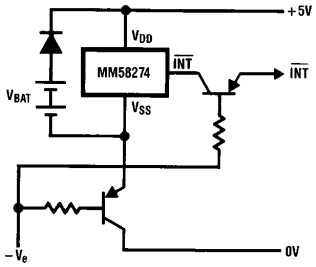

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FIGURE 11. Negative Voltage Driven Supply Disconnection Scheme (Decoupling Capacitors Omitted for Clarity)

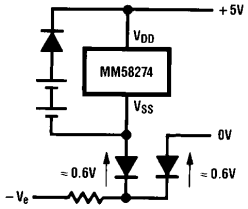

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FIGURE 12. Diode Equivalent Circuit of *Figure 11*

1.3.4 Other Methods

There are many other possibilities for supply disconnection schemes, i.e., relay disconnection. When designing a disconnection scheme, the performance must be analyzed both with the system power applied and with system power absent. Check for leakage paths and undue voltage drops and try to set up so that disconnection and reconnection will take place as near to the backup voltage as possible.

1.4 POWER FAIL PROTECTION

One of the major causes of unreliability in RTC designs is due to inadequate power failure protection. As the system is powered up and down, the μP and surrounding logic can produce numerous spurious signals, including spurious writes and illegal control signals (i.e., RD and WR both active together).

Bipolar logic devices can produce spikes and glitches as the internal biasing switches off around 3V–3.5V, and the transistors operate in their linear region for a short time. Any such spurious signals, if applied to the RTC, could cause the time data to be corrupted. Systems using 74HC logic and CMOS processors are less stringent in their power failure requirements as the devices tend to work right down to around 2V. Some form of write protection is still required, however.

In order to protect the time data, the system must be physically prevented from writing to the clock when the power supply is not stable. The ideal situation is to ban Write access to the clock before the system +5V starts to fail, and then keep the chip ''locked-out'' until the power is restored and stabilized. This ideal access control signal is illustrated in *Figure 13*.

Three methods of power fail protection are discussed, although there are also many other possibilities.

1.4.1 Write Protect Switch

By far the simplest and potentially the most hazard-free method is to use a switch on the WR control line to the clock *(Figure 14)*. This is completely adequate, but requires the intervention of an operator to alter time data or program interrupts.

Some thought must be given to ensuring that the operator cannot accidentally leave the WR line switched in. This may be achieved by the physical access method used (i.e., the machine is impossible to operate or switch off when in the time setting mode, because of the placement of access hatches, etc.) or with software. The switch state could be sensed by trying to alter the data in the Tens of Years counter or Interrupt register just prior to leaving the clock setting routine, and refusing to leave the routine until the WR switch has been opened. The switch condition should similarly be checked whenever the system is initialized or reset.

The physical location of the switch should also be considered for ease of accessibility. How easy the switch is to reach will depend on the system; i.e., in some cases a ''tamper proof'' clock may be required.

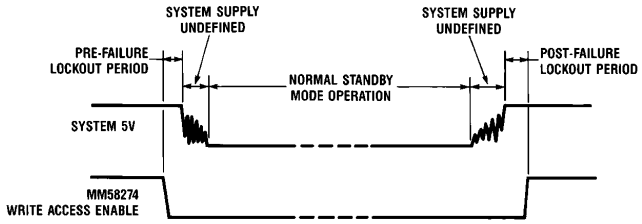

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FIGURE 13. RTC Access Lockout Definition

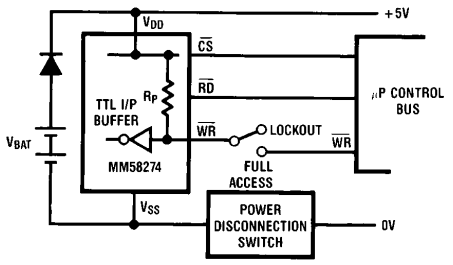

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FIGURE 14. Write Protection by Manually Switching WR

1.4.2 5V Sensing

The circuit of *Figure 15* senses the system 5V supply and prevents access to the clock if the supply falls below 4.2V–4.3V. This circuit should be used where only the system 5V is available for reference. The LM139 comparator and associated components sense the 5V supply and generate the power fail signal (P.Fail). The 74HC75 and components disconnect the WR line.

R3 and ZD1 provide a reference voltage of 2V–3V for the comparator. R4 and VR1 form a potential divider chain sensing the 5V line, and VR1 is adjusted to switch the comparator output at 4.2V–4.3V. An alternative to VR1 would be to use a pair of close tolerance resistors (±2%) with values selected to suit the Zener diode reference used. The combination of R4, D3 and C2 provide an RC time constant to delay the comparator when sensing the return of 5V (to provide the post-failure delay in *Figure 13*). The LM139 has an open-collector output which is held low when 5V is present and is switched off when 5V fails. This line is pulled high by R5 to flag power failure (P.Fail). Since the comparator is a linear device drawing a bias current, it is powered by the system 5V supply to avoid consuming battery power.

One 74HC75 package contains four latches, of which two are used. These are transparent latches controlled by the "G" input. With G high, the latch is transparent and the Q and $\overline{Q}$ outputs follow the Data input. When G is low, the state of Q and $\overline{Q}$ on the falling edge is latched. In this way, F2 prevents P.Fail from locking out the clock if there is a Write cycle in progress. F1 isolates the WR input on the clock when F2 passes the P.Fail signal. C1, R2 and D1 do not slow the advent of P.Fail, but they cause a delay in the release of the function to mask any comparator noise or oscillation as the comparator switches off or on (i.e., during the undefined supply periods).

D2, C3 and R6 smooth the comparator supply and help it to function effectively. The time constants of the RC networks should be selected to suit the power supply of the system that is used. Comparing the functioning of this circuit with the ideal case of *Figure 13* shows that most of the conditions can be satisfied, except that there is no real pre-failure lock-out period. This cannot be achieved without some form of look ahead power failure.

As an alternative to F1 a permanently powered 74HC4066 analog switch could be used as the isolating component *(Figure 16)*. The 74HC4066 does not require pull-up resistors on its inputs as there are no internal CMOS buffers inside this device which must be controlled. The resistor on the WR line is for the benefit of the 74HC75.

Note that both of the devices mentioned must be permanently powered from the battery to be useful in this way. Unused gates in any such device must *NOT* be used in combinational logic that is not permanently powered. All unused inputs should be tied to V_{DD} or V_{SS} to render them inactive.

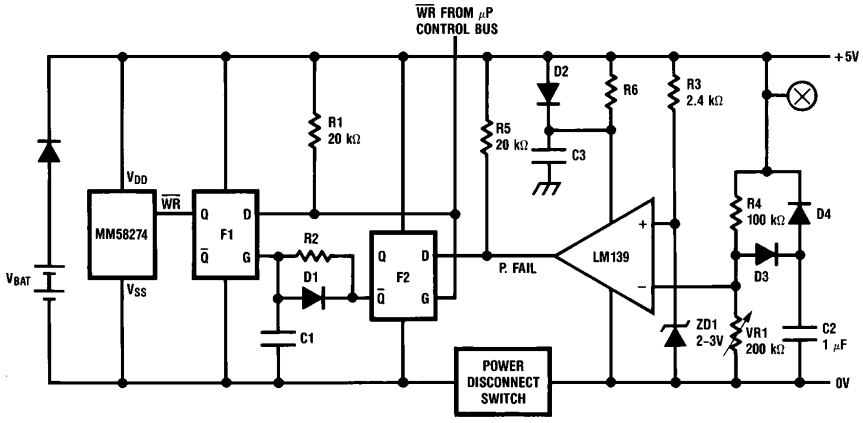

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FIGURE 15. Power Supply Failure Detection and Write Protection Circuitry

1.4.3 Supply Pre-Sense

The same circuit of *Figure 15* can be used with unregulated supplies or other voltage lines which will fail before the 5V line. To achieve this, point X is connected to the sensed voltage instead of 5V, and the R4/VR1 ratio is adjusted to suit. The major benefit here is that advance warning of an impending 5V failure can be detected, allowing a pre-failure lockout signal to be generated.

Less precision is required to sense the unregulated supply than the system 5V supply. Consequently less complex circuitry can be used to do the detection and this is reflected in the circuit of *Figure 17*. Most 5V regulators will operate with an input voltage from 7V to 25V. Typically the input voltage is around 9V to 12V, giving some headroom. In *Figure 17* this voltage is high enough to drive a current through the Zener diode and turn on transistor TR1, holding P.Fail low. R_{LIM} limits the Zener current. The Zener voltage is selected to switch off before the regulator fails, around 7.5V–8.5V depending on the time constant of the supply. With no current, TR1 switches off and R_P pulls P.Fail high.

When power is re-applied the 5V supply will stabilize before the Zener switches on, removing P.Fail. To provide a longer post-failure lockout period R_{LIM} could be replaced with two resistors and a diode/capacitor delay as in *Figure 15*.

Figure 18 is another extension of the same basic idea to provide an advance interrupt signal to allow μP housekeeping before the RTC (and CMOS RAM) is locked out. The extra rectifying components D1, C_t and R_t keep $\overline{NMI}$ off as long as input power is present. Time constant τ_2 is selected to be at 2–3 times faster than τ_1, the supply time constant. The interrupt signal is thus asserted before P.Fail.

1.4.4 Switching Power Supplies

Switching power supplies are available which generate power failure signals. This signal may be adequate for direct use as a P.Fail line, but the manufacturer's information should be consulted to determine the suitability of a given power unit. P.Fail must still be gated with the Write signal for the clock, regardless of the actual detection method employed.

1.4.5 Summary

The general guidelines for power fail protection are:

1. Physically isolate the WR input to the clock. The μP cannot be relied upon to logically operate the isolation mechanism.
2. The clock should be isolated before the 5V power line starts to fail, and stay isolated until after it has reestablished.
3. Consider the action of the sensing and protection circuitry if the supplies oscillate or if a momentary glitch occurs.
4. The Power Fail signal must be gated with Write strobes to the RTC. A foreshortened Write may also cause data corruption.
5. Logic components (and ICs in general) should be avoided when designing power failure schemes. Discrete components are far more predictable in their performance when the power supplies are not well defined. The exception to this general rule is when using permanently powered HCMOS logic devices. They will function in a reliable manner down to 2V.

System-powered logic devices cannot be relied on for power failure or Write isolation (not even CMOS).

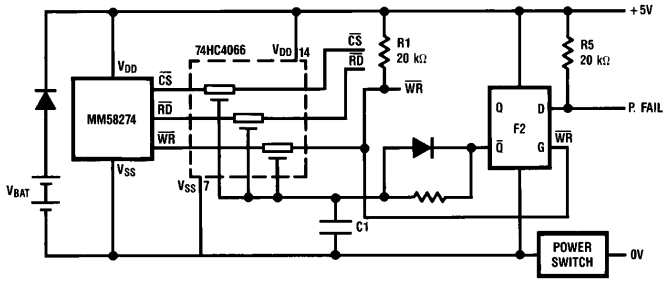

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FIGURE 16. F1 Replaced by a 74HC4066 Analog Switch (Pull-Up Resistors Not Required on $\overline{CS}$ or $\overline{RD}$ Inputs)

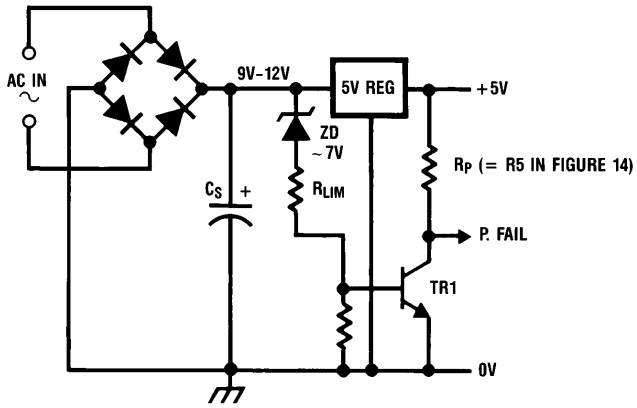

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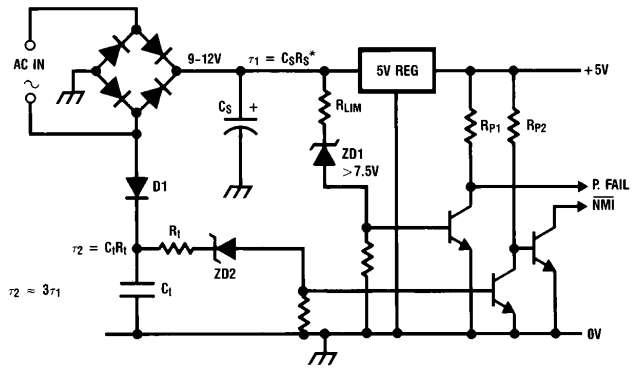
FIGURE 17. Power Fail Signal Generation from Unregulated Supplies



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*R_S = Equivalent Resistance of the System.

FIGURE 18. Power Fail Circuit with μP Housekeeping Interrupt

2.0 SOFTWARE

2.1 DATA VALIDATION

The MM58274C data sheet describes in some detail three different methods of reading the clock and validating the real-time data. These techniques are reproduced in Appendix A-1. Rather than repeating the data sheet examples, this applications note examines the principles that lie behind the techniques suggested.

The basic problem is that the μP must somehow be synchronized with the changes in real-time in order to read valid data. This synchronization can either be done prior to reading the time data (pre-read), or after reading the data (post-read synchronization).

2.1.1 Post-Read Synchronization

Using the Data-Changed Flag (DCF) or the lowest order time register as outlined in the appendix: Time Reading using DCF and Time Reading with very slow Read cycles; are both examples of post-read synchronization.

What this means is that the data is read out first, and then verified. This is achieved by defining a random time-slot, started by the first DCF or low order register read, and ended by the second such read. If DCF has not been set during the time-slot or the lowest order register has not changed, then no real-time change occurred during that time-slot. All real-time reads during the time-slot are thus guaranteed.

2.1.2 Pre-Read Synchronization

The Interrupt Timer technique uses pre-read synchronization. Once it has been initialized as described, the interrupt timer times out just after the real-time data has changed. Thus the μP is guaranteed a full 100 ms period in which to read the time counters before the next change occurs.

The interrupt timer has to be synchronized with the real-time counters because it is an independent unit which may be started and stopped at any time by the μP. This software synchronization is achieved by using another pre-read technique. The timer is set up and ready to go, but then the μP waits for DCF to occur before issuing the start command. The same technique could be used to actually read the time-data, but post-read synchronization is faster.

2.2 INTERRUPT AS A "DATA-CHANGED" FLAG

DCF is set every 100 ms when the 1/10ths of seconds counter is changed. When the time is only being read to the nearest second or minute, it would be useful to have a flag which is only set by a change in the lowest order counter being used.

If the interrupt output from the clock is not being used, the timer can be used as a programmable data-changed flag. To achieve this, the timer is set up and started in exactly the same way as described for interrupt time reading (Appendix A-1). The interrupt output, however, should be left unconnected. When reading the real-time data, the technique used is the same as for the normal Data-Changed Flag except that the Interrupt Flag is tested instead of DCF.

Note that the lowest order real-time register which is to be read out should be used to initially synchronize the counter. The interrupt timer is started when the real-time counter value is seen to change.

2.3 WRITING WITHOUT HALTING TIME-KEEPING

For most purposes the RTC should be halted when the time is being set, especially if large numbers of counters are being updated. The clock can also then be re-started in synchronism with an external time reference. If only a few counters are to be altered and the clock is already synchronized, then this can be done without stopping the clock. An example of a minor change which may be undertaken in this way is daylight savings (winter/summer change of hour).

The problem to be overcome when writing in this way is that the write strobe may coincide with a time change pulse. As the time counters are synchronous, the 100 ms clock pulse is fed to each one. Writing to one counter may cause a spurious carry to be generated from that counter, causing the next one up the chain to be incremented.

Since a spurious carry will only affect the next counter if it coincides with a time update pulse, the solution is once again to synchronize clock access with the real-time change. The most suitable method for this is pre-read synchronization. In other words, the μP must wait for DCF to be set before starting to write data to the clock, giving a guaranteed 100 ms period for writing.

2.4 THE CLOCK AS A μP WATCHDOG

The interrupt timer can be used as a μP watchdog circuit, operating on a non-maskable interrupt input to the μP. The timer is set up in either single or repeat interrupt mode for the watchdog period required: 0.1s, 0.5s or 1 second are probably the most useful times for this. Synchronization with real-time is not required.

In the main program loop the μP writes to the clock, stopping and then re-starting the interrupt timer. The timer period selected will depend on how long the main loop takes to execute. As long as the μP continues to execute the loop, no time-outs occur and no interrupts are generated. If the μP fails for some reason to reset the timer, it eventually times out, generating the initializing interrupt to restore operations.

2.5 THE JAPANESE CALENDAR

Because the MM58274C has a programmable leap year counter, this allows the possibility of programming for the Japanese Showa calendar. The Japanese calender counts years from the time that the present Japanese Emperor comes to power.

The normal procedure for the MM58274C is to program "the number of years since last leap year." This remains the same whether the clock is loaded with the Gregorian or Showa year. When software is used to calculate the leap year count value from the year, then the formula used must be modified.

The formula for the Gregorian year is:

Leap Year Value = [Gregorian Year/4] REMAINDER

Whereas for the Showa year the formula is:

Leap Year Value = [(Showa Year + 1)/4] REMAINDER

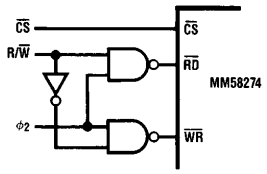
Leap Year Value is the number from 0 to 3 which is written into the leap year counter, and is the REMAINDER of the integer calculations shown above.

3.0 MISCELLANY

3.1 CONNECTION TO NON Microbus™ SYSTEMS

Adding the MM58274C to non Microbus processors is made fairly straightforward because of the flexibility of the control signal timing. *Figure 19* shows two examples of logic to connect to clock to a 6502/6800 microprocessor bus.

Figure 19a the $\overline{RD}$ and $\overline{WR}$ inputs are strobed, generating reasonably typical Microbus type control signals. In *Figure 19b*, CS is used as the strobe signal. There is no particular advantage to either circuit, they are just variations on the same theme. This circuit flexibility may be used to advantage to save SSI packages in the board design.



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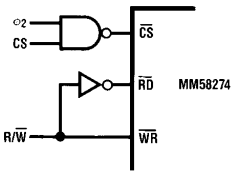
a)



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b)

FIGURE 19. 6800/6502 μP Bus Interface

3.2 TEST MODE

Test Mode is used by National Semiconductor when the MM58274C is tested during manufacture. It enables the real-time counters to be clocked rapidly through their full count sequence.

The MM58274C counters are clocked synchronously to simplify μP access, with ripple carry signals from each counter to the next. In Test Mode some of these carries are intercepted and permanently asserted causing the counters to count each clock pulse. The prescaler is also bypassed so that the counters count every clock applied to the Osc In pin. The Test Mode counter connection is shown in *Figure 20*.

If Test Mode is to be used for incoming inspection or device verification, then the clock waveform of *Figure 21* should be applied to the oscillator input (Osc In, pin 15). The MM58274C uses semi-dynamic flip-flops in the counters which are only fully static when the oscillator input is high. Thus *Figure 21* shows that the oscillator waveform is normally high, pulsing low to clock the real-time counters. The time data in the counters changes on the rising edge of Osc In.

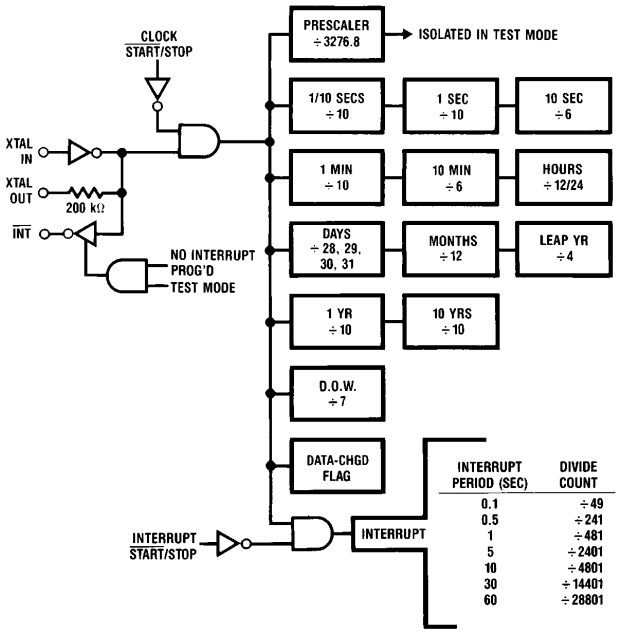

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FIGURE 20. Test Mode Interconnection Diagram of Internal Counter Stages

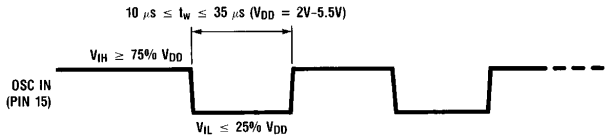

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FIGURE 21. Oscillator Waveform for Counter Clocking in Test Mode

The pulse width limits for reliable clocking are shown on the diagram. When running with a 32 kHz crystal, the normal pulse width is 15.26 μs. With no forcing input, the oscillator will self bias to around 2.5V (V_{DD} = 5V). While a few hundred mV swing above and below this level is sufficient to drive the oscillator, for guaranteed test clocking the input should swing between $V_{IH} \geq 75\%\ V_{DD}$ and $V_{IL} \leq 25\%\ V_{DD}$.

3.3 TEST MODE AND OSCILLATOR SETTING

When Test Mode is used to set the oscillator frequency, the interrupt timer must be disabled (interrupt register programmed with all 0s) for the oscillator frequency to appear on the interrupt output. No test equipment should be connected directly to either oscillator pin, as the added loading will alter the characteristics of the oscillator making precise tuning impossible.

Note that oscillator frequency will vary slightly as the supply varies between operating and standby voltages. Typically this variation will be around ± 6 seconds per month ($V_{STANDBY}$ = 2.4V), slowing at standby voltage. When the clock will spend the greater part of its working life in standby mode, it may prove worthwhile to correct for this in the tuning. This can be done by tuning at standby voltage (by writing the RTC into test mode, then disconnecting it from the system to tune on battery backup). Alternatively, the clock can be slightly overtuned at operational voltage, tuning to 32.7681 kHz.

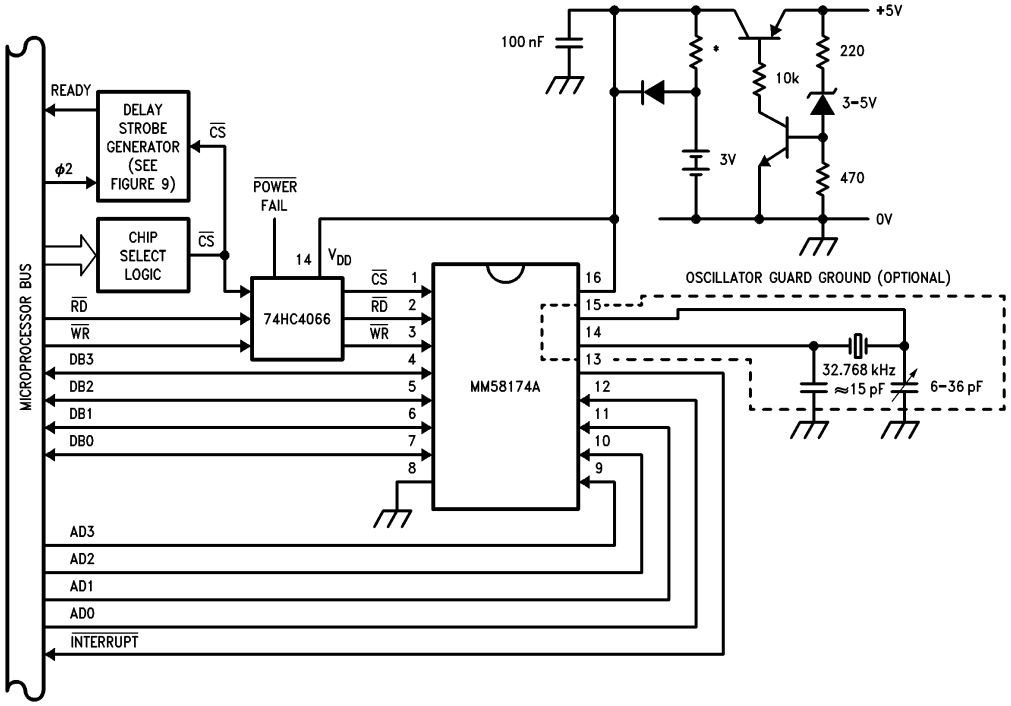
In a similar way, where the RTC spends equal amounts of time in both operational and standby modes (i.e., powered by day, standby at night), the oscillator may be tuned somewhere between the two conditions. Following these tuning suggestions will not eliminate time-keeping errors, but they will help in minimizing them.

Time-keeping accuracy cannot be exactly specified. It depends on the quality of the components used in the oscillator circuit and their physical layout, also the stability of the supply voltage, the variations in ambient temperture, etc. With good components and a reasonably stable environment however, time-keeping accuracy to within 4 seconds/month can be achieved, although 8 seconds/month is somewhat more typical in practical systems.

3.4 UPGRADING AN MM58174A SYSTEM WITH THE MM58274C

The MM58274C has the same pin-out as the MM58174A and can be used as a direct replacement, with certain reservations. The two devices are not quite the same in their external circuit appearances, and this is reflected in their applications circuits. In addition, the MM58274C is not software compatible with the MM58174A, requiring a change in the operating system to use the MM58274C.

Figure 22 shows the circuit diagram for the MM58174A system connection. There are two major differences between this and the MM58274C diagram *(Figure 1);* a) the oscillator circuit and b) the supply disconnection scheme.



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*Use resistor with Ni-Cad cells only.

FIGURE 22. MM58174A System Installation

a) The Oscillator Circuit

The MM58274C normally operates with an 18 pF–20 pF fixed loading capacitor as opposed to the 15 pF of the MM58174A. This is a reflection of the greater internal capacitance of the MM58174A, rather than any change in the characteristics of the oscillator itself. The MM58274C will operate using a 15 pF capacitor, but the oscillator will probably need to be retrimmed.

Operating with a 15 pF capacitor will make the oscillator more sensitive to change in the environment, i.e., temperature, voltage, moisture, etc. This will result in lower accuracy in time-keeping. The oscillator is more prone to stopping at low voltage. Oscillation would normally be maintained down to 1.8V–1.9V (although not guaranteed); with a 15 pF load it may only oscillate down to 2.0V–2.1V. It is thus important to check the battery regularly and replace it before the RTC voltage falls below 2.2V.

Where possible the 15 pF capacitor should be replaced by an 18 pF–20 pF capacitor (anywhere in the range 18 pF–20 pF is adequate), or a second 3 pF–5 pF capacitor may be added in parallel with the 15 pF.

Note: When components have been soldered into the oscillator circuit, allow the circuit to cool to room temperature before attempting to retune the oscillator.

The change of pin of the tuning capacitor (from OSC Out to Osc In) is not critical.

b) The Supply Disconnection Scheme

The MM58174A uses mostly pull-down devices on its μP inputs to pull the inputs to CMOS levels, and so the 5V power line is disconnected on this device. The two exceptions to this are the $\overline{CS}$ and $\overline{WR}$ inputs which have pull-up resistors to inactivate the internal write strobe. As *Figure 5a* shows, there is a leakage path through these pins, which in most MM58174A installations are individually isolated.

The largest penalty in inserting an MM58274C into an MM58174A circuit is the battery current that is lost through the pull-up devices. This will increase the typical supply current from 4 μA to 50–100 μA and it is up to the individual user to decide whether or not this drain is tolerable in a particular application.

The most important requirement is that the $\overline{WR}$ input should be electrically isolated or current leakage through pin inputs may force the inputs low enough to cause spurious writes to occur. Since it is already customary to isolate these inputs for the MM58174A, this may not be a problem. Where this has not been done, either the circuit will have to be modified or the $\overline{WR}$ PCB track can be cut and a switch or some extra circuitry added to allow isolation.

Note that power fail disconnection and input isolation may be achieved using the same components. In *Figure 22* the MM74HC4066 analog switch will do both jobs.

The current drained by the input pull-ups may be minimized with some attention to the data/address driving devices. It is often possible to replace LSTTL devices with standard 7400 series devices and reduce the leakage (at the cost of some increase in operating current). Many 7400 series device outputs lack diodes in the right places to pass leakage currents. LSTTL devices will, for the main part, have these diodes. CMOS devices will always have diodes to both power rails on inputs and outputs.

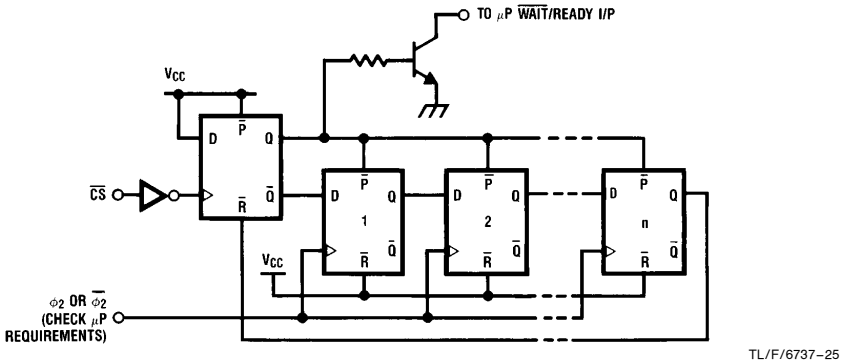
There is no hard and fast rule for this. Where devices from one manufacturer work, the same part from a different one may not. Some trial and error experimentation may prove worthwhile in selected devices.

3.5 WAIT STATE GENERATION FOR FAST μPs

Although the MM58274C has faster access times than the MM58174A, in many cases, the μP will be too fast to directly access the RTC. *Figure 23* shows a circuit which will produce wait states of any length required to enable the RTC to be accessed, using the 74HC74 dual D-type flip-flop.

The RTC $\overline{CS}$ signal clocks up a logic 1 on the Q output of the first F/F, removing the Preset from all the other F/Fs and pulling the μP WAIT line low, via the transistor. The other F/Fs 1 to n, form a shift register clocked by the ϕ_2 system clock.

After n ϕ_2 clocks (where n is the number of flip-flops in the shift register) a logic 0 shifts out from the nth F/F, resetting the main flip-flop. The main F/F then presets the shift register and clears the WAIT signal, ready for the next $\overline{CS}$ edge to repeat the cycle. On power-up the delay generator will initialize itself after a maximum of n system clocks have occurred so no reset signal is required. Some μPs demand that a $\overline{WAIT}$/READY input is synchronized with ϕ_2 of the system clock. This can readily be achieved by selecting the correct ϕ_2 edge as the clock signal for the shift register chain.



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Flip-Flop—MM74HC74 D-Type Latch

FIGURE 23. Access Delay Generator (Clocked Wait State Generator)

APPENDIX A-1. READING VALID REAL-TIME DATA

TIME READING USING DCF

Using the Data-Changed Flag (DCF) technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1. Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*
2. Read time registers: *All desired time registers are read out in a block.*
3. Read the control register and test DCF: *If DCF is still clear (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

TIME READING USING AN INTERRUPT

In systems such as point-of-sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined above is ideal for this type of system. Where the μP must respond to any change in real-time (e.g., industrial timers/process controllers, TV/VCR clocks or any system where real-time is displayed) then the interrupt timer may be for time reading. Software is used to synchronize the interrupt timer with the time changing as outlined below:

1. Select the interrupt register (write 2 or 3 to ADDR0).
2. Program for repeated interrupts of the desired time interval (see Table IIb in Appendix A-2): *Do not start the timer yet*.
3. Read control register AD0: *This is a dummy read to reset the data-changed flag.*
4. Read control register AD0 repeatedly until data-changed flag is set.
5. Write 0 or 2 to control register. Interrupt timing commences.

When interrupt occurs, read out all required time data. There is no need to test DCF as the interrupt ''pre-synchronizes'' the time reading already. The interrupt flag is automatically reset by reading from ADDR0 to test it. In repeat interrupt mode, the timer continues to run with no further μP intervention necessary.

TIME READING WITH VERY SLOW READ CYCLES

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used or where high level interpreted language routines are used) then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1. Read and store the value of the *lowest* order time register required.
2. Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.
3. Re-read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no other register has changed either.

APPENDIX A-2. FUNCTIONAL TRUTH TABLES FOR MM58274C

TABLE I. Address Decoding for Internal Registers

Register Selected	Address Bits				Access
	AD3	AD2	AD1	AD0	
0 Control Register	0	0	0	0	Split Read and Write
1 Tenths of Secs	0	0	0	1	Read Only
2 Units Seconds	0	0	1	0	R/W
3 Tens Seconds	0	0	1	1	R/W
4 Units Minutes	0	1	0	0	R/W
5 Tens Minutes	0	1	0	1	R/W
6 Units Hours	0	1	1	0	R/W
7 Tens Hours	0	1	1	1	R/W
8 Units Days	1	0	0	0	R/W
9 Tens Days	1	0	0	1	R/W
10 Units Months	1	0	1	0	R/W
11 Tens Months	1	0	1	1	R/W
12 Units Years	1	1	0	0	R/W
13 Tens Years	1	1	0	1	R/W
14 Day of Week	1	1	1	0	R/W
15 Clock Setting/Interrupt Registers	1	1	1	1	R/W

TABLE IIa. Clock Setting Register Layout

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12 Hour Mode)			X		0 = AM 1 = PM 0 in 24 Hour Mode	R/W
12–24 Hour Select Bit				X	0 = 12 Hour Mode 1 = 24 Hour Mode	R/W

TABLE IIb. Interrupt Control Register

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt Output Cleared, Start/Stop Bit Set to 1.	X	0	0	0
0.1 Second		0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1

Timing Accuracy:
Single Interrupt Mode (all time delays): ±1 ms
Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).

DB3 = 0 for Single Interrupt DB3 = 1 for Repeated Interrupt

TABLE III. The Control Register Layout

Access (ADDR0)	DB3	DB2	DB1	DB0
Reaf From:	Data Changed Flag	0	0	Interrupt Flag
Write To:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clk. Set Reg. 1 = Int. Reg.	Interrupt Start/Stop 0 = Int. Run 1 = Int. Stop

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