CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
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SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters—2 of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 ½-digit DPM and ADD3701 3 ¾-digit DPM) while the other 2 (ADC3511 3 ½-digit A/D and ADC3711 3 ¾-digit A/D) have addressable BCD outputs. These last 2 devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 ½-digit types divide the input into 2,000 counts plus sign, while the 3 ¾-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 ½-digit converters require 200 ms per conversion; 3 ¾-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the supply must be isolated from the inputs. Without an isolated supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

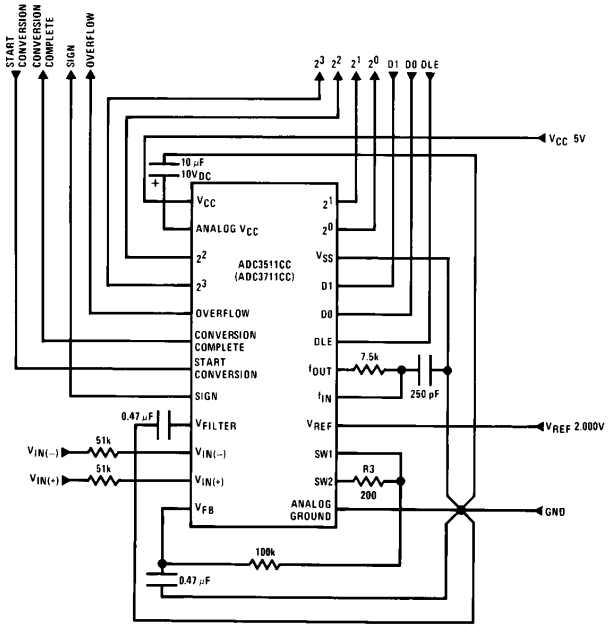

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FIGURE 1. Basic A/D Converter

RRD-B30M115/Printed in U. S. A.

BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal ''EEEE'' plus an Overflow output.

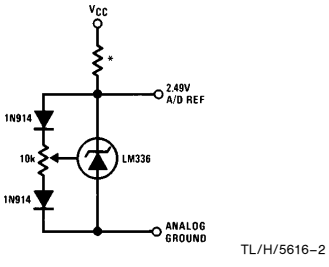
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*.



$$*R = \frac{2.49V}{(2N + 1)\ mA}\quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

One reference can be used for many A/D's. The values of the upper series resistor R1 depends on the number of converters used.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3* and *4*. *Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multi-channel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a ''1'' is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a ''1'' in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of ''1's'' in the status word. The routine loads the address pointer to digit 4 of the selected converter. The

program then calls a subroutine which goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

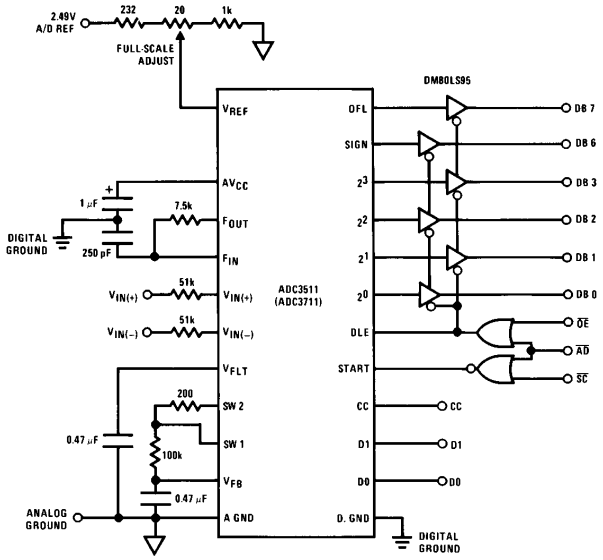


FIGURE 3. Dual Polarity A/D Requires that Inputs are Isolated from the Supply. Input Range Is ±1.999V.

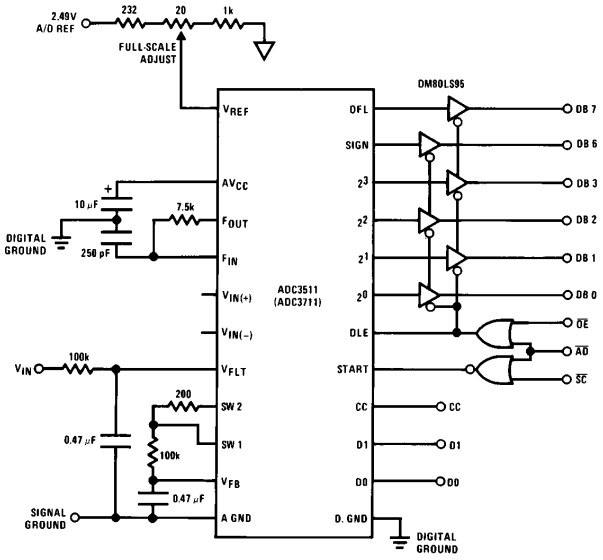


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FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range Is + 1.999V.

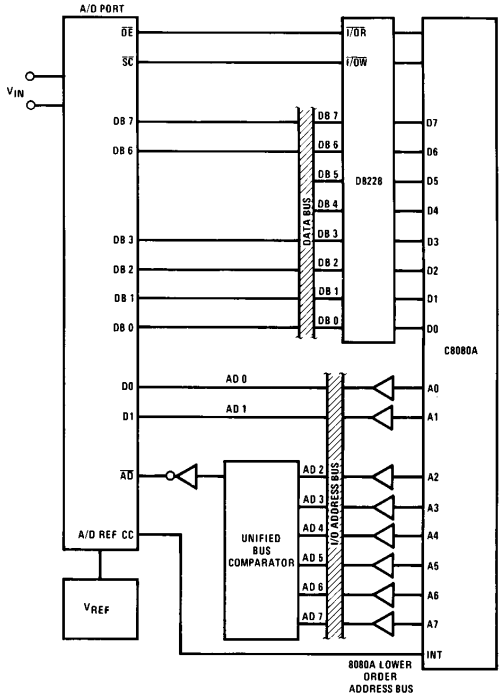

FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

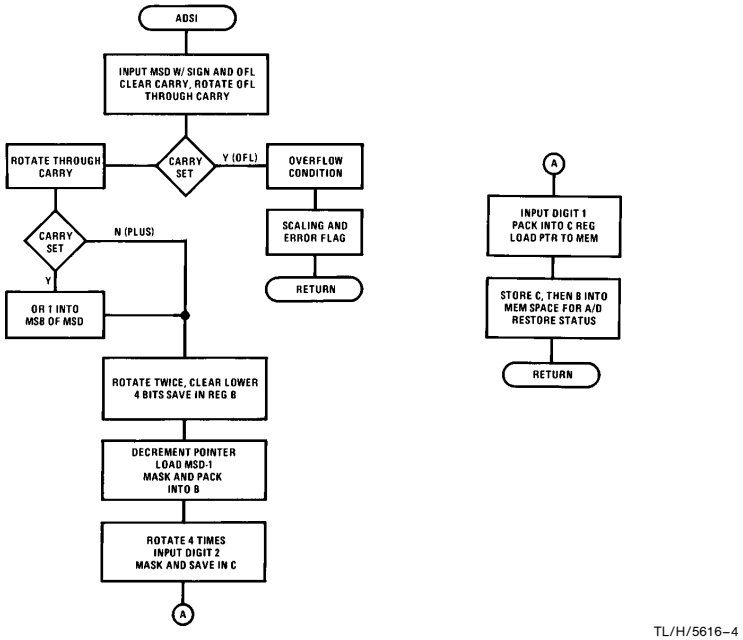

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FIGURE 6. Flow Chart for Single Channel A/D Converter

Routine 1. Single Channel Interrupt Service Routine

LABEL	OPCODE	OPERAND	COMMENT
ADIS:	PUSH	PSW	; A/D interrupt service
	PUSH	H	; save
	PUSH	B	; current status
	IN	ADD 4	; input A/D digit 4
	IN	ADD 4	; delay
	ORA		; reset carry
	RAL		; rotate OFL thru carry
	JC	OFL	; overflow condition
	RAL		; rotate sign thru carry
	JC	PLUS	; positive input
	ORI	20H	; OR 1 into MSB, neg input
PLUS:	RAL		; shift
	RAL		; into position
	ANI	FO	; mask lower bits
	MOV	BA	; save in B
	IN	ADD 3	; input digit 3
	IN	ADD 3	; delay
	ANI	OF	; mask higher bits
	OR	B	; pack into B
	MOV	B, A	; save in B
	IN	ADD 2	; input digit 2
	IN	ADD 2	; delay
	RAL		; rotate
	RAL		; into
	RAL		; upper
	RAL		; 4 bits
	ANI	FO	; mask lower bits
	MOV	C, A	; save in C
	IN	ADD 1	; in digit 1
	IN	ADD 1	; delay
	ANI	OF	; mask upper bits
	OR	C	; pack
	MOV	C, A	; save in C
	LXI	H, ADMS	; load ptr to A/D ; Mem, space
	MOV	M, C	; save C in memory
	INX	H	; point next
	MOV	M, B	; save B in memory
	OUT	ADD 1	; start new conversion
	POP	B	; restore
	POP	H	; previous
	POP	PSW	; status
	EI		; enable interrupts
	RET		; return to main program

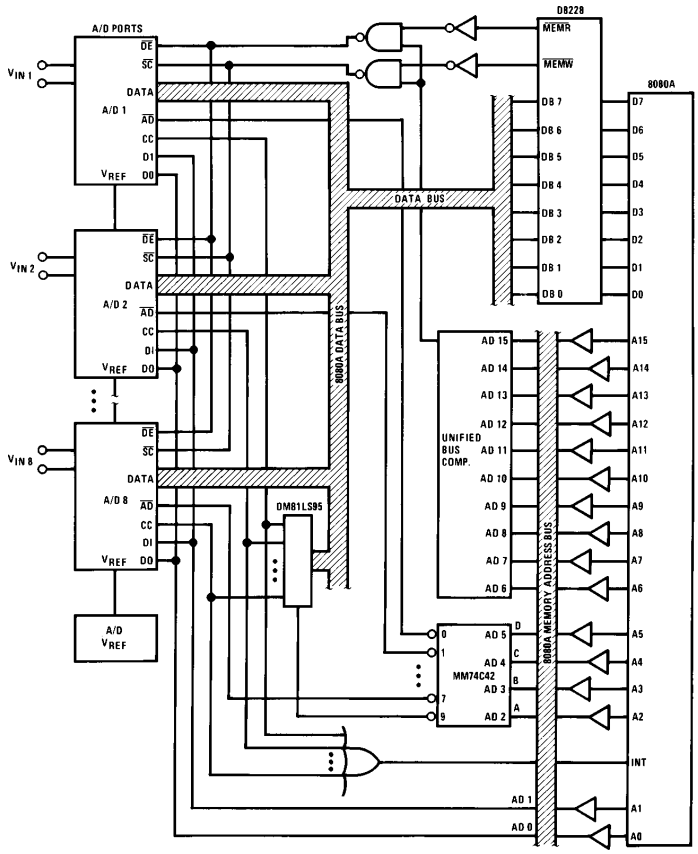

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FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

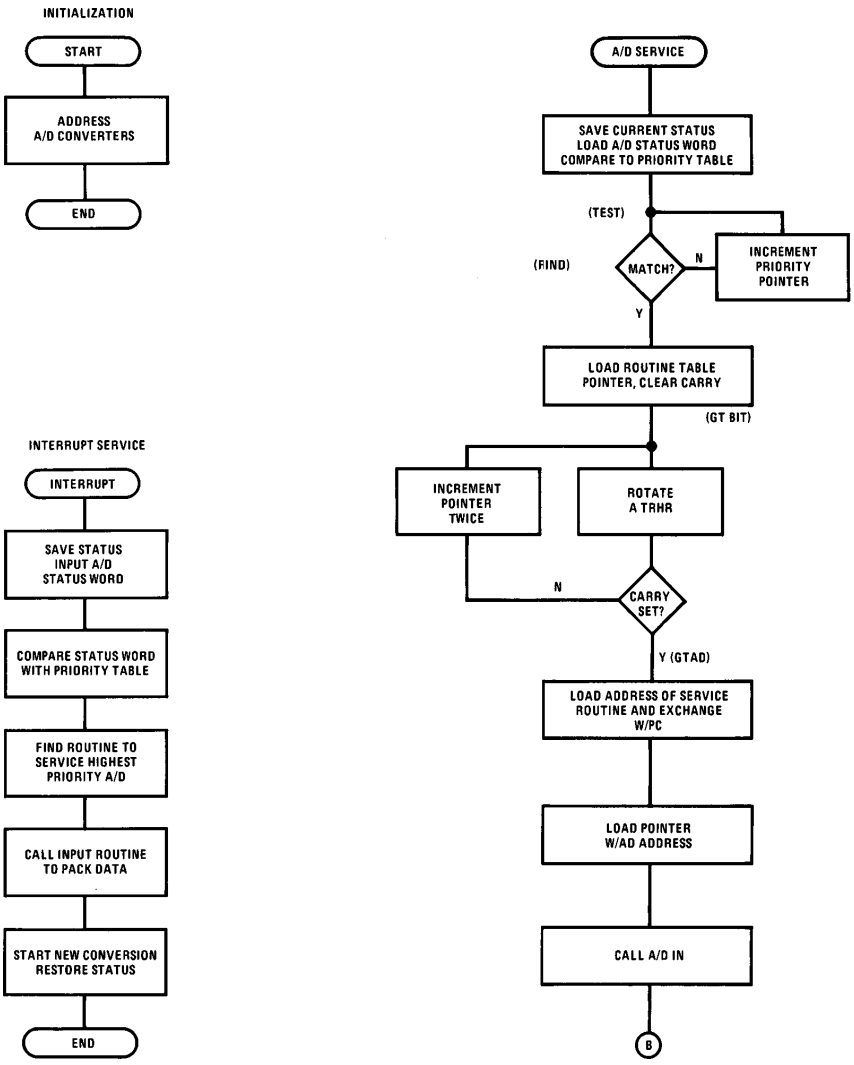

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FIGURE 8. Flow Charts of A/D Routines

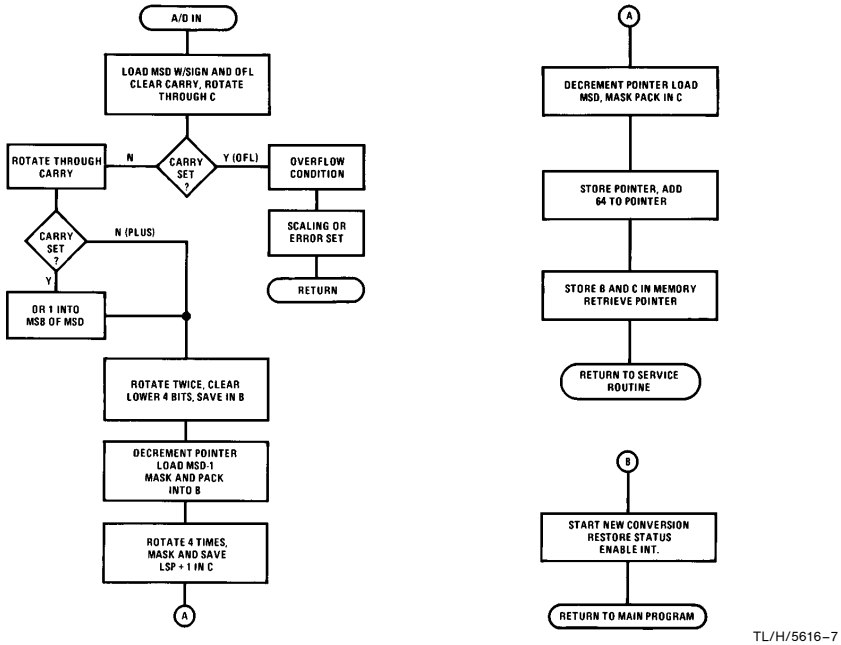

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FIGURE 8. Flow Charts of A/D Routines (Continued)

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

LABEL	OPCODE	OPERAND	COMMENT
IAD:	PUSH	PSW	; interrupt from A/D
	PUSH	H	; save H & L on stack
	PUSH	B	; save B & C on stack
	PUSH	D	; save D & E on stack
	LXI	H, ADWD	; pickup A/D status word
	MOV	6, M	; move word into B
	LXI	H, PRTBL	; pickup priority tbl pointer
TEST:	MOV	A, B	; place status word in accum.
	ANA	M	; mask with priority table
	JNZ	FIND	; match jump to Find
	INX	H	; point to lower priority
	JMP	TEST	; try again
FIND:	LXI	H, RTBL	; pickup routine tbl pointer
	ORA	A	; reset carry
GTBIT:	RAR		; rotate thru carry
	JC	GTAD	; bit was found
	INX	H	; point to
	INX	H	; next routine
	JMP	GTBIT	; try again
GTAD:	MOV	E, M	; move first byte into E
	INX	H	; point to next byte
	MOV	D, M	; move second byte into D
	XCGH		; exchange DE, HL
	PCHL		; jump to input routine
INAD1:	LXI	H, AD1	; pickup pointer to A/D 1
	CALL	ADIN	; call common input routine
	MOV	M, A	; start new conversion
	JMP	DONE	; all done
INAD2:	LXI	H, AD2	; pickup pointer to A/D 2
	CALL	ADIN	; call input routine
	MOV	M, A	; start new conversion
	JMP	DONE	; all done
	•		
	•		
	•		
DONE:	POP	D	; restore D
	POP	B	; restore B
	POP	H	; restore H
	POP	PSW	; restore PSW
	EI		; enable interrupts
	RET		; return to main program
PRTBL:	DB	04H	; 0000C100 AD3 highest priority
	DB	03H	; 0000011 AD2 & AD1 next priority

Routine 2. 8-channel Interrupt Service Routine with Software Priority (Continued)

```
LABEL  OPCODE  OPERAND   COMMENT
PRTBL:   DB      10H     ; 00010000 AD5
                           lowest priority
RTBL:    DW      1000H   ; routine for A/D 1
         DW      100CH   ; routine for A/D 2
         •
         •
         •
         DW      1060H   ; routine for A/D 8
ADIN:    MOV     A, M    ; Input MSD plus
                           OFL & SIGN
         MOV     A, M    ; delay
         ORA     A       ; reset carry
         RAL             ; rotate left thru
                           carry, OFL
         JC      OFL     ; jump to overflow
                           if set
         RAL             ; rotate left thru
                           carry, sign
         JC      PLUS    ; jump to plus if set
         OR1     20H     ; OR1 into BCD,
                           MSB for minus
PLUS:    RAL
         RAL
         ANI     FO      ; mask lower order
                           bits
         MOV     B, A    ; save in B
         DCR     H       ; point to MSD-1
         MOV     A, M    ; input MSD-1
         MOV     A, M    ; delay
         ANI     OF      ; mask higher 4 bits
         OR      B       ; pack MSD and MSD-1
         MOV     B, A    ; save in B
         DCR     H       ; point to LSD + 1
         MOV     A, M    ; input LSD + 1
         MOV     A, M    ; delay
         RAL             ; rotate
         RAL             ; into
         RAL             ; upper
         RAL             ; 4 bits
         ANI     FO      ; mask lower bits
         MOV     C, A    ; save in C
         DCR     H       ; point to LSD
         MOV     A, M    ; input LSD
         MOV     A, M    ; delay
         ANI     OF      ; mask upper bits
         OR      C       ; pack
         MOV     C, A    ; save in C
         SHLD    TEMP    ; store HL in temp
         MOV     A, L    ; move L in accum.
         ACI     64      ; generate lower
                           address
         MOV     L, A    ; above memory
                           mapped
         MOV     A, H    ; converter addresses
         ACI     O       ; include carry
         MOV     H, A    ; to upper bits
         MOV     M, C    ; store C
         INX     H       ; then
         MOV     M, B    ; store B
         LHLD    TEMP    ; retrieve HL
         RET             ; return
```

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal $_{REF}$ (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

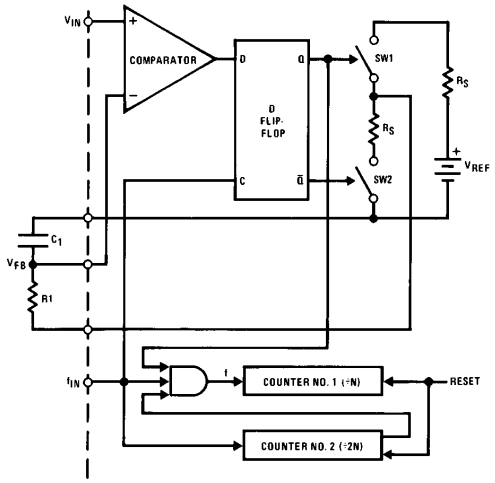
$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



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$V_{IN} = V_{FB} = V_{REF} \times$ (duty cycle)

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

Electrical Characteristics

ADC3511CC, ADC3711CC 4.75 ≤ V_{CC} ≤ 5.25V; −40°C ≤ T_A + 85°C, f = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

Parameter		Conditions	Min	Typ (Note 2)	Max	Units
	Non-Linearity	(Note 3) V_{IN} = 0 − 2V Full-Scale V_{IN} = 0 − 200 mV Full-Scale	−0.05	+0.025	0.05	% of Full-Scale
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
$V_{IN}+$, $V_{IN}-$	Analog Input Current	T_A = 25°C	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = ½ counts and 0.05% of full-scale = 1 count. For the ADC3711CCL: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

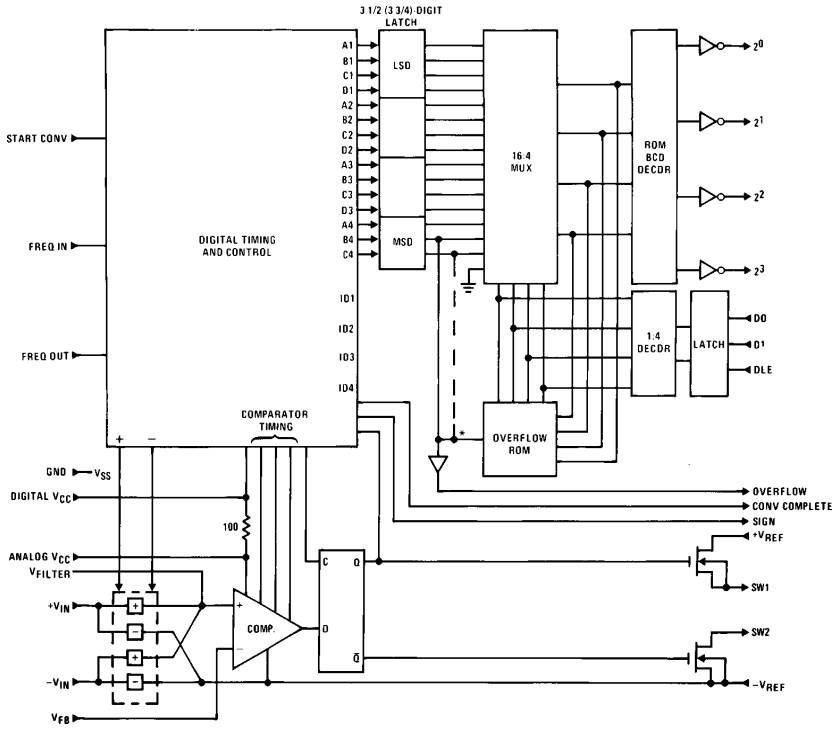

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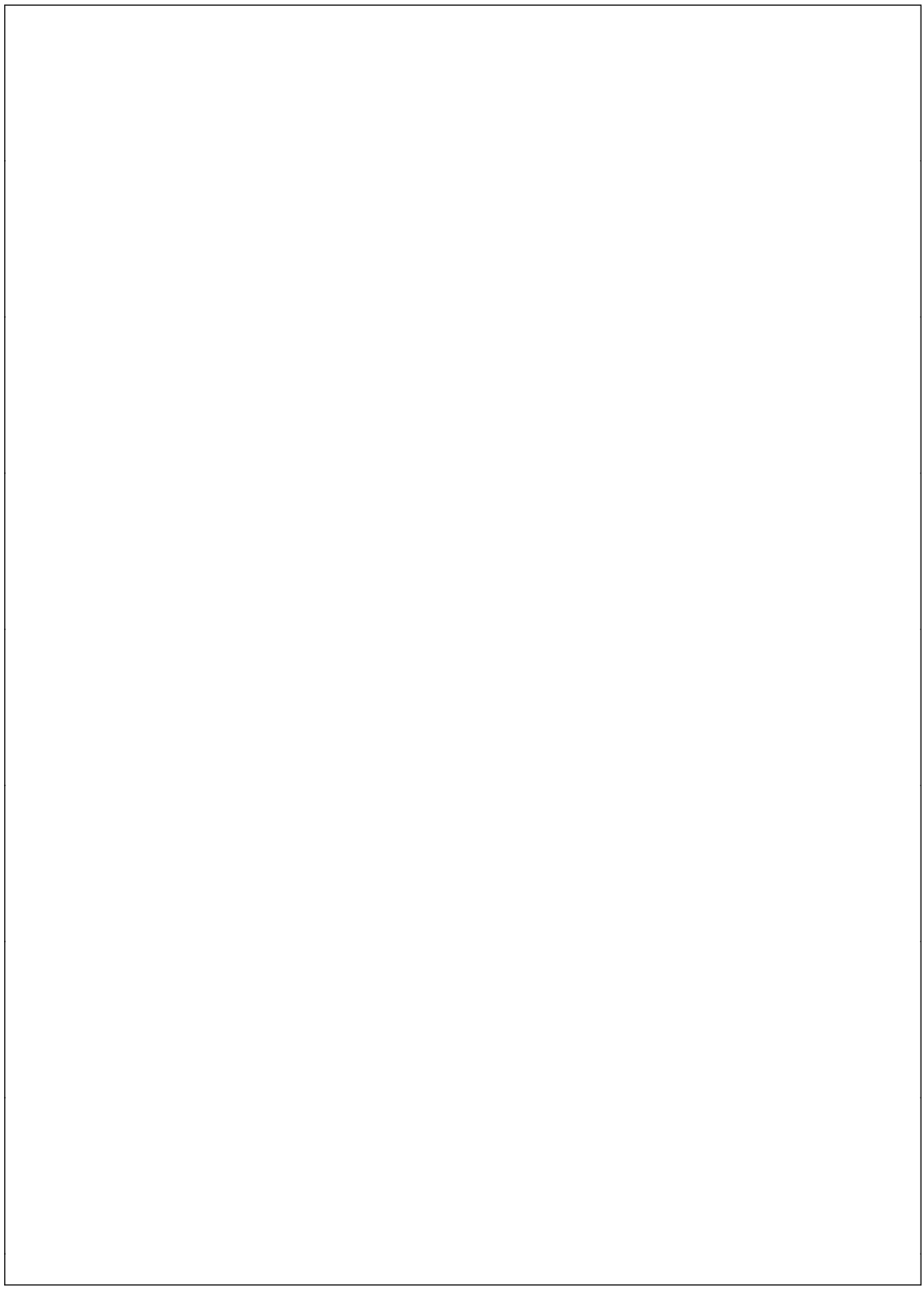
FIGURE A2. ADC3511 3½-Digit A/D (*ADC3711 3¾-Digit A/D) Block Diagram



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