MOTOROLA
Semiconductor Products Inc.

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Application Note

GUIDE TO THYRISTOR APPLICATIONS

INTRODUCTION

To successfully apply thyristors, an understanding of their characteristics, ratings, and limitations is imperative. In this note, significant thyristor characteristics, the basis of their ratings, and their relationship to circuit design are discussed.

Several different kinds of thyristors exist, as shown in Table 1. SCR's are the most widely used as power control elements; triacs are quite popular in lower current (under 40 A) ac power applications. Diacs, SUS's and SBS's are most commonly used as gate trigger devices for the power control elements.

Before considering thyristor characteristics in detail, a brief review of their operation based upon the common two-thyristor analogy of an SCR is in order.

BASIC BEHAVIOR

The bistable action of thyristors is readily explained by analysis of the structure of an SCR. This analysis is related to any operating quadrant of triac because a triac may be considered as two parallel SCR's oriented in opposite directions. Figure 1(a) shows the schematic symbol for an SCR, and Figure 1(b) shows the p-n-p-n structure the symbol represents. In the two-transistor model for the SCR shown in Figure 1(c), the interconnections of the two transistors are such that regenerative action occurs. Observe that if current is injected into any leg of the model, the gain of the transistors (if sufficiently high) causes this current to be amplified in another leg. In order for regeneration to occur, it has been shown that it is necessary for the sum of the common base current gains (α) of the two transistors to exceed unity. Therefore, because the junction leakage currents are relatively small and current gain is designed to be low at the leakage current level, the PNPN device remains off unless external current is applied. When sufficient trigger current is applied (to the gate, for example, in the case of an SCR) to raise the loop gain to unity, regeneration occurs and the on-state principal current is limited primarily by external circuit impedance. If the initiating trigger current is removed, the thyristor remains in the "on" state, providing the current level is high enough to meet the unity gain criteria. This critical current is called latching current.

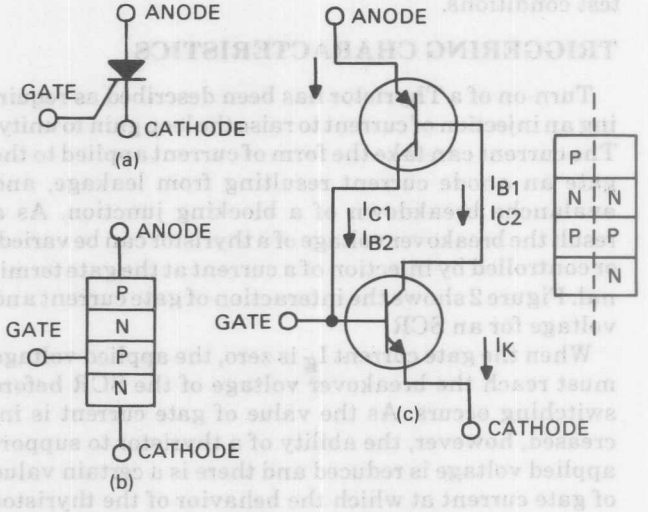


FIGURE 1 — Two-transistor analogy of an SCR: (a) schematic symbol of SCR; (b) p-n-p-n structure represented by schematic symbol; (c) two-transistor model of SCR.

In order to turn off a thyristor, some change in current must occur to reduce the loop gain below unity. From the model, it appears that shorting the gate to cathode would accomplish this, however in an actual SCR structure, the gate area is only a fraction of the cathode area and very little current is diverted by the short. In practice the principal current must be reduced below a certain level, called holding current, before gain falls below unity and turn-off may commence.

In fabricating practical SCR's and Triacs, generally a "shorted emitter" design is used in which, schematically, a resistor is added from gate to cathode or gate to MTI. Because current is diverted from the N-base through the resistor, the gate trigger current, latching current and holding current all increase. One of the principal reasons for the shunt resistance is to improve dynamic performance at elevated temperatures. Without the shunt, leakage current on most high current thyristors could initiate turn-on action at high temperatures.

Sensitive gate thyristors employ a high resistance shunt or none at all; consequently, their characteristics can be altered dramatically by use of an external resistance. An external resistance has a minor effect on most shorted emitter designs.

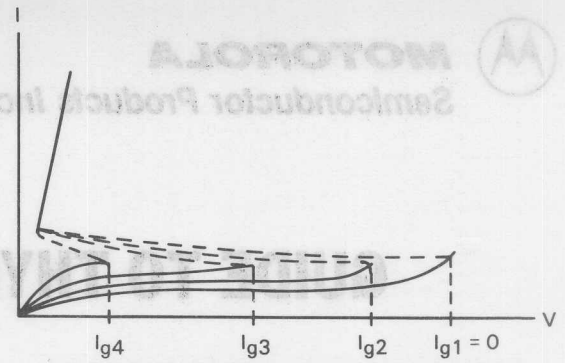
Junction temperature is the primary variable affecting thyristor characteristics. Increased temperatures change characteristics in the direction such that the thyristor is easier to turn on and keep on. Consequently, circuit conditions which determine turn-on must be designed to operate at the lowest anticipated junction temperatures, while circuit conditions which are to turn off the thyristor or prevent false triggering must be designed to operate at the maximum junction temperature.

Thyristor specifications are usually written with case temperatures specified and with electrical conditions such that the power dissipation is low so that the junction temperature essentially equals the case temperature. It is incumbent upon the user to properly account for changes in characteristics caused by the circuit operating conditions being different from the test conditions.

TRIGGERING CHARACTERISTICS

Turn-on of a Thyristor has been described as requiring an injection of current to raise the loop gain to unity. The current can take the form of current applied to the gate an anode current resulting from leakage, and avalanche breakdown of a blocking junction. As a result the breakover voltage of a thyristor can be varied, or controlled by injection of a current at the gate terminal. Figure 2 shows the interaction of gate current and voltage for an SCR.

When the gate current I_g is zero, the applied voltage must reach the breakover voltage of the SCR before switching occurs. As the value of gate current is increased, however, the ability of a thyristor to support applied voltage is reduced and there is a certain value of gate current at which the behavior of the thyristor closely resembles that of a rectifier. Because thyristor turn-on, as a result of exceeding the breakover voltage, can produce high instantaneous power dissipation non-uniformly distributed over the die area during



THYRISTOR BREAKOVER AS FUNCTION OF GATE CURRENT

FIGURE 2 — Thyristor Characteristics Illustrating Breakover as a Function of Gate Current.

the switching transition, extreme temperatures resulting in die failure may occur unless the magnitude and rate of rise of principal current (di/dt) is restricted to tolerable levels. For normal operation, therefore, SCR's and triacs are operated at applied voltages lower than the breakover voltage, and are made to switch to the ON state by gate signals of sufficient amplitude to assure complete turn-on independent of the applied voltage. On the other hand, Diacs and other thyristor trigger devices are designed to be triggered by anode breakover; nevertheless they also have di/dt and peak current limits which must be adhered to.

A triac displays the same general appearance for operation with negative current and voltage, however the situation is more complex as a triac can be switched on by either polarity of gate signal regardless of the voltage polarity across the main terminals. The various combinations of gate and main terminal polarities are described by a quadrant system as shown in Figure 3. Relative sensitivity is dependent upon the physical structure of a particular triac, but as a rule sensitivity is highest in quadrant I, and quadrant IV is generally considerably less sensitive than the others.

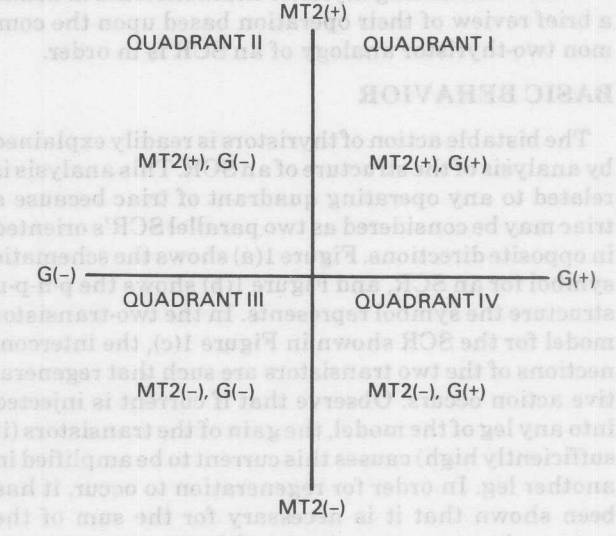


FIGURE 3 — QUADRANT DEFINITIONS FOR A TRIAC

Gate sensitivity of a triac as a function of temperature is shown in Figure 4.

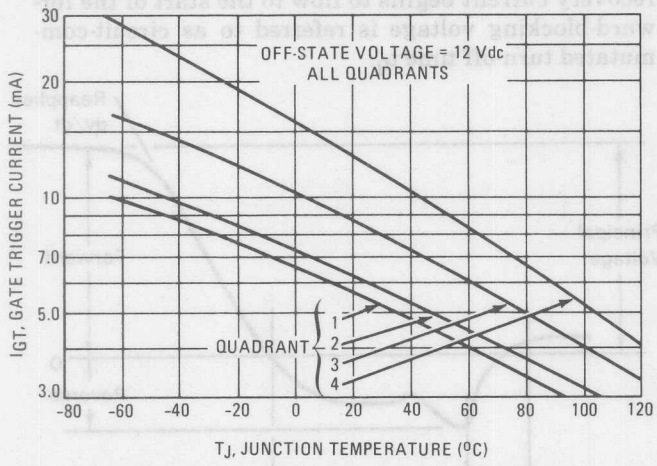


FIGURE 4 — TYPICAL TRIAC TRIGGERING SENSITIVITY IN THE FOUR TRIGGER QUADRANTS

Since both the junction leakage currents and the current gain of the "transistor" elements increases with temperature, the magnitude of the required gate trigger current decreases as temperature increases. The gate - which can be regarded as a diode - exhibits a decreasing voltage drop as temperature increases. Thus it is important that the gate trigger circuit be designed to deliver sufficient current to the gate at the lowest temperature anticipated.

It is also advisable to observe the maximum gate current, as well as peak and average power dissipation ratings. Also in the negative direction, the maximum gate ratings should be observed. Both positive and negative gate limits are often given on the data sheets and they may indicate that protective devices such as voltage clamps and current limiters may be required in some applications. It is generally inadvisable to dissipate power in the reverse direction.

Although the criteria for turn-on has been described in terms of current, it is more basic to consider the thyristor as being charge controlled (Figures 1 and 2). Accordingly, as the duration of the trigger pulse is reduced, its amplitude must be correspondingly increased. Figure 5 shows typical behavior at various pulse widths and temperatures.

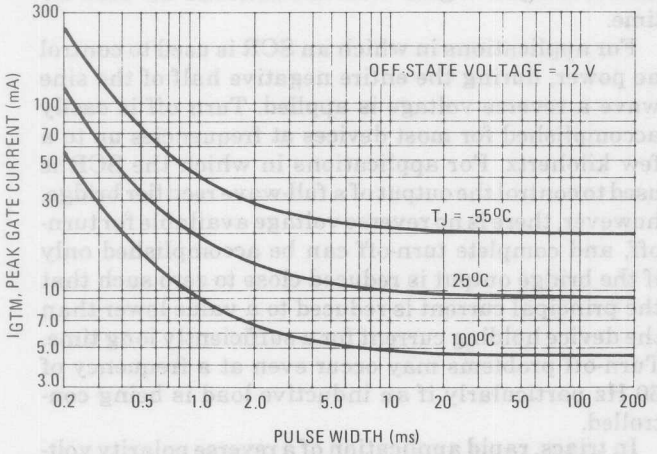


FIGURE 5 — TYPICAL BEHAVIOR OF GATE TRIGGER CURRENT AS PULSE WIDTH AND TEMPERATURE ARE VARIED

The gate pulse width required to trigger a thyristor also depends upon the time required for the anode current to reach the latching value. It may be necessary to maintain a gate signal throughout the conduction period in applications where the load is highly inductive or where the anode current may swing below the holding value within the conduction period.

When triggering an SCR with a dc current, excess leakage in the reverse direction normally occurs if the trigger signal is maintained during the reverse blocking phase of the anode voltage. This happens because the SCR operates like a remote base transistor having a gain which is generally about 0.5. When high gate drive currents are used, substantial dissipation could occur in the SCR or a significant current could flow in the load; therefore, some means usually must be provided to remove the gate signal during the reverse blocking phase.

LATCH AND HOLD CHARACTERISTICS

In the section under basic behavior, it was mentioned that it is necessary to have sufficient principal current flowing to raise the loop gain to unity in order for the thyristor to remain in the on-state when the trigger signal is removed. The principal current level required is called latching current, I_L. The latching current is primarily only affected by temperature on shorted emitter structures although triacs show some dependency upon gate current in quadrant II.

In order to allow turn-off, the principal current must be reduced to a level below that of the latching current; the current where turn-off occurs is called holding current, I_H. The holding current is likewise similarly affected by temperature and also is dependent upon gate impedance.

Reverse voltage on the gate of an SCR markedly increases the latch and hold levels while forward bias on thyristor gates may significantly lower these levels from those specified on the data sheet, which are normally given with the gate open. Sometimes, failure to account for this causes latch or hold problems when thyristors are being driven from transistors whose saturation voltages are a few tenths of a volt.

Thyristors made with a shorted emitter construction are obviously not as sensitive to the gate circuit conditions as devices which have no built in shunt.

SWITCHING CHARACTERISTICS

When triacs or SCR's are triggered by a gate signal, the turn-on time consists of two stages, a delay time, t_d, and a rise time, t_r, as shown in Figure 6. The total gate controlled turn-on time, t_{gt}, is usually defined as the time interval between the 50 percent point of the leading edge of the gate trigger voltage and 90 percent point of the principal current. The rise time t_r is the time interval required for the principal current to rise from 10 to 90 percent of its maximum value. A resistive load is usually specified.

Delay time decreases slightly as the peak off-state voltage increases. It is primarily related to the magnitude of the gate-trigger current and shows a relationship which is roughly inversely proportional.

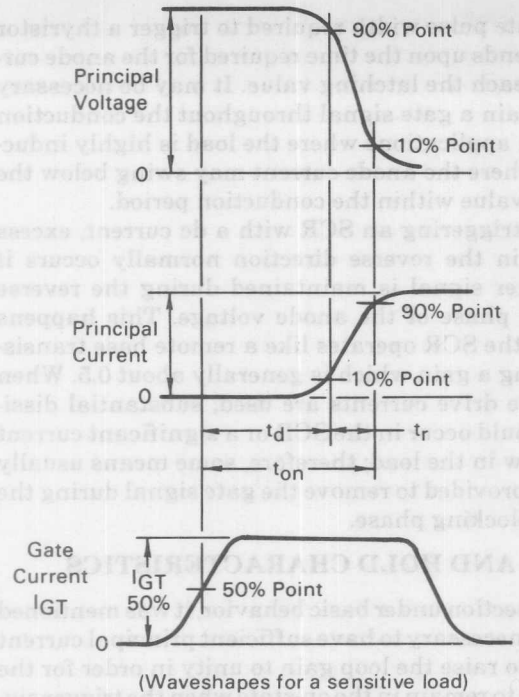


FIGURE 6 — WAVESHAPES ILLUSTRATING THYRISTOR TURN-ON TIME FOR A RESISTIVE LOAD

The rise time is influenced primarily by the off-state voltage, as high voltage causes an increase in regenerative gain. Of major importance in the rise time interval is the relationship between principal voltage and current flow through the thyristor $\frac{di}{dt}$. During this time the dynamic voltage drop is high and the current density due to the possible rapid rate of change can produce localized hot spots in the die. This may permanently degrade the blocking characteristics. Therefore, it is important that power dissipation during turn-on be restricted to safe levels.

Turn-off time is a property associated only with SCR's and other unidirectional devices. (In triacs or bidirectional devices a reverse voltage cannot be used to provide circuit-commutated turn-off voltage because a reverse voltage applied to one half of the structure would be a forward-bias voltage to the other half.) For turn-off times in SCR's, the recovery period consists of two stages, a reverse recovery time and a gate or forward blocking recovery time, as shown in Figure 7

When the forward current of an SCR is reduced to zero at the end of a conduction period, application of reverse voltage between the anode and cathode terminals causes reverse current flow in the SCR. The current persists until the time that the reverse current decreases to the leakage level. Reverse recovery time (t_{rr}) is usually measured from the point where the principal current changes polarity to a specified point on the reverse current waveform as indicated in Figure 7. During this period the anode and cathode junctions are being swept free of charge so that they may support reverse voltage. A second recovery period, called the gate recovery time, t_{gr}, must elapse for the charge stored in the forward-blocking junction to recombine so that forward-blocking voltage can be reapplied and successfully blocked by the SCR. The gate recovery time of an SCR is usually much longer than the reverse recovery time. The total time from the instant reverse recovery current begins to flow to the start of the forward-blocking voltage is referred to as circuit-commutated turn-off time t_q.

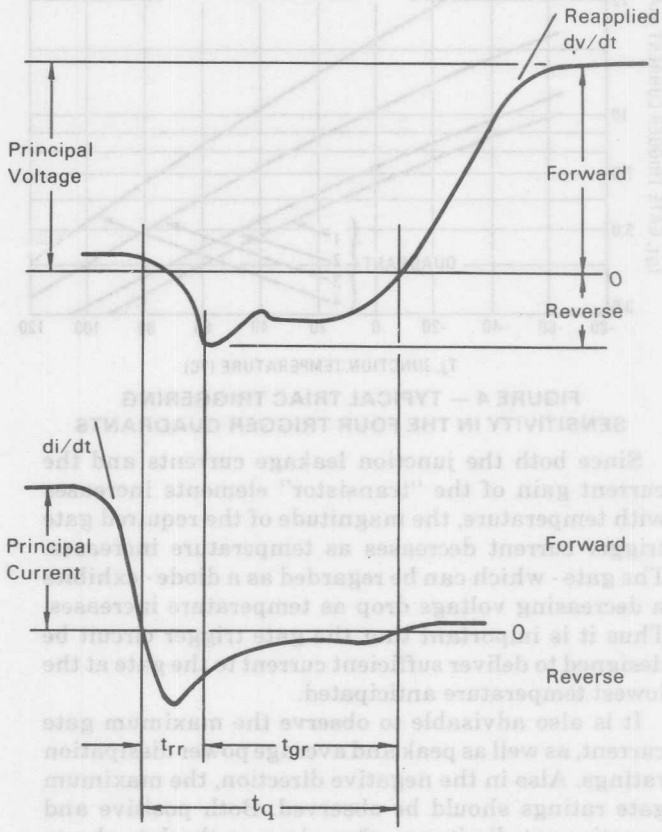


FIGURE 7 — WAVESHAPES ILLUSTRATING THYRISTOR TURN-OFF TIME

Turn-off time depends upon a number of circuit conditions including on-state current prior to turn-off, rate of change of current during the forward-to-reverse transition, reverse-blocking voltage, rate of change of reapplied forward voltage, the gate bias, and junction temperature, Increasing junction temperature and on-state current both increase turn-off time and have a more significant effect than any of the other factors. Negative gate bias will decrease the turn-off time.

For applications in which an SCR is used to control ac power, during the entire negative half of the sine wave a reverse voltage is applied. Turn off is easily accomplished for most devices at frequencies up to a few kilohertz. For applications in which the SCR is used to control the output of a full-wave rectifier bridge, however, there is no reverse voltage available for turn-off, and complete turn-off can be accomplished only if the bridge output is reduced close to zero such that the principal current is reduced to a value lower than the device holding current for a sufficiently long time. Turn-off problems may occur even at a frequency of 60 Hz particularly if an inductive load is being controlled.

In triacs, rapid application of a reverse polarity voltage does not cause turn-off because the main blocking junctions are common to both halves of the device.

When the first half of the triac structure (SCR-1) is in the conducting state, a quantity of charge accumulates in the n-type region as a result of the principal current flow. As the principal current crosses the zero reference point, a reverse current is established as a result of the charge remaining in the n-type region, which is common to both halves of the device. Consequently, the reverse recovery current becomes a forward current to the second half of the triac. The current resulting from stored charge causes the second half of the triac to go into the conducting state in the absence of a gate signal. Once current conduction has been established by application of a gate signal, therefore, complete loss in power control can occur as a result of interaction within the n-type base region of the triac unless sufficient time elapses or the rate of application of the reverse polarity voltage is slow enough to allow nearly all the charge to recombine in the common n-type region. Therefore, triacs are generally limited to low-frequency -60 Hz applications. Turn off or commutation of triacs is more severe with inductive loads than with resistive loads because of the phase lag between voltage and current associated with inductive loads. Figure 8 shows the waveforms for an inductive load with lagging current power factor. At the time the current reaches zero crossover (Point A), the half of the triac in conduction begins to commutate when the principal current falls below the holding current. At the instant the conducting half of the triac turns off, an applied voltage opposite the current polarity is applied across the triac terminals (Point B). Because this voltage is a forward bias to the second half of the triac, the suddenly reapplied voltage in conjunction with the remaining stored charge in the high-voltage junction reduces the over-all device capability to support voltage. The result is a loss of power control to the load, and the device remains in the conducting state in absence of a gate signal. The measure of triac turn-off ability is the rate of rise of the opposite polarity voltage it can handle without remaining on. It is called commutating dv/dt (dv/dt [c]). Circuit conditions and temperature affect dv/dt (c) in a manner similar to the way t_q is affected in an SCR.

It is imperative that some means be provided to restrict the rate of rise of reapplied voltage to a value which will permit triac turn-off under the conditions of inductive load. A commonly accepted method for keeping the commutating dv/dt within tolerable levels is to use an RC snubber network in parallel with the main terminals of the triac. Because the rate of rise of applied voltage at the triac terminal is a function of the load impedance and the RC snubber network, the circuit can be evaluated under worst-case conditions of operating case temperature and maximum principal current. The values of resistance and capacitance in the snubber are then adjusted so that the rate of rise of commutating dv/dt stress is within the specified minimum limit under any of the conditions mentioned above. The value of snubber resistance should be high enough to limit the snubber capacitance discharge currents during turn-on and dampen the LC oscillation during commutation. The combination of snubber values having highest resistance and lowest capacitance that provides satisfactory operation is generally preferred.

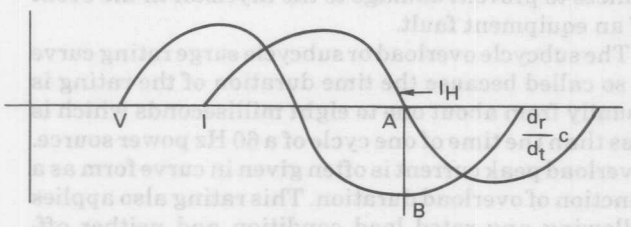


FIGURE 8 — Inductive Load Waveforms

FALSE TRIGGERING

Circuit conditions can cause thyristors to turn on in the absence of the trigger signal. False triggering may result from:

1) A high rate of rise of anode voltage, (the dv/dt effect).
2) Transient voltages causing anode breakover.
3) Spurious gate signals.

Static dv/dt effect: When a source voltage is suddenly applied to a thyristor which is in the OFF state, it may switch from the OFF state to the conducting state. If the thyristor is controlling alternating voltage, "false" turn-on resulting from a transient imposed voltage is limited to no more than one-half cycle of the applied voltage because turn-off occurs during the zero current crossing. However, if the principal voltage is dc voltage, the transient may cause switching to the ON state and turn-off could then be achieved only by a circuit interruption.

The switching from the OFF state caused by a rapid rate of rise of anode voltage is the result of the internal capacitance of the thyristor. A voltage wavefront impressed across the terminals of a thyristor causes a capacitance-charging current to flow through the device which is a function of the rate of rise of applied off-state voltage (i = C dv/dt). If the rate of rise of voltage exceeds a critical value, the capacitance charging current exceeds the gate triggering current and causes device turn-on. Operation at elevated junction temperatures reduces the thyristor ability to support a steep rising voltage dv/dt because of increased sensitivity.

dv/dt ability can be improved quite markedly in sensitive gate devices and to some extent in shorted emitter designs by a resistance from gate to cathode (or MT1) however reverse bias voltage is even more effective in an SCR. More commonly, a snubber network is used to keep the dv/dt within the limits of the thyristor when the gate is open.

TRANSIENT VOLTAGES: — Voltage transients which occur in electrical systems as a result of disturbance on the ac line caused by various sources such as energizing transformers, load switching, solenoid closure, contractors and the like may generate voltages which are above the ratings of thyristors. Thyristors, in general, switch from the OFF state to the ON state whenever the breakover voltage of the device is

exceeded, and energy is then transferred to the load. However, unless a thyristor is specified for use in a breakover mode, care should be exercised to ensure that breakover does not occur, as some devices may incur surface damage with a resultant degradation of blocking characteristics. It is good proctice when thyristors are exposed to a heavy transient environment to provide some form of transient suppression.

For applications in which low-energy, long-duration transients may be encountered, it is advisable to use thyristors that have voltage ratings greater than the highest voltage transient expected in the system. The use of voltage clipping cells (MOV or Zener) is also an effective method to hold transient below thyristor ratings. The use of an RC snubber is effective in reducing the effects of the high-energy short-duration transients more frequently encountered. The snubber is commonly required to prevent the static dv/dt limits from being exceeded, and often may be satisfactory in limiting the amplitude of the voltage transients as well.

For all applications, the dv/dt limits may not be exceeded. This is the minimum value of the rate of rise off-state voltage applied immediately to the MT1-MT2 terminals after the principle current of the opposing polarity has decreased to zero.

SPURIOUS GATE SIGNALS: In noisy electrical environments, it is possible for enough energy to cause gate triggering to be coupled into the gate wiring by stray capacitance or electromagnetic induction. It is therefore, adviseable to keep the gate lead short and have the common return directly to the cathode or MT1. In extreme cases, shielded wire may be required. Another aid commonly used is to connect a capacitance on the order of 0.01 to 0.1 μF across the gate and cathode terminals. This has the added advantage of increasing the thyristor dv/dt capability, since it forms a capacitive divider with the anode to gate capacitance. The gate capacitor also reduces the rate of application of gate trigger current which may cause di/dt failures if a high inrush load is present.

THYRISTOR RATINGS

To insure long life and proper operation, it is important that operating conditions be restrained from exceeding thyristor ratings. The most important and fundamental ratings are temperature and voltage which are interrelated to some extent. The voltage ratings are applicable only up to the maximum temperature ratings of a particular part number. The temperature rating may be chosen by the manufacturer to insure satisfactory voltage ratings, switching speeds, or dv/dt ability.

OPERATING CURRENT RATINGS

Current ratings are not independently established as a rule. The values are chosen such that at a practical case temperature the power dissipation will not cause the junction temperature rating to be exceeded.

Various manufacturers may choose different criteria to establish ratings. At Motorola, use is made of the thermal response of the semiconductor and worst case values of on-state voltage and thermal resistance, to guarantee the junction temperature is at or below its rated value. Values shown on data sheets consequently differ somewhat from those computed from the standard formula:

$$T_C\,(max) = T\,(rated) - R_{\theta JC} \times P_D\,(AV)$$

where

T_C (max) = Maximum allowable case temperature

T (rated) = Rated junction temperature or maximum rated case temperature with zero principal current and rated ac blocking voltage applied.

$R_{\theta JC}$ = Junction to case thermal resistance

P_D (AV) = Average power dissipation

The above formula is generally suitable for estimating case temperature in situations not covered by data sheet information. Worst case values should be used for thermal resistance and power dissipation.

OVERLOAD CURRENT RATINGS

Overload current ratings may be divided into two types: non-repetitive and repetitive.

Non-repetitive overloads are those which occur rarely and are not a part of the normal application of the device. Examples of such overloads are faults in the equipment in which the devices are used and accidental shorting of the load. Non-repetitive overload ratings permit the device to exceed its maximum operating junction temperature for short periods of time because this overload rating applies following any rated load condition. In the case of a reverse blocking thyristor or SCR, the device must block rated voltage in the reverse direction during the current overload. However, no type of thyristor is required to block off-stage voltage at any time during or immediately following the overload. Thus, in the case of a triac, the device need not block in either direction during or immediately following the overload. Usually only approximately one hundred such current overloads are permitted over the life of the device. These non-repetitive overload ratings just described may be divided into two types: multicycle (which include single cycle) and subcycle. For an SCR, the multicycle overload current rating, or surge current ratings as it is commonly called, is generally presented as a curve giving the maximum peak values of half sine wave on-state current as a function of overload duration measured in number of cycles for a 60 Hz frequency.

For a triac, the current waveform used in the rating is a full sine wave. Multicycle surge curves are used to select proper circuit breakers and series line impedances to prevent damage to the thyristor in the event of an equipment fault.

The subcycle overload or subcycle surge rating curve is so called because the time duration of the rating is usually from about one to eight milliseconds which is less than the time of one cycle of a 60 Hz power source. Overload peak current is often given in curve form as a function of overload duration. This rating also applies following any rated load condition and neither off-state nor reverse blocking capability is required on the part of the thyristor immediately following the overload current. The subcycle surge current rating

may be used to select the proper current-limiting fuse for protection of the thyristor in the event of an equipment fault. Since this use of the rating is so common, manufacturers simply publish the i^1t rating in place of the subcycle current overload curve because fuses are commonly rated in terms of i^2t. The i^2t rating can be approximated from the single cycle surve rating (I_{TSM}) by using:

$$i^2t = I^2_{TSM} \times t/2$$

where the time t is the time base of the overload, i.e., 8.33 mSec for a 60 Hz frequency.

Repetitive overloads are those which are an intended part of the application such as a motor drive application. Since this type of overload may occur a large number of times during the life of the thyristor, its rated maximum operating junction temperature must not be exceeded during the overload if long thyristor life is required. Since this type of overload may have a complex current waveform and duty-cycle, a current rating analysis involving the use of the transient thermal impedance characteristics is often the only practical approach. In this type of analysis, the thyristor junction-to-case transient thermal impedance characteristic is added to the user's heat dissipator transient thermal impedance characteristic. Then by the superposition of power waveforms in conjunction with the composite thermal impedance curve, the overload current rating can be obtained. The exact calculation procedure is found in the power semiconductor literature.[2,3,4]

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