MITSUBISHI SEMICONDUCTORS 1985

HIGH SPEED CMOS LOGIC

QCI QUANTUM COEFFICIENT INCORPORATED
2680 No. First St., Suite 204
San Jose, CA 95134
Phone (408) 942-1070

DATA BOOK

MITSUBISHI ELECTRIC

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PREFACE

Thank you for your continued patronage of Mitsubishi Electric and our semiconductor products.

Semiconductor devices are a mainstay of the burgeoning electronics industry, where they are finding more and more applications, and are meeting demands for increased sophistication and diversification of performance and function.

The new high-speed CMOS logic M74HC00P series is now being mass-produced and marketed by Mitsubishi Electric Corporation in it's special efforts to broaden its product line of semiconductors and to produce a broad range of new high-performance, high-reliability semiconductor products.

This data book includes the data required for each of the 23 Mitsubishi products now being marketed for the first time.

For information concerning other Mitsubishi Electric semiconductors, please refer to our various data books.

February 1985

Mitsubishi Electric Corporation
Managing Director
Semiconductor Division
Junsuke Amano

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● **M74HC32P** Quadruple 2-Input Positive OR Gate ..... 2 —21
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＊ **M74HC125P** Quadruple 3-State Noninverting Buffer ..... ——
＊ **M74HC126P** Quadruple 3-State Noninverting Buffer ..... ——
＊ **M74HC132P** Quadruple 2-Input Schmitt-Trigger Positive NAND Gate ..... ——
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＊M74HC253P	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	—
＊M74HC257P	Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	—
＊M74HC259P	8-Bit Addressable Latch/1-of-8 Decoder	—
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＊M74HC283P	4-Bit Binary Full Adder with Fast Carry	—
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＊M74HC299P	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	—
＊M74HC365P	Hex 3-State Noninverting Buffer with Common Enables	—
＊M74HC366P	Hex 3-State Inverting Buffer with Common Enables	—
＊M74HC367P	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections	—
＊M74HC368P	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections	—
＊M74HC373P	Octal 3-State Noninverting D-Type Transparent Latch	—
＊M74HCT373P	Octal 3-State Noninverting D-Type Transparent Latch with LSTTL-Compatible Inputs	—
＊M74HC374P	Octal 3-State Noninverting D-Type Flip-Flop	—
＊M74HCT374P	Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	—
＊M74HC375P	Dual 2-Bit Transparent Latch	—
＊M74HC390P	Dual 4-Stage Binary Ripple Counter with ÷2 and ÷5 Sections	—
＊M74HC393P	Dual 4-Stage Binary Ripple Counter	—
＊M74HC533P	Octal 3-State Inverting D-Type Transparent Latch	—
＊M74HC534P	Octal 3-State Inverting D-Type Flip-Flop	—

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＊M74HC540P	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	——
＊M74HC541P	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	——
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＊M74HC564P	Octal 3-State Inverting D-Type Flip-Flop	——
＊M74HC595P	8-Bit Serial-Input/Serial-or Parallel-Output Shift Register with Latched 3-State Outputs	——
＊M74HC640P	Octal 3-State Inverting Bus Transceiver	——
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＊M74HC646P	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	——
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＊M74HC4020P	14-Stage Binary Ripple Counter	——
＊M74HC4022P	Octal Counter/Divider	——
＊M74HC4024P	7-Stage Binary Ripple Counter	——
＊M74HC4040P	12-Stage Binary Ripple Counter	——
＊M74HC4049P	Hex Inverting Buffer/Logic-Level Down Converter	——
＊M74HC4050P	Hex Noninverting Buffer/Logic-Level Down Converter	——
＊M74HC4051P	8-Channel Analog Multiplexer/Demultiplexer	——
＊M74HC4052P	Dual 4-Channel Analog Multiplexer/Demultiplexer	——
＊M74HC4053P	Triple 2-Channel Analog Multiplexer/Demultiplexer	——
＊M74HC4066P	Quadruple Analog Switch/Multiplexer/Demultiplexer with Enhanced ON-Resistance Linearity	——
＊M74HC4078P	8-Input Positive NOR/OR Gate	——
＊M74HC4511P	BCD-to-Seven-Segment Latch/Decoder/Display Driver	——
＊M74HC4514P	1-of-16 Decoder/Demultiplexer with Address Latch	——
＊M74HC4518P	Dual BCD Counter	——
＊M74HC4520P	Dual 4-Bit Binary Counter	——
＊M74HC4538P	Dual Precision Monostable Multivibrator(Retriggerable, Resettable)	——
＊M74HC4543P	BCD-to Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	——

GUIDANCE 1

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Conditions (V_{CC}=4.5V, T_a=−40∼+85℃, switching characteristics are at C_L=50pF)

INVERTERS

Circuit function	Type	Electrical characteristics				Package outlines	Page
		High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
Hex Unbuffered Inverter	**M74HCU04P**	−4	4	21	21	14P4	2 — 7
Hex Inverter	**M74HC04P**	—	—	—	—	14P4	—
Hex Inverter with LSTTL-Compatible Inputs	**M74HCT04P**	—	—	—	—	14P4	—
Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs	**M74HCT05P**	—	—	—	—	14P4	—
Hex Inverting Buffer/Logic-Level Down Converter	**M74HC4049P**	—	—	—	—	16P4	—

NAND GATES

Quadruple 2-Input Positive NAND Gate	**M74HC00P**	−4	4	23	23	14P4	2 — 1
Quadruple 2-Input Positive NAND Gate with LSTTL-Compatible Inputs	**M74HCT00P**	—	—	—	—	14P4	—
Quadruple 2-Input Positive NAND Gate with Open-Drain Outputs	**M74HC03P**	—	—	—	—	14P4	—
Triple 3-Input Positive NAND Gate	**M74HC10P**	−4	4	24	24	14P4	2 —13
Dual 4-Input Positive NAND Gate	**M74HC20P**	—	—	—	—	14P4	—
8-Input Positive NAND Gate	**M74HC30P**	—	—	—	—	14P4	—
13-Input Positive NAND Gate	**M74HC133P**	—	—	—	—	16P4	—

AND GATES

Quadruple 2-Input Positive AND Gate	**M74HC08P**	−4	4	30	30	14P4	2 —10
Triple 3-Input Positive AND Gate	**M74HC11P**	—	—	—	—	14P4	—

NOR GATES

Quadruple 2-Input Positive NOR Gate	**M74HC02P**	−4	4	23	23	14P4	2 — 4
Triple 3-Input Positive NOR Gate	**M74HC27P**	−4	4	23	23	14P4	2 —16
Dual 4-Input Positive NOR Gate	**M74HC4002P**	−4	4	30	30	14P4	2 —86
8-Input Positive NOR/OR Gate	**M74HC4078P**	—	—	—	—	14P4	—

OR GATES

Quadruple 2-Input Positive OR Gate	**M74HC32P**	−4	4	25	25	14P4	2 —19
8-Input Positive NOR/OR Gate	**M74HC4078P**	—	—	—	—	14P4	—

EXCLUSIVE OR GATE

Quadruple 2-Input Exclusive OR Gate	**M74HC86P**	−4	4	30	30	14P4	2 —41

EXCLUSIVE NOR GATE

Quadruple 2-Input Exclusive NOR Gate	**M74HC266P**	−4	4	30	30	14P4	2 —79

AND-OR-INVERTER GATE

2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	**M74HC51P**	—	—	—	—	14P4	—

INDEX BY FUNCTION

BUFFERS/LINE DRIVERS

Circuit function	Output		Type	Electrical characteristics				Package outlines	Page
	2 state	3 state		High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
Quadruple 3-State Noninverting Buffer		NI	**M74HC125P**	—	—	—	—	14P4	—
Quadruple 3-State Noninverting Buffer		NI	**M74HC126P**	—	—	—	—	14P4	—
Hex 3-State Noninverting Buffer with Common Enables		NI	**M74HC365P**	—	—	—	—	16P4	—
Hex 3-State Inverter Buffer with Common Enables		I	**M74HC366P**	—	—	—	—	16P4	—
Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections		NI	**M74HC367P**	—	—	—	—	16P4	—
Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections		N	**M74HC368P**	—	—	—	—	16P4	—
Hex Inverting Buffer/Logic-Level Down Converter	I		**M74HC4049P**	—	—	—	—	16P4	—
Hex Noninverting Buffer/Logic-Level Down Converter	NI		**M74HC4050P**	—	—	—	—	16P4	—
Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	**M74HC240P**	−6	6	25	25	20P4	2−66
Octal 3-State Inverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		I	**M74HCT240P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	**M74HC241P**	−6	6	29	29	20P4	2−70
Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	**M74HCT241P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	**M74HC244P**	−6	6	29	29	20P4	2−75
Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	**M74HCT244P**	—	—	—	—	20P4	—
Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	**M74HC540P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	**M74HC541P**	—	—	—	—	20P4	—

I : Invert output NI : Non-invert output

BUS TRANSCEIVERS

Quadruple 3-State Inverting Bus Transceiver		I	**M74HC242P**	—	—	—	—	20P4	—
Quadruple 3-State Noninverting Bus Transceiver		NI	**M74HC243P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Bus Transceiver		NI	**M74HC245P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs		NI	**M74HCT245P**	—	—	—	—	20P4	—
Octal 3-State Inverting Bus Transceiver		I	**M74HC640P**	—	—	—	—	20P4	—
Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs		I	**M74HCT640P**	—	—	—	—	20P4	—
Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop		NI	**M74HC646P**	—	—	—	—	24P4D	—
Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop		I	**M74HC648P**	—	—	—	—	24P4D	—

I : Invert output NI : Non-invert output

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SCHMITT TRIGGERS

Circuit function	Type	Electrical characteristics				Package outlines	Page
		Positive-going threshold voltage (V)	Negative-going threshold voltage (V)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
Hex Schmitt-Trigger Inverter	**M74HC14P**	—	—	—	—	14P4	—
Quadruple 2-Input Schmitt-Trigger Positive NAND Gate	**M74HC132P**	—	—	—	—	14P4	—

J-K FLIP FLOPS

Circuit function	Type	Electrical characteristics			Trigger	Preset	Clear	Package outlines	Page
		Operation frequency (MHz)	Setup time (ns)	Hold time (ns)					
Dual J-K Flip-Flop with Reset	**M74HC73P**	21	25	0	↓	—	⎍	14P4	2—26
Dual J-K Flip-Flop with Reset	**M74HC107P**	21	25	0	↓	—	⎍	14P4	2—44
Dual J-K Flip-Flop with Set and Reset	**M74HC76P**	21	25	0	↓	⎍	⎍	16P4	2—36
Dual J-K Flip-Flop with Set and Reset	**M74HC112P**	—	—	—	↓	⎍	⎍	16P4	—
Dual J-$\overline{K}$ Flip-Flop with Set and Reset	**M74HC109P**	—	—	—	↑	⎍	⎍	16P4	—

↑ : Positive-going edge ↓ : Negative-going edge ⎍ : Active low-level

D-TYPE FLIP FLOPS

Dual D-Type Flip-Flop with Set and Reset	**M74HC74P**	21	25	5	↑	⎍	⎍	14P4	2—31
Quadruple D-Type Flip-Flop with Common Clock and Reset	**M74HC175P**	—	—	—	↑	—	⎍	16P4	—
Quadruple 3-State D-Type Flip-Flop with Common Clock and Reset	**M74HC173P**	—	—	—	↑	—	—	16P4	—
Hex D-Type Flip-Flop with Common Clock and Reset	**M74HC174P**	21	25	5	↑	—	⎍	16P4	2—62
Octal D-Type Flip-Flop with Common Clock and Reset	**M74HC273P**	21	25	0	↑	—	⎍	20P4	2—82
Octal 3-State Noninverting D-Type Flip-Flop	**M74HC374P**	—	—	—	↑	—	—	20P4	—
Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	**M74HCT374P**	—	—	—	↑	—	—	20P4	—
Octal 3-State Inverting D-Type Flip-Flop	**M74HC534P**	—	—	—	↑	—	—	20P4	—
Octal 3-State Inverting D-Type Flip-Flop	**M74HC564P**	—	—	—	↑	—	—	20P4	—
Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	**M74HC646P**	—	—	—	↑	—	—	24P4D	—
Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop	**M74HC648P**	—	—	—	↑	—	—	24P4D	—

↑ : Positive-going edge ⎍ : Active low-level

SYNCHRONOUS BINARY COUNTERS

Circuit function	Type	Electrical characteristics: Count frequency (MHz)	Trigger	Preset	Clear	Package outlines	Page
Presettable 4-Bit Binary Counter with Asynchronous Reset	**M74HC161P**	—	↑	Ⓢ	⊔Ⓐ	16P4	—
Presettable 4-Bit Binary Counter with Synchronous Reset	**M74HC163P**	—	↑	Ⓢ	⊔Ⓢ	16P4	—
Presettable 4-Bit Binary Up/Down Counter with Reset	**M74HC193P**	—	↑	Ⓐ	⊓Ⓐ	16P4	—
Dual 4-Bit Binary Counter	**M74HC4520P**	—	↑	—	⊓Ⓐ	16P4	—

↑ : Positive-going edge ⊓: Active high-level ⊔: Active low-level Ⓐ : Asynchronous Ⓢ : Synchronous

SYNCHRONOUS DECADE COUNTERS

Presettable BCD Counter with Asynchronous Reset	**M74HC160P**	—	↑	Ⓢ	⊔Ⓐ	16P4	—
Presettable BCD Counter with Synchronous Reset	**M74HC162P**	—	↑	Ⓢ	⊔Ⓢ	16P4	—
Presettable BCD Up/Down Counter with Reset	**M74HC192P**	—	↑	Ⓐ	⊓Ⓐ	16P4	—
Decade Counter/Divider	**M74HC4017P**	—	↑	—	⊓Ⓐ	16P4	—
Dual BCD Counter	**M74HC4518P**	—	↑	—	⊓Ⓐ	16P4	—

↑ : Positive-going edge ⊓: Active high-level ⊔: Active low-level Ⓐ : Asynchronous Ⓢ : Synchronous

OCTAL COUNTER/DIVIDER

Octal Counter/Divider	**M74HC4022P**	—	Note	—	⊓	16P4	—

⊓: Active high-level

Note : Positive-going edge, ↑ ($\overline{CE}$ is low-state), when the CLOCK pin is used. Negative-going edge, ↓ (CP is high-state), when the $\overline{CLOCK\ ENABLE}$ pin is used.

MONOSTABLE MULTIVIBRATORS

Circuit function	Type	Electrical characteristics: External timing resistor/capacitor for setting output pulse width	Retrigger	Clear	Package outlines	Page
Dual Retriggerable Monostable Multivibrator	**M74HC123P**	1~1MΩ/no restriction	○	○	16P4	—
Dual Monostable Multivibrator	**M74HC221P**	1~1MΩ/no restriction	○	○	16P4	—
Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	**M74HC4538P**	1~1MΩ/no restriction	○	○	16P4	—

LATCHES

Circuit function	Type	Electrical characteristics: Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)	Setup time (ns)	Hold time (ns)	Enable	Clear	Package outlines	Page
Dual 2-Bit Transparent Latch	**M74HC75P**	—	—	—	—	⊔	—	16P4	—
Dual 2-Bit Transparent Latch	**M74HC375P**	—	—	—	—	⊔	—	16P4	—
8-Bit Addressable Latch/1-of-8 Decoder	**M74HC259P**	—	—	—	—	⊔	⊔	16P4	—
Octal 3-State Noninverting D-Type Transparent Latch	**M74HC373P**	—	—	—	—	⊔	⊔	20P4	—
Octal 3-State Noninverting D-Type Transparent Latch with LSTTL-Compatible Inputs	**M74HCT373P**	—	—	—	—	⊔	⊔	20P4	—
Octal 3-State Inverting D-Type Transparent Latch	**M74HC533P**	—	—	—	—	⊔	⊔	20P4	—
Octal 3-State Inverting D-Type Transparent Latch	**M74HC563P**	—	—	—	—	⊔	⊔	20P4	—

⊓: Active high-level ⊔: Active low-level

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SHIFT REGISTERS

Circuit function	Type	Electrical characteristics: Shift frequency (MHz)	Trigger	Operating modes: Right shift	Operating modes: Left shift	Operating modes: Parallel load	Clear	Package outlines	Page
4-Bit Bidirectional Universal Shift Register	**M74HC194P**	—	↑	○	○	○	⊔	16P4	—
4-Bit Universal Shift Register	**M74HC195P**	—	↑	○	—	○	⊔	16P4	—
8-Bit Serial-Input/Parallel-Output Shift Register	**M74HC164P**	—	↑	○	—	—	⊔	14P4	—
8-Bit Serial-or Parallel-Input/Serial-Output Shift Register	**M74HC165P**	—	↑	○	—	○	—	16P4	—
8-Bit Serial-or Parallel-Input/Serial-Output Shift Register with Reset	**M74HC166P**	—	↑	○	—	○	⊔	16P4	—
8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	**M74HC299P**	—	↑	○	○	○	⊔	20P4	—
8-Bit Serial-Input/Serial-or Parallel-Output Shift Register with Latched 3-State Outputs	**M74HC595P**	—	↑	○	—	—	⊔	16P4	—

↑ : Positive-going edge ⊔: Active low-level

BINARY RIPPLE COUNTERS

Circuit function	Type	Electrical characteristics: Count frequency (MHz)	Trigger	Clear	Package outlines	Page
Dual 4-Stage Binary Ripple Counter	**M74HC393P**	—	↓	⊓	14P4	—
7-Stage Binary Ripple Counter	**M74HC4024P**	—	↓	⊓	14P4	—
12-Stage Binary Ripple Counter	**M74HC4040P**	—	↓	⊓	16P4	—
14-Stage Binary Ripple Counter	**M74HC4020P**	—	↓	⊓	16P4	—

↓ : Negative-going edge ⊓: Active high-level

ASYNCHRONOUS DECADE COUNTER

Dual 4-Stage Binary Ripple Counter with ÷2 and ÷5 Sections	**M74HC390P**	—	↓	⊓	16P4	—

↓ : Negative-going edge ⊓: Active high-level

ANALOG SWITCHES/MULTIPLEXERS

Circuit function	Type	Electrical characteristics: ON resistance V_I=2.5V (Ω)	Electrical characteristics: Propagation time(ns): Data input to output	Electrical characteristics: Propagation time(ns): Control (inhibit) input to output	Package outlines	Page
Quad Analog Switch/Multiplexer/Demultiplexer with Enhanced ON-Resistance Linearity	**M74HC4066P**	—	—	—	14P4	—
8-Channel Analog Multiplexer/Demultiplexer	**M74HC4051P**	—	—	—	16P4	—
Dual 4-Channel Analog Multiplexer/Demultiplexer	**M74HC4052P**	—	—	—	16P4	—
Triple 2-Channel Analog Multiplexer/Demultiplexer	**M74HC4053P**	—	—	—	16P4	—

DATA SELECTORS/DIGITAL MULTIPLEXERS

Circuit function	Output	Type	Electrical characteristics: Propagation time(ns) Strobe (inhibit) to output	Select input to output	Data input to output	Package outlines	Page
Quadruple 2-Input Noninverting Data Selector/Multiplexer	NI	**M74HC157P**	29	32	32	16P4	2—54
Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	**M74HC257P**	—	—	—	16P4	—
Quadruple 2-Input Inverting Data Selector/Multiplexer	I	**M74HC158P**	29	32	32	16P4	2—58
Dual 4-Input Data Selector/Multiplexer	NI	**M74HC153P**	—	—	—	16P4	—
Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	**M74HC253P**	—	—	—	16P4	—
8-Input Data Selector/Multiplexer	NI, I	**M74HC151P**	—	—	—	16P4	—
8-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI, I	**M74HC251P**	—	—	—	16P4	—
Quadruple 2-Input Data Selector/Multiplexer with Output Latch	NI	**M74HC298P**	—	—	—	16P4	—

I : Invert output NI : Non invert output 3S : Three state

DECODERS

Circuit function	Type	Electrical characteristics: Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)	Package outlines	Page
1-of-8 Decoder/Demultiplexer	**M74HC138P**	38	50	16P4	2—49
1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	**M74HCT138P**	—	—	16P4	—
1-of-8 Decoder/Demultiplexer with Address Latch	**M74HC237P**	—	—	16P4	—
8-Bit Addressable Latch/1-of-8 Decoder	**M74HC259P**	—	—	16P4	—
1-of-10 Decoder	**M74HC42P**	38	38	16P4	2—22
1-of-16 Decoder/Demultiplexer	**M74HC154P**	—	—	24P4D	—
BCD-to-Seven-Segment Latch/Decoder/Display Driver	**M74HC4511P**	—	—	16P4	—
BCD-to-Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	**M74HC4543P**	—	—	16P4	—

Segment Identification of M74HC4511P, M74HC4543P

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9						

INDEX BY FUNCTION

ENCODERS

Circuit function	Type	Electrical characteristics		Package outlines	Page
		Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
Octal-to-BCD Priority Encoder	**M74HC148P**	—	—	16P4	—
Decimal-to-BCD Priority Encoder	**M74HC147P**	—	—	16P4	—

COMPARATORS

4-Bit Magnitude Comparator	**M74HC85P**	—	—	16P4	—
8-Bit Equality Comparator	**M74HC688P**	—	—	20P4	—

FULL ADDER

4-Bit Binary Full Adder with Fast Carry	**M74HC283P**	—	—	16P4	—

PARITY GENERATOR/CHECKER

9-Bit Odd/Even Parity Generator/Checker	**M74HC280P**	—	—	14P4	—

SYMBOLOGY

SYMBOLOGY

Symbol	Discriptions	
C_I	Input capacitance	
C_L	Load capacitance	Extenally connected load capacitance.
C_O	Output disabled capacitance	The output capacitance when the output is disabled.
C_{PD}	Power dissipation capacitance	Internal capacitance of the IC calculated from operation supply current.
C_X	External timing capacitance	External connected capacitanc used to set the output pulse width of a monostable multivibrator.
f_I	Input frequency	The sinewave frequency applied to the input terminal.
fmax	Maximum repetition frequency	Maximum input repetition frequency for normal IC operation.
GND	Ground	
H	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level.
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative.
I_{CC}	Supply current	The current flowing into the V_{CC} supply terminal.
I_{DD}	Supply current	The current flowing into the V_{DD} supply terminal.
I_I	Input current	Input current flowing into an input terminal when a voltage is applied.
I_{IH}	High-level input current	The current flowing into an input when a specified high voltage is applied.
I_{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied.
I_O	Output current	Output current flowing into ICs are taken to be positive and those flowing out as negative.
I_{OFF}	Off-state leakage current	The current flowing between the input and output of an analog switch is in the off state.
I_{OH}	High-level output curent	The current flowing out of an output which is in the high state.
I_{OL}	Low-level output current	The current flowing into an output which is in the low state.
I_{OZH}	Off-state high-level output current	The current flowing into a disable 3-state output with a specified high output voltage applied.
I_{OZL}	Off-state low-level output current	The current flowing out of a disabled 3-state output with a specified low output voltage applied.
L	Indicates the low level	Used in voltage current suffixes to indicate the low potential level.
O	Indicates output	
P_d	Power dissipation	Product of the supply voltage and the supply current.
R_I	Input resistance	Externally connected intput resistance.
R_L	Load resistance	Externally connected load resistance.
R_{OFF}	OFF resistance	The DC resistance between the input and output of an analog switch is in the off state.
R_{ON}	ON resistance	The DC resistance between the input and output of an analog switch is in the on state.
R_X	External connected timing resistor	Externally connected resistor used to set the output pulse width of a monostable multivibrator.
T_a	Operating free-air temperature	The temperature of the environment surrounding an IC.
t_f	Falltime	Amount of time for the clock pulse changing from high to low.
t_h	Hold time	Amount of time that input conditions must be held after related inputs arrive.
T_{opr}	Operating temperatuer	The ambient temperature range for normal IC operation.
t_{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time.
t_{PHL}	High-level to low-level output propagation time	Amount of time required from a change of input signal until the output changes from high to low.
t_{PHZ}	Output disable time from high-level	Amount of time required from a chage of input signal until the output changes from high to high-impedance.
t_{PLH}	Low-level to high-level output propagation time	Amount of time required from a change of input signal until the ourtput signal until output chages from low to high.
t_{PLZ}	Output disable time from low-level	Amount of time requied from a change of input signal until the output changes from low to high-impedance.
t_{PZH}	Output enable time to high-level	Amount of time required from a change of input signal until the output changes from high-impedance to high.
t_{PZL}	Output enable time to low-level	Amount of time required from a change of input signal unmtil the output changes from high-impedance to low.
t_r	Risetime	Amount of time for the clock pulse changing from low to high.
t_{rec}	Recovery time	Time from the point at which the input states are cancelled until the next clock pulse may be applied.
T_{stg}	Storage temperature	The range of surrounding storage temperature for an IC.
t_{SU}	Setup time	Amount of time that the input conditions must be maintained before related inputs are changed.

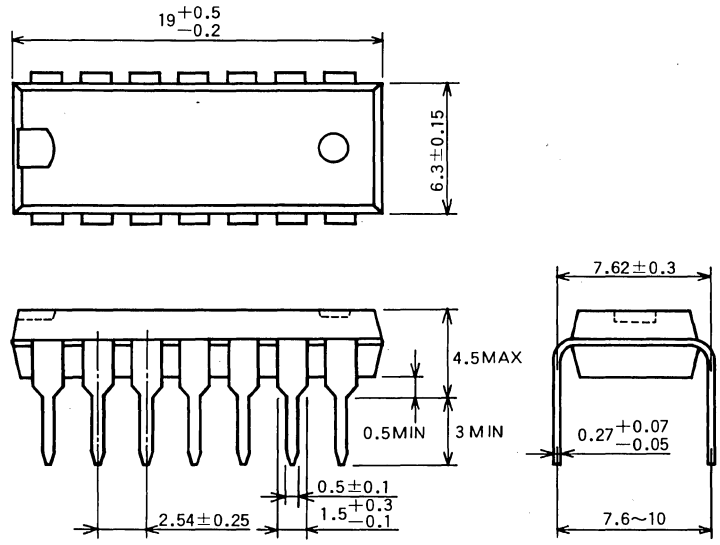
SYMBOLOGY

Symbol	Discriptions	
t_{THL}	High-level to low-level output transition time	The time required for the output waveform voltage value to change from the 90% point to the 10% point.
t_{TLH}	Low-level to high-level output transition time	The time required for the output waveform voltage value to change from the 10% point to the 90% point.
t_W	Pulse width	The time required for a pulse to change from one specified level to another.
t_{WQ}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator.
V_{CC}	V_{CC} supply voltage	
V_{DD}	V_{DD} supply voltage	
V_{EE}	V_{EE} supply voltage	
V_H	Hysteresis voltage	This voltage is the difference between the positive-going threshold and the negative-going threshold voltages of the Schmitt trigger circuit.
V_I	Input voltage	Voltage applied to an input.
V_{IH}	High-level input voltage	The range of input voltages that represents a logic high in the system.
V_{IL}	Low-level input voltage	The range of input voltages that represents a logic low in the system.
V_O	Output voltage	Voltage applied to or appearing at an ouptut.
V_{OH}	High-level output voltage	Voltage at an ouptut in the high state.
V_{OL}	Low-level output voltage	Voltage at an output in the low state.
V_{SS}	V_{SS} supply voltage	
V_T	Threshold voltage	The input voltage beyond at which the output changes.
V_{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to high.
V_{T-}	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changeing from high to low.
Z	Indicates the high-impedance state	Indicates that the output is in the high-impedance state.

PACKAGE OUTLINES

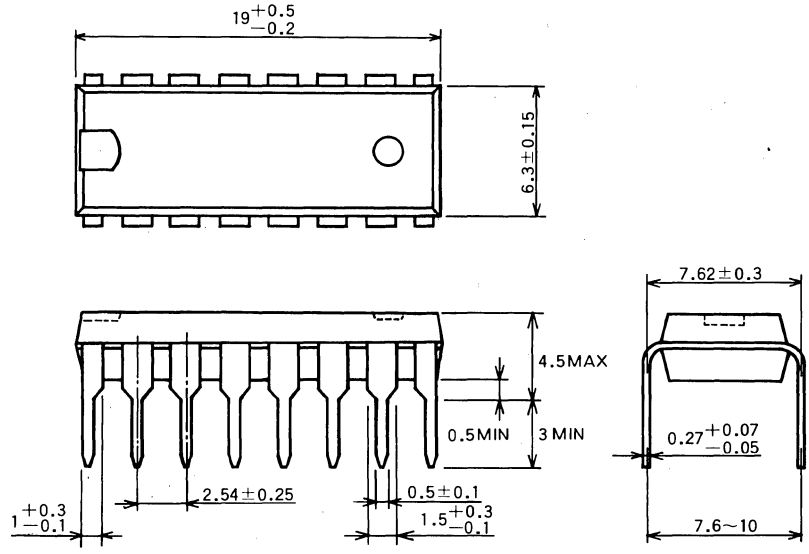
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimensions in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

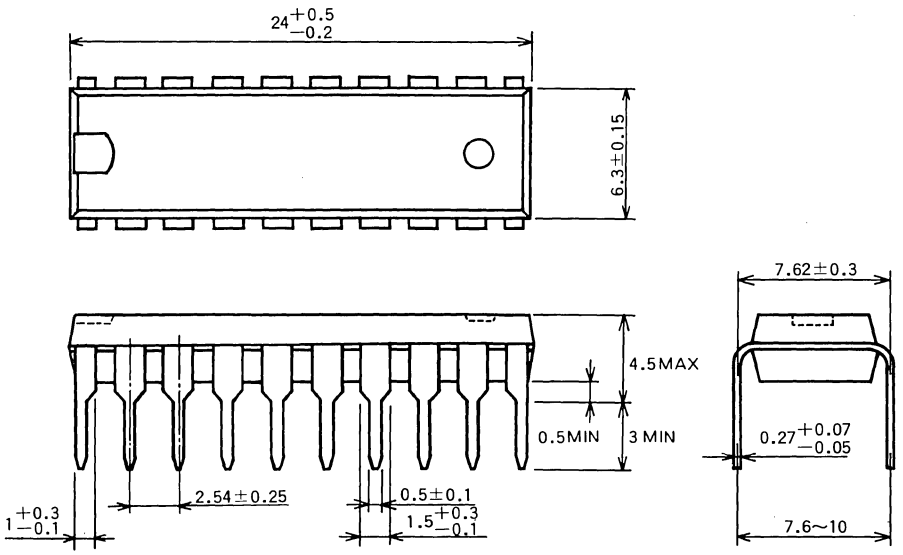
Dimensions in mm



PACKAGE OUTLINES

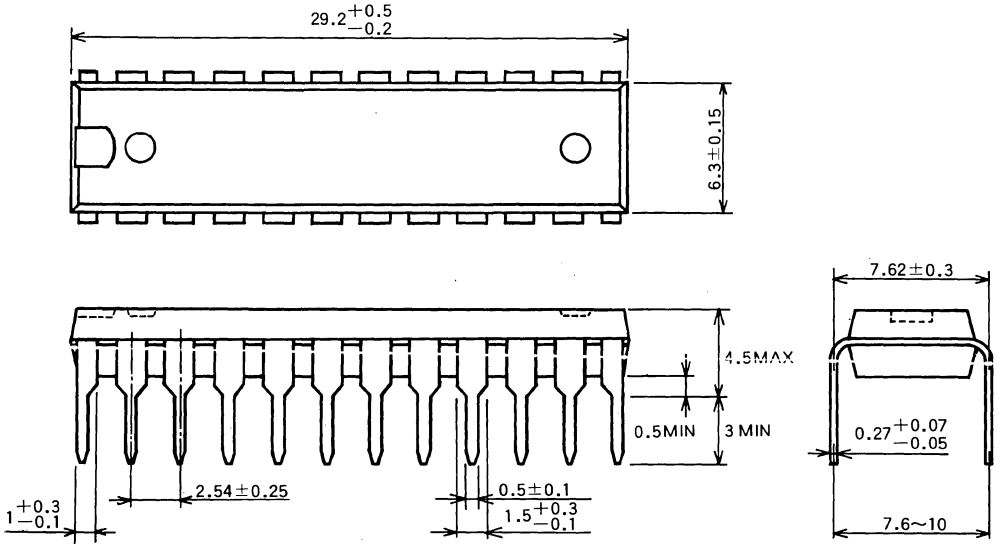
TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimensions in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIL

Dimensions in mm



DATA SHEETS

2

M74HC00P

QUADRUPLE 2-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC00P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

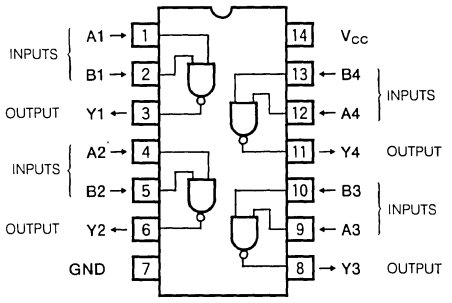
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC00P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

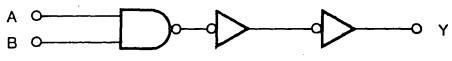
When both A and B inputs are high, output Y is low, and when at least one of the inputs is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

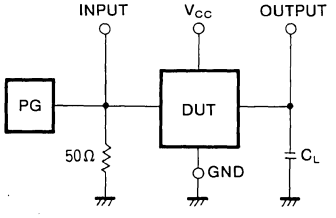
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				25				pF

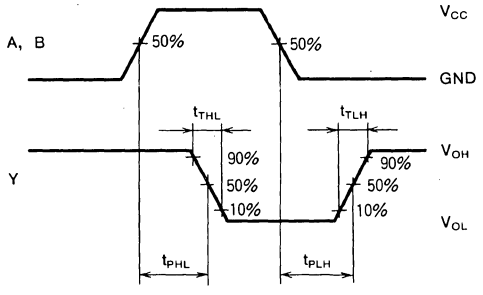
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC02P

QUADRUPLE 2-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC02P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

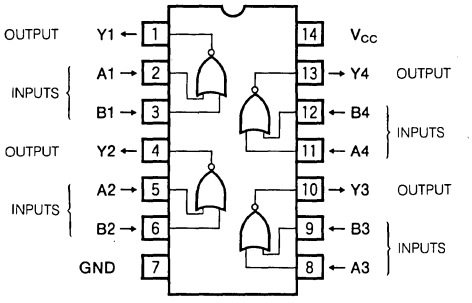
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC02P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS02.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both A and B inputs are low, output Y is high, and when at least one of the inputs is high, the output is low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

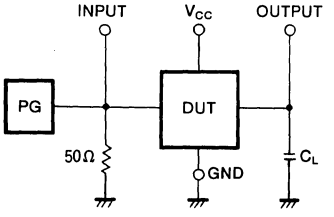
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

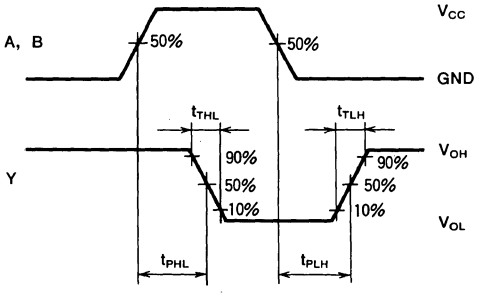
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCU04P

HEX UNBUFFERED INVERTER

DESCRIPTION

The M74HCU04P is a semiconductor integrated circuit consisting of six unbuffered inverters.

FEATURES

- High-speed: 7ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

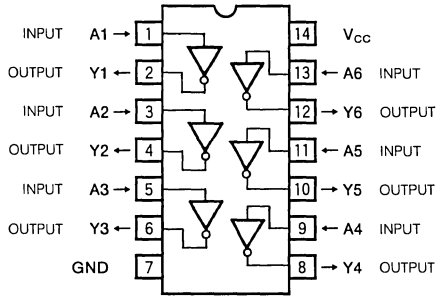
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

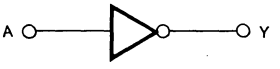
Use of silicon gate technology allows the M74HCU04P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04. Unbuffered Y outputs make this device suitable for linear circuit applications such as oscillators and amplifier circuits as well as logic system applications. However, consideration must be given in linear circuit applications dissipated power is much greater than of the 4000B series.
When input A is high, output Y is low, and when input A is low, output Y is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH INVERTER)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime			no Limit	ns

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.2V, $\|I_O\|$ = 20μA	2.0	1.7			1.7		V
		V_O = 0.5V, $\|I_O\|$ = 20μA	4.5	3.6			3.6		
		V_O = 0.5V, $\|I_O\|$ = 20μA	6.0	4.8			4.8		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.2V, $\|I_O\|$ = 20μA	2.0			0.3		0.3	V
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	4.5			0.8		0.8	
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	6.0			1.1		1.1	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OL} = −20μA	2.0	1.8			1.8		V
			4.5	4.0			4.0		
			6.0	5.5			5.5		
		V_I = GND, I_{OH} = −4.0mA	4.5	3.98			3.84		
		V_I = GND, I_{OH} = −5.2mA	6.0	5.48			5.34		
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = −20μA	2.0			0.2		0.2	V
			4.5			0.5		0.5	
			6.0			0.5		0.5	
		V_I = V_{CC}, I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{CC}, I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

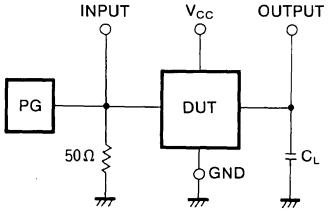
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				13	ns
t_{PHL}					13	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			82		103	ns
			4.5			16		21	
			6.0			14		18	
t_{PHL}			2.0			82		103	
			4.5			16		21	
			6.0			14		18	
C_I	Input capacitance					15		15	pF
C_{PD}	Power dissipation capacitance (Note 2)				25				pF

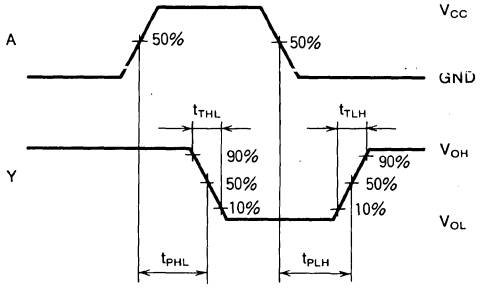
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC08P

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC08P is a semiconductor integrated circuit consisting of four 2-input positive-logic AND, usable as negative-logic OR gates.

FEATURES

- High-speed: 9.5ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

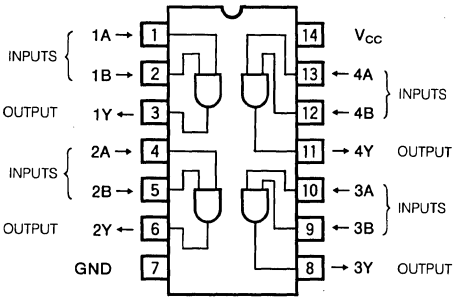
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC08P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

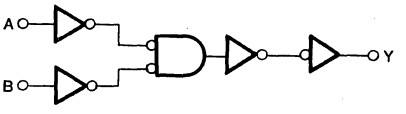
When both A and B inputs are high, output Y is high, and when at least one of the inputs is low, the output is low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

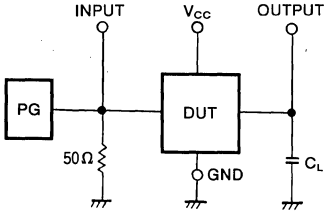
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
t_{PHL}			2.0			121		151	
			4.5			24		30	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				40				pF

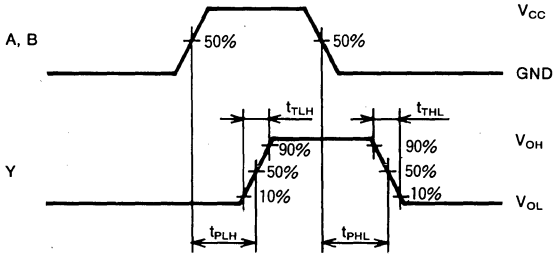
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC10P

TRIPLE 3-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC10P is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND, usable as negative-logic NOR gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

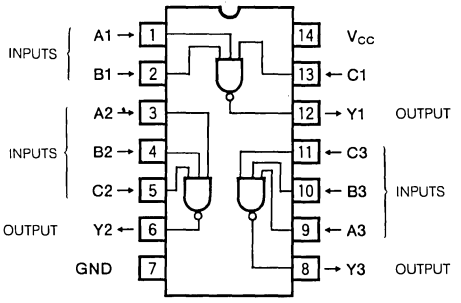
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC10P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS10.

Buffered Y outputs improve input-to-output transfer characteristics and reduce output impedance variations with respect to input voltage variations.

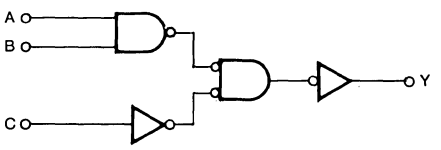
When all inputs A, B and C are high, output Y is low, and when at least one of the inputs is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

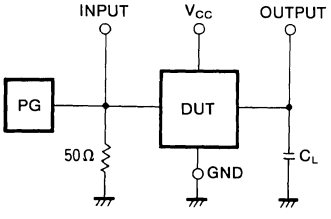
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			95		120	
			4.5			19		24	
			6.0			16		20	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				36				pF

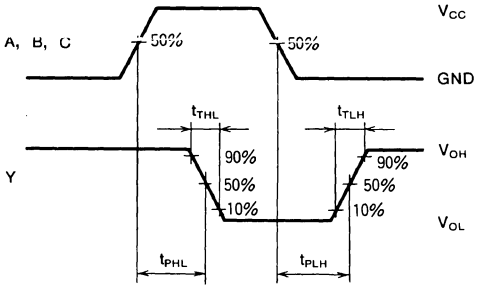
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC27P

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC27P is a semiconductor integrated circuit consisting of three 3-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

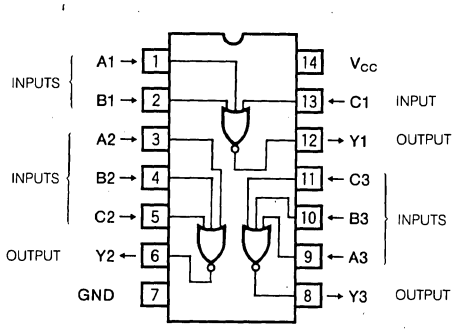
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC27P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS27.

Buffered Y outputs improve input-to-output transfer characteristics and reduce output impedance variations with respect to input voltage variations.

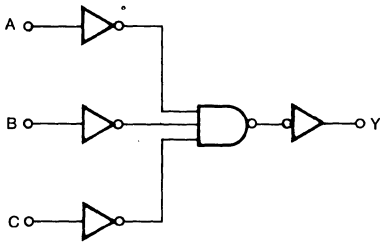
When all inputs A, B, and C are low, output Y is high, and when at least one of the inputs is high, the output is low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

N = B + C

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

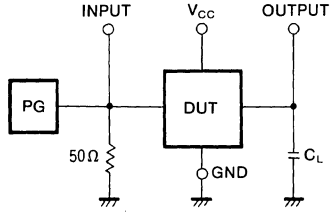
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

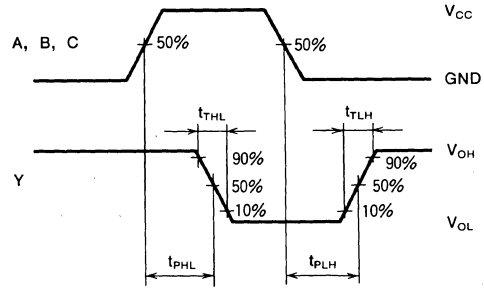
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC32P

QUADRUPLE 2-INPUT POSITIVE OR GATE

DESCRIPTION

The M74HC32P is a semiconductor integrated circuit consisting of four 2-input positive-logic OR, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

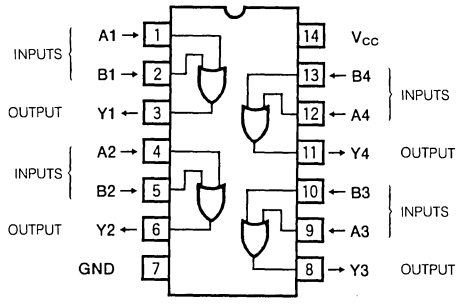
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC32P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS32.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

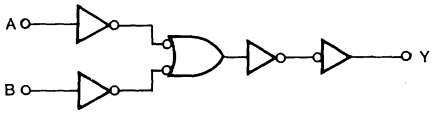
When both A and B inputs are low, output Y is low, and when at least one of the inputs is high, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

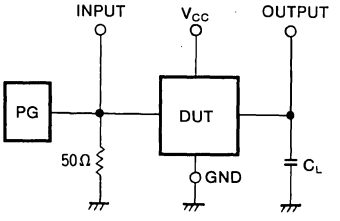
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				18	ns
t_{PHL}					18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)								pF

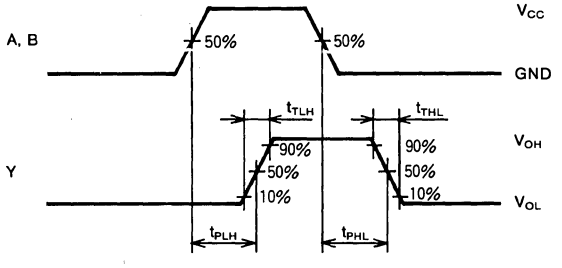
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC42P

1-OF-10 DECODER

DESCRIPTION

The M74HC42P is a semiconductor integrated circuit consisting of a BCD to decimal decoder.

FEATURES

- Active-low output
- High speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

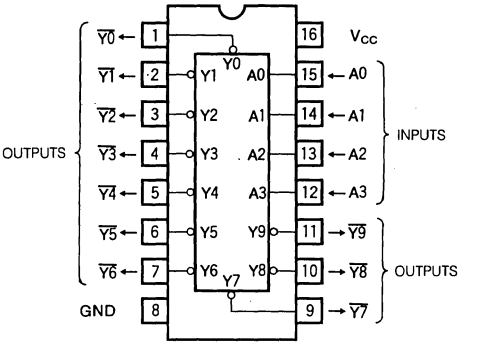
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC42P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS42.

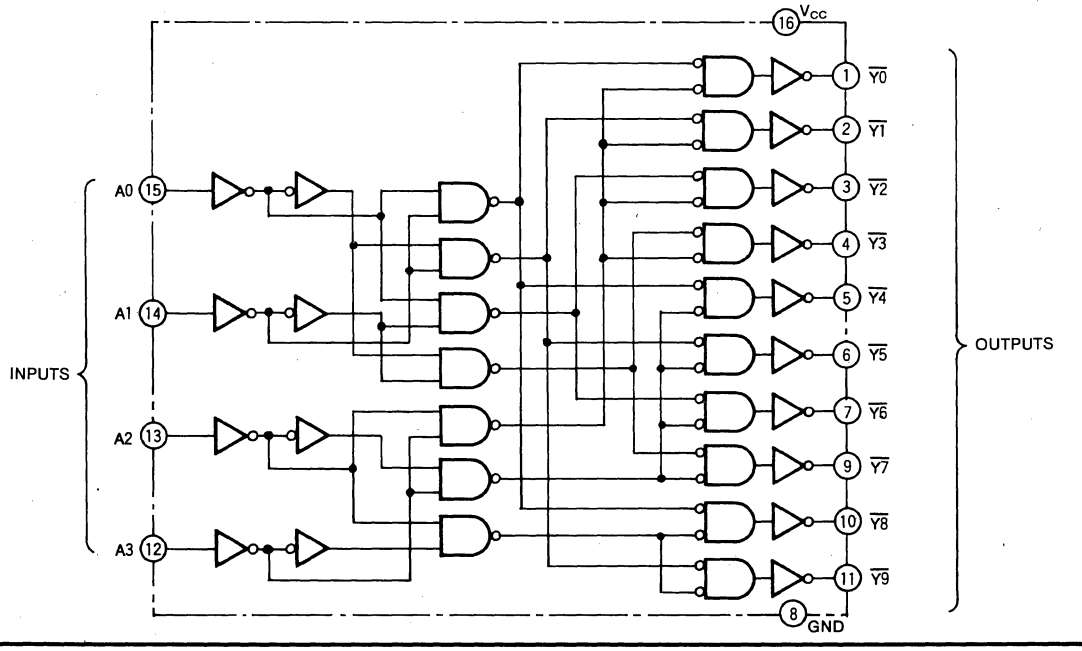
When a BCD code is applied to inputs A0, A1, A2, and A3, the one output of the outputs $\overline{Y0}$ through $\overline{Y9}$ corresponding to this input value changes to low and all others become high. Use A0 for the least significant bit and A3 for the most significant bit. If a value of ten or greater is applied to the inputs (A0 through A3), all outputs will go high.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE

Decimal number	Inputs				Outputs									
	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

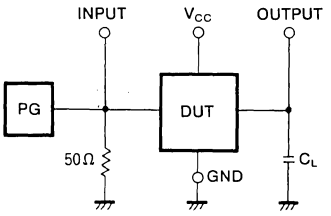
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				25	ns
t_{PHL}					25	

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)								pF

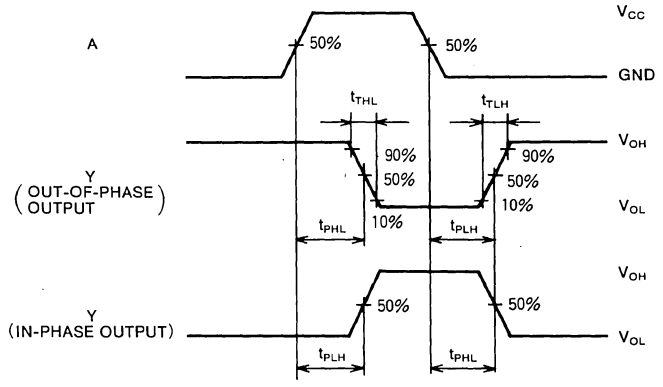
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC73P

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC73P is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

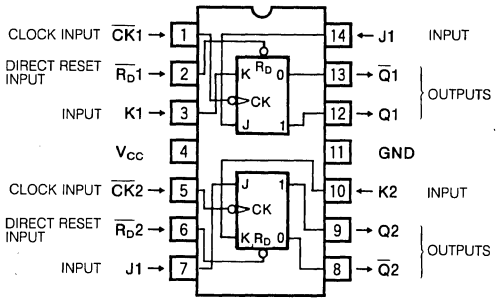
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

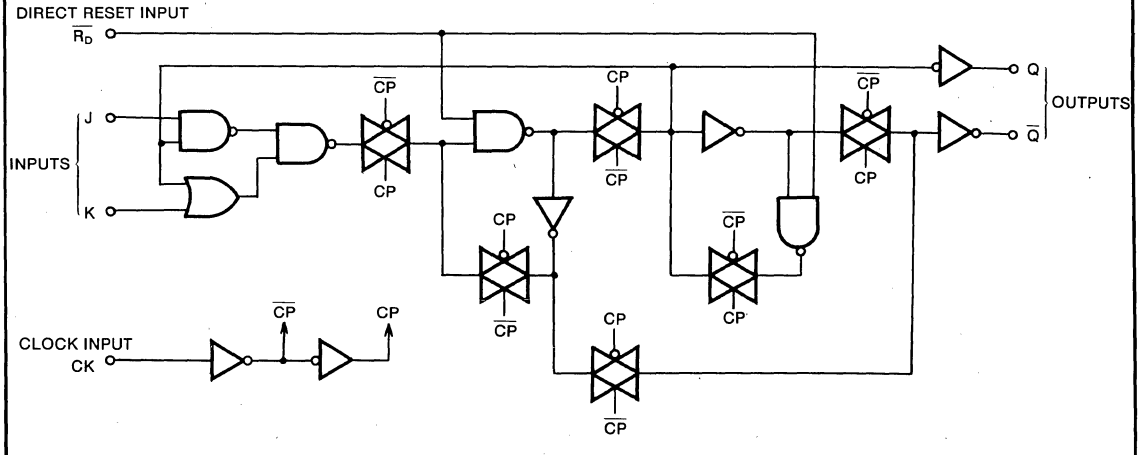
Use of silicon gate technology allows the M74HC73P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS73.

The M74HC73P contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset input $\overline{R_D}$, and both J and K inputs.

When $\overline{CK}$ changes from high-level to low-level, the data just previously at J and K signals appear in output Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ become low-level and high-level respectively, irrespective of the state of the other input signals. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high.

A unit, the M74HC107P, having the same functions and electrical characteristics as the M74HC73P but with pins 7 and 14 being GND and Vcc respectively is also available.

LOGIC DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed.
$\overline{Q}^0$: Output state $\overline{Q}^0$ before clock input changed.
Toggle : Inverted state before clock input changed.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PHL}					21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

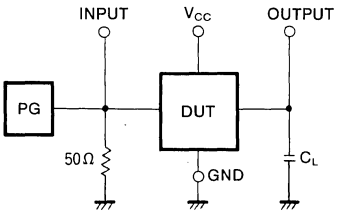
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			155		194	ns
			4.5			31		39	
			6.0			26		32	
t_{PHL}			2.0			155		194	
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

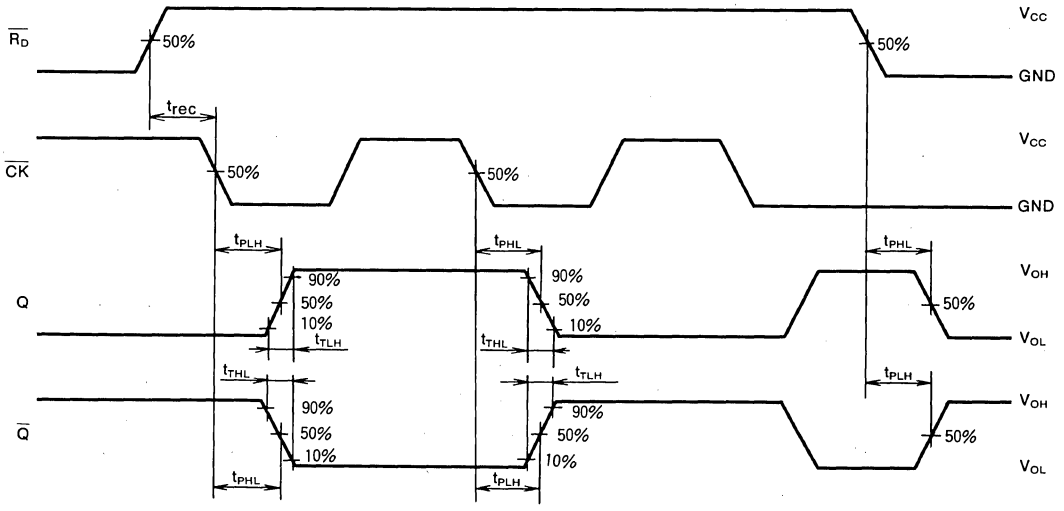
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J and K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J and K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

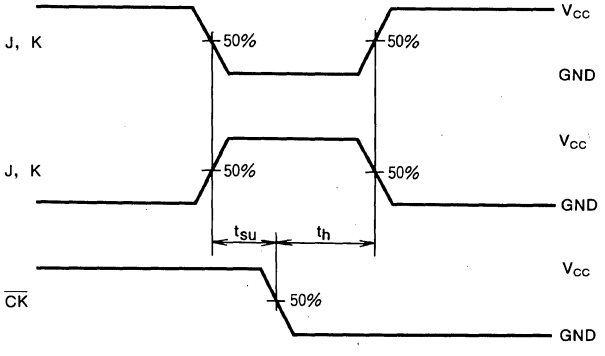
Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC74P

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC74P is a semiconductor integrated circuit consisting of two positive-edge triggered D-types flip flops with independent clock, data, and direct set and reset inputs.

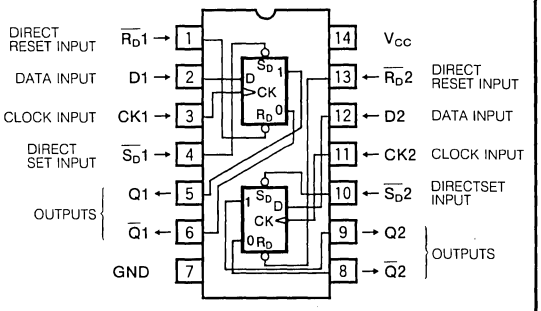
FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

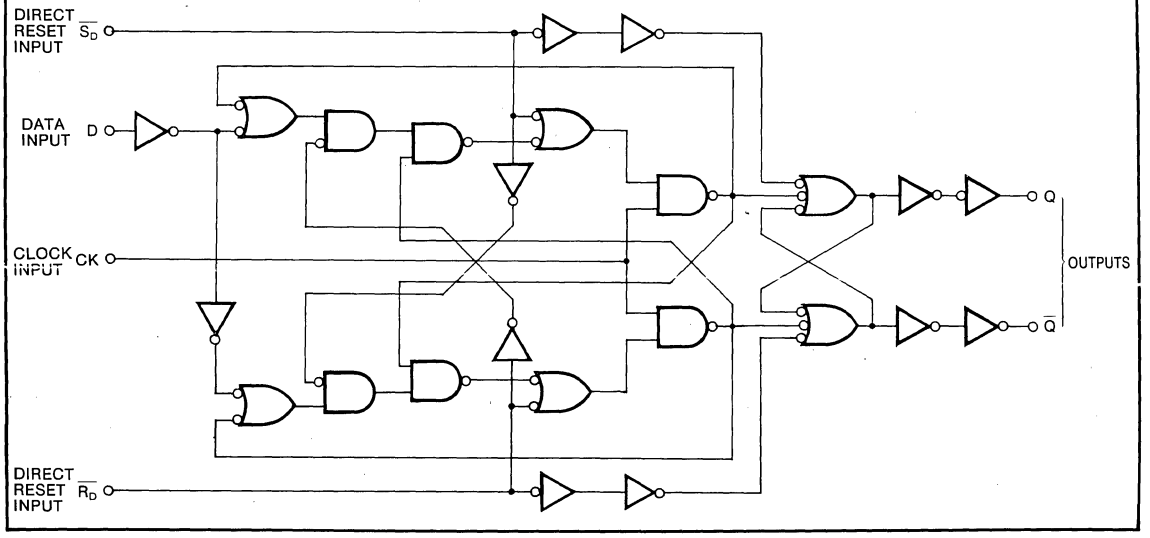
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC74P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS74.

The M74HC74P contains two independent D-type flip flops, each circuit with clock input CK, direct set input $\overline{S_D}$, and direct reset input $\overline{R_D}$.

When used as a D-type flip flop, both $\overline{S_D}$ and $\overline{R_D}$ are held at high. When clock input CK changes from low-level to high-level, the data just previously input at D appears at the output Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ are both high-level but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	H	X	Q^0	$\overline{Q}^0$
H	H	↓	X	Q^0	$\overline{Q}^0$

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed.
$\overline{Q}^0$: Output state $\overline{Q}^0$ before clock input changed.
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ are both high-level but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

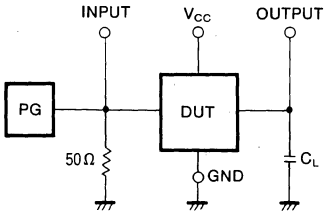
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)				30	ns
t_{PHL}					30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)				40	ns
t_{PHL}					40	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				47				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Cricuit

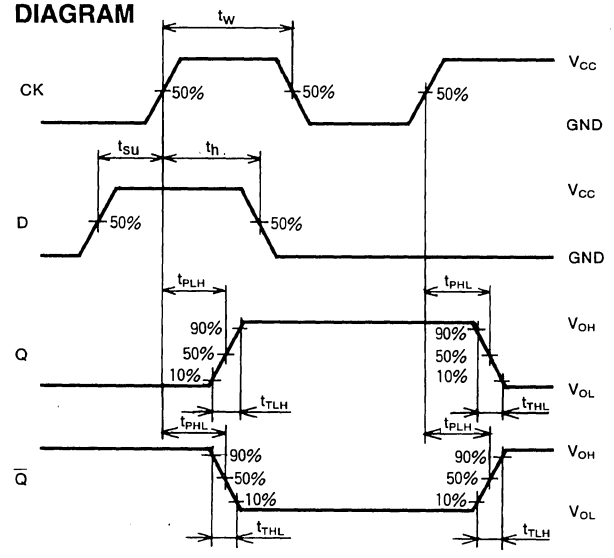


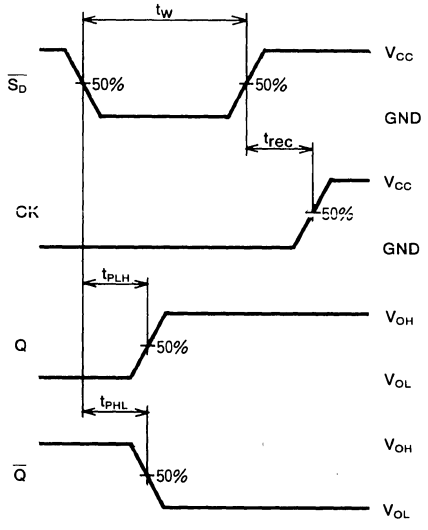
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

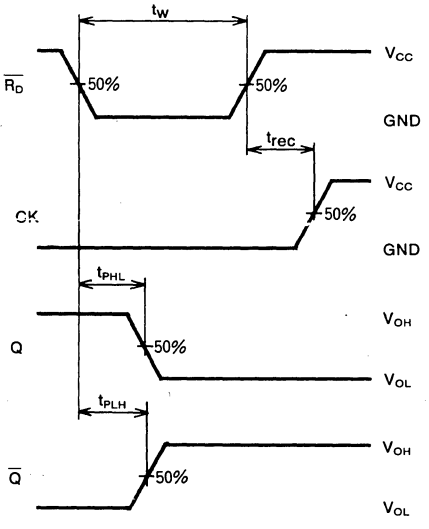
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$, $\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

TIMING DIAGRAM







M74HC76P

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC76P is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

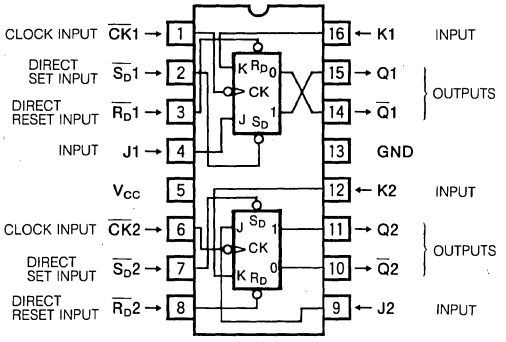
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

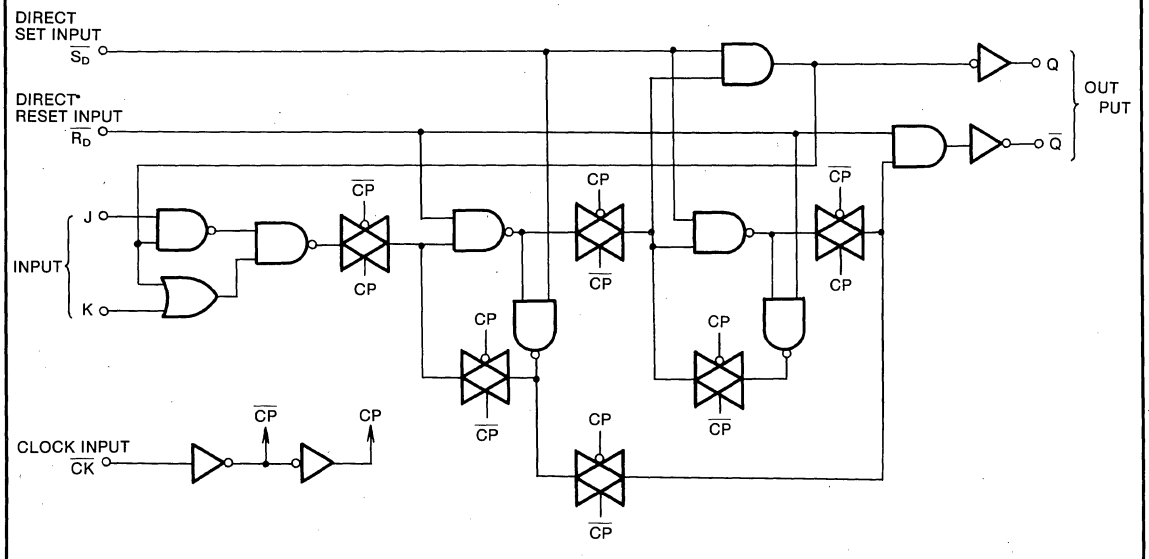
Use of silicon gate technology allows the M74HC76P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS76.

The M74HC76P contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$ inputs, and both J and K inputs.

When $\overline{CK}$ changes from high-level to low-level, the data just previously input at J and K signals appear in output Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ become low, Q and $\overline{Q}$ both become high-level but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high.

An integrated circuit, the M74HC112P, is also available. This IC has same functions and electrical characteristics as the M74HC76P but with pin 8 being GND and pin 16 V_{CC}.

LOGIC DIAGRAM (EACH GATE)



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FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed.
$\overline{Q}^0$: Output state $\overline{Q}_0$ before clock input changed.
Toggle : Inverted state before clock input changed.
* : When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are both high-level but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)				21	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)				26	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time ($\overline{S_D}$ – Q, $\overline{Q}$)				28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

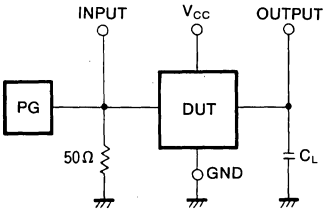
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			22		27	
t_{PHL}			2.0			126		160	
			4.5			25		32	
			6.0			22		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)		2.0			155		191	ns
			4.5			31		39	
			6.0			26		33	
t_{PHL}			2.0			155		191	
			4.5			31		39	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ – Q, $\overline{Q}$)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		210	
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

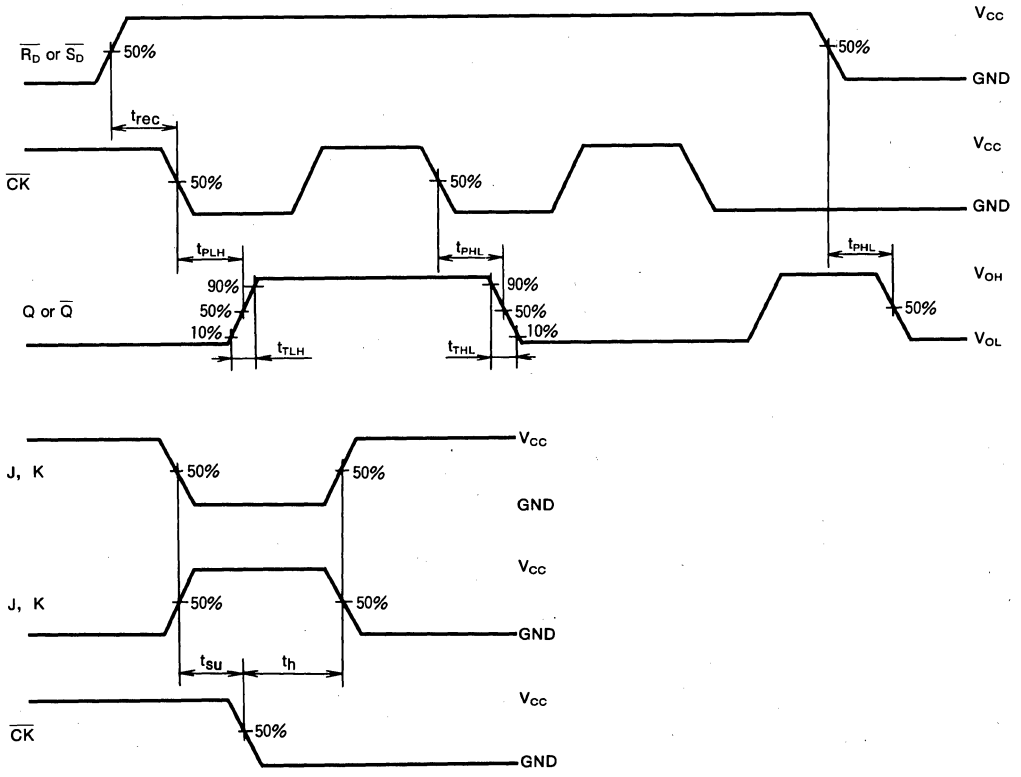
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$, $\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC86P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74HC86P is a semiconductor integrated circuit consisting of four 2-input exclusive OR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC86P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS86.

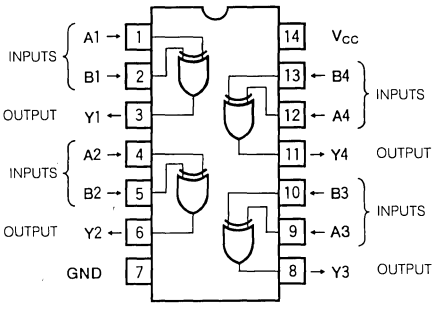
Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, output Y is low, and when the levels of the two inputs are opposite, the output is high.

FUNCTION TABLE

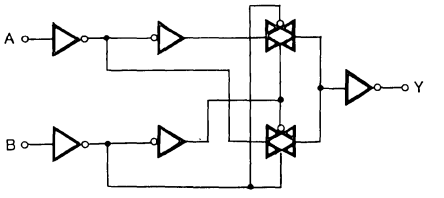
Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} / I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} / I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

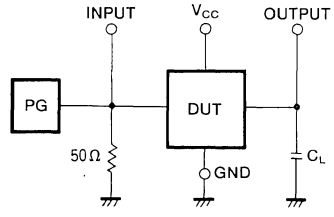
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				41				pF

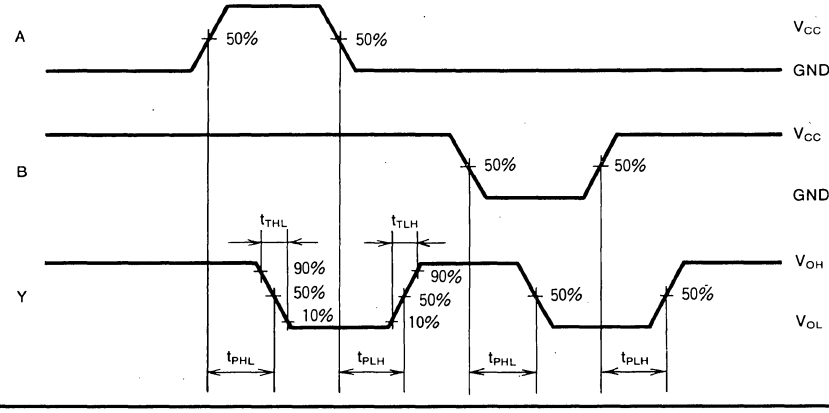
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC107P

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC107P is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

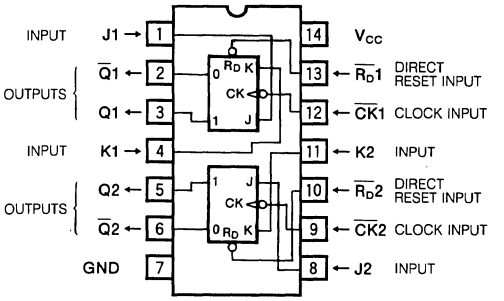
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

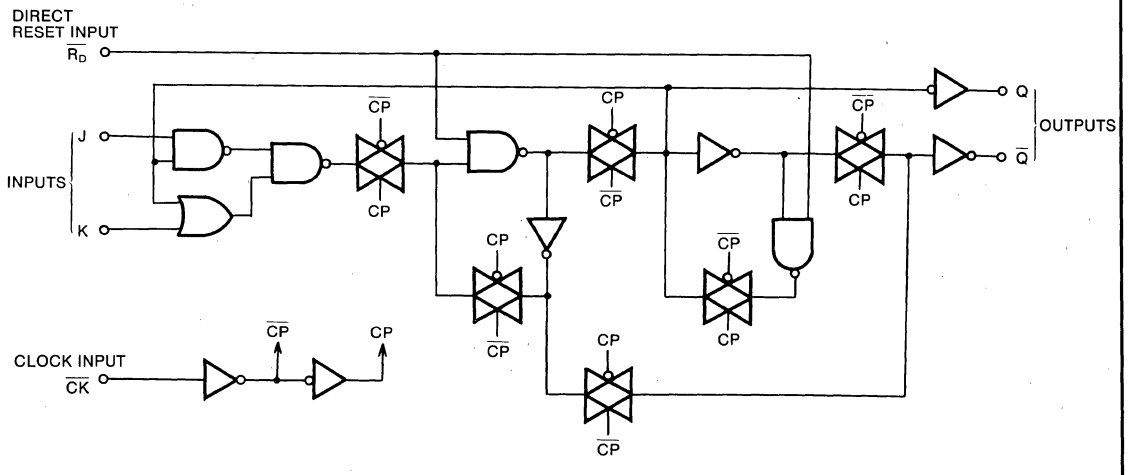
Use of silicon gate technology allows the M74HC107P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS107.

The M74HC107P contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset $\overline{R_D}$, and both J and K inputs.

When $\overline{CK}$ changes from high-level to low-level, the data just previously input at J and K signals appear in output Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ become low-level and high-level respectively, irrespective of the state of the other input signals. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high.

M74HC107P and M74HC73P are functionally and electrically identical, differing only in pin arrangement.

LOGIC DIAGRAM (EACH FLIP FLOP)



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FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed.
$\overline{Q}^0$: Output state $\overline{Q}^0$ before clock input changed.
Toggle : Inverted state before clock input changed.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PHL}					21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

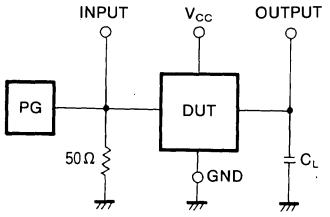
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			155		194	ns
			4.5			31		39	
			6.0			26		32	
t_{PHL}			2.0			155		194	
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

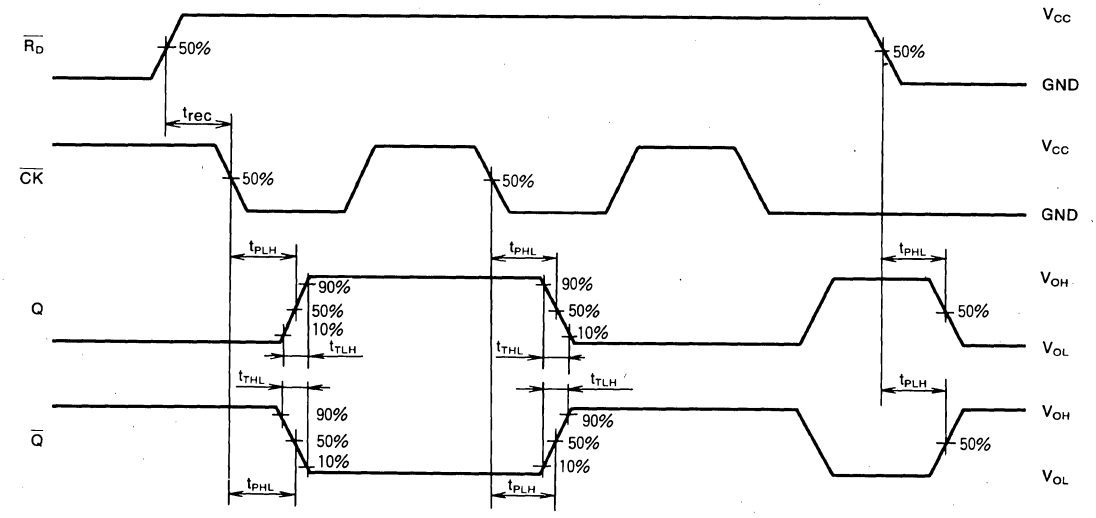
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J and K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J and K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

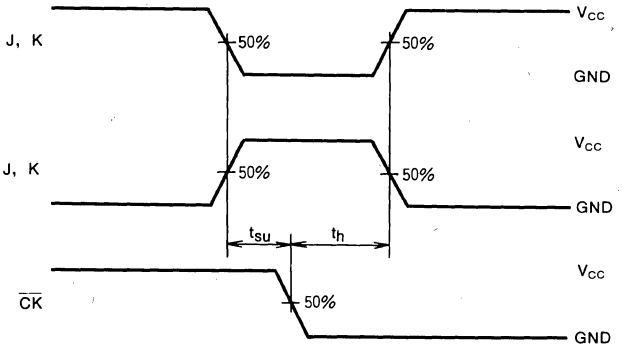
Note 3. Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC138P

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC138P is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with chip-select inputs.

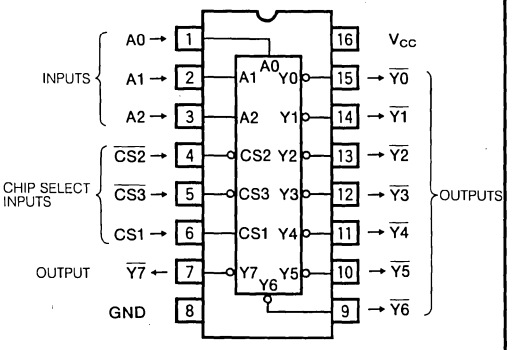
FEATURES

- Selection of three types of chip inputs
- Expansion up to 24 outputs possible with externally connection.
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

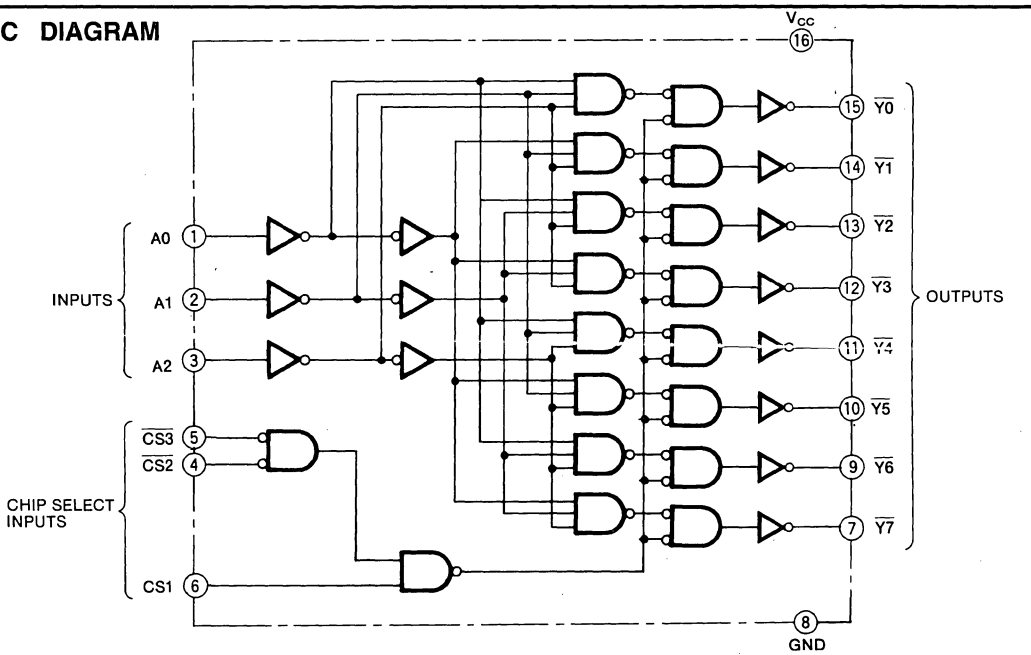
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC138P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

When operated as a decoder, the inputs A0, A1, and A2 are designated with a 3-bit binary code, the one ouptut of $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value becomes low-level and the remaining seven outputs become high-level. In this case, chip select input CS1 must be high-level while $\overline{CS2}$ and $\overline{CS3}$ are held at low-level. When CS1, $\overline{CS2}$, and $\overline{CS3}$ are in conditions other than those given above, the outputs are all high-level irrespective of the level of A0 through A2.

When operated as a 1-line to 8-line demultiplexer, CS1, $\overline{CS2}$ or $\overline{CS3}$ is used as Data Input and A0, A1 and A2 input are as slecting input.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

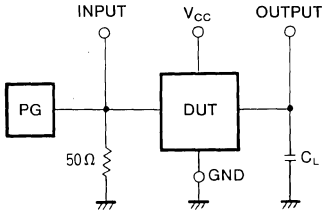
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				25	ns
t_{PHL}					35	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)				25	ns
t_{PHL}					25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				25	ns
t_{PHL}					30	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)				82				pF

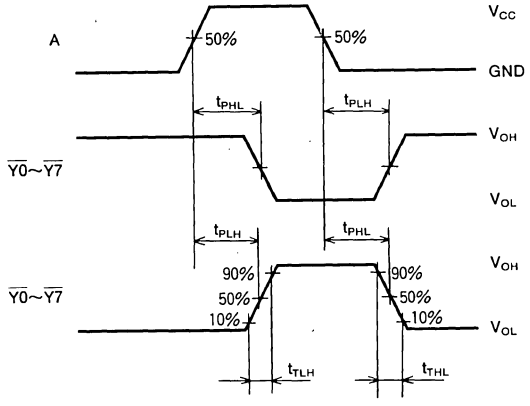
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

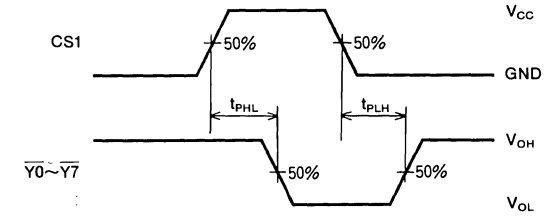
Note 3 : Test Cricuit

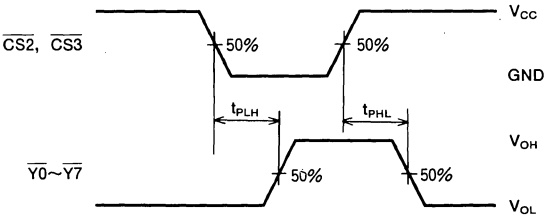


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC157P

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC157P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

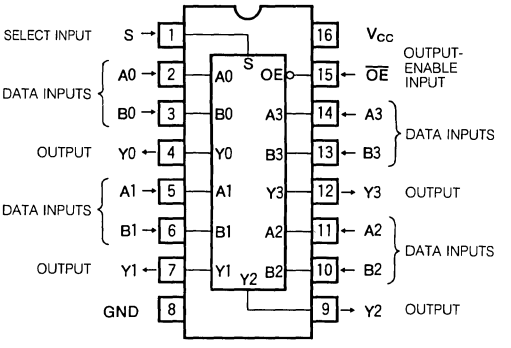
Use of silicon gate technology allows the M74HC157P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS157.

The M74HC157P consists of four circuits each combining data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into to serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B data will be serial output at Y synchronous with the clock pulse in the order A-B. Both S and ouput-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ becomes high, all the outputs, Y0 though Y3, become low-level irrespective of input signals.

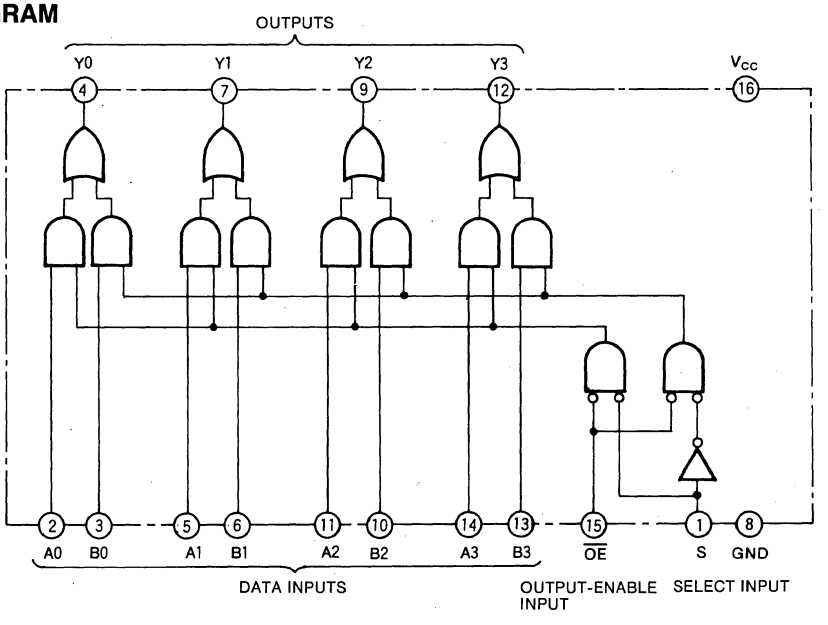
M74HC157P and M74HC257P are identical in function and in pin arrangement, differing in that the output of M74HC257P is 3-state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	Limits −40～+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

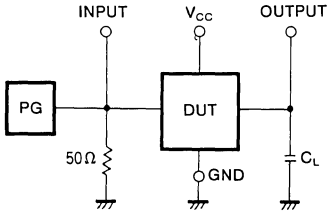
Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A, B − Y)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (S − Y)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time ($\overline{OE}$ − Y)				18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)				51				pF

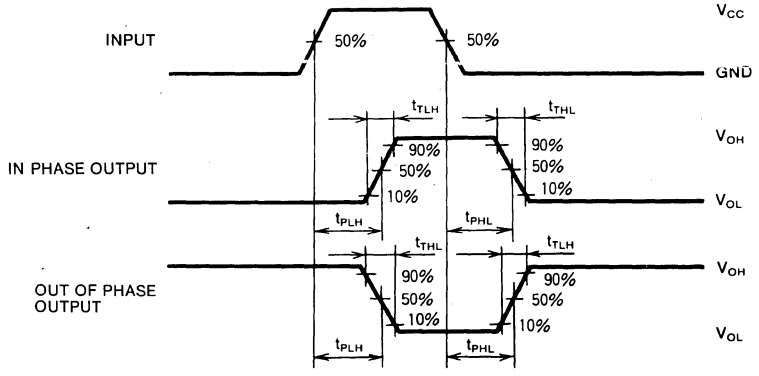
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC158P

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC158P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

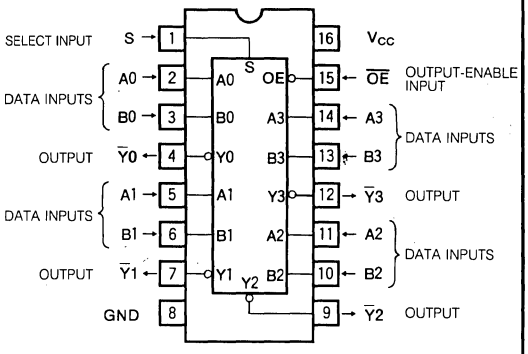
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC158P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS158.

The M74HC158P consists of four circuits each combining data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into to serial data using time-division.

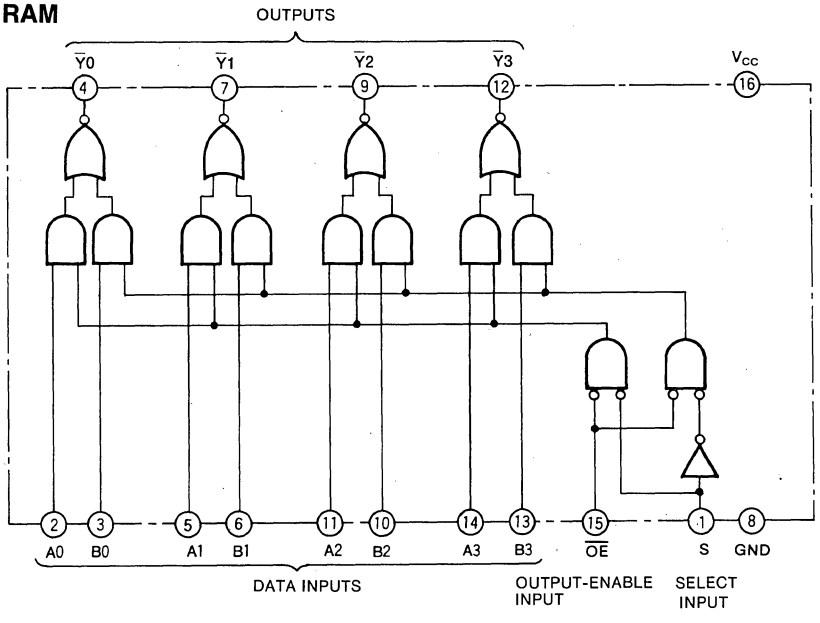
The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is inverted and output at pin $\overline{Y}$. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the inverted A and B data will be serial output at $\overline{Y}$ synchronous with the clock pulse in the order A-B. Both S and ouput-enable input are common to all four circuits. When $\overline{OE}$ becomes high-level, all the outputs, $\overline{Y}$0 though $\overline{Y}$3, become high-level irrespective of input level signals.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		4.4		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

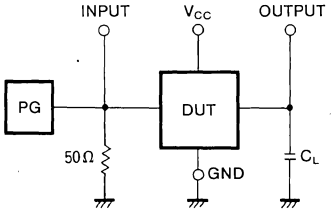
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)				20	ns
t_{PHL}					20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)				20	ns
t_{PHL}					20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)				18	ns
t_{PHL}					18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				82				pF

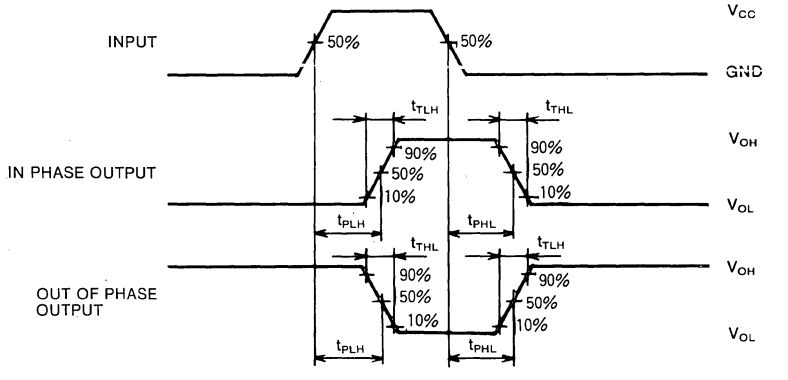
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC174P

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC174P is a semiconductor integrated circuit consisting of six edge-triggered D-type flip flops with common clock and direct reset inputs, as well as independent data input.

FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

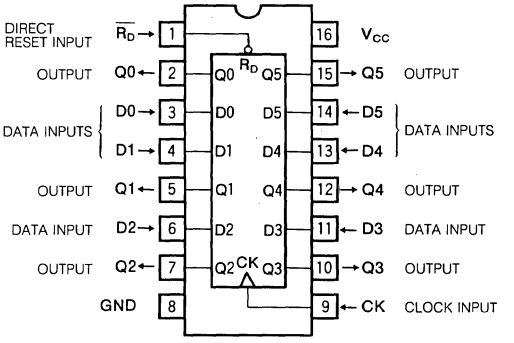
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC174P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS174.

The M74HC174P contains six edge-triggered D-type flip flops, sharing common clock CK and direct reset $\overline{R_D}$ inputs. When clock input CK changes from low-level to high-level the data just previously input at D appears at the Q output in accordance with the function table given.

When $\overline{R_D}$ becomes low, all the Q outputs become low irrespective of the other input signals. When used as a D-type flip flop, $\overline{R_D}$ is held at high-level.

PIN CONFIGURATION (TOP VIEW)



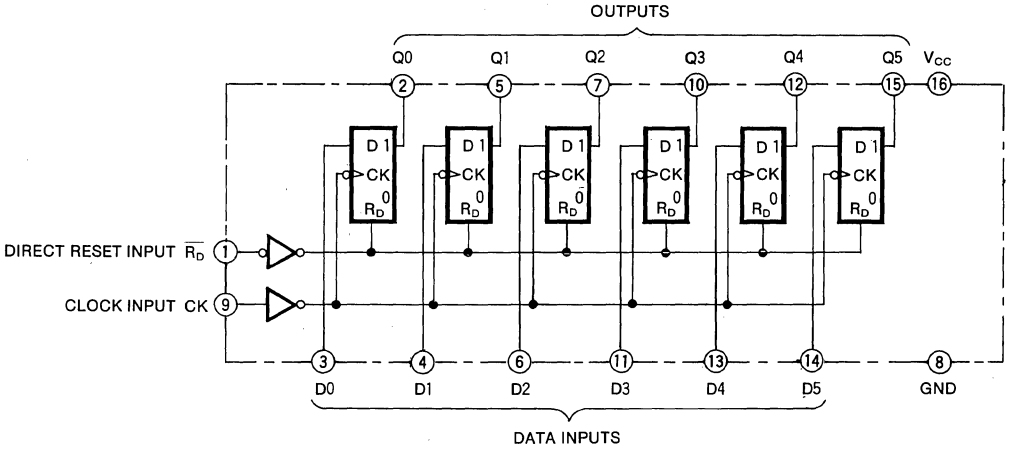
Outline 16P4

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
H	↑	H	H
H	↑	L	L
H	↓	X	Q^0
L	X	X	L
H	L	X	Q^0

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				30	ns
t_{PHL}					30	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

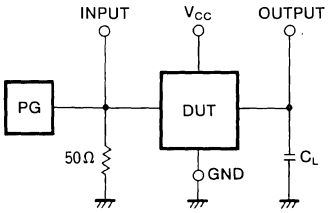
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		206	
			4.5			33		41	
			6.0			28		35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)				64				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

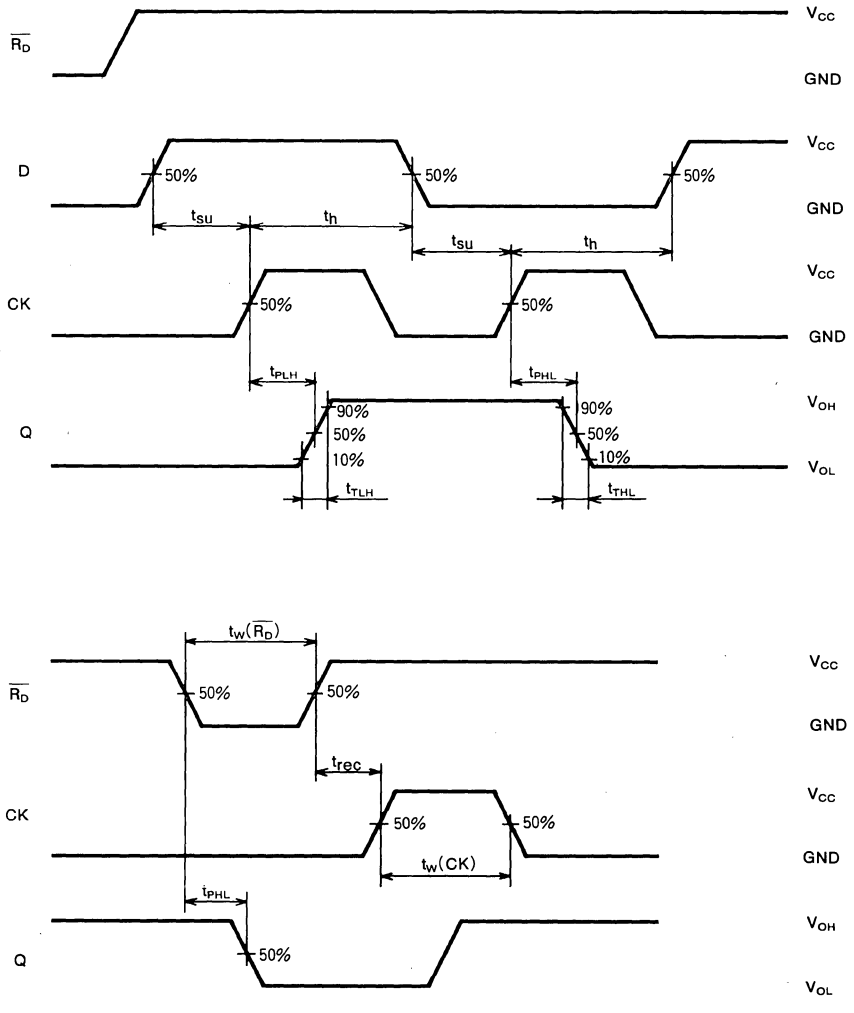
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w(CK)	Clock pulse width		2.0			80		106	ns
			4.5			16		20	
			6.0			14		18	
$t_w(\overline{R_D})$	Direct clear pulse width		2.0			80		106	ns
			4.5			16		20	
			6.0			14		18	
t_{su}	D setup time with respect to CK		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_h	D hold time with respect to CK		2.0			5		5	ns
			4.5			5		5	
			6.0			5		5	
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0			5		5	ns
			4.5			5		5	
			6.0			5		5	

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC240P

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240P is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

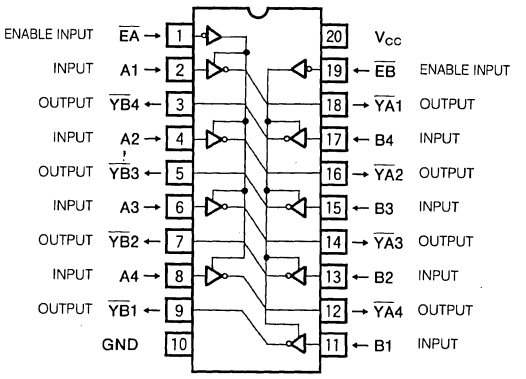
The M74HC240P consists of two independent blocks and each block has four buffered circuits.

When enable $\overline{E}$ is low and A (or B) is low then output $\overline{Y}$ is high-level. However, if A (or B) is high then $\overline{Y}$ is low-level.

When $\overline{E}$ is high then all outputs within the block become high-impedance state, irrespective of A (or B).

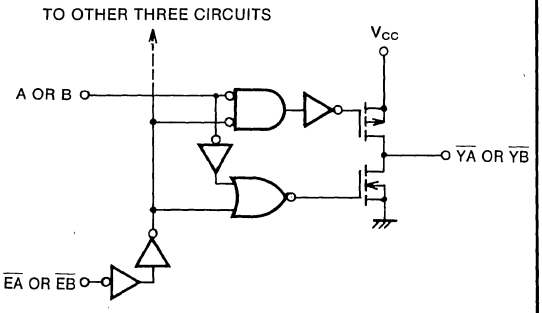
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Outputs
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IL}, I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IL}, I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IL}, I_{OH} = −6.0mA	4.5	4.18			4.13		
		V_I = V_{IL}, I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 6.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL}, I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

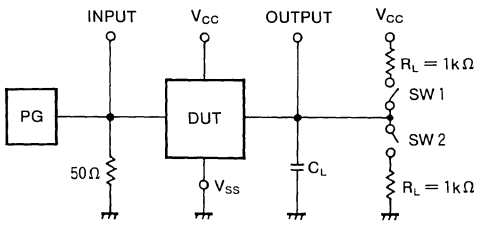
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from high-level and low-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to high-level and low-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)	C_L = 50pF (Note 3)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 3)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from high-level and low-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to high-level and low-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Three-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}							
C_{PD}	Power dissipation capacitance (Note 4)				57				

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

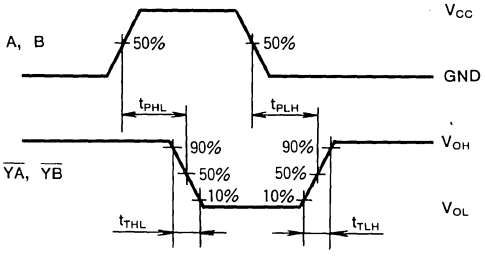
Note 3 : Test Cricuit

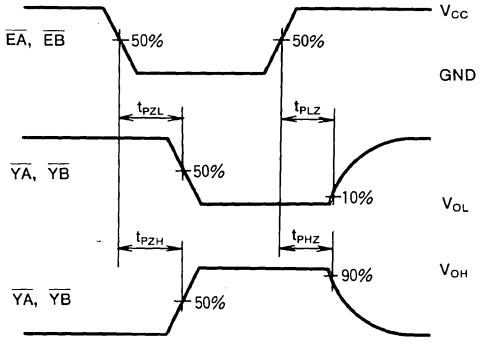


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC241P

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241P is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

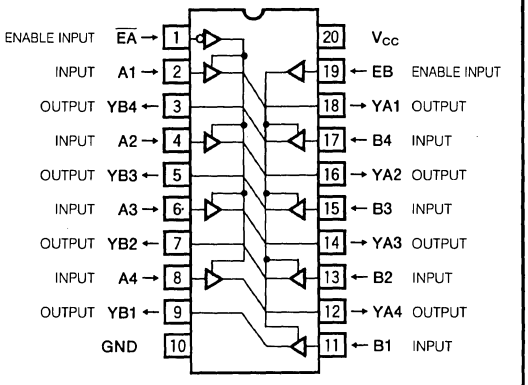
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

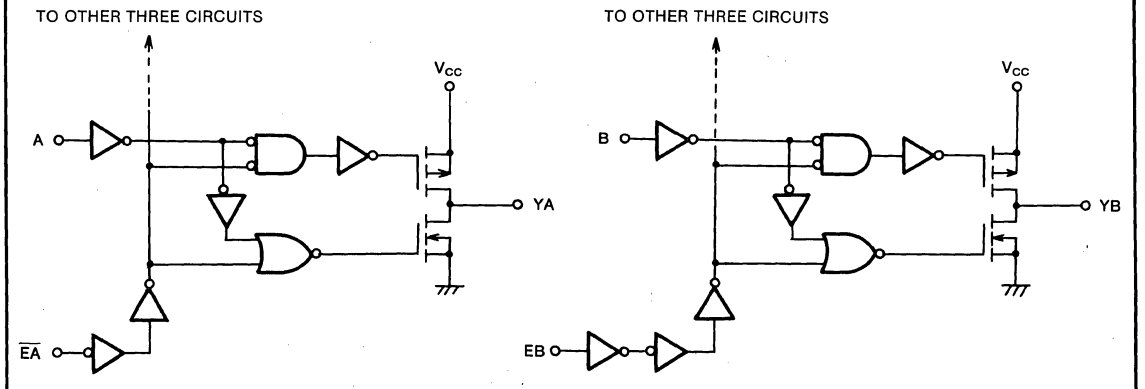
Use of silicon gate technology allows the M74HC241P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The M74HC241P consists of two independent blocks with each block containing four buffers.

When enable $\overline{EA}$ is low and input A is low then output YA is low-level. However, if A is high then YA is high-level. Inverted in the other block, a high-level enable EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all outputs within the block become high-impedance state, irrespective of A or B.

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.13			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

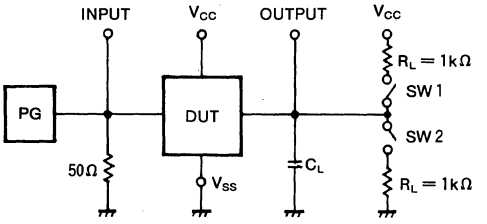
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				20	ns
t_{PHL}					20	
t_{PLZ}	Output disable time from high-level and low-level ($\overline{EA}$ − YA, EB − YB)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to high-level and low-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 3)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 3)	2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from high-level and low-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to high-level and low-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Three-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND							
C_{PD}	Power dissipation capacitance (Note 4)				59				

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

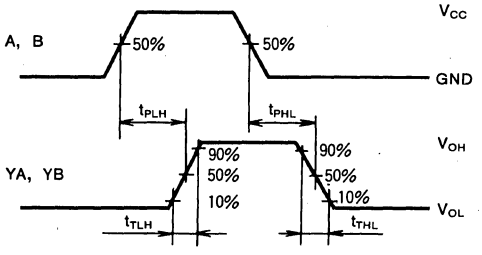
Note 3 : Test Cricuit

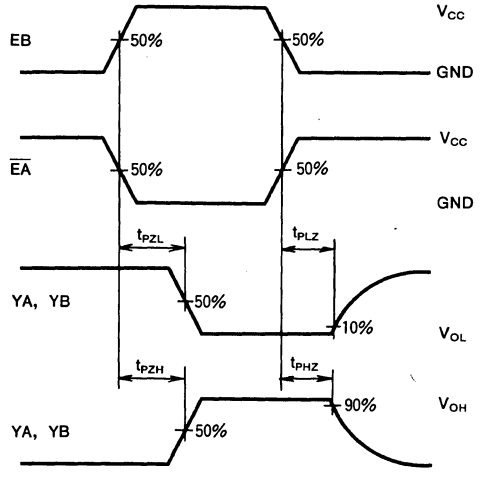


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC244P

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244P is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

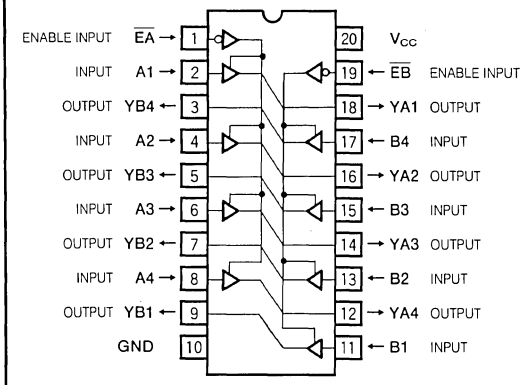
The M74HC244P consists of two independent blocks with each block containing four buffers.

When enable $\overline{E}$ is low and input A (or B) is low then output Y is low-level. However, if A (or B) is high then Y is high-level.

When $\overline{E}$ is High then all outputs within the block become high-impedance state, irrespective of A or B.

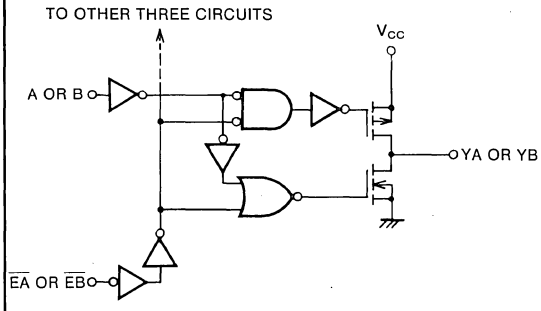
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Outputs
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

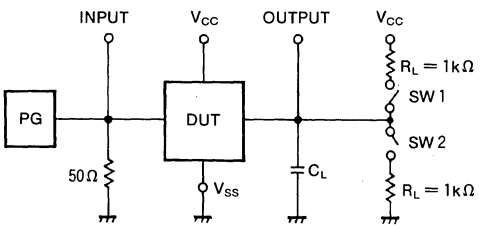
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A − YA, B − YB)				20	
t_{PLZ}	Output disable time from high-level and low-level	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}	($\overline{EA}$ − YA, $\overline{EB}$ − YB)				25	
t_{PZL}	Output enable time to high-level and low-level	C_L = 50pF (Note 3)			28	ns
t_{PZH}	($\overline{EA}$ − YA, $\overline{EB}$ − YB)				28	

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 3)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 3)	2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from high-level and low-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to high-level and low-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Three-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}							
C_{PD}	Power dissipation capacitance (Note 4)				57				

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

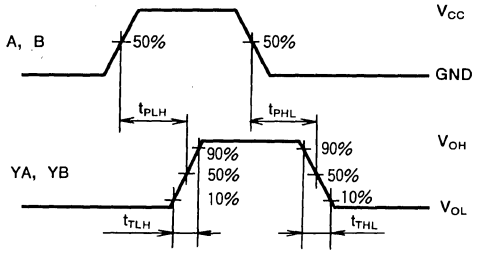
Note 3 : Test Cricuit

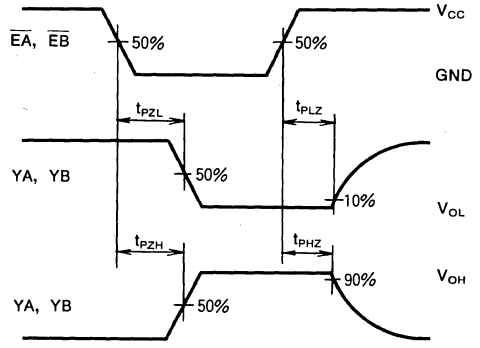


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC266P

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The M74HC266P is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

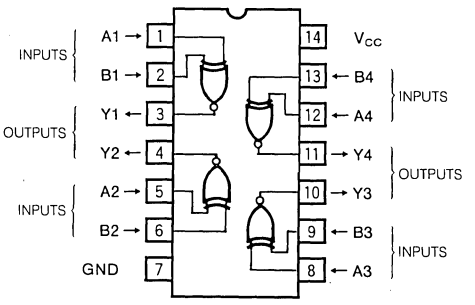
Use of silicon gate technology allows the M74HC266P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are high-level or low-level, output Y is high-level, and when the levels of A and B are opposite then Y is low-level.

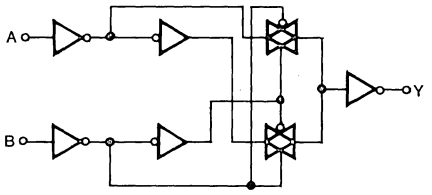
Note that the output of M74HC266P and 74LS266 differ in that the output of the M74HC266P is not open drain.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

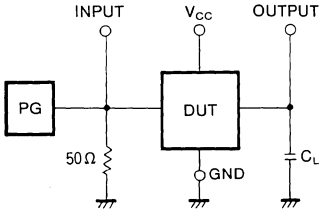
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				38				pF

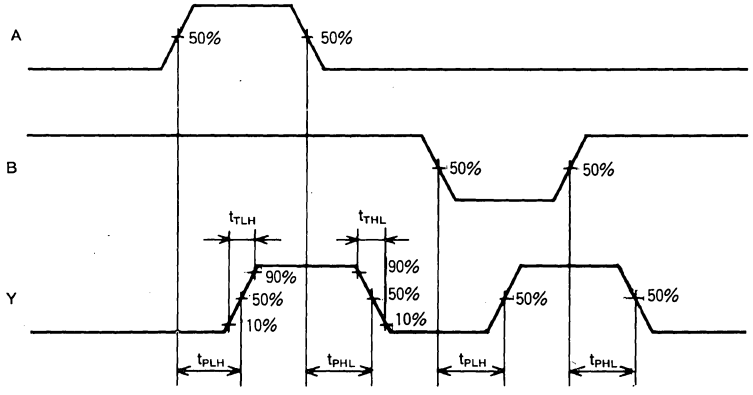
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC273P

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC273P is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

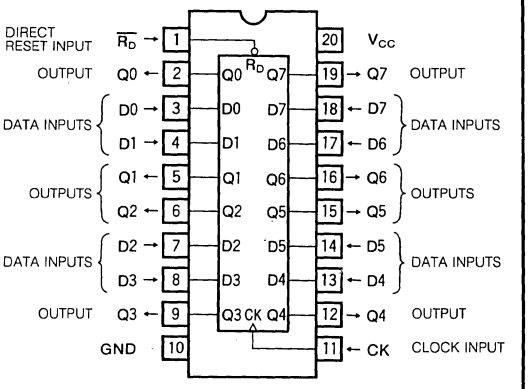
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC273P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS273.

The M74HC273P contains eight edge-triggered D-type flip flops, sharing common clock CK and direct reset $\overline{R_D}$ inputs. When clock input CK changes from low-level to high-level the data just previously input at D appears at the Q output in accordance with the function table given.

When $\overline{R_D}$ is low then all outputs, 0Q through 7Q, become low-level irrespective of the state of either CK or data inputs, 0D through 7D. When used as a D-type flip flop, $\overline{R_D}$ is held at high-level.

PIN CONFIGURATION (TOP VIEW)



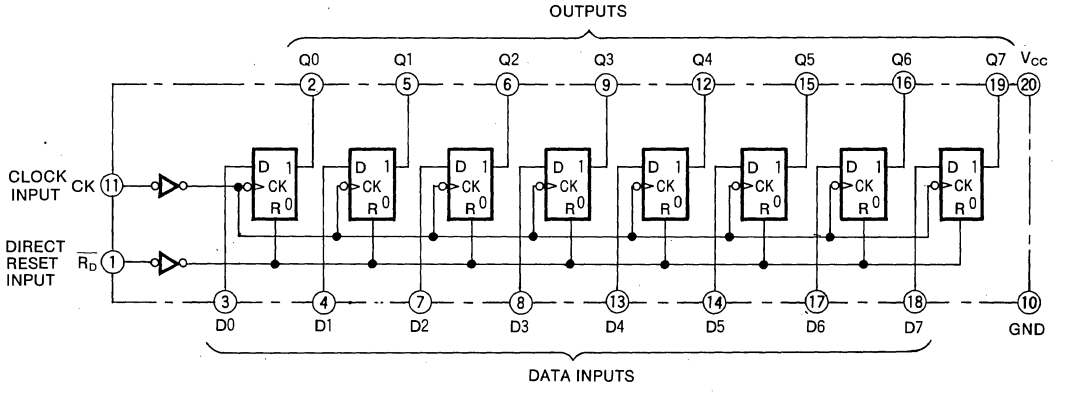
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0
H	↓	X	Q^0

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed.
X : Irrelevant

LOGIC DIAGRAM



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OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−1.5∼V_{CC}+1.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : T_a = −40∼+65℃ and T_a = 65∼85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −4.0mA	4.5	4.18			4.13		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)			30	MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				27	ns
t_{PHL}					27	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

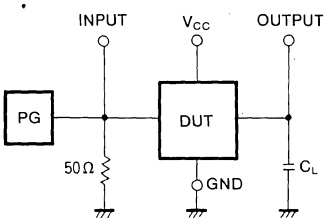
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			160		202	
			4.5			32		40	
			6.0			27		34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

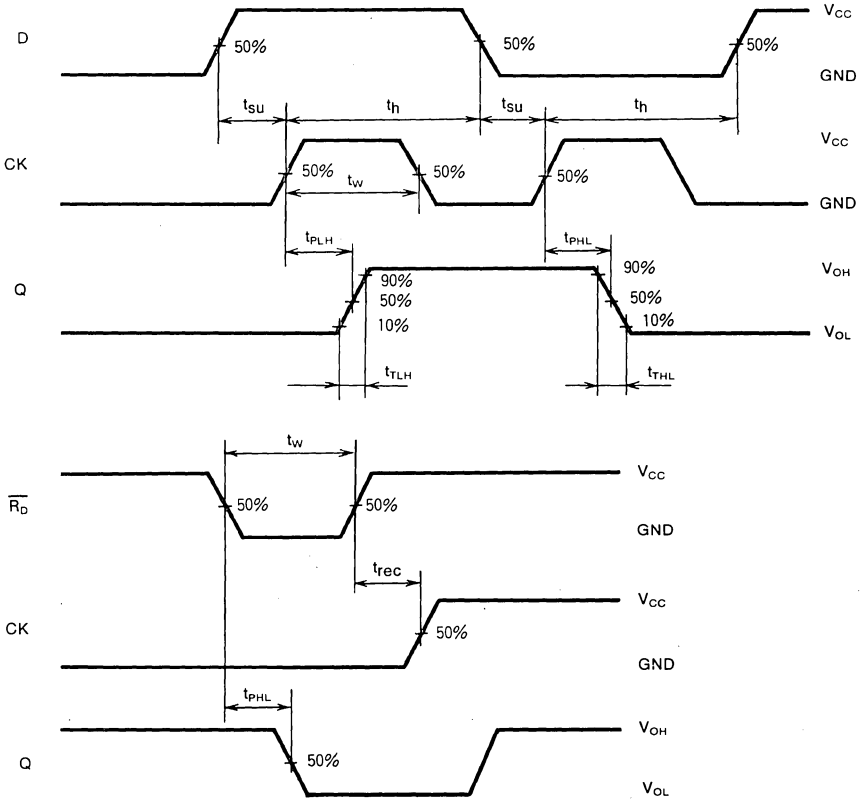
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ pulse width		2.0			80		101	ns
			4.5			16		20	
			6.0			14		17	
t_{su}	D setup time with respect to CK		2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_h	D hold time with respect to CK		2.0			0		0	ns
			4.5			0		0	
			6.0			0		0	
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC4002P

DUAL 4-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC4002P is a semiconductor integrated circuit consisting of two 4-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 20% of V_{CC}, min (V_{CC}=5V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

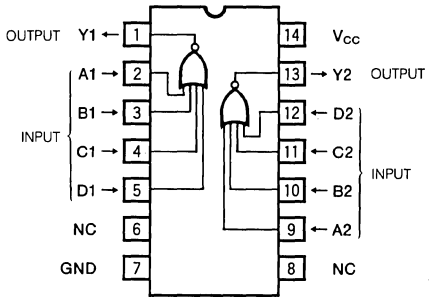
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4002P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTLs.

Buffered Y outputs improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When inputs A, B, C, and D are low, output Y is high, and when at least one of the inputs is high, output Y is low.

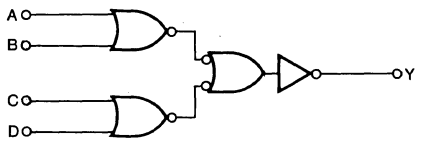
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

N = B + C + D

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−1.5~V_{CC}+1.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : T_a = −40~+65℃ and T_a = 65~85℃ are derated at −12mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

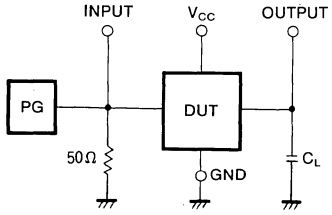
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

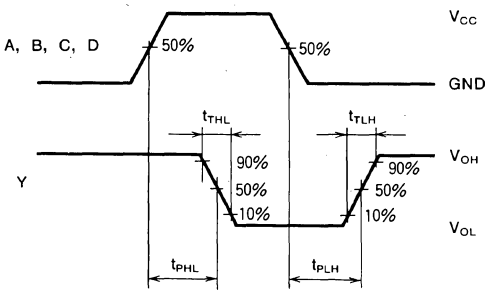
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Cricuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

CONTACT ADDRESSES FOR FURTHER INFORMATION

JAPAN
Electronics Marketing Division
Mitsubishi Electric Corporation
2-3, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Telex: 24532 MELCO J
Telephone: (03) 218-3473
(03) 218-3499
Facsimile: (03) 214-5570

Overseas Marketing Manager
Kita-Itami Works
4-1, Mizuhara, Itami-shi,
Hyogo-ken 664, Japan
Telex: 526408 KMELCO J
Telephone: (0727) 82-5131
Facsimile: (0727) 82-5131 (Day)
(0727) 82-6294 (Night)

HONG KONG
Ryoden Electric Engineering Co., Ltd.
22nd fl., Leighton Centre
77, Leighton Road
Causeway Bay, Hong Kong
Telex: 73411 RYODN HX
Telephone: (5) 7907021
Facsimile: (852) 123-4344

TAIWAN
MELCO Taiwan Co., Ltd.
6th fl., Chung-Ling Bldg.,
363, Sec. 2, Fu-Hsing S. Road
Taipei, R.O.C.
Telephone: (704) 0247
Facsimile: (704) 4244

U.S.A.
Mitsubishi Electronics America, Inc.
1050 East Anques Avenue
Sunnyvale, CA 94086, U.S.A.
Telex: 172296 MELA SUVL
Telephone: (408) 730-5900
Facsimile: (408) 730-4972

Mitsubishi Electronics America, Inc.
200 Unicorn Park Drive
Woburn, MA 01801, U.S.A.
Telex: 951796 MELASB WOBN
Telephone: (617) 938-1220
Facsimile: (617) 938-1075

Mitsubishi Electronics America, Inc.
3247 West Story Road,
Los Colinas Business Park
Irving, TX 75062, U.S.A.
Telephone: (214) 258-1266
Facsimile: (214) 659-9313

Mitsubishi Electronics America, Inc.
799 North Bierman Circle,
Mt. Prospect, ILL 60056, U.S.A.
Telex: 270636 MESA CHI-MPCT
Telephone: (312) 298-9223~8
Facsimile: (312) 298-9223~8

WEST GERMANY
Mitsubishi Electric Europe GmbH
Brandenburger Str. 40
4030 Ratingen 1, West Germany
Telex: 8585070 MED D
Telephone: (02102) 4860
Facsimile: (02102) 486-115

U.K.
Mitsubishi Electric (U.K.) Ltd.
Centre Point, (18th Floor)
103 New Oxford st.,
London WC1, England, U.K.
Telex: 296195 MELCO G
Telephone: (01) 379-7160
Facsimile: (01) 836-0699

AUSTRALIA
Mitsubishi Electric Australia Pty. Ltd.
73-75, Epping Road, North Ride,
N.S.W. 2113 Australia
P.O. Box 1567 Macquarie Centre
N.S.W. 2113
Telex: MESYD AA 26614
Telephone: (02) 888-5777
Facsimile: (02) 887-3635

MITSUBISHI SEMICONDUCTORS
HIGH SPEED CMOS LOGIC

February, First Edition 1985

Editioned by
Committee of editing of Mitsubishi Semiconductor Data Book

Published by
Mitsubishi Electric Corp., Semiconductor Division

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MITSUBISHI SEMICONDCTORS HIGH SPEED CMOS LOGIC 1985

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: MITSUBISHI DENKI BLDG., MARUNOUCHI, TOKYO 100. TELEX: J24532 CABLE: MELCO TOKYO

H-C5741-A KI-8502 Printed in Japan (ROD)

New publication, effective Feb. 1985
Specifications subject to change without notice.