Microchip

PIC®16C71

8-Bit CMOS EPROM Microcontroller with A/D Converter

FEATURES

High Performance RISC-like CPU

- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 14-bit wide instructions
- 8-bit wide data path
- 1024 x 14 on-chip EPROM program memory
- 36 x 8 general purpose registers (SRAM)
- 15 special function hardware registers
- 8 levels deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources: External INT pin, RTCC timer, A/D conversion completion and interrupt on change on four port B pins

Peripheral features

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- 8 bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- A/D converter module:
  - 4 analog inputs multiplexed into one A/D converter
  - Sample and hold
  - 20 µs conversion time/channel
  - 8-bit resolution with ±1 LSB accuracy
  - External reference input, VREF (VREF ≤ VDD)
  - Analog input range: VSS to VREF

Special microcontroller features

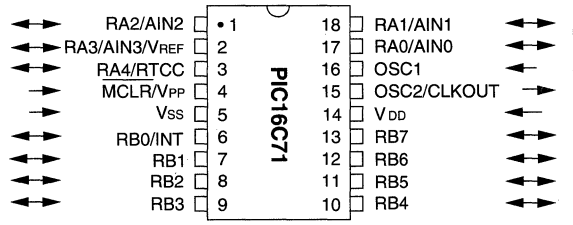
- Power on reset
- Power up timer
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- User selectable oscillator options:
  - RC oscillator: RC
  - Crystal/resonator: XT
  - High speed crystal/resonator: HS
  - Power saving low frequency crystal: LP
- Serial, In-System Programming (ISP) of EPROM program memory using only two pins

CMOS technology

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 3.0V to 6.0V
  - Industrial: 3.0V to 6.0V
  - Automotive: 3.0V to 6.0V
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz (with A/D off)
  - < 1 µA typical standby current @ 3V

FIGURE A - PIN CONFIGURATION

PDIP, SOIC, CERDIP Window



INTRODUCTION

The PIC16C71 is a high performance, low cost, CMOS, fully static EPROM based 8-bit microcontroller with on-chip Analog to Digital converter.
It is the first member of a new and improved family of PIC16CXX microcontrollers (customers familiar with the PIC16C5X products may refer to Appendix A for a list of enhancements).
Its high performance is due to all single word instructions (14-bit wide) that are executed in single cycle (200 ns at 20 MHz clock) except for program-branches which take two cycles (400 ns).
The PIC16C71 has four interrupt sources and an eight level hardware stack.

The peripherals include an 8 bit timer/counter with 8 bit prescaler (effectively a 16 bit timer), 13 bi-directional I/O pins and an 8 bit A/D converter. The high current drive (25 mA max. sink, 20 mA max source) of the I/O pins help reduce external drivers and therefore, system cost.

The A/D converter has four channels, sample and hold, 8 bit resolution with ±1 LSB accuracy. Conversion time is typically 30 µs including sampling time.

The PIC16C71 product is supported by an assembler, an in-circuit emulator and a production quality programmer. All the tools are supported on IBM PC and compatible machines.

FIGURE B: PIC16C71 BLOCK DIAGRAM

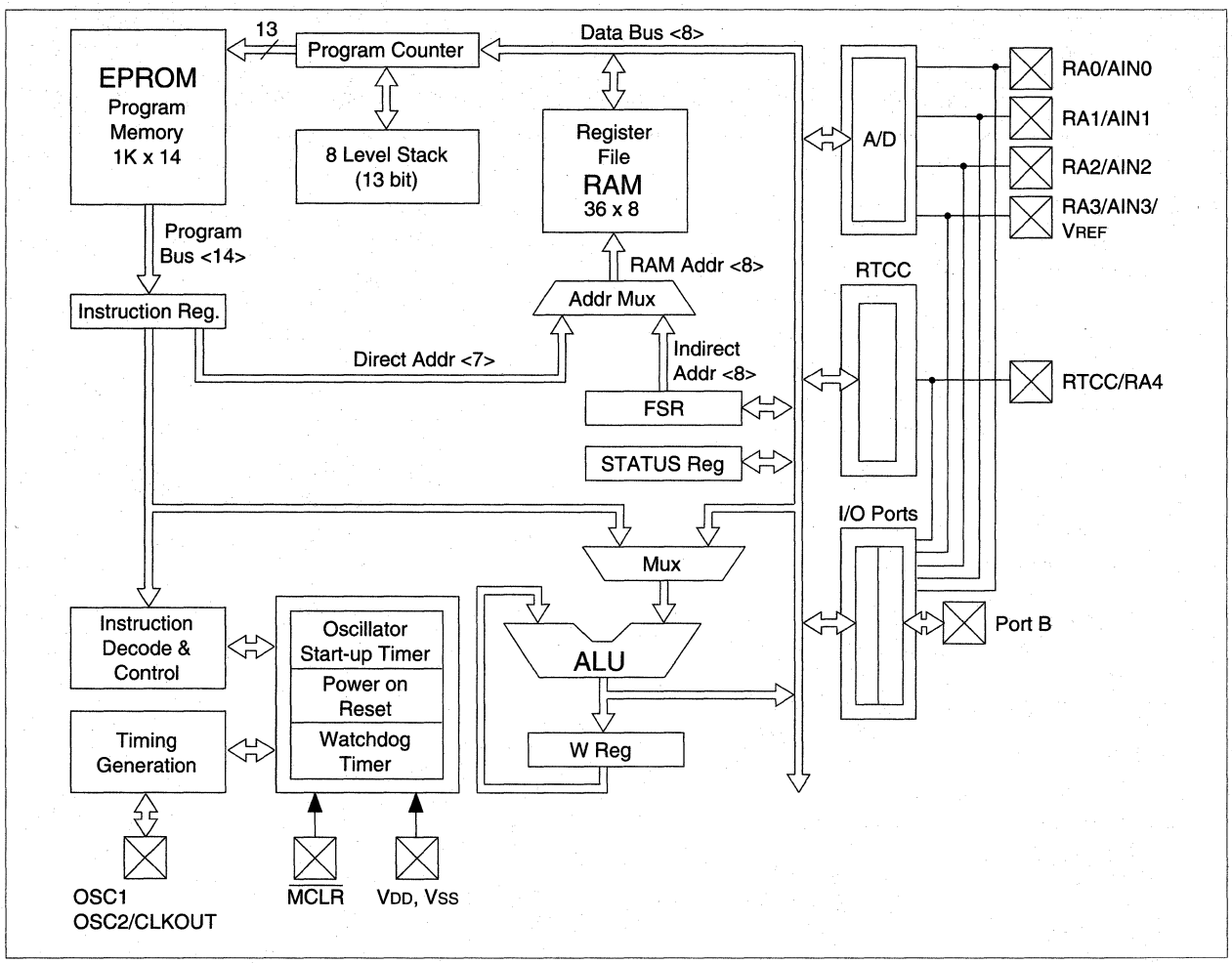


Table of Contents

Table of Figures

Table of Tables

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1.0 GENERAL DESCRIPTION

The PIC16C71 is a low cost, high performance, CMOS, fully static, EPROM-based 8-bit microcontroller with on-chip analog to digital converter. It employs an advanced RISC-like architecture. A reduced set of 35 instructions, all single word instructions (14-bit wide), all single cycle instructions (200ns) except for 2-cycle program branches, instruction pipe-lining, large register set and separate instruction and data memory (Harvard architecture) schemes are some of the architectural innovation used to achieve very high performance. The PIC16C71 typically achieves a 2:1 code compression and a 5:1 speed improvement over other 8 bit microcontrollers in its class.

The PIC16C71 is equipped with special features to reduce external components and thus reduce cost, enhance system reliability and reduce power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution and the LP oscillator minimizes power consumption. The SLEEP (power down) mode offers power saving. The user can wake up the chip from SLEEP through external interrupts and reset.

A highly reliable watchdog timer with its own on-chip RC oscillator provides protection against software malfunction.

The UV-erasable cerdip-packaged versions are ideal for code development while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontroller while benefiting from the OTP flexibility.

1.1 UPWARD COMPATIBILITY WITH PIC16C5X

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an improved version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to PIC16C71 (see Appendix B).

1.2 APPLICATIONS

The PIC16C71 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, pointing devices, and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use, and I/O flexibility makes the PIC16C71 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

2.0 PIC16C71 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C71 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in cerdip package is optimal for prototype development and pilot series.

The UV erasable version can be erased and reprogrammed to any of the oscillator modes etc. Microchip's PRO MASTER™ programmer supports programming of the PIC16C71.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the oscillator fuses, configuration fuses and optionally, the ID locations must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C71 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C71 uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC16C71, op-codes are 14-bit wide making it possible to have all single word instructions. A 14 bit wide program memory access bus fetches a 14 bit instruction in a single cycle. A two-stage pipeline

overlaps fetch and execution of instructions. Consequently, all instructions (35 in all) execute in a single cycle (200ns @ 20 MHz) except for program branches.

The PIC16C71 address 1K x 14 program memory space, all on-chip. Program execution is internal only (microcontroller mode).

The PIC16C71 can directly or indirectly address its 48 register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C71 has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C71 simple yet efficient. In addition, the learning curve is reduced significantly.

3.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3.2.1.

3.3 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" in PIC16C71 consists of Q1, Q2, Q3 and Q4. Instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction.

A fetch cycle begins with the program counter (PC) incrementing in Q1.

3.1 - PIC16C71 PINOUT DESCRIPTION

Pin name	Pin Type	Pin function	
		Normal operation	Serial In-System Programming (ISP) Mode
VDD	P	Power	Power
VSS	P	Ground	Ground
OSC1	I	Clock input/oscillator connection	-
OSC2/CLKOUT	I/O	Oscillator connection/CLKOUT output. It is CLKOUT in RC oscillator mode and oscillator connection in all other modes.	-
$\overline{MCLR}$/VPP	I/P	Master clear (external reset) input. Active low. It has Schmitt trigger input buffer.	Master clear/programming voltage (VPP) supply
RA4/RTCC	I/O	Open-drain output/input pin. It is also the clock input to RTCC timer/counter: Schmitt trigger input buffer	-
RA0/AIN0	I/O	Bidirectional I/O pin/Analog input channel 0. As digital input it has TTL input levels	-
RA1/AIN1	I/O	Bidirectional I/O pin/Analog input channel 1. As digital input it has TTL input levels	-
RA2/AIN2	I/O	Bidirectional I/O pin/Analog input channel 2. As digital input it has TTL input levels	-
RA3/AIN3/VREF	I/O	Bidirectional I/O pin/Analog input channel 3/Analog reference voltage input . As digital input it has TTL input levels	-
RB0/INT	I/O	Bidirectional I/O pin/External interrupt input. TTL input levels	-
RB1	I/O	Bidirectional I/O pin. TTL input levels	-
RB2	I/O	Bidirectional I/O pin. TTL input levels	-
RB3	I/O	Bidirectional I/O pin. TTL input levels	-
RB4	I/O	Bidirectional I/O pin. TTL input levels	-
RB5	I/O	Bidirectional I/O pin. TTL input levels	-
RB6	I/O	Bidirectional I/O pin. TTL input levels	Clock input
RB7	I/O	Bidirectional I/O pin. TTL input levels	Data input/output

Legend: I = input, O = output, I/O = input/output, P = power. -: Not used.

FIGURE 3.2.1 - CLOCK/INSTRUCTION CYCLE

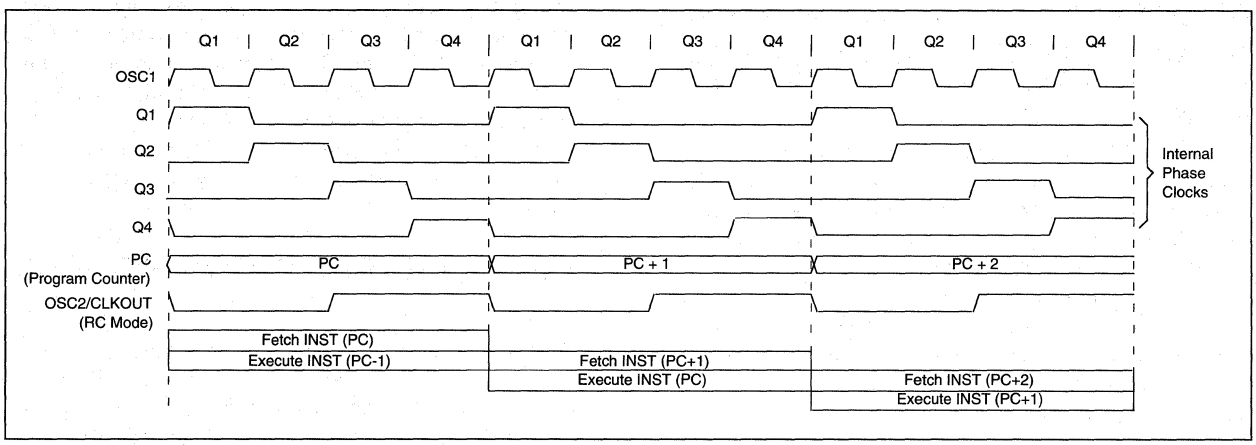


FIGURE 3.4.1 - PROGRAM MEMORY MAP AND STACK

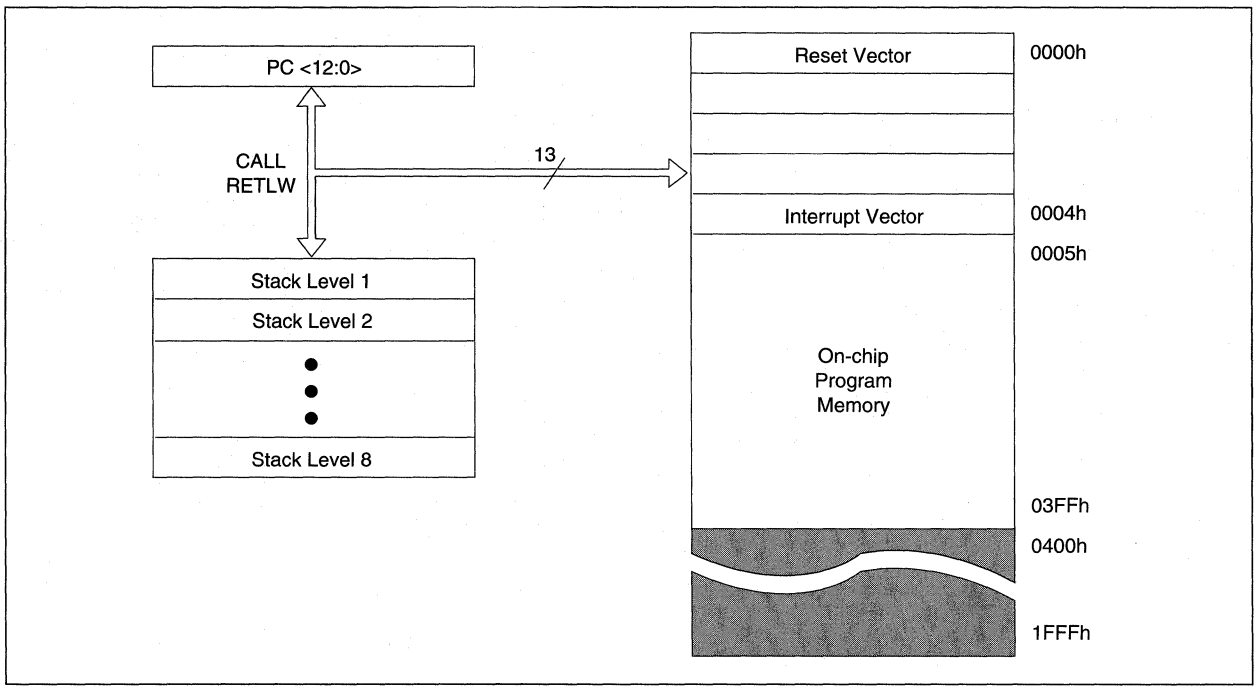
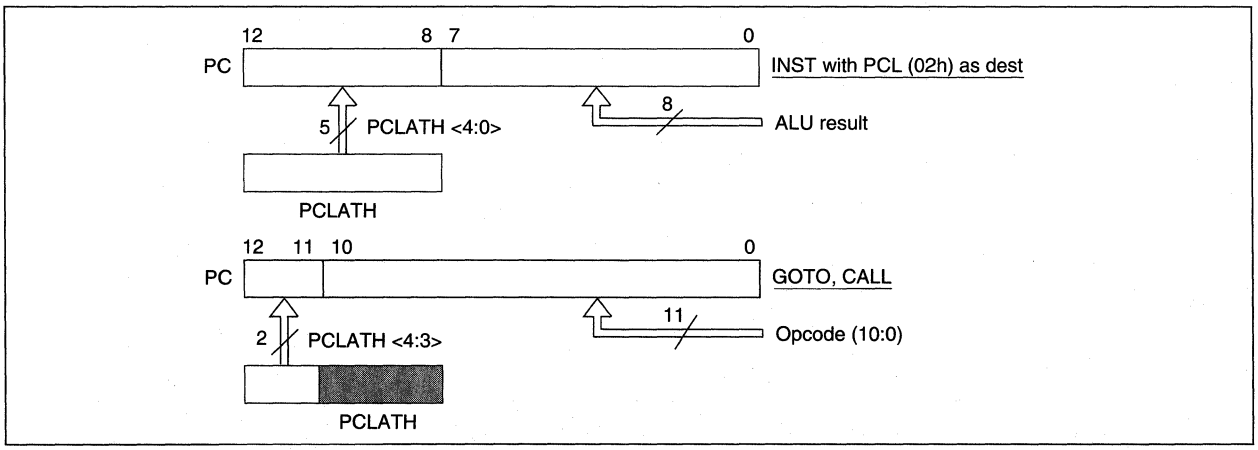


FIGURE 3.5.1 - LOADING OF PC IN DIFFERENT SITUATIONS



The fetched instruction is latched into the "Instruction Register (IR)" which is decoded and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

3.4 Program Memory Organization

The PIC16C71 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. In PIC16C71 only the first 1K x 14 (0000h - 03FFh) are physically implemented. Accessing a location above 3FFh will cause a wrap-around within the first 1K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h.

3.5 Program Counter Module

The program counter (PC) is 13-bit wide. The low byte, PCL is a readable and writable register (02h). The high byte of the PC, PCH is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (0Ah). When the PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in figure 3.5.1.

3.6 Stack

The PIC16C71 has an 8 deep x 13 bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is pushed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is popped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH (0Ah) is not affected by a PUSH or a POP operation.

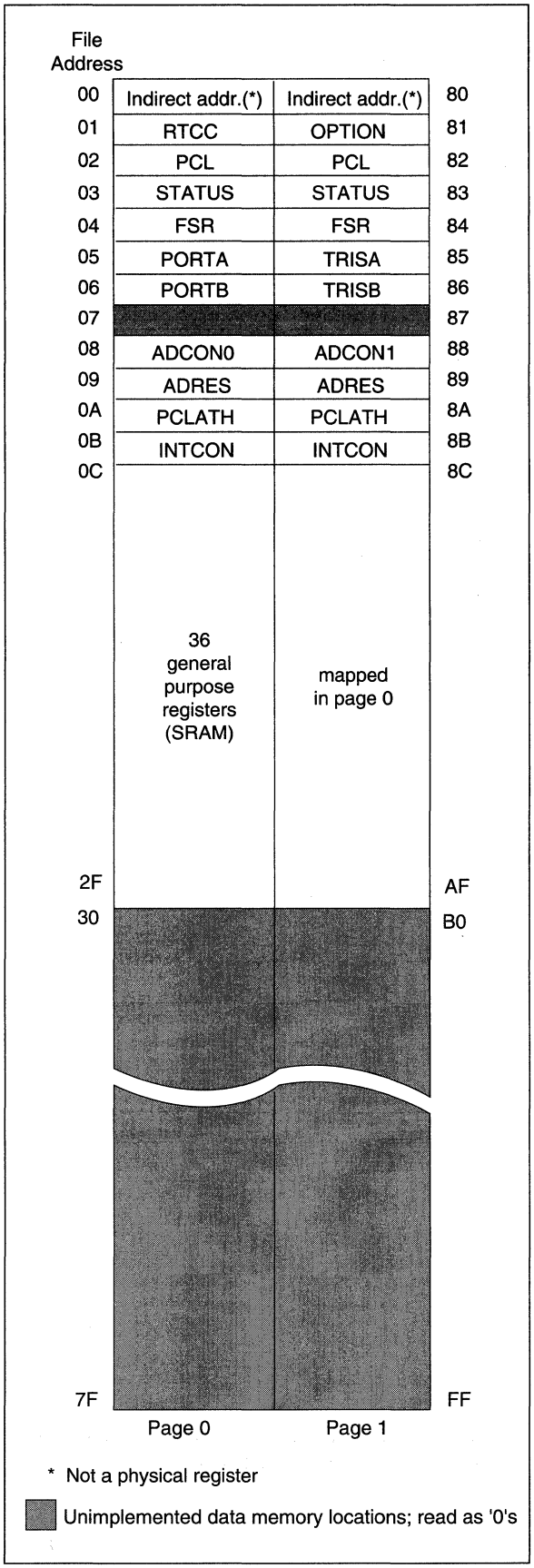
3.7 Register File Organization

The register file, in PIC16C71 is organized as 128 x 8. It is accessed either directly or indirectly through file select register FSR. It is also referred to as the data memory. There are several register file page select bits in the STATUS register allowing up to four pages. However, in the PIC16C71 data memory extends only up to 2Fh. The first 12 locations are used to map special function registers. Locations 0Ch - 2Fh are general purpose registers implemented as static RAM. Some special function registers are mapped in page 1. When in page 1, accessing locations 8Ch - AFh will access the RAM in page 0 (Figure 3.7.1).

3.8 Indirect Addressing Register

Indirect addressing is possible by using file address 00h. Any instruction using f0 as file register actually accesses data pointed to by the file select register, FSR (address 04h). Reading f0 itself indirectly will produce 00h. Writing to f0 indirectly results in a no-operation (although status bits may be affected).

FIGURE 3.7.1 - DATA MEMORY MAP



3.9 STATUS Register (f03)

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for data memory.

The status register (f03) can be destination for any instruction like any other register. However, the status bits are set following the write. Furthermore, TO and PD bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF f3 will clear all bits except for TO and PD and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see section "Instruction Set Summary" (Section 4.0)

3.9.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS

The carry bit (C) is a carry out in addition operations (ADDWF, ADDLW) and a borrow out in subtract operations (SUBWF, SUBLW). The following examples explain operation of carry/borrow bit:

```
;SUBLW Example #1
;
MOVLW   0x01    ;wreg=1
SUBLW   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
MOVLW   0x02    ;wreg=2
SUBLW   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
;
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF    ;
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e.: it is a borrow in subtract operations.

3.9.2 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The "TO" and "PD" bits in the status register f03 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or MCLR pin.
These status bits are only affected by events listed in Table 3.9.1.1.

TABLE 3.9.2.1 - EVENTS AFFECTING PD/ TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Timeout	0	U	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

U: unchanged

Note: A WDT timeout will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 3.9.2.2 reflects the status of PD and TO after the corresponding event.

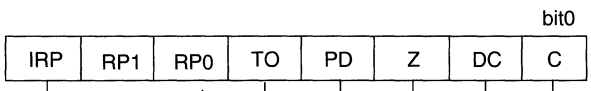
TABLE 3.9.2.2 - PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	MCLR wake-up from SLEEP
1	1	Power-up
U	U	MCLR reset during normal operation

U: unchanged

Note: The PD and TO bit maintain their status until an event of Table 3.9.2.1 occurs. A low-pulse on the MCLR input does not change the PD and TO status bits.

FIGURE 3.9.1 - STATUS REGISTER



ADDRESS:	03h
RESET CONDITION:	000??XXX
TO, PD are set or reset as shown in Table 3.9.2.1	

CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero. Reset otherwise.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is reset to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is reset to "0" by a watchdog timer time out.

REGISTER PAGE SELECT BITS FOR DIRECT ADDRESSING:

RP1,0: 00 : page 0 (00h - 7Fh)
01 : page 1 (80h - FFh)
10 : page 2 (100h - 17Fh)
11 : page 3 (180h - 1FFh)

Each page is 128 bytes.
Only RP0 is useful in PIC16C71. Bit RP1 can be used as a general purpose read/write bit. However, this may affect upward compatibility with future products.

REGISTER PAGE SELECT BITS FOR INDIRECT ADDRESSING:

IRP: 0 : page 0,1 (00h - FFh)
1 : page 2,3 (100h - 1FFh)

This bit is effectively not used in the PIC16C71.
It may be used as a general purpose read/write bit. However, this may affect upward compatibility with future product.

3.10 Arithmetic and Logic Unit (ALU)

The ALU is 8 bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. In two-operand instructions, typically one operand is the working register (W register) or the accumulator. The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

3.11 W Register

The W register is an 8-bit working register (or accumulator) used for ALU operations. It is not an addressable register.

3.12 INTERRUPTS

The PIC16C71 has four sources of interrupt: external interrupt from RB0/INT pin, RTCC timer/counter overflow interrupt, end of conversion interrupt from A/D module, and interrupt on change on RB<7:4> pins. The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global mask bits. The only exception is A/D conversion completion interrupt flag (ADIF) which resides in ADCON register.

A global interrupt enable bit, GIE (bit 7, INTCON) enables (if = 1) all un-masked interrupts or disables (if = 0) all interrupts. Individual interrupts can be disabled through their corresponding mask bit in INTCON register. GIE is cleared on reset.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-

FIGURE 3.12.1 - INTERRUPT LOGIC

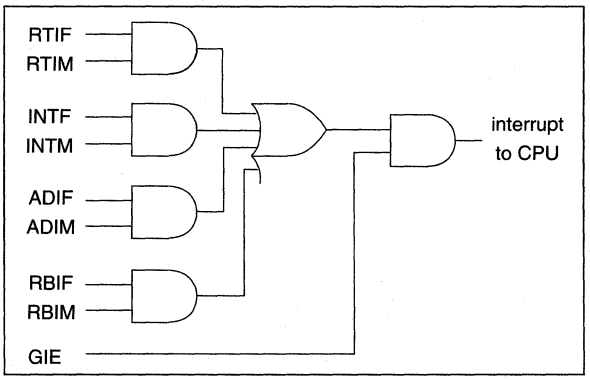
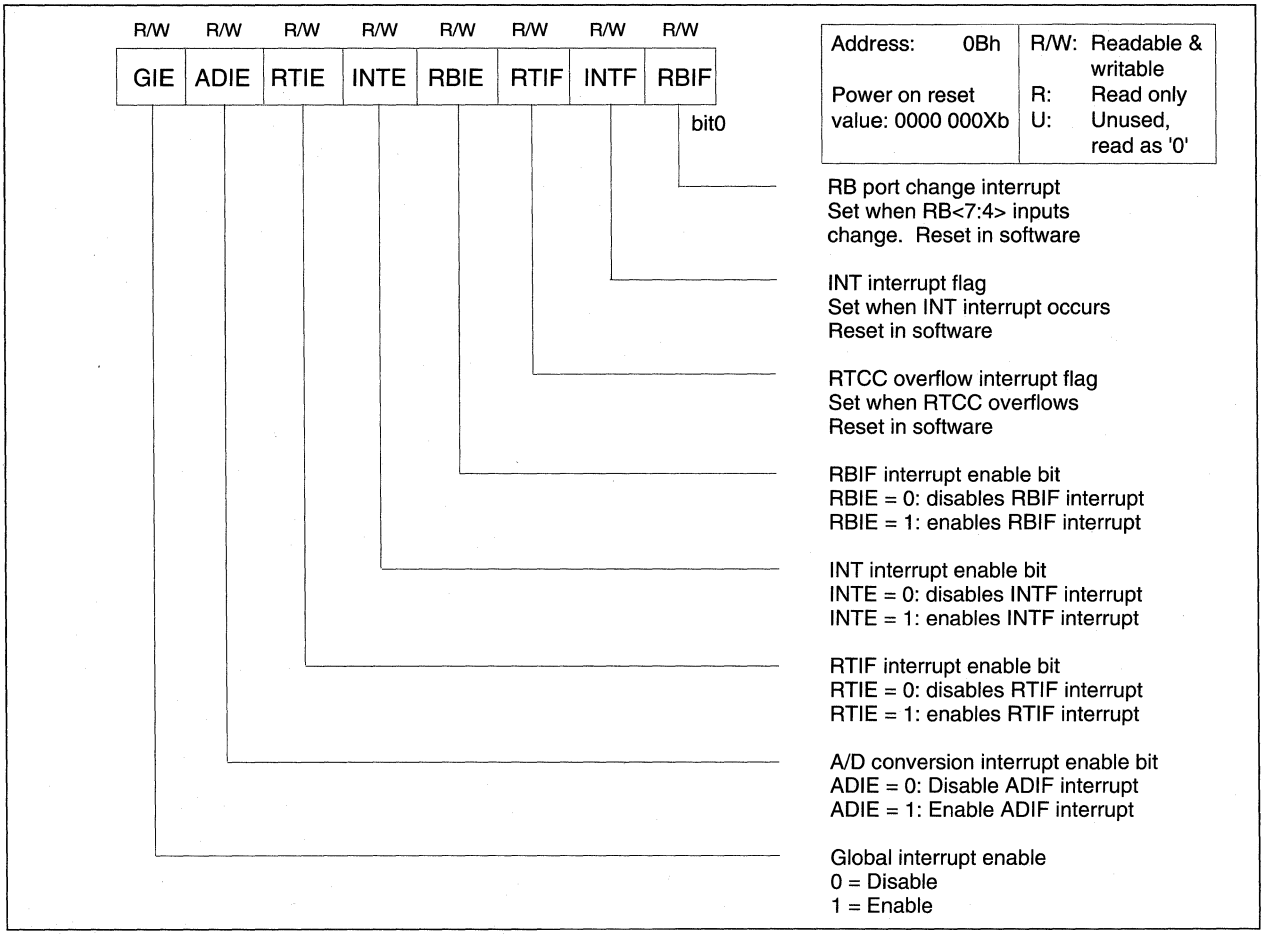


FIGURE 3.12.2 - INTCON REGISTER



enabling interrupts to avoid recursive interrupts. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit to re-enable interrupts.

3.12.1 INT Interrupt

External interrupt on RB0/INT pin is edge triggered: either rising (if INTEDG = 1, bit6 of OPTION register) or falling (if INTEDG = 0). When a valid edge appears on INT pin, INTF bit is set (bit1, INTCON register). This interrupt can be disabled by setting INTE control bit (bit4, INTCON) to '0'. INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP if INTE bit was set to '1' prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See section 5.5 for details on SLEEP.

3.12.2 RTCC Interrupt

RTCC interrupt is generated when the RTCC timer/counter overflows from FFh to 00h. It sets the RTIF bit (bit2, INTCON). The interrupt can be masked by setting RTIE bit (bit5, INTCON) to '0'. RTIF bit must be cleared in software in the RTCC interrupt service routine before re-enabling this interrupt. The RTCC interrupt can not wake the processor from SLEEP since the timer is shut off during SLEEP.

3.12.3 Port RB Interrupt

Port B has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in bit0, INTCON). Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIM (bit3, INTCON) bit.

b) Read Port B. This will end mismatch condition. Next, clear RBIF bit.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

3.13 A/D INTERRUPT

The A/D converter sets the end of conversion interrupt flag, ADIF (bit1, ADCON) when a conversion is complete. The interrupt can be masked by setting ADIE bit (bit6, INTCON) to '0'. See section 6.6 for details on A/D interrupt.

4.0 INSTRUCTION SET SUMMARY

Each PIC instruction is a 14-bit word divided into an OP CODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC instruction set summary in Table 4.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.
For literal and control operations, "k" represents an eight or eleven bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 4.1

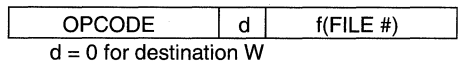
Note 1: The PIC16C71 has 35 instructions. Two additional instructions, TRIS and OPTION, are included only for compatibility with the PIC16C5X products. Their use in new code is strongly recommended against since TRIS and OPTION are made addressible registers, the user may simply write to them. These instructions may not be supported in future PIC16CXX products.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

Note 3: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

4.1 INSTRUCTION SET

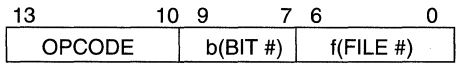
BYTE-ORIENTED FILE REGISTER OPERATIONS



d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status affected	Notes
00 0111 dfff ffff	07ff	Add W and f	**ADDWF**	**f, d**	W + f → d	C, DC, Z	2,3
00 0101 dfff ffff	05ff	AND W and f	**ANDWF**	**f, d**	W & f → d	Z	2,3
00 0001 1fff ffff	018f	Clear f	**CLRF**	**f**	0 → f	Z	3
00 0001 0XXX XXXX	0100	Clear W	**CLRW**	**-**	0 → W	Z	
00 1001 dfff ffff	09ff	Complement f	**COMF**	**f, d**	$\bar{f}$ → d	Z	2,3
00 0011 dfff ffff	03ff	Decrement f	**DECF**	**f, d**	f -1 → d	Z	2,3
00 1011 dfff ffff	0Bff	Decrement f,Skip if Zero	**DECFSZ**	**f, d**	f - 1 → d, skip if zero	None	2,3
00 1010 dfff ffff	0Aff	Increment f	**INCF**	**f, d**	f + 1 → d	Z	2,3
00 1111 dfff ffff	0Fff	Increment f,Skip if zero	**INCFSZ**	**f, d**	f + 1 → d, skip if zero	None	2,3
00 0100 dfff ffff	04ff	Inclusive OR W and f	**IORWF**	**f, d**	W v f → d	Z	2,3
00 1000 dfff ffff	08ff	Move f	**MOVF**	**f, d**	f → d	Z	2,3
00 0000 1fff ffff	008f	Move W to f	**MOVWF**	**f**	W → f	None	3
00 0000 0XX0 0000	0000	No Operation	**NOP**	**-**	-	None	
00 1101 dfff ffff	0Dff	Rotate left f	**RLF**	**f, d**	f(n)→d(n+1), C →d(0), f(7) →C	C	2,3
00 1100 dfff ffff	0Cff	Rotate right f	**RRF**	**f, d**	f(n)→d(n-1), C→d(7), f(0)→C	C	2,3
00 0010 dfff ffff	02ff	Subtract W from f	**SUBWF**	**f, d**	f - W → d [f + $\overline{W}$ + 1 → d]	C, DC, Z	2,3
00 1110 dfff ffff	0Eff	Swap halves f	**SWAPF**	**f, d**	f(0-3) ↔ f(4-7) → d	None	2,3
00 0110 dfff ffff	06ff	Exclusive OR W and f	**XORWF**	**f, d**	W ⊕ f → d	Z	2,3

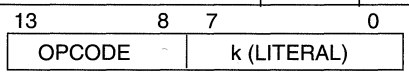
BIT-ORIENTED FILE REGISTER OPERATIONS



b = 3-bit bit address
f = 7-bit file register address

01 00bb bfff ffff	1bff	Bit Clear f	**BCF**	**f, b**	0 → f(b)	None	2,3
01 01bb bfff ffff	1bff	Bit Set f	**BSF**	**f, b**	1 → f(b)	None	2,3
01 10bb bfff ffff	1bff	Bit Test f,Skip if Clear	**BTFSC**	**f, b**	Test bit (b) in file (f): Skip if clear	None	
01 11bb bfff ffff	1bff	Bit Test f, Skip if Set	**BTFSS**	**f, b**	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS



k = 8-bit immediate value.

11 111X kkkk kkkk	3Ekk	Add literal to W	**ADDLW**	**k**	k + W → W	C,DC,Z	
11 1001 kkkk kkkk	39kk	AND Literal and W	**ANDLW**	**k**	k & W→ W	Z	
10 0kkk kkkk kkkk	2kkk	Call subroutine	**CALL**	**k**	PC + 1 → TOS, k → PC <10:0>, PCLATH <4:3> → PC <12:11>;	None	
00 0000 0110 0100	0064	Clear Watchdog timer	**CLRWDT**	**-**	0→WDT(and prescaler,if assigned)	TO, PD	
10 1kkk kkkk kkkk	2kkk	Go To address	**GOTO**	**k**	k → PC <10:0>, PCLATH <4:3> → PC <12:11>;	None	
11 1000 kkkk kkkk	38kk	Incl. OR Literal and W	**IORLW**	**k**	k v W → W	Z	
11 00XX kkkk kkkk	30kk	Move Literal to W	**MOVLW**	**k**	k → W	None	
00 0000 0000 1001	0009	Return from interrupt	**RETFIE**	**-**	TOS → PC, '1' → GIE	None	
11 01XX kkkk kkkk	34kk	Return, place literal in W	**RETLW**	**k**	k → W, TOS→ PC	None	
00 0000 0000 1000	0008	Return from subroutine	**RETURN**	**-**	TOS → PC	None	
00 0000 0110 0011	0063	Go into standby mode	**SLEEP**	**-**	0 → WDT, stop oscillator	TO, PD	
11 110X kkkk kkkk	3Ckk	Subtract W from literal	**SUBLW**	**k**	k - W → W	C,DC,Z	
11 1010 kkkk kkkk	3Akk	Excl. OR Literal and W	**XORLW**	**k**	k ⊕ W → W	Z	

00 0000 0110 0010	0062	Load OPTION register	**OPTION**	**-**	W → OPTION register	None	1
00 0000 0110 0fff	006f	Tristate port f	**TRIS**	**f**	W→ I/O control register f	None	1

X = 0 or 1. The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
Notes: See previous page

4.2 INSTRUCTION DESCRIPTION

ADDLW Add Literal to W

Syntax: ADDLW k

Encoding:	11	111X	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W + k) → W

Status bits: C, DC, Z

Description: The contents of the W register are added to the eight bit literal "k" and the result is placed in the W register.

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	00	0111	dfff	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: C, DC, Z

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

ANDLW AND Literal and W

Syntax: ANDLW k

Encoding:	11	1001	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	00	0101	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	01	00bb	bfff	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in register "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	01	01bb	bfff	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in register "f" is set to 1.

BTFSC Bit Test, skip if Clear

Syntax: BTFSC f,b

Encoding:	01	10bb	bfff	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in register "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTFSS Bit Test, skip if Set

Syntax: BTFSS f,b

Encoding:	01	11bb	bfff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit '"b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

CALL Subroutine Call

Syntax: CALL k

Encoding:	10	0kkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS, k → PC<10:0>, PCLATH<4:3> → PC<12:11>;

Status bits: None

Description: Subroutine call. First, return address (PC + 1) is pushed into the stack. The eleven bit value is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two cycle instruction.

CLRF Clear f

Syntax: CLRF f

Encoding:	00	0001	1fff	ffff

Words: 1

Cycles: 1

Operation: 00h → f

Status bits: Z

Description: The contents of register "f" are set to 0.

CLRW Clear W Register

Syntax: CLRW

Encoding:	00	0001	0XXX	XXXX

Words: 1

Cycles: 1

Operation: 00h →W

Status bits: Z

Description: W registered is cleared. Zero bit (Z) is set.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	00	0000	0110	0100

Words: 1

Cycles: 1

Operation: 00h →WDT, 0 → WDT prescaler,

Status bits: 1 → TO, 1 → PD

Description: CLRWDT instruction resets the watchdog timer.It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	00	1001	dfff	ffff

Words: 1

Cycles: 1

Operation: $\bar{f}$ → d

Status bits: Z

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

DECF Decrement f

Syntax: DECF f,d

Encoding:	00	0011	dfff	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: C, DC, Z

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:	00	1011	dfff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:	10	1kkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<10:0>, PCLATH<4:3> → PC<12:11>

Status bits: None

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:	00	1010	dfff	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: C, DC, Z

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:	00	1111	dfff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f + 1) → d, skip if result = 0

Status bits: None

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: IORLW k

Encoding:	11	1000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:	00	0100	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:	11	00XX	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVF Move f

Syntax: MOVF f,d

Encoding:	00	1000	dfff	ffff

Words: 1

Cycles: 1

Operation: f → d

Status bits: Z

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. It is useful, however, to test a file register since status flag Z is affected.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:	00	0000	1fff	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to register "f".

NOP No Operation

Syntax: NOP

Encoding:	00	0000	0XX0	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

OPTION Load Option Register

Syntax: OPTION

Encoding:	00	0000	0110	0010

Words: 1

Cycles: 1

Operation: W → OPTION;

Status bits: None

Description: The contents of the W register is loaded in the OPTION register. Refer to Fig. 6.5.1 for OPTION register settings.

This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it. To maintain upward compatibility with future PIC16CXX products, **do not use this instruction.**

RETFIE Return from Interrupt

Syntax: RETFIE

Encoding:	00	0000	0000	1001

Words: 1

Cycles: 2

Operation: TOS → PC, 1 → GIE;

Status bits: GLINTD

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (bit 7, register INTCON). This is a two cycle instruction.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	11	01XX	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN Return from Subroutine

Syntax: RETURN

Encoding:	00	0000	0000	1000

Words: 1

Cycles: 2

Operation: TOS → PC;

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

RLF Rotate Left f through Carry

Syntax: RLF f,d

Encoding:	00	1101	dfff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".

RRF Rotate Right f through Carry

Syntax: RRF f,d

Encoding:	00	1100	dfff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>, f<0> → C, C → d<7>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

SLEEP

Syntax: SLEEP

Encoding:	00	0000	0110	0011

Words: 1

Cycles: 1

Operation: 0 → PD, 1 → TO;
00h → WDT, 0 → WDT prescaler;

Status bits: TO, PD

Description: The power down status bit (PD) is cleared. Time-out status bit (TO) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBLW Subtract W from Literal

Syntax: SUBLW k

Encoding:	11	110X	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (k - W) → W

Status bits: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight bit literal "k". The result is placed in the W register.

```
Example
;SUBLW Example #1
;
MOVLW   0x01    ;wreg=1
SUBLW   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
MOVLW   0x02    ;wreg=2
SUBLW   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
```

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:	00	0010	dfff	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: C, DC, Z

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

```
Example:
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
```

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	00	1110	dfff	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>;

Status bits: None

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

TRIS Load TRIS Register

Syntax: TRIS f

Encoding:	00	0000	0110	0fff

Words: 1

Cycles: 1

Operation: W → I/O Control Register f

Status bits: None

Description: The I/O Control Register (or data direction register of the I/O port) is loaded with the contents of the W register.

The TRIS instruction configures an I/O port to either output or input (high-impedance). The valid values for "f" are 5 & 6 for PIC16C71.

This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them. To maintain upward compatibility with future PIC16CXX products, **do not use this instruction**.

A '1' in the TRIS register configures the corresponding port pin as an input. A '0' in the TRIS register configures the corresponding port pin as an output.

```
Example:
MOVLW   0x0F
TRIS    6
```

I/O Port B (F6) is configured such that the 4 pins corresponding to the LSBs of Port B are inputs (h-impedance) and the other 4 pins are outputs.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:	11	1010	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:	00	0110	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

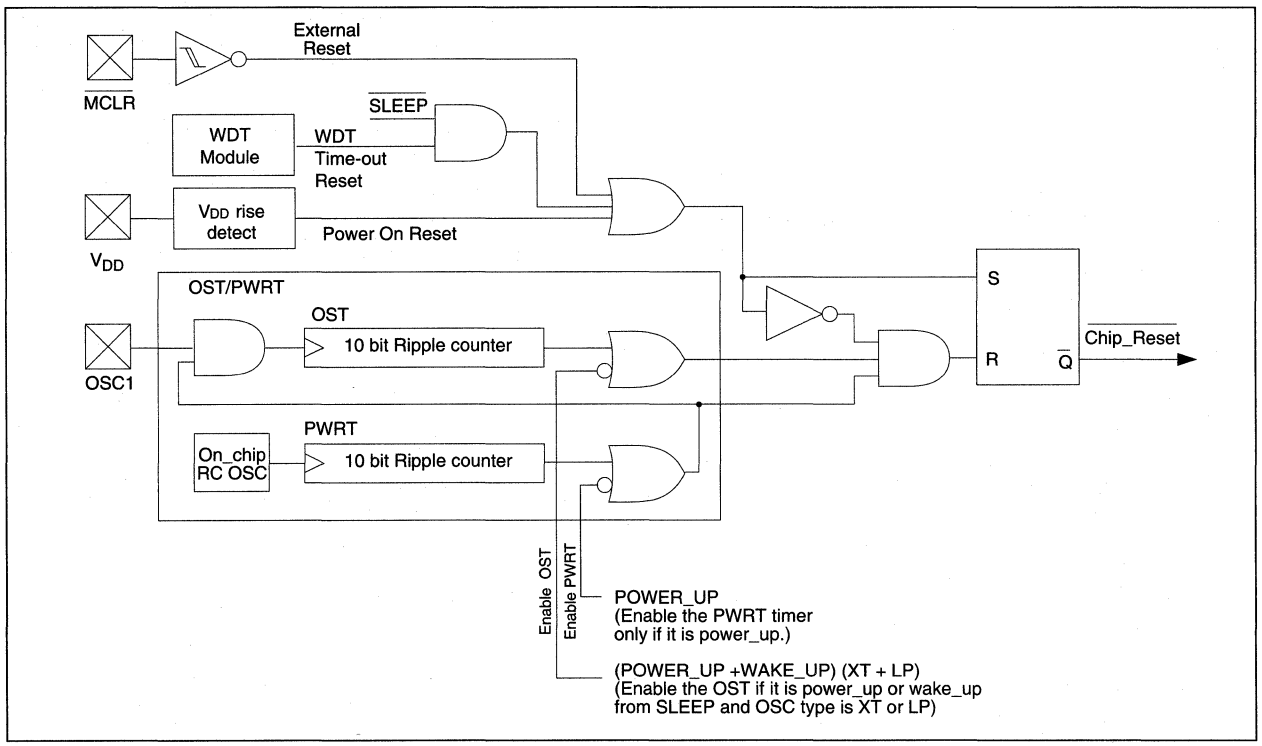
5.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16C71 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

The PIC16C71 has a watchdog timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the oscillator start-up timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the power-up timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, watchdog timer time-out or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EPROM configuration bits (fuses) are used to select various options (section 5.6).

FIGURE 5.0.1 - SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.1 RESET

The PIC16C71 differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{\text{MCLR}}$ Reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

Some registers are not reset in any way; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), on $\overline{\text{MCLR}}$ or WDT reset during normal operation and on $\overline{\text{MCLR}}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as resume of normal operation. There are a few exceptions to this. The PC is always reset to all 0's (0000h). Finally, TO and PD bits are set or cleared differently in different reset situations as indicated in section 3.8.1. These bits are used in software to determine the nature of reset. See Table 5.1.1 for a full description of reset states of all registers.

5.2 Power-on-reset (POR), Power-up-timer (PWRT) and Oscillator Start-up timer (OST)

Power-on-reset (POR): A power-on-reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 2.0V). To take advantage of the POR, just tie MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create power-on-reset.

TABLE 5.1.1 RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on reset (POR)	WDT time-out reset during normal operation	WDT time-out reset during SLEEP	$\overline{MCLR}$ reset during normal	$\overline{MCLR}$ reset during SLEEP	Wake-up through interrupt
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
INDIR	00h	-	-	-	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1	0000h	0000h	PC + 1
STATUS	03h	0001 1xxx	0000 1uuu	uuu0 0uuu	000u uuuu	000u 0uuu	uuu1 0uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TRIS A	85h	---1 1111	---1 1111	---u uuuu	---1 1111	---1 1111	---u uuuu
TRIS B	86h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
ADCON0	08h	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu
ADCON1	88h	---- --00	---- --00	---- --uu	---- --00	---- --00	---- --uu
ADRES	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu	0000 000u	0000 0000	uuuu uuuu*

Legend: - = unimplemented, reads as '0'
u = unchanged
x = unknown

* In the event of wake-up through interrupt, one or more of the interrupt flags will be set. Other bits in INTCON will remain unchanged.

The POR circuit does not produce internal reset when VDD declines (or goes through a brown-out).

Power-up Timer (PWRT): The power-up timer provides a fixed 72ms time-out on power-up only, from POR. The power-up timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if = 1) or disable (if = 0 or programmed) the power-up timer (section 5.6).

The power-up time delay will vary from chip to chip and due to VDD and temperature. See DC parameters for details.

Oscillator Start-up Timer (OST): The oscillator start-up timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on power-on reset or wake-up from SLEEP.

Time-out Sequence: On power up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then TOST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE set to '0' (PWRT disabled), there will be no time-out at all. Figures 5.2.1 and 5.2.2 depict time-out sequences.

Since the time-outs occur from POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC operating in conjunction.

TABLE 5.2.1 - TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	-	-

FIGURE 5.2.1 TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 1

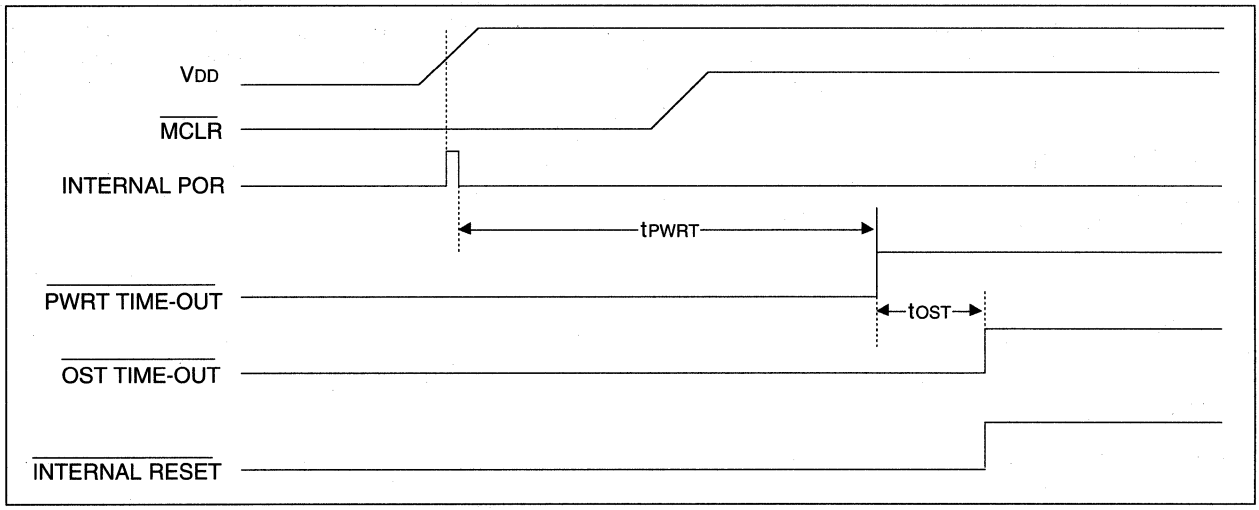


FIGURE 5.2.2 TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 2

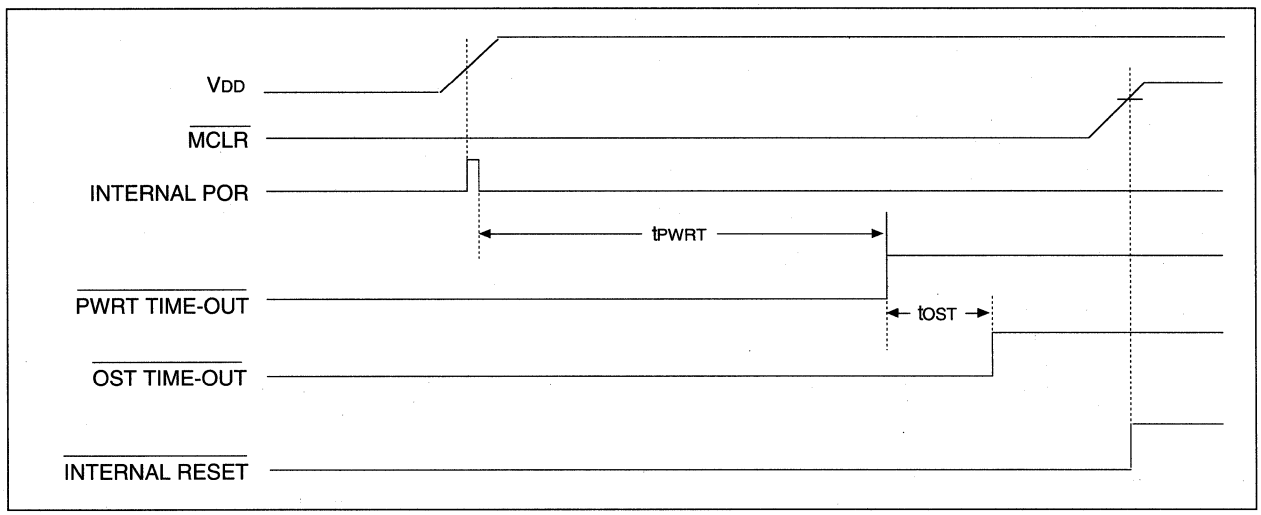


FIGURE 5.2.3 TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

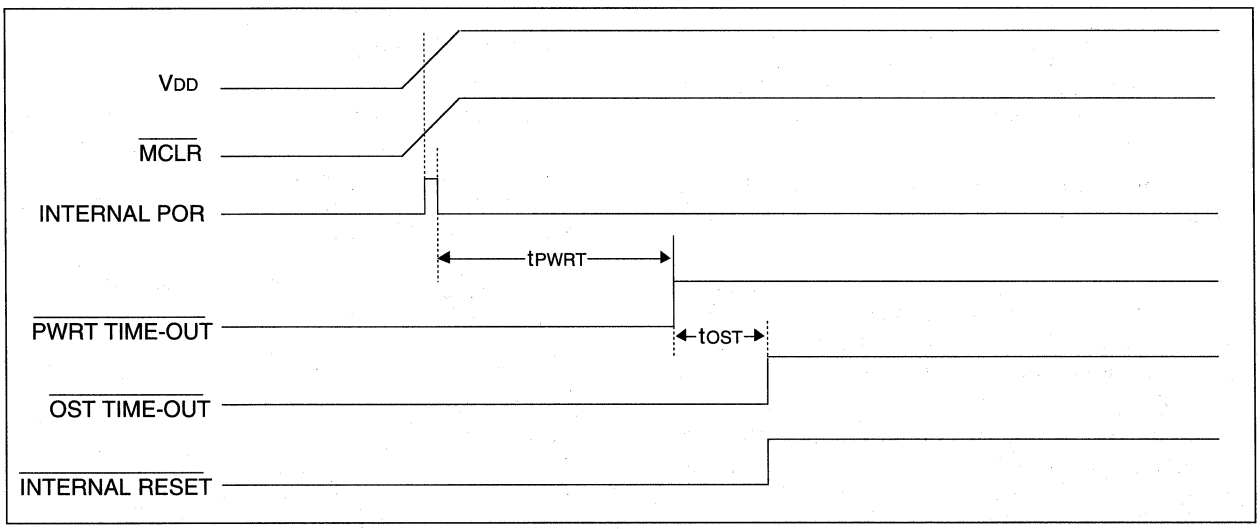
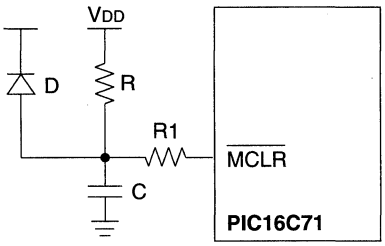


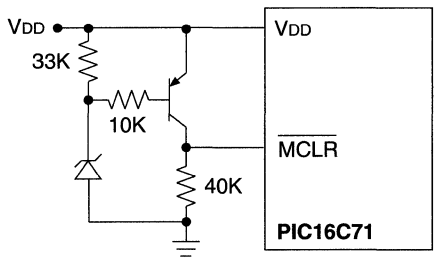
FIGURE 5.2.4 - EXTERNAL POWER ON RESET CIRCUIT



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ is recommended to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

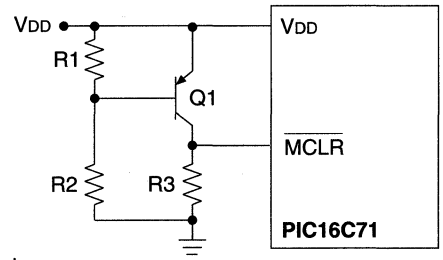
FIGURE 5.2.5 - BROWN OUT PROTECTION CIRCUIT 1



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 5.2.6 - BROWN OUT PROTECTION CIRCUIT 2



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

5.3 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (section 5.6).

5.3.1 WDT Period

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

5.3.2 WDT Programming Considerations

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

5.4 OSCILLATOR CONFIGURATIONS

5.4.1 Oscillator Types

The PIC16C71 can be operated in 4 different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes.

5.4.2 Crystal Oscillator

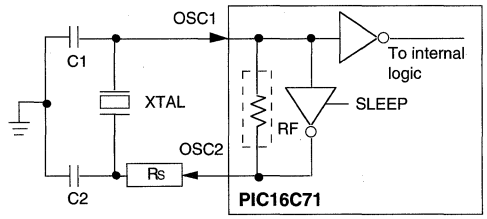
In XT, HS, or LP modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 5.4.1).

TABLE 5.4.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 5.4.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



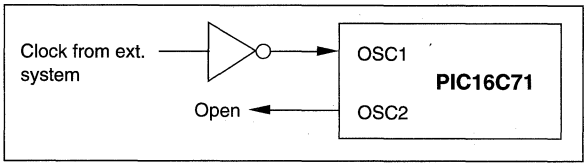
Rs is recommended for "HS" devices (100Ω < Rs < 1K). Rs may also be used in XT mode for AT strip-cut crystalg. See Tables 5.4.1 and 5.4.2 for recommended values of C1, C2 and Rs.

TABLE 5.4.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 5.4.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)



5.4.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 5.4.3 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

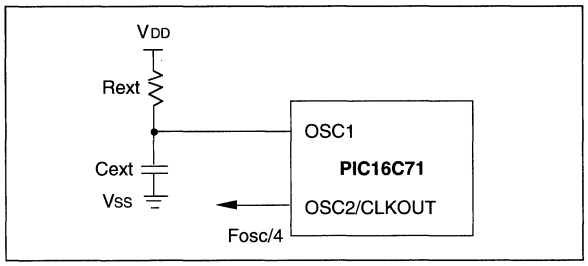
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See table in section 9.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in section 9.0 for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3.2.1 for timing).

FIGURE 5.4.3 - RC OSCILLATOR (RC TYPE ONLY)



5.5 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f03) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PortB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time out does not drive $\overline{MCLR}$ pin low.

5.5.1 Wake-up from SLEEP

The device can wake up from SLEEP through one of the following events:

a. External reset input on $\overline{MCLR}$ pin

b. Watchdog timer timeout reset (if WDT was enabled)

c. Interrupt from INT pin, RB port change or A/D converter.

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device reset. PD bit, which is set on power-up is cleared when SLEEP is invoked. TO bit is cleared if WDT time-out occurred (and caused wake-up).

For the device to wake up through an interrupt, the corresponding interrupt mask bit must be enabled. On wake-up, the device will continue to execute code in-line if global interrupt was disabled (GIE = 0) or branch to interrupt service routine if GIE was enabled.

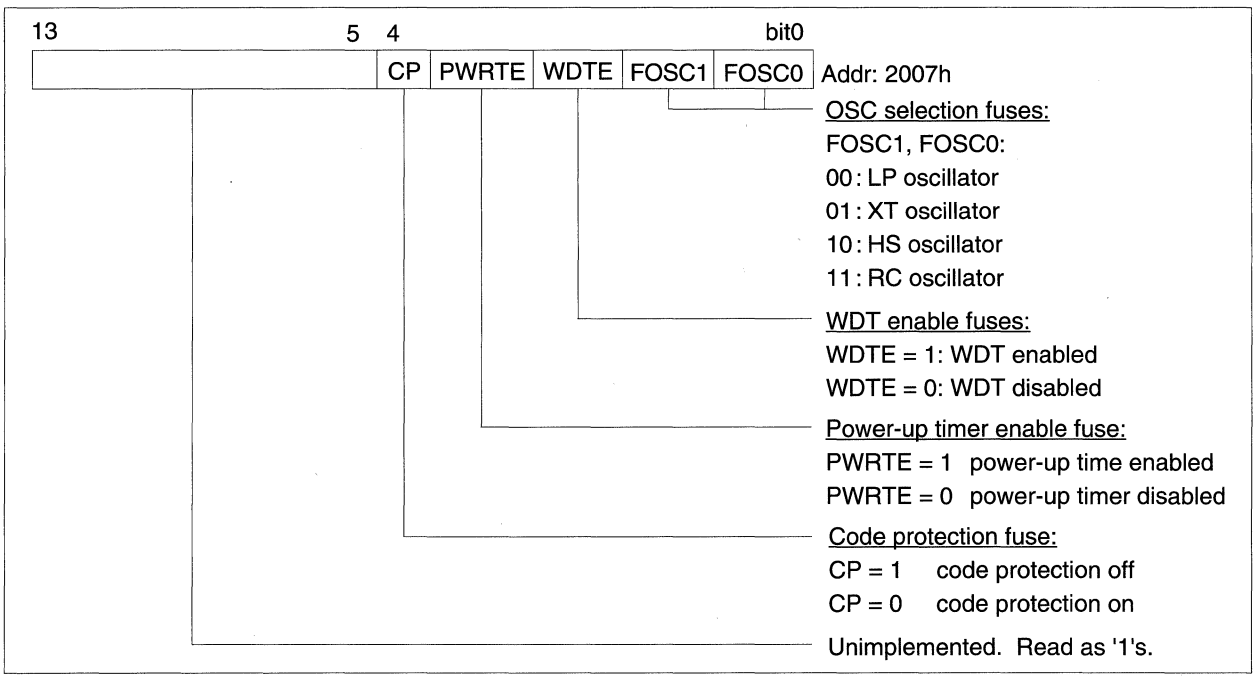
5.6 CONFIGURATION FUSES

The PIC16C71 has five configuration fuses which are EPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh). However, through a special mode, this location can be accessed during programming.

See description of fuses in figure 5.6.1.

FIGURE 5.6.1: CONFIGURATION WORD



5.7 ID LOCATIONS

The PIC16C71 has four ID locations (2000h - 2003h) mapped in the test program memory for storing code revision number, manufacturing information or other useful information. As with the configuration word, these locations are readable and writable through a programmer. They are not accessible during normal code execution.

If the chip is code protected, it is recommended that the user uses only the lower seven bits of the ID locations and program the higher seven bits as '1'. This way the ID locations will be readable even after code protection.

5.8 CODE PROTECTION

The code in the program memory can be protected by blowing the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 0040h and above are protected against programming.

It is still possible to program locations 0000h - 003Fh, the ID locations and the configuration fuses.

5.8.1 Verifying a Code-protected PIC

When code protected verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC against this file.

6.0 OVERVIEW OF PERIPHERALS

The PIC16C71 has 13 I/O pins organized as two I/O ports, PortA (5 bit) and PortB (8-bit). It has an 8-bit timer/counter (RTCC) with a programmable 8-bit prescaler and an analog to digital converter module. The A/D converter has up to four analog inputs, internal or external reference, 8 bit resolution and a typical 20µs conversion time.

6.1 PORTA

PortA is a 5 bit wide port with pins RA0 - RA4. Port pins RA<3:0> are bidirectional whereas RA4 has a open-collector output. PortA is file register 05h. Its corresponding direction control register TRISA is mapped in page 1 of register file at address 85h. TRISA is a five-bit wide register with bits <4:0>.

Pins RA<3:0> are multiplexed with analog input channels AIN3 - AIN0. Pin RA3 is further multiplexed with external reference voltage VREF for the ADC. Two bits in control register ADCON1 (file register 88h) are used to configure these pins as digital (i.e. port) or analog pins. When configured as analog inputs, these pins will read as '0's and the TRISA register bits will have no effect. Upon power-on reset, RA<3:0> are configured as analog inputs.

FIGURE 6.1.1 - BLOCK DIAGRAM OF RA0 - RA3 PINS

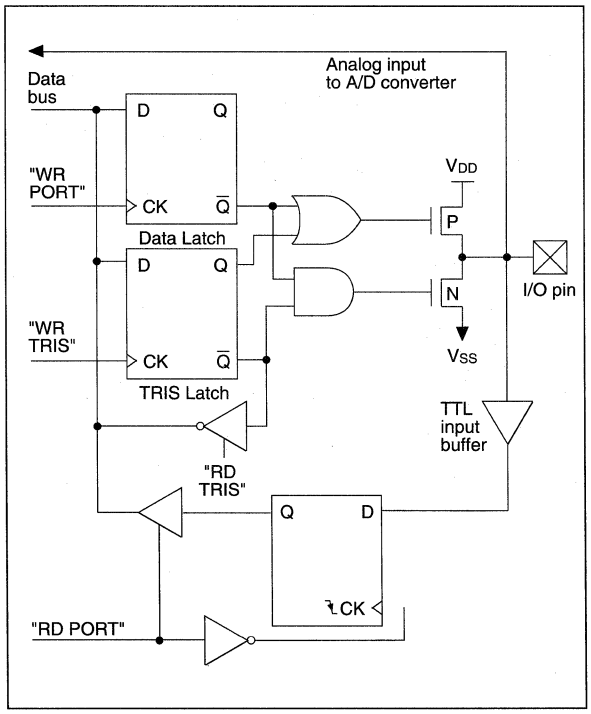


TABLE 6.1.1 - PORTA FUNCTIONS

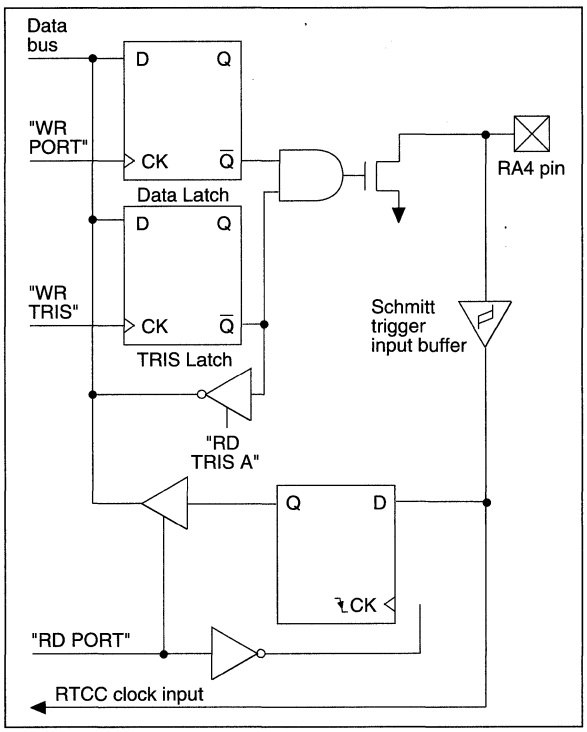
Port Pin	Bit	Pin Function	Alternate Function
RA0/AIN0	bit0	Input/output port. TTL input levels	Analog input channel 0
RA1/AIN1	bit1	Input/output port. TTL input levels	Analog input channel 1
RA2/AIN2	bit2	Input/output port. TTL input levels	Analog input channel 2
RA3/AIN3/VREF	bit3	Input/output port. TTL input levels	Analog input channel 3 or external reference voltage input (VREF)
RA4/RT	bit4	Input/output port. Output is open collector type. Input is Schmitt trigger type.	External clock input for RTCC timer/counter

TABLE 6.1.2 - SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PortA pins when read PortA latch when written	05h	---X XXXX
TRISA	PortA data direction register	85h, PAGE1	---1 1111
ADCON1	A/D converter control register	88h, PAGE1	---- --00

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to table 5.1.1.

FIGURE 6.1.2 - BLOCK DIAGRAM OF RA4 PIN



6.2 PORTB

PortB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB sets the corresponding port pin as an input. Reading PortB register reads the status of the pins whereas writing to it will write to the port latch.

Each of the PortB pins has a weak internal pull-up (~250 µA typical). The weak pull-up is automatically turned off if the port pin is configured as an output. A single control bit RBPU (bit 7, OPTION register) can turn off (RBPU = 1) all the pull-ups. The pull-ups are disabled on power on reset.

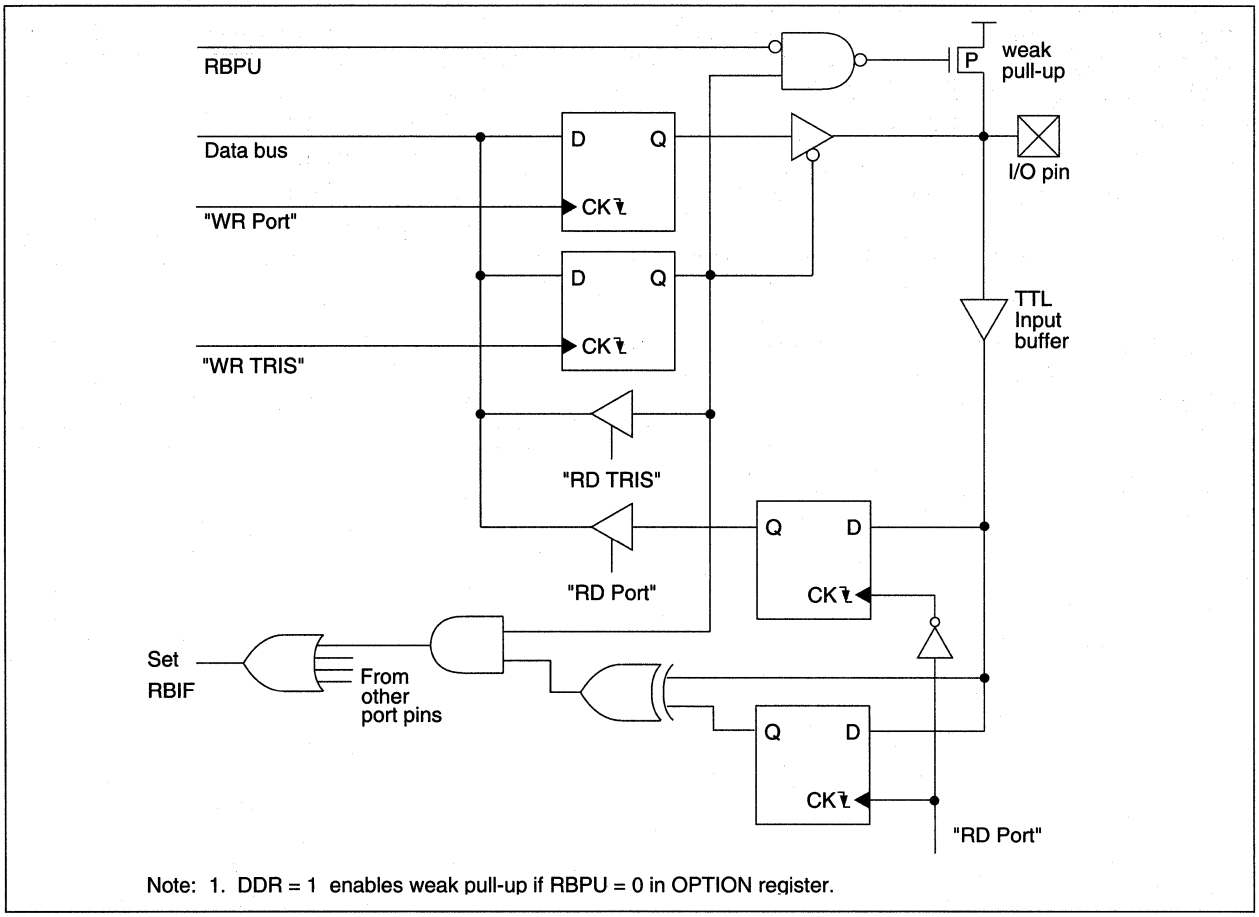
Port B has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are sampled and latched every Q1. The new input is compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in bit0, INTCON). Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIE (bit3, INTCON) bit.

b) Read Port B. This will end mismatch condition. Next, clear RBIF bit.

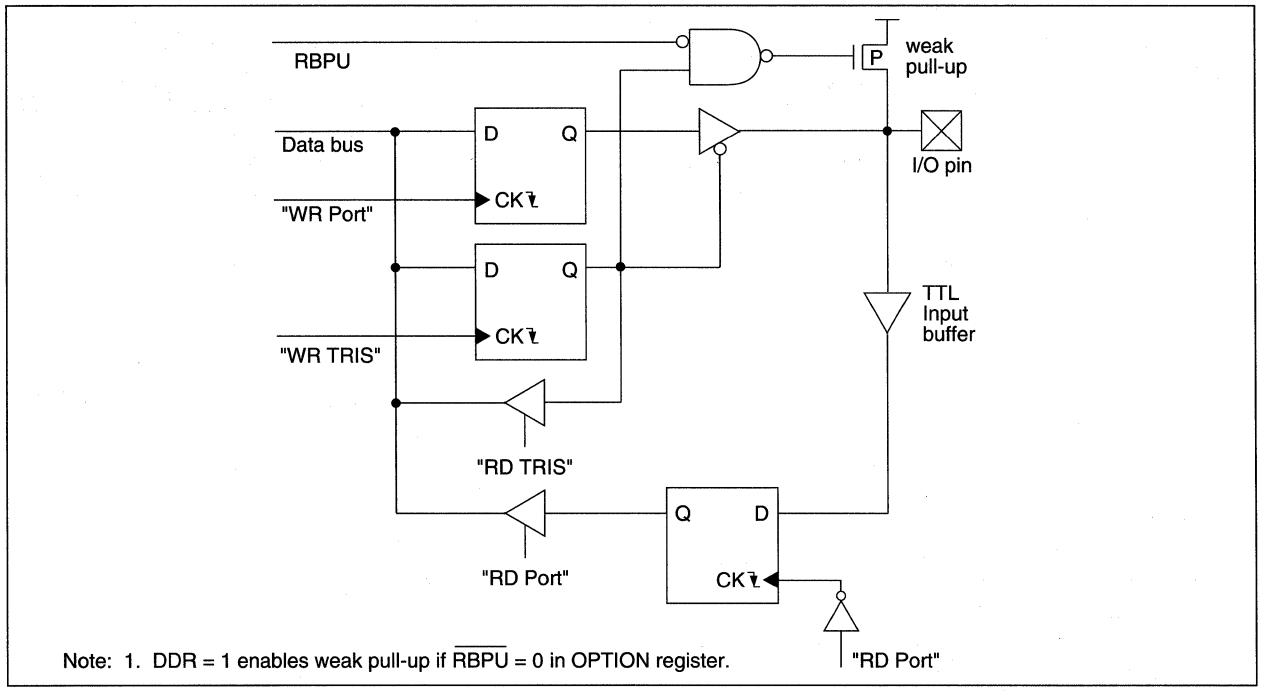
This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

FIGURE 6.2.1 - BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. DDR = 1 enables weak pull-up if RBPU = 0 in OPTION register.

FIGURE 6.2.2 - BLOCK DIAGRAM OF PORT PINS RB<3:0>



Note: 1. DDR = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = 0 in OPTION register.

Finally, port pin RB0 is multiplexed with external interrupt input INT.

TABLE 6.2.1 - PORTB FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RB0/INT	bit0	Input/output port pin. TTL input levels and internal software programmable weak pull-up	External interrupt input
RB1	bit1	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB2	bit2	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB3	bit3	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB4	bit4	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB5	bit5	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB6	bit6	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB7	bit7	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change

TABLE 6.2.2 - SUMMARY OF PORTB REGISTERS

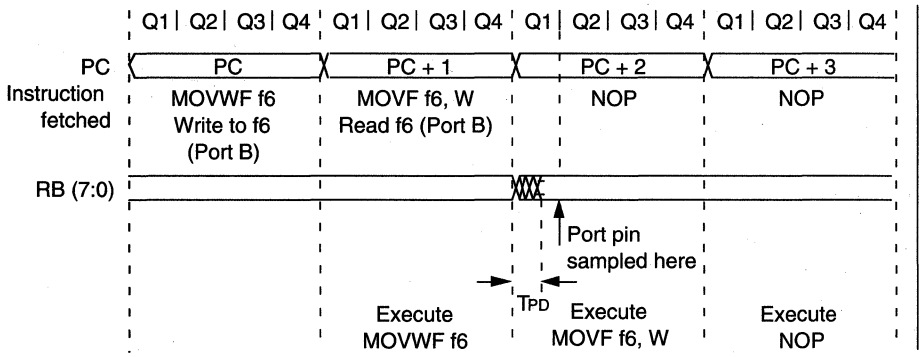
Register Name	Function	Address	Power-on Reset Value
PORTB	PortB pins when read PortB latch when written	06h	XXXX XXXX
TRISB	PortB data direction register	86h	1111 1111
OPTION	Weak pull-up on/off control ($\overline{\text{RBPU}}$ bit)	88h	1111 1111

6.3 I/O PROGRAMMING CONSIDERATIONS

6.3.1 BIDIRECTIONAL I/O PORTS

a) Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.
For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).



Note:

This example shows write to port B followed by a read from port B. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

6.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see figure 6.3.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

6.3.3 OPERATION IN NOISY ENVIRONMENT

In noisy application environments, such as keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes. The on-chip watchdog timer will take care of all situations involving program sequence "lock-ups." However, if an I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lock-up" situation without leading to a watchdog timer timeout. Thus, it is recommended to redefine all I/O pins in regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading input data or writing output data .

6.4 Real Time Clock/Counter (RTCC)

The RTCC timer/counter has the following features:

- 8 bit timer/counter
- Readable and writable (file address 01h)
- 8 bit software programmable prescaler
- Internal or external clock select

Figure 6.4.1 is a simplified block diagram of the RTCC module.

Timer mode is selected by setting RTS bit to '0' (OPTION register). In timer mode, the RTCC will increment every instruction cycle (without prescaler). If RTCC (f01) is written, increment is inhibited for the following two cycles (see figures 6.4.2 and 6.4.3). The user can work around this by writing an adjusted value to the RTCC.

Counter mode is selected by setting RTS bit to '1' (OPTION register). In this mode RTCC will increment either on every rising or falling edge of pin RA4/RTCC. This is determined by control bit RTE (OPTION register). RTE = 0 selects rising edge. Restrictions on external clock input is discussed in detail in section 6.4.1.

The prescaler is shared between the RTCC and the watchdog timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION register). PSA = 0 will assign the prescaler to RTCC. The prescaler is not readable or writable. When the prescaler is assigned to the RTCC, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.4.2 details the operation of the prescaler.

6.4.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 6.4.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 5) is the same as RTCC clock input and therefore the requirements are:

TRTH = RTCC high time ≥ 2tosc + 20 ns

TRTL = RTCC low time ≥ 2tosc + 20 ns

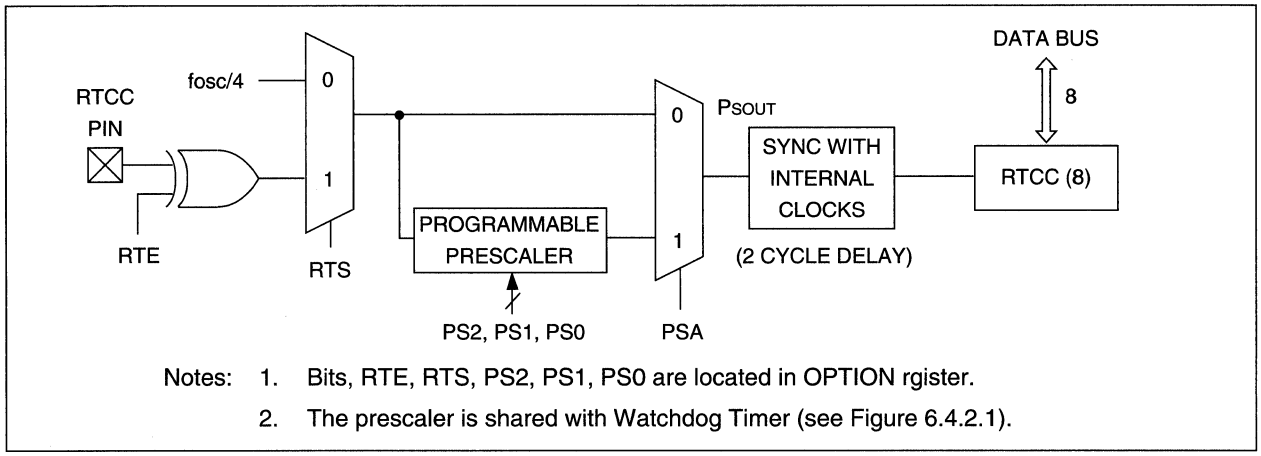
When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: PSOUT high time = PSOUT low time = $\frac{N.T_{RT}}{2}$
where TRT = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N.T_{RT}}{2} \geq$ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

TRT = RTCC period ≥ (4 tosc + 40 ns)/N
TRTH = RTCC high time ≥ 10 ns
TRTL = RTCC low time ≥ 10 ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 6.4.1.1, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

FIGURE 6.4.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in OPTION rgister.
2. The prescaler is shared with Watchdog Timer (see Figure 6.4.2.1).

FIGURE 6.4.2 - RTCC TIMING: INT CLOCK/NO PRESCALE

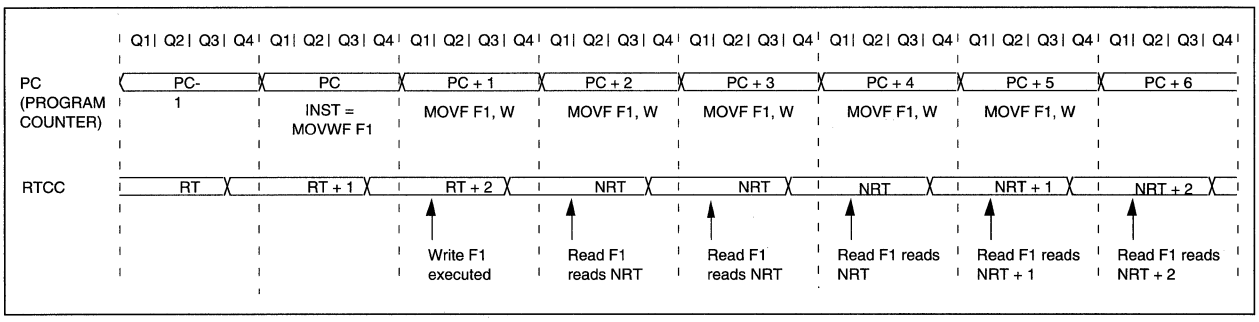


FIGURE 6.4.3 - RTCC TIMING: INT CLOCK/PRESCALE 1:2

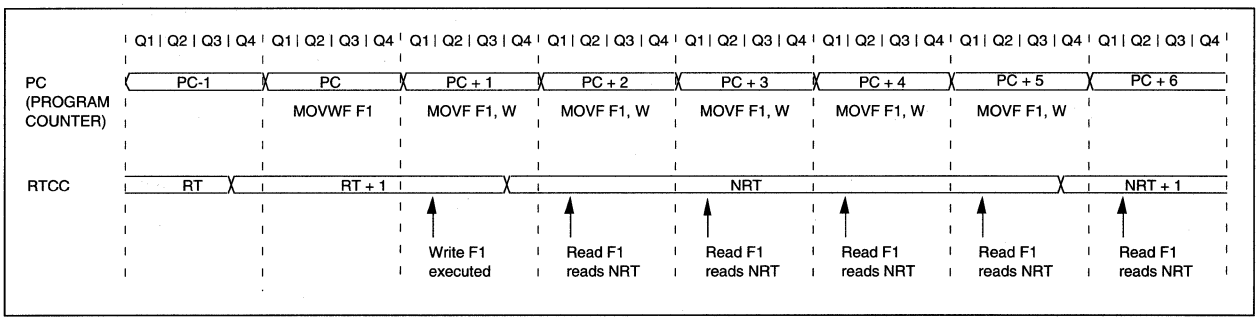
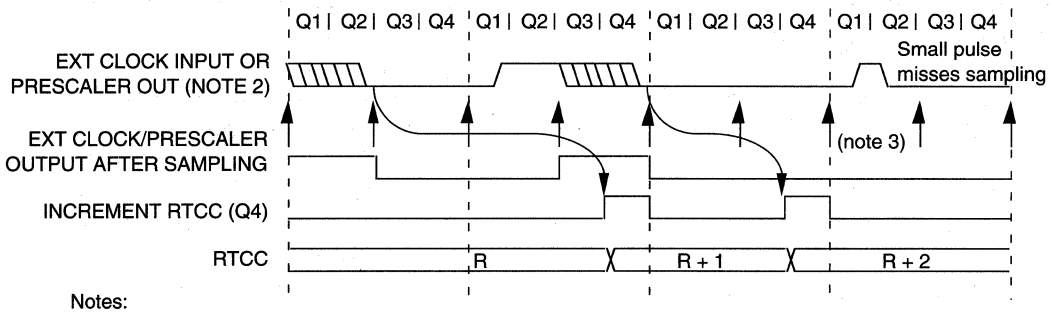


FIGURE 6.4.1.1 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:
1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

6.4.2 Prescaler

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the watchdog timer, respectively (Figure 6.4.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio. When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the watchdog timer. The prescaler is not readable or writable.

6.4.2.1 SWITCHING PRESCALER ASSIGNMENT

Changing prescaler from RTCC to WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'  ; Select internal clock and select new
2. OPTION              ; prescaler value. If new prescale value
                       ; is = '000' or '001', then select any other
                       ; prescale value temporarily.
3. CLRF 1              ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'  ; Select WDT, do not change prescale
                       ; value.
5. OPTION              ;
6. CLRWDT              ; Clears WDT and prescaler.
7. MOVLW B'xxxx1xxx'   ; Select new prescale value.
8. OPTION              ;
```

Step 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT              ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'  ; Select RTCC, new prescale value
                       ; and clock source
3. OPTION              ;
```

6.5 OPTION REGISTER

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt, the RTCC and the weak pull-ups on PortB.

TABLE 6.4 - SUMMARY OF RTCC REGISTERS

Register Name	Function	Address	Power-on Reset Value
RTCC	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for RTCC	81h	1111 1111
INTCON	RTCC overflow interrupt flag and mask bits	0Bh	0000 000X

FIGURE 6.4.2.1 - BLOCK DIAGRAM OF THE RTCC/WDT PRESCALER

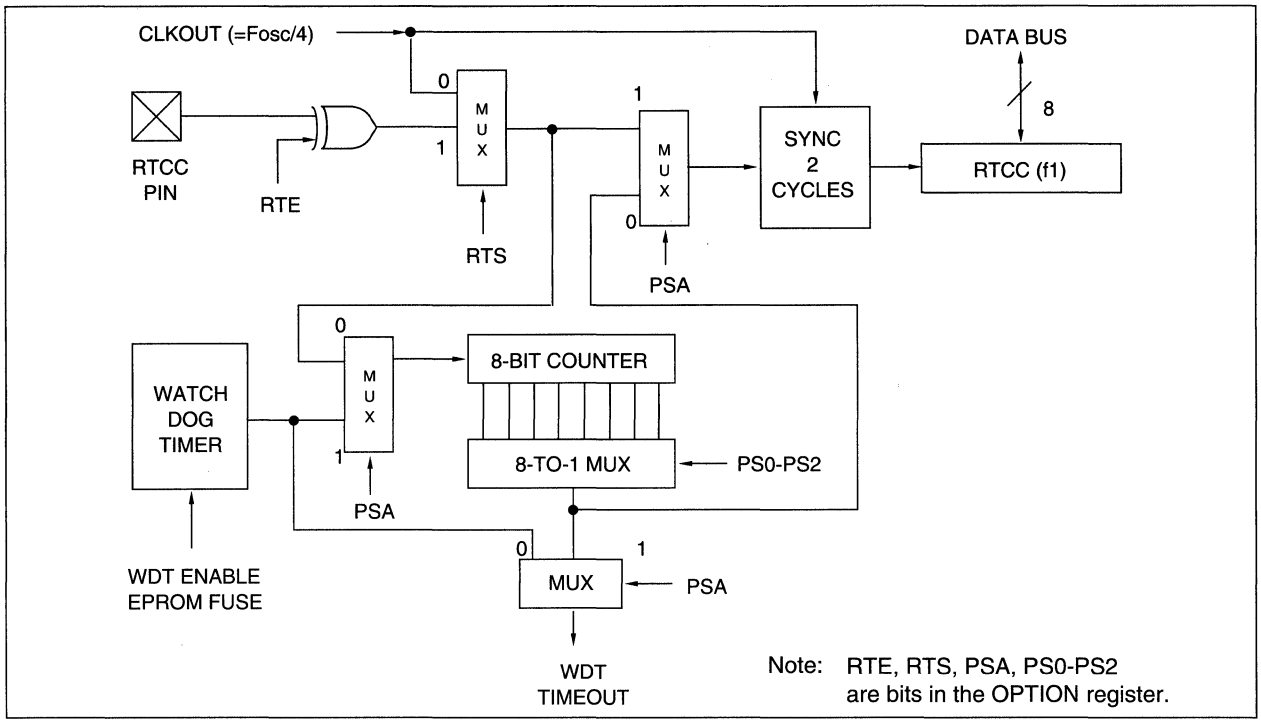
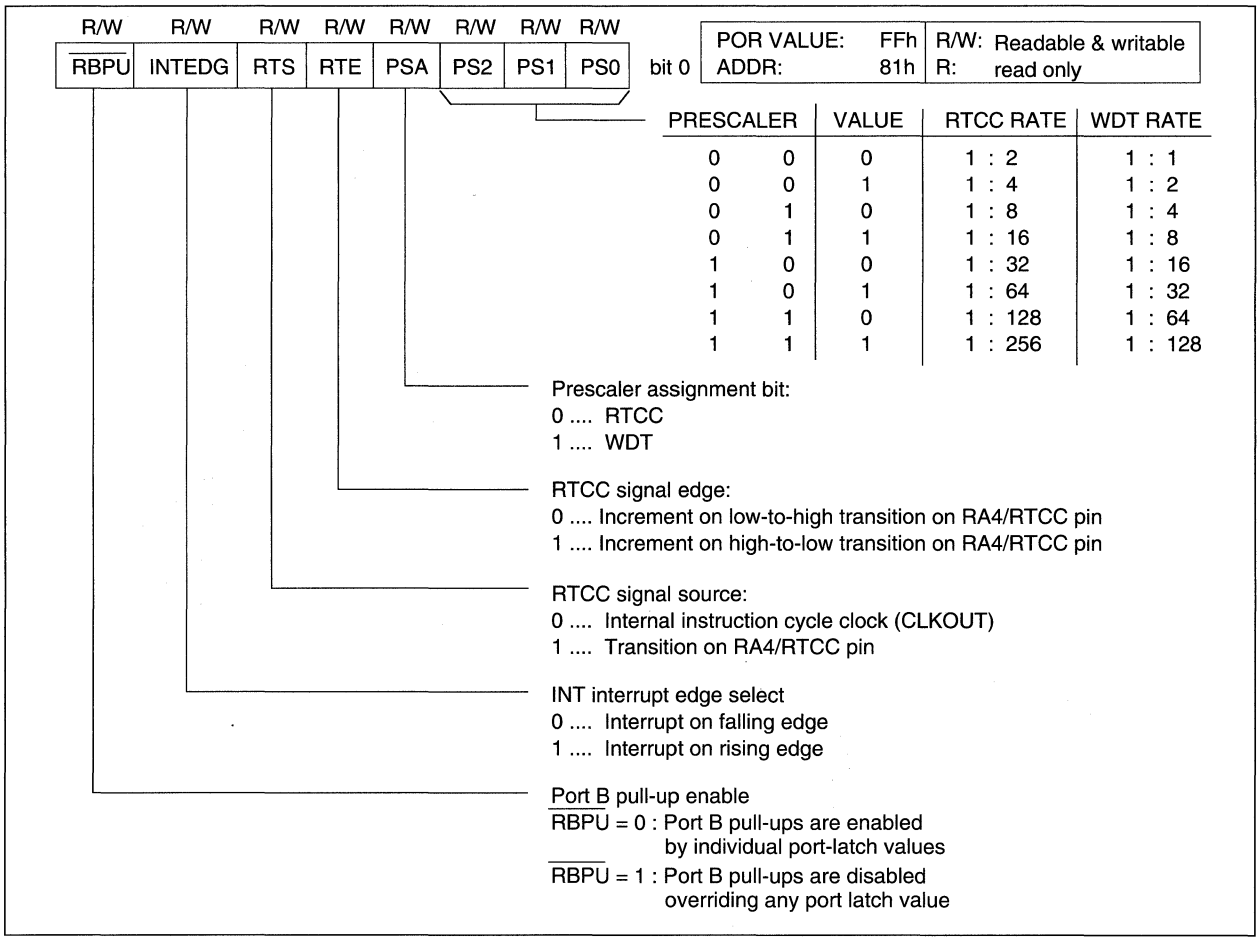


FIGURE 6.5.1 - OPTION REGISTER



6.6 A/D CONVERTER

The A/D converter module has four analog input channels multiplexed into one sample and hold and A/D converter. Reference voltage VREF can come externally from RA3/AIN3/VREF pin or internally from VDD. The converter itself is of successive approximation type and produces an 8-bit result in the ADRES register (address 09h). A conversion is initiated by setting a control bit (GO/DONE, ADCON register). Prior to conversion, the appropriate channel must be selected and enough time allowed for sampling to complete. The conversion time is a function of the oscillator cycle. The minimum conversion time required is 20 µs. At the end of conversion the GO/DONE bit is cleared and the A/D interrupt is activated. The overall accuracy (zero error, full scale error, integral error and quantization error) is less than ±1 LSB for VDD = 5.12V and VREF = VDD. The resolution and accuracy is less when VREF is less than VDD or for VDD less than 5.12V (see specifications for details).

FIGURE 6.6.1 - A/D CONTROL AND STATUS REGISTER (ADCON0, ADDRESS 08h)

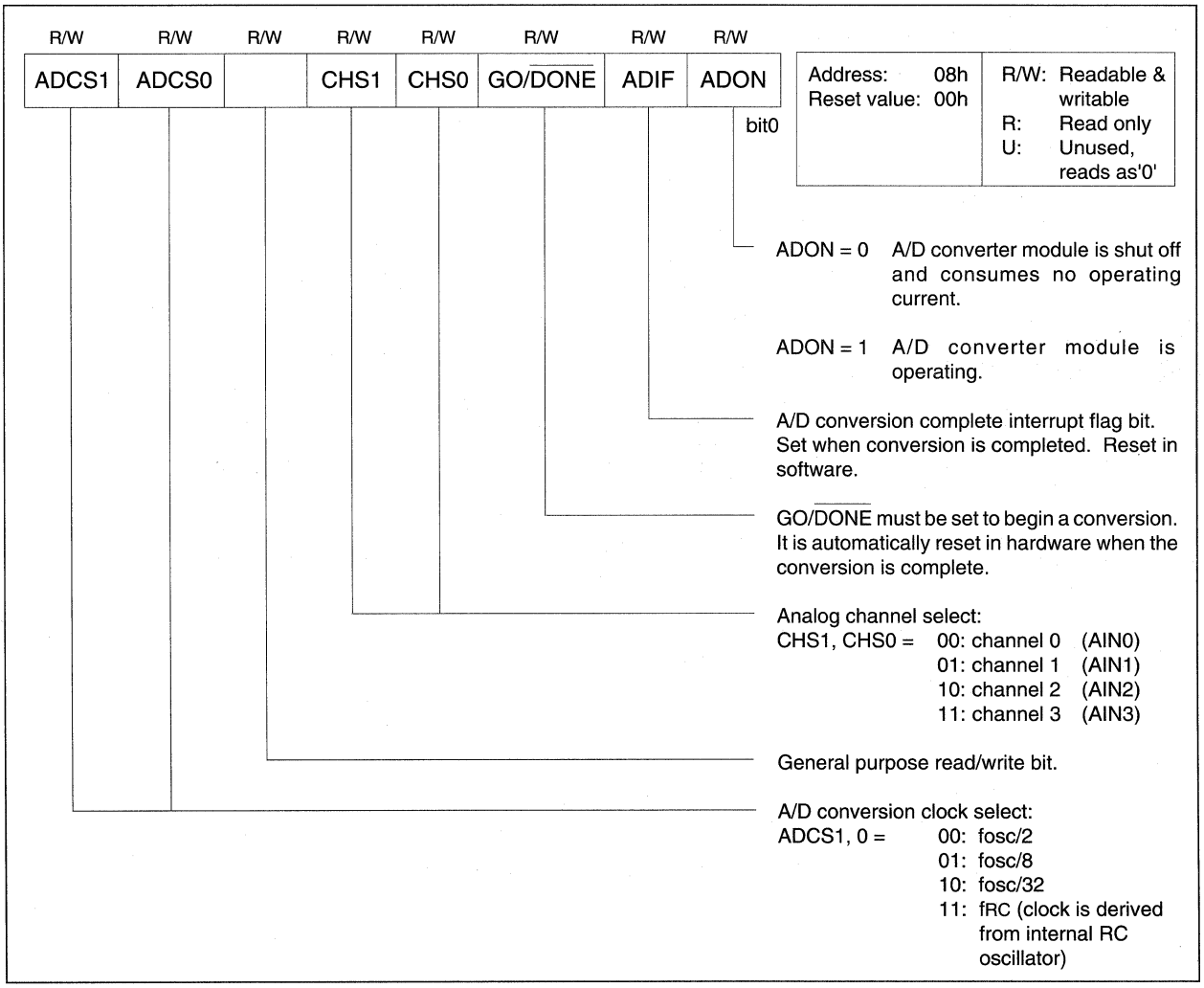


FIGURE 6.6.2 - A/D CONTROL REGISTER (ADCON1, ADDRESS 88h)

U	U	U	U	U	U	R/W	R/W
-	-	-	-	-	-	PCFG1	PCFG0
							bit0

Address: 08h
POR value: 00h

R/W: Readable & writable
R: Read only
U: Unimplemented, reads as'0'

PCFG1, 0 configures the RA0-RA3 pins in various modes:

PCFG1, 0	RA0, RA1	RA2	RA3	VREF
0 0	analog inputs	analog input	analog input	VDD
0 1	analog inputs	analog input	ref input	RA3
1 0	analog inputs	digital input	digital input	VDD
1 1	digital inputs	digital input	digital input	-

6.6.1 A/D Clocking Scheme

The A/D converter operates on its own clock, tad, derived from either the OSC1 clock input or from its own on-chip RC oscillator as follows:

Control bit ADCS1, ADCS0	tad (must be > 2 μs)
00	2 tosc
01	8 tosc
10	32 tosc
11	tRC (2 μs-6 μs, 4 μs nominal)

The conversion time for each bit is tad. The total conversion time is 10tad. Selection must be made such that tad is at least 2 μs.

At low frequencies, the RC oscillator can be selected to maintain shorter conversion time. The RC oscillator frequency varies considerably with voltage, temperature and process parameters (2 μs to 6 μs period, nominally 4 μs).

6.6.2 A/D Operation during SLEEP

To reduce operating current all biasing circuits in the A/D block that consume DC current are shut off when ADON bit is a '0'. If a conversion is in progress using RC oscillator, it will be completed. The ADIF interrupt flag bit will be set and the chip will wake up if the ADIE interrupt enable bit is a '1'. Since, during SLEEP, the switching noise is eliminated, the conversion accuracy will be the maximum possible. This provides a means for getting accurate conversions while operating the processor at high clock rates.

If SLEEP is invoked during a conversion that uses OSC1 clock, the conversion will be aborted. The A/D converter will be shut off. The user must re-initialize the conversion, starting with resampling.

6.6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6.6.3.1. First, the user must configure the TRISA register such that the analog pins are configured as inputs. Second, since the analog pins are connected to digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore must be between VSS and VDD. If input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. To minimize the possibility of damage to the analog inputs due to latch-up a minimum source impedance of 500Ω is recommended. A maximum source impedance of 10KΩ is recommended for the analog sources. At this impedance, the maximum possible error caused by the leakage current is ±5 mV or ±0.25 LSB at VDD = VREF = 5V (10KΩ x 0.5 μA).

The other reason to limit the maximum source impedance is to be able to capture the analog input voltage on to the holding capacitor. The time constant to charge Chold is (see figure 6.6.3.1):

= Chold (Ric + RSS + RS) where RS = source impedance

≈ 51.2 pF (2KΩ +RS) Ric + RSS ≈ 2KΩ

≈ 51.2 pF x 12KΩ (assuming RS = 10KΩ)

= 0.6144 μs = T

from the capacitive charging equation:

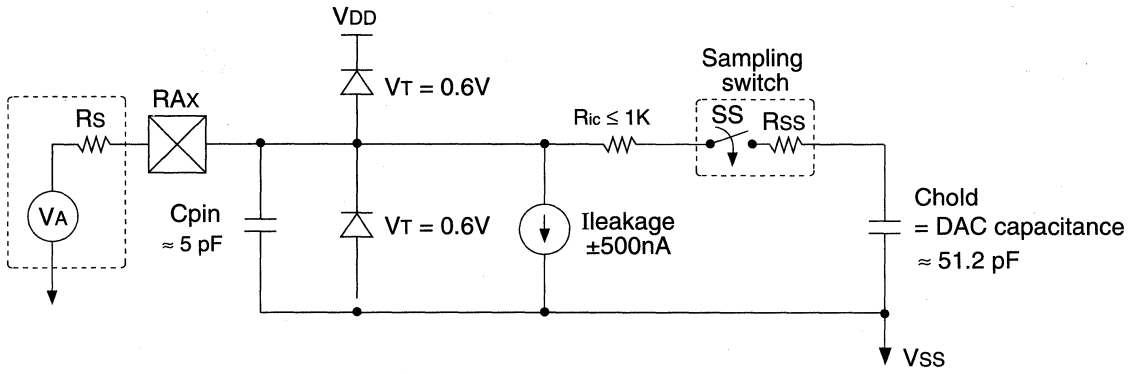
$V_{hold} = V_A (1-e^{-t/T})$

for 1/8 LSB error at VDD = 5V

$e^{-t/T} = \frac{2.5\ mV}{5000\ mV}$

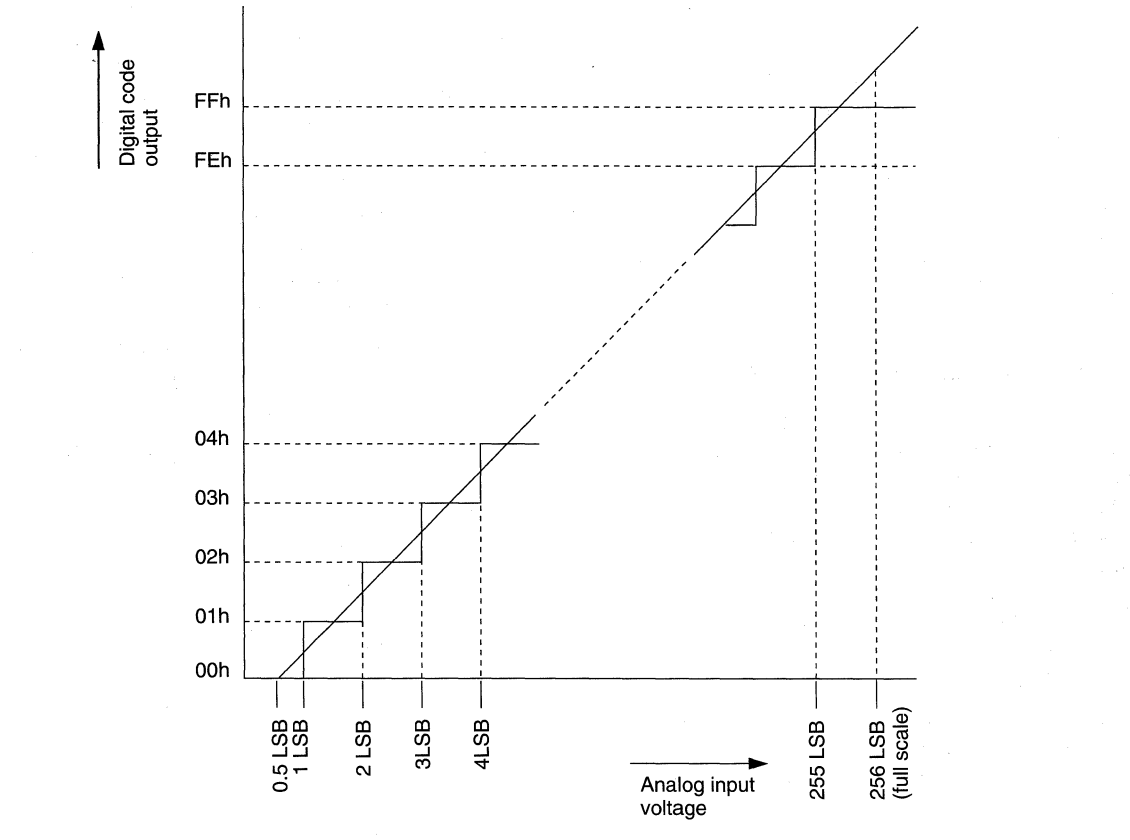
or t ≈ 7.6T = 4.67μs (required sampling time)

FIGURE 6.6.3.1 - ANALOG INPUT MODEL



Legend		
	Cpin	= input capacitance
	VT	= threshold voltage
	Ileakage	= leakage current at the pin due to various junctions
	Ric	= interconnect resistance
	RSS	= on resistance of the switch
	SS	= sampling switch
	Chold	= sample/hold capacitance (from DAC)
	Rs	= source impedance of the analog input
	VA	= analog input voltage

FIGURE 6.6.5.1 - TRANSFER FUNCTION



External RC filter is sometimes added for anti-aliasing. Once again, the value of the R should be such that the total source impedance is kept under 10KΩ. Any external component connected to an analog input pin, such as a capacitor or a zener diode, should have very little leakage current.

6.6.4 Sample and Hold (S/H)

The sample and hold circuit consists of a sampling switch SS (figure 6.6.3.1) and the S/H capacitor whose value is typically 51 pF.

As long as ADON control bit is '1' (bit 0, ADCON 0) and a valid analog input channel is selected, the input will be continuously sampled. There is no command to start or stop sampling. When a conversion is started, sampling is ended and conversion begins on the voltage across the S/H capacitor. The sample and hold, therefore can be more accurately described as "track and hold".

After a conversion is completed, sampling begins after a delay of 2tad. (tad = A/D conversion clock). The user must keep this in mind when allowing for adequate sampling time.

6.6.5 Transfer Function

The ideal transfer function of the A/D converter is as follows: The first transition occurs when input voltage (V_A) is 1 LSB (or full scale/256). Figure 6.6.5.1 shows the ideal transfer function.

6.6.6 SUMMARY OF A/D REGISTERS

Register name/bits	Function	Address
ADRES	A/D result register	09h
ADCON0	A/D control and status register	08h
ADCON1	A/D control register	88h
INTCON (bit ADIE)	Interrupt control register	0Bh

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Ambient temperature under bias ..... -55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.6V to V_{DD} +0.6V
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 100 mA
Max. Current into an input pin ..... ±500 nA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 20 mA
Max. Output Current sunk by I/O port A ..... 80 mA
Max. Output Current sunk by I/O port B ..... 150 mA
Max. Output Current sourced by I/O port A ..... 50 mA
Max. Output Current sourced by I/O port B ..... 100 mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or compliance to AC and DC parametric specifications at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum Ioh\} + \sum\{(V_{DD}-Voh) \times Ioh\} + \sum(Vol \times Iol)$

2. Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

7.1 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 4.0V to 6.0V

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage						
	VDD	4.0		6.0	V	XT, RC and LP osc configuration
	VDD	4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5 *		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS *		V	See section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 5.2 for details on power on reset
Supply Current (Note 3)						
	IDD1		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
	IDD2		35	70	µA	FOSC = 32 KHz, VDD = 4.0V, WDT disabled, LP osc config., A/D off (Note 6)
	IDD3		9	20	mA	FOSC = 20 MHz, VDD = 5.5V, HS osc configuration (PIC16C71-20)
Power Down Current (Note 4)						
	IPD1		7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +125°C
	IPD2		1.0	14	µA	VDD = 4.0V, WDT disabled, 0°C to +70°C
	IPD3		1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
	IPD4		1.0	20	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are guaranteed through characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 7.5.

7.2 DC CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 125°C for automotive, -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 3.0V to 6.0V					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
	VDD	3.0		6.0	V	XT, RC and LP osc configuration
	VDD	4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5 *		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS *		V	See section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 5.2 for details on power on reset
Supply Current (Note 3)						
	IDD1		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
	IDD2		15	32	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled, LP osc config., A/D off (Note 6)
Power Down Current (Note 4)						
	IPD1		5	20	µA	VDD = 3.0V, WDT enabled, -40°C to +125°C
	IPD2		0.6	9	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
	IPD3		0.6	12	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
	IPD4		0.6	16	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C

* These parameters are guaranteed through characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 7.5.

7.3 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 7.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL1	VSS		0.2 VDD	V	
$\overline{MCLR}$, RTCC, OSC1 (in RC configuration)	VIL2	VSS		0.2 VDD	V	Note 2
OSC1 (in XT, HS and LP configuration)	VIL3	VSS		0.3 VDD	V	
Input High Voltage						
I/O ports	VIH1	2.0		VDD	V	VDD ≤ 5.5V
	VIH1	0.36 VDD				For entire VDD range
$\overline{MCLR}$ RTCC, OSC1 (in RC configuration)	VIH2	0.8 VDD		VDD	V	Note 2
OSC1 (XT, HS and LP configuration)	VIH3	0.7 VDD		VDD	V	
Input Leakage Current (Notes 3, 4)						
I/O port RB	IIL1			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
I/O port RA	IIL2			±0.5	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$, RTCC	IIL3			±5	µA	VSS ≤ VPIN ≤ VDD
OSC1	IIL4			±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
Output Low Voltage						
I/O Ports	VOL1			0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
	VOL1			0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT	VOL2			0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)	VOL2			0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 4)	VOH1	VDD-0.7			V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
	VOH1	VDD-0.7			V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT	VOH2	VDD-0.7			V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)	VOH2	VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

7.4 AC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

* Guaranteed by characterization, but not tested.

(Notes on next page)

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial

Operating voltage VDD range as described in DC spec table 7.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	XT and RC osc mode
	FOSC	DC		4	MHz	HS osc mode (PIC16C71-04, PIC16LC71-04)
	FOSC	DC		20	MHz	HS osc mode (PIC16C71-20)
	FOSC	DC		200	KHz	LP osc mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC osc mode
	FOSC	0.1		4	MHz	XT osc mode
	FOSC	1		4	MHz	HS osc mode (PIC16C71-04 PIC16LC71-04)
	FOSC	1		20	MHz	HS osc mode (PIC16C71-20)
	FOSC	DC		200	KHz	LP osc mode
Instruction Cycle Time (Note 2)	TCY	1.0	4/FOSC	DC	µs	
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
MCLR Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	7*	18*	33*	ms	VDD = 5V, -40°C to +125°C
Oscillation Start-up Timer Period	TOST		1024 tosc		ms	tosc = OSC1 period
Power up timer period	TPWRT	28*	72*	132*	ms	VDD = 5V, -40°C to +125°C
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUT↓ (RC Mode)	TPD			40*	ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
All I/O pins	CIO			50	pF	

NOTES TO TABLE 7.4

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: For a detailed explanation of RTCC input clock requirements see section 6.4.1.

Note 4: Clock-in high-time is the duration for which clock input is at VIHOSC or higher. Clock-in low-time is the duration for which clock input is at VIHOSC or lower.

7.5 A/D CONVERTER CHARACTERISTICS:

PIC16C71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16C71-20 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS	**Standard Conditions (unless otherwise stated)** Operating temperature -40°C to +125°C for automotive, TA = -40°C to +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial, VDD = 5.12V					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 5.12V (Note 2)
Integral error	NINT	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Differential error	NDIF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Full scale error	NFS	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Offset error	NOFF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Monotonicity	-	-	guaranteed	-	-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 2.0	2tosc 8tosc 32tosc 4.0	- - - 6.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	For 10KΩ source impedance, to guarantee less than 1/8 LSB sampling error. (Note 3)
A/D conversion current (VDD)	Iad	-	180	-	µA	Average current consumption when A/D is on (Note 4)
VREF input current (Note 5)	IREF	-	-	1 10	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: The error will be more for lower VREF and/or lower VDD.

Note 3: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 4: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 5: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

7.6 A/D CONVERTER CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS		Standard Conditions (unless otherwise stated) Operating temperature -40°C to +125°C for automotive, TA = -40°C to +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial, VDD = 3.0V				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 3.0V (Note 2)
Integral error	NINT	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Differential error	NDIF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Full scale error	NFS	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Offset error	NOFF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Monotonicity	-	-	guaranteed	-	-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 3.0	2tosc 8tosc 32tosc 6.0	- - - 9.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	For 10KΩ source impedance, to guarantee less than 1/8 LSB sampling error. (Note 3)
A/D conversion current (VDD)	Iad	-	90	-	µA	Average current consumption when A/D is on (Note 4)
VREF input current (Note 5)	IREF	-	-	1 10	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V.

Note 3: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 4: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 5: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

7.6.1 Electrical Structure of Pins

FIGURE 7.6.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

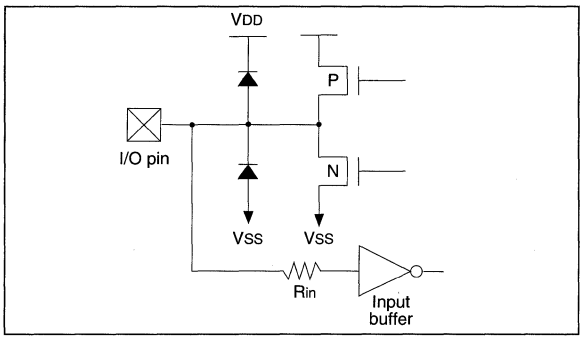
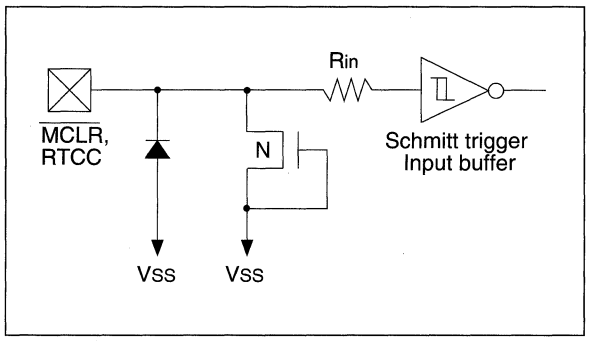


FIGURE 7.6.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



Notes to figures 7.6.1 and 7.6.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

8.0 TIMING DIAGRAMS

FIGURE 8.0.1 - RTCC TIMING

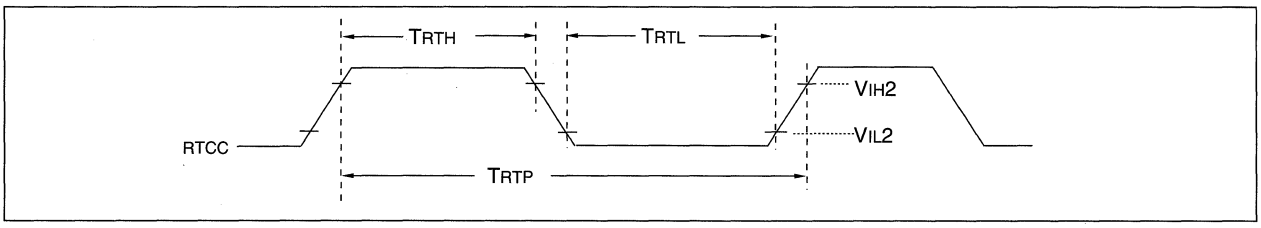


FIGURE 8.0.2 - OSCILLATOR START-UP TIMING (PIC16C71RC)

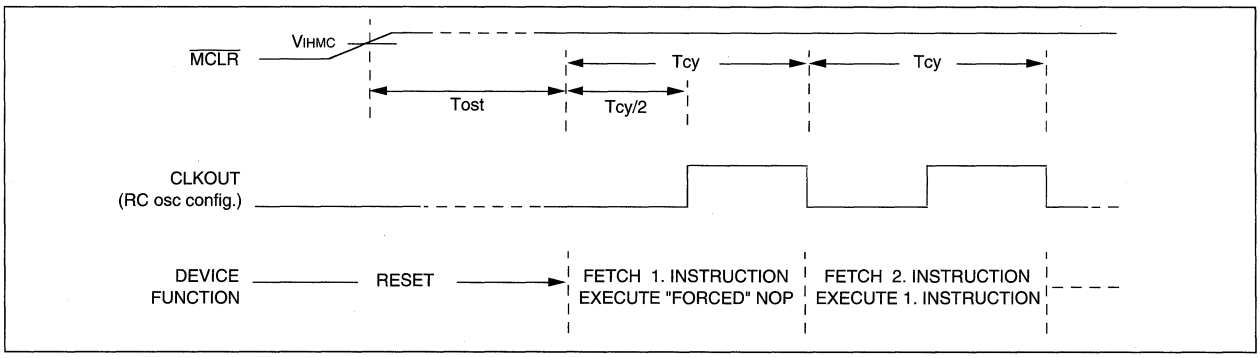
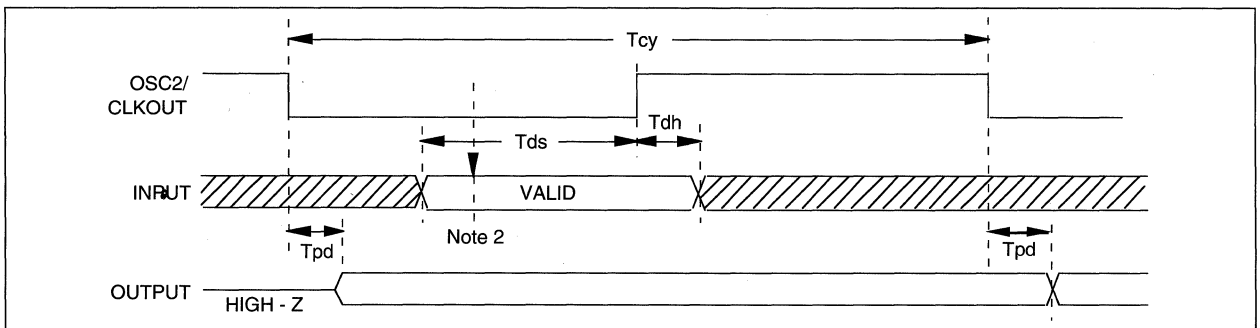


FIGURE 8.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes: 1. The CLKOUT output is available only in RC oscillator mode.
2. Internally, this is the point where input data is sampled. Since no timing edge is externally available, setup and hold times are specified with respect to the rising edge of CLKOUT.

9.0 DC & AC CHARACTERISTICS GRAPHS/TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. **In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 9.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

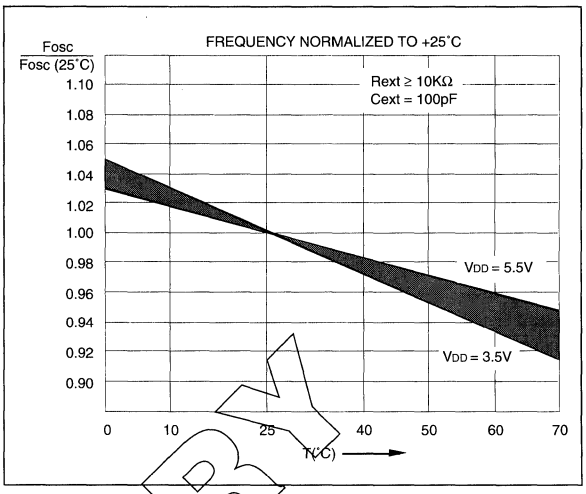


FIGURE 9.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

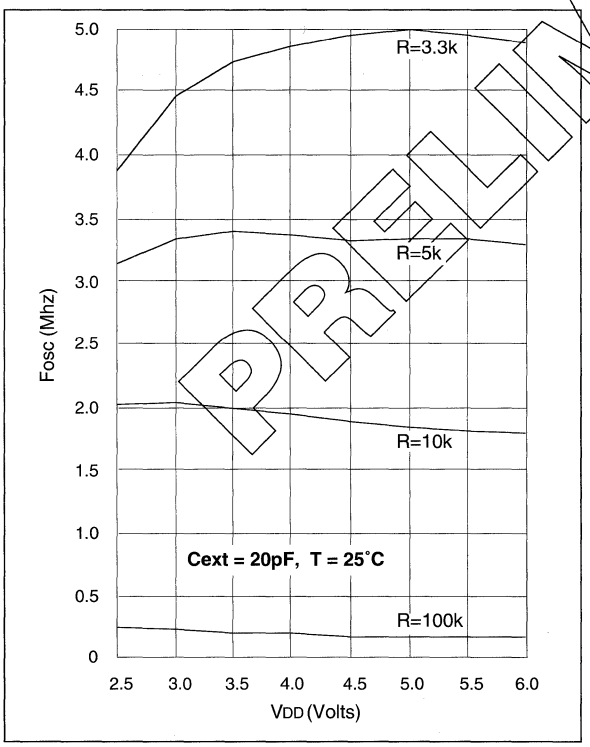
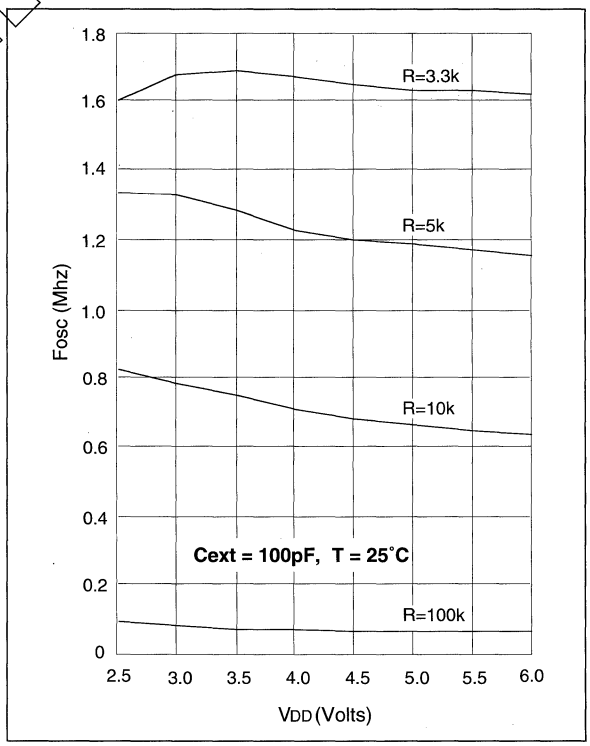


FIGURE 9.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD



Note: The gray shaded regions are outside normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

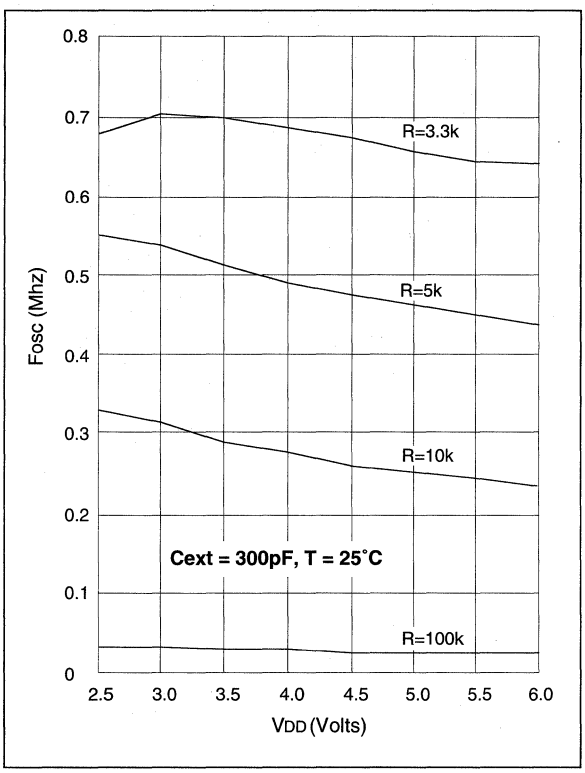


TABLE 9.0.1 - RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	4.71 MHz	± 28%
	5k	3.31 MHz	± 25%
	10k	1.91 MHz	± 24%
	100k	207.76 KHz	± 39%
100pf	3.3k	1.65 MHz	± 18%
	5k	1.23 MHz	± 21%
	10k	711.54 KHz	± 18%
	100k	75.62 KHz	± 28%
300pf	3.3k	672.78 KHz	± 14%
	5k	489.49 KHz	± 13%
	10k	275.73 KHz	± 13%
	100k	28.12 KHz	± 23%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 9.0.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

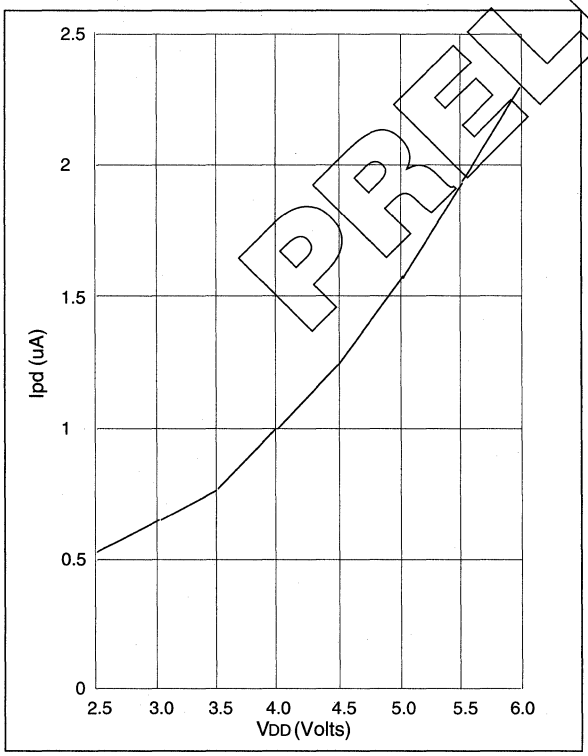
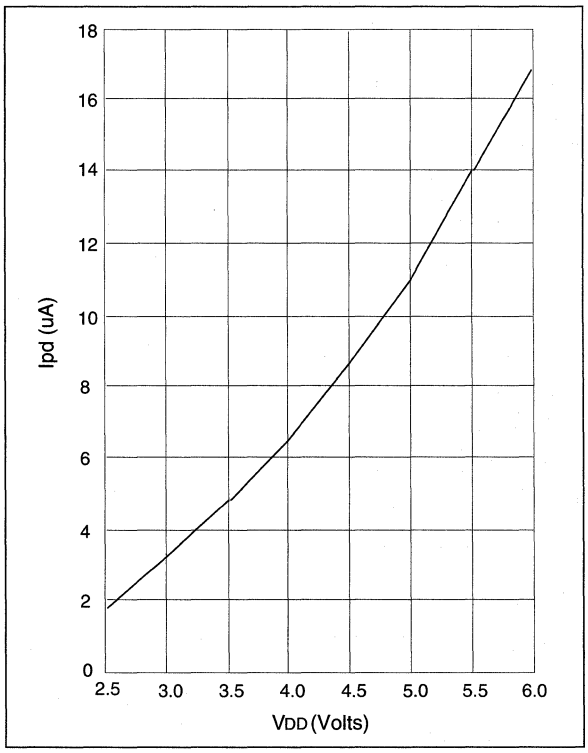


FIGURE 9.0.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C



Note 1: The gray shaded regions are outside normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

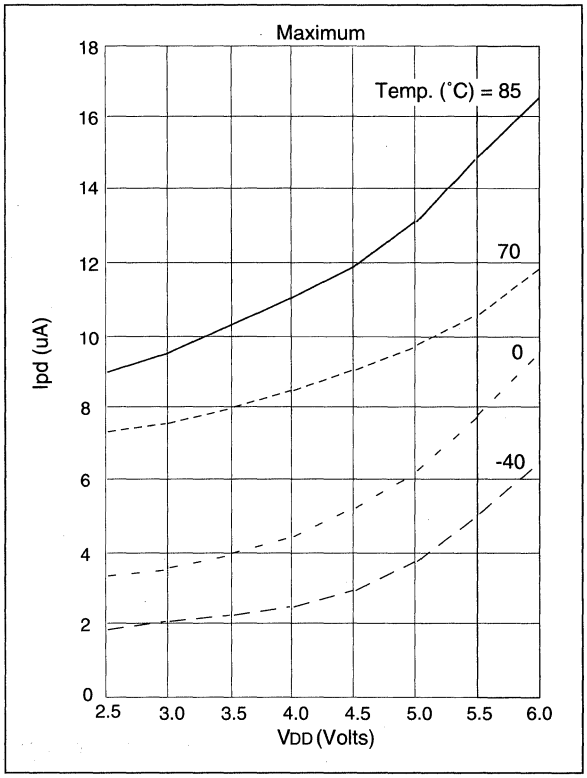
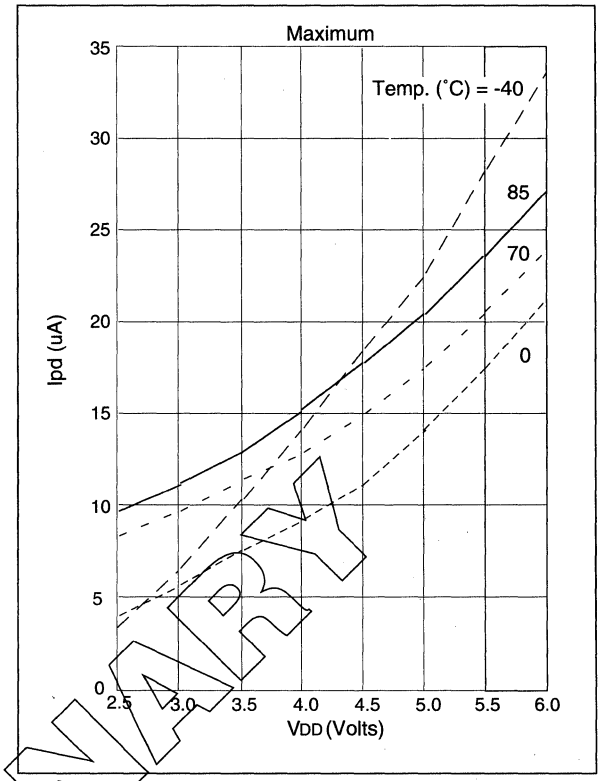


FIGURE 9.0.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

Note 1: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

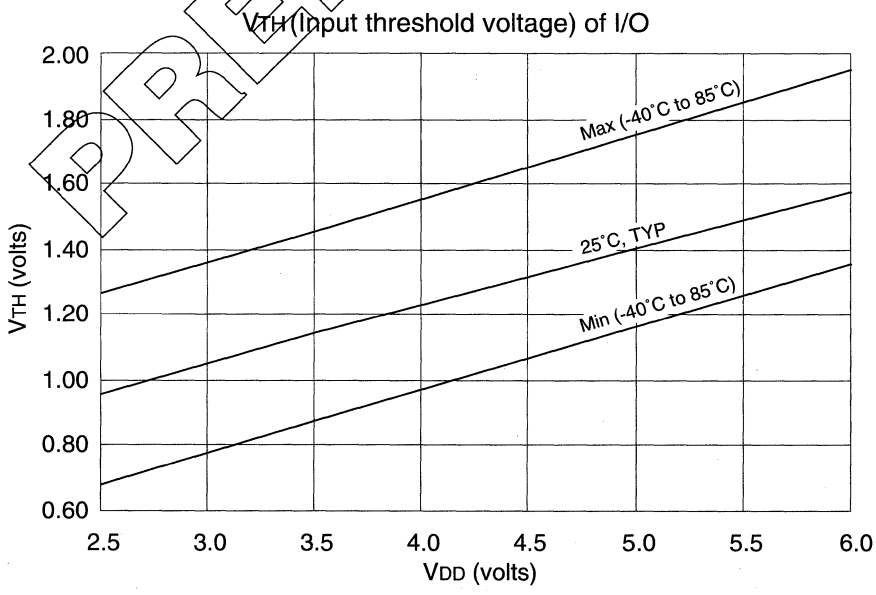
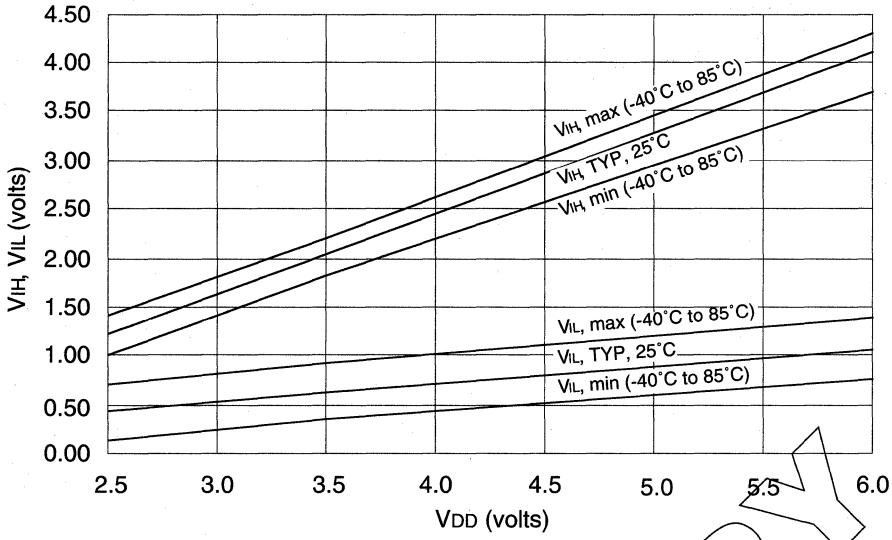
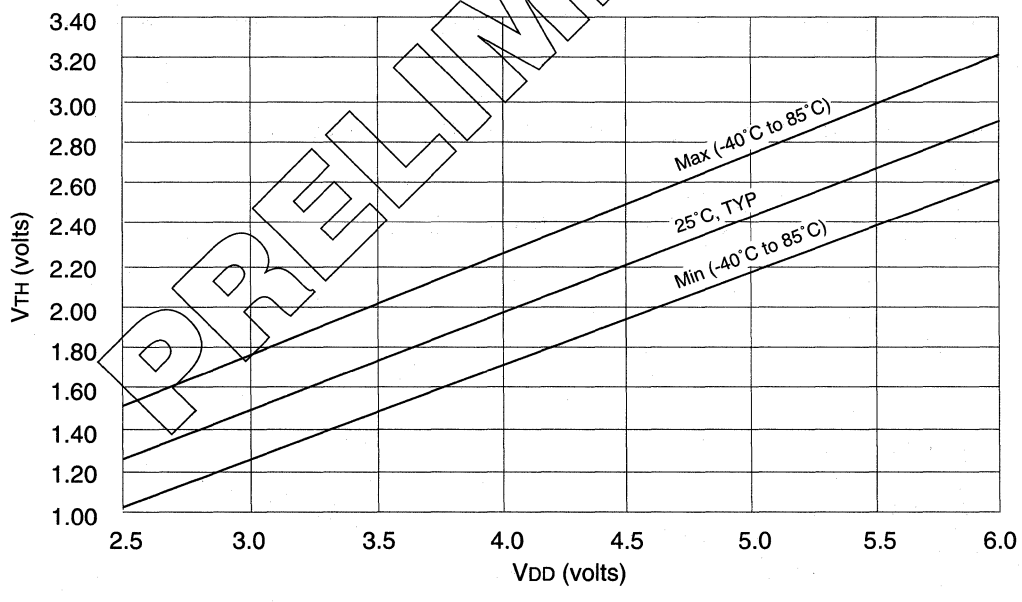


FIGURE 9.0.10 - VIH, VIL OF $\overline{\text{MCLR}}$, RTCC AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 9.0.11 - VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

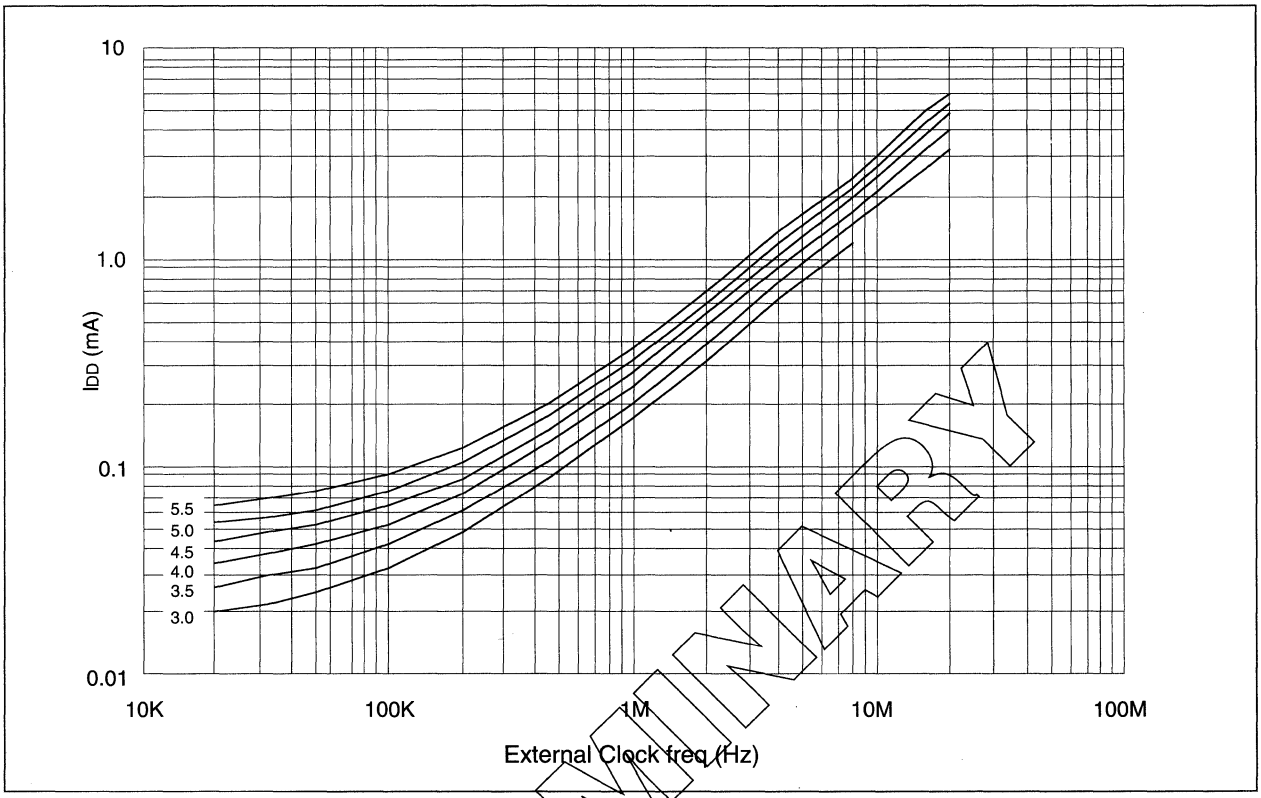


FIGURE 9.0.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

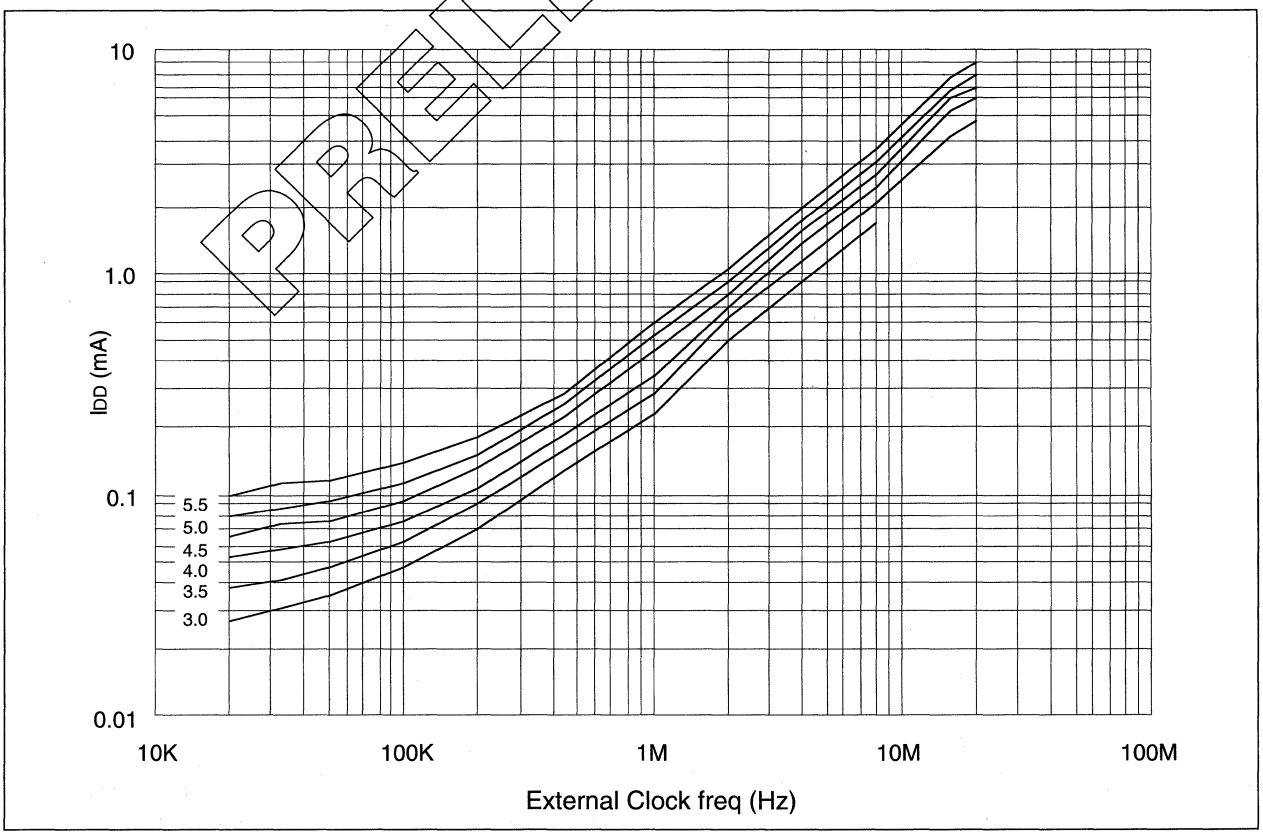


FIGURE 9.0.14 - WDT Timer Time-out Period vs VDD

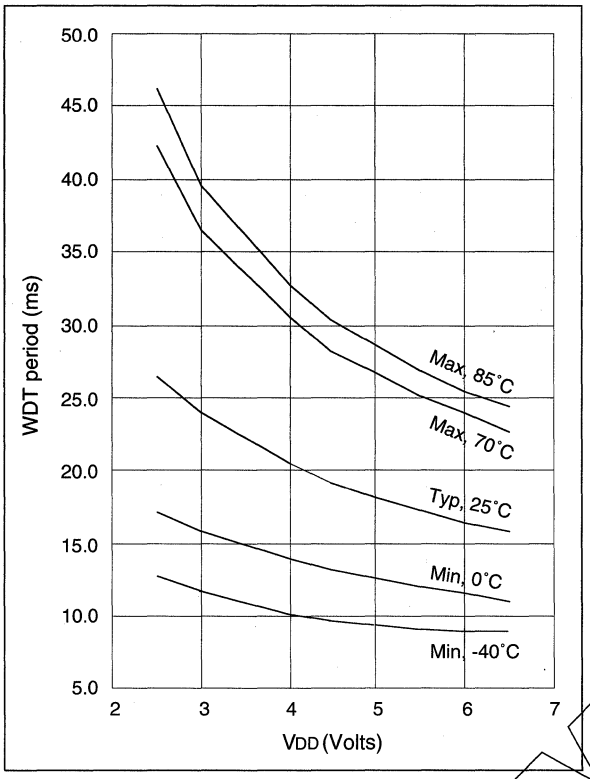


FIGURE 9.0.15 - Transconductance (gm) of HS Oscillator vs VDD

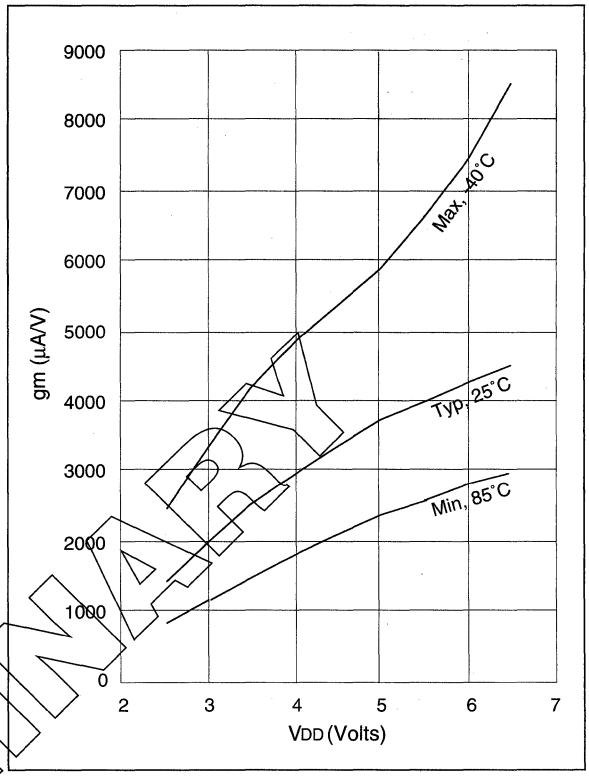


FIGURE 9.0.16 - Transconductance (gm) of LP Oscillator vs VDD

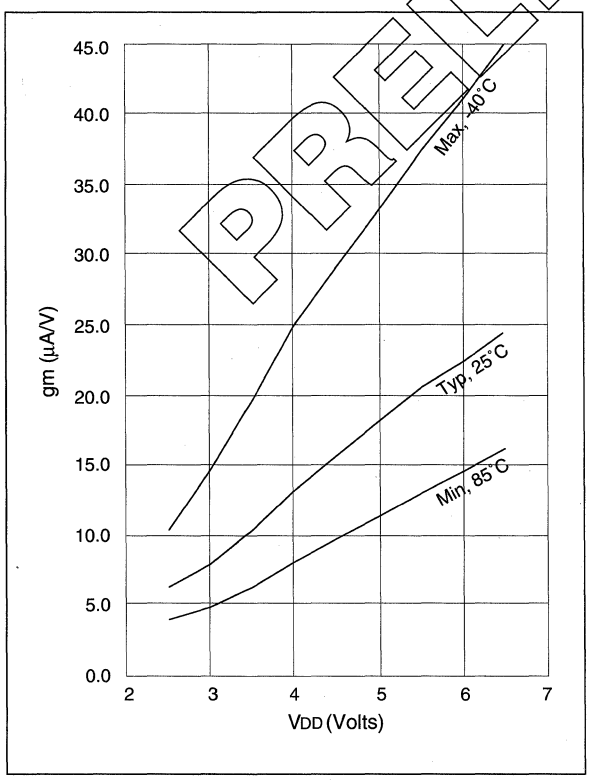
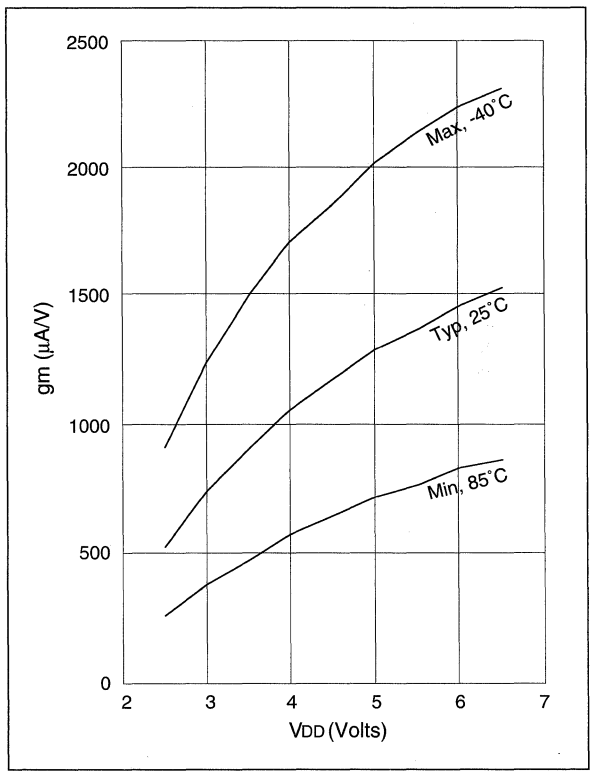


FIGURE 9.0.17 - Transconductance (gm) of XT Oscillator vs VDD



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.18 - IOH vs VOH, VDD = 3V

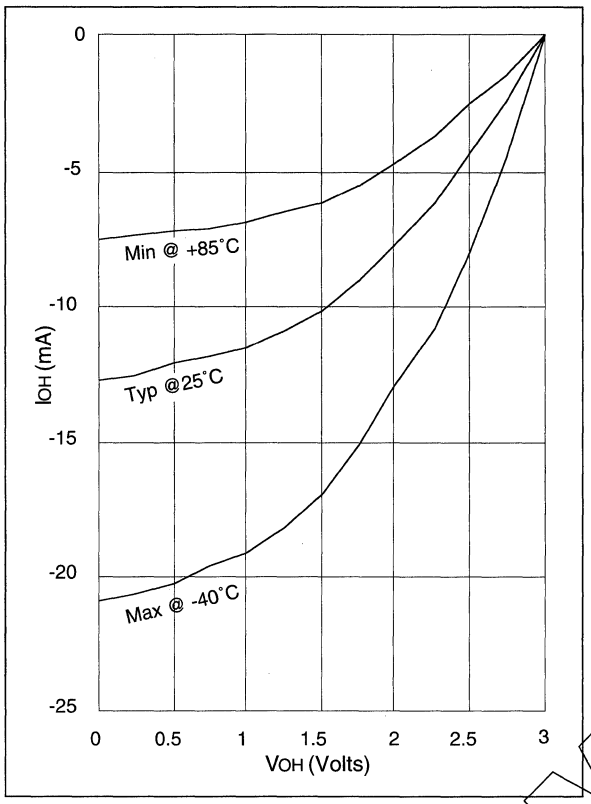


FIGURE 9.0.19 - IOH vs VOH, VDD = 5V

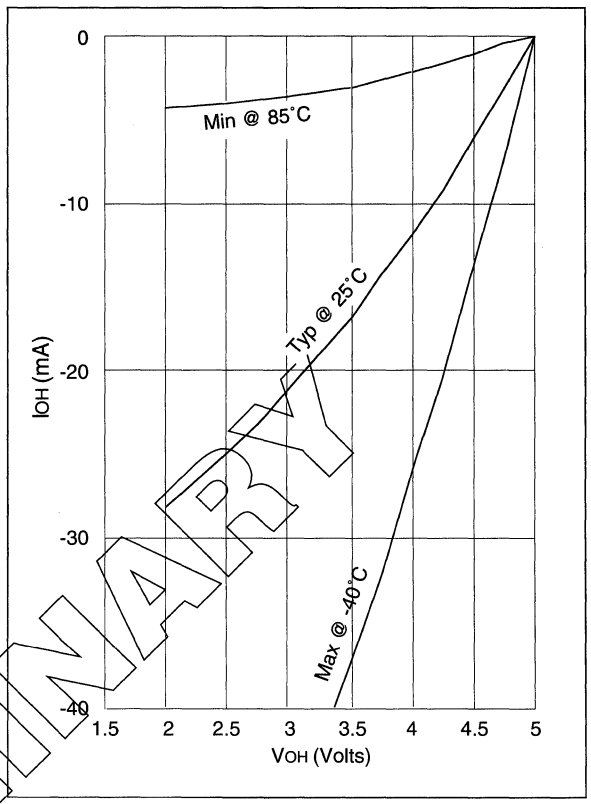


FIGURE 9.0.20 - IOL vs VOL, VDD = 3V

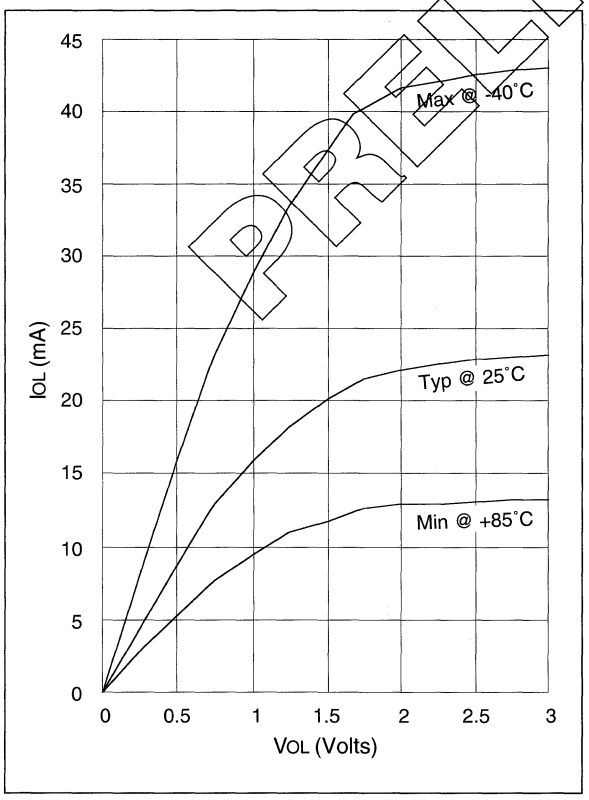
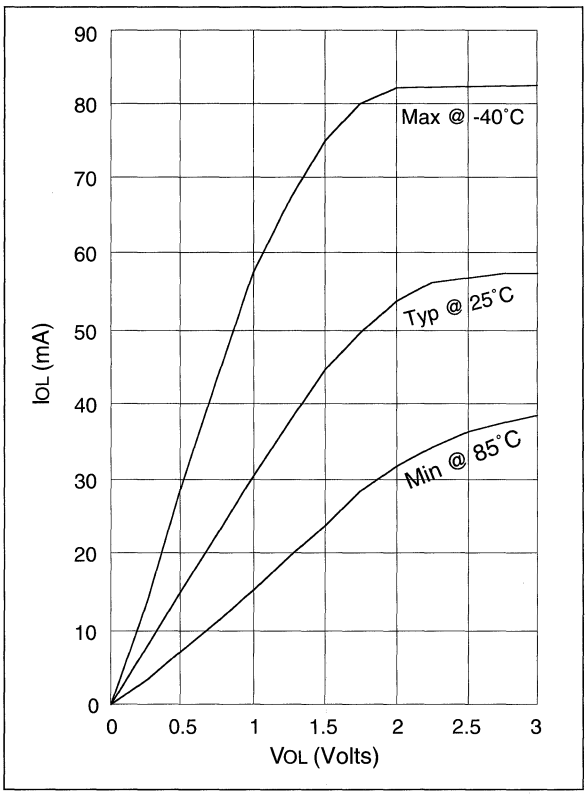


FIGURE 9.0.21 - IOL vs VOL, VDD = 5V



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

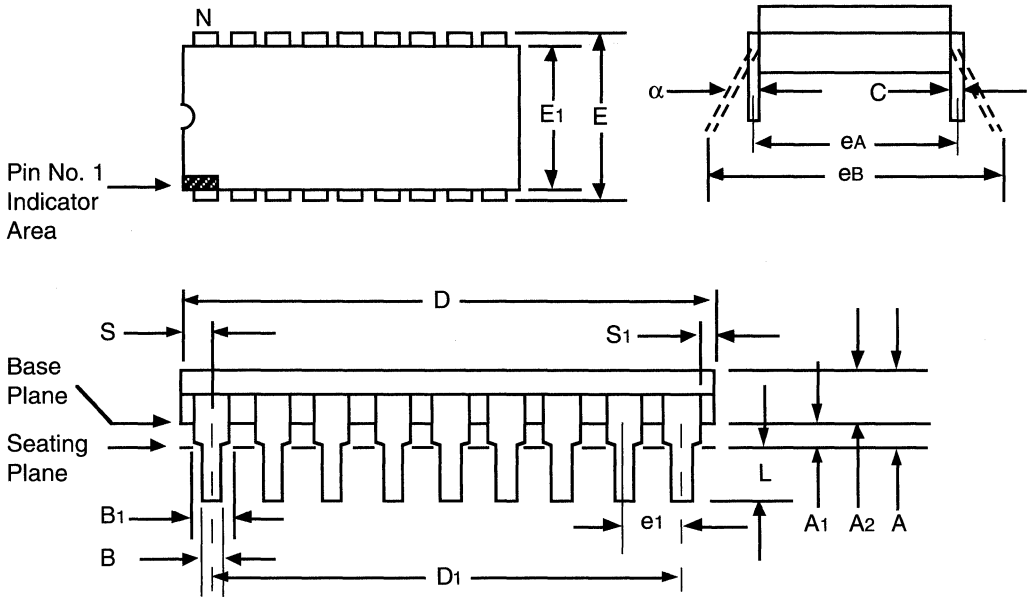
TABLE 9.0.2 - INPUT CAPACITANCE *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

10.0 PACKAGING DIAGRAMS AND DIMENSIONS

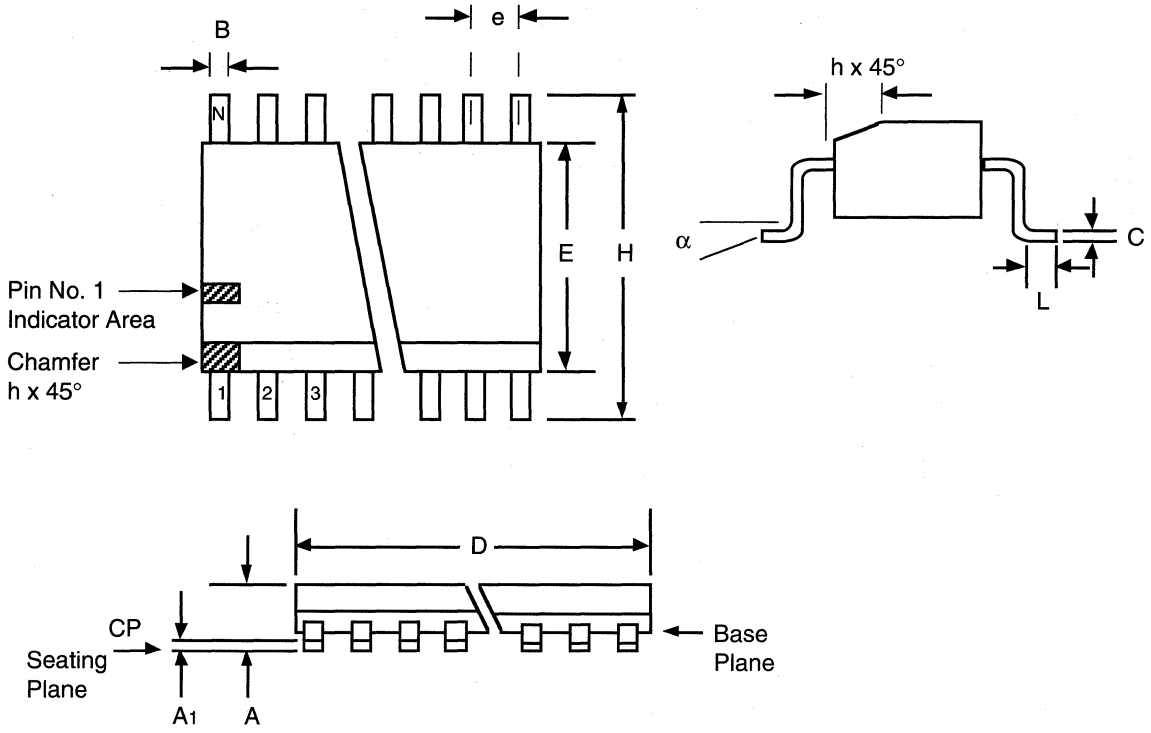
10.1 18-LEAD PLASTIC DUAL IN-LINE (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	**Reference**	0.800	0.800	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

10.2 18-LEAD PLASTIC SURFACE MOUNT (SOIC - WIDE, 300 mil BODY)

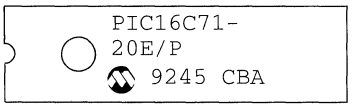


Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	**Typical**	0.050	0.050	**Typical**
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

10.3 PACKAGE MARKING INFORMATION

18L PDIP

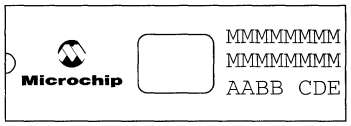
Example



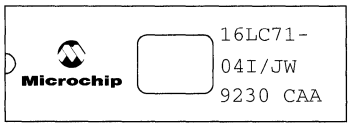
18L SOIC

Example

18L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

11.0 PROGRAMMING THE PIC16C71

The PIC16C71 is programmed using one of two methods, serial or parallel. The serial mode will allow the PIC16C71 to be programmed while in the users system using only five pins: VDD, VSS, MCLR/VPP, RB6 and RB7. This allows for increased design flexability. The parallel mode will provide faster programming as the data is loaded into the PIC16C71 with a greater throughput. Either mode may be selected at the start of the programming process. The parallel mode is intended for programmers. Only the "serial mode" is described here. You can get complete programming information in the PIC16C71 programming specification (DS30153).

11.1 Hardware Requirements

The PIC16C71 requires two programmable power supplies, one for VDD (4.5V to 5.5V) and one for VPP (VDD +4.5 to 14V). Both supplies should have a minimum resolution of 0.25V.

11.2 Programming Mode Entry

The programming mode for the PIC16C71 allows programming of user program memory, special locations used for ID, and the configuration fuses for the PIC16C71. This enters programming mode by raising MCLR/VPP from VIL to VIHH (high voltage) while keeping RB6 and RB7 pins at VIL.

11.3 User Program Memory Map

The user memory space extends from 0000h to 1FFFh (8K), of which 1K (0000h - 03FFh) is physically implemented. In actual implementation the on-chip user program memory is accessed by the lower 10 bits of the PC, with the upper 3 bits of the PC ignored. Therefore if the PC is greater than 3FFh, it will wrap around and address a location within the physically implemented memory.

In programming mode the program memory space extends from 0000h to 3FFFh, with the first half (0000h-1FFFh) being user program memory and the second half (2000h-3FFFh) being configuration memory. The PC will increment from 0000h to 1FFFh to 2000h to 3FFFh and wrap around to 2000h (not to 0000h). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program mode.

In the configuration memory space, 2000h-207Fh are utilized. When in configuration memory, as in the user memory, the 2000h-23FFh segment is repeatedly accessed as PC exceeds 23FFh.

11.4 Serial Program/Verify Operation

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled 6 times. Each command bit is latched on the falling edge of the clock with the least significant bit (lsb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time of 100ns with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1us between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output lsb first. Therefore, during a read operation the lsb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the lsb will be latched on the falling edge of the second cycle. A minimum 1us delay is also specified between consecutive commands.

The commands that are available are:

11.4.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000 hex. By then applying 16 cycles to the clock pin, the chip will load 14 bits in as the "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in figure 11.3.1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking MCLR low (Vil).

11.4.2 Load Data

After receiving this command, the chip will load in 14 bits as a "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in figure 11.4.2.2.

11.4.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedence) after the 16th rising edge. A timing diagram of this command is shown in figure 11.4.3.1.

11.4.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in figure 11.4.4.1.

FIGURE 11.3.1 - PROGRAM MEMORY MAPPING

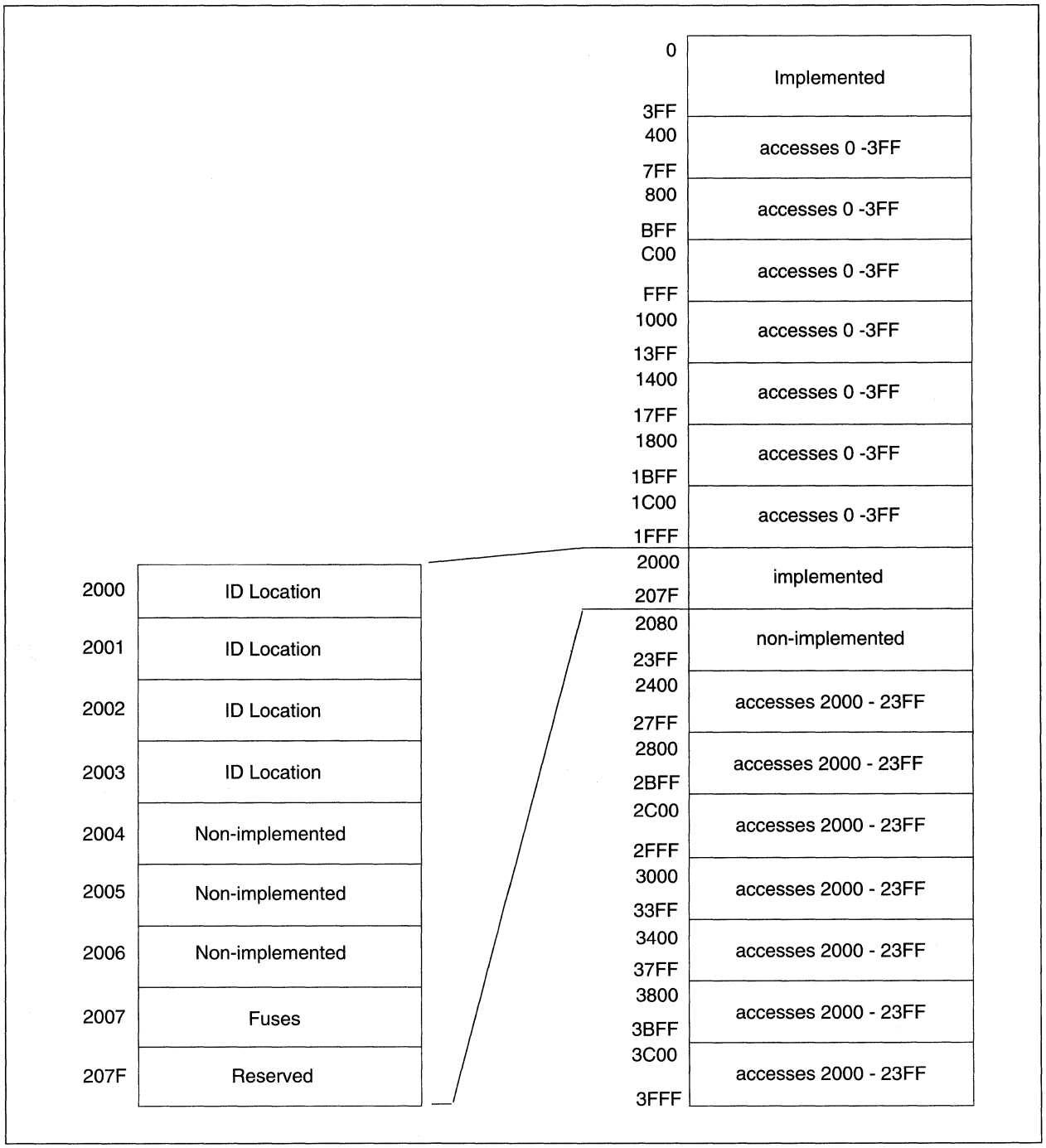


TABLE 11.4.1 - COMMAND MAPPING (SERIAL OPERATION)

Command	Mapping (msb ... lsb)	Data
Load Configuration	X X 0 0 0 X	0, data(14), 0
Load Data	X X 0 0 1 X	0, data(14), 0
Read Data	X X 0 1 0 X	0, data(14), 0
Increment Address	X X 0 1 1 X	
Begin programming	X X 1 0 0 X	
End Programming	X X 1 1 1 X	

FIGURE 11.4.2.2 - LOAD DATA COMMAND (SERIAL PROGRAM/VERIFY)

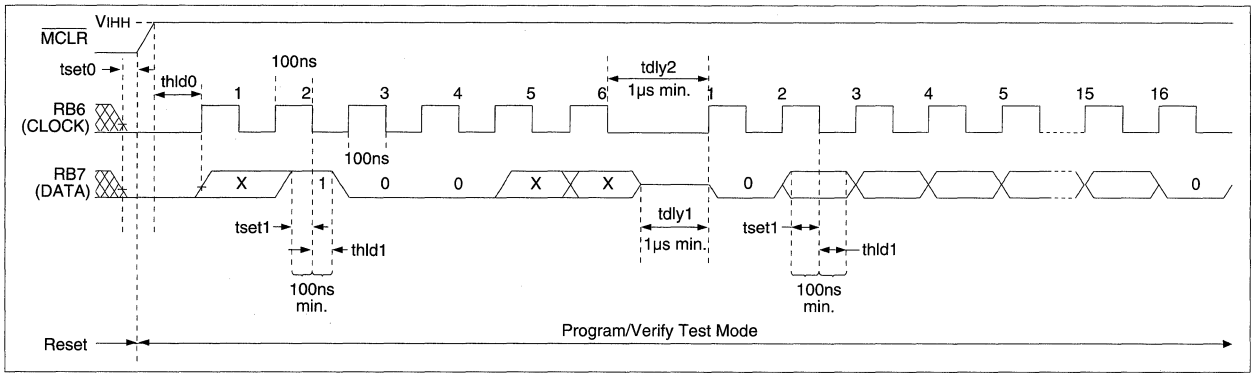


FIGURE 11.4.3.1 - READ DATA COMMAND (SERIAL PROGRAM/VERIFY)

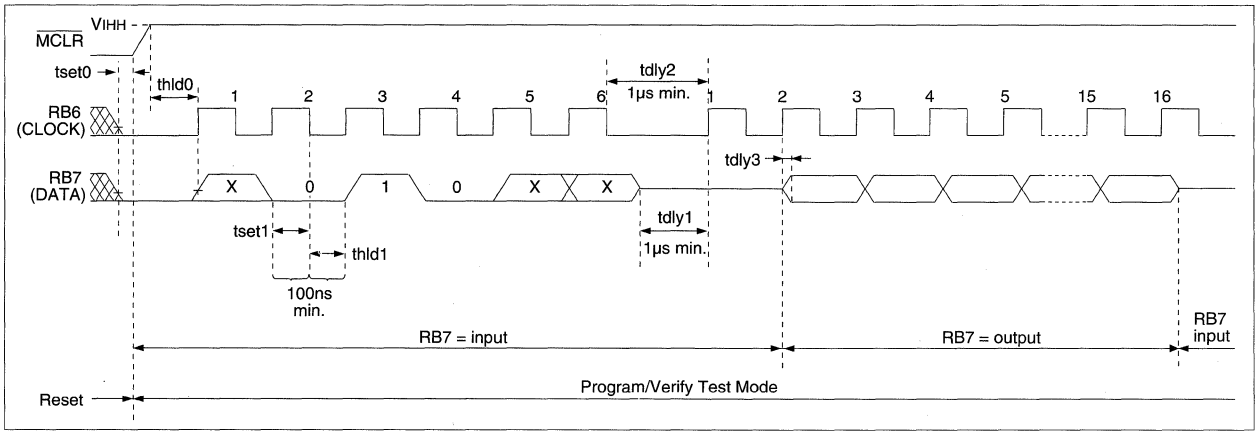
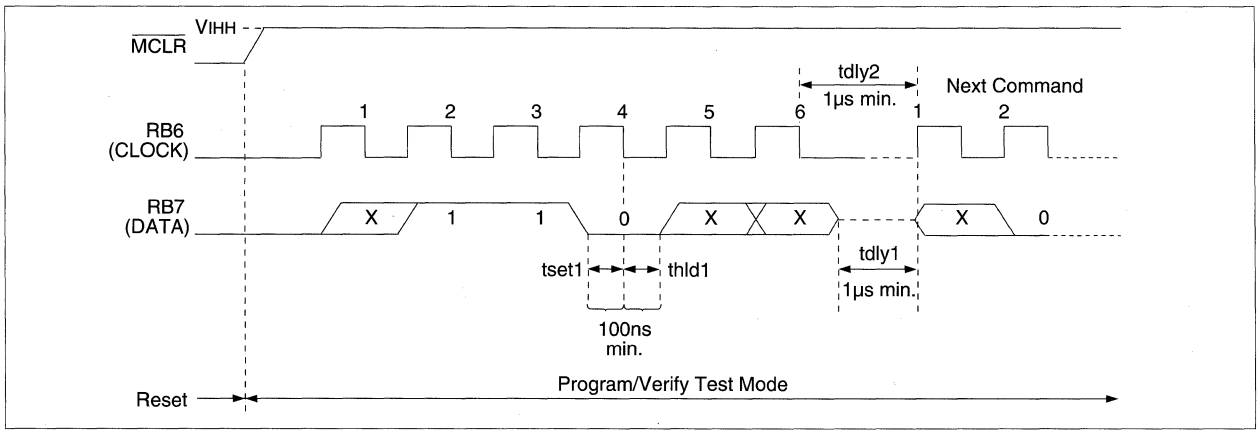


FIGURE 11.4.4.1 - INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



11.4.5 Begin Programming

A load command (load configuration or load data) must be given before the begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100 µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

11.4.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

All commands are transmitted lsb first. Data words are also transmitted lsb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1us is required between a command and a data word (or another command).

12.0 DEVELOPMENT SUPPORT

12.1 PICMASTER™: High Performance Universal In-Circuit Emulator System

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16CXX and PIC17CXX families. This system currently supports the PIC16CR54, PIC16C54, PIC16C55, PIC16C56 and PIC16C57, and PIC17C42 processors. PIC16C71 support is planned.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.0 environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a programmer unit and a macro assembler program.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an Electronic Bulletin Board System (EBBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

12.1.1 Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user.

To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.X system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

12.1.2 Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to an IBM PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

The Windows 3.X System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16Cxx processor and a PIC17Cxx processor).

FIGURE 12.1.1 - PICMASTER

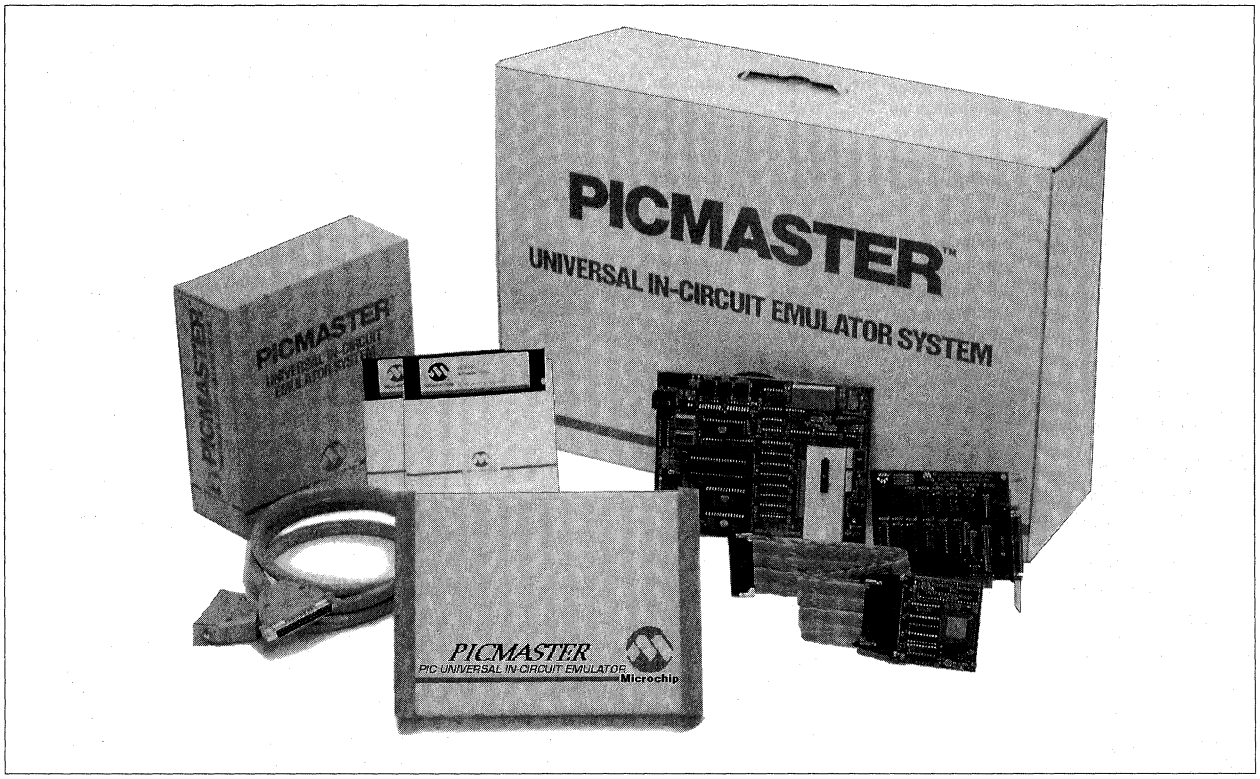


FIGURE 12.1.2 - PICMASTER SYSTEM CONFIGURATION

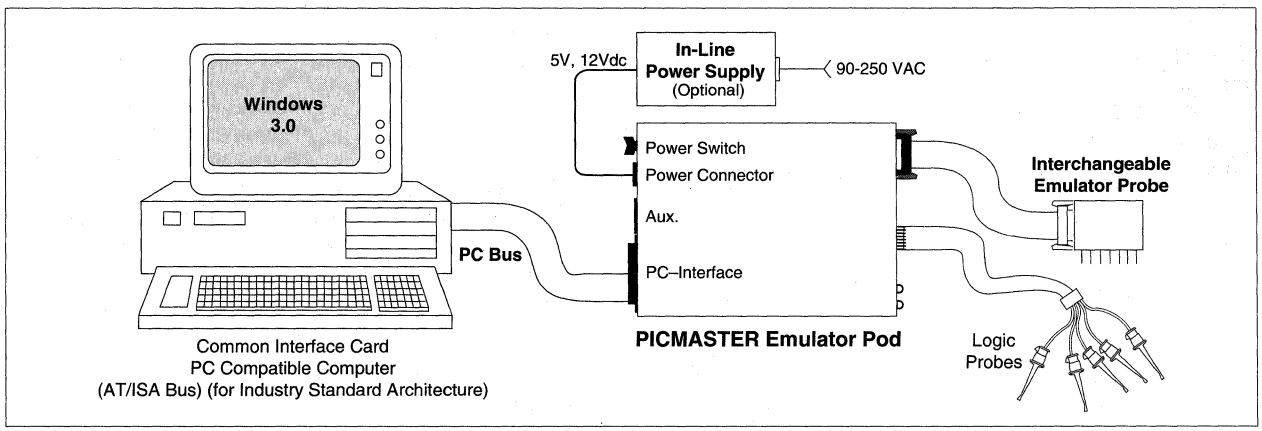
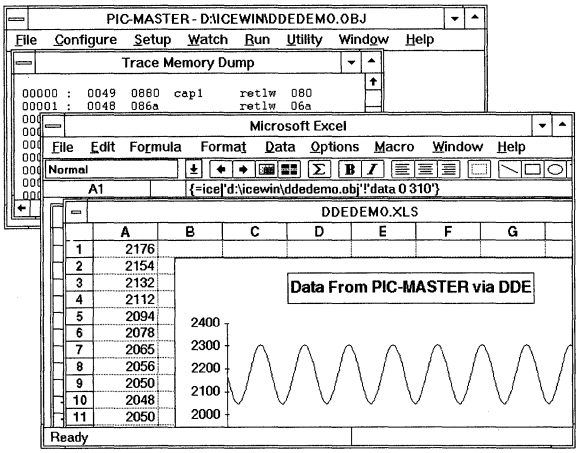


FIGURE 12.1.3 - PICMASTER TYPICAL SCREEN



12.2 PICALC Cross-Assembler

The PIC Cross Assembler PICALC is a PC hosted software development tool supporting the PIC16C5X series microcontrollers. PICALC offers a full featured Macro and Conditional assembly capability. It can also generate various object code formats including several Hex formats to support Microchip's proprietary development tools as well as third party tools. Also supports Hex (default), Decimal and Octal Source and listing formats. An assembler users manual is available for detailed support.

12.3 PRO MASTER™

The PRO MASTER programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MASTER has programmable VDD and VPP supplies which allows it to verify the PIC at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MASTER can read, verify or program a part. It can also set fuse configuration and code-protect in this mode. It's EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

In PC-hosted mode, the PRO MASTER connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MASTER has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. It is planned that the PRO MASTER will support all current and future PIC16CXX and PIC17CXX processors. Currently socket modules are available for the PIC16C54, PIC16C55, PIC16C56, PIC16C57, PIC17C42 and the PIC16C71.

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers oscillator start-up timer (OST) and power-up timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PortB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. Location 07h (PortC) is unimplemented and not a general purpose register.
15. FSR is made a full eight bit register.
16. "In system programming" is made possible. The user can program the PIC16C71 using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).

APPENDIX B

To convert code written for PIC16C5X to PIC16C71, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.
6. Note that location 07h is an unimplemented data memory location.

Notes:

Notes:

Notes:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. For the *currently available code-combinations*, refer to previous page.

PART NO. - XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank for OTP and Windowed Parts)	
Package:	P = PDIP	
	SO = SOIC (Gull Wing, 300 mil body)	
	JW = CERDIP Window	
Temperature Range:	- = 0°C to +70°C (T for tape/reel)	
	I = -40°C to +85°C (S for tape/reel)	
	E = -40°C to +125°C	
Frequency Range:	04 = 4 MHz	
	20 = 20 MHz	
Device:	PIC16C71 : VDD range 4.0V to 6.0V	
	PIC16LC71 : VDD range 3.0V to 6.0V	

Examples:

a) PIC16C71 - 04/P301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern # 301
b) PIC16LC71I - 04/SO = Industrial temp., SOIC package, 4 MHz, extended VDD limits
c) PIC16C71E - 20/P = Automotive temp., PDIP package, 20 MHz, normal VDD limits

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