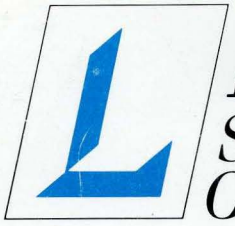


Lattice
Semiconductor
Corporation

GAL® DATA BOOK

High Performance
CMOS Reprogrammable Logic

Spring 1988

Dear Engineering Professional,

Thank you for your interest in Lattice's high performance GAL® (Generic Array Logic) products.

GAL® devices offer you high speed, low power and unprecedented levels of quality. Every GAL® device is **100%** tested before being shipped to customers --- saving your company the expense of programming fall-out and board level failures that are so common among other programmable logic technologies.

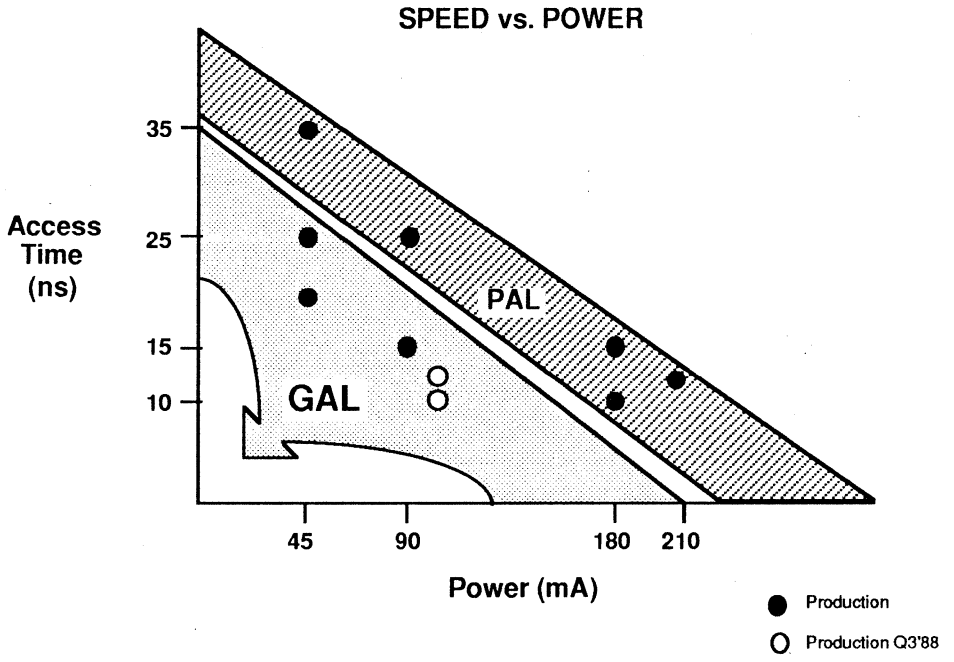
Going beyond high performance and high quality PLDs, Lattice is committed to developing more advanced and innovative GAL® products. Lattice's GAL®39V18, and ispGAL®16Z8 (capable of being reprogrammed "in-system") are the first in a series of advanced devices Lattice is introducing.

Thank you again for your interest. We look forward to helping you find solutions to your system performance requirements.

Sincerely,

Lattice Semiconductor

E²CMOS GAL .....



..... Beats Bipolar!!

Quarter Power GAL16V8Q and GAL20V8Q devices outperform the traditional Bipolar "A" PAL® device at 25% of the power!

	Quarter Power 25ns GAL Devices		15ns Half Power GAL Devices	
	MAX	TYP	MAX	TYP
tpd	25ns	17ns	15ns	12ns
tco	15ns	11ns	12ns	9ns
ICC	45mA	30mA	90mA	60mA

TABLE OF CONTENTS

E²CMOS Reprogrammable GENERIC ARRAY LOGIC

Definition of Datasheet Levels

Datasheet Identification	Product Status	Definition
Advanced	In Design	This datasheet contains advance information and specifications are subject to change without notice.
Preliminary	Sampling or Pre-Production	This datasheet contains preliminary data and supplementary data will be published at a later date. Lattice reserves the right to make changes at any time without notice.
No Identification	Full Production	This datasheet contains final specifications. Lattice reserves the right to make changes at any time without notice.

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FAX (503) 681-3037
TELEX 277338 LSC UR

Lattice Semiconductor Corporation

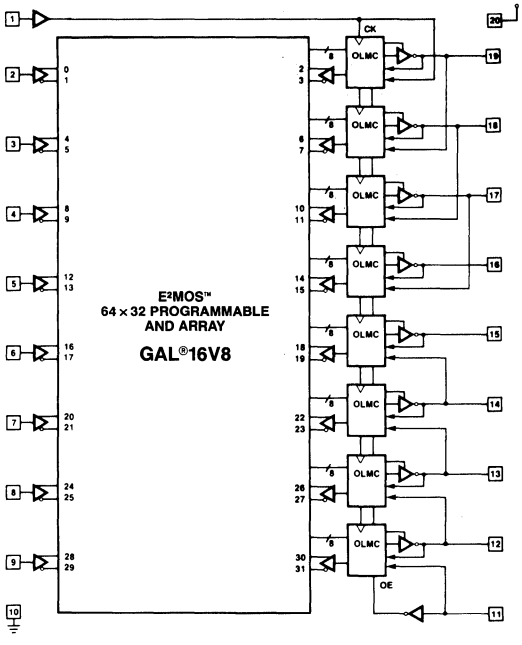
GAL® 16V8

GENERIC ARRAY LOGIC

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— Low Power: 45mA Max Active**
  - **— High Speed: 15ns Access Max**
    25ns Access Max
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **SECURITY CELL PREVENTS COPYING LOGIC**
- **DATA RETENTION EXCEEDS 20 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The LATTICE E²CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 20-pin GAL®16V8 features 8 programmable Output Logic Macrocells (OLMCs) allowing each output to be configured by the user. Additionally, the GAL®16V8 is capable of emulating, in a functional/fuse map/parametric compatible device, all common 20-pin PAL® device architectures.

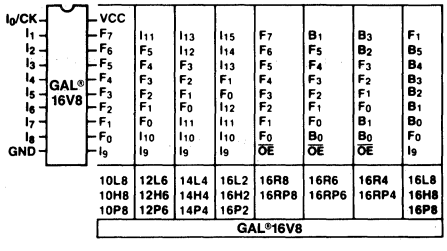
Programming is accomplished using readily available hardware and software tools. LATTICE guarantees a minimum 100 erase/write cycles and that data retention exceeds 20 years.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of the GAL® devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

PIN NAMES

I_0-I_{15}	INPUT	$\overline{OE}$	OUTPUT ENABLE
CK	CLOCK INPUT	V_{CC}	POWER (+5V)
B_0-B_5	BIDIRECTIONAL	GND	GROUND
F_0-F_7	OUTPUT		

GAL®16V8 EMULATING PAL® DEVICES



FEBRUARY, 1988

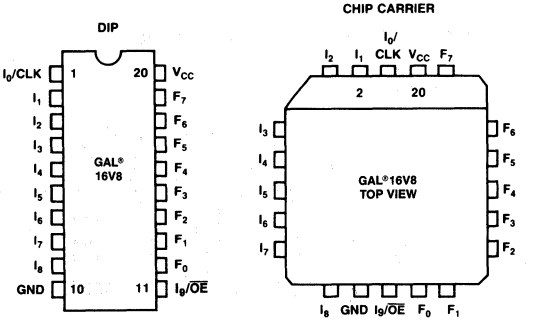
GAL® 16V8 HIGH PERFORMANCE E²CMOS™ GENERIC ARRAY LOGIC

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} . . . . . −.5 to +7V
Input voltage applied. . . . . −2.5 to V_{CC} +1.0V
Off-state output voltage applied . . −2.5 to V_{CC} +1.0V
Storage temperature. . . . . −65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

PIN CONFIGURATION



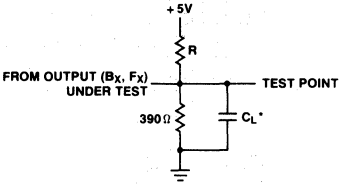
OPERATING RANGE

SYMBOL	PARAMETER	TEMPERATURE RANGE									UNIT
		MILITARY			INDUSTRIAL			COMMERCIAL			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	V
T_A	Ambient temperature				−40		85	0		75	°C
T_C	Case temperature	−55		125							°C

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.



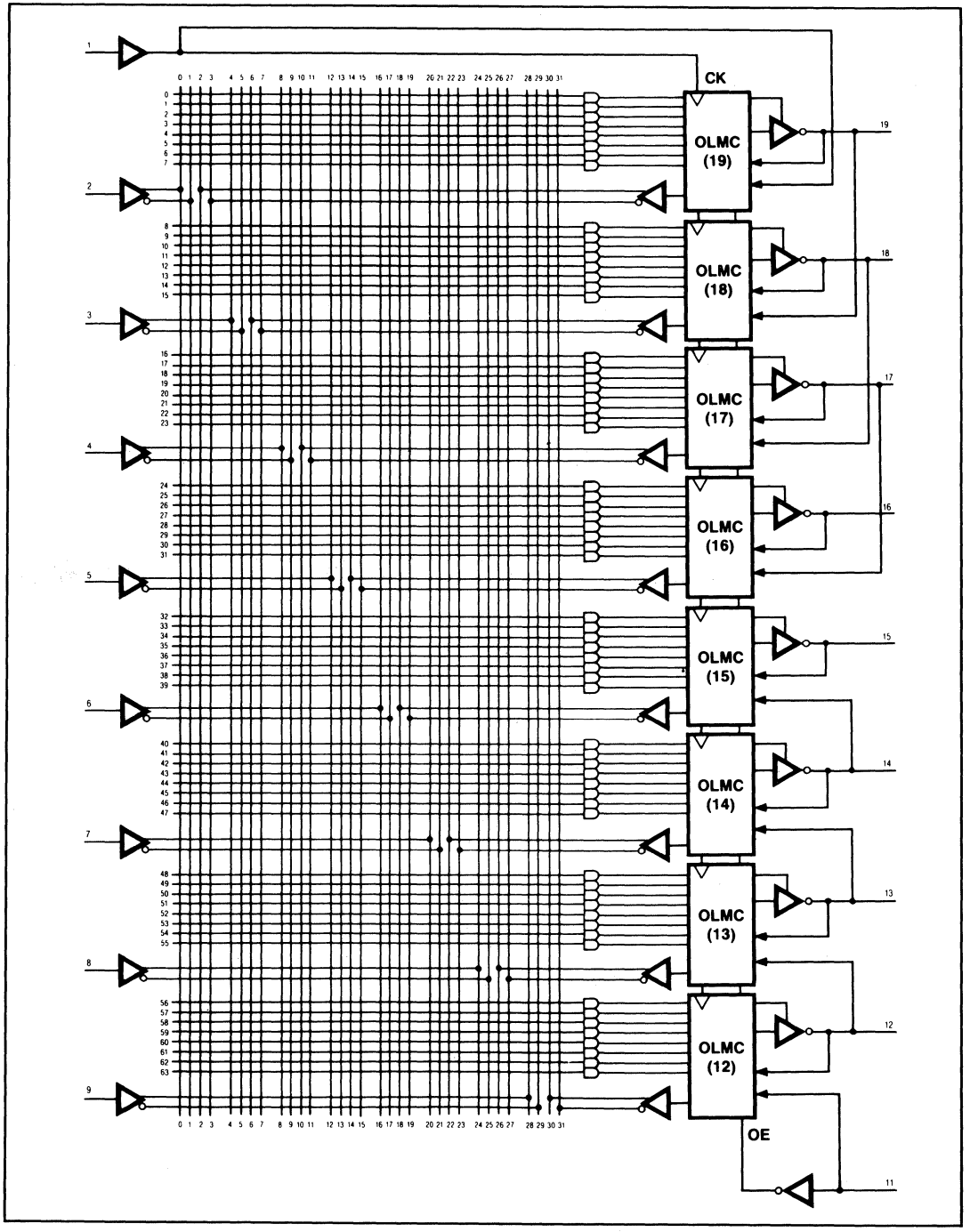
*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = 2.0V
C_B	Bidirectional Pin Cap	15	pF	V_{CC} = 5.0V, V_B = 2.0V

*Guaranteed but not 100% tested.

GAL®16V8 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS

QUARTER POWER GAL®16V8

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz $V_{CC} = V_{CC}$ MAX		COM'L	—	45	mA
				MIL/IND	—	55	mA
I_{OS}[1]	Output Short Circuit	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} MIN	I_{OL} = 24mA	COM/IND	—	0.5	V
			I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} = V_{CC} MIN	I_{OH} = −3.2mA	COM/IND	2.4	—	V
			I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

HALF POWER GAL®16V8

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz $V_{CC} = V_{CC}$ MAX		COM'L	—	90	mA
				MIL/IND	—	110	mA
I_{OS}[1]	Output Short Circuit	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} MIN	I_{OL} = 24mA	COM/IND	—	0.5	V
			I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} = V_{CC} MIN	I_{OH} = −3.2mA	COM/IND	2.4	—	V
			I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

[1]One output at a time for a maximum duration of one second.

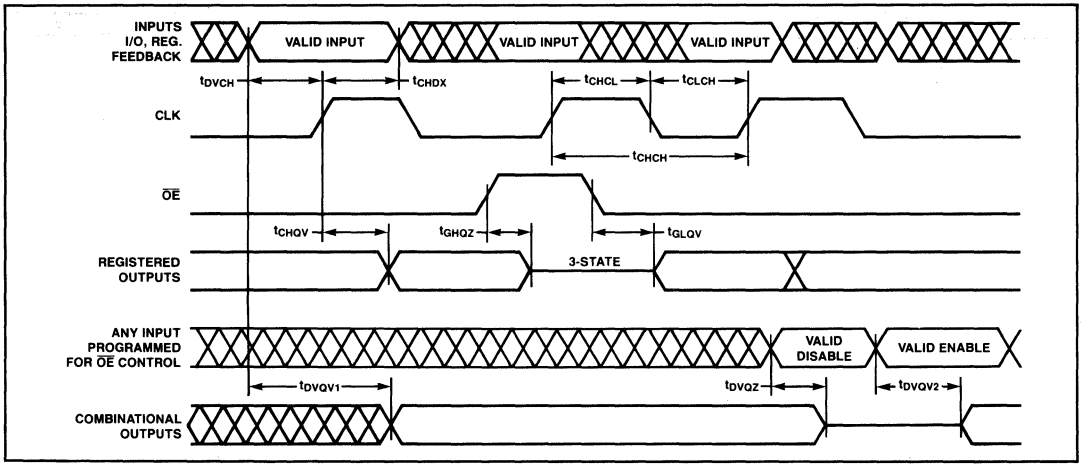
SWITCHING CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL	PARAMETER		TEMPERATURE RANGE: COMMERCIAL/INDUSTRIAL — GAL®16V8-15 MIN	GAL®16V8-15 MAX	GAL®16V8-25 MIN	GAL®16V8-25 MAX	GAL®16V8-20 MIN	GAL®16V8-20 MAX	TEMPERATURE RANGE: MILITARY — GAL®16V8-30 MIN	GAL®16V8-30 MAX	UNITS	TEST CONDITIONS[1] R(Ω)	TEST CONDITIONS[1] C_L(pF)
T_{DVQV1}	Delay from Input to Active Output		—	15	—	25	—	20	—	30	ns	200	50
T_{DVQV2}	Product Term Enable Access Time to Active Output		—	15	—	25	—	20	—	30	ns	Active High R = ∞ Active Low R = 200	50
T_{DVQZ2}	Product Term Disable to Output Off		—	15	—	25	—	20	—	30	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GHQZ2}	$\overline{OE}$ (Output Enable) High to Outputs Off		—	15	—	20	—	18	—	25	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GLQV}	$\overline{OE}$ (Output Enable) Access Time		—	15	—	20	—	18	—	25	ns	Active High R = ∞ Active Low R = 200	50
T_{CHQV}	Clock High to Output Valid Access Time		—	12	—	15	—	15	—	20	ns	200	50
T_{DVCH}	Input or Feedback Data Setup Time		12	—	20	—	15	—	25	—	ns	—	—
T_{CHDX}	Input or Feedback Data Hold Time		0	—	0	—	0	—	0	—	ns	—	—
T_{CHCH} T_{CHCL} T_{CLCH}	Clock Period (T_{DVCH} + T_{CHQV}) Clock Width High Clock Width Low		24 10 10	— — —	35 15 15	— — —	30 12 12	— — —	45 15 15	— — —	ns ns ns	—	—
f_{MAX}	Maximum Frequency	Feedback	41.6		28.5		33.3		22.2		MHz	200	50
		No Feedback	50.0		33.3		41.6		33.3				

[1] Refer also to AC test conditions.

[2] 3-State levels are measured 0.5V from steady-state active level.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL (OLMC)

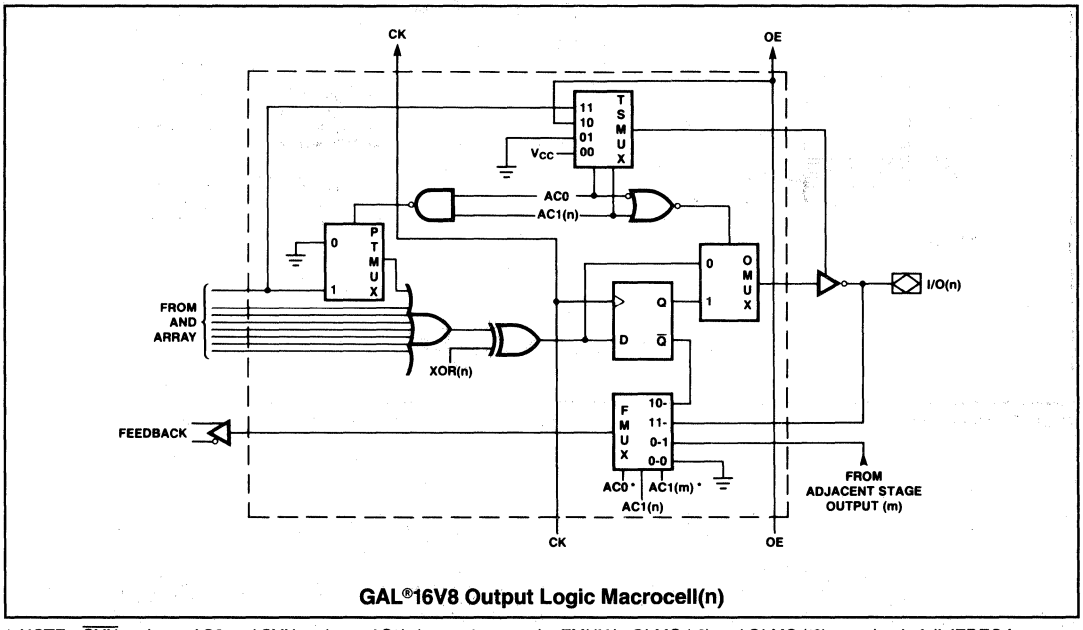
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable can be connected to all outputs, or separate inputs or product terms can be used to provide individual output enable controls. The output logic macrocell provides the designer with maximal output flexibility in matching signal requirements, thus providing more functions than possible with existing 20-pin PAL® devices.

The various configurations of the output logic macrocell are controlled by programming certain cells (SYN, AC0, AC1(n), and the XOR(n) polarity bits) within the 82-bit architecture control word. The SYN bit determines whether or not a device will have registered output capability or will have purely combinational outputs. It also replaces the AC0 bit in the two outermost macrocells, OLMC (12) and OLMC (19). When first setting up the device architecture, this is the first bit to choose.

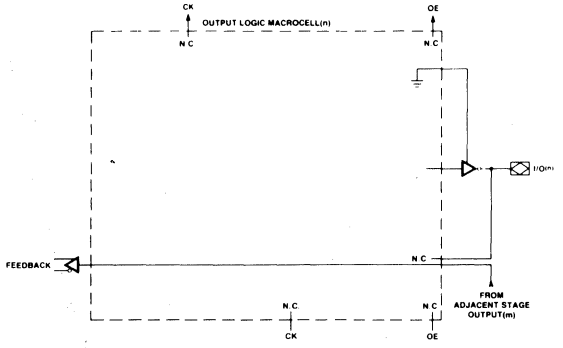
Architecture control bit AC0 and the eight AC1(n) bits direct the outputs to be wired always on, always off (as an input), have common $\overline{OE}$ control (pin 11), or to be three-state controlled separately from a product term. The architecture control bits also determine the source of the array feedback term through the FMUX, and select either combinational or registered outputs.

The five valid macrocell configurations are shown in each of the macrocell equivalent diagrams. In all cases, the eight XOR(n) bits individually determine each output's polarity. The truth table associated with each diagram shows the bit values of the SYN, AC0, and AC1(n) that set the macrocell to the configuration shown.



GAL®16V8 Output Logic Macrocell(n)

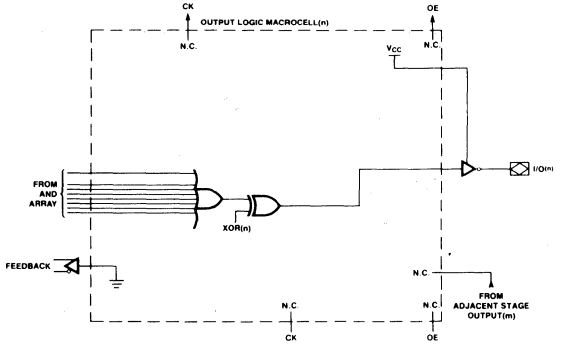
* NOTE—$\overline{SYN}$ replaces AC0 and SYN replaces AC1(m) as an input to the FMUX in OLMC (12) and OLMC (19) to maintain full JEDEC fuse map compatibility with PAL® type device architectures.



SYN	AC0	AC1(n)	FUNCTION
1	0	1	INPUT MODE (i.e. 12L6, 14P4)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
THE OUTPUT BUFFER IS DISABLED.

Dedicated Input Mode



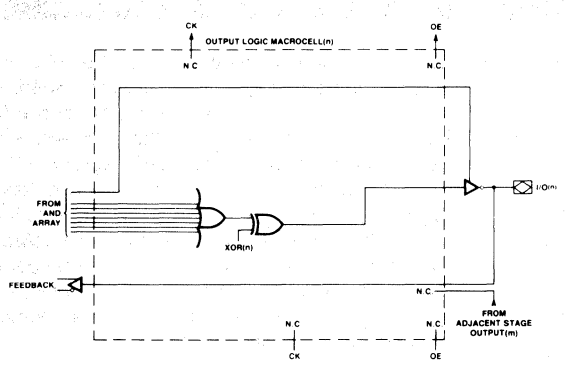
SYN	AC0	AC1(n)	FUNCTION
1	0	0	ALL OUTPUTS COMBINATIONAL (i.e. 10L8, 12H6)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
ALL OUTPUTS ARE COMBINATIONAL AND ALWAYS ACTIVE.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Dedicated Combinational Output

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

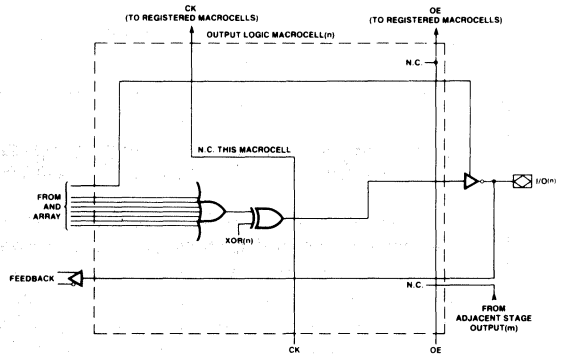


SYN	AC0	AC1(n)	FUNCTION
1	1	1	ALL OUTPUTS COMBINATIONAL (i.e. 16L8, 16H8)

IN THIS ARCHITECTURE MODE, PINS 1 AND 11 ARE DATA INPUTS. ALL OUTPUTS ARE COMBINATIONAL.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Combinational Output

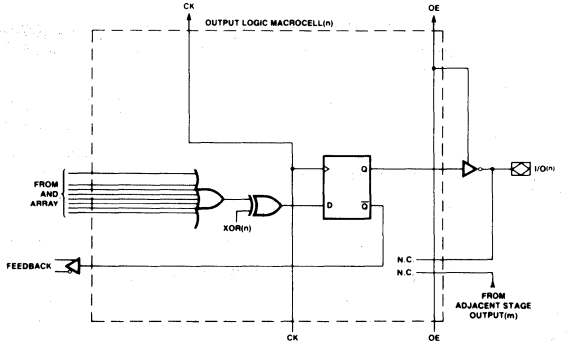


SYN	AC0	AC1(n)	FUNCTION
0	1	1	COMBINATIONAL OUTPUT IN A REGISTERED DEVICE

IN THIS ARCHITECTURE MODE, PIN 1 = CK, PIN 11 = $\overline{OE}$. THIS MACROCELL IS COMBINATIONAL, BUT AT LEAST ONE OF THE OTHERS IS REGISTERED OUTPUT.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Combinational Output in a Registered Device



SYN	AC0	AC1(n)	FUNCTION
0	1	0	OUTPUT REGISTERED (i.e. 16R8)

IN THIS ARCHITECTURE MODE, PIN 1 = CK, PIN 11 = $\overline{OE}$.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Registered Active High or Low Output

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ROW ADDRESS MAP DESCRIPTION

Figure 1 shows a block diagram of the row address map. There are a total of 36 unique row addresses available to the user when programming the GAL®16V8 devices. Row addresses 0–31 each contain 64 bits of input term data. This is the user array where the custom logic pattern is programmed. Row 32 is the electronic signature word. It has 64 bits available for any user-defined purpose. Rows 33–59 are reserved by the manufacturer and are not available to users.

Row 60 contains the architecture and output polarity information. The 82 bits within this word are programmed to configure the device for a specific application. Row 61 contains a one bit security cell that when programmed prevents further programming verification of the array. Row 63 is the row that is addressed to perform a bulk erase of the device, resetting it back to a virgin state. Each of these functions is described in the following sections.

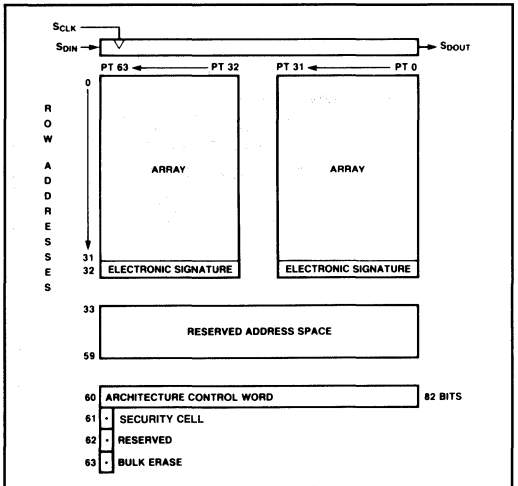


Figure 1. GAL®16V8 Row Address Map Block Diagram

ELECTRONIC SIGNATURE WORD

An electronic signature word is provided with every GAL®16V8 device. It resides at row address 32 and contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

ARCHITECTURE CONTROL WORD

All of the various configurations of the GAL®16V8 devices are controlled by programming cells within the 82-bit architecture control word that resides at row 60. The location of specific bits within the architecture control word is shown in the control word diagram in Figure 2. The function of the SYN, AC0 and AC1(n) bits have been explained in the output logic macrocell description. The eight polarity bits determine each output's polarity individually by selectively correct logic. The numbers below the XOR(n) and AC1(n) bits in the architecture control word diagram shows the output device pin number that the polarity bits control.

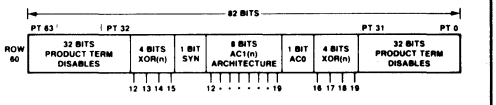


Figure 2. GAL®16V8 Architecture Control Word Diagram

SECURITY CELL

Row address 61 contains the security cell (one bit). The security cell is provided on all GAL®16V8 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array (rows 0–31). The cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Signature data is **always** available to the user.

BULK ERASE MODE

By addressing row 63 during a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its virgin state.

Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL®16V8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. Figure 3 shows the pin functions necessary to preload the registers. The register preload timing and pin voltage levels necessary to perform the function are shown below. This test mode is ntered by raising PRLD to V_{IES}, which enables the serial data in (S_{DIN}) buffer and the serial data out (S_{DOUT}) buffer. Data is then serially shifted into the registers on each rising edge of the clock, DCLK. Only the macrocells with registered output configurations are loaded. If only 3 outputs have registers, then only 3 bits need be shifted in. The registers are loaded from the bottom up, as shown in Figure 3.

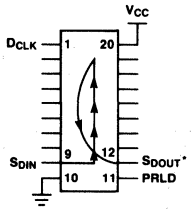


Figure 3. Output Register Preload Pinout

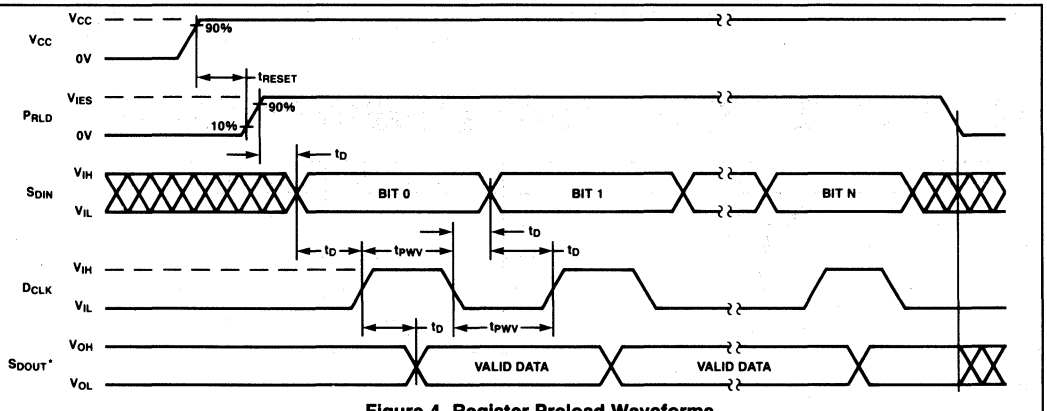


Figure 4. Register Preload Waveforms

Note: The S_{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V_{CC} with a 10K Ω resistor.

LATCH-UP PROTECTION

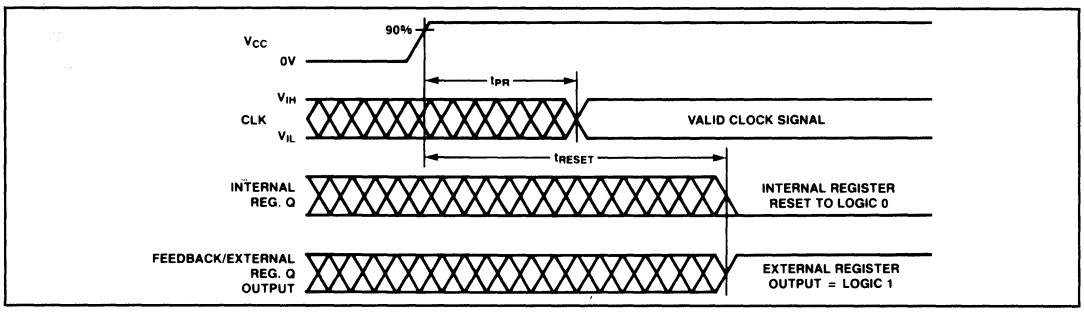
GAL® devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL® devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL® devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and 3-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL®16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

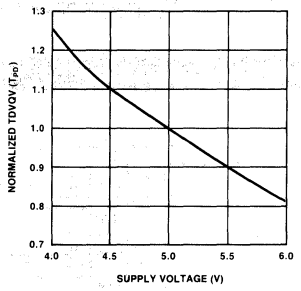
The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL®16V8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL®16V8 TEST PARAMETRIC SPECIFICATIONS

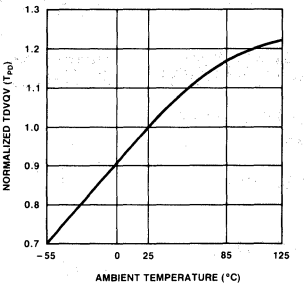
SYMBOL	PARAMETER	MIN.	TYP	MAX	UNITS
V_{IH}	Input Voltage (High)	2.40	—	V_{CC}	V
V_{IL}	Input Voltage (Low)	0.00	—	0.50	V
V_{IES}	Register Preload Input Voltage	14.5	15	15.5	V
V_{OH}*	Output Voltage (High)*	2.40	—	V_{CC}	V
V_{OL}*	Output Voltage (Low)*	0.00	—	0.50	V
I_{IH}, I_{IL}	Input Current	—	±1	±10	μA
t_{PWV}	Verify Pulse Width	1	5	10	μS
t_D	Pulse Sequence Delay	1	5	10	μS
t_{PR}	Reset Circuit Power-Up	—		100	nS
t_{RESET}	Register Reset Time From Valid V_{CC}	—		45	μS

*NOTE—The S_{DOUT} output buffer is an open drain output. This pin should be terminated to V_{CC} with a 10K resistor.

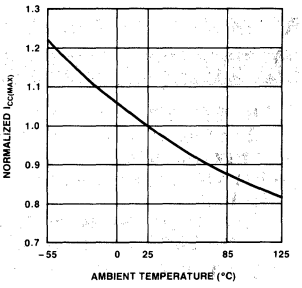
NORMALIZED TDVQV (T_{PD}) VS. SUPPLY VOLTAGE



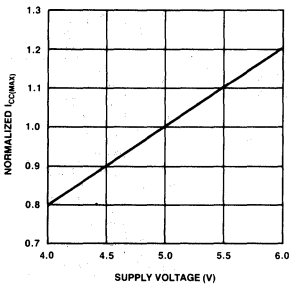
NORMALIZED TDVQV (T_{PD}) VS TEMPERATURE



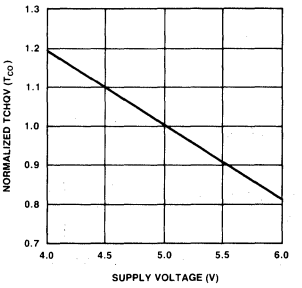
NORMALIZED $I_{CC(MAX)}$ VS. TEMPERATURE



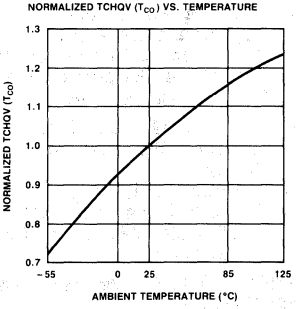
NORMALIZED $I_{CC(MAX)}$ VS. SUPPLY VOLTAGE



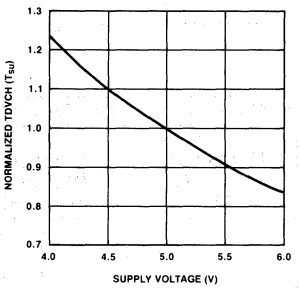
NORMALIZED TCHQV (T_{CO}) VS. SUPPLY VOLTAGE



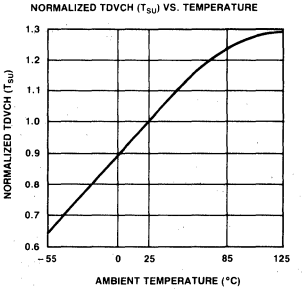
NORMALIZED TCHQV (T_{CO}) VS. TEMPERATURE



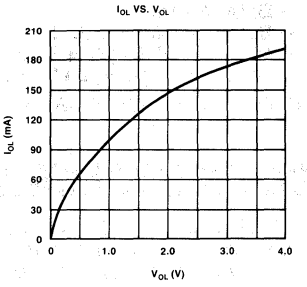
NORMALIZED TDVCH (T_{SU}) VS. SUPPLY VOLTAGE



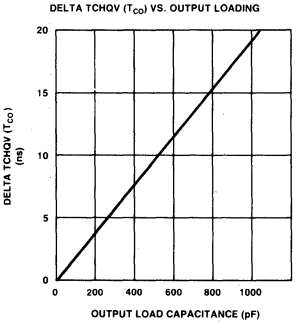
NORMALIZED TDVCH (T_{SU}) VS. TEMPERATURE



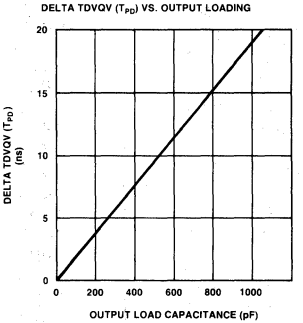
I_{OL} VS. V_{OL}



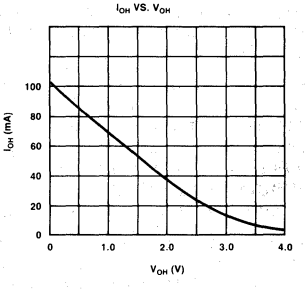
DELTA TCHQV (T_{CO}) VS. OUTPUT LOADING



DELTA TDVQV (T_{PD}) VS. OUTPUT LOADING



I_{OH} VS. V_{OH}



Lattice Semiconductor Corporation

GAL® 16V8A

ULTRA HIGH SPEED E²CMOS™
GENERIC ARRAY LOGIC

PRELIMINARY INFORMATION

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 24 mA Outputs**
  - **— UltraMOS® III Advanced CMOS Technology**
- **50% REDUCTION IN POWER**
  - **— 90ma Typ I_{CC}**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (< 50ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin 'D'PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

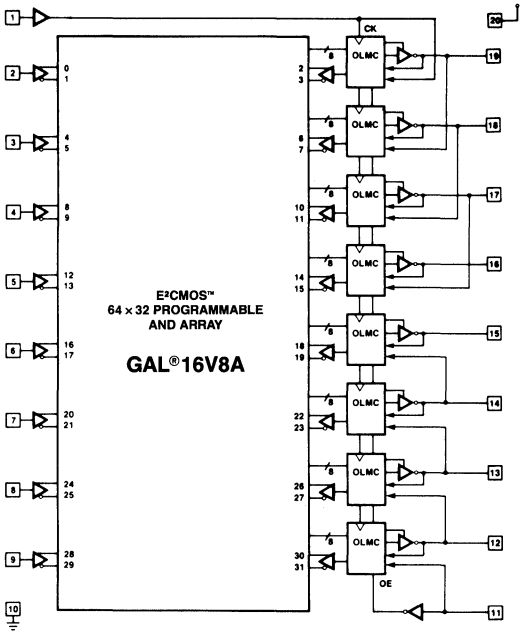
DESCRIPTION

The GAL®16V8A-12, at 12 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL®16V8A-12 to consume just 90ma typical I_{CC} which represents a 50% savings in power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing each Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL®16V8A are the PAL® architectures listed in the table on the right. The GAL®16V8A is capable of emulating any of these PAL® architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/write cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



GAL®/PAL® COMPARISON—10/12/15 ns DEVICES

PART TYPE	GAL®16V8A ARCHITECTURE EMULATION 90ma	PAL®16xx AVAILABILITY 90ma	PAL®16xx AVAILABILITY 180ma
16L8	✓		✓
16H8	✓		
16R8	✓		✓
16R6	✓		✓
16R4	✓		✓
16P8	✓		
16RP8	✓		
16RP6	✓		
16RP4	✓		
10L8	✓		
12L6	✓		
14L4	✓		
16L2	✓		
10H8	✓		
12H6	✓		
14H4	✓		
16H2	✓		
10P8	✓		
12P6	✓		
14P4	✓		
16P2	✓		
16V8	✓		

FEBRUARY, 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OREGON 97208

APPLICATIONS HOTLINE: 1-800-FASTGAL

GAL® 16V8A
ULTRA HIGH SPEED E²CMOS™
GENERIC ARRAY LOGIC

SWITCHING CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL				UNITS	TEST CONDITIONS	
			GAL®16V8A-12		GAL®16V8A-10				
			MIN.	MAX.	MIN.	MAX.		R(Ω)	C_L(pF)
T_{DVQV1}	Delay from Input to Active Output		—	12	—	10	ns	200	50
T_{DVQV2}	Product Term Enable Access Time to Active Output		—	12	—	10	ns	Active High R = ∞ Active Low R = 200	50
T_{DVQZ}[1]	Product Term Disable to Output Off		—	12	—	10	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GHQZ}[1]	$\overline{OE}$ (Output Enable) High to Outputs Off		—	10	—	10	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GLQV}	$\overline{OE}$ (Output Enable) Access Time		—	10	—	10	ns	Active High R = ∞ Active Low = 200	50
T_{CHQV}	Clock High to Output Valid Access Time		—	10	—	8	ns	200	50
T_{DVCH}	Input or Feedback Data Setup Time		12	—	10	—	ns	—	—
T_{CHDX}	Input or Feedback Data Hold Time		0	—	0	—	ns	—	—
T_{CHCH} T_{CHCL} T_{CLCH}	Clock Period (T_{DVCH} + T_{CHQV}) Clock Width High Clock Width Low		22 8 8	— — —	18 8 8	— — —	ns ns ns	—	—
f_{MAX}	Maximum Frequency	Feedback	45.5		55.5				
		No Feedback	62.5		62.5				

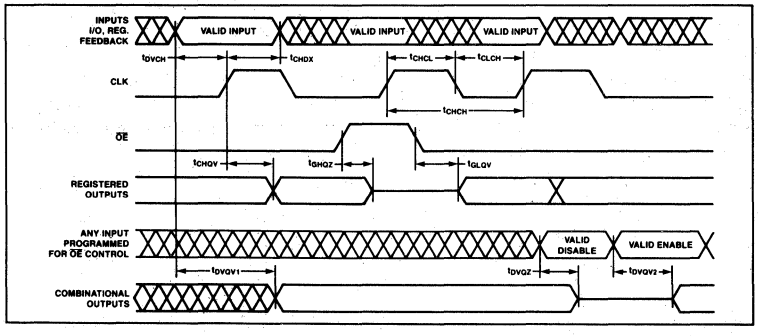
[1] 3-State levels are measured 0.5V from steady-state active level.

ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS (HALF-POWER)

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	GND ≤ V_{IN} < V_{CC} MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	GND ≤ V_{IN} < V_{CC} MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz		COM'L	—	115	mA
		V_{CC} = V_{CC} MAX		MIL	—	140	mA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} =	I_{OL} = 24mA	COM'L	—	0.5	V
		V_{CC} MIN	I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} =	I_{OH} = −3.2mA	COM'L	2.4	—	V
		V_{CC} MIN	I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

NOTE: For detailed technology, logic, timing, programming information and specifications, refer to the GAL16V8 datasheet.

SWITCHING WAVEFORMS



Lattice Semiconductor Corporation

GAL®20V8

GENERIC ARRAY LOGIC

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— Low Power: 45mA Max Active**
  - **— High Speed: 15ns Access Max**
    25ns Access Max
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **SECURITY CELL PREVENTS COPYING LOGIC**
- **DATA RETENTION EXCEEDS 20 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

DESCRIPTION

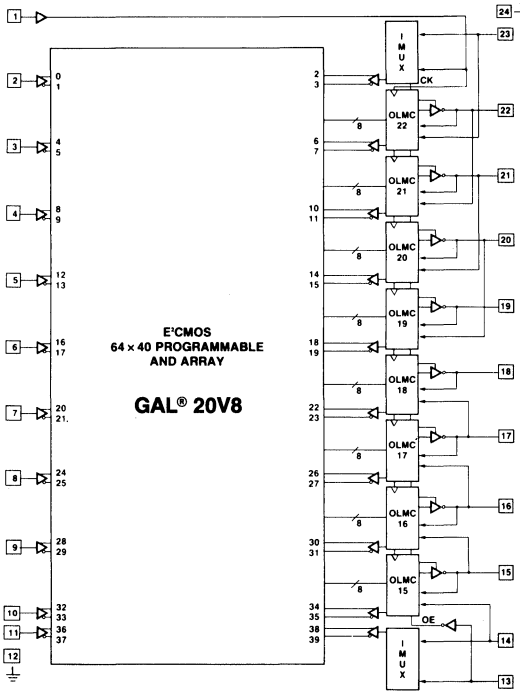
The LATTICE E²CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL®20V8 features 8 programmable Output Logic Macrocells (OLMCs) allowing each output to be configured by the user. Additionally, the GAL®20V8 is capable of emulating, in a functional/fuse map/parametric compatible device, all common 24-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. LATTICE guarantees a minimum 100 erase/write cycles and that data retention exceeds 20 years.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of the GAL® devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

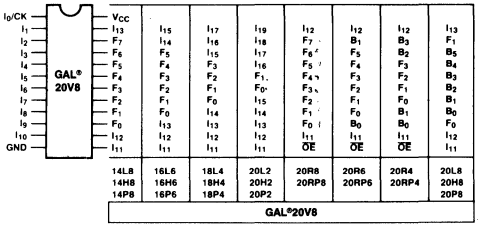
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I_0-I_{19}	INPUT	$\overline{OE}$	OUTPUT ENABLE
CK	CLOCK INPUT	V_{CC}	POWER (+5V)
B_0-B_5	BIDIRECTIONAL	GND	GROUND
F_0-F_7	OUTPUT		

GAL®20V8 EMULATING PAL® DEVICES



FEBRUARY, 1988

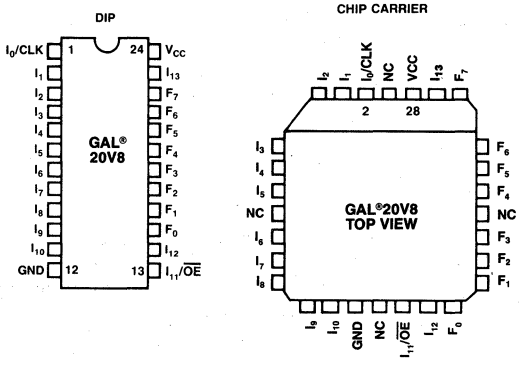
GAL®20V8 HIGH PERFORMANCE E²CMOS™ GENERIC ARRAY LOGIC

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} . . . . . −.5 to +7V
Input voltage applied. . . . . −2.5 to V_{CC} +1.0V
Off-state output voltage applied . . −2.5 to V_{CC} +1.0V
Storage temperature. . . . . −65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

PIN CONFIGURATION



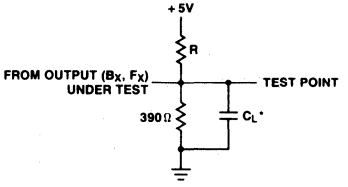
OPERATING RANGE

SYMBOL	PARAMETER	TEMPERATURE RANGE									UNIT
		MILITARY			INDUSTRIAL			COMMERCIAL			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	V
T_A	Ambient temperature				−40		85	0		75	°C
T_C	Case temperature	−55		125							°C

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.



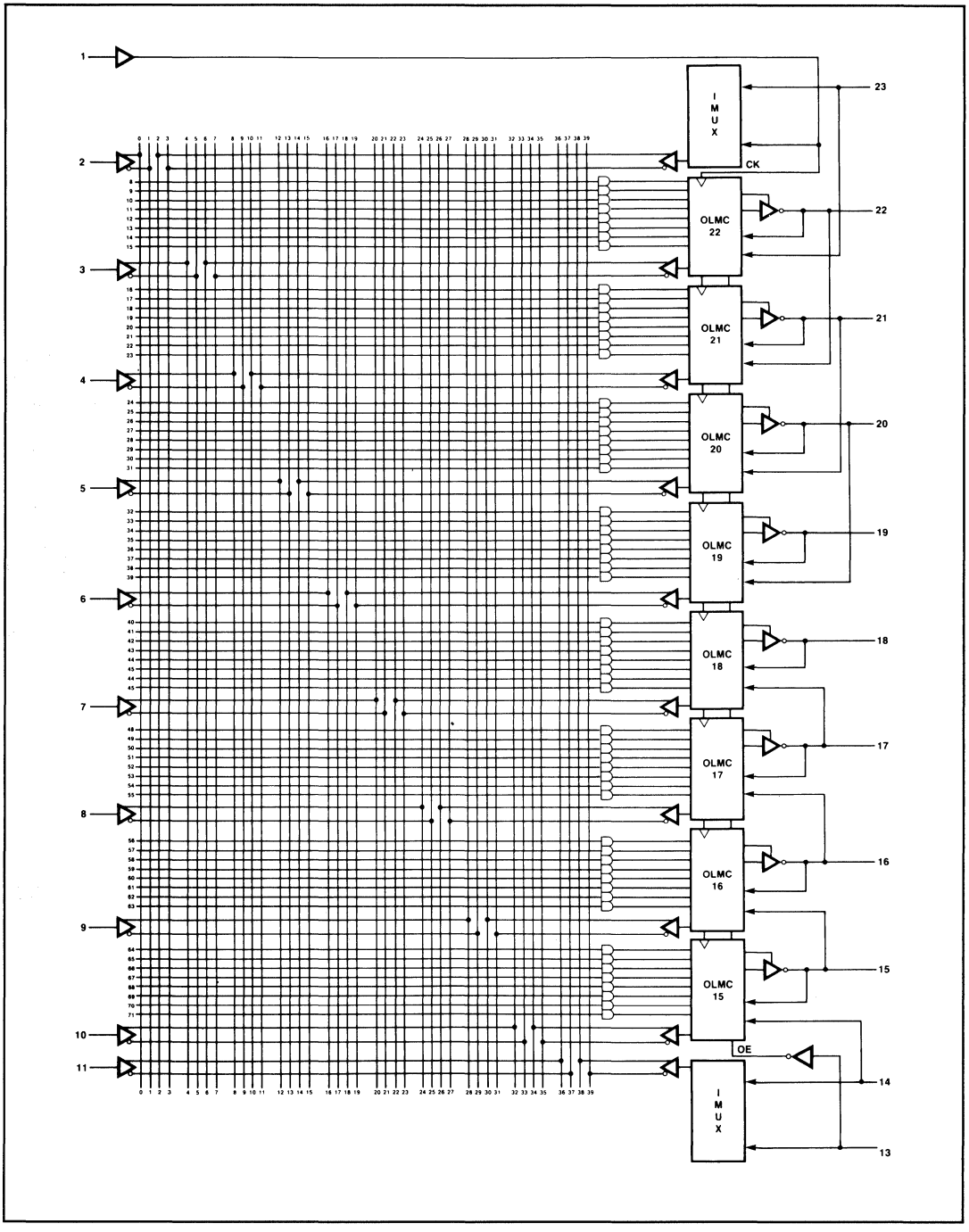
*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = 2.0V
C_B	Bidirectional Pin Cap	15	pF	V_{CC} = 5.0V, V_B = 2.0V

*Guaranteed but not 100% tested.

GAL®20V8 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS

QUARTER POWER GAL®20V8

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz $V_{CC} = V_{CC}$ MAX		COM'L	—	45	mA
				MIL/IND	—	55	mA
I_{OS}[1]	Output Short Circuit	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} =	I_{OL} = 24mA	COM/IND	—	0.5	V
		V_{CC} MIN	I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} = V_{CC} MIN	I_{OH} = −3.2mA	COM/IND	2.4	—	V
			I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

HALF POWER GAL®20V8

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz		COM'L	—	90	mA
		$V_{CC} = V_{CC}$ MAX		MIL/IND	—	110	mA
I_{OS}[1]	Output Short Circuit	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} =	I_{OL} = 24mA	COM/IND	—	0.5	V
		V_{CC} MIN	I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} = V_{CC} MIN	I_{OH} = −3.2mA	COM/IND	2.4	—	V
			I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

[1] One output at a time for a maximum duration of one second.

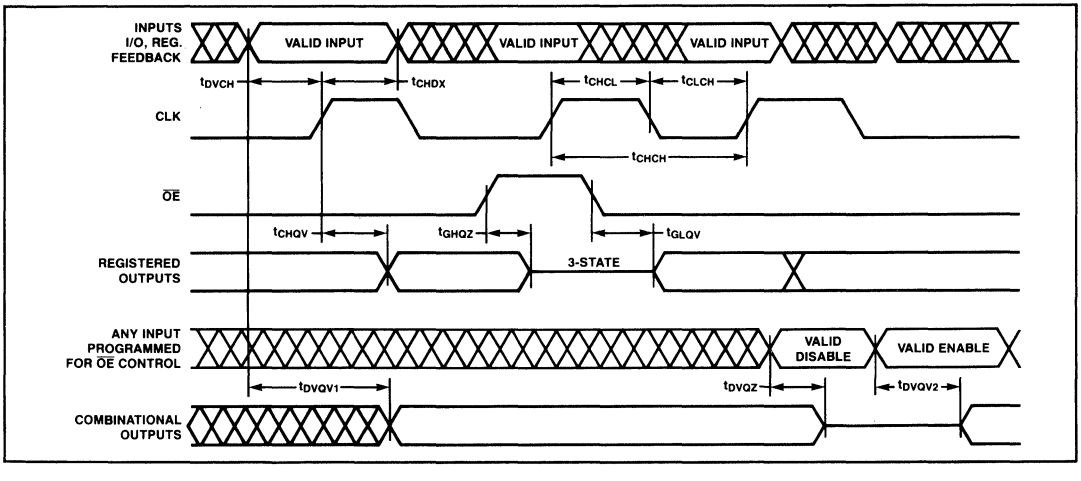
SWITCHING CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL	PARAMETER		TEMPERATURE RANGE: COMMERCIAL/INDUSTRIAL — GAL®20V8-15 MIN	GAL®20V8-15 MAX	GAL®20V8-25 MIN	GAL®20V8-25 MAX	GAL®20V8-20 MIN	GAL®20V8-20 MAX	TEMPERATURE RANGE: MILITARY — GAL®20V8-30 MIN	GAL®20V8-30 MAX	UNITS	TEST CONDITIONS[1] R(Ω)	TEST CONDITIONS[1] C_L(pF)
T_{DVQV1}	Delay from Input to Active Output		—	15	—	25	—	20	—	30	ns	200	50
T_{DVQV2}	Product Term Enable Access Time to Active Output		—	15	—	25	—	20	—	30	ns	Active High R = ∞ Active Low R = 200	50
T_{DVQZ2}	Product Term Disable to Output Off		—	15	—	25	—	20	—	30	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GHQZ2}	$\overline{OE}$ (Output Enable) High to Outputs Off		—	15	—	20	—	18	—	25	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GLQV}	$\overline{OE}$ (Output Enable) Access Time		—	15	—	20	—	18	—	25	ns	Active High R = ∞ Active Low = 200	50
T_{CHQV}	Clock High to Output Valid Access Time		—	12	—	15	—	15	—	20	ns	200	50
T_{DVCH}	Input or Feedback Data Setup Time		12	—	20	—	15	—	25	—	ns	—	—
T_{CHDX}	Input or Feedback Data Hold Time		0	—	0	—	0	—	0	—	ns	—	—
T_{CHCH}	Clock Period (T_{DVCH} + T_{CHQV})		24	—	35	—	30	—	45	—	ns	—	—
T_{CHCL}	Clock Width High		10	—	15	—	12	—	15	—	ns		
T_{CLCH}	Clock Width Low		10	—	15	—	12	—	15	—	ns		
f_{MAX}	Maximum Frequency	Feedback	41.6		28.5		33.3		22.2		MHz	200	50
		No Feedback	50.0		33.3		41.6		33.3				

[1] Refer also to AC test conditions.

[2] 3-State levels are measured 0.5V from steady-state active level.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL (OLMC)

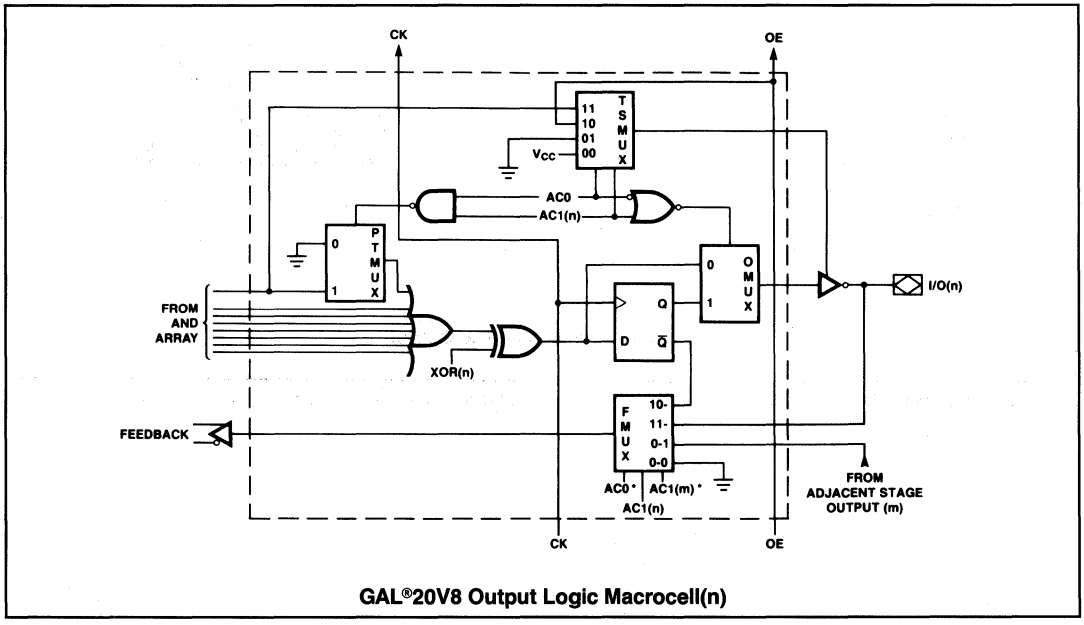
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable can be connected to all outputs, or separate inputs or product terms can be used to provide individual output enable controls. The output logic macrocell provides the designer with maximal output flexibility in matching signal requirements, thus providing more functions than possible with existing 24-pin PAL® devices.

The various configurations of the output logic macrocell are controlled by programming certain cells (SYN, AC0, AC1(n), and the XOR(n) polarity bits) within the 82-bit architecture control word. The SYN bit determines whether or not a device will have registered output capability or will have purely combinational outputs. It also replaces the AC0 bit in the two outermost macrocells, OLMC (15) and OLMC (22). When first setting up the device architecture, this is the first bit to choose.

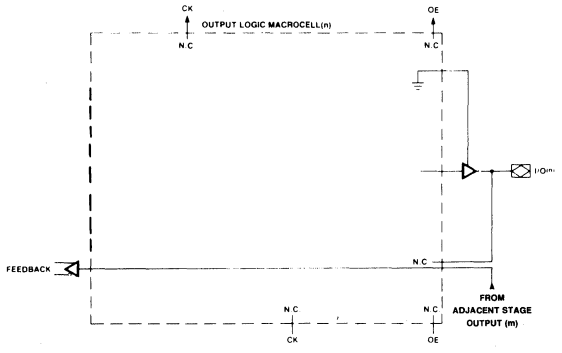
Architecture control bit AC0 and the eight AC1(n) bits direct the outputs to be wired always on, always off (as an input), have common $\overline{OE}$ control (pin 13), or to be three-state controlled separately from a product term. The architecture control bits also determine the source of the array feedback term through the FMUX, and select either combinational or registered outputs.

The five valid macrocell configurations are shown in each of the macrocell equivalent diagrams. In all cases, the eight XOR(n) bits individually determine each output's polarity. The truth table associated with each diagram shows the bit values of the SYN, AC0, and AC1(n) that set the macrocell to the configuration shown.



GAL®20V8 Output Logic Macrocell(n)

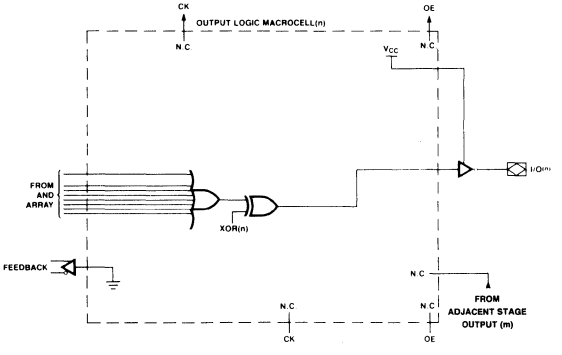
* NOTE—$\overline{SYN}$ replaces AC0 and SYN replaces AC1(m) as an input to the FMUX in OLMC (15) and OLMC (22) to maintain full JEDEC fuse map compatibility with PAL® type device architectures.



SYN	AC0	AC1(n)	FUNCTION
1	0	1	INPUT MODE (i.e. 20L2, 18P4)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 13 ARE DATA INPUTS.
THE OUTPUT BUFFER IS DISABLED.

Dedicated Input Mode



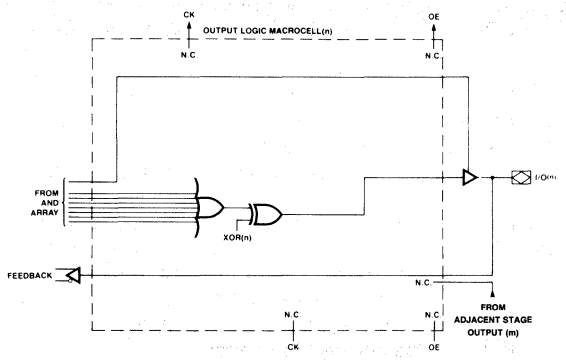
SYN	AC0	AC1(n)	FUNCTION
1	0	0	ALL OUTPUTS COMBINATIONAL (i.e. 16H6)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 13 ARE DATA INPUTS.
ALL MACROCELLS CONFIGURED AS OUTPUTS
ARE COMBINATIONAL AND ALWAYS ACTIVE.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Dedicated Combinational Output

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

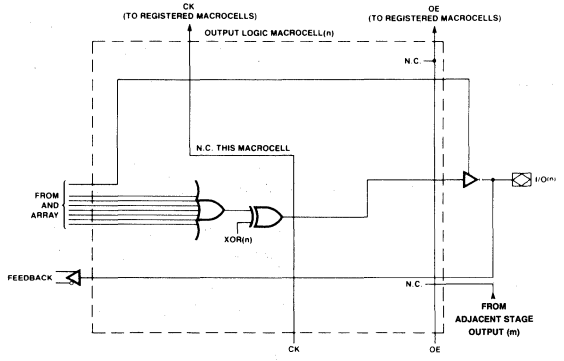


SYN	AC0	AC1(n)	FUNCTION
1	1	1	ALL OUTPUTS COMBINATIONAL (i.e. 20L8, 20H8)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 13 ARE DATA INPUTS.
ALL OUTPUTS ARE COMBINATIONAL.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Combinational Output

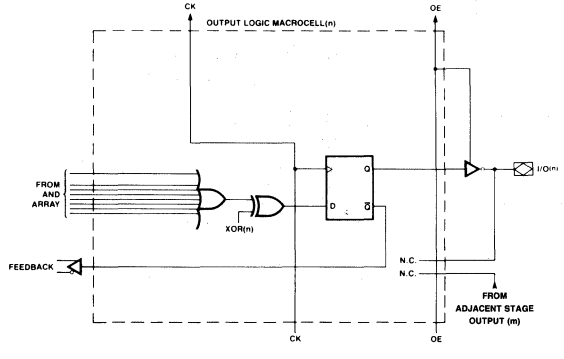


SYN	AC0	AC1(n)	FUNCTION
0	1	1	COMBINATIONAL OUTPUT IN A REGISTERED DEVICE

IN THIS ARCHITECTURE MODE,
PIN 1 = CK, PIN 13 = $\overline{OE}$. THIS MACROCELL
IS COMBINATIONAL, BUT AT LEAST ONE
OF THE OTHERS IS A REGISTERED OUTPUT.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Combinational Output in a Registered Device



SYN	AC0	AC1(n)	FUNCTION
0	1	0	OUTPUT REGISTERED (i.e. 20R8)

IN THIS ARCHITECTURE MODE,
PIN 1 = CK, PIN 13 = $\overline{OE}$.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

Registered Active High or Low Output

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ROW ADDRESS MAP DESCRIPTION

Figure 1 shows a block diagram of the row address map. There are a total of 44 unique row addresses available to the user when programming the GAL®20V8 devices. Row addresses 0–39 each contain 64 bits of input term data. This is the user array where the custom logic pattern is programmed. Row 40 is the electronic signature word. It has 64 bits available for any user-defined purpose. Rows 41–59 are reserved by the manufacturer and are not available to users.

Row 60 contains the architecture and output polarity information. The 82 bits within this word are programmed to configure the device for a specific application. Row 61 contains a one bit security cell that when programmed prevents further programming verification of the array. Row 63 is the row that is addressed to perform a bulk erase of the device, resetting it back to a virgin state. Each of these functions is described in the following sections.

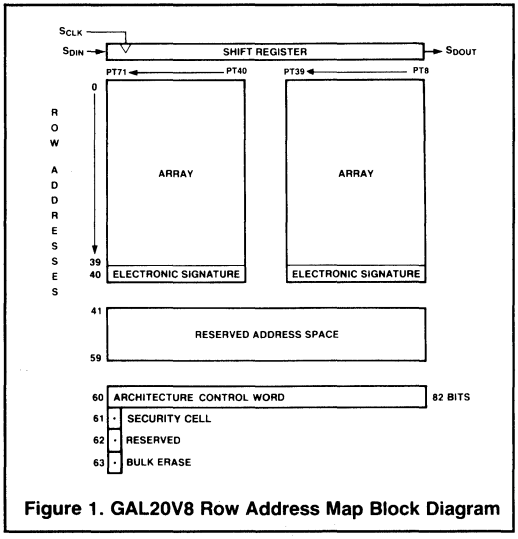


Figure 1. GAL20V8 Row Address Map Block Diagram

ELECTRONIC SIGNATURE WORD

An electronic signature word is provided with every GAL®20V8 device. It resides at row address 40 and contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

ARCHITECTURE CONTROL WORD

All of the various configurations of the GAL®20V8 devices are controlled by programming cells within the 82-bit architecture control word that resides at row 60. The location of specific bits within the architecture control word is shown in the control word diagram in Figure 2. The function of the SYN, AC0 and AC1(n) bits have been explained in the output logic macrocell description. The eight polarity bits determine each output's polarity individually by selectively correct logic. The numbers below the XOR(n) and AC1(n) bits in the architecture control word diagram shows the output device pin number that the polarity bits control.

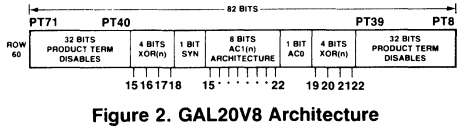


Figure 2. GAL20V8 Architecture Control Word Diagram

SECURITY CELL

Row address 61 contains the security cell (one bit). The security cell is provided on all GAL®20V8 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array (rows 0–39). The cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Signature data is **always** available to the user.

BULK ERASE MODE

By addressing row 63 during a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its virgin state.

Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL®20V8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. Figure 3 shows the pin functions necessary to preload the registers. The register preload timing and pin voltage levels necessary to perform the function are shown below. This test mode is entered by raising PRLD to V_{IES}, which enables the serial data in (S_{DIN}) buffer and the serial data out (S_{DOUT}) buffer. Data is then serially shifted into the registers on each rising edge of the clock, DCLK. Only the macrocells with registered output configurations are loaded. If only 3 outputs have registers, then only 3 bits need be shifted in. The registers are loaded from the bottom up, as shown in Figure 3.

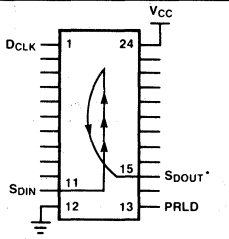


Figure 3. Output Register Preload Pinout

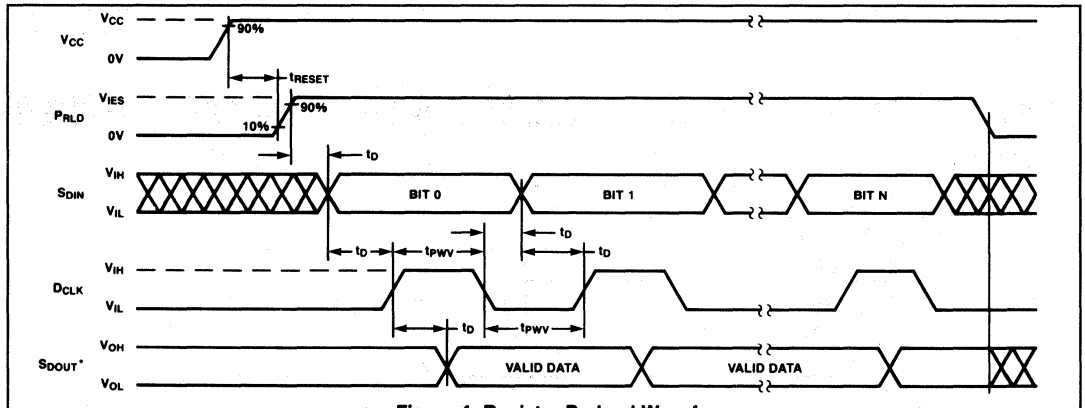


Figure 4. Register Preload Waveforms

Note: The S_{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V_{CC} with a 10K Ω resistor.

LATCHUP PROTECTION

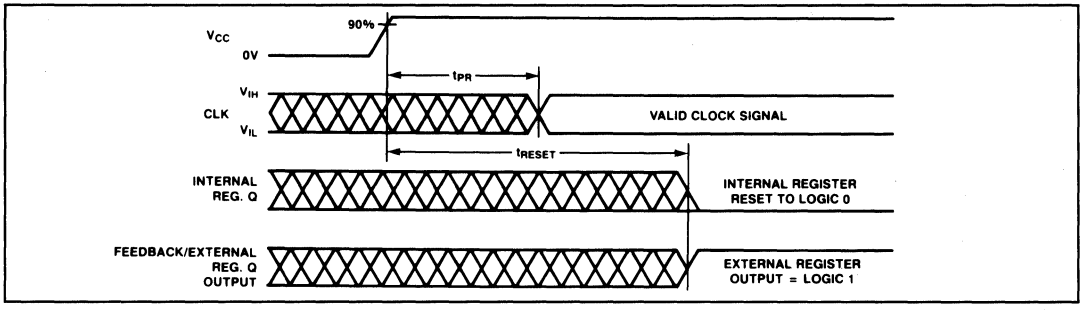
GAL® devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL® devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load the driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL® devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and 3-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL®20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

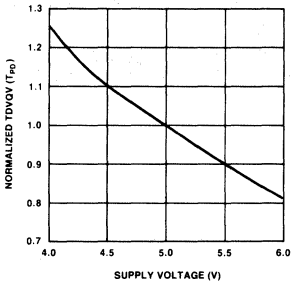
The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL®20V8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL®20V8 TEST PARAMETRIC SPECIFICATIONS

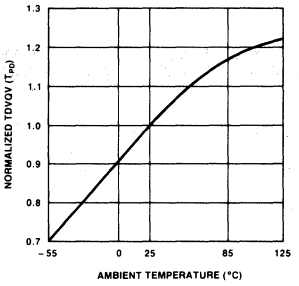
SYMBOL	PARAMETER	MIN.	TYP	MAX	UNITS
V_{IH}	Input Voltage (High)	2.40	—	V_{CC}	V
V_{IL}	Input Voltage (Low)	0.00	—	0.50	V
V_{IES}	Register Preload Input Voltage	14.5	15	15.5	V
V_{OH}*	Output Voltage (High)*	2.40	—	V_{CC}	V
V_{OL}*	Output Voltage (Low)*	0.00	—	0.50	V
I_{IH}, I_{IL}	Input Current	—	±1	±10	μA
t_{PWV}	Verify Pulse Width	1	5	10	μS
t_D	Pulse Sequence Delay	1	5	10	μS
t_{PR}	Reset Circuit Power-Up	—		100	nS
t_{RESET}	Register Reset Time From Valid V_{CC}	—		45	μS

*NOTE—The S_{DOUT} output buffer is an open drain output. This pin should be terminated to V_{CC} with a 10K resistor.

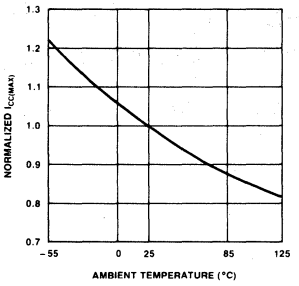
NORMALIZED TDVQV (T_{PD}) VS. SUPPLY VOLTAGE



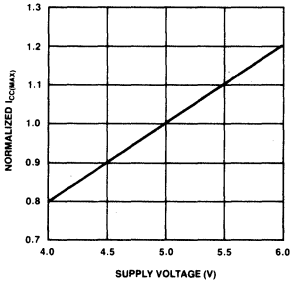
NORMALIZED TDVQV (T_{PD}) VS TEMPERATURE



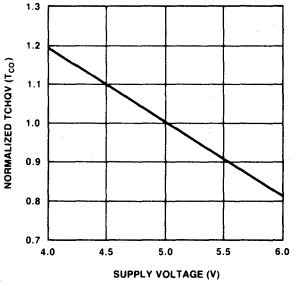
NORMALIZED $I_{CC(MAX)}$ VS. TEMPERATURE



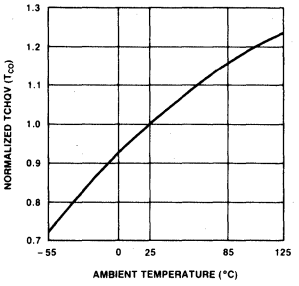
NORMALIZED $I_{CC(MAX)}$ VS. SUPPLY VOLTAGE



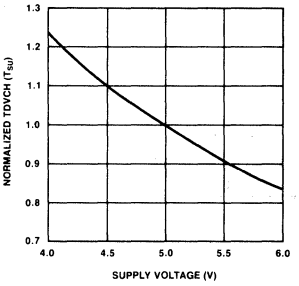
NORMALIZED TCHQV (T_{CO}) VS. SUPPLY VOLTAGE



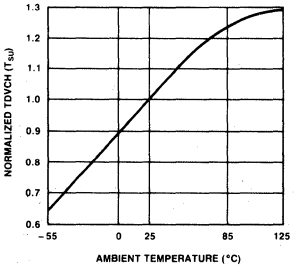
NORMALIZED TCHQV (T_{CO}) VS. TEMPERATURE



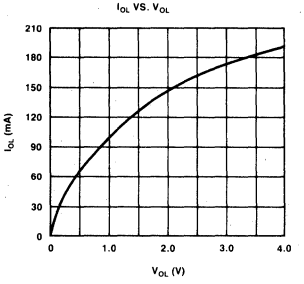
NORMALIZED TDVCH (T_{SU}) VS. SUPPLY VOLTAGE



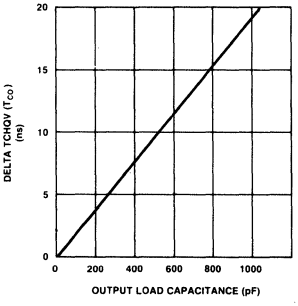
NORMALIZED TDVCH (T_{SU}) VS. TEMPERATURE



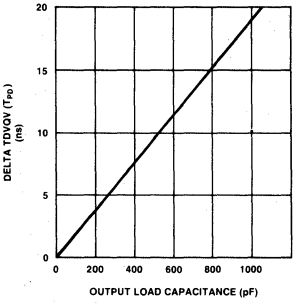
I_{OL} VS. V_{OL}



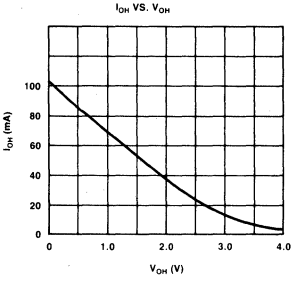
DELTA TCHQV (T_{CO}) VS. OUTPUT LOADING



DELTA TDVQV (T_{PD}) VS. OUTPUT LOADING



I_{OH} VS. V_{OH}



Lattice Semiconductor Corporation

GAL®20V8A

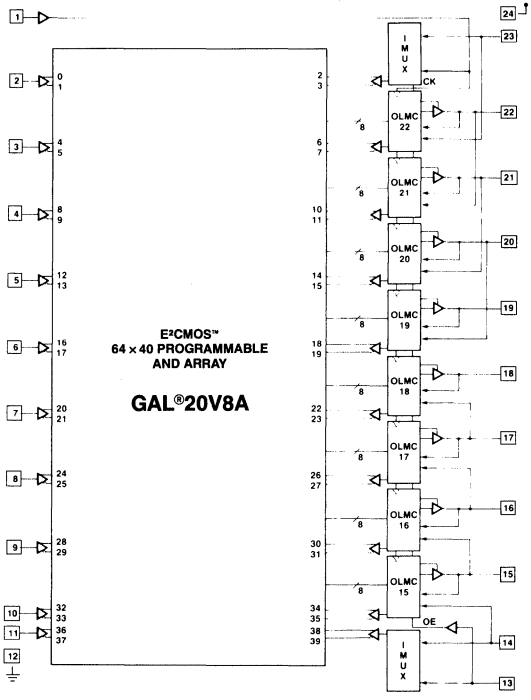
ULTRA HIGH SPEED E²CMOS™
GENERIC ARRAY LOGIC

PRELIMINARY INFORMATION

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 24 mA Outputs**
  - **— UltraMOS® III Advanced CMOS Technology**
- **50% REDUCTION IN POWER**
  - **— 90ma Typ I_{CC}**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (< 50ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 24-pin 'D'PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Video Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The GAL®20V8A-12, at 12 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL®20V8A-12 to consume just 90ma typical I_{CC} which represents a 50% savings in power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing each Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL®20V8A are the PAL® architectures listed in the table on the right. The GAL®20V8A is capable of emulating any of these PAL® architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/write cycles and that data retention exceeds 20 years.

GAL®/PAL® COMPARISON—10/12/15 ns DEVICES

PART TYPE	GAL®20V8A ARCHITECTURE EMULATION 90ma	PAL®20xx AVAILABILITY 90ma	180ma
20L8	✓		✓
20H8	✓		
20R8	✓		✓
20R6	✓		✓
20R4	✓		✓
20P8	✓		
20RP8	✓		
20RP6	✓		
20RP4	✓		
14L8	✓		
16L6	✓		
18L4	✓		
20L2	✓		
14H8	✓		
16H6	✓		
18H4	✓		
20H2	✓		
14P8	✓		
16P6	✓		
18P4	✓		
20P2	✓		
20V8	✓		

FEBRUARY, 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OREGON 97208 APPLICATIONS HOTLINE: 1-800-FASTGAL

GAL®20V8A
ULTRA HIGH SPEED E²CMOS™
GENERIC ARRAY LOGIC

SWITCHING CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL				UNITS	TEST CONDITIONS	
			GAL®20V8A-12		GAL®20V8A-10				
			MIN.	MAX.	MIN.	MAX.		R(Ω)	C_L(pF)
T_{DVQV1}	Delay from Input to Active Output		—	12	—	10	ns	200	50
T_{DVQV2}	Product Term Enable Access Time to Active Output		—	12	—	10	ns	Active High R = ∞ Active Low R = 200	50
T_{DVQZ}[1]	Product Term Disable to Output Off		—	12	—	10	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GHQZ}[1]	$\overline{OE}$ (Output Enable) High to Outputs Off		—	10	—	10	ns	From V_{OH} R = ∞ From V_{OL} R = 200	5
T_{GLQV}	$\overline{OE}$ (Output Enable) Access Time		—	10	—	10	ns	Active High R = ∞ From V_{OL} R = 200	50
T_{CHQV}	Clock High to Output Valid Access Time		—	10	—	8	ns	200	50
T_{DVCH}	Input or Feedback Data Setup Time		12	—	10	—	ns	—	—
T_{CHDX}	Input or Feedback Data Hold Time		0	—	0	—	ns	—	—
T_{CHCH} T_{CHCL} T_{CLCH}	Clock Period (T_{DVCH} + T_{CHQV}) Clock Width High Clock Width Low		22 8 8	— — —	18 8 8	— — —	ns ns ns	—	—
f_{MAX}	Maximum Frequency	SYNCH. Feedback	45.5		55.5				
		ASYNCH. No Feedback	62.5		62.5				

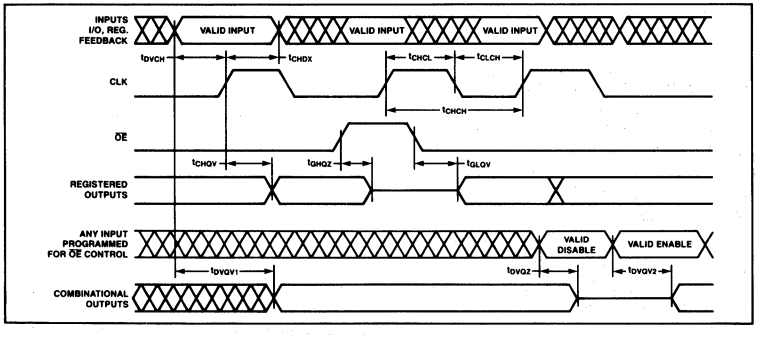
[1] 3-State levels are measured 0.5V from steady-state active level.

ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS (HALF-POWER)

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	GND ≤ V_{IN} < V_{CC} MAX			—	±10	μA
I_{FZL} I_{FZH}	Output Pin Leakage Current	GND ≤ V_{IN} < V_{CC} MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz V_{CC} = V_{CC} MAX		COM'L MIL	— —	115 140	mA mA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} =	I_{OL} = 24mA	COM'L	—	0.5	V
		V_{CC} MIN	I_{OL} = 12mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} =	I_{OH} = −3.2mA	COM'L	2.4	—	V
		V_{CC} MIN	I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

NOTE: For detailed technology, logic, timing, programming information and specifications, refer to the GAL20V8 datasheet.

SWITCHING WAVEFORMS



Lattice Semiconductor Corporation

GAL®39V18

GENERIC ARRAY LOGIC

PRELIMINARY

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **— Instantly Reconfigurable Logic**
  - **— Instantly Reprogrammable Cells**
  - **— Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— Low Power: 90mA Typical**
  - **— High Speed: 15ns Max. Clock to Output Delay**
    25ns Max. Setup Time
    30ns Max. Propagation Delay
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **— 10 Output Logic Macro Cells**
  - **— 8 State Logic Macro Cells**
  - **— 20 Input and I/O Logic Macro Cells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— Separate State Register and Input Clock Pins**
  - **— Functionally Supersets Existing 24-pin PAL® and IFL™ Devices**
  - **— Asynchronous Clocking**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **20-YEAR DATA RETENTION**

DESCRIPTION

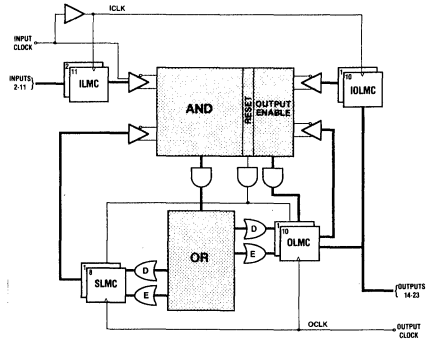
Using a high performance E²CMOS™ technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL®39V18. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL®39V18 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL®39V18 has 10 programmable Output Logic MacroCells (OLMC) and 8 programmable "buried" State Logic MacroCells (SLMC). In addition, there are 10 Input Logic MacroCells (ILMC) and 10 I/O Logic MacroCells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS™ reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL®39V18 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature word is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



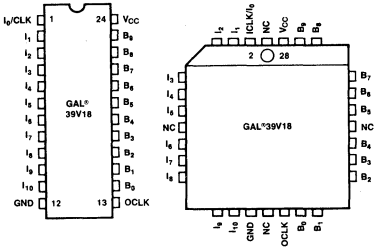
MACRO CELL NAMES

ILMC	INPUT LOGIC MACRO CELL
IOLMC	I/O LOGIC MACRO CELL
SLMC	STATE LOGIC MACRO CELL
OLMC	OUTPUT LOGIC MACRO CELL

PIN NAMES

I_0-I_{10}	INPUT	B_0-B_9	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION



FEBRUARY, 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OR 97208

APPLICATIONS HOTLINE: 1-800-FASTGAL

GAL®39V18 GENERIC ARRAY LOGIC

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} . . . . . −.5 to +7V
Input voltage applied. . . . . −2.5 to V_{CC} +1.0V
Off-state output voltage applied . . −2.5 to V_{CC} +1.0V
Storage temperature. . . . . −65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

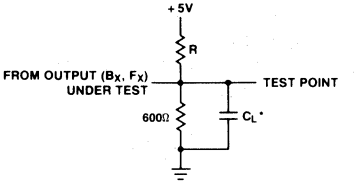
OPERATING RANGE

SYMBOL	PARAMETER	TEMPERATURE RANGE									UNIT
		MILITARY			INDUSTRIAL			COMMERCIAL			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	V
T_A	Ambient temperature				−40		85	0		75	°C
T_C	Case temperature	−55		125							°C

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.



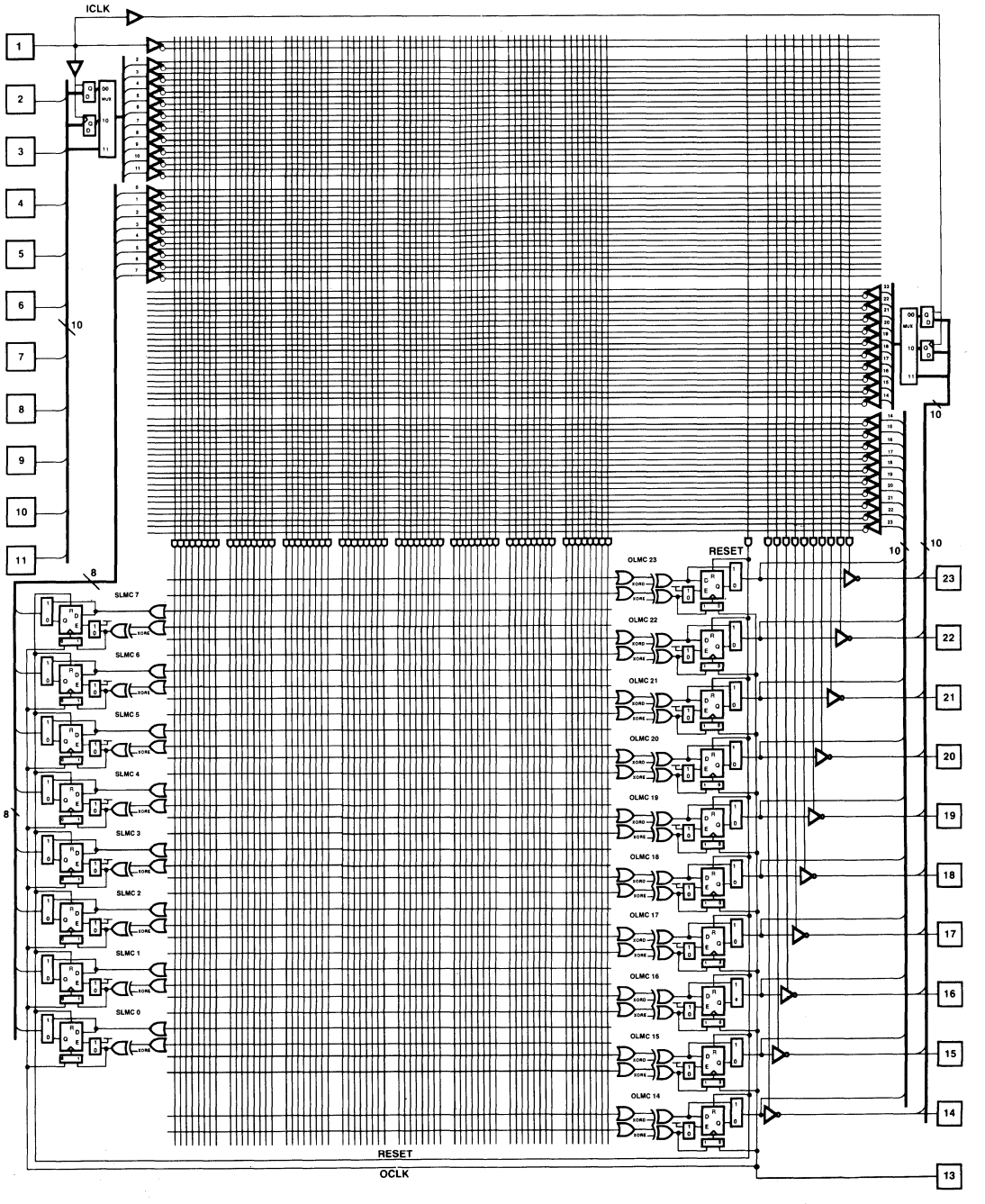
*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE[1] (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	12	pF	V_{CC} = 5.0V, V_I = 2.0V
C_F	Output Capacitance	15	pF	V_{CC} = 5.0V, V_F = 2.0V
C_B	Bidirectional Pin Cap	15	pF	V_{CC} = 5.0V, V_B = 2.0V

*Guaranteed but not 100% tested.

GAL®39V18 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP. RANGE	MIN.	MAX.	UNITS
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ MAX			—	±10	μA
I_{BZH} I_{BZL}	Bidirectional Pin Leakage Current	$GND \le V_{IN} < V_{CC}$ MAX			—	±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz		COM'L	—	130	mA
		$V_{CC} = V_{CC}$ MAX		MIL/IND	—	150	mA
I_{OS}[1]	Output Short Circuit	V_{CC} = 5.0V V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} =	I_{OL} = 16mA	COM/IND	—	0.5	V
		V_{CC} MIN	I_{OL} = 8mA	MIL	—	0.5	V
V_{OH}	Output High Voltage	V_{CC} =	I_{OH} = −3.2mA	COM/IND	2.4	—	V
		V_{CC} MIN	I_{OH} = −2.0mA	MIL	2.4	—	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{IL}	Input Low Voltage				—	0.8	V

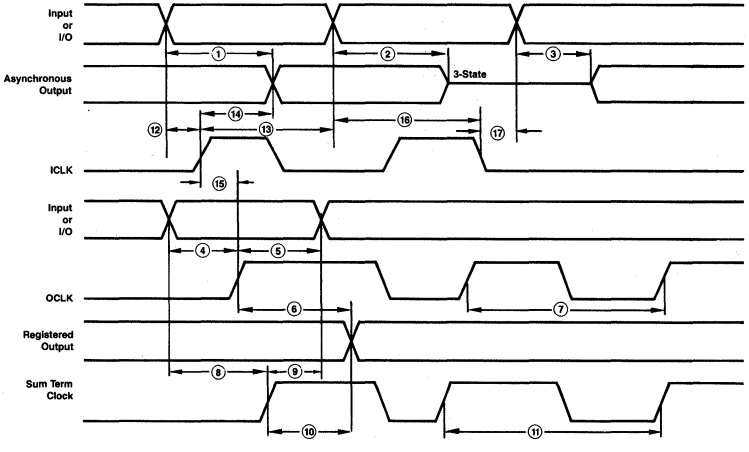
[1] One output at a time for a maximum duration of one second.

SWITCHING CHARACTERISTICS OVER OPERATING CONDITIONS

SYMBOL NO.	SYMBOL	PARAMETER	COM/IND		MIL			TEST CONDITIONS	
			MIN	MAX	MIN	MAX	UNITS	R(Ω)	C_L(pF)
1	T_{DVQV1}	Delay From Input or I/O to Output	—	30	—	40	ns	300	50
2	T_{DVQZ}	Delay From Input or I/O to Outputs Off (disable)	—	25	—	35	ns	Infinite	5
3	T_{DVQV2}	Delay From Input or I/O to Outputs On (enable)	—	25	—	35	ns	Infinite	50
4	T_{DVC1H}	Input or I/O Setup Time to OCLK	25	—	35	—	ns	300	50
5	T_{C1HDX}	Input or I/O Hold Time after OCLK	−5	—	−5	—	ns	300	50
6	T_{C1HQV}	OCLK To Output Valid Delay	—	15	—	20	ns	300	50
7	Period 1	OCLK Cycle Time ($T_{DVC1H} + T_{C1HQV}$)	—	40	—	55	ns	300	50
8	T_{DVD1V}	Input or I/O Setup Time to Sumterm CLK	7.5	—	10	—	ns	300	50
9	T_{D1VDX}	Input or I/O Hold Time after Sumterm CLK	—	12.5	—	17.5	ns	300	50
10	T_{D1VQV}	Sumterm CLK to Output Delay	—	35	—	45	ns	300	50
11	Period 2	STCLK Cycle Time ($T_{DVD1V} + T_{D1VQV}$)	—	42.5	—	55	ns	300	50
12	T_{DVC2H}	Input or I/O Setup Time to ICLK	2.5	—	5	—	ns	300	50
13	T_{C2HDX}	Input or I/O Hold Time after ICLK	—	5	—	7.5	ns	300	50
14	T_{C2HQV}	Delay From ICLK to Asynchronous Output Valid	—	35	—	45	ns	300	50
15	T_{C2HC1H}	Register Setup Time After ICLK	30	—	40	—	ns	300	50
16	T_{DVC2L}	Input or I/O Setup Time to Latch	2.5	—	5	—	ns	300	50
17	T_{C2LDX}	Input or I/O Hold Time after Latch	—	5	—	7.5	ns	300	50
—	TRESET	Input, I/O or Feedback to Reset	—	40	—	50	ns	—	—

LEGEND: T = Time D = Data Q = Output Z = Hi-Z V = Valid H = High L = Low X = Change C1 = OCLK C2 = ICLK D1 = Sumterm Clock Input

SWITCHING WAVEFORMS



INPUT LOGIC MACRO CELL (ILMC) AND I/O LOGIC MACRO CELL (IOLMC)

The GAL®39V18 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells (transparent when high) and as a clock for registered macrocells (positive edge triggered).

Configurable input blocks can be used to advantage by system designers. Registered inputs are popular for synchronization and data merging. Transparent latches are useful when the input data is invalid outside a known time window. Direct inputs are used in systems where the input data is well ordered in time. With the GAL®39V18, external registers and latches are not necessary.

The various configurations of the input and I/O macrocells are controlled by programming four architecture control bits (INLATCH, INSYN, IOLATCH, IOSYN) within the 68-bit architecture control word. The SYN bits determine whether the macrocells will have register/latch capability or will be strictly asynchronous. The LATCH bits select between latched and registered inputs.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the values of the LATCH and SYN bits required to set the macrocell to the configuration shown.

OUTPUT LOGIC MACRO CELL (OLMC) / STATE LOGIC MACRO CELL (SLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the State Logic MacroCells (SLMC), as they are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic MacroCells (OLMC).

Like the ILMC and IOLMC discussed above, output and state logic macrocells are configured by programming specific bits in the architecture control word (CKS(i), OUTSYN(i), XORD(i), XORE(i)), but unlike the input macrocells which must be configured in blocks, these macrocells are configurable on a macrocell-by-macrocell basis. Throughout this data sheet, i = [14...23] for OLMCs and i = [0...7] for SLMCs.

State and Output Logic MacroCells may be set to one of three valid configurations: combinational, D-type registered with sum term (asynchronous) clock, or D/E-type registered. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selectable through the XORD(i) architecture bits. Polarity selection is not necessary for SLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selectable through the XORE(i) architecture control bits.

When CKS(i) = 1 and OUTSYN(i) = 0, macrocell "i" is set as "D/E-type registered." In this configuration, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When CKS(i) = 0 and OUTSYN(i) = 0, macrocell "i" is set as "D-type registered with sum term clock." In this configuration, the register is enabled and its "E" sum term is routed directly to the clock input. This allows for the popular "asynchronous programmable clock" feature, selectable on a register-by-register basis.

When CKS(i) = 0 and OUTSYN(i) = 1, macrocell "i" is set as "combinational." Configuring a SLMC in this manner turns it into a complement array. Complement arrays are used to construct multi-level logic.

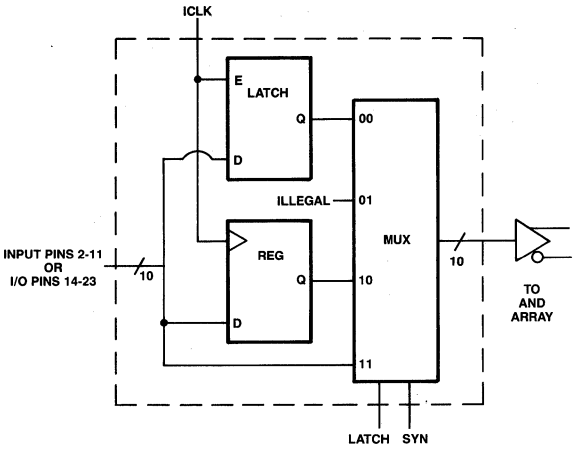
Registers in both the Output and State Logic Macrocells feature a RESET input. This active high input allows the registers to be simultaneously and asynchronously reset from a common signal. The source of this signal is the RESET product term. Registers reset to a logic zero, but since the output buffers invert, a logic one will be present at the device pins.

There are two possible feedback paths from each OLMC: one from before the output buffer (this is the normal path), and one from after the output buffer, through the IOLMCs. The second path is usable as a feedback only when the associated bi-directional pin is being used as an output; during input operations it becomes the input data path, turning the associated OLMC into an additional buried state macrocell.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register construct can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

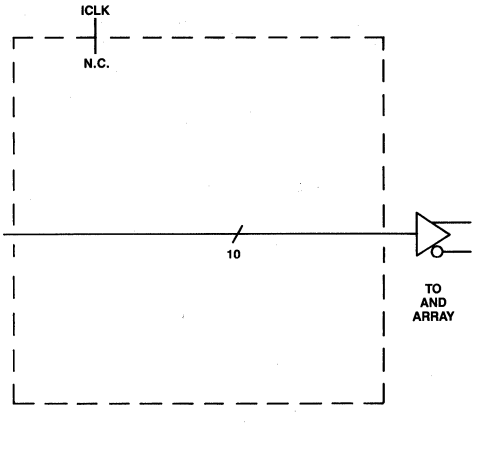
The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the bit value of CKS(i) and OUTSYN(i) required to set the macrocell to the configuration shown.

ILMC/IOLMC CONFIGURATIONS



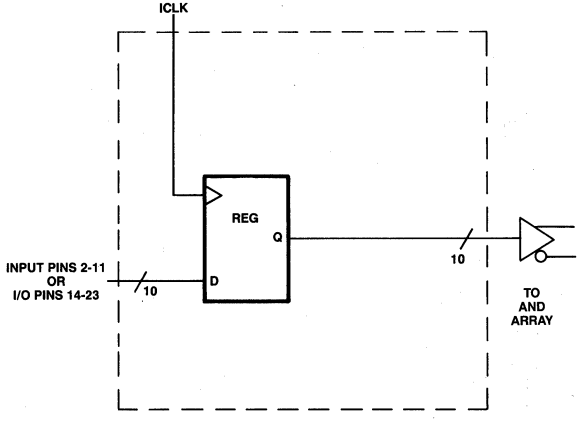
ILMC/IOLMC

Generic Block Diagram



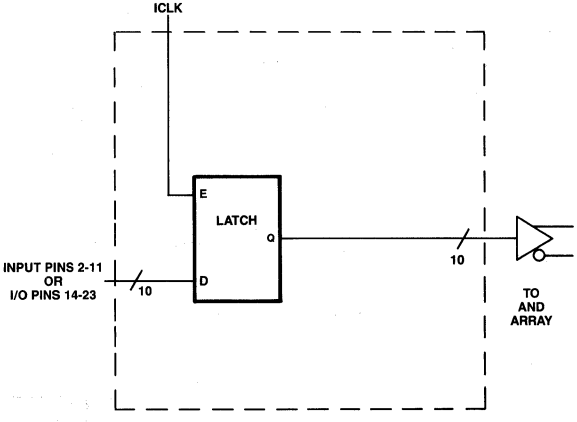
Asynchronous Input

LATCH	SYN
1	1



Registered Input

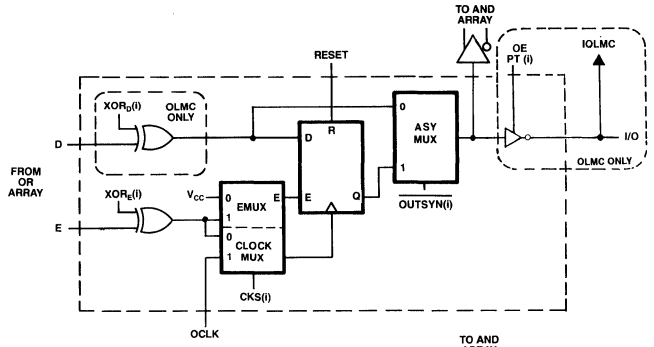
LATCH	SYN
1	0



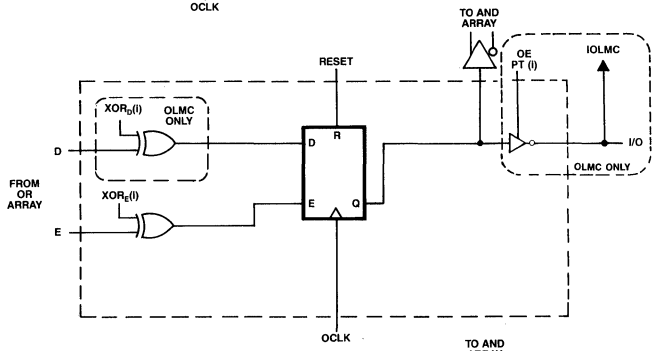
Latched Input

LATCH	SYN
0	0

OLMC/SLMC CONFIGURATIONS

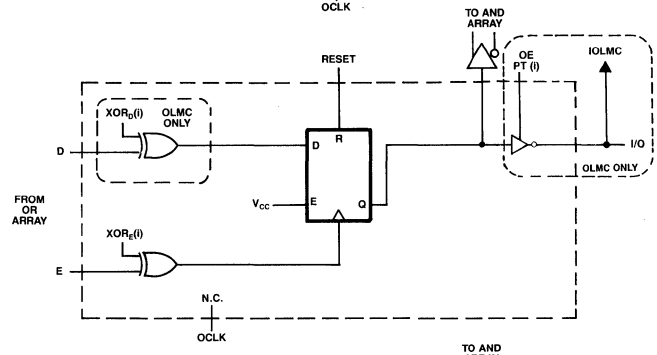


OLMC/SLMC
Block Diagram



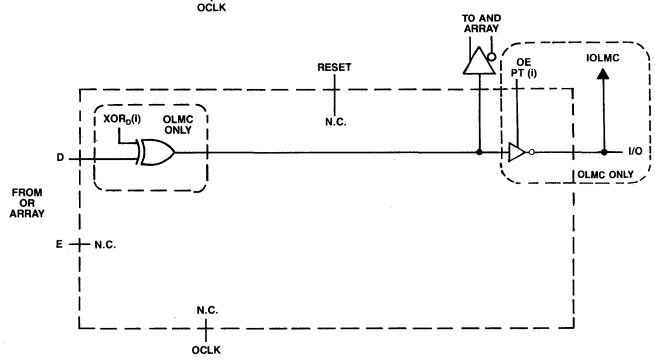
D/E Type Registered

CKS(i)	OUTSYN(i)
1	0



D-Type Registered with Sum Term Asynchronous Clock

CKS(i)	OUTSYN(i)
0	0



Combinational

CKS(i)	OUTSYN(i)
0	1

ARRAY DESCRIPTION

The GAL®39V18 E^2 reprogrammable array is subdivided into three smaller arrays: AND, OR, and Architecture. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 input terms by 75 product term outputs. The 20 input and I/O logic macrocells, 8 SLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complemented forms). Product terms 0-63 serve as inputs to the OR array. Product term 64 is the RESET PT; it generates the RESET signal described in the earlier discussion of output and state logic macrocells. Product terms 65-74 are the output enable product terms; they control the output buffers, thus enabling device pins 14-23 to be bi-directional or 3-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. Product terms 0-63 of the AND array serve as the inputs to this array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 SLMCs, one "D" term and one "E" term to each.

ARCHITECTURE ARRAY

The various configurations of the GAL®39V18 are enabled by programming cells within the architecture control word. This 68-bit word contains all of the chip configuration data. This data includes: XORD(i), XORE(i), CKS(i), OUTSYN(i), INLATCH, INSYN, IOLATCH, and IOSYN. The function of each of these bits has been previously explained.

ELECTRONIC SIGNATURE WORD

Every GAL®39V18 device contains an electronic signature word. The Electronic Signature word is a 72-bit user definable storage area, which can be used to store inventory control data, pattern revision numbers, manufacture date, etc. Signature data is always available to the user, regardless of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL®39V18 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND, OR, and architecture arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Electronic Signature data is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal machine operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

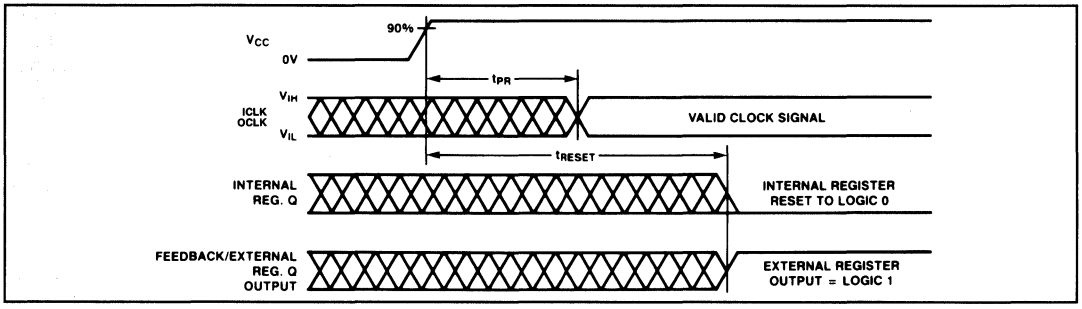
All of the registers in the GAL®39V18 can be preloaded, including the input, I/O, and state registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

INPUT BUFFERS

GAL® devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than "traditional bipolar devices." This allows for a greater fan out from the driving logic.

GAL® devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and 3-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL®39V18 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL®39V18. First, the V_{CC} rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (t_{PR}). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL®39V18 RESET TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNITS
t_{PR}	Reset Circuit Power-Up	—		100	nS
t_{RESET}	Register Reset Time From Valid V_{CC}	—		45	μS

NOTES

Lattice Semiconductor Corporation

ispGAL™ 16Z8

In-System re-Programmable
GENERIC ARRAY LOGIC

ADVANCED INFORMATION

FEATURES

- **IN-SYSTEM RECONFIGURABLE—5-VOLT ONLY PROGRAMMING**
  - **— Change Logic "On the Fly" (in less than 1 s)**
  - **— Nonvolatile E² Technology**
- **DIAGNOSTICS MODE FOR CONTROLLABILITY AND OBSERVABILITY OF SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— High Speed: 25ns Max Propagation Delay**
  - **— Low Power: 90mA Max Active**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DATA RETENTION EXCEEDS 10 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **APPLICATIONS INCLUDE:**
  - **— Reconfigurable Interfaces**
  - **— Copy Protection and Security Schemes**
    - **— erasable hardware**
    - **— password systems**
    - **— proprietary hardware/software interlocks**

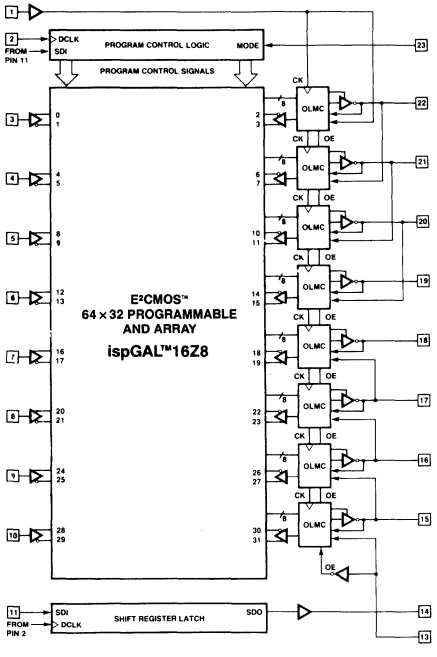
DESCRIPTION

The LATTICE ispGAL™16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system reprogrammability and real time, in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using LATTICE UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL™16Z8 is architecturally and parametrically identical to the 20-pin GAL®16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are used only during programming. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS™ reprogrammable cells, enable complete AC, DC, programmability, and functionality testing of each ispGAL™16Z8 during manufacturing and allows LATTICE to guarantee 100% performance to all specifications.

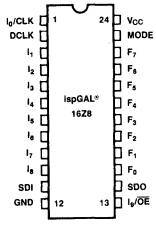
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I_0-I_{15}	INPUT	MODE	MODE CONTROL
CLK	CLOCK INPUT	DCLK	DATA CLOCK
B_0-B_5	BI-DIRECTIONAL	SDI	SERIAL DATA IN
F_0-F_7	OUTPUT	SDO	SERIAL DATA OUT
$\overline{G}(\overline{OE})$	OUTPUT ENABLE	V_{CC}	POWER (+5V)
GND	GROUND		

PIN CONFIGURATION



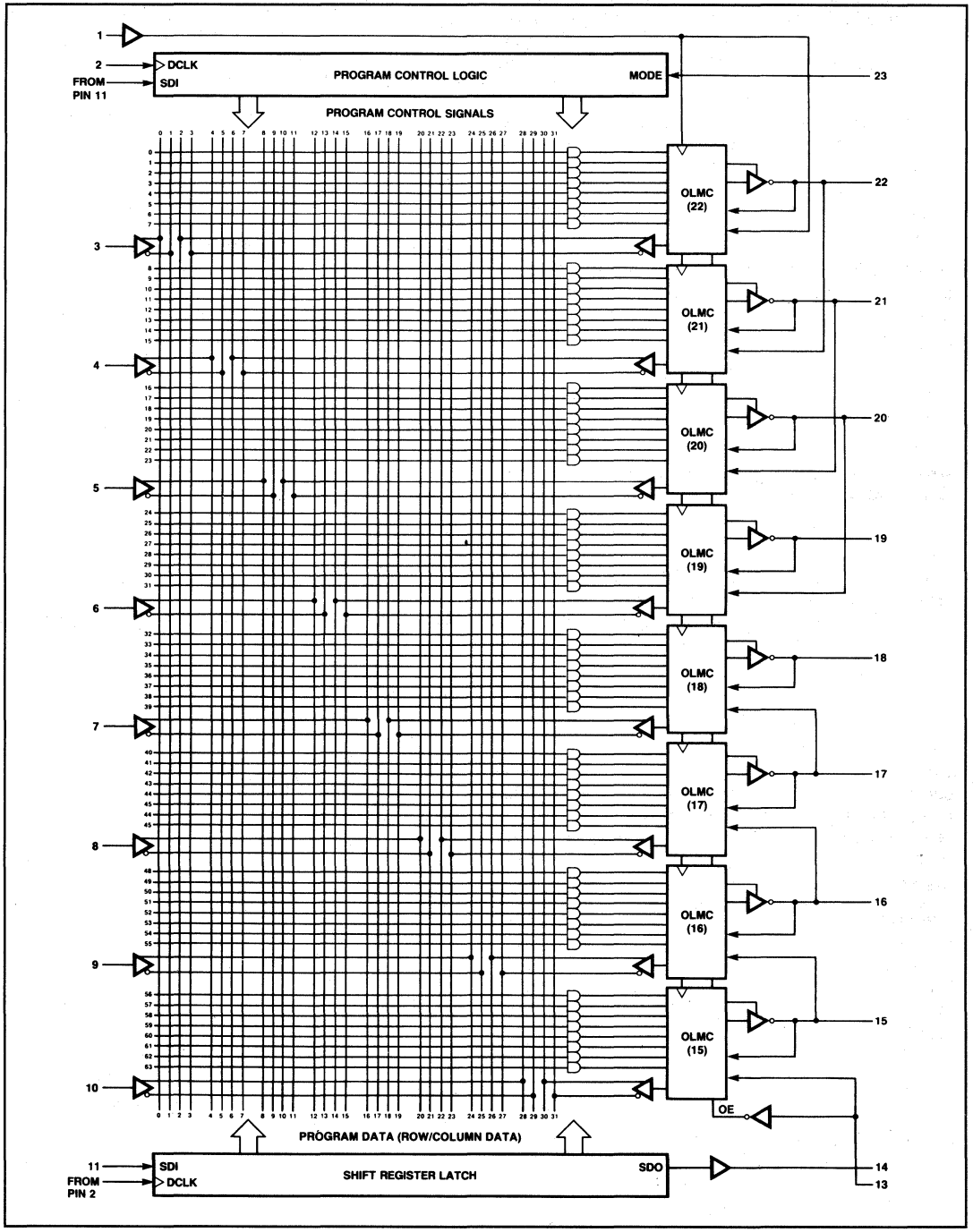
FEBRUARY, 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OR 97208

APPLICATIONS HOTLINE: 1-800-FASTGAL

ispGAL™ 16Z8
In-System re-Programmable
GENERIC ARRAY LOGIC

ispGAL™16Z8 LOGIC DIAGRAM



OVERVIEW

The ispGAL™16Z8 device has three basic modes of operation: NORMAL, DIAGNOSTIC and PROGRAM. These three modes are controlled by the system designer through the use of a sophisticated on-chip state machine.

In addition, the ispGAL™16Z8 has been optimized so that the use of 2 or more devices on a board requires the same amount of control overhead as a single device would. This Serial Loop approach applies to the DIAGNOSTIC and PROGRAM operation modes of the device.

Detailed information on the characteristics, control options and timing for each of the operating modes is available. Contact your sales representative for a copy of this document.

The balance of this document will perform a general review of the operation of the ispGAL™16Z8 in its various modes and will explain the use of these control pins.

MODE CONTROL & OPERATION

The signals used to control this device are the same for both the DIAGNOSTIC and PROGRAM modes. During NORMAL mode the control pins serve no function other than to control the transition to another mode. The shared control pin approach allows for a simple multi-mode operation with minimal system or board overhead.

The four control signals are TTL level signals; MODE, DCLK, SDI and SDO. These signals are used to transition from mode to mode and through each of the five states as shown in Figure 1. MODE is used only to control the on-chip state machine. DCLK is used for mode control and for the orderly clocking of data into the 16Z8 from the SDI (serial data in) pin as well as out of the device through the SDO (serial data out) pin. SDI is also used for state machine control.

The current state cannot be explicitly observed, however, an "escape" sequence ("HL") to the NORMAL mode is always available to start the process fresh. Caution should be used when using this escape path as the pattern in the device may not be valid if an erase or reprogramming operation was in progress.

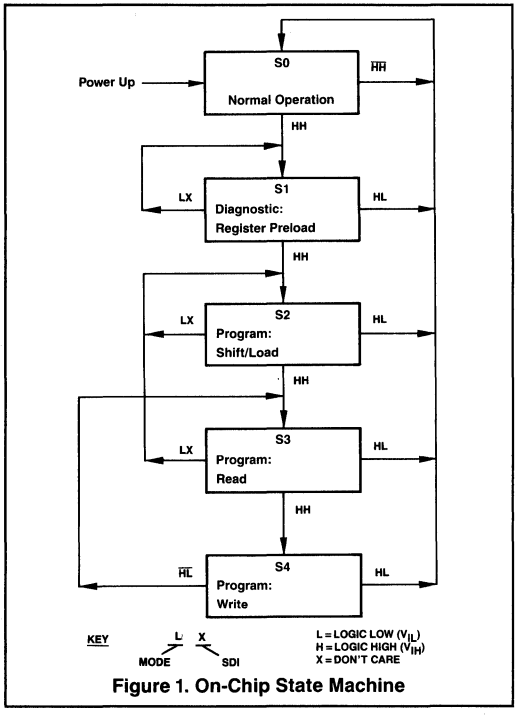


Figure 1. On-Chip State Machine

DIAGNOSTIC MODE

From the NORMAL mode the device transitions to the DIAGNOSTIC:Preload state (mode:state). In this mode the values in the Macrocell registers can be interrogated or "pre-"loaded for diagnostic testing of the system. Advanced system design requires full control and observability of all registers on a board.

Upon entry to the DIAGNOSTIC:Preload state the data on the device output pins (15-22) is latched and held to its 1, 0 or three-state condition. This is important as the DIAGNOSTIC:Preload state configures a serial loop from the SDI pin through each of the registers to the SDO pin. Data is shifted across all of the registers during diagnostics (Figure 2). The latching of the current output data insures that the system is not influenced by the changing register contents until such time as the DIAGNOSTIC:Preload state is exited.

The access to the macrocell data is through the SDI and SDO pins. While in the DIAGNOSTIC:Preload state the value in each register is serially shifted out through SDO with each pulse of the DCLK pin. Similarly, new data can be pre-loaded into the registers through the SDI pin.

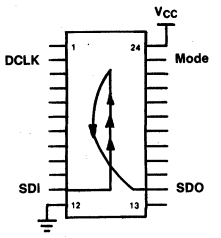


Figure 2. Diagnostic/Program Pinout

The number of registers in a 16Z8 is a function of the configuration of each macrocell. The length of the serial path, and therefore the number of bits of data shifted in or out of the device, is a function of the number of macrocells which are configured to have registers.

PROGRAM MODE

The PROGRAM mode can only be entered from the DIAGNOSTIC:Preload state. When this transition is made the value of the user programmable Three-State Bit (TSB) is examined to determine the data condition that is held on the device output pins 15-22. The data can either remain latched to 1-0-Z as in the DIAGNOSTIC mode or the data can be forced to high impedance. Again, this feature allows complete control of the system during programming.

The DIAGNOSTIC mode consists of three states of the on-chip state machine: SHIFT, READ and WRITE. Proper sequencing of these states is necessary to program and verify the device. Programming and verification is accomplished using a Serial Register Latch (SRL) to program or verify a row of data at a time.

PROGRAM:Shift

During the PROGRAM:Shift state the 88 bit SRL is serially loaded with 82 bits of data and 6 bits of row address for each row to be programmed. The architecture and Electronic Signature of the 16Z8 are also programmed in the same manner. DCLK is used to shift data into SDI for the loading process.

PROGRAM:Read

Verification of data in the array is accomplished in the PROGRAM:Read state. Exiting the PROGRAM:Read state to the PROGRAM:Shift state causes the contents of the array row to be copied to the SRL. This data can be shifted out as outlined above. Programming the Security Cell prevents valid data from being loaded into the SRL. This feature is provided to prevent subsequent copying of the cell patterns.

PROGRAM:Write

The actual programming cycle occurs in the PROGRAM:Write state. The data to be programmed is loaded into the SRL in the PROGRAM:Shift state prior to executing the write cycle. It is the responsibility of the system control logic to assure that the device stays in the PROGRAM:Write state for a sufficient time to program the E^2 cells, approximately 10 ms. The PROGRAM:Write state is then exited to the PROGRAM:Read state for verification of the data.

The 16Z8 is completely erased by addressing an "erase" row address using the same process outlined above. It is necessary to bulk-erase the device prior to rewriting any pattern into the device as each row write cycle does not include an automatic erase of that row.

The entire programming process takes less than ½ second. The bulk erase is 10 ms, and each of the 36 programmable rows can be loaded, programmed and verified in approximately 10.5 ms for a total time of 0.39 seconds. During this time the device output pins are latched or high impedance and the 16Z8 is not responding to changes on its input pins. The system must accommodate this programming time.

SERIAL DIAGNOSTIC/PROGRAM LOOP OPERATION

Figure 3 shows a typical ispGAL™16Z8 system. Notice that several devices have been cascaded together to form a serial programming loop. This arrangement allows the simultaneous transfer of programming and diagnostic data through every ispGAL™ device in the system with no additional control logic necessary. When controlling multiple devices in such a loop, the basic diagnostic and programming algorithms remain unchanged. However, there are some additional considerations.

In a serial programming loop, the SDO of the first device is connected to the SDI of the second, the SDO of the second to the SDI of the third, and so on. DCLK and MODE are common for every device. With such an arrangement, devices in the loop are always in the same state, but the data being shifted into their respective SRLs may be different. Note that, before data reaches the SDI input of any given device, it must first pass through the 88-bit SRL of every device ahead of it in the loop. The SRL is asynchronously bypassed (SDO = SDI) whenever MODE = 1 allowing SDI to function as both a data and mode control pin.

In a serial diagnostic loop the length of the loop is a function of the number of OLMC registers being used. On the other hand, in a serial programming loop, data transfers always occur in multiples of 88-bits, as the data must pass through the SRL of other devices in the loop.

Because all devices in a loop are always in the same state, reprogramming just one out of "n" devices would seem to be a problem. This, however, is not the case, as several options exist. The most obvious solution is to simply reprogram all of the devices, even if the new pattern is the same as the old. The system "down" time is effectively the same since all the devices reprogram in parallel.

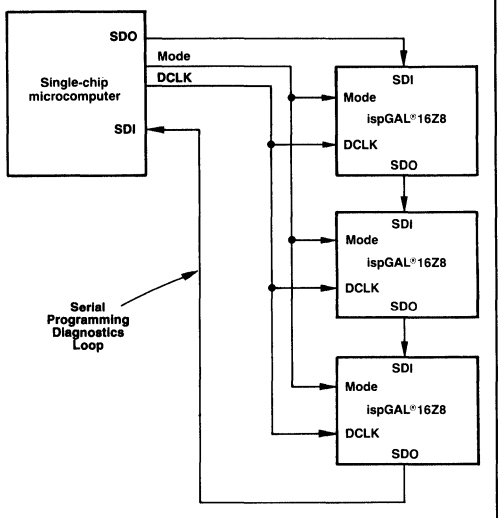


Figure 3. Typical ispGAL™16Z8 System

INTRODUCTION

While the purchase price of a programmable logic device is an important consideration in identifying the most cost-effective solution for a system design, it is clearly not the only criterion. Hidden costs attributable to product testing, yield fallout, inventory management, and other factors can dramatically impact the final cost of using a PLD.

This brief investigates the overhead associated with PLD usage and the advantages of testable and reprogrammable E²CMOS GAL devices over one-time-programmable PLDs.

The GAL family of programmable logic devices is manufactured on a state-of-the art E²CMOS process that not only provides a better speed-power product than the best bipolar devices, but offers an advantage unique among PLD manufacturers: guaranteed programming and post-programming yields of 100%.

The 100%-yield guarantee is the culmination of years of Lattice Semiconductor's circuit-design and manufacturing experience applied to the GAL device. The only way to be able to make this 100% yield statement — and to supply product that actually meets the 100% criterion — is to fully test all functions of the device, prior to shipment.

The electrically erasable (EE) matrix, unlike previous PLD matrix technologies (bipolar fuse-link and UV-erasable PROM), permits full testing of the programmability and reprogrammability of each and every matrix cell. The ability to pattern the actual matrix is extremely significant, since it also allows Lattice to test the functionality of each of the Macrocell logic blocks, under various worst-case configurations. This test approach is referred to at Lattice as 'Actual Test'. Unlike other PLD manufacturers' approaches, which include imprecise correlations, simulations, test rows, and phantom arrays, Actual Test conclusively verifies AC and DC performance of every cell in every GAL device.

Eliminates Incoming QA

A consequence of Actual Test is that GAL devices do not require the typical incoming Quality Assurance testing that traditional fuse-link bipolar PLDs require. As such, the cost savings of using GAL devices begins the moment the parts arrive, since the average cost of an incoming QA operation — hardware, software development and maintenance, and handling — is approximately 7% of the raw device cost. Moreover, GAL devices become the optimal choice for implementation of Just-In-Time or Dock-To- Stock programs, since they eliminate the expense and time required by the incoming inspection process.

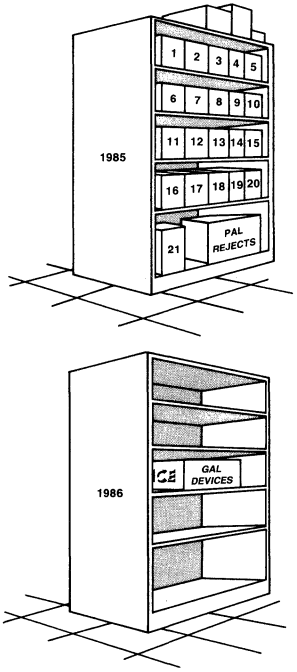
Still, a number of users require that all devices undergo incoming QA. In those cases, the use of GAL devices still simplifies the issue. A single generic test program can be used to test all configurations of the E²CMOS-based GAL device. The expense of generating and maintaining a test program for every architecture (16L8, 16R4, 10P8, and so on) is eliminated with Generic Array Logic.

Since the QA test for fuse-link PLDs, by its nature, requires the destructive patterning of the fuse array, QA testing of bipolar PAL devices can only be done through a sample plan. At best, a sample plan can provide a crude estimate of fuse-link yield loss; moreover, sampled devices cannot be erased and must be subsequently thrown away. GAL devices, utilizing the E²CMOS process can be patterned and erased at will, allowing 100% QA of all specifications and configurations. And, the devices can, of course, be erased to allow full reuse of the sample units in manufacturing.

Simplified Inventory Management

The generic architecture and high performance of the GAL devices allow two basic devices — the 20-pin GAL16V8 and 24-pin GAL20V8 — to directly replace approximately 70% of PLD device types currently available, including 100% of the most popular types ('L8,' 'R8,' 'R6,' and 'R4') and a sizable portion of the 'IFL' and EPLD devices. The obvious benefit of using GAL

Figure 1. Inventory Reduction with GAL Devices



devices is a substantial reduction in the number of part types that need be stocked (Figure 1).

Inventory management of dozens of speed-power options and device architectures is a painful process. The ideal cost of managing a device inventory adds some 2% of direct overhead; the real cost can be significantly greater, due to the risk that a shortage, 'outage,' or obsolete stock condition will exist. Improper planning could result in a shut-down of the assembly line. The generic architecture allows the GAL device to serve as insurance whenever needed to meet an immediate shortfall. The yields, at 100%, allow full planning confidence that the problem is solved.

Disposition of rejects is another inventory-management issue. The raw cost of the rejects themselves (at a 2% to 5% fallout rate) is compounded by the associated paperwork of obtaining a replacement or credit for the bad devices. Studies show that every time a buyer or purchasing agent picks up the phone or generates a debit memo, some $30 to $50 is spent. Followup activity — 2 or 3 calls or letters — compounds the expense. Meanwhile, the manufacturing inventory is short of devices. What's more, carrying additional 'safety-stock' as insurance against a temporary shortage results in a higher inventory-carrying cost.

100% Yields Reduce System Cost

Perfect yields, as provided through Actual Test, allow the manufacturing environment to run in a fully predictable manner. This allows purchasing and production-control to accurately schedule all activities and product for system build. Just-In-Time material-requisition systems assume that the material will arrive on time, in the exact quantity necessary. With GAL devices, the source product inventory can be allocated for programming to various patterns with full confidence that the final patterned devices will be in the quantity and of the quality desired.

A rule of thumb, commonly known as the 'Factor of Ten Rule' (Table 1), details the cost of a failing unit throughout the manufacturing process. The point is that unit cost is not nearly as important as its contribution to subsequent costs (or savings). The Rule basically states that the cost of detecting and replacing a defective device increases by an order of magnitude for each subsequent step of the manufacturing process.

Table 1. Factor of Ten Rule

COST*	MULTIPLIER	OPERATION
$ 5.00	X	RAW COST OF DEVICE
$ 50.00	10X	COST OF DETECTING AND REPAIRING A BOARD FAILURE
$ 500.00	100X	COST OF DETECTING AND REPAIRING A SYSTEM FAILURE
$5,000.00 +	1,000X	COST OF REPAIRING A FIELD FAILURE

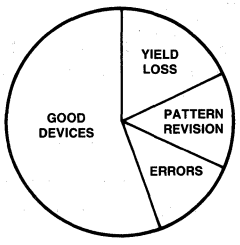
*EACH SUCCESSIVE OPERATION RESULTS IN 10 TIMES THE COST TO DETECT THE FAILING DEVICE. $5.00 DEVICE COST ASSUMED — USE YOUR ACTUAL COST AND A 10× MULTIPLIER TO OBTAIN ACTUAL NUMBERS.

It is extremely important to recognize that the additional difficulty and cost of using traditional PLDs has implications far beyond what the observed programming yield fallout portends. The hidden costs, time and expense aggravation of board failures (10x device cost to detect and repair), system failures (100x device cost), and the potential for field failures far outweigh the simple 2% to 5% yield losses observed on a programming fixture.

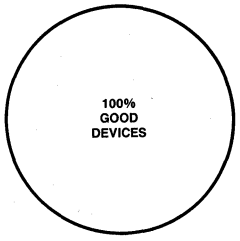
Figure 2 illustrates the differences between traditional PAL device yield loss and the 100% yields of the GAL devices. Notice that even operator errors and engineering pattern revisions are recoverable with GAL devices, which can be instantly erased and reprogrammed to the proper architecture and logic pattern.

In a typical manufacturing environment, device programming hardware patterns the array, and assuming the engineer has provided test vectors, the hardware performs a basic (slow) functional test of the device.

Figure 2. Yield Loss Comparison



TRADITIONAL PLD APPROACH



GAL APPROACH

Yield losses at these two operations average 2% to 5% and 1% to 2%, respectively.

What is not tested adequately at the PAL programming operation is the effect of partially programmed fuses that result in degraded AC performance or marginal reliability of the device. These failures are caught at board test and/or after board burn-in. Typical bipolar functional and AC parametric failure rates range between 0.5% and 2% for all manufacturers of fuse-link PAL devices. Even if one assumes the minimum failure rate of 0.5%, the system failure rates are still greatly magnified.

Two mechanisms are used to detect the failures of PAL devices: board test and system test. Using the 'Factor of Ten Rule' and assuming that board test fully screens bad devices (AC fallout), if a conservative device failure rate of 0.5% were observed, the actual parts cost would be:

$$\begin{aligned} Acost &= Pcost + (Pcost * 10 * 0.5\%) \\ &= Pcost + Pcost * 0.05 \\ &= 1.05 * Pcost \end{aligned}$$

Performing the screening at the system level, under the same scenario, makes a dramatic difference in the cost of the device:

$$\begin{aligned} Acost &= Pcost + (Pcost * 100 * 0.5\%) \\ &= Pcost + Pcost * 0.5 \\ &= 1.5 * Pcost \end{aligned}$$

These two different cost factors were determined using the conservative failure rate of 0.5%. Using the GAL device, with its 0% failure rate, provides instead a cost factor of 1; i.e., no additional cost burden is generated.

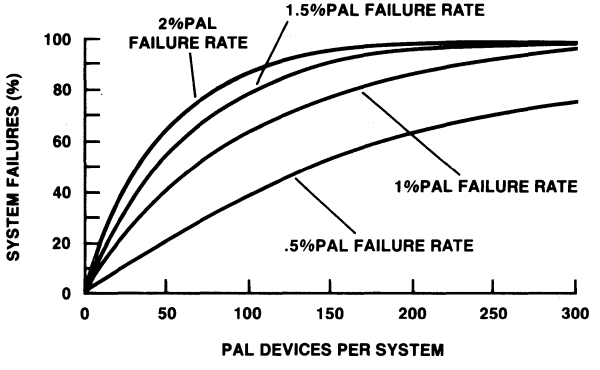
The problem caused by PLD failures obviously grows in proportion to the number of devices in a system, since the probability of a failure among a group of PAL devices is higher than that for a single device. Figure 3 plots the probability of a board or system not working, as a function of the number of devices per system, for a variety of device failure rates.

For example, at a unit failure rate of 1.0%, a system incorporating 30 PAL devices will exhibit a 25% failure rate. That means that 1 out of every 4 systems will have to be reworked, at tremendous cost. The replacement of an average 0.5% of the units in a system results in an actual 8% adder to the hidden device cost.

The difficulty in replacing board failures is compounded by the removal of soldered units. It is quite easy to destroy a board with the removal and replacement of a defective device.

Systems that fail in the field are not only the most costly in terms of dollars and cents, but in customer relations, as well. They require responding rapidly and performing repairs in a less-than-ideal environment, without the complete tools and supplies available at the factory. Field failures will always occur to some degree. However, the use of GALs can help reduce field repair costs when they do occur — even if the failing device is a traditional bipolar PLD — since the generic, erasable nature of GAL devices allows a minimum of field inventory to be carried, to debug system failure problems caused by other devices. The panel on the next page provides guidelines for calculating PLD usage costs. □

Figure 3. Probability of System Failures Using Bipolar PLDs



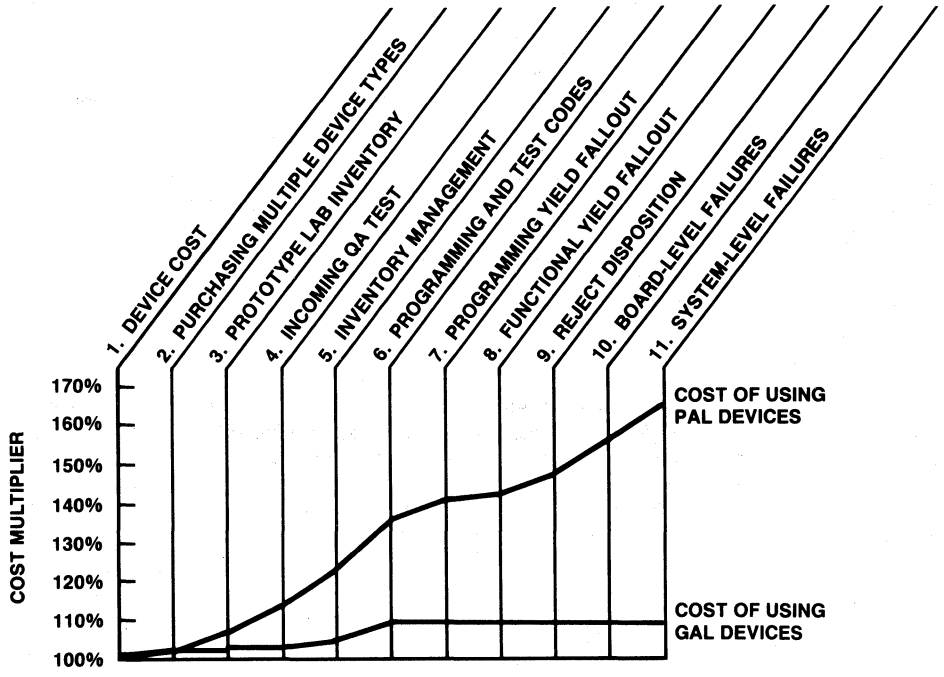
PLD COST ANALYSIS

The cost of using a PLD goes well beyond simply the raw device cost. Programming and vector-test yields are obvious contributors to higher unit cost. The less-obvious and hidden costs tend to be much more difficult to identify and quantify.

The purpose of the costing example is to provide the basis for your own cost analysis, using your own overhead and yield numbers. Estimates for reasonable ranges of the cost contributors are shown as a guide to using your own numbers.

The explanation for each of the contributors to the device cost multiplier follow the figure. These cost multipliers include the overhead for each operation, and as a result, are higher than the observed costs.

The example shown is based on actual data from a 100,000-piece-per-year user of traditional bipolar PLDs. The environment is a typical, high-volume, quality-controlled one. The GAL device checks in at 1.09 times the normalized cost, while the actual cost of using the bipolar PLD is 1.66 times — almost 40% higher.



1 ***Device cost*** *is normalized to unity so that the raw purchase price has no bearing on the other cost factors.*

2 ***Purchasing Multiple Device Types*** *instead of the single GAL device adds to overhead in the purchasing and receiving departments. This contributes approximately 2% as the availability, quality, and quantity issues are resolved with each order. The GAL approach reduces this number to 1.25% with inventory simplification.*

3 ***Prototype Lab Inventory*** *and usage typically adds 5% to maintain experimentation stock of multiple device types for board debug. The GAL device multiplier is 1%, since the device can be reused over and over again.*

4 ***Incoming QA Test*** *and programs cost more than may be immediately apparent, with a 7% adder. The generation and maintenance of the software and hardware for the dozens of bipolar devices is considerably more expensive than the single GAL device software required. No sample-program waste is induced. Only the aspects of handling are required for GAL devices, resulting in a reduction to 1% (or 0%, if you eliminate the incoming QA operation entirely).*

5 ***Inventory Management*** *includes shelf space, safety stock, depreciation, obsolete stock write-off and personnel to maintain adequate control of the units. A typical overhead is 10%. The simplfied GAL operation involves no safety or obsolete stock and a minimum of device types, adding a maximum 2% to 3% to overhead.*

6 ***Programming and Test*** *includes all handling and hardware expenses. Inventory issuance, counting and returns, handling during the program/test operation, labels, and paperwork contribute to a 12% multiplier. The 100% yielding, generic GAL approach reduces the problem to 4%.*

7 ***Programming Yield Fallout*** *is directly observed as bad units. A typical bipolar range is 1% to 4%. GAL devices have 0% yield fallout — guaranteed.*

8 ***Functional Yield Fallout*** *is detected by the device programmer immediately after programming, through the use of test vectors, and can average 1% to 3%. GAL devices guarantee 0% functional fallout. It should be noted that using test vectors does not screen out inadequate for AC performance, which will be manifested as a board failure.*

9 ***Reject Disposition*** *overhead runs 5% to obtain replacements and credits for fuse-link devices. Zero rejects with GAL devices eliminates costs associated with reject disposition. Notice that the cumulative multiplier for only the program/test/reject of fuse-link devices is 1.10, compared with GAL devices' 1.00 multiplier.*

10 ***Board-Level Failures*** *are typically where AC failures are detected. The 'Factor of Ten Rule' exacerbates the impact of the observed 1% to 4% fallout to an overall cost impact of 7% to 10%. GAL devices exhibit no board-level fallout (and therefore no cost impact). Board throughput is also a major cost contributor, with typical reworks of 20% to 30% a consequence of PAL quality levels.*

11 ***System-Level Failures*** *add 8% to 15% to the PLD cost, taking into consideration a 100x 'Factor of Ten Rule' multiple. GAL devices again provide 100% yields, and therefore exhibit no system-level-failure cost impact.* □

INTRODUCTION

The dictionary definition of metastability is "a situation that is characterized by a slight margin of stability." When applied to bi-stable (digital) logic, the term refers to an undesirable marginally stable output state between VIL max and VIH min.

Metastability can occur in bi-stable storage elements (registers, latches, memories, etc.) when setup and/or hold times are violated. Since setup and hold times vary with temperature and operating voltage, among other factors, the times referred to here are not the min/max numbers printed in data sheets, but rather the actual times for the given set of operating conditions. Typical applications where such times are likely to be violated include bus & memory arbiters, interfaces, synchronizers, and other state machines employing asynchronous inputs or asynchronous clocks.

Metastability manifests itself in a number of different ways. Common responses are (shown as they might be captured on a digital oscilloscope in Figure 1): runt pulse (1a), decreased output slew rate (1b), output oscillation (1c), and increased clock-to-output time (1d). By definition, the phenomenon of metastability is statistical in nature. Not only is entry into the state uncertain, but the time spent there is also variable.

Because PLDs are commonplace in today's designs, a thorough understanding of their metastable behavior is crucial. In some applications, output anomalies shorter than one clock cycle may be acceptable, but in applications where the register output is used as a control signal (clock, bus grant, chip select, etc.) for other circuitry, faults such as runt pulses and oscillation cannot be tolerated.

This report will not study the causes or characteristics of metastability in great detail; excellent material has already been prepared on this subject [1-5]. Rather, this report will introduce a mathematical model for the metastable phenomenon, discuss potential test methodologies, present and compare test results from various bipolar and CMOS PLDs, and discuss how to interpret the data. This report will close with suggestions on how to design metastable tolerant systems.

DERIVATION OF CONSTANTS

The basic premise of all metastability models is that a device's output is more likely to have settled to a valid state in time(t) than in time(t-n). In fact, the failure probability distribution follows an exponential curve. Figure 2 shows a typical failure frequency plot.

It is accepted [1] that metastable failures can be accurately modeled by the equation:

$$\log(MTBF) = \log(MAX) - b(\Delta - \Delta o) \quad (1)$$

In this equation, MAX represents the maximum failure rate for a particular environment, Δ is the time delayed before sampling the DUT (Device Under Test) output, and Δo is the time at which the number of failures starts to decrease. On a failure frequency plot (such as the one in Figure 2), Δo represents the knee of the curve. The constant b is rate at which the frequency of failures decreases after the knee is reached.

Recall that:

$$\log X = a \ln(X), \text{ where } a = \log(e)$$

Substituting this into (1):

$$a \ln(MTBF) = a \ln(MAX) - b(\Delta - \Delta o) \quad (2)$$

MAX is related to the clock frequency (fCLOCK) and data frequency (fDATA). That is,

$$MAX = (k1 * fCLOCK * fDATA) \quad (3)$$

Substituting (3) into (2) and applying some algebra:

$$a \ln(MTBF) = a \ln(k1 * fCLOCK * fDATA) - b(\Delta - \Delta o)$$

$$\ln(MTBF) - \ln(k1 * fCLOCK * fDATA) = -b/a(\Delta - \Delta o)$$

$$\ln(MTBF/(k1 * fCLOCK * fDATA)) = -b/a(\Delta - \Delta o)$$

$$MTBF/(k1 * fCLOCK * fDATA) = e^{-b/a(\Delta - \Delta o)}$$

Setting k2 = b/a and rearranging the equation yields:

$$MTBF = k1 * fCLOCK * fDATA * e^{-k2(\Delta - \Delta o)} \quad (4)$$

When used with equation (4), the constants k1, k2, and Δo, completely describe a particular device's metastable characteristics; they indicate how quickly a device can resolve the metastable condition. Devices which transition out of the metastable region quickly are characterized by a

small Δo and a large k2.

The constant k1 is peculiar to the test apparatus (it can be thought of as a "scaling factor"). The maximum metastable failure rate (MAX) is limited by fCLOCK; a failure cannot occur if the device isn't clocked. Likewise, it is true that a metastable failure cannot occur unless data has changed. So, if fDATA < fCLOCK, then MAX = fDATA. This was the case in the test fixture Lattice used (fCLOCK=10MHZ, fDATA=2.5MHz). Substituting MAX = fDATA back into equation (3) yields: k1 = 1/fCLOCK, so k1 = 100ns for our tests.

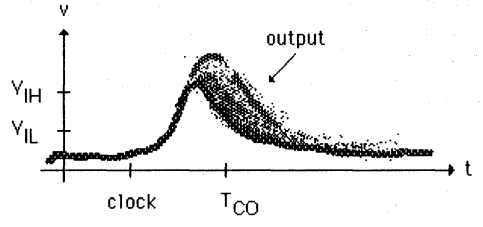
TEST FIXTURE

The goal of testing a particular device's metastable characteristics is to generate real numbers for the constants k2 and Δo. To do this, the device must first be forced into the metastable state. This is done by intentionally violating setup and/or hold times. Once metastable, the output can be observed on an oscilloscope or used to increment an event counter.

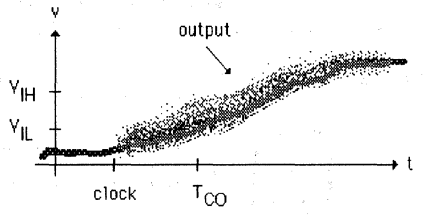
Traditional Approach

One approach to characterizing a device's metastable behavior employs a test fixture similar to that shown in Figure 3a. In such a fixture, data to the device includes a "jitter band" so that the device sees changing data as it is clocked. The DUT output is fed to a window comparator to determine when it is in the metastable region (between VIL max and VIH min). The comparator output can be sampled periodically and used to increment an event counter.

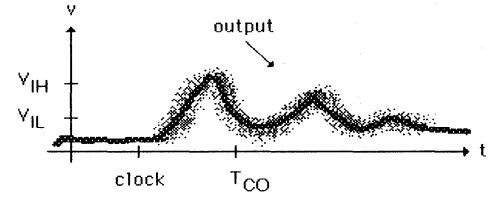
This method of testing, though it directly yields MTBF



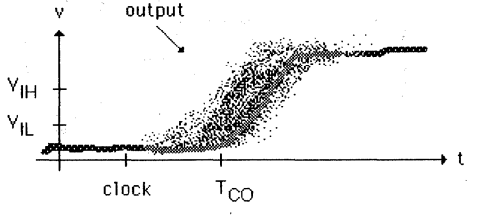
1a. Runt Pulse



1b. Decreased Slew Rate



1c. Output Oscillation



1d. Increased T_{CO}

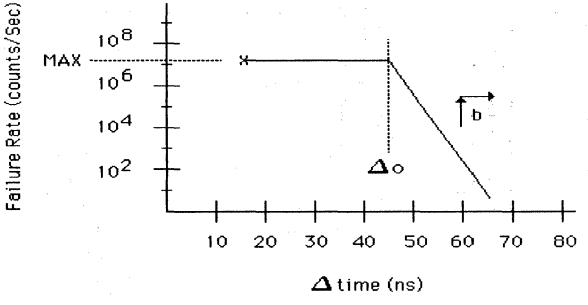


Figure 2. Typical Failure Frequency Plot

numbers, has some drawbacks. The first is that it does not distinguish between the different types of metastable behavior (runt pulse, oscillation, slow rise/fall time, delayed transition), and it may have difficulty detecting every type. Also, the registers used in the detector circuit itself may become metastable, which would adversely affect the results.

A New Approach

The test method used to gather data for this report used the circuit shown in Figure 3b. The tester employed an "infinite precision" variable delay circuit to control clock placement with respect to data. This arrangement allowed exact worst case placement of the clock, so as to induce metastability with nearly every clock pulse.

Using a digital oscilloscope (Tektronix 11402) in point accumulate mode, metastable failures were recorded over a lengthy period of time. A hardcopy was then made and the constants empirically obtained (details below).

The oscilloscope approach, being visual in nature, enables the designer to make educated decisions regarding maximum clock and data rates, as well as the suitability of using the output to drive other circuitry. The five minute sample period used in our tests contained approximately 750 million failures. Much longer sample periods were evaluated, but they provided no perceptible gain in usable information.

A slight disadvantage of this approach is that extracting k2 and Δo values from the hardcopies is not straightforward. Because each point on the hardcopy can represent any number of actual samples (between one and 1.5 million), one cannot simply count the points at time(t) for the MTBF at that time (although, in the case of the scattered points, the probability is low that a single isolated point represents more than one sample).

To generate values for k2 and Δo, it was necessary to refer to previous metastability studies [1]. By studying the output plots of devices with known constants, certain relationships were established. For example, it was determined that Δo represents the time from the leading edge of the output until

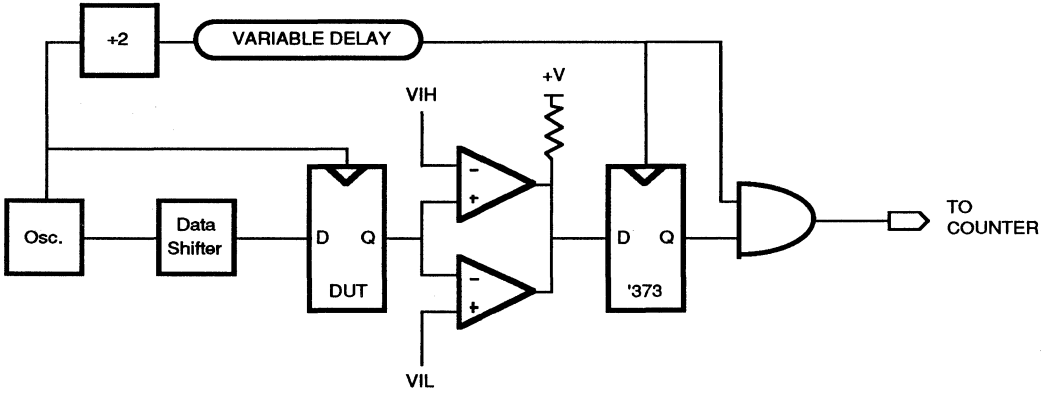


Figure 3a. Traditional Metastability Test Circuit

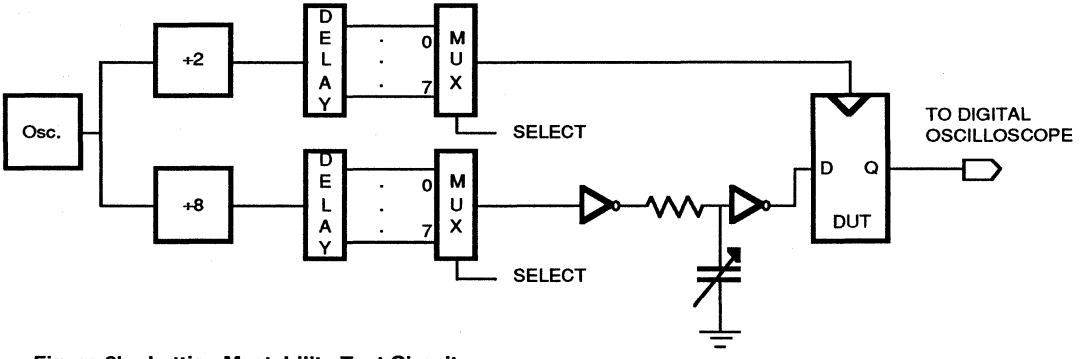


Figure 3b. Lattice Mestability Test Circuit

the "dot density" starts to decrease measurably. It should be noted that Δo in previous studies included device propagation delays, whereas in our test it does not.

The time from Δo until the dot density equals zero was defined to be the "time to metastable release" or simply time(r). The relationship between k2 and time(r) is given below in (5), and shown graphically in Figure 4. Recall that MAX=2.5x10^6 and a=log(e).

$$k2 = \log(MAX)/(time(r)*a) = 14.73/time(r) \qquad (5)$$

INTERPRETING THE RESULTS

In addition to examining E²CMOS GAL devices, this study also tested several bipolar PAL devices as well as other CMOS PLDs. To insure that the results of this study would be relevant, all necessary precautions were observed: the devices were of recent vintage and were acquired blindly through distributors; multiple samples of each device were tested and the results combined; all devices had either fixed 16R8 architectures or were configured to emulate the 16R8 architecture; the devices were programmed from the same JEDEC fuse map file (the source equations and the JEDEC fuse map file are presented in Listing 1).

Plots 1 through 4 on the following pages are some of the oscilloscope plots generated for this study. The top waveform in each plot is the clock signal and the middle trace is the data input. The horizontal scale is 10ns per division, so the exact data setup time that caused the metastable condition can be read directly. The vertical scale is 2V per division for the top two traces, and 1V per division for the bottom trace. Only the bottom trace is aligned with the voltage scale on the left margin of the plot.

The bottom waveform in each plot is the device output (the only signal captured in point accumulate mode). In every case, the output signal plot shows two stable levels after the transition. This is a direct result of the "indecision" caused by metastability; on some cycles the output settled to a high level, while on others it settled to a low level.

Plot 1 shows the response of a bipolar PAL16R8B (15ns). Notice the very well defined runt pulse (this correlates with previous data gathered on similar devices by the manufacturer [1]). The absence of a secondary trace along ground indicates that the output always starts to transition to a high level, even when it finally settles to a low level. This characteristic makes the device unsuitable for use in control path applications (when metastability is possible). All of the bipolar parts examined showed similar results.

Plot 2 is from a UV-EPLD. This CMOS device, as did all CMOS PLDs Lattice tested, exhibited characteristics far superior to bipolar parts. This can be attributed, in part, to the higher switching speed of CMOS logic. GAL devices, for example, have output slew rates approaching 5V/ns, compared to about 1V/ns for bipolar devices.

Plot 3 is from a GAL16V8-15 and Plot 4 is from a

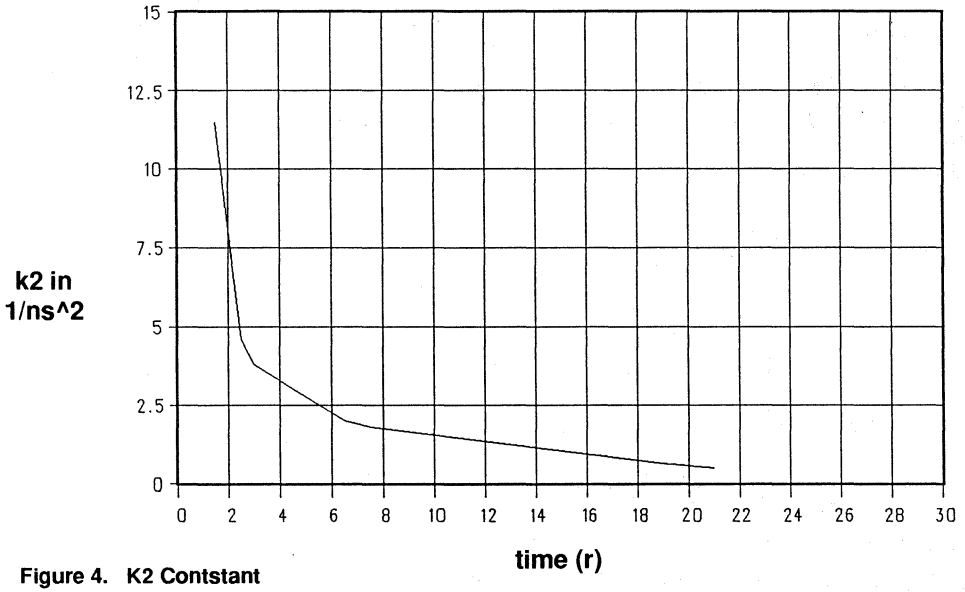


Figure 4. K2 Contstant

GAL39V18ES. Aside from the fact that setup time violations may cause tCO to increase by a small (but random) amount, the outputs are very clean and well behaved. The fact that there are no runt pulses or other anomalies is extremely significant, as the GAL39V18 not only allows asynchronous clocking, but encourages that activity. Compare Plots 3 & 4 with Plot 2. Just as the characteristics of CMOS PLDs (in general) are superior to those of bipolar PLDs, the metastable response of GAL devices is noticeably better than that of UV-CMOS EPLDs.

For reference purposes, Plots 5 through 7 are included. Plot 5 shows a normal (ie. non-metastable) GAL16V8-15 transition, and Plot 5 a normal PAL16R8B transition. Plot 7 is from a TTL flip-flop (TI7474). For consistency, only rising edges have been shown. Our tests also covered falling edges which, in general, were interesting but did not provide any additional information.

For a more quantitative look at the phenomenon of metastability, refer to the table beneath each plot. These tables list the measured values of the constants Δo and k2 for the device whose plot is shown, and for similar devices. Recall that large k2 and small Δo values are desirable. The numbers in the tables correlate closely with the results of earlier tests [1,5], confirming the validity of our test method.

Since all current GAL devices possess very similar register and output buffer circuitry, and all are fabricated using the same basic process, the data shown in Table 1 for the GAL16V8 is considered applicable to all devices and speed grades in the GAL family.

USING THE RESULTS

If a register enters the metastable state in a system, then data was obviously unstable as the register was being clocked. The argument over which data should have been captured (old or new) is academic as the register will randomly pick one or the other. Signals in most asynchronous systems are active for more than one clock cycle, so if they are missed initially, they could be captured on a subsequent clock cycle.

It is the task of the state machine designer to take adequate precautions against metastability causing illegal states to be entered. One way to do this is by using "gray codes" when ordering states. Gray code state equations allow only one state bit to change during a state transition. Thus, the worst metastability could do would be to delay a state transition by one clock cycle. If more than one bit were allowed to change, the outcome would be purely random, and probably illegal. Figure 5 shows examples of both cases.

Other solutions are to externally (or internally) synchronize the asynchronous signals, or to increase cycle times to allow time for metastable outputs to settle. An example of the latter solution is given below.

It is worth noting at this point that state machines (synchronous or asynchronous) can fail for reasons other than metastability. A not insignificant component of a PLD's specified setup time is directly attributable to internal data skewing [2]. Data skewing is the inevitable result of differing signal path lengths, loading conditions, and gate delays. Stated another way, each input to output path has its own set of actual AC specifications. If insufficient setup time has passed, different "versions" of the same data may be present at the inputs of different registers as they are clocked. A good example of this is:

```
Output_Pin19 := Input_Pin2;
Output_Pin15 := !Input_Pin2;
```

If clocked at precisely the right moment after an input transition, one register will capture old data while the other captures new data, resulting in a system failure. This condition, though also the result of a setup time violation, should not be confused with metastability (the "incorrect" data that is captured has normal output characteristics); it is, pure and simply, the result of a violation of specifications. Incidentally, there is less than 1.5ns of skew between the various paths through a 15ns GAL device.

Example

To determine the maximum clock rate (given an acceptable error rate) that a particular device will allow in an asynchronous environment, equation (4) is used. For example, the system shown in Figure 6 utilizes a 9600 baud (bits/sec) asynchronous data stream. The system clock period is tCO+tPD+tSU+Δ. For a MTBF of 1 year:

$$3.2\text{x}10\text{-}8 = [(1\text{x}10\text{-}7)(1/(\Delta+49))(9600)]e^{-[9(\Delta-2)]}$$

Solving for Δ yields Δ=2.796ns, or about 3ns, for a cycle time of 52ns. Referring back to Plot 2, the additional delay of 3ns intuitively makes sense. Remember, in terms of setup and hold time violations, the oscilloscope plots were made under worst case failure conditions; the scattered dots could represent MTBFs of days, years, or even millenniums in a typical asynchronous environment.

Due to the extremely quick metastable settling times of GAL devices, a relatively small increase in the cycle time will produce a dramatic improvement in reliability. In the above example, by increasing Δ to 4ns, a MTBF of 15,556 years is achieved, while a Δ of 5ns yields an MTBF of 47.25 million years!

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2. K.Rubin (Force Computers), "Metastability Testing in PALs," Wescon/87 Conference Record (San Francisco, November 17-19, 1987). Los Angeles: Electronics Conventions Management, Inc, 1987, pp 16/1 1-10.

3. K.Nootbaar (Applied Microcircuits Corp.), "Design, Testing, and Application of a Metastable Hardened Flip-Flop," ibid., pp 16/2 1-9.

4. J.Birkner (MMI), "Understanding Metastability," ibid., pp 16/3 1-3.

5. R.K.Breuninger, K.Frank, "Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families," application note SDAA004, Texas Instruments, 1985.

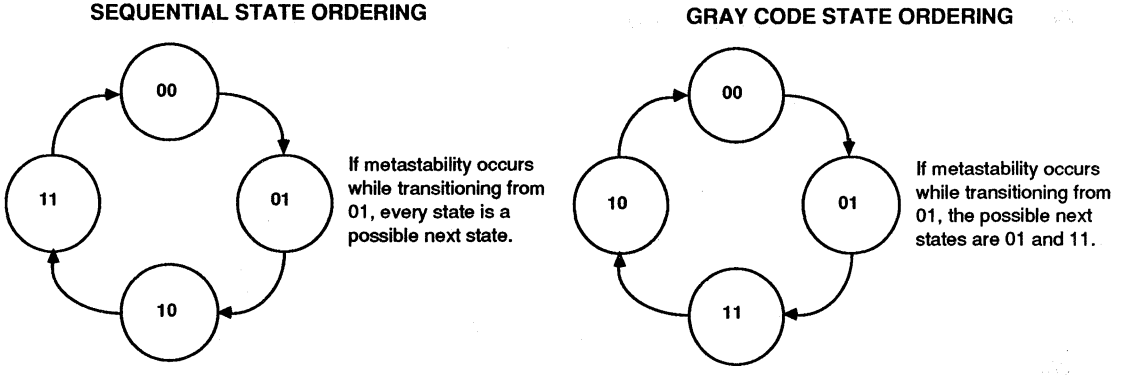


Figure 5.

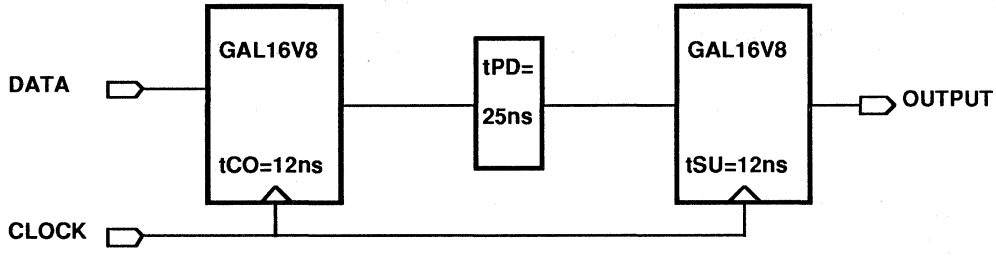


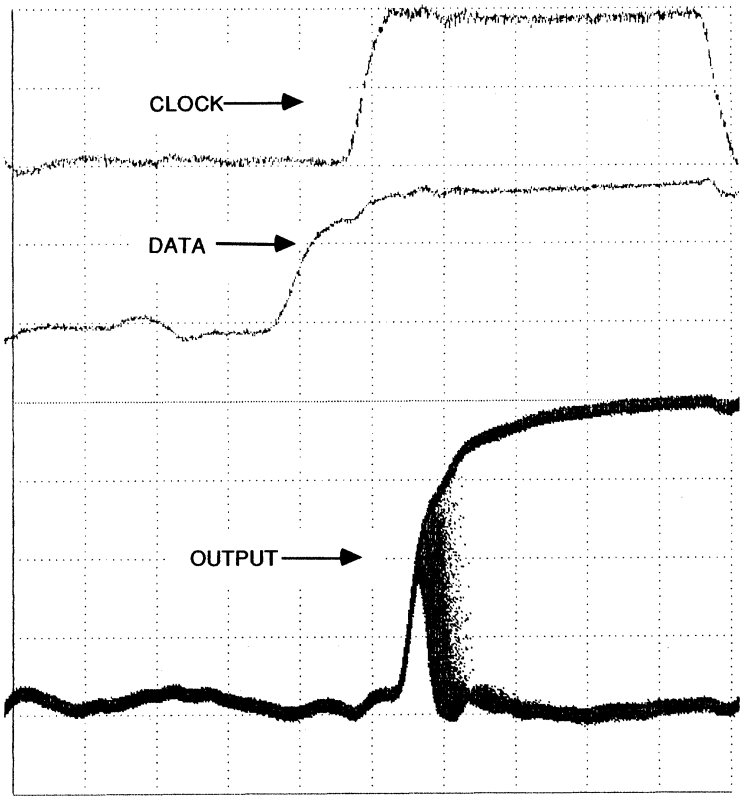
Figure 6.

```
MODULE metastable

TITLE 'Metastable Test
Pattern'

uOO Device 'P16R8';

d       PIN   2;
q1,q2   PIN   12,19;
        EQUATIONS
q1 := d;
q2 := d;
        End metastable
```

Listing 1a. Source equations

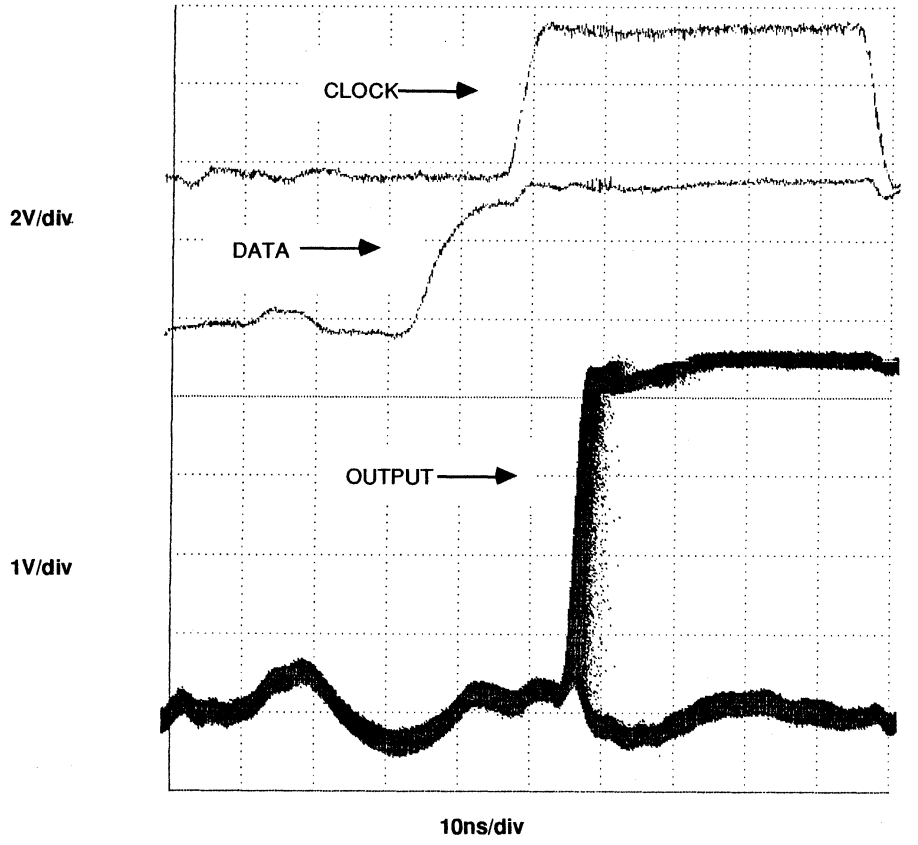
```
JEDEC file for: P16R8
Metastability Test Pattern*
QP20* QF2048* F0*
L0000 10111111111111111111111111111111*
L1792 10111111111111111111111111111111*
C07F4*
```

Listing 1b. JEDEC file



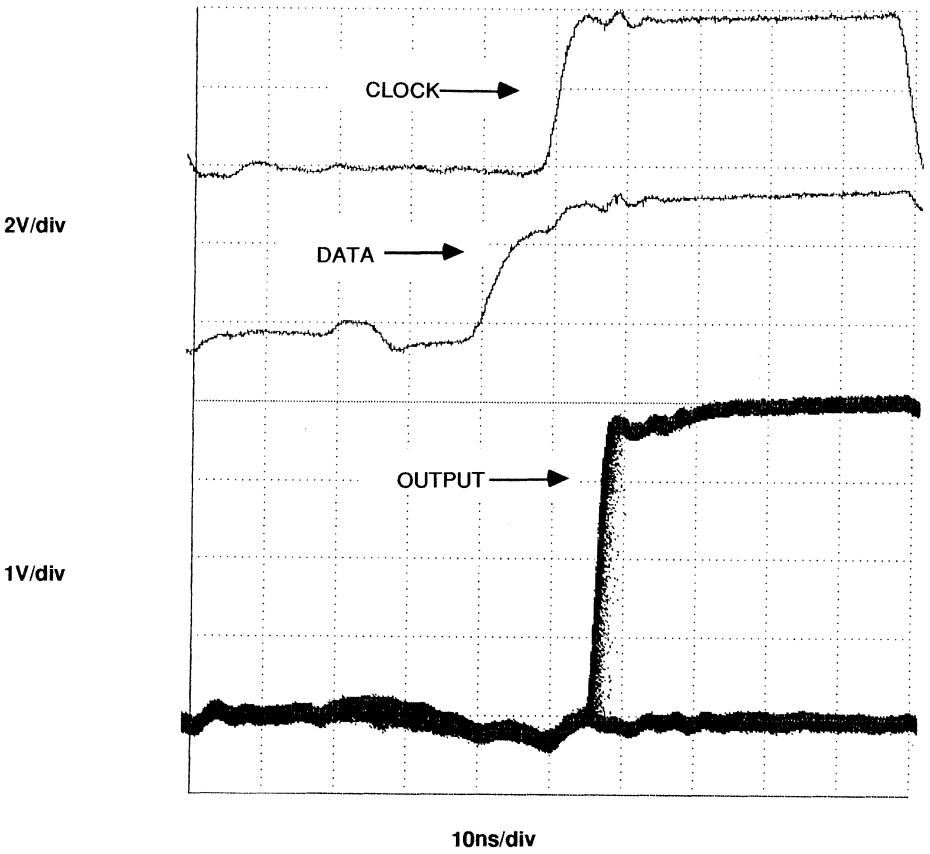
Plot 1. PAL16R8B

Part #	Date Code	∆o (ns)	k2/ns^{-2}
PAL16R8A	8721	11	2.0
PAL16R8B	8722	6	3.0
AmPAL16R8A	8631	8	1.9
TIBPAL16R8-15	8723	5	1.25



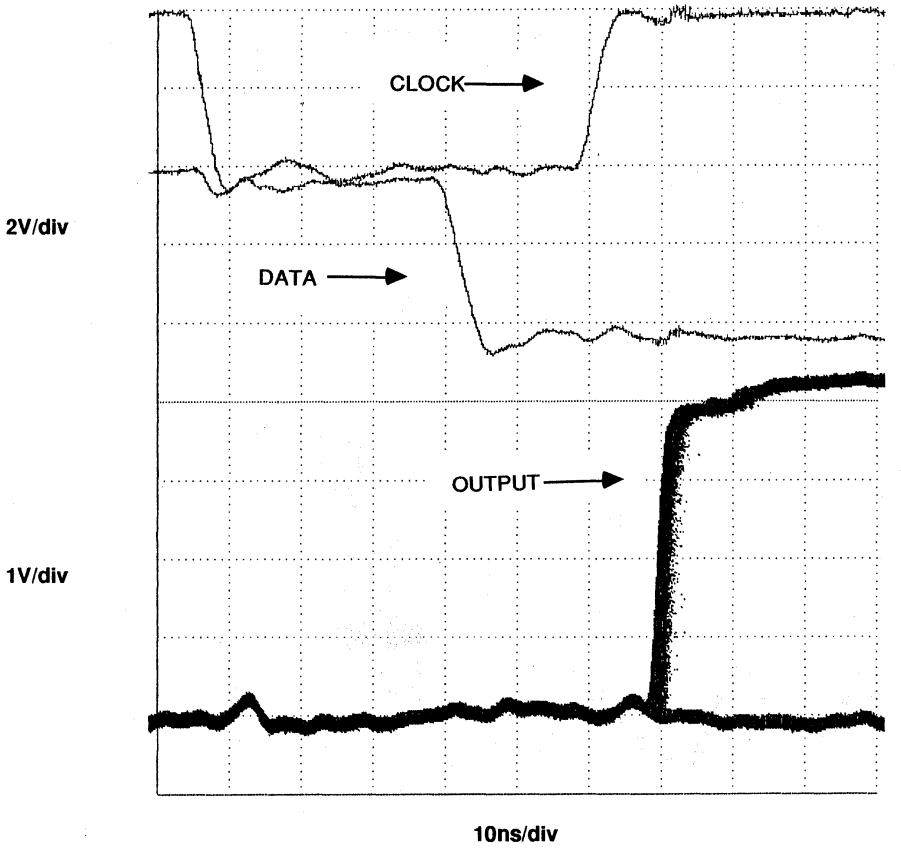
Plot 2. CYPALC16R8-25

Part #	Date Code	∆o (ns)	k2/ns^{-2}
CYPALC16R8-25	8622	3	3.75



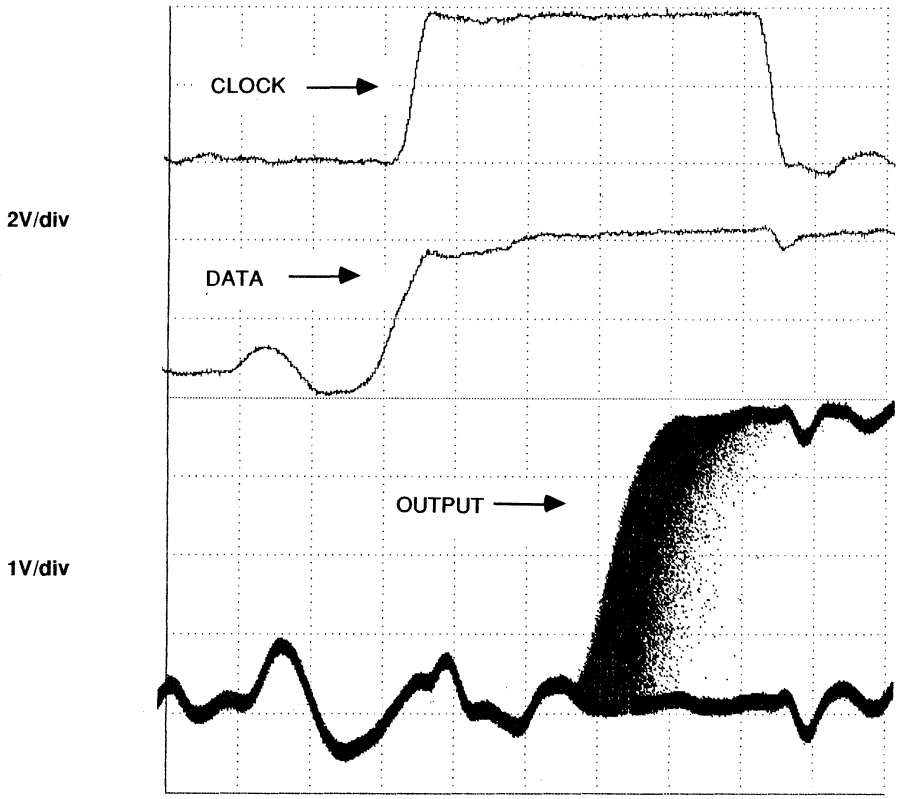
Plot 3. Lattice GAL16V8-15L

Part #	Date Code	△o (ns)	k2/ns^{-2}
GAL16V8-15	8731	2	8
GAL16V8-25	8730	2	8



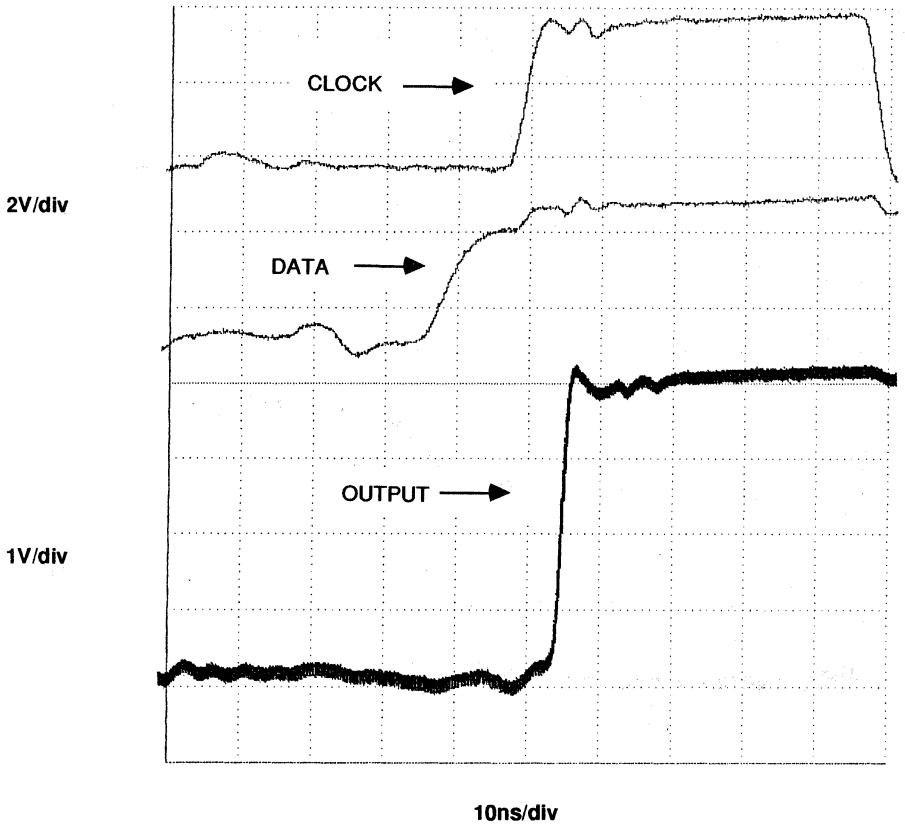
Plot 4. Lattice GAL39V18ES

Part #	Date Code	∆o (ns)	k2/ns^{-2}
GAL39V18ES	8652	1	6.25

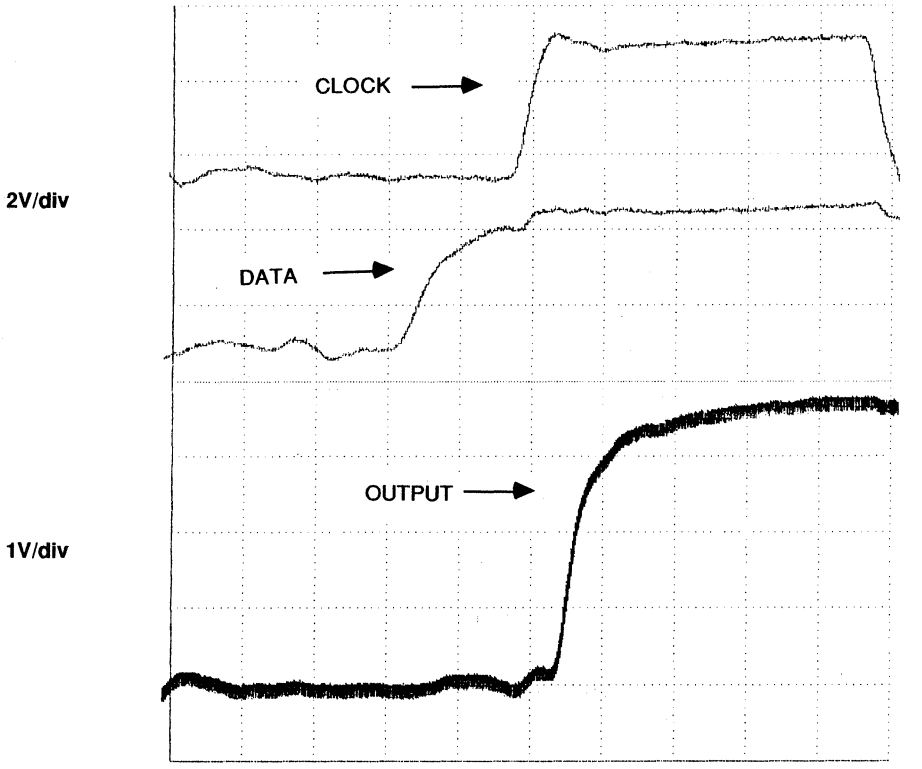


Plot 7. 7474

Part #	Date Code	∆o (ns)	k2/ns^{-2}
SN7474N	7615	6	1.3
9N74/7474	7341	7	1.25



Plot 5. Normal Lattice GAL16V8-15L Transition



Plot 6. Normal PAL16R8B Transition

Although it is possible to program GAL® devices manually, LATTICE strongly recommends the use of approved programming hardware and software. Programming on unapproved equipment will generally void all guarantees.

Approved equipment includes LATTICE programming algorithms that program the array, automatically configure the architecture control word, and track the number of program cycles each device has experienced (this information is stored within each GAL® device). This in turn assures data retention and reliability. Contact the factory for specific conditions which must be met to gain programming equipment approval, the most current list of approved GAL® development tools, or other current programming information.

PROGRAMMER/DEVELOPMENT SYSTEMS

VENDOR	MODEL	16V8	20V8	16Z8	39V18	16V8A	20V8A
DATA I/O	M29B	v04	v04	v04	**	**	**
	PT 303A-011	v03	v03	v03	**	**	**
	PT 303A-009	†	†	n.a.	n.a.	n.a.	n.a.
	Unisite 40	v1.7	v1.7	**	**	**	**
	M60A	v11	v11	**	**	**	**
	M60H	**	**	**	**	**	**
DIGITAL MEDIA	IQ-180	**	**	**	**	**	**
INLAB	MODEL 28	**	**	**	**	**	**
JMC	Promac P3	**	**	n.a.	n.a.	n.a.	n.a.
	Promac P11	**	**	**	**	**	**
KONTRON	MPP80S	**	**	**	**	**	**
LOGICAL DEVICES	Allpro	**	**	**	**	**	**
OLIVER ADVANCED ENG.	Omni-64	**	**	**	**	**	**
PROGRAMMABLE LOGIC TECH.	Logic Lab	2.10	2.10	2.10	2.10	**	**
QWERTY INC.	GPR-1000	2.0	2.0	n.a.	n.a.	2.3	2.3
	GPR-1000+	1.0	1.0	n.a.	1.0	1.0	1.0
STAG	ZL30A/ZL32	30A21	30A21	**	**	**	**
	PPZ	**	**	**	**	**	**
SYSTEM GENERAL	SGUP-85	**	**	**	**	**	**

SOFTWARE DEVELOPMENT TOOLS ††

VENDOR	PACKAGE	16V8/A	20V8/A	16Z8	39V18
CAPILANO COMPUTING	LPLC	††	††	n.a.	n.a.
DATA I/O	ABEL	v1.13	v2.0	v3.0	v3.0
	PLDtest	††	††	††	n.a.
	DASH-ABEL	v1.0	v1.0	v1.0	n.a.
HEWLETT-PACKARD	PLD Design sys.	††	††	n.a.	n.a.
ISDATA	LOG/iC	**	**	**	**
MINC	PLDesigner	**	**	**	**
MONOLITHIC MEMORIES	PALASM	††	††	n.a.	n.a.
PERSONAL CAD SYSTEMS	CUPL	v2.1	v2.1	v2.15	v2.15
PISTOHL ELECTRONICS	E.LP.	††	††	n.a.	n.a.
PROGRAMMABLE LOGIC TECH.	FAST MAP	v2.1	v2.1	n.a.	n.a.
	LC-9000	v1.5	v1.5	n.a.	v1.5
QWERTY INC.	PLAQ	1.0	1.0	n.a.	1.0

** Revision being qualified
† Lattice modified hardware only
†† When emulating PAL® devices any revision of the software can be used to create the JEDEC file. Most programming hardware will automatically configure the GAL® architecture or use the PALtoGAL™ software utility to modify the JEDEC file before programming.

Qualifications and revision levels effective 2/15/88

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Fax: (408) 279-3752

Pistohl Electronics
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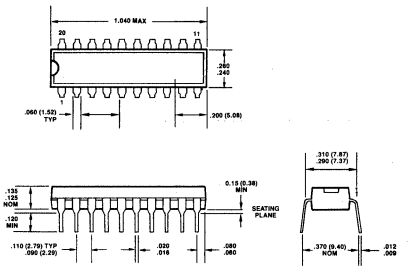
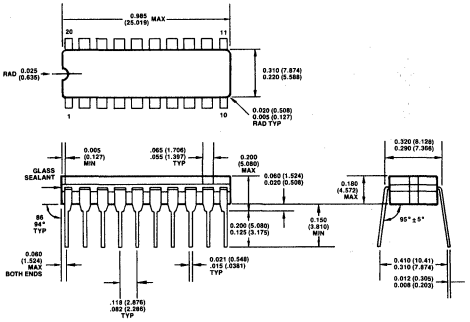
NOTE: Lattice Semiconductor assumes no responsibility for the suitability or accuracy of third-party development tools. Lattice will provide, upon request, a list of qualified and approved suppliers indicating that a factory qualification of the tool has been performed.

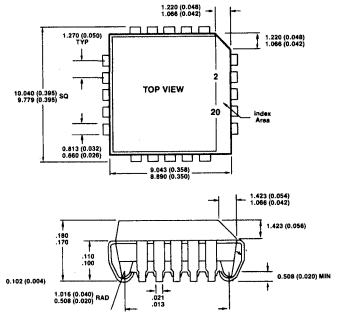
20-PIN, 300-MIL PLASTIC DIP



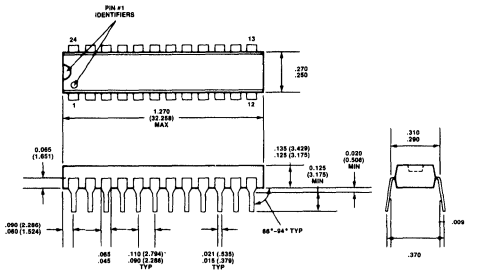
20-PIN, 300-MIL CERDIP



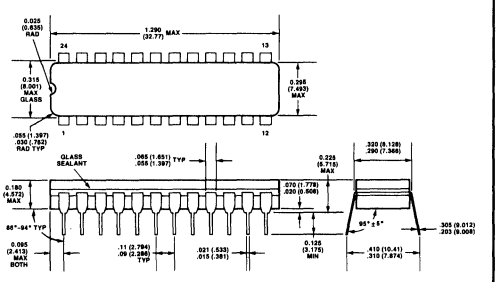
20-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



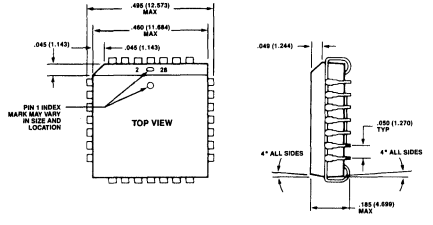
24-PIN, 300-MIL PLASTIC DIP



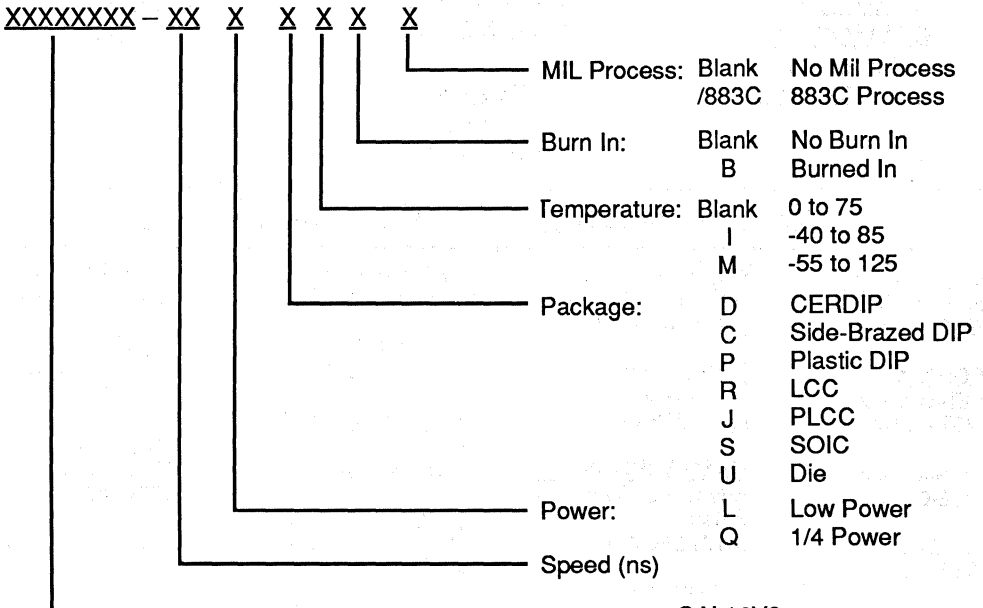
24-PIN, 300-MIL CERDIP



28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



PART NUMBER DESCRIPTION



Note 1: All fields are adjacent with no irbedded spaces.
The Mil process, Burn-in, and Temperature fields are optional.
All other fields must be marked.

Note 2: When "883C" is indicated , "M" and "B" are excluded.

Note 3: "B" refers to 168 hours burn-in be yond the standard amount of burn-in required for commercial product reliability requirements at that time.

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