

## New Product Data Sheets

Data Sheet	Description
<a href="#">ispLSI 2064V</a>	New 3.3 Volt ispLSI Device: 70 or 37 I/O, 64 Macrocells, ispLSI 2000 Architecture
<a href="#">ispLSI 2096V</a>	New 3.3 Volt ispLSI Device: 104 I/O, 96 Macrocells, ispLSI 2000 Architecture
<a href="#">ispLSI 2128V</a>	New 3.3 Volt ispLSI Device: 138 or 74 I/O, 128 Macrocells, ispLSI 2000 Architecture
<a href="#">ispLSI 3160</a>	New ispLSI Device: 160 I/O, 160 Macrocells, ispLSI 3000 Architecture
<a href="#">ispLSI 3256E</a>	New ispLSI Device: 258 I/O, 256 Macrocells, ispLSI 3000 Architecture
<a href="#">ispLSI 3256A</a>	New ispLSI Device: 128 I/O, 256 Macrocells, ispLSI 3000 Architecture

## Updates to Existing Data Sheets

Data Sheet	Description
<a href="#">ispLSI 1016E</a>	Addition of New 80 MHz Speed Grade
<a href="#">ispLSI 1048C</a>	Final SMD Numbers for Military Grade Devices
<a href="#">ispLSI 2032</a>	Addition of New 180 MHz Speed Grade
<a href="#">ispLSI 2032V/LV</a>	Addition of New 100 MHz Speed Grade
<a href="#">GAL16V8</a>	Addition of New Speed Grades for the 16V8D
<a href="#">GAL16LV8</a>	New 5V Compatible Inputs for GAL16LV8D
<a href="#">GAL20LV8</a>	New 5V Compatible Inputs for GAL20LV8D
<a href="#">GAL22LV10</a>	New 5V Compatible Inputs for GAL22LV10D
<a href="#">ispGAL22V10</a>	Addition of 28-Pin SSOP Pin Configuration
<a href="#">pDS Software</a>	Addition of Multiple Edit Windows
<a href="#">ISP Synario System</a>	New Support for Windows 95 and Additional Devices
<a href="#">pDS+ Synario Software</a>	New Support for Windows 95 and Additional Devices

## New Application Notes

[Lattice ISP in Cellular Switching Stations](#)

[Implementing Lattice ISP and Boundary Scan Daisy Chains](#)

[The Basics of One-Wire ISP with an ISP-IrDA Example](#)

[DMA Controller Using an ispLSI 6192SM](#)

[PCMCIA Interface in an ispLSI 2064](#)

# What's New

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Multiple FIFO Configuration in ispLSI 6192

24-Bit Adder Implementation in a CPLD

ispLSI 3192 to 6192 Design Conversion

Interfacing SDRAMs to Pentium Processors

Optimizing an ispLSI Design

## Other

Document	Description
<a href="#">Tape and Reel Specifications</a>	Addition of Tape and Reel Specifications for TQFP, PQFP and MQFP Packages
<a href="#">Thermal Management</a>	Addition of Thermal Resistance Specifications for 48-pin TQFP, 160-pin PQFP and 304-pin MQFP Packages
<a href="#">Package Diagrams</a>	Addition of 160-pin PQFP Diagram
<a href="#">Worldwide Web Site</a>	New Section Describing Lattice's Worldwide Web Site