21154 PCI-to-PCI Bridge

Specification Update

July 2004

Notice: The 21154 may contain design defects or errors known as errata which may cause the behavior of the 21154 to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 278295-017

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Revision History

Date	Version	Description
July 2004	017	Updated Errata 9. description.
2/25/05	016	The following changes have been made in this version: • Updated status for Errata 7. and Errata 9. on page 11. • Revised Pin 1 Designator Change description in "Specification Changes" on page 11. • Added Errata 10. "Secondary Address pins are driven incorrectly during reset." on page 21. • Added documentation change "Updated Version of PCI Local Bus Specification" on page 36.
3/1/02	015	The following changes have been made in this Specification Update: • Updated Errata table status column on page 11. Updated status for Erratas 1 through 6. • Added Recommendation #1 fix for Errata 6 "Secondary Clocks Outputs s_clk_o<9:0> May Not Start-up Properly Under Some Conditions". Moved previously existing fix recommendation for Errata 6 to become the second recommendation. • Added Errata 9, "21154AE/BE May Experience Performance Problems or Hangs when P_VIO = 3.3V" on page 20. • Updated Specification Clarification 1 title description on page 23. • Updated links in this document.
6/25/01	014	Updated Errata #1 description in Table , "Errata" on page 11 and added new worst-case conditions tables for Tval description,Section 1 on page 15
6/8/01	013	Updated Errata #1 title description in Table , "Errata" on page 11 and added worst-case conditions for Tval description,Section 1 on page 15

Date	Version	Description
5/8/01	012	Added information for AE and BE versions of the 21154 product
		Updated Errata #5 AC Marking state in Table , "Errata" on page 11
		Updated status state for Errata #4, #5, #6, and #8 in Table , "Errata" on page 11 and in descriptions in "Errata" on page 15
		Updated descriptions for Errata #1 and #3 in Table , "Errata" on page 11
		Added last two rows to Table 1, "21154 Markings" on page 14
		Updated description for "Tval Timing Issues When Running at 66 MHz for All PCI Signals. Tval timing improved on the 21154BE." on page 15
		Updated description for "Hold Time Issues for All PCI Signals (Both Bused and Control) on the 21154." on page 16
		Added changes #2, #3, and #4 in "Specification Changes" on page 22
		Added toTable , "Documentation Changes" on page 13 that include: • "Updated Version of PCI Local Bus Specification" on page 35 • "Section 4.1, Updated s_clk and p_clk description" on page 35 • "Section 4.2, Updated Clock Outputs" on page 35 • "Section 4.4.1, Added Note at End of Section." on page 35 • "Section 4.5, Table 5 Product Part Numbers have been updated." on page 36. ***Note:*** These documentation changes have been implemented in Version 003 of the *21154 PCI-to-PCI Bridge Hardware Implementation Application Note*.
4/30/01	011	The Steppings columns in the "Errata" table, "Specification Changes" table, and "Specification Clarifications" on page 11 were changed to Markings to more accurately reflect the revisions of the component.
		Errata #3 (Setup Issues With PCI Control Signals When Running at 66 MHz on the 21154BC) of this Specification Update was found to be invalid and is now listed as Fixed.
		The term "REV_ID6" was removed from the problem section of Errata 3, Setup Issues With PCI Control Signals When Running at 66 MHz on the 21154BC. on page 16.
		Errata 7, GPIO 66 MHz Timing May Cause Secondary Clocks to be Disabled was added.
		Errata 8, Bus Conflict Occurs During Configuration on AGP Port of Some Chip Sets. was added.
		Documentation Changes 12, Section 10.2, Secondary Clock Control, Figure 19, 15, and 18, Section 4.4.1, Serial Clock Mask Shift, Figure 3 were modified, and documentation change 15, Section 10.2.1, Mask and Load Shift Timing Events for 66 MHz Operation was added.
12/15/00	010	Documentation changes 17, 18, and 19, referenced the wrong document number. The correct document number has been updated in the Summary Table of Changes. All references to the 21554 have been changed to 21154. Figures in documentation changes 13 and 20 have been updated. Errata 3 now has stepping C included as an errata in the Summary Table of Changes.
11/13/00	009	Corrected speed settings for 21154AB/AC/BC Markings.
10/02/00	008	Added errata 6.

Date	Version	Description
9/18/00	007	Modified description of trst_l, tms and tdi signal, added a new section on JTAG testing. Modified the description of the trst_l specification clarification. Modified order of serial stream in Figure 20, Clock Mask and Load Timing. Added note for pull-up resistor for output clocks. Added specification change to PBGA package dimensions for coplanarity maximum value. Added documentation changes 21 and 22: descriptions of two signals when secondary bus speed set for 66 MHz.
2/7/00	006	Modified order of serial stream in table 34, gpio Serial Data format. Modified the description for Dword bit 0. Modified Figure 19, Example of gpio Clock Mask Implementation on the System Board. Modified Figure 20, Clock Mask and Load Shift Timing. Clarified definition of trst_l signal.
12/14/99	005	Modified description of the clamp circuit errata. Added 64-bit data bus width errata.
9/1/99	004	Added documentation change item 6 for 66 MHz operation. Updated Hold time errata. Added clamp circuit errata.
8/11/99	003	Tsetup test conditions found to be invalid. Device meets 3 ns Tsetup limit on all pins.
7/29/99	002	Added updated boundary scan order pin list.
7/19/99	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents. This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21154 PCI-to-PCI Bridge Datasheet	278108
21154 PCI-to-PCI Bridge Configuration Application Note	278080
21154 PCI-to-PCI Bridge Hardware Implementation Application Note	278081
21154 PCI-to-PCI Bridge Evaluation Board User's Guide	278133

Nomenclature

Errata are design defects or errors. These may cause the 21154 PCI-to-PCI Bridge's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (data sheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 21154 PCI-to-PCI Bridge product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
N.A.	Not applicable.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Markings					Page	Status	ERRATA
	AB	AC	BC	AE	BE			
1	N/A	N/A	X	N/A	X	15	No Fix	Tval Timing Issues When Running at 66 MHz for All PCI Signals. Tval timing improved on the 21154BE.
2	X	X	X	X	X	16	No Fix	Hold Time Issues for All PCI Signals (Both Bused and Control) on the 21154.
3						16	Fixed	Setup Issues With PCI Control Signals When Running at 66 MHz on the 21154BC.
4		X	X			16	Fixed	Clamp Circuit May Not Function Properly Under All Conditions
5	X	X	X			17	Fixed	64-Bit Data Bus Width not Maintained when Transitioning from PCI Bus Power Management States D3 to D0
6		X	X			17	Fixed	Secondary Clocks Outputs s_clk_o<9:0> May Not Start-up Properly Under Some Conditions
7	N/A	N/A	X	N/A	X	19	No Fix	GPIO 66 MHz Timing May Cause Secondary Clocks to be Disabled
8	N/A	N/A	X			20	Fixed	Bus Conflict Occurs During Configuration on AGP Port of Some Chip Sets.
9				X	X	20	No Fix	21154AE/BE May Experience Performance Problems or Hangs when P_VIO = 3.3V
10				X	X	21	No Fix	Secondary Address pins are driven incorrectly during reset.

Specification Changes

No.	Markings					Page	Status	SPECIFICATION CHANGES
	AB	AC	BC	AE	BE			
1		X	X	X	X	22	Doc	PBGA Package Dimensions for Coplanarity Changed from Maximum Value 0.15 mm to Maximum Value of 0.2 mm
2				X	X	22	Doc	PCI Configuration Space Registers have changed.
3				X	X	22	Doc	Pin 1 Designator Change
4				X	X	22	Doc	Power Management Capability Change

Specification Clarifications

No.	Markings					Page	Status	SPECIFICATION CLARIFICATIONS
	AB	AC	BC	AE	BE			
1	X	X	X	X	X	23	Doc	Signal trst_l must be driven low to disable JTAG for normal operation

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278108	24	Doc	Section 17.2, Table 40, Absolute Maximum Ratings
2	278108	24	Doc	Section 18.0, Paragraph 1
3	278108	24	Doc	Section 18.0, Figure 25, 304-Point 2-Layer PBGA Package
4	278108	24	Doc	Section 18.0, Table 51, 304-Point 2-Layer PBGA Package Dimensions
5	278108	25	Doc	Section 16.2, Table 39, Boundary Scan Order
6	278133	28	Doc	Section 4.3, Paragraph 1
7	278108	28	Doc	Section 16.7, Initialization, Paragraph 1
8	278081	28	Doc	Section 5.1, Initialization, Description
9	278081	29	Doc	Section 6.3.1, Signal trst_l Pull-Down Resistor, New Section
10	278108	29	Doc	Section 2.10, JTAG Signals, Table 13
11	278080	30	Doc	Section 5.0, System Initialization, Last Paragraph
12	278108	30	Doc	Section 10.2, Secondary Clock Control, Figure 19
13	278108	30	Doc	Section 10.2, Secondary Clock Control, Figure 20
14	278108	31	Doc	Section 10.2, Secondary Clock Control, Table 34
15	278108	31	Doc	Section 10.2.1, Mask and Load Shift Timing Events for 66 MHz Operation
16	278080	32	Doc	Section 15.1.3, Primary Command Register, Table Description
17	278081	33	Doc	Section 4.4.1, Serial Clock Mask Shift, Table 4
18	278081	33	Doc	Section 4.4.1, Serial Clock Mask Shift, Figure 3
19	278081	34	Doc	Section 4.4.1, Serial Clock Mask Shift, Figure 4
20	278081	34	Doc	Section 4.2, 21154 Output Clocks
21	278108	35	Doc	Section 18.0, Table 51, 304-Point 2-Layer PBGA Package Dimensions
22	278108	35	Doc	Section 2.5, Secondary Bus Arbitration Signals, Table 8
23	278108	35	Doc	Section 2.9, Miscellaneous Signals, Table 12
24	278081	35	Doc	Updated Version of PCI Local Bus Specification
25	278081	35	Doc	Section 4.1, Updated s_clk and p_clk description
26	278081	35	Doc	Section 4.2, Updated Clock Outputs
27	278081	35	Doc	Section 4.4.1, Added Note at End of Section.
28	278081	36	Doc	Section 4.5, Table 5 Product Part Numbers have been updated.
29	278108 278080 278081 278133	36	Doc	Updated Version of PCI Local Bus Specification

Identification Information

Markings

The 21154 is a legacy component that was initially introduced by Digital Semiconductor, a business division of Digital Equipment Corporation. The characteristics are described in Table 1.

Table 1. 21154 Markings

Package Markings	REV_ID Register Value[a]	Package Type	Speed (MHz)	Stepping
Digital Semiconductor 21154AA DC1062B	01h	304PBGA	33	B
Digital Semiconductor 21154AB DC1062C	02h	304PBGA	33	C
Intel 21154AC DC1113A	05h	304PBGA	33	A
Intel 21154BC DC1113A	05h	304PBGA	66	A
Intel 21154AC DC1113B	05h	304PBGA	33	B
Intel 21154BC DC1113B	05h	304PBGA	66	B
Intel FW21154AE	00h	304PBGA	33	E
Intel FW21154BE	00h	304PBGA	66	E

a. Identified in a PCI system by reading the value in the REV_ID register.

Errata

1. Tval Timing Issues When Running at 66 MHz for All PCI Signals. Tval timing improved on the 21154BE.

Problem: This problem exists for parts with REV_ID 5 and REV_ID 0.

Two worst-case slow conditions exist. The 21154BC and 21154BE were tested under two different sets of worst-case slow conditions.

Table 2. Definition of Worst Case Slow Conditions

Worst-Case Slow	T_{test} [T_j] (^oC)	Process Variation (Intel Defined)	V_{dd} (V)
Condition 1	85	S - slow	3.0
Condition 2[a]	108	SS - very slow	3.0

a. The FW21154BE worst case slow condition 2 includes the very slow processing corner, 108 ^{o} C junction temperature, no airflow, 4 layer coupon, 3.0 V V_{dd}, and bus switched data (all 1s and all 0s flowing upstream from a fully loaded secondary) with no interrupts. Any improvement in the thermal factors (Θja), board design, V_{dd}, data transition density, and interrupt density and Tval will be < 6.0 ns at 85 ^{o} C junction temperature.

Table 3. Comparison of the 21154BC and the 21154BE Performance

Product	Worst-case Slow Condition	Tval V_V (ns)	Tval Z_V (ns)
21154BC	1	6.5	8.0
21154BC	2	No data	No data
21154BE	1	<6.4	<6.25
21154BE	2	7.35	7.35

Implication: This miss for Tval on PCI control signals may reduce total flight time (Tprop) when running at 66 MHz. The 21154BE meets or exceeds the 21154BC performance under the worst-case slow conditions.

Note: The FW21154BE worst case slow condition 2 includes the very slow processing corner, 108 ^{o} C junction temperature, no airflow, 4 layer coupon, 3.0 V Vdd, and bus switched data (all 1s and all 0s flowing upstream from a fully loaded secondary) with no interrupts. Any improvement in the thermal factors (Θja), board design, Vdd, data transition density, and interrupt density and Tval will be < 6.0 ns at 85 ^{o} C junction temperature.

Workaround: There are no workarounds for this erratum.

Note: Refer to the *21154 PCI-to-PCI Bridge Specification Update* Errata table for current errata. All errata listed are fixed in the 21154AE/BE version except for Errata #1, #2, and #7.

Status: No Fix: See "Summary Table of Changes" on page 10.

2. Hold Time Issues for All PCI Signals (Both Bused and Control) on the 21154.

Problem: This problem exists for parts with REV_ID 2, REV_ID 5 and REV_ID 0.

The *PCI Local Bus Specification, Revision 2.2*, specifies a Hold time of 0 ns in Section 7.6.4.2. The 21154AB requires a minimum hold time of 1.4 ns. Both the 21154AC/BC and 21154AE/BE require a minimum hold time of 1.375 ns.

Implication: Most PCI devices will function properly with this difference to the Hold time specification.

Workaround: There are no workarounds for this erratum.

Status: No Fix: See "Summary Table of Changes" on page 10.

3. Setup Issues With PCI Control Signals When Running at 66 MHz on the 21154BC.

Problem: This problem was originally believed to exist for parts with REV_ID 5.

Setup time issues on the following 66 MHz PCI control signals: p_frame_l, p_irdy_l, p_trdy_l, s_frame_l, s_irdy_l, s_trdy_l. The *PCI Local Bus Specification, Revision 2.2*, specifies a Setup time of 3 ns for all devices when running at 66 MHz in Section 7.6.4.2. The 21154BC requires a minimum worst-case setup time of 4.5 ns.

Implication: The Tsetup specification miss on PCI control signals must be considered in the overall timing budget for designs that use this product, and may reduce total flight time (Tprop) when running at 66 MHz.

Workaround: This errata was caused by a test-fixture problem and is invalid.

Status: Fixed

4. Clamp Circuit May Not Function Properly Under All Conditions

Problem: This problem has been found on parts with REV_ID 5. When either the primary or secondary vio pins are connected to 3.3 volts, the 21154's clamping circuit may not function properly.

Implication: Dependent on the application environment, oscillations or "ringing" have been observed on some PCI control signals (for example, STOP#). The circuitry to generate the input clamp voltages of both the 21154AC and 21154 BC is different than that of the 21154AB.

Workaround: When the application topology allows it (short bus lengths, direct etch runs), connecting 3.3 volts to these pins should produce desired results. The use of p_vio and s_vio for both the 21154AC and 21154BC will be determined by the customer application. Designs that adhere to the "Expansion Board Specification" of the *PCI Local Bus Specification, Revision 2.2* are not affected. Designs whose topology might include long bus lengths might find that connecting s_vio or p_vio to 5 volts leads to improved signal integrity for the corresponding bus. As such, Intel recommends thorough signal integrity analyses prior to a decision on which voltage to connect to these pins.

If there is any 5-volt PCI device on a bus segment, the vio pin for that segment should be tied to the 5 volt supply.

Status: Fixed

5. 64-Bit Data Bus Width not Maintained when Transitioning from PCI Bus Power Management States D3 to D0

Problem: When transitioning from PCI Bus Power Management states D3 hot to D0 hot, the 21154 performs an internal reset of the primary bus circuits and clears the REQ64 status of the primary bus. The secondary bus continues to operate at 64-bit data bus width but the primary bus width reverts back to a 32-bit data bus width. The 21154 drives the AD<63:32> with whatever data is next in its queue and may drive incorrect parity for AD<63:32> as well.

Implication: The 21154 can cause bus contention on AD<63:32> resulting in data corruption and device damage. This erratum may also cause some systems to hang or report parity errors.

Workaround: This problem can be avoided by treating the 21154 as a PCI Bus Power Management legacy device by not using the PCI Bus Power Management capabilities.

Status: Fixed

6. Secondary Clocks Outputs s_clk_o<9:0> May Not Start-up Properly Under Some Conditions

Note: This errata only applies to applications that use the 21154 for secondary clocks.

Problem: This problem has been found on the 21154AC and 21154BC. Under repeated and frequent power cycling, the secondary clock circuits may not power up in the proper state, resulting in the device not coming out of reset after power up.

Implication: In a system with a 21154AC or 21154BC that has one of its **s_clk_o<9:0>** outputs fed back to provide the **s_cl**k, it is possible that the **s_clk_o<9:0>** output clocks will be driven and remain low, keeping **s_rst_l** asserted, during system power up.

This happens occasionally when a latch whose output disables the serial shift registers on the Secondary clock control powers up in a high state and the shift register bit corresponding to the **s_clk_o<9:0>** output that is fed back also powers up in the high state.

Workaround: Two workarounds are provided for this errata:

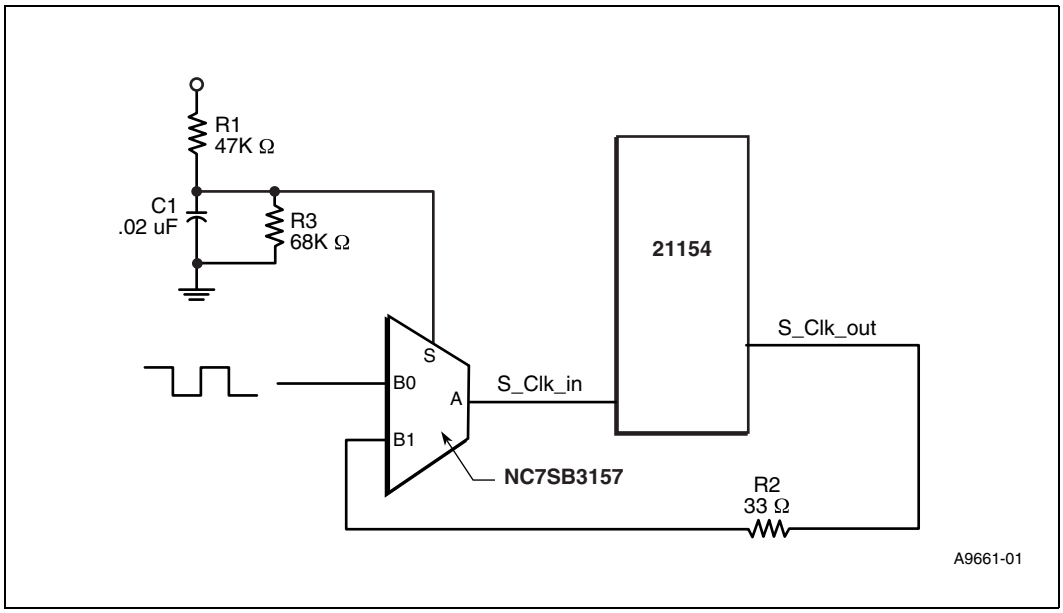
- The first is the recommended workaround which ensure proper operation of the secondary clock outputs s_clk_0<0:9>.
- The second workaround ensures the secondary clock outputs operate properly but could result in contention between the s_ckl_0 output and the buffer.

1. Figure 1 illustrates the first recommendation - a circuit where an on-board pulse source is gated via the B0 input of the multiplexer to the S_Clock_in pin of the 21150.

   At time 0, the S input of the multiplexer is low, allowing pulses from the on-board pulse source, connected to the B0 input, to be provided to the 21150 S_Clk input pin. When the time determined by the R/C network is satisfied, the S input pin will be in a logic High state. The multiplexer will then shut off the input pulse from S0 and will direct the S_Clock_out pulses via the B1 multiplexer input, into S_Clock_in

   The values used for the R/C network should be selected to allow a minimum of 2 pulses to be delivered to the 21150 after Vdd has reached 3.0V at a frequency not to exceed the appropriate PCI component. i.e. 30 ns for a 33Mhz bridge. These values should be chosen based on the rise time of the power supply and the frequency of the on board pulse source. The values given for R1, R3, and C1 are for example purposes only.

Figure 1. S_Clock Multiplexer Workaround Circuit for Errata 6.

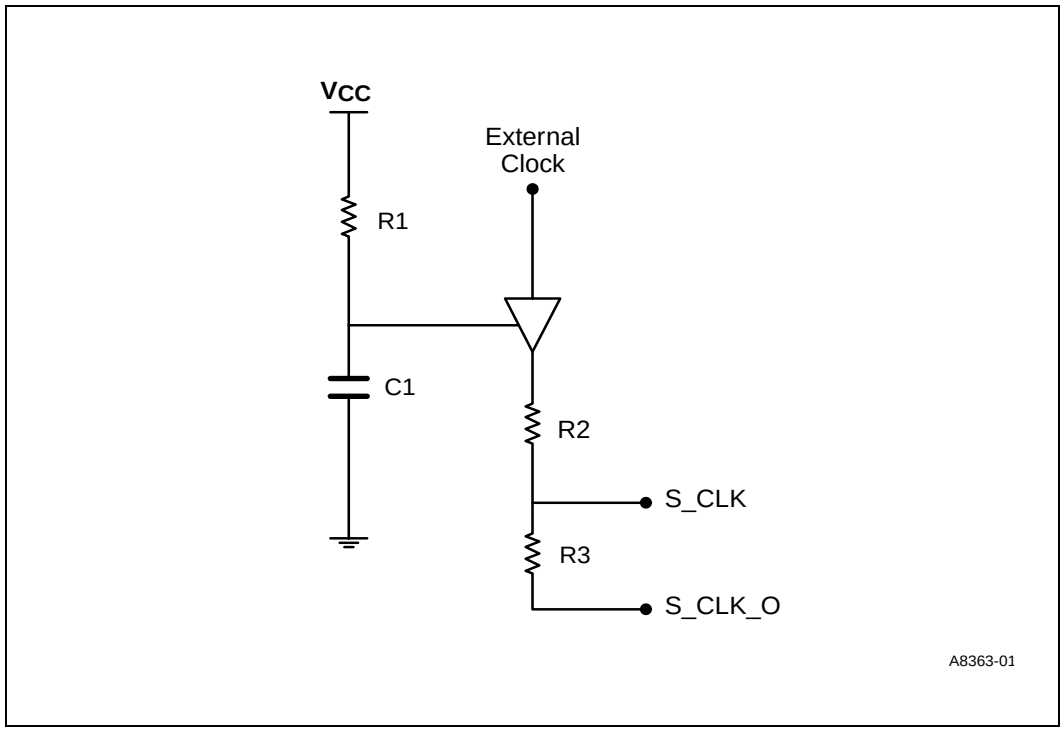


Note: The NC7SB3157 2:1 Multiplexer / Demultiplexer Bus Switch used in this example has a maximum propagation delay of 800ps that should be taken into consideration when matching trace lengths of the clock lines to avoid introducing excessive skew in the clocks. All S_Clock etch lengths must be matched to within 2ns @ 33Mhx or 1ns @66Mhz. The addition of this circuit requires that the etch length for the S_clock_in signal be reduced to compensate for the 800ps delay.

2. In the second recommendation, to guarantee the proper initialization of the **s_clk** circuits, the addition of an external circuit that provides a minimum of two transitions on the **s_clk** input during the power-up ramp is necessary. This can be done using a solution that drives an external clock onto the **s_clk** input while 3.3V Vcc is ramping during power up.

   Figure 2 illustrates the use of a tristable buffer to provide multiple pulses to the **s_clk** input. The Vcc ramp rate and R1,C1 time constant determine the duration and amplitude of the pulses generated during power up. The R2-R3 values are chosen based on applicable board etch impedance-matching requirements.

Figure 2. Recommended Circuit for a Tristable Buffer



The following should be considered in calculating the R1,C1 time constant:

— Make the time constant of the circuit as short as possible, while still ensuring that a minimum of two pulses are generated during the Vcc ramp.

— Phase delay between **s_clk_o** and the external clock should be minimized.

— Matching the external clock and **s_clk_o** frequencies to reduce contention**.**

— Laboratory experiments using **p_clk** as the external clock and a R1C1 time constant between 40 and 60 percent of the Vcc ramp have been successful using this configuration. However the use of **p_clk** as the external clock violates the PCI bus specification for loading of the primary clock.

Status: Fixed

7. GPIO 66 MHz Timing May Cause Secondary Clocks to be Disabled

Problem: In the Secondary Clock Control function, the msk_in pin may be used with an external shift register to selectively disable secondary clock output pins. At 66 MHz the timing of the interface between the gpio pins and the external shift register may cause some secondary clock outputs to be incorrectly disabled.
The setup time of the recommended 74F166 shift register is not compatible with the timing of the **gpio<2>**, and **gpio<0>** outputs of the 21154 PCI-to-PCI bridge. Pin **gpio<2>** driving the shift register load/shift enable (**PE#**), does not provide the necessary setup time for the **gpio<0>**. Signal **gpio<0>** is used as a clock to initiate the parallel load of the 74F166 shift register data inputs. The timing is referred to as Tgsval.

Note: This errata does not apply when operating at 33 MHz or if the external shift register is not used and **msk_in** is grounded enabling all secondary clocks.

Implication: At 66 MHz the setup time mismatch between the shift register parallel inputs and **PE#** pin and gpio pins may cause the shift register to be incorrectly loaded. This could result in the secondary clocks to be incorrectly disabled.

Workaround: In order to provide an appropriate setup time, a buffer must be added to delay **gpio<2>** with respect to **gpio<0>**. This buffer (or buffers) provides the delay for **gpio<2>** to correctly load the parallel data inputs of 74F166 registers. A setup time of at least 3ns is required at the shift register for **PE#** to load.

Note: For more information, see Section 10.2.1, Mask and Load Shift Timing Events for 66 MHz Operation in this specification update.

Status: No Fix

8. Bus Conflict Occurs During Configuration on AGP Port of Some Chip Sets.

Problem: The 21154 Bridge accepts type zero configuration cycles on its primary bus. It also accepts Type 1 configuration cycles on its primary bus and forwards them, if they are addressed to a bus number between its secondary and subsequent bus numbers, which are assigned to the bridge by system software. The secondary and subsequent bus number registers are set to zero by reset. Some chipsets supporting AGP use Type 1 configuration cycles to program themselves. The chipset has set its own address to be bus 0, device 0. Unfortunately, this creates a conflict if the bridge's downstream bus number registers have not yet been programmed to a non-zero value. This conflict occurs when both the chipset and bridge respond to Type One Configuration cycles to bus 0 resulting in bus contention.

Implication: Both the AGP interface and the 21154 Bridge will respond to the same Type 1 bus transaction causing bus signal contention.

Workaround: None

Status: Fixed

9. 21154AE/BE May Experience Performance Problems or Hangs when P_VIO = 3.3V

Problem: Intel has received reports of performance problems due to excessive retries and hangs in a few applications when P_VIO and/or S_VIO =3.3V. The retry issue has been observed in several types Video, Fibre Channel and Gigabit Ethernet modules with the time to failure ranging from 7 minutes to 39 hours.

The symptom of this issue is that a delayed read is initiated on the primary bus. It is immediately responded to with retry and stored as a CAM entry. The request is played out on the secondary bus and the device receives the data. The CAM entry becomes corrupt due to noise on the core ground. This causes the read request on the primary bus to match the CAM entry, but the bridge does not respond with the data. As the CAM entry is matched, no additional read request is made on the secondary bus, but the primary bus never receives the data, only retries. This causes the initiating master to continue to retry the read, making no progress. The 21154 will eventually discard that read data when the primary master timeout timer expires (2^{10} or 2^{15} clock cycles). The delayed read transaction is then reinitiated on the primary bus and usually completes normally. This causes a 30.7 µs or 983 µs delay (at 33MHz) depending on the setting of the primary master timeout bit.

The same issue and scenario has also been reported on delayed reads from the secondary bus to the primary bus.

The root cause is due to changes in the internal grounding scheme implemented in the 21154AE/BE - an approximate 400mV reduction in the noise immunity occurred in the CAM circuitry. The data stored within the CAM (Content Addressable Memory) circuitry becomes

corrupted resulting in a mismatch when the transaction is retried causing the transaction to be retried continuously. The primary master timeout timer times out (2^{10} or 2^{15} clock cycles), discards the data, and reinitiates the transaction on the next cycle. This transaction usually completes as a normal delayed read transaction.

Since the 21154 is a highly symmetrical device and the CAM circuitry is duplicated on both the primary and secondary interfaces the issue may occur on either an upstream or downstream delayed read transactions.

Implication: Applications using P_VIO and/or S_VIO=3.3V may experience excessive retries due to a reduction in noise immunity in the CAM section of the chip. When P_VIO and/or S_VIO is set above ~3.8V the biasing of the input transistor effectively reduces the resulting core ground undershoot that is coupled through the ESD protection clamp.

This issue has only been reported in a very small number of high performance applications such as Video cards, Gigabit Ethernet and 100MByte/s Fibre Channel with P_VIO and/or S_VIO set to 3.3V. Other lower performance applications and implementations with P_VIO and S_VIO set to 5V have not reported the issue. This may also manifest as a layout sensitivity issue.

Workaround: Setting P_VIO and S_VIO to 5V has proven to eliminate these issues on current designs. Many 21154 designs that implemented the errata 4 work around are already biasing the P_VIO and S_VIO pins to 5V and should not experience the issues.

Note: P_VIO and S_VIO pins set the value of the voltage clamp only and has no affect on the signaling levels of the bus.

Status: No Fix

10. Secondary Address pins are driven incorrectly during reset.

Problem: During reset S_AD <63:0>, C/BE# and PAR are driven high. The *PCI Local Bus Specification* requires that these pins be driven low during reset.

Implication: In applications where multiple PCI components implemented on the secondary bus may drive the bus during reset, there is a potential for device contention if the 21154AE/BE is driving high and the other device/devices are driving low. This contention may cause excessive power dissipation in the 21154 and could potentially damage the device.

Workaround: There is no known work around.

Status: No Fix

Specification Changes

1. PBGA Package Dimensions for Coplanarity Changed from Maximum Value 0.15 mm to Maximum Value of 0.2 mm

Per PCN notification 961, the 304-point 2-layer PBGA package dimensions for symbol aaa, coplanarity, are changed from maximum value 0.15 mm to maximum value 0.2 mm.

Note: **The following changes (2-4) are specific to the 21154AE/BE version of the product only.**

2. PCI Configuration Space Registers have changed.

Table 1. Register Changes

Register	Offset	Old Value	New Value
Vendor ID	00:01	1011h	8086h
Device ID	02:03	0026h	B154h
Revision ID	08	05h	00h

3. Pin 1 Designator Change

Viewing the text label printed on top of the 21154AE/BE package (marking side), the Pin 1 designator appears in the lower left hand corner of the package. The Pin 1 designator for previous steppings was located in the upper left hand corner of the package.

Note: The pin designations have not changed. The only change was that the printed label was rotated 90^{o}.

4. Power Management Capability Change

The pmeena_l pin was changed on the 21154AE/BE to indicate that devices on the secondary side of the bridge do not support the PME# pin. It is up to the software then to scan the device to actually determine PME# pin support. This is described in Table 2 that follows:

Table 2. Power Management Capability Changes

Description	Value
Pin Number	D11
Previous Name	Vdd
Previous Function	Power Input
New Name	pmeena_l
Function	Input
Operation	This can be tied to either Vdd or Vss (ground). This effects the value of bits [31:27], PME_SUP, of the Power Management Register (dword address DCh, offset DEh).
Vdd	These 5 bits should read a 00000[a], as in previous steppings.
Vss	These 5 bits should read as 11111.

a. 00000 indicates that the device behind the bridge does not support PME#.

Specification Clarifications

1. Signal trst_l must be driven low to disable JTAG for normal operation

The signal trst_l resets the JTAG circuitry while asserted low. This signal also enables normal JTAG TAP controller operation when high. For normal PCI-to-PCI bridge operation, disable JTAG by pulling trst_l low using a 5K resistor.

Documentation Changes

1. Section 17.2, Table 40, Absolute Maximum Ratings

Maximum power P_{wc} is changed from 2.2W to 2.9W.

Table 40. Absolute Maximum Ratings

Parameter	Minimum	Maximum
Junction temperature, T_j	—	125°C
Maximum voltage applied to signal pins	—	5.5 V
Supply voltage, V_{cc}	—	3.9 V
Maximum Power, P_{wc}	—	2.9 W
Storage temperature range, T_{sg}	-55°C	125°C

2. Section 18.0, Paragraph 1

Section 18.0. Paragraph 1 is changed to read as follows:

The 21154 variants are contained in the 304-point plastic ball grid array (PBGA) packages shown in Figure 25. The 21154AC/BC and 21154AE/BE variants utilize a 4-layer 304-point PBGA. All other variants utilize a 2-layer 304-point PBGA.

3. Section 18.0, Figure 25, 304-Point 2-Layer PBGA Package

Section 18.0, Figure 25 title is changed to read as follows:

304-Point PBGA Package (2-Layer and 4-Layer)

4. Section 18.0, Table 51, 304-Point 2-Layer PBGA Package Dimensions

Section 18.0, Table 51 title is changed to read as follows:

304-Point PBGA Package Dimensions (2-Layer and 4-Layer)

5. Section 16.2, Table 39, Boundary Scan Order

The boundary-scan order pin call outs change from pin R4 through pin R21. The correct pin call out is:

Table 39. Boundary Scan Order (Sheet 1 of 3)

Pin Number	Signal Name	Boundary Scan Order	By Group Disable	Group Disable Cell
R4	bpcce	NA/127	—	
NOTE: A new signal, bpcce, was added on pin R4 for the 21154AB and later revisions. From pin R4 through pin R21, two values are provided in the xxx/yyy format: the boundary-scan register number in the xxx field is for the 21154AA version only, and the boundary-scan register number in the yyy field is for the 21154AB and later revisions.				
T3	p_clk	127/128	—	
T2	V_{ss}	128/129	—	Group Disable 3
U3	p_req_l	129/130	3	
U2	p_ad<31>	130/131	2	
U4	p_ad<30>	131/132	2	
U1	p_ad<29>	132/133	2	
V2	p_ad<28>	133/134	2	
V1	p_ad<27>	134/135	2	
V3	p_ad<26>	135/136	2	
W2	p_ad<25>	136/137	2	
W1	p_ad<24>	137/138	2	
Y2	p_cbe_l<3>	138/139	2	
Y1	p_idsel	139/140	—	
W4	p_ad<23>	140/141	2	
Y3	p_ad<22>	141/142	2	
AA1	p_ad<21>	142/143	2	
AA3	p_ad<20>	143/144	2	
Y4	p_ad<19>	144/145	2	
AB3	p_ad<18>	145/146	2	
AA4	p_ad<17>	146/147	2	
Y5	p_ad<16>	147/148	2	
AC4	V_{ss}	148/149	—	Group Disable 2
AB4	p_cbe_l<2>	149/150	2	
AA5	p_frame_l	150/151	1	
AC5	p_irdy_l	151/152	1	
AB5	p_trdy_l	152/153	1	
AA6	p_devsel_l	153/154	1	
AC6	p_stop_l	154/155	1	
AB6	p_lock_l	155/156	1	
—	V_{ss}	156/157	—	Group Disable 1

Table 39. Boundary Scan Order (Sheet 2 of 3)

Pin Number	Signal Name	Boundary Scan Order	By Group Disable	Group Disable Cell
AC7	p_perr_l	157/158	1	
Y7	p_serr_l	158/159	1	
AB7	p_par	159/160	0	
AA7	p_cbe_l<1>	160/161	0	
AB8	p_ad<15>	161/162	0	
AA8	p_ad<14>	162/163	0	
AC9	p_ad<13>	163/164	0	
AB9	p_ad<12>	164/165	0	
AA9	p_ad<11>	165/166	0	
AC10	p_ad<10>	166/167	0	
AB10	p_m66ena	167/168	0	
AA10	p_ad<9>	168/169	0	
Y11	p_ad<8>	169/170	0	
AC11	p_cbe_l<0>	170/171	0	
AB11	p_ad<7>	171/172	0	
AA11	p_ad<6>	172/173	0	
AA12	p_ad<5>	173/174	0	
AB12	p_ad<4>	174/175	0	
AB13	p_ad<3>	175/176	0	
AA13	p_ad<2>	176/177	0	
Y13	p_ad<1>	177/178	0	
AA14	p_ad<0>	178/179	0	
AB14	p_ack64_l	179/180	0	
AC14	p_req64_l	180/181	0	
AA15	p_cbe_l<7>	181/182	0	
AB15	p_cbe_l<6>	182/183	0	
Y15	p_cbe_l<5>	183/184	0	
AC15	p_cbe_l<4>	184/185	0	
AA16	p_ad<63>	185/186	0	
AB16	p_ad<62>	186/187	0	
AA17	p_ad<61>	187/188	0	
AB17	p_ad<60>	188/189	0	
Y17	p_ad<59>	189/190	0	
AB18	p_ad<58>	190/191	0	
AC18	p_ad<57>	191/192	0	
AA18	p_ad<56>	192/193	0	
AC19	p_ad<55>	193/194	0	
AA19	p_ad<54>	194/195	0	

Table 39. Boundary Scan Order (Sheet 3 of 3)

Pin Number	Signal Name	Boundary Scan Order	By Group Disable	Group Disable Cell
AB20	p_ad<53>	195/196	0	
Y19	p_ad<52>	196/197	0	
AA20	p_ad<51>	197/198	0	
AB21	p_ad<50>	198/199	0	
AC21	p_ad<49>	199/200	0	
AA21	p_ad<48>	200/201	0	
Y20	p_ad<47>	201/202	0	
AA23	p_ad<46>	202/203	0	
Y21	p_ad<45>	203/204	0	
W20	p_ad<44>	204/205	0	
Y23	p_ad<43>	205/206	0	
W21	p_ad<42>	206/207	0	
W23	p_ad<41>	207/208	0	
W22	p_ad<40>	208/209	0	
V21	p_ad<39>	209/210	0	
V23	p_ad<38>	210/211	0	
V22	p_ad<37>	211/212	0	
U23	p_ad<36>	212/213	0	
U20	p_ad<35>	213/214	0	
U22	p_ad<34>	214/215	0	
U21	V_{ss}	215/216	—	Group Disable 0
T23	p_ad<33>	216/217	0	
T22	p_ad<32>	217/218	0	
T21	p_par64	218/219	0	
R22	config66	219/220	—	
R21	msk_in	220/221	—	

6. Section 4.3, Paragraph 1

Section 4.3, Paragraph 1 is changed to read as follows:

Some versions of the 21154 support 66 MHz operation. Versions marked 21154Ax are not tested to be 66 MHz capable. Versions of the 21154 marked 21154Bx are capable of 66 MHz operation.

7. Section 16.7, Initialization, Paragraph 1

This section has been changed to:

The test access port controller and the instruction register output latches are initialized and JTAG is disabled while the trst_l input is asserted low. While signal trst_l is low, the test access port controller enters the test-logic reset state. This results in the instruction register being reset which holds the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled and the device performs normal functions. The test access port controller leaves this state only after trst_l (low) goes high and an appropriate JTAG test operation sequence is sent on the tms and tck pins.

For the 21154 to operate properly, the JTAG logic must be reset. There are two ways to reset this logic:

- The controller will reset asynchronously with the assertion of TRST_L.
- The controller will reset synchronously after five TCK clock cycles, with TMS held high.

Note: During normal 21154 operation the JTAG logic must be disabled by pulling trst_l low using a 5K resistor.

8. Section 5.1, Initialization, Description

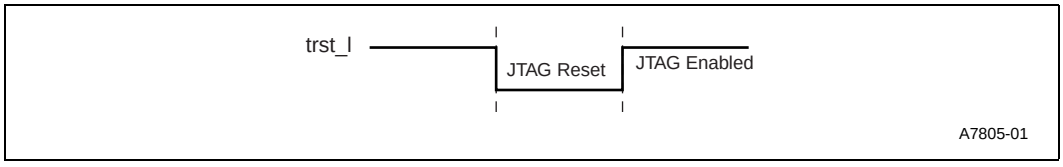
This section has been changed to:

The test access port controller and the instruction register output latches are initialized and JTAG is disabled while the trst_l input is asserted low (see Figure 5). While signal trst_l is low, the test access port controller enters the test-logic reset state. This results in the instruction register being reset which holds the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled, and the device performs normal functions. The test access port controller leaves this state only after trst_l (low) goes high and an appropriate JTAG test operation sequence is sent on the tms and tck pins.

For the 21154 to operate properly, the JTAG logic must be reset. There are two ways to reset this logic:

- The controller will reset asynchronously with the assertion of trst_l.
- The controller will reset synchronously after five TCK clock cycles, with TMS held high..

Figure 5. Signal trst_l States



Note: During normal 21154 operation the JTAG logic must be disabled by pulling trst_l low using a 5K ohm resistor.

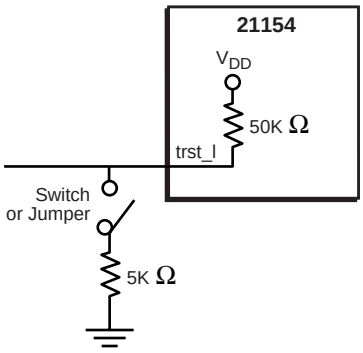
9. Section 6.3.1, Signal trst_l Pull-Down Resistor, New Section

The following new section has been added:

A 5 K Ω pull-down resistor is required on trst_l for normal PCI-to-PCI bridge operation. However, some JTAG test results may be inconclusive if the 5 K Ω resistor remains in the circuit. To obtain accurate JTAG results, Intel recommends one of the following solutions:

- Verify that the JTAG test equipment, after driving trst_l low to reset the TAP controller, constantly drives trst_l high during JTAG tests. If this signal is not constantly driven high, the 5 K Ω resistor will pull the signal to a low state.
- Remove the 5 K Ω resistor during JTAG tests. This resistor must be installed during normal PCI-to-PCI bridge operation.
- Design external circuits with a switch or jumper to isolate the 5 K Ω resistor during JTAG tests (see Figure 6). This switch must enable the resistor during normal PCI-to-PCI bridge operation.

Figure 6. Removal of Pull-Down Resistor for JTAG Testing



10. Section 2.10, JTAG Signals, Table 13

The description for trst_l has been changed as follows:

Table 13. JTAG Signals

Signal Name	Type	Description
tdi	I	JTAG serial data in. Signal tdi is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on tdi is sampled on the rising edge of tck. An unterminated tdi is pulled high by a weak pull-up resistor internal to the device.
tms	I	JTAG test mode select. Signal tms causes state transitions in the test access port (TAP) controller. An unterminated tms is pulled high by a weak pull-up resistor internal to the device.
trst_l	I	JTAG TAP reset and disable. When asserted low, JTAG is disabled and the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. An unterminated trst_l is pulled high by a weak pull-up resistor internal to the device. The TAP controller must be reset before the JTAG circuits can function. For normal JTAG TAP port operation, this signal must be high. For normal PCI-to-PCI bridge operation of the device, this signal must be pulled low using a 5K resistor.

11. Section 5.0, System Initialization, Last Paragraph

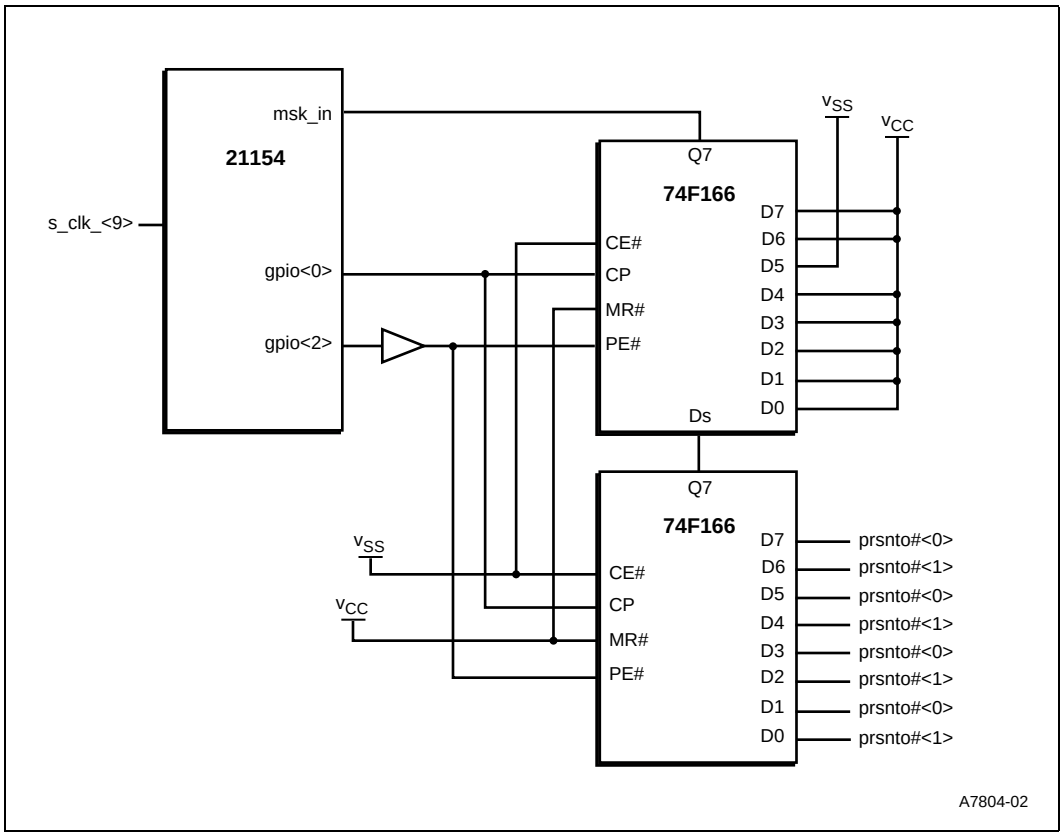
The last paragraph in this section has been changed to:

For information on initializing JTAG, see the *21154 PCI-to-PCI Bridge Hardware Implementation Application Note*.

12. Section 10.2, Secondary Clock Control, Figure 19

This figure now appears as follows:

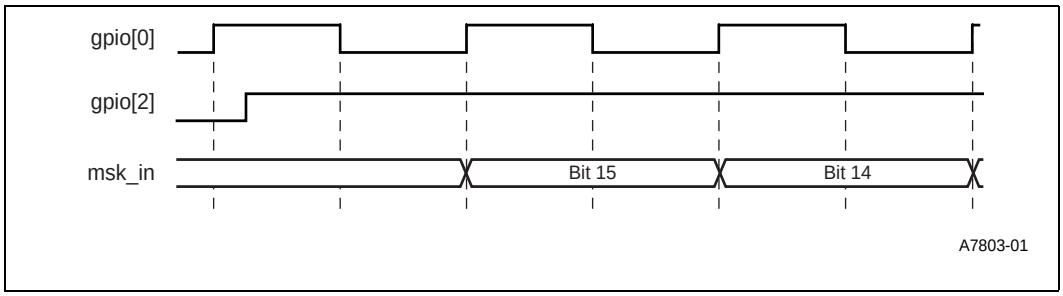
Figure 19 Example of GPIO Clock Mask Implementation on the System Board



13. Section 10.2, Secondary Clock Control, Figure 20

This figure now appears as follows:

Figure 20. Clock Mask and Load Shift Timing



14. Section 10.2, Secondary Clock Control, Table 34

This table has been re-arranged to indicate the gpio serial data format. It now appears as follows:

Table 34. GPIO Serial Data Format

Bit	Description	s_clk_o Output
<15:14>	Reserved	Not applicable
<13>	21154 s_clk input	9
<12>	Device 8	8
<11>	Device 7	7
<10>	Device 6	6
<9>	Device 5	5
<8>	Device 4	4
<7:6>	Slot 3 PRSNT#<1:0> or device 3	3
<5:4>	Slot 2 PRSNT#<1:0> or device 2	2
<3:2>	Slot 1 PRSNT#<1:0> or device 1	1
<1:0>	Slot 0 PRSNT#<1:0> or device 0	0

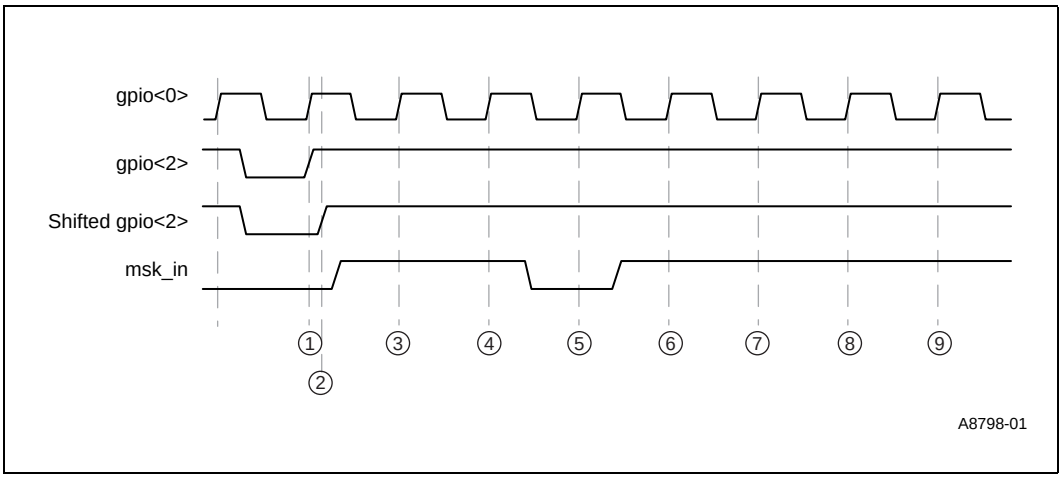
15. Section 10.2.1, Mask and Load Shift Timing Events for 66 MHz Operation

The following new section has been added:

The following list provides the timing sequence for 66 MHz operation for an example circuit as shown in Figure 19 and the timing diagram in Figure 21.

1. The **gpio<2>** original coming from the 21154 does not provide 3ns setup time needed to provide the parallel load enable **PE#** of the 74F166.
2. The shifted **gpio<2>** is delayed by ~9ns to provide ample setup time to enable the parallel of the shift register connected to pin 15 of the 74F166.
3. Bit 15 input **D6** of the shift register is pulled high, to Vcc.
4. Bit 14 input **D7** is pulled high, to Vcc. These signals are not used internally in the 21154.
5. Bit **13 s_clk_o<9>** is a feedback to the 21154 **s_clk_o** input. To enable **s_clk_o<9>** in all cases the **D5** input of the shift register is grounded, to Vss.
6. Bit 12 **s_clk_o<8>** is disabled.
7. Bit 11 **s_clk_o<7>** is disabled.
8. Bit 10 **s_clk_o<6>** is disabled.
9. Bit 9 **s_clk_o<5>** is disabled.

Figure 21. Clock Mask and Load Shift Timing



16. Section 15.1.3, Primary Command Register, Table Description

Changed the description in Dword 0 for when it is a one. It now appears as follows:

Primary Command Register

Dword Bit	Name	R/W	Description
0	I/O space enable	R/W	Controls the 21154's response to I/O transactions on the primary interface. 0 = The 21154 does not respond to I/O transactions initiated on the primary bus. 1 = The 21154 response to I/O transactions initiated on the primary bus is in the enabled state. Reset value: 0.

17. Section 4.4.1, Serial Clock Mask Shift, Table 4

Table 4 has been changed as follows:

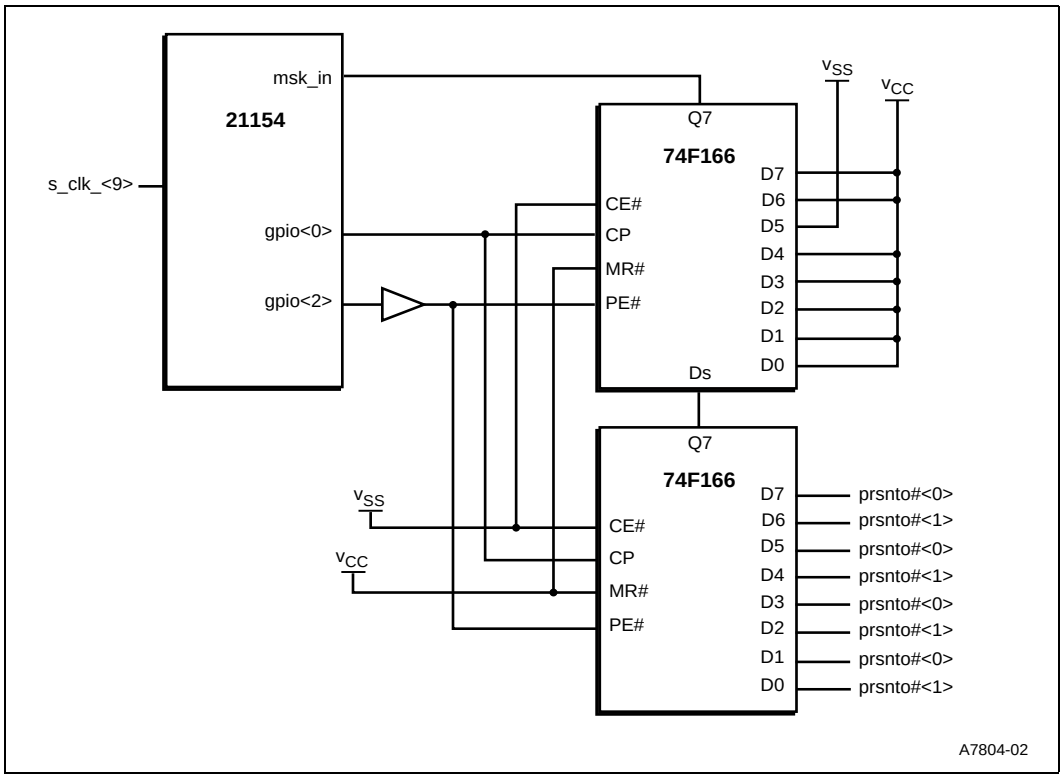
Table 4. GPIO Serial Data Format

Bit	Description	s_clk_o Output
<15>	Reserved	Not applicable
<14>	Reserved	Not applicable
<13>	21154 s_clk input	9
<12>	Device 8	8
<11>	Device 7	7
<10>	Device 6	6
<9>	Device 5	5
<8>	Device 4	4
<7:6>	Slot 3 PRSNT#<1:0> or device 3	3
<5:4>	Slot 2 PRSNT#<1:0> or device 2	2
<3:2>	Slot 1 PRSNT#<1:0> or device 1	1
<1:0>	Slot 0PRSNT#<1:0> or device 0	0

18. Section 4.4.1, Serial Clock Mask Shift, Figure 3

Figure 3 has been updated as follows:

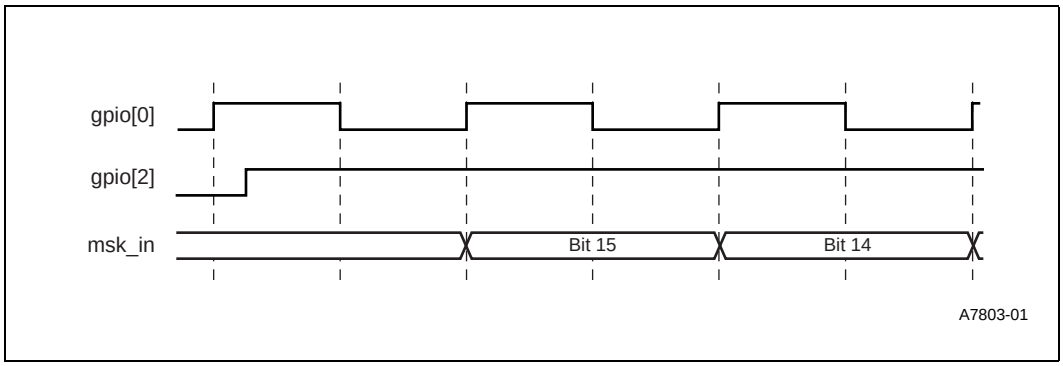
Figure 3 Example of GPIO Clock Mask Implementation on the System Board



19. Section 4.4.1, Serial Clock Mask Shift, Figure 4

Figure 4 now appears as follows:

Figure 4. Clock Mask Load and Shift Timing



20. Section 4.2, 21154 Output Clocks

This note has been added to the end of the section:

Note: Intel recommends that a 22K pull-up resistor be placed on s_clk to better insure proper initialization on power-up.

21. Section 18.0, Table 51, 304-Point 2-Layer PBGA Package Dimensions

The maximum value for symbol aaa, dimension coplanarity has been changed from 0.15 mm to a value of 0.2 mm.

22. Section 2.5, Secondary Bus Arbitration Signals, Table 8

This sentence is added to the end of the description for s_req_l <8:0>:

"When the secondary bus is set to operate at 66 MHz, s_req_l <8:4> is disabled."

This sentence is added to the end of the description for s_gnt_l<8:0>:

"When the secondary bus is set to operate at 66 MHz, s_gnt_1 <8:4> is disabled."

23. Section 2.9, Miscellaneous Signals, Table 12

This sentence is added at the end of the description for S_m66ena:

"When the secondary bus is set to operate at 66 MHz, s_req_l <8:4> and s_gnt_1<8:4> are disabled."

24. Updated Version of PCI Local Bus Specification

All places in the *21154 Hardware Bridge Hardware Implementation Application Note* where the *PCI Local Bus Specification* is mentioned was updated from version 2.1 to version 2.2.

25. Section 4.1, Updated s_clk and p_clk description

The first two paragraphs and the first bullet in Section 4.1 now appear as follows:

4.1 21154 Clocking Domains

The 21154 has two clocking domains: one for the primary PCI interface and one for the secondary PCI interface. Each PCI interface has a separate clock input. The primary interface is controlled by the primary clock input, p_clk, and the secondary interface and arbiter is controlled by the secondary clock input, s_clk.

The edge relationship between s_clk and p_clk is well defined. The relationship between the p_clk and s_clk inputs has the following restrictions:

- The 21154 operates at a maximum frequency of 66 MHz, and s_clk always operates at the same frequency or half the frequency of p_clk.

26. Section 4.2, Updated Clock Outputs

The first bulleted item in Section 4.2 now appears as follows:

- All clock outputs operate at the same or half the frequency as p_clk.

27. Section 4.4.1, Added Note at End of Section.

The note added to the end of Section 4.4.1 appears as follows:

Note: Refer to Errata #7 previously in this document for an explanation of an added external buffer on the output of gpio <2> to use this feature at 66 MHz.

28. Section 4.5, Table 5 Product Part Numbers have been updated.

Table 5 now appears as follows:

Table 5. Low-Skew Clock Buffers

Vendor	Part Number (5V)	Part Number (3.3V)
Texas Instruments	CDC328A	CDCV304
National Semiconductor	CGS74B2525	CGS574CT2524
IDC	1DT74FCT805CT	QS53805

29. Updated Version of PCI Local Bus Specification

All references in the *21154 PCI-to-PCI Bridge* documentation where the *PCI Local Bus Specification* is mentioned were updated from version 2.2 to version 2.3.