82346
SYSTEM CONTROLLER

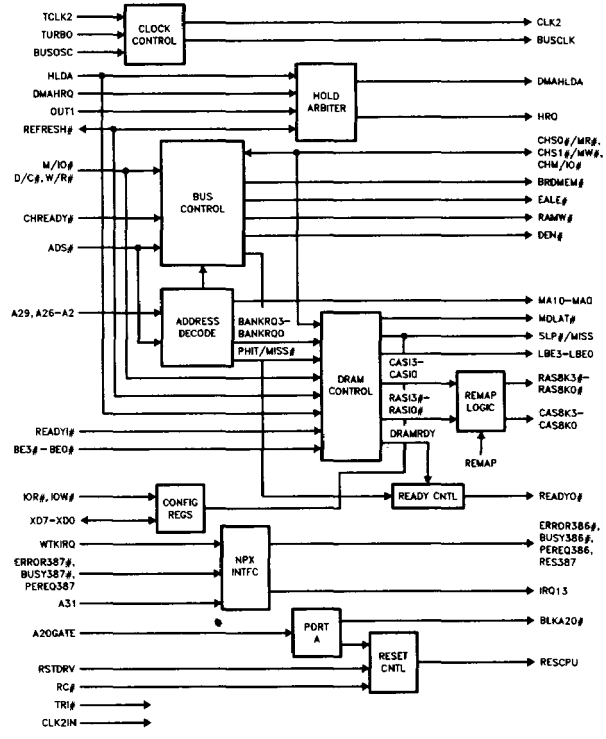
The 82346 System Controller is highly configurable via software. No hardware jumpers are required. Defaults on reset for the configuration registers mimic the compatibility requirements of the original IBM PC/AT® as closely as possible. These power-up defaults allow any possible configuration of the system to boot at the CPU's rated speed. However, operational capabilities are reduced until the configuration registers are set to mirror the true system configuration. This normally occurs during BIOS power-on self-test in a manner completely transparent to the user.

The System Controller is designed to perform in systems running up to 33 MHz. Built-in page mode operation, two- or four-way interleaving and fully programmable memory timing allow the PC designer to maximize system performance using low cost DRAMs. Programmable memory timing allows the system to be setup to perfectly match the requirements of the chosen DRAMs; standard or custom. These adjustments can often be made without incurring the penalty of additional wait states.

1

The System Controller handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the 82344 ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. The former method is the standard PC/AT-compatible mode where on- and off-board refreshes are performed synchronously. In decoupled mode, the timing of on- and off-board refreshes are independent. Both may be programmed for independent, slower than normal rates. This allows use of low power, slow refresh DRAMs. The 82346 controls all timing in both modes. In all cases, refreshes are staggered to minmize power supply loading and attendant noise on the VDD and ground pins.

IBM PC/AT® is a registered trademark of IBM Corporation.



240842-1

Block Diagram

October 1990
Order Number: 240842-001

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are possible. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function performs this task by switching the internal RASI# and CASI# signals between the external RAS# and CAS pins. This allows internal addresses generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

Active low RASBK# signals are generated to directly drive DRAM banks. Active high CASBK and LBE signals are externally decoded with NAND gates to provide 16 active low CAS# signals. This scheme provides extra timing margin and lower cost since NAND gates are cheaper and faster than equivalent OR gates.

To maintain use of low cost DRAMs through the full 33 MHz range of the system, special cache support is added. This minimizes the external glue logic required by other systems. The chip set is easily interfaced to the Intel 385DX cache controller.

Full EEMS support is provided in hardware for the complete full LIM EMS 4.0® standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill to 256k for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to E0000h. These twelve registers can alternatively be mapped in the A0000-BFFFFh and D0000-DFFFFh range by changing a configuration bit in the 82346. All registers are capable of translating over the complete 64 MByte range of on-board DRAM. Users preferring an alternate plug-in EMS solution can disable the on-board EMS system as well as system board DRAM, as required, down to 256k.

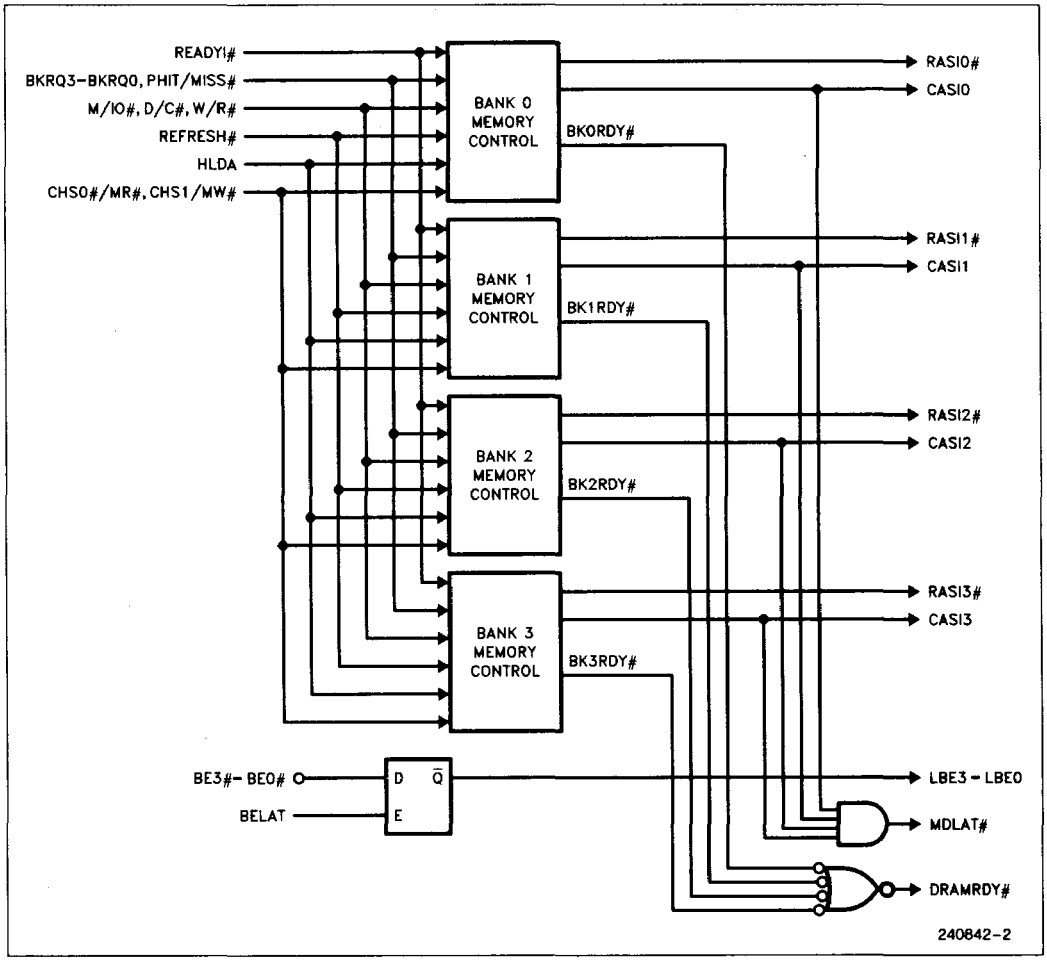
Shadowing features are supported on all 16k boundaries between 640k and 1M. EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided. These controls are overridden by EMS in segments for which it is enabled.

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

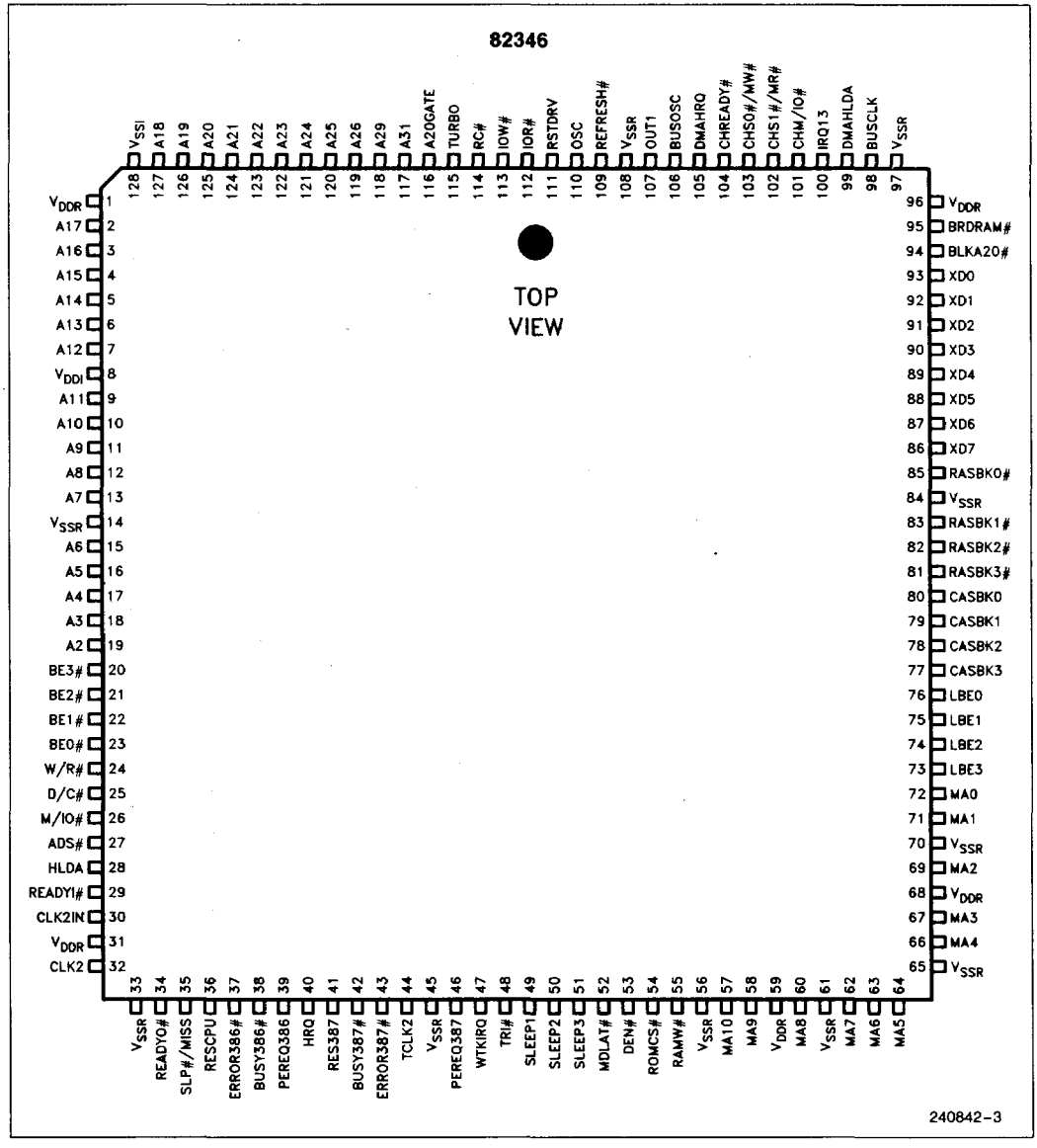
The System Controller is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller, which actually interfaces with the bus. The bus may run synchronously with the CPU's CLK2 or asynchronously via an external oscillator. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3 or 4.

LIM EMS 4.0® is a registered trademark of Lotus Development Corporation, Intel Corporation, and Microsoft Corporation.

MEMORY CONTROLLER BLOCK DIAGRAM



PIN DIAGRAM


82346
TOP
VIEW
1 VDDR
2 A17
3 A16
4 A15
5 A14
6 A13
7 A12
8 VDDI
9 A11
10 A10
11 A9
12 A8
13 A7
14 VSSR
15 A6
16 A5
17 A4
18 A3
19 A2
20 BE3#
21 BE2#
22 BE1#
23 BE0#
24 W/R#
25 D/C#
26 M/IO#
27 ADS#
28 HLDA
29 READYI#
30 CLK2IN
31 VDDR
32 CLK2
33 VSSR
34 READYO#
35 SLP#/MISS
36 RESCPU
37 ERROR386#
38 BUSY386#
39 PEREQ386
40 HRQ
41 RES387
42 BUSY387#
43 ERROR387#
44 TCLK2
45 VSSR
46 PEREQ387
47 WTKIRQ
48 TRI#
49 SLEEP1
50 SLEEP2
51 SLEEP3
52 MDLAT#
53 DEN#
54 ROMCS#
55 RAMW#
56 VSSR
57 MA10
58 MA9
59 VDDR
60 MA8
61 VSSR
62 MA7
63 MA6
64 MA5
65 VSSR
66 MA4
67 MA3
68 VDDR
69 MA2
70 VSSR
71 MA1
72 MA0
73 LBE3
74 LBE2
75 LBE1
76 LBE0
77 CASBK3
78 CASBK2
79 CASBK1
80 CASBK0
81 RASBK3#
82 RASBK2#
83 RASBK1#
84 VSSR
85 RASBK0#
86 XD7
87 XD6
88 XD5
89 XD4
90 XD3
91 XD2
92 XD1
93 XD0
94 BLKA20#
95 BRDRAM#
96 VDDR
97 VSSR
98 BUSCLK
99 DMAHLDA
100 IRQ13
101 CHM/IO#
102 CHS1#/MR#
103 CHS0#/MW#
104 CHREADY#
105 DMAHRQ
106 BUSOSC
107 OUT1
108 VSSR
109 REFRESH#
110 OSC
111 RSTDRV
112 IOR#
113 IOW#
114 RC#
115 TURBO
116 A20GATE
117 A31
118 A29
119 A26
120 A25
121 A24
122 A23
123 A22
124 A21
125 A20
126 A19
127 A18
128 VSSI
240842-3

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A31, A29, A26	119–117	I-TPU	A26 is used to prevent aliasing above 64 MByte. A29 is used to separate upper BIOS accesses from Weitek 3167 accesses. A 31 is used to determine 387DX accesses. These address lines are driven only by the CPU. When HLDA is active, these signals are held low internally. Since externally these pins are three-stated, this is required in order to prevent errant Bus Master and DMA accesses to on-board memory.
A25–2	120–127, 2–7, 9–13, 15–19	I-TTL	Address bits driven by the CPU when it is Bus Master. They are driven by the 82344 Bus Controller whenever HLDA is active. These bits allow direct access of up to 64 Mbytes of memory.
BE3# – BE0#	20–23	I-TTL	**BYTE ENABLES 3 THROUGH 0, ACTIVE LOW:** These signals are driven by the CPU or the 82344.
W/R#	24	I-TPU	WRITE or active low READ enable driven by the CPU. W/R# is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. The bus cycle types include: Interrupt Acknowledge, Halt, Shutdown, I/O Reads and Writes, Memory Data Reads and Writes, and Memory Code reads. WR# is internally pulled up.
D/C#	25	I-TPU	DATA or active low CODE enable driven by the CPU. D/C# is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/R# definition for bus cycle types. D/C# is internally pulled up.
M/IO#	26	I-TPU	MEMORY or active low I/O enable driven by the CPU. M/IO# is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/R# definition for bus cycle types. M/IO# is internally pulled up.
ADS#	27	I-TPU	**ADDRESS STROBE, ACTIVE LOW:** Driven by the CPU as an indicator that the address and control signals currently supplied by the CPU are valid. Ths signal is used internally to indicate that the data and command are valid and to determine the beginning of a memory cycle. ADS# is internally pulled up.
CLK2IN	30	I-CMOS	This is the main clock input to the System Controller and is connected to the CLK2 signal that is output by the System Controller. This signal is used internally to clock the System Controller's logic.
TCLK2	44	I-TTL	This input is connected to a crystal ocscillator whose frequency is equal to two times the system frequency. The TTL level oscillator output is converted internally to CMOS levels and sent to the CLK2 output.
CLK2	32	O	This output signal is a CMOS level converted TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
SLP#/MISS	35	IO-od	As a "power on reset" default, this bit is an output that reflects the inverse state of the SLEEP[7] configuration register bit. It is active low when sleep mode is active. Sleep mode is activated by setting SLEEP[7] = 1. When configuration register CTRL1(0) = 1, this pin becomes a MISS input for use with a future 82340 compatible product.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS (Continued)			
READYO#	34	O	**READY OUT, ACTIVE LOW:** This signal is an indication that the current memory or I/O bus cycle is complete. It is generated from the internal DRAM controller or the synchronized version of CHREADY# for slot bus accesses. Outside the chip it is ORed with any other local bus I/O or master such as a coprocessor or cache controller. The culmination of these ORed READY signals is sent to the 386DX and is also connected to the System Controller's ReadyL# input.
READYI#	29	I-TTL	**READY INPUT, ACTIVE LOW:** This signal is the ORed READY signals from the coprocessor, cache controller, or other optional add-in device. See the READYO# description for more details on how the signal is used inside the System Controller.
HLDA	28	I-TTL	**HOLD ACKNOWLEDGE, ACTIVE HIGH:** This signal is issued by the CPU in response to the HRQ driven by the System Controller. It indicates that the CPU is floating its outputs to the high impedance state so that another master can take control of the bus. When HLDA is active, the memory control is generated from CHS1#/MR# and CHS0#/MW# rather than CPU status signals.
HRQ	40	O	**HOLD REQUEST, ACTIVE HIGH:** Driven by the System Controller to the CPU, this output indicates that a bus master, such as a DMA or AT channel master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synchronized to CLK2.
RESCPU	36	O	**RESET CPU, ACTIVE HIGH:** This signal is sent to the CPU by the System Controller. It is issued in response to the control bit for software reset located in the Port A register or a dummy read to I/O port EFh. It is also issued in response to signals on the RSTDRV or RC inputs and in response to System Controller detection of a shutdown command. In all cases, it is synchronized to CLK2.
ERROR386#	37	O	**ERROR 386, ACTIVE LOW:** This signal is sent to the 386DX. On any CPU reset it is pulled low to set the 386DX to 32-bit coprocessor interface mode.
BUSY386#	38	O	**BUSY 386, ACTIVE LOW:** This signal is sent to the 386DX. The state of BUSY387# is always passed through to BUSY387# indicating that the 387DX is processing a command. On occurrence of an ERROR387# signal, it is latched and held active until an occurrence of a write to ports F0h, F1h, or RES387. The former case is the normal mechanism used to reset the active latched signal. The latter two are resets. Since ERROR387# generates IRQ13 for PC/AT-compatibility, BUSY386# is held active to prevent software access of the 387DX until the interrupt service routine writes F0h. The System Controller also activates BUSY386# for 16 CLK2 cycles when no 387DX is connected and I/O writes to the coprocessor space are detected.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS (Continued)			
PEREQ386	39	O	**PROCESSOR EXTENSION REQUEST 386, ACTIVE HIGH:** Sent to the CPU in response to a PEREQ387, which is issued by the coprocessor to the System Controller. It indicates to the CPU that the coprocessor is requesting a data operand to be sent to or from memory by the CPU. For PC/AT-compatiblity, PEREQ386 is returned active on occurrence of ERROR387# after BUSY387# has gone inactive. A write to F0h by the interrupt 13 handler returns control of the PEREQ386 signal to directly follow the PEREQ387 input.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
RAMW#	55	O	**RAM ACTIVE LOW WRITE OR ACTIVE HIGH READ:** Output to the 82345 Data Buffer and DRAM memory to control the direction of data flow of the on-board memory. It is a result of the address and bus control decode. It is active during memory write cycles and is high at all other times.
MA10–MA0	57, 58, 60, 62–64, 66, 67, 69, 71, 72	O	**MEMORY ADDRESSES 10 THROUGH 0:** These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the bus master addresses. Along with LBE3–LBE0 they allow addressing of up to 16 MBytes per bank.
RASBK3#–RASBK0#	81–83, 85	O	**ROW ADDRESS STROBE BANK 0 THROUGH 3, ACTIVE LOW:** These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is completely programmable.
CASBK3–CASBK0	77–80	O	**COLUMN ADDRESS STROBE BANK 0 THROUGH 3:** These signals are the respective column address strobes for each of the banks. These signals are externally gated (NAND) with the LBE signals to generate the CAS# strobes for each byte of a DRAM memory bank.
LBE3–LBE0	73–76	O	**LATCHED BYTE ENABLE 0 THROUGH 3, ACTIVE HIGH:** These signals select one of four banks to access memory data from when an on-board memory access is activated. They are the latched version of the CPU's BE3#–BE0# signals when the CPU is bus master or is the latched version of SA1, SA0, and BHE# when the master or DMA is in control.
REFRESH#	109	I-CMOS/ O-OD	**REFRESH SIGNAL, ACTIVE LOW:** This output is used by the System Controller to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the System Controller that it has decoded a refresh request command and is initiating an off-board refresh cycle.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
ON-BOARD MEMORY SYSTEM INTERFCE SIGNALS (Continued)			
ROMCS#	54	O	**ROM CHIP SELECT:** This output is active in CPU mode only (CPUHLDA is negated). It is active anytime the address on the A bus selects the address range between AFFE0000-AFFFFFFF, BFFE0000-BFFFFFFF, EFFE0000-EFFFFFFF, or FFFE0000h-FFFFFFFFh. It is also active during a memory read of 000E0000h-000FFFFFh when RAM-MAP[7] = 1. On reset, it also decodes the middle BIOS space between 00FE0000h-00FFFFFFh. However, this decode space can be changed via internal configuration register to System Board DRAM space after RESET if desired. NOTE: The lower ROM are from 00FE0000h-00FFFFFFh is impacted by shadow and/or EMS. Any 16k segments for which EMS is active (00EXXXXh only) or for which the shadow code had been changed from its 00b default are mapped out of the -ROMCS space.
COPROCESSOR SIGNALS			
PEREQ387	46	I-TPD	**COPROCESSOR EXTENSION REQUEST, ACTIVE HIGH:** this input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT-compatibility, this signal is gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQ386.
ERROR387#	43	I-TPU	This is an active low numerics signal which is driven by the coprocessor to indicate that an error has occurred in the previous instruction. This signal is decoded internally with BUSY387# to produce IRQ13.
BUSY387#	42	I-TPU	This is an active low numerics input signal which is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQ386 and BUSY386#.
RES387	41	O	**RESET 387, ACTIVE HIGH:** This output is connected to the 387DX reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the CPURESET signal is also activated. A write to port F1h only resets the coprocessor. A software FNINT signal must occur after an F1h generated reset before the coprocessor is reset to the same internal state that a 287 is put into by a hardware reset alone. For, compatibility, the F1h reset may be disabled by setting bit 6 of MISCSET to 1.
WTKIRQ	47	I-TPD	**WEITEK 3167 INTERRUPT REQUEST, ACTIVE HIGH:** An input from the Weitek 3167 coprocessor.
IRQ13	100	O	**INTERRUPT REQUEST 13, ACTIVE HIGH:** This signal is driven to the Bus Controller to indicate than an error has occurred within the coprocessor. This signal is a decode of the BUSY387# and ERROR387# inputs ORed with the WTKIRQ input.
BUS CONTROL SIGNALS			
CHREADY#	104	I-CMOS	**CHANNEL READY, ACTIVE LOW:** This signal is issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with ready signals from the coprocessor and DRAM controller to form the final version of READYO# which is sent to the CPU.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
BUS CONTROL SIGNALS (Continued)			
CHS0#/MW#	103	IO-TTL	**CHANNEL SELECT 0/MEMORY WRITE, ACTIVE LOW:** This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with CHS1# and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller. Activation of CPUHLDA reverses this signal to become an input from the Bus Controller. It is then a MEMW# signal for DMA or bus master access to system memory.
CHS1#/MR#	102	IO-TTL	**CHANNEL SELECT 1/MEMORY READ, ACTIVE LOW:** This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with CHS0# and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller. Activation of CPUHLDA reverses this signal to become an input from the Bus Controller. It is the a MEMR# signal for DMA or bus master access to system memory.
CHM/-IO	101	O	**CHANNEL MEMORY/ACTIVE LOW IO:** A decode of the M/IO# signal sent by the CPU to the System Controller. It is an indicator that the current bus cycle is a channel access. When combined with CHS0#, and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller.
BLKA20#	94	O	**BLOCK A20, ACTIVE LOW:** Driven to the Bus Controller to deactivate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 MByte memory boundary. Port A bit 1 may be directly written or set by a dummy read of I/O port EEh. BLKA20# is forced high when HLDA is active. (Refer to the "Sleep Mode Control Subsystem" section.)
BUSOSC	106	I-TTL	**BUS OSCILLATOR:** This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the System Controller's internal configuration registers are set for asynchronous slot bus mode. This signal is two times the AT bus clock speed (SYSCLK).
BUSCLK	98	O-TTL	**BUS CLOCK:** This is the source clock used by the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is a programmable division from CLK2 or BUSOSC when in a synchronous bus mode.
DMAHRQ	105	I-CMOS	**DMA HOLD REQUEST, ACTIVE HIGH:** This input is sent by the Bus Controller, it is internally synchronized by the System Controller before it is sent out to the CPU as the HRQ signal. It is the indicator of the DMA controller or an other bus masters' desire to control the bus.
DMAHLDA	99	O	**DMA HOLD ACKNOWLEDGE, ACTIVE HIGH:** This output to the Bus controller indicates that the current hold acknowledge state is for the DMA controller or an other bus master.
BRDRAM#	95	O	**BOARD DRAM, ACTIVE LOW:** An output to Bus Controller and Data Buffer to indicate that on-board DRAM is being addressed.
OUT1	107	I-CMOS	Indicate a refresh request from the Bus Controller.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
PERIPHERAL INTERFACE SIGNALS			
A20GATE	116	I-TTL	**ADDRESS BIT 20 ENABLE:** This is an input from the keyboard controller and is used internally along with Port A bit 1 to determine if address bit 20 from the CPU is true or gated low. It also determines the state of BLKA20#.
TURBO	115	I-TTL	**TURBO, ACTIVE HIGH:** This input to the System Controller determines the speed at which the system board operates. It is normally the externally ANDed signal from the keyboard controller and a turbo switch. It is internally ANDed with a software settable latch. When high, operation is full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET. A range is provided that allows slow operation at or below 8 MHz for any valid CPU speed. Slow speed takes precedence. When any one request for slow mode is present, slow mode is active. Turbo mode is active only when all TURBO requests are active.
RC#	114	I-TTL	**RESET CONTROL, ACTIVE LOW:** The falling edge of this signal causes a RESCPU signal. RC# is generated by the keyboard controller and its inverse is ORed with Port A bit 0 to form RESCPU.
SLEEP1	49	O-OD	**SLEEP SIGNAL 1, ACTIVE HIGH:** This pin is the logical OR of the enable and external control bits (bits 1 and 7) of the sleep indexed configuration register. It can be used with external interface logic to control external devices. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive. It is pulled low when inactive and three-states when active. An external pull-up is required. This allows an external interface to control logic operation at voltages different than VDD.
SLEEP2	50	O-OD	**SLEEP SIGNAL 2, ACTIVE HIGH:** This pin is the logical OR of the enable and external control bits (bits 2 and 7) of the sleep indexed configuration register. It can be used with external interface logic to control external devices. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive. It is pulled low when inactive and three-states when active. An external pull-up is required. This allows an external interface to control logic operation at voltages different than VDD.
SLEEP3	51	O-OD	SLEEP SIGNAL 3, ACTIVE HIGH: This pin is the logical OR of the enable and external control bits (bits 3 and 7) of the Sleep indexed configuration register. It can be used with external interface logic to control external devices. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive. It is pulled low when inactive and three-states when active. An external pull-up is required. This allows an external interface to control logic operation at voltages different than VDD.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE SIGNALS			
XD7-XD0	86-93	IO-TTL	**PERIPHERAL DATA BUS:** This bus is used to read and write the internal configuration registers.
DEN#	53	O	**DATA ENABLE, ACTIVE LOW:** This signal is an output to the 82345 Data Buffer to enable data transfers on the local bus. This signal is low during any CPU read cycles or INTA cycles.
IOR#	112	I-TTL	**I/O READ CYCLE, ACTIVE LOW:** Driven by the Bus Controller to indicate to the 82346 that an I/O read cycle is occurring on the bus. Whenever an I/O cycle occurs, the memory interface signals are inactive.
IOW#	113	I-TTL	**I/O WRITE CYCLE, ACTIVE LOW:** Driven by the Bus Controller to indicate to the 82346 that an I/O write cycle is occurring on the bus. Whenever an I/O cycle occurs, the memory interface signals are inactive.
RSTDRV	111	I-TTL	**RESET DRIVE, ACTIVE HIGH:** This reset signal is output by the Bus Controller. It indicates that a hardware reset signal has been activated. This is the same signal which is output to the channel. This signal is used to reset internal logic and to derive the RESCPU which is output by the System Controller.
MDLAT#	52	O	**MEMORY DATA BUS LATCH:** This is an output signal to the Data Buffer. On the rising edge, the Data Buffer latches the memory data bus. MDLAT# is low anytime one of the CASBK signals is high. When low, the Data Buffer latches are transparent.
OSC	110	I-TTL	**OSCILLATOR:** This is the buffered input of the external 14.318 MHz oscillator.
TEST MODE PIN			
TRI#	48	I1	**THREE-STATE:** This pin is used to drive all outputs to a high impedance state. When TRI# is low, all outputs and bidirectional pins are three-stated.
POWER AND GROUND PINS			
The power connections are split into an internal supply for the core-logic, and a pad-ring supply for the I/O drivers. Each supply should be individually bypassed with decoupling capacitors.			
VDDR	1, 31, 59, 68, 96	PWR	Pad-ring power connection, nominally +5V. These pins along with the VSSR pins should be separately bypassed.
VSSR	14, 33, 45, 56, 61, 65, 70, 84, 97 108	GND	Pad-ring ground connection, nominally 0V. These pins along with the VDDR pins should be separately bypassed.
VDDI	8	PWR	Internal core-logic power connection, nominally +5V. This pin along with the VSSI pin should be separately bypassed.
VSSI	128	GND	Internal core-logic ground connection, nominally 0V. This pin along with the VDDI pin should be separately bypassed.

Signal Type Legend

Signal Code	Signal Type
I-TTL	TTL Level Input
I-TPD	Input with 30 kΩ Pull-Down Resistor
I-TPU	Input with 30 kΩ Pull-Up Resistor
I-TSPU	Schmitt-Trigger Input with 30 kΩ Pull-Up Resistor
I-CMOS	CMOS Level Input
IO-TTL	TTL Level Input/Output
IT-OD	TTL Level Input/Open

Signal Code	Signal Type
IO-OD	Input or Open Drain, Slow Turn On
O	CMOS and TTL Level Compatible Output
O-TTL	TTL Level Output
O-TS	Three-State Level Output
I1	Input used for Testing Purposes
GND	Ground
PWR	Power