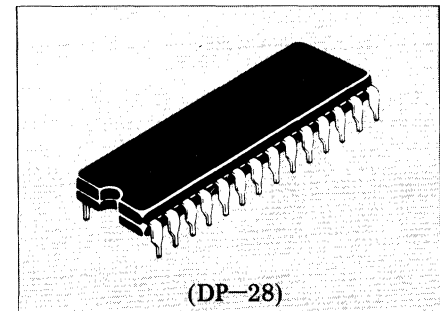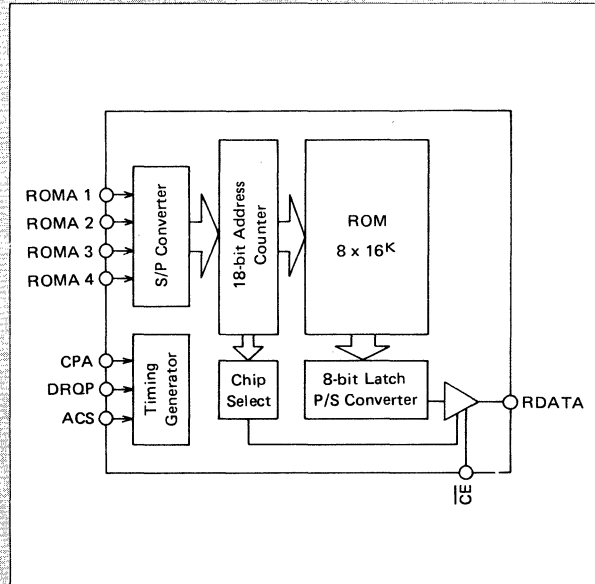# HITACHI MOS LSI HD44881

◎ HITACHI

128k-bit CMOS Speech Synthesis ROM

HD44881 is low speed large scale ROM for speech synthesis system. This LSI has a counter and a series/parallel data converter, and can be connected with speech synthesis LSI (HD61880 or HD61885) without external parts.
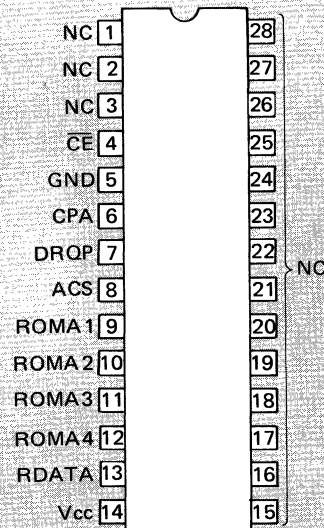
■ FEATURES

- 128k-bit (8 x 16k) Mask ROM
- 1 bit series output
- 18-bit internal address counter
- Chip select logic with mask program
- Low power dissipation by using CMOS dynamic ROM
    - Operating Power : 1 mW typ.
    - Standby Power : 5μW max.
- Single 5V power supply operation

(DP—28)

■ BLOCK DIAGRAM

■ PIN ASSIGNMENT

NC	1	28
NC	2	27
NC	3	26
CE	4	25
GND	5	24
CPA	6	23
DRQP	7	22 NC
ACS	8	21
ROMA1	9	20
ROMA2	10	19
ROMA3	11	18
ROMA4	12	17
RDATA	13	16
Vcc	14	15

(Top View)

■ SYSTEM SPECIFICATIONS
● Composition of Address Counter

As HD44881 is a dynamic ROM, clock (CPA) must be applied all the time during operation.

Since this LSI has an internal address counter, reading out of data needs only the setup of the starting address to the counter. After that operation, the following serial data can be read out automatically (without any treat of addresses). This function is useful to process the starting data such as speech data.

This address counter consists of 18 bits. The lower 14 bits are used for the internal address, and the upper 4 bits are for the selection of chips (called page address). Since this counter is a 18-bit serial counter, there is no need to set up the address counter again even while the page is changed (transmission between chips). The page addresses given to each chip are determined when ROM is designed, and then programmed with mask.
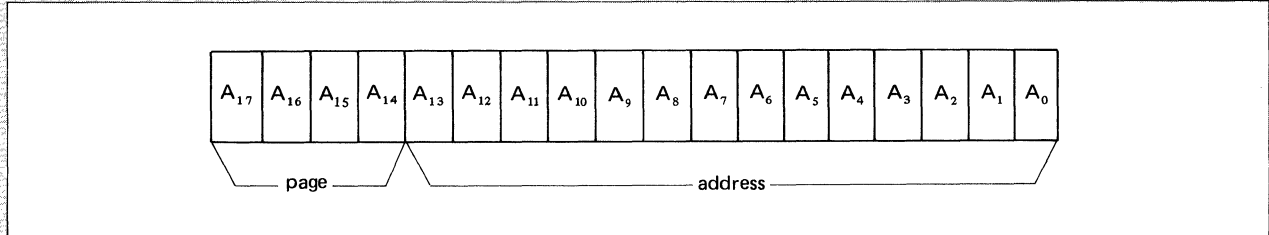
● Operating Timing Chart

Operating timing chart is shown below. These I/O timings are generated in the speech synthesis LSI, so that the user is not be bothered by these timings when connecting speech synthesis LSI with ROM directly.
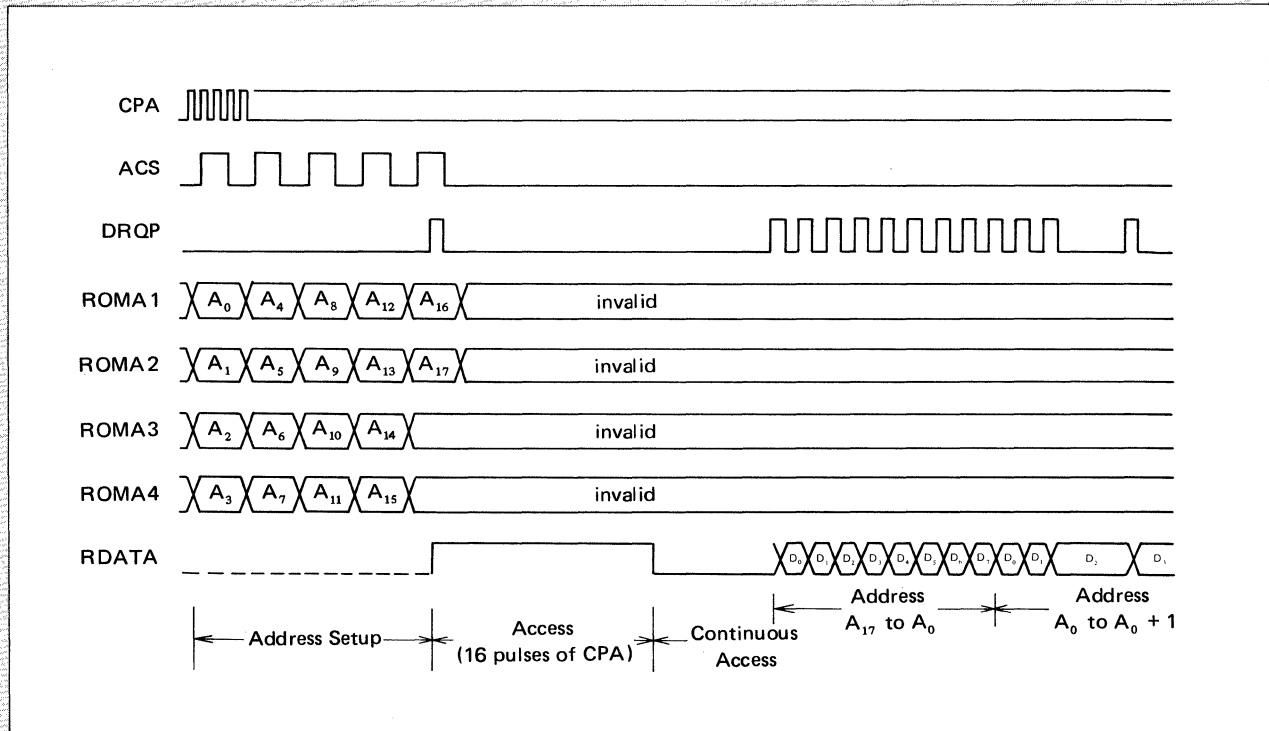
● Address Setup

The 18 bits data for address counter are applied from ROMA1 to ROMA4, as series input data by each 4 bits. ACS is a synchronous (shift) signal for series/parallel converting. When the final data is applied, ACS and DRQP signals shall be "High" to show the completion of data.

2

● **Access**

After the setup of the starting address data (ACS = DRQP = 1), RDATA output shall be "High" while ROM access is performing (16 pulses of CPA). At this time, data access is impossible. While RDATA is "Low" after 16 pulses of CPA, reading out of data is enable.

● **Continuous Access**

After the reading out become possible, serial data is read out by one bit per a DRQP (Data Request Pulse). These internal implementations, ROM access and series/parallel converting, are in pipeline system. So that, the serial access can be performed when the address is changing.

● **Standby Mode**

This LSI has a standby mode to achieve super low power dissipation. In this mode, the internal power supply of LSI is turned OFF by turning $\overline{CE}$ signal to "High". At this time, output terminal RDATA has high impedance.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage	V_T	-0.3 to Vcc $+0.3$	V
Supply Voltage	Vcc	-0.3 to $+7.0$	V
Operating Temperature	T_{opr}	-20 to $+75$	°C
Storage Temperature	T_{stg}	-55 to $+125$	°C

■ ELECTRICAL CHARACTERISTICS

● **DC Characteristics (Vcc = 5 V ± 10%, Ta = − 20 to +75°C)**

Item	Symbol	Test Condition	min	typ	max	Unit
Input Voltage	V_{IH}		Vcc − 1.0	—	—	V
	V_{IL}		—	—	1.0	V
Output Voltage	V_{OH}	$I_{OH} = -0.5\,mA$	Vcc − 0.6	—	—	V
	V_{OL}	$I_{OL} = 0.5\,mA$	—	—	0.6	V
Input Leakage Current	I_{IL}	$V_{IN} = 0$ to Vcc	—	—	1.0	μA
Output Leakage Current	I_{OL}	$V_{IN} = 0$ to Vcc At High Impedance	—	—	1.0	μA
Operating Supply Current	I_{CC}	No-Load Output Vcc or GND Input	—	—	500	μA
Standby Supply Current	I_{CCS}	No-Load Output $\overline{CE} = Vcc - 0.2\,V$	—	—	10	μA

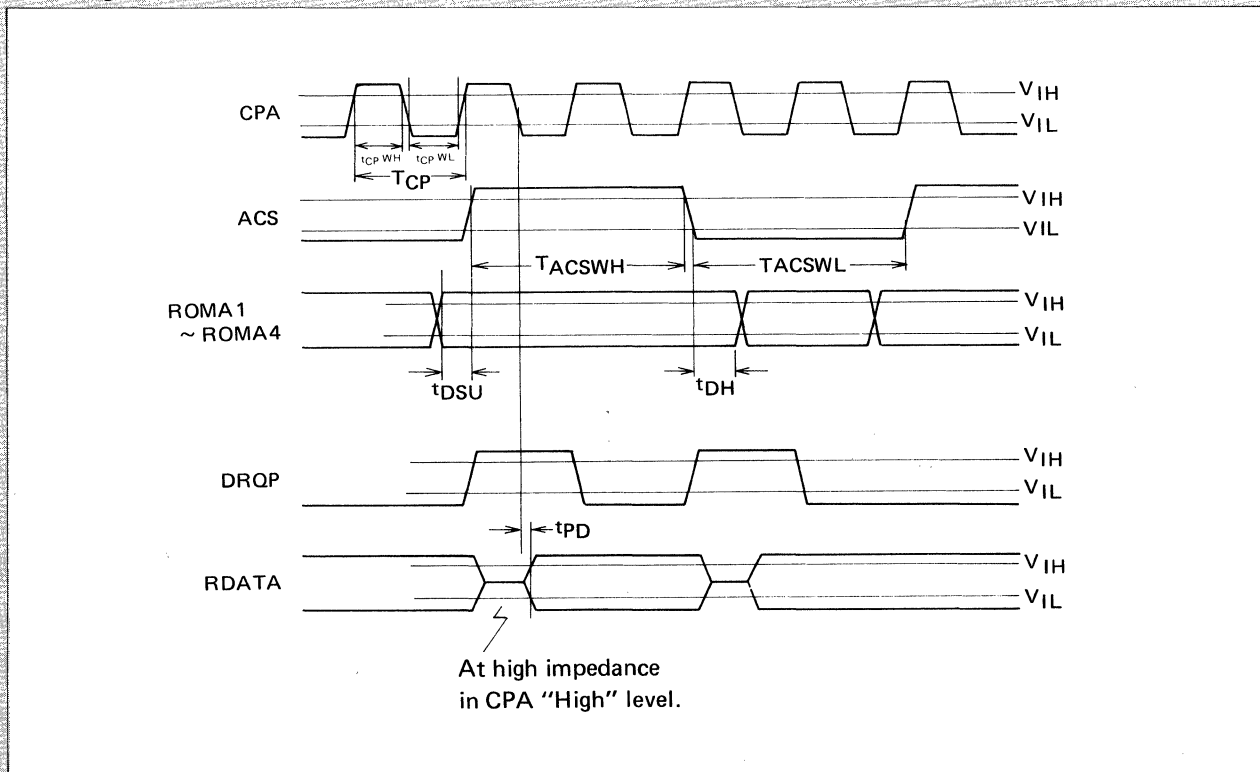● AC Characteristics (VCC = 5 V ± 10%, Ta = − 20 to + 75°C)

Item	Symbol	Value min	Value typ	Value max	Unit
Clock Cycle	f_{CP}	150	—	210	kHz
Clock Pulse Width	t_{CPWH}	2.0	—	—	μs
	t_{CPWL}	2.0	—	—	μs
ACS Pulse Width *	t_{ACSWH}	$2 \cdot T_{CP}$	—	—	
	t_{ACSWL}	$2 \cdot T_{CP}$	—	—	
Data Setup Time	t_{DSU}	4.0	—	—	μs
Data Hold Time	t_{DH}	0	—	—	μs
Output Delay Time **	t_{PD}	—	—	4.0	μs

* Applied to direct addresses when microcomputer specifies them using HD61885.
When A16 and A17 are applied, ACS pulse width should be at least 3 times T_{CP}.

** $C_L = 100$pF

*** $T_{CP} = 1/f_{CP}$

● Timing Chart

At high impedance
in CPA "High" level.