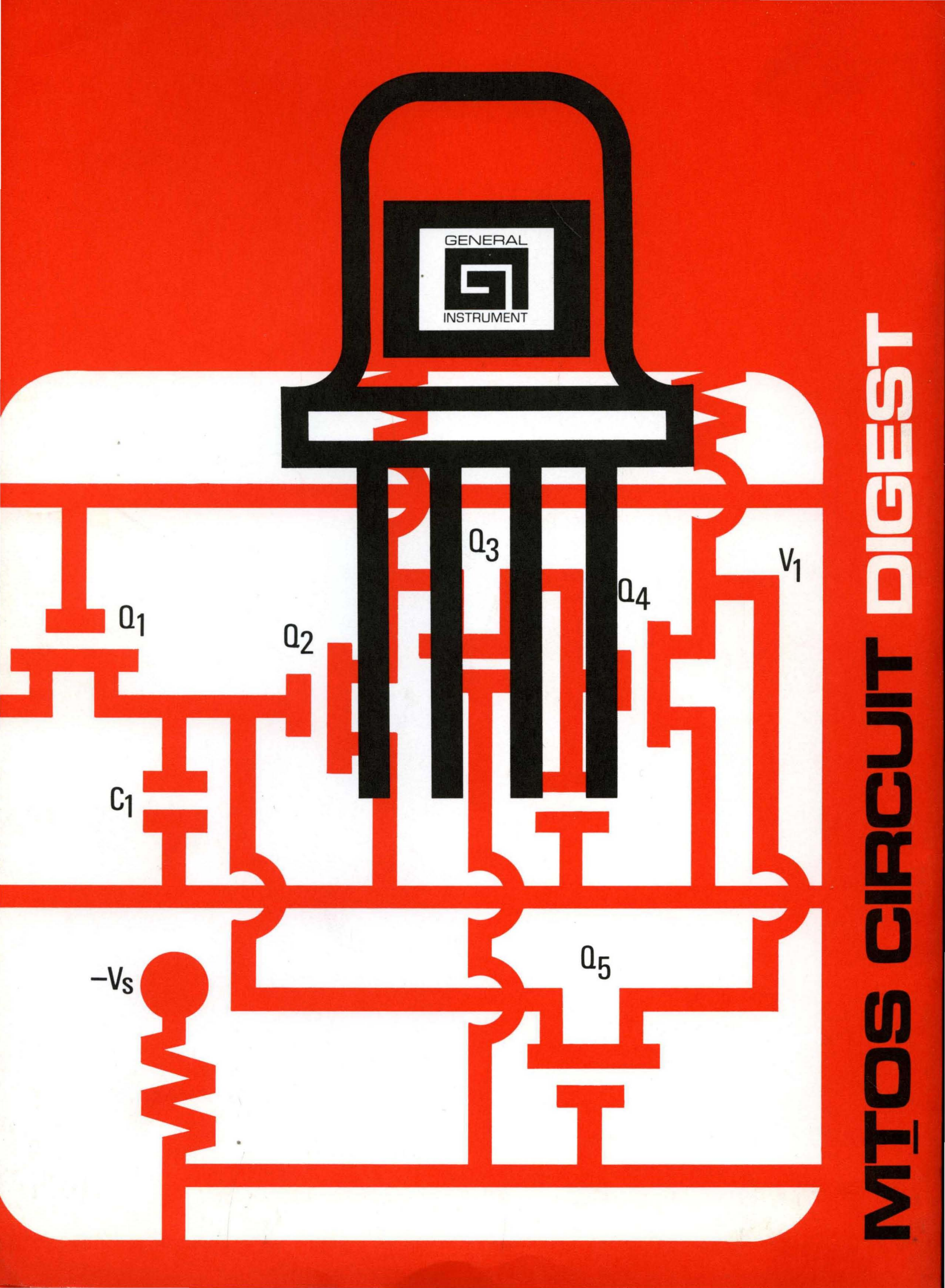
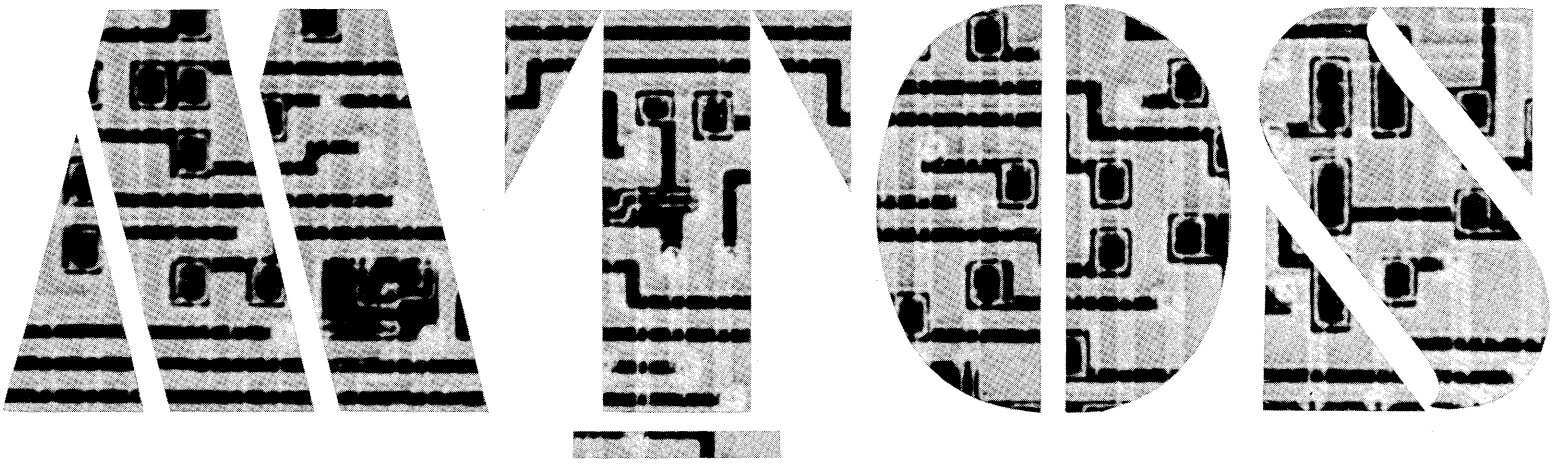
GENERAL INSTRUMENT

MTOS CIRCUIT DIGEST



GENERAL INSTRUMENT



CONDENSED CATALOG 1967

MTOS STANDARD PRODUCTS

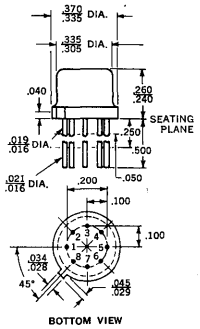
MTOS MICROCIRCUIT ARRAYS (T_A = −55°C to +85°C)

SHIFT REGISTERS		STATIC	DYNAMIC	FREQUENCY	NUMBER OF BITS	INPUT		OUTPUT		NUMBER OF CLOCKS	SUPPLY VOLTAGE (VOLTS)	CASE #
TYPE	FUNCTION					PARALLEL	SERIES	PARALLEL	SERIES			
MEM 3005PP	5-BIT PARALLEL IN/ PARALLEL OUT	X		dc to 1.0 MHz	5	X	X	X		2	−27V ± 1V	3,12
MEM 3005SP	5-BIT SERIAL IN/ PARALLEL OUT	X		dc to 1.0 MHz	5		X	X		2	−13V ± 1V −27V ± 1V	7,2
MEM 3008PS	8-BIT 2ϕ PARALLEL IN/SERIAL OUT	X		dc to 1.0 MHz	8	X	X		X	2	−13V ± 1V −27V ± 1V	3,12
MEM 3012SP	12-BIT SERIAL IN/ PARALLEL OUT	X		dc to 1.0 MHz	12		X	X		1	−27V ± 1V	3,12
MEM 3016-2	DUAL 16-BIT	X		dc to 1.0 MHz	32(16,16)		X		X	2	−13V ± 1V −27V ± 1V	7
MEM 3016-2D	DUAL 16-BIT		X	10 kHz to 1.0 MHz	32(16,16)		X		X	2	−13V ± 1V −27V ± 1V	7
MEM 3020	20-BIT	X		dc to 1.0 MHz	20		X		X	2	−13V ± 1V −27V ± 1V	2
MEM 3021	21-BIT	X		dc to 500 kHz	21(1,4,16)		X		X	1	−27V ± 1V	7
MEM 3021B	21-BIT	X		dc to 250 kHz	21(1,4,16)		X		X	1	−27V ± 1V	7
MEM 3032	6-1ϕ BINARY WEIGHTED	X		dc to 1.0 MHz	32(1,1,2,4,8,16)		X		X	1	−13V ± 1V −27V ± 1V	3,12
MEM 3050	DUAL 25-BIT		X	10 kHz to 500 kHz	50(25,25)		X		X	2	−27V ± 1V	7
MEM 3064	64-BIT SERIAL ACCUMULATOR		X	10 kHz to 5.0 MHz	64		X		X	4	NONE	6,7,11
MEM 3100	DUAL 50-BIT		X	10 kHz to 1.0 MHz	100 (50,50)		X		X	2	−13V ± 1V −27V ± 1V	6,7,11

LARGE DIGITAL SUBSYSTEMS		POWER CONSUMPTION	SUPPLY VOLTAGE (VOLTS)	CLOCK RATE	DESCRIPTION	CASE #
TYPE	FUNCTION					
MEM 5014	A/D-D/A CONVERTER ELEMENT	135 mW	−27V ± 2V	dc to 200 kHz	Complete logic and analog switching for 10-bit successive approximation A/D converter.	10
MEM 5015	16 CHANNEL RANDOM ACCESS MULTIPLEXER	70 mW	−27V ± 1V	100 kHz	Sixteen Channel Multiplexer with address storage and decoding.	10
MEM 5116	16 CHANNEL RANDOM SEQUENTIAL ACCESS MULTIPLEXER	100 mW	−27V ± 1V	100 kHz	Sixteen Channel Multiplexer with parallel access counter and decoding.	10
MEM 5021	DDA ELEMENT	100 mW	−13V ± 1V −27V ± 1V	500 kHz	Ternary type DDA performing rectangular integration.	9
MEM 5031	SERVO ADDER	25 mW	−13V ± 1V −27V ± 1V	dc to 1.0 MHz	Shift Register content decision unit used in conjunction with the MEM 5021	6,7,11
MEM 5035	SIGMA DELTA "Y" SUMMER	25 mW	−13V ± 1V	10 kHz to 1.0 MHz	2 Input Delta "Y" Summer used in conjunction with the MEM 5021	6,11
S-C-100	MINIATURE A/D CONVERTER SYSTEM	300 mW	−27V ± 2V −15V ± 2V +15V ± 2V REF. VOLT	100 kHz	Complete 10-BIT A/D Converter System	*

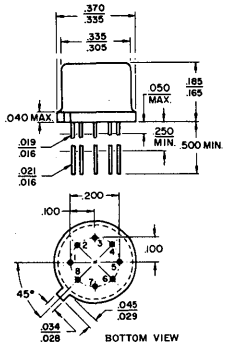
*29 pin ELCO connector

CASE 1



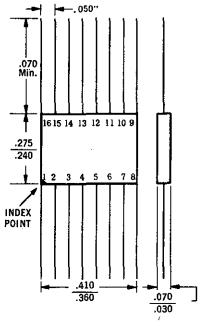
TO-77

CASE 2



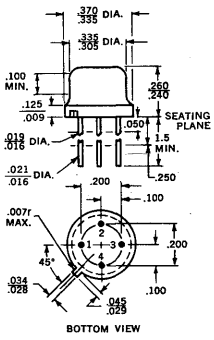
TO-78

CASE 3



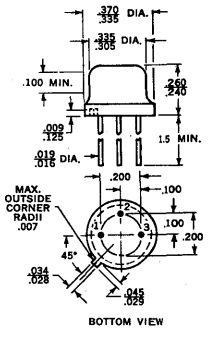
16 LEAD FLAT PACK

CASE 4



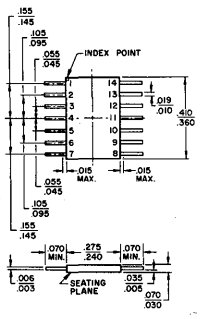
TO-33

CASE 5



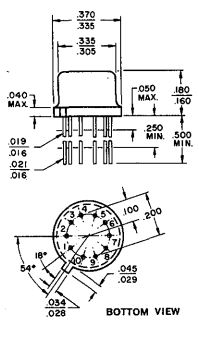
TO-5

CASE 6



TO-87

CASE 7



TO-74

MTOS STANDARD PRODUCTS

MTOS SILICON P-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTORS ($T_A = 25°C$, BODY GROUNDED)										
TYPE	V_{GST} (VOLTS TYP)	I_D (ON) (mA TYP)	I_{DSS} (nA TYP)	I_{GSS} (nA TYP)	BV_{DSS} (VOLTS)	BV_{GSS} (VOLTS)	Y_{fs} (μmho TYP)	C_{gd} (pf TYP)	r_{DS} ON (Ω TYP)	CASE #
MEM 511	—4.0	—6	—0.5	—0.1	—30	—30	2500	2.0	150	8
MEM 517	—3.5	—60	—0.8	—0.1	—30	—25	12,000	10	30	4
MEM 517A	—3.5	—60	—0.8	—0.1	—30	—25	12,000	10	30	5
MEM 517B	—3.5	—60	—0.8	—0.1	—30	—25	12,000	10	30	8
MEM 520	—4.0	—6	—0.5	— .03	—30	NA	2500	2.0	150	8
MEM 550	—4.0	—5	—0.1	—0.1	—30	—25	1400	1.1	250	1
MEM 551	—4.0	—5	—0.5	— .03	—30	NA	1400	1.1	250	1
2N4353	—4.0	—6	—0.5	—0.1	—30	—30	2500	2.0	150	8

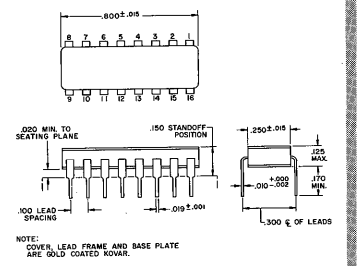
LOGIC CIRCUITS ($T_A = -55°C$ to $+85°C$)		POWER CONSUMPTION (mW)	SUPPLY VOLTAGE (VOLTS)	PROPAGATION DELAY (ns)	CAPACITANCE (pf) (TYP)	FREQUENCY (kHz)	CASE #
TYPE	FUNCTION						
MEM 1000	DUAL FULL ADDER	< 70 TOTAL	−13V ±1V −27V ±1V	350 (TYP)	3.0	——	6,11
MEM 1002	DUAL 3-INPUT NOR GATE	< 40 (MAX)	−27V ±1V	200 (TYP)	3.0	——	7
MEM 1005	R-S-T FLIP-FLOP	< 80	−27V ±1V	950 (MAX)	3.0	dc to 500 kHz	7
MEM 1008	DUAL EXCLUSIVE OR/NOT GATE	50 (TYP)	−27V ±1V	500 (TYP)	3.0	——	7
MEM 1013	QUAD 2 INPUT NOR GATE	9 mW/circuit	−13V ±1V −27V ±1V	300 (TYP)	3.0	——	3,12
MEM 1014	QUAD 2 INPUT AND GATE	14 [Circ. (1,2,3)] 42 [Circuits 4,5]*	−13V ±1V −27V ±1V	300 (TYP)	3.0	——	3,12
MEM 1015	DUAL J K FLIP-FLOP	60	−13V ±1V −27V ±1V	——	3.0	dc to 1.0 MHz	9
MEM 1022	9-BIT PARALLEL PARITY DETECTOR	50	−27V ±1V	500 (TYP)	3.0	dc to 500	6,11
MEM 1050	4 STAGE BINARY UP-DOWN COUNTER	300	−27V ±1V	——	2.0	——	3,12
MEM 1051	BUFFERED D/A CONVERTER	25	-13V ±1.5V −25V ±3V	——	3.0	dc to 500 kHz	6,11

*The MEM 1014 provides Four 2-Input and Gates (Circuits 1, 2, 3, 4) plus One 2-Input N and Gate (Circuit 5)

MULTIPLEXER CIRCUITS ($T_A = -55°C$ to $+85°C$)		OFF RESISTANCE (Ω TYP)	ON RESISTANCE (Ω TYP)	CAPACITANCE (pf) Cgd	BV_{DSS} (VOLTS)	BV_{GSS} (VOLTS)	CASE #
TYPE	FUNCTION						
MEM 2002	5 CHANNELS (4 Channels —Common Drain)	10^{10}	200	1.1	−30	−30	6,11
MEM 2003	4 CHANNELS (Protective Diodes)	10^{10}	200	1.1	−30	−30	7
MEM 2004	4 CHANNELS (No Diodes)	10^{10}	200	1.1	−30	±60	7
MEM 2005	4 CHANNELS (Dual 2 Channel)	10^{10}	200	1.1	−30	−30	6,11
MEM 2006	3 CHANNELS (2 Channels —Common Drain)	10^{10}	200	1.1	−30	−30	7
MEM 2009	6 CHANNELS (Protective Diodes)	10^{10}	150	1.9	−30	−30	6,11
MEM 2017	6 CHANNELS (Protective Diodes)	10^{10}	700	0.5	−50	−50	6,11

SERIES SHUNT CHOPPER		OFFSET VOLTAGE	CLOCK ϕ	FREQUENCY (kHz)	ON RESISTANCE PER UNIT (SERIES OR SHUNT) (Ω TYP)	OFF RESISTANCE PER UNIT (SERIES OR SHUNT) (Ω TYP)	SIGNAL VOLTAGE HANDLING RANGE (TYP)	CASE #
TYPE	FUNCTION							
MEM 2008	INTEGRATED SERIES SHUNT CHOP. CIRCUIT	0	1	100	6K	10^{12}	1μV−10V	2

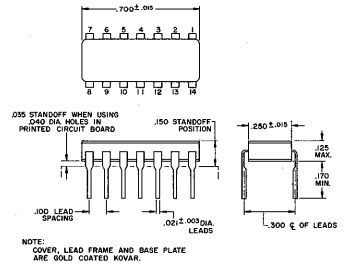
CASE 12



NOTE: COVER, LEAD FRAME AND BASE PLATE ARE GOLD COATED KOVAR.

DUAL IN-LINE 16 LEAD

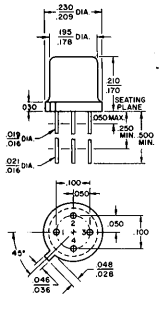
CASE 11



NOTE: COVER, LEAD FRAME AND BASE PLATE ARE GOLD COATED KOVAR.

DUAL IN-LINE 14 LEAD

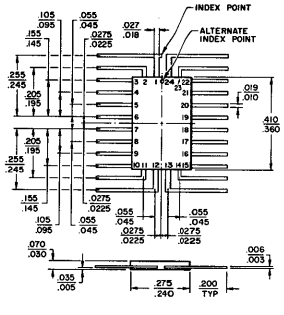
CASE 8



BOTTOM VIEW

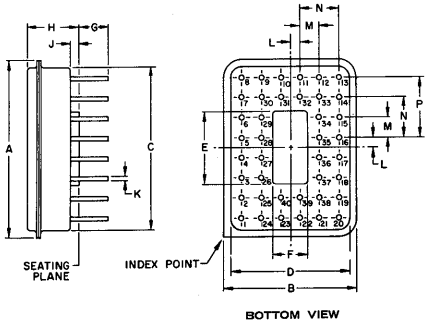
TO-72

CASE 9



24 LEAD FLAT PACK

CASE 10



BOTTOM VIEW

SYMBOL	INCHES MIN.	INCHES MAX.
A	.880	.895
B	.685	.695
C	.812	.820
D	.609	.620
E	.365	.385
F	.175	.195
G	.125	.160
H	.264 REF.	
J	.031	.075
K	.018	.022
L	.0475	.0525
M	.095	.105
N	.195	.205
P	.295	.305

40 LEAD IN-LINE

Note: All dimensions in inches.

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Printed in U.S.A.

GENERAL INSTRUMENT

MTOS TRANSISTOR

P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
March, 1967

MEM 511

FEATURES:

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:

(Designed Primarily For Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers

MAXIMUM RATINGS:

($T_A = 25°C$, unless otherwise specified)

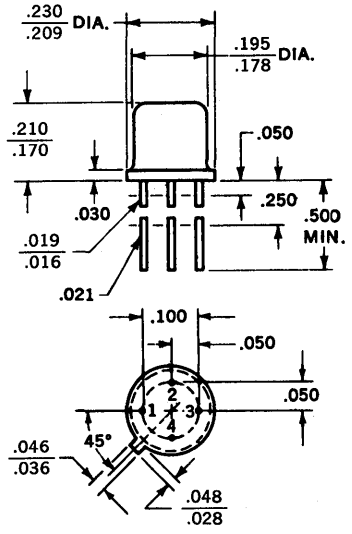
Drain to Source Voltage ..... —30V
Gate to Source Voltage ..... —30V
Gate to Drain Voltage ..... —30V
Drain Current ..... —50mA
Gate Current (Forward Direction for Zener Clamp) ..... +0.1mA
Storage Temperature ..... —50 to 150°C
Operating Junction Temperature ..... —50 to 125°C
Total Dissipation at 25°C Case Temperature 650mW
Total Dissipation at 25°C Ambient Temperature 225mW

ELECTRICAL CHARACTERISTICS:

($T_A = 25°C$, unless otherwise specified — body grounded).

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate Source Cutoff Voltage	—3		—6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		—0.5	—10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current			—1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	— 3	—6		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	—30			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, $V_{GS} = V_{DS} = -10V$ 10MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			3	pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance			2.5	pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	$V_{GS} = -15V$, $I_{DS} = -1mA$

TO-72 PACKAGE

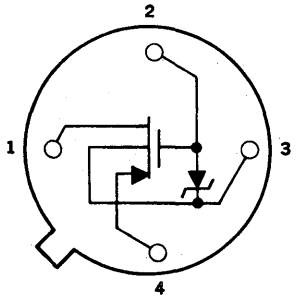


Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

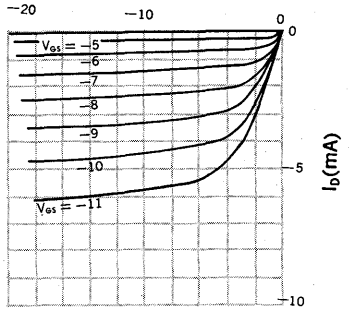
Lead
1. Drain
2. Gate
3. Body (Case)
4. Source



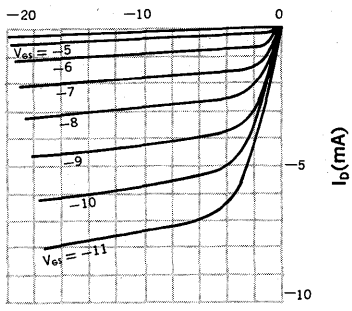
T6001C

TYPICAL CHARACTERISTIC CURVES
MEM 511

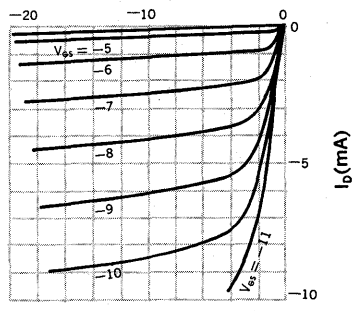
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



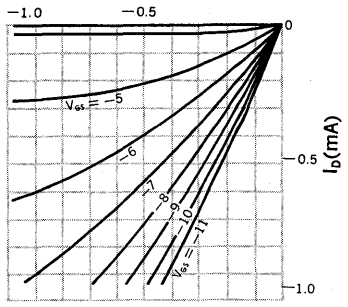
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



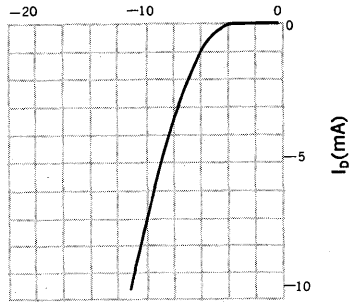
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



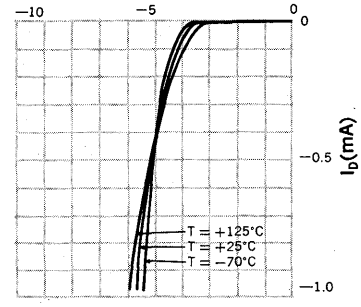
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



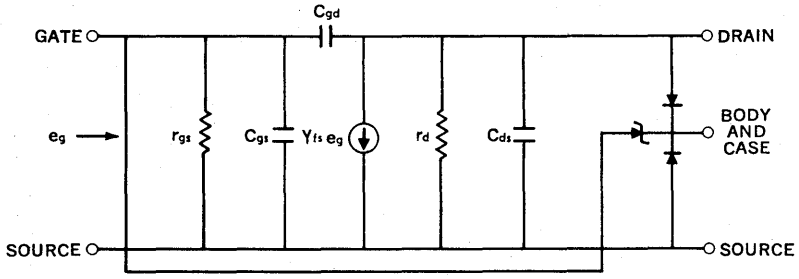
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6$ mA



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

HANDLING PRECAUTIONS

MEM 511 insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10^{15} ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

GENERAL INSTRUMENT

MTOS TRANSISTOR

P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
March, 1967

2N4353

FEATURES

- 10^{12} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF and IF amplifiers
- Multiplexers
- Analog switches

MAXIMUM RATINGS:

Temperature

Storage Temperature Range, T_{stg} ..... −60°C to 125°C

Lead (Terminal) Temperature, 1/16" from the seated surface (or case) for 10 seconds ..... 230°C

Voltage at 25°C Free-Air Temperature

Forward Gate-Source Voltage ..... −30V

Drain-Source Voltage ..... −30V

Drain-Gate Voltage ..... −30V

Current

Reverse Gate Current ..... +1 mA

Forward Gate Current ..... −.01 mA

Drain Current ..... −100 mA

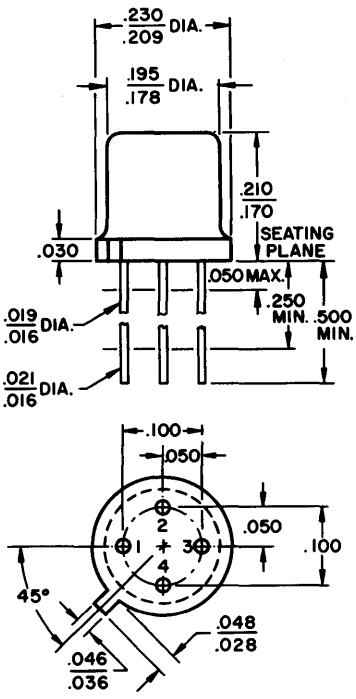
Power

Continuous Device Dissipation at or below 25°C Free-Air Temperature ..... 250 mW

Linear Derating Factor ..... 2 mW/°C

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$I_{G(f)}$	Gate Forward Current		−1.0	nA	$V_{GS} = -20V$, $V_{DS} = 0V$
$I_{G(f)}$	Gate Forward Current		−50	nA	$V_{GS} = -20V$, $V_{DS} = 0V$, $T_A = 85°C$
$V_{(BR)GSS}$	Gate-Source Reverse Breakdown Voltage		+3.0	V	$I_G = 1$ mA, $V_{DS} = 0V$
$V_{GS(f)}$	Gate-Source Forward Voltage	−30	−60	V	$I_G = -.01$ mA, $V_{DS} = 0V$
BV_{SDS}	Source-Drain Breakdown Voltage	−30		V	$I_S = -.01$ mA, $V_{GD} = 0V$
BV_{DSS}	Drain-Source Breakdown Voltage	−30		V	$I_D = -.01$ mA, $V_{GS} = 0V$
$I_{D(on)}$	"ON" Drain Current	−30		mA	$V_{DS} = -10V$, $V_{GS} = -20V$ Pulse Test: 300 μs pw, 2% Duty-Cycle
V_{GS}	Gate-Source Voltage	−7.0	−13	V	$V_{DS} = -10V$, $I_D = -10$ mA
$V_{GS(th)}$	Gate-Source Threshold Voltage	−3.0	−5.0	V	$V_{DS} = -10V$, $I_D = -10$ μA
I_{DSS}	Zero-Gate-Voltage Drain Current		−5	nA	$V_{DS} = -10V$, $V_{GS} = 0V$
I_{SDS}	Zero-Gate-Voltage Source Current		−5	nA	$V_{SD} = -10V$, $V_{GD} = 0V$
$r_{DS(on)}$	Static Drain-Source "ON" Resistance		300	Ohms	$I_D = -0.1$ mA, $V_{GS} = -20V$
Y_{fs}	Transadmittance	1000	4000	μmhos	$V_{DS} = -10V$, $I_D = -10$ mA
Y_{os}	Output Admittance		350	μmhos	1 kHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{ISS}	Input Capacitance		12	pF	1 MHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{RSS}	Reverse Transfer Capacitance		4	pF	1 MHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{DGO}	Drain-Gate Capacitance		4	pF	1 MHz $V_{DG} = -10V$, $I_S = 0$ mA
$Re_{(Yfs)}$	Forward Transconductance	900		μmhos	30 MHz $V_{DS} = -10V$, $I_D = -10$ mA

TO-72



Bottom view

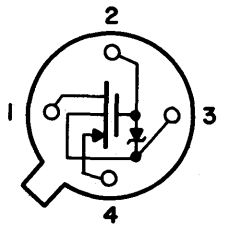
NOTE: All dimensions in inches

TERMINALS

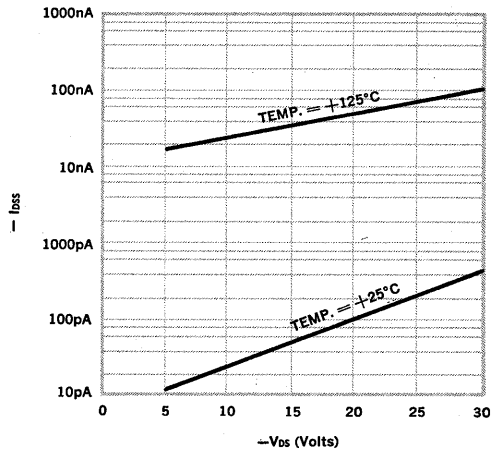
LEAD	FUNCTION
1	Drain
2	Gate
3	Body (Case)
4	Source

NOTE: Case Material — Metallic (Electrically Non-insulated)

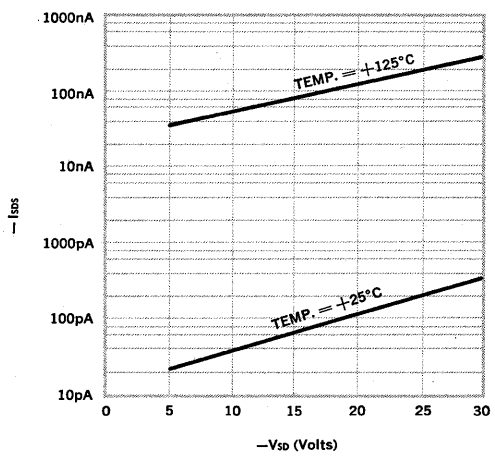
TERMINAL DIAGRAM



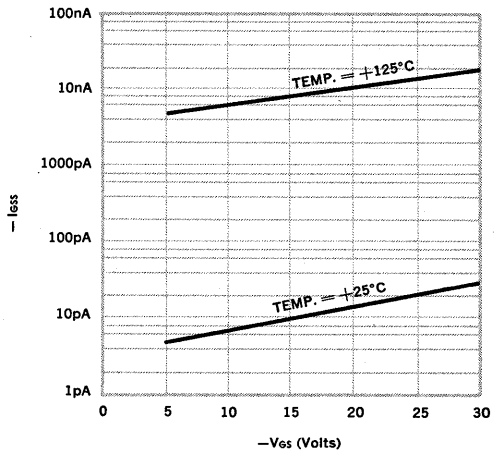
DRAIN LEAKAGE VS DRAIN VOLTAGE



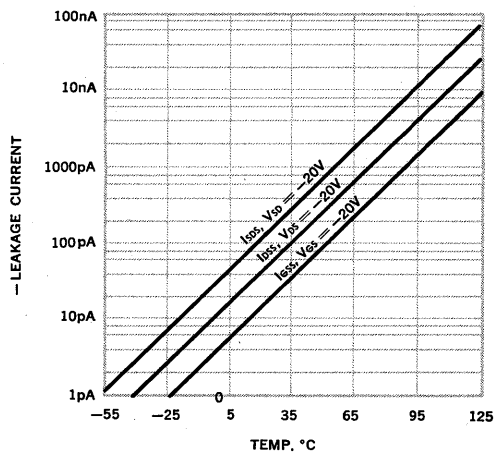
SOURCE LEAKAGE VS SOURCE VOLTAGE



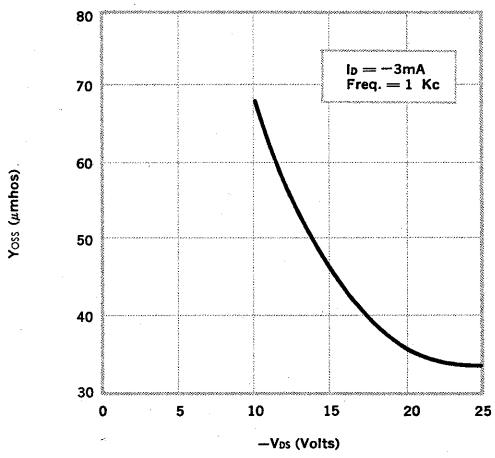
GATE LEAKAGE VS GATE VOLTAGE



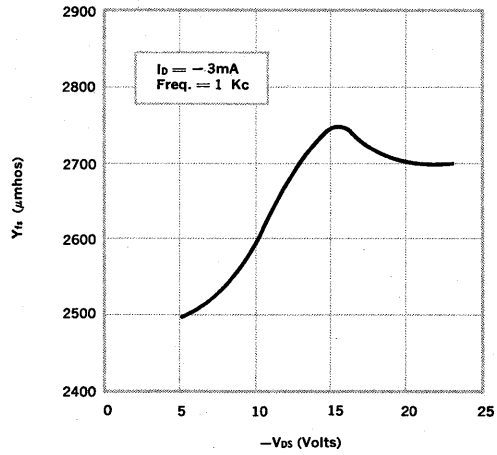
LEAKAGE CURRENT VS TEMPERATURE



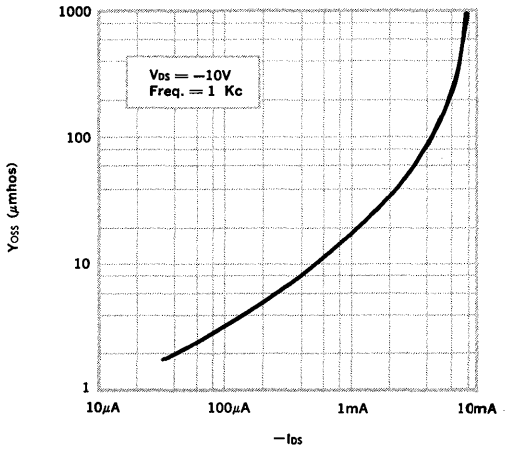
OUTPUT ADMITTANCE VS DRAIN VOLTAGE



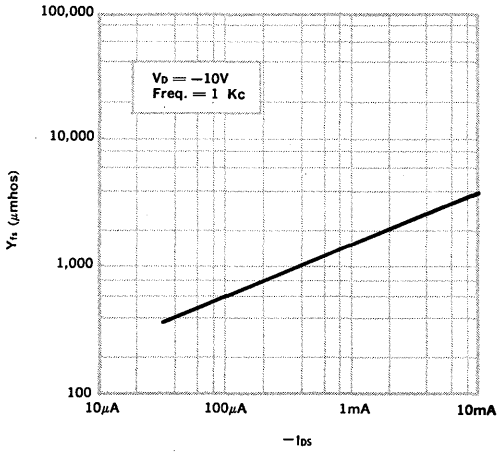
FORWARD TRANSADMITTANCE VS DRAIN VOLTAGE



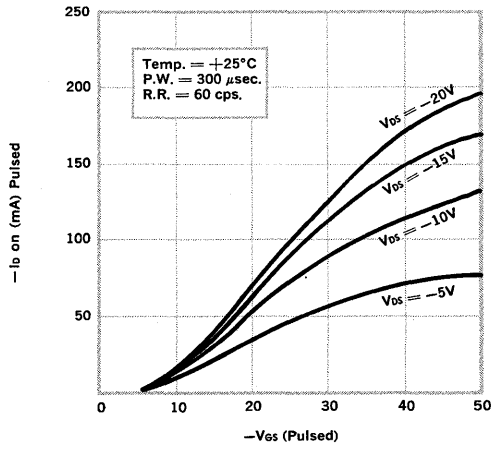
OUTPUT ADMITTANCE VS DRAIN CURRENT



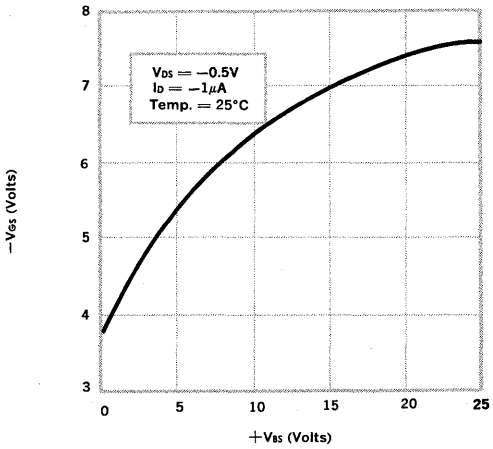
FORWARD TRANSADMITTANCE VS DRAIN CURRENT



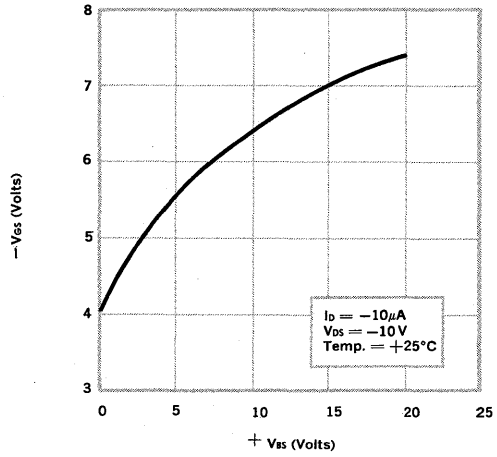
DRAIN CURRENT (PULSED) VS GATE VOLTAGE (PULSED)



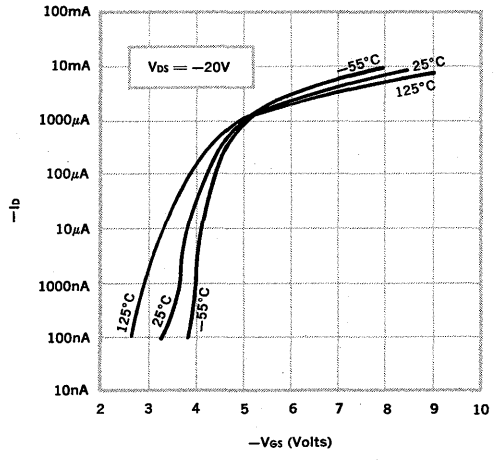
GATE VOLTAGE VS BODY TO SOURCE VOLTAGE



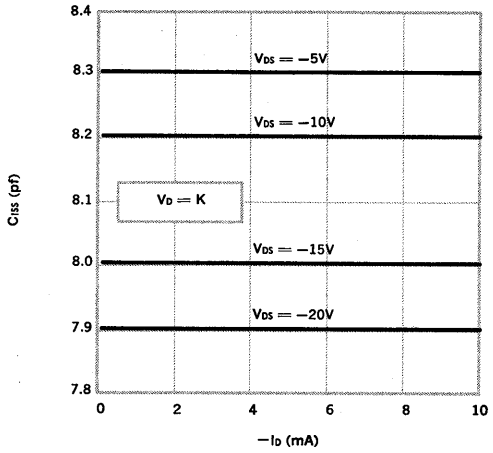
GATE VOLTAGE VS BODY TO SOURCE VOLTAGE



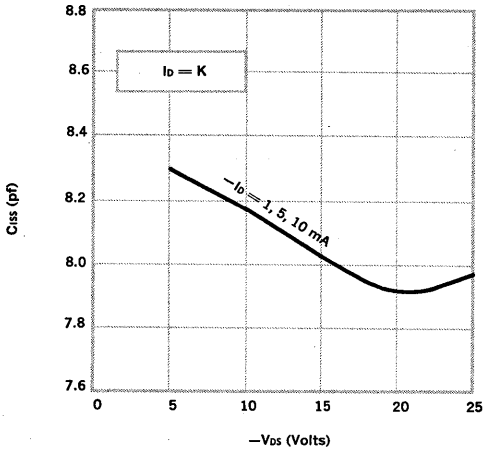
DRAIN CURRENT VS GATE VOLTAGE



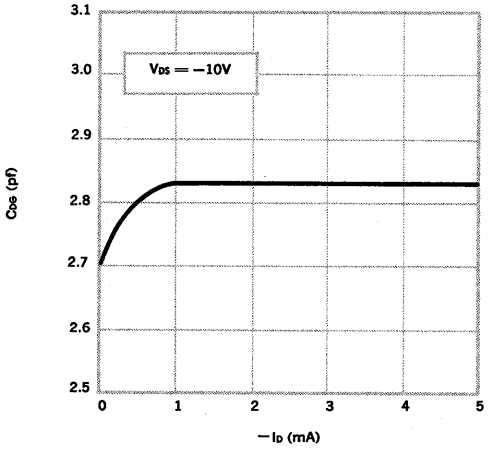
INPUT CAPACITANCE VS DRAIN CURRENT



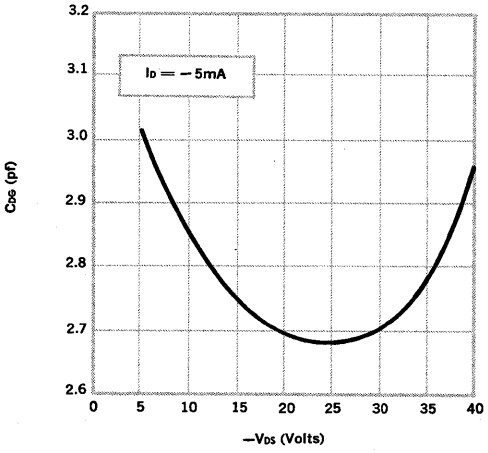
INPUT CAPACITANCE VS DRAIN VOLTAGE



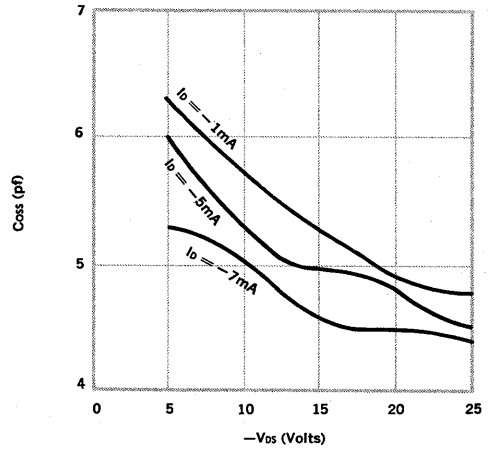
DRAIN TO GATE CAPACITANCE VS DRAIN CURRENT



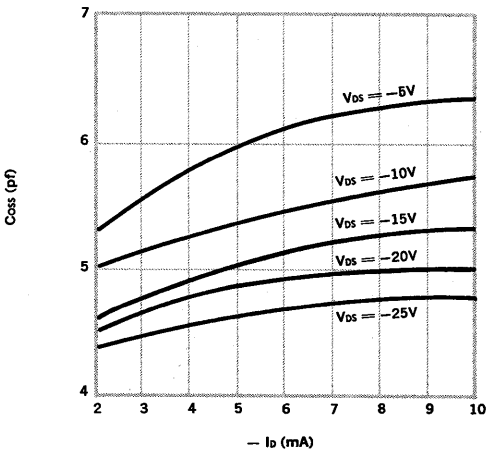
DRAIN TO GATE CAPACITANCE VS DRAIN VOLTAGE



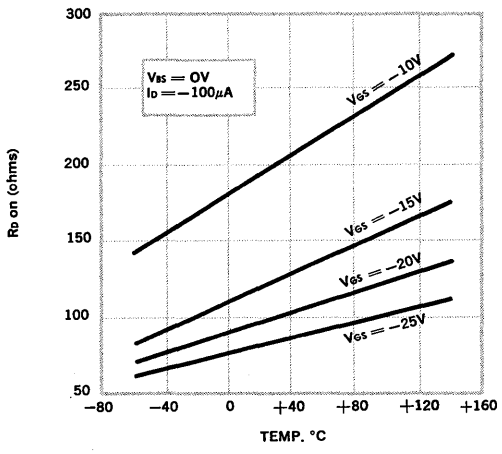
OUTPUT CAPACITANCE VS DRAIN VOLTAGE



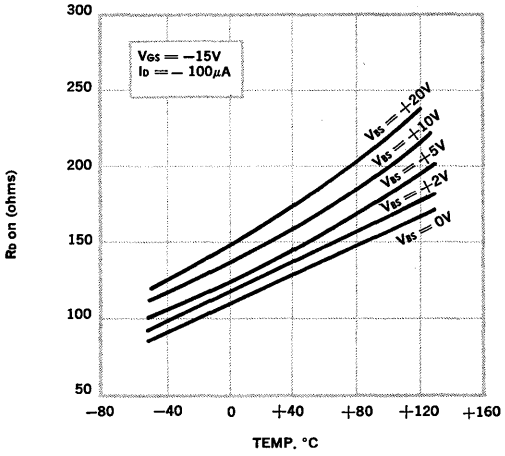
OUTPUT CAPACITANCE VS DRAIN CURRENT



DYNAMIC DRAIN RESISTANCE VS TEMPERATURE

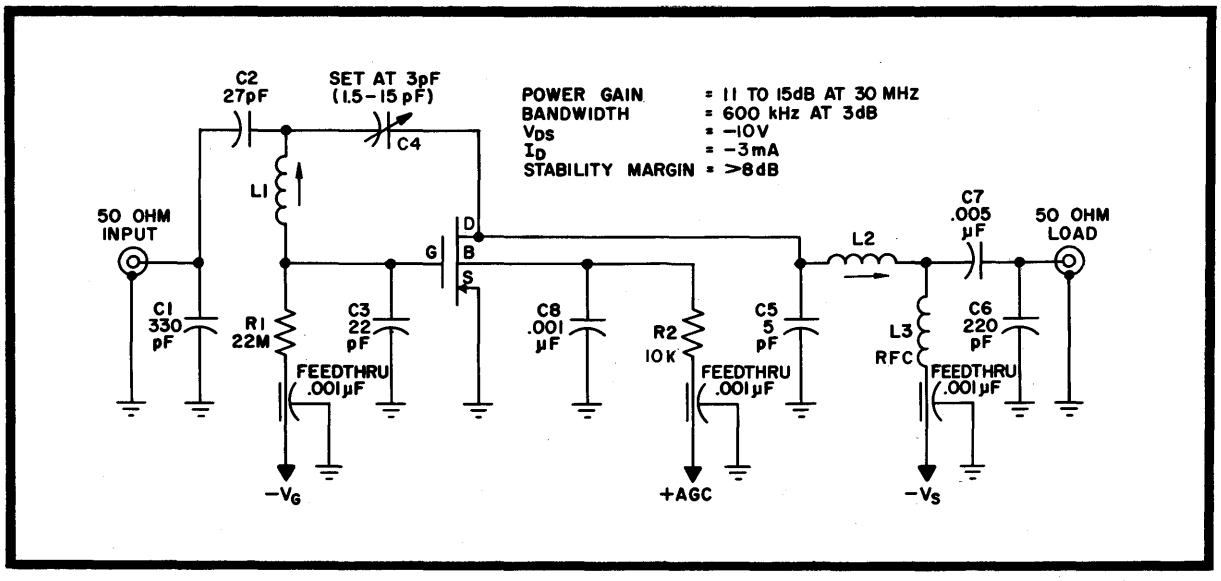


DYNAMIC DRAIN RESISTANCE VS TEMPERATURE



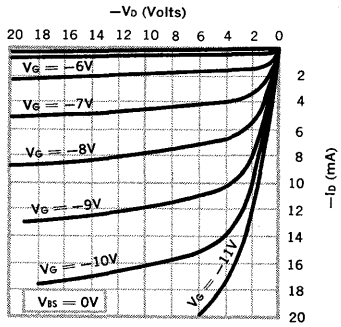
APPLICATIONS

30 MHz Amplifier Utilizing a 2N4353

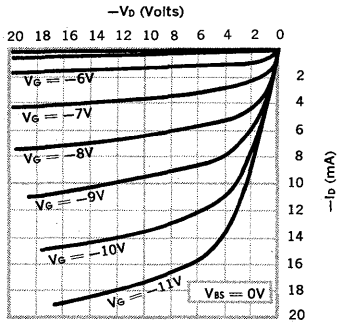


All curves have been plotted from photographs taken with a Tektronix Curve Tracer, Model 575

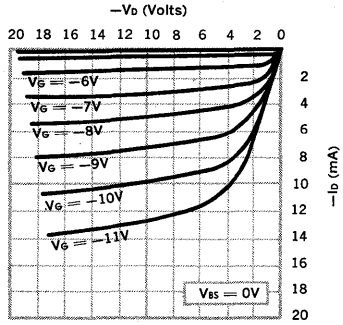
DRAIN CHARACTERISTICS AT −55°C



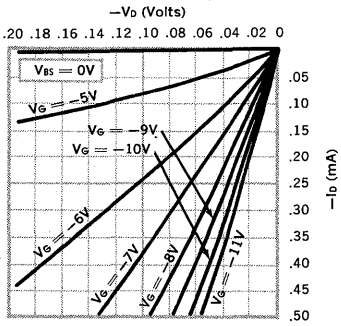
DRAIN CHARACTERISTICS AT 25°C



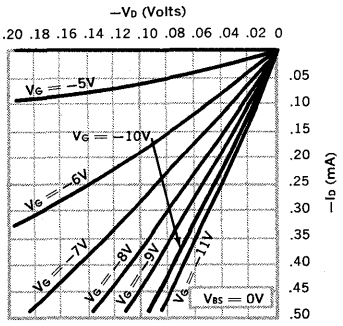
DRAIN CHARACTERISTICS AT 125°C



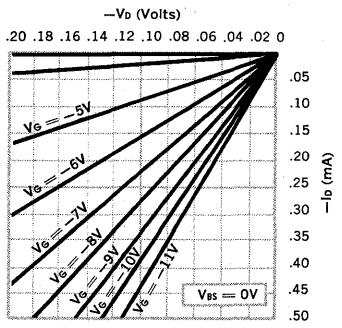
DRAIN CHARACTERISTICS AT −55°C



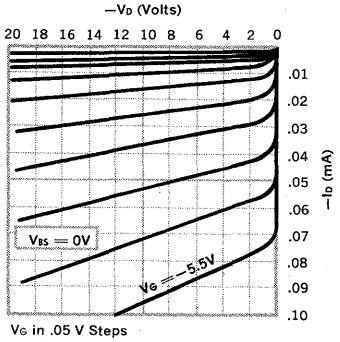
DRAIN CHARACTERISTICS AT 25°C



DRAIN CHARACTERISTICS AT 125°C

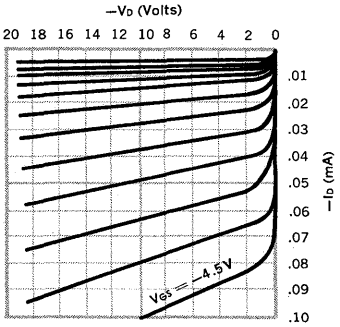


DRAIN CHARACTERISTICS AT −55°C



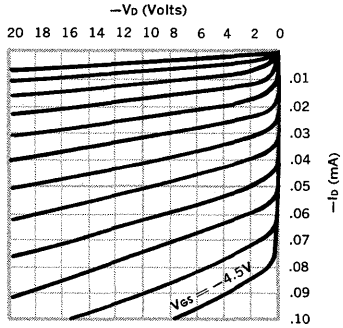
VG in .05 V Steps

DRAIN CHARACTERISTICS AT 25°C



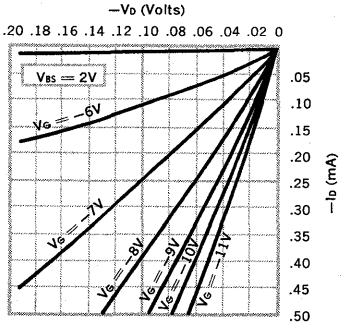
VBS = 0V, .05 V Steps

DRAIN CHARACTERISTICS AT 125°C

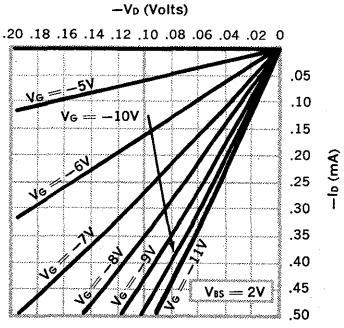


VBS = 0V, .05 V Steps

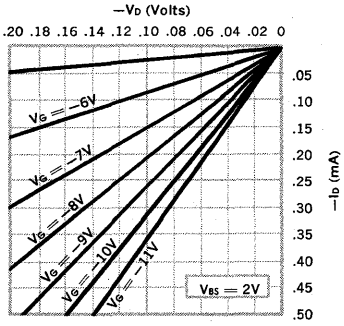
DRAIN CHARACTERISTICS AT −55°C



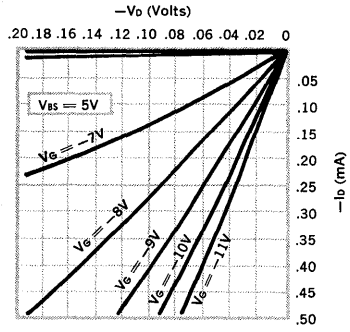
DRAIN CHARACTERISTICS AT 25°C



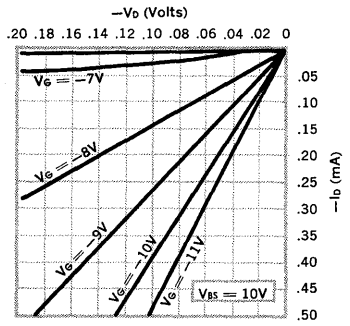
DRAIN CHARACTERISTICS AT 125°C



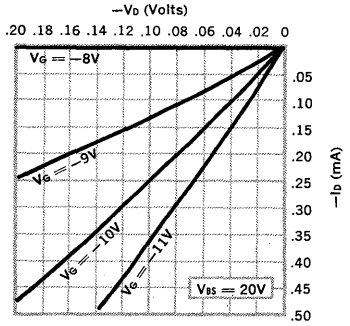
DRAIN CHARACTERISTICS AT −55°C



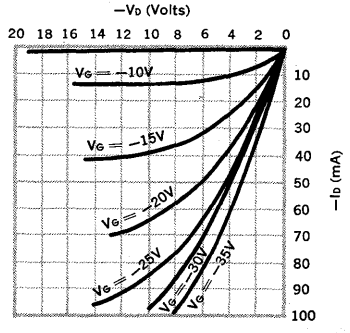
DRAIN CHARACTERISTICS AT −55°C



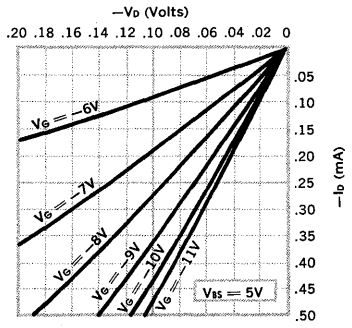
DRAIN CHARACTERISTICS AT −55°C



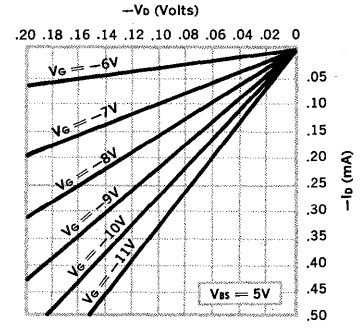
DRAIN CHARACTERISTICS AT 25°C



DRAIN CHARACTERISTICS AT 25°C



DRAIN CHARACTERISTICS AT 125°C



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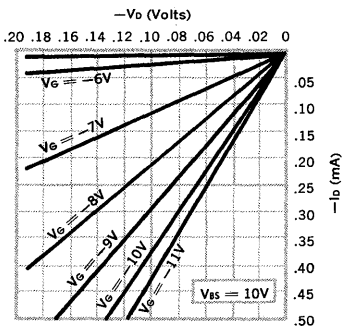

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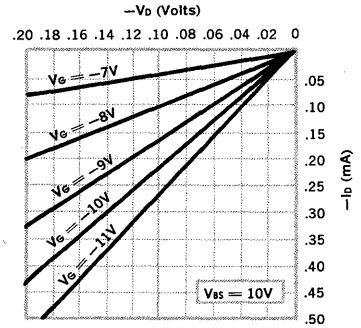
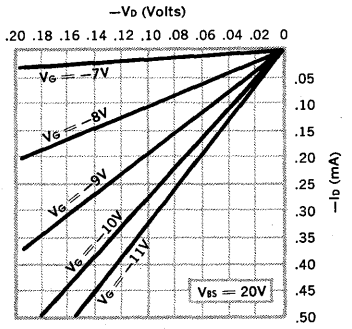
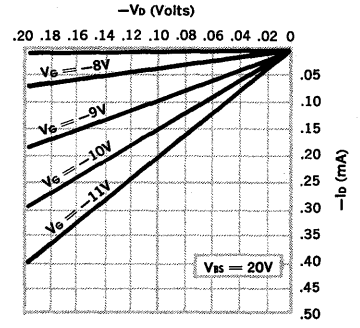


DRAIN CHARACTERISTICS AT 25°C



DRAIN CHARACTERISTICS AT 125°C



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GENERAL INSTRUMENT

POWER MTOS TRANSISTOR

P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
March, 1967

MEM 517

FEATURES:

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS:

($T_A = 25°C$, unless otherwise specified)

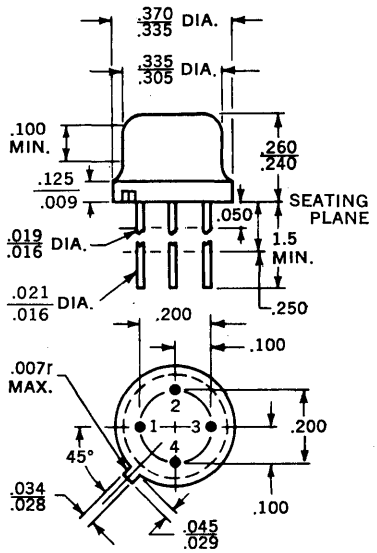
Drain to Source Voltage	−30V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watt

ELECTRICAL CHARACTERISTICS:

($T_A = 25°C$, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	−2.5		−5	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		−0.8	−50	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current		−0.1	−1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	−25	−60		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	−30	−50		Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	$I_{GS} = -10\mu A$, $V_{DS} = 0V$
Y_{fs}	Transadmittance		12000		μmho	1 kHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance		10		pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance		10		pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		0.15		pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	$V_{GS} = -20V$, $I_{DS} = -10mA$
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	$V_{GS} = -10V$, $I_{DS} = -10mA$

TO-33

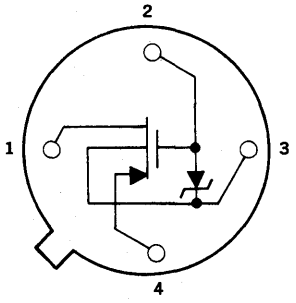


Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

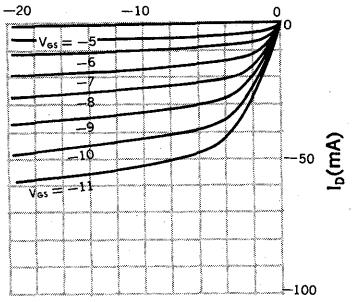
Lead
1. Drain
2. Gate
3. Body (Case)
4. Source



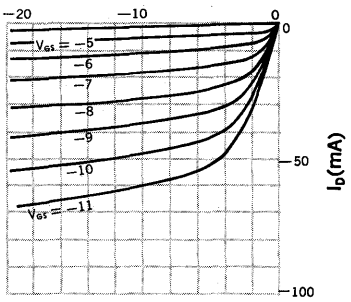
P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR MEM 517

TYPICAL CHARACTERISTIC CURVES
MEM 517

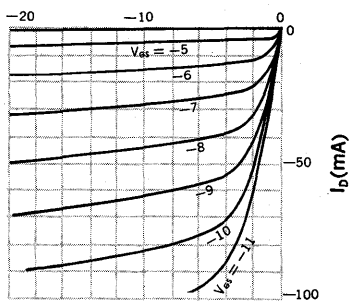
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



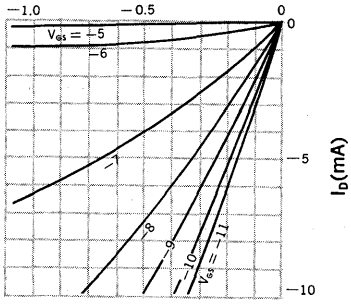
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



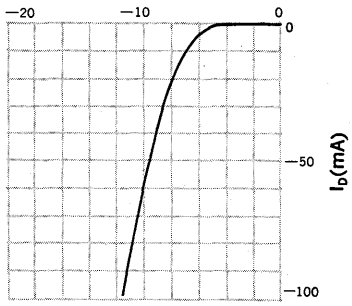
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



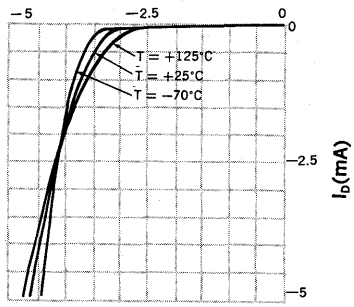
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



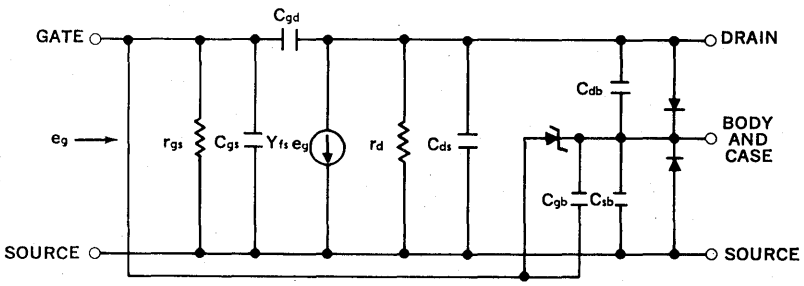
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	10	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	0.15	pF
C_{gb}	Gate to body capacitance	6	pF
C_{db}	Drain to body capacitance	10	pF
C_{sb}	Source to body capacitance	20	pF
Y_{fs}	Forward transadmittance	12000	μmho

HANDLING PRECAUTIONS

MEM 517 insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10^{15} ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

GENERAL INSTRUMENT

POWER MTOS TRANSISTOR

P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
March, 1967

MEM 517A

FEATURES:

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:

(Designed Primarily For Low-Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS:

(T_A = 25°C, unless otherwise specified)

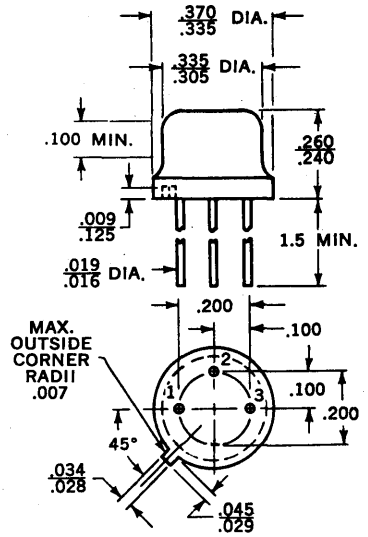
Drain to Source Voltage	−30V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watt

ELECTRICAL CHARACTERISTICS:

(T_A = 25°C, unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate Source Cutoff Voltage	−2.5		−5	Volts	V_{GS} = V_{DS}, I_D = −10μA
I_{DSS}	Drain Leakage Current		−0.8	−50	nA	V_{DS} = −20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		−0.1	−1	nA	V_{GS} = −15V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−25	−60		mA	V_{GS} = V_{DS} = −10V
BV_{DSS}	Drain-Source Breakdown	−30	−50		Volts	I_D = −10μA, V_{GS} = 0V
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	I_{GS} = −10μA, V_{DS} = 0V
Y_{fs}	Transadmittance		12000		μmho	1 kHz, V_{GS} = V_{DS} = −10V
C_{gs}	Gate to Source Capacitance		16		pF	V_{GS} = V_{DS} = −10V
C_{gd}	Gate to Drain Capacitance		10		pF	V_{GS} = V_{DS} = −10V
C_{ds}	Drain to Source Capacitance		10		pF	V_{GS} = V_{DS} = −10V
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	V_{GS} = −20V, I_{DS} = −10mA
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	V_{GS} = −10V, I_{DS} = −10mA

TO-5 PACKAGE



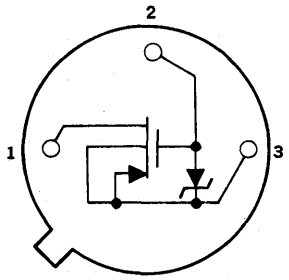
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

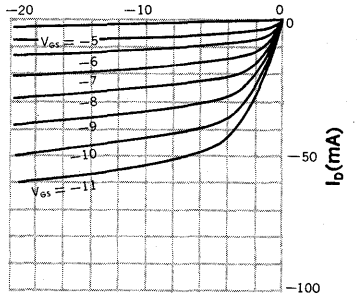
1. Drain
2. Gate
3. Source & Body (Case)



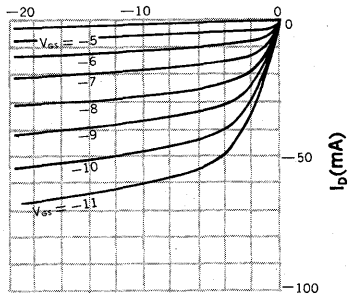
P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR MEM 517A

TYPICAL CHARACTERISTIC CURVES
MEM 517A

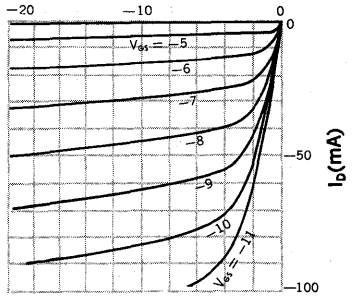
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



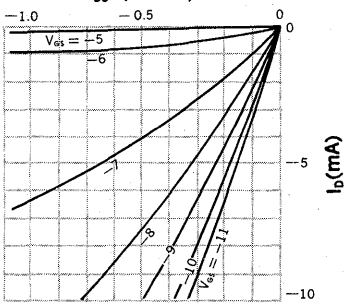
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



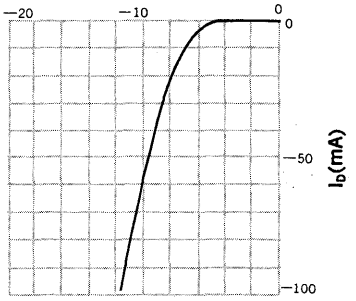
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



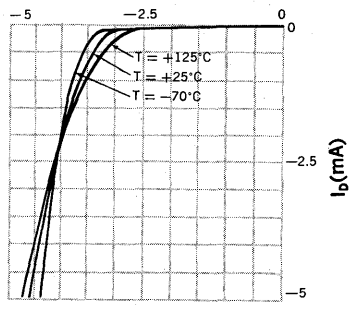
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



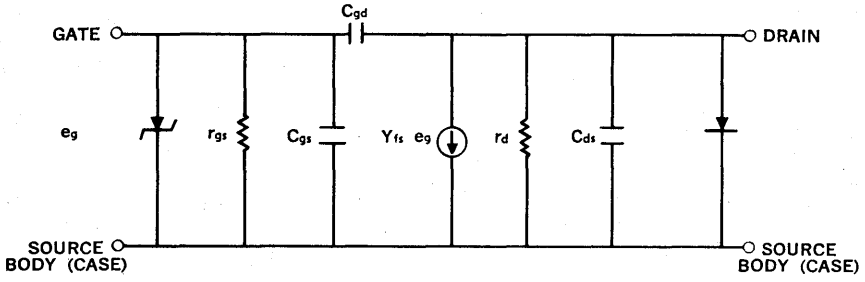
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	16	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	10	pF
Y_{fs}	Forward transadmittance	12000	μmho

HANDLING PRECAUTIONS

MEM 517A insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10^{15} ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

GENERAL INSTRUMENT

MTOS TRANSISTOR

P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
March, 1967

MEM 520

FEATURES:

- 10^{15} ohms input resistance
- Normally off with zero gate voltage
- Square Law linear transfer characteristics

APPLICATIONS:

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- RF and IF amplifiers
- Multiplexers

MAXIMUM RATINGS:

($T_A = 25°C$, unless otherwise specified)

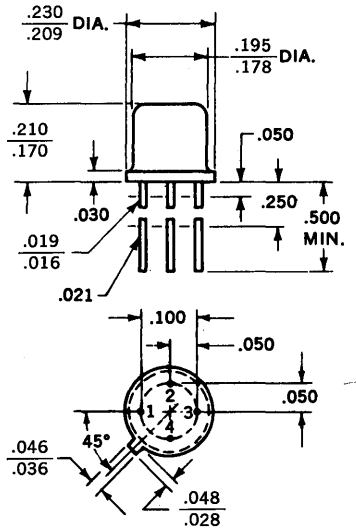
Drain to Source Voltage	—30V
Gate to Source Voltage	—40V
Gate to Drain Voltage	—40V
Drain Current	—50mA
Storage Temperature	—50 to 150°C
Operating Junction Temperature	—50 to 125°C
Total Dissipation at 25°C Case Temperature	650mW
Total Dissipation at 25°C Ambient Temperature	225mW

ELECTRICAL CHARACTERISTICS:

($T_A = 25°C$, unless otherwise specified — body grounded).

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate Source Cutoff Voltage	—3		—6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		—0.5	—10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current		—.03	—3	pA	$V_{GS} = -40V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	— 3			mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	—30			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, $V_{GS} = V_{DS} = -10V$ 10MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			3	pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance			2.5	pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	$V_{GS} = -15V$, $I_{DS} = -1mA$

TO-72 PACKAGE

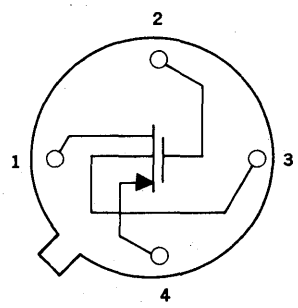


Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

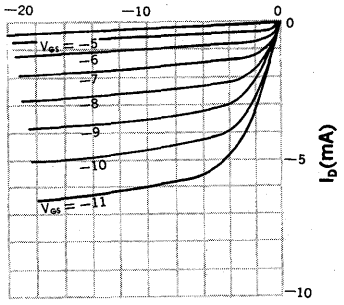
Lead
1. Drain
2. Gate
3. Body (Case)
4. Source



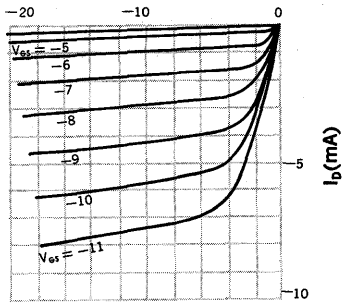
T6025C

TYPICAL CHARACTERISTIC CURVES
MEM 520

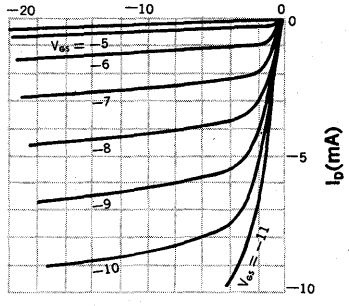
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



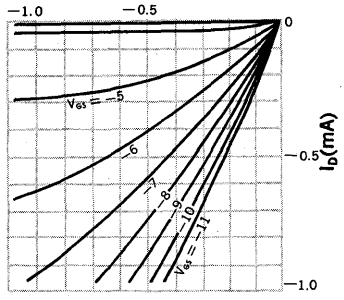
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



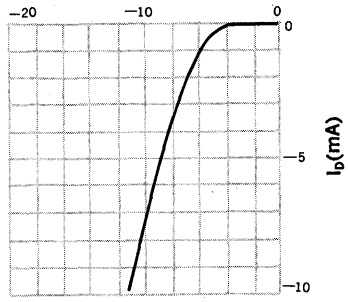
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



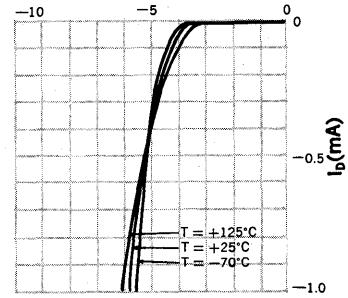
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



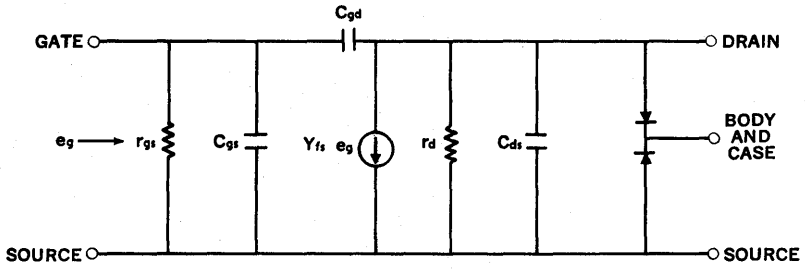
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance	10^{15}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

HANDLING PRECAUTIONS

The MEM 520 insulated gate field effect transistors have very high gate resistance, (10^{15} ohm typical). This resistance, combined with the gate capacitance, requires that every precaution be taken during testing and handling in order to prevent charge build up and possible gate breakdown.

The shorting of the gate lead to the other leads during handling will protect the gate from breakdown.

GENERAL INSTRUMENT

VHF AMPLIFIER DUAL GATE TYPE

N-CHANNEL ENHANCEMENT–DEPLETION MODE SILICON DUAL INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
DECEMBER, 1967

MEM 554C

FEATURES

- 10^{15} ohms input resistance
- Dual Gate Cascode operation
- Low 3_{rd} order distortion
- Reverse AGC capability
- Linear mixing capability
- High gain — low noise through VHF range
- Low feedback capacitance — .025 pf typ.

APPLICATIONS

- TV Tuners (RF & Mixer)
- FM Tuners (RF & Mixer)
- IF Amplifiers
- Synchronous Detectors
- Wideband Amplifiers

MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise specified)

Drain-to-source voltage, V_{DS}	+20V
Gate No. 1-to-source voltage, V_{G1S}	+1 to −10V
Gate No. 2-to-source voltage, V_{G2S}	±10V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−65 to +150°C
Operating Junction Temperature	−65 to +125°C
Total Dissipation at 25°C Case Temperature	300 mw
Total Dissipation at 25°C Ambient Temperature	150 mw
at 100°C Ambient Temperature	150 mw

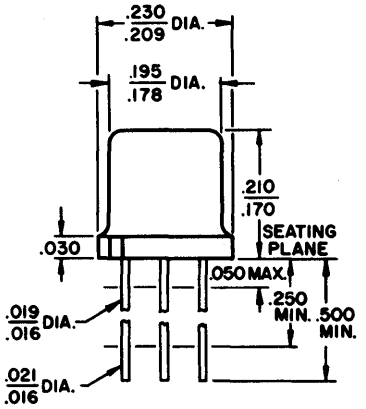
Derate Linearly from 100°C to 125°C at 6 mW/°C

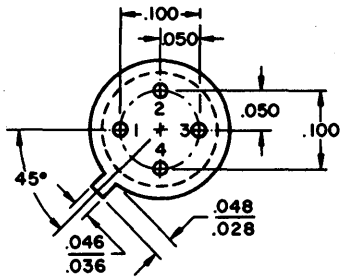
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	$V_{G1} = V_{G2} = -4V$, $I_D = 100uA$
I_{G1SS}	Gate No. 1 Leakage Current	—	—	1.0	nA	$V_{G1S} = -20V$, $V_{G2S} = V_{DS} = 0V$
I_{G2SS}	Gate No. 2 Leakage Current	—	—	1.0	nA	$V_{G2S} = -20V$, $V_{G1S} = V_{DS} = 0V$
$I_{D(off)}$	Drain to Source Leakage Current	—	—	100	uA	$V_{DS} = +20V$, $V_{G1} = V_{G2} = -4.0V$
$V_{G1S(off)}$	Gate No. 1-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G2S} = +4.0V$
$V_{G2S(off)}$	Gate No. 2-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G1S} = 0V$
I_{DSS}	Zero signal Gate voltage drain current	3	—	30	mA	$V_{DS} = +15V$, $V_{G2} = +4.0V$ $V_{G1} = 0V$
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	5.0	7.0	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 1 MHz
C_{oss}	Small-signal, short circuit drain-to-source capacitance	—	2.5	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 1 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	.02	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 1 MHz
G_{fsl}	Forward trans-conductance of gate No. 1	6000	—	—	umhos	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 1 kHz
G_{ps}	Power gain (See fig. 1 for measurements circuits)	15	—	—	db.	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
NF	Noise Figure** (See Fig. 1 for Measurement Circuit)	—	—	5.0	db.	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
E_{int}	Interefering signal level at gate for 1% Cross Modulation Distortion	—	120	—	mV	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ Desired frequency = 200 MHz Undesired frequency = 150 MHz Input unturned

*V_{G1S} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

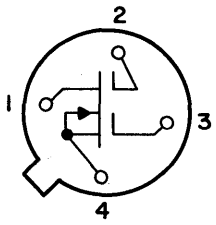
TO-72





Bottom view
NOTE: All dimensions in inches

TERMINAL DIAGRAM



LEAD

1. Drain
2. Gate No. 2
3. Gate No. 1
4. Source, substrate and case

N-CHANNEL ENHANCEMENT–DEPLETION MODE SILICON DUAL INSULATED GATE FIELD EFFECT TRANSISTOR

MEM 554 C

Fig. 1 200 MHz Power Gain and Noise Figure Test Circuit

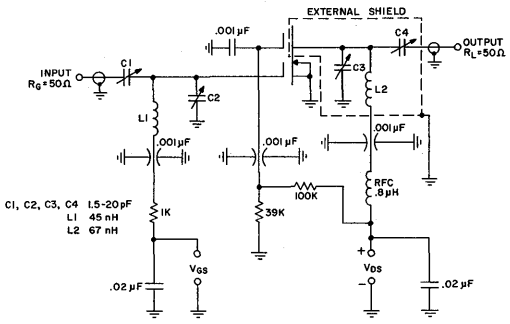


Fig. 2 Power Gain vs. Drain Current

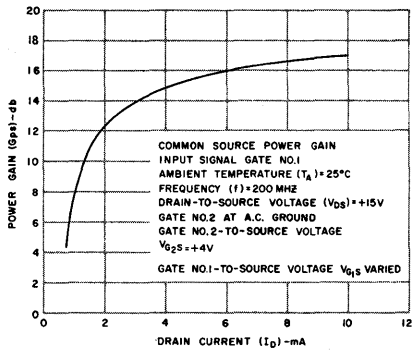


Fig. 3 Noise Figure vs. Drain Current

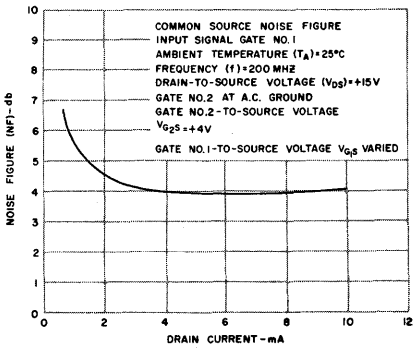


Fig. 4 Gate No. 2 Gain Control Curve

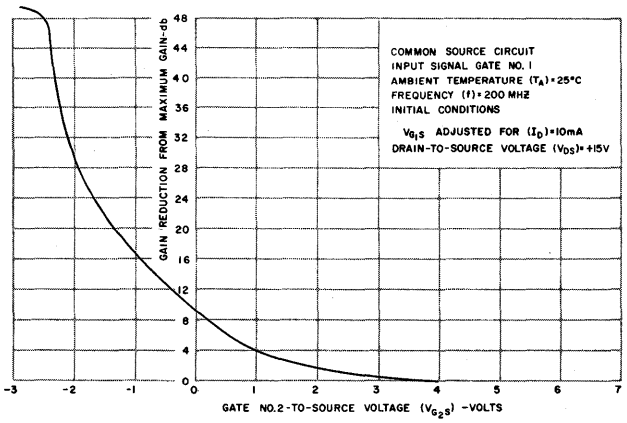


Fig. 5 Noise Figure vs. Gate No. 2-to-source voltage

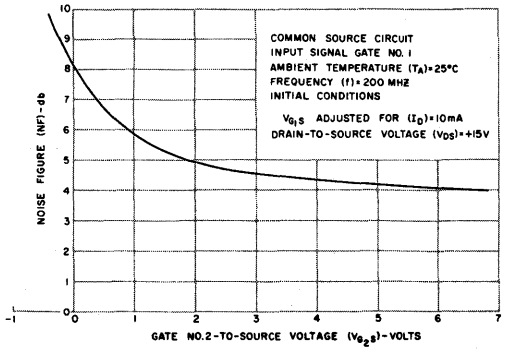
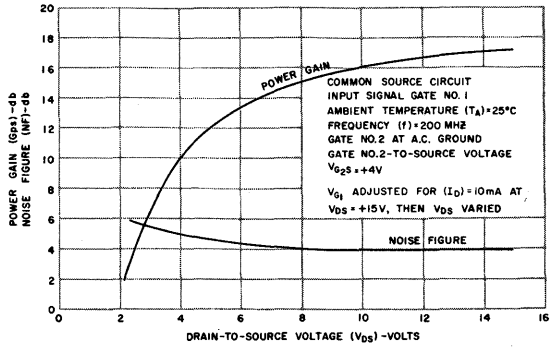


Fig. 6 Power Gain and Noise Figure vs. V_{DS}



HANDLING PRECAUTIONS

The MEM 554 C insulated gate field effect transistors have very high gate resistance, (10^{15} ohm typical). This resistance, combined with the gate capacitance, requires that every precaution be taken during testing and handling in order to prevent charge build up and possible gate breakdown.

The shorting of the gate lead to the other leads during handling will protect the gate from breakdown.

GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

DUAL FULL ADDER

MEM 1000

DUAL FULL ADDER

DESCRIPTION

The MEM 1000 is a dual full adder constructed on a single monolithic chip utilizing MTOS (metal-thick-oxide-silicon) P-channel enhancement mode transistors. It is a rugged low power consumption device designed to perform Boolean arithmetic operations that require sum and carry outputs.

OPERATION

The MEM 1000 is described by the following logic equations:
Each sum output = $ABC + A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C$
Each carry output = $AB + BC + AC$

FEATURES

- Buffered Outputs
- High Input Impedance
- High Noise Immunity
- Large Fanout
- Low Power Consumption
- Monolithic Construction

MAXIMUM RATINGS

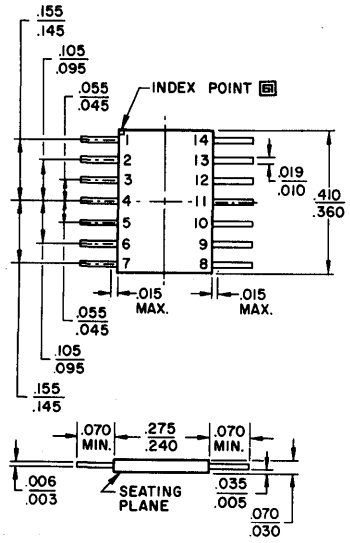
Drain Voltage ($-V_{DD}$)	−30 Volts to + 0.3 Volt
Gate Voltage ($-V_{GG}$)	−30 Volts to + 0.3 Volt
Clock And Data Input Voltages	−30 Volts to + 0.3 Volt
Storage Temperature	−55°C to + 150°C
Operating Temperature Range	−55°C to + 85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)
$V_{DD} = -13$ Volts ± 1 Volt, $V_{GG} = -27$ Volts ± 1 Volt
Load = 10 MΩ and 25 pF., $T_A = -55°C$ to + 85°C

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Pulse Width	500	—	—	nS	
Capacitance	—	—	5.0	pF	
Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Outputs					
Logic "0"	—	<−0.3	−0.5	Volt	$I_{OUT} \leq .15$ mA
Logic "1"	−11	—	$-V_{DD}$	Volts	$R_{LOAD} = 100$ KΩ
Propagation Delay Plus Rise Time or Fall Time	—	350	500	nS	SEE FIG. 2
Impedance to Ground	—	2000	3000	Ohms	Output at Logic "0"
Drive Capability	−10	−11	—	Volts	Output at Logic "1" $R_{LOAD} = 27$K
Capacitance Drive Capability	—	—	25	pF	
Supply Current Drain					
V_{GG}	—	1.4	2.0	mA	All Outputs at Logic "0"
V_{DD}	—	—	0.1	mA	All Outputs at Logic "0"
V_{GG}	—	—	0.1	mA	All Outputs at Logic "1"
V_{DD}	—	1.2	1.8	mA	All Outputs at Logic "1" (no loading)

TO-87



Note: All dimensions in inches.

TERMINALS

P/N	Function
1	Input C_2
2	Input B_2
3	Input A_2
4	$-V_{GG}$
5	Input A_1
6	Input B_1
7	Input C_1
8	Ground
9	Output S_1
10	Output C_1
11	Output C_2
12	Output S_2
13	V_{DD}
14	No Connection

MEM 1000

FIGURE 1 LOGIC BLOCK DIAGRAM

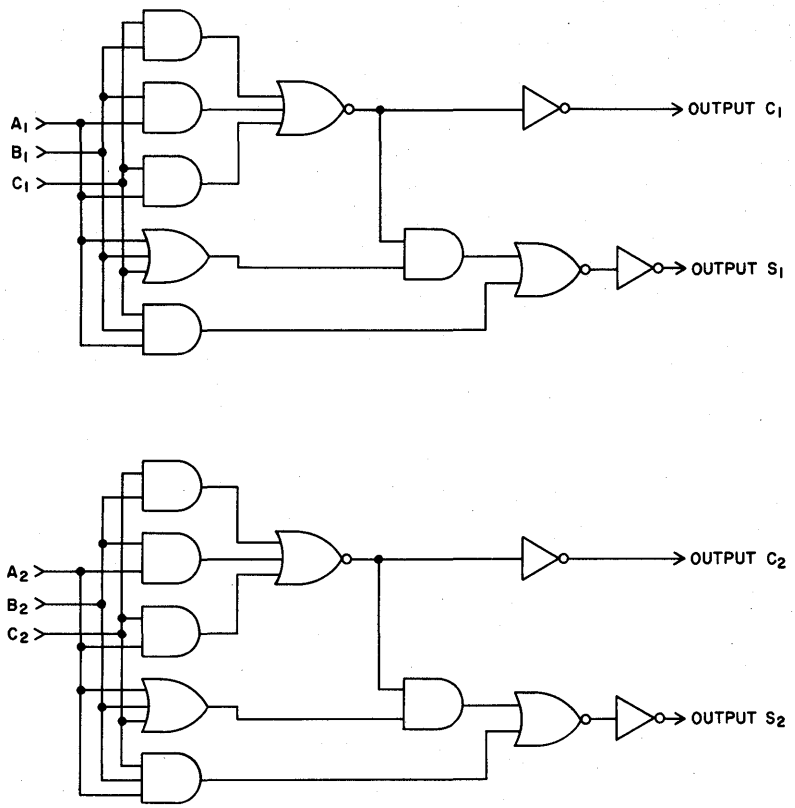
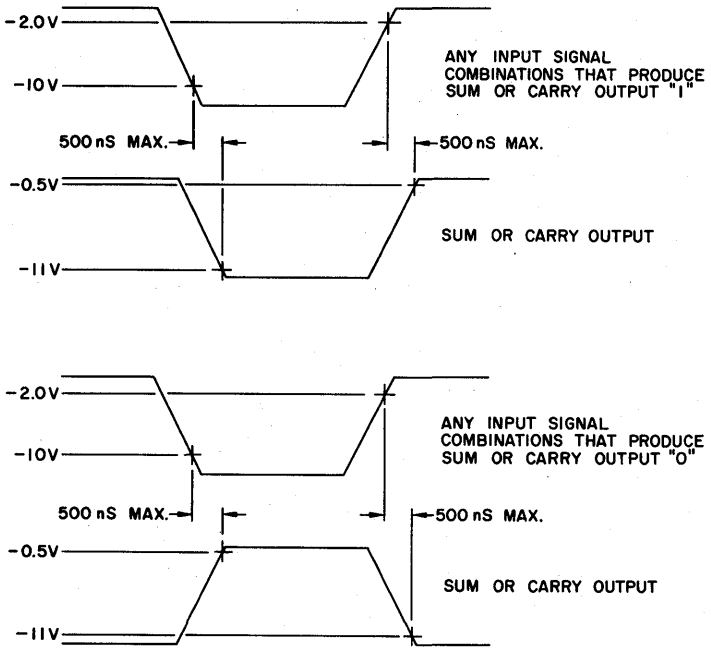


FIGURE 2 TIMING DIAGRAM



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Hicksville, L. I., N.Y. 11802
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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

DUAL 3-INPUT NOR-GATE

MEM 1002

DESCRIPTION

The MEM 1002 is a dual three input NOR gate constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. It is a rugged, low power consumption unit designed for use in timing, decoding and multiplexing applications.

OPERATION

The MEM 1002 is described by the following logic equation:

$$\text{Each Output} = \overline{A + B + C}$$

FEATURES

- Buffered outputs
- High input impedance
- High noise immunity
- Large fanout
- Low power consumption
- Monolithic construction

MAXIMUM RATINGS

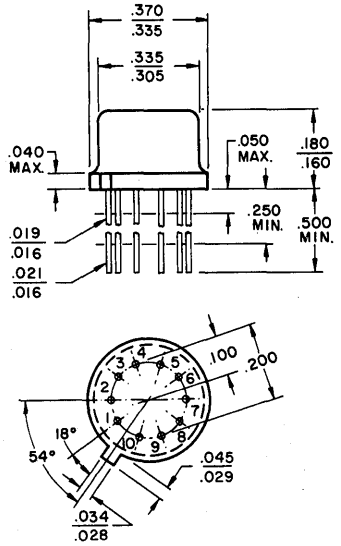
Drain Voltage (V_{DD})	−30 V to +.3 V
Logic Input Voltage	−30 V to +.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

$V_{DD} = -27$ Volts ±1 Volt, $R_L = 10M\Omega$, $C_L = 25pF$, $T_A = -55°C$ to $+85°C$ (unless otherwise specified)

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Pulse Width	500	—	—	nS	
Capacitance	—	—	5.0	pF	
Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Outputs					
Logic "0"	—	<−0.3	−0.5	Volt	
Logic "1"	−11	>−12	−22	Volts	
Propagation Delay Plus Rise Time or Fall Time	—	200	330	nS	SEE FIG. 1
Impedance to Ground	—	2500	4000	Ohms	$V_{in} = -10$ Volts $I_{out} = 1.0$ mA
Drive Capability	−10	>−11	—	Volts	$V_{in} = 0$ Volts $R_L = 27$ KΩ
Capacitance Drive Capability	—	—	25	pF	
Supply Current Drain per Gate	—	0.7	1.3	mA	$V_{in} = -10$ Volts No Load

LOW PROFILE 10 LEAD TO-74



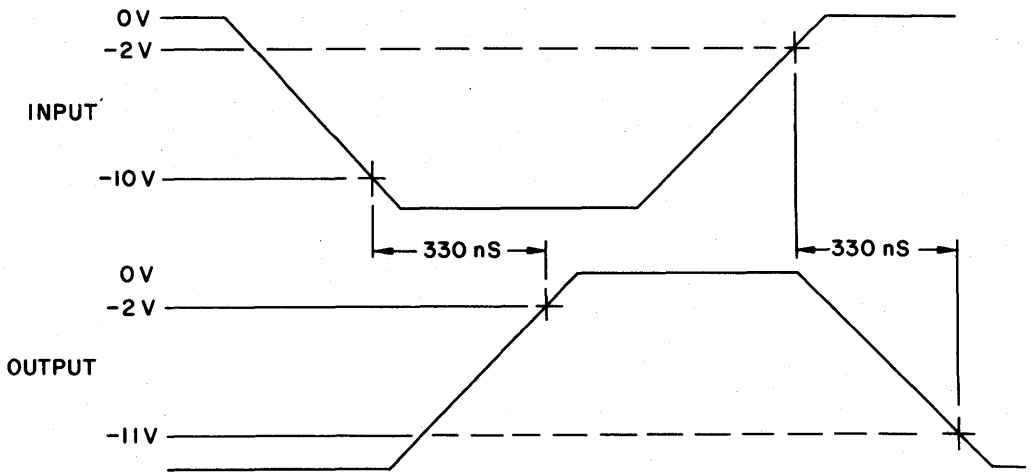
Bottom view
NOTE: All dimensions in inches

TERMINALS

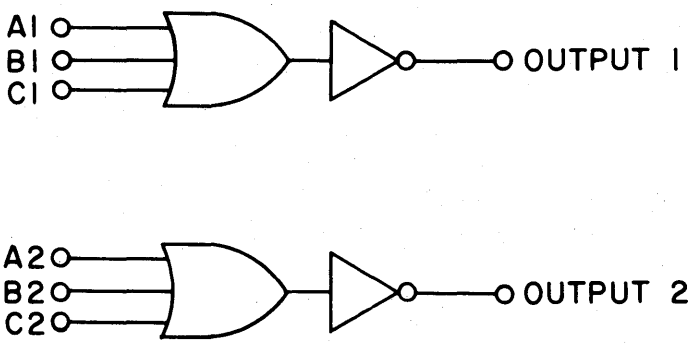
P/N	Function
1	Input A1
2	Input B1
3	Input C1
4	Output 1
5	Ground
6	Input A2
7	Input B2
8	Input C2
9	Output 2
10	$-V_{DD}$

DUAL 3-INPUT NOR-GATE MEM 1002

FIGURE 1



LOGIC DIAGRAM



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

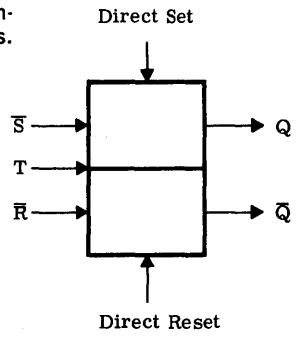
MEM 1005

R̄-S̄-T FLIP-FLOP

DESCRIPTION

The MEM 1005 R̄-S̄-T Flip-Flop is constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. The flip-flop outputs trigger on the negative going edge of the clock. The set and reset inputs are complementary inputs. The unit also has direct set and reset inputs.

LOGIC DIAGRAM



MAXIMUM RATINGS

Clock and Input Voltage ..... −30V to +.3V
Drain Voltage ($-V_{dd}$) ..... −30V to +.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

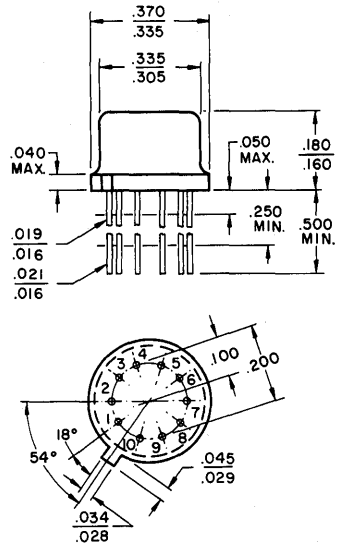
STANDARD CONDITIONS (unless otherwise specified):
$V_{dd} = -27$ Volts ±1 Volt, Load = 10MΩ and 25pF.
$T_A = -55°C$ to +85°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs & Clock					
Logic "0"	0	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Frequency	dc	—	500	kHz	
Pulse Width (ϕ_{pw})	400	—	—	nsec.	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	20.0	μsec.	
Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Capacitance	—	—	5.0	pF	
Outputs					
Logic "0"	—	−0.5	−1.0	Volt	dc to 500 kHz
Logic "1"	−11	−12	—	Volts	dc to 500 kHz
Propagation Delay and Fall Time (t_{pd1})	—	—	950	nsec.	SEE FIG. 1
Propagation Delay and Rise Time (t_{pd2})	—	—	500	nsec.	SEE FIG. 1
Capacitance Drive Capability	—	—	25	pF	
Impedance to Ground (Output a Logic "0")	—	—	2000	Ohms	
Drive Capability	−10	−11	—	Volts	$R_L = 27$ K
Supply Current	—	—	2.6	mA	

TRUTH TABLE

DIRECT SET	DIRECT RESET	S̄ĒT	R̄ĒSĒT	Q_N	Q_N+1	COMMENTS
0	0	0	1	0	1	Clocked set, reset. Outputs change state on negative going edge of clock.
0	0	0	1	1	1	
0	0	1	0	0	0	
0	0	1	0	1	0	
1	0	{0, 1, 1}	{1, 0, 1}	{0, 1}	1	Direct Set. Output changes state on negative going edge of Direct Set input.
0	1	{0, 1, 1}	{1, 0, 1}	{0, 1}	0	Direct Reset. Output changes state on negative going edge of Direct Reset input.
{0, 1}	{0, 1}	0	0	{0, 1}	Undefined	Non-allowable input combination on S̄ĒT, R̄ĒSĒT inputs.
1	1	{0, 1}	{0, 1}	{0, 1}	Undefined	Non-allowable input combination on Direct Set, Direct Reset inputs.

LOW PROFILE 10 LEAD TO-74



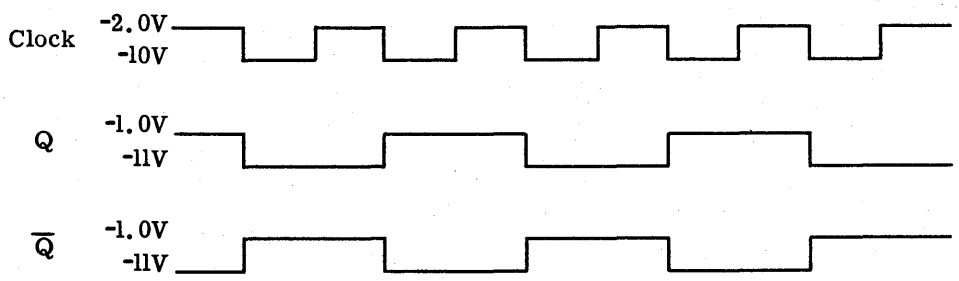
Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	Function
1	Direct Reset Input
2	True Output (Q)
3	R̄ĒSĒT Input
4	Clock Input
5	Ground
6	S̄ĒT Input
7	False Output (Q̄)
8	Direct Set Input
9	No Connection
10	Drain Voltage ($-V_{dd}$)

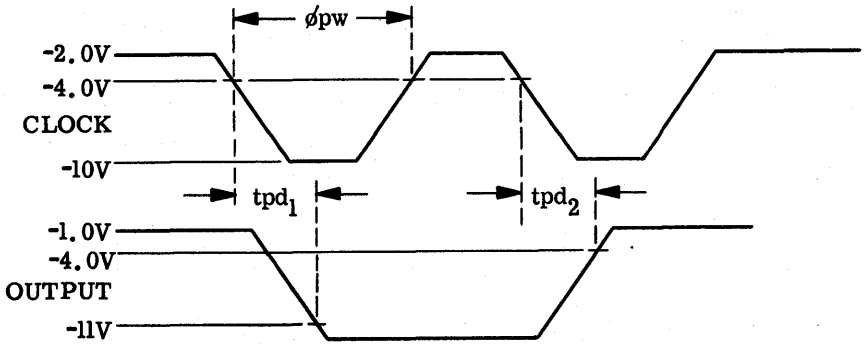
R̄-S̄-T FLIP-FLOP MEM 1005

TYPICAL TIMING DIAGRAM (Binary Mode of Operation)

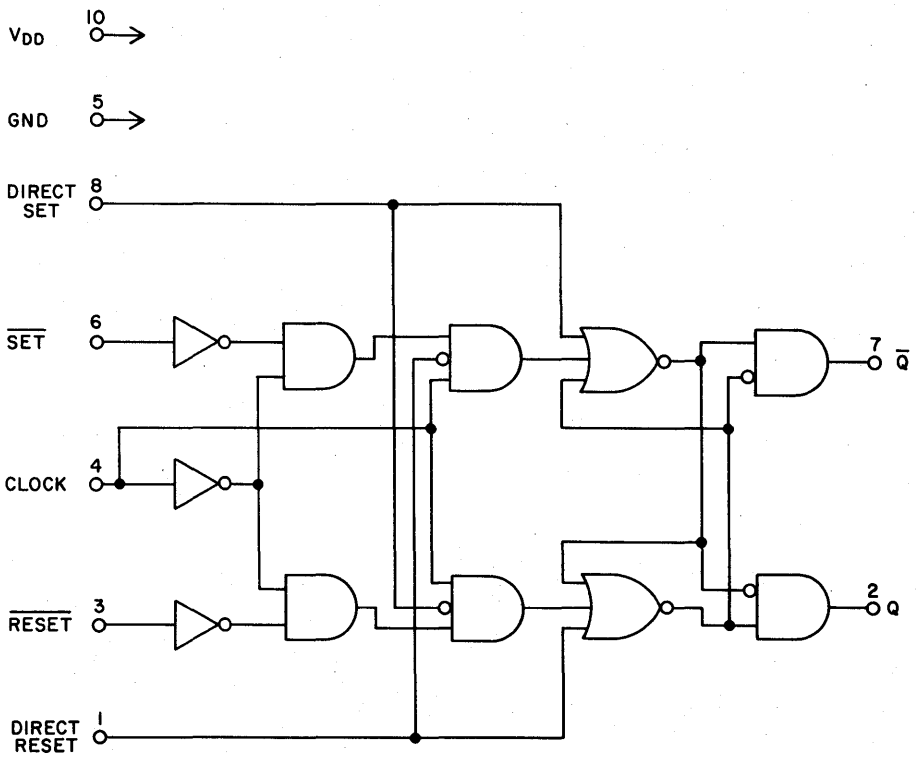


NOTE: Direct set and reset must be tied to a Logical "0".

FIGURE 1



$\overline{R}$-$\overline{S}$-T FLIP FLOP BLOCK DIAGRAM



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

DUAL EXCLUSIVE OR/NOT GATE

MEM 1008

DUAL EXCLUSIVE OR/NOT GATE

DESCRIPTION

The MEM 1008 is a dual exclusive OR/NOT gate constructed on a single monolithic chip with MTOS P-channel enhancement mode transistors. It is a rugged, low power consumption unit designed for use in timing, decoding and comparing applications.

OPERATION

The MEM 1008 is described by the following logic equation:

$$\text{OUTPUT} = A\bar{B} + \bar{A}B$$

MAXIMUM RATINGS

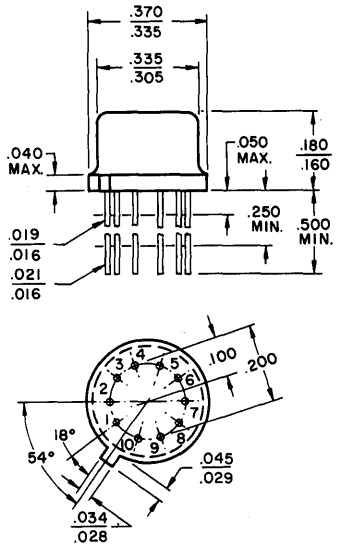
Drain Voltage (V_{dd}) ..... −30 Volts to 0.3V
Logic Input Voltage ..... −30 Volts to 0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified):
Load = 10 MΩ and 25 pF, V_{dd} = −27 Volts ±1 Volt, T_a = −55°C to +85°C

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Pulse Width	500	—	—	nS	
Leakage Current	—	—	5.0	μA	V_{in} = −20V
Capacitance	—	3.0	5.0	pF	V_{in} = 0V
Outputs					
Logic "0"	—	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
Propagation Delay Plus Rise Time (t_{pd1})	—	300	450	nS	SEE FIG. 1
Propagation Delay Plus Fall Time (t_{pd2})	—	300	450	nS	SEE FIG. 1
Impedance to Ground (Output at Logic "0")	—	2000	3000	Ohms	V_{in} A = 0V, V_{in} B = −10V or V_{in} A = −10V, V_{in} B = 0V
Drive Capability (Output at Logic "1")	−10	−11	—	Volts	R_L = 27 KΩ V_{in} A = V_{in} B = 0V or −10V
Capacitance Drive Capability	—	—	25	pF	
Supply Current Drain per Output Function	—	1.3	2.3	mA	

LOW PROFILE 10 LEAD TO-74



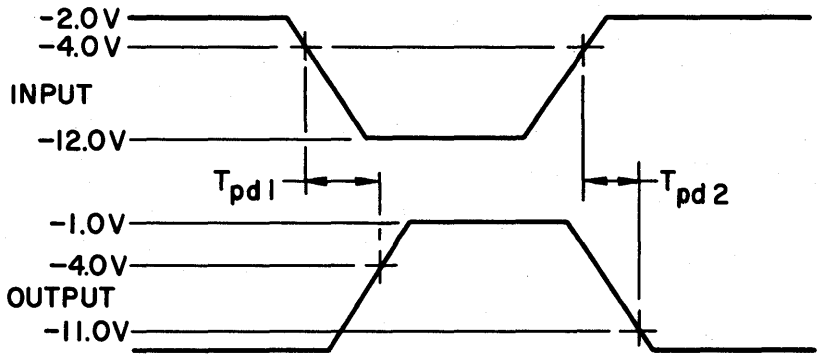
Bottom view
NOTE: All dimensions in inches

TERMINALS

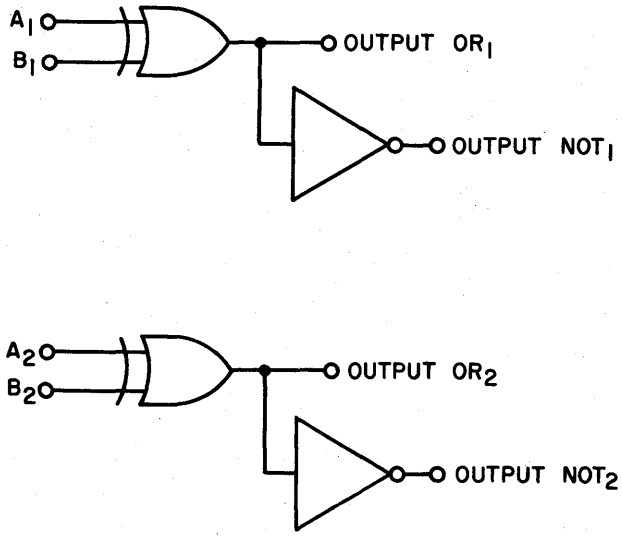
P/N	FUNCTION
1	Input B2
2	Input A2
3	Input A1
4	Input B1
5	Ground
6	Output OR1
7	Output NOT1
8	Output NOT2
9	Output OR2
10	$-V_{dd}$

MEM 1008

FIGURE 1



LOGIC DIAGRAM



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GENERAL INSTRUMENT

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MTOS INTEGRATED CIRCUIT

ADVANCE
JULY, 1967

QUAD 2-INPUT NOR-GATE

MEM 1013

QUAD 2-INPUT NOR-GATE MEM 1013

DESCRIPTION

The MEM 1013 is a QUAD 2-INPUT NOR-GATE constructed on a single monolithic chip utilizing MTOS P-Channel enhancement mode transistors. It is a rugged, low power consumption unit designed for use in timing, decoding and multiplexing circuits.

OPERATION

The MEM 1013 is described by the following equation:

Each Output $= \overline{A + B}$

FEATURES

- Buffered Outputs
- High Input Impedance
- High Noise Immunity
- Large Fan Out
- Low Power Consumption
- Monolithic Construction

MAXIMUM RATINGS

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Logic Input Voltage	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

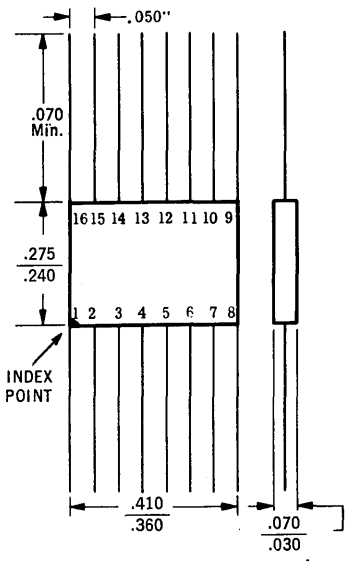
ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)

$V_{GG} = -27$ Volts ±1 Volt, $R_L = 1.0M\Omega$, $C_L = 25pF$, $T_A = -55°C$ to +85°C, $V_{DD} = -13$ Volts ±1 Volt

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Pulse Width	500	—	—	nS	
Capacitance	—	—	5.0	pF	
Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Outputs					
Logic "0"	—	<−0.3	−0.5	Volt	$I_{out} \leq 0.12$ mA
Logic "1"	−11	−12	V_{DD}	Volts	$R_L = 100K$ Ohms
Propagation Delay					
Plus Rise Time or Fall Time ($T_{pdl,2}$)	—	200	330	nS	See Figure 1
Impedance to Ground	—	2500	4000	Ohms	$V_{in} = -10$ Volts $I_{out} = 1.0$ mA
Drive Capability:					
Capacitance	—	—	25	pF	
Logic "1" Level	−10	−11	—	Volts	$V_{in} = 0$ Volts $R_L = 25K$ Ohms
Logic "1" Level	−5.0	—	—	Volts	$V_{in} = 0$ Volts $R_L = 4K$ Ohms
Supply Current Drain (per NOR gate)	—	0.25	0.5	mA	$V_{in} = -10$ Volts No Load

16-LEAD FLAT PACK



Note: All dimensions in inches

TERMINALS

P/N	Function
1	Ground
2	Input B_4
3	Output 4
4	Input A_4
5	V_{GG}
6	Input B_3
7	Output 3
8	Input A_3
9	V_{DD}
10	Input B_2
11	Ground
12	Output 2
13	Input A_2
14	Input B_1
15	Output 1
16	Input A_1

LOGIC DIAGRAM

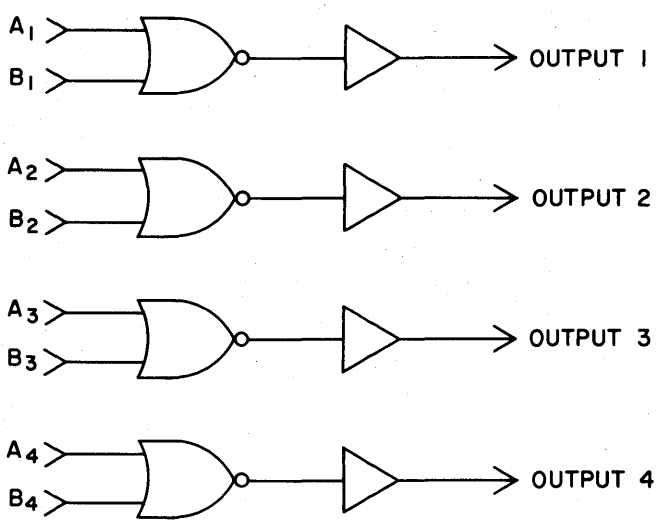
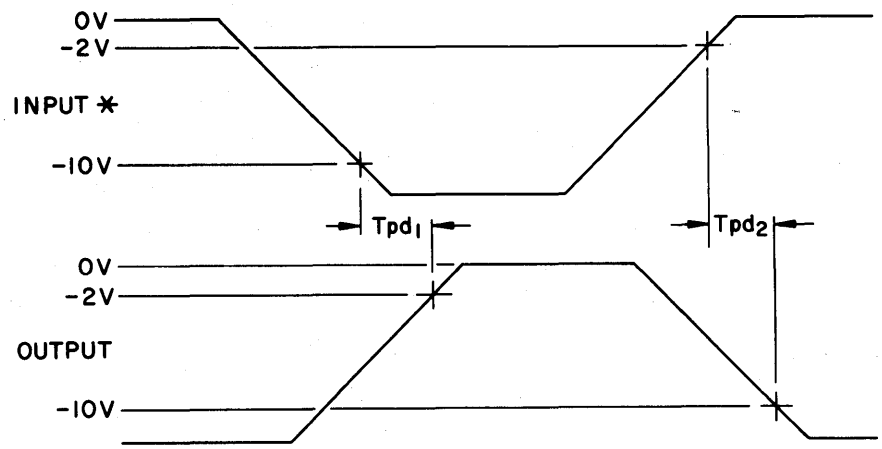


FIGURE 1



* OTHER INPUT = 0 VOLTS

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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
JULY, 1967

QUAD 2-INPUT AND GATE

MEM 1014

QUAD 2-INPUT AND GATE — MEM 1014

DESCRIPTION

The MEM 1014 is a QUAD 2-INPUT AND GATE constructed on a single monolithic chip utilizing MTOS P-Channel enhancement mode transistors. It is a rugged, low power consumption unit designed for use in timing, decoding and multiplexing applications.

OPERATION

The MEM 1014 is described by the following equation:

Each Output (1, 2, 3 & 4) $= A \cdot B$
Output (4) also provides $\overline{A \cdot B}$

FEATURES

- Buffered Outputs
- High Input Impedance
- High Noise Immunity
- Large Fan Out
- Low Power Consumption
- Monolithic Construction

MAXIMUM RATINGS

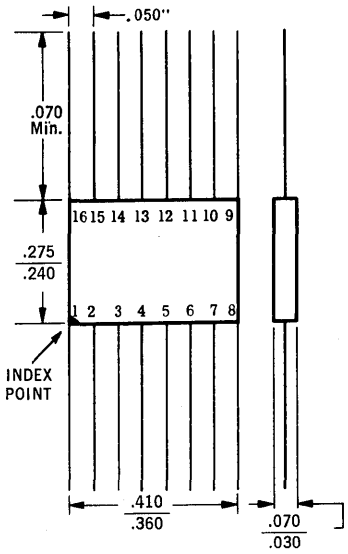
Drain Voltage (V_{DD})	−20 Volts to +0.3V
Gate Voltage (V_{GG})	−30 Volts to +0.3V
Logic Input Voltage	−30 Volts to +0.3V
Storage Temperature	−55°C to +100°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)
$V_{GG} = -27$ Volts ±1 Volt, $R_L = 1.0M\Omega$, $C_L = 25$ pF, $T_A = -55°C$ to +85°C
$V_{DD} = -13.0$ Volts ±1 Volt

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Frequency	dc	—	1.0	MHz	
Pulse Width	500	—	—	nS	
Capacitance	—	—	5.0	pF	
Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Outputs					
Logic "0"	—	< −0.5	−1.0	Volt	$I_{out} \leq 0.15$ mA
Logic "1"	−11	−12	V_{DD}	Volts	$R_L = 100K$
Propagation Delay Plus Fall Time					
$T_{(pd1)}$	—	250	350	nS	See Figure 1
$T_{(pd4)}$	—	250	350	nS	See Figure 1
Propagation Delay Plus Rise Time					
$T_{(pd2)}$	—	300	400	nS	See Figure 1
$T_{(pd3)}$	—	200	275	nS	See Figure 1
Impedance to Ground	—	3000	5500	Ohms	
Drive Capability	−10	−11	—	Volts	$R_L = 25K$ Ohms, $V_{in} = 0$ Volts
Drive Capability	−5.0	—	—	Volts	$R_L = 4K$ Ohms
Capacitance	—	—	25	pF	
Supply Current: (Per "AND" gates 1, 2, and 3)					
V_{DD}	—	—	0.5	mA	
V_{GG}	—	—	0.8	mA	
(Gate 4 total)					
V_{DD}	—	—	0	mA	
V_{GG}	—	—	1.6	mA	

16-LEAD FLAT PACK



Note: All dimensions in inches

TERMINALS

P/N	Function
1	Input B_3
2	Output 3
3	Output 4
4	$\overline{\text{Output 4}}$
5	Input B_4
6	Input A_4
7	V_{GG}
8	Input A_2
9	Input B_2
10	Output 2
11	V_{DD}
12	Output 1
13	Ground
14	Input B_1
15	Input A_1
16	Input A_3

LOGIC DIAGRAM

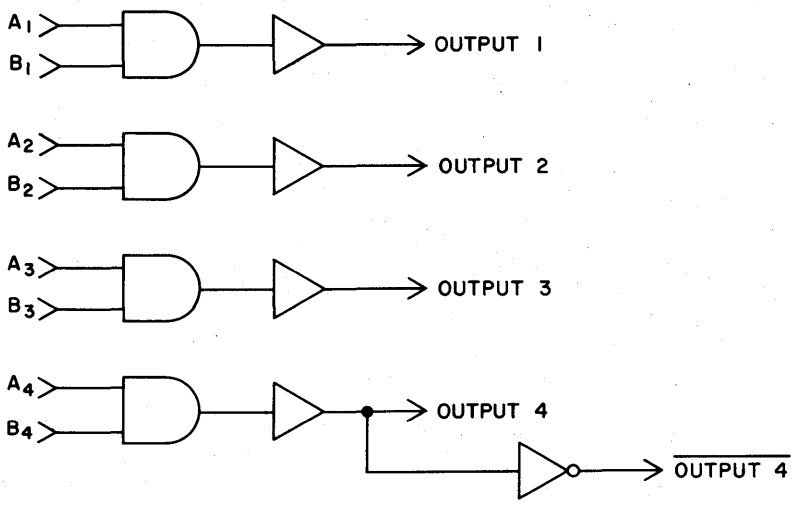
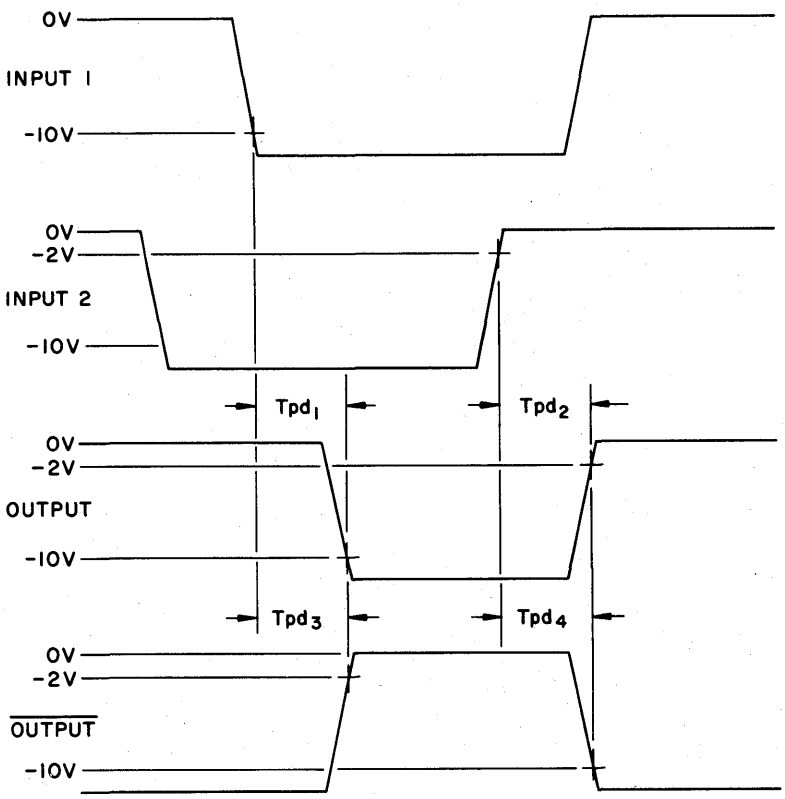


FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT MTOS INTEGRATED CIRCUIT

DUAL J/K FLIP-FLOP

ADVANCE
JULY 1, 1967

MEM 1015

DESCRIPTION

The MEM 1015 dual J-K flip-flop is constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. A chip contains two identical flip-flops. Each has a separate clock input, two J inputs (OR'ed together) and two K inputs (OR'ed together), a direct set and a direct reset. A truth table is provided which describes the output switching conditions for all input combinations.

TRUTH TABLE

Q_n	J_1	J_2	K_1	K_2	S	R	Q_{n+1}	Notes
0 1	0 0	0 0	0 0	0 0	0 0	0 0	0 1	No change of state of outputs.
Ø	{0 1 1 0 1 1}		0	0	0	0	1	J input must be "1" when clock is "1." Outputs change state on trailing edge of clock input (positive going edge).
Ø	0	0	{0 1 1 0 1 1}		0	0	0	K input must be "1" when clock is "1." Outputs change state on trainling edge of clock input (positive going edge).
Q_n	{0 1 1 0 1 1}		{0 1 1 0 1 1}		0	0	$\overline{Q}_n$	Toggle mode. Inputs must be "1" when clock is "1." Outputs change state on trailing edge of clock input (positive going).
Ø	Ø		Ø		0	1	0	Direct reset. Outputs change state on leading edge of reset input (negative going edge).
Ø	Ø		Ø		1	0	1	Direct set. Outputs change state on leading edge of set input (negative going edge).
Ø	Ø		Ø		1	1	X	Non-allowable condition.

Ø = don't care
X = undefined state

MAXIMUM RATINGS

Drain Voltage (V_{dd}) ..... −30V to +0.3V
Gate Voltage (V_{GG}) ..... −30V to +0.3V
Logic Input Voltage ..... −30V to +0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

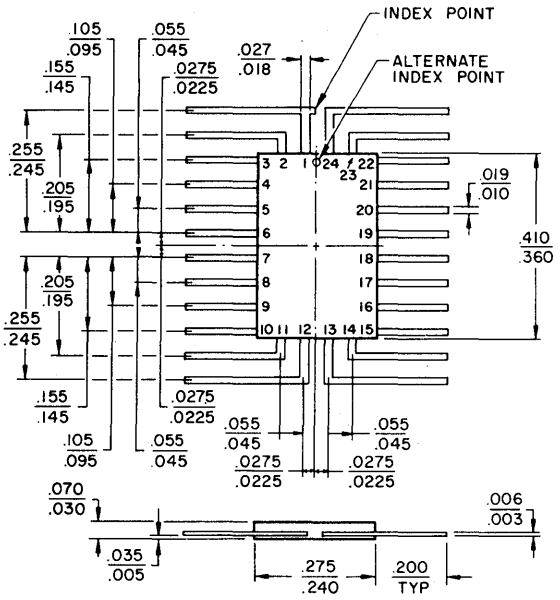
ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)

$V_{GG} = -27$ Volts ± 1 Volt, $R_L = 1.0M\Omega$, $C_L = 25$ pF, $T_A = -55°C$ to $+85°C$,
$V_{DD} = -13$ Volts ± 1 Volt.

Characteristics	Min	Typ	Max	Units	Conditions
Clock Input					
Repetition rate	d.c.	—	1.0	MHz	
Rise & fall time (10% to 90%)	—	—	50.0	μS	
Logic "0" level	—	—	2.0	Volts	
Logic "1" level	−10	—	—	Volts	
Leakage current	—	—	5.0	μA	$V_{CLOCK} = -20$ volts
Control Inputs					
Logic "0" level	—	—	2.0	Volts	
Logic "1" level	−10	—	—	Volts	
Leakage current	—	—	5.0	μA	$V_{in} = -20$ volts
Capacity	—	2.0	3.0	pF	
Outputs					
Propagation delay (Tpd) (50% clock to 50% output)	—	300	350	nS	(See Fig. 1)
Rise time (10% to 90%)	—	120	150	nS	−9.0 volts to −2.2 volts
Fall time (10% to 90%)	—	160	200	nS	−2.2 volts to −9.0 volts
Voltage drive capability	−10	—	—	Volts	$R_L = 25K$ ohms to ground
Capacitance drive capability	—	—	25	pF	
Impedance to ground	—	1000	2500	Ohms	$I_{out} = 1.0$ mA
Supply Current					
I_{GG}	—	3.2	4.75	mA	
I_{DD}	—	2.0	2.8	mA	

24 LEAD FLAT PACK



Note: All dimensions in inches.

TERMINALS

P/N	FUNCTION	P/N	FUNCTION
1	Ground	13	No connection
2	J_{1A}	14	J_{2B}
3	$Clock_A$	15	K_{1B}
4	$Reset_A$	16	K_{2B}
5	Set_A	17	$\overline{Q}_B$
6	V_{GG}	18	Q_B
7	Set_B	19	V_{DD}
8	$Reset_B$	20	Q_A
9	$Clock_B$	21	$\overline{Q}_A$
10	J_{1B}	22	K_{2A}
11	Ground	23	K_{1A}
12	No connection	24	J_{2A}

TYPICAL WAVEFORMS

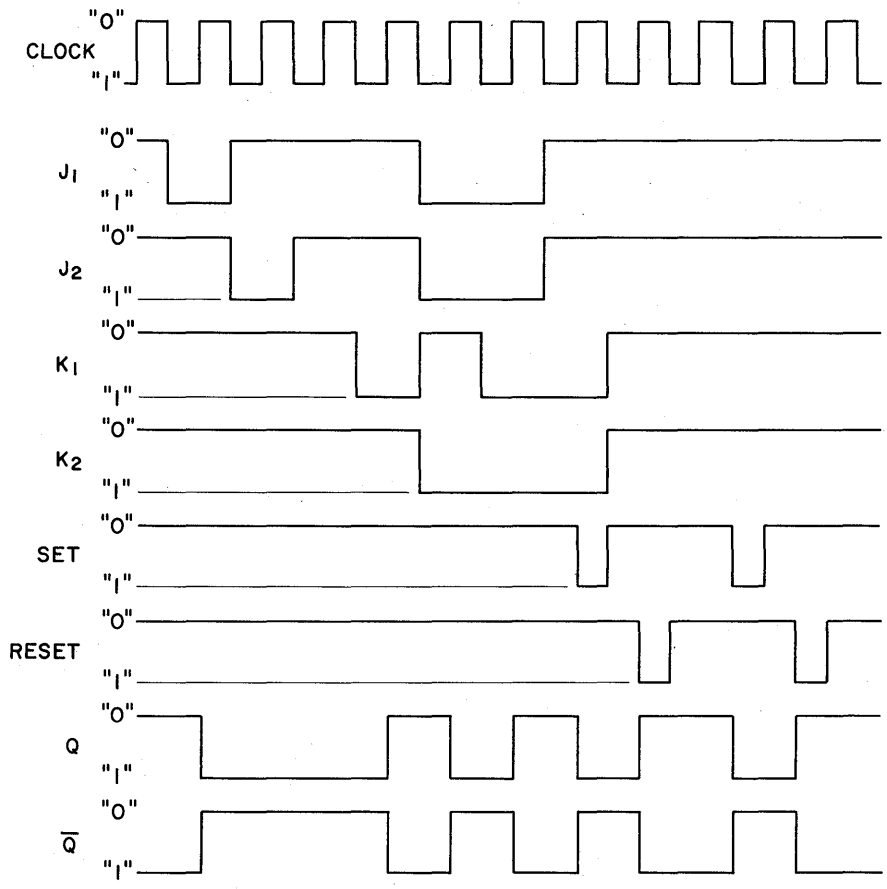
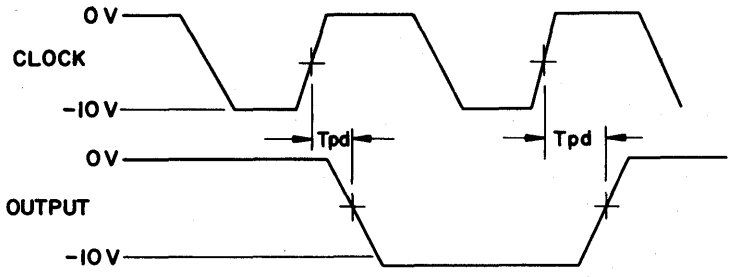


FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
APRIL, 1967

PARITY DETECTOR

MEM 1022

DESCRIPTION

The MEM 1022 Parity Detector checks and generates both odd and even parity of up to nine parallel bits. The circuit is constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-channel enhancement mode transistors. As a parity generator, an input word (up to nine bits in length) is applied to inputs A through K. If words of less than nine bits are used, unused inputs are connected to ground. Output terminal 2 is the formed parity bit when even parity is desired; output terminal 3 is the formed parity bit when odd parity is desired.

When used to check parity, the input word (up to nine bits including the parity bit) is applied to inputs A through K. If words of less than nine bits are used, unused inputs are connected to ground. When checking even parity, output terminal 3 will be a "1" if the check is correct, and a "0" if incorrect. When checking odd parity, output terminal 2 will be a "1" if the check is correct and a "0" if incorrect.
The propagation time for input K is less than the propagation time for the other inputs.

The MEM 1022 circuits may be interconnected to check or generate parity of words that are greater than nine bits in length. This is illustrated in Figure 2.

FEATURES

- Monolithic Construction
- Propagation Time Less Than 750 nS
- Zener Network Protection On All Inputs
- High Noise Immunity (1 Volt Minimum)
- Complementary Outputs
- Low Power Consumption

MAXIMUM RATINGS

Logic Input Voltages ..... −30V
Drain Voltage (V_{DD}) ..... −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

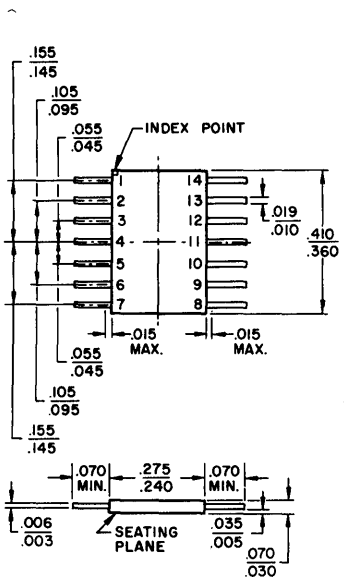
NOTE: A voltage which is more positive than 0.3V with respect to the substrate should not be applied to any pin.

ELECTRICAL CHARACTERISTICS

V_{DD} (Supply Voltage) = −27V ± 1V, R_L = 10 MΩ
C_L = 10 pF, T_A = −55°C to +85°C (unless otherwise specified)

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs					
Logic "0"	—	0	−2.0	Volt	
Logic "1"	−10	−12	−28	Volt	
Leakage Current	—	—	1.0	μA	V_{in} = −20V
Capacitance	—	3	—	pF	V_{in} = 0V
Outputs					
Logic "0"	—	−0.5	−1.0	Volt	
Logic "1"	−11	−15	—	Volt	
Impedance to Ground (Logic "0")	—	—	3.5	kΩ	
Impedance to V_{DD} (Logic "1")	—	—	3.5	kΩ	
Rise Time (negative transition)	—	—	500	nS	10% to 90%
Fall Time (positive transition)	—	—	300	nS	10% to 90%
Propagation Time					
Inputs A thru H	—	500	750	nS	Measured at 50% Points
Input K	—	300	500	nS	Measured at 50% Points
Supply Current Drain	—	—	3	mA	

TO-87



Note: All dimensions in inches

TERMINALS

P/N	Function
1	Ground
2	Odd Output
3	Even Output
4	K
5	V_{DD}
6	H
7	G
8	F
9	E
10	A
11	B
12	C
13	D
14	No Connection

PARITY DETECTOR MEM 1022

FIGURE 1: PARITY DETECTOR CIRCUIT-LOGIC DIAGRAM

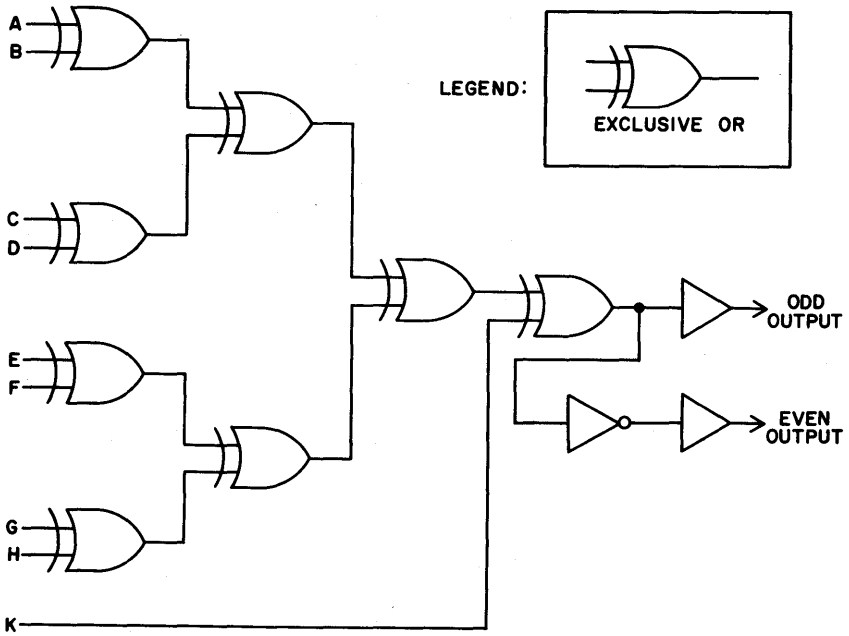
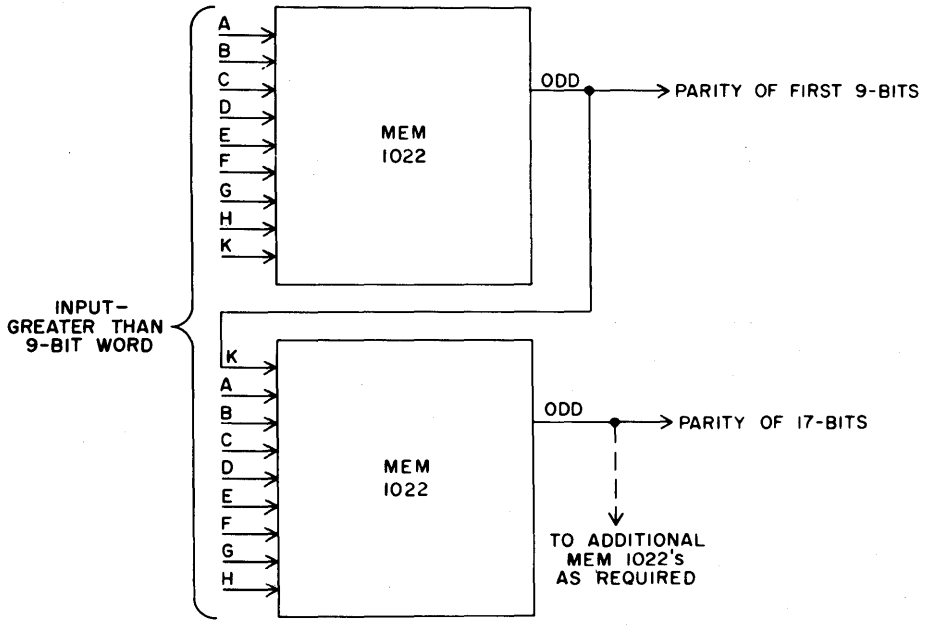


FIGURE 2: INTERCONNECTION DIAGRAM FOR PARITY OF MORE THAN NINE BITS



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GENERAL INSTRUMENT

MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

P CHANNEL—ENHANCEMENT MODE FOUR STAGE BINARY UP-DOWN COUNTER

MEM 1050

DESCRIPTION

The MEM 1050 is a four-stage up-down binary counter constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P Channel enhancement mode transistors. The chip contains 128 MTOS devices. It is a rugged, lower power consumption unit primarily designed for industrial control, servo or digital counters, and timing and decoder applications.

All gating functions are performed with "NAND" logic. Since the trailing edges of the clock input signal (which has a very fast rise time) are used for triggering the flip-flops, race problems are eliminated and no delaying capacitors are required; this feature allows the utilization of a much smaller chip.

FEATURES

- Complementary outputs.
- Complementary clock not needed.
- No miss in count if up and down enable inputs (UO, DO) change state during "0" logic level of clock (FO).
- Loading of one or more outputs does not affect the rest of the outputs or internal counting. Each output has a push-pull driver.
- Trailing-edge triggering. Higher speed, no race problems.
- Serial operation of any number of units to increase digits.
- Sharp breakdown diodes to protect inputs against overvoltage spikes.
- High input impedance.
- Wide frequency range (DC to over 160 kHz).
- High noise immunity.
- High fanout.
- Very low power consumption.
- Monolithic single chip construction.

MAXIMUM RATINGS

Drain Voltage (V_{DD})	−30V to +.3V
Logic Input Voltage	−30V to +.3V
Storage Temperature	−55°C to 150°C
Operating Temperature Range	−55°C to +85°C

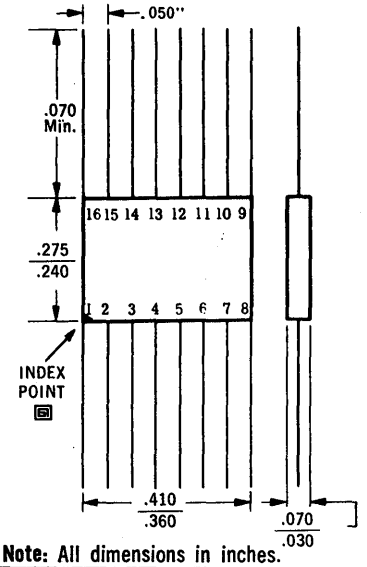
ELECTRICAL CHARACTERISTICS*

V_{DD} = 27 Volts ±1 Volt, Load = 1.0MΩ and 10pF, T_A = −55°C to +85°C

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	d.c.	—	160	kHz	SEE FIG. 1
Clock Pulse Width	4.7	—	—	μsec	
Clock Pulse Rise & Fall Time (10% to 90%)	—	—	10	μsec	
UO and DO Pulse Width	1.0	—	—	μsec	
Clock, UO, DO, Logic Levels					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Fan-In	—	—	1.0		
Input Leakage Current	—	—	1.0	μA	V_{in} = −20 volts
Output Logic Levels					
Logic "0"	—	—	−1.0	Volt	d.c. to 160 kHz
Logic "1"	−11	−12	—	Volts	d.c. to 160 kHz
Propagation Delay Plus Fall Time (t_{pdfn})					
Outputs F1 & $\overline{F1}$ (t_{pdf1})	—	—	2.6	μsec	SEE FIG. 1
Outputs F2 & $\overline{F2}$ (t_{pdf2})	—	—	2.8	μsec	SEE FIG. 1
Outputs F4 & $\overline{F4}$ (t_{pdf4})	—	—	3.0	μsec	SEE FIG. 1
Outputs F8 & $\overline{F8}$ (t_{pdf8})	—	—	3.2	μsec	SEE FIG. 1
Propagation Delay Plus Rise Time (t_{pdrn})					
Outputs F1 & $\overline{F1}$ (t_{pdr1})	—	—	.8	μsec	SEE FIG. 1
Outputs F2 & $\overline{F2}$ (t_{pdr2})	—	—	.9	μsec	SEE FIG. 1
Outputs F4 & $\overline{F4}$ (t_{pdr4})	—	—	1.0	μsec	SEE FIG. 1
Outputs F8 & $\overline{F8}$ (t_{pdr8})	—	—	1.3	μsec	SEE FIG. 1
Propagation Delay Plus Fall Time (t_{pdlU8})	—	—	4.5	μsec	SEE FIG. 1
Propagation Delay Plus Rise Time (t_{pd2U8})	—	—	1.5	μsec	SEE FIG. 1
Propagation Delay Plus Fall Time (t_{pdlD8})	—	—	4.5	μsec	SEE FIG. 1
Propagation Delay Plus Rise Time (t_{pd2D8})	—	—	1.5	μsec	SEE FIG. 1
Fan-Out (F1, $\overline{F1}$, F2, $\overline{F2}$, F4, $\overline{F4}$, F8, $\overline{F8}$)	—	—	3.0		
Fan-Out (U8, D8)	—	—	1.0		
Impedance to Ground	—	—	1500	Ohms	Output a Logic "0"
Short Circuit Current to Ground	0.4	—	—	mA	Output a Logic "1", T_a = 25°C
Input Capacitance	—	2.0	4.0	pF	V_{in} = 0 Volts
Supply Current Drain	—	—	11	mA	

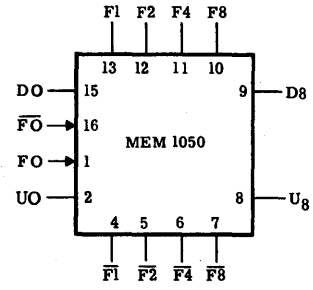
*** Unless otherwise specified**

16-LEAD FLAT PACK



Note: All dimensions in inches.

LOGIC SYMBOL



TERMINALS

P/N	FUNCTION
Inputs*	
1	FO — Clock
2	UO — Up Count Enable, 2^0
15	DO — Down Count Enable, 2^0
16	$\overline{FO}$ — Clock
Outputs	
4	F1 — 2^0 Digit
5	$\overline{F2}$ — 2^1 Digit
6	$\overline{F4}$ — 2^2 Digit
7	$\overline{F8}$ — 2^3 Digit
8	U8 — Up Count Enable, 2^3
9	D8 — Down Count Enable, 2^3
10	F8 — 2^3 Digit
11	F4 — 2^2 Digit
12	F2 — 2^1 Digit
13	F1 — 2^0 Digit
Supply	
3	GND — Ground
14	V_{DD} — Drain Voltage

*No input must be left floating during operation.

OPERATION

To count up, set DO = "0", UO = "1", FO = $\overline{FO}$ = clock
To count down, set DO = "1", UO = "0", FO = $\overline{FO}$ = clock
To stop count, set DO = "0", UO = "0", or stop clock

To count by more than 16, connect two or more units as follows:

UNIT (n)		UNIT (n+1)
F8	→	FO
$\overline{F8}$	→	$\overline{FO}$
U8	→	UO
D8	→	DO

LOGIC DIAGRAM

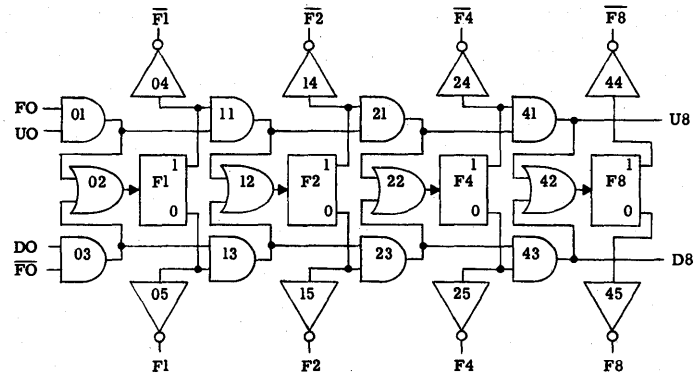
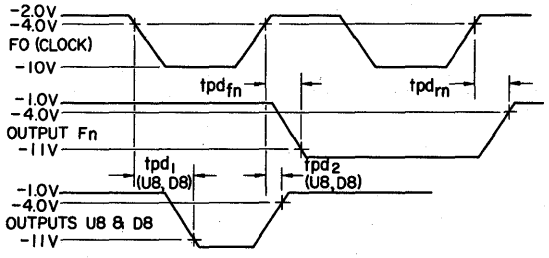
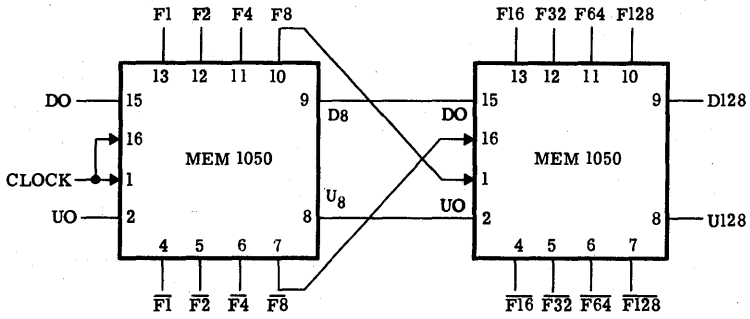


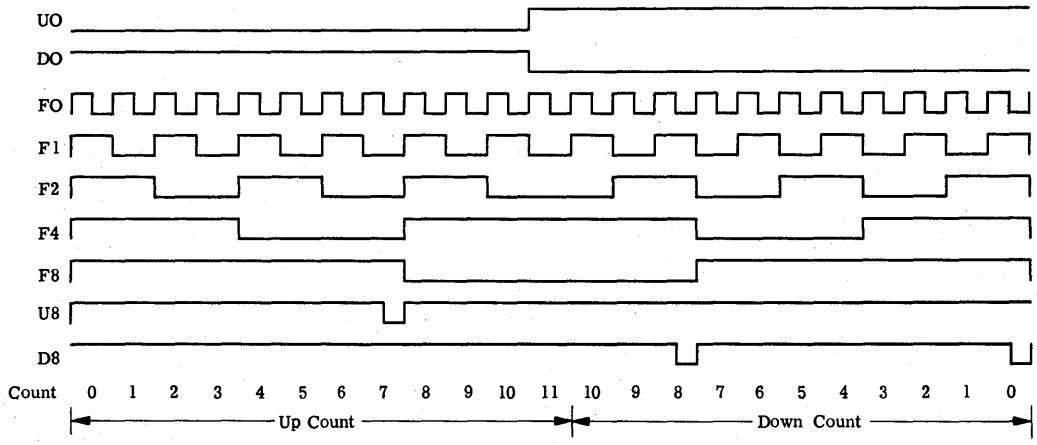
FIGURE 1



0-255 COUNT USING TWO UNITS SERIALLY CONNECTED



WAVEFORMS



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
JUNE, 1967

4 CHANNEL DIGITAL-TO-ANALOG CONVERTER ELEMENT

MEM 1051

DESCRIPTION

The MEM 1051 is a Four Channel Digital-to-Analog Converter Element, constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. Each channel contains two flip-flops connected in a master-slave configuration, and an output switch.

In operation, a logic "1" on the "Load" input will cause the data on the four data input lines (D1-D4) to be entered into the four "master" flip-flops. A logic "1" on the "Enable" input will cause the data in the "master" flip-flops to be transferred into the "slave" flip-flops. A logic "1" in any slave flip-flop will turn "on" the corresponding output switch. The output switches are designed for current summing in digital-to-analog conversion.

FEATURES

- High speed and wide frequency range (d.c. to 500 kHz)
- Low power consumption
- Low switch "on" resistance
- Equal "on" switch resistance for all switches
- Low charge transfer to output
- Low output leakage current
- Data storage capability

MAXIMUM RATINGS

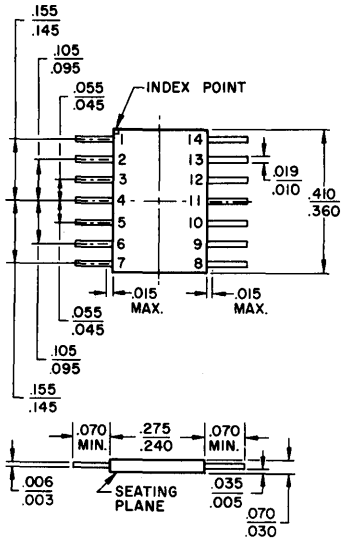
Drain Voltage (V_{DD})	−30V to + 0.3V
Logic Input Voltage	−30V to + 0.3V
Storage Temperature	−55°C to + 150°C
Operating Temperature	−55°C to + 85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
$V_{DD} = -13$ Volts ± 1.5 Volts, $V_{GG} = -25$ Volts ± 3 Volts, $T_A = -55°C$ to + 85°C

CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
Data Input Pulse Repetition Rate	d.c.	—	500	kHz	
"Enable" and "Load" Input Pulse Widths	1	—	—	μS	
Input Logic Levels					
Logic "0"	—	—	−2	Volts	
Logic "1"	−10	—	—	Volts	
Charge Transfer (Per Switch)	—	—	10	pC	
Input Leakage	—	—	1	μA	$V_{IN} = -15$ Volts
"On" Resistance (R_1-R_4)	—	350	400	OHMS	Pin 4 @ Ground
"On" Resistance Temperature Coefficient	—	—	.5%/°C		+25°C to +45°C
"On" Resistance Change:					
With V_{DD}	—	10%	25%		V_{DD}: −11.5 Volts to −14.5 Volts
With V_{GG}	—	—	2%		V_{GG}: − 22 Volts to −28 Volts
Output Leakage	—	—	1	nA	R_1 — R_4 Off, Pin 4 @ −1 Volt, R_1 — R_4 @ −4 Volts
Power Dissipation	—	25	35	mW	

TO-87

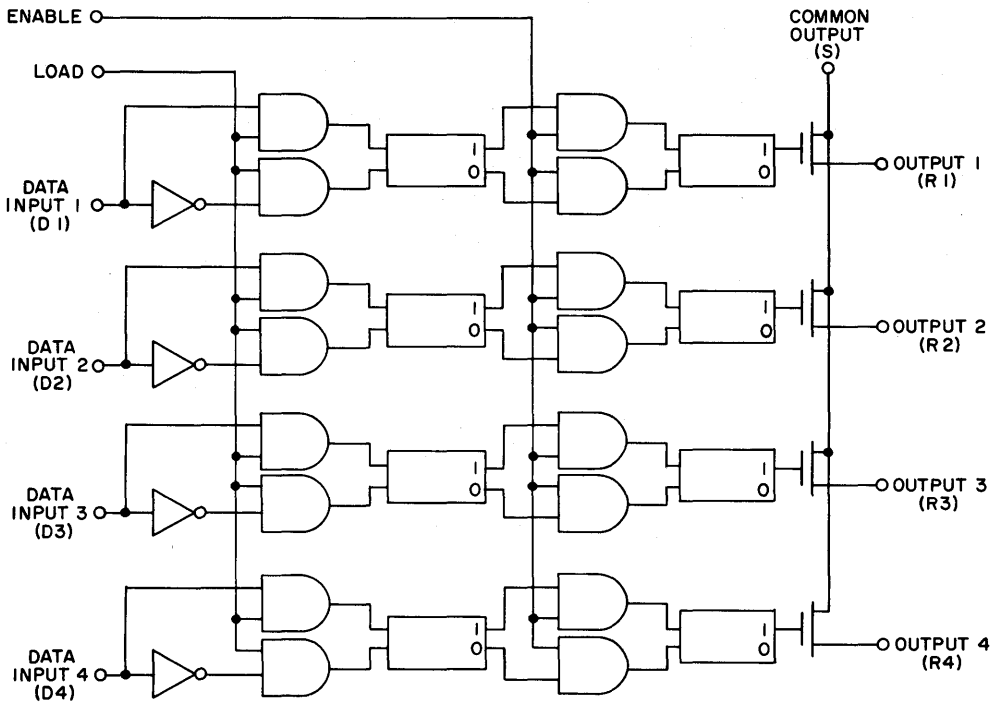


Note: All dimensions in inches.

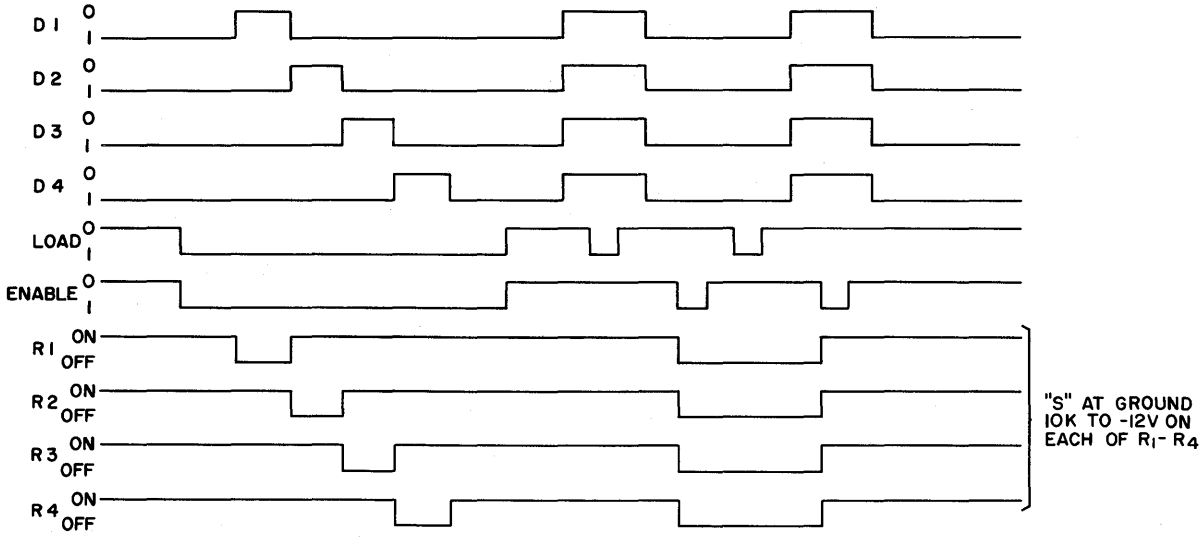
TERMINALS

P/N	Function
1	Ground
2	R_1 (Output 1)
3	R_2 (Output 2)
4	S (Common Output)
5	R_3 (Output 3)
6	R_4 (Output 4)
7	V_{GG}
8	Load (Parallel Data Enter Command)
9	D_4 (Logic Input 4)
10	D_3 (Logic Input 3)
11	V_{DD}
12	D_2 (Logic Input 2)
13	D_1 (Logic Input 1)
14	Enable (Parallel Data Transfer Command)

LOGIC BLOCK DIAGRAM



TYPICAL TIMING DIAGRAM



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
JUNE, 1967

MULTIPLEXER GATE DEVICES

MEM 2002-
MEM 2006

MULTIPLEXER GATE DEVICES

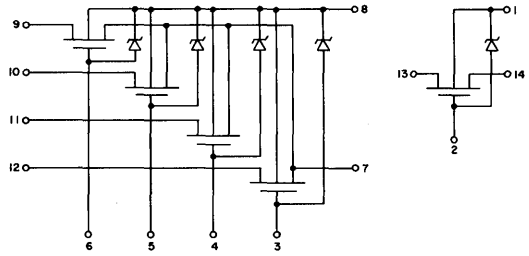
MEM 2002-2006

GENERAL DESCRIPTION

The Multiplexer gates contain silicon P-Channel insulated gate enhancement mode field effect transistors. Several device packages provide an MTOS gate circuit completely isolated from the Multiplex gate network.

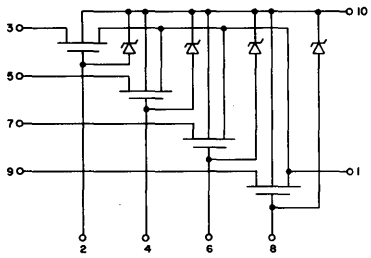
FEATURES

- Isolation of Gate Control Voltage
- Low Drive Power Requirements
- Ratio of "ON" to "OFF" Resistance > 200 db
- Multiplexing in Both Directions



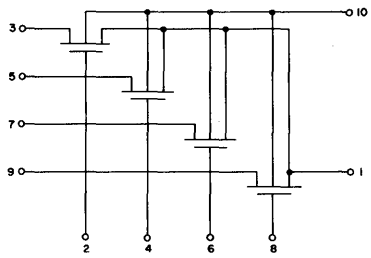
MEM 2002

Package: **TO-87**



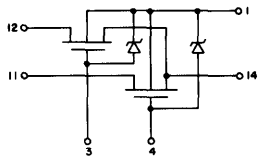
MEM 2003

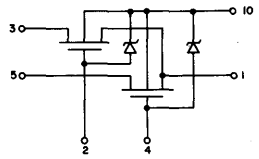
Package: **TO-74**

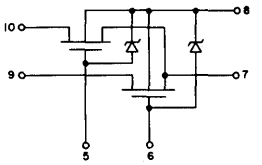


MEM 2004

Package: **TO-74**

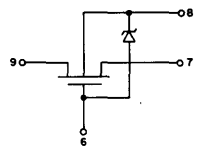






MEM 2005

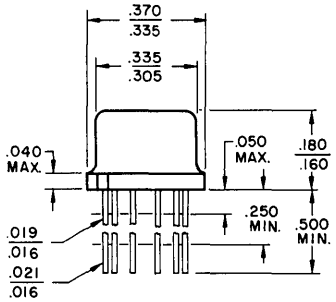
Package: **TO-87**

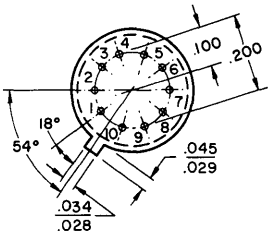


MEM 2006

Package: **TO-74**

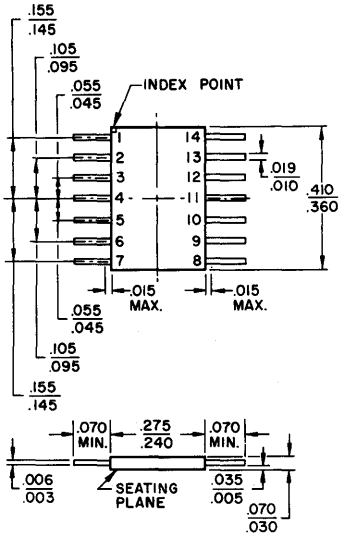
LOW PROFILE 10 LEAD TO-74





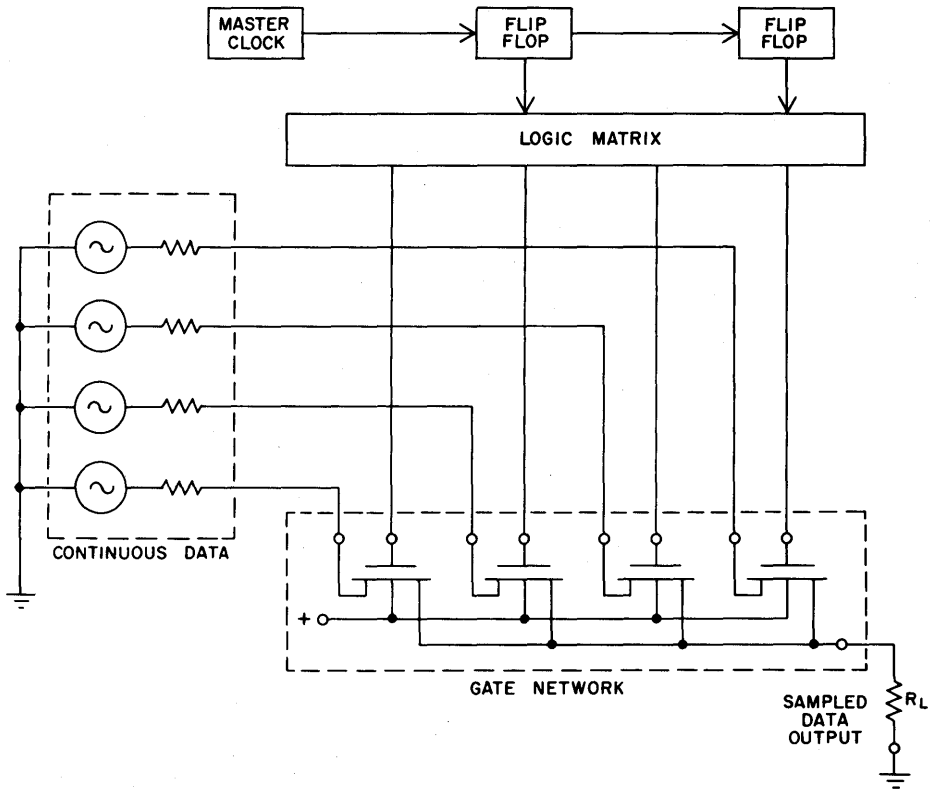
Bottom view
NOTE: All dimensions in inches

TO-87



Note: All dimensions in inches.

FIG. 1: 4 CHANNEL MULTIPLEXER



ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{GST}	Gate Threshold Voltage	−3		−6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current*			−5	nA	$V_{GS} = V_{BS} = 0V$, $V_{DS} = -20V$
I_{GSS}	Gate Leakage Current (All except MEM 2004)			−1	nA	$V_{GS} = -20V$, $V_{DS} = V_{BS} = 0V$
I_{GSS}	Gate Leakage Current (MEM 2004)			−4	pA	$V_{GS} = -40V$, $V_{DS} = V_{BS} = 0$
I_{SDS}	Source Leakage Current			−5	nA	$V_{GD} = V_{BD} = 0V$, $V_{SD} = -20V$
BV_{DSS}	Drain-Source Breakdown	−30			Volts	$V_{GS} = V_{BS} = 0V$, $I_D = -10\mu A$
BV_{SDS}	Source-Drain Breakdown	−30			Volts	$V_{GD} = V_{BD} = 0V$, $I_S = -10\mu A$
BV_{GSS}	Gate to Source Breakdown (All except MEM 2004)	−30			Volts	$V_{DS} = V_{BS} = 0V$, $I_G = -10\mu A$
BV_{GSS}	Gate to Source Breakdown** (MEM 2004)	±60	±100		Volts	$V_{DS} = V_{BS} = 0$
$I_{D(on)}$	Drain Current	−4	−10		mA	$V_{DS} = V_{GS} = -10V$
$V_{G(r)}$	Reverse Gate Voltage (Except MEM 2004)		+1.5		Volts	$I_{GS} = 0.1mA$
$R_{DS(on)}$	Drain to Source "ON" Resistance		200	500	Ohms	$V_{GS} = -15V$, $I_D = -0.1mA$
C_{gs}	Gate to Source Capacitance		1.1		pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance		1.1		pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		0.2		pF	$V_{DS} = -10V$, $I_D = -0.1mA$

*Average for number of drains in parallel.
**This breakdown voltage should not be exceeded.

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GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

SERIES-SHUNT CHOPPER

MEM 2008

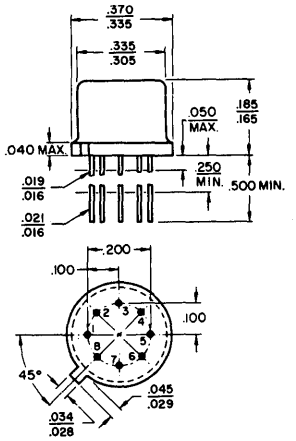
GENERAL DESCRIPTION:

The MEM 2008 is designed to be used as an effective chopper of voltages from source resistances in the megohm region, as well as lower impedances, with a minimum amount of spiking, noise, etc.

FEATURES:

- Integrated zener clamp protects the gate
- Zero offset voltage
- Isolated drive signal
- Extremely low drive power required
- High ratio of "ON" to "OFF" resistance of series and shunt MTOS devices (approximately 200 db)

TO-78



Bottom view
NOTE: All dimensions in inches

ELECTRICAL CHARACTERISTICS:

(T_A = 25°C)

CHARACTERISTIC	TYPICAL	UNIT	CONDITION
Output Leakage to all other leads	−10	pA	V = −10V
Maximum Chopping Frequency	100	kHz	
Maximum Input Signal Voltage	−20	Volts	

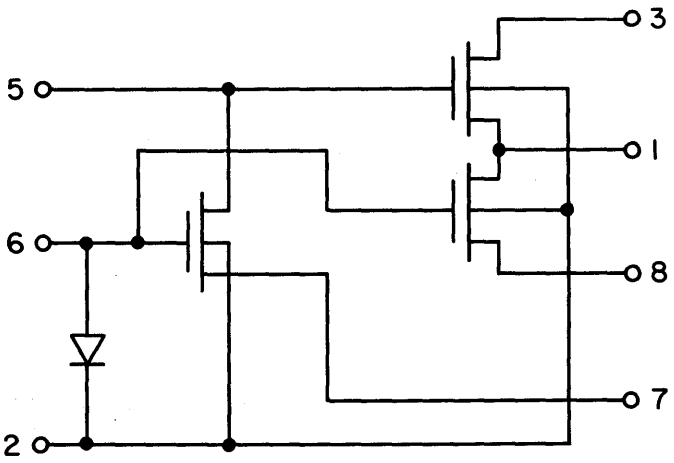


FIGURE 1 — INTEGRATED CHOPPER

SERIES-SHUNT CHOPPER MEM 2008

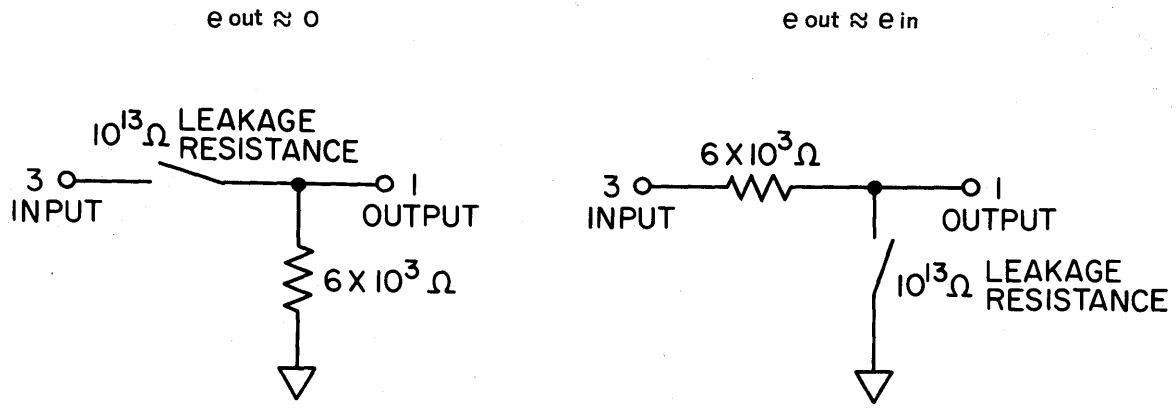


FIGURE 2
EQUIVALENT CIRCUIT FOR INTEGRATED CHOPPER

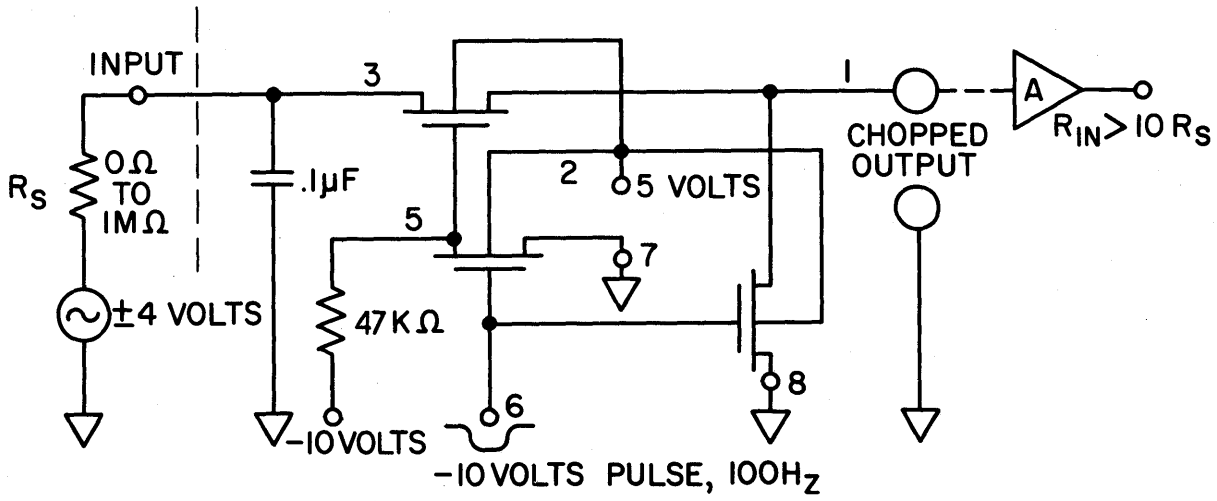


FIGURE 3
TYPICAL SERIES SHUNT CHOPPER CIRCUIT USING THE MEM 2008 INTEGRATED CIRCUIT

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T-6014

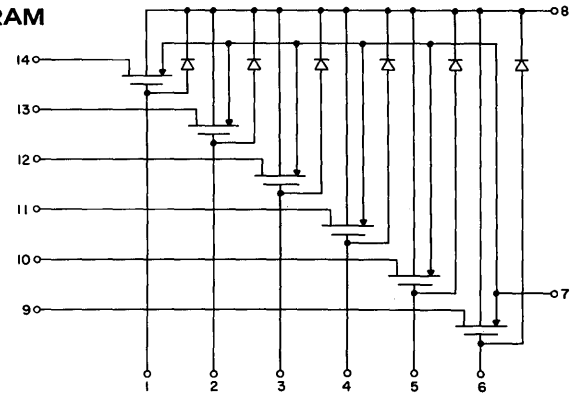
GENERAL INSTRUMENT
MTOS MULTIPLEXER

P CHANNEL — ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

ADVANCE
MARCH, 1967

MEM2009

CIRCUIT DIAGRAM



FEATURES

- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- Low "on" Resistance

APPLICATIONS
MULTIPLEXING

- Analog Multiplexing
- Time division multiplexing
- Chopping

MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

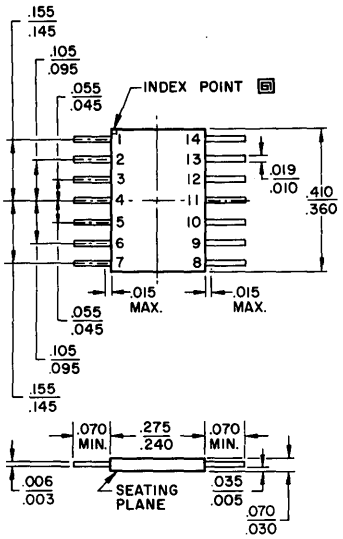
Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	−50 mA
Gate Current (forward direction for zener clamp)	+0.1 mA
Storage Temperature	−50 to 150°C
Operating Ambient Temperature	−50 to 85°C
Operating Junction Temperature	−50 to 125°C
Total dissipation at 25°C Ambient Temperature	900 mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	150 mW

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	−2.5		−6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$
I_{DSS}	Drain Leakage Current		−0.2	−3.0	nA	$V_{DS} = -20V$, $V_{GS} = 0$
I_{SDS}	Source Leakage Current (Total for all Units)		−1.2	−12	nA	$V_{SD} = -20V$, $V_{GS} = 0$
I_{GSS}	Gate Leakage Current		−0.1	−1.0	nA	$V_{GS} = -20V$, $V_{DS} = 0$
$I_{D(ON)}$	Drain Current	−3.0	−6.0		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain—Source Breakdown	−30			Volts	$I_D = -10\ \mu A$, $V_{GS} = 0V$
BV_{SDS}	Source—Drain Breakdown	−30			Volts	$I_S = -10\ \mu A$, $V_{GD} = 0V$
BV_{GSS}	Gate—Source Breakdown	−30		−60	Volts	$I_G = -10\ \mu A$, $V_{DS} = 0V$
Y_{fs}	Transadmittance		2500		μmho	1 kHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate To Source Capacitance		3.0	6.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{gd}	Gate To Drain Capacitance		1.9	3.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{ds}	Drain To Source Capacitance		1.7	3.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain To Source On Resistance		150	400	Ohms	$V_{GS} = -20V$, $I_D = 100\ \mu A$

TO-87

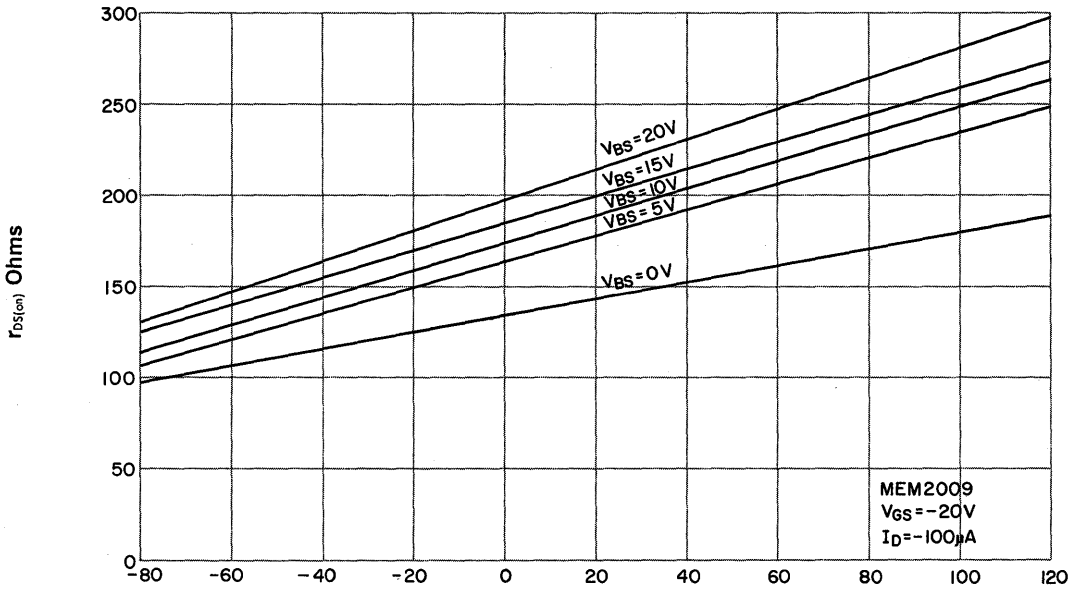


Note: All dimensions in inches.

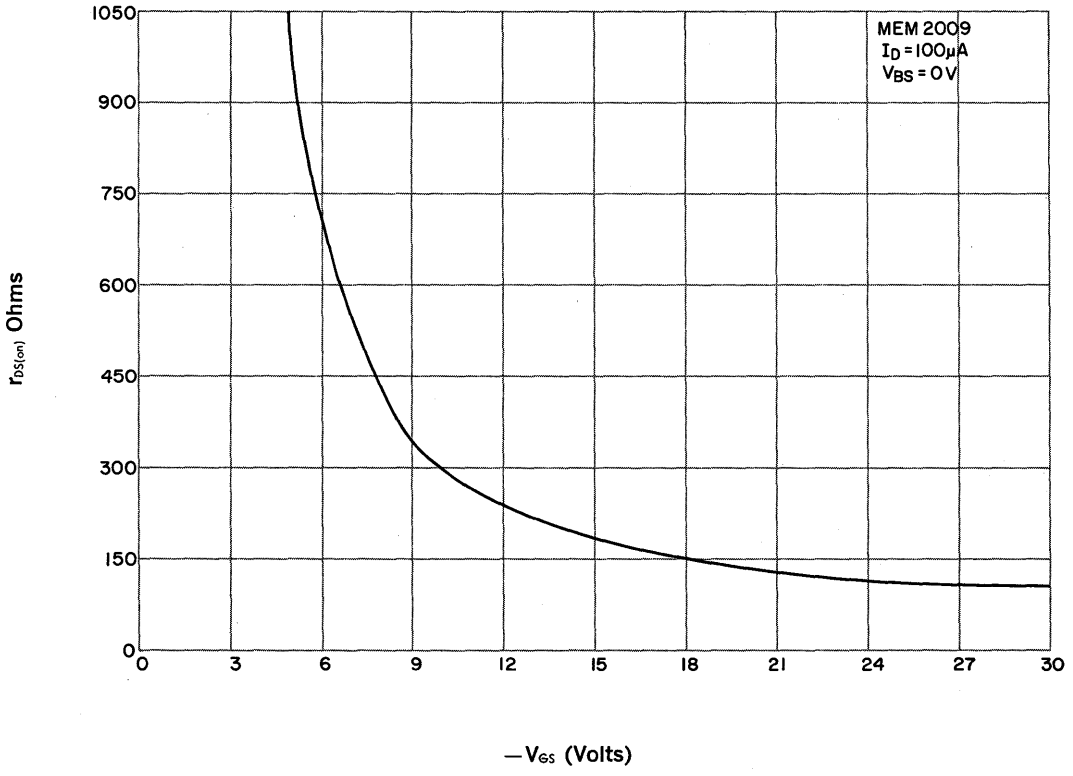
TERMINALS

P/N	FUNCTION
1	Gate 1
2	Gate 2
3	Gate 3
4	Gate 4
5	Gate 5
6	Gate 6
7	Source
8	Substrate
9	Drain 6
10	Drain 5
11	Drain 4
12	Drain 3
13	Drain 2
14	Drain 1

DRAIN TO SOURCE, ON RESISTANCE VERSUS TEMPERATURE



ON RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



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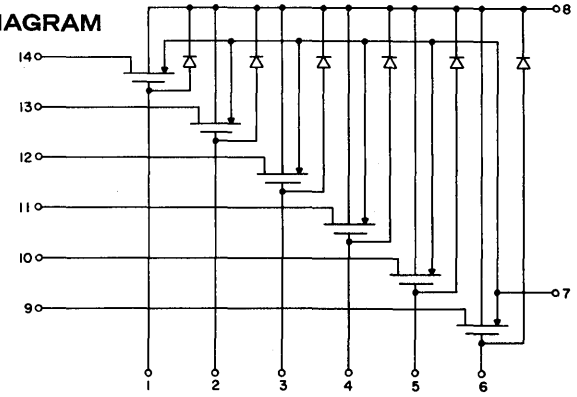
GENERAL INSTRUMENT
HIGH VOLTAGE MTOS MULTIPLEXER

PRELIMINARY
JULY, 1967

P CHANNEL — ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

MEM 2017

CIRCUIT DIAGRAM



FEATURES

- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- High Drain, Source and Gate Breakdown Voltages

APPLICATIONS MULTIPLEXING

- Analog Multiplexing
- Time division multiplexing
- Chopping

MAXIMUM RATINGS

($T_A = 25°C$, unless otherwise specified — body grounded)

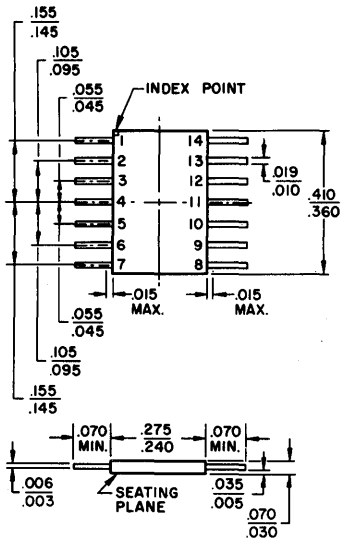
Drain to Source Voltage	—80V
Gate to Source Voltage	—80V
Gate to Drain Voltage	—80V
Drain Current	—20mA
Gate Current (forward direction for zener clamp)	+0.1mA
Storage Temperature	—50 to 150°C
Operating Ambient Temperature	—50 to 85°C
Operating Junction Temperature	—50 to 125°C
Total dissipation at 25°C Ambient Temperature	300mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	50mW

ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	—3.0		—6.0	Volts	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$
I_{DSS}	Drain Leakage Current		—0.2	—0.5	nA	$V_{DS} = -20V$, $V_{GS} = 0$
I_{SDS}	Source Leakage Current (Total for all Units)		—1.0	—2.0	nA	$V_{SD} = -20V$, $V_{GS} = 0$
I_{GSS}	Gate Leakage Current		—0.1	—0.5	nA	$V_{GS} = -20V$, $V_{DS} = 0$
$I_{D(ON)}$	Drain Current	—1.0	—3.0		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain—Source Breakdown	—50	—65	—80	Volts	$I_D = -10\ \mu A$, $V_{GS} = 0V$
BV_{SDS}	Source—Drain Breakdown	—50	—60	—80	Volts	$I_S = -10\ \mu A$, $V_{GD} = 0V$
BV_{GSS}	Gate—Source Breakdown	—50	—70	—80	Volts	$I_G = -10\ \mu A$, $V_{DS} = 0V$
Y_{fs}	Transadmittance		700		μmho	1 kHz, $V_{DS} = -20V$, $I_D = -5mA$
C_{gs}	Gate To Source Capacitance		0.2	0.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{gd}	Gate To Drain Capacitance		0.2	0.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{ds}	Drain To Source Capacitance		1.0	2.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain To Source On Resistance		700	1000	Ohms	$V_{GS} = -20V$, $I_D = 100\ \mu A$

TO-87



Note: All dimensions in inches

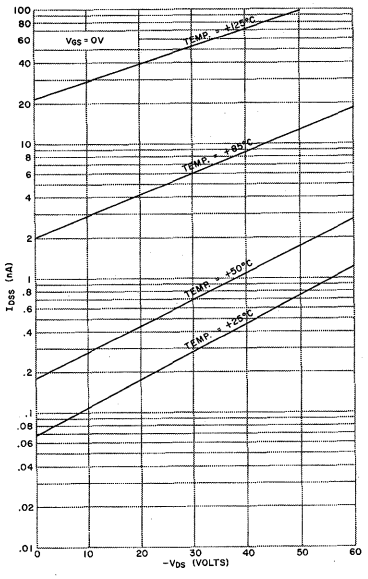
TERMINALS

P/N	FUNCTION
1	Gate 1
2	Gate 2
3	Gate 3
4	Gate 4
5	Gate 5
6	Gate 6
7	Source
8	Substrate
9	Drain 6
10	Drain 5
11	Drain 4
12	Drain 3
13	Drain 2
14	Drain 1

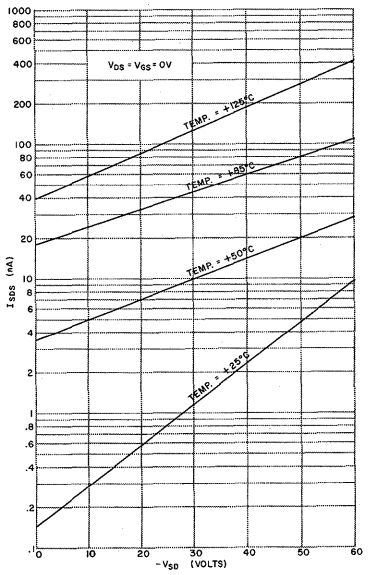
P CHANNEL — ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR MEM 2017

TYPICAL ELECTRICAL CHARACTERISTICS

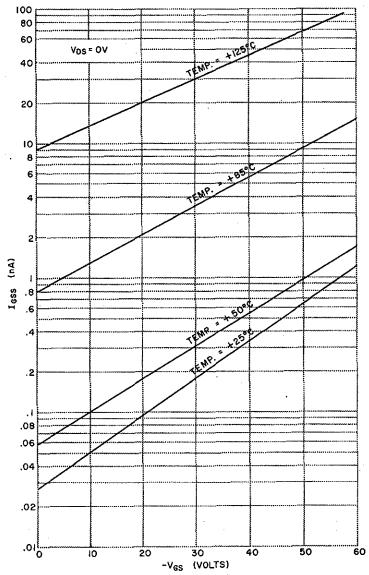
DRAIN LEAKAGE VS DRAIN VOLTAGE



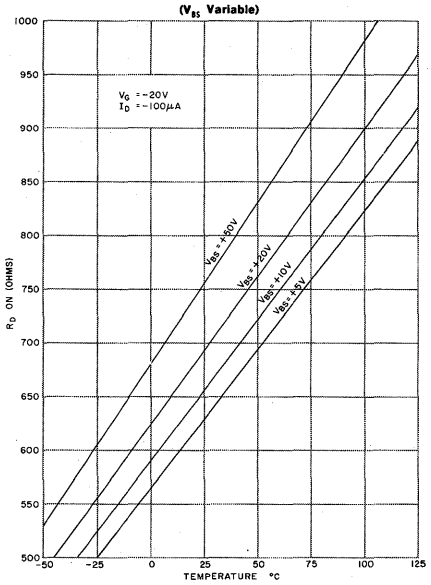
SOURCE LEAKAGE VS SOURCE VOLTAGE



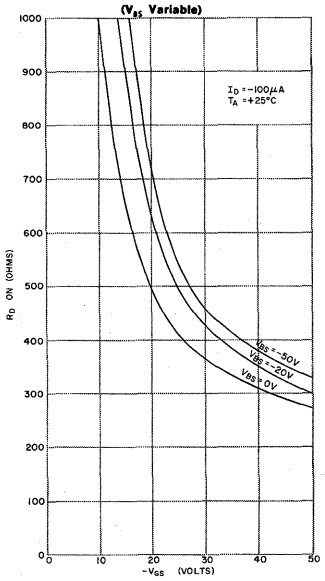
GATE LEAKAGE VS GATE VOLTAGE



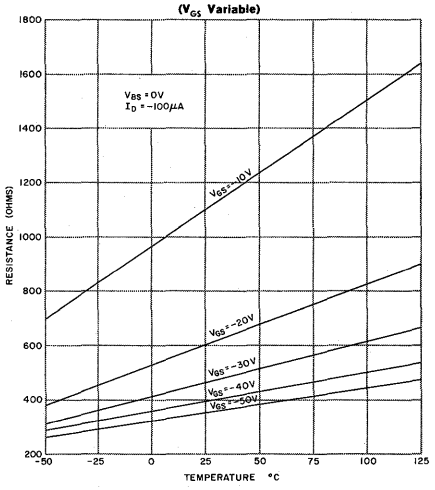
DRAIN RESRISTANCE VS TEMPERATURE
(V_{BS} Variable)



DRAIN RESISTANCE VS GATE VOLTAGE
(V_{BS} Variable)



DRAIN RESISTANCE VS TEMPERATURE
(V_{GS} Variable)



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MTOS INTEGRATED CIRCUIT

ADVANCE
DECEMBER, 1967

MEM 3005SP

5-BIT SERIAL IN-PARALLEL OUT SHIFT REGISTER

DESCRIPTION

The MEM 3005SP is a 5-bit static shift register constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-channel enhancement mode transistors. With two clock inputs ($\phi1$ and $\phi2$) supplied, the unit can operate from d.c. to 1 MHz in serial mode.

In serial operation, data present on the serial data input line is shifted into the register at $\phi1$ time, and similarly, the data previously stored in the first stage is shifted into the second stage, second to third, third to fourth and fourth to fifth.

The shifted data appears on the outputs in time sequence with the negative edge of $\phi2$ clock pulse. Thus the true outputs of each stage are available at $\phi2$ time. Each bit of delay has a cross-coupled flip-flop in order that data might be stored indefinitely between clock pulses. For long term storage, it is necessary for $\phi2$ to be a logic "1" and $\phi1$ a logic "0". Note that it is important that $\phi1$ and $\phi2$ are not at a logic "1" simultaneously, otherwise all stages shall assume the same state as the serial data input (Pin 5).

MAXIMUM RATINGS

Power Supplies (V_{DD} & V_{GG}) ..... −30 Volts to +0.3 Volts
Clock and Data Input Voltage ..... −30 Volts to +0.3 Volts
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS (SEE FIGURE 1)

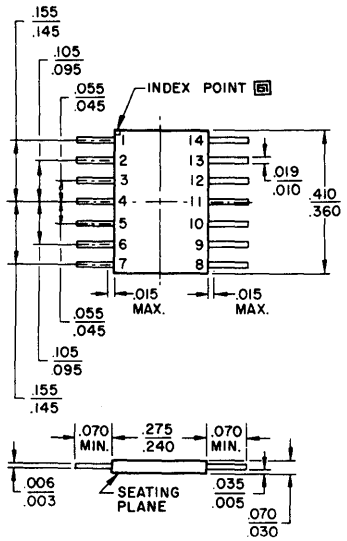
A. Standard Conditions (unless otherwise specified)

$V_{DD} = -13$ Volts ± 1 Volt Load = 1.0 MΩ and 10pF

$V_{GG} = -27$ Volts ± 1 Volt $T_A = -55°C$ to +85°C

ELECTRICAL CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
CLOCKS					
Repetition Rate	d.c.	—	1.0	MHz	
Pulse Widths					
$\phi1$	0.2	—	10	μS	
$\phi2$	0.4	—	—	μS	
Delay (ϕd)	0.01	—	10	μS	
Rise and Fall Time, t_r, t_f (10% to 90%)	—	—	5.0	μS	
Logic Levels					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−26	—	−28	Volts	
Input Capacitance					
$\phi1$	—	2.0	4.0	pF	$\phi1 = \phi2 = 0$ Volts
$\phi2$	—	4.0	6.0	pF	$\phi1 = \phi2 = 0$ Volts
Input Impedance					
$\phi1$	250	—	—	K ohms	
$\phi2$	60	250	—	K ohms	
DATA INPUT					
Pulse Width (D_{pw})	0.2	—	—	μS	90% Points
Capacitance	—	2.0	3.0	pF	$V_{IN} = 0$ Volts
Logic Levels					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Leakage Current	—	—	1.0	μA	$V_{IN} = -20$ Volts
Noise Immunity	1.0	2.0	—	Volts	Nominal Power Supply Voltages
OUTPUTS					
Logic Levels					
Logic "0"	—	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
Impedance to Ground	—	2.0	3.0	K ohms	Output a Logic "0"
Drive Capability	−10	−11	—	Volts	R = 27K to Ground
Drive Capability	−5.0	—	—	Volts	R = 4K to Ground
Short Circuit Current to Ground	5.0	—	10	mA	Output a Logic "1"
POWER SUPPLY CURRENT DRAIN					
V_{DD}	—	—	2.0	mA	$V_{DD} = -13$ Volts
V_{GG}	—	—	1.0	mA	$V_{GG} = -27$ Volts

TO-87



Note: All dimensions in inches.

TERMINALS

P/N	FUNCTION
1	V_{SS} (Ground)
2	$\phi2$
3	V_{GG}
4	$\phi1$
5	Data In
6	V_{SS} (Ground)
7	No connection
8	No connection
9	Out 1 (Parallel Outputs)
10	Out 2
11	Out 3
12	Out 4
13	Out 5
14	V_{DD}

FUNCTIONAL DIAGRAM

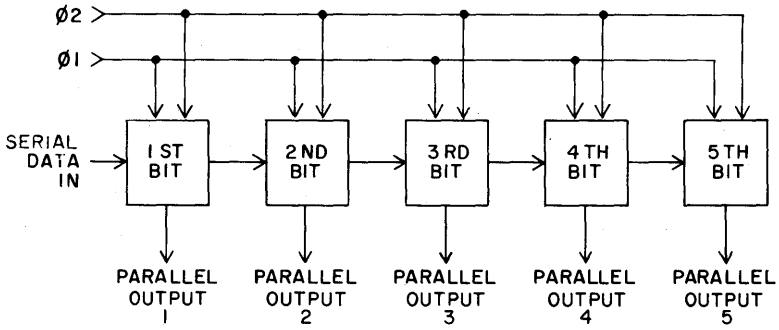
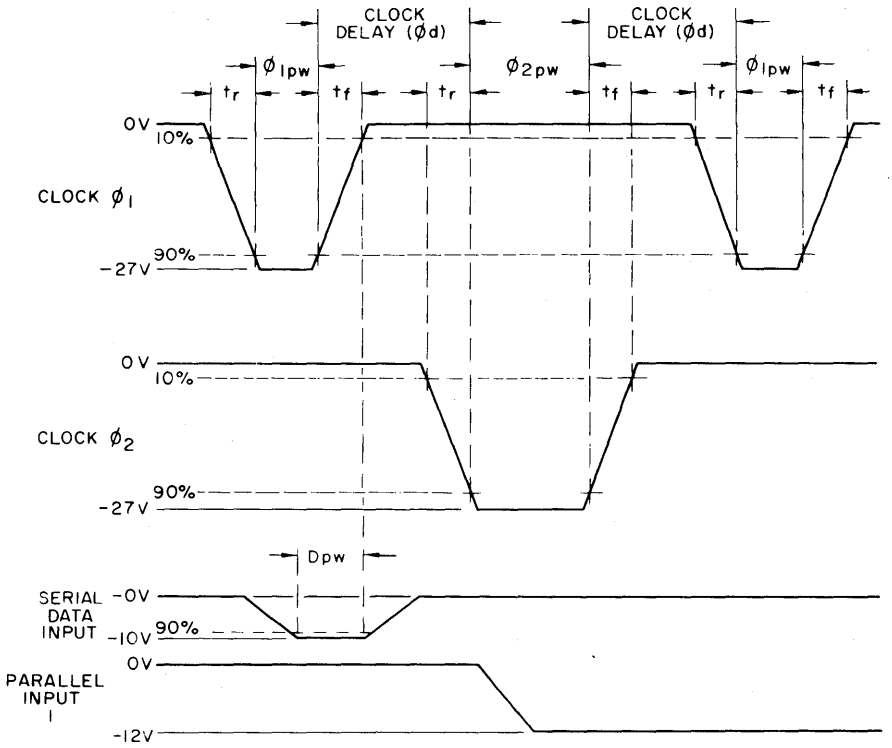
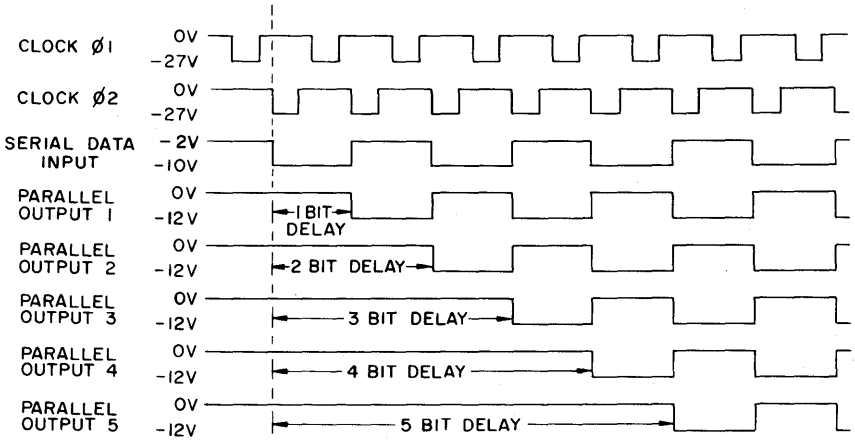


FIGURE 1



TYPICAL TIMING DIAGRAM FOR NORMAL DEVICE OPERATION



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

12-BIT SERIAL IN-PARALLEL OUT

MEM 3012SP

DESCRIPTION

The MEM 3012SP is a 12-Bit d.c. serial input parallel output shift register constructed on a single monolithic chip with MTOS P-channel enhancement mode transistors. This unit will operate from d.c. to 100 kHz.

MAXIMUM RATINGS

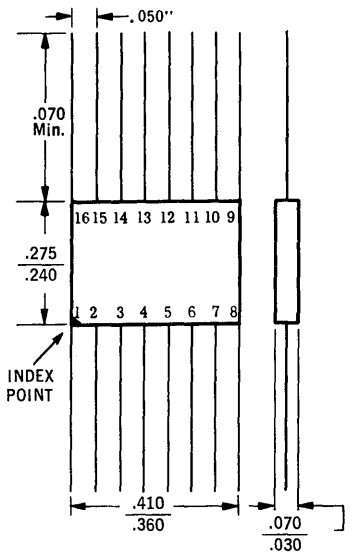
Drain Voltage ($-V_{dd}$) ..... −30V to +.3V
Clock and Input Voltages ..... −30V to +.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified):
$V_{dd} = -27$ Volts ±1 Volt, Load = 10MΩ and 10pF.
$T_A = -55°C$ to +85°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	100	kHz	
Clock Pulse Width (ϕ_{pw})	0.4	—	30	μsec.	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	10	μsec.	
Clock & Data Input Logic Levels					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Clock Fan-In	—	—	3		
Data Input Pulse Width (D_{pw})	0.3	—	—	μsec.	$\phi_{pw} = 0.4$ μsec. SEE FIG. 1
Data Fan-In	—	—	1		
Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Output Logic Levels					
Logic "0"	—	−0.5	−1.0	Volt	d.c. to 100 kHz
Logic "1"	−11	−12	—	Volts	
Propagation Delay Plus Fall Time (t_{pd1})	—	—	5.0	μsec.	SEE FIG. 1
Propagation Delay Plus Rise Time (t_{pd2})	—	—	2.0	μsec.	SEE FIG. 1
Fan-Out	—	—	5		
Output Impedance to Ground (Output a Logic "0")	—	—	3000	Ohms	
Supply Current Drain	—	—	6.0	mA	

16 Lead Flatpack

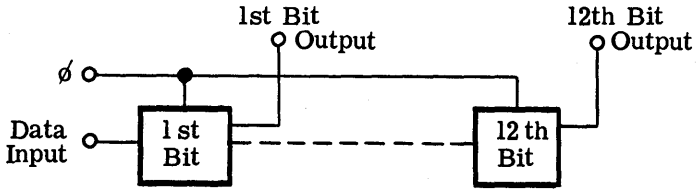


Note: All dimensions in inches.

TERMINALS

P/N	Function
1	Ground
2	Output 6
3	Output 5
4	Output 4
5	Output 3
6	Output 2
7	Output 1
8	Data Input
9	$-V_{dd}$
10	Clock (ϕ)
11	Output 12
12	Output 11
13	Output 10
14	Output 9
15	Output 8
16	Output 7

LOGIC DIAGRAM



TYPICAL TIMING DIAGRAM

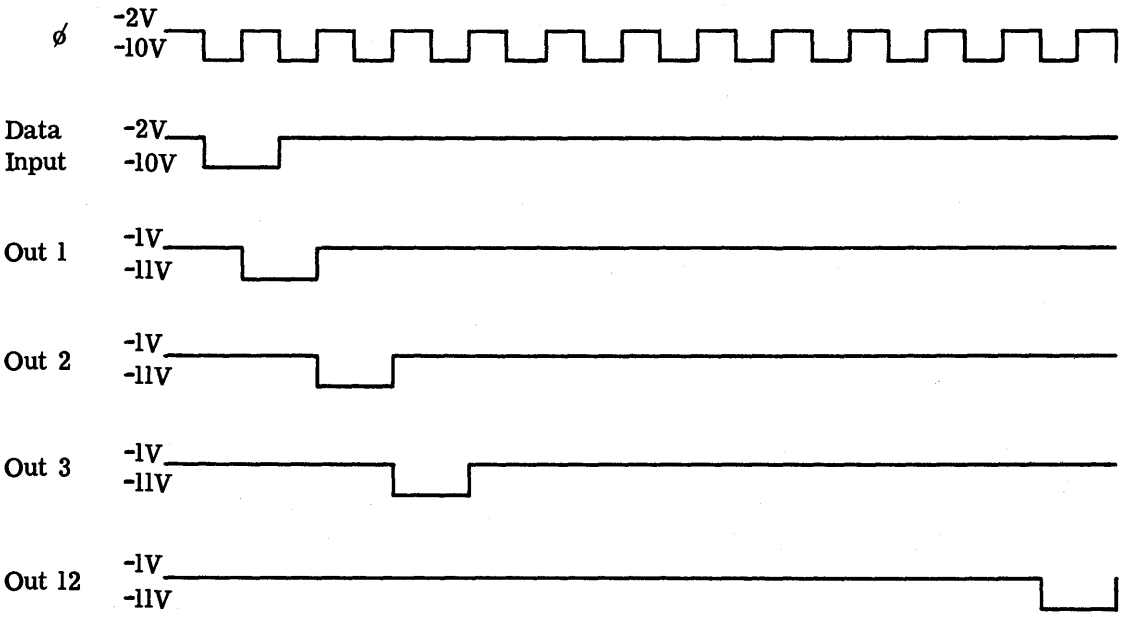
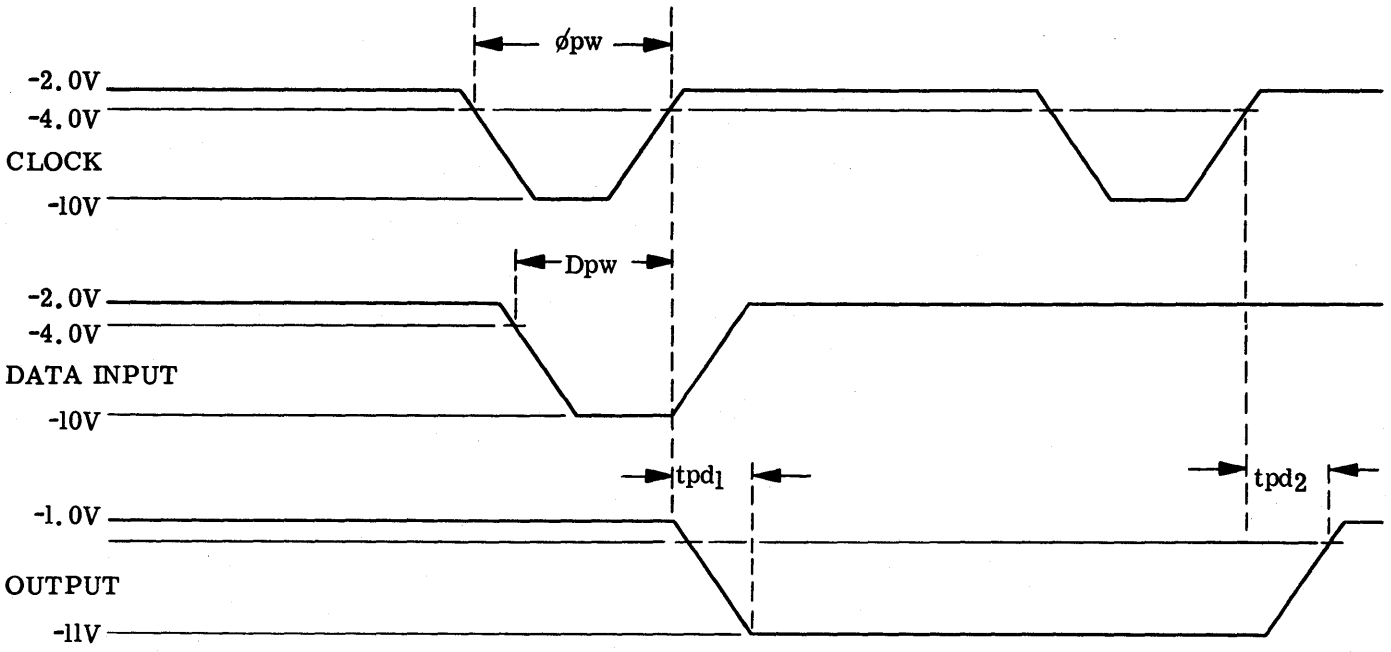


FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

21-BIT SHIFT REGISTER

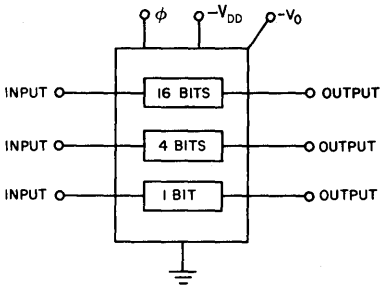
MEM 3021

DESCRIPTION

The MEM 3021 is a 1, 4 and 16 bit static shift register constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between clock pulses. Only a single phase clock pulse (ϕ) has to be supplied; the additional 180° out of phase clock pulse ($\overline{\phi}$) is generated in the chip.

The outputs will change on the positive edge of the clock pulse. The supply voltage ($-V_O$) for the output stages can have any value between ground and −28 volts. By letting $-V_O$ be just a few volts it is possible to have the shift register drive other types of low voltage NPN transistor logic.

LOGIC DIAGRAM



MAXIMUM RATINGS

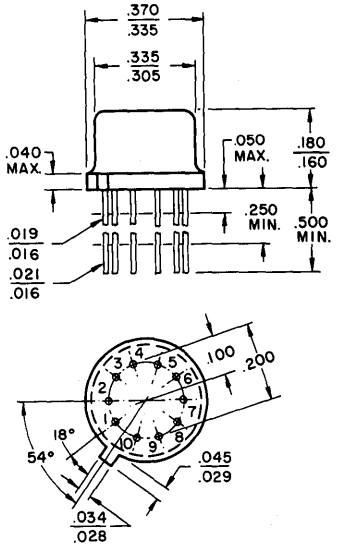
Drain Voltage	−30 Volts to +.3 Volt
Clock and Input Voltages	−30 Volts to +.3 Volt
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
$V_{dd} = V_O = 27$ Volts ±1 Volt, Load = 10MΩ and 10pF. $T_A = -55°C$ to +85°C

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	500	kHz	
Clock Pulse Width (ϕ_{pw})	1.0	—	10	μsec	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	4.0	μsec	
Clock Input Capacitance	—	—	6.0	pF	$V_{in} = 0$ Volts
Clock & Data Input Logic Levels Logic "0" Logic "1"	— −10	— —	−2.0 —	Volts Volts	
Data Input Pulse Width (D_{pw})	1.0	—	—	μsec	SEE FIG. 1 $\phi_{pw} = 1.0$ μsec
Data Fan-In	—	—	1.0		
Clock & Data Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Output Logic Levels Logic "0" Logic "1"	— −11	−0.5 −12	−1.0 —	Volt Volts	ϕ = dc to 250 kHz
Fan-Out	—	—	5.0		
Output Impedance to Ground	—	—	5.0	KΩ	(output A Logic "0")
Output Drive Capability	−10	−11	—	Volts	$R_L = 17K$ Ohms
Output Drive Capability	−5.0	—	—	Volts	$R_L = 4K$ Ohms
Supply Current Drain	—	—	5.4	mA	

LOW PROFILE 10 LEAD TO-74



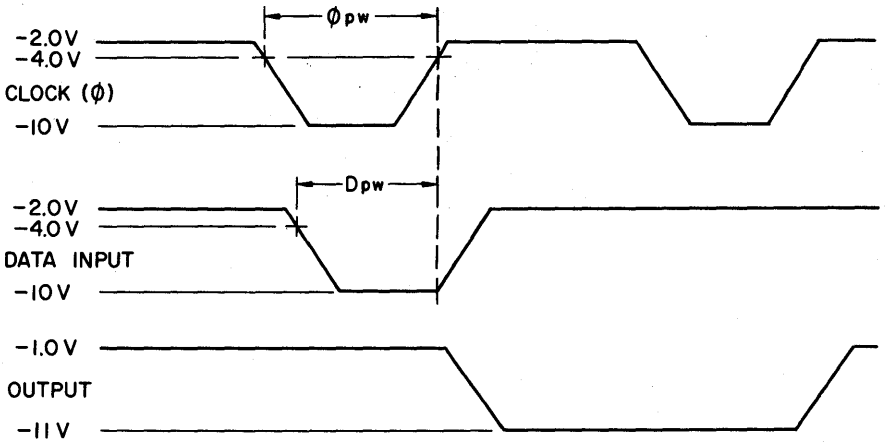
Bottom view
NOTE: All dimensions in inches

TERMINALS

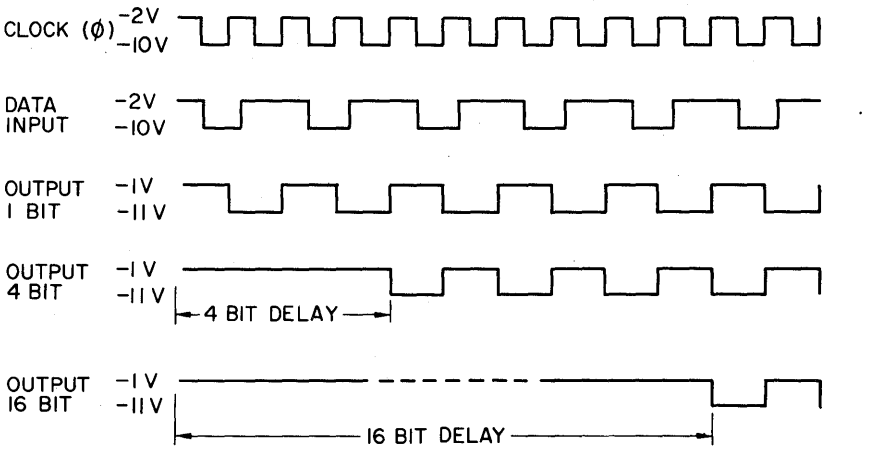
P/N	Function
1	Input (16 Bit)
2	Clock (ϕ)
3	Output Supply Voltage ($-V_O$)
4	Output (16 Bit)
5	Ground
6	Output (4 Bit)
7	Output (1 Bit)
8	Input (1 Bit)
9	Input (4 Bit)
10	Drain Voltage ($-V_{dd}$)

21-BIT SHIFT REGISTER MEM 3021

FIGURE 1

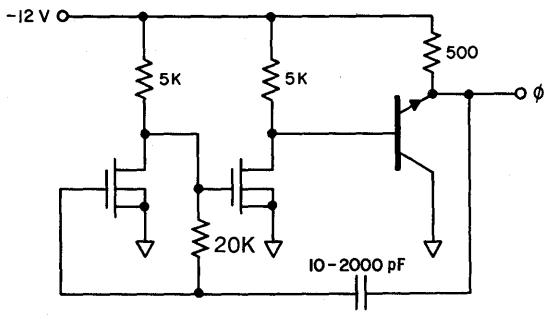


TYPICAL TIMING DIAGRAM

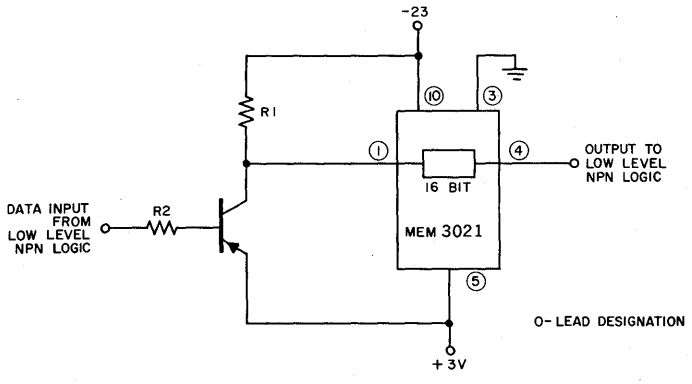


APPLICATIONS

The shift pulse can be supplied from a clock generator as shown below. The shift pulse amplitude requirement is the same as the logic swing required.



The shift register may be interfaced with low level NPN transistor logic, if desired, by using the circuit below.



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

21-BIT SHIFT REGISTER

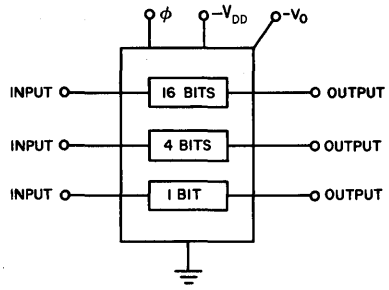
MEM 3021B

DESCRIPTION

The MEM 3021B is a 1, 4 and 16 bit static shift register constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between clock pulses. Only a single phase clock pulse (ϕ) has to be supplied; the additional 180° out of phase clock pulse ($\overline{\phi}$) is generated in the chip.

The outputs will change on the positive edge of the clock pulse. The supply voltage ($-V_O$) for the output stages can have any value between ground and −28 volts. By letting $-V_O$ be just a few volts it is possible to have the shift register drive other types of low voltage NPN transistor logic.

LOGIC DIAGRAM



MAXIMUM RATINGS

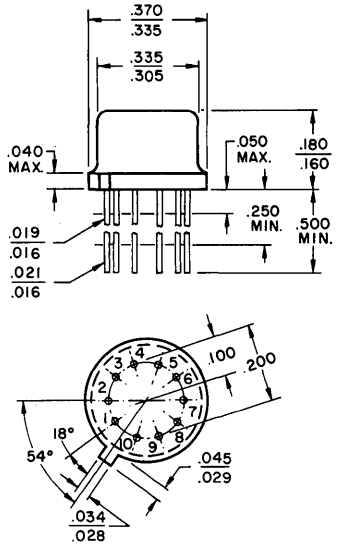
Drain Voltage	−30 Volts to +.3 Volt
Clock and Input Voltages	−30 Volts to +.3 Volt
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
$V_{dd} = V_O = 27$ Volts ±1 Volt, Load = 10MΩ and 10pF. $T_A = -55°C$ to +85°C

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	250	kHz	
Clock Pulse Width (ϕ_{pw})	1.0	—	10	μsec	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	4.0	μsec	
Clock Input Capacitance	—	—	6.0	pF	V_{in} = 0 Volts
Clock & Data Input Logic Levels Logic "0" Logic "1"	 — −10	 — —	 −2.0 —	 Volts Volts	
Data Input Pulse Width (D_{pw})	1.0	—	—	μsec	SEE FIG. 1 ϕ_{pw} = 1.0 μsec
Data Fan-In	—	—	1.0		
Clock & Data Input Leakage Current	—	—	1.0	μA	V_{in} = −20 Volts
Output Logic Levels Logic "0" Logic "1"	 — −11	 −0.5 −12	 −1.0 —	 Volt Volts	ϕ = dc to 250 kHz
Fan-Out	—	—	5.0		
Output Impedance to Ground	—	—	5.0	KΩ	(output A Logic "0")
Output Drive Capability	−10	−11	—	Volts	R_L = 17K Ohms
Output Drive Capability	−5.0	—	—	Volts	R_L = 4K Ohms
Supply Current Drain	—	—	5.4	mA	

LOW PROFILE 10 LEAD TO-74



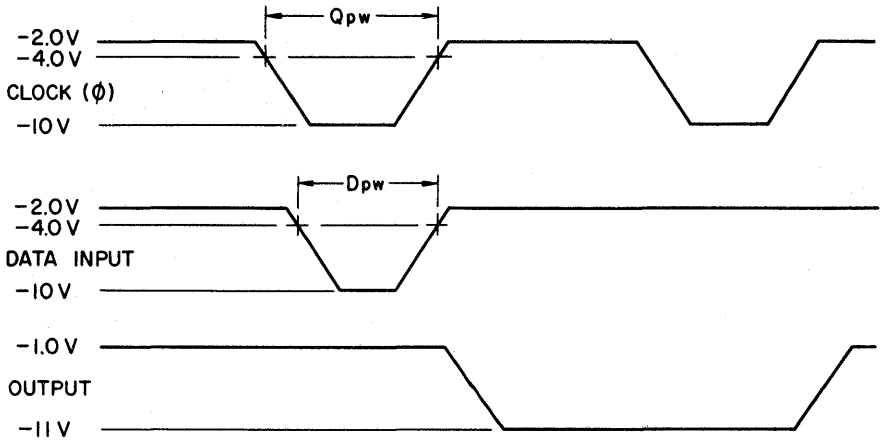
Bottom view
NOTE: All dimensions in inches

TERMINALS

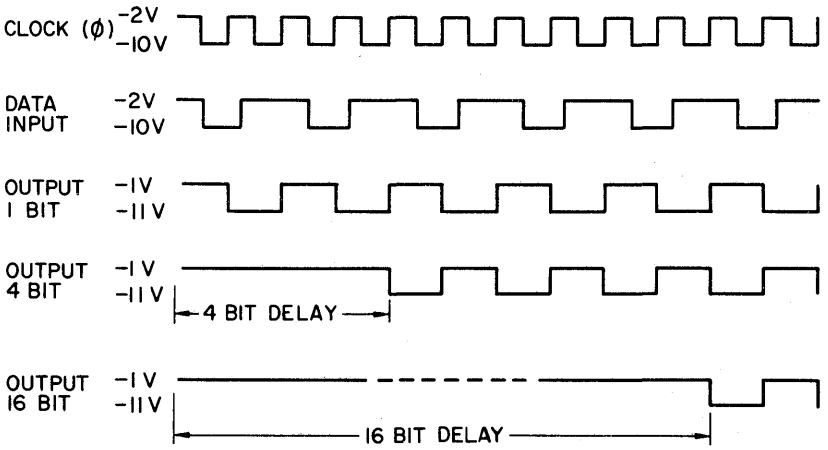
P/N	Function
1	Input (16 Bit)
2	Clock (ϕ)
3	Output Supply Voltage ($-V_O$)
4	Output (16 Bit)
5	Ground
6	Output (4 Bit)
7	Output (1 Bit)
8	Input (1 Bit)
9	Input (4 Bit)
10	Drain Voltage ($-V_{dd}$)

21-BIT SHIFT REGISTER MEM 3021B

FIGURE 1

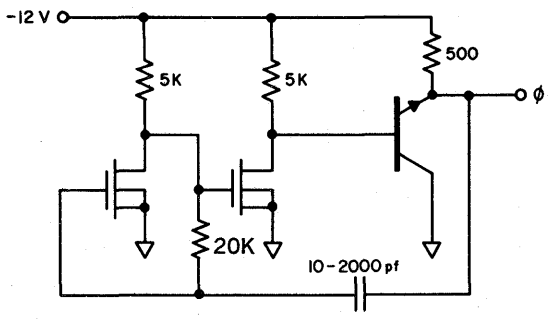


TYPICAL TIMING DIAGRAM

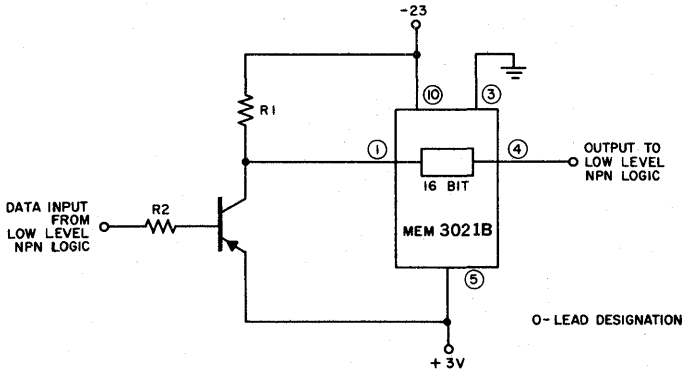


APPLICATIONS

The shift pulse can be supplied from a clock generator as shown below. The shift pulse amplitude requirement is the same as the logic swing required.



The shift register may be interfaced with low level NPN transistor logic, if desired, by using the circuit below.



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GENERAL INSTRUMENT

GENERAL INSTRUMENT MTOS INTEGRATED CIRCUIT

6 - 1Ø BINARY WEIGHTED SHIFT REGISTERS

ADVANCE

NOVEMBER, 1967

MEM 3032

DESCRIPTION

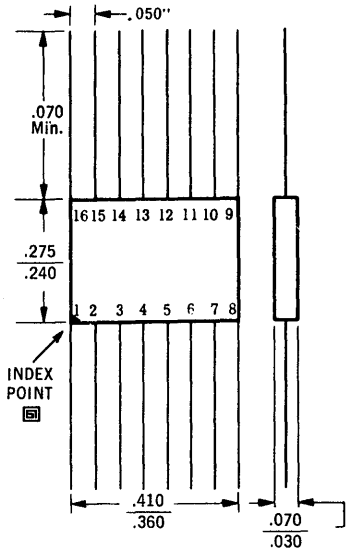
The MEM 3032 consists of six separate and distinct static shift registers, constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-Channel enhancement mode transistors. Each of the six registers have separate external inputs and outputs and may be used independently (refer to the Functional Block Diagram). Their lengths are binary weighted. By interconnecting the registers, any time delay between 1 and 32 bits may be achieved (examples: output of 1 bit to input of 4 bit = 5 bit delay; output of 8 bit to input of 2 bit = 10 bit delay, etc.).

The externally applied shift pulse (ϕ) will advance the information in all six registers by one complete bit for every complete period. New data will be accepted at any input during the time interval when the shift pulse (ϕ) is at the negative level (logic "1"). Data transitions will occur at the outputs only after the trailing edge of the shift pulse returns to a logic "O". Each register will hold its current data until another shift pulse is applied. Shift pulses may be applied at repetition rates from D.C. to 1 Megahertz.

FEATURES

- Binary Weighted Shift Registers For Any Count Frequency Division
- 1 MHz Shift Register Operation
- Monolithic Construction
- Zener Network Protection On All Circuits
- High Noise Immunity (1 volt minimum)
- Low Power Consumption (175mW)
- 16 Lead Flat Package
- Compatible With General Instrument Logic Family and Multiplexer System
- Six Separate Shift Registers

16-LEAD FLAT PACK



Note: All dimensions in inches

TERMINALS

P/N	FUNCTION
1	V_{SS}—Power Supply (Normally Ground)
2	16 BIT S.R. Input
3	(First) 1 BIT S.R. Output
4	(First) 1 BIT S.R. Input
5	16 BIT S.R. Output
6	Shift Pulse Input (ϕ)
7	V_{DD} Power Supply (Normally —13V)
8	V_{GG} Power Supply (Normally —27V)
9	8 BIT S.R. Input
10	(Second) 1 BIT S.R. Output
11	(Second) 1 BIT S.R. Input
12	2 BIT S.R. Output
13	2 BIT S.R. Input
14	4 BIT S.R. Output
15	4 BIT S.R. Input
16	8 BIT S.R. Output

MAXIMUM RATINGS

Drain Voltage (V_{DD}) ..... −30 Volts to +0.5 Volts
Gate Voltage (V_{GG}) ..... −30 Volts to +0.5 Volts
Shift Pulse & Data Input Voltage ..... −30 Volts to +0.5 Volts
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

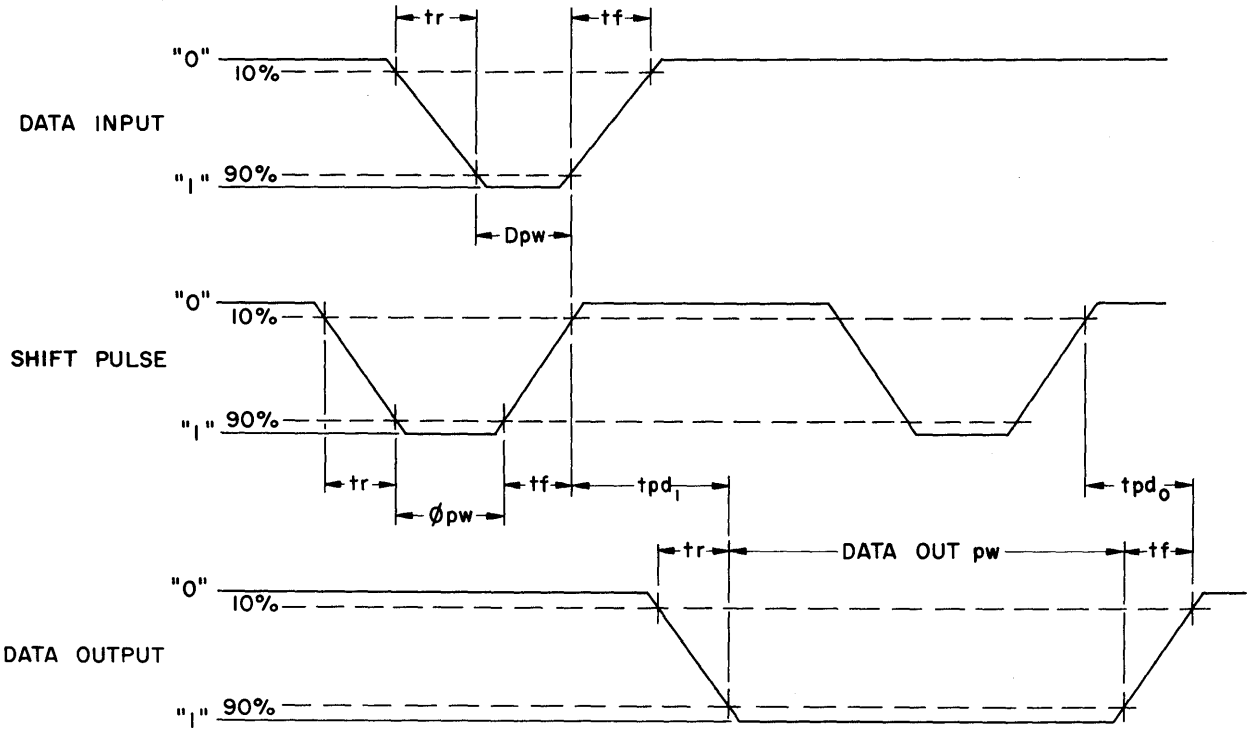
ELECTRICAL CHARACTERISTICS

Standard Conditions (Unless otherwise stated)
$V_{DD} = -13$ Volts ± 1 Volt, $V_{GG} = -27$ Volts ± 1 Volt
Load = 1.0MΩ and 10pF, $T_A = -55°C$ to + 85°C

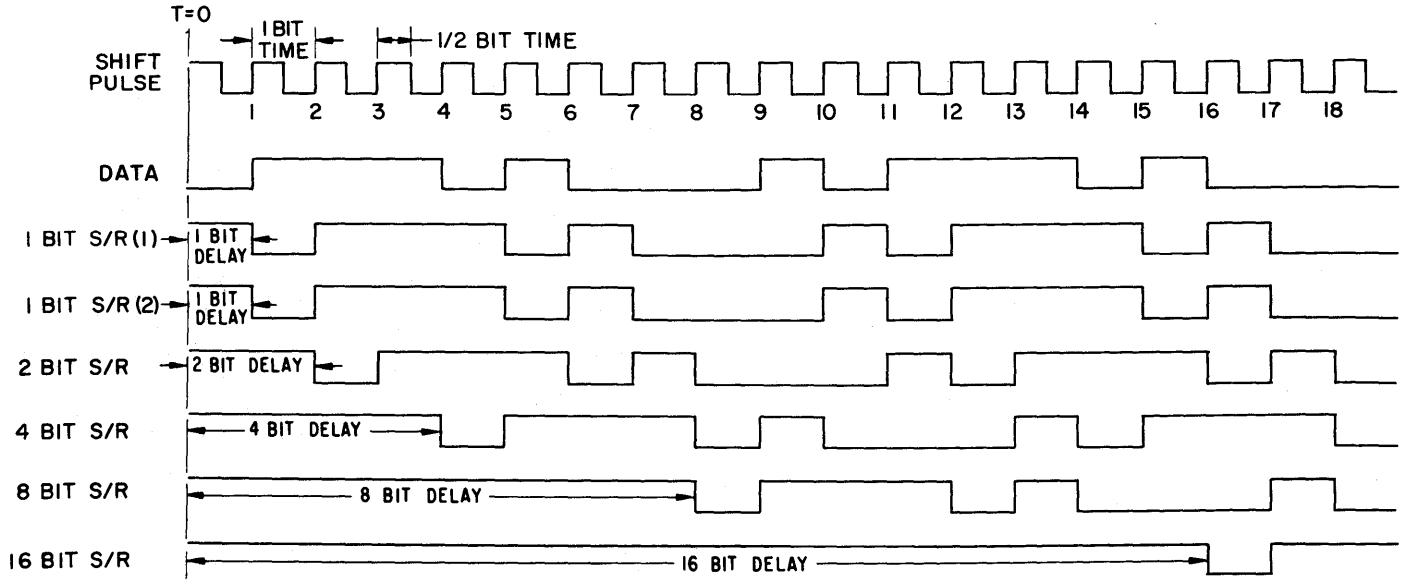
Electrical Characteristics	Min	Typ	Max	Units	Conditions
Shift Pulse (SEE FIGURE 1)					
Repetition Rate					
Lower Limit	d.c.*	—	—	Hz	@ Pw = .25 usec.
Upper Limit	1.0*	1.5	2.0	MHz	@ Pw = .25 usec.
Pulse Width					
Lower Limit (shortest possible time interval)	0.2	.25*	—	μS	@ 1 MHz
Upper Limit (longest permissible time interval)	10*	1000	5000	μS	@ 50 kHz Square Wave
Logic Levels					
Logic "0"	+0.5	0.0	−2.0*	Volts	
Logic "1"	−5.0	−9.0*	−27	Volts	(90% points)
Input Capacitance	—	—	6.0	pF	$V_{in} = 0$ Volts
Rise and Fall Times (t_r & t_f)	—	—	5.0*	μS	50 kHz sine wave shift pulse input
Input Data (SEE FIGURE 1)					
Pulse Width	.05	1.0*	—	μS	(90% points)
Logic Levels					
Logic "0"	+0.5	0.0	−2.0*	Volts	
Logic "1"	−5.0	−9.0*	−27	Volts	(90% points)
Input Capacitance	—	2.0	3.0	pF	
Leakage Current	—	—	0.5	μA	$V_{in} = -12$ Volts
Noise Immunity	1.0*	2.0	—	Volts	Nominal Power Supply Voltages
Outputs (SEE FIGURE 1)					
Logic Levels					
Logic "0"	(V_{SS})	−0.5	−1.0*	Volt	
Logic "1"	−11*	−12	(V_{DD})	Volts	
Impedance to V_{SS}					
Output At Logic "0"	1.0	2.0	3.0*	kΩ	
Short Circuit Current To Ground					
Output At Logic "1"	5.0*	10	—	mA	Nominal Power Supply Voltages
Drive Capability					
Output At Logic "1"	−10*	−11	(V_{DD})	Volts	$R_L = 27$kΩ to Ground
Output At Logic "1"	−5.0*	−7.0	(V_{DD})	Volts	$R_L = 4$kΩ to Ground
Power Supply Current Drain					
V_{DD}	—	6.0	10*	mA	$V_{DD} = -13$ Volts
V_{GG}	—	2.0	4.0*	.mA	$V_{GG} = -27$ Volts

*Indicates the level of performance each device must meet prior to being accepted for shipping.

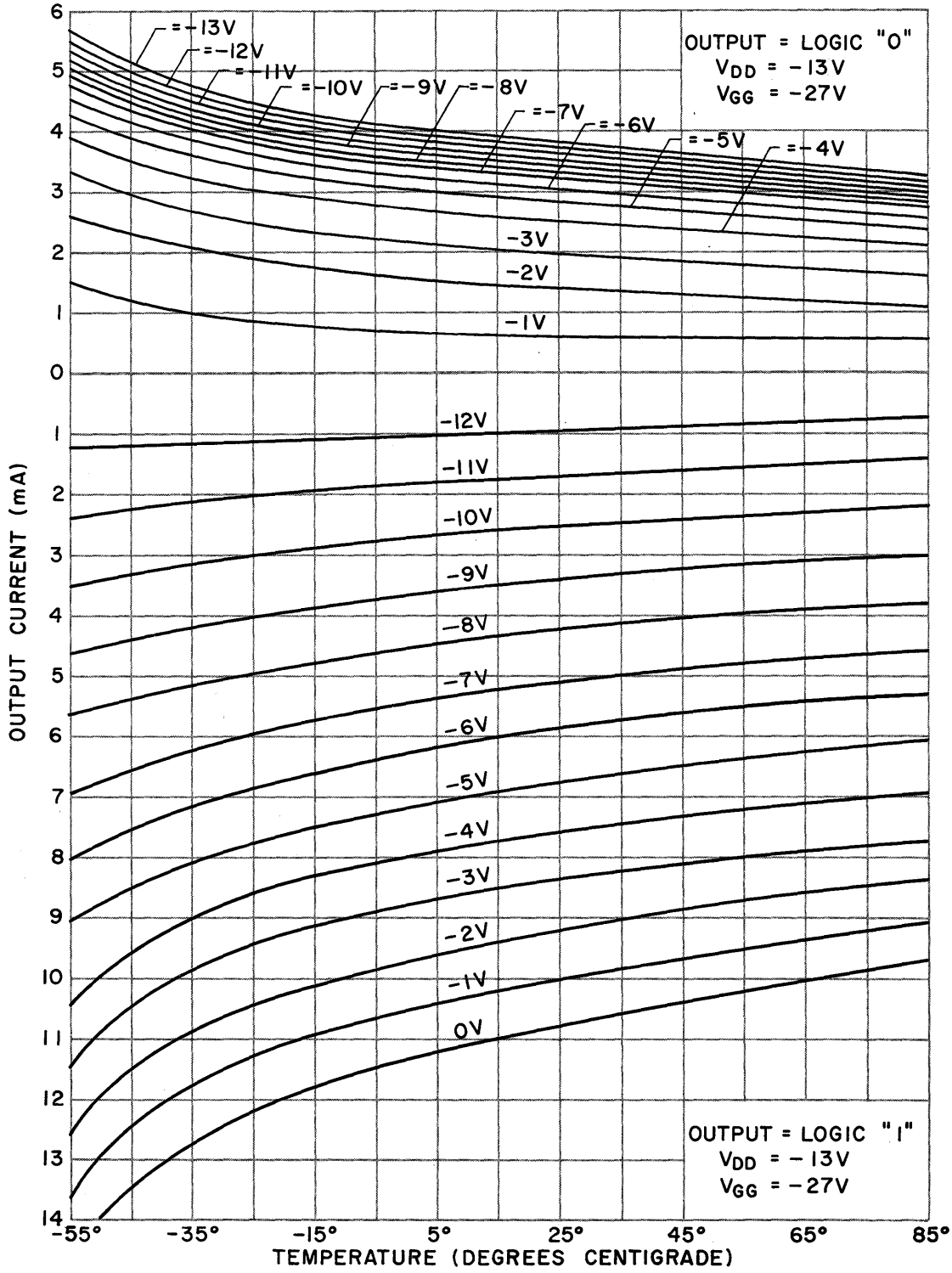
FIGURE 1



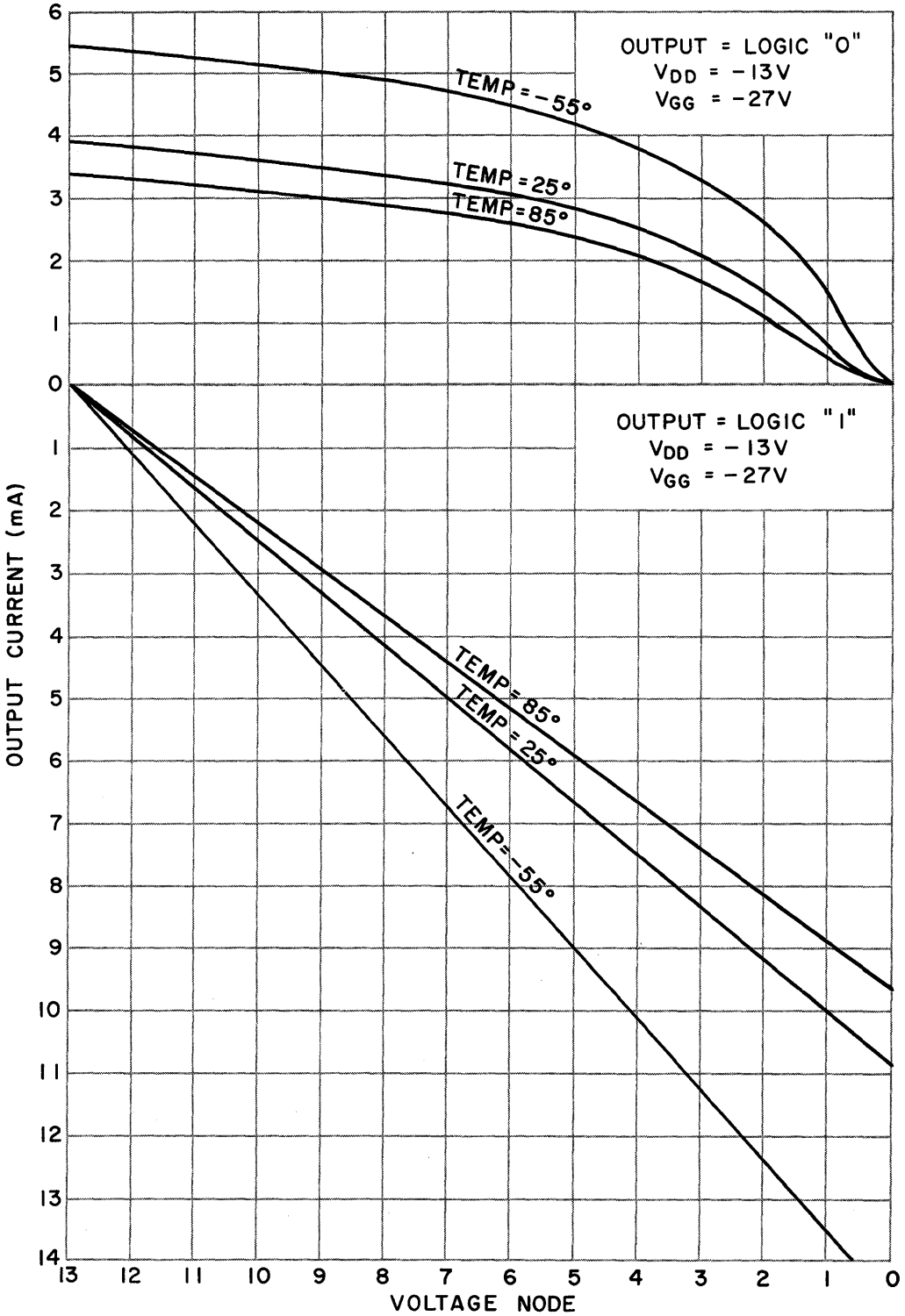
TYPICAL TIMING DIAGRAM



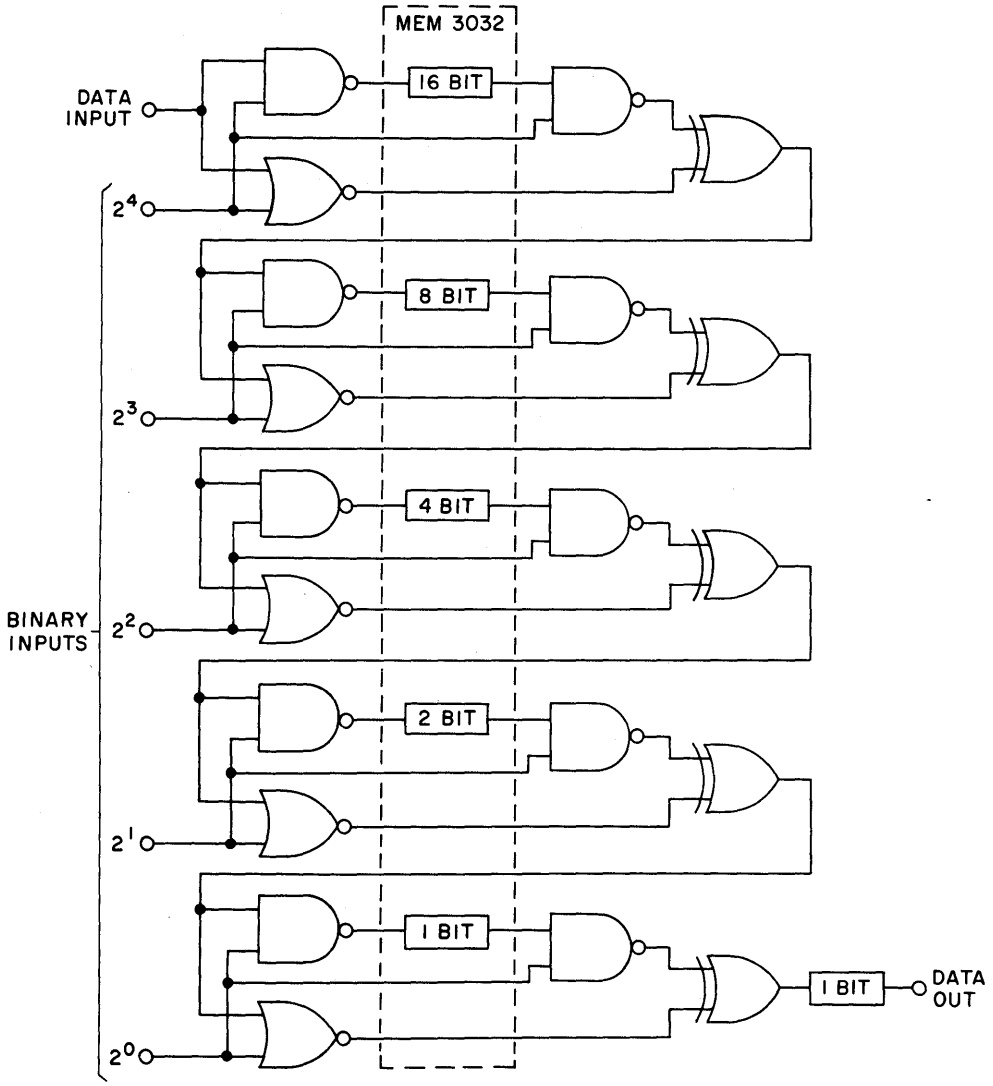
OUTPUT CURRENT VS TEMPERATURE (OUTPUT VOLTAGE CONSTANT)



OUTPUT CURRENT VS OUTPUT VOLTAGE (TEMPERATURE CONSTANT)



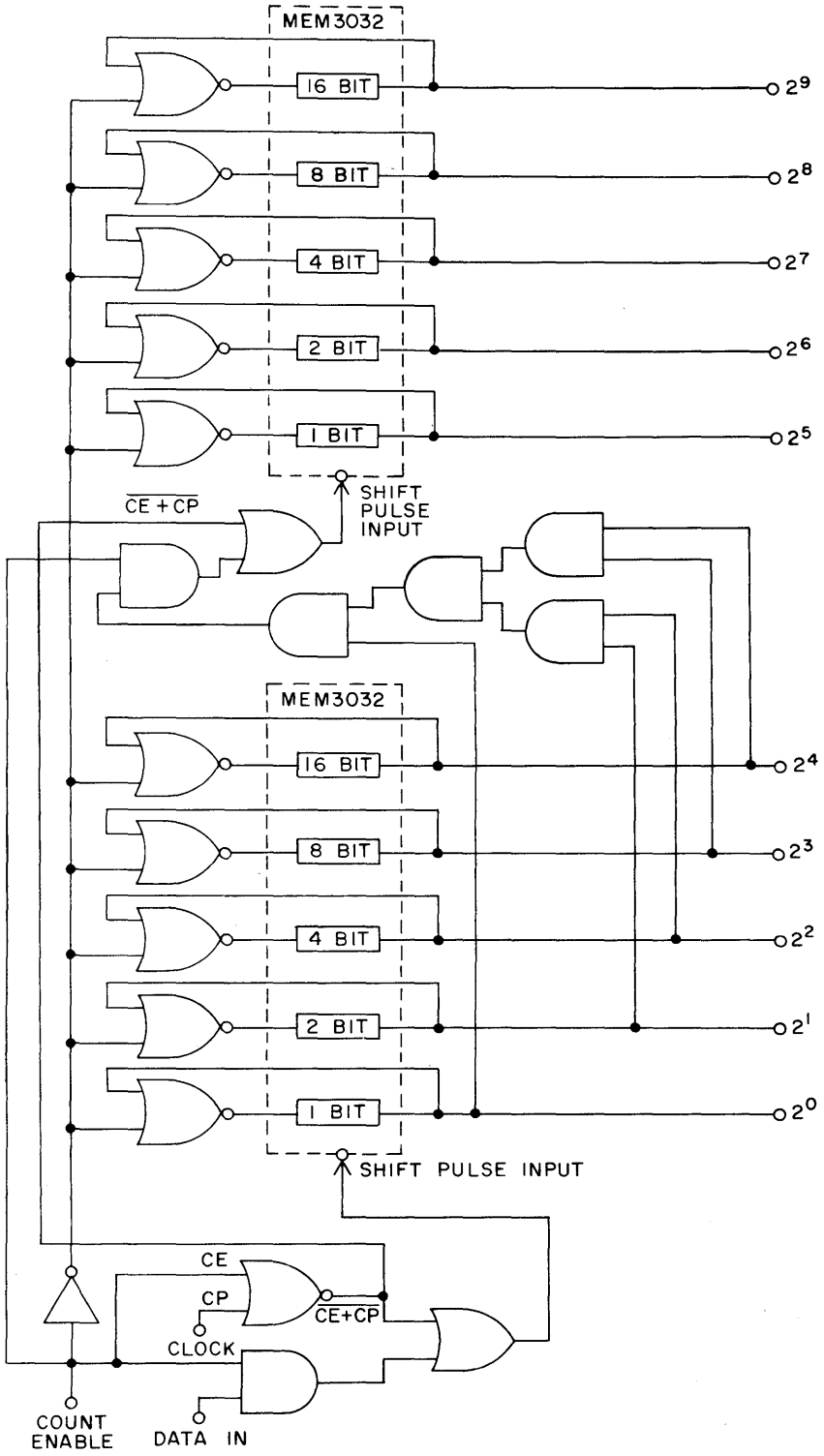
ELECTRONICALLY VARIABLE 1 TO 32-BIT DELAY CIRCUIT



Data presented to the "Data Input" jack of this circuit is electronically gated to any, or all of the six binary weighted registers of the MEM 3032. The gating is determined by a 5 bit binary word at the circuits "Binary Input" jacks. A fixed one bit delay is present at all times, adding a one bit delay to whatever the binary weight of the input word is.

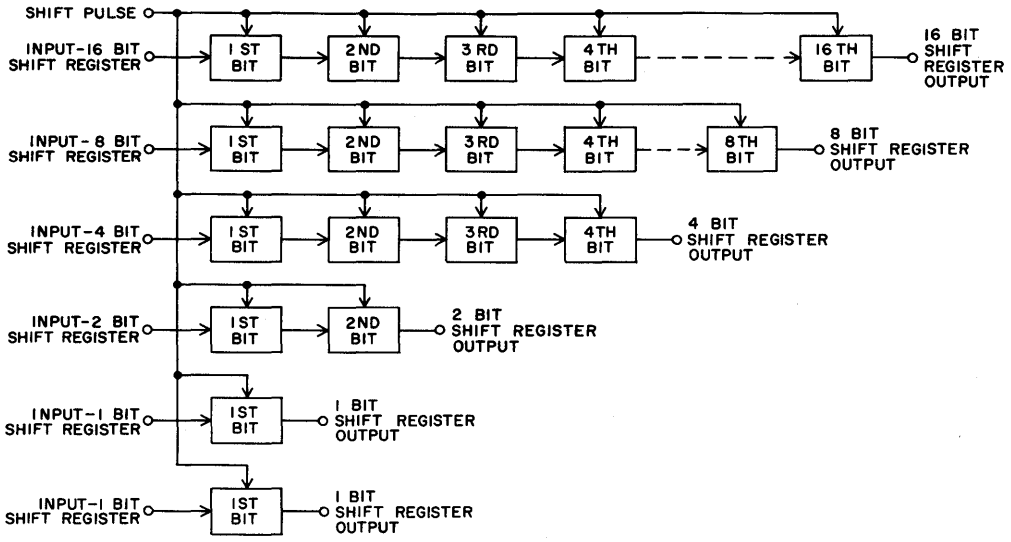
For example: Binary input word = 0101 = 5 = 5 bits of delay + one "fixed" bit of delay = 6 bits of delay at the output jack. The gating may be accomplished with standard GI logic family devices or by using the GI MEM 550 dual MTOS transistors and 10 KΩ carbon resistors connected to the V_{DD} power supply.

10-BIT BINARY COUNTER

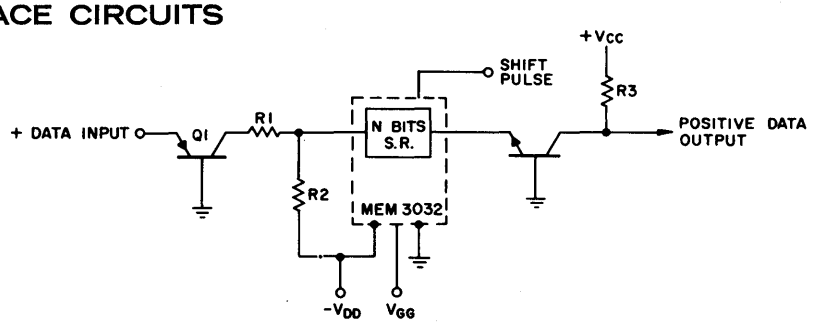


In this application, two (2) MEM 3032s are employed to form a 10 bit binary counter. A minimum of 16 external clock pulses are required at the "clock" jack to clear the counter between count cycles. During the count cycle, which is initiated by a negative ("logic 1") level applied to the "count enable" jack, the counter will count negative pulses applied to the "data in" jack. The 2 input NOR GATES could be GI MEM 1013s which are "QUAD 2-INPUT NOR GATE MTOS integrated circuits." The 2 input AND GATES could be MEM 1014s which are "QUAD 2-INPUT AND GATE MTOS integrated circuits."

FUNCTIONAL BLOCK DIAGRAM

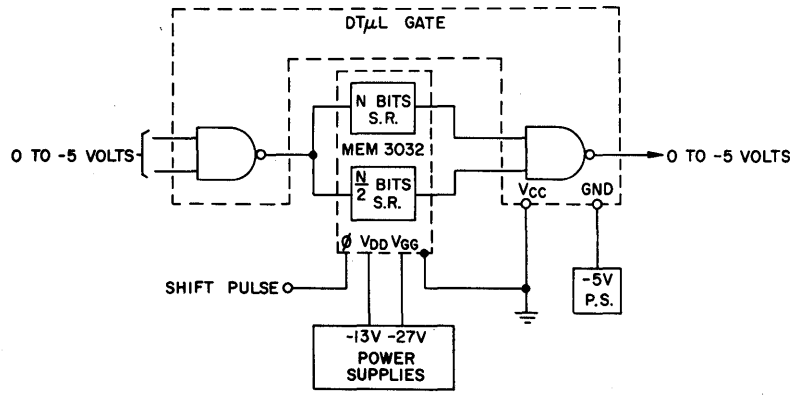


TYPICAL INTERFACE CIRCUITS



With this type of interfacing, the MEM 3032 will accept positive input data and deliver positive output data. The resistor values depend on the voltage levels used. When transistor Q1 is forward biased, the D.C. voltage at the junction of R1 and R2 should be 0 to —2 volts.

R1 protects the shift register from a positive voltage on the input which would occur if Q1 were to be shorted.



This type of arrangement requires no additional interface, and may also be used with TTL circuits. The DTμL circuit accepts negative data input and delivers negative output data.

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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

DUAL 25-BIT SHIFT REGISTER

MEM 3050

DESCRIPTION

The MEM 3050 is a dual 25-Bit dynamic shift register constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors.

MAXIMUM RATINGS

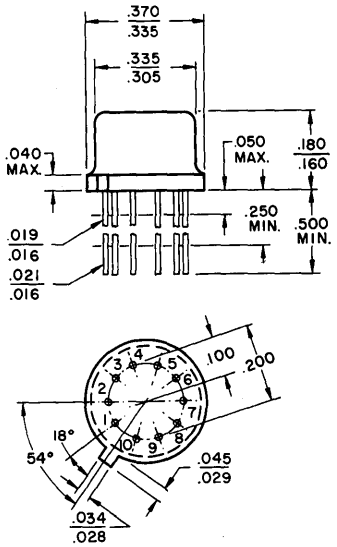
Clock Voltages ($\phi 1$ and $\phi 2$) ..... −30V to +.3V
Data Input Voltage ..... −30V to +.3V
Supply Voltage (V_s) ..... −30V to +.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified):
Load = 10MΩ and 10pF.
V_s = −27 Volts ±1 Volt, $\phi 1$ and $\phi 2$ = −27 Volts ±1 Volt.
R1 = 20KΩ, T_A = −55°C to +85°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	10	—	—	kHz	$\phi 1_{pw}$ = 45 μsec. $\phi 2_{pw}$ = 45 μsec.
Clock Repetition Rate	—	—	500	kHz	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec.
Clock Pulse Width ($\phi 1_{pw}$ and $\phi 2_{pw}$)	400	—	—	nsec.	SEE FIG. 1
Clock Delay (ϕd)	400	—	—	nsec.	SEE FIG. 1
Clock Logic Levels Logic "0" Logic "1"	 0 −26	 — —	 −0.5 −28	 Volts Volts	
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	100	nsec.	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec.
Data Input Logic Levels Logic "0" Logic "1"	 0 −11	 — —	 −2.0 —	 Volts Volts	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec.
Data Pulse Width (D_{pw})	200	—	—	nsec.	ϕd = 0.4 μsec. SEE FIG. 1
Output Logic Levels Logic "0" Logic "1"	 — −14	 — —	 −1.0 —	 Volt Volts	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec.
Output Fall time ($_{tf}$)	—	—	550	nsec.	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec. SEE FIG. 1
Fan-In	—	—	1.0		
Fan-Out	—	—	5.0		
Output Pulse Width (O_{pw})	1.0	—	—	μsec.	$\phi 1_{pw}$ = 0.4 μsec. $\phi 2_{pw}$ = 0.4 μsec. SEE FIG. 1
Output Impedance to Ground	—	—	1000	Ohms	Output a Logic "0"
Clock Input Leakage Current	—	—	100	μA	V_{in} = −26 Volts
Data Input Capacitance	—	4.0	—	pF	V_{in} = 0 Volts
Clock Input Capacitance	—	10.0	—	pF	V_{in} = 0 Volts

LOW PROFILE 10 LEAD TO-74



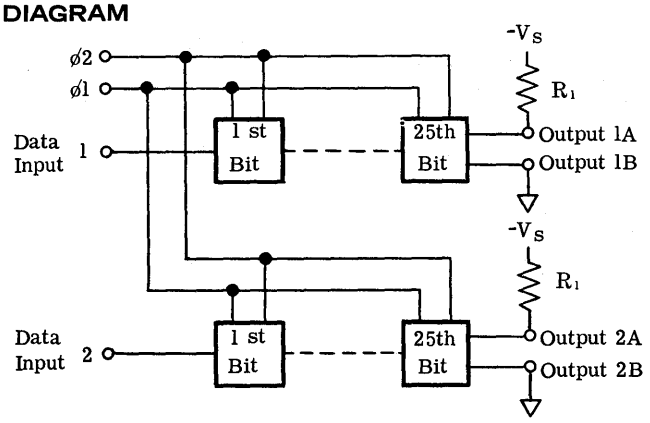
Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	Function
1	Data Input 1
2	Output 1A
3	Output 1B
4	Clock $\phi 2$
5	Ground
6	Clock $\phi 1$
7	Output 2B
8	Output 2A
9	Data Input 2
10	No Connection

DUAL 25-BIT SHIFT REGISTER MEM 3050

LOGIC DIAGRAM



NOTE: The output transistor requires an external resistor and a −12 to −27 volt power supply. When connected as shown in the logic diagram, the output of the 25th stage will be inverted with respect to its Data Input. When a non-inverted output is required, Output 1A (or 2A) can be connected to −Vs, and R_1 connected between Output 1B (or 2B) and ground. The output stage will then operate as a non-inverting source follower.

TYPICAL TIMING DIAGRAM

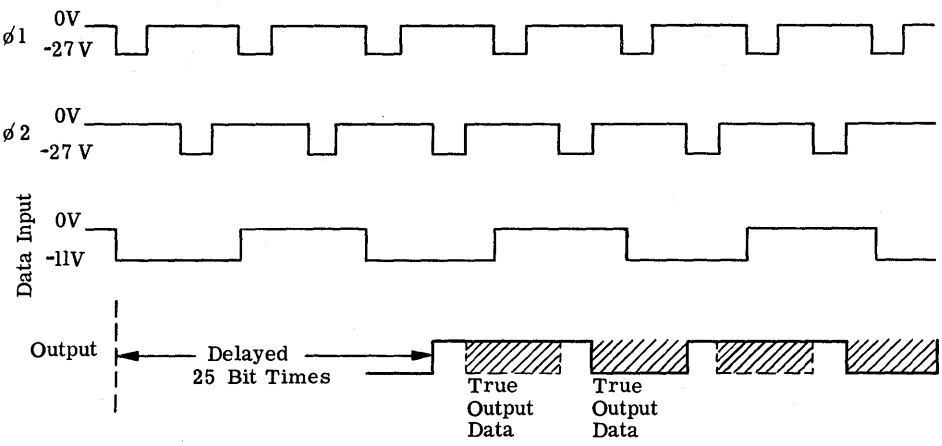
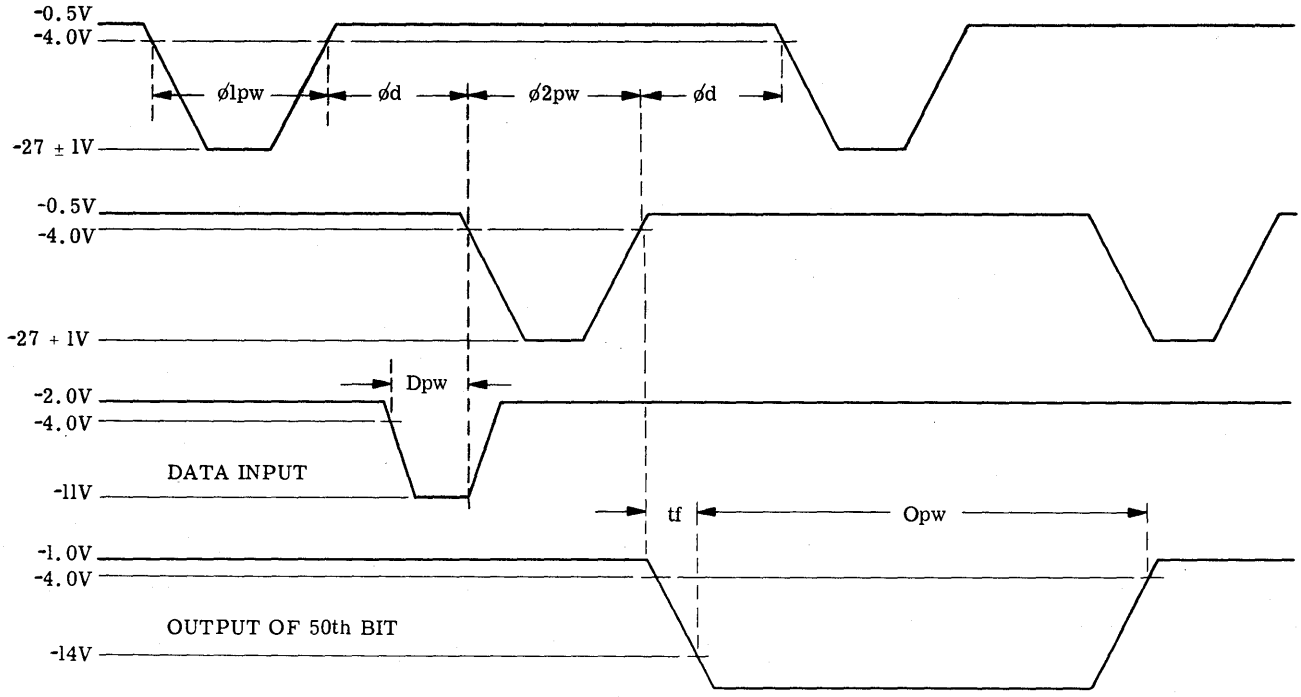


FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
DECEMBER, 1967

64-BIT SERIAL ACCUMULATOR

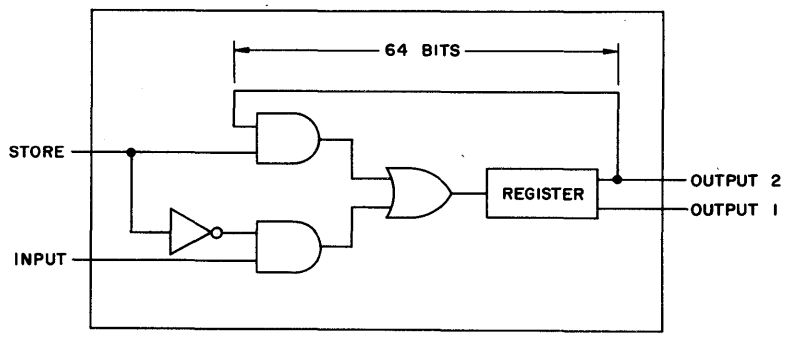
MEM 3064

DESCRIPTION

The 64-Bit Serial Accumulator consists of a 64-bit dynamic shift register plus logic for loading or recirculating information within the circuit. The device is constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-channel enhancement mode transistors.

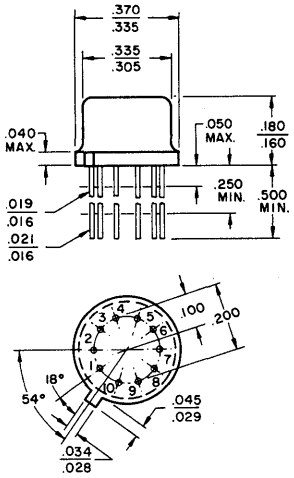
The accumulator operates at frequencies from 10 kHz to 5 MHz. Each individual stage of the register dissipates 400 μ watts during 5 MHz operation. The power dissipation of each of these stages decreases proportionally with frequency. Both data and $\overline{\text{data}}$ outputs are available, each of these output stages dissipates 24 mW at 5 MHz into a 12 picofarad load.

One accumulator circuit can drive directly into another without the addition of any external components.



LOGIC DIAGRAM

LOW PROFILE 10 LEAD TO-74

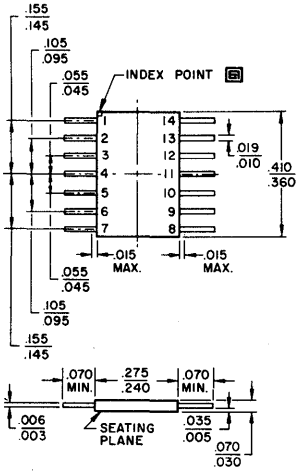


Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	FUNCTION
1	Ground
2	$\phi 3$
3	$\phi 1$
4	Store
5	No Connection
6	$\phi 2$
7	Output 2 (Data)
8	$\phi 4$
9	Input
10	Output 1 ($\overline{\text{Data}}$)

TO-87



Note: All dimensions in inches.

TERMINALS

P/N	FUNCTION
1	Ground
2	$\phi 3$
3	$\phi 1$
4	Store
5	No Connection
6	No Connection
7	No Connection
8	No Connection
9	No Connection
10	$\phi 2$
11	Output 2 (Data)
12	$\phi 4$
13	Input
14	Output 1 ($\overline{\text{Data}}$)

MAXIMUM RATINGS

Clock Voltages (ϕ_1, ϕ_2, ϕ_3, ϕ_4) ..... −30V to +0.3V
Data Input & Store Voltages ..... −30V to +0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

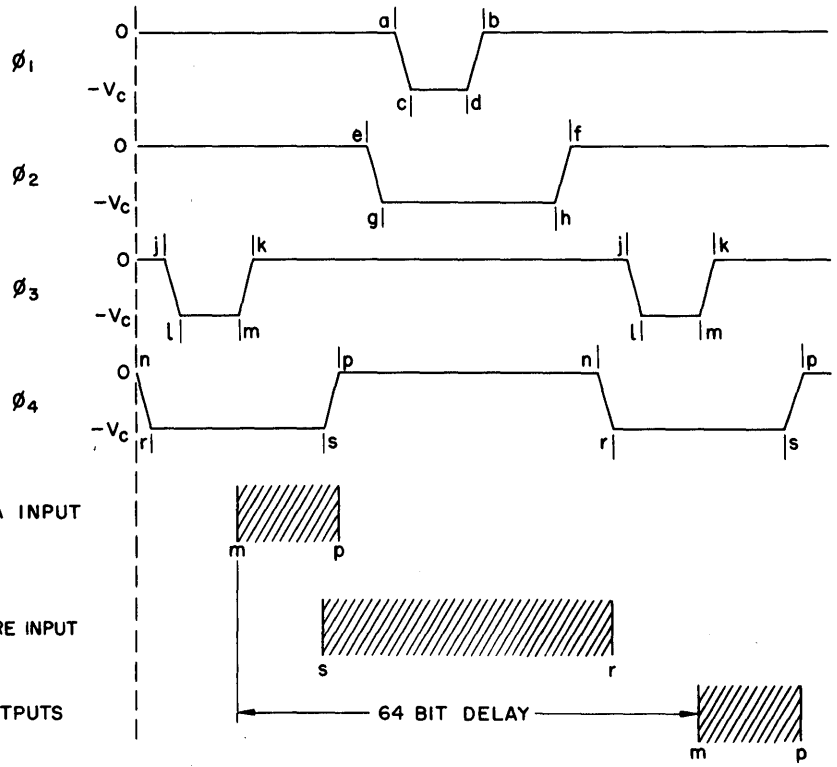
Standard Conditions (unless otherwise specified)

Load = 10MΩ and 12pF, T_A = −55°C to +85°C

Characteristic	Min	Typ	Max	Units	Conditions
Clock Repetition Rate	.01	—	5.0	MHz	
Clock Pulse Width (ϕ_1 & ϕ_3)	35	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Pulse Width (ϕ_2 & ϕ_4)	85	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Logic Levels					
Logic "0"	+0.3	—	−1.0	Volt	
Logic "1"	−24	—	−27	Volts	
Data & Store Input Logic Levels					
Logic "1"	−10	—	−24	Volts	
Logic "0"	0	—	−2.0	Volts	
Logic "0"	0	—	−4.0	Volts	$t_{ks} \leq 100$ nS SEE FIGURE 1
Data Input Pulse Width	35	—	—	nS	Stable During t_{mp} SEE FIGURE 1
Store Pulse Width	85	—	—	nS	Stable During t_{sr} SEE FIGURE 1
Clock Input Capacity					
ϕ_1, ϕ_3, ϕ_4	—	—	10	pF	
ϕ_2	—	—	10	pF	Plus Output Capacitive Load
Data & Store Input Capacity	—	—	2.0	pF	
Input Leakage To Ground (Clock Input Terminals)	—	—	100	μA	V_{IN} = −27V
Input Leakage To Ground (Data & Store Terminals)	—	—	5.0	μA	V_{IN} = −20V
Output Logic Levels*					
Logic "0"	0	—	−2.0	Volts	Stable During t_{mp} For $t_{fm} \geq 100$ nS
Logic "0"	0	—	−4.0	Volts	Stable During t_{mp} For $t_{fm} < 100$ nS
Logic "1"	−11	—	−24	Volts	

*A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

FIGURE 1.

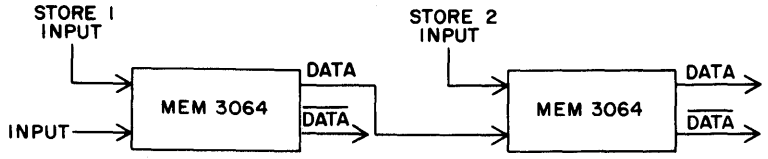


MINIMUM CLOCK REQUIREMENTS

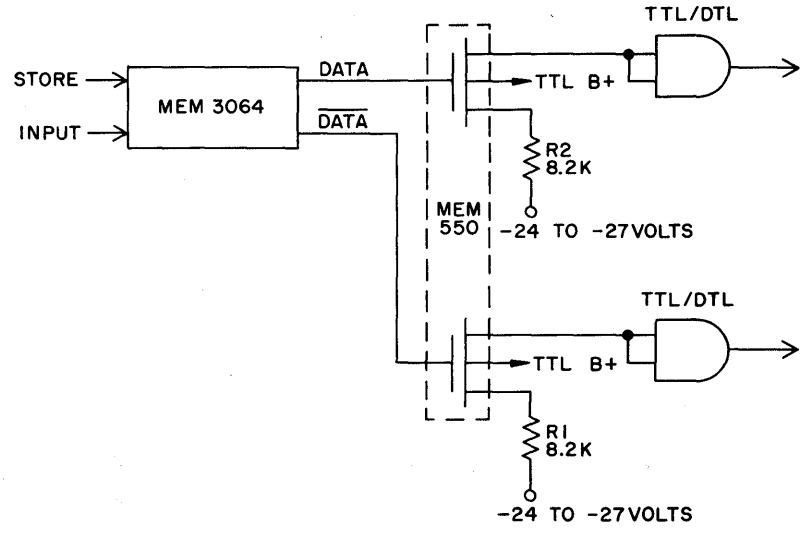
CHARACTERISTIC	SYMBOL	MINIMUM VALUE (nS)
ϕ_1 Pulse Width	t c d	35
ϕ_3 Pulse Width	t l m	35
ϕ_2 Pulse Width	t g h	85
ϕ_4 Pulse Width	t r s	85, 1 μS (Max)
Sampling Width 1	t b h	35
Sampling Width 2	t k s	35
ϕ_4—ϕ_1 Overlap	t p a	0
ϕ_2—ϕ_3 Overlap	t f j	0
ϕ_2—ϕ_4 Overlap	t f n	0, 1 μS (Max)
ϕ_4—ϕ_2 Overlap	t p e	0
ϕ_3 Precharge Time	t r m	35
ϕ_1 Precharge Time	t g d	35

Designations ϕ_1, ϕ_2, ϕ_3, ϕ_4 on this data sheet are arbitrary and may be rearranged to correspond with designations on other MTOS data sheets. The relative timing however must be maintained as shown.

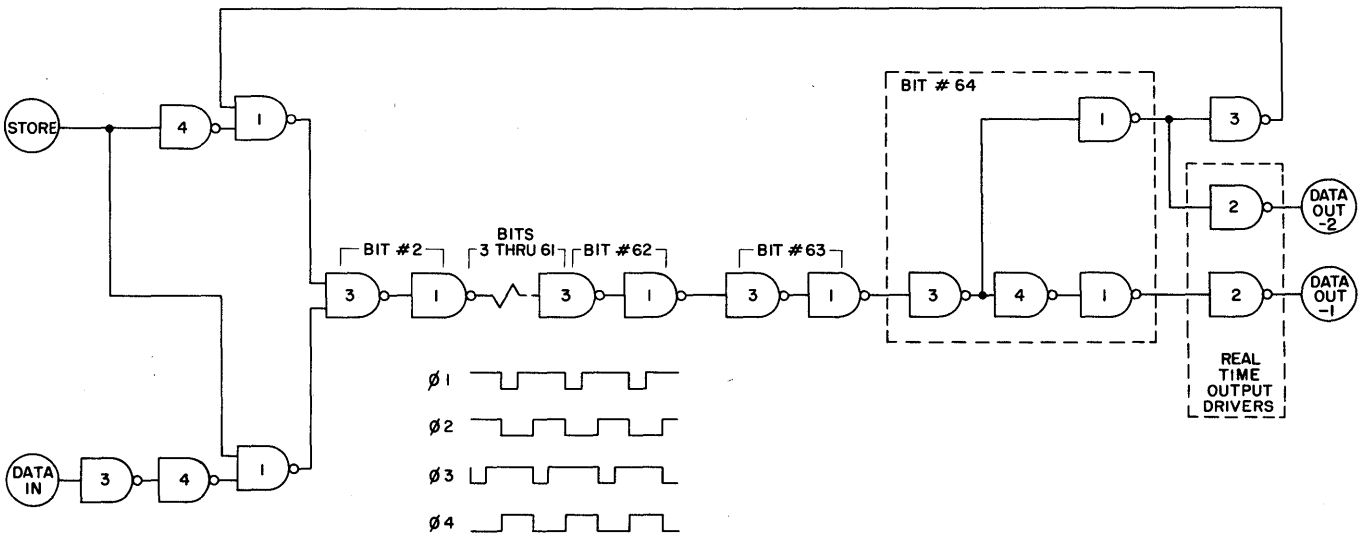
TYPICAL MEM 3064 INTERCONNECTION DIAGRAM

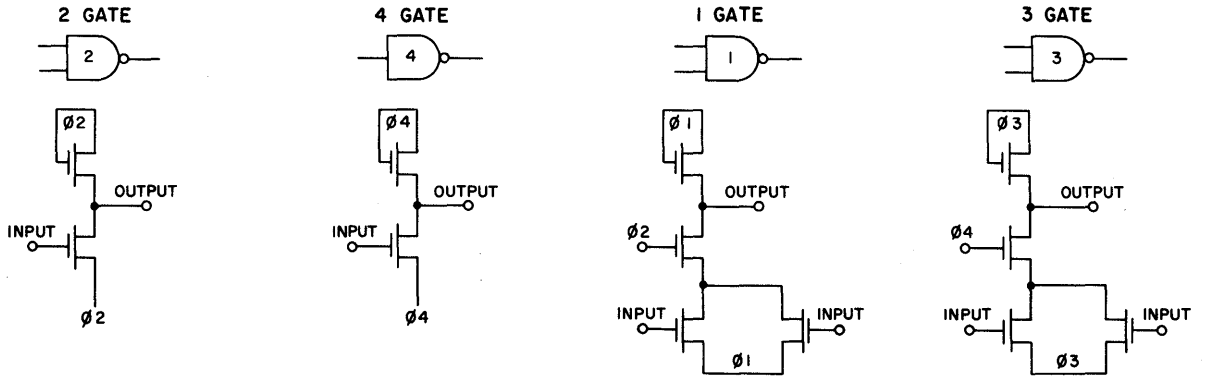


TYPICAL INTERFACE CIRCUIT



SCHEMATIC DIAGRAM MEM 3064





PRECHARGE TIME Ø2
SAMPLING TIME $\overline{Ø2}$

PRECHARGE TIME Ø4
SAMPLING TIME $\overline{Ø4}$

PRECHARGE TIME Ø1
SAMPLING TIME Ø2 $\overline{Ø1}$

PRECHARGE TIME Ø3
SAMPLING TIME Ø4 $\overline{Ø3}$

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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

PRELIMINARY

AUGUST, 1967

DUAL 50-BIT SHIFT REGISTER

MEM 3100

DUAL 50-BIT SHIFT REGISTER MEM 3100

DESCRIPTION

The MEM 3100 is a dual 50-bit dynamic shift register constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. The unit incorporates two store controls to provide the permanent and independent storage of data in each 50-bit register. The outputs are DC stable and are capable of delivering current from either device of the push-pull output.

MAXIMUM RATINGS

Clock Voltages (ϕ_1 and ϕ_2)	−30V to +0.3V
Data Input Voltage	−30V to +0.3V
Supply Voltage (V_{DD})	−30V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARATERISTICS

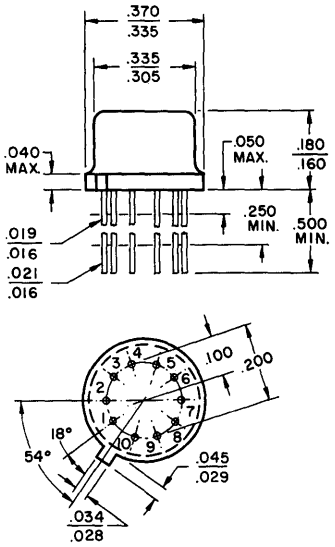
Standard Conditions (unless otherwise specified)
V_{DD} = −13 Volts ± 1 Volt, ϕ_1 and ϕ_2 = −26 Volts ± 2 Volts
LOAD = 1.0 MΩ and 10 pF, T_A = −55°C to +85°C

ELECTRICAL CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
SHIFT PULSES (See Fig. 1)					
Repetition Rate					
Lower Limit	—	10*	—	kHz	@ $\phi1_{pw}$ = $\phi2_{pw}$ = ϕd = 25μsec.
Upper Limit	—	1.0*	—	MHz	@ $\phi1_{pw}$ = $\phi2_{pw}$ = ϕd = .25μsec.
Pulse Widths					
Lower Limit					
$\phi1_{pw}$ & $\phi2_{pw}$	0.2	0.25*	—	uS	@ 1.0 MHz
Upper Limit					
$\phi1_{pw}$	1.0	25*	30	uS	@ 10 kHz
ϕ_{2pw}	1.0	25*	50	uS	@ 10 kHz
Clock Delay (ϕd)					
Lower Limit	0.2	0.25*	0.3	uS	@ 1 MHz
Upper Limit	1.0	25*		uS	@ 10 kHz
Logic Levels					
Logic "0"	+0.3	0.0	−2.0*	Volts	
Logic "1"	−24*	−26	−28*	Volts	
Input Capacitance	—	25	—	pF	V_{in} = 0 Volts
Rise and Fall Times (tr & tf)	—	—	50	nS	@ 1.0 MHz
INPUT DATA (See Figure 1)					
Pulse Width	ϕd	—	—		
Logic Levels					
Logic "0"	+0.3	0.0	−2.0*	Volts	
Logic "1"	−7.0	−10.0*	−27	Volts	
Input Capacitance	1.0	2.0	3.0	pF	V_{in} = 0 Volts
Leakage Current	—	0.1	0.5	uA	V_{in} = −12 Volts
Noise Immunity	1.0*	2.0	—	Volts	Nominal power supply voltages
STORE COMMAND					
Logic "0"	+0.3	0.0	−2.0*	Volts	Enables data input
Logic "1"	−7.0	−10.0*	−27.0	Volts	Stores data in register
OUTPUTS (See Figure 1)					
Logic "0"	(V_{SS})	−0.5	−1.0*	Volt	
Logic "1"	−10	−11*	V_{DD}	Volts	
Fall Time	—	100	—	nS	(10% to 90% points)
Rise Time	—	100	—	nS	(10% to 90% points)
Impedance	—	—	3K*	OHMS	Output a Logic "0"
Drive Capability					
Output at Logic Level "1"	−10.0*	−11.0	(V_{DD})	Volts	R_L = 25K to ground
Output at Logic Level "1"	−5.0*	−7.0	(V_{DD})	Volts	R_L = 4K to ground
POWER SUPPLY CURRENT DRAIN					
V_{DD}	—	1.0	2.0*	mA	

Correct device operation assured for the following two frequencies @ final test: 10 kHz, 1.0 MHz

*Indicates the level of performance each device must meet prior to being accepted for shipping.

LOW PROFILE 10 LEAD TO-74



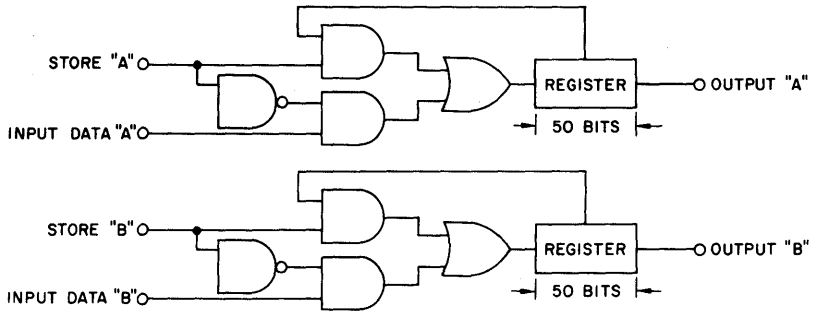
Bottom view

NOTE: All dimensions in inches

TERMINALS

P/N	Function
1	Store Command (50B)
2	V_{DD}
3	ϕ_2
4	Data Output (50B)
5	Ground
6	Data Output (50A)
7	ϕ_1
8	Store Command (50A)
9	Data Input (50A)
10	Data Input (50B)

LOGIC DIAGRAM



TYPICAL TIMING DIAGRAM

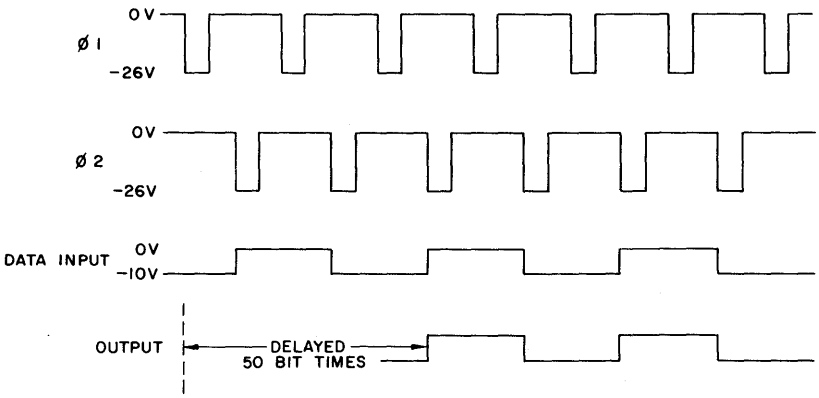
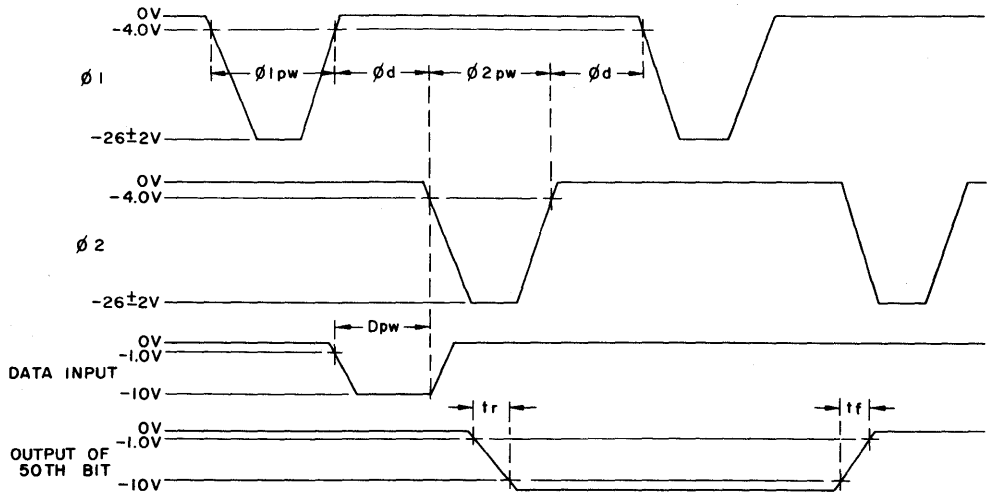


FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

ANALOG-TO-DIGITAL CONVERTER SYSTEM

S-C-100

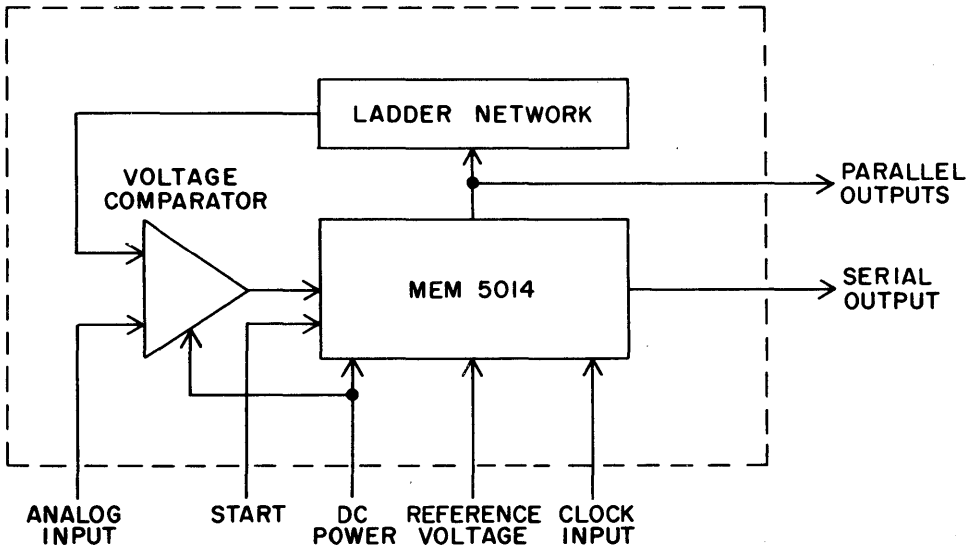
DESCRIPTION

The S-C-100 is an Analog-to-Digital Converter System containing an MEM 5014 (A/D MTOS Integrated Circuit), a precision ladder network, a voltage comparator, and several discrete components. All components are incorporated on a printed circuit plug-in board with a 29 pin connector.

The system features 8, 9 or 10 bit operation over the range 0°C to + 70°C and can deliver a serial or parallel binary output at 100 kHz bit rate. Power, clock, and reference voltage must be supplied to the basic unit, but can be included as optional features.

FEATURES

- Up to 10 Bit Operation
- 100 kHz Bit Rate
- Low Power Consumption (less than 300 mW total)
- Miniature Size
- Serial and Parallel Outputs



SIMPLIFIED BLOCK DIAGRAM
A/D CONVERTER SYSTEM

ELECTRICAL — (Temperature Range 0°C to + 70°C)

Power Requirements: −27V ± 1V @ 6 mA; +15V ± 2V @ 5 mA; −15V ± 2V @ 5 mA — Regulation 3%

V_{REF} = −5.5V to −8.8V @ 1mA

Input Logic Levels: Logic Zero = 0 to −2V; Logic One = −10V to −28V

Output Logic Levels (except parallel data): Logic Zero = 0 to −1V; Logic One = −11V to −15V

Parallel Data Output: Logic Zero = 0V; Logic One = V_{ref}

NOTE: Maximum permissable load on parallel outputs is 2.0 MΩ and 100 pF.

Clock Requirements: −11 volt pulses, 2 to 10 μS wide and at the desired bit rate

Maximum Speed (Complete 10 Bit Conversion): 10 kHz

Analog Input Range: 0 to 0.91 V_{REF} for above range of V_{REF}

Effective Input Resistance: 250 KΩ

Number of Bits: 8, 9, or 10

Accuracy: ± 1 LSB

Input Signals: Analog Input, 8 or 10 Bit Control Line, Start Pulse

Output Signals: End of Conversion, Serial Output, Parallel Output

MECHANICAL SPECIFICATIONS:

Size: 3" x 3¾" x ⅝"

Connector: 29 Pin

Sockets provided for all I.C.'s (Optional)

Weight: 3 oz.

ENVIRONMENTAL SPECIFICATIONS:

Shock: 50 g

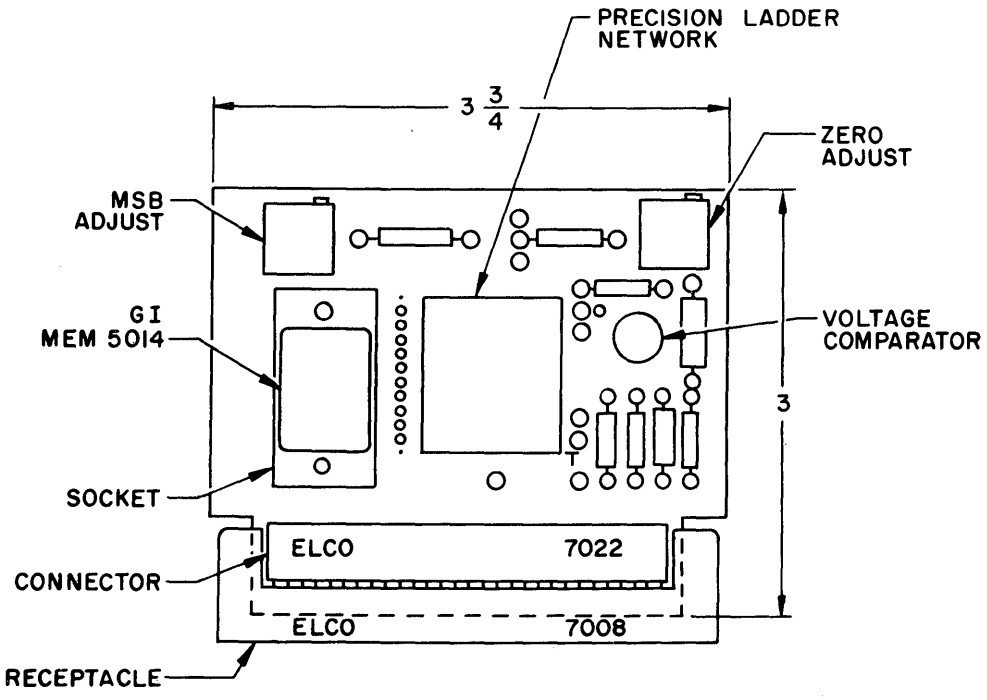
Temperature: 0° to 70°C

Humidity: 95%

AVAILABLE OPTIONS:

Digital-to-Analog Mode Operation
Low Impedance Parallel Outputs
Other Input Signal Ranges (including bi-polar)
Sample-&-Hold and Multiplexer Front Ends
Military Temperature Range
Alternate Packaging Configuration (including miniature encapsulated modules)
Clock Generator
Reference Regulator
Power Supplies

PACKAGE — 29 PIN PLUG-IN

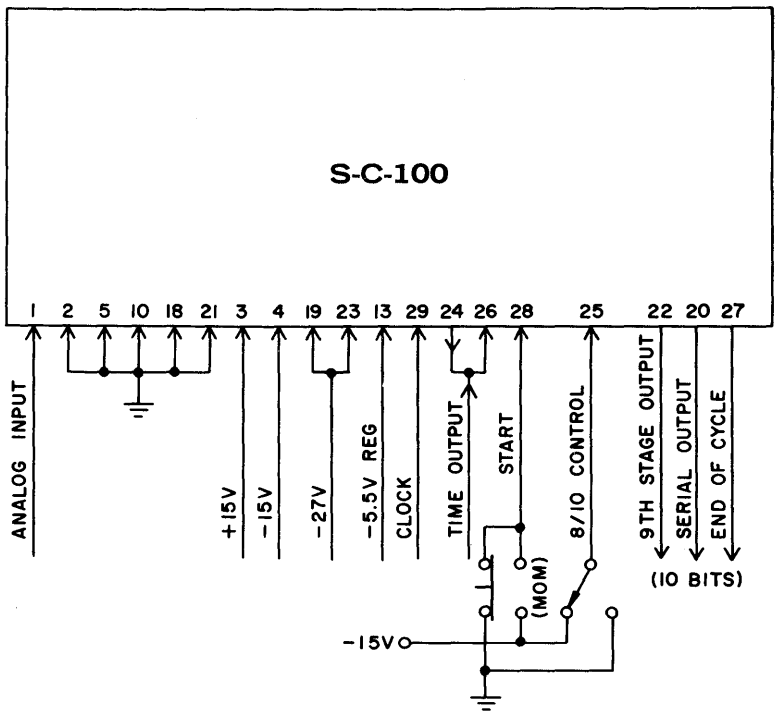


MAXIMUM HEIGHT WITH IC SOCKET: 5/8"
MAXIMUM HEIGHT WITHOUT IC SOCKET: 7/16"

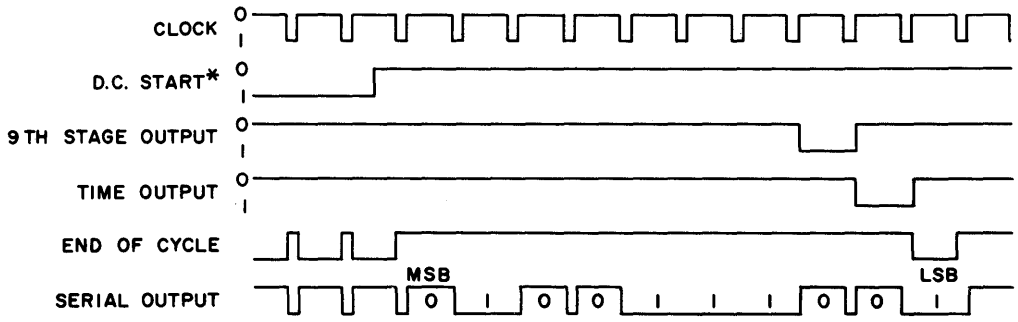
TERMINALS

PIN #	SIGNAL	PIN #	SIGNAL
1	Analog Input	16	2^1 Output
2	Input Ground	17	2^0 Output
3	+ 15V	18	Data Reset
4	— 15V	19	—27V
5	Time Register Input	20	Serial Output
6	2^9 Output	21	Digital Ground
7	2^8 Output	22	Ninth Stage Output
8	2^7 Output	23	Transfer
9	2^6 Output	24	Time Output
10	Power Ground	25	8/10 Control Line
11	2^5 Output	26	AC Start
12	2^4 Output	27	End of Cycle
13	Reference Voltage	28	DC Start
14	2^3 Output	29	Clock
15	2^2 Output		

TYPICAL CONNECTIONS



TYPICAL WAVEFORMS



*Converter will run continuously if DC START is held at ground and will always determine the MSB output on the first clock cycle after a positive transition of DC START.

For single conversion operation on external command, remove the jumper between pins 24 & 26, apply command to DC START, and ground pin 26.

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600 West John Street
Hicksville, L. I., N.Y. 11802
(516) OV 1-8000

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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
DECEMBER, 1967

RANDOM ACCESS MULTIPLEXER

MEM 5015

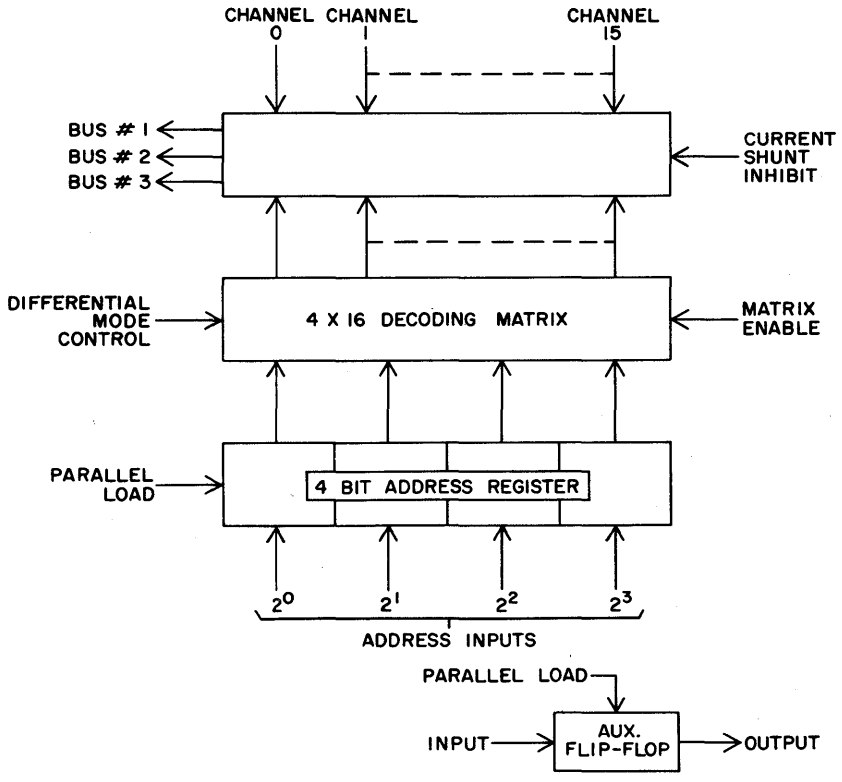
DESCRIPTION

The MEM 5015 is a Monolithic MTOS Large Scale Integrated Circuit containing 223 P-channel enhancement mode transistors operating as a 16-channel randomly addressable multiplexer. The unit consists of four address holding flip-flops, a "four-in sixteen-out" decoding matrix, 16 single-pole double-throw switches, and auxiliary logic for increased versatility.

The Current Shunt Inhibit control line permits the selection of Current Mode or Voltage Mode multiplexing, while the Differential Control allows the switches to operate as eight ganged pairs. The Matrix Enable line allows multiple MEM 5015's to be connected to form larger multiplexing arrays.

FEATURES

- Extremely High Off-Resistance
- Zener Network Protection on All Inputs
- Low Crosstalk
- Zero Offset Switches
- High Noise Immunity on Logic Inputs
- Low Power Consumption (80 mW)
- 40 Lead Plug-In Package



MEM 5015 RANDOM ACCESS MULTIPLEXER BLOCK DIAGRAM

MAXIMUM RATINGS

Input Voltages	−30V
Drain Voltage (V_{DD})	−30V
Bus Voltages (Bus 1, Bus 2, Bus 3)	−30V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

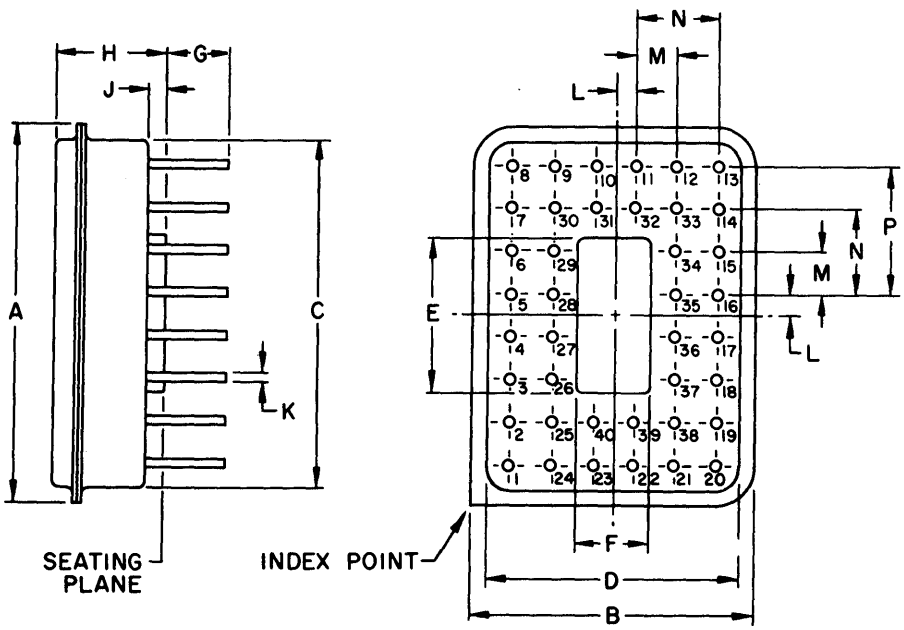
NOTE: A voltage which is more positive than 0.3 volts with respect to the ground terminal should not be applied to any pin. When it is necessary to operate with positive inputs, the ground terminal should be raised to the highest positive potential, and the V_{DD} supply reduced by the same amount.

ELECTRICAL CHARACTERISTICS

$V_{DD} = -27V \pm 1V$, $R_L = 1.0M\Omega$, $C_L = 10$ pF, $T_A = -55°C$ to $+85°C$
(unless otherwise specified)

Parameter	Min	Typ	Max	Units	Test Conditions
Logic Inputs					
Logic "0"	0	—	−2.0	Volts	
Logic "1"	−10	−12	−30	Volts	
Current Shunt Inhibit	−26	—	−30	Volts	
Parallel Load					
Amplitude	−10	−12	−30	Volts	
Width	2.0		—	μsec	
Frequency	d.c.		100	kHz	
Aux. F/F Output					
Logic "0"	0	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
R_{ON} — Series Switch (Current Mode)	800	1100	1500	Ohms	$I_{DS} = 45$ μA Bus 2 = Bus 3 = 0 Volts $T_A = 25°C$
R_{ON} — Series Switch (Voltage Mode)	1000	1200	2000	Ohms	$V_{IN} = -5V$, $R_L = 300$ kΩ $T_A = 25°C$
R_{ON} — Shunt Switch (Current Mode Only)		1500	2500	Ohms	$I_{IN} = 45$ μA Bus 1 = 0 Volts $T_A = 25°C$
R_{OFF} — All Switches		1000		MΩ	$T_A = 25°C$
Analog Input Capacitance (per channel)		15	30	pF	f = 1.0 MHz
$R_{D'ON}$ Temperature Coefficient		0.3		%/°C	
Input Leakage					
Analog Inputs		1.0	2.0	nA	$V_{IN} = -10V$ } $T_A = +25°C$
Bus 2, 3		3.0	10.0	nA	$V_{IN} = -10V$ }
Bus 1		6.0	15.0	nA	$V_{IN} = -10V$ }
Turn On Time (T_{ON})		2.0	2.5	μS	From −10 Volt Point on Parallel Load to 90% Point on Output Waveform
Power Dissipation		80		mW	$V_{DD} = -27V$
Supply Current Drain		3.0		mA	$V_{DD} = -27V$

PACKAGE — 40 LEAD PLUG-IN

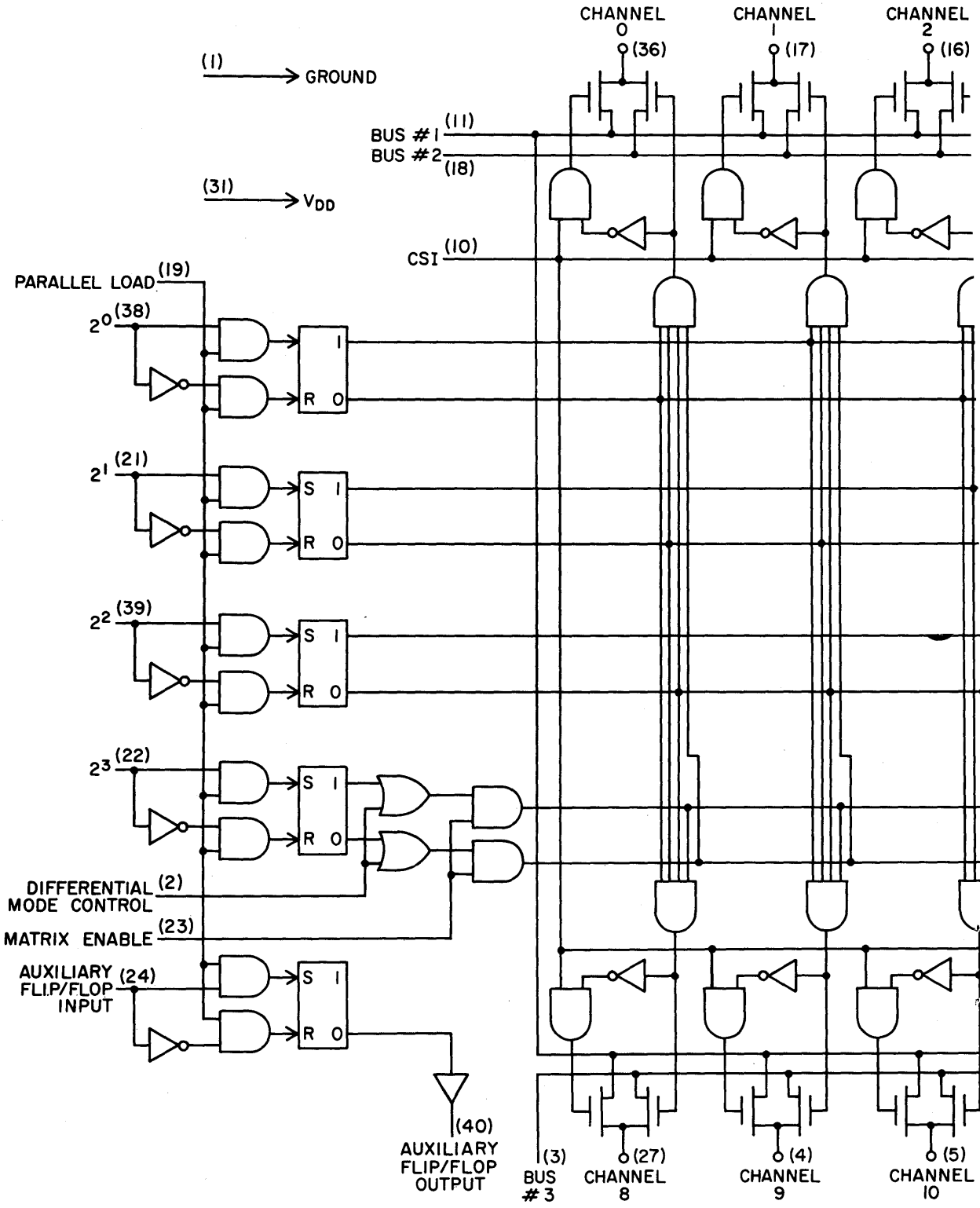


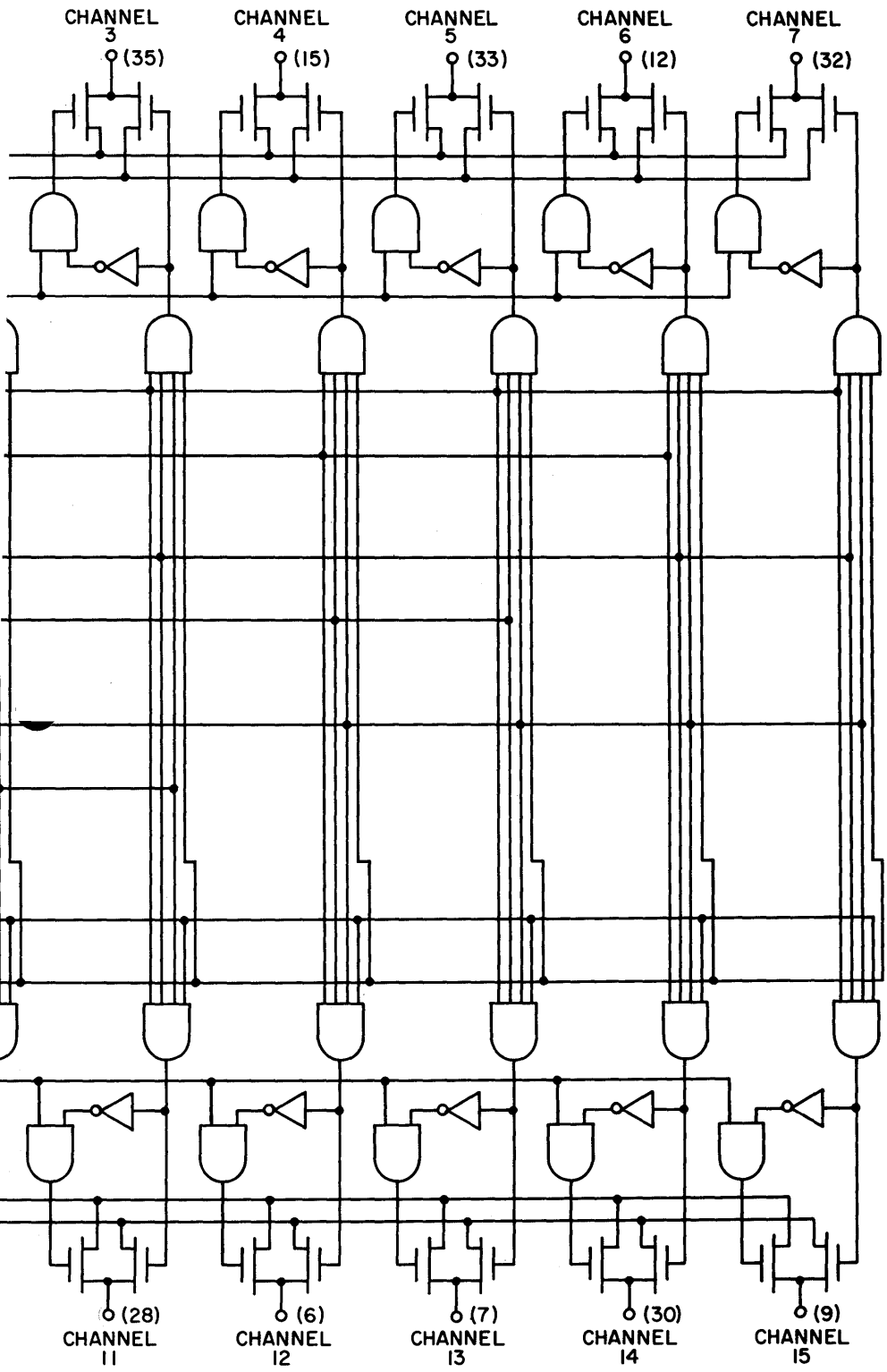
SYMBOL	INCHES	
	MIN.	MAX.
A	.880	.895
B	.685	.695
C	.812	.820
D	.609	.620
E	.365	.385
F	.175	.195
G	.125	.160
H	.264 REF.	
J	.031	.075
K	.018	.022
L	.0475	.0525
M	.095	.105
N	.195	.205
P	.295	.305

TERMINALS

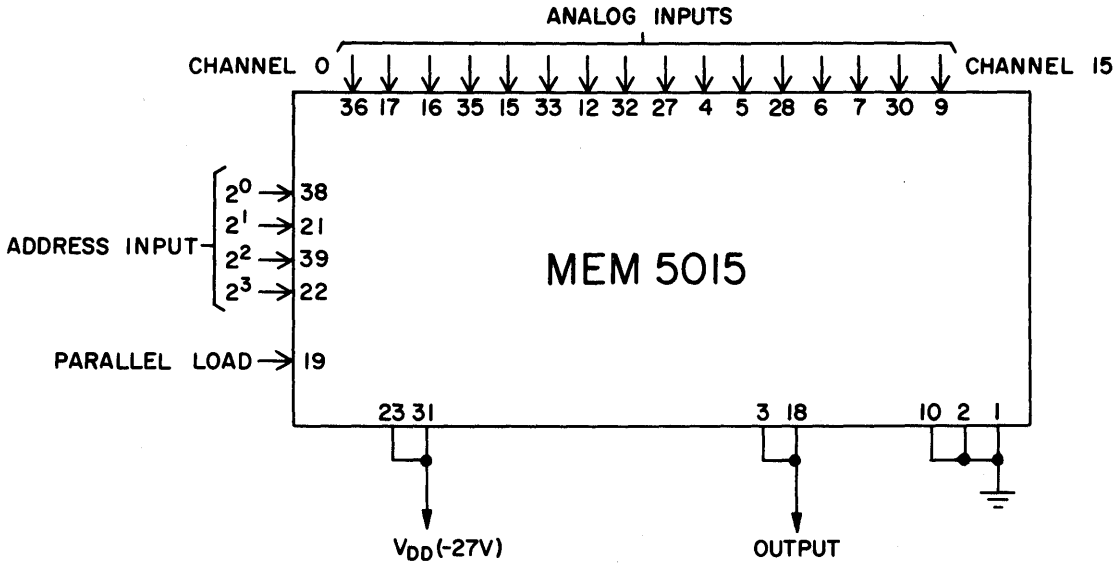
P/N	FUNCTION	P/N	FUNCTION
1	Ground	21	2^1 Input
2	Differential Mode Control	22	2^3 Input
3	Bus #3	23	Matrix Enable
4	Channel 9	24	Auxiliary Flip-Flop Input
5	Channel 10	25	No Connection
6	Channel 12	26	No Connection
7	Channel 13	27	Channel 8
8	No Connection	28	Channel 11
9	Channel 15	29	No Connection
10	Current Shunt Inhibit	30	Channel 14
11	Bus #1	31	V_{DD}
12	Channel 6	32	Channel 7
13	No Connection	33	Channel 5
14	No Connection	34	No Connection
15	Channel 4	35	Channel 3
16	Channel 2	36	Channel 0
17	Channel 1	37	No Connection
18	Bus #2	38	2^0 Input
19	Parallel Load	39	2^2 Input
20	No Connection	40	Auxiliary Flip-Flop Output

LOGIC DIAGRAM




CHANNEL 3
(35)
CHANNEL 4
(15)
CHANNEL 5
(33)
CHANNEL 6
(12)
CHANNEL 7
(32)
(28)
CHANNEL 11
(6)
CHANNEL 12
(7)
CHANNEL 13
(30)
CHANNEL 14
(9)
CHANNEL 15

TYPICAL CONNECTIONS, VOLTAGE MODE



VOLTAGE MODE OPERATION

To multiplex in the voltage mode, pin 10 is connected to ground. A four bit address is placed on the Address Input lines and the Parallel Load is pulsed. The MTOSFET switch corresponding to the binary address will close connecting the signal on that channel to the common bus (Bus #2 or Bus #3). See Logic Diagram for the arrangement of buses. Bus #2 and Bus #3 may be connected together forming one common output terminal. The address will remain stored and the switch will remain closed until a new address is strobed into the address register.

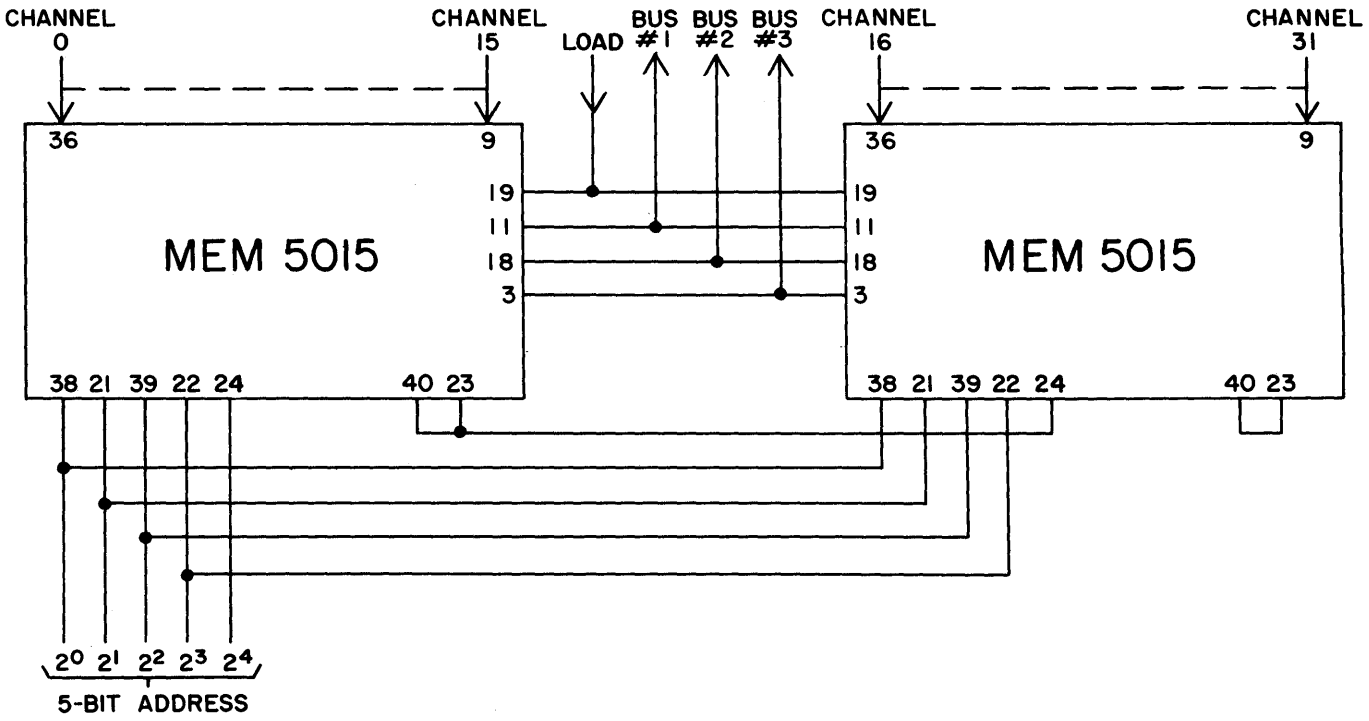
CURRENT MODE OPERATION

To multiplex in the current mode, pin 10 is connected to V_{DD}. Operation is similar to Voltage Mode Multiplexing with the exception that all 15 unselected input channels are connected to Bus #1, which can be used as a current return.

DIFFERENTIAL MODE OPERATION

By connecting pin number 2 (DIFFERENTIAL MODE CONTROL) to the logic "1" level, the MEM 5015 can be made to operate in the Differential Mode. In this mode, the contribution of the 2^3 input is removed from the decoding matrix, so that pairs of channels (1 and 9, 2 and 10, 3 and 11, etc.) are activated simultaneously. The Differential Mode may be used in either Current Mode, or Voltage Mode operation. Note that each pair consists of a Bus #2 switch and a Bus #3 switch permitting isolation of the two signals when both switches are closed.

FIGURE 1: INTERCONNECTION FOR 32-CHANNEL OPERATION



AUXILIARY FLIP-FLOP

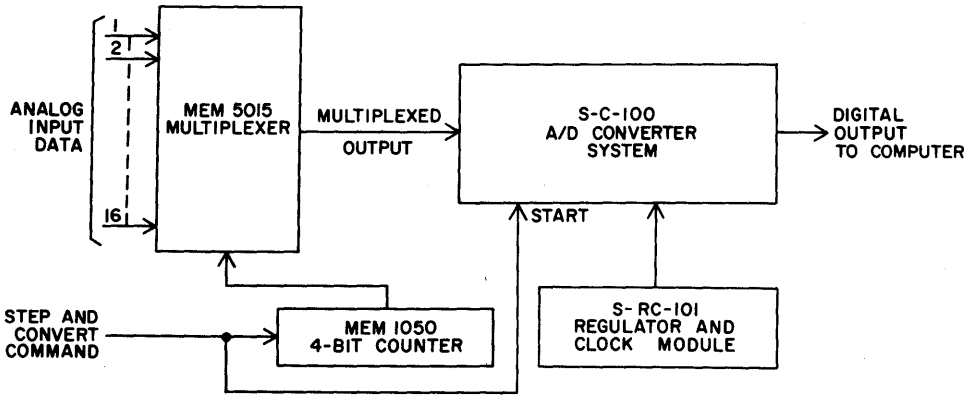
The Auxiliary Flip-Flop stores the data presented to it at pin number 24, the Auxiliary Flip-Flop Input. Loading of information is under the control of the Parallel Load command, pin number 19. The output of the Auxiliary Flip-Flop (pin number 40) is the inverse of the data entered. The Auxiliary Flip-Flop is used to store additional address bits when several MEM 5015's are used in systems with more than 16 channels.

MATRIX ENABLE AND EXPANDED MODE OPERATION

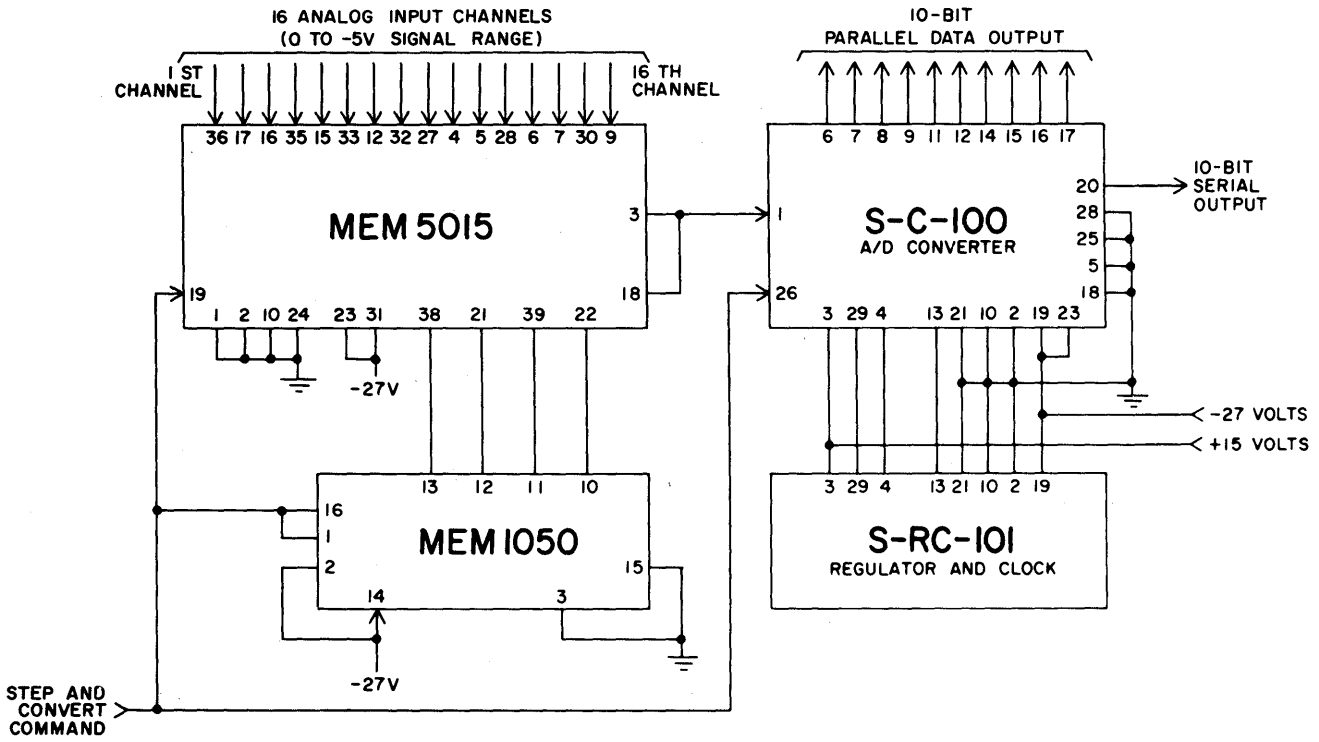
The decoding matrix in the MEM 5015 is activated by connecting the MATRIX ENABLE line, pin number 23, to a logic "1". It is, therefore, possible to expand the operation to 32 channels by using two MEM 5015's and activating one MATRIX ENABLE line at a time. Figure 1 shows how the two units are interconnected for this purpose.

Any number of MEM 5015's can be operated in parallel when the correct MATRIX ENABLE input signals are provided for each module.

A SIXTEEN CHANNEL SEQUENTIAL SCAN MULTIPLEXER AND ANALOG-TO-DIGITAL CONVERTER SYSTEM USING MTOS COMPONENTS.



BLOCK DIAGRAM



INTERCONNECTION DIAGRAM

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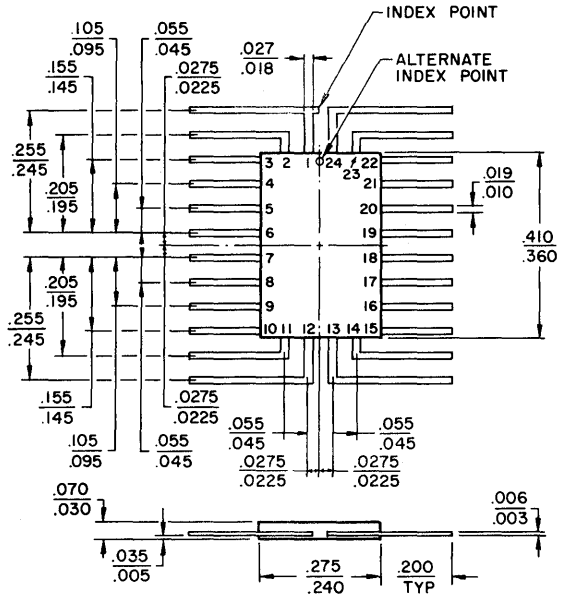
GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
MARCH, 1967

DIGITAL DIFFERENTIAL ADDER ELEMENT

MEM 5021

24 LEAD FLAT PACK



Note: All dimensions in inches.

DESCRIPTION

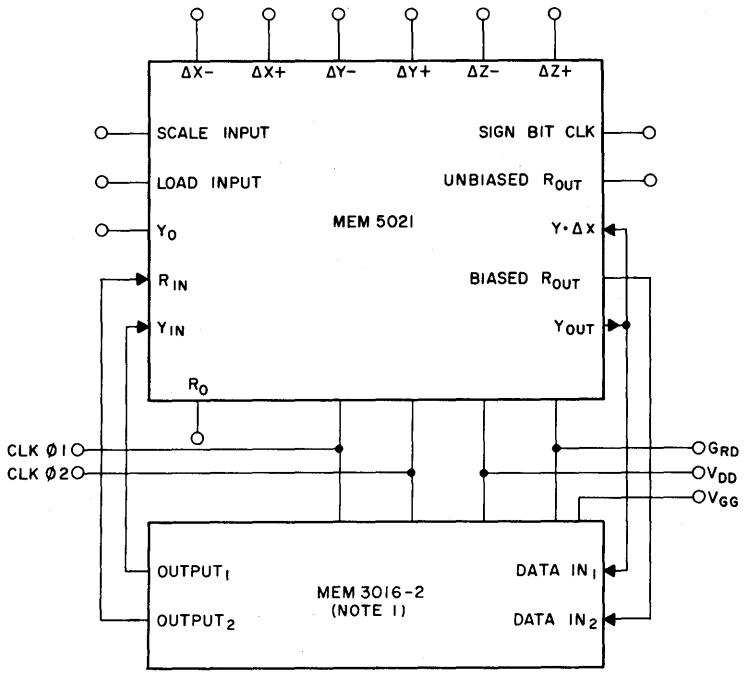
The MEM 5021 is a Digital Differential Analyzer Adder Element constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. This element when used in conjunction with a dual shift register forms a complete Digital Differential Analyzer Integrator (DDA) of ternary type. The DDA is designed to be used in parallel operation and performs rectangular integration. The DDA integrator can be used in a variety of control system applications or to solve any differential equation.

The function diagram shows the adder element connected to a dual shift register in the standard configuration. The overflow and underflow outputs ($\Delta z+$ and $\Delta z-$) and internal carry are stored in d.c. flip flops so that the unit may be operated to d.c. For d.c. operation, ϕ_1 must be a Logic "0" (ground) and ϕ_2 must be a Logic "1" (negative). The timing diagram shows the relative timing of the clocks to the outputs. Note that ϕ_1 and ϕ_2 must not be negative at the same time. The numbers in the shift registers are serial, least significant bit (LSB) first, sign bit last; negative numbers are in 2's complement form. The scaling is accomplished for each integrator by inserting a single "one" into the scale input at the time of the LSB of that number. For detailed information about scaling, inserting initial conditions, and biased and unbiased roundoff error consult the General Instrument application note entitled "MTOS Integrated Digital Differential Analyzer".

TERMINALS

P/N	FUNCTION
1	$Y\Delta x$ Input
2	Y Adder Output (Y_{out})
3	Ground
4	Initial Conditions Input (Y_o)
5	Initial Conditions Load Input
6	Y Adder Input (Y_{in})
7	Scale Input
8	Y Adder Subtract Input ($\Delta y-$)
9	Y Adder Add Input ($\Delta y+$)
10	Sign Bit Clock
11	Overflow Output ($\Delta z+$)
12	No Connection
13	No Connection
14	Clock (ϕ_2)
15	Clock (ϕ_1)
16	Underflow Output ($\Delta z-$)
17	Initial Conditions Input (R_o)
18	Biased R Adder Output (R_{out})
19	Unbiased R Adder Output (R_{out})
20	No Connection
21	Drain Voltage ($-V_{DD}$)
22	R Adder Input (R_{in})
23	R Adder Subtract Input ($\Delta x-$)
24	R Adder Add Input ($\Delta x+$)

FUNCTION DIAGRAM



NOTE 1: The MEM 3016-2 is a dual 16 bit, d.c. to 1 Mc, shift register.

FEATURES

- Parallel, ternary integrator usable with any length shift register
- Arbitrary scaling
- Initial conditions easily inserted
- Biased or unbiased R remainder
- Adders are separate and can be used independently
- $\Sigma\Delta y$ is possible using additional elements
- Inputs protected against static damage

MAXIMUM RATINGS

Clock Voltages (ϕ_1 and ϕ_2)	−30V to +0.3V
Input Voltages	−30V to +0.3V
Drain Voltage (V_{DD})	−20V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

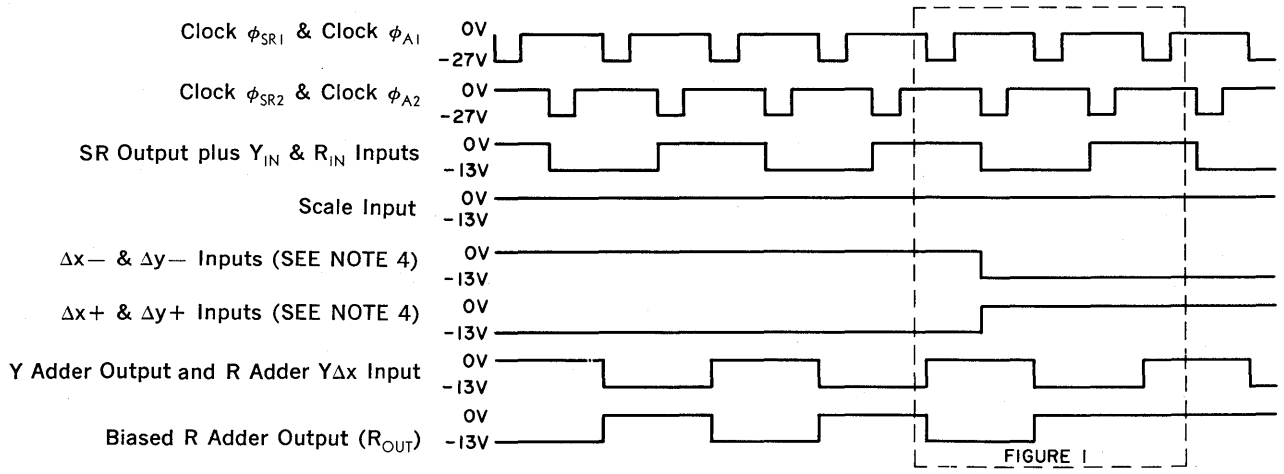
Standard Conditions (unless otherwise specified)
Load = 1.0MΩ and 10pF, $\phi_1 = \phi_2 = -27$ Volts ±1 Volt
$V_{DD} = -13$ Volts ±1 Volt, $T_A = -55°C$ to $+85°C$

Characteristic	Min	Typ	Max	Units	Conditions
Clock Repetition Rate	dc	—	500	kHz	
Clock Pulse Widths					
ϕ_{pw1}	0.9	—	10	μS	SEE FIG. 1
ϕ_{pw2}	0.9	—	—	μS	SEE FIG. 1
Clock Delay (ϕ_d)	0.1	—	—	μS	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	0.1	μS	
Clock Pulse Logic Levels (ϕ_1 and ϕ_2)					
Logic "0"	—	—	−2.0	V	
Logic "1"	−26	—	−28	V	
Clock Pulse Input Capacitance	—	20	—	pF	$\phi_1 = \phi_2 = 0V$
Clock Input Current (ϕ_2)	—	—	100	μA	$\phi_1 = 0V$, $\phi_2 = -26V$
Clock Input Current (ϕ_1)	—	1.8	2.5	mA	$\phi_1 = -26V$, $\phi_2 = 0V$
Input Logic Levels					
Logic "0"	—	—	−2.0	V	
Logic "1"	−10	—	—	V	
Input Pulse Width	0.9	—	—	μS	
Input Capacitance	—	3.0	—	pF	$V_{in} = 0V$
Input Leakage Current	—	—	1.0	μA	$V_{in} = -20V$
Output Logic Levels					
Logic "0"	—	−0.5	−1.0	V	
Logic "1"	−11	−12	—	V	
Propagation Delay plus Rise & Fall Time					
T_{pdyr1}, T_{pdyr2} See Note 2	—	500	750	nS	SEE FIG. 1
T_{pdy1}, T_{pdy2} See Note 3	—	250	400	nS	SEE FIG. 1
Noise Immunity	1.0	—	—	V	dc to 500 kHz
Output Impedance to Ground (Output at Logic "0")	—	—	3500	Ohms	
Output Drive Capability (Output at Logic "1")	−10	−11	—	V	$R_L = 20$ K Ohms
Output Drive Capability (Output at Logic "1")	−5.0	—	—	V	$R_L = 10$ K Ohms
Supply Current Drain	—	—	6.0	mA	f = 500 kHz

NOTE 2: T_{pdyr1} and T_{pdyr2} represent the total propagation delay plus rise and fall times through the R Adder (biased output which is the worst case) and the Y Adder in series.

NOTE 3: T_{pdy1} and T_{pdy2} represent the propagation delay plus rise and fall times of the Y Adder only.

TYPICAL TIMING DIAGRAM

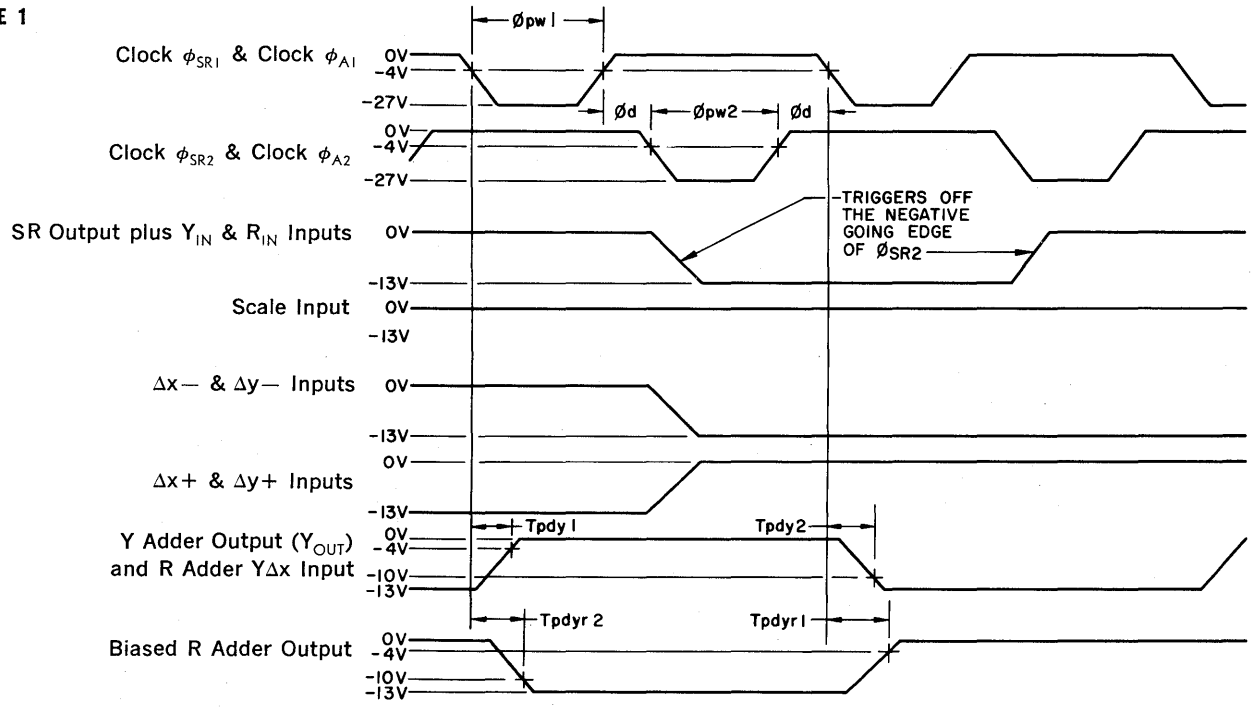


NOTE 4: The Δx and Δy input waveforms are shown changing state on the negative going edge of the DDA clock ϕ_{A2}. These same waveforms are also representative of when the overflow (Δz) and underflow (Δz—) outputs of the DDA change state.

DEFINITIONS:

ϕ_{SR1} — Clock ϕ_1 Of Shift Register
ϕ_{SR2} — Clock ϕ_2 Of Shift Register
ϕ_{A1} — Clock ϕ_1 Of Adder Element
ϕ_{A2} — Clock ϕ_2 Of Adder Element

FIGURE 1



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

SERVO ADDER

ADVANCE
DECEMBER, 1967

MEM 5031

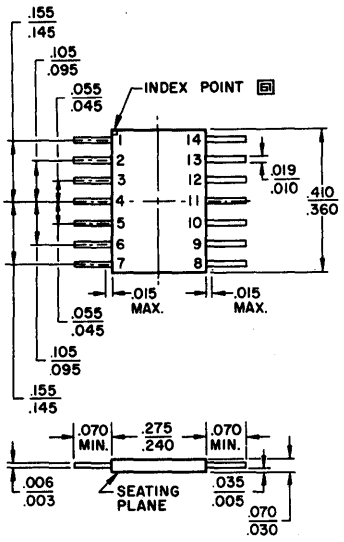
DESCRIPTION

The MEM 5031 is a static logic element which serially examines a shift register and determines whether the contents are greater than, equal to, or less than zero. The unit is constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-Channel enhancement mode transistors.

The information in the register should be organized least significant bit first, sign bit last. There are two push-pull outputs, designated "positive" and "negative." With the $\Delta X +$ input a logic "1" and the content of the register positive, the "positive" output shall indicate a logic "1" during the entire next word time. The "negative" output shall indicate a logic "1" for a negative content. For a content of zero, both outputs shall indicate a logic "0." Two ΔX inputs control whether or not the input number is examined at all. If $\Delta X +$ is a logic "1", a positive number shall indicate positive. If $\Delta X -$ is a logical "1", a positive number shall indicate negative and a negative number shall indicate positive. If both ΔX inputs are a logic "0", any number shall indicate zero (i.e., it is not examined). The unit is designed to be used in conjunction with an MEM 5021 for solving differential equations.

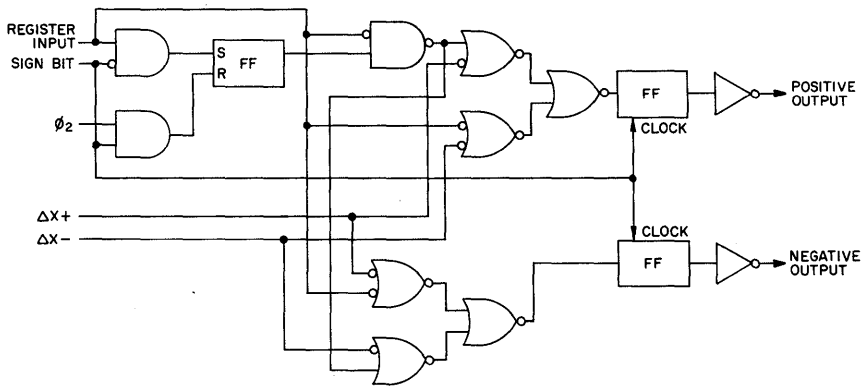
In order to obtain d.c. stability at low frequencies, it is necessary that the $\phi 1$ clock be a logic "0" and the $\phi 2$ clock be a logic "1." Note that it is important that the $\phi 1$ and $\phi 2$ clocks are not at a logic "1" simultaneously.

TO-87



Note: All dimensions in inches.

LOGIC DIAGRAM



TERMINALS

P/N	FUNCTION
1	Negative Output
2	V_{GG}
3	V_{DD}
4	Positive Output
5	Ground
6	$\Delta X-$
7	Register Input
8	No Connection
9	Ground
10	No Connection
11	Sign bit
12	Clock $\phi 1$
13	$\Delta X+$
14	Clock $\phi 2$

MEM 5031

MAXIMUM RATINGS

Clock Voltages ($\phi 1$ and $\phi 2$)	−30V to + 0.3V
Input Voltages	−30V to + 0.3V
Drain Voltage ($-V_{DD}$)	−30V to + 0.3V
Gate Voltage ($-V_{GG}$)	−30V to + 0.3V
Storage Temperature	−55°C to + 150°C
Operating Temperature	−55°C to + 85°C

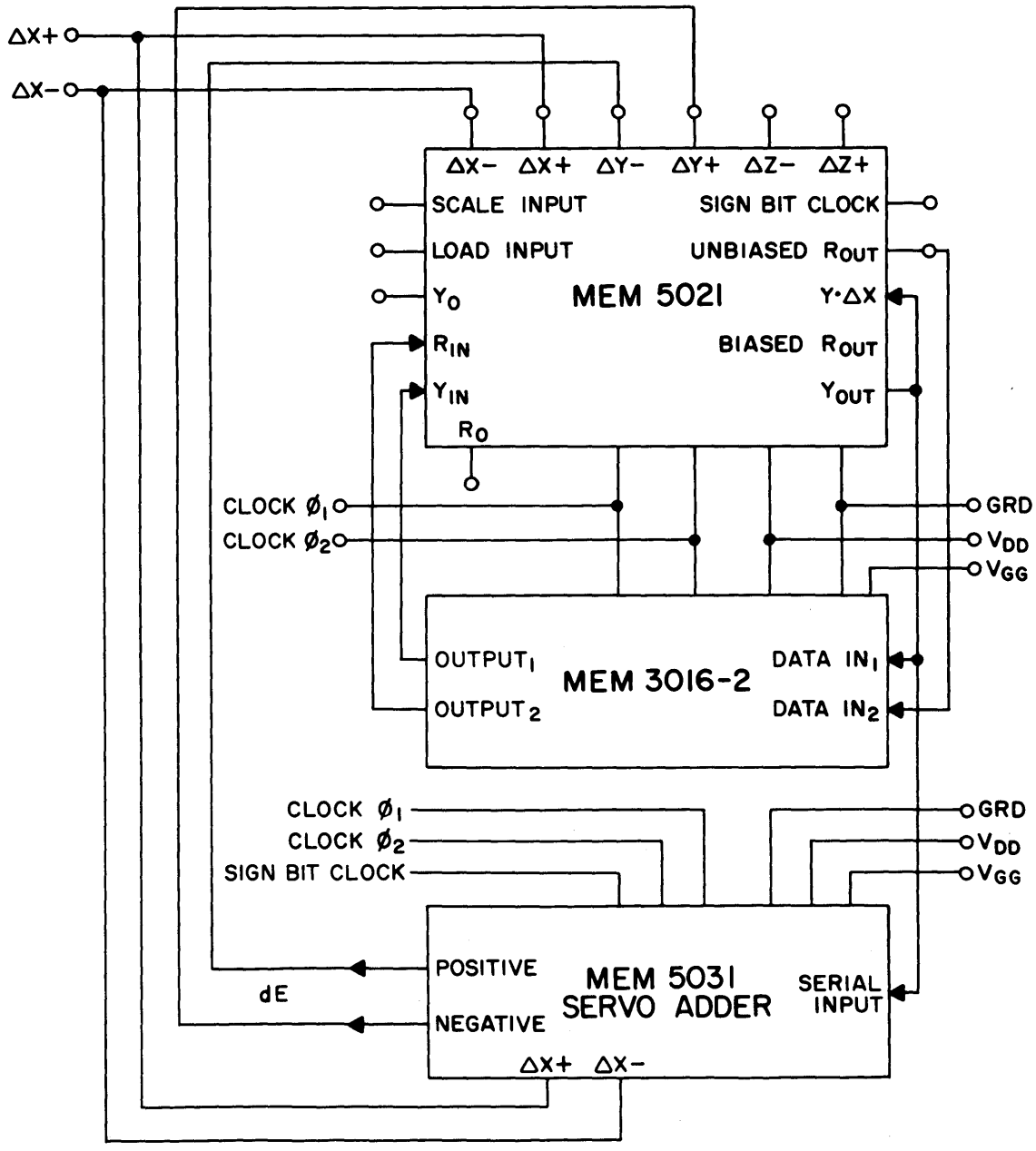
ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
$V_{DD} = -13V \pm 1$ Volt, $V_{GG} = -27V \pm 1$ Volt, Load = 1.0 MΩ and 10 pF, $T_A = -55°C$ to + 85°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	COND.
Clock Rep. Rate	d.c.	—	1.0	MHz	
Clock Pulse Widths					
$\phi 1$ pw	0.4	—	10	μS	SEE FIG. 1
$\phi 2$ pw	0.4	—	—	μS	SEE FIG. 1
Clock Pulse, Rise & Fall time 10% - 90%	—	—	4.0	μS	
Clock Pulse Logic levels ($\phi 1$, $\phi 2$)					
Logic "0"	+0.3	—	−2.0	Volts	
Logic "1"	−26	—	−28	Volts	
Clock Pulse Input Capacitance ($\phi 1$, $\phi 2$)	—	2.0	3.0	pF	
Data Input Capacitance	—	2.0	3.0	pF	Vin = 0 Volts
Data Input Logic Levels					
Logic "0"	+0.3	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Input Pulse Width	0.9	—	—	μS	
Data Input Capacitance	—	3.0	—	pF	Vin = 0 Volts
Input Leakage Current	—	—	1.0	μA	Vin = −20 Volts
Output Logic Levels					
Logic "0"	—	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
Propagation Delay Plus Rise and Fall Time					
Tpd_1	—	120	400	nS	SEE NOTE 1
Tpd_2	—	120	400	nS	SEE NOTE 2
Noise Immunity	1.0	—	—	Volt	d.c. to 1.0 MHz
Output Impedance to Grd.	—	—	3.5	KΩ	at Logic "0"
Output Drive Capability	−10	−11	—	Volts	$R_L = 75$ KΩ, $V_{DD} = -13V$
(Logic "1")	−5	—	—	Volts	$R_L = 10$ KΩ, $V_{DD} = -13V$
Supply Current Drain	—	1.5	2.0	mA	f = 1.0 MHz

NOTE 1. Tpd_1 represents the total propagation delay plus rise time of both outputs.
NOTE 2. Tpd_2 represents the total propagation delay plus fall time of both outputs.

FUNCTION DIAGRAM



TYPICAL TIMING DIAGRAM

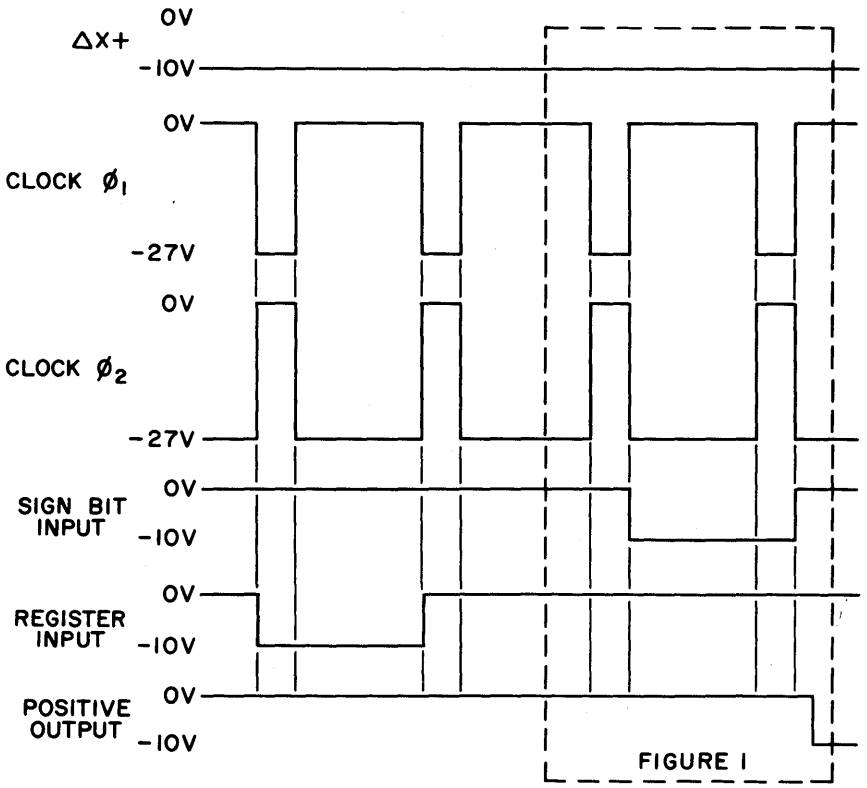
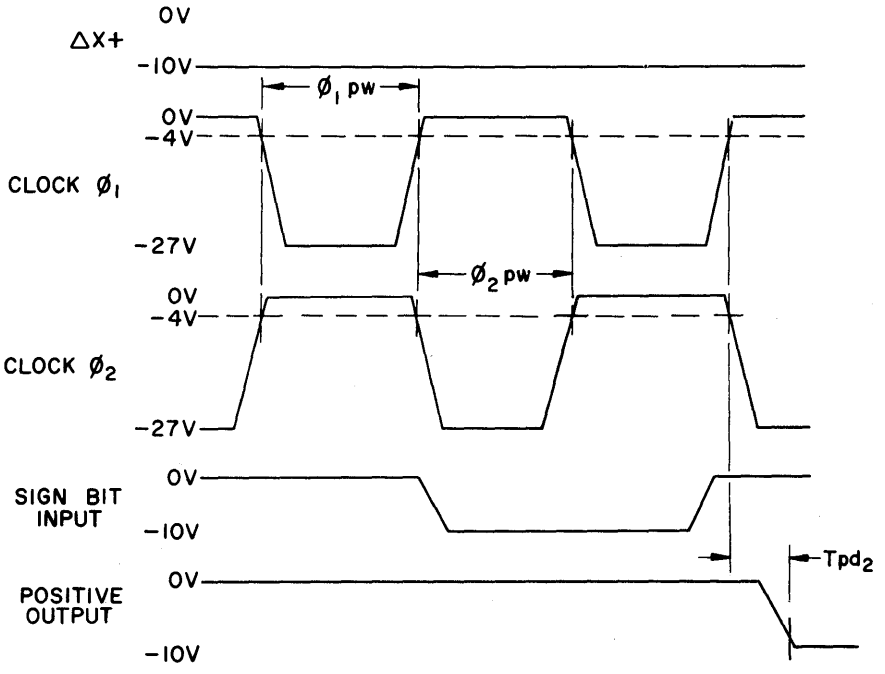


FIGURE 1



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GENERAL INSTRUMENT

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MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

16 CHANNEL RANDOM/SEQUENTIAL ACCESS MULTIPLEXER

MEM 5116

DESCRIPTION

The MEM 5116 is a 16 Channel Random/Sequential Access Multiplexer module containing a programmable counter and decoder, and a 16 channel multiplexer. The device is constructed on a single monolithic chip utilizing MTOS (metal-thick-oxide-silicon) P-channel enhancement mode transistors.
Due to the nature of the programmable counter and decoder, various combinations of the module can be utilized to expand to any number of channels.

FEATURES:

- High "off" resistance
- Zener input protection
- Low leakage to summing junction
- Low crosstalk
- Random sequential modes of addressing
- Sync. output establishes channel 1 ref.
- Low power consumption
- 40 lead plug-in package
- Low "on" resistance

MAXIMUM RATINGS:

Input Voltages ..... −30V to +0.3V
Drain Voltage (V_{DD}) ..... −30V to +0.3V
Storage Temp. ..... −55°C to +150°C
Operating Temp. ..... −55°C to +85°C

NOTE: A voltage which is greater than 0.3 volts positive with respect to the ground terminal should not be applied to any pin. Where it is necessary to operate with positive inputs, the ground terminal should be raised to the highest positive potential, and the V_{DD} supply reduced by the same amount.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
$V_{DD} = -27V \pm 1V$, $R_L = 300K$, $C_L = 10pF$, $T_A = -55°C$ to $+85°C$

Characteristics	Min.	Typ.	Max.	Units	Test Conditions
Clock Repetition Rate	d.c.	—	500	kHz	
Logic "0"	0	—	−2.0	Volts	
Logic "1"	−10	−12	−28	Volts	
Pulse Width	1.0	—	10	μS	
Clock Input Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Preset and Sync. Inputs					
Logic Levels					
Logic "0"	0	—	−2.0	Volts	
Logic "1"	−10	−12	−28	Volts	
Sync. Pulse Width	2.0	—	—	μS	
Input Leakage Current	—	—	5.0	μA	$V_{in} = -20$ Volts
Sync. Output					
Logic "0"	0	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
Output Impedance to Ground	—	3000	5000	Ohms	Output a Logic "0"
R_D (on)	1000	1500	2000	Ohms	$V_{in} = -5.0V$, $R_L = 300K$
R off per switch	—	1000	—	MΩ	$V_{in} = -5.0V$, $T_A = +25°C$
Analog input capacitance (per channel)	—	15	—	pF	Freq. = 1.0 MHz
R_D (on) temperature coefficient	—	0.3	—	%/°C	
Analog input leakage	—	800	—	pA	$V_{in} = -5.0V$, $T_A = +25°C$
Analog output leakage	—	10	—	nA	$V_{OUT} = -5.0V$, $T_A = +25°C$
Turn on time (T_{ON}) (Sequential Mode)	—	1	—	μS	from −10V point on count pulse to 90% point on output waveform
Turn on time (T_{ON}) (Random Mode)	—	0.5	—	μS	from −10V point on parallel load pulse to 90% on output waveform
Power dissipation	—	108	—	mW	$V_{DD} = -27V$
Supply current drain	—	4	—	mA	$V_{DD} = -27V$

FIGURE 1: BLOCK DIAGRAM 16 CHANNEL RANDOM/ SEQUENTIAL ACCESS MULTIPLEXER

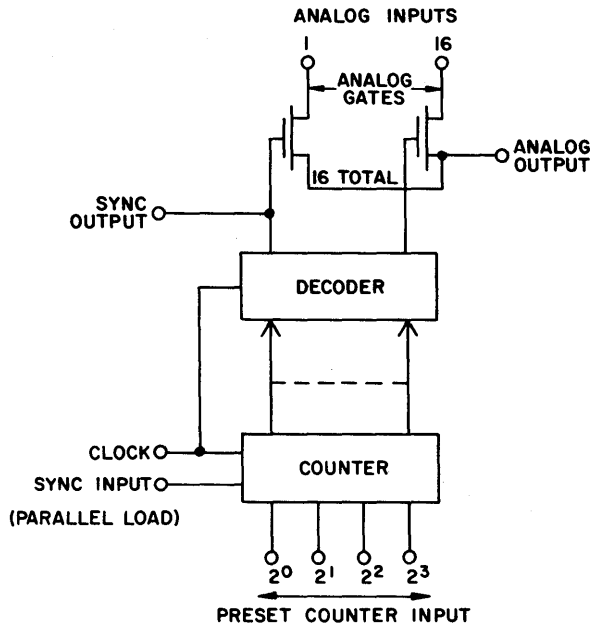


FIGURE 2: TYPICAL CONNECTION FOR MEM 5116

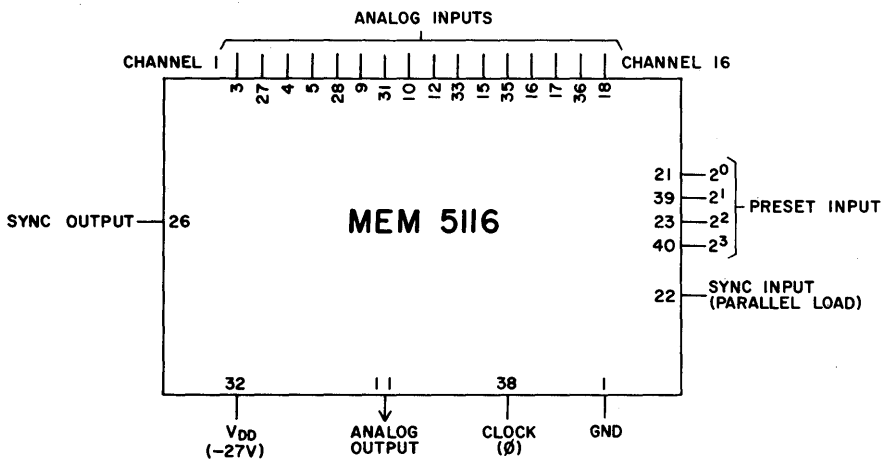
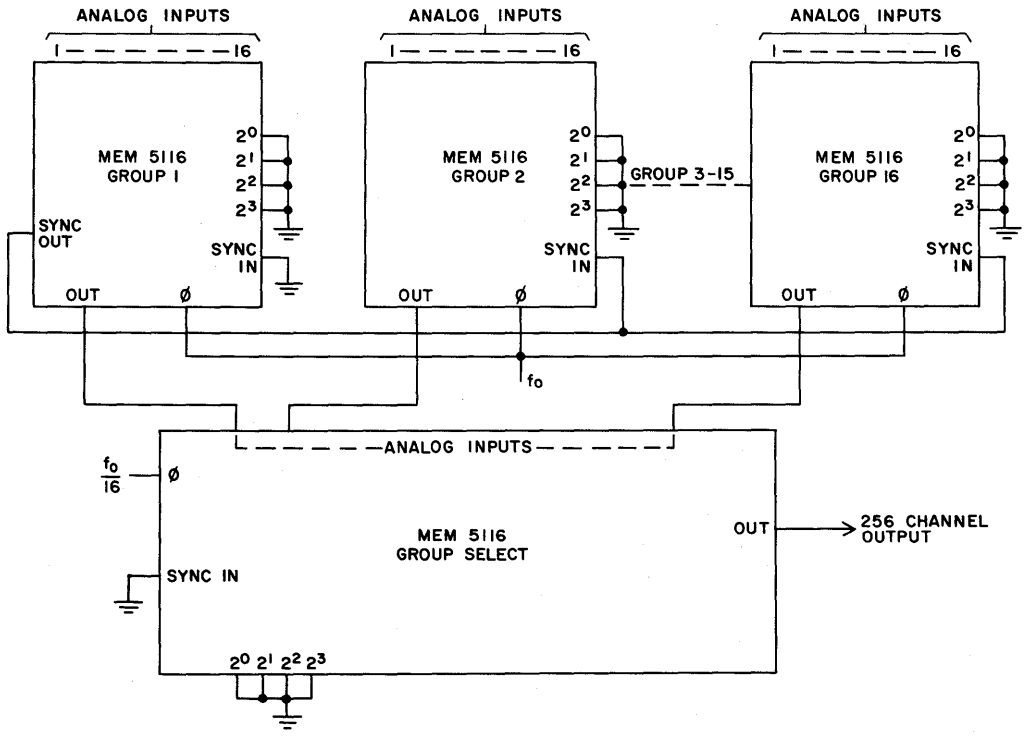
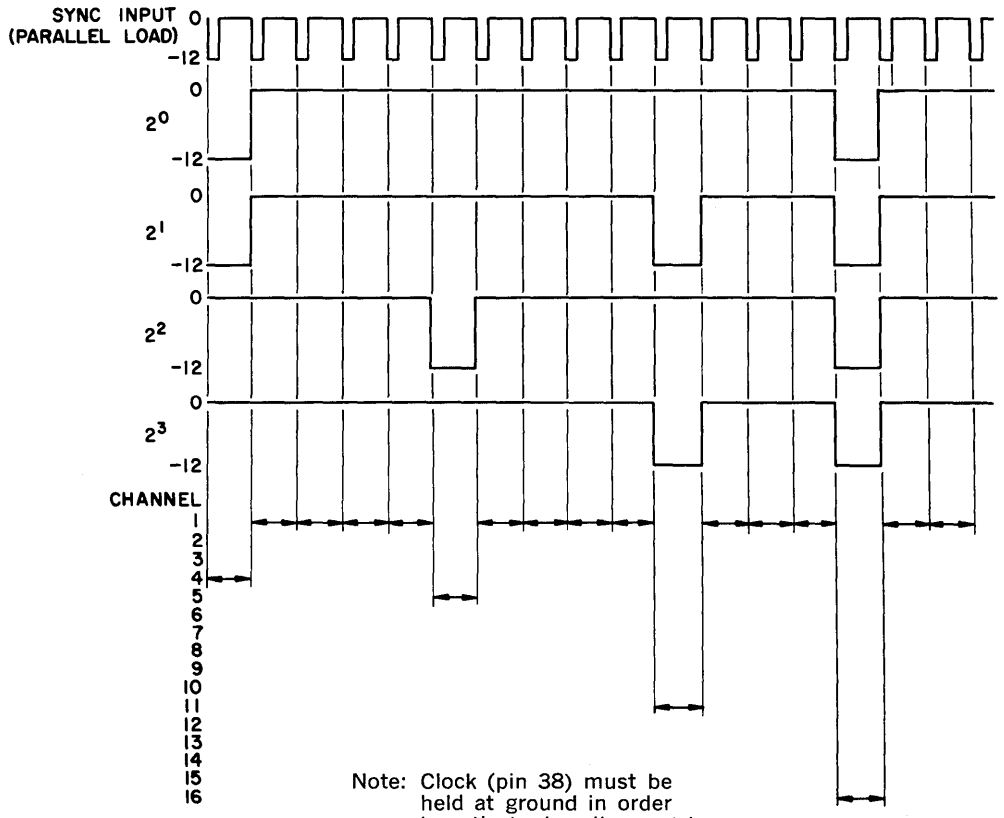


FIGURE 3: INTERCONNECTION FOR 256 CHANNEL OPERATION



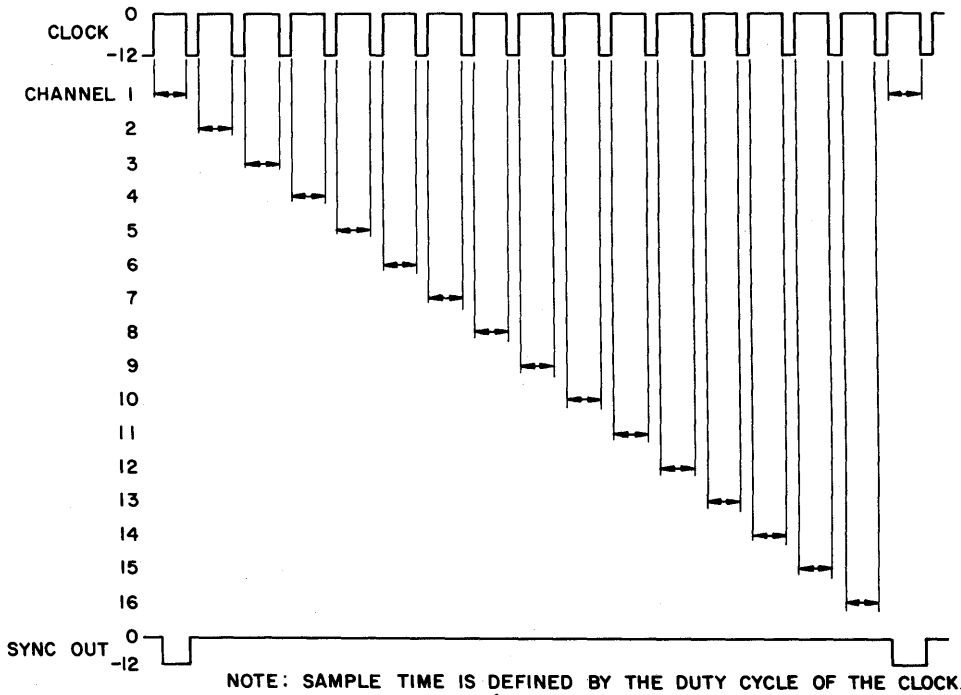
Expanded Mode Operation — The MEM 5116 can be connected to accommodate any number of channels. By enabling Groups 2 through 16 from the Sync Output of Group 1 and tying all Preset lines to ground, all Groups count synchronously. The output of each group is then coupled to the Analog Input of a Group Select.

RANDOM ACCESS MODE OPERATION



Note: Clock (pin 38) must be held at ground in order to activate decoding matrix

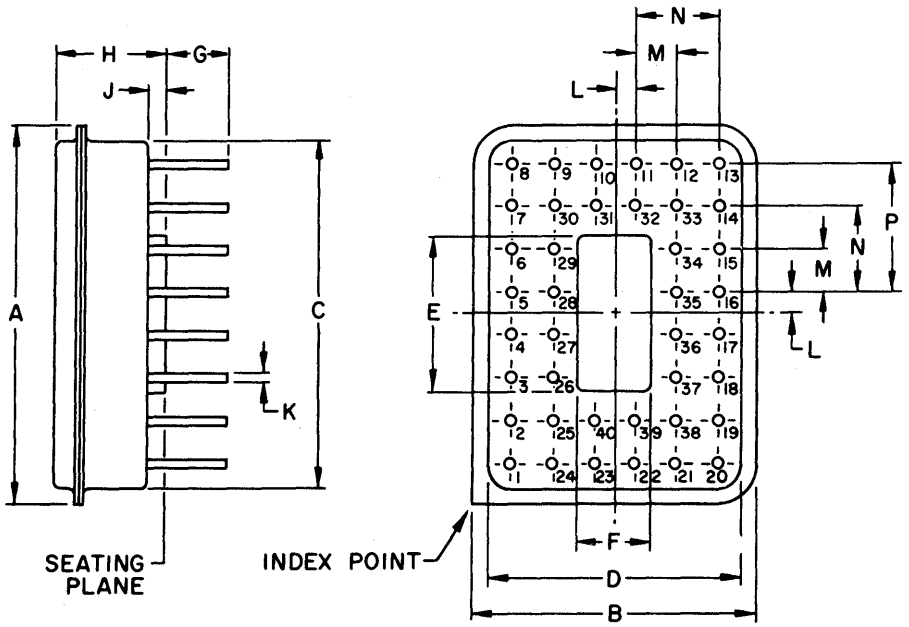
SEQUENTIAL MODE OPERATION



NOTE: SAMPLE TIME IS DEFINED BY THE DUTY CYCLE OF THE CLOCK.

$$\text{SAMPLE TIME} = \frac{1}{\text{CLOCK FREQ}} - \text{CLOCK PULSE WIDTH.}$$

PACKAGE — 40 LEAD PLUG-IN



BOTTOM VIEW

SYMBOL	INCHES	
	MIN.	MAX.
A	.880	.895
B	.685	.695
C	.812	.820
D	.609	.620
E	.365	.385
F	.175	.195
G	.125	.160
H	.264 REF.	
J	.031	.075
K	.018	.022
L	.0475	.0525
M	.095	.105
N	.195	.205
P	.295	.305

TERMINALS

P/N	FUNCTION	P/N	FUNCTION	P/N	FUNCTION
1	Ground	14	No Connection	28	A_5
2	No Connection	15	A_{11}	29	No Connection
3	A_1	16	A_{13}	30	No Connection
4	A_3	17	A_{14}	31	A_7
5	A_4	18	A_{16}	32	V_{DD}
6	No Connection	19	No Connection	33	A_{10}
7	No Connection	20	No Connection	34	No Connection
8	No Connection	21	Preset 2^0	35	A_{12}
9	A_6	22	Sync. Input	36	A_{15}
10	A_8	23	Preset 2^2	37	No Connection
11	Analog Output	24	No Connection	38	Clock
12	A_9	25	No Connection	39	Preset 2^1
13	No Connection	26	Sync. Output	40	Preset 2^3
		27	A_2		

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RANDOM ACCESS MEMORY CELL

PRELIMINARY
JULY, 1967

MEM 5132

New

GENERAL DESCRIPTION:

The GI MEM 5132 is a 32-bit random access memory cell designed for both large and small memory system applications. The monolithic circuit contains 32 DC storage flip-flops and address decoding for reading and writing. It is intended for use in medium and large arrays as a scratch-pad memory and as a replacement for core memory systems. Upon application of the correct binary address and strobe pulse, any one bit word may be updated or read out on the corresponding data in or out terminals.

The word length may be expanded to any arbitrary number by adding additional MEM 5132's. The number of bits per word corresponds to the number of additional memory cells. When the corresponding address and strobe wires are tied together and activated, an entire word may be updated or read out in parallel.

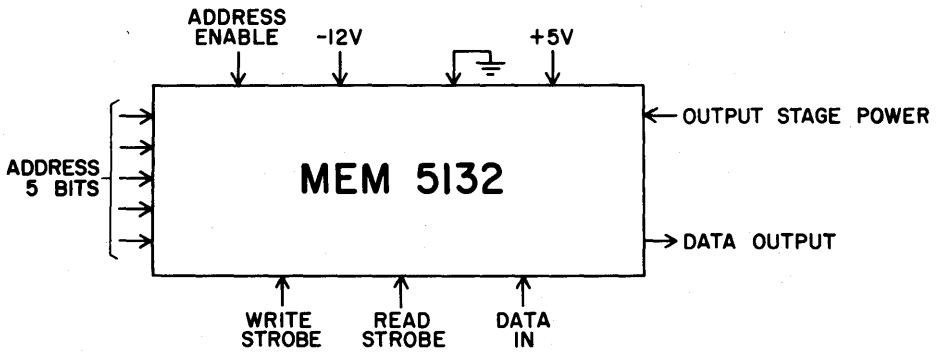
FEATURES:

- Directly Interfaceable with TTL or DTL
- Low Power
- High Speed
- Non-Destructive Readout
- Small Size — 14 Lead Flatpack
- High Noise Immunity
- High Input Impedance
- Cell Expander Input
- Full Temperature Range (−55°C to +85°C)

TYPICAL ELECTRICAL CHARACTERISTICS (−55°C to +85°C)

Supply Voltage	−12V and +5V
Power	60 mW
Cycle Time	500 nS
Logic Levels	"0" = OV "1" = +5V
Noise Immunity	1 V
"0" Level Output Current Sink	1.6mA

BLOCK DIAGRAM



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GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
OCTOBER, 1967

64-BIT SERIAL ACCUMULATOR

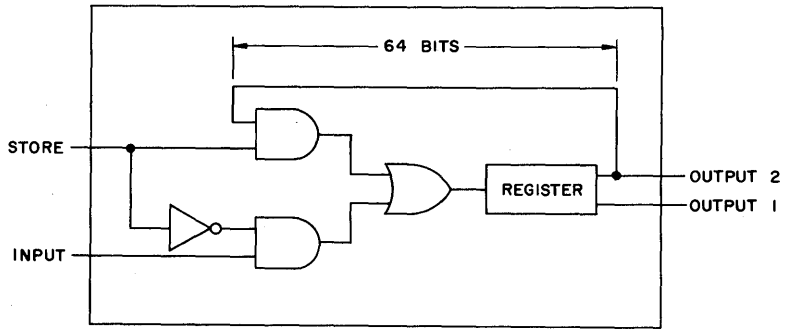
MEM 3064 B

DESCRIPTION

The 64-Bit Serial Accumulator consists of a 64-bit dynamic shift register plus logic for loading or recirculating information within the circuit. The device is constructed on a single monolithic chip utilizing MTOS (Metal-Thick-Oxide-Silicon) P-channel enhancement mode transistors.

The accumulator operates at frequencies from 10 kHz to 2 MHz. Each individual stage of the register dissipates $<200\,\mu$ watts during 2 MHz operation. The power dissipation of each of these stages decreases proportionally with frequency. Both data and $\overline{\text{data}}$ outputs are available, each of these output stages dissipates <12 mW at 2 MHz into a 12 picofarad load.

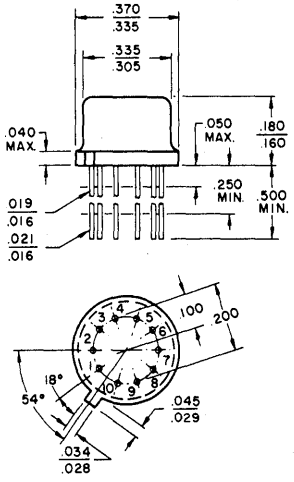
One accumulator circuit can drive directly into another without the addition of any external components.



LOGIC DIAGRAM

STANDARD PACKAGE

LOW PROFILE 10 LEAD
TO-74



Bottom view

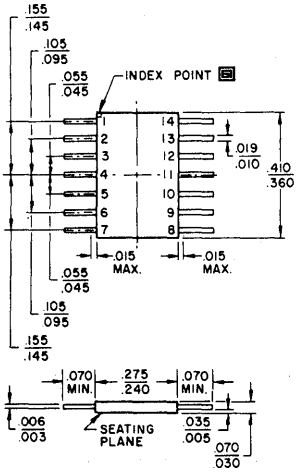
NOTE: All dimensions in inches

TERMINALS

P/N	FUNCTION
1	Ground
2	$\phi 3$
3	$\phi 1$
4	Store
5	No Connection
6	$\phi 2$
7	Output 2 (Data)
8	$\phi 4$
9	Input
10	Output 1 ($\overline{\text{Data}}$)

OPTIONAL PACKAGE

TO-87



Note: All dimensions in inches.

TERMINALS

P/N	FUNCTION
1	Ground
2	$\phi 3$
3	$\phi 1$
4	Store
5	No Connection
6	No Connection
7	No Connection
8	No Connection
9	No Connection
10	$\phi 2$
11	Output 2 (Data)
12	$\phi 4$
13	Input
14	Output 1 ($\overline{\text{Data}}$)

MAXIMUM RATINGS

Clock Voltages (ϕ_1, ϕ_2, ϕ_3, ϕ_4) ..... −30V to +0.3V
Data Input & Store Voltages ..... −30V to +0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)

Load = 10MΩ and 12pF, T_A = −55°C to +85°C

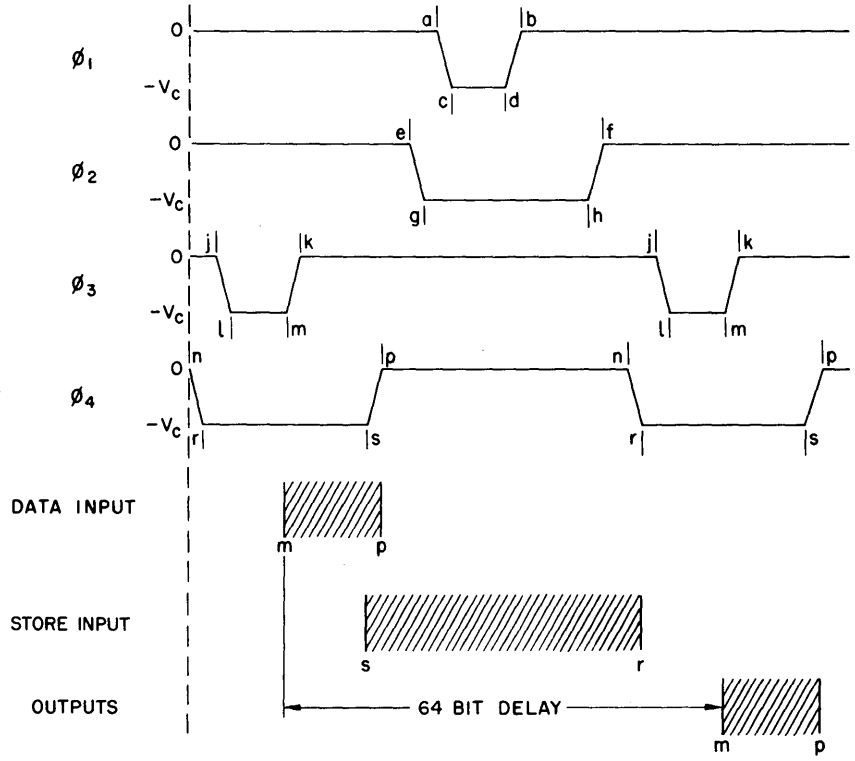
Characteristic	Min	Typ	Max	Units	Conditions
Clock Repetition Rate	.01	—	2.0	MHz	
Clock Pulse Width (ϕ_1 & ϕ_3)	100	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Pulse Width (ϕ_2 & ϕ_4)	200	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Logic Levels					
Logic "0"	+0.3	—	−1.0	Volt	
Logic "1"	−24	—	−27	Volts	
Data & Store Input Levels					
Logic "1"	−10	—	−24	Volts	
Logic "0"	0	—	−2.0	Volts	
Data Input Pulse Width	100	—	—	nS	Stable During t_{mp} SEE FIGURE 1
Store Pulse Width	200	—	—	nS	Stable During t_{sr} SEE FIGURE 1
Clock Input Capacity					
ϕ_1, ϕ_3, ϕ_4	—	—	10	pF	
ϕ_2	—	—	10	pF	Plus Output Capacitive Load
Data & Store Input Capacity	—	—	2.0	pF	
Input Leakage To Ground (Clock Input Terminals)	—	—	100	μA	V_{IN} = −27V
Input Leakage To Ground (Data & Store Terminals)	—	—	5.0	μA	V_{IN} = −20V
Output Logic Levels*					
Logic "0"	0	—	−2.0	Volts	Stable During t_{mp}
Logic "1"	−11	—	−24	Volts	Stable During t_{mp}

*A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

FIGURE 1.

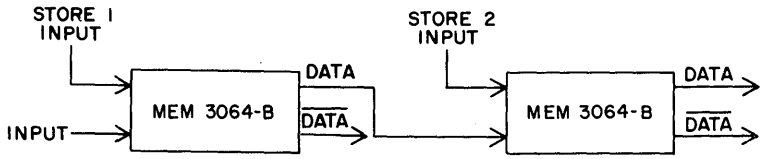
MINIMUM CLOCK REQUIREMENTS

CHARACTERISTIC	SYMBOL	MINIMUM VALUE (nS)	MAXIMUM VALUE (uS)
ϕ_1 Pulse Width	t c d	100	
ϕ_2 Pulse Width	t l m	100	
ϕ_3 Pulse Width	t g h	200	
ϕ_4 Pulse Width	t r s	200	1.0
Sampling Width 1	t b h	100	
Sampling Width 2	t k s	100	
ϕ_4 — ϕ_1 Overlap	t p a	0	
ϕ_2 — ϕ_3 Overlap	t f j	0	
ϕ_2 — ϕ_4 Overlap	t f n	0	1.0
ϕ_4 — ϕ_2 Overlap	t p e	0	
ϕ_3 Precharge Time	t r m	100	
ϕ_1 Precharge Time	t g d	100	

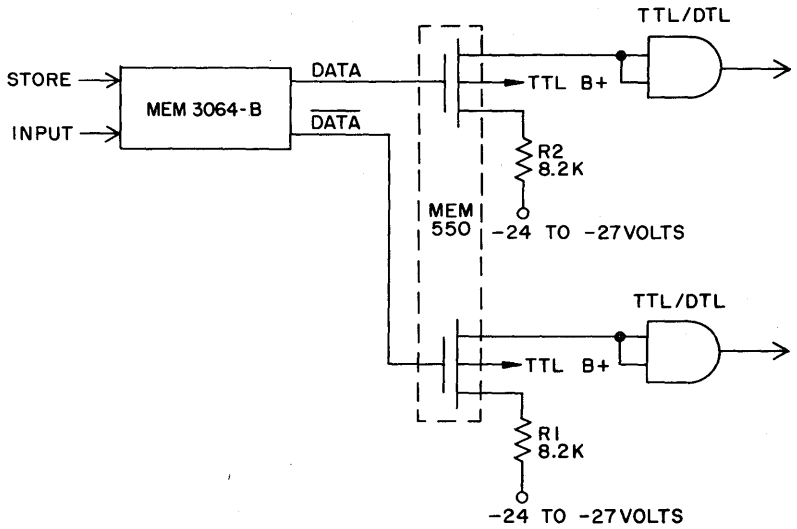


Designations ϕ_1, ϕ_2, ϕ_3, ϕ_4 on this data sheet are arbitrary and may be rearranged to correspond with designations on other MTOS data sheets. The relative timing however must be maintained as shown.

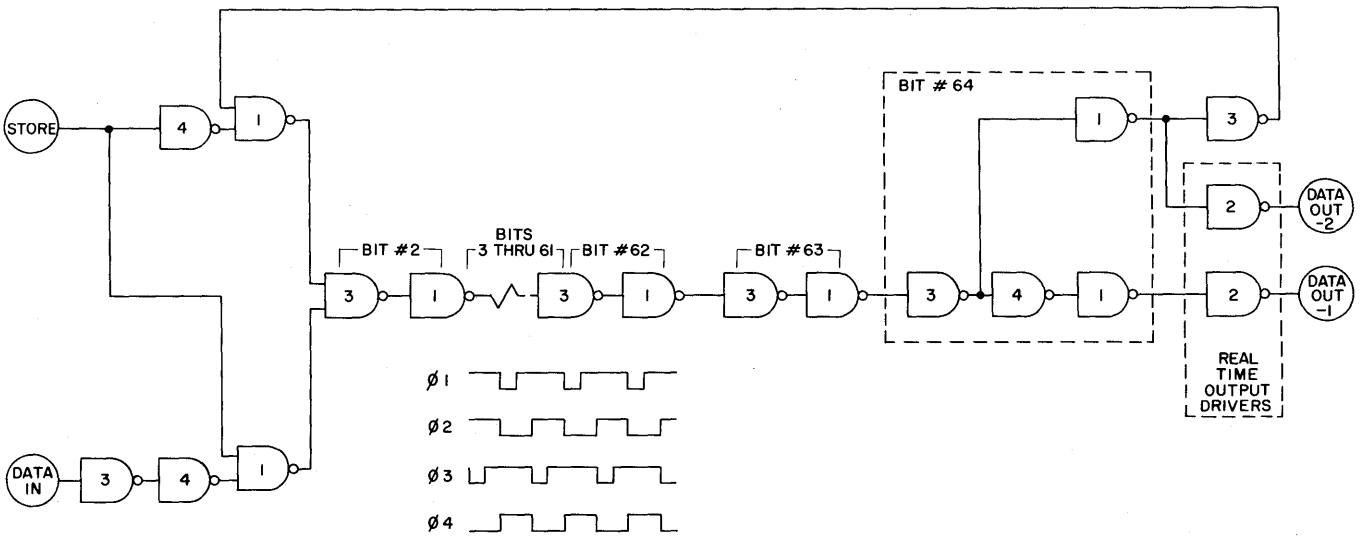
TYPICAL MEM 3064 B INTERCONNECTION DIAGRAM

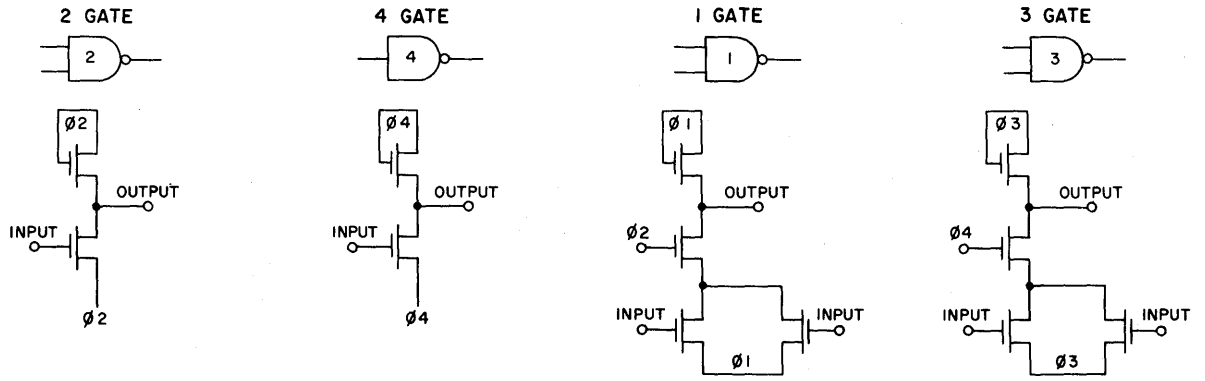


TYPICAL INTERFACE CIRCUIT



SCHEMATIC DIAGRAM MEM 3064 B





PRECHARGE TIME Ø2
SAMPLING TIME $\overline{Ø2}$

PRECHARGE TIME Ø4
SAMPLING TIME $\overline{Ø4}$

PRECHARGE TIME Ø1
SAMPLING TIME Ø2 $\overline{Ø1}$

PRECHARGE TIME Ø3
SAMPLING TIME Ø4 $\overline{Ø3}$

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GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
OCTOBER, 1967

DUAL 64-BIT SERIAL ACCUMULATOR

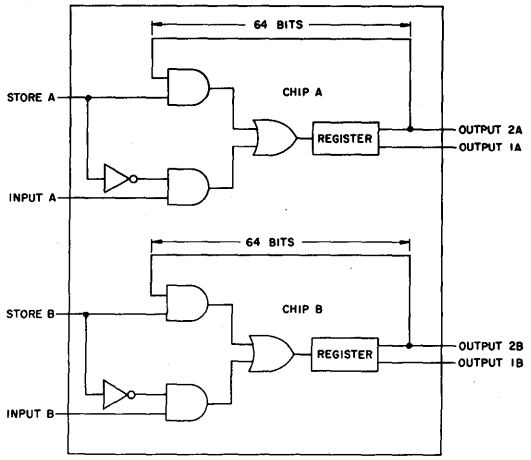
MEM 3064-2B

DESCRIPTION

The Dual 64-Bit Serial Accumulator consists of two 64-bit dynamic shift registers plus logic for loading or recirculating information within each circuit. The device is constructed on two monolithic chips utilizing MTOS (Metal-Thick-Oxide-Silicon) P-channel enhancement mode transistors.

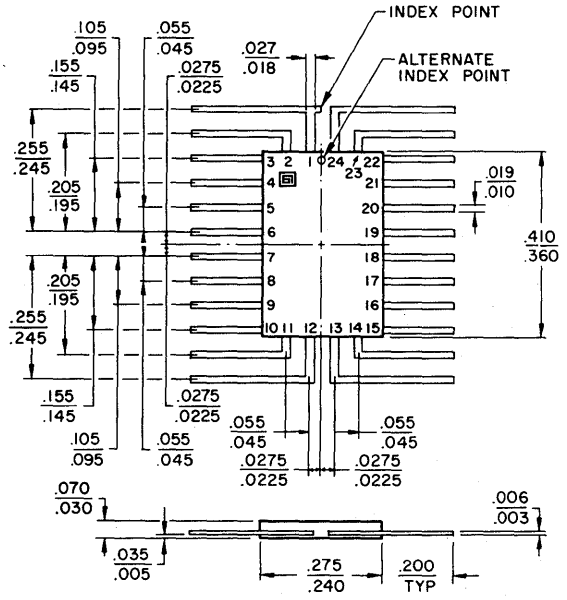
The dual accumulator operates at frequencies from 10 kHz to 2 MHz. Each individual register stage dissipates <200 μwatts during 2 MHz operation. The power dissipation of each of these stages decreases proportionally with frequency. Both data and $\overline{\text{data}}$ outputs are available, each of these output stages dissipates <12 mW at 2 MHz into a 12 picofarad load.

One accumulator circuit can drive directly into another without the addition of any external components.



LOGIC DIAGRAM

24 LEAD FLAT PACK



Note: All dimensions in inches.

TERMINALS

P/N	FUNCTION	P/N	FUNCTION
1	Ground	13	No Connection
2	No Connection	14	ϕ 2B
3	No Connection	15	Output 2 (Data B)
4	ϕ 3A	16	ϕ 4B
5	ϕ 1A	17	Input B
6	Store A	18	Output 1 ($\overline{\text{Data}}$ B)
7	No Connection	19	ϕ 2A
8	ϕ 3B	20	Output 2 (Data A)
9	ϕ 1B	21	ϕ 4A
10	Store B	22	Input A
11	No Connection	23	Output 1 ($\overline{\text{Data}}$ A)
12	No Connection	24	No Connection

MAXIMUM RATINGS

Clock Voltages (ϕ_1, ϕ_2, ϕ_3, ϕ_4) ..... −30V to +0.3V
Data Input & Store Voltages ..... −30V to +0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +85°C

ELECTRICAL CHARACTERISTICS (Each Accumulator)

Standard Conditions (unless otherwise specified)

Load = 10MΩ and 12pF, T_A = −55°C to +85°C

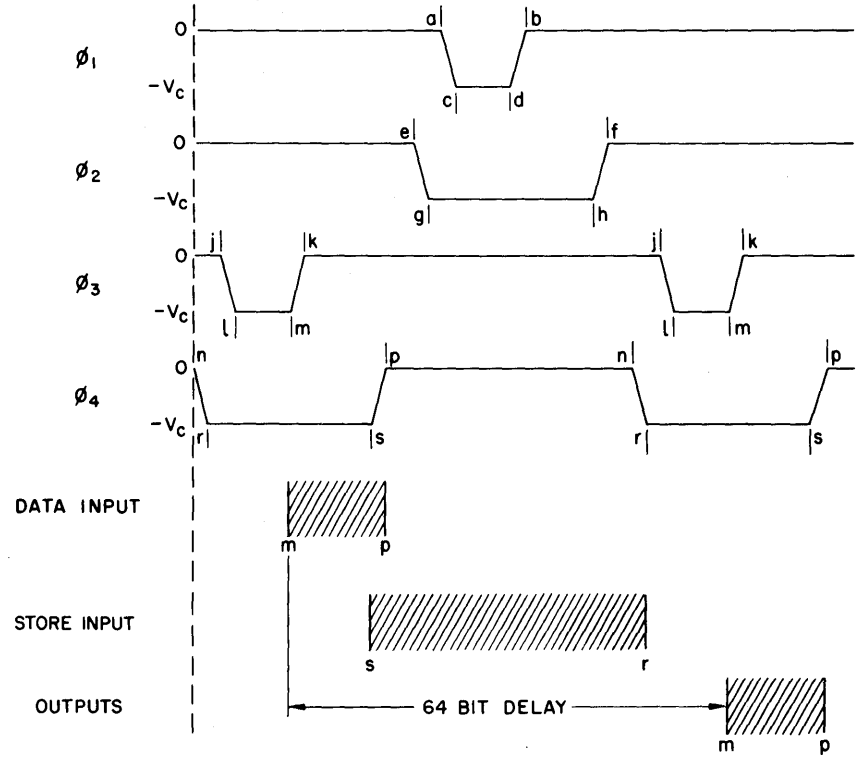
Characteristic	Min	Typ	Max	Units	Conditions
Clock Repetition Rate	.01	—	2.0	MHz	
Clock Pulse Width (ϕ_1 & ϕ_3)	100	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Pulse Width (ϕ_2 & ϕ_4)	200	—	—	nS	@ −24 Volts SEE FIGURE 1
Clock Logic Levels					
Logic "0"	+0.3	—	−1.0	Volt	
Logic "1"	−24	—	−27	Volts	
Data & Store Input Levels					
Logic "1"	−10	—	−24	Volts	
Logic "0"	0	—	−2.0	Volts	
Data Input Pulse Width	100	—	—	nS	Stable During t_{mp} SEE FIGURE 1
Store Pulse Width	200	—	—	nS	Stable During t_{sr} SEE FIGURE 1
Clock Input Capacity					
ϕ_1, ϕ_3, ϕ_4	—	—	10	pF	
ϕ_2	—	—	10	pF	Plus Output Capacitive Load
Data & Store Input Capacity	—	—	2.0	pF	
Input Leakage To Ground (Clock Input Terminals)	—	—	100	μA	V_{IN} = −27V
Input Leakage To Ground (Data & Store Terminals)	—	—	5.0	μA	V_{IN} = −20V
Output Logic Levels*					
Logic "0"	0	—	−2.0	Volts	Stable During t_{mp}
Logic "1"	−11	—	−24	Volts	Stable During t_{mp}

*A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

FIGURE 1.

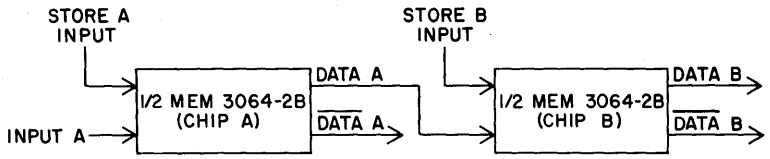
MINIMUM CLOCK REQUIREMENTS

CHARACTERISTIC	SYMBOL	MINIMUM VALUE (nS)	MAXIMUM VALUE (uS)
ϕ_1 Pulse Width	t c d	100	
ϕ_2 Pulse Width	t l m	100	
ϕ_3 Pulse Width	t g h	200	
ϕ_4 Pulse Width	t r s	200	1.0
Sampling Width 1	t b h	100	
Sampling Width 2	t k s	100	
ϕ_4 — ϕ_1 Overlap	t p a	0	
ϕ_2 — ϕ_3 Overlap	t f j	0	
ϕ_2 — ϕ_4 Overlap	t f n	0	1.0
ϕ_4 — ϕ_2 Overlap	t p e	0	
ϕ_3 Precharge Time	t r m	100	
ϕ_1 Precharge Time	t g d	100	

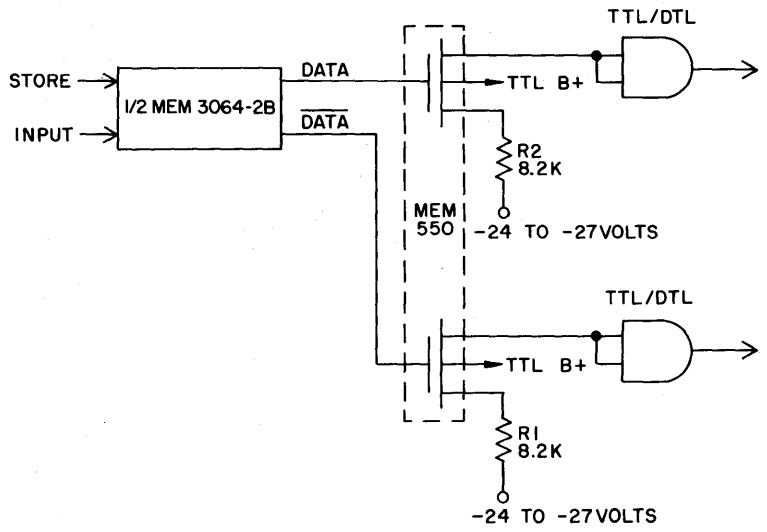


Designations ϕ_1, ϕ_2, ϕ_3, ϕ_4 on this data sheet are arbitrary and may be rearranged to correspond with designations on other MTOS data sheets. The relative timing however must be maintained as shown.

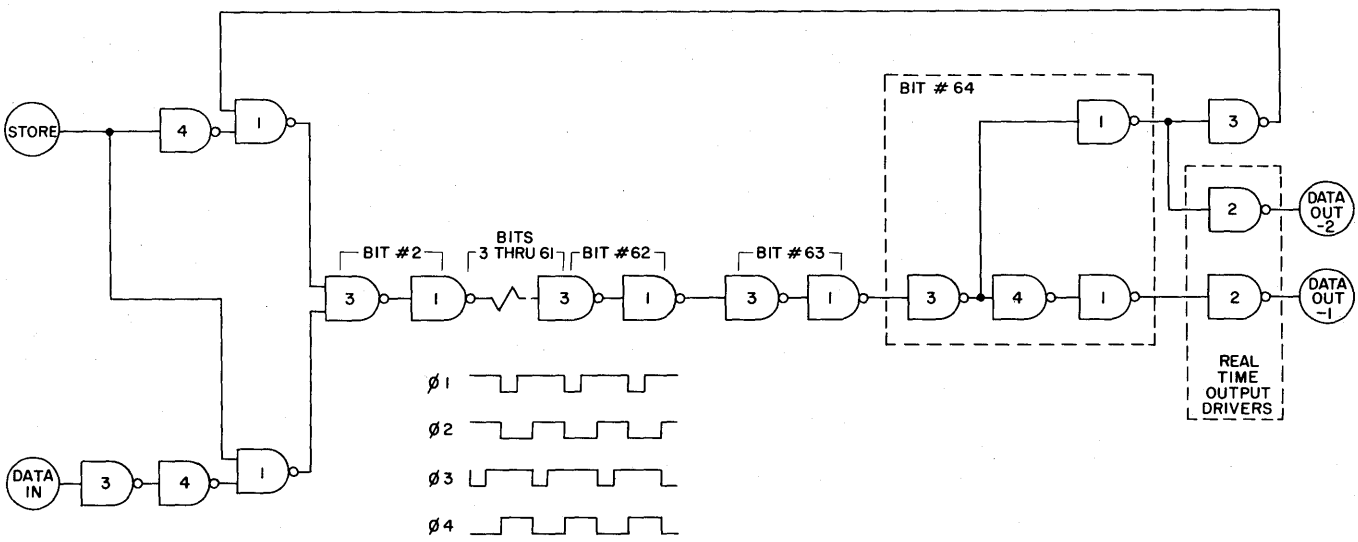
TYPICAL MEM 3064-2B INTERCONNECTION DIAGRAM

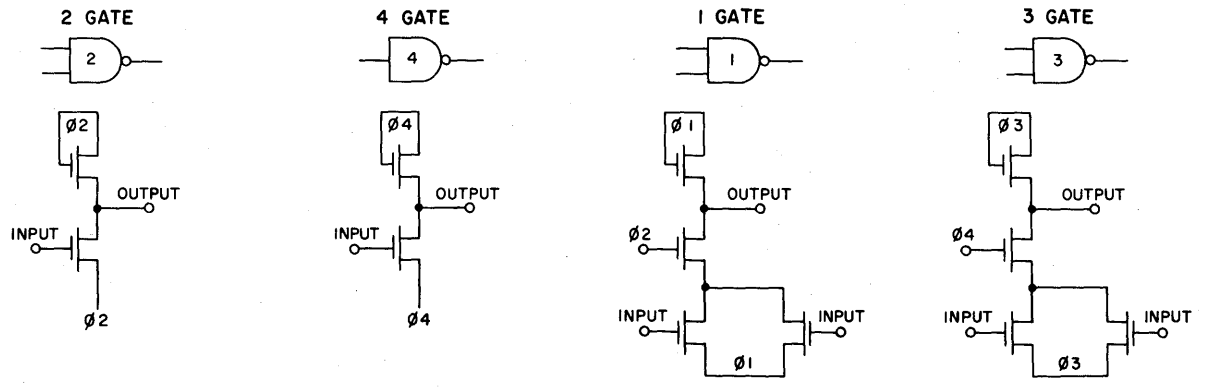


TYPICAL INTERFACE CIRCUIT



SCHEMATIC DIAGRAM MEM 3064-2B (CHIP A OR B)





PRECHARGE TIME Ø2
SAMPLING TIME $\overline{Ø2}$

PRECHARGE TIME Ø4
SAMPLING TIME $\overline{Ø4}$

PRECHARGE TIME Ø1
SAMPLING TIME Ø2 $\overline{Ø1}$

PRECHARGE TIME Ø3
SAMPLING TIME Ø4 $\overline{Ø3}$

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GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

ADVANCE
NOVEMBER, 1967

10-BIT A/D-D/A CONVERTER ELEMENT

MEM 5014

DESCRIPTION

The MEM 5014 is a Monolithic MTOS Integrated Circuit containing 275 active components. It performs all the logic and analog switching functions for 10-bit successive approximation analog-to-digital conversion. In addition, it operates in two other major modes — as a 10-bit digital-to-analog converter or a 10-channel analog multiplexer.

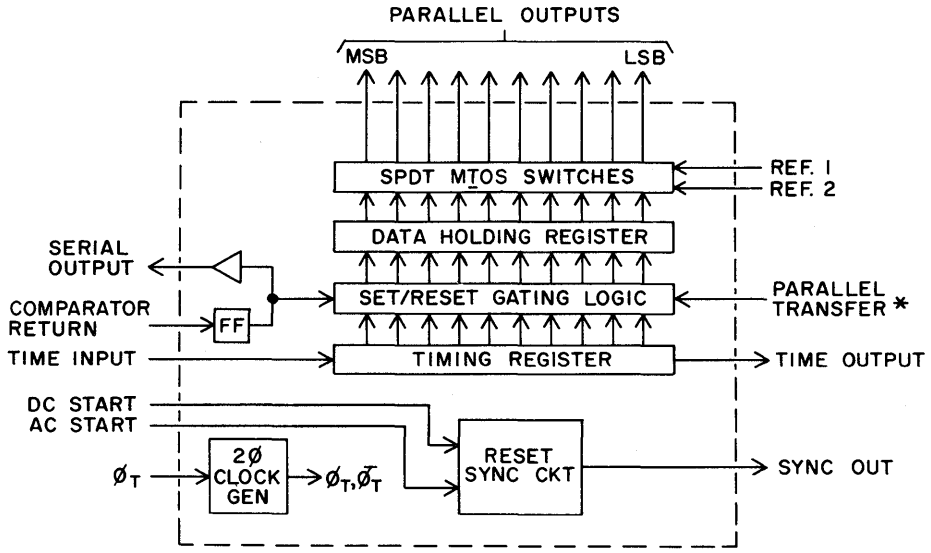
As an analog-to-digital converter, the MEM 5014 is used in conjunction with an external precision ladder network and voltage comparator. This mode provides both serial and parallel binary outputs.

The MEM 5014 is packaged in a 40 lead hermetically sealed in-line package whch can be soldered to a printed circuit board or used with a 40 pin socket.

FEATURES

- Contains all logic and ladder drivers for 10-bit successive approximation analog-to-digital conversion mode
- 10-bit digital-to-analog converter mode
- 10-channel current multiplexer mode
- DC to 200 kHz serial bit rate
- Monolithic construction
- Zener network protection on all inputs
- High noise immunity (1 Volt Minimum)
- Serial and Parallel data outputs
- Low power consumption (135 mW)
- 40 lead plug-in package
- Compatible with General Instrument logic family and multiplexer systems

MEM 5014 SIMPLIFIED BLOCK DIAGRAM



* CONTENTS OF TIME TO DATA REGISTER

MAXIMUM RATINGS

Input Voltages ..... −30V
Drain Voltage (V_{DD}) ..... −30V
Reference Voltages ($V_{REF}1$, $V_{REF}2$) ..... −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

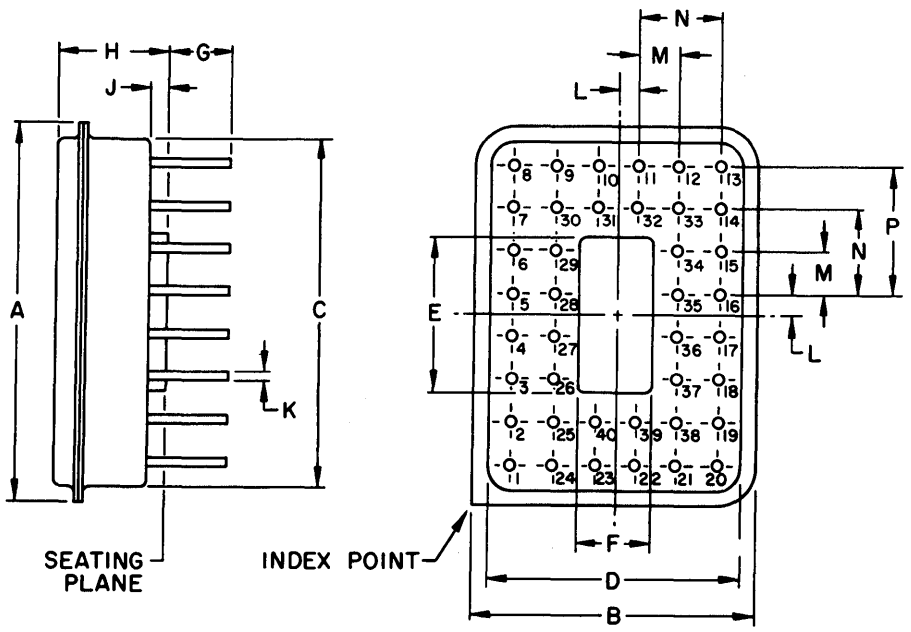
NOTE: A voltage which is more positive than .3 volts with respect to the ground terminal should not be applied to any pin.

ELECTRICAL CHARACTERISTICS

V_{DD} (Supply Voltage) = −27V ± 1V, R_L = 1.0 MΩ, C_L = 10 pF, T_A = −55°C to +85°C (unless otherwise specified)

Characteristic	Min	Typ	Max	Units	Conditions
Logic Inputs					
Logic "0"	0	—	−2.0	Volts	V_{DD} = −27V
Logic "1"	−10	−12	−30	Volts	V_{DD} = −27V
Clock					
Amplitude	−10	−12	−30	Volts	
Width	1.0	—	10	μS	
Frequency	DC	—	200	kHz	
Input Leakage	—	—	5.0	μA	V_{IN} = −20V
Logic Outputs					
Except Parallel Data Outputs					
Logic "0"	0	−0.5	−1.0	Volt	
Logic "1"	−11	−12	—	Volts	
Logic "1"	−10	—	—	Volts	R_L = 68KΩ
Rise Time (positive transition)	—	1.0	—	μS	10% to 90%, C_L = 40 pF
Fall Time (negative transition)	—	3.0	—	μS	10% to 90%, C_L = 40 pF
Parallel Data Logic Level					
Logic "0"	—	V_{REF1}	—	Volts	0 ≤ $V_{REF}1$ ≤ −10V, R_L = 2 MΩ
Logic "1"	—	V_{REF2}	—	Volts	0 ≤ $V_{REF}2$ ≤ −10V, R_L = 2 MΩ
Rise Time	—	1.0	—	μS	10% to 90%, C_L = 100 pF
Fall Time	—	3.0	—	μS	10% to 90%, C_L = 100 pF
Ladder Switches					
MSB $R_{D(ON)}$	450	560	600	Ohms	V_{DD} = −27V, V_{REF} = −5.0V, T_A = 25°C
2nd MSB $R_{D(ON)}$	500	1000	1100	Ohms	V_{DD} = −27V, V_{REF} = −5.0V, T_A = 25°C
3rd MSB thru LSB	800	1100	1400	Ohms	V_{DD} = −27V, V_{REF} = −5.0V, T_A = 25°C
Individual Switch Leakage	—	0.1	5.0	nA	V_{REF} = −10V, T_A = 25°C
Ref Line Leakage	—	0.5	15	nA	V_{REF} = −10V, T_A = 25°C
$R_{D(ON)}$ Temp. Coefficient	—	0.3	—	%/°C	
$R_{D(ON)}$ Temp. Coefficient Tracking	—	.03	—	%/°C	
Supply Current Drain	—	5.0	—	mA	V_{DD} = −27V
Network Dissipation	—	135	—	mW	V_{DD} = −27V

PACKAGE — 40 LEAD PLUG-IN



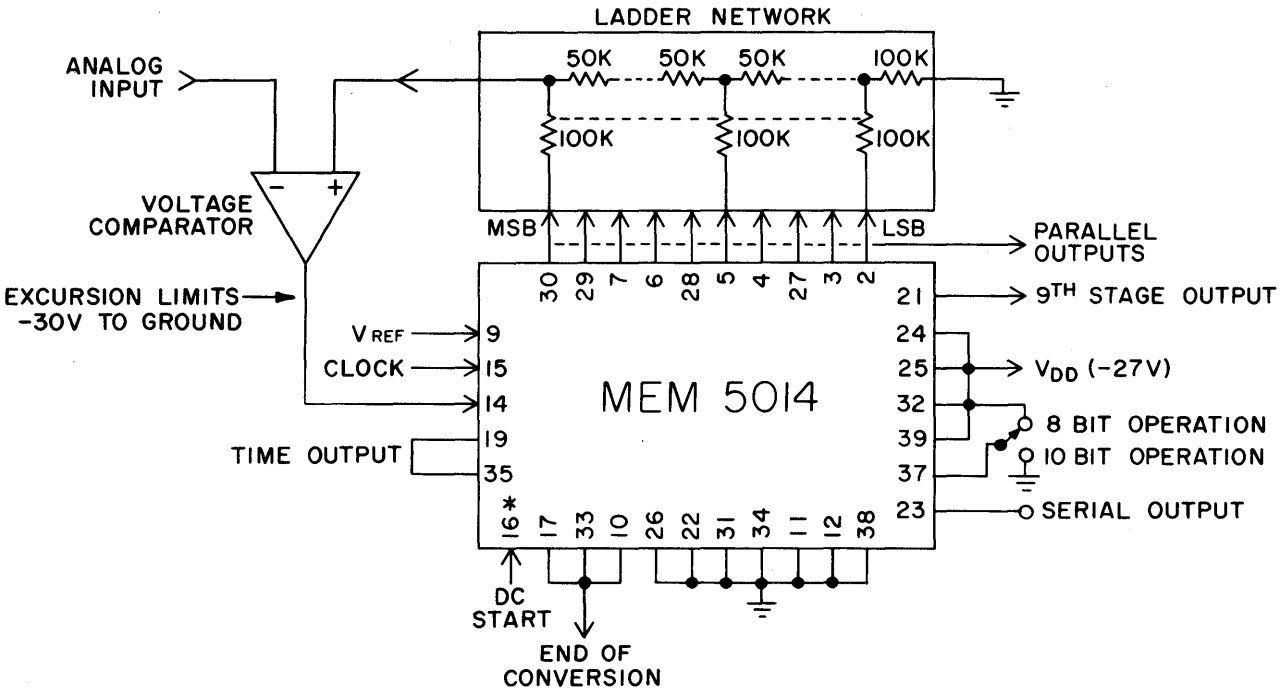
BOTTOM VIEW

SYMBOL	INCHES	
	MIN.	MAX.
A	.880	.895
B	.685	.695
C	.812	.820
D	.609	.620
E	.365	.385
F	.175	.195
G	.125	.160
H	.264 REF.	
J	.031	.075
K	.018	.022
L	.0475	.0525
M	.095	.105
N	.195	.205
P	.295	.305

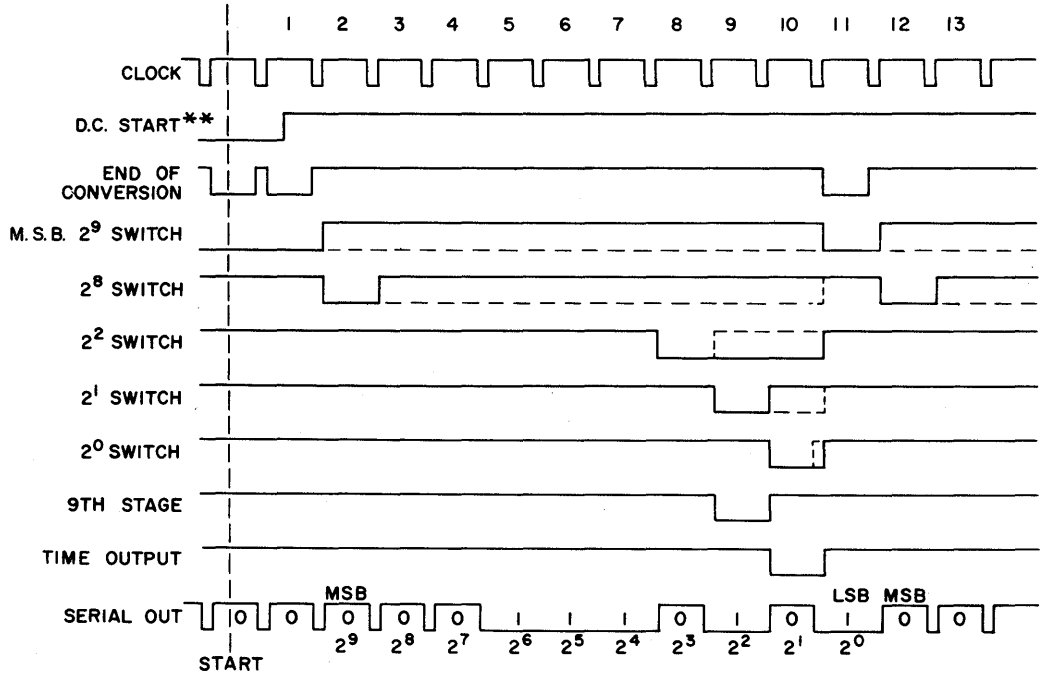
TERMINALS

P/N	FUNCTION	P/N	FUNCTION
1	No Connection	21	9th Stage Output
2	2^0 Switch	22	(Connect to Ground)
3	2^1 Switch	23	Serial Output
4	2^3 Switch	24	(Connect to V_{DD})
5	2^4 Switch	25	V_{DD}
6	2^6 Switch	26	Reference 1
7	2^7 Switch	27	2^2 Switch
8	No Connection	28	2^5 Switch
9	Reference 2	29	2^8 Switch
10	Data Preset	30	2^9 Switch
11	(Connect to Ground)	31	Data Reset
12	Time Input	32	(Connect to Pin 39)
13	No Connection	33	Time Preset
14	Comparator Return	34	Time Reset
15	$\emptyset_T$ (Time Clock)	35	AC Start
16	DC Start	36	No Connection
17	Sync. Output	37	8/10 Control
18	No Connection	38	Ground
19	Time Output	39	Transfer
20	No Connection	40	No Connection

TYPICAL CONNECTIONS — A/D MODE



TYPICAL WAVEFORMS — A/D MODE

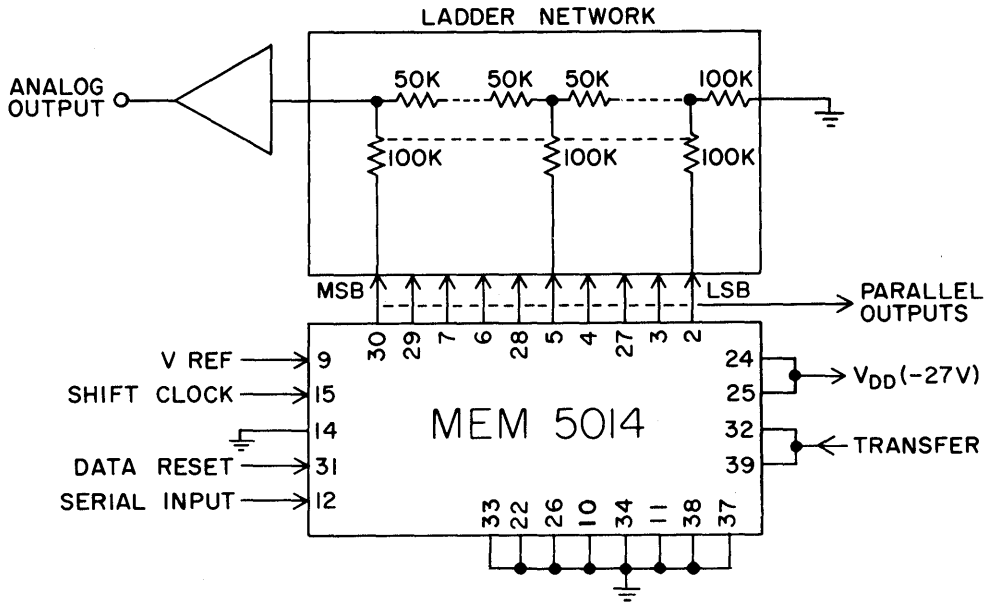


NOTE: ON EARLY UNITS, SERIAL OUTPUT MAY BE INVERTED FROM THAT SHOWN.

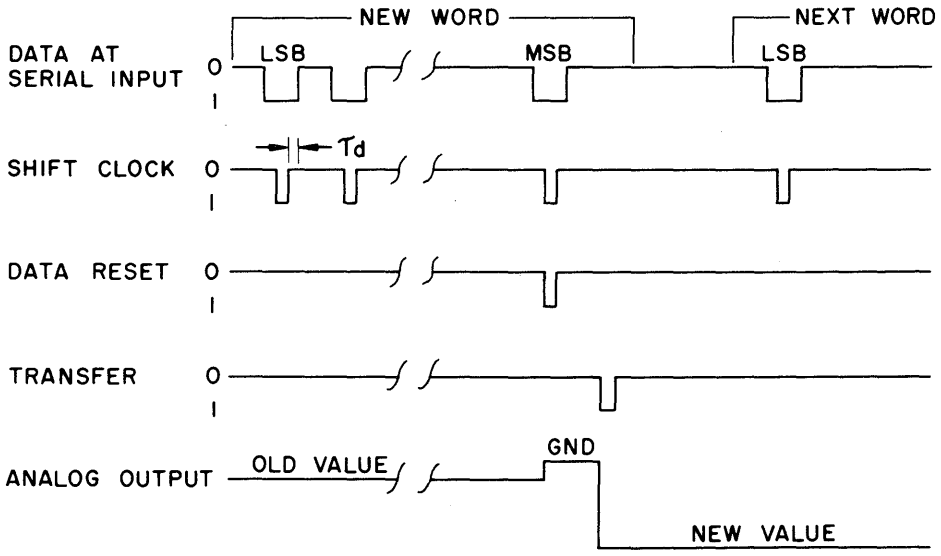
*Pin 16 should be pulsed negative to start A/D convertor and then held at ground.

**Converter will run continuously if DC START is held at ground and will always determine the MSB output on the first clock cycle after a positive transition of DC START.
For single conversion operation on external command, remove the jumper between pins 19 & 35, apply command to DC START, and ground pin 35.

TYPICAL CONNECTIONS — D/A CONVERTER MODE

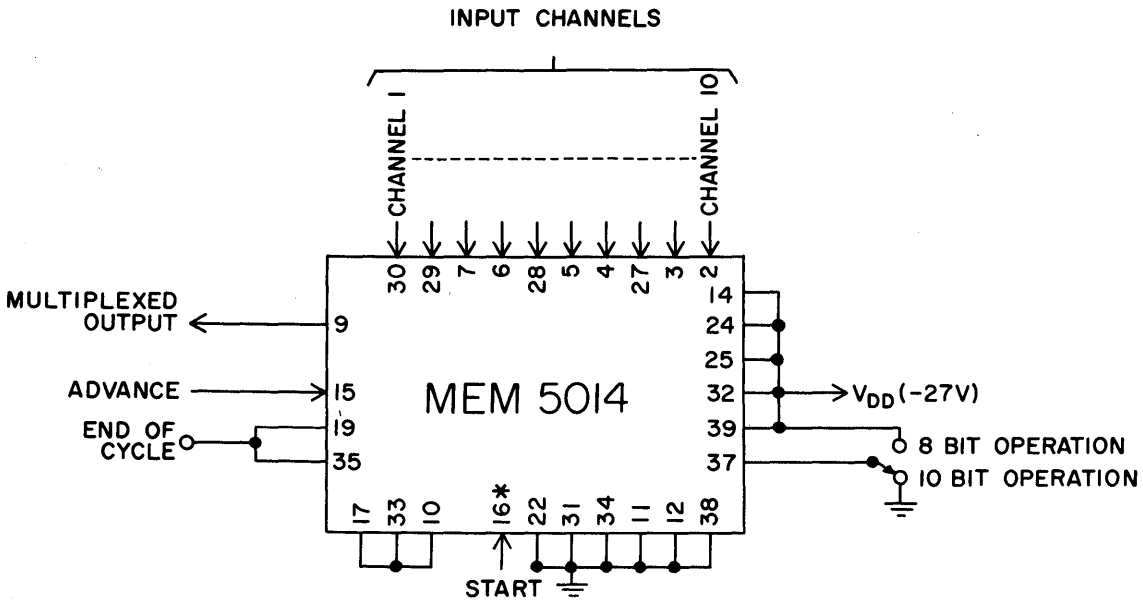


TYPICAL WAVEFORMS — D/A CONVERTER MODE



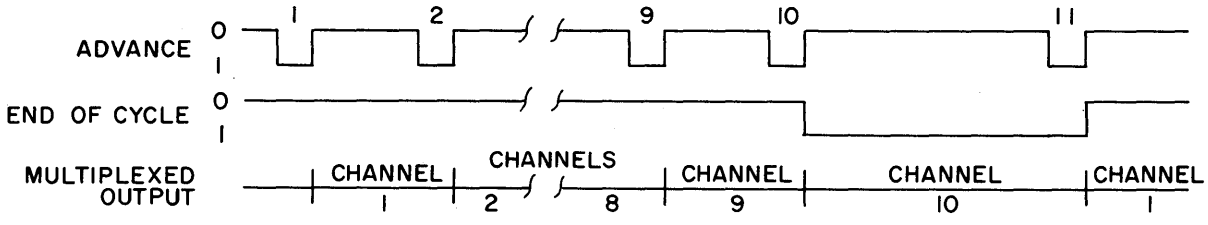
Td = 200nS (MIN)

TYPICAL CONNECTIONS — CURRENT MODE MULTIPLEXER

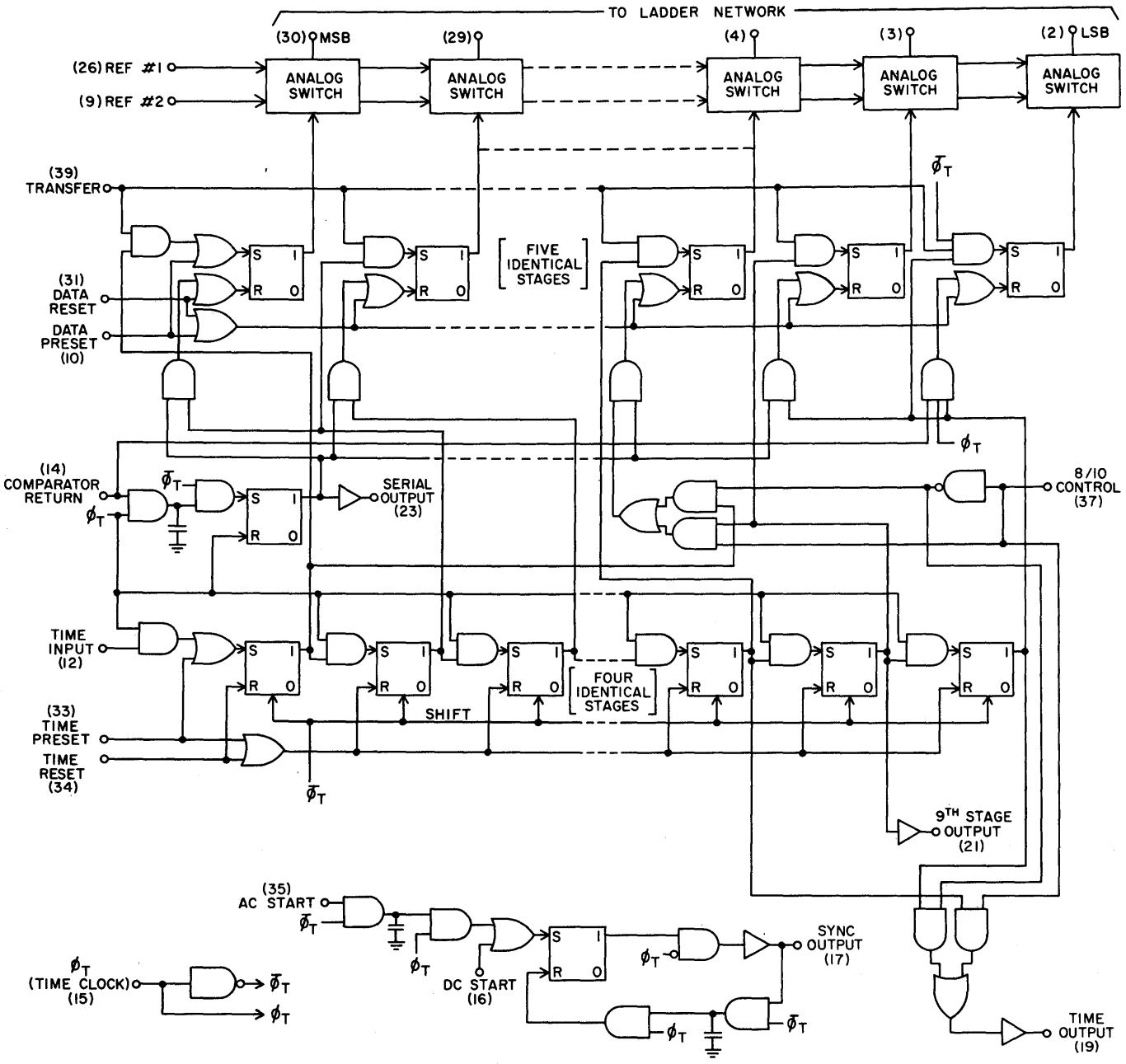


*Pin 16 should be pulsed negative to start the multiplexer and then held at ground.

TYPICAL WAVEFORMS — MULTIPLEXER MODE



MEM 5014 LOGIC DIAGRAM



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Hicksville, L. I., N. Y. 11802
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Printed in U.S.A.

GENERAL INSTRUMENT

GENERAL INSTRUMENT
MTOS INTEGRATED CIRCUIT

2 INPUT ΔY ADDER

ADVANCE
DECEMBER, 1967

MEM 5035

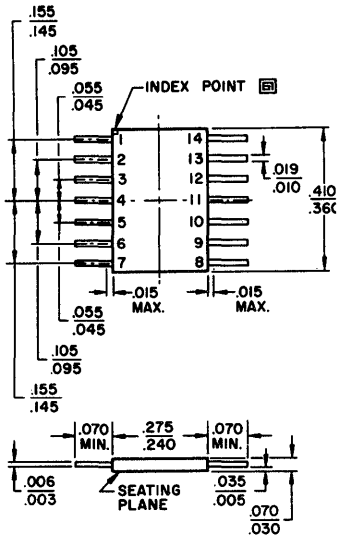
DESCRIPTION

The MEM 5035 is a 2 input ΔY Adder constructed on a single monolithic chip utilizing MTOS P-channel enhancement mode transistors. This element is designed to be used with the Digital Differential Analyzer Element (MEM 5021) to provide two additional ΔY inputs, each with a scale input. These additional inputs, like the normal ΔY inputs of the Digital Differential Analyzer Element are of the ternary type.

The Logic Diagram shows the internal logic blocks of the MEM 5035 2 input ΔY Adder element. The input flip-flops, one for each ΔY input, are set when a negative increment is detected. Carry flip-flop C_1, is the less significant flip-flop, with C_{2b} being the more significant flip-flop and flip-flop C_{2a} generating a one bit delay. A partial sum of both incremental inputs and the Carry flip-flops is formed as shown. This partial addition occurs one bit time before the actual addition to the Y in by the half adder. The half adder then drives the output amplifier.

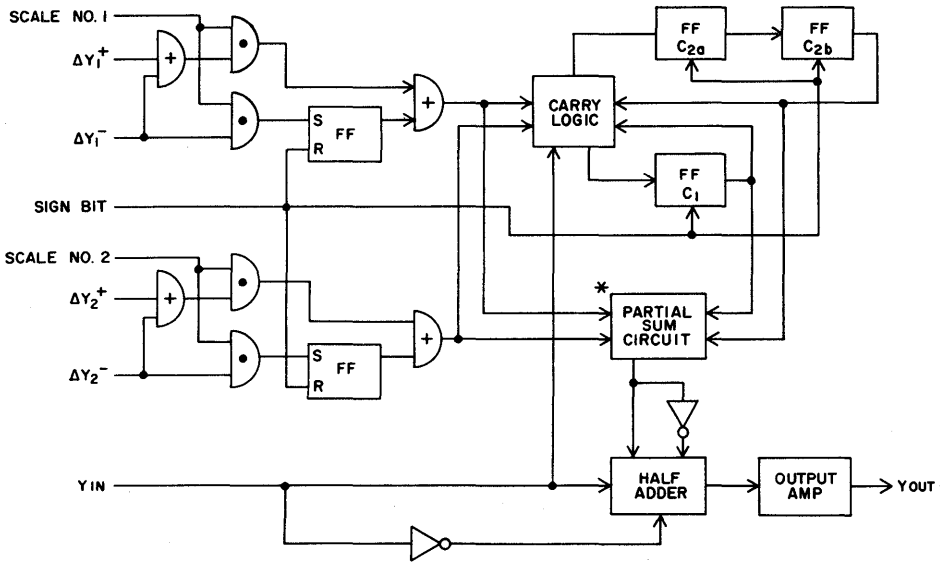
The function diagram shows the connections between the MEM 5035 2 input ΔY adder, the MEM 5021 digital differential analyzer, and the MEM 3016-2 a Dual 16 bit shift register. The timing diagram shows the relative timing of the various clocks to the output. Note, the occurance of the incremental addition is one bit time after the scale bit. The numbers in the shift registers are serial, least significant bit (LSB) first, sign bit last negative numbers are in 2's compliment form. For more information consult the General Instrument application note entitled, "MTOS Integrated Digital Differential Analyzer", and "Servo Adder".

TO-87



Note: All dimensions in inches

LOGIC BLOCK DIAGRAM OF THE MEM 5035 2-INPUT INCREMENTED ΔY ADDER ELEMENT



* ONE BIT DELAY OCCURS THROUGH INPUT AND SUM CIRCUIT.

TERMINALS

P/N	FUNCTION
1	#1 Y Adder Add Input (ΔY_1+)
2	#1 Scale Input
3	#1 Y Adder Subtract Input (ΔY_1-)
4	#2 Scale Input
5	#2 Y Adder Subtract Input (ΔY_2-)
6	#2 Y Adder Add Input (ΔY_2+)
7	Sign Bit
8	Drain Voltage ($-V_{dd}$)
9	Y Adder Output (Y_{out})
10	Gate Voltage ($-V_{gg}$)
11	Ground
12	Y Adder Input (Y_{in})
13	Clock (ϕ_2)
14	Clock (ϕ_1)

MAXIMUM RATINGS

Clock Voltages (ϕ_1 and ϕ_2) ..... −30V to +0.3V
Input Voltages ..... −30V to +0.3V
Drain Voltage (V_{DD}) ..... −20V to +0.3V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −55°C to +85°C

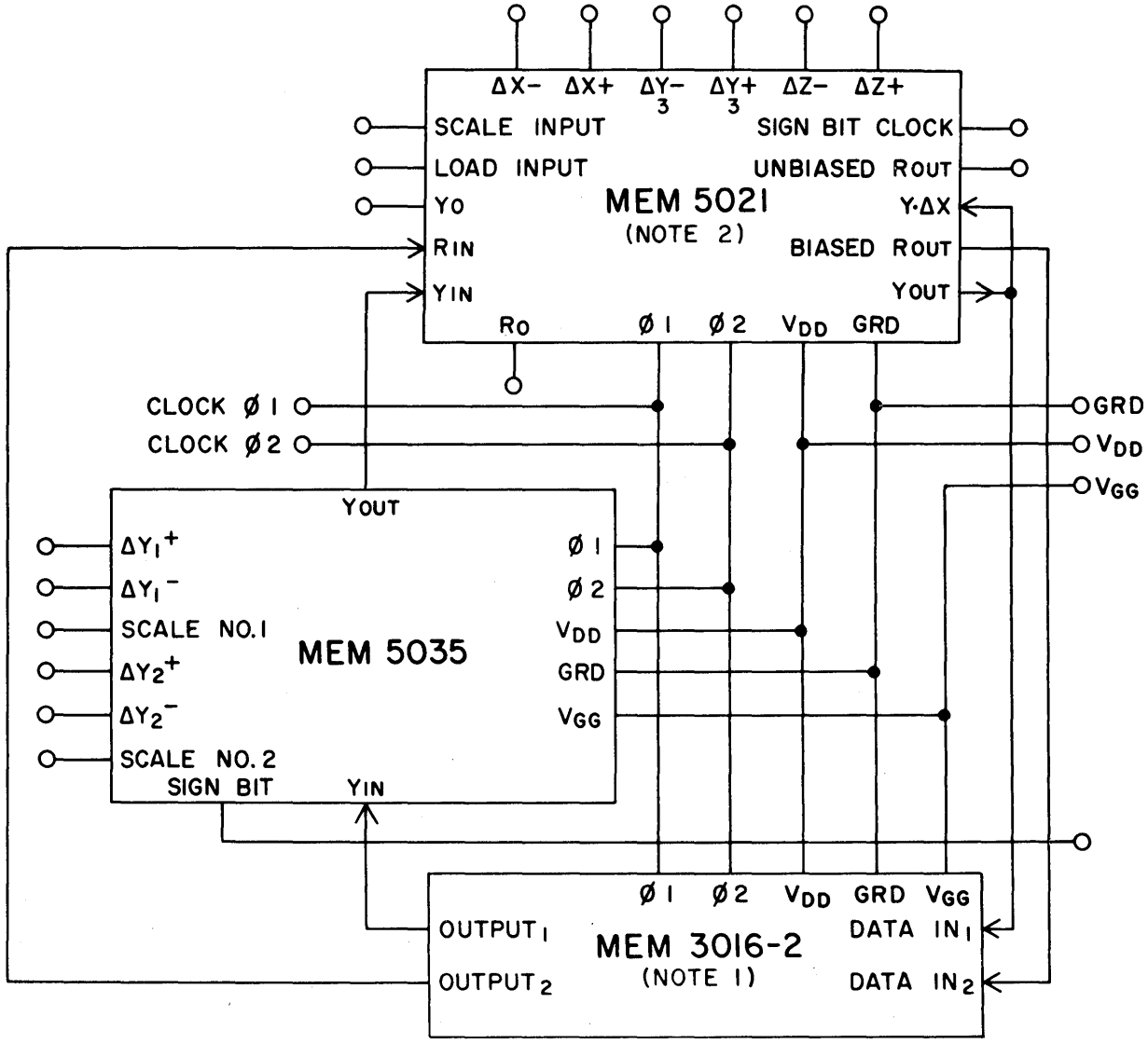
ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise specified)
Load = 100MΩ and 10 pF, $\phi_1 = \phi_2 = -27$ Volts ±1 Volt
$V_{DD} = -13$ Volts ±1 Volt, $T_A = -55°C$ to +85°C

Characteristic	Min	Typ	Max	Units	Conditions
Clock Repetition Rate	10	—	500	kHz	
Clock Pulse Widths					
ϕ_{pw1}	0.40	—	10	μS	SEE FIG. 1
ϕ_{pw2}	0.10	—	—	μS	SEE FIG. 1
Clock Delay (ϕ_d)	0.30	—	—	μS	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	0.1	μS	
Clock Pulse Logic Levels (ϕ_1 and ϕ_2)					
Logic "0"	—	—	−2.0	V	
Logic "1"	−26	—	−28	V	
Clock Pulse Input Capacitance	—	20	—	pF	$\phi_1 = \phi_2 = 0V$
Clock Input Current (ϕ_1)	—	—	100	μA	$\phi_1 = 0V$, $\phi_2 = -26V$
Clock Input Current (ϕ_2)	—	1.8	2.5	mA	$\phi_1 = -26V$, $\phi_2 = 0V$
Input Logic Levels					
Logic "0"	—	—	−2.0	V	
Logic "1"	−10	—	—	V	
Input Pulse Width	0.9	—	—	μS	
Input Capacitance	—	3.0	—	pF	$V_{in} = 0V$
Input Leakage Current	—	—	1.0	μA	$V_{in} = -20V$
Output Logic Levels					
Logic "0"	—	−0.5	−1.0	V	
Logic "1"	−11	−12	—	V	
Propagation Delay plus Rise & Fall Time					
T_{pd1} } See Note 2	—	100	250	nS	SEE FIG. 1
T_{pd2} }	—	—	—	nS	SEE FIG. 1
Noise Immunity	1.0	—	—	V	dc to 500 kHz
Output Impedance to Ground (Output at Logic "0")	—	—	3500	Ohms	
Output Drive Capability (Output at Logic "1")	−10	−11	—	V	R_L = 75 K Ohms
Output Drive Capability (Output at Logic "1")	−5.0	—	—	V	R_1 = 10 K Ohms
Supply Current Drain	—	—	6.0	mA	f = 500 kHz

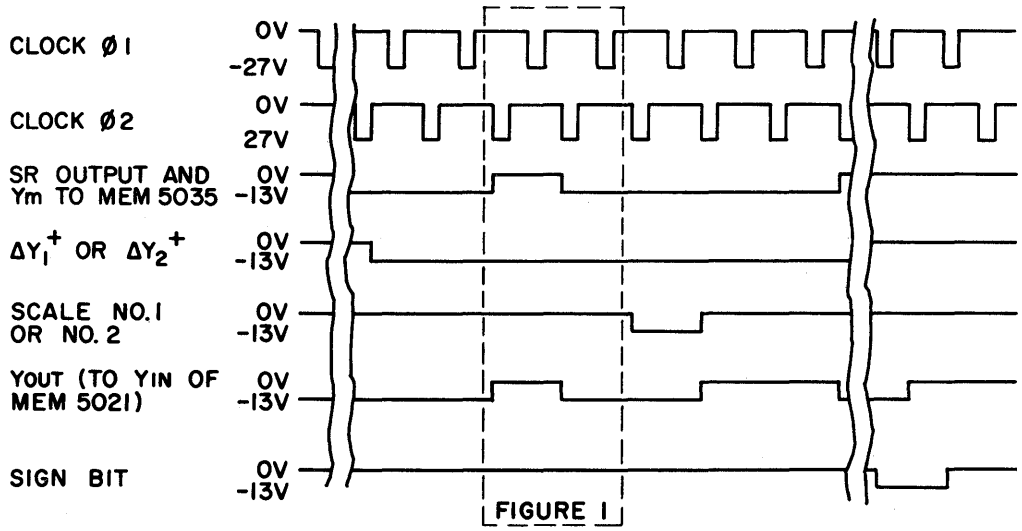
NOTE 2: T_1 and T_2 represent the propagation delay plus rise and fall times of the MEM 5035 Element.

FUNCTION DIAGRAM



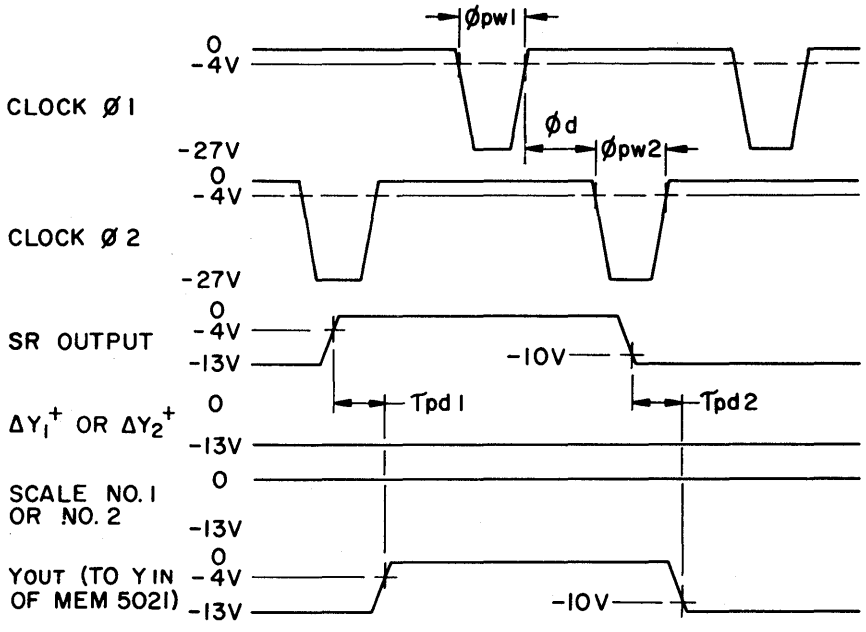
NOTE: 1: The MEM 3016-2 is a dual 16 bit, d.c. to 1 MC, shift register.
NOTE: 2: The MEM 5021 is the Digital Differential Analyzer Element.

TYPICAL TIMING DIAGRAM



NOTE: INCREMENTAL ADDITION OCCURS ONE BIT TIME AFTER THE SCALE BIT.

FIGURE 1



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600 West John Street
Hicksville, L. I., N.Y. 11802
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