Non-Volatile Memory Data Book

GENERAL INSTRUMENT

NON-VOLATILE MEMORY DATA BOOK

TABLE OF CONTENTS

GENERAL INSTRUMENT

SECTION 1

READ ONLY MEMORIES

GENERAL INSTRUMENT

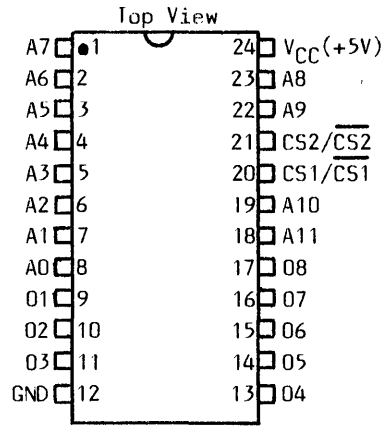
32,768 BIT STATIC READ ONLY MEMORY

FEATURES:

- 4096 x 8 organization
- Fully static operation - no clocks required
- Single +5V +10% supply
- 450ns access time: RO9432B
- 300ns access time: RO9432C
- 250ns access time: RO9432DS
- 200ns access time: RO9432D
- Inputs and outputs TTL compatible
- Three state outputs - under the control of two mask programmable chip select inputs
- Output drive capability of 2 TTL loads 100pf
- Low power dissipation
- Totally automated custom programming
- Pin compatible with 2532 EPROM
- ESD protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883

PIN CONFIGURATION

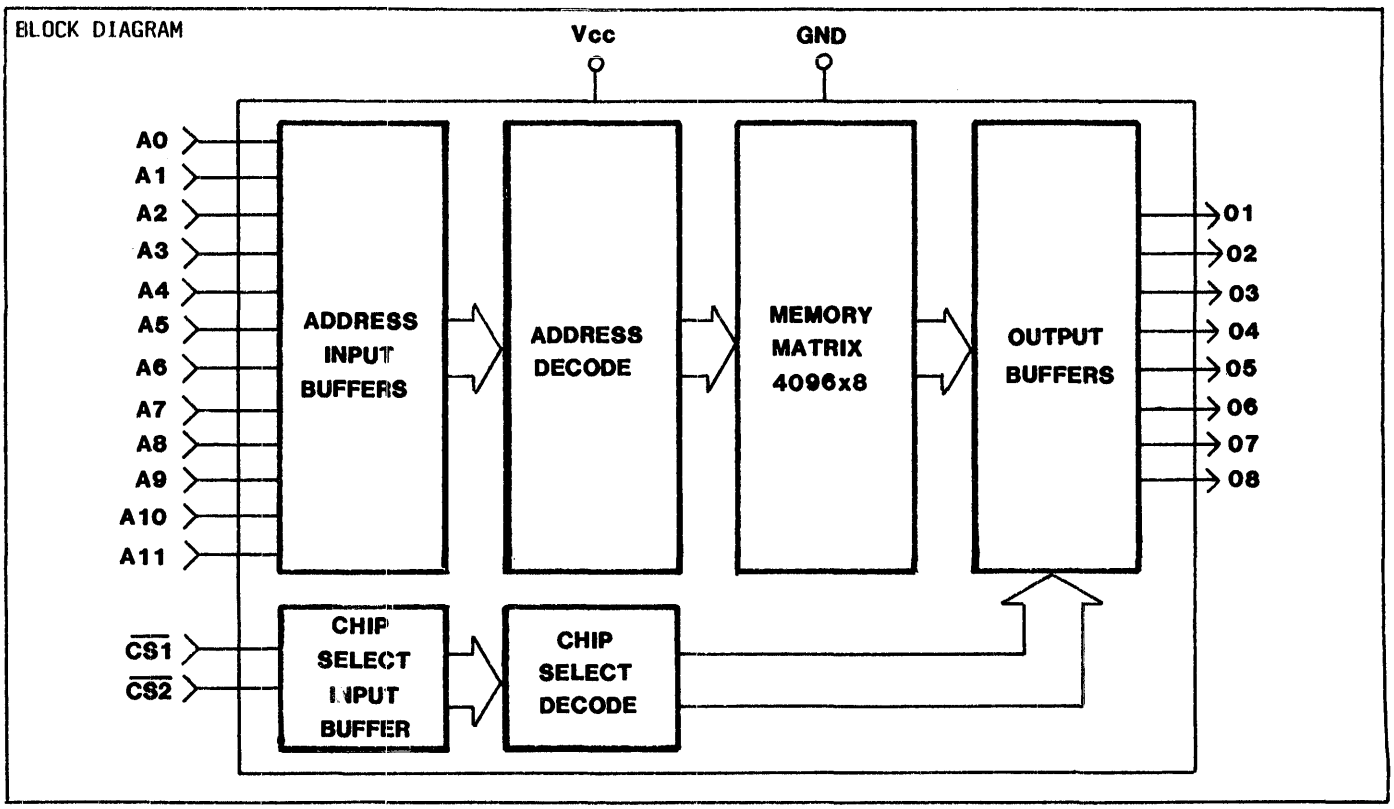
24 LEAD DUAL-IN-LINE



DESCRIPTION

The RO9432 is a 32,768 bit fully static Read Only Memory utilizing MOS N-Channel Silicon Gate Ion Implanted technology. It is organized 4096 words by 8 bits and operates from a single +5 Volt power supply with ±10% supply tolerance. All inputs are TTL compatible, and the three-state outputs can drive two standard TTL loads each.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Inut Voltages (with Respect to GND)..... -0.5V to +7.0V
Storage Temperature..... -65°C to +150°C

Standard Conditions (unless otherwise noted):
V_{CC} = +5V ±10%
Operating Temperature T_A = 0°C to +70°C
Output Loading Two TTL Loads + C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-0.5	-	0.8	V	
Input High Voltage	V_{IH}	2.0	-	V_{CC}	V	
Input Load Current	I_{IL}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Output Low Voltage	V_{OL}	-	-	0.40	V	I_{OL} = +3.2mA
Output High Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200µA
Output Leakage Current	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current	I_{CC}	-	-	100	mA	All Inputs +5.5V, Outputs Loaded

AC CHARACTERISTICS

		RO9432B		RO9432C		RO9432DS		RO9432D			
Characteristic	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	300	-	250	-	200	ns	
Chip Select Access Time	t_{ACS}	-	150	-	100	-	85	-	70	ns	
Chip Deselect Time	t_{OFF}	-	150	-	100	-	85	-	70	ns	
Output Hold After Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns	
Capacitance**											
Input Capacitance	C_{IN}	-	7	-	7	-	7	-	7	pf	T_A=25°C,F=1MHz
Output Capacitance	C_{OUT}	-	10	-	10	-	10	-	10	pf	T_A=25°C,F=1MHz

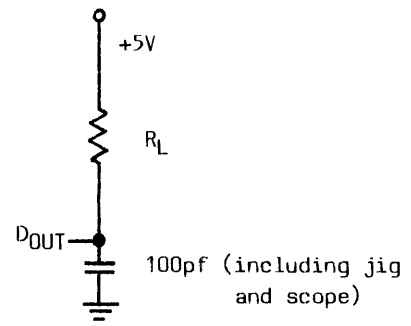
**Capacitance is periodically samples and is not 100% tested.

AC TEST CONDITIONS

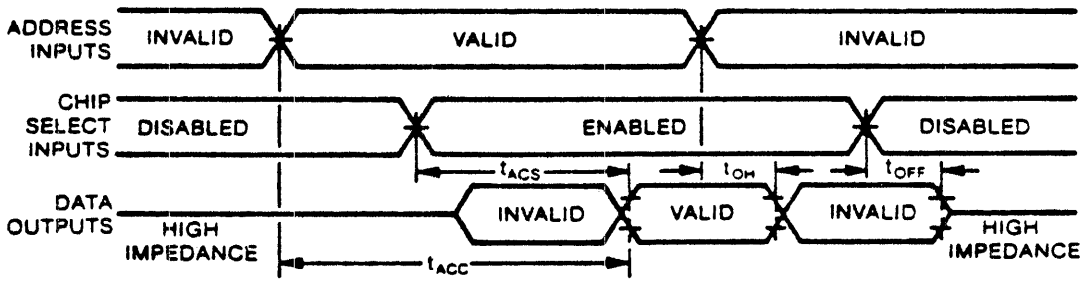
Input Pulse Levels..... 0.4V to 2.4V
Input Rise and Fall Times..... 10ns
Timing Measurement Levels:
  Input..... 1.5V
  Output..... 0.8V to 2.0V
Output Load..... 2TTL Loads +100pf (See Figure 1)

CONDITIONS OF TEST FOR AC CHARACTERISTICS

Figure 1



TIMING DIAGRAM



DEFINITIONS

Access Time, T_{ACC}
Access time is the maximum time between the application of a valid Address and the corresponding Data Out.

Output Hold After Address Change, T_{OH}
Output Hold After Address Change is the minimum time after an Address change that the previous data remains valid.

Chip Select Access Time, T_{ACS}
Chip Select Access Time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Chip Deselect Time, T_{OFF}
Chip Deselect Time is the delay between Chip Selects becoming false and output stages going to the high impdedance state.

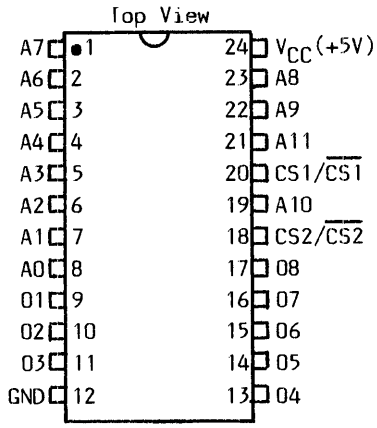
32,768 BIT STATIC READ ONLY MEMORY

FEATURES:

- 4096 x 8 organization
- Fully static operation - no clocks required
- Single +5V +10% supply
- 450ns access time: RO9433B
- 300ns access time: RO9433C
- 250ns access time: RO9433DS
- 200ns access time: RO9433D
- Inputs and outputs TTL compatible
- Three state outputs - under the control of two mask programmable chip select inputs
- Output drive capability of 2 TTL loads 100pf
- Low power dissipation
- Totally automated custom programming
- Pin compatible with 2732 EPROM
- ESD protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD 883

PIN CONFIGURATION

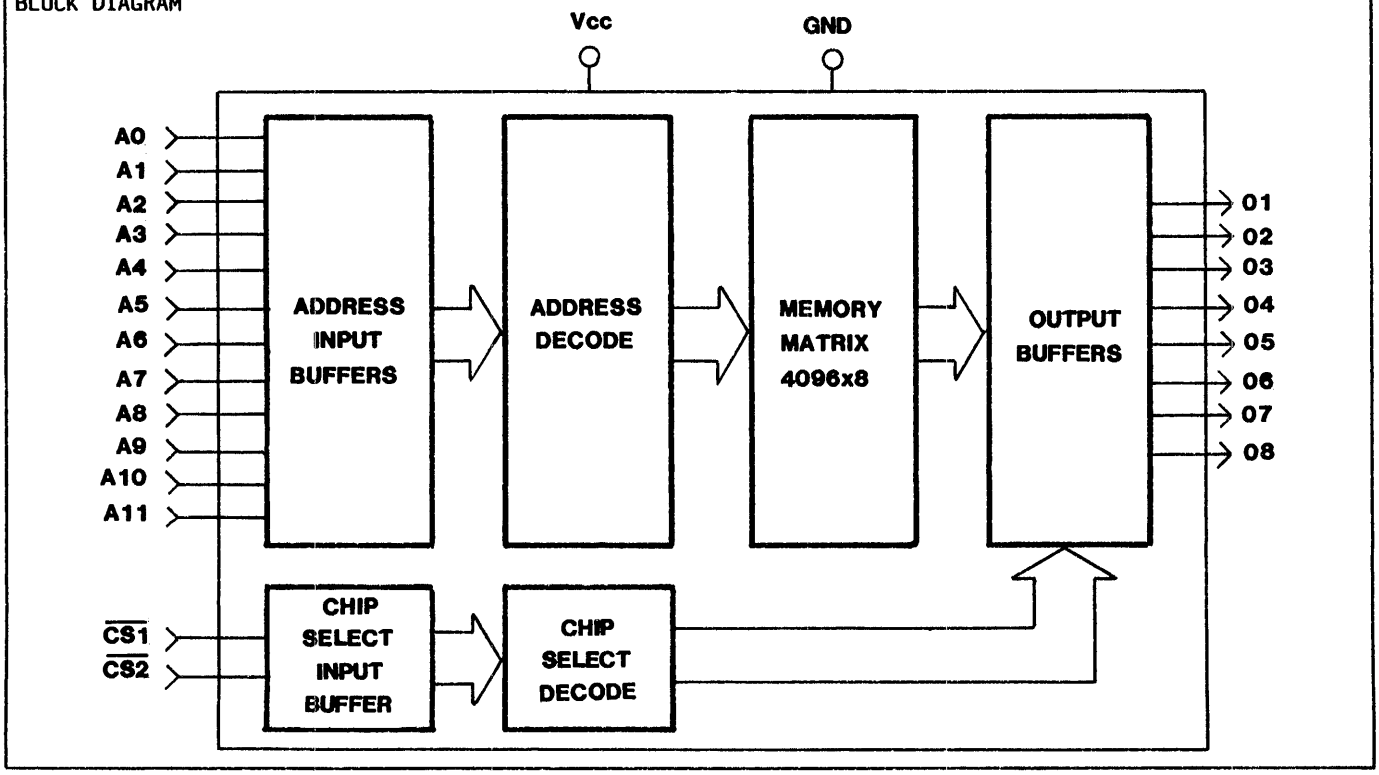
24 LEAD DUAL-IN-LINE



DESCRIPTION

The RO9433 is a 32,768 bit fully static Read Only Memory utilizing MOS N-Channel Silicon Gate Ion Implanted technology. It is organized 4096 words by 8 bits and operates from a single +5 Volt power supply with ±10% supply tolerance. All inputs are TTL compatible, and the three-state outputs can drive two standard TTL loads each.

BLOCK DIAGRAM



DS10003D-1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Inut Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±10%

Operating Temperature T_A = 0°C to +70°C

Output Loading Two TTL Loads + C_L TOTAL = 100pf

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, CHIP SELECTS Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-	-	10	µA	V_{IN} = 0.4V tp V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current	I_{CC}	-	-	100	mA	All inputs +5.5V, Outputs Unloaded

AC CHARACTERISTICS

		RO9433B		RO9433C		RO9433DS		RO9433D			
Characteristic	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	300	-	250	-	200	ns	
Chip Select Access Time	t_{ACS}	-	150	-	100	-	85	-	70	ns	
Chip Deselect Time	t_{OFF}	-	150	-	100	-	85	-	70	ns	
Output Hold After Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns	
Capacitance** Input Capacitance	C_{IN}	-	7	-	7	-	7	-	7	pf	T_A=25°C,F=1MHz
Output Capacitance	C_{OUT}	-	10	-	10	-	10	-	10	pf	T_A=25°C,F=1MHz

**Capacitance is periodically sampled and is not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels..... 0.4V to 2.4V

Input Rise and Fall Times..... 10ns

Timing Measurement Levels:

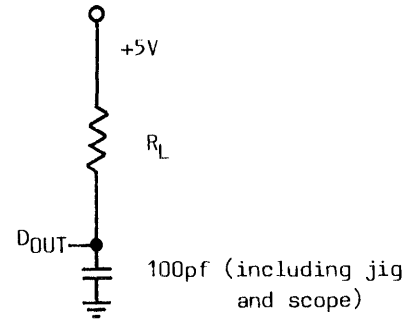
Input..... 1.5V

Output..... 0.8V to 2.0V

Output Load..... 2TTL Loads +100pf (See Figure 1)

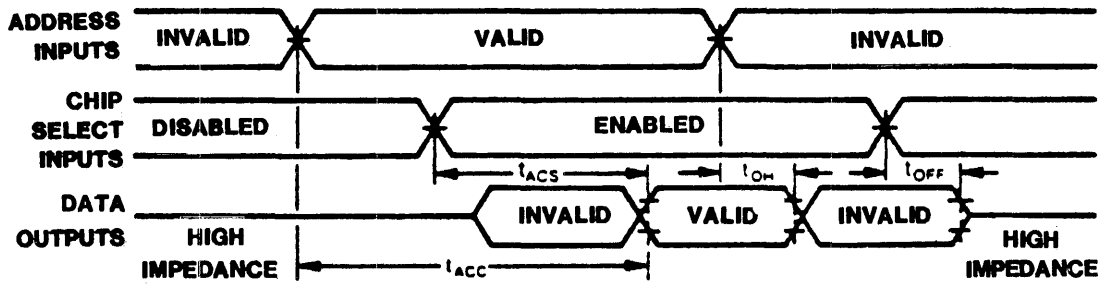
CONDITIONS OF TEST FOR AC CHARACTERISTICS

Figure 1



DS10003D-2

TIMING DIAGRAM



DEFINITIONS

Access Time, T_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding Data Out.

Output Hold After Address Change, T_{OH}

Output Hold After Address Change is the minimum time after an Address change that the previous data remains valid.

Chip Select Access Time, T_{ACS}

Chip Select Access Time is the maximum delay between Chip Selects becoming true and and Output Data becoming valid.

Chip Deselect Time, T_{OFF}

Chip Deselect Time is the delay between Chip Selects becoming false and output stages going to the high impdedance state.

65,536 BIT STATIC READ ONLY MEMORY

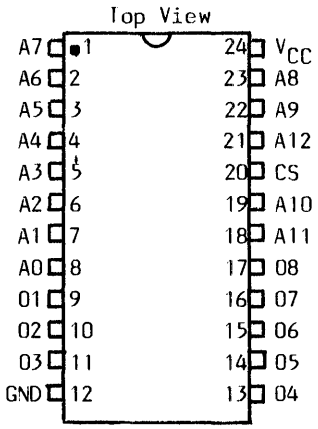
FEATURES:

- 8192 x 8 organization
- Fully static operation
- Single +5V ±10% / ±5% supply (RO94164)
- Inputs and outputs TTL compatible
- Three state outputs
- Output drive capability of 2 TTL/1 TTL Load and 100pf
- 24 pin JEDEC approved pinout
- ESD protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

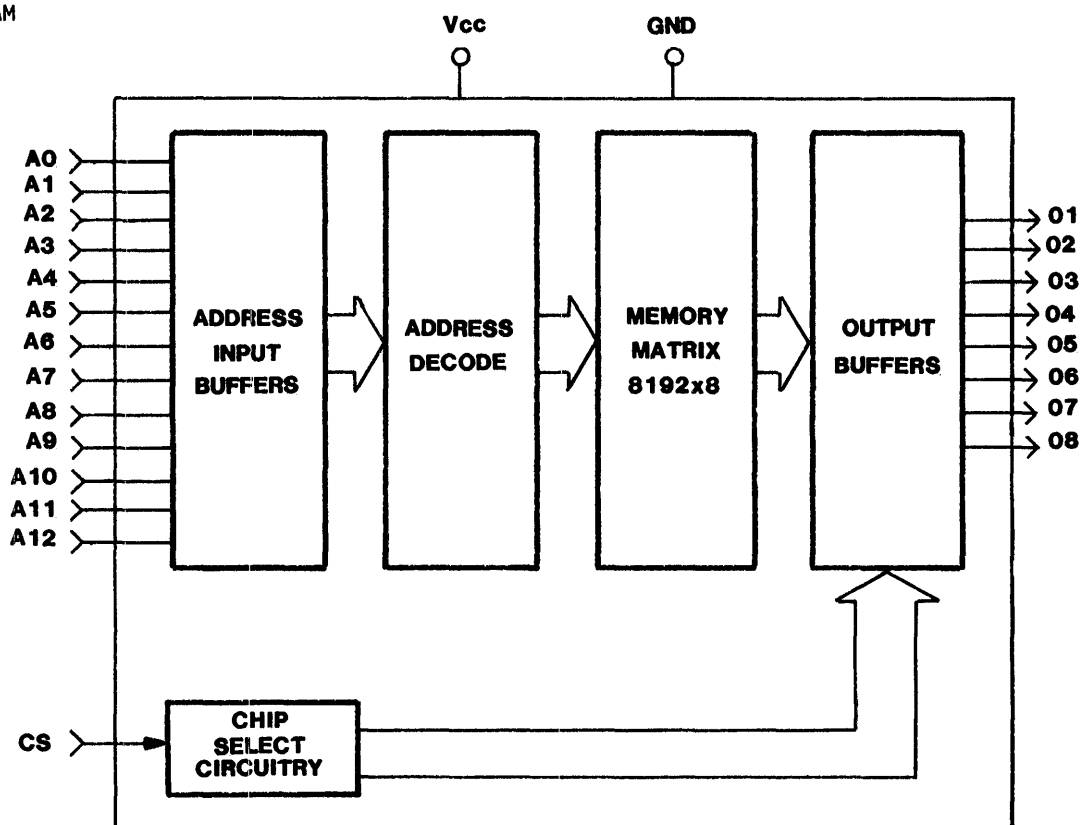
RO9464/RO94164



DESCRIPTION

The General Instrument RO9464 and RO94164 Series are 65,536 Bit Static Read Only Memories organized as 8192 eight-bit words and are ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate technology, the RO9464 and RO94164 Series provide the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 volt power supply and low power dissipation. The RO9464 and RO94164 Series offer the best combination of high performance, large bit storage and simple interfacing of any MOS Read Only Memory available today.

BLOCK DIAGRAM



DS10006B-1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature..... -65°C to +150°C
V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V
Power Dissipation..... 1.0W

Standard Conditions (unless otherwise noted):
Operating Temperature T_A = 0°C to +70°C
V_{CC} = +5V ±10% / ±5% (RO94164)

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Output High Level	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200µA/-100µA (RO94164)
Output Low Level	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA/1.6mA (RO94164)
Input High Level	V_{IH}	2.0	-	V_{CC}	V	
Input Low Level	V_{IL}	-	-	0.8	V	
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Operating Supply Current	I_{CC}	-	-	100	mA	Note 1, V_{OUT} = 5.5/5.25V (RO94164)

AC CHARACTERISTICS

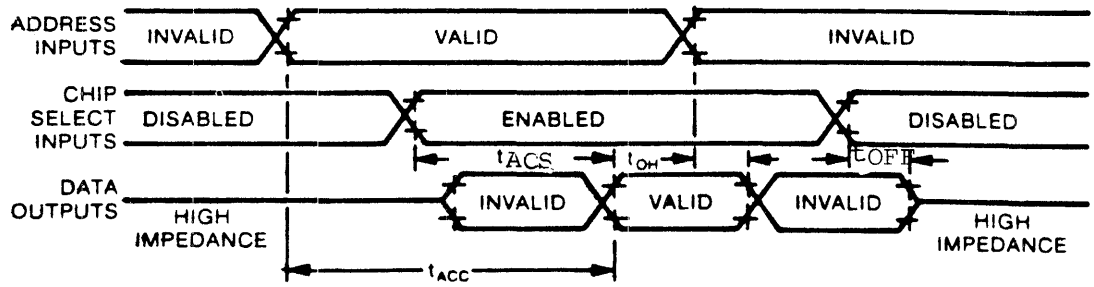
		RO9464B RO94164B		RO9464CS RO94164CS		RO9464C RO94164C		RO9464DS			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	ns	
Output Hold After Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns	Note 2
Chip Select Access Time	t_{ACS}	-	150	-	125	-	100	-	100	ns	
Output Disable Time	t_{OFF}	-	150	-	125	-	100	-	100	ns	
Capacitance**											
Input Capacitance	C_I	-	7	-	7	-	7	-	7	pf	F=1.0MHz, T_A = +25°C
Output Capacitance	C_O	-	10	-	10	-	10	-	10	pf	F=1.0MHz, T_A = +25°C

**Capacitance is periodically sampled and is not 100% tested.

NOTES:
1. Measured with device selected and outputs unloaded.
2. This parameter is periodically sampled and is not 100% tested.

PART NUMBER	MAXIMUM ACCESS TIME	V_{CC} SUPPLY TOLERANCE	TTL LOADS
RO94164B	450ns	5%	1
RO94164CS	350ns	5%	1
RO94164C	300ns	5%	1
RO9464B	450ns	10%	2
RO9464CS	350ns	10%	2
RO9464C	300ns	10%	2
RO9464DS	250ns	10%	2

TIMING DIAGRAM



DEFINITIONS

Access Time, T_{ACC}
Access time is the maximum time between the application of a valid Address and the corresponding Data Out.

Output Hold Delay, T_{OH}
Output hold delay is the minimum time after an address change that the previous data remains valid.

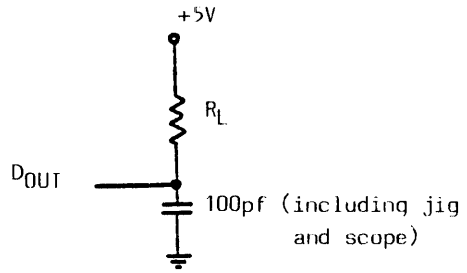
Chip Select to Output Time, T_{ACS}
CS is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Chip Deselect Time, T_{OFF}
Chip deselect time is the delay between Chip Selects becoming false and output stages going to the high impdedance state.

AC TEST CONDITIONS

Input Pulse Levels..... 0.8V to 2.0V
Input Rise and Fall Times..... $\leq$ 10 nsec
Timing Measurement Levels:... Output 0.8V and 2.0V
Output Load..... See Figure 1

FIGURE 1



65,536 BIT STATIC READ ONLY MEMORY

FEATURES:

- 8192 x 8 organization
- Fully static operation
- Single +5V ± 10% supply
- Inputs and outputs TTL compatible
- Three state outputs
- 28 pin JEDEC approved pinout (RO9864A)
- ESD protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883

DESCRIPTION

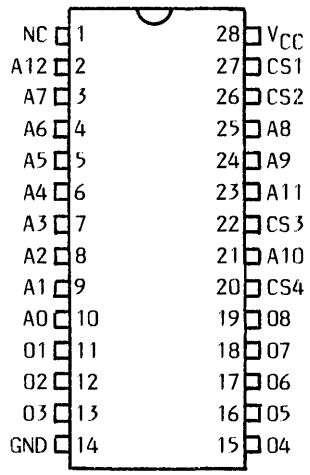
The General Instrument RO9864 and RO9864A series are 65,536 bit static read only memories organized as 8192 eight-bit words and are ideally suited for microprocessor memory applications fabricated with General Instrument N-channel silicon gate technology, the RO9864 and RO9864A series provide the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 volt power supply and a low power dissipation. The RO9864 and RO9864A series offer the best combination of high performance, large bit storage and simple interfacing of any MOS read only memory available today.

The RO9864 series provides four fully programmable chip selects (CS3 and CS4 are on Pins 22 and 20 respectively) which enables a memory system to contain up to sixteen RO9864s without using any external address decode circuitry.

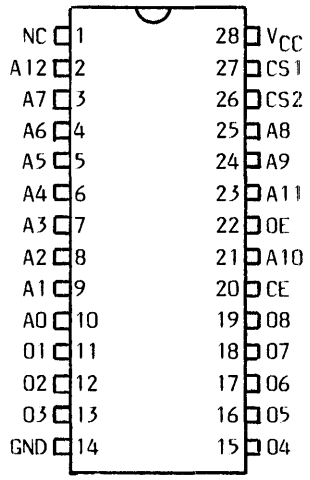
The RO9864A series offers an automatic down feature. Power down is controlled by Pin 20, the Chip Enable (CE) input. When CE goes high, the device will power down and remain in a low power standby mode as long as CE remains high. Pin 22 provides the Output Enable (OE) function allowing additional bus control.

PIN CONFIGURATION
28 LEAD DUAL-IN-LINE

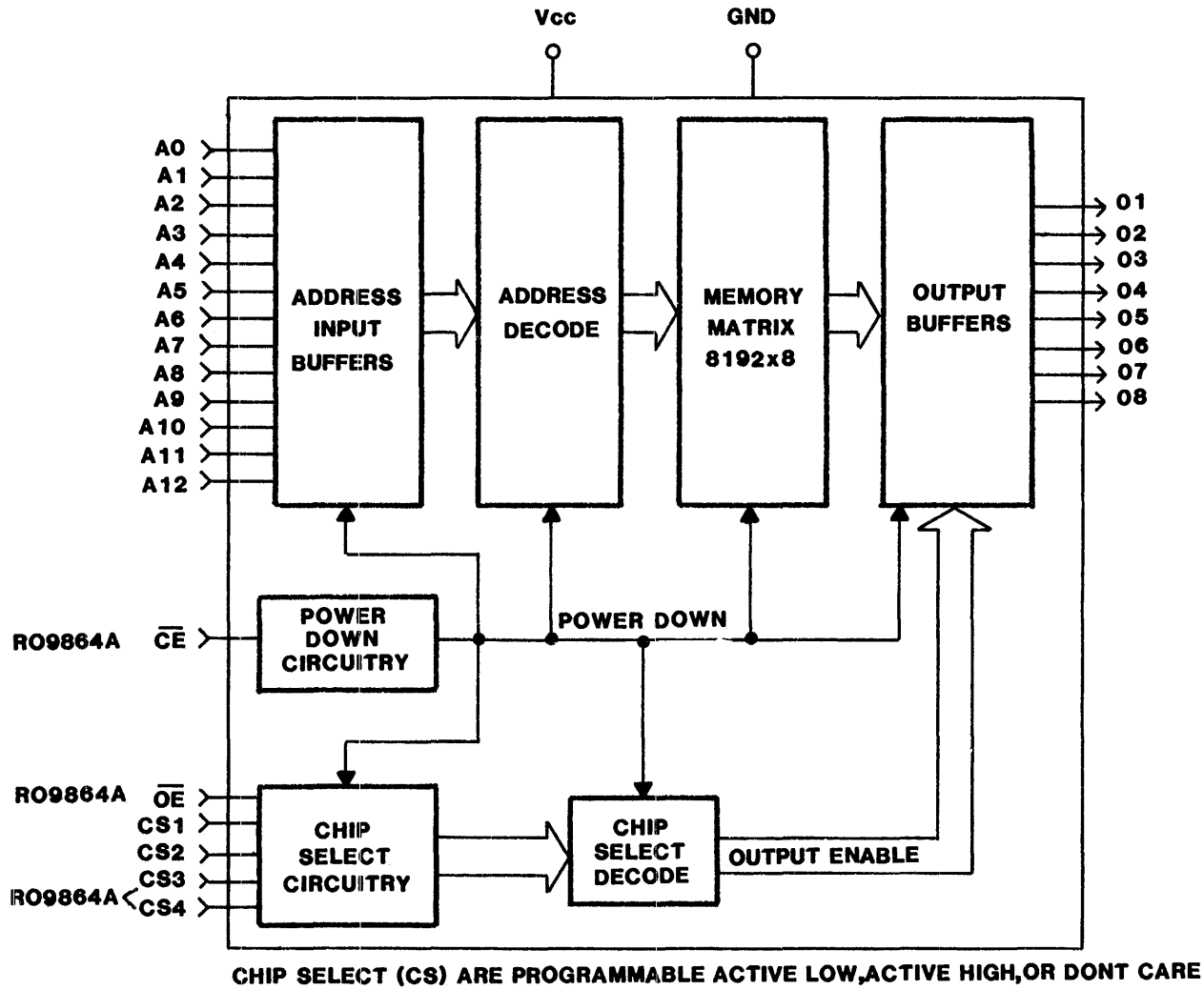
RO9864 Top View



RO9864A Top View



BLOCK DIAGRAM



CHIP SELECT (CS) ARE PROGRAMMABLE ACTIVE LOW,ACTIVE HIGH,OR DONT CARE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature..... -65°C to +150°C
V_{CC} and Applied Voltages
(with respect to GND)..... -0.5V to +7.0V
Power Dissipation..... 1.0W

Standard Conditions (unless otherwise noted):
Operating Temperature T_A = 0°C to +70°C
V_{CC} = +5V ± 10%

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Output High Level	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200µA
Output Low Level	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Input High Level	V_{IH}	2.0	-	V_{CC}	V	
Input Low Level	V_{IL}	-0.5	-	0.8	V	
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Operating Supply Current	I_{CC}	-	-	100	mA	Note 1
Standby Supply Current	I_{SB}	-	-	12	mA	Note 2

AC CHARACTERISTICS

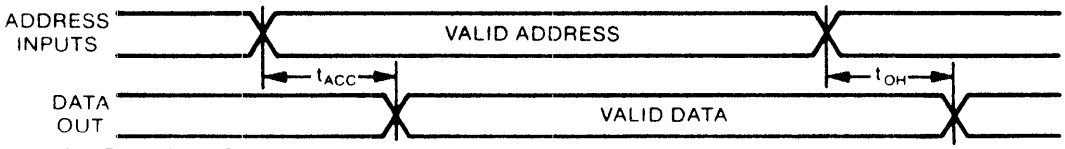
		RO9864B RO9864AB		RO9864CS RO9864ACS		RO9864C RO9864AC		RO9864DS RO9864ADS		RO9864D RO9864AD			
Characteristic	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Output Hold After Address Change	t_{OH}	10	-	10	-	10	-	10	-	5	-	ns	
Chip Enable Access Time	t_{ACE}	-	450	-	350	-	300	-	250	-	200	ns	Note 3
Chip Select Access Time	t_{ACS}	-	150	-	125	-	100	-	100	-	85	ns	
Output Enable Access Time	t_{AOE}	-	150	-	125	-	100	-	100	-	85	ns	Note 3
Output Low Z Delay	t_{LZ}	10	-	10	-	10	-	10	-	5	-	ns	Note 4
Output High Z Delay	t_{HZ}	-	150	-	125	-	100	-	85	-	85	ns	Note 5

NOTES:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. Applies to "A" versions only.
4. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and $\overline{CS}$ going active, whichever occurs last.
5. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or $\overline{CS}$ going inactive, whichever occurs first.

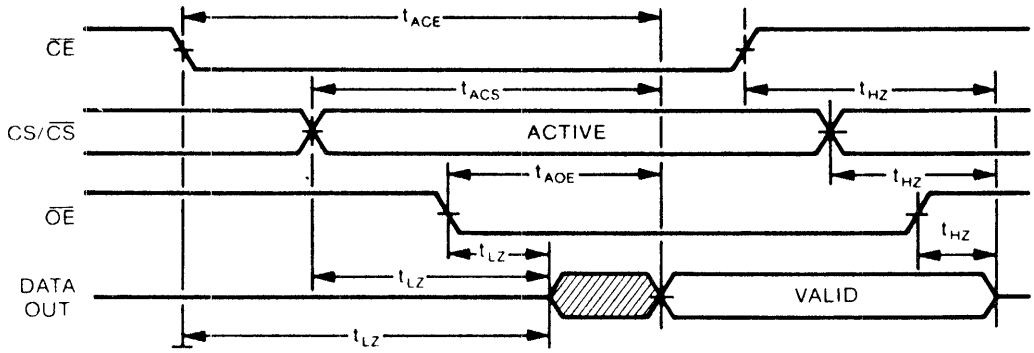
PART NUMBER	MAXIMUM ACCESS TIME	OPERATING CURRENT	STANDBY CURRENT
R09864B	450ns	100mA	NA
R09864CS	350ns	100mA	NA
R09864C	300ns	100mA	NA
R09864DS	250ns	100mA	NA
R09864D	200ns	85mA	NA
R09864AB	450ns	100mA	12mA
R09864ACS	350ns	100mA	12mA
R098964AC	300ns	100mA	12mA
R09864ADS	250ns	100mA	12mA
R09864AD	200ns	85mA	12mA

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW,CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	See Figure 1

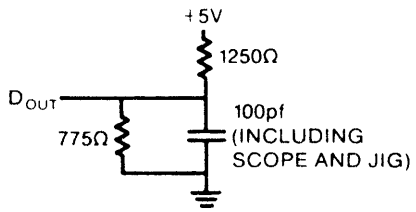


Fig. 1

131,072 BIT STATIC READ ONLY MEMORY

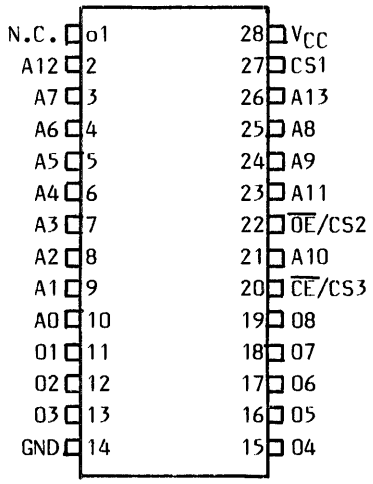
FEATURES

- 16,384 x 8 organization
- Single +5V ±10% volt supply
- 450ns max access time: RO9128B
- 350ns max access time: RO9128CS
- 300ns max access time: RO9128C
- 250ns max access time: RO9128DS
- 200ns max access time: RO9128D
- Totally static operation
- Three state outputs
- All TTL compatible inputs/outputs
- 28 pin JEDEC approved pinout
- Programmable "FlexSelect"™ chip enable/disable/power down capabilities controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883B

PIN CONFIGURATION

28 LEAD DUAL-IN-LINE

Top View



DESCRIPTION

The General Instrument RO9128 is a 131,072 Bit Static Read Only Memory organized as 16,384 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9128 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

The RO9128 offers a programmable "Flexselect"™ chip enable/disable/power down feature controlled by the chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and chip select (CS) inputs. These inputs can be programmed to implement various logic functions which provides the designer with a flexible and easy means of "chip selecting" and/or "powering down" the device. The chip select options are as shown on the following pages.

I) *Standard Chip Select requirements - Non-Power Down

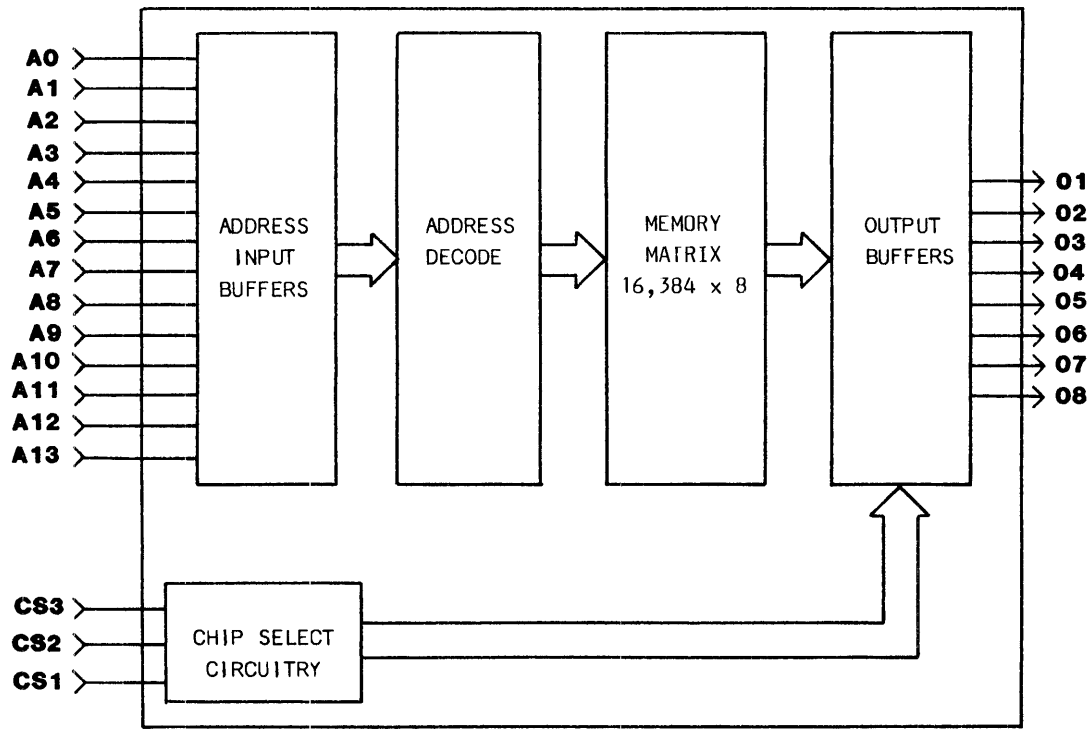
CS1 = 0,1 or don't care (Pin 27)
CS2 = 0,1 or don't care (Pin 22)
CS3 = 0,1 or don't care (Pin 20)

Logic Function $^{1}(CS1)\cdot{}^{1}(CS2)\cdot{}^{1}(CS3)$ = Chip Selected

^{1} Programmed in active state
"." = Logical "AND"

*Not available on "D" speed devices

BLOCK DIAGRAM



Chip selects (CS1, CS2, CS3) are programmable active low, active high or don't care.

II) Standard Chip Select requirements - Power Down

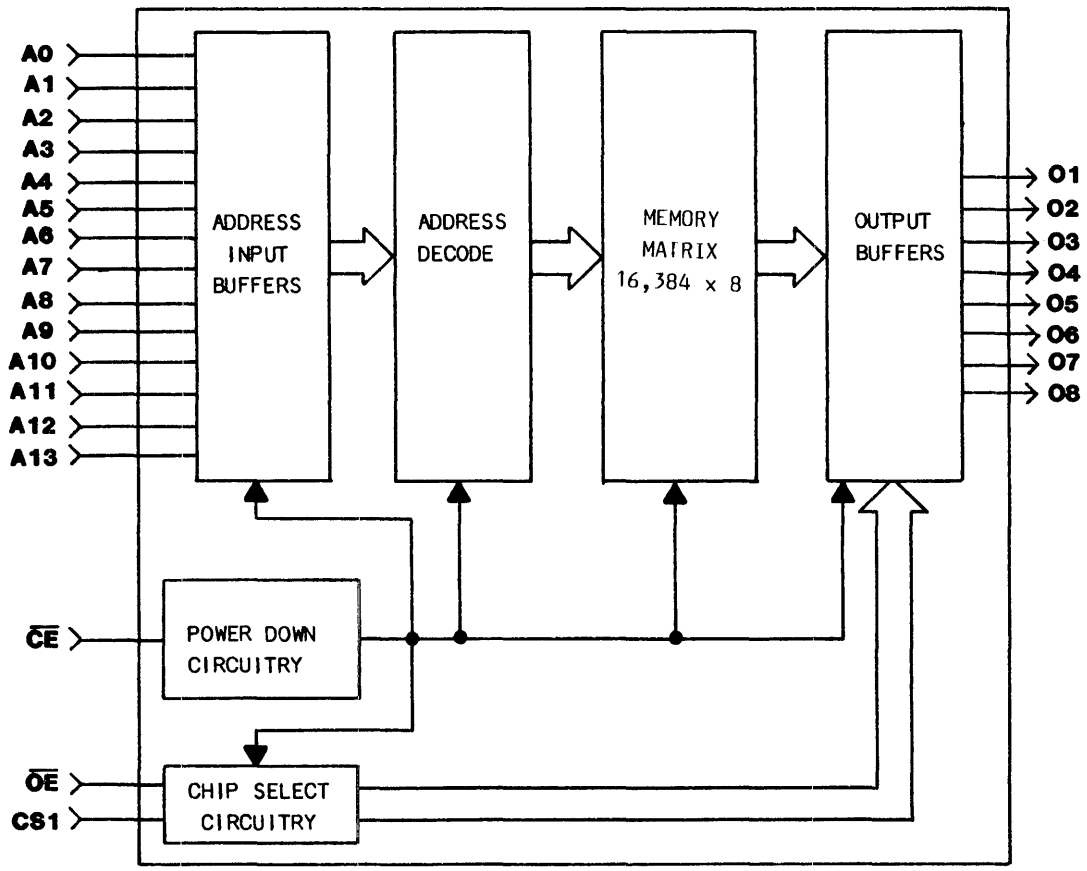
CS1 = 0,1 or don't care (Pin 27)

$\overline{OE}$ (Pin 22) When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power
$\overline{CE}$ (Pin 20) standby mode as long as $\overline{CE}$ remains high. $\overline{OE}$ and CS functions eliminate bus contention in multiple memory device systems.

Logic Function: $^{1}(CS1)\cdot(\overline{CE})\cdot(\overline{OE})$ = Chip Selected

[1]Programmed in active state
"." = LOGICAL "AND"

BLOCK DIAGRAM



Chip select (CS1) is programmable active low, active high, or don't care.

III) **"ORED" chip select requirement (chip selects at pins 20 (CE) and 22 (OE) function as a logical "OR").

* This is ideally suited for applications that have limited chip select decoding capabilities.

CS1 = 0,1 or don't care (Pin 27)

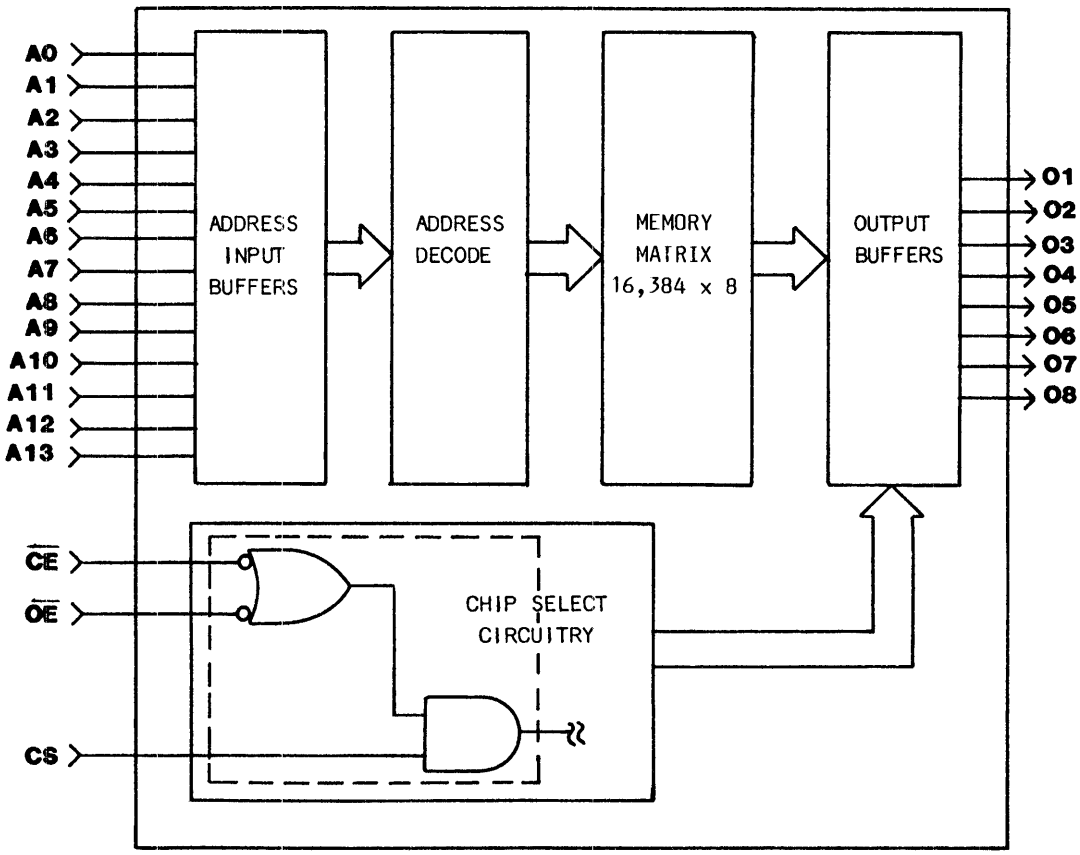
Logic Function: [1](CS).(CE + OE) = Chip Selected

[1]Programmed in active state

"." = LOGICAL "AND"
"+" = LOGICAL "OR"

**Not available on "D" speed devices

BLOCK DIAGRAM



Chip Select (CS1) is programmable active low, active high, or don't care.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to + 150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ±10%

Operating Temperature T_A = 0°C to + 70°C

Output Loading: Two TTL Loads, C_L TOTAL = 100pf

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, CE/CS3, OE/CS2, CS1 Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-10	-	+10	µA	V_{IN}=0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH}=-200µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL}=3.2mA
Leakage	I_{LO}	-10	-	+10	µA	V_{OUT}=0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	-	-	-	100	mA	Note 1
I_{CC} (Standby)	-	-	-	15	mA	Note 2,6
I_{CC} (Standby)	-	-	-	50	mA	Note 7

AC CHARACTERISTICS

		R09128B		R09128CS		R09128C		R09128DS		R09128D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Address Hold After Address Change	t_{OH}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Chip Enable Time	t_{ACE}	-	450	-	350	-	300	-	250	-	208	ns	
Chip Select, Output Enable Access Time	t_{ACS}	-	150	-	125	-	100	-	85	-	70	ns	Note 4
Output Disable Time	t_{OFF}	-	150	-	125	-	100	-	85	-	70	ns	
Output Low Z Delay	t_{LZ}	10	-	10	-	5	-	5	-	5	70	ns	Note 3
Output High Z Delay	t_{HZ}	-	150	-	125	-	100	-	85	-	70		
Capacitance***													
Input Capacitance	C_I	-	7	-	7	-	7	-	7	-	7	pf	F=1MHz, T_A=+25°C
Output Capacitance	C_O	-	10	-	10	-	10	-	10	-	10	pf	F=1MHz, T_A=+25°C

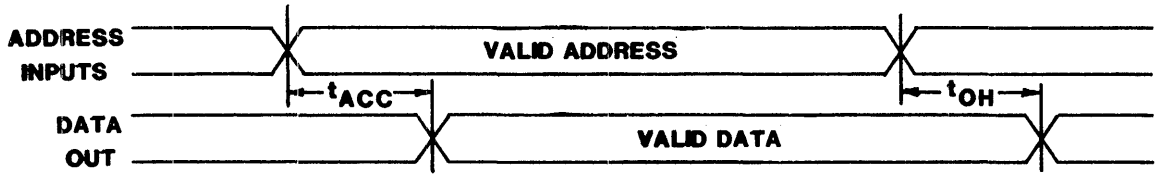
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

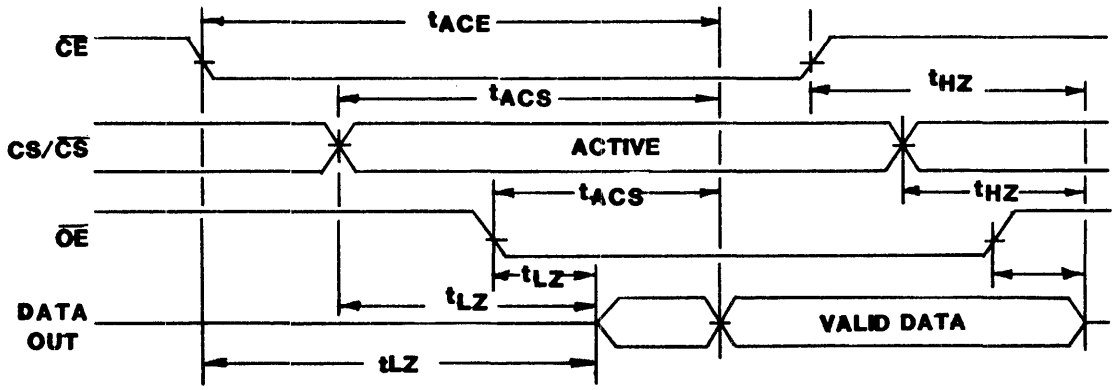
1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq$ 2.0V ("Power Down" programmed parts only).
3. These parameters are periodically sampled and are not 100% tested.
4. Access time to valid data measured from CS1 going active and/or $\overline{OE}$ going low which ever occurs last/first.
5. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ and/or $\overline{OE}$ going high or CS1 going active, which ever occurs last/first.
6. Applies to B, CS, and C speeds only.
7. Applies to DS, D speeds only.

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5/10ns
Timing Measurement Levels: Input/Output	0.8V AND 2.0V
Output Load	See Figure 1

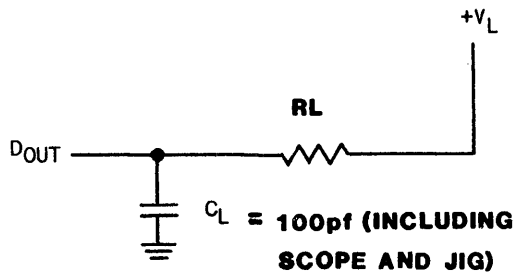


Fig. 1

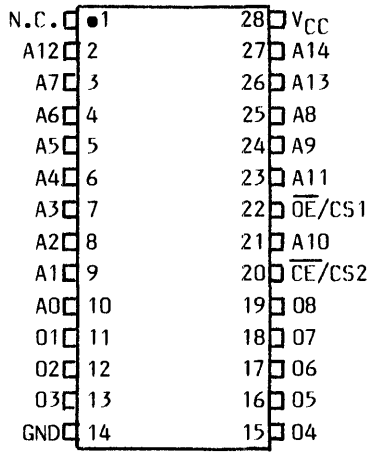
262,144 BIT STATIC READ ONLY MEMORY

FEATURES:

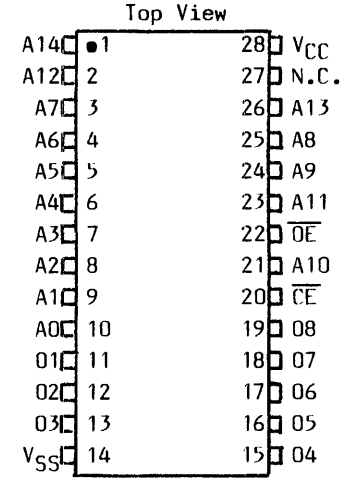
- 32,768 x 8 organization
- Single +5V ±10% supply
- 450ns max access time: RO9256B
- 350ns max access time: RO9256CS
- 300ns max access time: RO9256C
- 250ns max access time: RO9256DS
- 200ns max access time: RO9256D
- Totally static operation
- Three state outputs
- All TTL compatible input/outputs
- 28 Pin JEDEC approved pinout: RO9256
- Programmable "FlexSelect"™ chip enable/disable/power down capabilities controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883B
- Alternate 28 pin Mostek compatible pinout (RO9256A) available for DS/D speeds only

PIN CONFIGURATION
28 LEAD DUAL-IN-LINE

RO9256 — Top View



RO9256A — Top View



DESCRIPTION

The General Instrument RO9256 is a 262,144 Bit Static Read Only Memory organized as 32,768 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9256 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

Operation

Address (A0-A14)
The address-valid interval determines the device cycle time. The 15-bit positive logic address is decoded on-chip to select on the 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most significant bit of the word address.

Chip Select

Chip enable/disable/power down "FlexSelect"™. These inputs can be programmed during mask fabrication to implement various logic functions which provides the designer with a flexible and easy means of "chip selecting" and/or "powering down" the device. The "FlexSelect"™ options are on the following pages.

I) Standard Chip Select requirements - Non-Power Down

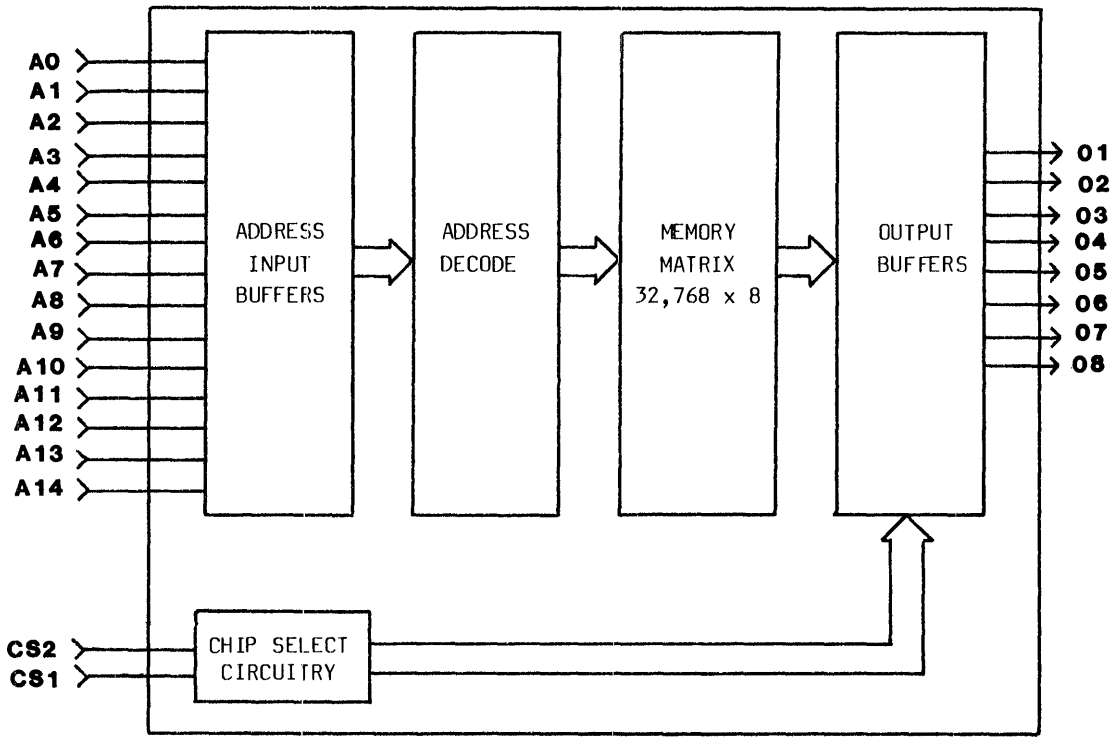
CS1 = 0,1 or don't care (Pin 22)
CS2 = 0,1 or don't care (Pin 20)

Logic Function ^{1}(CS1)•^{1}(CS2) = Chip Selected

^{1} Programmed in active state
"•" = Logical "AND"

* Not available for "D" speed devices
**Not available for Mostek pinout device, RO9256A

BLOCK DIAGRAM



Chip selects (CS1, CS2) are programmable active low, active high or don't care.

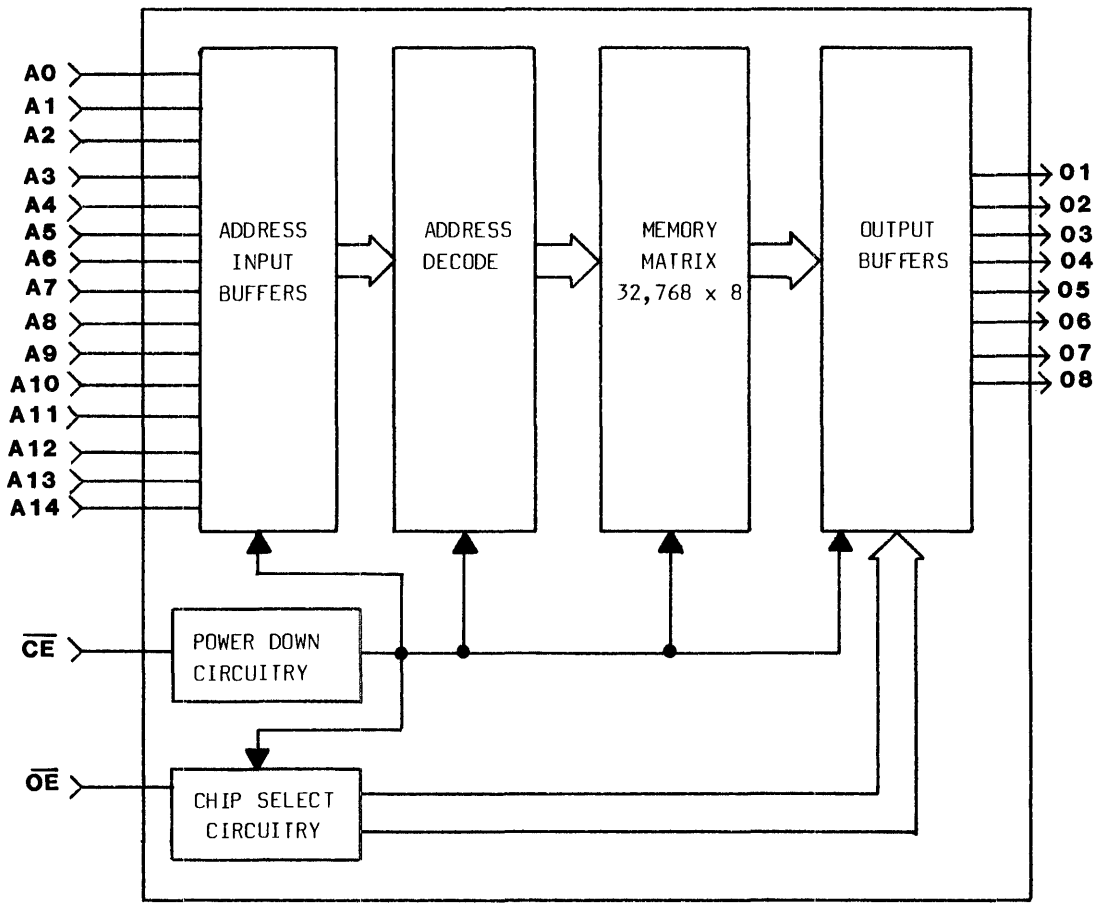
II) Standard Chip Select requirements - Power Down

$\overline{OE}$ (Pin 22) When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power
$\overline{CE}$ (Pin 20) standby mode as long as $\overline{CE}$ remains high. The $\overline{OE}$ function eliminates bus contention in multiple memory device systems.

Logic Function: $(\overline{CE})\bullet(\overline{OE})$ = Chip Selected

"•" = LOGICAL "AND"

BLOCK DIAGRAM



DS10015B-3

III) "ORED" chip select requirement (chip selects at pins 20 ($\overline{CE}$) and 22 ($\overline{OE}$) function as a logical "OR").

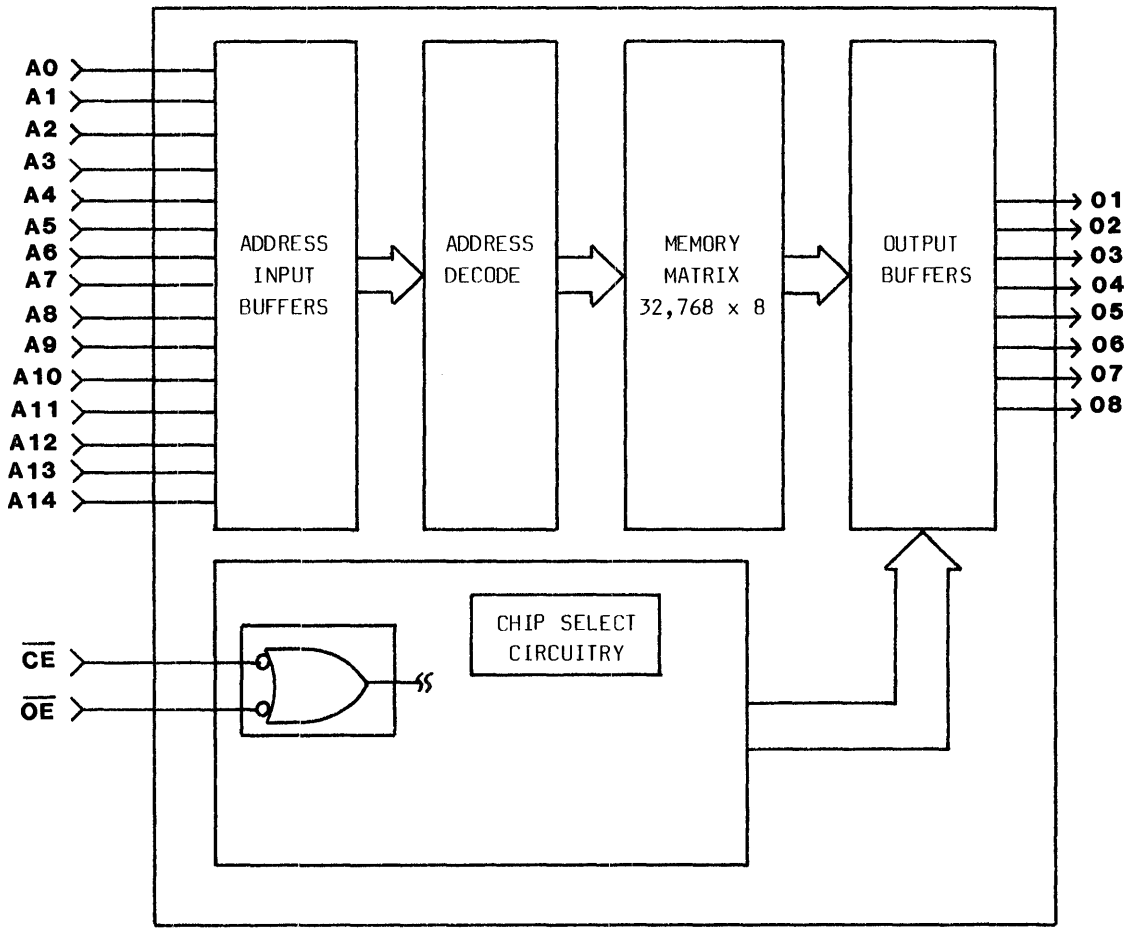
*This is ideally suited for applications that have limited chip select decoding capabilities.

Logic Function: ($\overline{CE}$ + $\overline{OE}$) = Chip Selected

"+" = LOGICAL "OR"

** Not available for D speed devices
***Not available for Mostek pinout device, RO9256A

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ±10%

Operating Temperature T_A = 0°C to + 70°C

Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS2, $\overline{OE}$/CS1 Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-10	-	+10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	-10	-	+10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	-	-	-	100	mA	Note 1
I_{CC} (Standby)	-	-	-	20	mA	Note 2
I_{CC} (Standby) D-speed only	-	-	-	50	mA	Note 2

AC CHARACTERISTICS		RO9256B		RO9256CS		RO9256C		RO9256DS		RO9256D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Address Hold After Address Change	t_{OH}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Chip Enable Time	t_{ACE}	-	450	-	350	-	300	-	250	-	200	ns	
Chip Select, Output Enable Access Time	t_{ACS}	-	150	-	125	-	100	-	85	-	70	ns	Note 4
Output Disable Time	t_{OFF}	-	150	-	125	-	100	-	85	-	70	ns	
Output Low Z Delay	t_{LZ}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Output High Z Delay	t_{HZ}	-	150	-	125	-	100	-	85	-	70	ns	Note 5
Capacitance***													
Input Capacitance	C_I	-	7	-	7	-	7	-	7	-	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	-	10	-	10	-	10	-	10	-	10	pf	F = 1MHz, T_A = +25°C

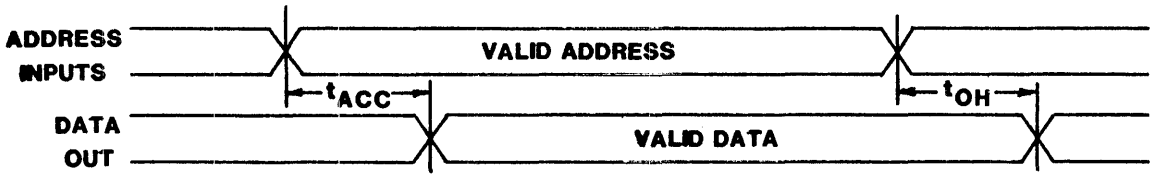
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

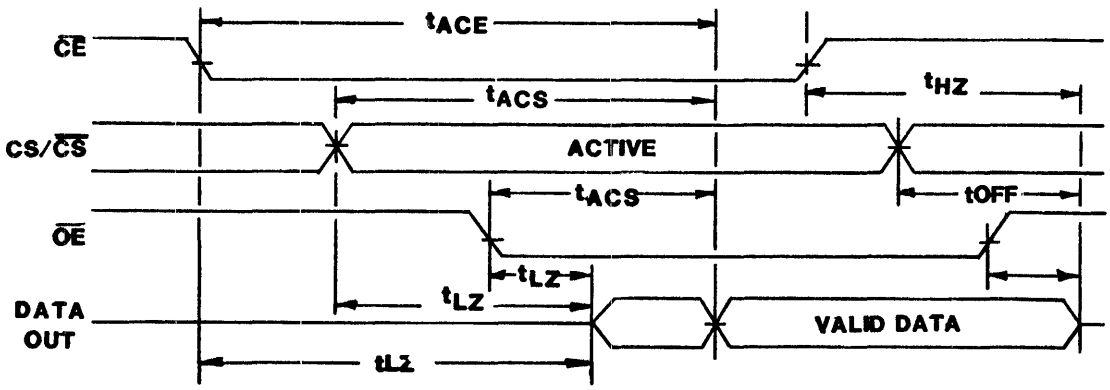
1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq$ 2.0V ("Power Down" programmed parts only).
3. These parameters are periodically sampled and not 100% tested.
4. Access time to valid data measured from CS1 going active and/or $\overline{OE}$ going low whichever occurs last/first.
5. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ and/or $\overline{OE}$ going high or CS1 going active, which ever occurs first/last.

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5/10ns
Timing Measurement Levels: Input/Output	0.8V AND 2.0V
Output Load	See Figure 1

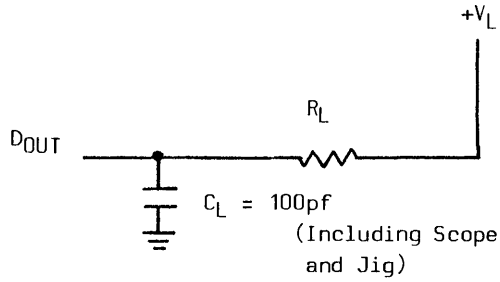


Fig. 1

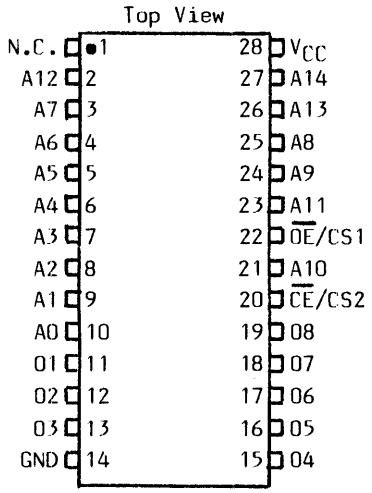
262,144 BIT STATIC READ ONLY MEMORY

FEATURES:

- 32,768 x 8 organization
- Single +5 Volt Supply
- 450ns max access time: ROC256B
- 350ns max access time: ROC256CS
- 300ns max access time: ROC256C
- 250ns max access time: ROC256DS
- 200ns max access time: ROC256D
- Totally static operation
- Three state outputs
- All TTL compatible input/outputs
- 28 Pin JEDEC approved pinout
- Programmable "FlexSelect"™ chip enable/disable/power down capabilities controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883B
- Low Power Dissipation:
  I_{CC} (Active) max @ 5.5V, 0°C = 40mA,
  I_{CC} (Standby) max @ 5.5V, 0°C = 1mA

PIN CONFIGURATION

28 LEAD DUAL-IN-LINE



DESCRIPTION

The General Instrument ROC256 is a 262,144 Bit CMOS Static Read Only Memory organized as 32,768 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument CMOS Silicon Gate Technology, the ROC256 provides the designer with a high performance, easy to use CMOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

Operation

Address (A0-A14)
The address-valid interval determines the device cycle time. The 15-bit positive logic address is decoded on-chip to select on the 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most significant bit of the word address.

Chip Select

Chip enable/disable/power down "FlexSelect"™. These inputs can be programmed during mask fabrication to implement various logic functions which provides the designer with a flexible and easy means of "chip selecting" and/or "powering down" the device. The "FlexSelect"™ options are explained on the following pages.

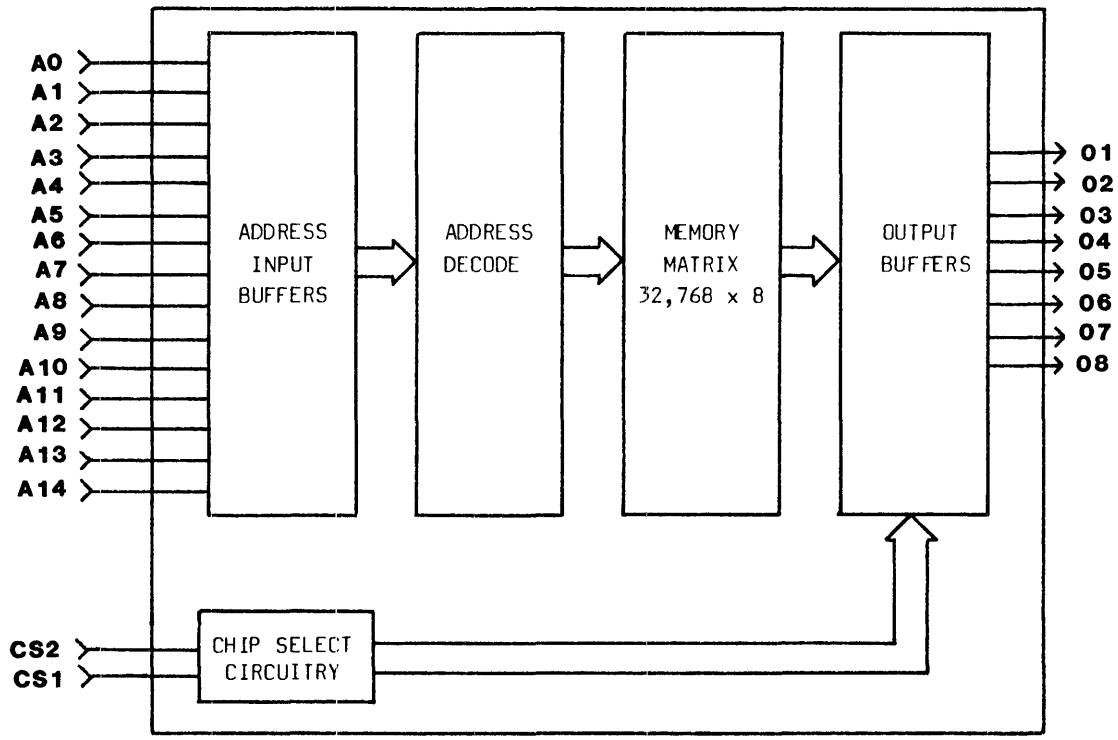
I) Standard Chip Select requirements - Non-Power Down

CS1 = 0,1 or don't care (Pin 22)
CS2 = 0,1 or don't care (Pin 20)

Logic Function ^{1}(CS1).^{1}(CS2) = Chip Selected

^{1} Programmed in active state
"." = Logical "AND"

BLOCK DIAGRAM



Chip selects (CS1, CS2) are programmable active low, active high or don't care.

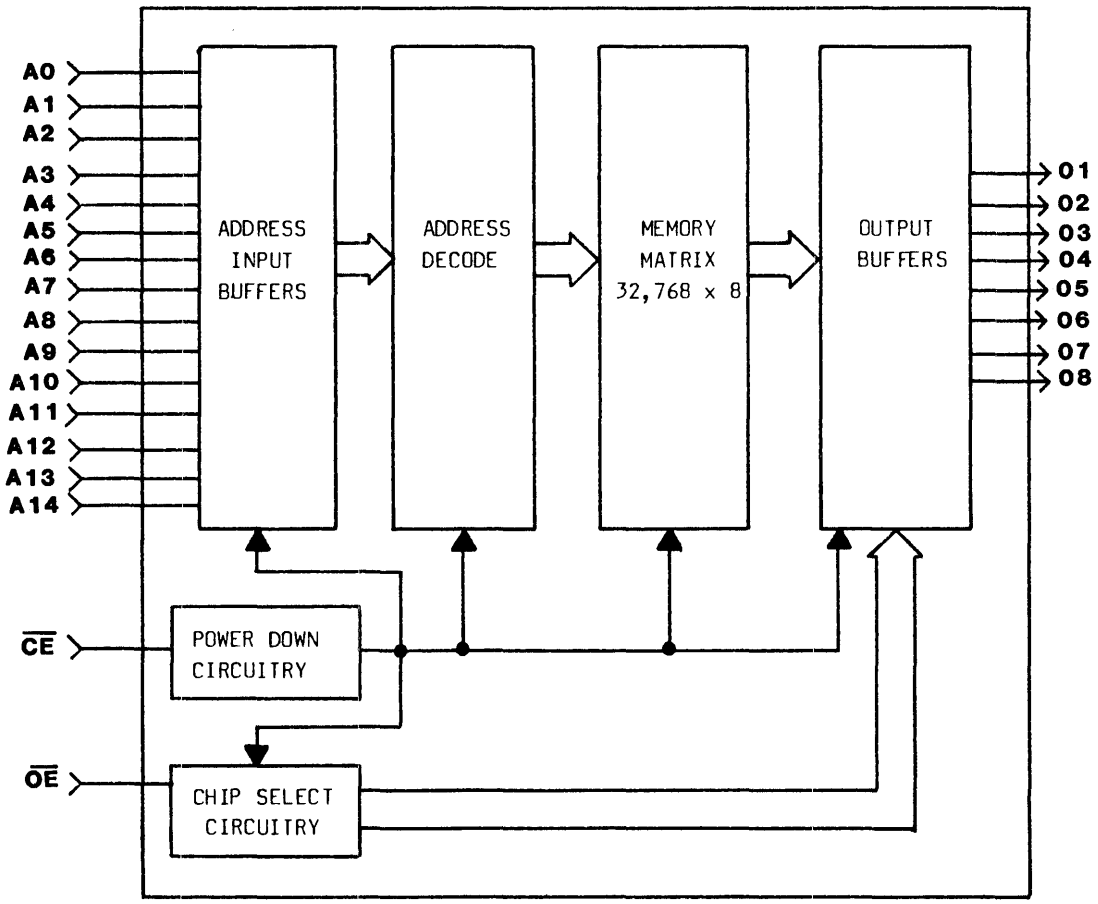
II) Standard Chip Select requirements - Power Down

$\overline{OE}$ (Pin 22) When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power
$\overline{CE}$ (Pin 20) standby mode as long as $\overline{CE}$ remains high. The $\overline{OE}$ function eliminates bus contention in multiple memory device systems.

Logic Function: $(\overline{CE})\cdot(\overline{OE})$ = Chip Selected

"." = LOGICAL "AND"

BLOCK DIAGRAM



DS10018A-3

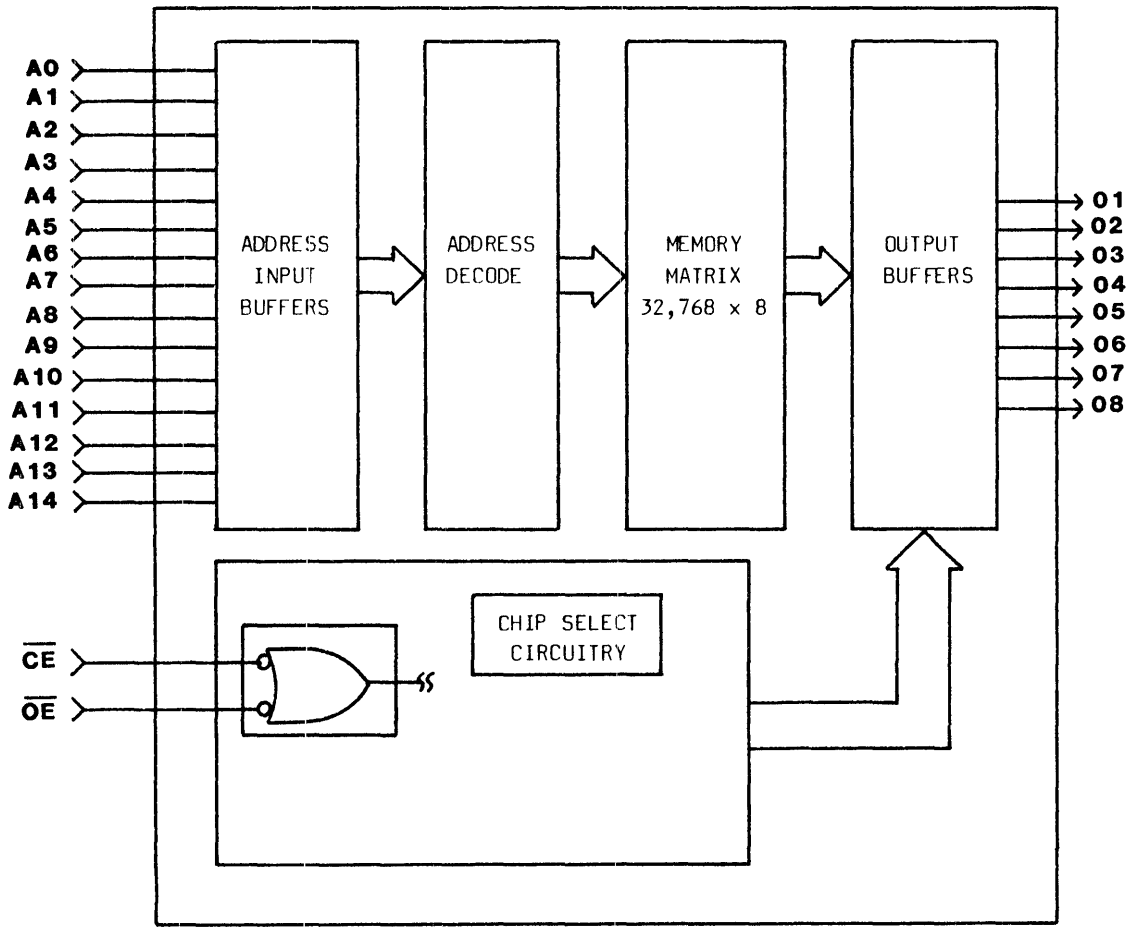
III) "ORED" chip select requirement (chip selects at pins 20 ($\overline{CE}$) and 22 ($\overline{OE}$) function as a logical "OR").

*This is ideally suited for applications that have limited chip select decoding capabilities.

Logic Function: ($\overline{CE}$ + $\overline{OE}$) = Chip Selected

"+" = LOGICAL "OR"

BLOCK DIAGRAM



DS10018A-4

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ±10%

Operating Temperature T_A = 0°C to + 70°C

Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS2, $\overline{OE}$/CS1 Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-10	-	+10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	-10	-	+10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	-	-	-	40	mA	Note 1
I_{CC} (Standby)	-	-	-	1	mA	Note 2

AC CHARACTERISTICS

		ROC256B		ROC256CS		ROC256C		ROC256DS		ROC256D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Address Hold After Address Change	t_{OH}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Chip Enable Time	t_{ACE}	-	450	-	350	-	300	-	250	-	200	ns	
Chip Select, Output Enable Access Time	t_{ACS}	-	150	-	125	-	100	-	85	-	70	ns	Note 4
Output Disable Time	t_{OFF}	-	150	-	125	-	100	-	85	-	70	ns	
Output Low Z Delay	t_{LZ}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Output High Z Delay	t_{HZ}	-	150	-	125	-	100	-	85	-	70	ns	Note 5
Capacitance***													
Input Capacitance	C_I	-	7	-	7	-	7	-	7	-	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	-	10	-	10	-	10	-	10	-	10	pf	F = 1MHz, T_A = +25°C

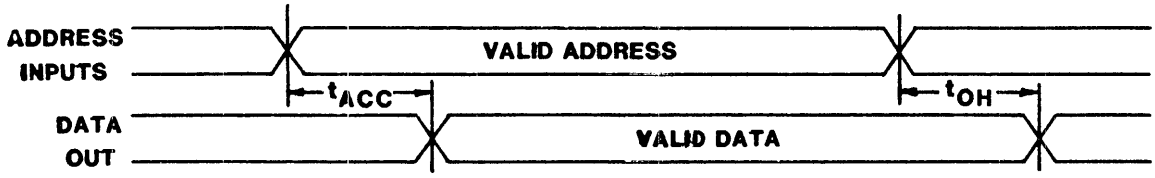
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

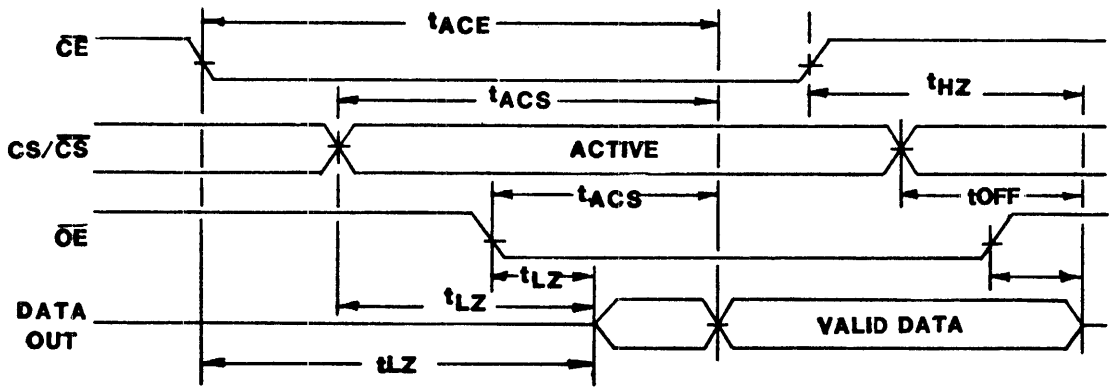
1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq$ 2.0V ("Power Down" programmed parts only).
3. These parameters are periodically sampled and not 100% tested.
4. Access time to valid data measured from CS1 going active and/or $\overline{OE}$ going low whichever occurs last/first.
5. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ and/or $\overline{OE}$ going high or CS1 going active, which ever occurs first/last.

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	≤10nsec
Timing Measurement Levels: Input/Output	0.8V AND 2.0V
Output Load	See Figure 1

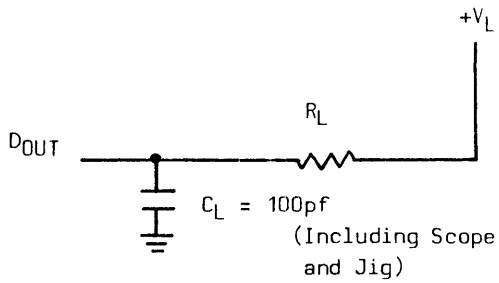


Fig. 1

GENERAL INSTRUMENT	RO9512XDS/D/ES VariPage™

PRELIMINARY INFORMATION

524,288 STATIC READ ONLY MEMORY

FEATURES:

- Mask programmable storage providing 64K x 8 bit words with programmable "VariPage"™ memory array organization
  - Single 64K Byte Pages: RO95120
  - Two 32K Byte Pages: RO95121
  - Four 16K Byte Pages: RO95122
- One programmable chip select (CS); RO9512X, or: power down feature (CE); RO9512XA
- 250ns max access time: RO9512XDS, RO9512XADS
- 200ns max access time: RO9512XD, RO9512XAD
- 150ns max access time: RO9512XES, RO9512XAES
- Fully static operation
- Single +5V ±10% supply
- Inputs and outputs TTL compatible
- Three state outputs - under the control of one mask programmable chip select input
- Low power dissipation
- 28 pin JEDEC approved pinout
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD 883B

DESCRIPTION

The General Instrument RO9512X is a 524,288 bit static read only memory capable of variable page organization. Fabricated with General Instrument's N-Channel Silicon Gate Technology, the RO9512X provides the designer with a high performance, flexible NMOS memory circuit featuring operation from a single +5V power supply and low power dissipation.

Memory Organization

The RO9512X is designed to offer a mask programmable option of choosing page sizes consistent with specific addressing limitations. For example, if only fifteen address lines are available, the RO9512X could be programmed to "bank select" on 256K page boundaries (i.e. two 32K x 8 pages), see block diagram.

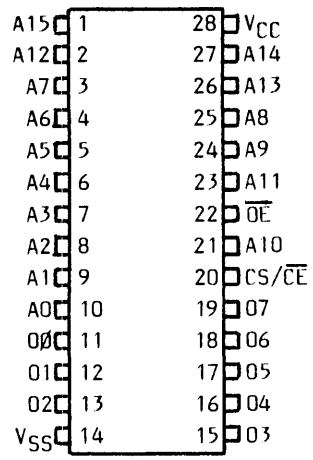
The RO9512X in its straight (non-paging) format, will utilize all sixteen address inputs for direct addressing. When programmed to bank select on either 16K or 32K byte page boundaries, page selection is accomplished via the write enable ($\overline{WE}$) and the three I/O pins.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

RO95120

64 x 8 organization

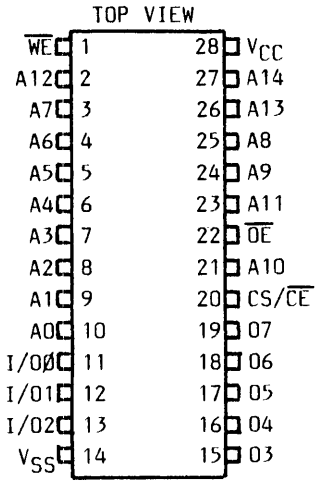
TOP VIEW



RO95121

(2) 32K x 8 organization

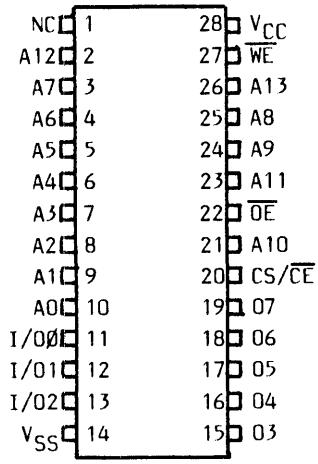
TOP VIEW



RO95122

(4) 16K x 8 organization

TOP VIEW



DS10019A-1

Operation

Address (A0-A13, A14-A15 optional)

The address valid interval determines the device cycle time. The positive logic address is decoded to select 16K, 32K, or 64K by 8-bit pages. A0 is the least significant bit and A15 is the most significant bit of the word address.

Chip Select (CS)

This is a programmable chip select which will be sacrificed if the power down option is selected. The address bus will tri-state when CS is in the inactive state.

Chip Enable ($\overline{CE}$)

The power down feature of the RO9512XA is controlled by the chip enable ($\overline{CE}$) input. If the power down feature is programmed, the device will go into a low current mode when $\overline{CE}$ is equal to or greater than 2.0 volts. The RO9512XA will remain in a low power standby mode as long as CE remains high.

Output Enable ($\overline{OE}$)

The $\overline{OE}$ functions as a chip select for the RO95121 and RO95122. The address bus will tri-state when $\overline{OE}$ is high.

Write Enable ($\overline{WE}$)

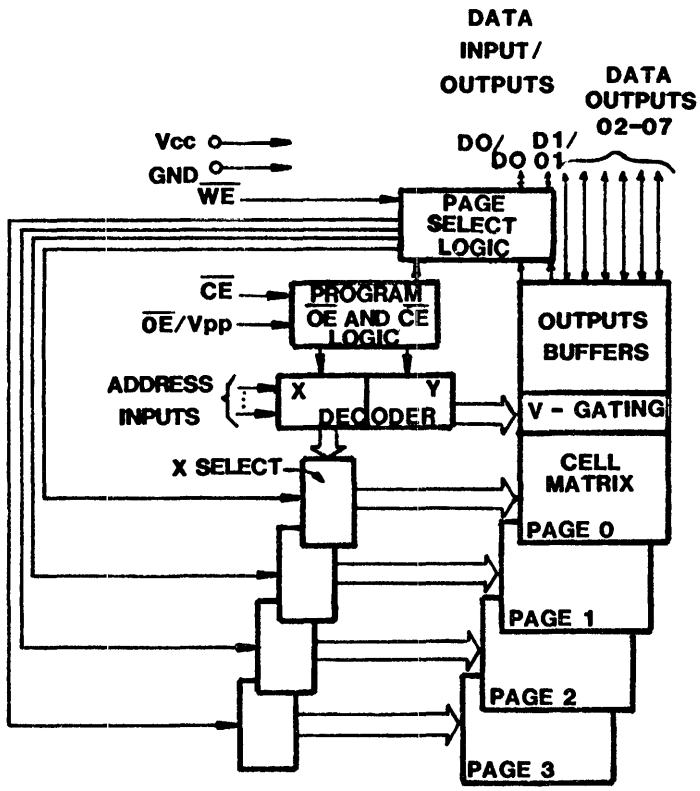
The $\overline{WE}$ pin allows the RO95121 or RO95122's RAM to accept a page transition address. The page address is entered via the three I/O pins and latched into the RAM on the rising edge of the $\overline{WE}$ signal. The three-bit page address is decoded as follows:

PAGE DEFINITIONS

	16K x 8 Pages			32K x 8 Pages		
Page	I/O^2	I/O^1	I/O^0	I/O^2	I/O^1	I/O^0
P_0	0	0	0	0	0	X
P_1	0	0	1	0	1	X
P_2	0	1	0	1	0	X
P_3	0	1	1	1	1	X
P_4	1	0	0	X	X	X
P_5	1	0	1	X	X	X
P_6	1	1	0	X	X	X
P_7	1	1	1	X	X	X

Note:
During power-up, the device will reset to page 0. Upon page selection, only the selected page will be powered, the non-selected pages will automatically power down.

BLOCK DIAGRAM: RO95121



DS10019A-2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages
(with Respect to GND)..... -0.5V to +7.0V
Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):
V_{CC} = 5V ± 10%
Operating Temperature T_A = 0°C to + 70°C
Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS, $\overline{OE}$ Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 2.1mA
Leakage	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active, Non-Paged)	I_{CC}	-	-	125	mA	Note 1
I_{CC} (Active, Paged)	I_{CC}	-	-	100	mA	Note 2
I_{CC} (Standby)	I_{CC}	-	-	30	mA	Note 3

READ OPERATION
AC CHARACTERISTICS

		RO951XDS		RO951XD		RO951XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address to Output Delay	t_{ACC}	-	250	-	200	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	-	250	-	200	-	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	-	85	-	70	-	55	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ High to Output Data Float	t_{DF}	0	85	0	70	0	55	ns	$\overline{CE}$ = V_{IL}, Note 4
Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occured First	t_{OH}	0	-	0	-	-	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

PAGE SELECT WRITE OPERATION
AC CHARACTERISTICS

		ALL SPEEDS			
Characteristics	Sym	Min	Max	Units	Conditions
CE to End of Write	t_{CW}	120	-	ns	$\overline{OE}$ = V_{IH}, Note 5
Write Pulse Width	t_{WP}	70	-	ns	$\overline{OE}$ = V_{IH}, Note 5
Write Recovery Time	t_{WR}	20	-	ns	
Data Setup Time	t_{DS}	40	-	ns	$\overline{OE}$ = V_{IH}
Data Hold Time	t_{DH}	20	-	ns	$\overline{OE}$ = V_{IH}
$\overline{CE}$ to Write Setup Time	t_{CS}	0	-	ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ Low From $\overline{OE}$ High Delay Time	t_{WH}	50	-	ns	Note 6

CAPACITANCE*** (T_A = 25°C, f = 1MHz)

		RO951XDS		RO951XD		RO951XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Input Capacitance	C_{IN}	-	7	-	7	-	7	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	10	-	10	-	10	pf	V_{OUT} = 0V

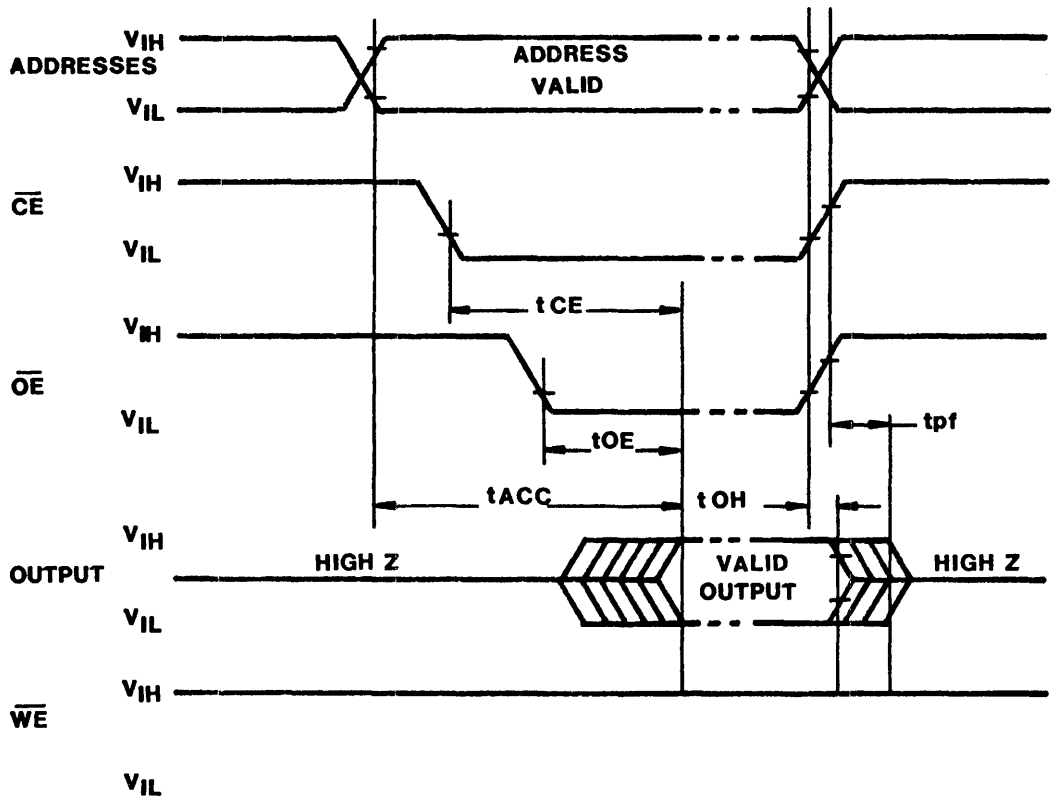
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

1. Measured with device selected and outputs unloaded.
2. Measured with device selected, non-active pages powered down, and outputs unloaded.
3. Device disabled with $\overline{CE} \geq$ 2.0V ("Powered Down" programmed parts only).
4. TDF = Output float time from $\overline{OE}$ or $\overline{CE}$ going high, whichever occurs last.
5. Write may be terminated either by $\overline{CE}$ or $\overline{WE}$.
6. $\overline{OE}$ must be high during write cycle.

TIMING DIAGRAMS

Read Operation



DS10019A-5

TIMING DIAGRAMS (cont'd)

Page Select Write Operation

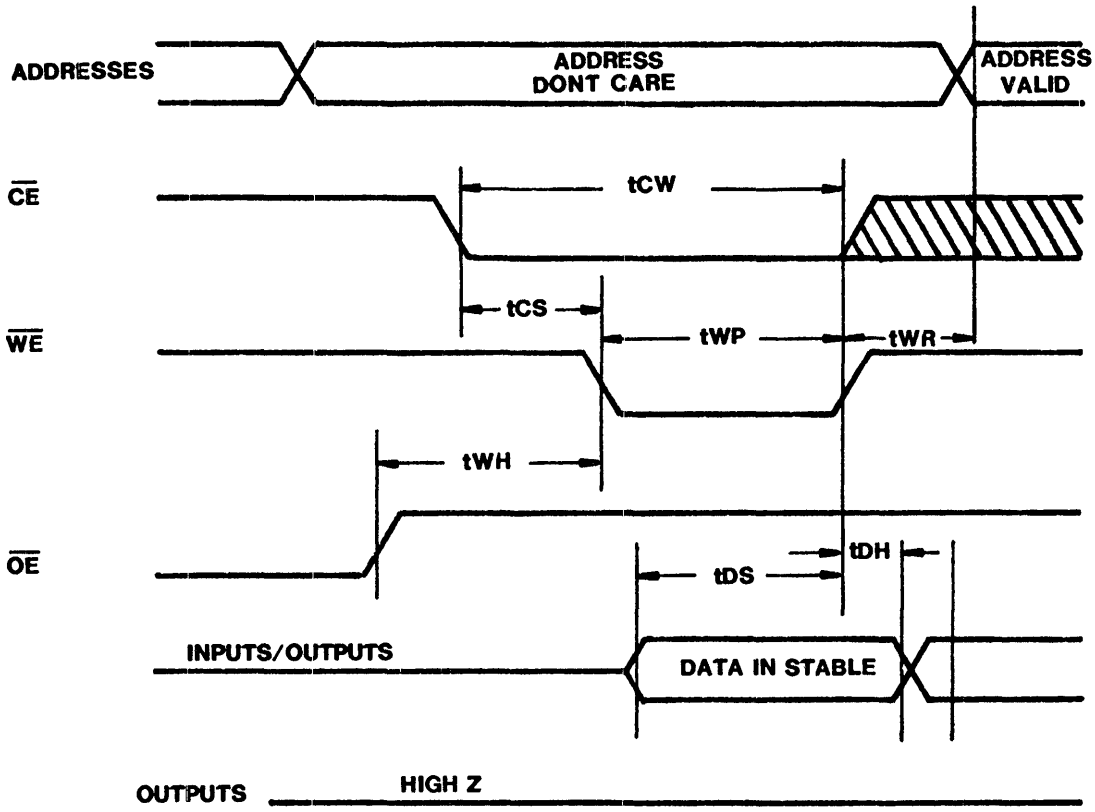
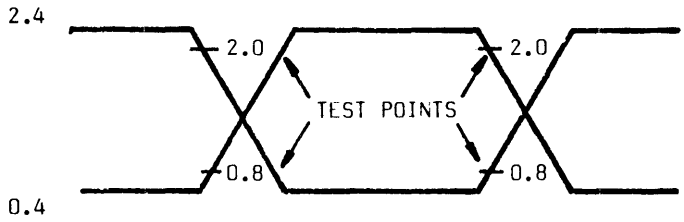


Figure 2
A.C. Testing Input/Output Waveform

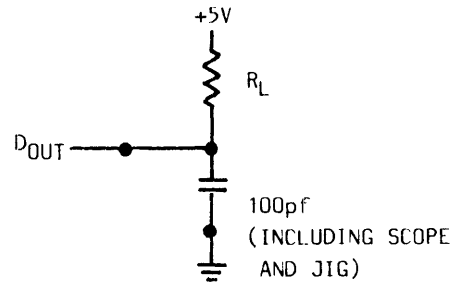


AC Testing inputs are driven at 2.4V for a logic 1 and 0.4V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

A.C. TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Falls Times	≤ 5nsec
Timing Measurement Levels: Input/Output	0.8V and 2.0V
Output Load	See Figure 1

Figure 1
A.C. Testing Load Circuit



524,288 STATIC READ ONLY MEMORY

FEATURES:

- Mask programmable storage providing 64K x 8 bit words with programmable "VariPage"™ memory array organization
  - Single 64K Byte Pages: ROC5120
  - Two 32K Byte Pages: ROC5121
  - Four 16K Byte Pages: ROC5122
- One programmable chip select (CS); ROC512X, or: power down feature (CE); ROC512XA
- 250ns max access time: ROC512XDS, ROC512XADS
- 200ns max access time: ROC512XD, ROC512XAD
- 150ns max access time: ROC512XES, ROC512XAES
- Fully static operation
- Single +5V ±10% supply
- Inputs and outputs TTL compatible
- Three state outputs - under the control of one mask programmable chip select input
- Low power dissipation
- 28 pin JEDEC approved pinout
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD 883B

DESCRIPTION

The General Instrument ROC512X is a 524,288 bit static read only memory capable of variable page organization. Fabricated with General Instrument's N-Channel Silicon Gate Technology, the ROC512X provides the designer with a high performance, flexible NMOS memory circuit featuring operation from a single +5V power supply and low power dissipation.

Memory Organization

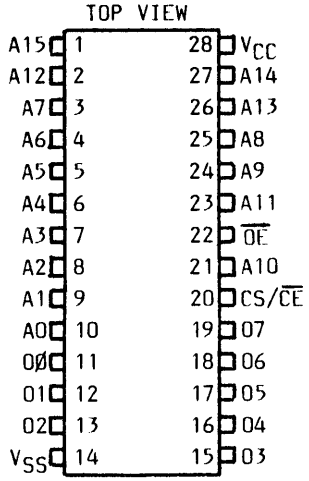
The ROC512X is designed to offer a mask programmable option of choosing page sizes consistent wit specific addressing limitations. For example, if only fifteen address lines are available, the ROC512X could be programmed to "bank select" on 256K page boundaries (i.e. two 32K x 8 pages), see block diagram.

The ROC512X in its straight (non-paging) format, will utilize all sixteen address inputs for direct addressing. When programmed to bank select on either 16K or 32K byte page boundaries, page selection is accomplished via the write enable ($\overline{WE}$) and the three I/O pins.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

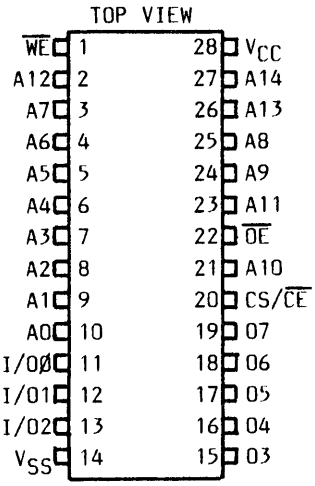
ROC5120

64K x 8 organization



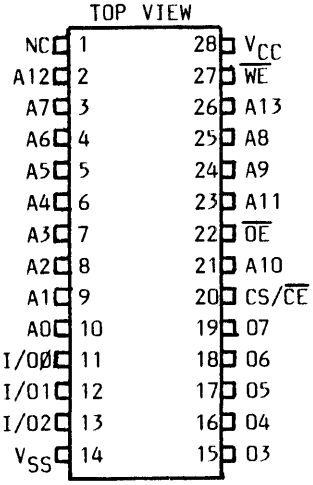
ROC5121

(2) 32K x 8 organization



ROC5122

(4) 16K x 8 organization



Operation

Address (A0-A13, A14-A15 optional)

The address valid interval determines the device cycle time. The positive logic address is decoded to select 16K, 32K, or 64K by 8-bit pages. A0 is the least significant bit and A15 is the most significant bit of the word address.

Chip Select (CS)

This is a programmable chip select which will be sacrificed if the power down option is selected. The address bus will tri-state when CS is in the inactive state.

Chip Enable ($\overline{CE}$)

The power down feature of the ROC512XA is controlled by the chip enable ($\overline{CE}$) input. If the power down feature is programmed, the device will go into a low current mode when $\overline{CE}$ is equal to or greater than 2.0 volts. The ROC512XA will remain in a low power standby mode as long as $\overline{CE}$ remains high.

Output Enable ($\overline{OE}$)

The $\overline{OE}$ functions as a chip select for the ROC5121 and ROC5122. The address bus will tri-state when $\overline{OE}$ is high.

Write Enable ($\overline{WE}$)

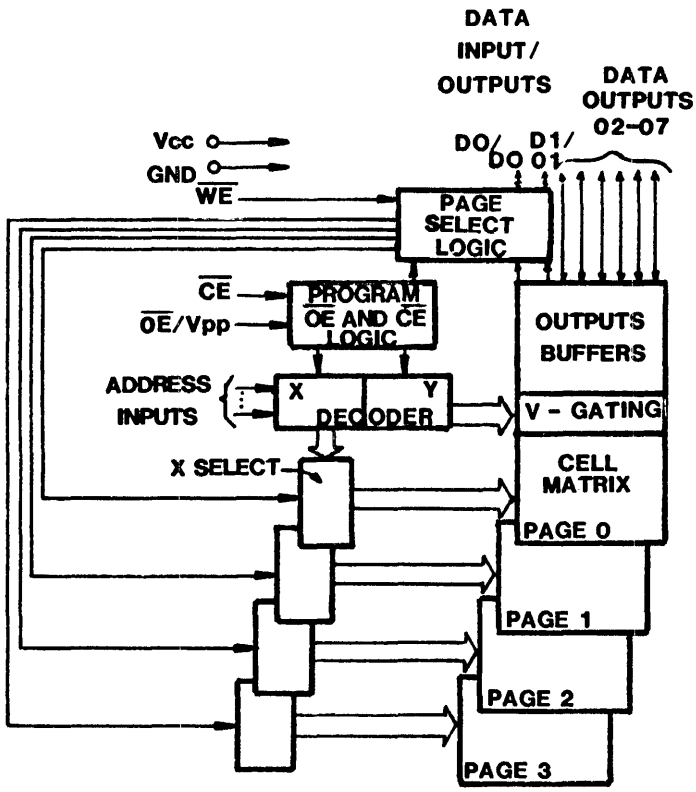
The $\overline{WE}$ pin allows the ROC5121 or ROC5122's RAM to accept a page transition address. The page address is entered via the three I/O pins and latched into the RAM on the rising edge of the $\overline{WE}$ signal. The three-bit page address is decoded as follows:

PAGE DEFINITIONS

	16K x 8 Pages			32K x 8 Pages		
Page	I/O^2	I/O^1	I/O^0	I/O^2	I/O^1	I/O^0
P_0	0	0	0	0	0	X
P_1	0	0	1	0	1	X
P_2	0	1	0	1	0	X
P_3	0	1	1	1	1	X
P_4	1	0	0	X	X	X
P_5	1	0	1	X	X	X
P_6	1	1	0	X	X	X
P_7	1	1	1	X	X	X

Note:
During power-up, the device will reset to page 0.

BLOCK DIAGRAM: ROC5121



DS10021A-2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages
(with Respect to GND)..... -0.5V to +7.0V
Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):
V_{CC} = 5V ± 10%
Operating Temperature T_A = 0°C to + 70°C
Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS, $\overline{OE}$ Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 2.1mA
Leakage	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	I_{CC}	-	-	35	mA	Note 1
I_{CC} (Standby)	I_{CC}	-	-	40	µA	Note 2

READ OPERATION
AC CHARACTERISTICS

		ROC51XDS		ROC51XD		ROC51XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address to Output Delay	t_{ACC}	-	250	-	200	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	-	250	-	200	-	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	-	85	-	70	-	55	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ High to Output Data Float	t_{DF}	0	85	0	70	0	55	ns	$\overline{CE}$ = V_{IL}, Note 3
Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occured First	t_{OH}	0	-	0	-	-	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

PAGE SELECT WRITE OPERATION
AC CHARACTERISTICS

		ALL SPEEDS			
Characteristics	Sym	Min	Max	Units	Conditions
$\overline{CE}$ to End of Write	t_{CW}	120	-	ns	$\overline{OE}$ = V_{IH}, Note 4
Write Pulse Width	t_{WP}	70	-	ns	$\overline{OE}$ = V_{IH}, Note 4
Write Recovery Time	t_{WR}	20	-	ns	
Data Setup Time	t_{DS}	40	-	ns	$\overline{OE}$ = V_{IH}
Data Hold Time	t_{DH}	20	-	ns	$\overline{OE}$ = V_{IH}
$\overline{CE}$ to Write Setup Time	t_{CS}	0	-	ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ Low From $\overline{OE}$ High Delay Time	t_{WH}	50	-	ns	Note 5

CAPACITANCE*** (T_A = 25°C, f = 1MHz)

		ROC51XDS		ROC51XD		ROC51XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Input Capacitance	C_{IN}	-	7	-	7	-	7	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	10	-	10	-	10	pf	V_{OUT} = 0V

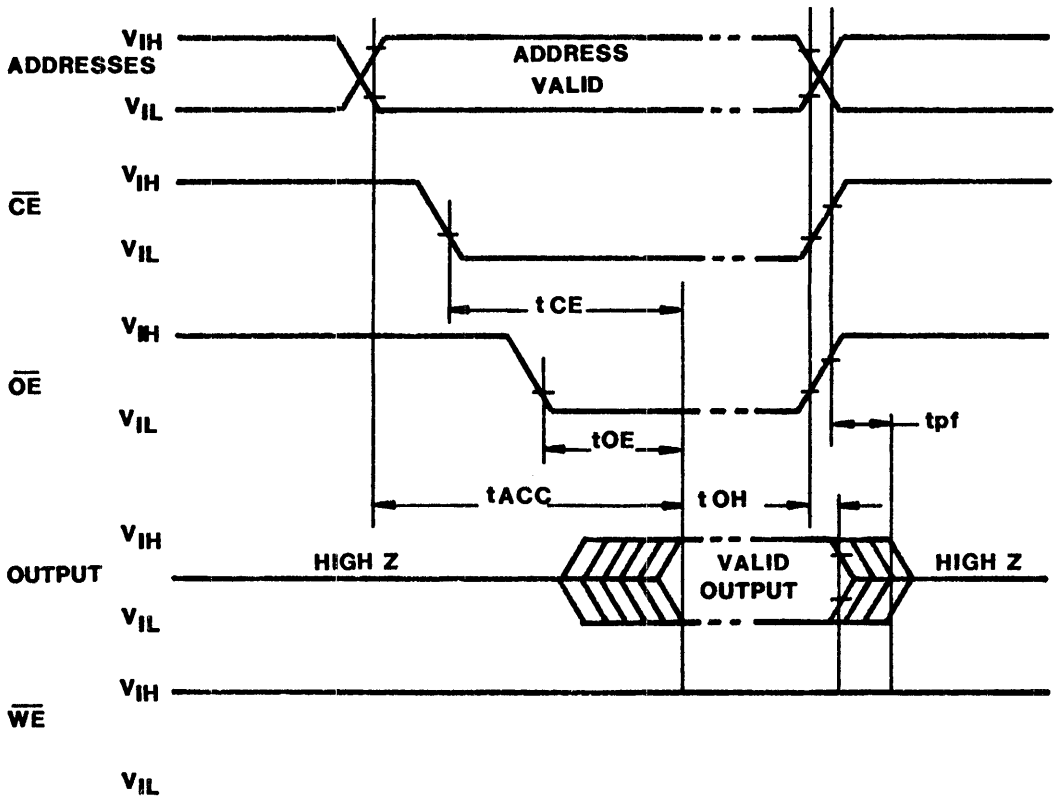
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq$ 2.0V ("Powered Down" programmed parts only).
3. TDF = Output float time from $\overline{OE}$ or $\overline{CE}$ going high, whichever occurs last.
4. Write may be terminated either by $\overline{CE}$ or $\overline{WE}$.
5. $\overline{OE}$ must be high during write cycle.

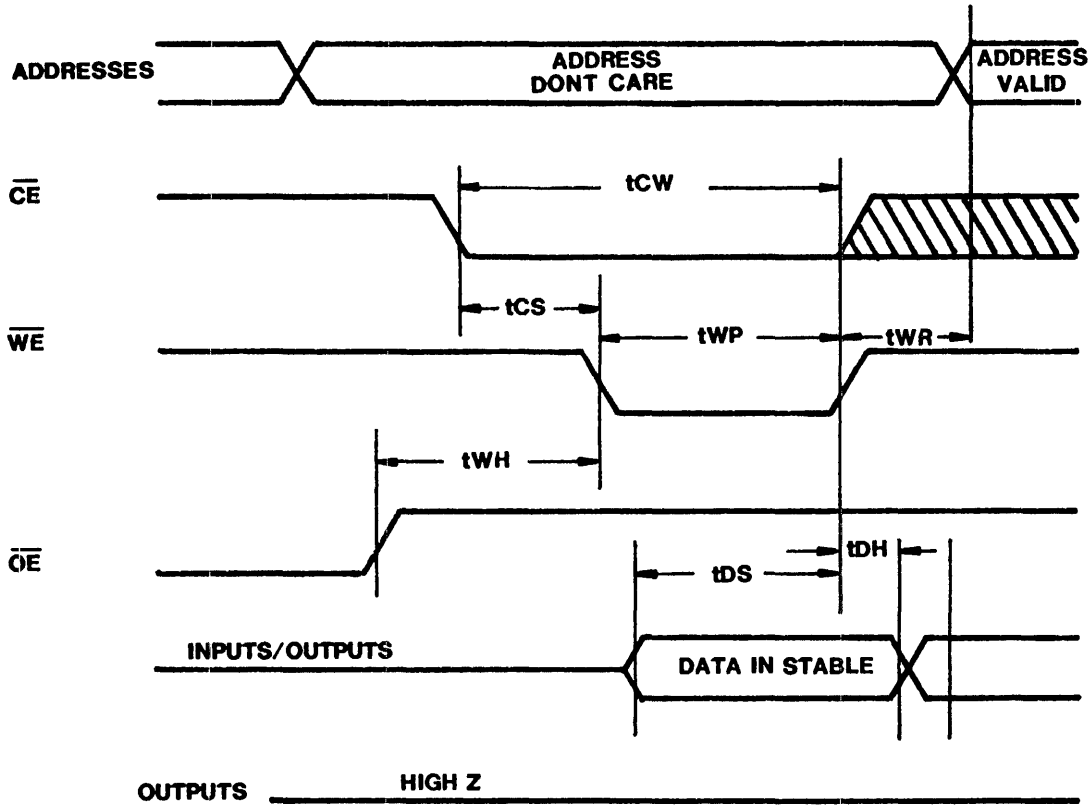
TIMING DIAGRAMS

Read Operation



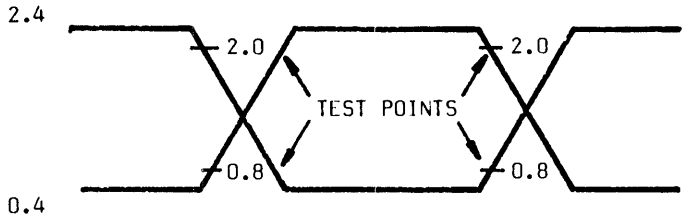
TIMING DIAGRAMS (cont'd)

Page Select Write Operation



DS10021A-6

Figure 2
A.C. Testing Input/Output Waveform

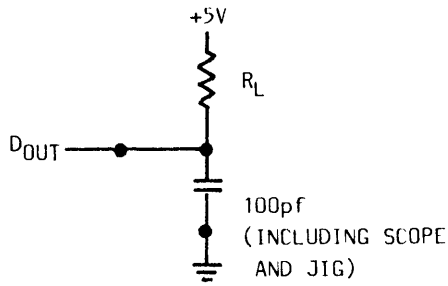


AC Testing inputs are driven at 2.4V for a logic 1 and 0.4V for a logic 0. Timing measurements are madet at 2.0V for a logic 1 and 0.8V for a logic 0.

A.C. TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Falls Times	≤ 5nsec
Timing Measurement Levels: Input/Output	0.8V and 2.0V
Output Load	See Figure 1

Figure 1
A.C. Testing Load Circuit



GENERAL INSTRUMENT	R09100XC/DS/D VariPage™

PRELIMINARY INFORMATION

ONE MEGABIT STATIC READ ONLY MEMORY

FEATURES:

- Mask programmable storage providing 128K x 8 bit words with programmable "VariPage"™ memory array organization
  - Single 128K Byte Pages: R091000
  - Four 32K Byte Pages: R091001
  - Eight 16K Byte Pages: R091002
- One programmable chip select (CS); R09100X, or: power down feature (CE); R09100XA
- 300ns max access time: R09100XC, R09100XAC
- 250ns* max access time: R09100XDS, R09100XADS
- 200ns* max access time: R09100XD, R09100XAD
- Fully static operation
- Single +5V ±10% supply
- Inputs and outputs TTL compatible
- Three state outputs - under the control of one mask programmable chip select input
- Low power dissipation
- 28 pin JEDEC approved pinout
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD 883B

DESCRIPTION

The General Instrument R09100X is a 1,048,576 bit static read only memory capable of variable page organization. Fabricated with General Instrument's N-Channel Silicon Gate Technology, the R09100X provides the designer with a high performance, flexible NMOS memory circuit featuring operation from a single +5V power supply and low power dissipation.

Memory Organization

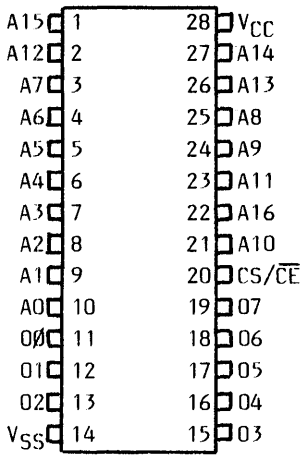
The R09100X is designed to offer a mask programmable option of choosing page sizes consistant with specific addressing limitations. For example, if only fifteen address lines are available, the R09100X could be programmed to "bank select" on 256K page boundaries (i.e. four 32K x 8 pages), see block diagram.

The R09100X in its straight (non-paging) format, will utilize all seventeen address inputs for direct addressing. When programmed to bank select on either 16K or 32K byte page boundaries, page selection is accomplished via the write enable ($\overline{WE}$) and the three I/O pins.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

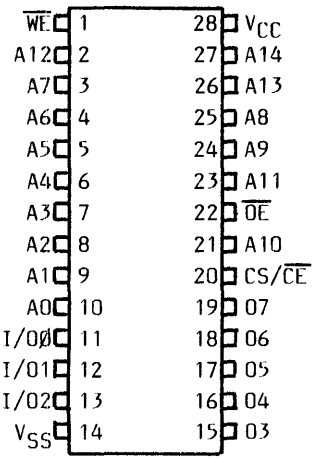
R091000 — TOP VIEW

128K x 8 organization



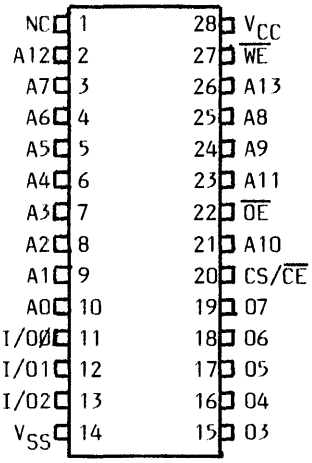
R091001 — TOP VIEW

(4) 32K x 8 organization



R091002 — TOP VIEW

(8) 16K x 8 organization



Operation

Address (A0-A13, A14-A16 optional)

The address valid interval determines the device cycle time. The positive logic address is decoded to select 16K, 32K, or 128K by 8-bit pages. A0 is the least significant bit and A16 is the most significant bit of the word address.

Chip Select (CS)

This is a programmable chip select which will be sacrificed if the power down option is selected. The address bus will tri-state when CS is in the inactive state.

Chip Enable ($\overline{CE}$)

The power down feature of the RO9100XA is controlled by the chip enable ($\overline{CE}$) input. If the power down feature is programmed, the device will go into a low current mode when $\overline{CE}$ is equal to or greater than 2.0 volts. The RO9100XA will remain in a low power standby mode as long as CE remains high.

Output Enable ($\overline{OE}$)

The $\overline{OE}$ functions as a chip select for the RO91001 and RO91002. The address bus will tri-state when $\overline{OE}$ is high.

Write Enable ($\overline{WE}$)

The $\overline{WE}$ pin allows the RO91001 or RO9102's RAM to accept a page transition address. The page address is entered via the three I/O pins and latched into the RAM on the rising edge of the $\overline{WE}$ signal. The three-bit page address is decoded as follows:

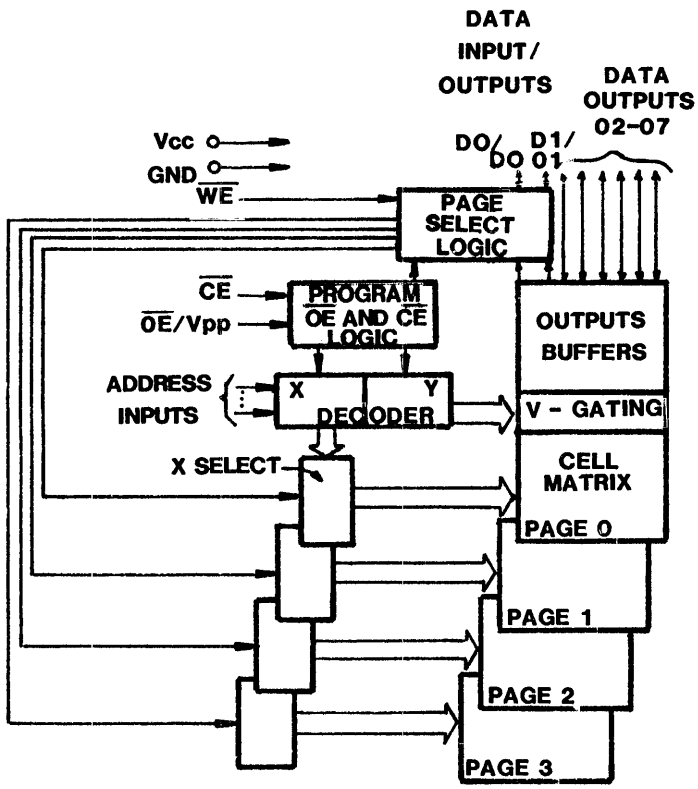
PAGE DEFINITIONS

	16K x 8 Pages			32K x 8 Pages		
Page	I/O^2	I/O^1	I/O^0	I/O^2	I/O^1	I/O^0
P_0	0	0	0	0	0	X
P_1	0	0	1	0	1	X
P_2	0	1	0	1	0	X
P_3	0	1	1	1	1	X
P_4	1	0	0	X	X	X
P_5	1	0	1	X	X	X
P_6	1	1	0	X	X	X
P_7	1	1	1	X	X	X

Note:

During power-up, the device will reset to page 0. Upon page selection, only the selected page will be powered, the non-selected pages will automatically power down.

BLOCK DIAGRAM: RO91001



DS10013C-2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ± 10%

Operating Temperature T_A = 0°C to + 70°C

Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS, $\overline{OE}$ Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 2.1mA
Leakage	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active, Non-Paged)	I_{CC}	-	-	150	mA	Note 1
I_{CC} (Active, Paged)	I_{CC}	-	-	125	mA	Note 2
I_{CC} (Standby)	I_{CC}	-	-	40	mA	Note 3

READ OPERATION
AC CHARACTERISTICS

		R09100XC		R09100XDS		R09100XD			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address to Output Delay	t_{ACC}	-	300	-	250	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	-	300	-	250	-	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	-	120	-	100	-	85	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ High to Output Data Float	t_{DF}	0	100	0	85	0	70	ns	$\overline{CE}$ = V_{IL}, Note 4
Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occured First	t_{OH}	0	-	0	-	-	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

PAGE SELECT WRITE OPERATION
AC CHARACTERISTICS

		R09100XC		R09100XDS		R09100XD			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
$\overline{CE}$ to End of Write	t_{CW}	180	-	180	-	180	-	ns	$\overline{OE}$ = V_{IH}, Note 5
Write Pulse Width	t_{WP}	100	-	100	-	100	-	ns	$\overline{OE}$ = V_{IH}, Note 5
Write Recovery Time	t_{WR}	20	-	20	-	20	-	ns	
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns	$\overline{OE}$ = V_{IH}
Data Hold Time	t_{DH}	20	-	20	-	20	-	ns	$\overline{OE}$ = V_{IH}
$\overline{CE}$ to Write Setup Time	t_{CS}	0	-	0	-	0	-	ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ Low From $\overline{OE}$ High Delay Time	t_{WH}	55	-	55	-	55	-	ns	Note 6

CAPACITANCE*** (T_A = 25°C, f = 1MHz)

		R09100XC		R09100XDS		R09100XD			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Input Capacitance	C_{IN}	-	7	-	7	-	7	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	10	-	10	-	10	pf	V_{OUT} = 0V

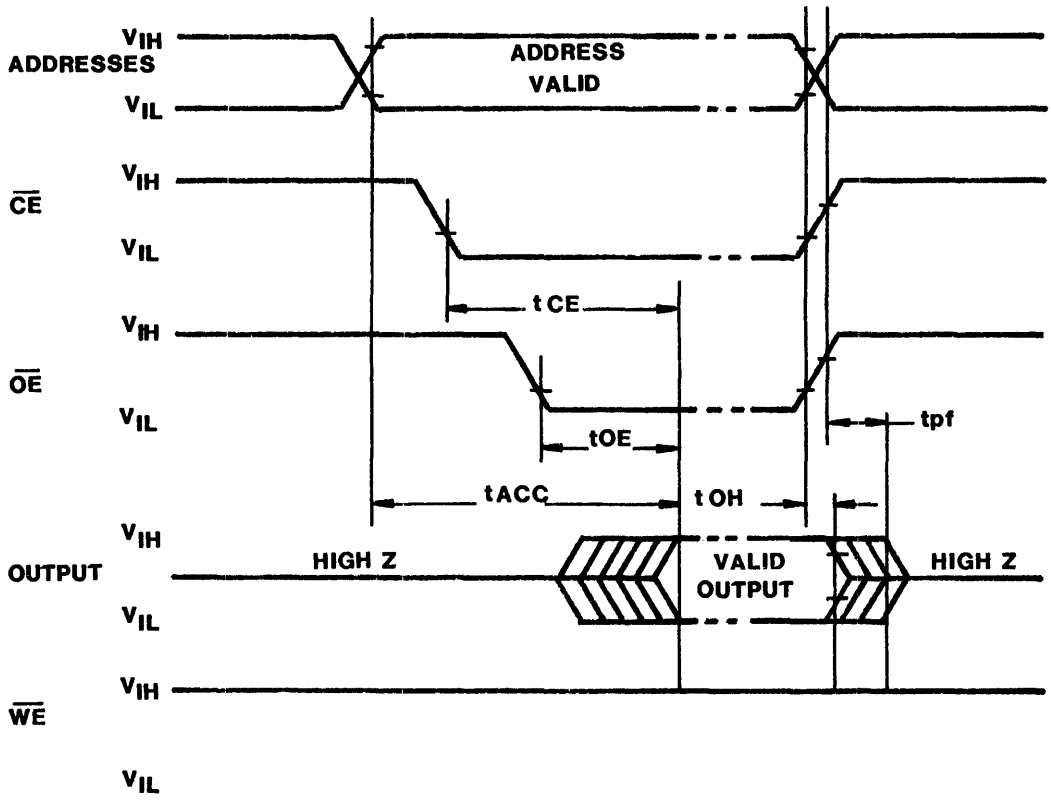
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

1. Measured with device selected and outputs unloaded.
2. Measured with device selected, non-active pages powered down, and outputs unloaded.
3. Device disabled with $\overline{CE} \geq 2.0V$ ("Powered Down" programmed parts only).
4. TDF = Output float time from $\overline{OE}$ or $\overline{CE}$ going high, whichever occurs last.
5. Write may be terminated either by $\overline{CE}$ or $\overline{WE}$.
6. $\overline{OE}$ must be high during write cycle.

TIMING DIAGRAMS

Read Operation



DS10013C-5

TIMING DIAGRAMS (cont'd)

Page Select Write Operation

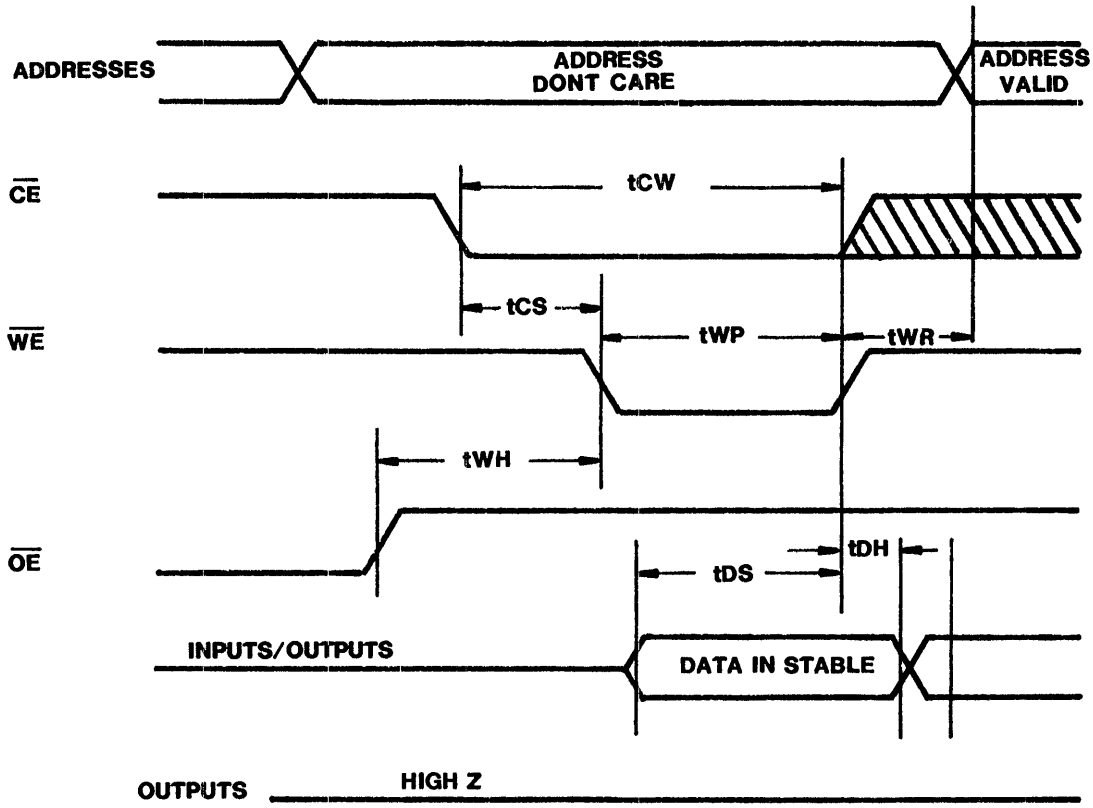
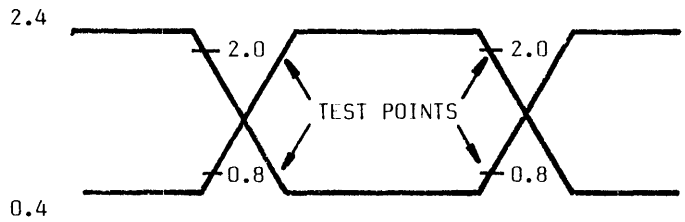


Figure 2
A.C. Testing Input/Output Waveform

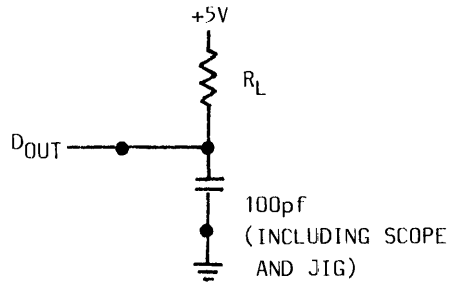


AC Testing inputs are driven at 2.4V for a logic 1 and 0.4V for a logic 0 timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

A.C. TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Falls Times	≤ 5nsec
Timing Measurement Levels: Input/Output	0.8V and 2.0V
Output Load	See Figure 1

Figure 1
A.C. Testing Load Circuit



ONE MEGABIT STATIC READ ONLY MEMORY

FEATURES:

- Mask programmable storage providing 128K x 8 bit words with programmable "VariPage"™ memory array organization
  - Single 128K Byte Pages: ROC1000
  - Four 32K Byte Pages: ROC1001
  - Eight 16K Byte Pages: ROC1002
- One programmable chip select (CS); ROC100X, or: power down feature (CE); ROC100XA
- 250ns max access time: ROC100XDS, ROC100XADS
- 200ns max access time: ROC100XD, ROC100XAD
- 150ns max access time: ROC100XES, ROC100XAES
- Fully static operation
- Single +5V ±10% supply
- Inputs and outputs TTL compatible
- Three state outputs - under the control of one mask programmable chip select input
- Low power dissipation
- 28 pin JEDEC approved pinout
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD 883B

DESCRIPTION

The General Instrument ROC100X is a 1,048,576 bit static read only memory capable of variable page organization. Fabricated with General Instrument's CMOS Silicon Gate Technology, the ROC100X provides the designer with a high performance, flexible CMOS memory circuit featuring operation from a single +5V power supply and low power dissipation.

Memory Organization

The ROC100X is designed to offer a mask programmable option of choosing page sizes consistent with specific addressing limitations. For example, if only fifteen address lines are available, the ROC100X could be programmed to "bank select" on 256K page boundaries (i.e. four 32K x 8 pages), see block diagram.

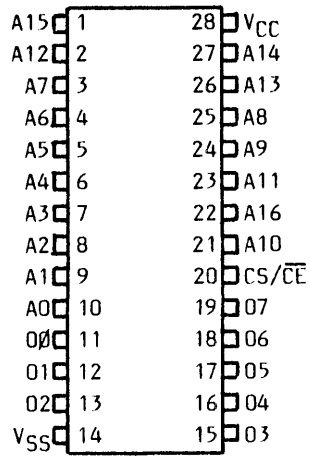
The ROC100X in its straight (non-paging) format, will utilize all seventeen address inputs for direct addressing. When programmed to bank select on either 16K or 32K byte page boundaries, page selection is accomplished via the write enable ($\overline{WE}$) and the three I/O pins.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

ROC1000

128K x 8 organization

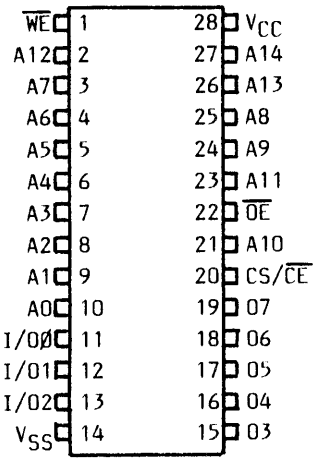
TOP VIEW



ROC1001

(4) 32K x 8 organization

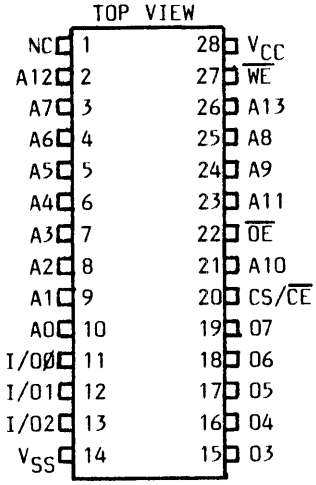
TOP VIEW



ROC1002

(8) 16K x 8 organization

TOP VIEW



Operation

Address (A0-A13, A14-A16 optional)
The address valid interval determines the device cycle time. The positive logic address is decoded to select 16K, 32K, or 128K by 8-bit pages. A0 is the least significant bit and A16 is the most significant bit of the word address.

Chip Select (CS)
This is a programmable chip select which will be sacrificed if the power down option is selected. The address bus will tri-state when CS is in the inactive state.

Chip Enable ($\overline{CE}$)
The power down feature of the ROC100XA is controlled by the chip enable ($\overline{CE}$) input. If the power down feature is programmed, the device will go into a low current mode when $\overline{CE}$ is equal to or greater than 2.0 volts. The ROC100XA will remain in a low power standby mode as long as $\overline{CE}$ remains high.

Output Enable ($\overline{OE}$)
The $\overline{OE}$ functions as a chip select for the ROC1001 and ROC1002. The address bus will tri-state when $\overline{OE}$ is high.

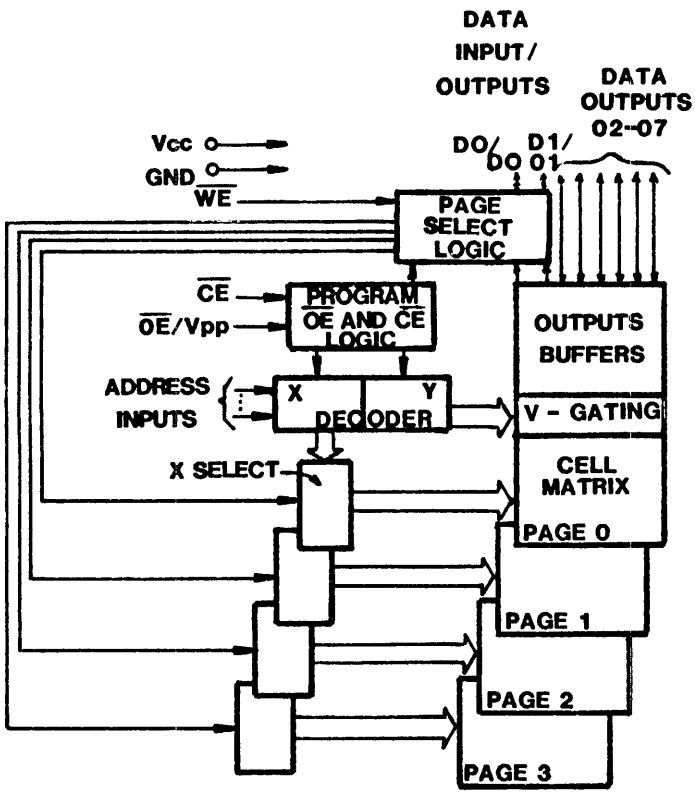
Write Enable ($\overline{WE}$)
The $\overline{WE}$ pin allows the ROC1001 or ROC102's RAM to accept a page transition address. The page address is entered via the three I/O pins and latched into the RAM on the rising edge of the $\overline{WE}$ signal. The three-bit page address is decoded as follows:

PAGE DEFINITIONS

	16K x 8 Pages			32K x 8 Pages		
Page	I/O^2	I/O^1	I/O^0	I/O^2	I/O^1	I/O^0
P_0	0	0	0	0	0	X
P_1	0	0	1	0	1	X
P_2	0	1	0	1	0	X
P_3	0	1	1	1	1	X
P_4	1	0	0	X	X	X
P_5	1	0	1	X	X	X
P_6	1	1	0	X	X	X
P_7	1	1	1	X	X	X

Note:
During power-up, the device will reset to page 0.

BLOCK DIAGRAM: ROC1001



DS10020A-2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages
(with Respect to GND)..... -0.5V to +7.0V
Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):
V_{CC} = 5V ± 10%
Operating Temperature T_A = 0°C to + 70°C
Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$/CS, $\overline{OE}$ Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-	-	10	µA	V_{IN} = 0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL} = 2.1mA
Leakage	I_{LO}	-	-	10	µA	V_{OUT} = 0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	I_{CCA}	-	-	40	mA	Note 1
I_{CC} (Standby)	I_{CCS}	-	-	50	uA	Note 2

READ OPERATION
AC CHARACTERISTICS

		ROC100XDS		ROC100XD		ROC100XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address to Output Delay	t_{ACC}	-	250	-	200	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	-	250	-	200	-	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	-	85	-	70	-	55	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ High to Output Data Float	t_{DF}	0	85	0	70	0	55	ns	$\overline{CE}$ = V_{IL}, Note 3
Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occured First	t_{OH}	0	-	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

PAGE SELECT WRITE OPERATION
AC CHARACTERISTICS

		ALL SPEEDS			
Characteristics	Sym	Min	Max	Units	Conditions
$\overline{CE}$ to End of Write	t_{CW}	120	-	ns	$\overline{OE}$ = V_{IH}, Note 4
Write Pulse Width	t_{WP}	70	-	ns	$\overline{OE}$ = V_{IH}, Note 4
Write Recovery Time	t_{WR}	20	-	ns	
Data Setup Time	t_{DS}	40	-	ns	$\overline{OE}$ = V_{IH}
Data Hold Time	t_{DH}	20	-	ns	$\overline{OE}$ = V_{IH}
$\overline{CE}$ to Write Setup Time	t_{CS}	0	-	ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ Low From $\overline{OE}$ High Delay Time	t_{WH}	50	-	ns	Note 5

CAPACITANCE*** (T_A = 25°C, f = 1MHz)

		ROC100XDS		ROC100XD		ROC100XES			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Input Capacitance	C_{IN}	-	7	-	7	-	7	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	10	-	10	-	10	pf	V_{OUT} = 0V

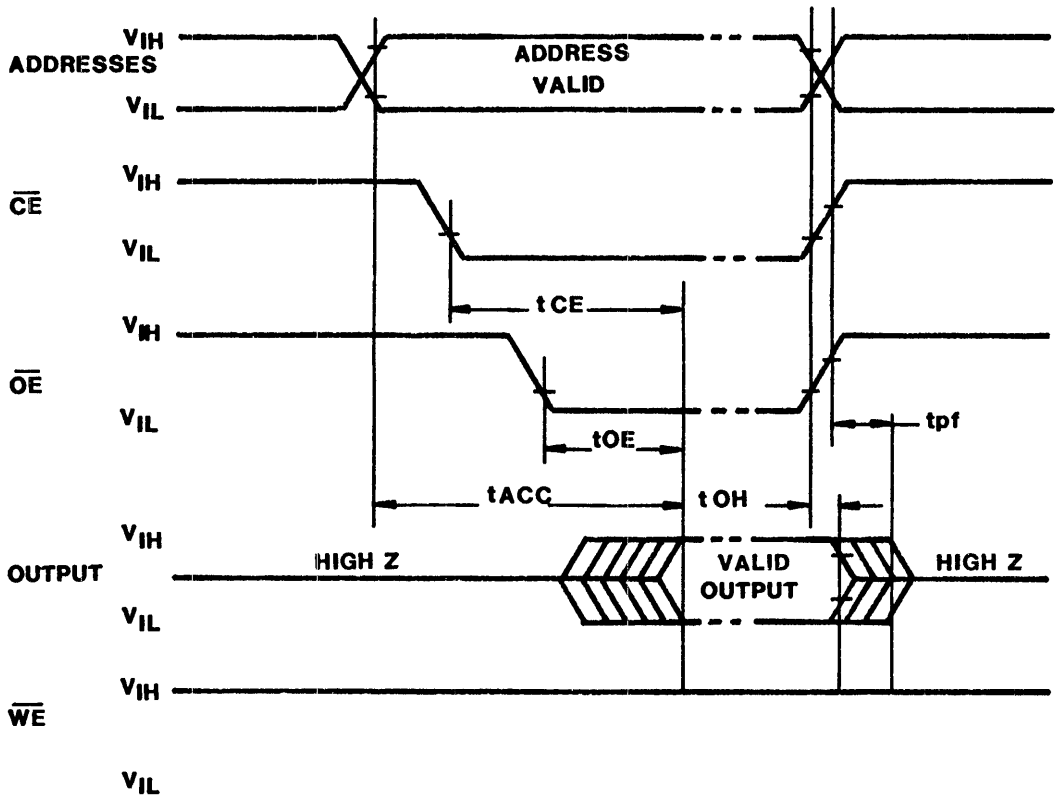
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq$ 2.0V ("Powered Down" programmed parts only).
3. TDF = Output float time from $\overline{OE}$ or $\overline{CE}$ going high, whichever occurs last.
4. Write may be terminated either by $\overline{CE}$ or $\overline{WE}$.
5. $\overline{OE}$ must be high during write cycle.

TIMING DIAGRAMS

Read Operation



DS10020A-5

TIMING DIAGRAMS (cont'd)

Page Select Write Operation

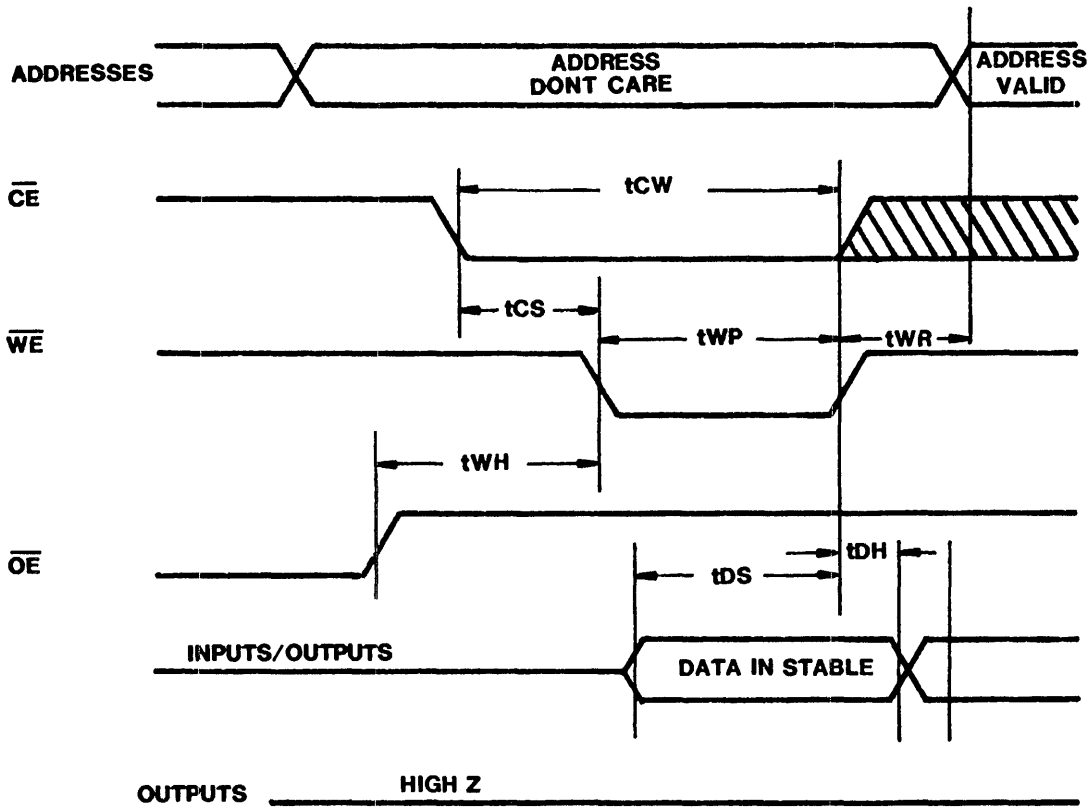
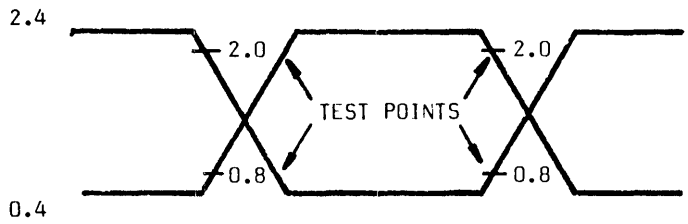


Figure 2
A.C. Testing Input/Output Waveform

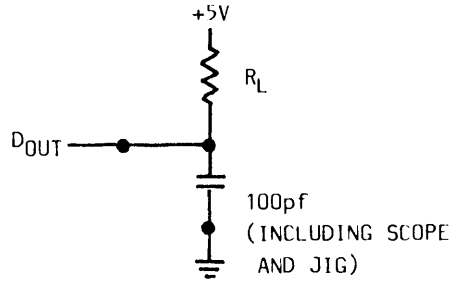


AC Testing inputs are driven at 2.4V for a logic 1 and 0.4V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

A.C. TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Falls Times	≤ 5nsec
Timing Measurement Levels: Input/Output	0.8V and 2.0V
Output Load	See Figure 1

Figure 1
A.C. Testing Load Circuit



SECTION 2

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORIES

Description	Operating Temperature	Part Number	Page Number
			Standard Parts: Serial
256 bit EEPROM - organized 16 x 16	Commercial (0°C to +70°C)	ER59256	2-3
	Industrial (-40°C to +85°C)	ER59256I	2-10
1K (1024) bit EEPROM - organized 128 x 8 or 64 x 16	Commercial (0°C to +70°C)	ER5911	2-17
	Industrial (-40°C to +85°C)	ER5911I	2-26
2K (2048) bit EEPROM - organized 256 x 8 or 128 x 16	Commercial (0°C to +70°C)	ER5912	2-35
	Industrial (-40°C to +85°C)	ER5912I	2-46
1K (1024) bit EEPROM - I^2C bus compatible organized 128 x 8	Commercial (0°C to +70°C)	PCD8572	2-57
	Industrial (-40°C to +85°C)	PCD8572I	2-66
2K (2048) bit EEPROM - I^2C bus compatible organized 256 x 8	Commercial (0°C to +70°C)	PCD8582	2-75
	Industrial (-40°C to +85°C)	PCD8582I	2-84

GENERAL INSTRUMENT

SECTION 2

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORIES (continued)

Description	Operating Temperature	Part Number	Page Number
		Standard Parts: Parallel	
1K (1024) bit EEPROM - organized 128 x 8	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)	ER5901 ER5901I	2-93 2-101
2K (2048) bit EEPROM - organized 256 x 8	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)	ER5902 ER5902I	2-109 2-116
4K (4096) bit EEPROM - organized 512 x 8	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)	ER5904 ER5904I	2-123 2-130
		Application Specific	
Non-Volatile Counter	Commercial (0°C to +70°C)	ER1000	2-137
8-bit microcomputer with on-board EEPROM - organized as 32 x 8 bit EEPROM and 512 x 12 bit mask programmable ROM.	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)	PIC16E57	2-144

GENERAL INSTRUMENT

GENERAL INSTRUMENT	ER59256

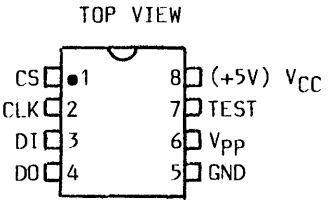
256 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES

- Low cost
- 16 x 16 serial EEPROM
- Single +5V only operation
- Binary addressing
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range
- Power on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line



DESCRIPTION

The ER59256 is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5V only operation and microcomputer compatible architecture. Six 9-bit instructions can be executed. See Table 1. The instruction format has a logical "1" as a start bit, four bits as an op code, and four bits of address. See Table 1.

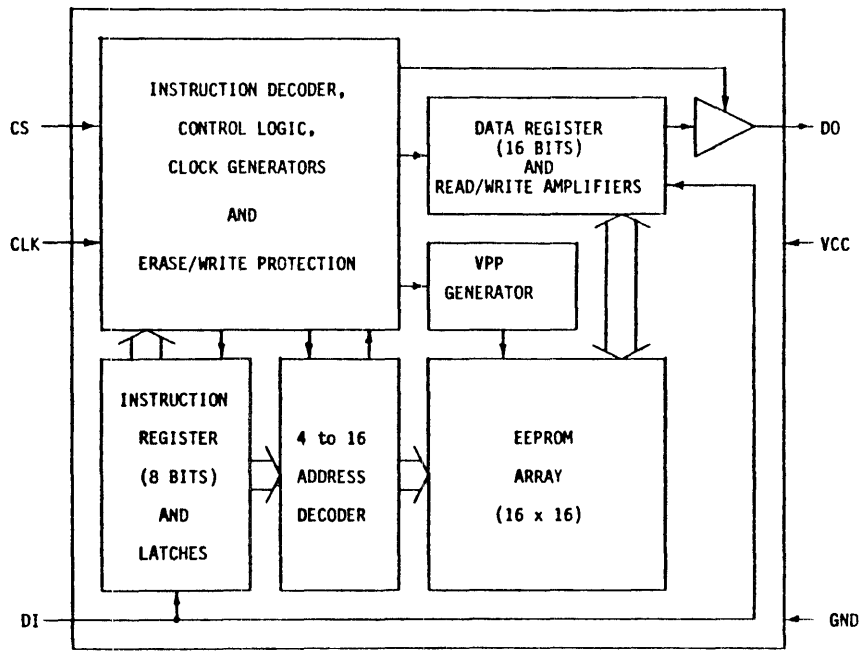
PIN FUNCTIONS

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground

TEST PINS

V_{PP}	High Voltage Test (Float)
TEST	EEPROM Margin Test (Ground/Float)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to 150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless otherwise noted)

V_{CC} = +5 ± 10% volts
GND = 0 volts
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability of fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
POWER SUPPLY REQUIREMENTS						
Operating Current	$I_{CC}1$	-	-	10	mA	V_{CC} = 5.5V, CS = 1
Standby Current	$I_{CC}2$	-	-	3	mA	V_{CC} = 5.5V, CS = 0
E/W Operating Current	$I_{CC}3$	-	-	12	mA	V_{CC} = 5.5V
Power Consumption (Operating)	$P_{CC}1$	-	-	55	mW	V_{CC} = 5.5V, CS = 1
Power Consumption (Standby)	$P_{CC}2$	-	-	17	mW	V_{CC} = 5.5V, CS = 0
Power Consumption (E/W)	$P_{CC}3$	-	-	66	mW	V_{CC} = 5.5V, CS = 1

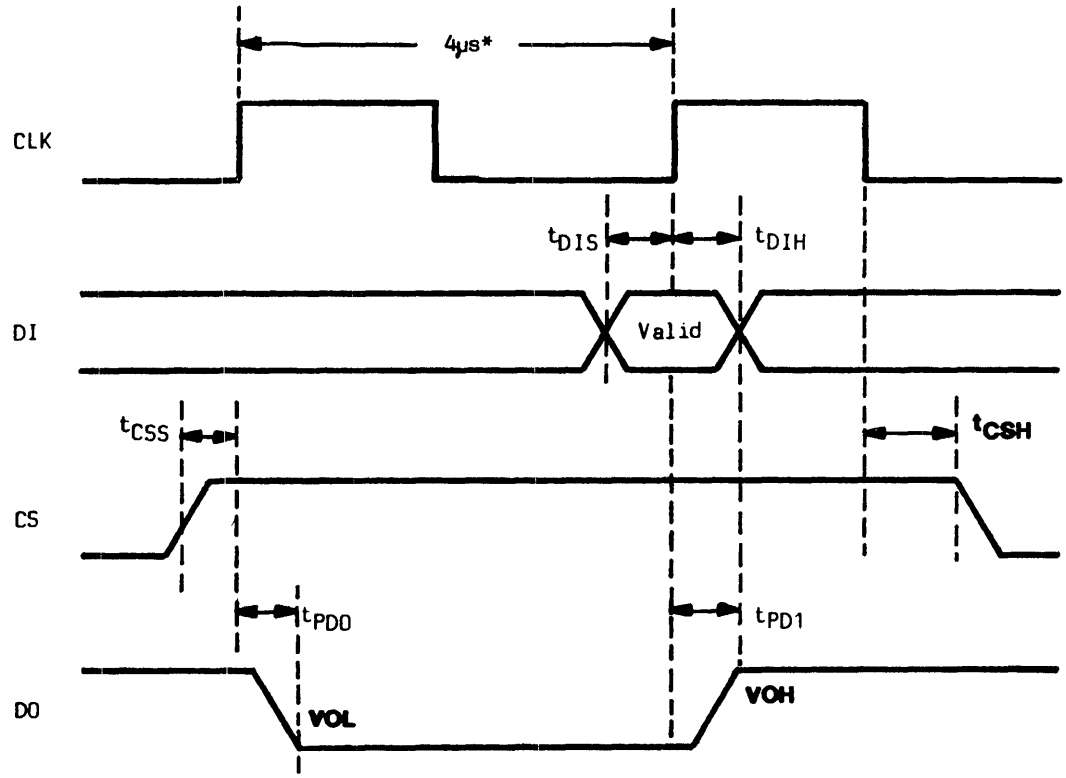
AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	f_{CLK}	0	-	250	KHZ	
Clock Duty Cycle	D_{CLK}	25	-	75	%	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
DO Output Delay (H to L)	t_{PDO}	-	-	2	µs	C_L = 100pf
DO Output Delay (L to H)	t_{PDI}	-	-	2	µs	C_L = 100pf
Erase/Write Pulse Width	$t_{E/W}$	10	-	30	ms	
Input Capacitance	C_I	-	-	6	pf	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pf	V_{OUT} = 0V

Table 1 - Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase Register A3A2A1A0
EWEN	1	0011	0000		Erase/write enable
EWDS	1	0000	0000		Erase/write disable
ERAL	1	0010	0000		Erase all registers

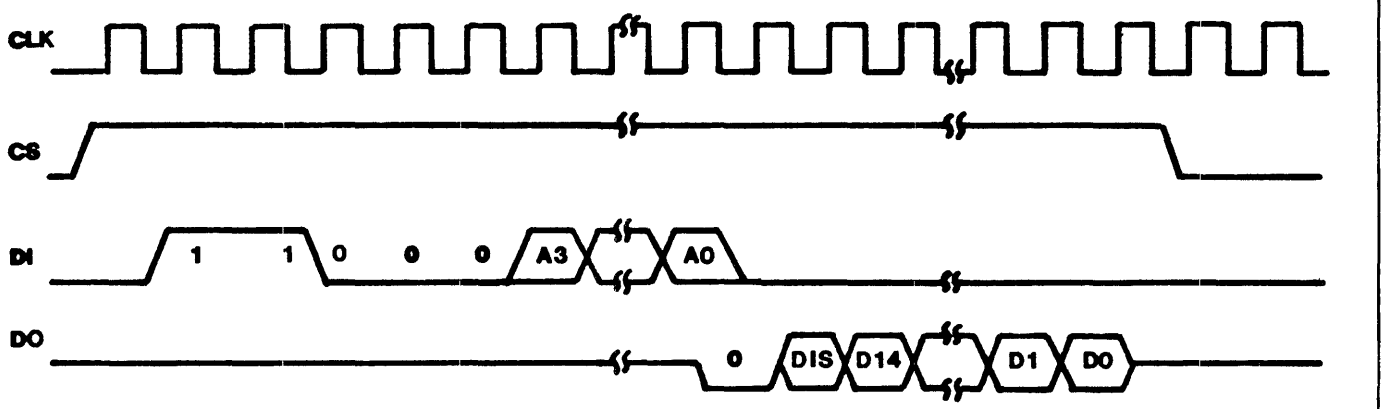
Figure 1. Synchronous Data Timing



*This is the maximum clock frequency.

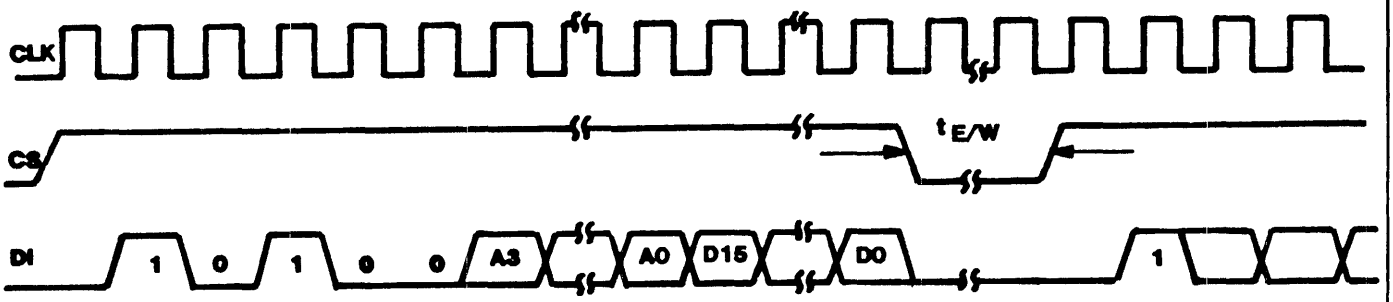
DS20014H-3

Figure 2. Read Mode



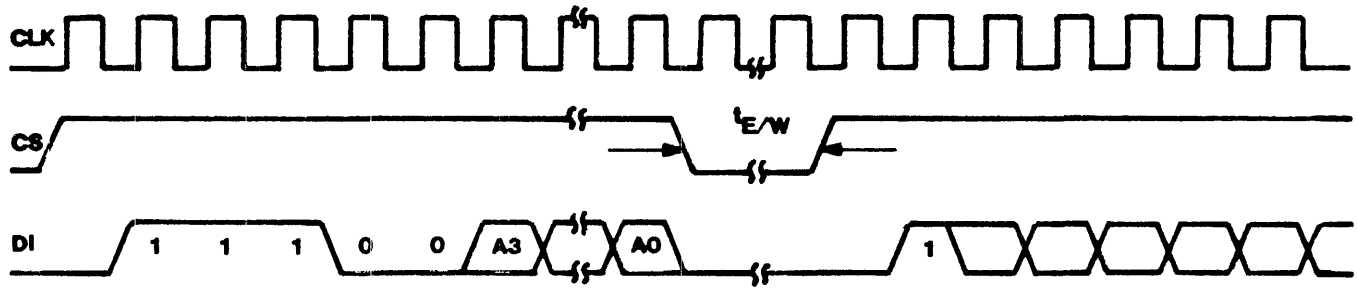
The READ instruction is the only instruction which outputs serial data on the DO pin. Only during the READ mode is the output pin (DO) valid. During all other modes the DO pin is in tri-state, eliminating bus contention. A dummy bit (logical "0") precedes the 16-bit output string. The output data changes during the high state of the system clock.

Figure 3. Write Mode



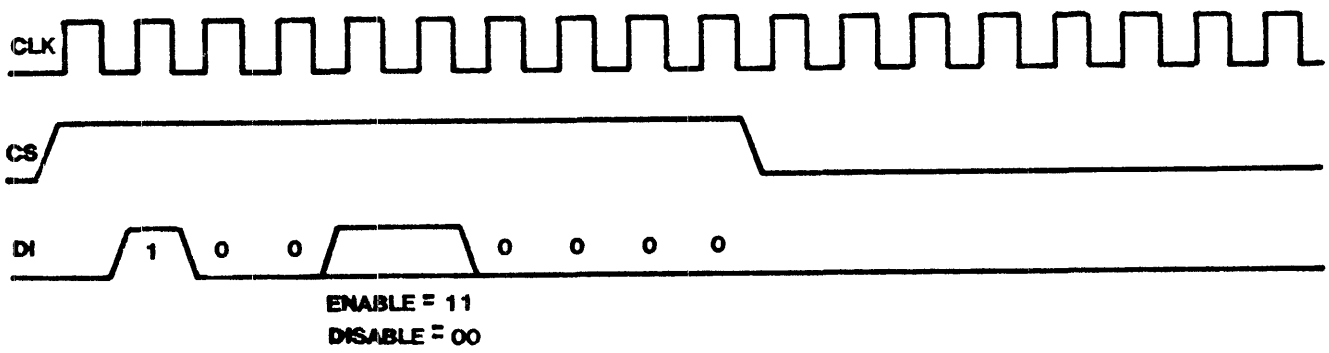
The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one CLK period, or followed by another instruction.

Figure 4. Erase Mode



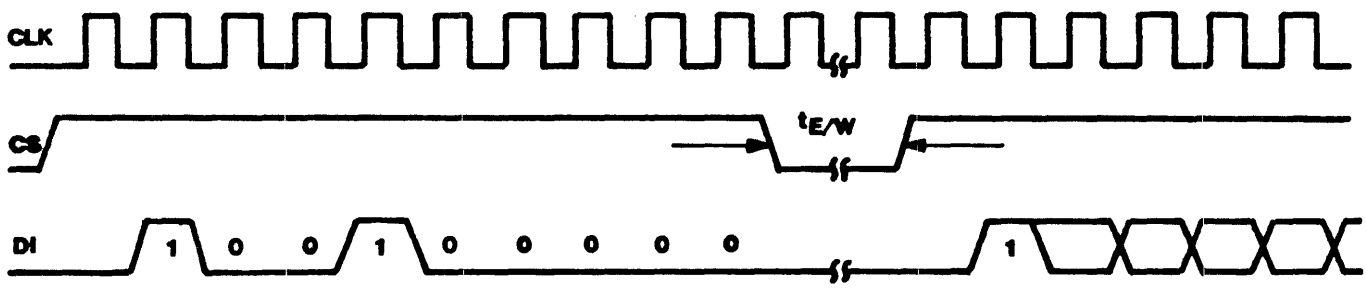
Like most E^2PROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one CLK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

Figure 5. Erase/Write Enable and Disable



Programming must be preceded once by an Erase/Write Enable (EWEN) instruction. Programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions. The device powers up in the Erase/Write Disable (EWDS) mode.

Figure 6. Chip Erase Mode

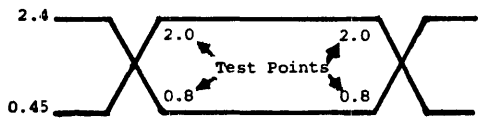


Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power On/Off Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

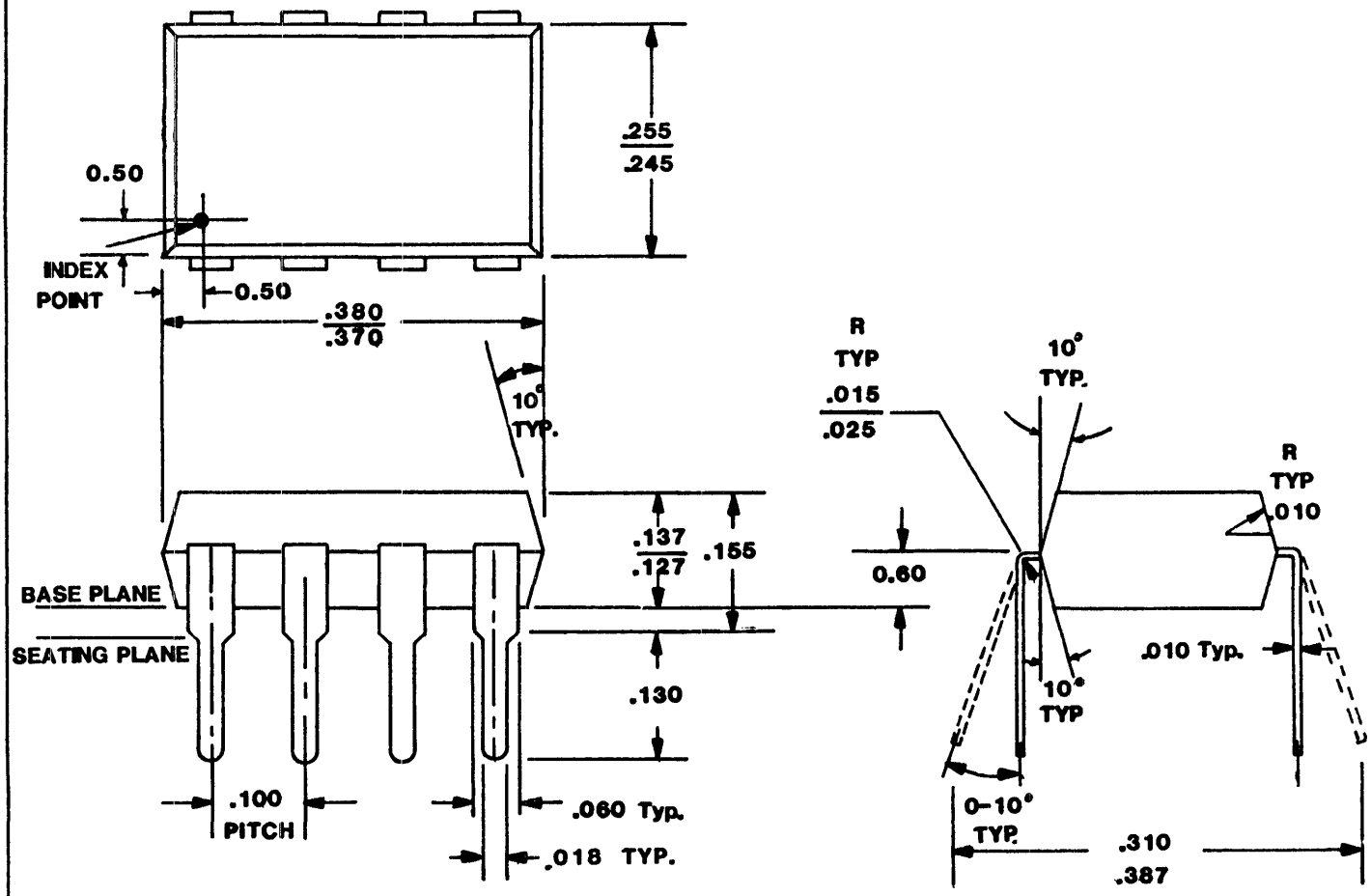
A.C. Testing Input/Output Waveform



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20014H-7

GENERAL INSTRUMENT	ER59256I

256 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

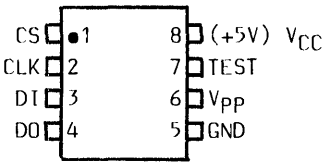
FEATURES

- Low cost
- 16 x 16 serial EEPROM
- Single +5V only operation
- Binary addressing
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- -40°C to +85°C operating ambient temperature range
- Power on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line

TOP VIEW



PIN FUNCTIONS

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground

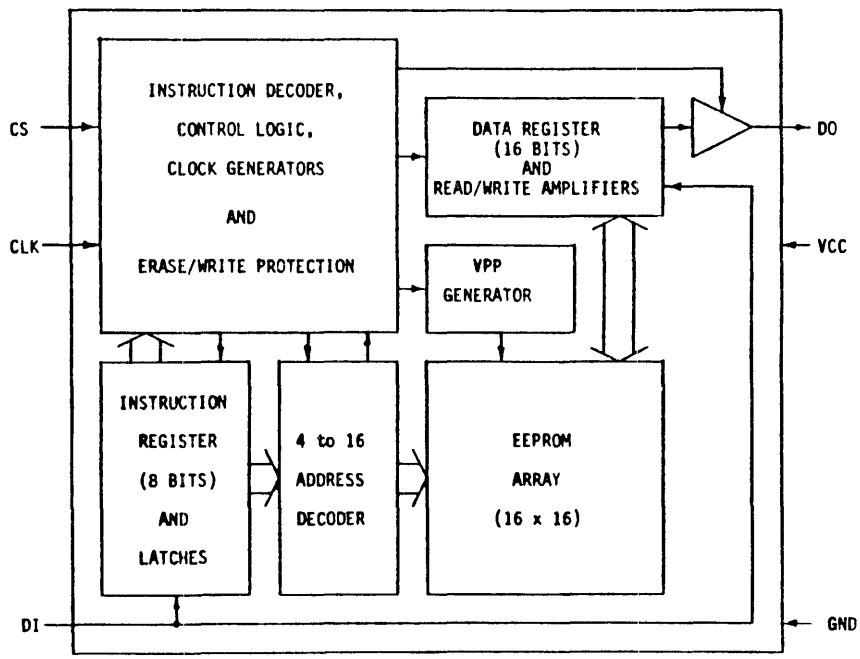
TEST PINS

V_{PP}	High Voltage Test (Float)
TEST	EEPROM Margin Test (Ground/Float)

DESCRIPTION

The ER59256I is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5V only operation and microcomputer compatible architecture. Six 9-bit instructions can be executed. See Table 1. The instruction format has a logical "1" as a start bit, four bits as an op code, and four bits of address. See Table 1.

BLOCK DIAGRAM



DS20021A-1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to 150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless otherwise noted)
V_{CC} = +5 + 10% volts
GND = 0 volts
Operating Temperature Range (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability of fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3.2mA
Input Leakage Current	I_{LI}	-	-	±10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	±10	µA	V_{OUT} = GND to V_{CC}
POWER SUPPLY REQUIREMENTS						
Operating Current	$I_{CC}1$	-	-	13	mA	V_{CC} = 5.5V, CS = 1
Standby Current	$I_{CC}2$	-	-	5	mA	V_{CC} = 5.5V, CS = 0
E/W Operating Current	$I_{CC}3$	-	-	15	mA	V_{CC} = 5.5V
Power Consumption (Operating)	$P_{CC}1$	-	-	72	mW	V_{CC} = 5.5V, CS = 1
Power Consumption (Standby)	$P_{CC}2$	-	-	28	mW	V_{CC} = 5.5V, CS = 0
Power Consumption (E/W)	$P_{CC}3$	-	-	83	mW	V_{CC} = 5.5V, CS = 1

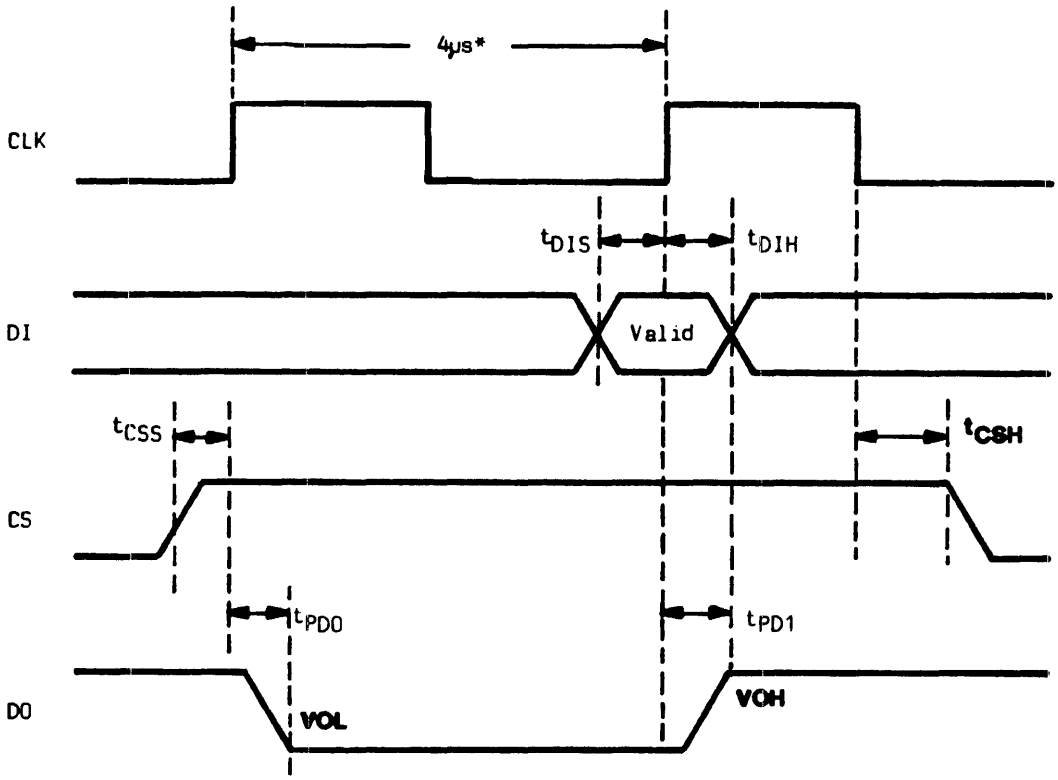
AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	f_{CLK}	0	-	250	KHZ	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
DO Output Delay (H to L)	t_{PDO}	-	-	2	µs	C_L = 100pf
DO Output Delay (L to H)	t_{PDI}	-	-	2	µs	C_L = 100pf
Erase/Write Pulse Width	$t_{E/W}$	10	-	30	ms	
Input Capacitance	C_I	-	-	6	pf	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pf	V_{OUT} = 0V

Table 1 - Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase Register A3A2A1A0
EWEN	1	0011	0000		Erase/write enable
EWDS	1	0000	0000		Erase/write disable
ERAL	1	0010	0000		Erase all registers

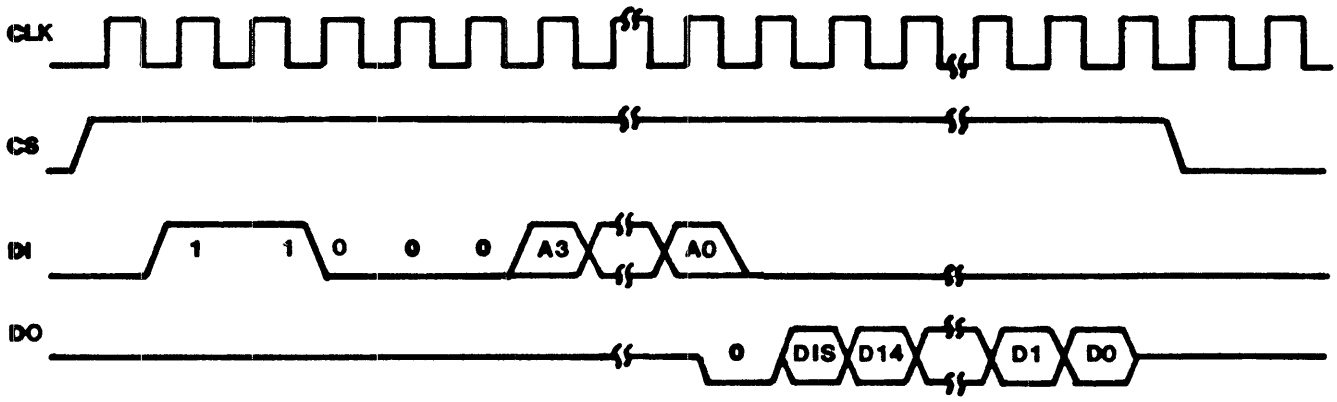
Figure 1. Synchronous Data Timing



*This is the maximum clock frequency.

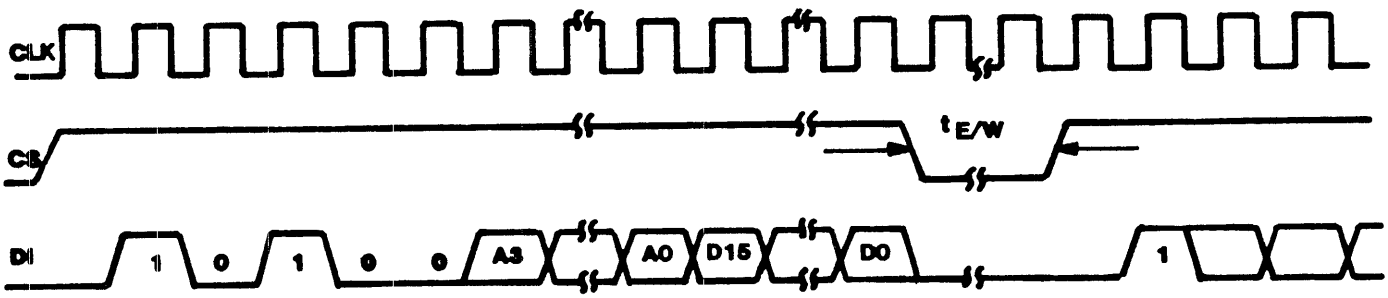
DS20021A-3

Figure 2. Read Mode



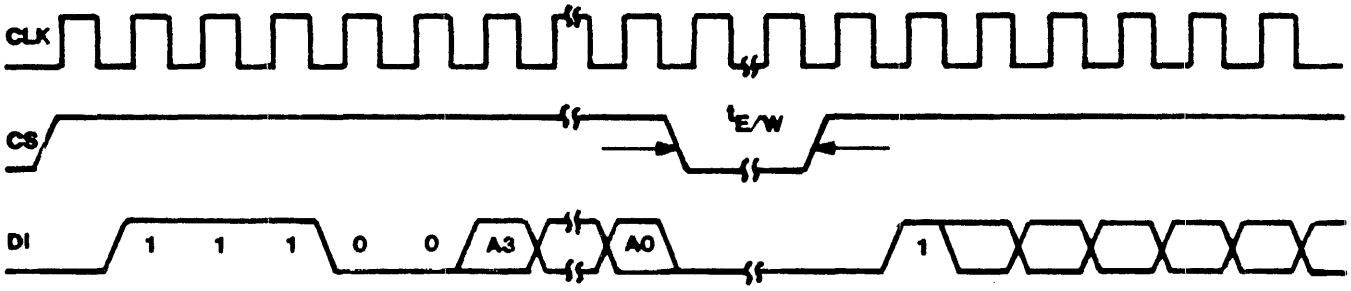
The READ instruction is the only instruction which outputs serial data on the DO pin. Only during the READ mode is the output pin (DO) valid. During all other modes the DO pin is in tri-state, eliminating bus contention. A dummy bit (logical "0") precedes the 16-bit output string. The output data changes during the high state of the system clock.

Figure 3. Write Mode



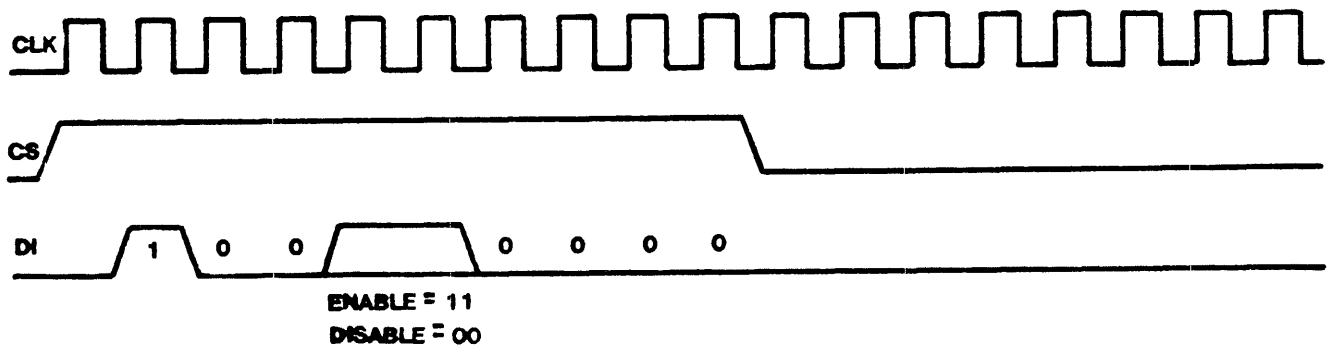
The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one CLK period, or followed by another instruction.

Figure 4. Erase Mode



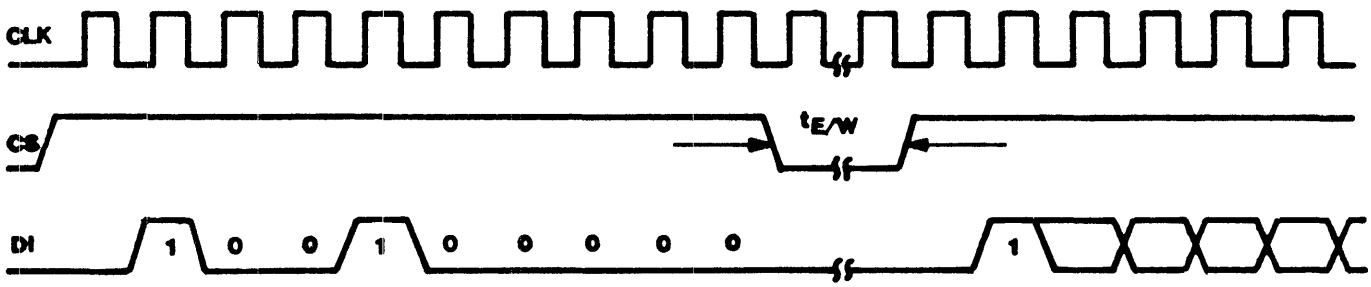
Like most E^2PROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one CLK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

Figure 5. Erase/Write Enable and Disable



Programming must be preceded once by an Erase/Write Enable (EWEN) instruction. Programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions. The device powers up in the Erase/Write Disable (EWDS) mode.

Figure 6. Chip Erase Mode

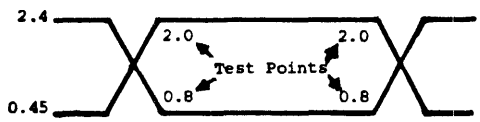


Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power On/Off Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

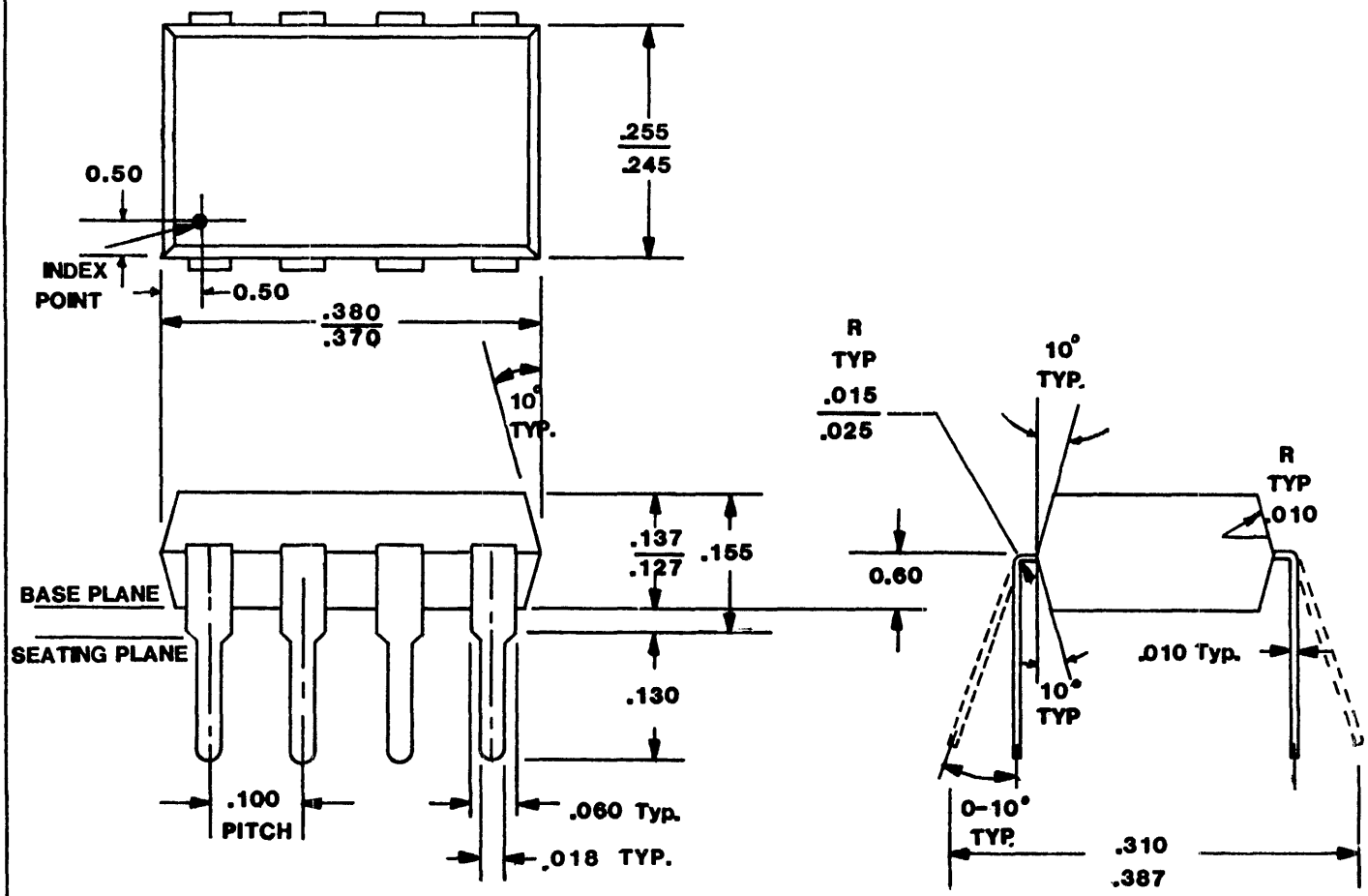
A.C. TESTING, INPUT AND OUTPUT WAVEFORMS



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20021A-7

GENERAL INSTRUMENT	ER5911

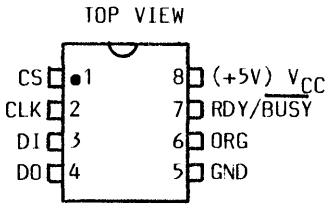
1024 SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES

- Low cost
- User-selectable organization: 64 x 16 or 128 x 8
- Single +5V only operation
- Binary addressing
- Fully automatic self-timed erase/write mode
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range
- Power-on/off data protection circuitry

PIN CONFIGURATION

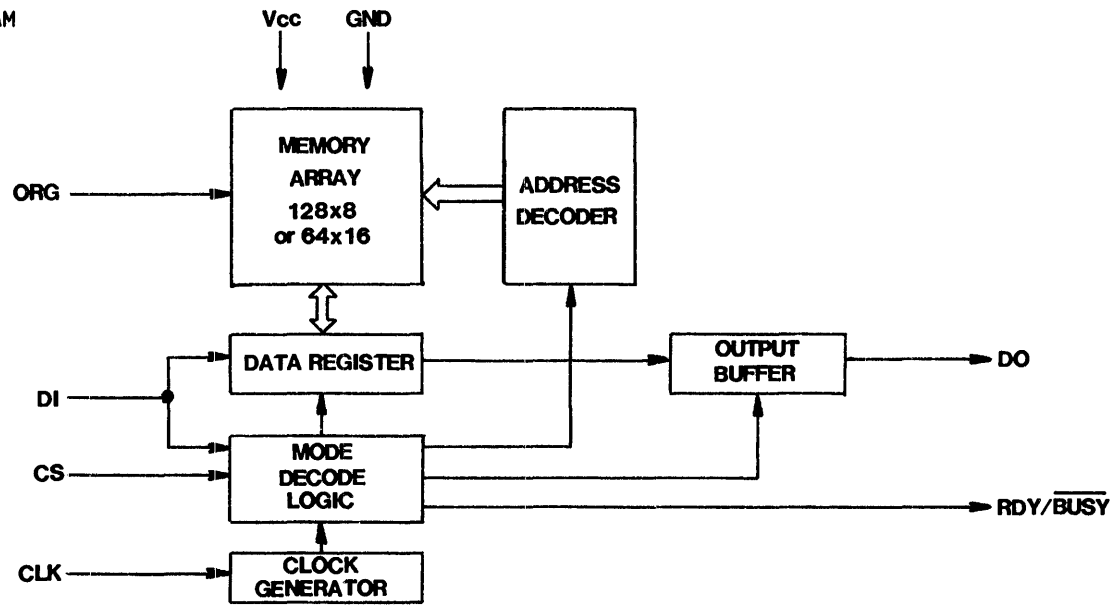
8 Pin Dual-In-Line



DESCRIPTION

The ER5911 is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. This device features +5V only operation, a self-timed reprogramming cycle and two user-selectable memory array organizations, 64 x 16 or 128 x 8, which are selectable externally by means of a one bit code applied to control pin ORG. The Input (DI) and Output (DO) pins are controlled by separate serial formats. When separate lines are used the DO output pin is valid only in the read mode and is in the high impedance state in all other modes, thus eliminating bus contention. Five instructions may be executed and the instruction length will be twelve bits when using the 128 x 8 organization and eleven bits when the 64 x 16 organization is used. The instruction format has a logical 1 as a start bit, four bits as an opcode and either six or seven address bits.

BLOCK DIAGRAM



DS20017F-1

PIN FUNCTIONS

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
RDY/$\overline{BUSY}$	Status Output
GND	Ground

ORG Memory Array Organization Selection Input. When the ORG pin is connected to +5V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0 0 0	A_6-A_0	A_5-A_0			Read Address A_N-A_0
PROGRAM	1	X 1 0 0	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
PEN	1	0 0 1 1	0000000	000000			Program Enable
PDS	1	0 0 0 0	0000000	000000			Program Disable
ERAL	1	0 0 1 0	0000000	000000			Erase All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and
without data retention)..... -65°C to +150°C
Soldering temperature of leads
(10 seconds)..... +300°C

Standard Conditions (Unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V +10% volts
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	-	10	mA	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	I_{CC}	-	-	12	mA	V_{CC} = 5.5V
Chip Deselected (STANDBY)	I_{CC}	-	-	3	mA	V_{CC} = 5.5V
Power Consumption						
Chip Selected	P_{CC}	-	-	55	mW	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	P_{CC}	-	-	66	mW	V_{CC} = 5.5V
Chip Deselected (STANDBY)	P_{CC}	-	-	17	mW	V_{CC} = 5.5V

AC CHARACTERISTICS (See Figure 1)

Characteristic	Sym	Min	Typ	Max	Units	Conditions
CLK Frequency	f_{CLK}	0	-	250	KHz	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
CLK Pulse Width	t_{CPW}	2.0	-	-	µs	
Data Output Delay	t_{PD1}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Data Output Delay	t_{PD0}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Status Low Time (programming time)	t_{PR}	20	40	75	ms	

Figure 1 Synchronous Data Timing

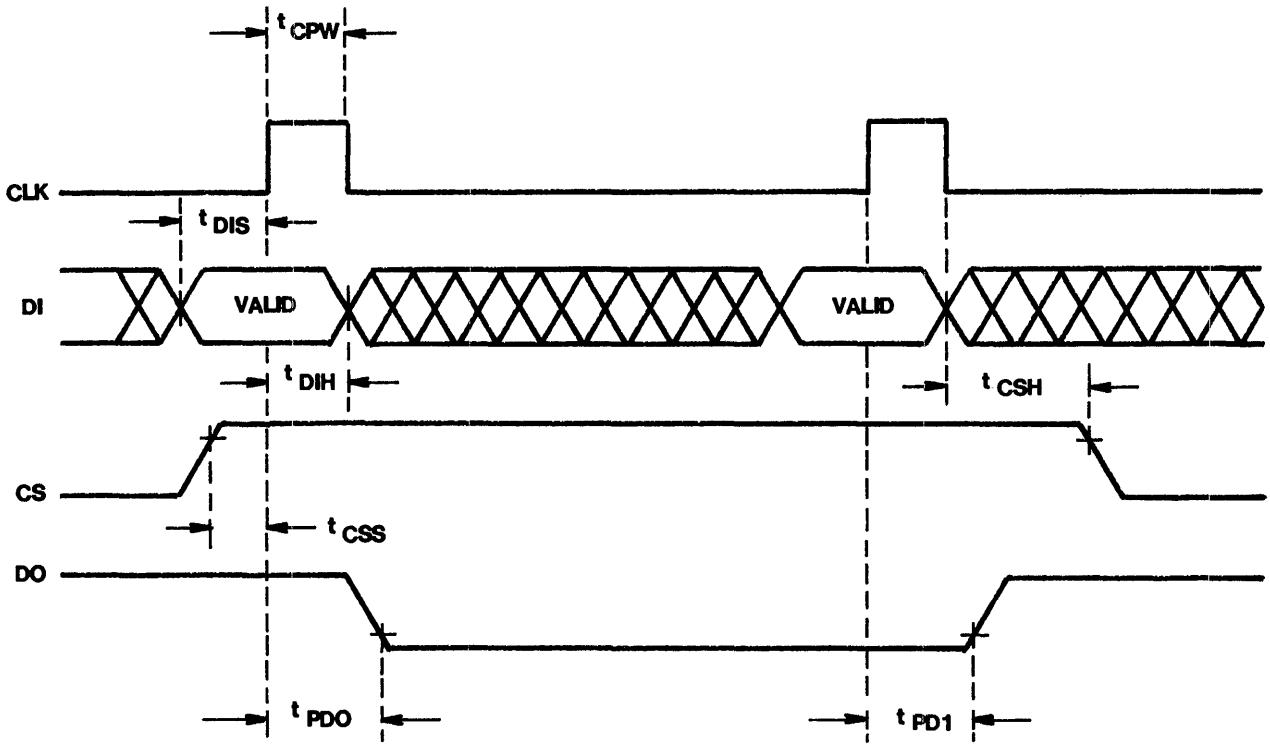
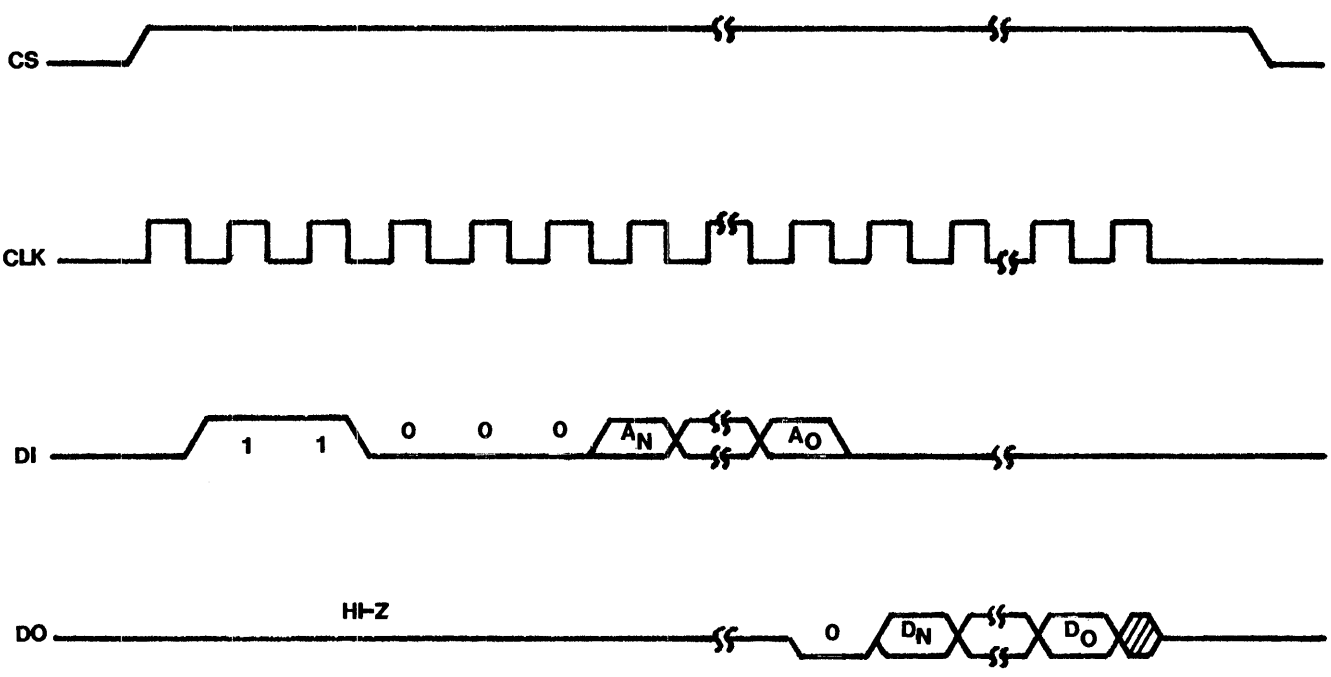


Figure 2 READ Mode

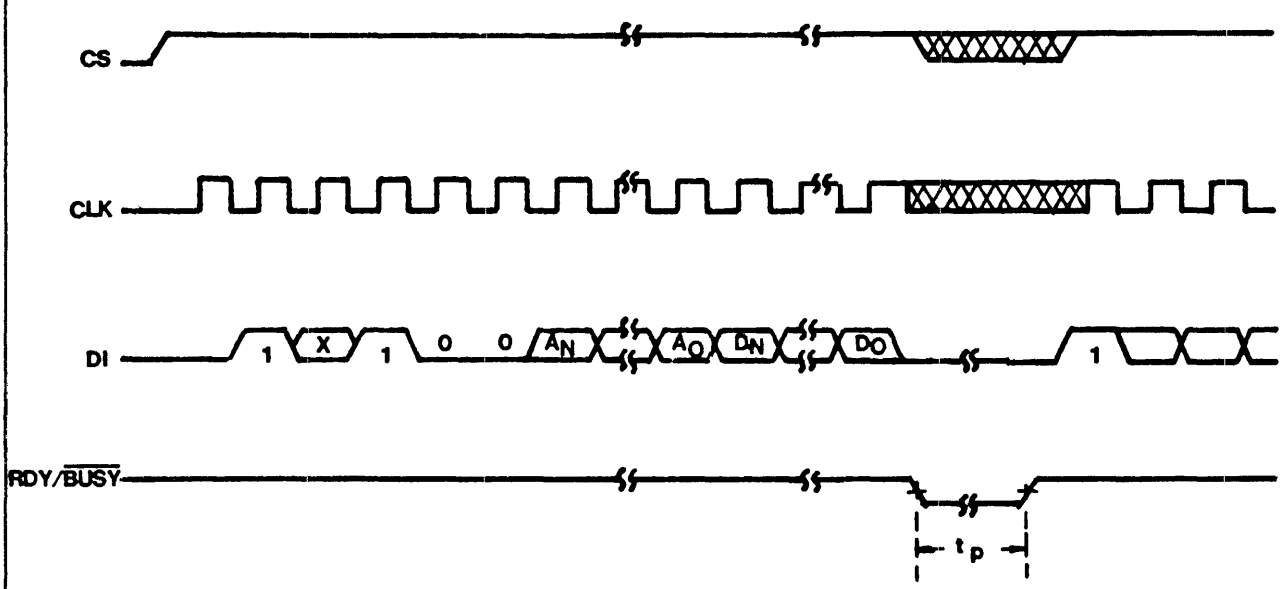


Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string. The output data changes during the high states of the system clock.

Figure 3 PROGRAM Mode



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Program Mode

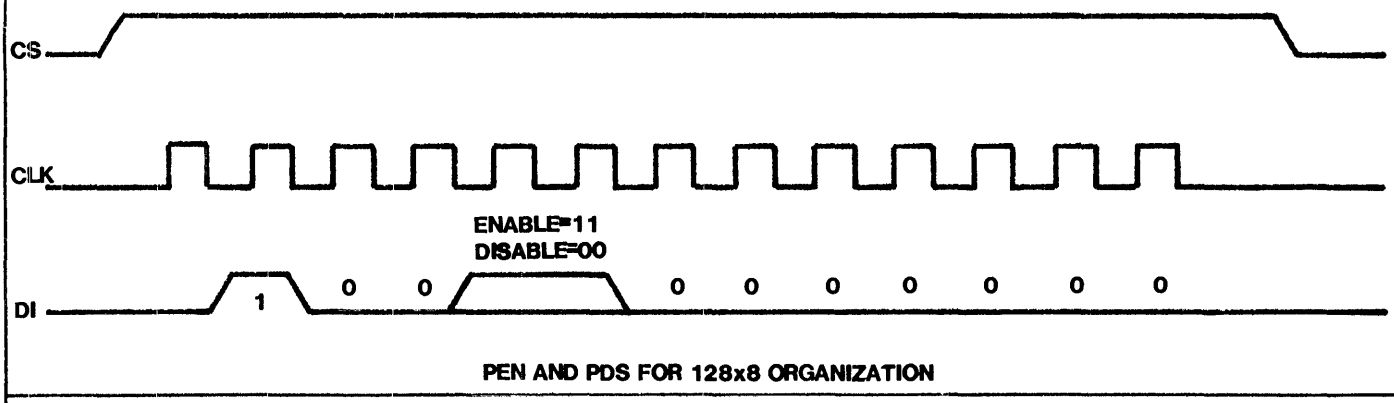
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

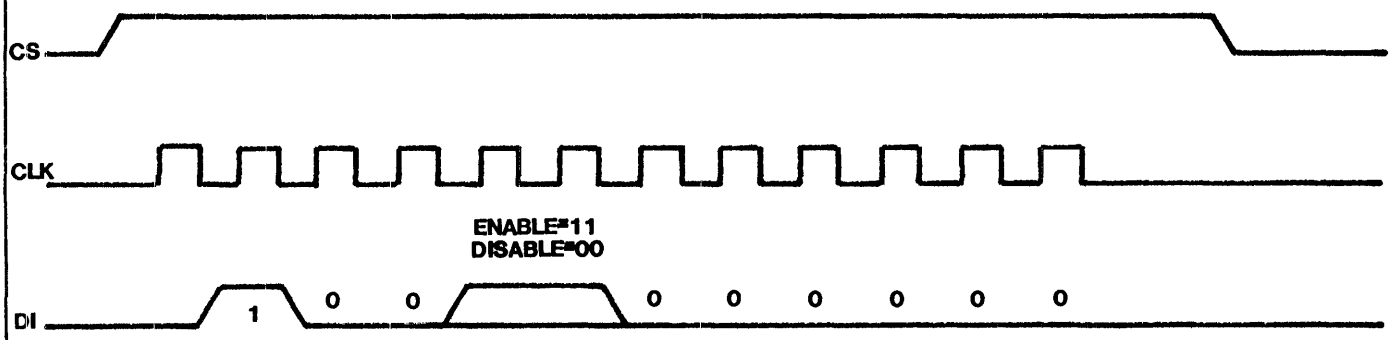
During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4 PEN (Program Enable) and PDS (Program Disable)



PEN AND PDS FOR 128x8 ORGANIZATION

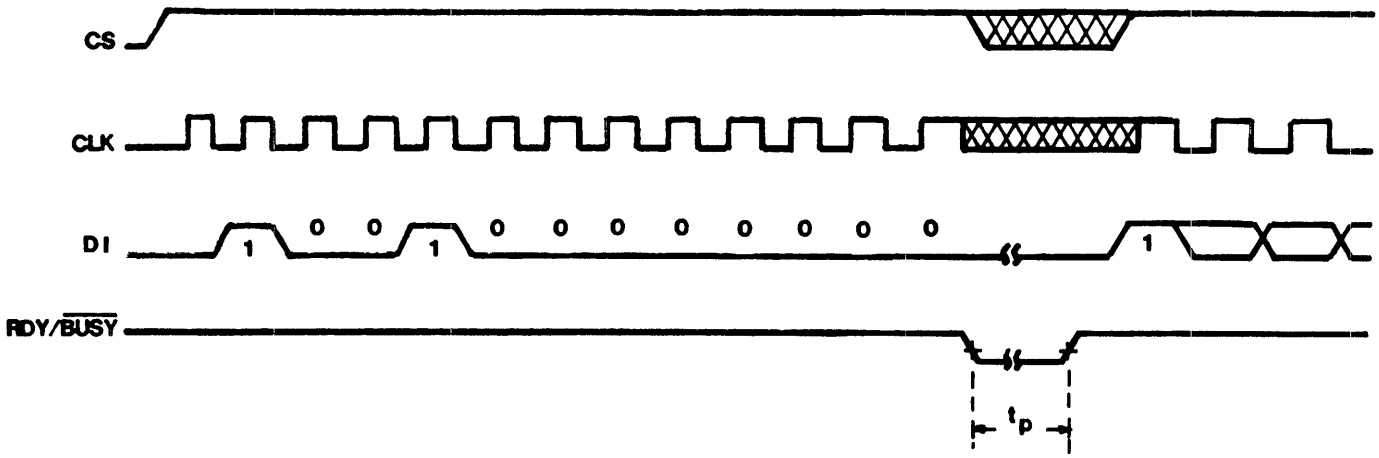


PEN AND PDS FOR 64x16 ORGANIZATION

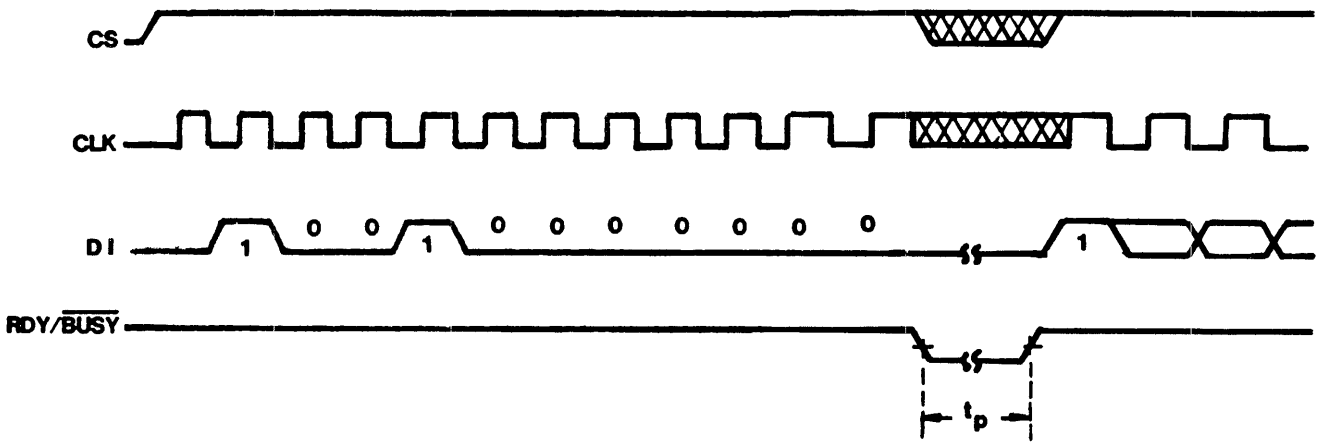
Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Figure 5 ERAL (Erase All) Mode (128 x 8)



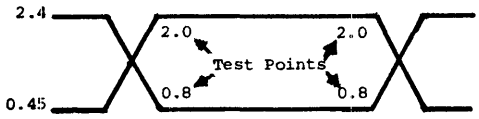
ERAL (Erase All) Mode (64 x 16)



Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a 1.

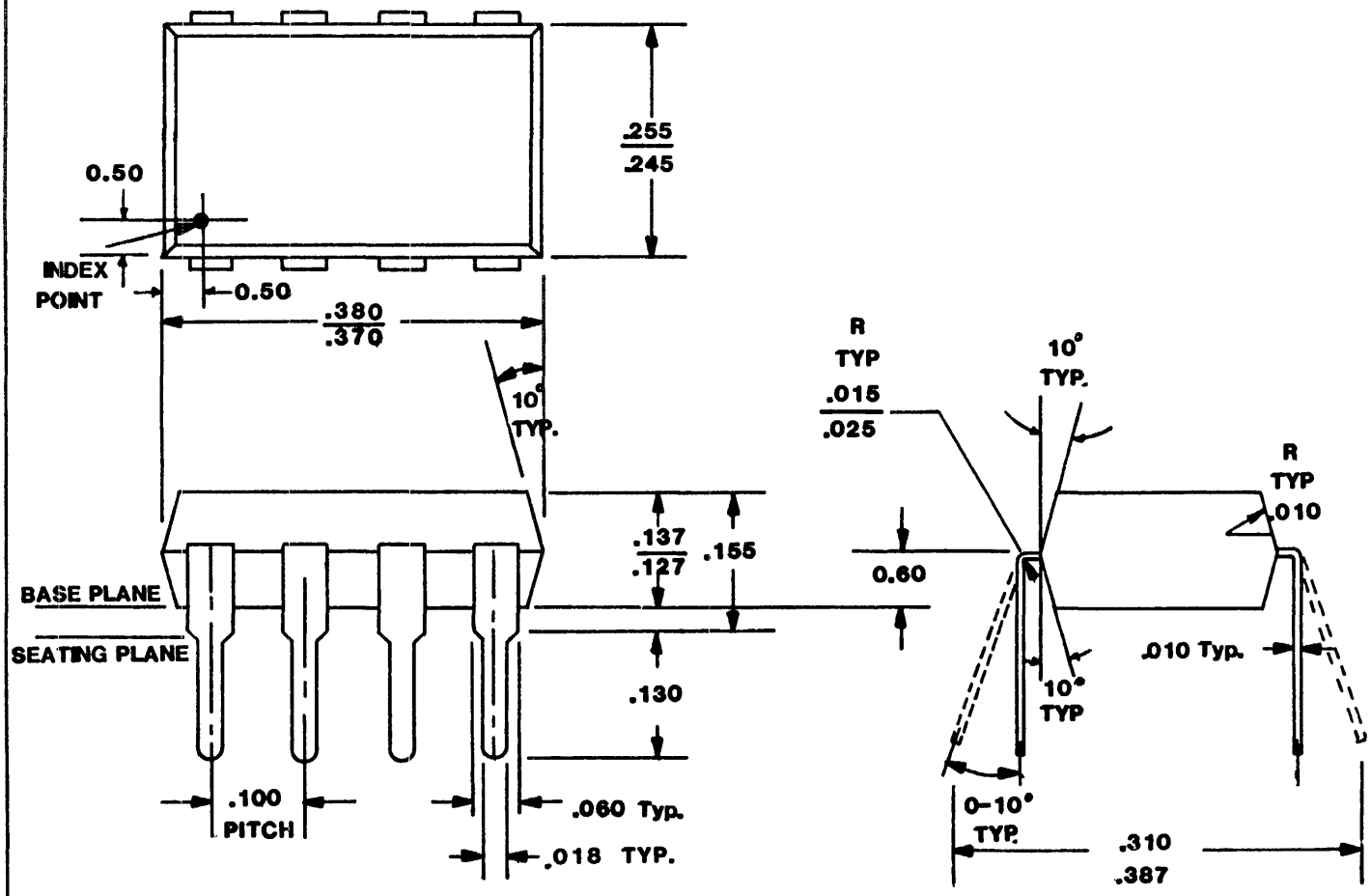
A.C. Testing Input/Output Waveform



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

1024 SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

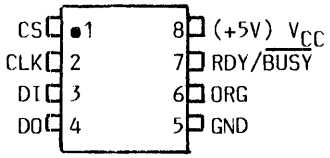
FEATURES

- Low cost
- User-selectable organization: 64 x 16 or 128 x 8
- Single +5V only operation
- Binary addressing
- Fully automatic self-timed erase/write mode
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- -40°C to +85°C operating ambient temperature range
- Power-on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line

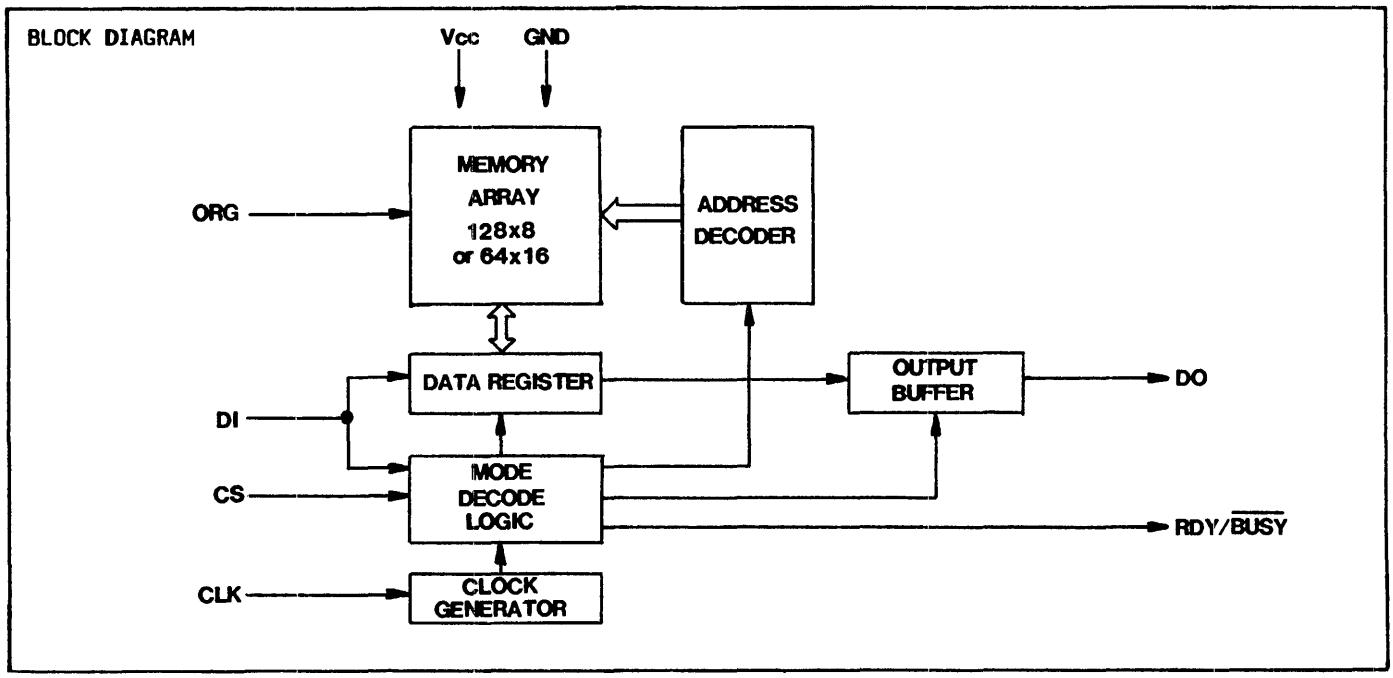
TOP VIEW



DESCRIPTION

The ER5911I is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. This device features +5V only operation, a self-timed reprogramming cycle and two user-selectable memory array organizations, 64 x 16 or 128 x 8, which are selectable externally by means of a one bit code applied to control pin ORG. The Input (DI) and Output (DO) pins are controlled by separate serial formats. When separate lines are used the DO output pin is valid only in the read mode and is in the high impedance state in all other modes, thus eliminating bus contention. Five instructions may be executed and the instruction length will be twelve bits when using the 128 x 8 organization and eleven bits when the 64 x 16 organization is used. The instruction format has a logical 1 as a start bit, four bits as an opcode and either six or seven address bits.

BLOCK DIAGRAM



PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5V Power Supply		
RDY/$\overline{BUSY}$	Status Output		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0 0 0	A_6-A_0	A_5-A_0			Read Address A_N-A_0
PROGRAM	1	X 1 0 0	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
PEN	1	0 0 1 1	0000000	000000			Program Enable
PDS	1	0 0 0 0	0000000	000000			Program Disable
ERAL	1	0 0 1 0	0000000	000000			Erase All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and
without data retention)..... -65°C to +150°C
Soldering temperature of leads
(10 seconds)..... +300°C

Standard Conditions (Unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V +10% volts
Operating Temperature Range (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400uA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	-	12	mA	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	I_{CC}	-	-	15	mA	V_{CC} = 5.5V
Chip Deselected (STANDBY)	I_{CC}	-	-	5	mA	V_{CC} = 5.5V
Power Consumption						
Chip Selected	P_{CC}	-	-	66	mW	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	P_{CC}	-	-	83	mW	V_{CC} = 5.5V
Chip Deselected (STANDBY)	P_{CC}	-	-	28	mW	V_{CC} = 5.5V

AC CHARACTERISTICS (See Figure 1)

Characteristic	Sym	Min	Typ	Max	Units	Conditions
CLK Frequency	f_{CLK}	0	-	250	KHz	
CLK Duty Cycle	D_{CLK}	25	-	75	%	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Selected Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
CLK Pulse Width	t_{CPW}	2.0	-	-	µs	
Data Output Delay	t_{PD1}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Data Output Delay	t_{PDO}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Status Low Time (programming time)	t_{PR}	20	40	75	ms	

Figure 1 Synchronous Data Timing

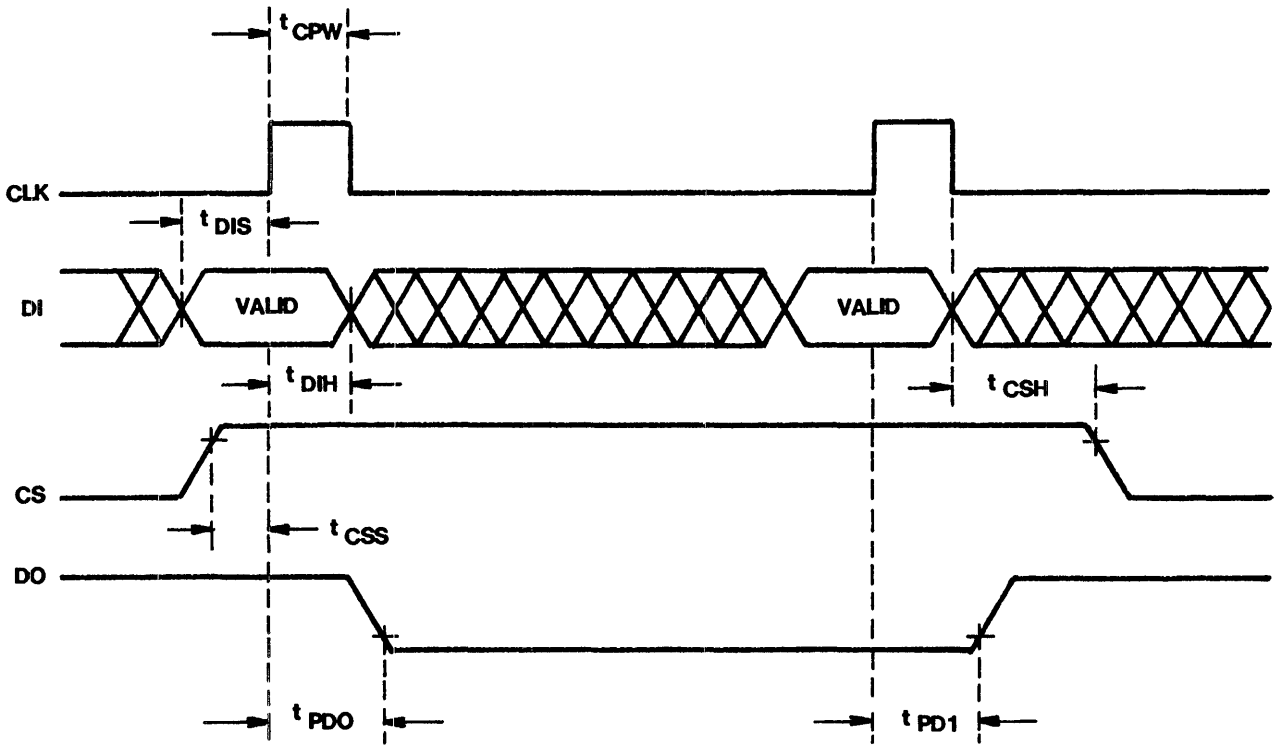
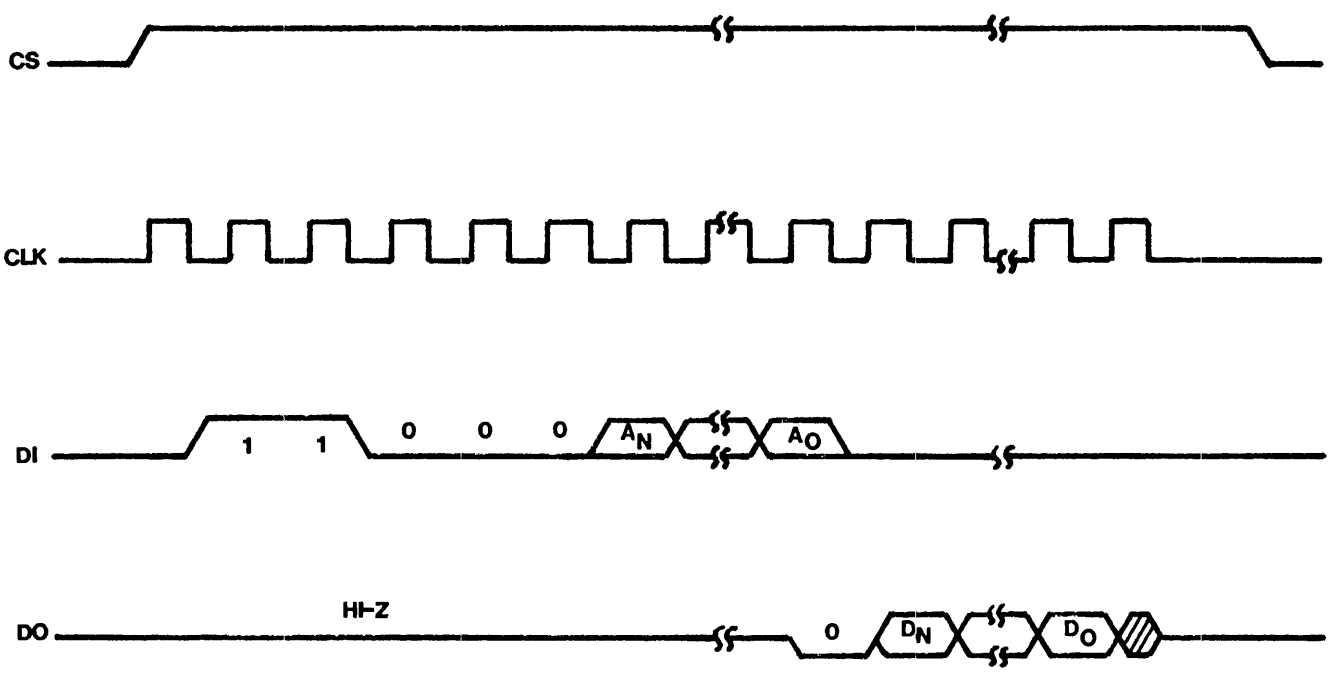


Figure 2 READ Mode

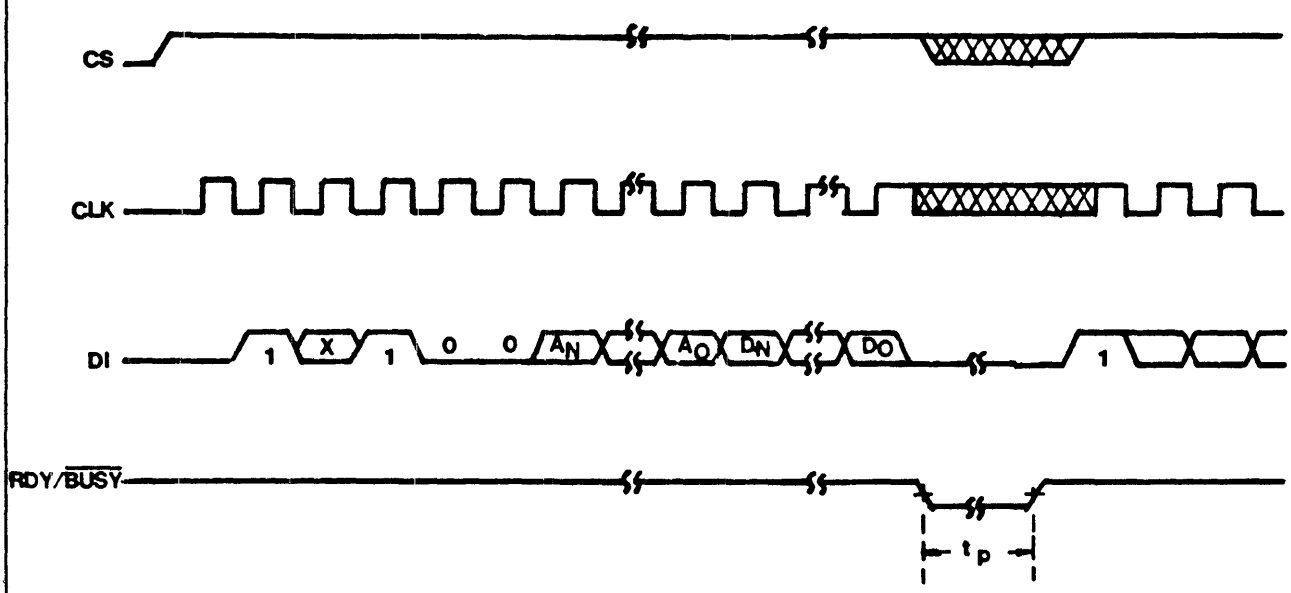


Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string. The output data changes during the high states of the system clock.

Figure 3 PROGRAM Mode



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Program Mode

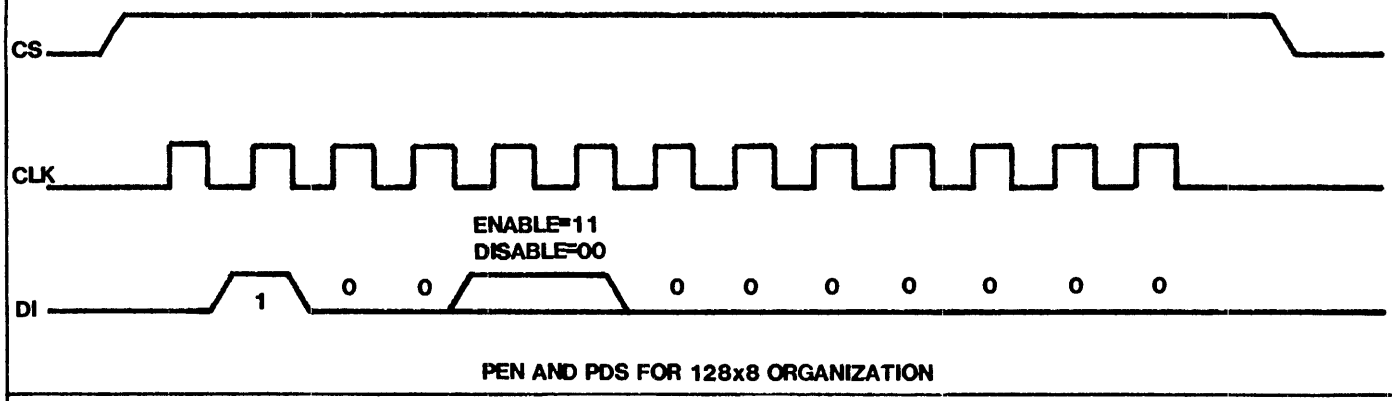
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

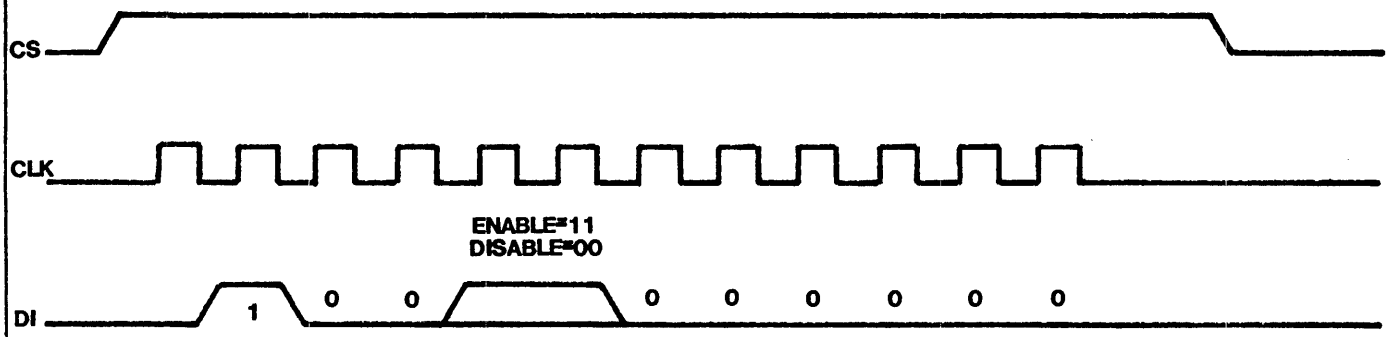
During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4 PEN (Program Enable) and PDS (Program Disable)



PEN AND PDS FOR 128x8 ORGANIZATION

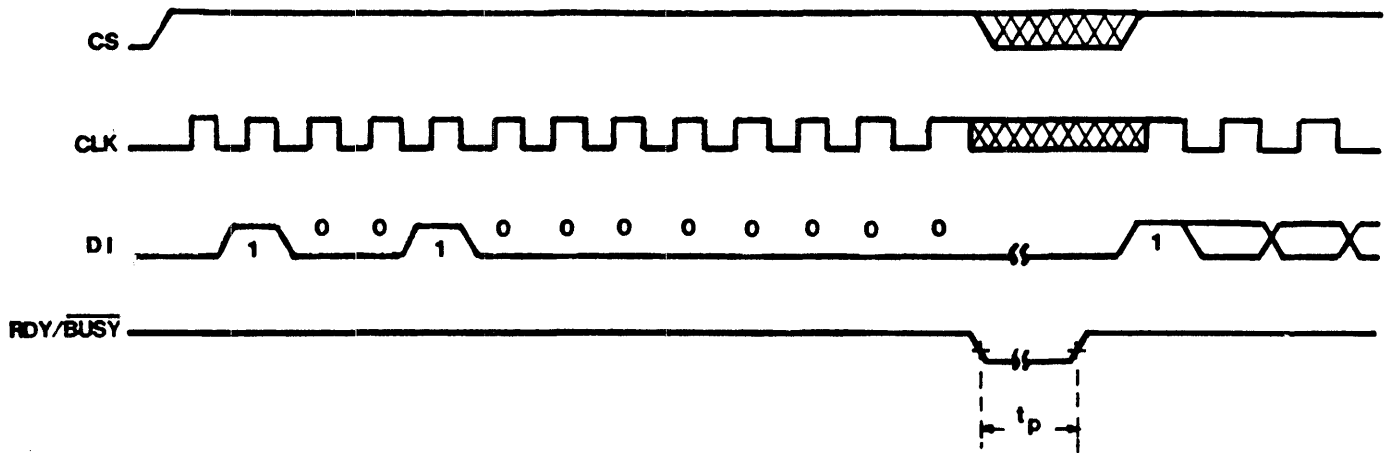


PEN AND PDS FOR 64x16 ORGANIZATION

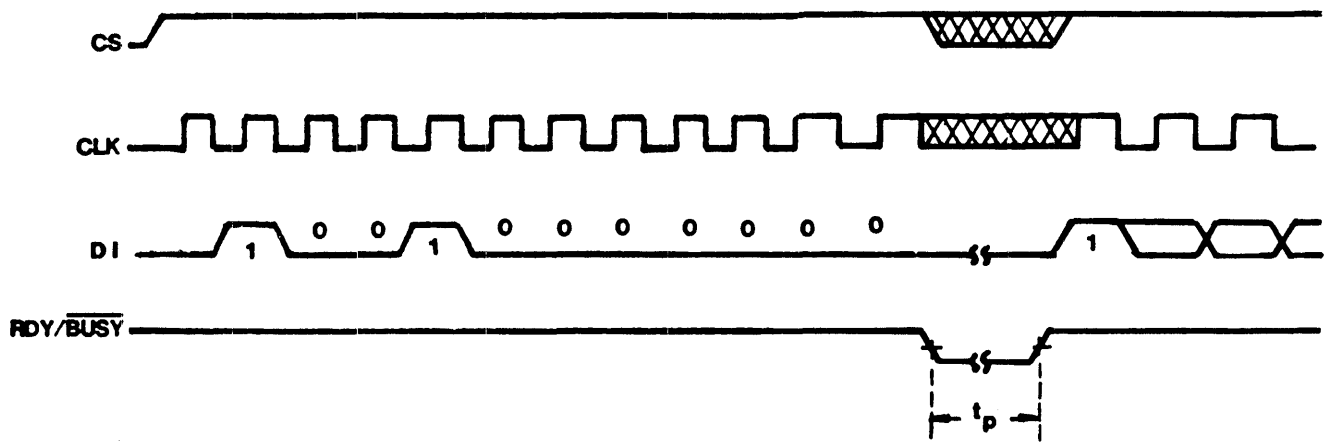
Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Figure 5 ERAL (Erase All) Mode (128 x 8)



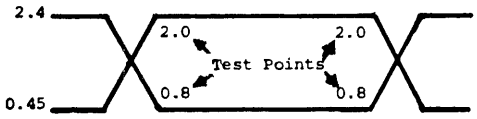
ERAL (Erase All) Mode (64 x 16)



Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a 1.

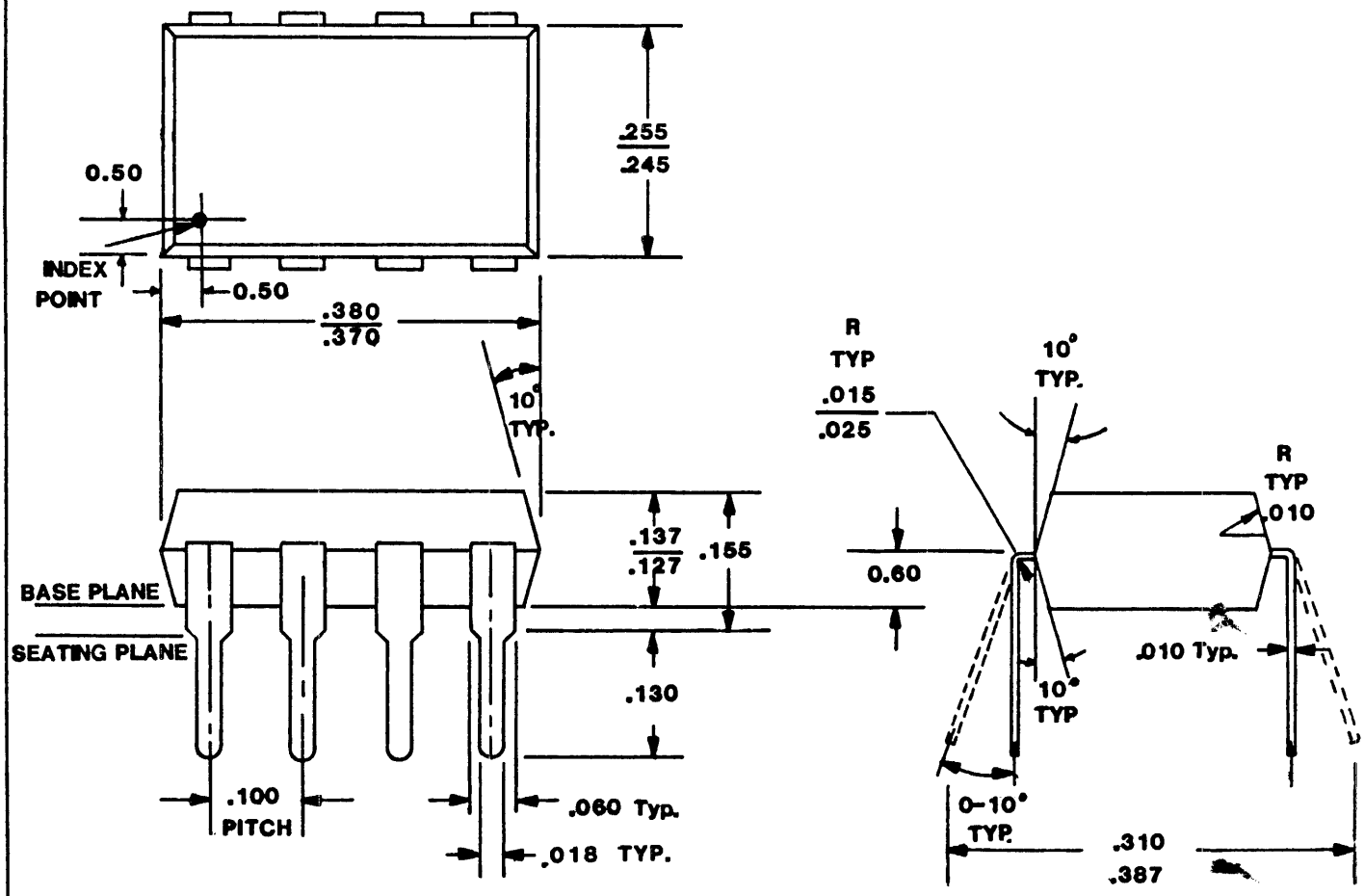
A.C. Testing Input/Output Waveform



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

2048 SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

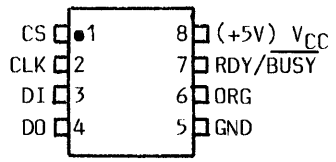
FEATURES

- Low cost
- User-selectable organization: 128 x 16 or 256 x 8
- Single +5V only operation
- Binary addressing
- Fully automatic self-timed erase/write mode
- Self timed separate erase and write modes
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range
- Power-on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line

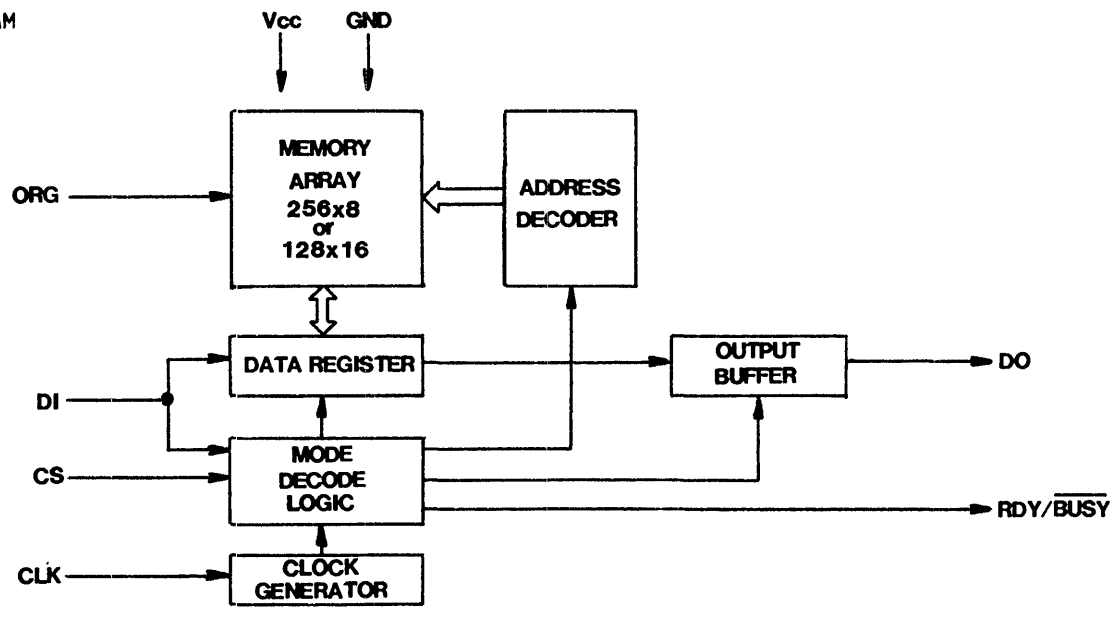
TOP VIEW



DESCRIPTION

The ER5912 is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. This device features +5V only operation, a self-timed reprogramming cycle as well as separate erase and write cycles and two user-selectable memory array organizations, 128 x 16 or 256 x 8, which are externally selectable by means of a one bit code applied to control pin ORG. The Data Input (DI) and Data Output (DO) pins are controlled by separate serial formats. When separate lines are used the DO output pin is valid only in the read mode and is in the high impedance state in all other modes, thus eliminating bus contention. Seven instructions may be executed and the instruction length will be thirteen bits when using the 256 x 8 organization and twelve bits when the 128 x 16 organization is used. The instruction format has a logical 1 as a start bit, four bits as an opcode and either seven or eight address bits.

BLOCK DIAGRAM



DS20024A-1

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5V the 128 x 16 organization is selected. When it is connected to ground the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5V Power Supply		
RDY/BUSY	Status Output		
GND	Ground		

INSTRUCTION SET

Instruction	Start Bit	opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0 0 0	A_7-A_0	A_6-A_0			Read Address A_N-A_0
PROGRAM	1	X 1 0 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
ERASE	1	1 1 1 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Erase Address A_N-A_0
WRITE	1	0 1 1 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Write Address A_N-A_0
PEN	1	0 0 1 1	00000000	0000000			Program Enable
PDS	1	0 0 0 0	00000000	0000000			Program Disable
ERAL	1	0 0 1 0	00000000	0000000			Erase All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and
without data retention)..... -65°C to +150°C
Soldering temperature of leads
(10 seconds)..... +300°C

Standard Conditions (Unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V +10% volts
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400uA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	-	10	mA	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	I_{CC}	-	-	12	mA	V_{CC} = 5.5V
Chip Deselected (STANDBY)	I_{CC}	-	-	3	mA	V_{CC} = 5.5V
Power Consumption						
Chip Selected	P_{CC}	-	-	55	mW	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	P_{CC}	-	-	66	mW	V_{CC} = 5.5V
Chip Deselected (STANDBY)	P_{CC}	-	-	17	mW	V_{CC} = 5.5V

AC CHARACTERISTICS (See Figure 1)

Characteristic	Sym	Min	Typ	Max	Units	Conditions
CLK Frequency	f_{CLK}	0	-	500	KHz	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
CLK Pulse Width	t_{CPW}	1.0	-	-	µs	
Data Output Delay	t_{PD1}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Data Output Delay	t_{PD0}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Status Low Time						
programming time	t_{PR}	20	30	40	ms	
erase time	t_{ER}	10	-	20	ms	
write time	t_{PR}	10	-	20	ms	

Figure 1 Synchronous Data Timing

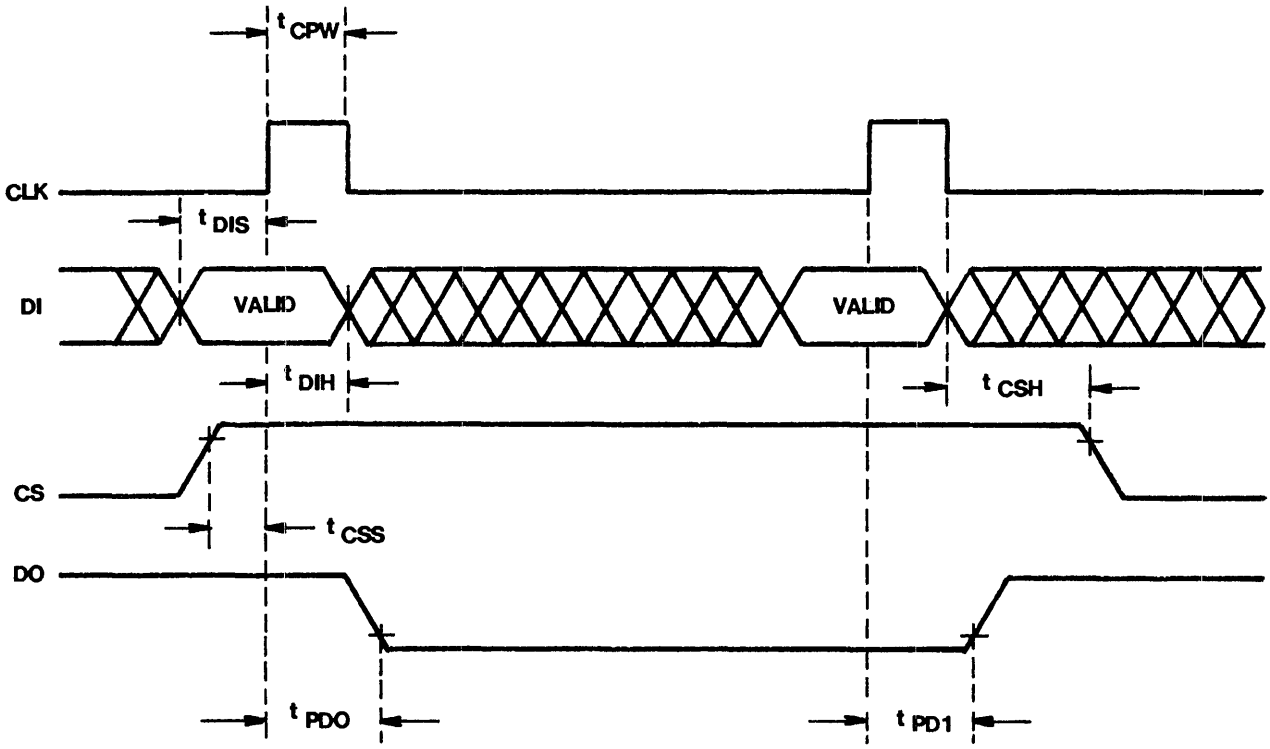
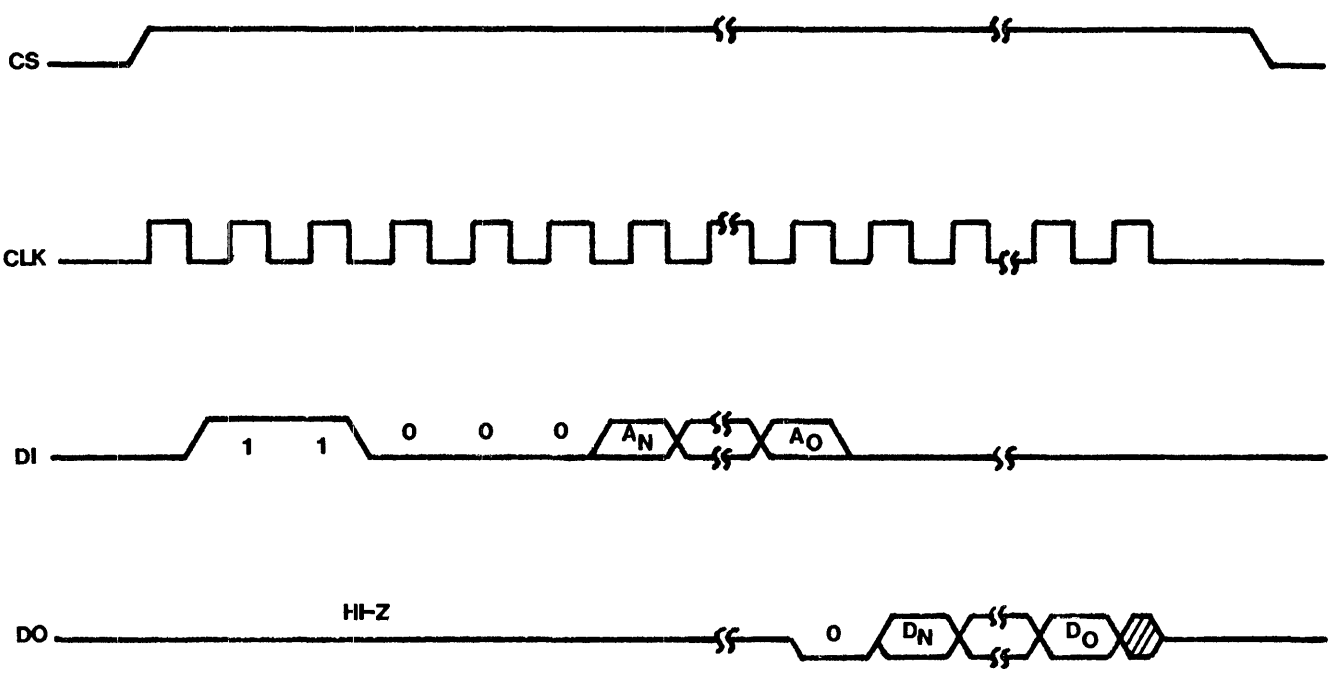


Figure 2 READ Mode

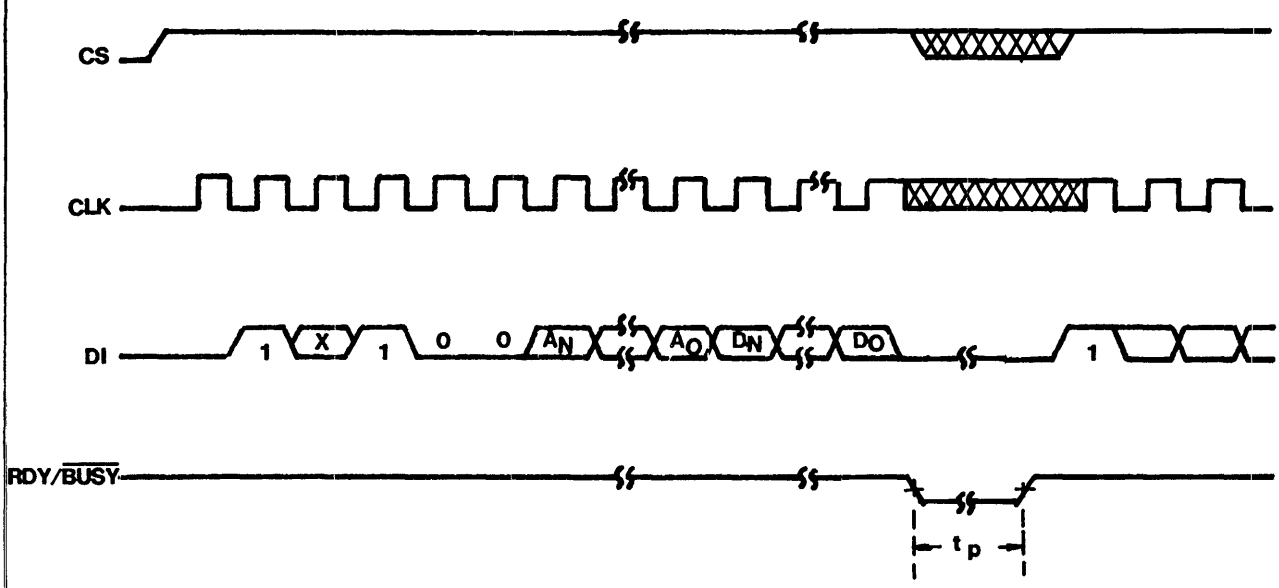


Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string.

Figure 3 PROGRAM Mode



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

Program Mode

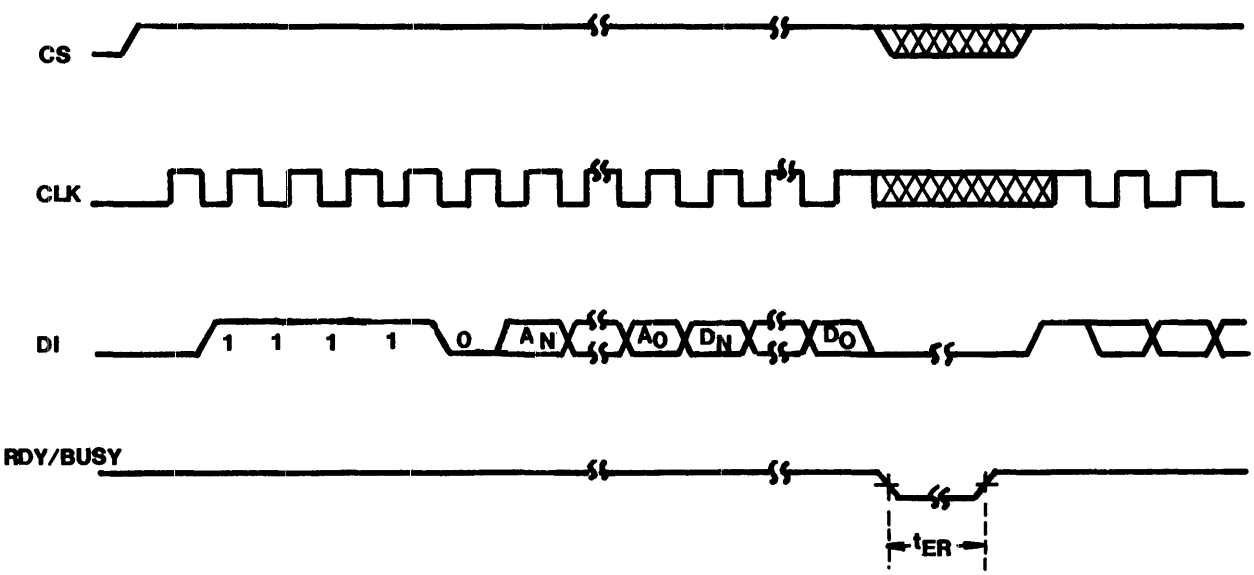
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4 ERASE Mode



Organization	A_N
256 x 8	A_7
128 x 16	A_6

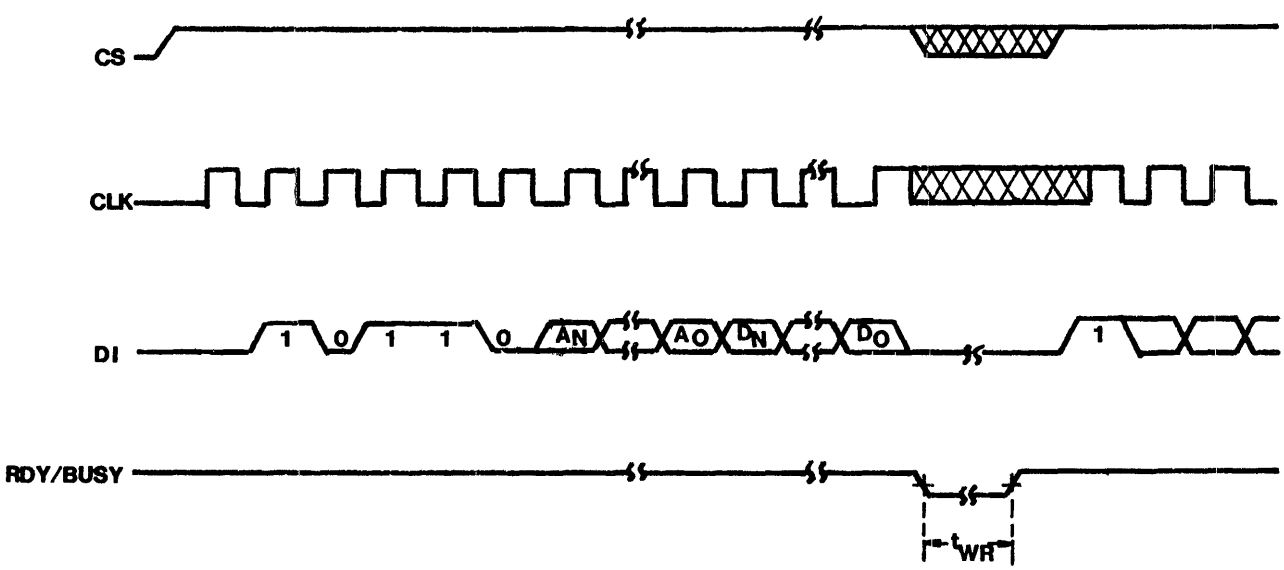
Erase Mode

The erase instruction is followed by seven or eight bits of address indicating the address to be erased (set to all 1's).

After the last address bit (A_0) has been entered the contents of the specified address will be erased.

During the erase sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the erase cycle as indicated by t_{ER}. The erase cycle is self-timed on the chip.

Figure 5 WRITE Mode



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

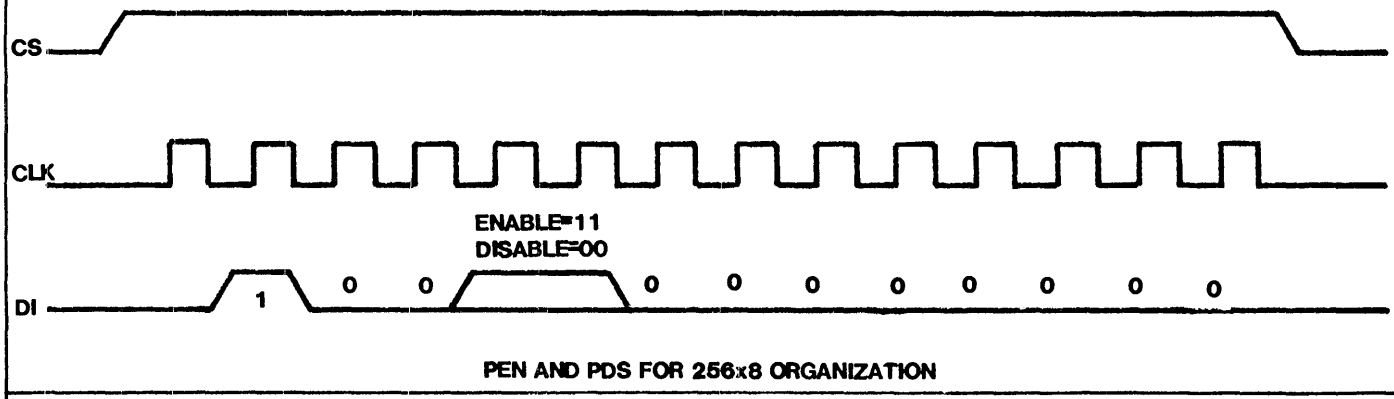
Write Mode

The write instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

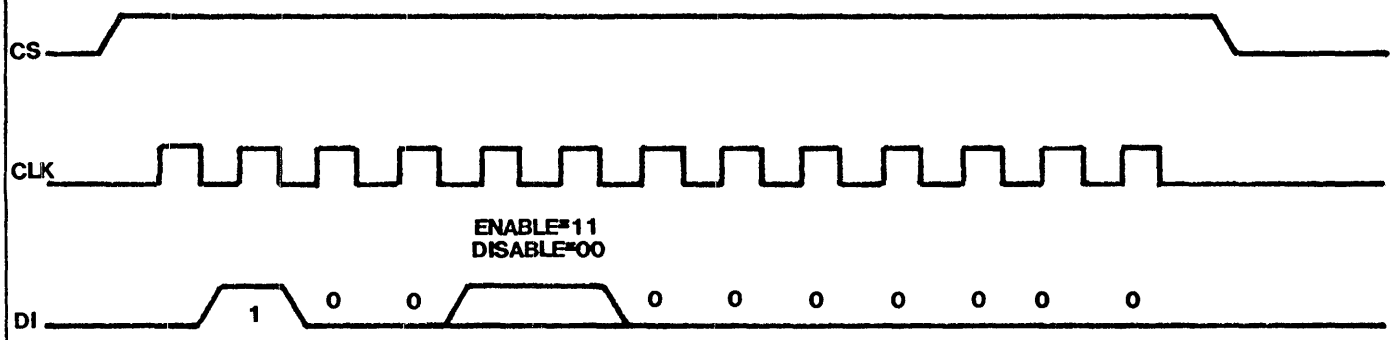
After the last data bit (D_0) has been shifted into the data register the new data will be written to the specified address. (Note that a write instruction must be preceeded by an erase instruction for programming since a write will only modify erased bits at that address.

During the write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the write cycle as indicated by t_{WR}. The write cycle is self-timed on the chip.

Figure 6 PEN (Program Enable and PDS (Program Disable)



PEN AND PDS FOR 256x8 ORGANIZATION



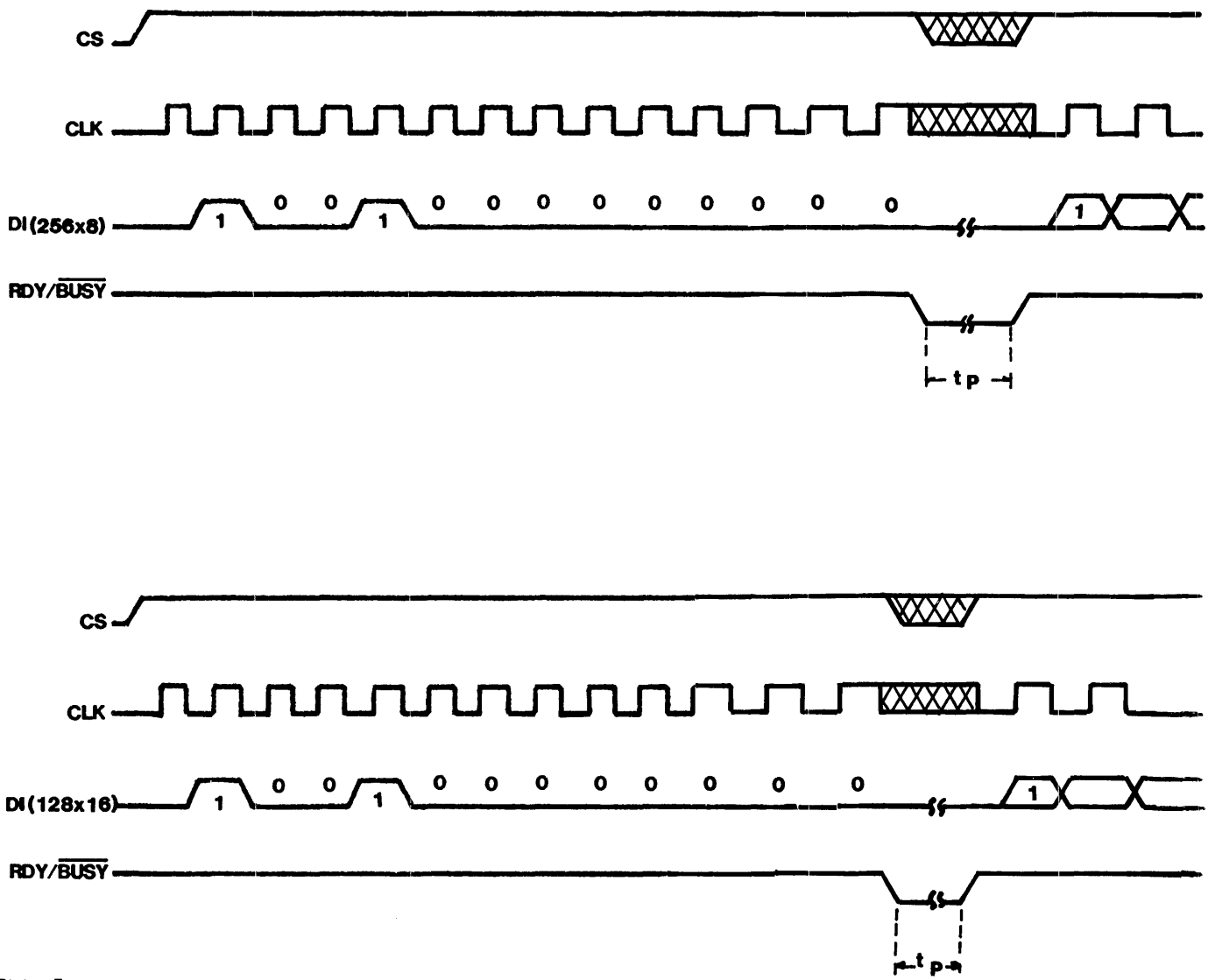
PEN AND PDS FOR 128 x 16 ORGANIZATION

Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Note that the ER5912I will power up with programming disabled.

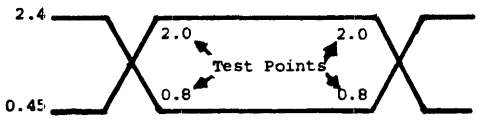
Figure 7 ERAL (Erase All) Mode



Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a 1.

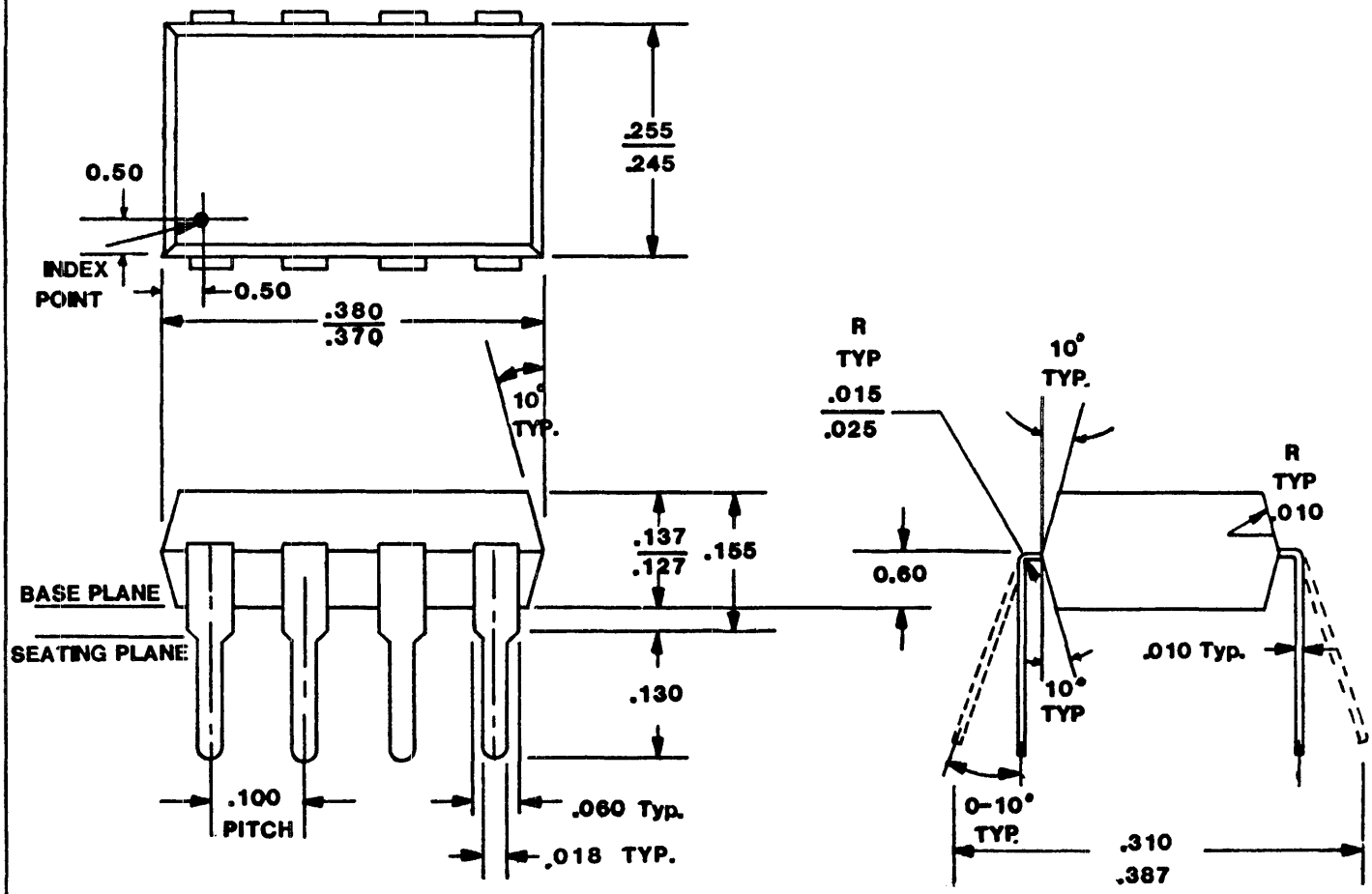
A.C. TESTING, INPUT AND OUTPUT WAVEFORMS



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

2048 SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

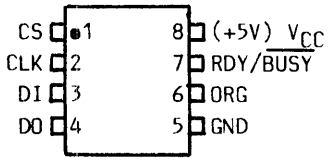
FEATURES

- Low cost
- User-selectable organization: 128 x 16 or 256 x 8
- Single +5V only operation
- Binary addressing
- Fully automatic self-timed erase/write mode
- Self timed separate erase and write modes
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- -40°C to +85°C operating ambient temperature range
- Power-on/off data protection circuitry

PIN CONFIGURATION

8 Pin Dual-In-Line

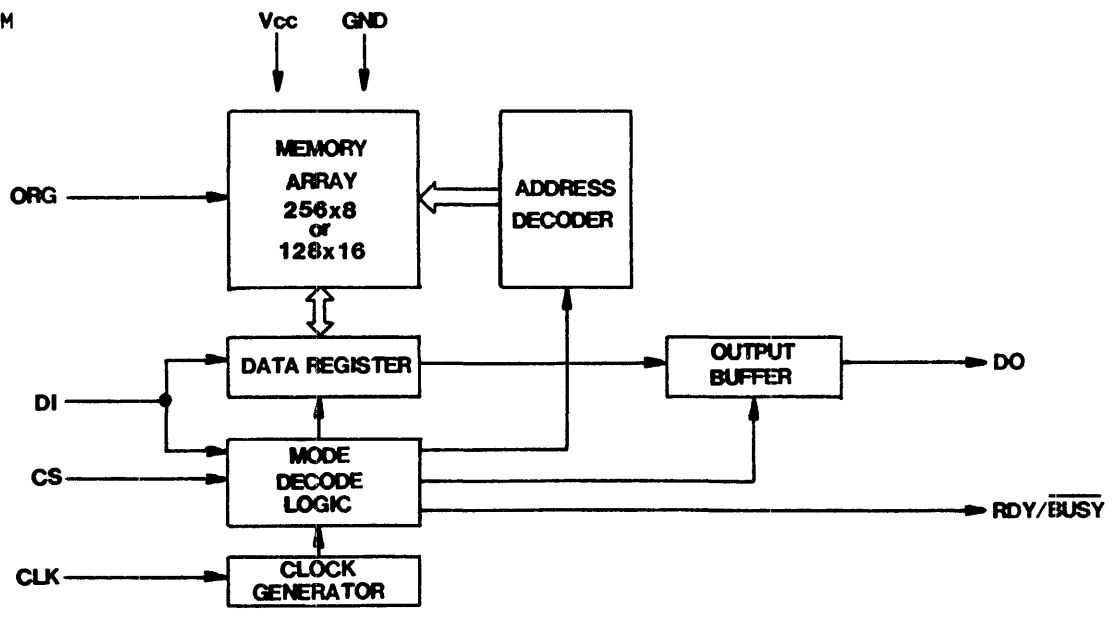
TOP VIEW



DESCRIPTION

The ER5912I is a low cost, serial EEPROM manufactured in General Instrument's highly reliable SNOS technology. This device features +5V only operation, a self-timed reprogramming cycle as well as separate erase and write cycles and two user-selectable memory array organizations, 128 x 16 or 256 x 8, which are externally selectable by means of a one bit code applied to control pin ORG. The Data Input (DI) and Data Output (DO) pins are controlled by separate serial formats. When separate lines are used the DO output pin is valid only in the read mode and is in the high impedance state in all other modes, thus eliminating bus contention. Seven instructions may be executed and the instruction length will be thirteen bits when using the 256 x 8 organization and twelve bits when the 128 x 16 organization is used. The instruction format has a logical 1 as a start bit, four bits as an opcode and either seven or eight address bits.

BLOCK DIAGRAM



DS20028A-1

		PIN FUNCTIONS	
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5V the 128 x 16 organization is selected. When it is connected to ground the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5V Power Supply		
RDY/BUSY	Status Output		
GND	Ground		

INSTRUCTION SET

Instruction	Start Bit	opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0 0 0	A_7-A_0	A_6-A_0			Read Address A_N-A_0
PROGRAM	1	X 1 0 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
ERASE	1	1 1 1 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Erase Address A_N-A_0
WRITE	1	0 1 1 0	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Write Address A_N-A_0
PEN	1	0 0 1 1	00000000	0000000			Program Enable
PDS	1	0 0 0 0	00000000	0000000			Program Disable
ERAL	1	0 0 1 0	00000000	0000000			Erase All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and
without data retention)..... -65°C to +150°C
Soldering temperature of leads
(10 seconds)..... +300°C

Standard Conditions (Unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V +10% volts
Operating Temperature Range (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400uA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{LI}	-	-	+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	+10	µA	V_{OUT} = GND to V_{CC}
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	-	13	mA	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	I_{CC}	-	-	15	mA	V_{CC} = 5.5V
Chip Deselected (STANDBY)	I_{CC}	-	-	5	mA	V_{CC} = 5.5V
Power Consumption						
Chip Selected	P_{CC}	-	-	72	mW	V_{CC} = 5.5V
Chip Selected (PROGRAM and ERAL modes)	P_{CC}	-	-	83	mW	V_{CC} = 5.5V
Chip Deselected (STANDBY)	P_{CC}	-	-	28	mW	V_{CC} = 5.5V

AC CHARACTERISTICS (See Figure 1)

Characteristic	Sym	Min	Typ	Max	Units	Conditions
CLK Frequency	f_{CLK}	0	-	500	KHz	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
CLK Pulse Width	t_{CPW}	1.0	-	-	µs	
Data Output Delay	t_{PD1}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Data Output Delay	t_{PDO}	-	-	2.0	µs	C_L = 100pf V_{OL} = 0.8V V_{OH} = 2.0V
Status Low Time						
programming time	t_{PR}	20	30	40	ms	
erase time	t_{ER}	10	-	20	ms	
write time	t_{PR}	10	-	20	ms	

Figure 1 Synchronous Data Timing

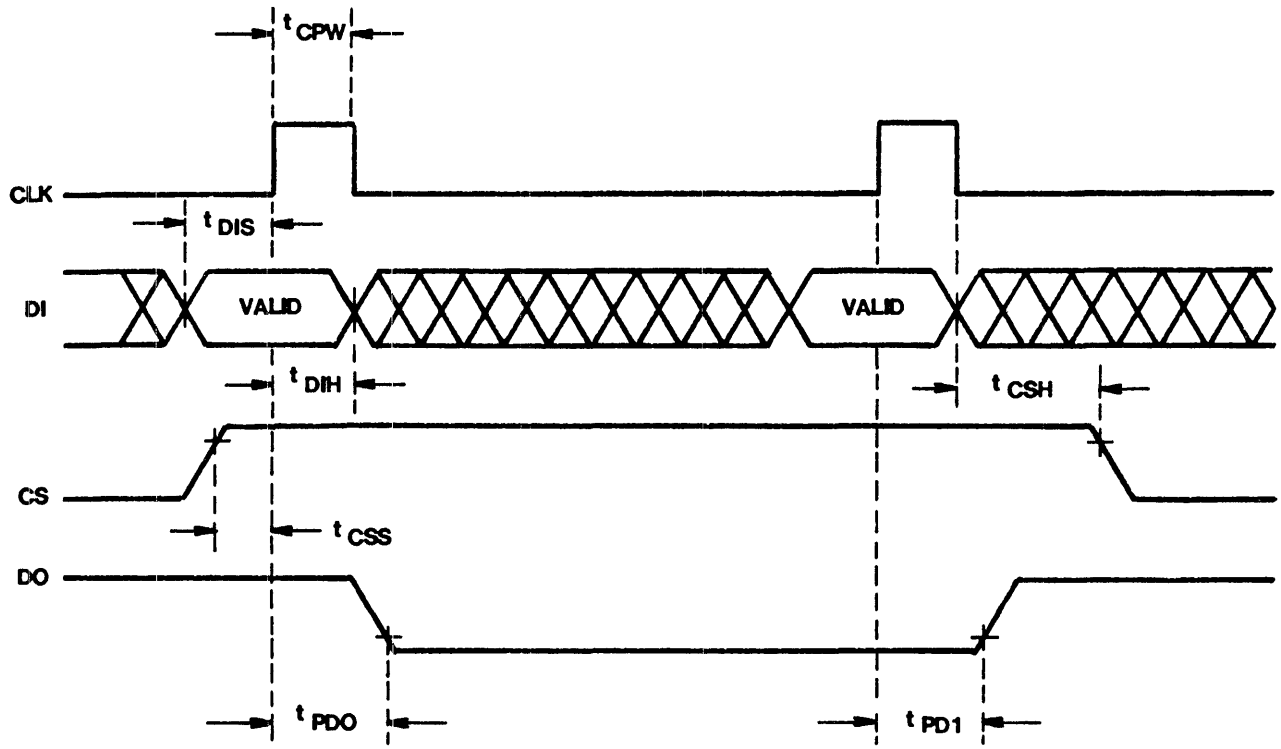
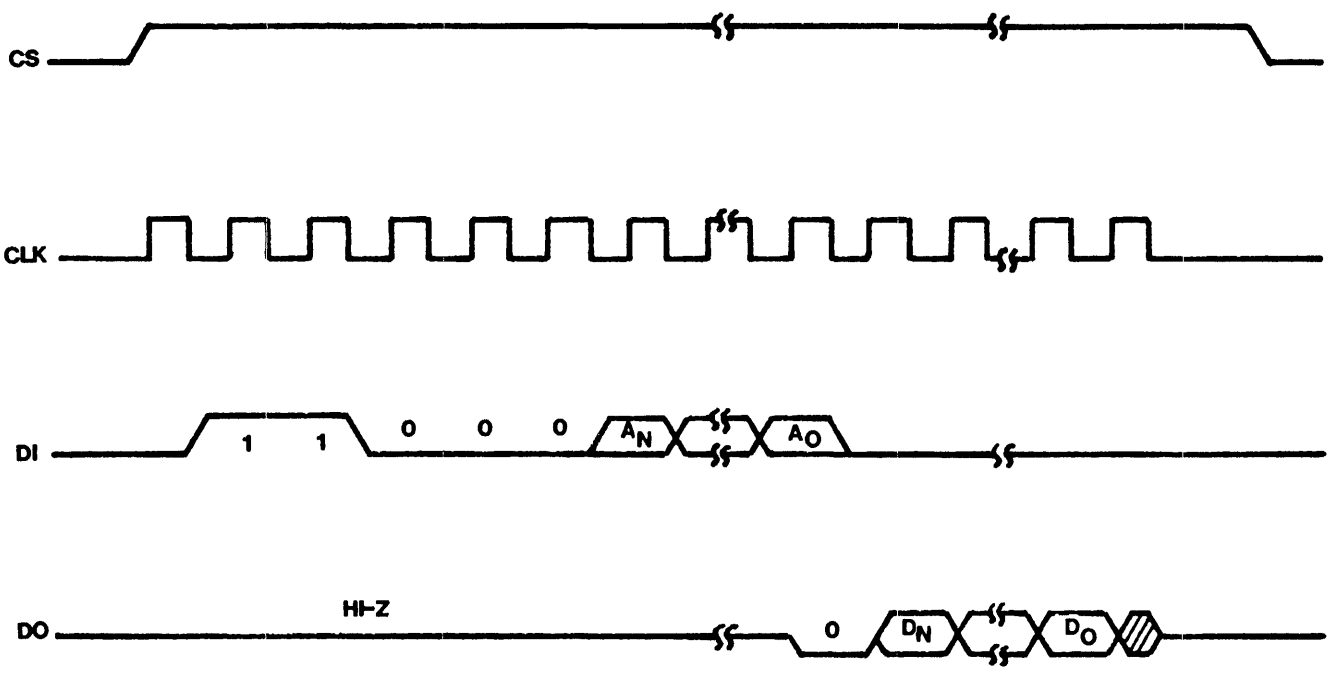


Figure 2 READ Mode

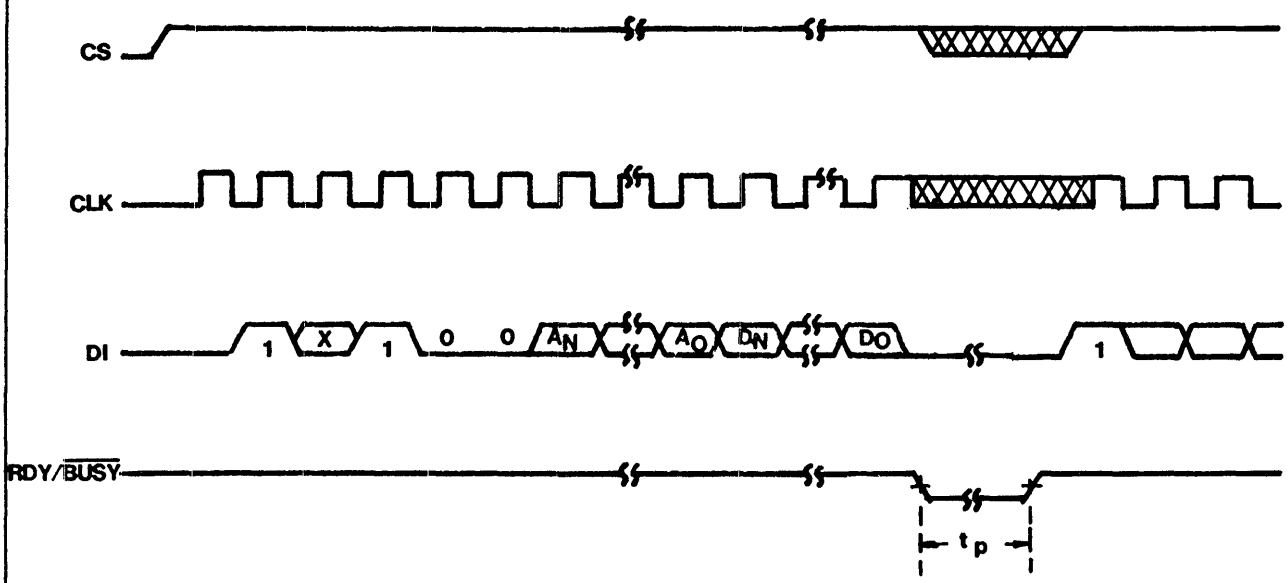


Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string.

Figure 3 PROGRAM Mode



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

Program Mode

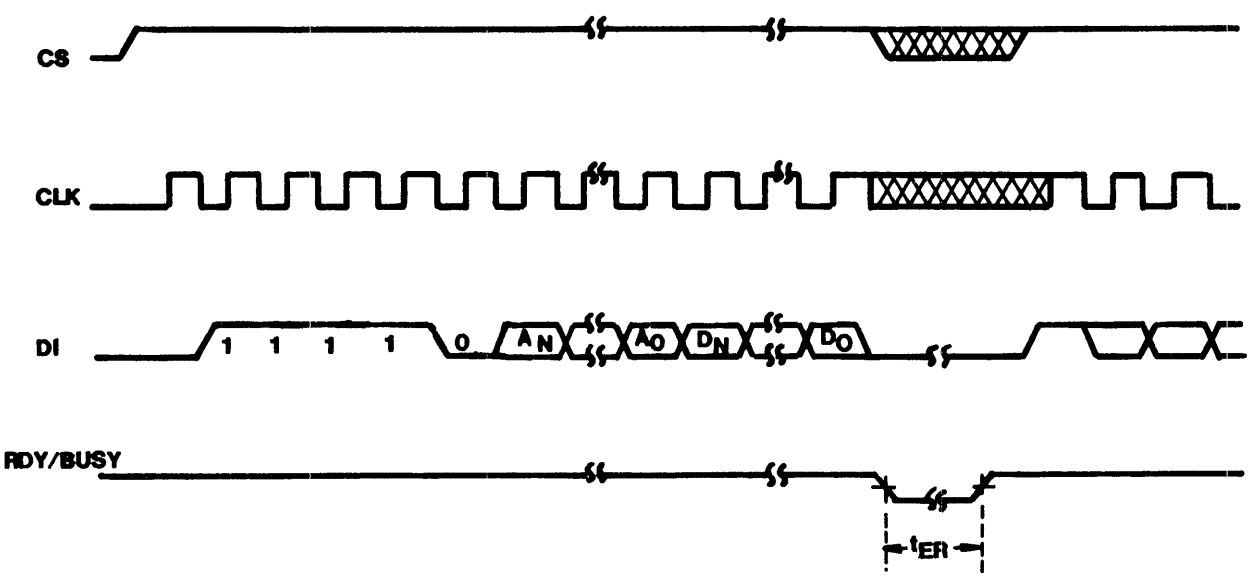
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4 ERASE Mode



Organization	A_N
256 x 8	A_7
128 x 16	A_6

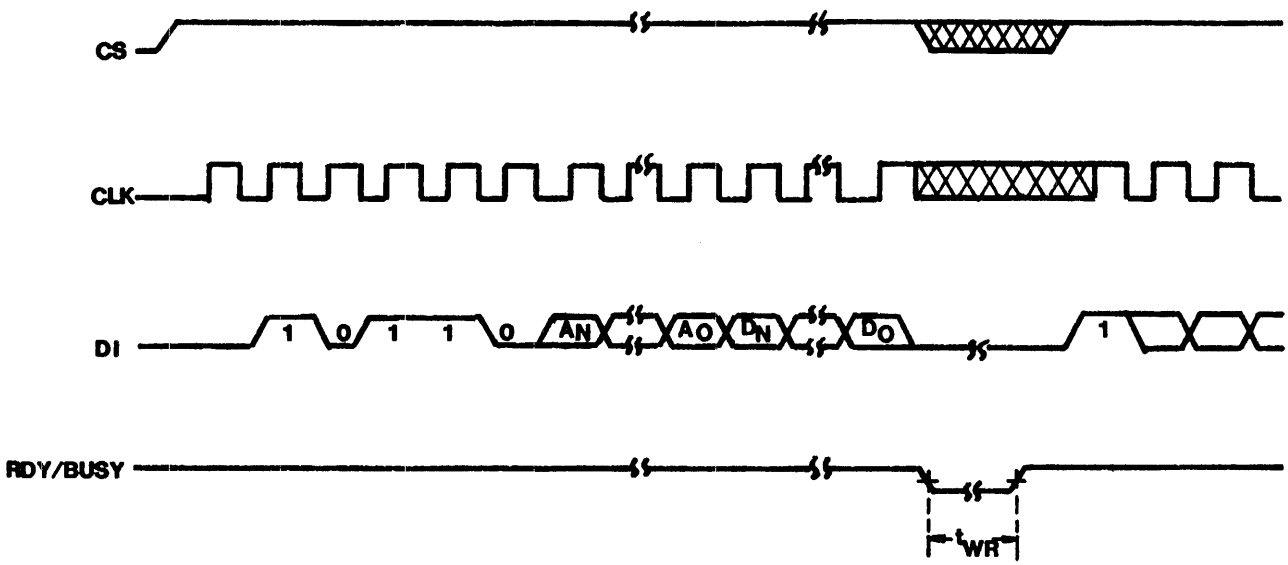
Erase Mode

The erase instruction is followed by seven or eight bits of address indicating the address to be erased (set to all 1's).

After the last address bit (A_0) has been entered the contents of the specified address will be erased.

During the erase sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the erase cycle as indicated by t_{ER}. The erase cycle is self-timed on the chip.

Figure 5 WRITE Mode



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

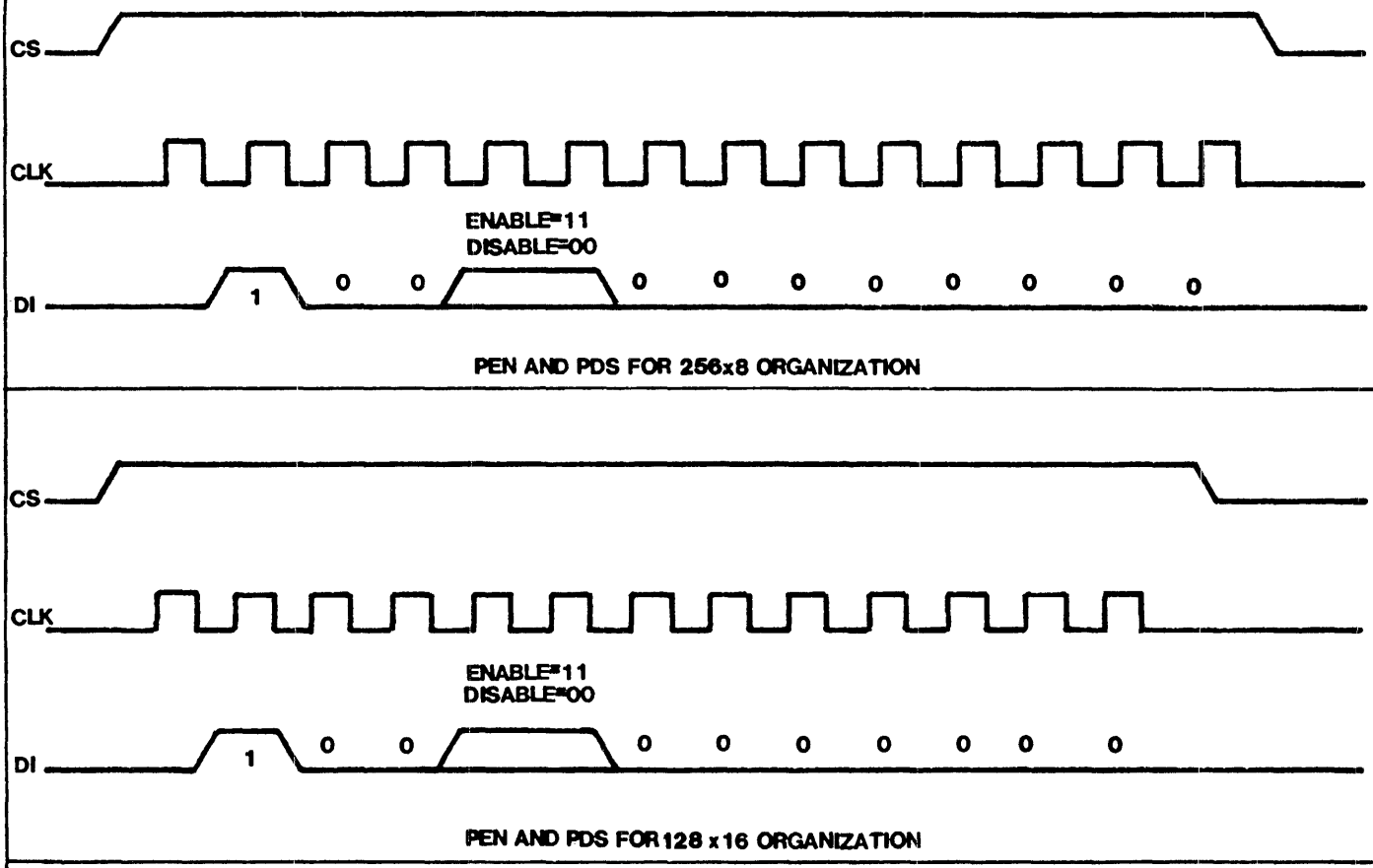
Write Mode

The write instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (D_0) has been shifted into the data register the new data will be written to the specified address. (Note that a write instruction must be preceeded by an erase instruction for programming since a write will only modify erased bits at that address.

During the write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the write cycle as indicated by t_{WR}. The write cycle is self-timed on the chip.

Figure 6 PEN (Program Enable and PDS (Program Disable)

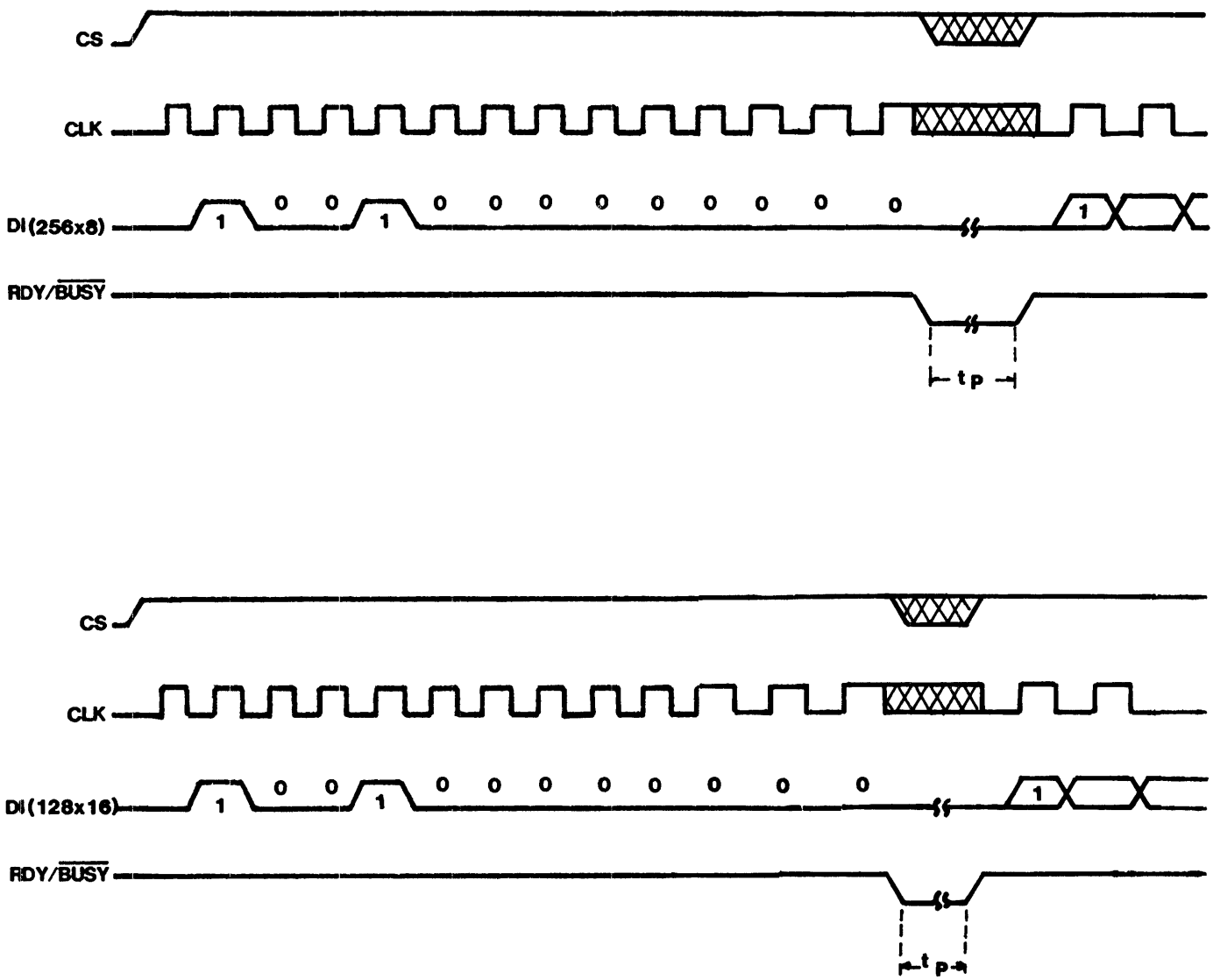


Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Note that the ER5912I will power up with programming disabled.

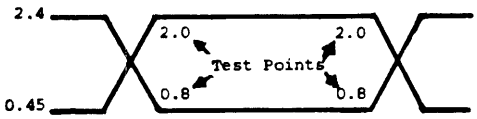
Figure 7 ERAL (Erase All) Mode



Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a 1.

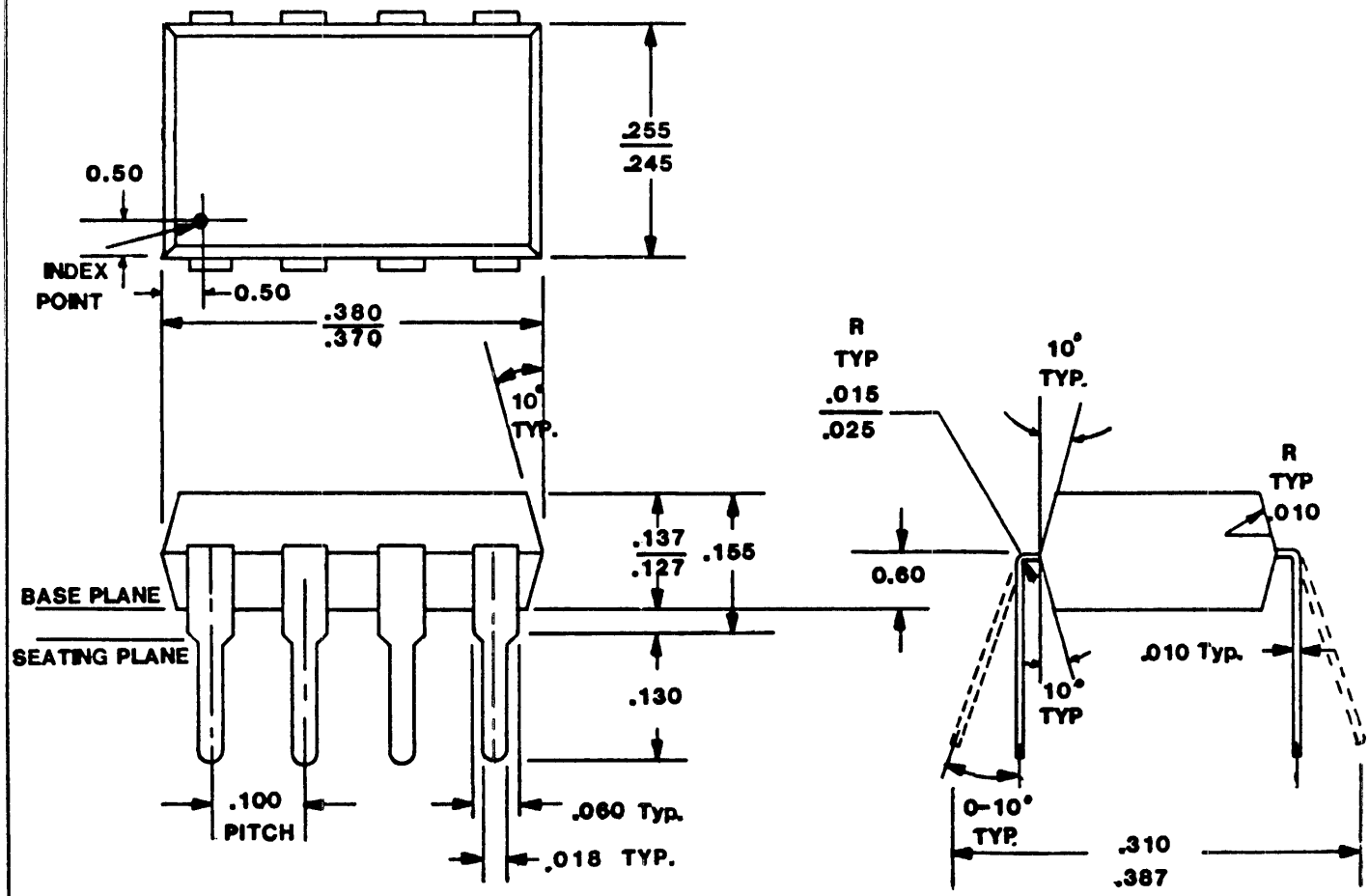
A.C. TESTING, INPUT AND OUTPUT WAVEFORMS



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

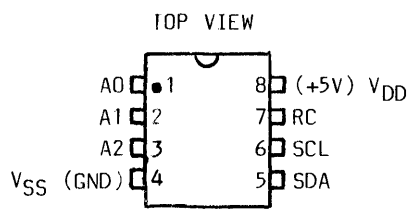
1024 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 128 x 8 serial EEPROM
- Single +5V only operation
- Compatible with the inter-integrated-circuit (I^2C) bus
- Fully TTL compatible inputs and outputs
- Unlimited read accesses
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range

PIN CONFIGURATION

8 LEAD DUAL IN LINE

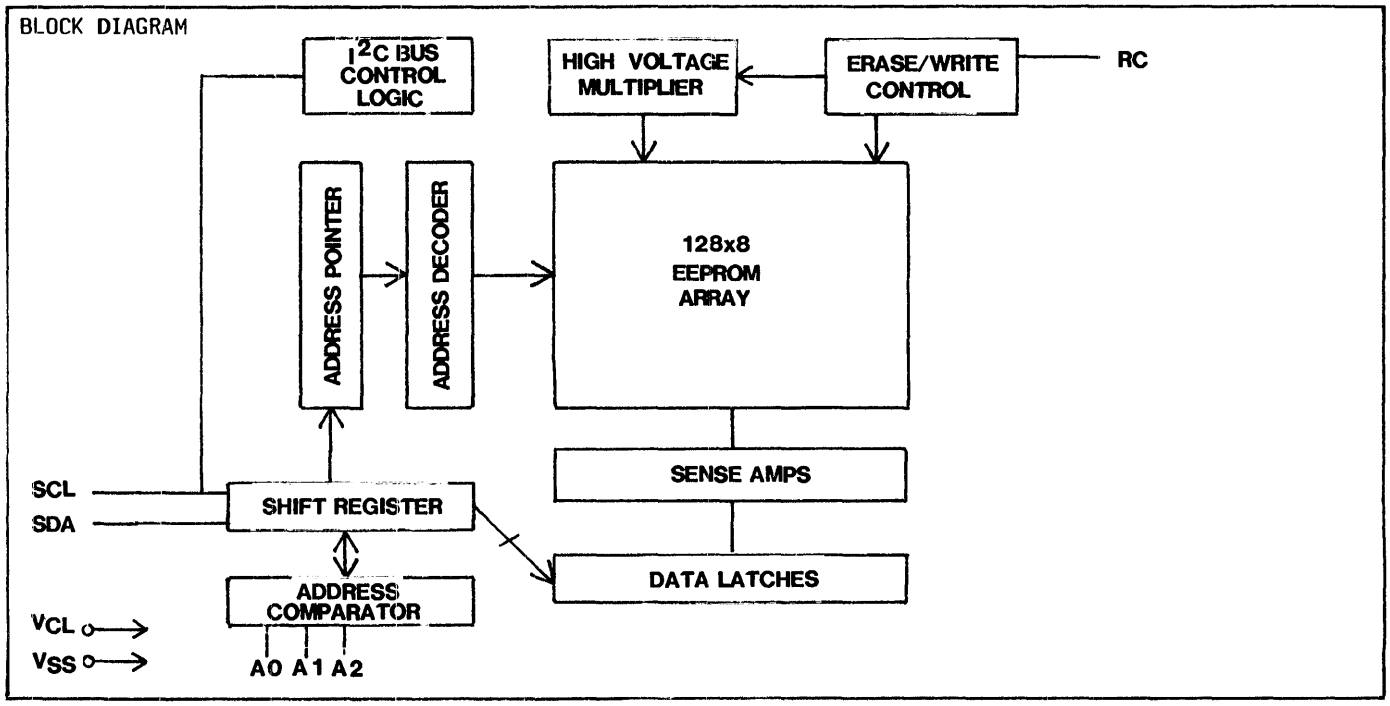


DESCRIPTION

The PCD8572 is a 1K EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I^2C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I^2C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400 pf maximum bus capacitance).

Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8572s may be connected to the I^2C bus.

BLOCK DIAGRAM



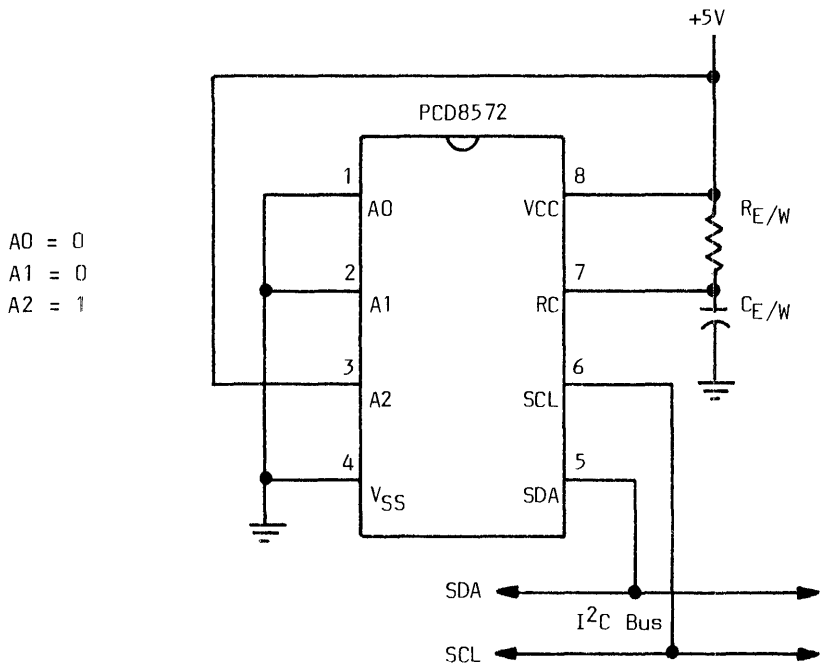
PIN FUNCTIONS

A0, A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input, Erase/Write
RC	Time Constant Network Input
V_{DD}	+5V Power Supply

Figure 1 below shows the typical manner in which the PCD8572 is interfaced to the I^2C bus. For purposes of illustration chip address A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8572s can be connected to the I^2C bus of a single system. The erase/write cycle time of this device $t_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:
When the PCD8572 is not used in an I^2C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 TYPICAL INTERFACE



DS20016D-2

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each reciever acknowledges with a nineth bit which must be provided by the user.

Within the I^2C bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The PCD8572 works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clockpulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (GND)
V_{DD} = +5 ± 10% volts
Ambient Operating Temperature (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

*ABSOLUTE MAXIMUM RATINGS

Characteristic	Sym	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	-0.3	-	7.0	V
Voltage On Any Input Pin	V_I	V_{SS}-0.8	-	V_{DD}+0.8	V
Ambient Operating Temperature	T_A	0	-	+70	°C
Storage Temperature (Unpowered and without data retention)	T_{STG}	-65	-	+150	°C
Current Into Any Input Pin	I_I	-	-	100	µA
Output Current	I_O	-	-	3	mA (SINK)
Soldering Temperature of Leads (10 seconds)	-	-	-	300	°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	I_{DDR}	-	15	-	mA	
Operating Supply Current WRITE/ERASE Mode	I_{DDW}	-	15	-	mA	
Operating Supply Current STANDBY Mode	I_{DDO}	-	12	-	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	I_{IL}	-	-	1	µA	
Output Leakage Current HIGH	I_{OH}	-	-	1	µA	
SCL Input and SDA Input/ Output Pins:						
High Level Input Voltage	V_{IH}	3.0	-	V_{DD}+0.8	V	
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V	
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3mA V_{DD} = 4.5V
A0, A1, A2 Pins:						
High Level Input Voltage	V_{IH}	V_{DD}-0.5	-	V_{DD}+0.5	V	
Low Level Input Voltage	V_{IL}	-0.3	-	0.5	V	

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	-	100	KHz	
The LOW period of the clock	t_{LOW}	4.7	-	-	µs	
The HIGH period of the clock	t_{HIGH}	4.0	-	-	µs	
SDA and SCL rise time	t_R	-	-	1	µs	
SDA and SCL fall time	t_F	-	-	300	ns	
START condition hold time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	µs	
Setup time for start condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	-	-	µs	
Data set-up time	$t_{SU;DAT}$	250	-	-	ns	
Data hold time for I^2C devices	$t_{HD;DAT}$	0	-	-	µs	See note 2
STOP condition set-up time	$t_{SU;STO}$	4.7	-	-	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	-	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/ write cycles)	$N_{E/W}$	-	-	10,000	E/W cycles	Per byte
Data Retention Time	t_S	10	-	-	Years	
Input Capacitance on SCL, SDA	C_I	-	-	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES:
1. All values referred to V_{IH} and V_{IL} levels.
2. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FIGURE 2A DATA TRANSFER SEQUENCE ON THE SERIAL BUS

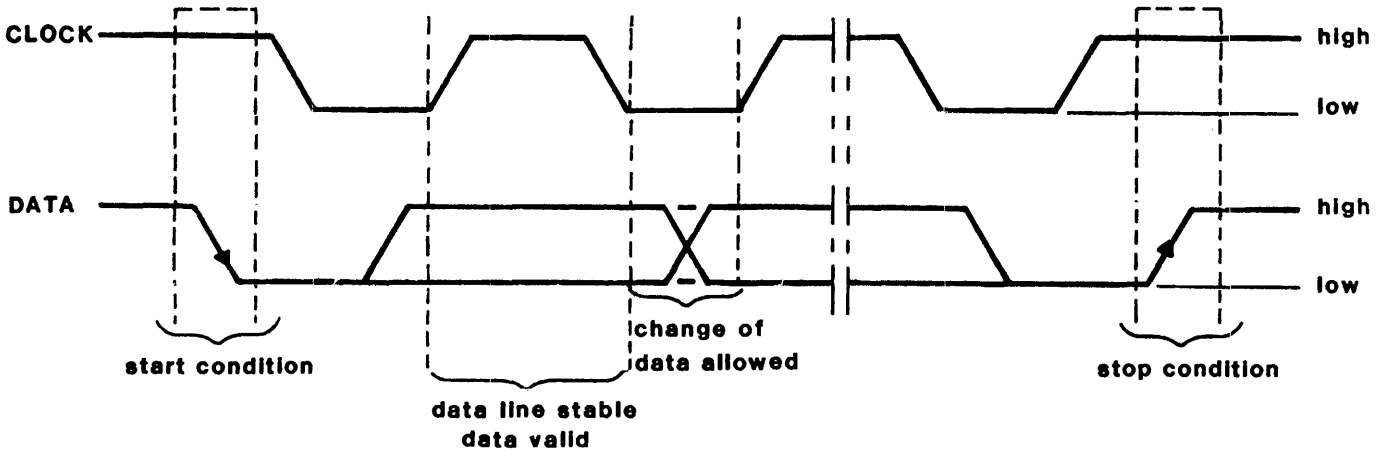
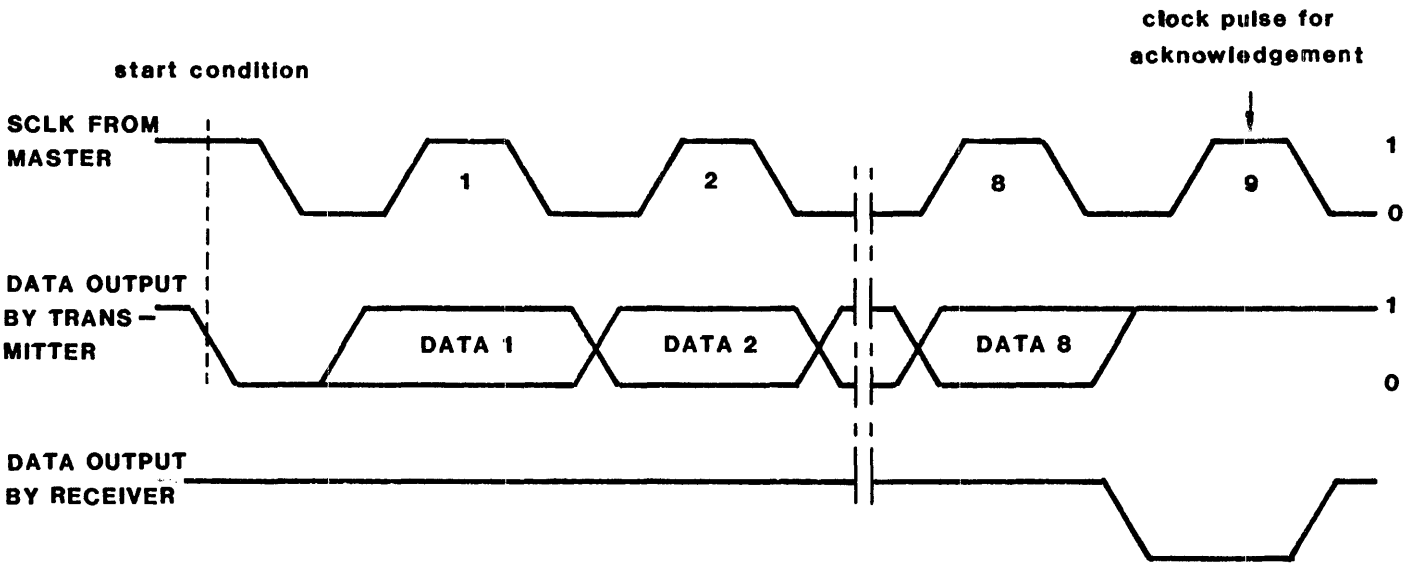


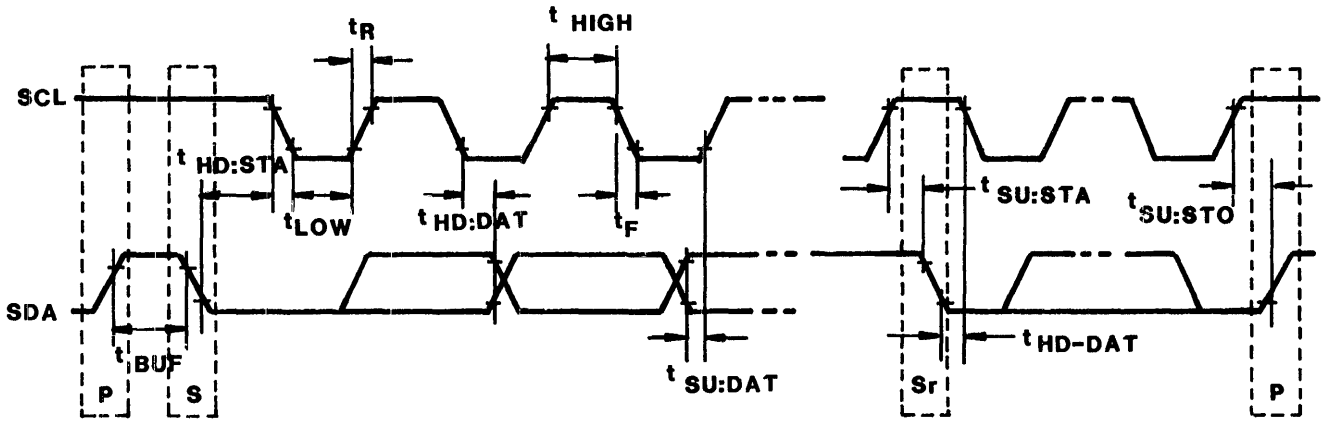
FIGURE 2B ACKNOWLEDGEMENT



ACKNOWLEDGEMENT

An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C I^2C BUS TIMING REQUIREMENTS

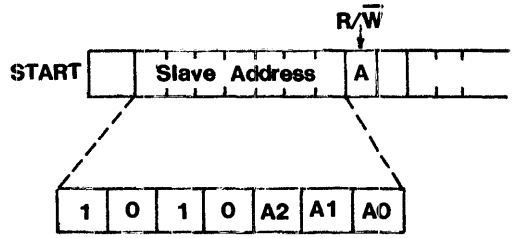


I^2C BUS PROTOCOL

A thorough description of the inter-IC bus specifications appears in the Philips document number IVE 81107 which is available upon request from General Instrument. The following is a condensed description of each mode of operation.

Chip Address (Slave Address) Allocation: The three chip address inputs of each PCD8572 (A2, A1, A0) must be externally connected to either +5V (V_{DD}) of ground (V_{SS}) thereby assigning to each PCD8572 a unique three-bit chip address. Up to eight PCD8572s may be connected to the I^2C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected PCD8572. The correct bus protocol is shown in figure 3.

FIGURE 3 SLAVE ADDRESS ALLOCATION



Erase/Write Mode: In this mode the master transmitter transmits to the PCD8572 slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address a logic 0 ($R/\overline{W}=0$) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8572. The PCD8572 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms. if two bytes are written.

Read Mode: In this mode the master reads the PCD8572 slave after setting the slave address. See figure 5. Following the write mode control bit ($R/\overline{W}=0$) and the acknowledge bit, the word address An is written to the on-chip address pointer.

Next the START condition and slave address are repeated followed by the READ mode control bit ($R/\overline{W}=1$). At this point the master transmitter becomes the master receiver and the PCD8572 slave receiver becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8572 slave transmitter will now place the data byte at address A_{n+1} on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8572 slave without first writing to the (voltaile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIGURE 4 ERASE + REWRITE MODE

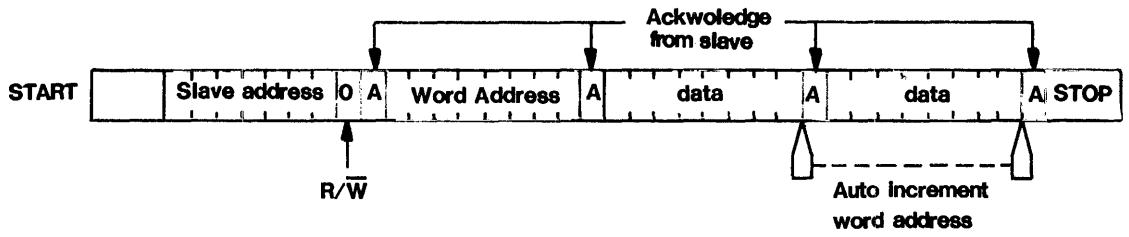


FIGURE 5 READ MODE

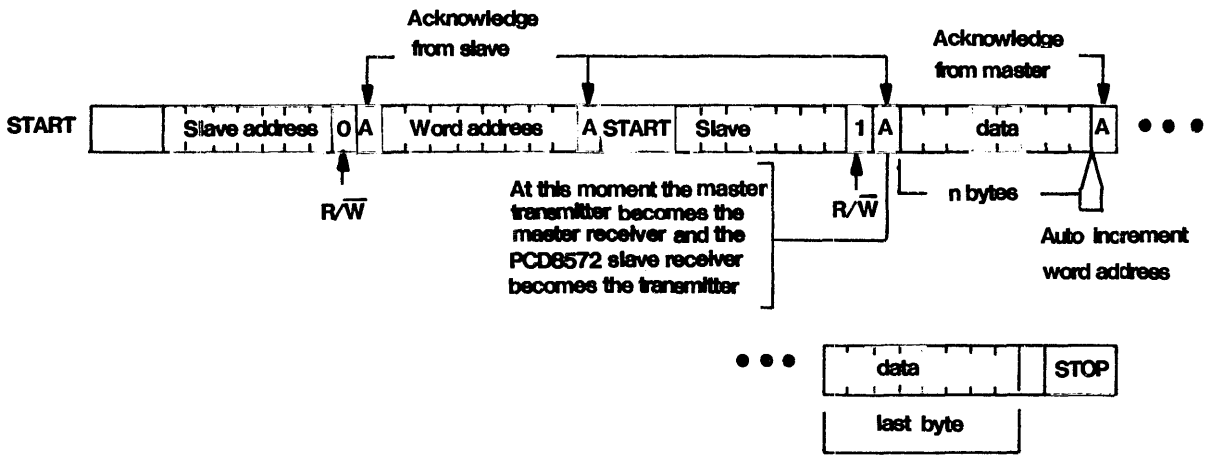
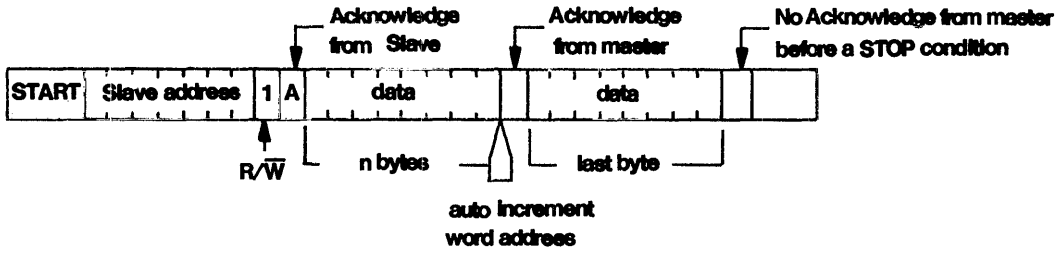
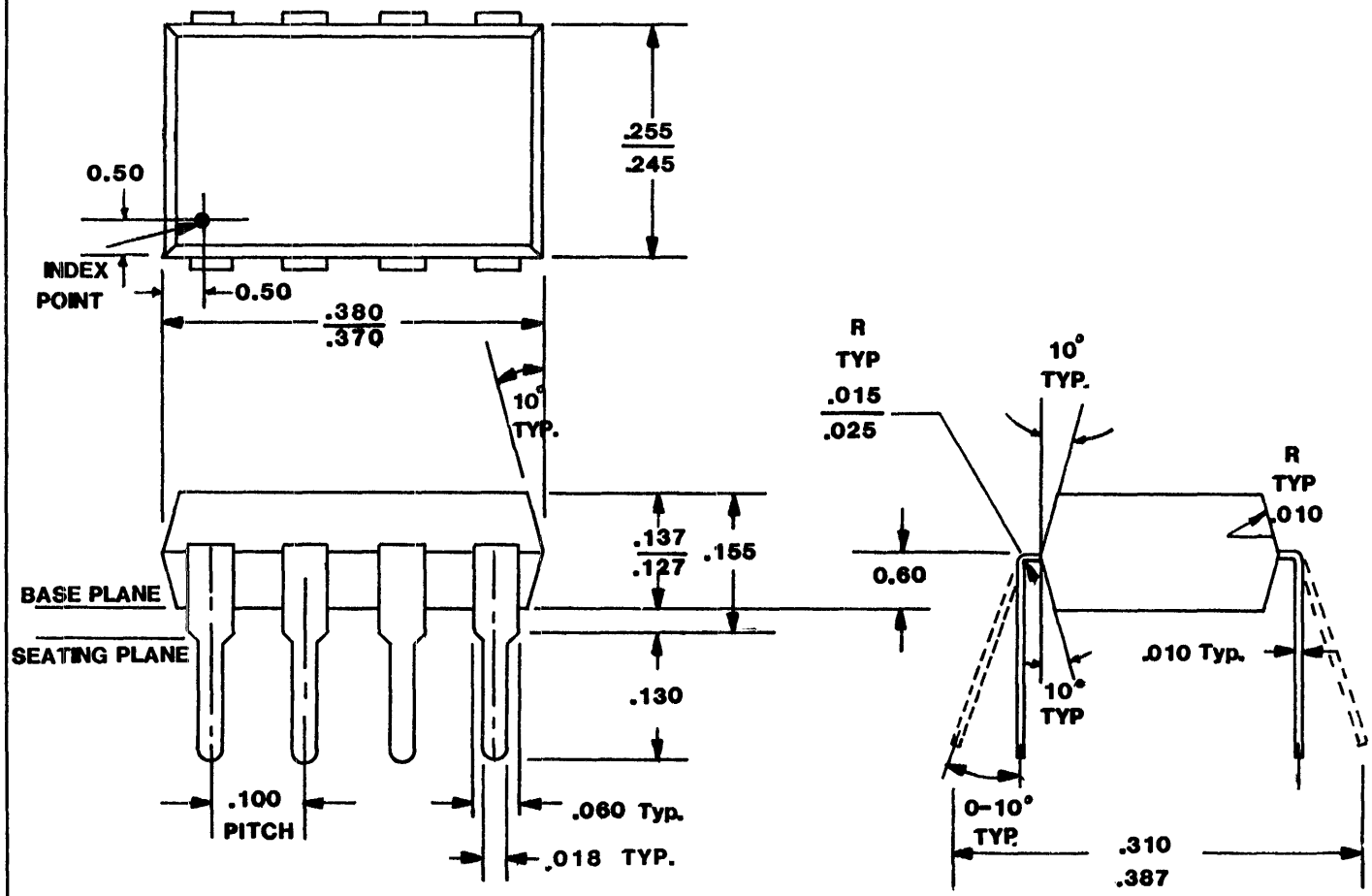


FIGURE 6 ALTERNATE READ MODE



PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

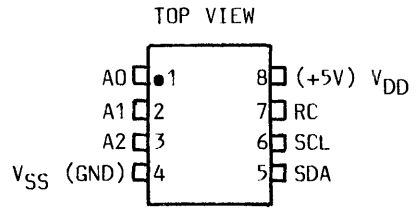
GENERAL INSTRUMENT	PCD8572I

1024 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 128 x 8 serial EEPROM
- Single +5V only operation
- Compatible with the inter-integrated-circuit (I^2C) bus
- Fully TTL compatible inputs and outputs
- Unlimited read accesses
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- -40°C to +85°C operating ambient temperature range

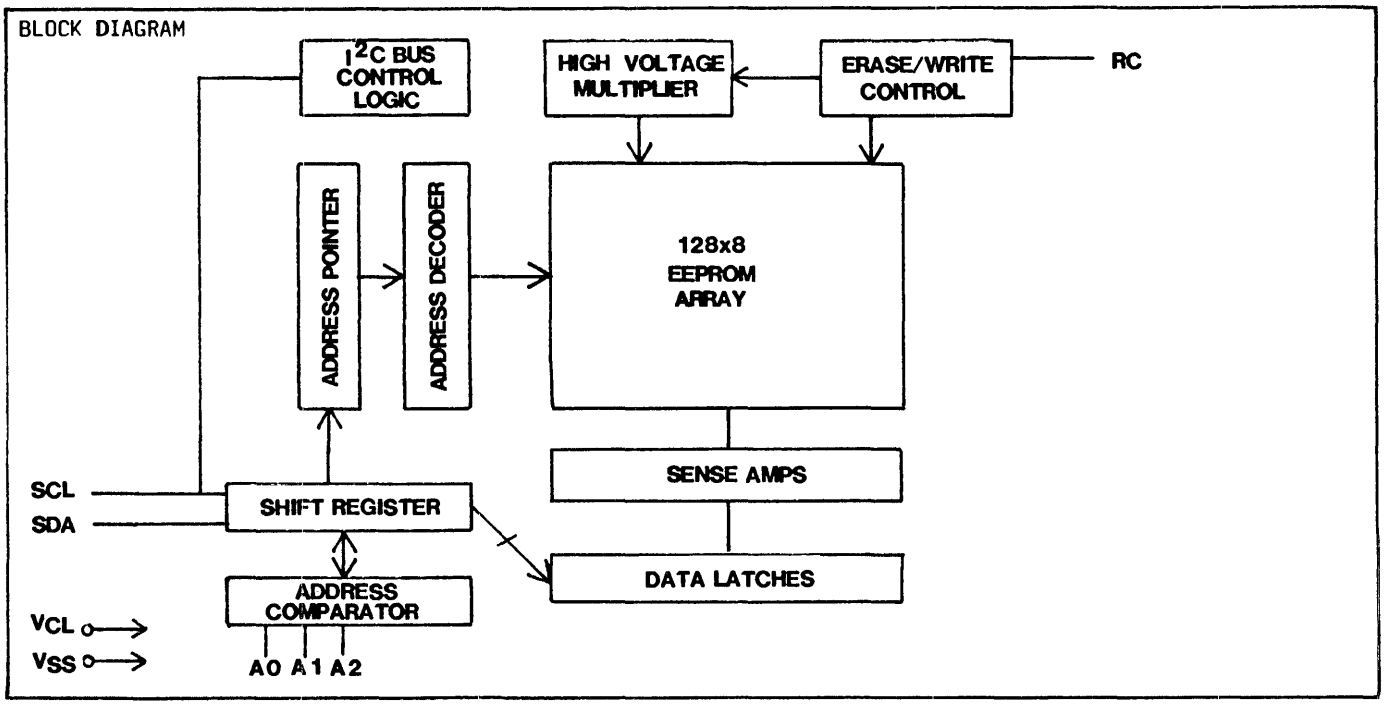
PIN CONFIGURATION
8 LEAD DUAL IN LINE



DESCRIPTION

The PCD8572I is a 1K EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I^2C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I^2C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400 pf maximum bus capacitance).

Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8572Is may be connected to the I^2C bus.



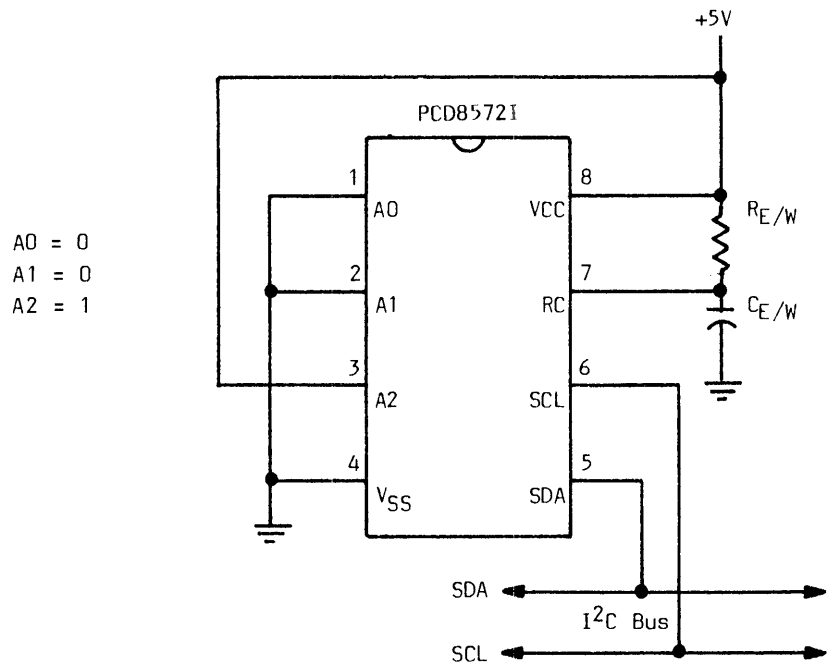
PIN FUNCTIONS

A0, A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input, Erase/Write
RC	Time Constant Network Input
V_{DD}	+5V Power Supply

Figure 1 below shows the typical manner in which the PCD8572I is interfaced to the I^2C bus. For purposes of illustration chip address A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8572Is can be connected to the I^2C bus of a single system. The erase/write cycle time of this device $T_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:
When the PCD8572I is not used in an I^2C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 TYPICAL INTERFACE



CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each reciever acknowledges with a nineth bit which must be provided by the user.

Within the I^2C bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The PCD8572I works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clockpulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (GND)
V_{DD} = +5 + 10% volts
Ambient Operating Temperature (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

*ABSOLUTE MAXIMUM RATINGS

Characteristic	Sym	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	-0.3	-	7.0	V
Voltage On Any Input Pin	V_I	V_{SS}-0.8	-	V_{DD}+0.8	V
Ambient Operating Temperature	T_A	0	-	+70	°C
Storage Temperature (Unpowered and without data retention)	T_{STG}	-65	-	+150	°C
Current Into Any Input Pin	I_I	-	-	100	µA
Output Curent	I_O	-	-	3	mA (SINK)
Soldering Temperature of Leads (10 seconds)	-	-	-	300	°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	I_{DDR}	-	15	-	mA	
Operating Supply Current WRITE/ERASE Mode	I_{DDW}	-	15	-	mA	
Operating Supply Current STANDBY Mode	I_{DDO}	-	12	-	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	I_{IL}	-	-	1	µA	
Output Leakage Current HIGH	I_{OH}	-	-	1	µA	
SCL Input and SDA Input/ Output Pins:						
High Level Input Voltage	V_{IH}	3.0	-	V_{DD}+0.8	V	
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V	
Low Level Output Voltage	V_{OH}	-	-	0.4	V	I_{OL} = 3mA V_{DD} = 4.5V
A0, A1, A2 Pins:						
High Level Input Voltage	V_{IH}	V_{DD}-0.5	-	V_{DD}+0.5	V	
Low Level Input Voltage	V_{IL}	-0.3	-	0.5	V	

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	-	100	KHz	
The LOW period of the clock	t_{LOW}	4.7	-	-	µs	
The HIGH period of the clock	t_{HIGH}	4.0	-	-	µs	
SDA and SCL rise time	t_R	-	-	1	µs	
SDA and SCL fall time	t_F	-	-	300	ns	
START condition hold time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	µs	
Setup time for start condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	-	-	µs	
Data set-up time	$t_{SU;DAT}$	250	-	-	ns	
Data hold time for I^2C devices	$t_{HD;DAT}$	0	-	-	µs	See note 2
STOP condition set-up time	$t_{SU;STO}$	4.7	-	-	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	-	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/ write cycles)	$N_{E/W}$	-	-	10,000	E/W cycles	Per byte
Data Retention Time	t_S	10	-	-	Years	
Input Capacitance on SCL, SDA	C_I	-	-	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES:
1. All values referred to V_{IH} and V_{IL} levels.
2. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FIGURE 2A DATA TRANSFER SEQUENCE ON THE SERIAL BUS

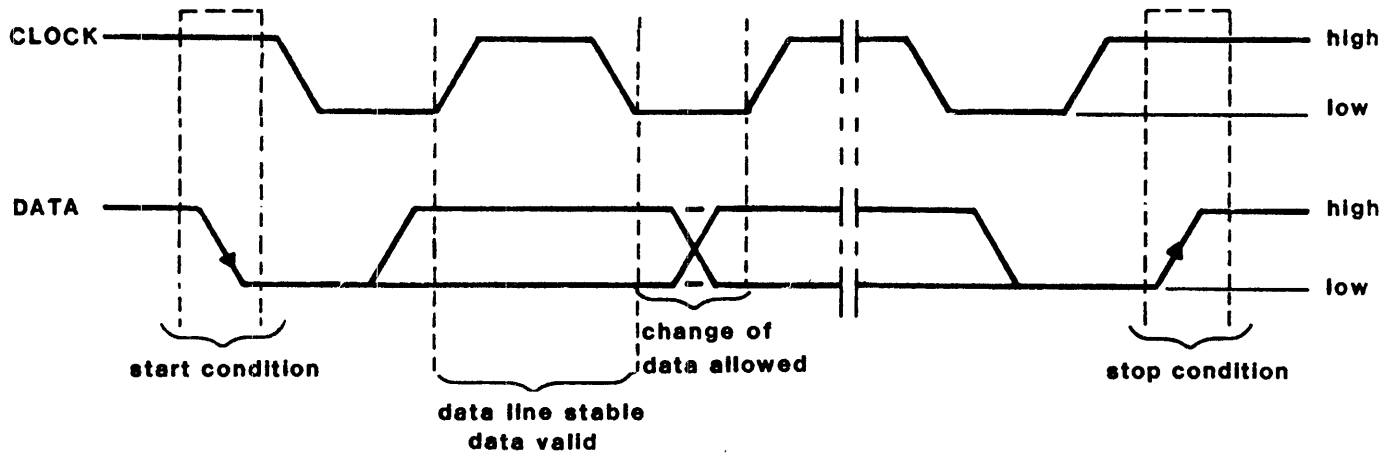
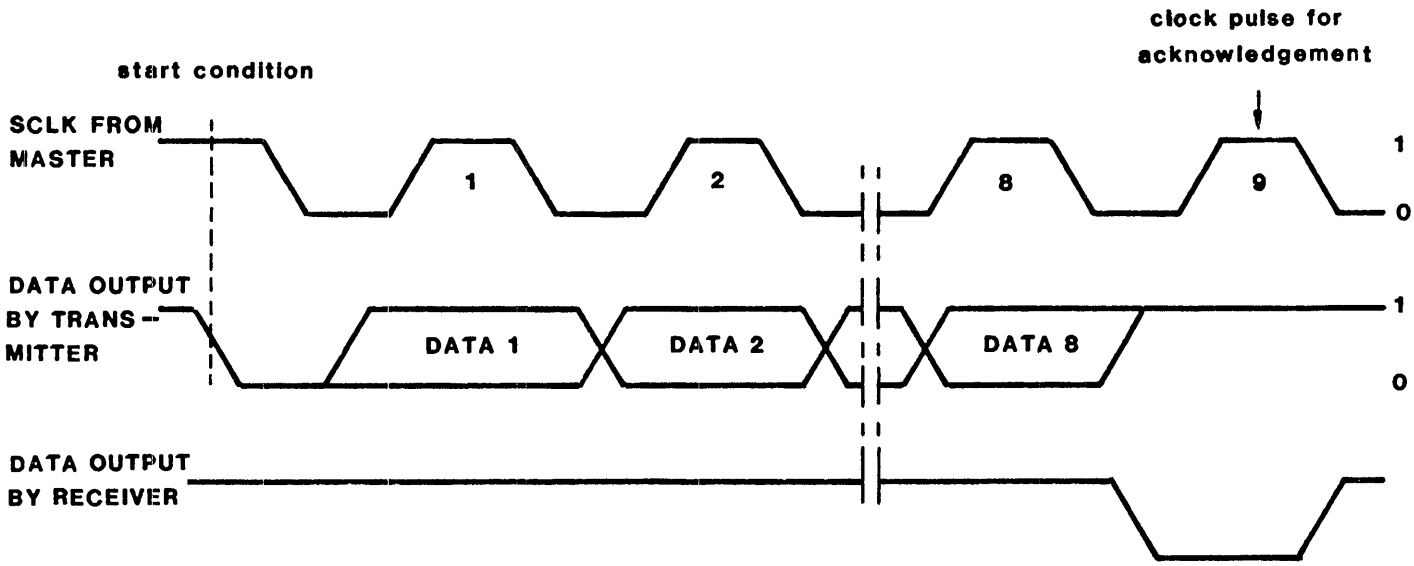


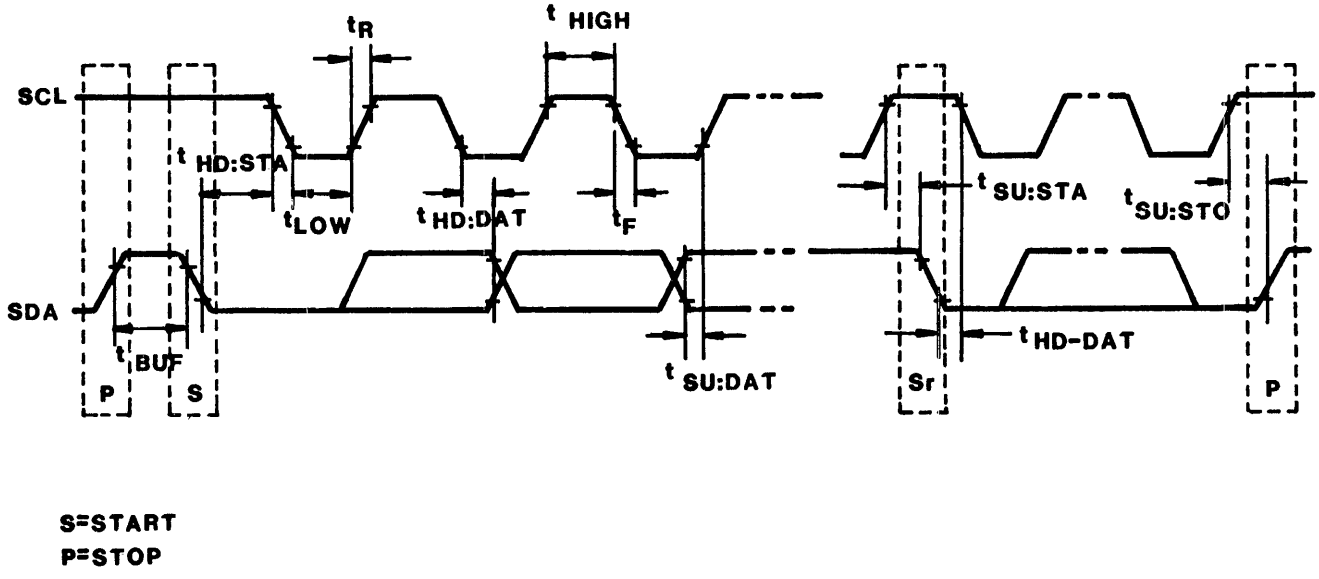
FIGURE 2B ACKNOWLEDGEMENT



ACKNOWLEDGEMENT

An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C I^2C BUS TIMING REQUIREMENTS

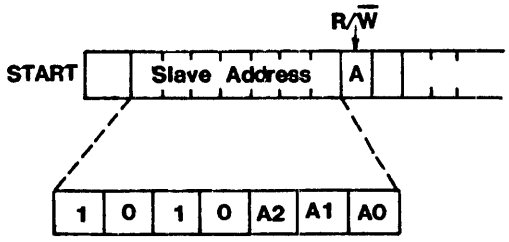


I^2C BUS PROTOCOL

A thorough description of the inter-IC bus specifications appears in the Philips document number TVE 81107 which is available upon request from General Instrument. The following is a condensed description of each mode of operation.

Chip Address (Slave Address) Allocation: The three chip address inputs of each PCD8572 (A2, A1, A0) must be externally connected to either +5V (V_{DD}) of ground (V_{SS}) thereby assigning to each PCD8572I a unique three-bit chip address. Up to eight PCD8572Is may be connected to the I^2C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected PCD8572I. The correct bus protocol is shown in figure 3.

FIGURE 3 SLAVE ADDRESS ALLOCATION



Erase/Write Mode: In this mode the master transmitter transmits to the PCD8572I slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address a logic 0 (R/W=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8572I. The PCD8572I slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms. if two bytes are written.

Read Mode: In this mode the master reads the PCD8572I slave after setting the slave address. See figure 5. Following the write mode control bit (R/W=0) and the acknowledge bit, the word address An is written to the on-chip address pointer.

Next the START condition and slave address are repeated followed by the READ mode control bit (R/W=1). At this point the master transmitter becomes the master receiver and the PCD8572I slave receiver becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8572I slave transmitter will now place the data byte at address A_{n+1} on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8572I slave without first writing to the (voltaile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIGURE 4 ERASE + REWRITE MODE

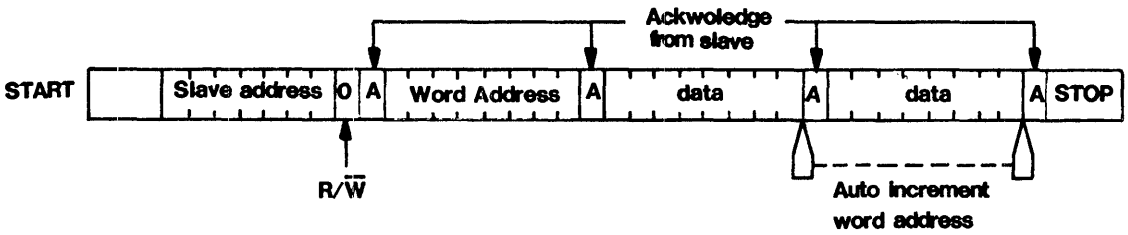


FIGURE 5 READ MODE

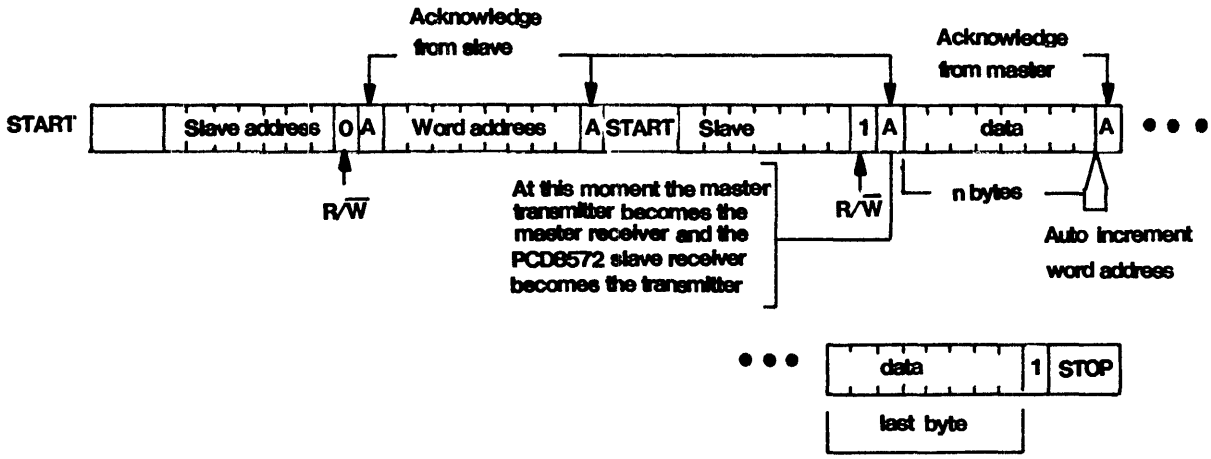
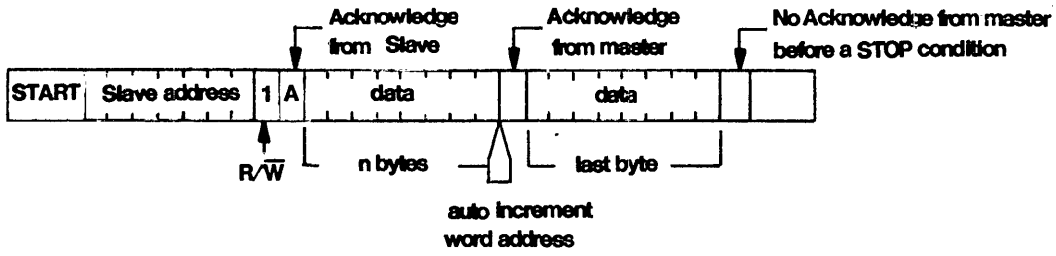
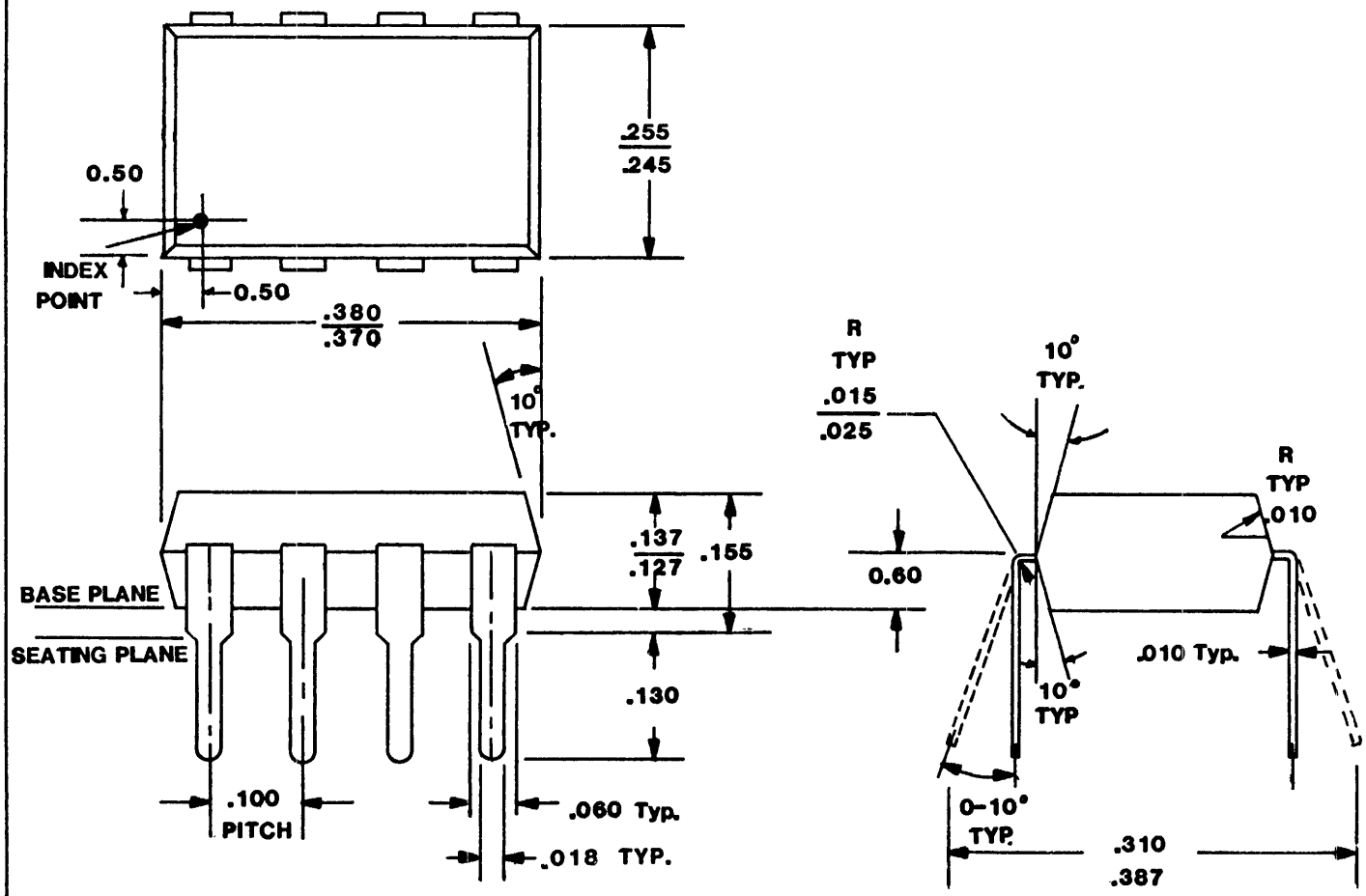


FIGURE 6 ALTERNATE READ MODE



PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20019A-9

1024 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

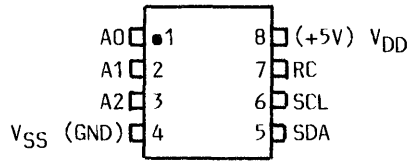
FEATURES:

- 256 x 8 serial EEPROM
- Single +5V only operation
- Compatible with the inter-integrated-circuit (I^2C) bus
- Fully TTL compatible inputs and outputs
- Unlimited read accesses
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range

PIN CONFIGURATION

8 LEAD DUAL IN LINE

TOP VIEW

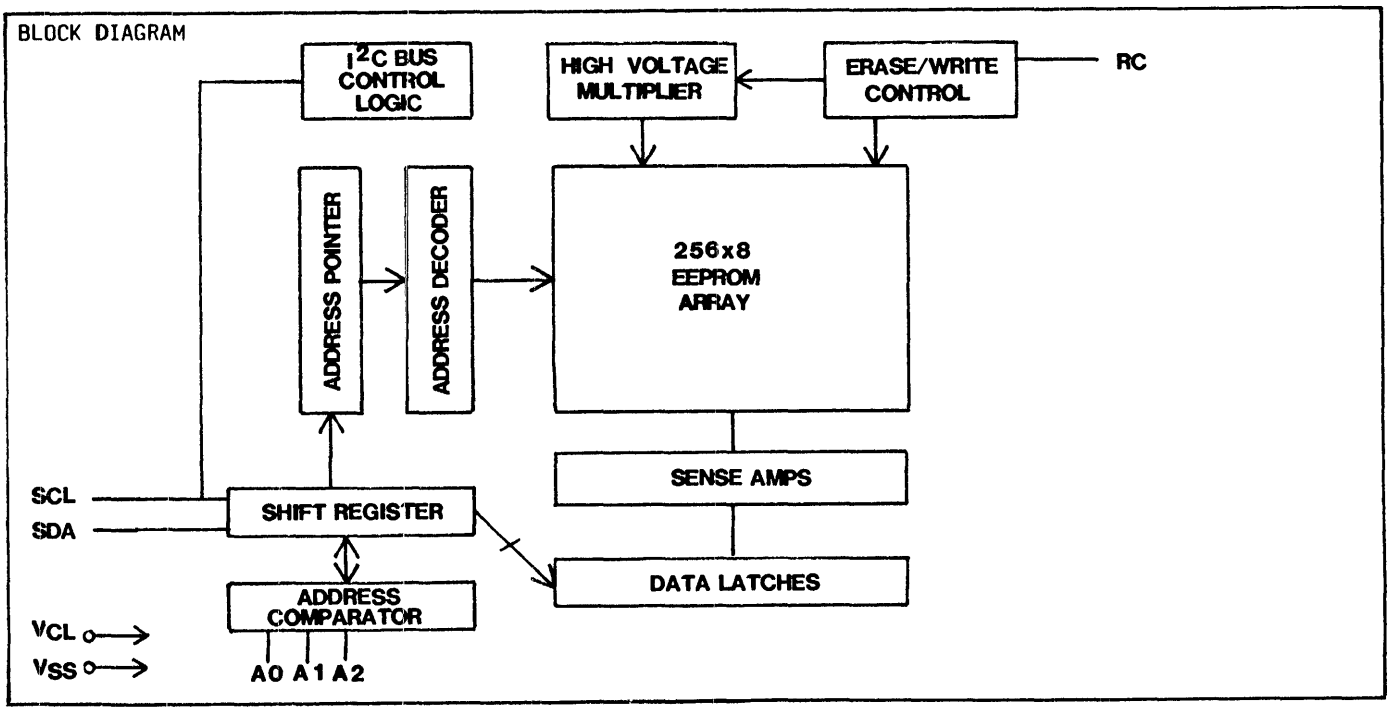


DESCRIPTION

The PCD8582 is a 2K EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I^2C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I^2C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400 pf maximum bus capacitance).

Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8582s may be connected to the I^2C bus.

BLOCK DIAGRAM



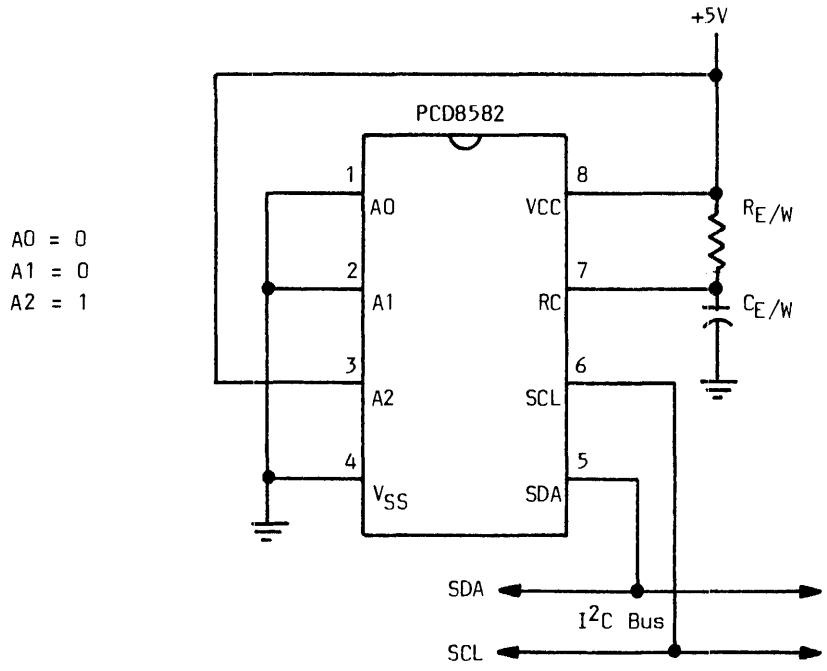
PIN FUNCTIONS

A0, A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input, Erase/Write
RC	Time Constant Network Input
V_{DD}	+5V Power Supply

Figure 1 below shows the typical manner in which the PCD8582 is interfaced to the I^2C bus. For purposes of illustration chip address A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8582s can be connected to the I^2C bus of a single system. The erase/write cycle time of this device $T_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:
When the PCD8582 is not used in an I^2C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 TYPICAL INTERFACE



CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each reciever acknowledges with a nineth bit which must be provided by the user.

Within the I^2C bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The PCD8582 works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (GND)
V_{DD} = +5 ± 10% volts
Ambient Operating Temperature (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

*ABSOLUTE MAXIMUM RATINGS

Characteristic	Sym	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	-0.3	-	7.0	V
Voltage On Any Input Pin	V_I	V_{SS}-0.8	-	V_{DD}+0.8	V
Ambient Operating Temperature	T_A	0	-	+70	°C
Storage Temperature (Unpowered and without data retention)	T_{STG}	-65	-	+150	°C
Current Into Any Input Pin	I_I	-	-	100	µA
Output Current	I_O	-	-	3	mA (SINK)
Soldering Temperature of Leads (10 seconds)	-	-	-	300	°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	I_{DDR}	-	15	-	mA	
Operating Supply Current WRITE/ERASE Mode	I_{DDW}	-	15	-	mA	
Operating Supply Current STANDBY Mode	I_{DDO}	-	12	-	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	I_{IL}	-	-	1	µA	
Output Leakage Current HIGH	I_{OH}	-	-	1	µA	
SCL Input and SDA Input/ Output Pins:						
High Level Input Voltage	V_{IH}	3.0	-	V_{DD}+0.8	V	
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V	
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3mA V_{DD} = 4.5V
A0, A1, A2 Pins:						
High Level Input Voltage	V_{IH}	V_{DD}-0.5	-	V_{DD}+0.5	V	
Low Level Input Voltage	V_{IL}	-0.3	-	0.5	V	

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	-	100	KHz	
The LOW period of the clock	t_{LOW}	4.7	-	-	µs	
The HIGH period of the clock	t_{HIGH}	4.0	-	-	µs	
SDA and SCL rise time	t_R	-	-	1	µs	
SDA and SCL fall time	t_F	-	-	300	ns	
START condition hold time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	µs	
Setup time for start condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	-	-	µs	
Data set-up time	$t_{SU;DAT}$	250	-	-	ns	
Data hold time for I^2C devices	$t_{HD;DAT}$	0	-	-	µs	See note 2
STOP condition set-up time	$t_{SU;STO}$	4.7	-	-	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	-	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/ write cycles)	$N_{E/W}$	-	-	10,000	E/W cycles	Per byte
Data Retention Time	t_S	10	-	-	Years	
Input Capacitance on SCL, SDA	C_I	-	-	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES:
1. All values referred to V_{IH} and V_{IL} levels.
2. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FIGURE 2A DATA TRANSFER SEQUENCE ON THE SERIAL BUS

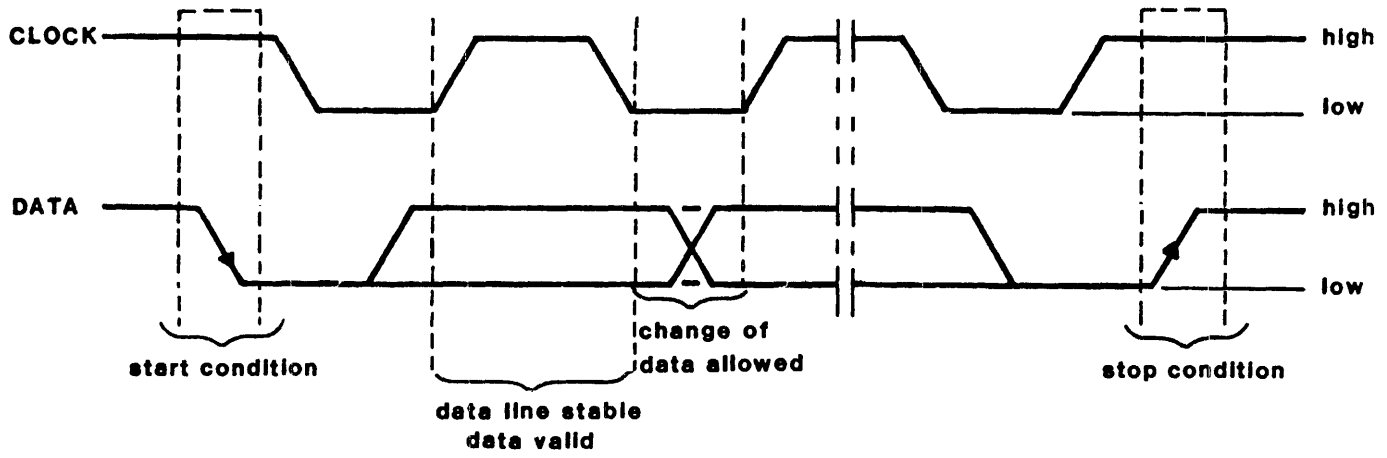
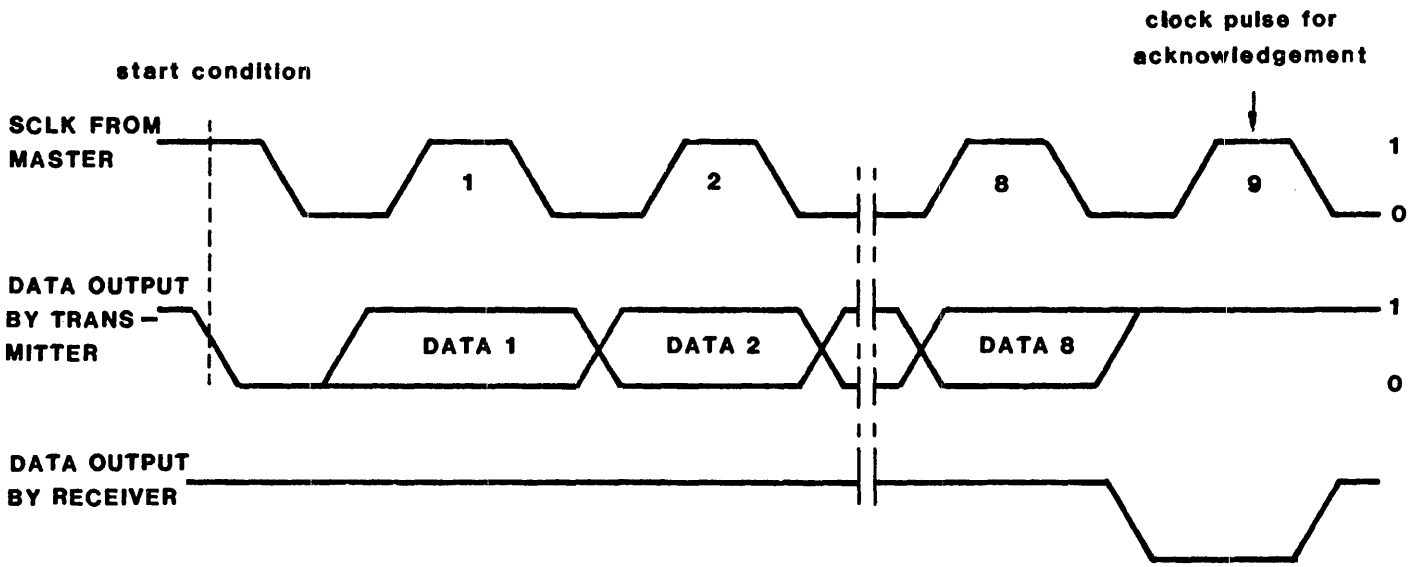


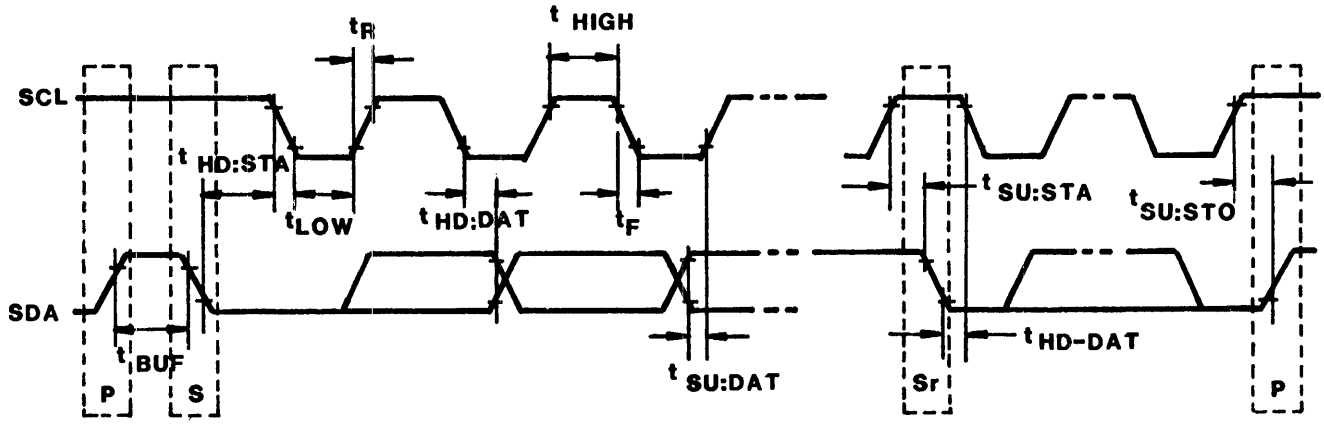
FIGURE 2B ACKNOWLEDGEMENT



ACKNOWLEDGEMENT

An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C I^2C BUS TIMING REQUIREMENTS

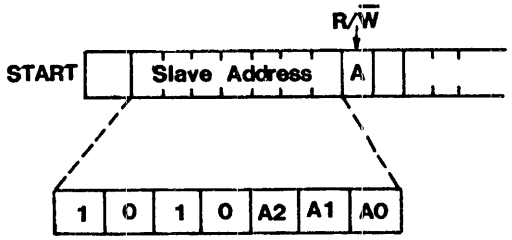


I^2C BUS PROTOCOL

A thorough description of the inter-IC bus specifications appears in the Philips document number TVE 81107 which is available upon request from General Instrument. The following is a condensed description of each mode of operation.

Chip Address (Slave Address) Allocation: The three chip address inputs of each PCD8582 (A2, A1, A0) must be externally connected to either +5V (V_{DD}) or ground (V_{SS}) thereby assigning to each PCD8582 a unique three-bit chip address. Up to eight PCD8582s may be connected to the I^2C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected PCD8582. The correct bus protocol is shown in figure 3.

FIGURE 3 SLAVE ADDRESS ALLOCATION



Erase/Write Mode: In this mode the master transmitter transmits to the PCD8582 slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address a logic 0 (R/W=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8582. The PCD8582 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms, if two bytes are written.

Read Mode: In this mode the master reads the PCD8582 slave after setting the slave address. See figure 5. Following the write mode control bit (R/W=0) and the acknowledge bit, the word address An is written to the on-chip address pointer.

Next the START condition and slave address are repeated followed by the READ mode control bit (R/W=1). At this point the master transmitter becomes the master receiver and the PCD8582 slave receiver becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8582 slave transmitter will now place the data byte at address A_{n+1} on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8582 slave without first writing to the (voltaile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIGURE 4 ERASE + REWRITE MODE

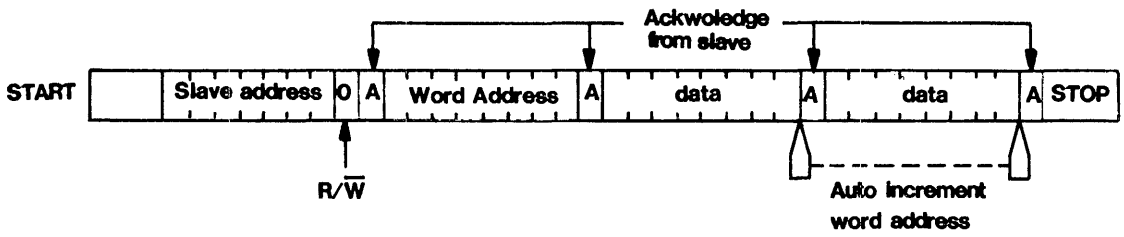


FIGURE 5 READ MODE

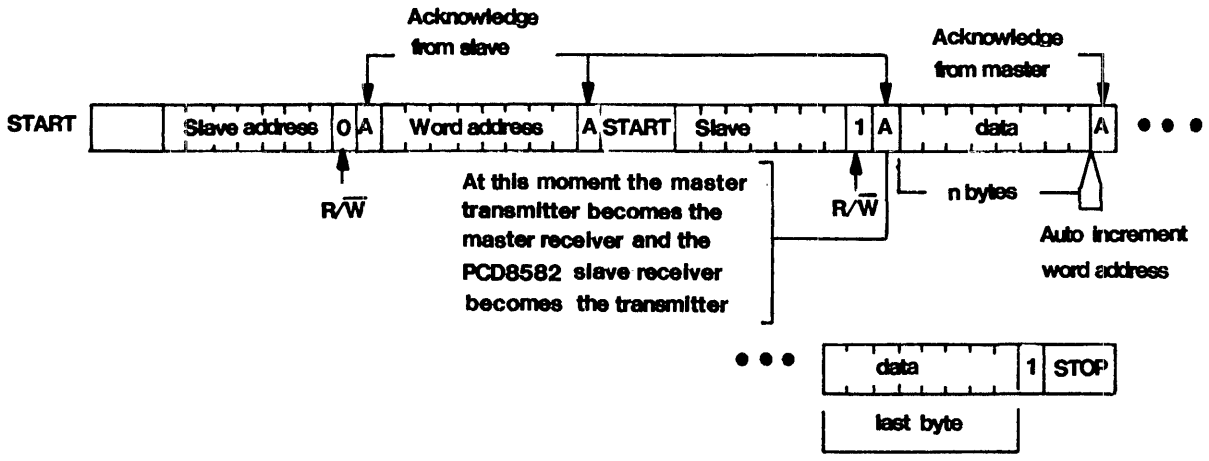
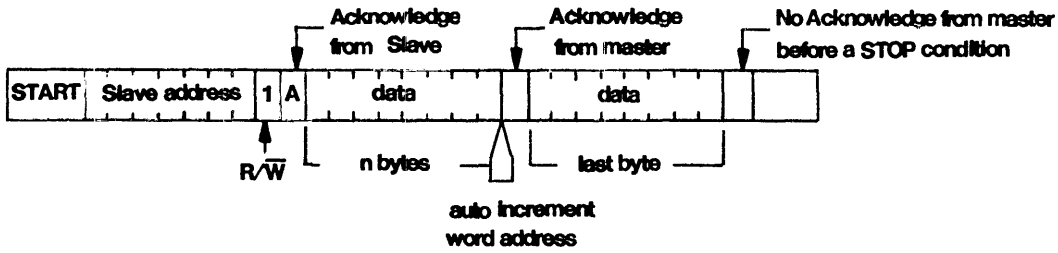
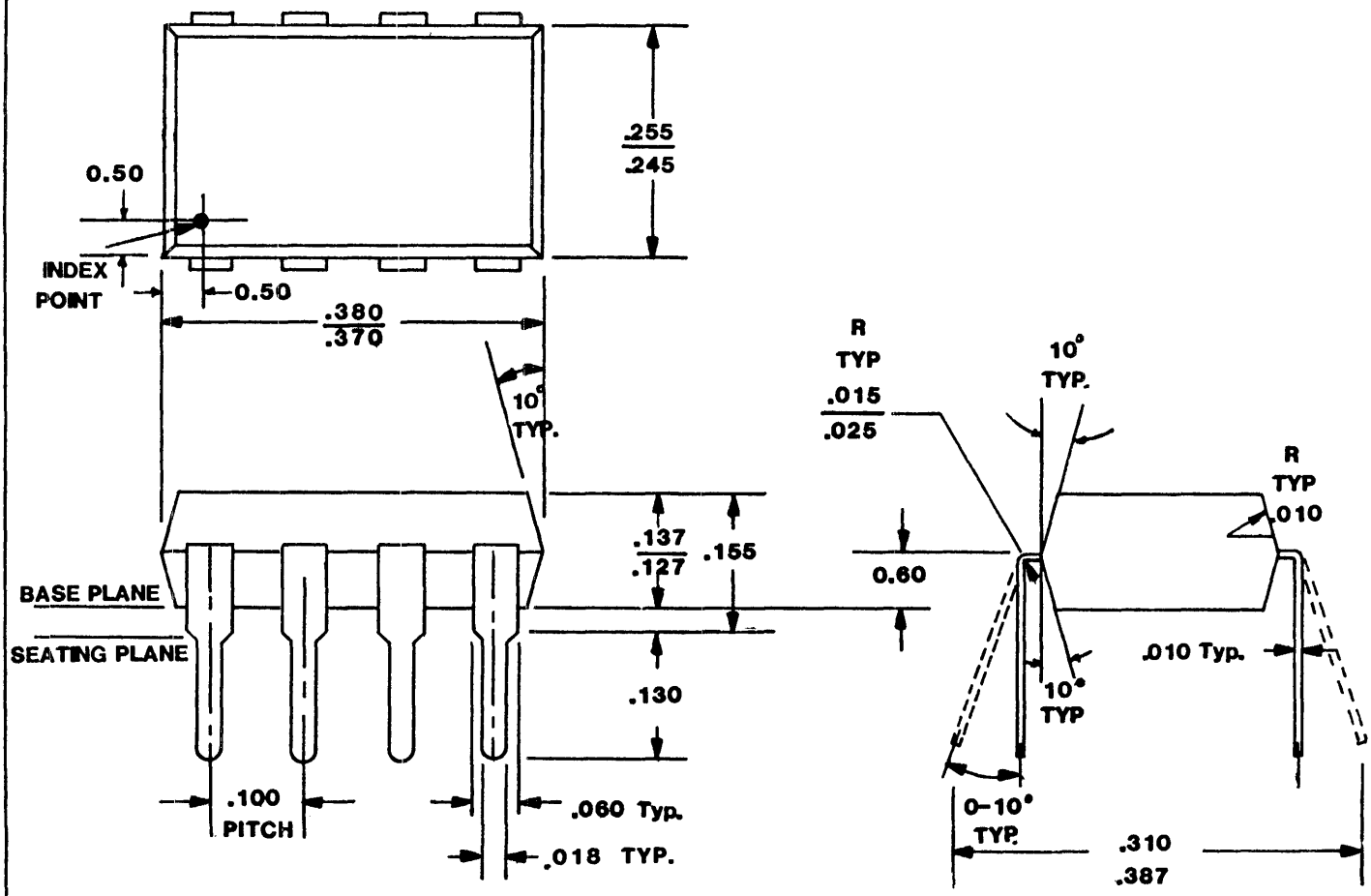


FIGURE 6 ALTERNATE READ MODE



PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

1024 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

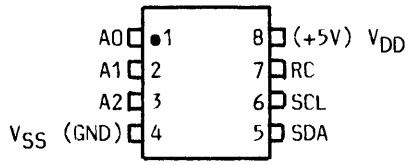
FEATURES:

- 256 x 8 serial EEPROM
- Single +5V only operation
- Compatible with the inter-integrated-circuit (I^2C) bus
- Fully TTL compatible inputs and outputs
- Unlimited read accesses
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- -40°C to +85°C operating ambient temperature range

PIN CONFIGURATION

8 LEAD DUAL IN LINE

TOP VIEW

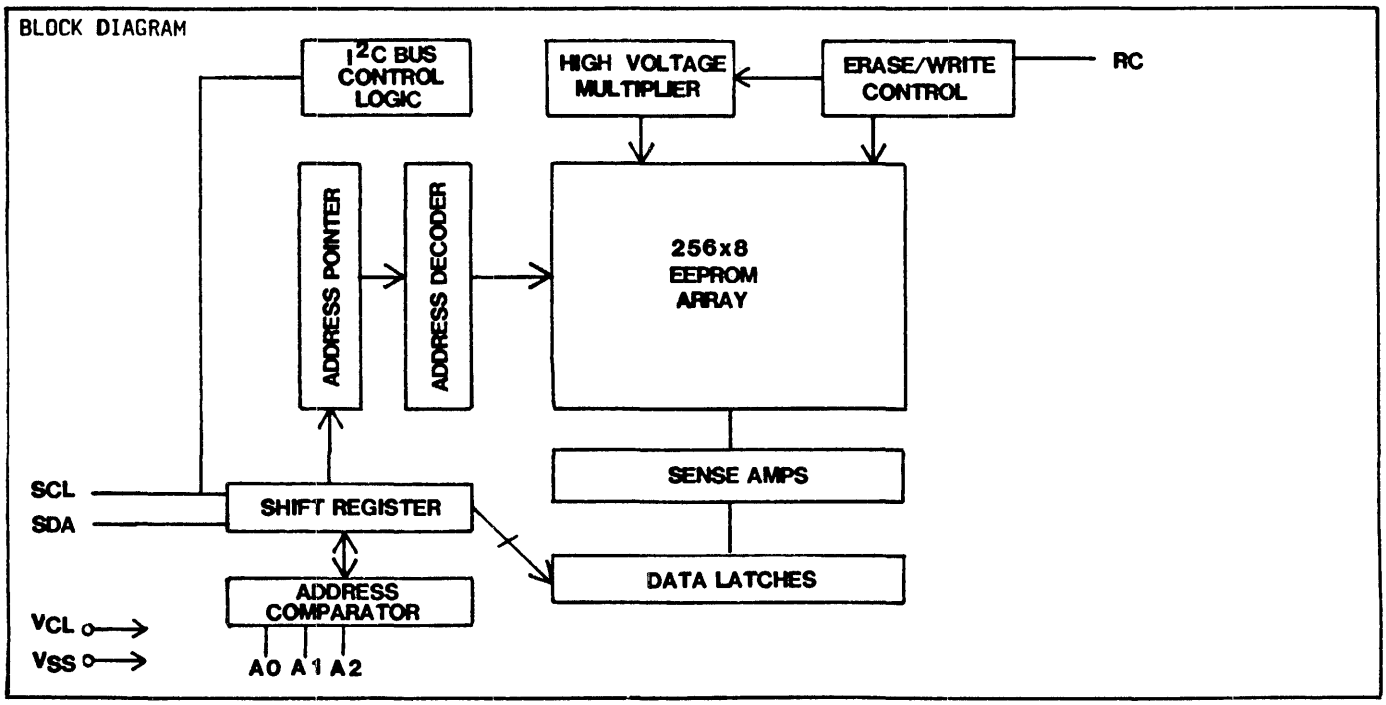


DESCRIPTION

The PCD8582I is a 2K EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I^2C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I^2C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400 pf maximum bus capacitance).

Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8582Is may be connected to the I^2C bus.

BLOCK DIAGRAM



DS20026A-1

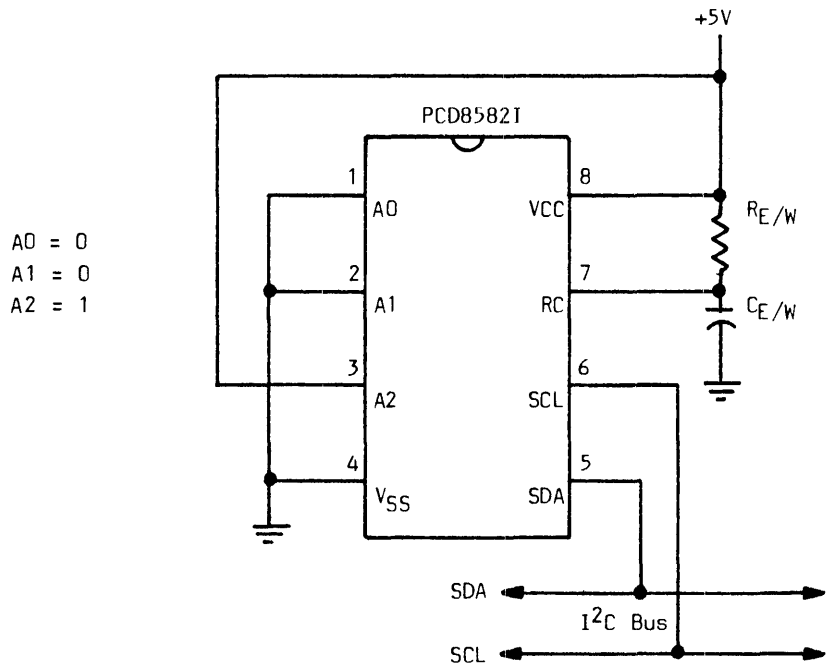
PIN FUNCTIONS

A0, A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input, Erase/Write
RC	Time Constant Network Input
V_{DD}	+5V Power Supply

Figure 1 below shows the typical manner in which the PCD8582I is interfaced to the I^2C bus. For purposes of illustration chip address A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8582Is can be connected to the I^2C bus of a single system. The erase/write cycle time of this device $T_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:
When the PCD8582I is not used in an I^2C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 TYPICAL INTERFACE



CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each reciever acknowledges with a nineth bit which must be provided by the user.

Within the I^2C bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The PCD8582I works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (GND)
V_{DD} = +5 ± 10% volts
Ambient Operating Temperature (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

*ABSOLUTE MAXIMUM RATINGS

Characteristic	Sym	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	-0.3	-	7.0	V
Voltage On Any Input Pin	V_I	V_{SS}-0.8	-	V_{DD}+0.8	V
Ambient Operating Temperature	T_A	0	-	+70	°C
Storage Temperature (Unpowered and without data retention)	T_{STG}	-65	-	+150	°C
Current Into Any Input Pin	I_I	-	-	100	µA
Output Current	I_O	-	-	3	mA (SINK)
Soldering Temperature of Leads (10 seconds)	-	-	-	300	°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	I_{DDR}	-	15	-	mA	
Operating Supply Current WRITE/ERASE Mode	I_{DDW}	-	15	-	mA	
Operating Supply Current STANDBY Mode	I_{DDO}	-	12	-	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	I_{IL}	-	-	1	µA	
Output Leakage Current HIGH	I_{OH}	-	-	1	µA	
SCL Input and SDA Input/ Output Pins:						
High Level Input Voltage	V_{IH}	3.0	-	V_{DD}+0.8	V	
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V	
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3mA V_{DD} = 4.5V
A0, A1, A2 Pins:						
High Level Input Voltage	V_{IH}	V_{DD}-0.5	-	V_{DD}+0.5	V	
Low Level Input Voltage	V_{IL}	-0.3	-	0.5	V	

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	-	100	KHz	
The LOW period of the clock	t_{LOW}	4.7	-	-	µs	
The HIGH period of the clock	t_{HIGH}	4.0	-	-	µs	
SDA and SCL rise time	t_R	-	-	1	µs	
SDA and SCL fall time	t_F	-	-	300	ns	
START condition hold time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	µs	
Setup time for start condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	-	-	µs	
Data set-up time	$t_{SU;DAT}$	250	-	-	ns	
Data hold time for I^2C devices	$t_{HD;DAT}$	0	-	-	µs	See note 2
STOP condition set-up time	$t_{SU;STO}$	4.7	-	-	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	-	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/ write cycles)	$N_{E/W}$	-	-	10,000	E/W cycles	Per byte
Data Retention Time	t_S	10	-	-	Years	
Input Capacitance on SCL, SDA	C_I	-	-	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES:
1. All values referred to V_{IH} and V_{IL} levels.
2. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FIGURE 2A DATA TRANSFER SEQUENCE ON THE SERIAL BUS

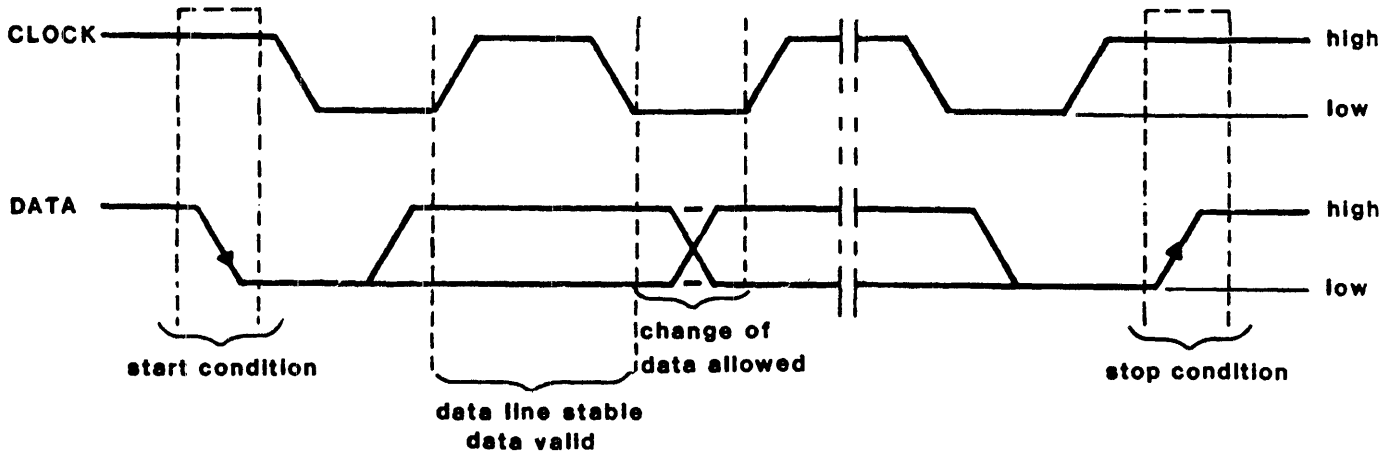
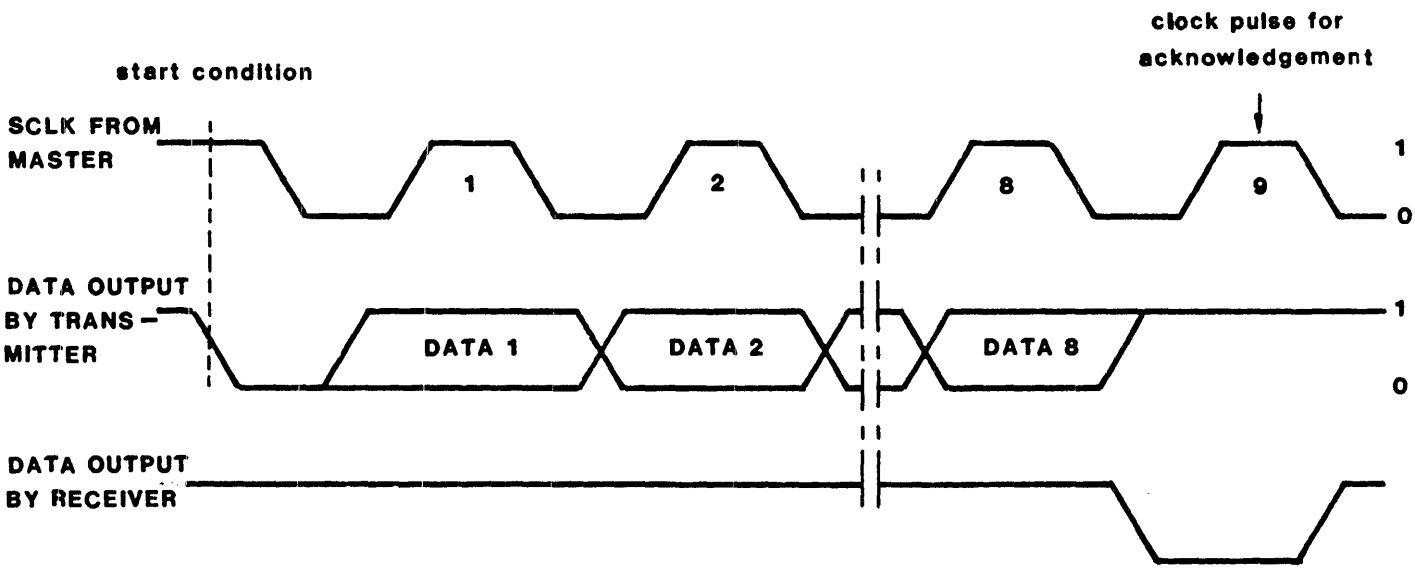


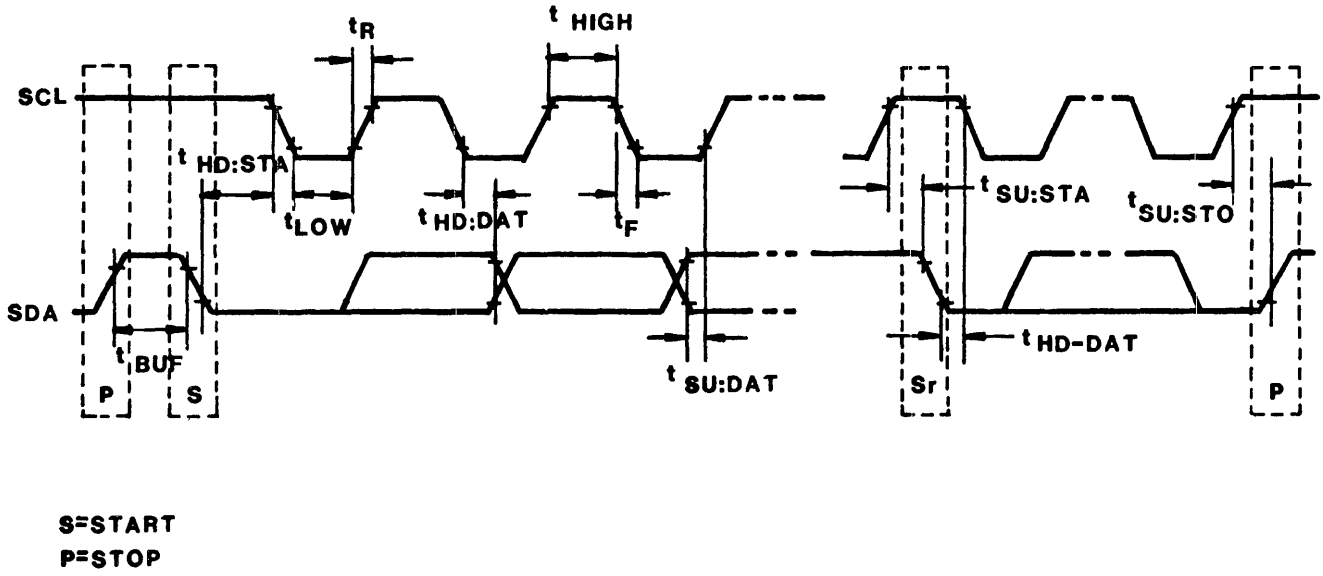
FIGURE 2B ACKNOWLEDGEMENT



ACKNOWLEDGEMENT

An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C I^2C BUS TIMING REQUIREMENTS

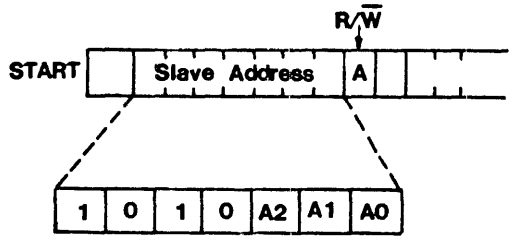


I^2C BUS PROTOCOL

A thorough description of the inter-IC bus specifications appears in the Philips document number TVE 81107 which is available upon request from General Instrument. The following is a condensed description of each mode of operation.

Chip Address (Slave Address) Allocation: The three chip address inputs of each PCD8582 (A2, A1, A0) must be externally connected to either +5V (V_{DD}) or ground (V_{SS}) thereby assigning to each PCD8582I a unique three-bit chip address. Up to eight PCD8582Is may be connected to the I^2C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected PCD8582I. The correct bus protocol is shown in figure 3.

FIGURE 3 SLAVE ADDRESS ALLOCATION



Erase/Write Mode: In this mode the master transmitter transmits to the PCD8582I slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address a logic 0 (R/W=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8582I. The PCD8582I slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms, if two bytes are written.

Read Mode: In this mode the master reads the PCD8582I slave after setting the slave address. See figure 5. Following the write mode control bit (R/W=0) and the acknowledge bit, the word address An is written to the on-chip address pointer.

Next the START condition and slave address are repeated followed by the READ mode control bit (R/W=1). At this point the master transmitter becomes the master receiver and the PCD8582I slave receiver becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8582I slave transmitter will now place the data byte at address A_{n+1} on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8582I slave without first writing to the (voltaile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIGURE 4 ERASE + REWRITE MODE

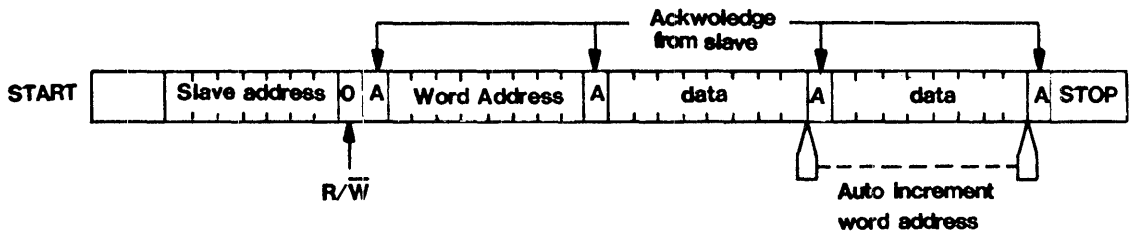


FIGURE 5 READ MODE

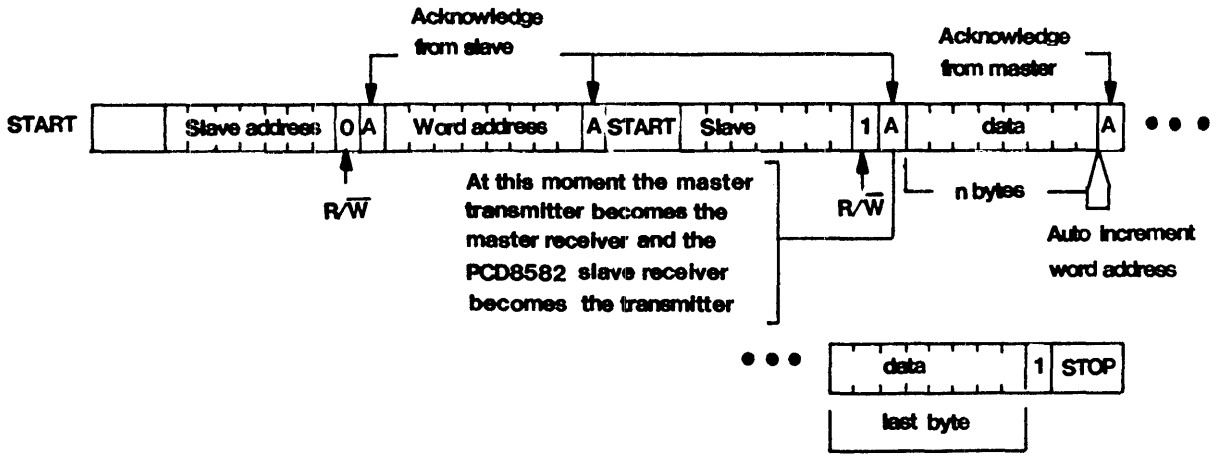
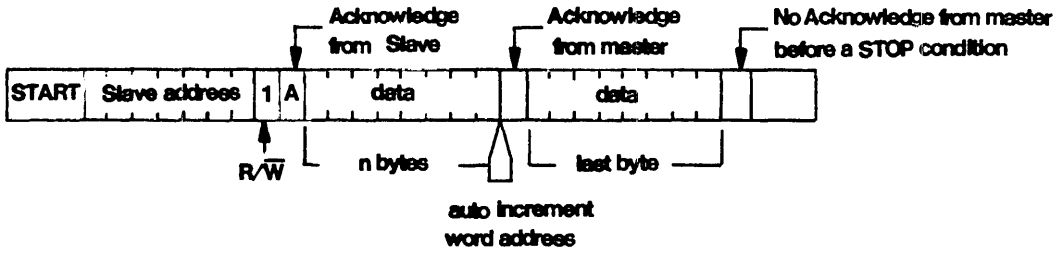
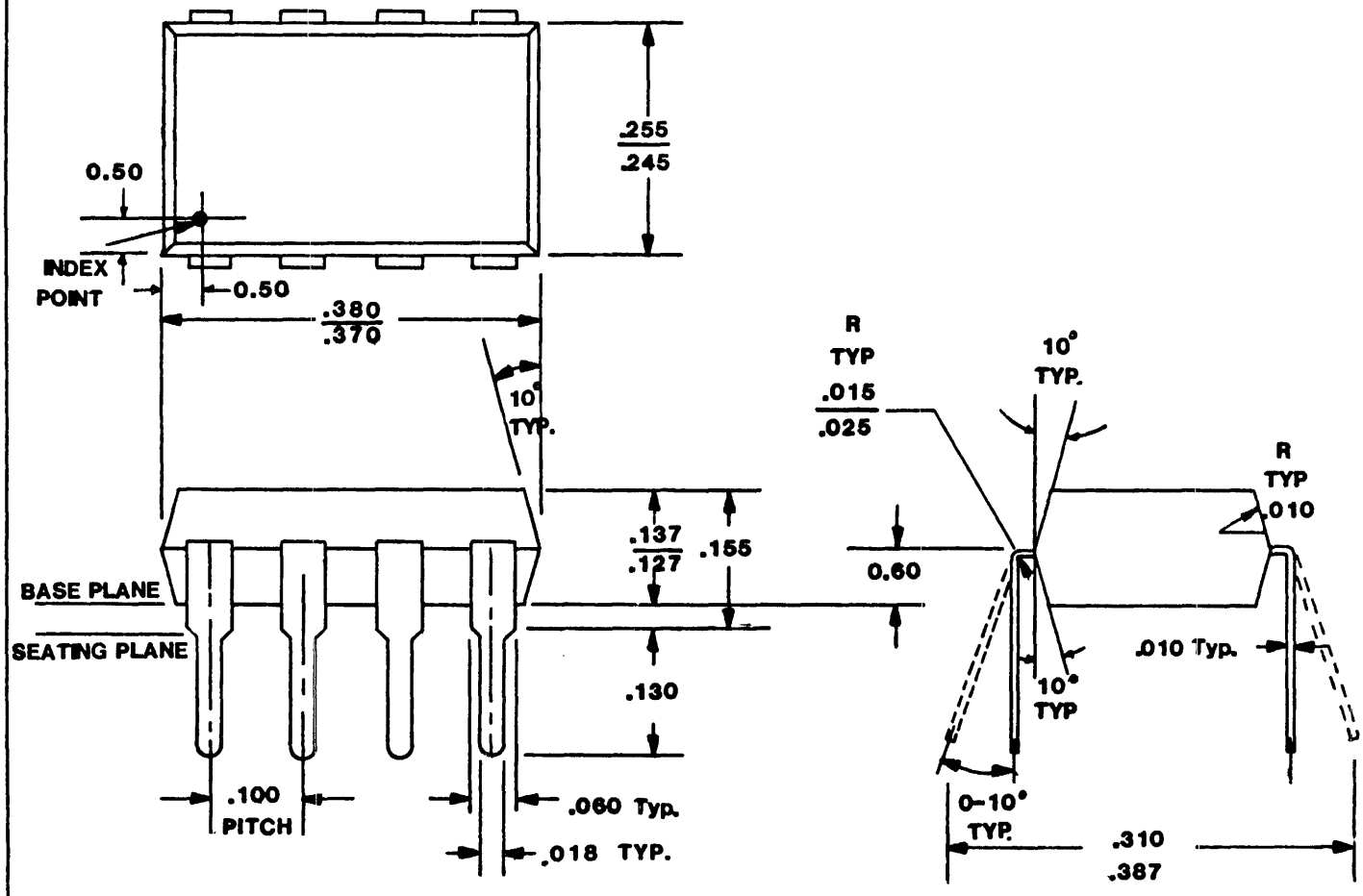


FIGURE 6 ALTERNATE READ MODE



PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20026A-9

GENERAL INSTRUMENT	ER5901

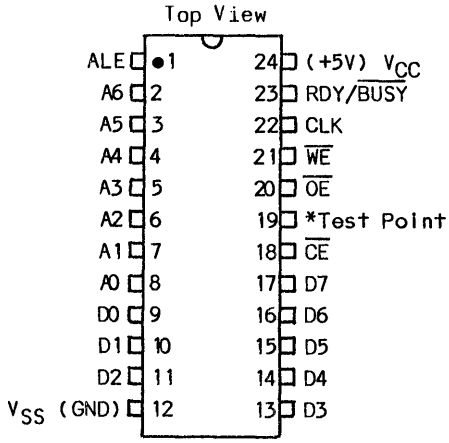
WORD ALTERABLE 1024 BIT ELECTRICALLY ERASABLE AND PROGRAMABLE ROM

FEATURES

- 1024 bits, organized 128 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Self-timing
- RC controlled write timing
- RDY/$\overline{BUSY}$ signal
- Address and data buses may be used separately or multiplexed
- $\overline{CE}$ and $\overline{OE}$ inputs to avoid bus contention
- Word Alterable
- Read Access time of less than 300ns
- On-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pin out
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

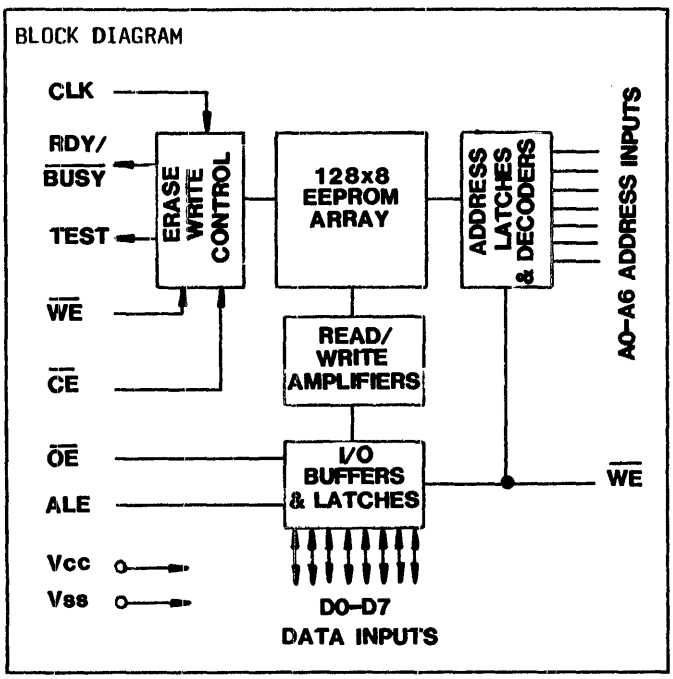


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5901 is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5901 can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5901 is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{BUSY}$ signal is available, the ER5901 frees the system for other tasks during the programming cycle. The READ/write logic is designed such that bus contention will be minimized by use of $\overline{OE}$ and $\overline{CE}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

Multiplexed Mode: Address & Data Tied To Data Bus[3]							
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ALE[1,2]	RDY/$\overline{BUSY}$	MODE	I/O	POWER
H	X	X	X	H	STANDBY	High Z	Standby
L	L	H	⎍	H	READ	D_{OUT}	ACTIVE
L	X	⎍	⎍	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	X	H	READ/Write inhibit	High Z	ACTIVE

1. In non-multiplexed mode, connect ALE and $\overline{WE}$ together.
2. In multiplexed mode, address inputs are latched on the falling edge, and data inputs are latched on the rising edge.
3. In non-multiplexed mode, address and data bus are separate.

Device Operation

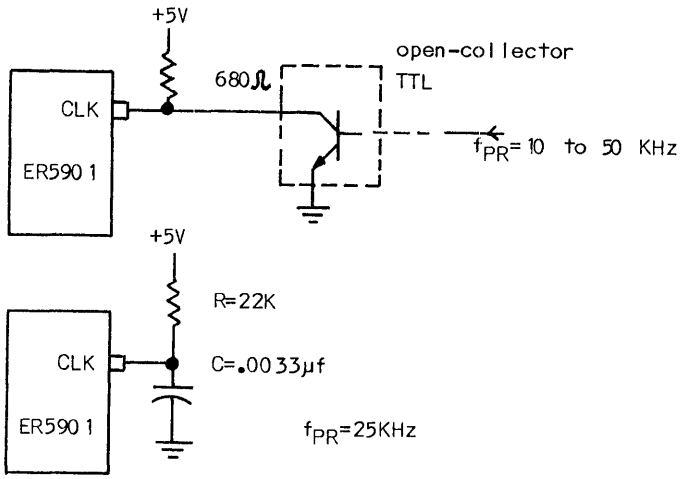
ADDRESSES:

The address inputs select one of the EEPROM 8-bit words. The address latch enable (ALE) is provided so the memory may be used with a multiplexed address and data bus. When this feature is not required, the address bus and data bus are separate and ALE may be tied to $\overline{WE}$.

CHIP ENABLE ($\overline{CE}$):

The chip enable terminal affects the data-in/data-out and write enable ($\overline{WE}$) terminals. When chip enable is high, the I/O terminals are in the floating or high impedance state.

Figure 5



PIN FUNCTIONS

Symbol	Function	Comments
ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
A0-A6	7 bit address	
D0-D7	8 bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	Used for chip selection.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprograming cycle; input data latched on a positive edge.
CLK	Timing Input	Defines clock frequency for reprograming. May be RC or external clock.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprograming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt power connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless other noted)
V_{SS} = GND
V_{CC} = +5V ±10%
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.5	-	+0.8	V	
CLK High Level Input Voltage	V_{IHT}	3.5		V_{CC}+1.0	V	
CLK Low Level Input Voltage	V_{ILT}	-0.5		+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA
Input Leakage Current	I_{IL}	-		±10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{OL}			±10	µA	V_{OUT} = GND to V_{CC}
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	60	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	50	60	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	330	440	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	275	330	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

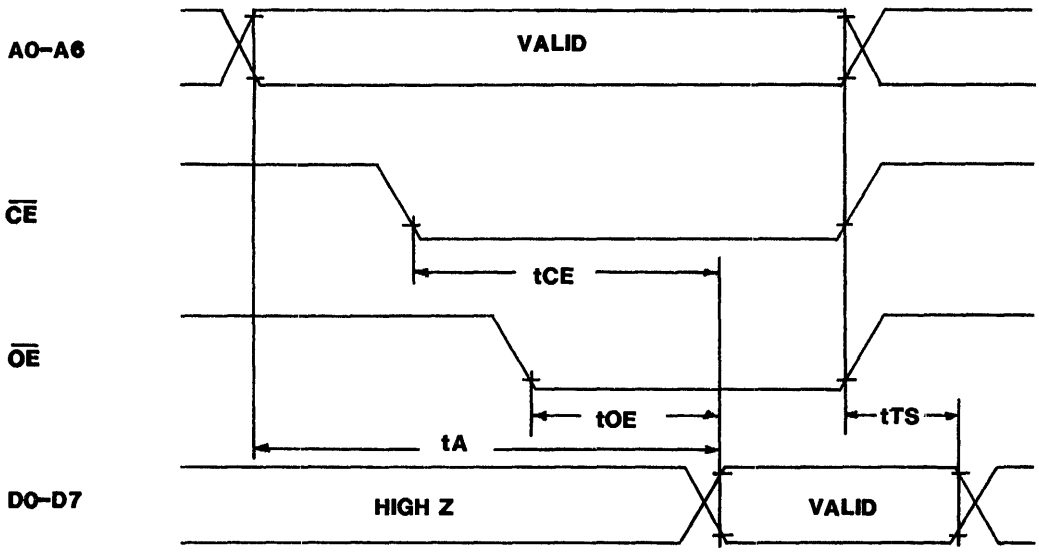
Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

MEMORY CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprograming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	Unlimited				

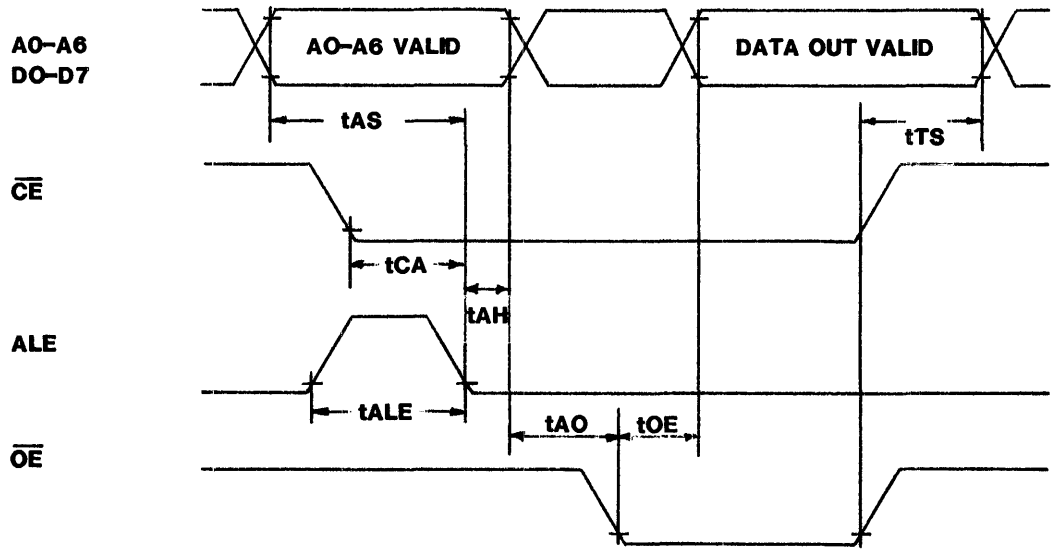
NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

FIGURE 1: READ MODE with separate address and data lines



READ MODE (Separate Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Access time - Address to output delay	t_A	-	-	300	ns	Load = 1TTL gate + C_L = 100 pF $\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	-	-	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	-	175	ns	$\overline{CE}$ = V_{IL}
Address, $\overline{CE}$ or $\overline{OE}$ to output tri-state	t_{TS}	10	-	150	ns	

FIGURE 2: READ MODE with Multiplexed Address and Data Lines



READ MODE (Multiplexed Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	-	-	ns	
ALE Pulse Width	t_{ALE}	175	-	-	ns	
Address Hold time	t_{AH}	50	-	-	ns	
Address float to Output Enable	t_{AO}	20	-	-	ns	
$\overline{OE}$ to output delay	t_{OE}	10	-	175	ns	$\overline{CE} = V_{IL}$
Address, $\overline{CE}$ or $\overline{OE}$ to output tri-state	t_{TS}	10	-	150	ns	

WRITE ENABLE ($\overline{WE}$):

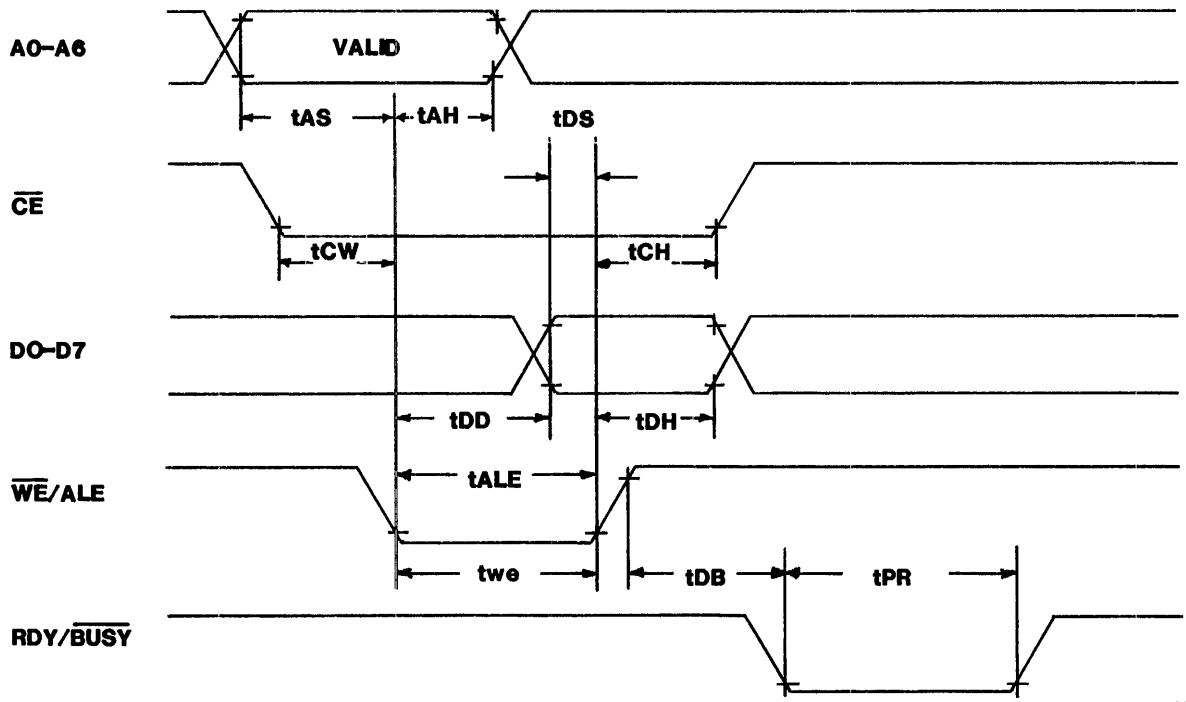
WRITE CYCLE:

By virtue of the on-chip reprogramming control and timing of the ER5901, a minimum amount of servicing is required from the host microprocessor.

The programming/writing of the ER5901 can be done in the multiplexed address and data mode or separate address and data mode. In the multiplexed mode, the ALE line is pulsed high while the address to be altered is presented to lines A0 to A6 of the selected device (see figure 4). The falling edge of ALE latches the address into the ER5901, and the information on the bus lines is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge, after a delay t_{DB} the RDY/$\overline{BUSY}$ output will go low for the the duration of the programming cycle.

In the separate data and address mode, the ALE may be tied to $\overline{WE}$ (see figure 3). With a stable address and data presented to the respective inputs of a selected device, the $\overline{WE}$/ALE line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output goes low and remains

FIGURE 3: Program Mode with separate Address and Data Lines



PROGRAM MODE (Separate Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Data delay time	t_{DD}	-	-	1	us	
Chip Enable to Write Enable Delay	t_{CW}	100	-	-	ns	
Data setup time	t_{DS}	175	-	-	ns	
Address hold time	t_{AH}	50	-	-	ns	
Write Enable Pulse Width	t_{WE}	175ns	-	100 µs	-	
Data hold time	t_{DH}	50	-	-	ns	
$\overline{WE}$ to $\overline{CE}$ delay	t_{CH}	0	-	-	ns	
Status Delay	t_{DB}	10	-	300	ns	
RDY/$\overline{BUSY}$ low time (programing time)	t_{PR}	20	-	100	ms	$t_{PR} = 1024 \div f_{PR}$
Address Latch Enable Pulse Width	t_{ALE}	175ns		100 µs	-	
Program Clock frequency	f_{PR}	10	-	50	KHZ	

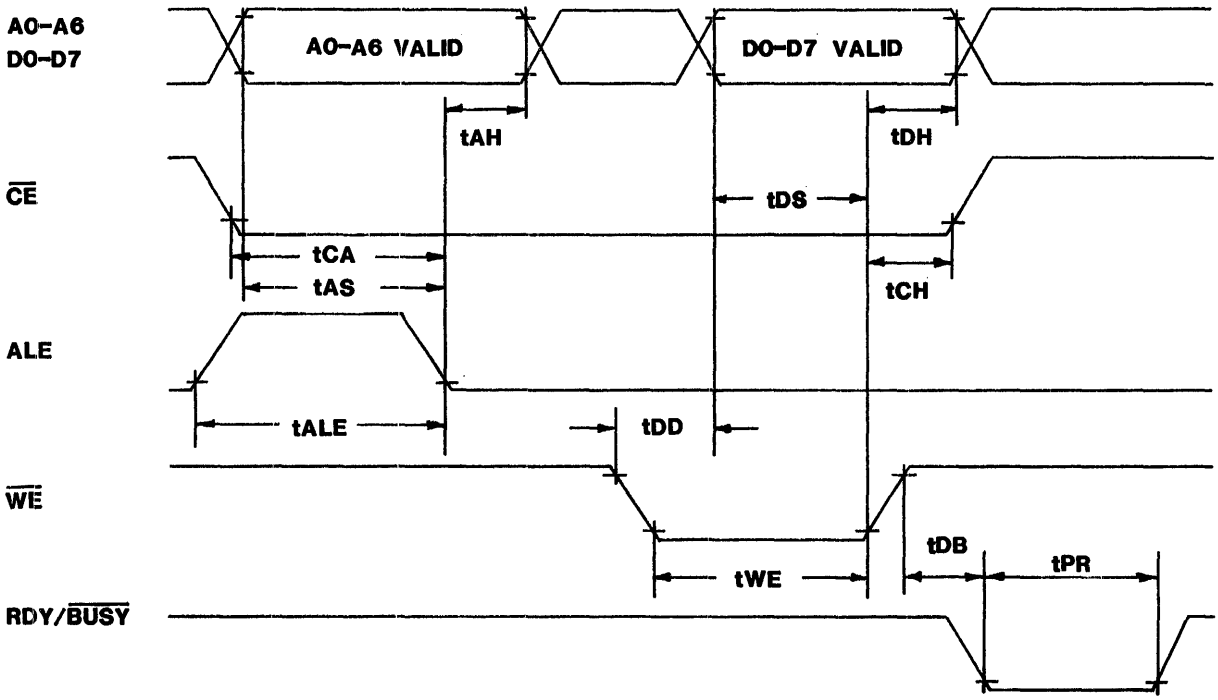
low for the duration of the programming cycle. All inputs to the ER5901 are disabled during a programming cycle.

OUTPUT ENABLE (OE): READ

Reading can be accomplished in the multiplexed or separate address and data bus mode as well. When reading in the multiplexed mode, the ALE line is pulsed high while a valid address is presented to the A0 to A6 inputs. The address is latched into the ER5901 on the falling edge of ALE. In order to avoid bus contention these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay, t_{OE}, the selected byte will appear on lines D0 to D7 until either $\overline{OE}$ or $\overline{CE}$ goes high (see figure 2).

When reading in the separate data and address mode, valid address and data must appear on the respective bus and they must remain there for the duration of the READ cycle because ALE doesn't latch the address in this mode (see figure 1). Data will appear on the data bus after a time delay t_{OE} measured from the falling edge of $\overline{OE}$.

FIGURE 4: Program Mode with Multiplexed Address and Data Lines



PROGRAM MODE (Multiplexed Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	-	-	ns	
ALE pulse width	t_{ALE}	175ns	-	100 µs	-	
Address hold time	t_{AH}	50	-	-	ns	
Data setup time	t_{DS}	175ns	-	100 µs	-	
$\overline{WE}$ pulse width	t_{WE}	175ns	-	100µs	-	
Data hold time	t_{DH}	20	-	-	ns	
$\overline{WE}$ to $\overline{CE}$ delay	t_{CH}	0	-	-	ns	
Status delay	t_{DB}	10	-	300	ns	
Status low time (programing time)	t_{PR}	20	-	100	ms	$t_{PR} = 1024 \div f_{PR}$
Data delay time	t_{DD}	-	-	1	µs	
Program clock frequency	f_{PR}	10	-	50	KHZ	

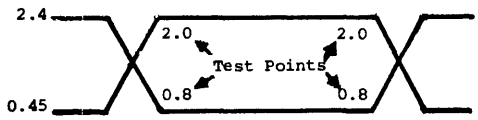
CLOCK CONSIDERATIONS (CLK):

The CLK is a schmitt trigger timing input which defines the clock frequency for the programming cycle. Either an RC combination or an external clock may be used for this input (see figure 5). Typical vales of R and C are 22K and .0033µF respectively, with 5% tolerance. As the clock rate increases, the write cycle will be shortened. In applications where data is updated often, the retention time need not be long, Therefore, the write cycle may be shorter than 20ms. When driving the ER5901 with an external clock, an open collector transistor with a 680 ohm pull-up resistor should be used. (See Figure 5). The logic levels (V_{IHT}, V_{ILT}) that apply to the clock input are defined in the table, "DC CHARACTERISTICS".

POWER-UP

During power-up it is recommended to hold $\overline{OE}$ high to minimize bus contention.

A.C. Testing Input/Output Waveform



A.C. Testing:

Inputs are driven at 2.4V for an input logic high and 0.45V for an input logic low. Timing measurements are made at 2.0V for a logic high and 0.8V for a logic low.

ON-CHIP DATA PROTECTION

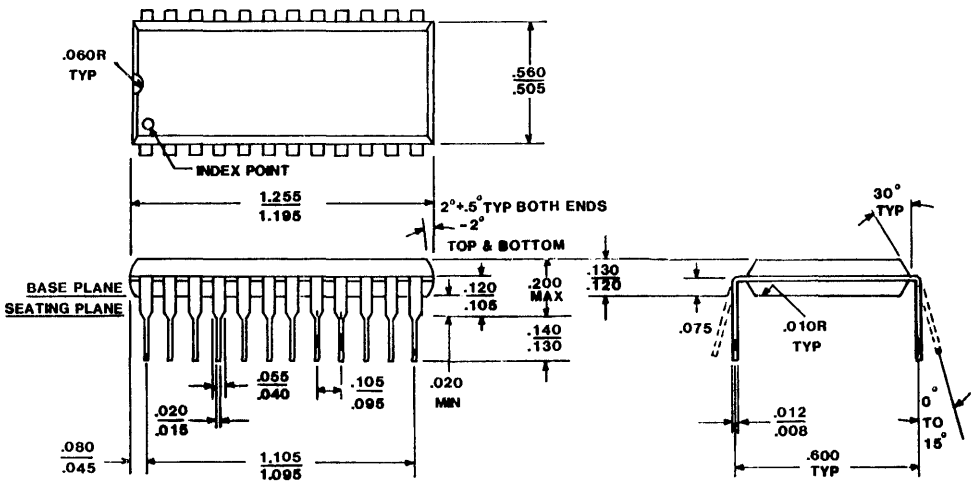
During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. Furthermore, during power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

NOTE:

Since all modes of operation are enabled when V_{CC} reaches between 2.8 and 3.5 volts, care must be taken to avoid a negative edge on the $\overline{WE}$ line ($t_{WE} \geq 50ns$) during power up. Such a spike may cause a write operation to occur.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

GENERAL INSTRUMENT	ER5901I

WORD ALTERABLE 1024 BIT ELECTRICALLY ERASABLE AND PROGRAMABLE ROM

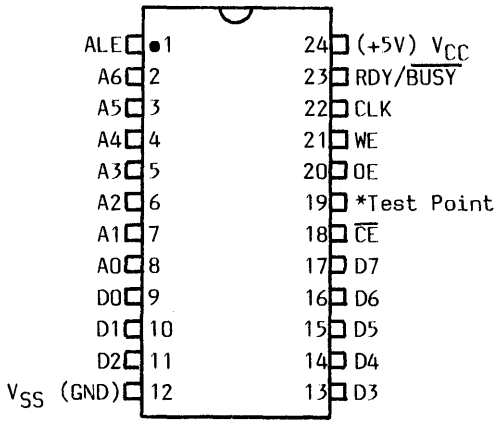
FEATURES

- 1024 bits, organized 128 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Self-timing
- RC controlled write timing
- RDY/$\overline{BUSY}$ signal
- Address and data buses may be used separately or multiplexed
- $\overline{CE}$ and $\overline{OE}$ inputs to avoid bus contention
- Word Alterable
- Read Access time of less than 300ns
- On-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pin out
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

Top View

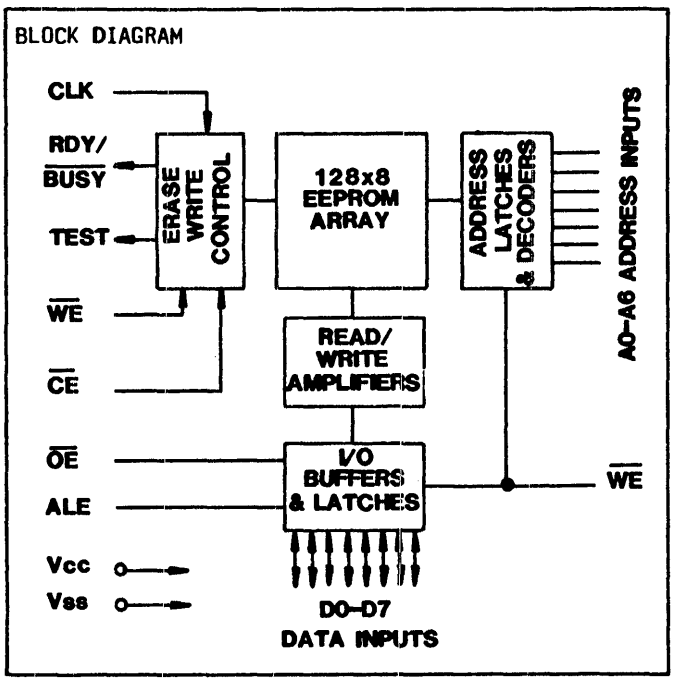


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5901I is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5901I can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5901I is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{BUSY}$ signal is available, the ER5901I frees the system for other tasks during the programming cycle. The READ/write logic is designed such that bus contention will be minimized by use of $\overline{OE}$ and $\overline{CE}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

Multiplexed Mode: Address & Data Tied To Data Bus[3]							
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ALE[1,2]	RDY/$\overline{BUSY}$	MODE	I/O	POWER
H	X	X	X	H	STANDBY	High Z	Standby
L	L	H	⎍	H	READ	D_{OUT}	ACTIVE
L	X	⎎	⎍	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	X	H	READ/Write inhibit	High Z	ACTIVE

1. In non-multiplexed mode, connect ALE and $\overline{WE}$ together.
2. In multiplexed mode, address inputs are latched on the falling edge, and data inputs are latched on the rising edge.
3. In non-multiplexed mode, address and data bus are separate.

Device Operation

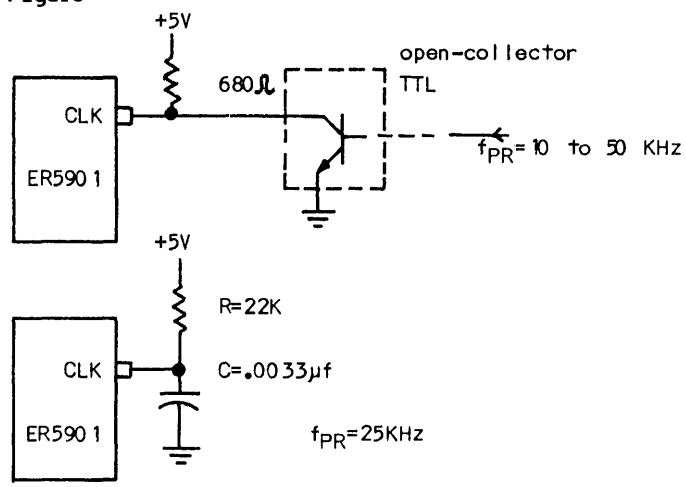
ADDRESSES:

The address inputs select one of the EEPROM 8-bit words. The address latch enable (ALE) is provided so the memory may be used with a multiplexed address and data bus. When this feature is not required, the address bus and data bus are separate and ALE may be tied to $\overline{WE}$.

CHIP ENABLE ($\overline{CE}$):

The chip enable terminal affects the data-in/data-out and write enable ($\overline{WE}$) terminals. When chip enable is high, the I/O terminals are in the floating or high impedance state.

Figure 5



PIN FUNCTIONS

Symbol	Function	Comments
ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
A0-A6	7 bit address	
D0-D7	8 bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	Used for chip selection.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprogramming cycle; input data latched on a positive edge.
CLK	Timing Input	Defines clock frequency for reprogramming. May be RC or external clock.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprogramming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt power connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V

Storage temperature (unpowered and without data retention)..... -65°C to +150°C

Soldering temperature of leads (10 seconds)..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty. expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

Standard Conditions (unless other noted)

V_{SS} = GND

V_{CC} = +5V $\pm$10%

Operating Temperature Range (T_A):

-40°C to +85°C (Industrial)

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-0.5	-	+0.8	V	
CLK High Level Input Voltage	V_{IHT}	3.5		V_{CC}+1.0	V	
CLK Low Level Input Voltage	V_{ILT}	-0.5		+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -200 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA
Input Leakage Current	I_{IL}	-		+10	µA	V_{IN} = GND to V_{CC}
Output Leakage Current	I_{OL}			+10	µA	V_{OUT} = GND to V_{CC}
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	60	90	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	50	70	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	330	495	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	275	385	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

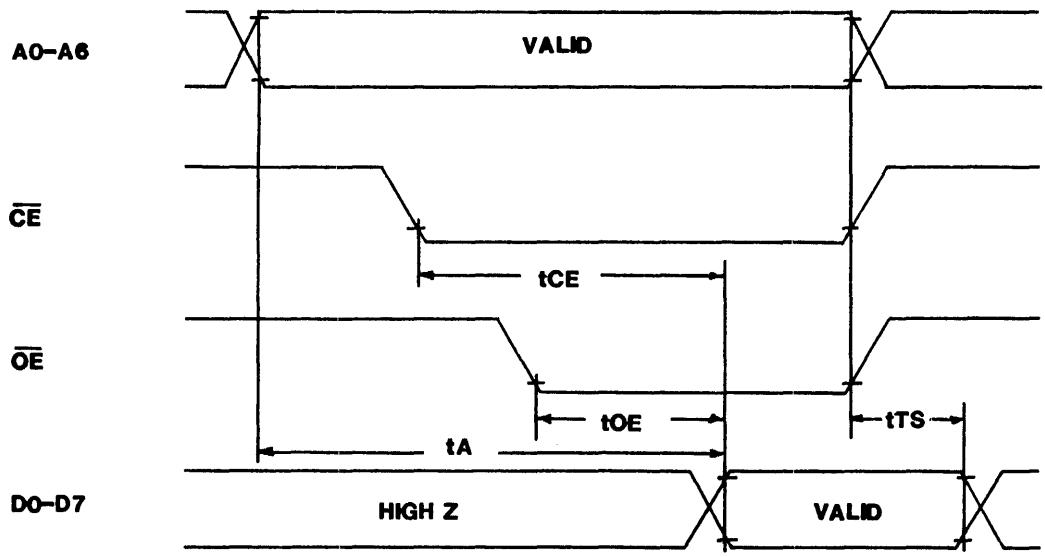
Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

MEMORY CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprograming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	Unlimited				

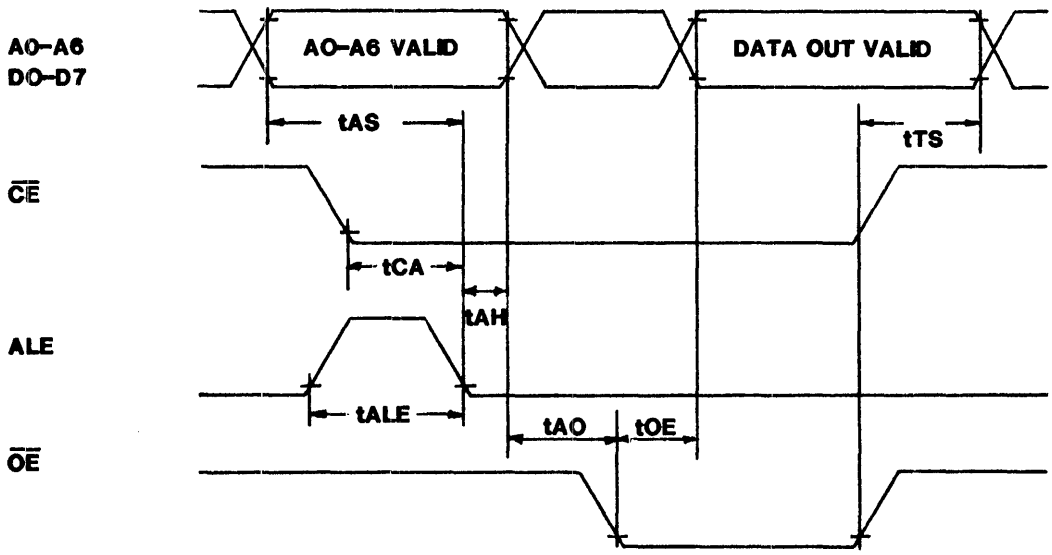
NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

FIGURE 1: READ MODE with separate address and data lines



READ MODE (Separate Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Access time - Address to output delay	t_A	-	-	300	ns	Load = 1TTL gate + C_L = 100 pF $\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	-	-	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	-	175	ns	$\overline{CE}$ = V_{IL}
Address, $\overline{CE}$ or $\overline{OE}$ to output tri-state	t_{TS}	10	-	150	ns	

FIGURE 2: READ MODE with Multiplexed Address and Data Lines



READ MODE (Multiplexed Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	-	-	ns	
ALE Pulse Width	t_{ALE}	175	-	-	ns	
Address Hold time	t_{AH}	50	-	-	ns	
Address float to Output Enable	t_{AO}	20	-	-	ns	
$\overline{OE}$ to output delay	t_{OE}	10	-	175	ns	$\overline{CE}$ = V_{IL}
Address, $\overline{CE}$ or $\overline{OE}$ to output tri-state	t_{TS}	10	-	150	ns	

WRITE ENABLE ($\overline{WE}$):

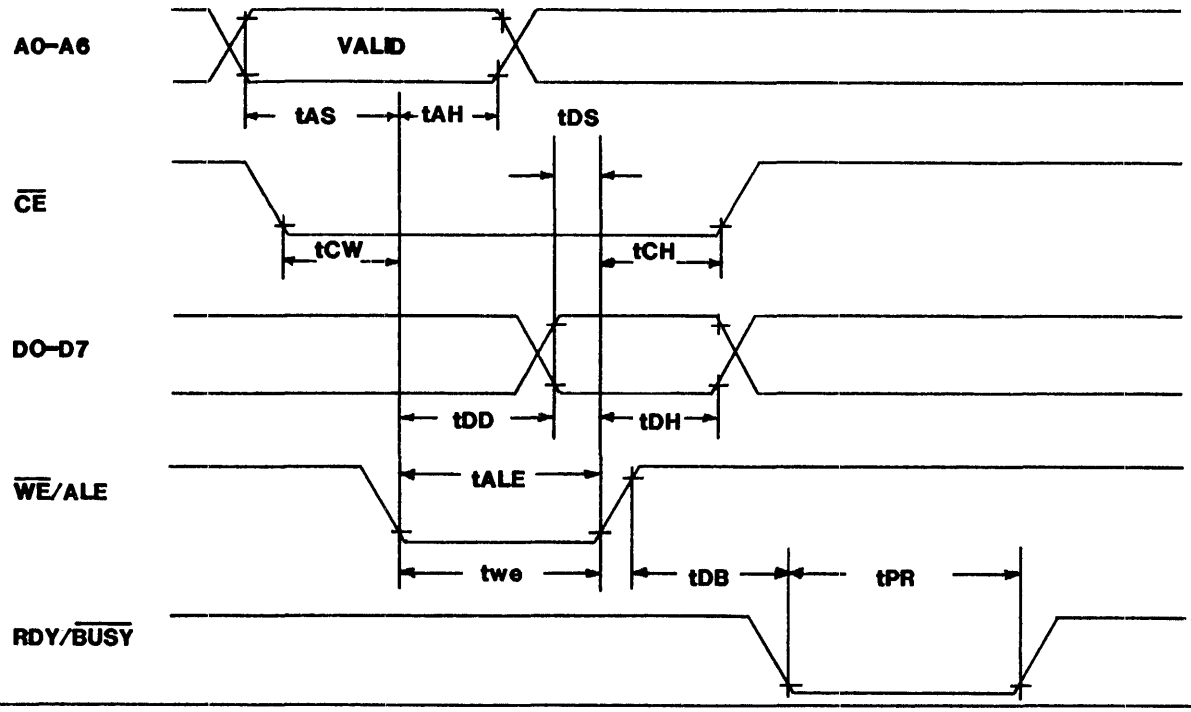
WRITE CYCLE:

By virtue of the on-chip reprogramming control and timing of the ER5901I, a mimimum amount of servicing is required from the host microprocessor.

The programming/writing of the ER5901I can be done in the multiplexed address and data mode or separate address and data mode. In the multiplexed mode, the ALE line is pulsed high while the address to be altered is presented to lines A0 to A6 of the selected device (see figure 4). The falling edge of ALE latches the address into the ER5901I, and the information on the bus lines is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge, after a delay t_{DB} the RDY/$\overline{BUSY}$ output will go low for the the duration of the programming cycle.

In the separate data and address mode, the ALE may be tied to $\overline{WE}$ (see figure 3). With a stable address and data presented to the respective inputs of a selected device, the $\overline{WE}$/ALE line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output goes low and remains

FIGURE 3: Program Mode with separate Address and Data Lines



PROGRAM MODE (Separate Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Data delay time	t_{DD}	-	-	1	us	
Chip Enable to Write Enable Delay	t_{CW}	100	-	-	ns	
Data setup time	t_{DS}	175	-	-	ns	
Address hold time	t_{AH}	50	-	-	ns	
Write Enable Pulse Width	t_{WE}	175ns	-	100µs	-	
Data hold time	t_{DH}	50	-	-	ns	
$\overline{WE}$ to $\overline{CE}$ delay	t_{CH}	0	-	-	ns	
Status Delay	t_{DB}	10	-	300	ns	
RDY/$\overline{BUSY}$ low time (programing time)	t_{PR}	20	-	100	ms	$t_{PR} = 1024 \div f_{PR}$
Address Latch Enable Pulse Width	t_{ALE}	175ns		100µs	-	
Program Clock frequency	f_{PR}	10	-	50	KHZ	

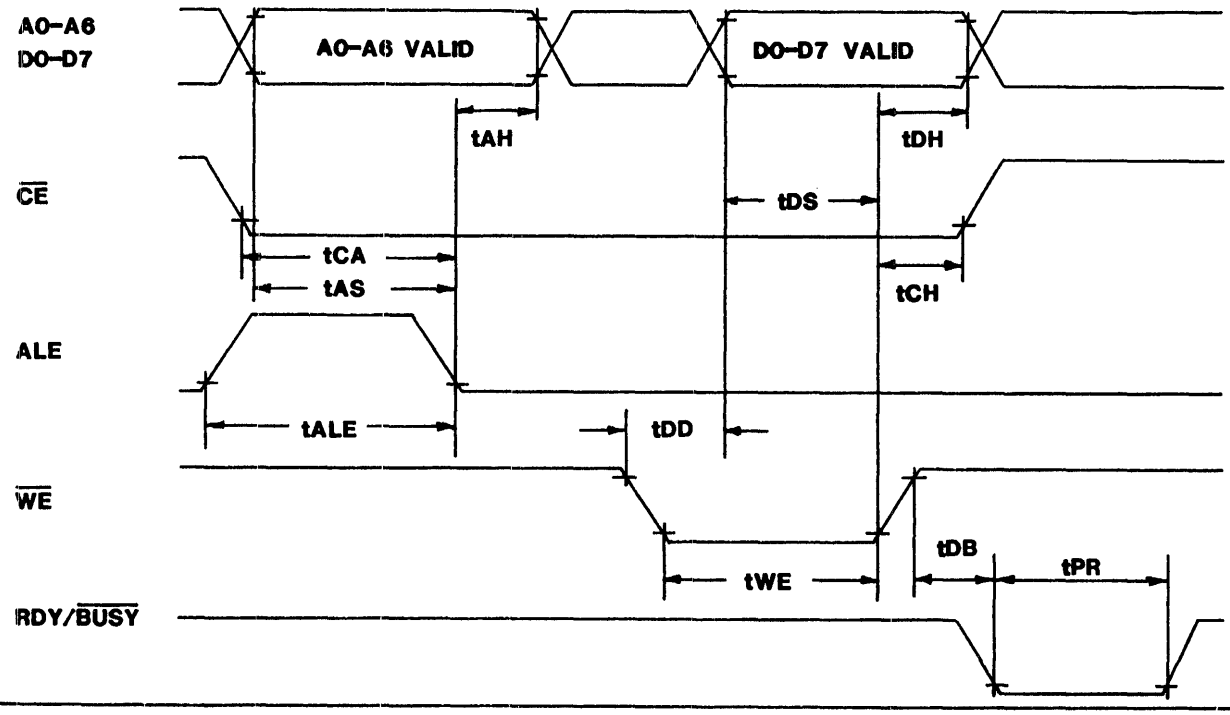
low for the duration of the programming cycle. All inputs to the ER5901I are disabled during a programming cycle.

OUTPUT ENABLE (OE): READ

Reading can be accomplished in the multiplexed or separate address and data bus mode as well. When reading in the multiplexed mode, the ALE line is pulsed high while a valid address is presented to the A0 to A6 inputs. The address is latched into the ER5901I on the falling edge of ALE. In order to avoid bus contention these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay, t_{OE}, the selected byte will appear on lines D0 to D7 until either $\overline{OE}$ or $\overline{CE}$ goes high (see figure 2).

When reading in the separate data and address mode, valid address and data must appear on the respective bus and they must remain there for the duration of the READ cycle because ALE doesn't latch the address in this mode (see figure 1). Data will appear on the data bus after a time delay t_{OE} measured from the falling edge of $\overline{OE}$.

FIGURE 4: Program Mode with Multiplexed Address and Data Lines



PROGRAM MODE (Multiplexed Address and Data Lines)	Sym	Min	Typ	Max	Unit	Conditions
Address setup time	t_{AS}	50	-	-	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	-	-	ns	
ALE pulse width	t_{ALE}	175ns	-	100µs	-	
Address hold time	t_{AH}	50	-	-	ns	
Data setup time	t_{DS}	175ns	-	100µs	-	
$\overline{WE}$ pulse width	t_{WE}	175ns	-	100µs	-	
Data hold time	t_{DH}	20	-	-	ns	
$\overline{WE}$ to $\overline{CE}$ delay	t_{CH}	0	-	-	ns	
Status delay	t_{DB}	10	-	300	ns	
Status low time (programing time)	t_{PR}	20	-	100	ms	$t_{PR} = 1024 \div f_{PR}$
Data delay time	t_{DD}	-	-	1	µs	
Program clock frequency	f_{PR}	10	-	50	KHZ	

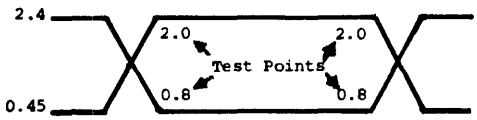
CLOCK CONSIDERATIONS (CLK):

The CLK is a schmitt trigger timing input which defines the clock frequency for the programming cycle. Either an RC combination or an external clock may be used for this input (see figure 5). Typical vales of R and C are 22K and .0033µF respectively, with 5% tolerance. As the clock rate increases, the write cycle will be shortened. In applications where data is updated often. the retention time need not be long, Therefore, the write cycle may be shorter than 20ms. When driving the ER5901I with an external clock, an open collector transistor with a 680 ohm pull-up resistor should be used. (See Figure 5). The logic levels (V_{IHT}, V_{ILT}) that apply to the clock input are defined in the table, "DC CHARACTERISTICS".

POWER-UP

During power-up it is recommended to hold $\overline{OE}$ high to minimize bus contention.

A.C. Testing, Input/Output Waveform



A.C. Testing:

Inputs are driven at 2.4V for an input logic high and 0.45V for an input logic low. Timing measurements are made at 2.0V for a logic high and 0.8V for a logic low.

ON-CHIP DATA PROTECTION

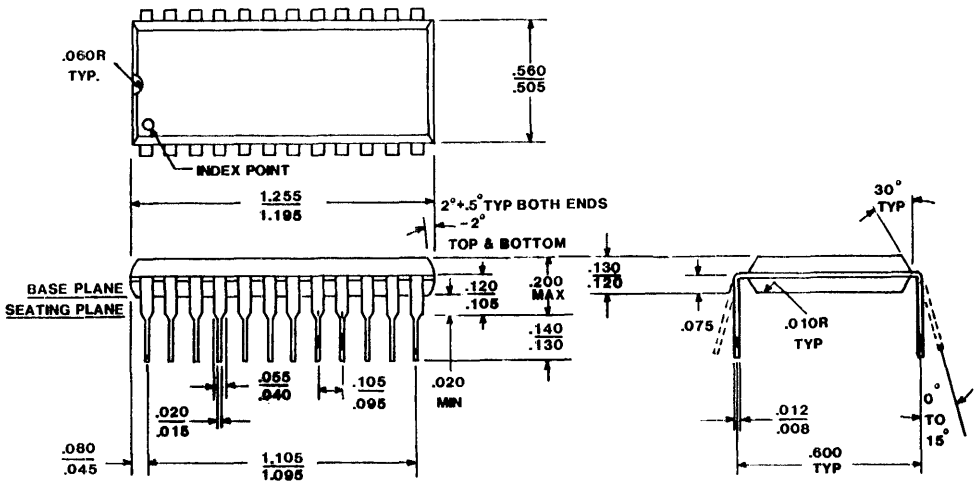
During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. Furthermore, during power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

NOTE:

Since all modes of operation are enabled when V_{CC} reaches between 2.8 and 3.5 volts, care must be taken to avoid a negative edge on the $\overline{WE}$ line ($t_{WE} \geq 50ns$) during power up. Such a spike may cause a write operation to occur.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20022A-8

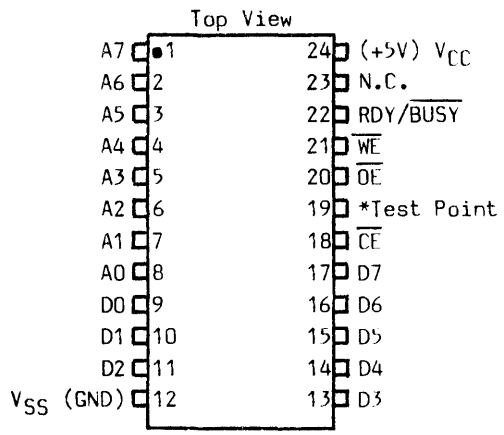
WORD ALTERABLE 2048 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 2048 bits, organized 256 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Automatic write timeout
- RDY/$\overline{BUSY}$ signal
- Optional high voltage program and chip erase modes
- $\overline{CE}$ and $\overline{OE}$ inputs to avoid bus contention
- Word alterable
- Read access time of less than 300ns
- Enhanced on-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pinout
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

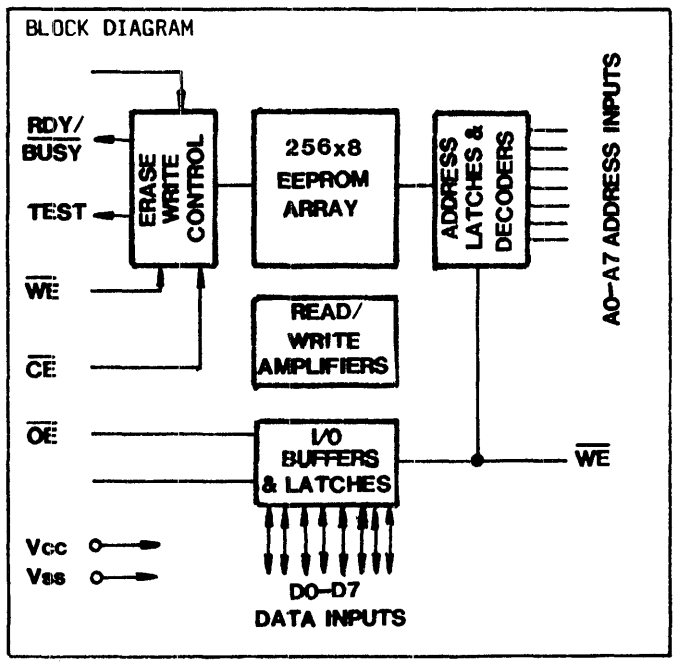


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5902 is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5902 can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5902 is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{BUSY}$ signal is available, the ER5902 frees the system for other tasks during the programming cycle. The read/write logic is designed such that bus contention will be minimized by use of $\overline{OE}$ and $\overline{CE}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

+5V ONLY OPERATION						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
H	X	X	H	STANDBY	High Z	STANDBY
L	L	H	H	READ	D_{OUT}	ACTIVE
L	H	⊓	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	H	READ/WRITE INHIBIT	High Z	ACTIVE

OPTIONAL HIGH VOLTAGE COMPATIBLE MODES						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
L	H	20-22V	L	BYTE ERASE	D_W=H	ACTIVE
L	H	20-22V	L	BYTE ERASE	D_W	ACTIVE
L	20-22V	20-22V	L	CHIP ERASE	D_{IN}=H	ACTIVE
L	22-22V	L	L	CHIP ERASE	D_{IN}=H	ACTIVE

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprogramming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	-	Unlimited			

NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

PIN FUNCTIONS

Symbol	Function	Comments
A0-A7	8 Bit Address	The address inputs select one of the EEPROM 8-bit words.
D0-D7	8 Bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	This input enables the chip for all modes of operation. When chip enable is high, the I/O terminals are in the floating or high impedance state.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprogramming cycle; input data latched on a positive edge.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprogramming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt Power Connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless other noted)

V_{SS} = GND
V_{CC} = +5V ±10%
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

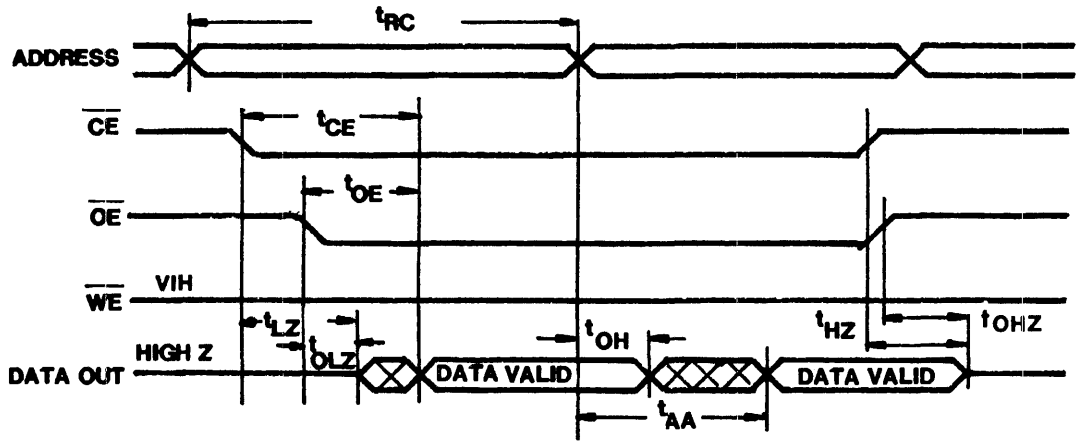
DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-1.0	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
Input Leakage Current	I_{IL}	-		10	µA	V_{IN} = 5.5V
Output Leakage Current	I_{OL}			10	µA	V_{IN} = 5.5V
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	60	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	-	50	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	330	440	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	-	275	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

FIGURE 1: READ MODE



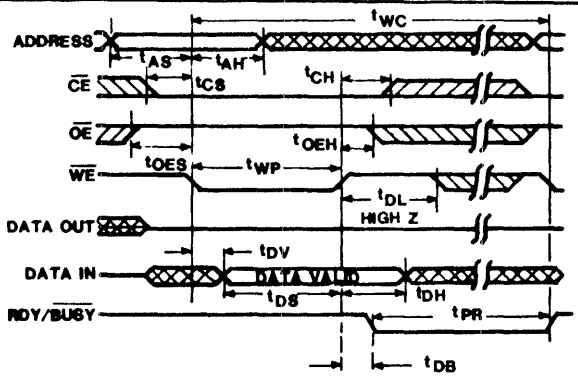
READ MODE	Sym	Min	Typ	Max	Unit	Conditions
Read Cycle Time	t_{RC}	300	-	-	ns	
Chip Enable Access Time	t_{CE}	-	-	300	ns	
Address Access Time	t_{AA}	-	-	300	ns	
Output Enable Access Time	t_{OE}	-	-	100	ns	
Chip Enable to Output Low Z	t_{LZ}	10	-	-	ns	
Chip Disable to Output in High Z	t_{HZ}	10	-	100	ns	
Output Enable to Output in Low Z	t_{OLZ}	50	-	-	ns	
Output Enable to Output in High Z	t_{OHZ}	10	-	100	ns	
Output Hold From Address Change	t_{OH}	20	-	-	ns	

READ MODE

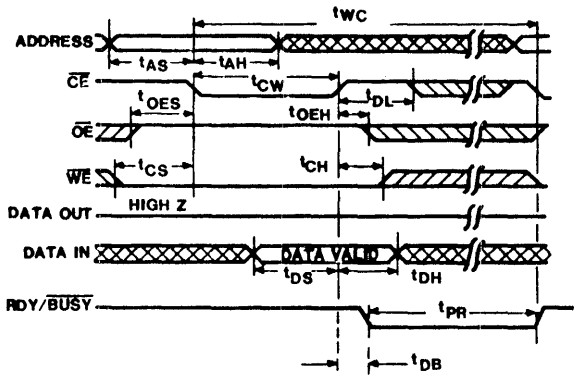
To initiate a read cycle, a valid address must appear on the A0 to A7 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will appear on the data lines D0 to D7 after a time delay t_{CE} measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 300 ns and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$ or an address line. $\overline{WE}$ is held high.

FIGURE 2: PROGRAM MODE

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



PROGRAM MODE	Sym	Min	Typ	Max	Unit	Conditions
Write Cycle Time	t_{WC}	20	-	40	ms	
Address Setup Time	t_{AS}	10	-	-	ns	
Address Hold Time	t_{AH}	70	-	-	ns	
Write Setup Time	t_{CS}	0	-	-	ns	
Write Hold Time	t_{CH}	0	-	-	ns	
Chip Enable to End of Write Input	t_{CW}	150	-	-	ns	
Output Enable Setup Time	t_{OES}	10	-	-	ns	
Output Enable Hold Time	t_{OEH}	10	-	-	ns	
Write Pulse Width	t_{WP}	150	-	-	ns	
Data Latch Time	t_{DL}	50	-	-	ns	
Programming Time	t_{PR}	20	-	40	ms	
Data Setup Time	t_{DS}	50	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
RDY/$\overline{BUSY}$	t_{DB}	-	-	100	ns	

WE CONTROLLED PROGRAM MODE

With a stable address and data word presented to the respective inputs of a selected device and $\overline{CE}$ of that device brought low, the $\overline{WE}$ line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$ latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

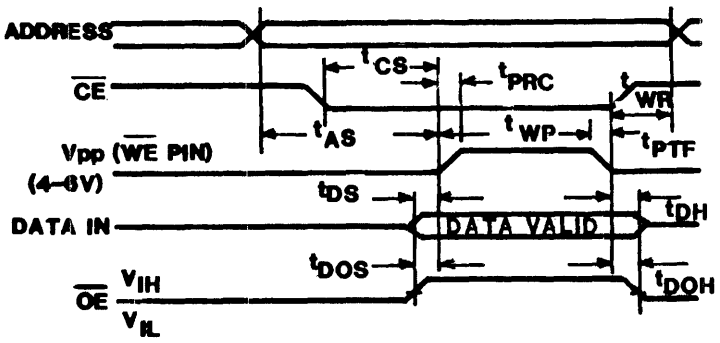
CE CONTROLLED PROGRAM MODE

In this mode, $\overline{WE}$ is brought low prior to selecting the ER5902. The falling and rising edges of the $\overline{CE}$ line will then latch the address and data respectively. A delay t_{DB} is timed from the rising edge of the $\overline{WE}$ line following which the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

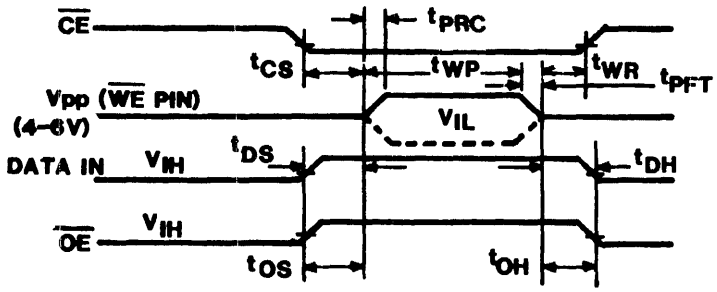
DS20029A-5

FIGURE 3: OPTIONAL HIGH VOLTAGE MODES

BYTE ERASE OR BYTE WRITE CYCLE



CHIP ERASE CYCLE



DC CHARACTERISTICS

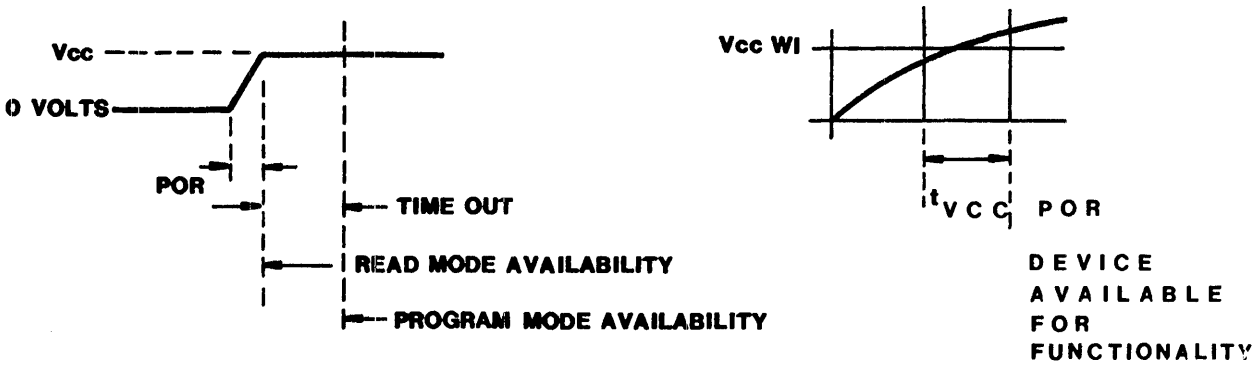
OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Write/Erase Voltage	V_{PP}	20	-	22	V	
V_{PP} Current (Byte Erase/Write)	I_{PP} (w)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $V_{PP}=22V$
$\overline{OE}$ Voltage (Chip Erase)	V_{OE}	20	-	22	V	$I_{OE}=10\mu A$
V_{PP} Current Inhibit	I_{PP} (i)	-	-	0.01	mA	$\overline{CE}=V_{IH}$, $V_{PP}=22V$
V_{PP} Current (Chip Erase)	I_{PP} (c)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{OE}$, $V_{PP}=22V$

AC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Add to V_{PP} Setup Time	t_{AS}	10	-	-	ns	
$\overline{CE}$ to V_{PP} Setup Time	t_{CS}	10	-	-	ns	
Data to V_{PP} Setup Time	t_{DS}	0	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	ns	$V_{PP}=6V$
Write Pulse Width	t_{WP}	150ns	-	15ms		
Write Recovery Time	t_{WR}	50	-	-	ns	$V_{PP}=6V$
Chip Erase Setup Time	t_{OS}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
Chip Erase Hold Time	t_{OH}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
V_{PP} RC Time Constant	t_{PRC}	-	-	750	µs	
V_{PP} Fall Time	t_{PFT}	-	-	100	us	$V_{PP}=6V$
Byte Erase/Write Setup Time	t_{BOS}	10	-	-	ns	$V_{PP}=6V$
Byte Erase/Write Hold Time	t_{BOH}	10	-	-	ns	$V_{PP}=6V$

DS20029A-6

FIGURE 4: ON CHIP DATA PROTECTION



ENHANCED ON-CHIP DATA PROTECTION

This protection circuitry minimizes the possibility of erronious program/eral cycles during device power up or down. When the power supply voltage, V_{CC} is below 3.5V, V_{CC} WI, (power up or down), the chip is held in a reset mode inhibiting all erase/write circuitry. On power up, after V_{CC} reaches the 3.5V level, a 10ms time out, t_{VCC}, will start during which the erase/write circuitry remains inhibited. This allows time for setting of inputs to the correct state. Additionally, a low state on $\overline{OE}$ will inhibit erase/write operations.

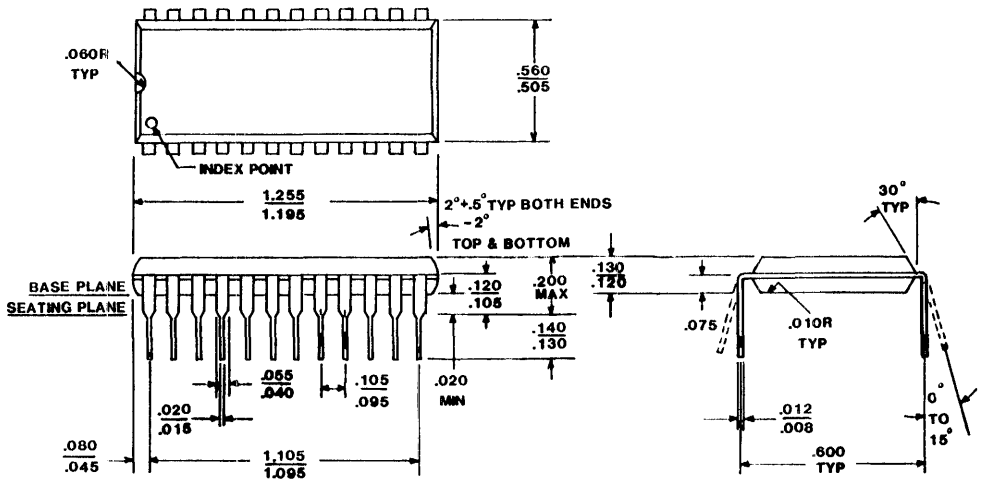
Read operations are not inhibited by the 10ms time out and may occur during this period.

OPTIONAL HIGH VOLTAGE PROGRAMMING AND CHIP ERASE FEATURES

Optional high voltage word erase, word write and 10ms chip erase features are available on the ER5902 (in addition to full +5V only operation) for pin-for-pin and operational compatibility with EEPROMs requiring additional high voltage power supplies.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

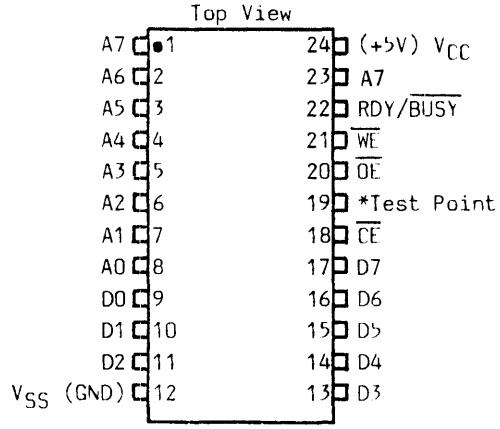
WORD ALTERABLE 2048 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 2048 bits, organized 256 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Automatic write timeout
- RDY/$\overline{\text{BUSY}}$ signal
- Optional high voltage program and chip erase modes
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ inputs to avoid bus contention
- Word alterable
- Read access time of less than 300ns
- Enhanced on-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pinout
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

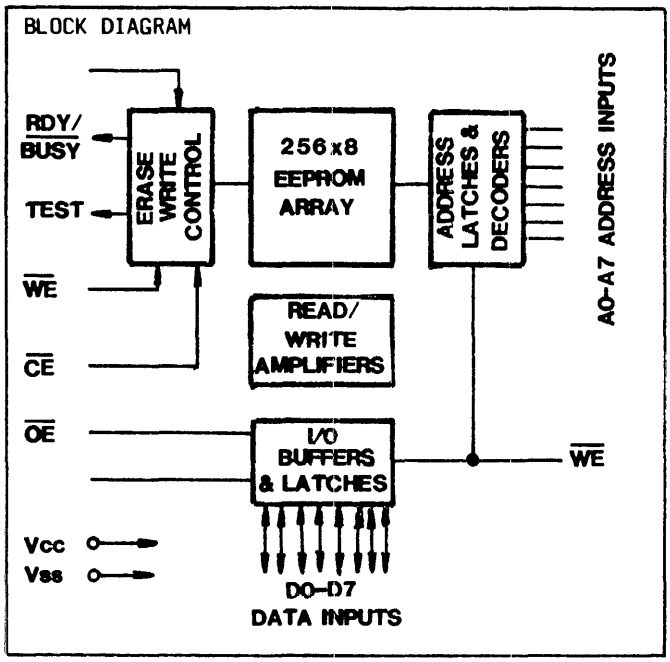


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5902I is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5902I can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5902I is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{\text{BUSY}}$ signal is available, the ER5902I frees the system for other tasks during the programming cycle. The read/write logic is designed such that bus contention will be minimized by use of $\overline{\text{OE}}$ and $\overline{\text{CE}}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

+5V ONLY OPERATION						
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	RDY/$\overline{\text{BUSY}}$	MODE	I/O	POWER
H	X	X	H	STANDBY	High Z	STANDBY
L	L	H	H	READ	D_{OUT}	ACTIVE
L	H	⌐	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	H	READ/WRITE INHIBIT	High Z	ACTIVE

OPTIONAL HIGH VOLTAGE COMPATIBLE MODES						
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	RDY/$\overline{\text{BUSY}}$	MODE	I/O	POWER
L	H	20-22V	L	BYTE ERASE	D_W=H	ACTIVE
L	H	20-22V	L	BYTE ERASE	D_W	ACTIVE
L	20-22V	20-22V	L	CHIP ERASE	D_{IN}=H	ACTIVE
L	22-22V	L	L	CHIP ERASE	D_{IN}=H	ACTIVE

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprogramming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	-	Unlimited			

NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

PIN FUNCTIONS

Symbol	Function	Comments
A0-A7	8 Bit Address	The address inputs select one of the EEPROM 8-bit words.
D0-D7	8 Bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	This input enables the chip for all modes of operation. When chip enable is high, the I/O terminals are in the floating or high impedance state.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprogramming cycle; input data latched on a positive edge.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprogramming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt Power Connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless other noted)

V_{SS} = GND
V_{CC} = +5V ±10%
Operating Temperature Range (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

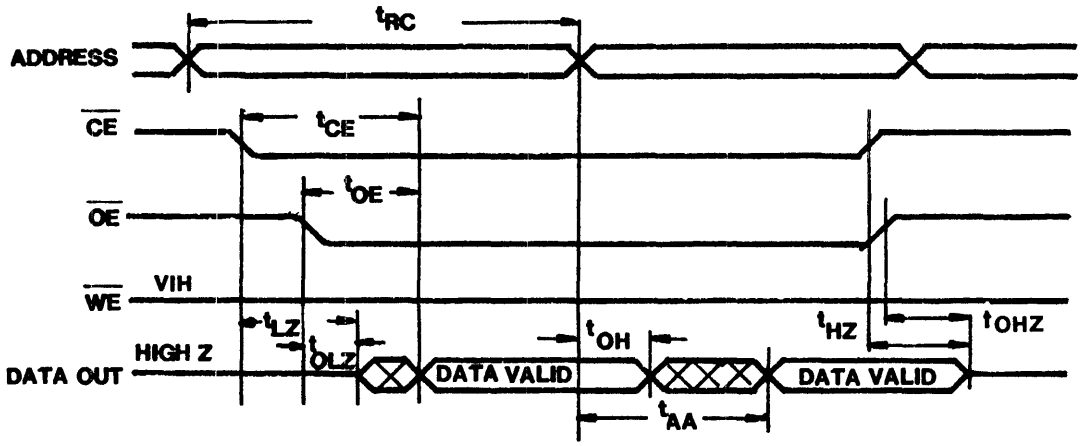
DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-1.0	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
Input Leakage Current	I_{IL}	-		10	µA	V_{IN} = 5.5V
Output Leakage Current	I_{OL}			10	µA	V_{IN} = 5.5V
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	60	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	-	50	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	330	440	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	-	275	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

FIGURE 1: READ MODE



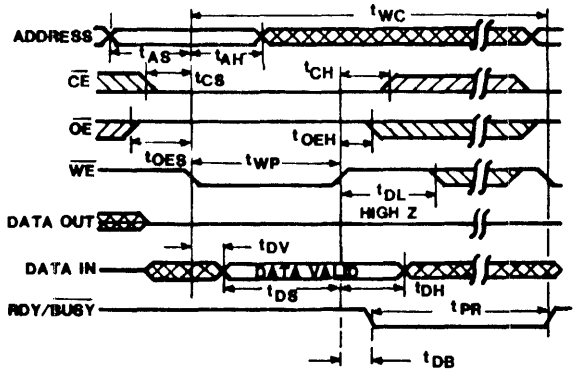
READ MODE	Sym	Min	Typ	Max	Unit	Conditions
Read Cycle Time	t_{RC}	300	-	-	ns	
Chip Enable Access Time	t_{CE}	-	-	300	ns	
Address Access Time	t_{AA}	-	-	300	ns	
Output Enable Access Time	t_{OE}	-	-	100	ns	
Chip Enable to Output Low Z	t_{LZ}	10	-	-	ns	
Chip Disable to Output in High Z	t_{HZ}	10	-	100	ns	
Output Enable to Output in Low Z	t_{OLZ}	50	-	-	ns	
Output Enable to Output in High Z	t_{OHZ}	10	-	100	ns	
Output Hold From Address Change	t_{OH}	20	-	-	ns	

READ MODE

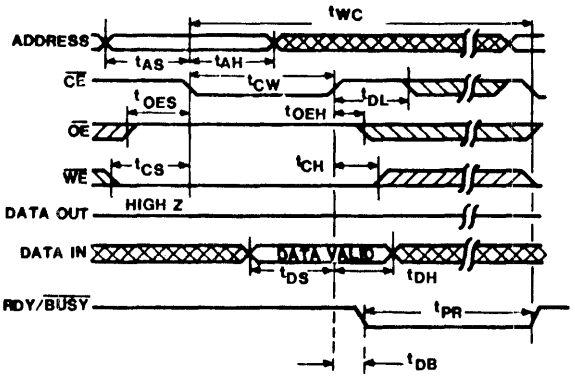
To initiate a read cycle, a valid address must appear on the A0 to A7 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will appear on the data lines D0 to D7 after a time delay t_{CE} measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 300 ns and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$ or an address line. $\overline{WE}$ is held high.

FIGURE 2: PROGRAM MODE

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



PROGRAM MODE	Sym	Min	Typ	Max	Unit	Conditions
Write Cycle Time	t_{WC}	20	-	40	ms	
Address Setup Time	t_{AS}	10	-	-	ns	
Address Hold Time	t_{AH}	70	-	-	ns	
Write Setup Time	t_{CS}	0	-	-	ns	
Write Hold Time	t_{CH}	0	-	-	ns	
Chip Enable to End of Write Input	t_{CW}	150	-	-	ns	
Output Enable Setup Time	t_{OES}	10	-	-	ns	
Output Enable Hold Time	t_{OEH}	10	-	-	ns	
Write Pulse Width	t_{WP}	150	-	-	ns	
Data Latch Time	t_{DL}	50	-	-	ns	
Programming Time	t_{PR}	20	-	40	ms	
Data Setup Time	t_{DS}	50	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
RDY/$\overline{BUSY}$	t_{DB}	-	-	100	ns	

WE CONTROLLED PROGRAM MODE

With a stable address and data word presented to the respective inputs of a selected device and $\overline{CE}$ of that device brought low, the $\overline{WE}$ line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$ latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

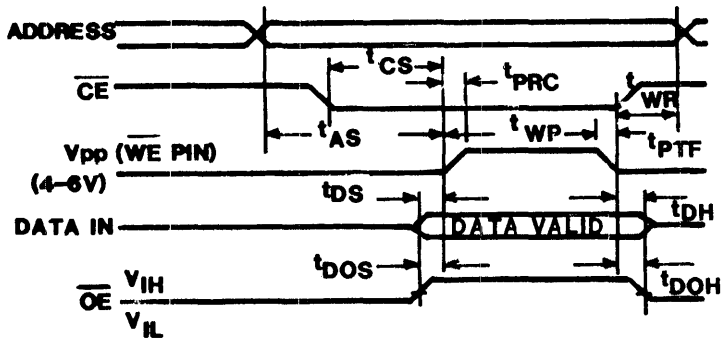
CE CONTROLLED PROGRAM MODE

In this mode, $\overline{WE}$ is brought low prior to selecting the ER5902I. The falling and rising edges of the $\overline{CE}$ line will then latch the address and data respectively. A delay t_{DB} is timed from the rising edge of the $\overline{WE}$ line following which the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

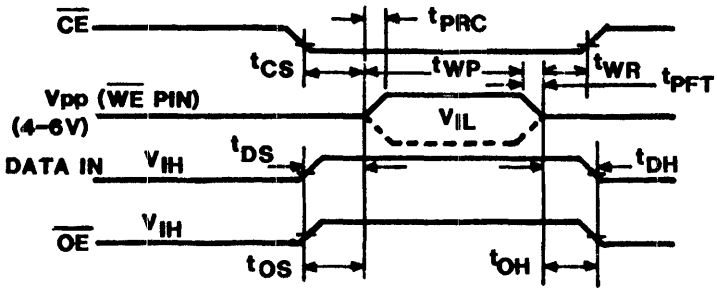
DS20030A-5

FIGURE 3: OPTIONAL HIGH VOLTAGE MODES

BYTE ERASE OR BYTE WRITE CYCLE



CHIP ERASE CYCLE



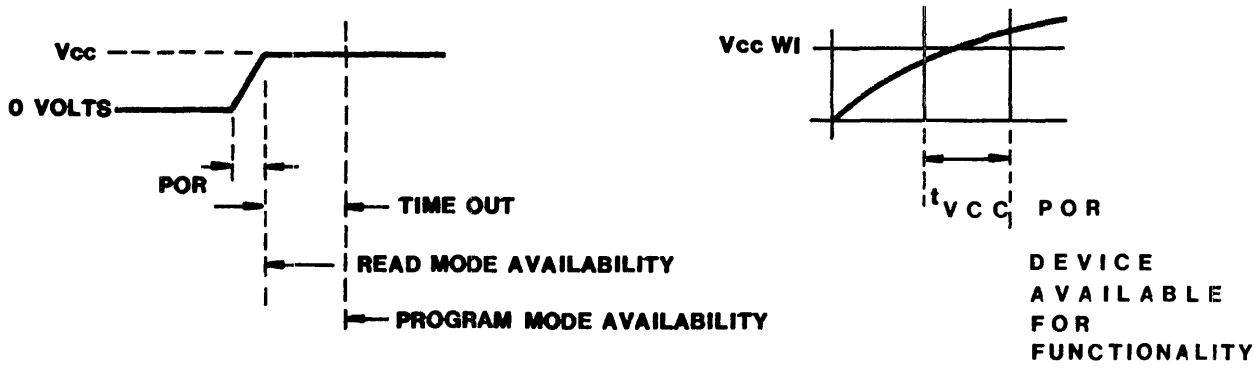
DC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Write/Erase Voltage	V_{PP}	20	-	22	V	
V_{PP} Current (Byte Erase/Write)	I_{PP} (w)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $V_{PP}=22V$
$\overline{OE}$ Voltage (Chip Erase)	V_{OE}	20	-	22	V	$I_{OE}=10\mu A$
V_{PP} Current Inhibit	I_{PP} (i)	-	-	0.01	mA	$\overline{CE}=V_{IH}$, $V_{PP}=22V$
V_{PP} Current (Chip Erase)	I_{PP} (c)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{OE}$, $V_{PP}=22V$

AC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Add to V_{PP} Setup Time	t_{AS}	10	-	-	ns	
$\overline{CE}$ to V_{PP} Setup Time	t_{CS}	10	-	-	ns	
Data to V_{PP} Setup Time	t_{DS}	0	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	ns	$V_{PP}=6V$
Write Pulse Width	t_{WP}	150ns	-	15ms		
Write Recovery Time	t_{WR}	50	-	-	ns	$V_{PP}=6V$
Chip Erase Setup Time	t_{OS}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
Chip Erase Hold Time	t_{OH}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
V_{PP} RC Time Constant	t_{PRC}	-	-	750	µs	
V_{PP} Fall Time	t_{PFT}	-	-	100	us	$V_{PP}=6V$
Byte Erase/Write Setup Time	t_{BOS}	10	-	-	ns	$V_{PP}=6V$
Byte Erase/Write Hold Time	t_{BOH}	10	-	-	ns	$V_{PP}=6V$

FIGURE 4: ON CHIP DATA PROTECTION



ENHANCED ON-CHIP DATA PROTECTION

This protection circuitry minimizes the possibility of erronious program/eral cycles during device power up or down. When the power supply voltage, V_{CC} is below 3.5V, V_{CC} WI, (power up or down), the chip is held in a reset mode inhibiting all erase/write circuitry. On power up, after V_{CC} reaches the 3.5V level, a 10ms time out, t_{VCC} will start during which the erase/write circuitry remains inhibited. This allows time for setting of inputs to the correct state. Additionally, a low state on $\overline{OE}$ will inhibit erase/write operations.

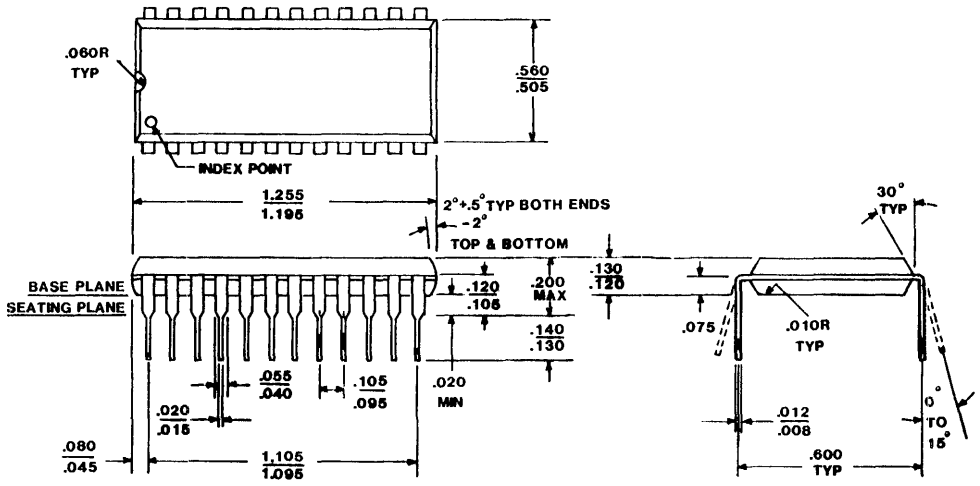
Read operations are not inhibited by the 10ms time out and may occur during this period.

OPTIONAL HIGH VOLTAGE PROGRAMMING AND CHIP ERASE FEATURES

Optional high voltage word erase, word write and 10ms chip erase features are available on the ER5902I (in addition to full +5V only operation) for pin-for-pin and operational compatibility with EEPROMs requiring additional high voltage power supplies.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

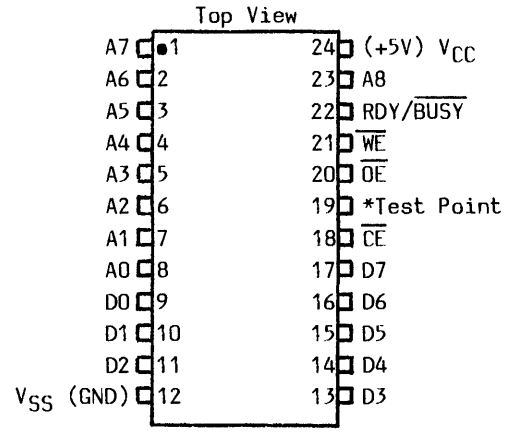
WORD ALTERABLE 4096 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 4096 bits, organized 512 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Automatic write timeout
- RDY/$\overline{BUSY}$ signal
- Optional high voltage program and chip erase modes
- $\overline{CE}$ and $\overline{OE}$ inputs to avoid bus contention
- Word alterable
- Read access time of less than 300ns
- Enhanced on-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pinout
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

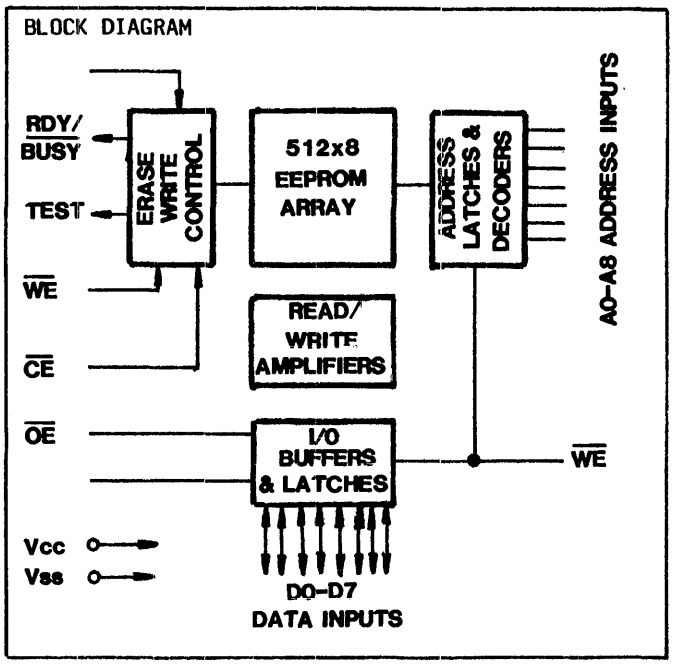


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5904 is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5904 can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5904 is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{BUSY}$ signal is available, the ER5904 frees the system for other tasks during the programming cycle. The read/write logic is designed such that bus contention will be minimized by use of $\overline{OE}$ and $\overline{CE}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

+5V ONLY OPERATION						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
H	X	X	H	STANDBY	High Z	STANDBY
L	L	H	H	READ	D_{OUT}	ACTIVE
L	H	⌐⌊	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	H	READ/WRITE INHIBIT	High Z	ACTIVE

OPTIONAL HIGH VOLTAGE COMPATIBLE MODES						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
L	H	20-22V	L	BYTE ERASE	D_W=H	ACTIVE
L	H	20-22V	L	BYTE ERASE	D_W	ACTIVE
L	20-22V	20-22V	L	CHIP ERASE	D_{IN}=H	ACTIVE
L	22-22V	L	L	CHIP ERASE	D_{IN}=H	ACTIVE

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprogramming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	-	Unlimited			

NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

PIN FUNCTIONS

Symbol	Function	Comments
A0-A8	9 Bit Address	The address inputs select one of the EEPROM 8-bit words.
D0-D7	8 Bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	This input enables the chip for all modes of operation. When chip enable is high, the I/O terminals are in the floating or high impedance state.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprogramming cycle; input data latched on a positive edge.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprogramming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt Power Connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless other noted)

V_{SS} = GND
V_{CC} = +5V ±10%
Operating Temperature Range (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

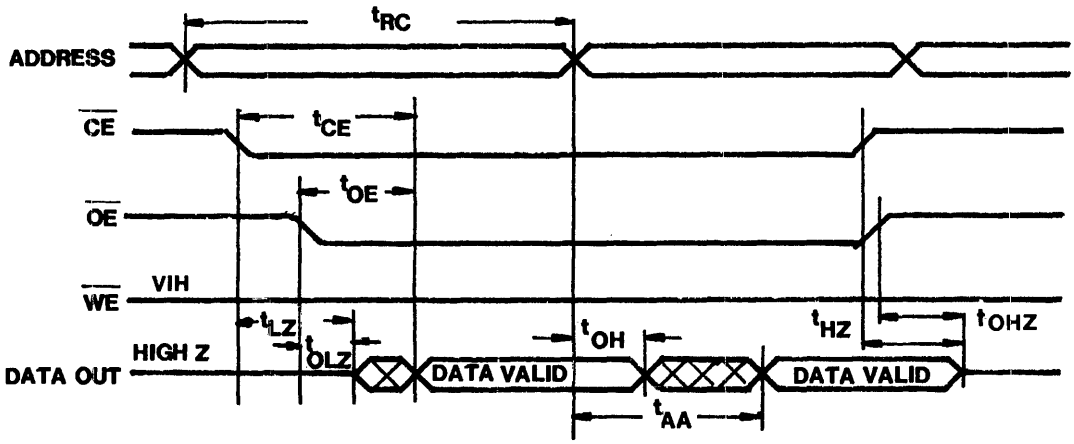
DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-1.0	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
Input Leakage Current	I_{IL}	-		10	µA	V_{IN} = 5.5V
Output Leakage Current	I_{OL}			10	µA	V_{IN} = 5.5V
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	60	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	-	50	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	330	440	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	-	275	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

FIGURE 1: READ MODE



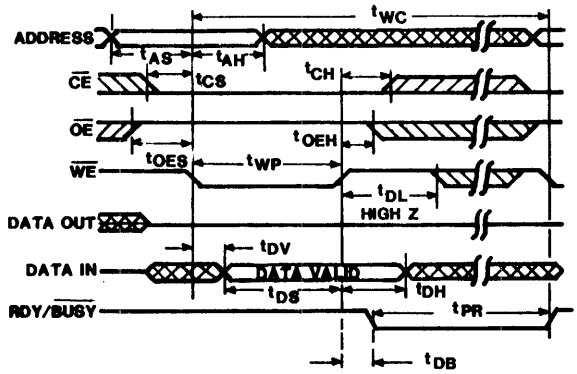
READ MODE	Sym	Min	Typ	Max	Unit	Conditions
Read Cycle Time	t_{RC}	300	-	-	ns	
Chip Enable Access Time	t_{CE}	-	-	300	ns	
Address Access Time	t_{AA}	-	-	300	ns	
Output Enable Access Time	t_{OE}	-	-	100	ns	
Chip Enable to Output Low Z	t_{LZ}	10	-	-	ns	
Chip Disable to Output in High Z	t_{HZ}	10	-	100	ns	
Output Enable to Output in Low Z	t_{OLZ}	50	-	-	ns	
Output Enable to Output in High Z	t_{OHZ}	10	-	100	ns	
Output Hold From Address Change	t_{OH}	20	-	-	ns	

READ MODE

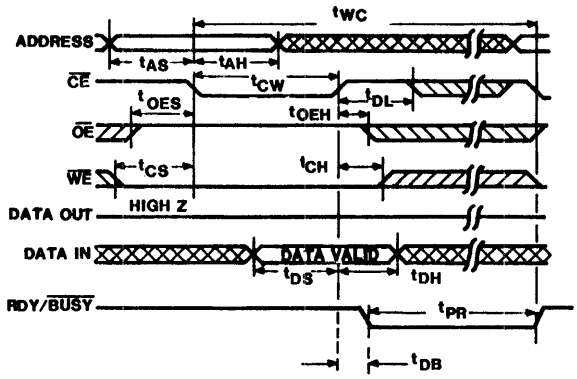
To initiate a read cycle, a valid address must appear on the A0 to A8 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will appear on the data lines D0 to D7 after a time delay t_{CE} measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 300 ns and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$ or an address line. $\overline{WE}$ is held high.

FIGURE 2: PROGRAM MODE

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



PROGRAM MODE	Sym	Min	Typ	Max	Unit	Conditions
Write Cycle Time	t_{WC}	20	-	40	ms	
Address Setup Time	t_{AS}	10	-	-	ns	
Address Hold Time	t_{AH}	70	-	-	ns	
Write Setup Time	t_{CS}	0	-	-	ns	
Write Hold Time	t_{CH}	0	-	-	ns	
Chip Enable to End of Write Input	t_{CW}	150	-	-	ns	
Output Enable Setup Time	t_{OES}	10	-	-	ns	
Output Enable Hold Time	t_{OEH}	10	-	-	ns	
Write Pulse Width	t_{WP}	150	-	-	ns	
Data Latch Time	t_{DL}	50	-	-	ns	
Programming Time	t_{PR}	20	-	40	ms	
Data Setup Time	t_{DS}	50	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
RDY/$\overline{BUSY}$	t_{DB}	-	-	100	ns	

WE CONTROLLED PROGRAM MODE

With a stable address and data word presented to the respective inputs of a selected device and $\overline{CE}$ of that device brought low, the $\overline{WE}$ line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$ latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

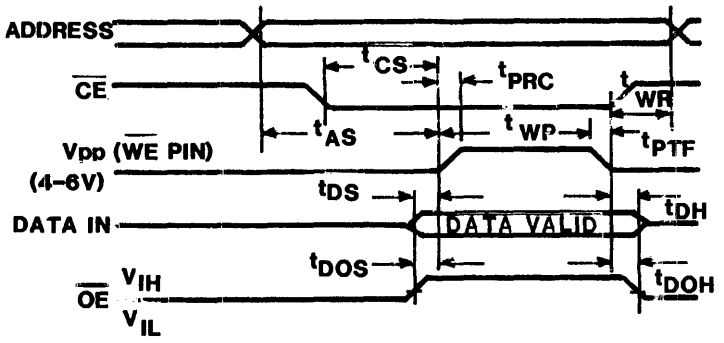
CE CONTROLLED PROGRAM MODE

In this mode, $\overline{WE}$ is brought low prior to selecting the ER5904. The falling and rising edges of the $\overline{CE}$ line will then latch the address and data respectively. A delay t_{DB} is timed from the rising edge of the $\overline{WE}$ line following which the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

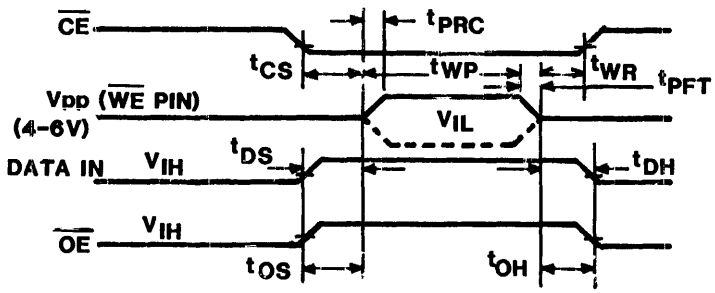
GENERAL INSTRUMENT	ER5904

FIGURE 3: OPTIONAL HIGH VOLTAGE MODES

BYTE ERASE OR BYTE WRITE CYCLE



CHIP ERASE CYCLE



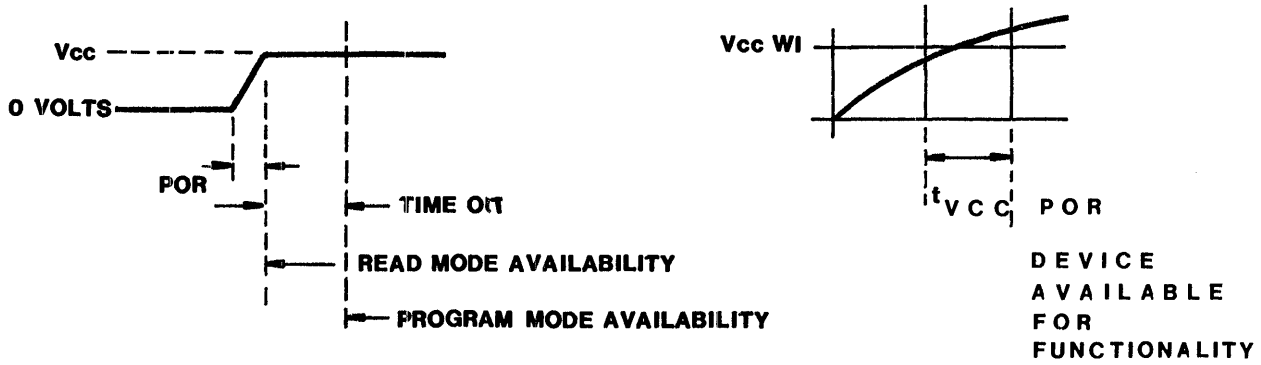
DC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Write/Erase Voltage	V_{PP}	20	-	22	V	
V_{PP} Current (Byte Erase/Write)	I_{PP} (w)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $V_{PP}=22V$
$\overline{OE}$ Voltage (Chip Erase)	V_{OE}	20	-	22	V	$I_{OE}=10\mu A$
V_{PP} Current Inhibit	I_{PP} (i)	-	-	0.01	mA	$\overline{CE}=V_{IH}$, $V_{PP}=22V$
V_{PP} Current (Chip Erase)	I_{PP} (c)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{OE}$, $V_{PP}=22V$

AC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Add to V_{PP} Setup Time	t_{AS}	10	-	-	ns	
$\overline{CE}$ to V_{PP} Setup Time	t_{CS}	10	-	-	ns	
Data to V_{PP} Setup Time	t_{DS}	0	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	ns	$V_{PP}=6V$
Write Pulse Width	t_{WP}	150ns	-	15ms		
Write Recovery Time	t_{WR}	50	-	-	ns	$V_{PP}=6V$
Chip Erase Setup Time	t_{OS}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
Chip Erase Hold Time	t_{OH}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
V_{PP} RC Time Constant	t_{PRC}	-	-	750	μs	
V_{PP} Fall Time	t_{PFT}	-	-	100	us	$V_{PP}=6V$
Byte Erase/Write Setup Time	t_{BOS}	10	-	-	ns	$V_{PP}=6V$
Byte Erase/Write Hold Time	t_{BOH}	10	-	-	ns	$V_{PP}=6V$

FIGURE 4: ON CHIP DATA PROTECTION



ENHANCED ON-CHIP DATA PROTECTION

This protection circuitry minimizes the possibility of erronious program/eral cycles during device power up or down. When the power supply voltage, V_{CC} is below 3.5V, V_{CC} WI, (power up or down), the chip is held in a reset mode inhibiting all erase/write circuitry. On power up, after V_{CC} reaches the 3.5V level, a 10ms time out, t_{VCC}, will start during which the erase/write circuitry remains inhibited. This allows time for setting of inputs to the correct state. Additionally, a low state on $\overline{OE}$ will inhibit erase/write operations.

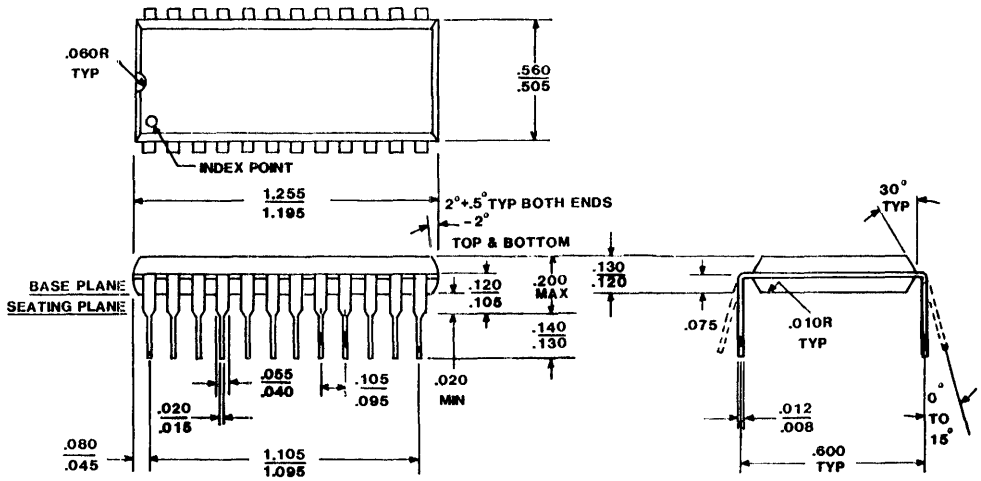
Read operations are not inhibited by the 10ms time out and may occur during this period.

OPTIONAL HIGH VOLTAGE PROGRAMMING AND CHIP ERASE FEATURES

Optional high voltage word erase, word write and 10ms chip erase features are available on the ER5904 (in addition to full +5V only operation) for pin-for-pin and operational compatibility with EEPROMs requiring additional high voltage power supplies.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

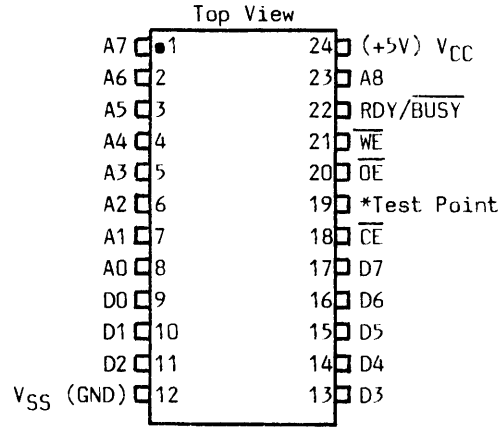
WORD ALTERABLE 4096 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 4096 bits, organized 512 x 8
- Single +5V only operation
- On-chip latching of addresses and data
- Automatic write timeout
- RDY/$\overline{BUSY}$ signal
- Optional high voltage program and chip erase modes
- $\overline{CE}$ and $\overline{OE}$ inputs to avoid bus contention
- Word alterable
- Read access time of less than 300ns
- Enhanced on-chip data protection
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL STD 883
- JEDEC approved byte-wide pinout
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word

PIN CONFIGURATION

24 LEAD DUAL-IN-LINE

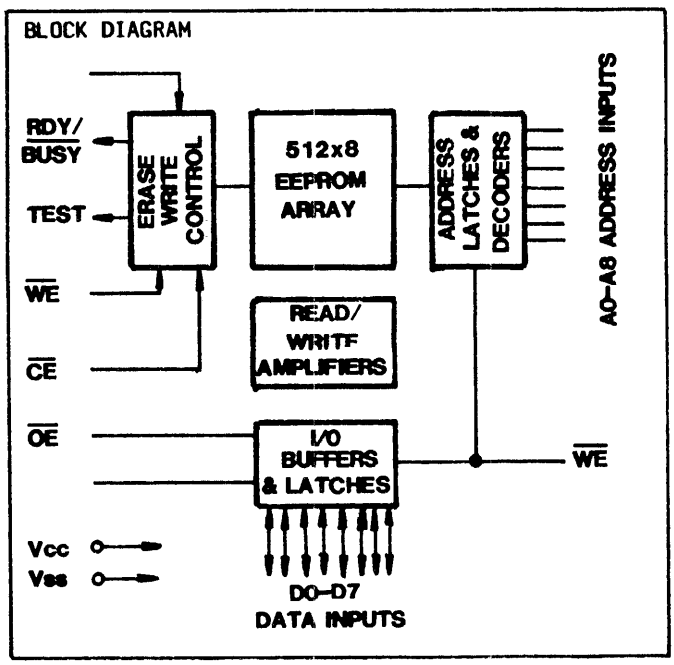


*Must be left unconnected.

DESCRIPTION

The General Instrument ER5904I is an Electrically Erasable Programmable Read Only Memory (EEPROM) with many ease of use features. The ER5904I can be modified using simple TTL level signals and a single +5V power supply. Writing data into the ER5904I is analogous to writing data in a static RAM. Since the address and data are internally latched and the RDY/$\overline{BUSY}$ signal is available, the ER5904I frees the system for other tasks during the programming cycle. The read/write logic is designed such that bus contention will be minimized by use of $\overline{OE}$ and $\overline{CE}$ inputs.

BLOCK DIAGRAM



TRUTH TABLE

+5V ONLY OPERATION						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
H	X	X	H	STANDBY	High Z	STANDBY
L	L	H	H	READ	D_{OUT}	ACTIVE
L	H	⊓	L	PROGRAM	D_{IN}	ACTIVE
L	H	H	H	READ/WRITE INHIBIT	High Z	ACTIVE

OPTIONAL HIGH VOLTAGE COMPATIBLE MODES						
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{BUSY}$	MODE	I/O	POWER
L	H	20-22V	L	BYTE ERASE	D_W=H	ACTIVE
L	H	20-22V	L	BYTE ERASE	D_W	ACTIVE
L	20-22V	20-22V	L	CHIP ERASE	D_{IN}=H	ACTIVE
L	22-22V	L	L	CHIP ERASE	D_{IN}=H	ACTIVE

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	-	V_{IH}, V_{OH}	-	V	
Written State	V_W	-	V_{IH}, V_{OL}	-	V	
Data Retention Time (powered or unpowered)	t_S	10	-		years	
Number of reprogramming cycles per byte	N_P	10^4	-	-	-	See note below
Number of Read Access between refresh	N_{RA}	-	Unlimited			

NOTE: There is a tradeoff to be made between the data retention time (t_S) and the number of reprogramming cycles (N_P) performed per address. A gradual reduction in retention time is experienced as the number of reprogramming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. General Instrument's SNOS EEPROMs are designed so that after 10^4 cycles a typical retention time is 10 years.

PIN FUNCTIONS

Symbol	Function	Comments
A0-A8	9 Bit Address	The address inputs select one of the EEPROM 8-bit words.
D0-D7	8 Bit Data I/O	
V_{SS}	Chip Ground Connection	
$\overline{CE}$	Chip Enable Input	This input enables the chip for all modes of operation. When chip enable is high, the I/O terminals are in the floating or high impedance state.
$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
$\overline{WE}$	Write Enable Input	Enables a reprogramming cycle; input data latched on a positive edge.
RDY/$\overline{BUSY}$	Status Output	Low when chip is in reprogramming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt Power Connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground..... +7V to -0.3V
Storage temperature (unpowered and without data retention)..... -65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

Standard Conditions (unless other noted)

V_{SS} = GND
V_{CC} = +5V ±10%
Operating Temperature Range (T_A):
-40°C to +85°C (Industrial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data Labelled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software

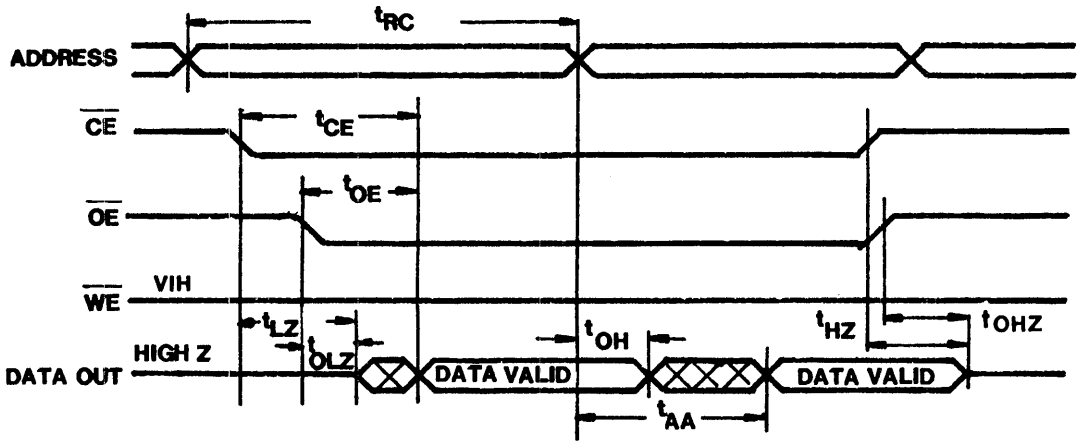
DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V	
Low Level Input Voltage	V_{IL}	-1.0	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = -400 µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
Input Leakage Current	I_{IL}	-		10	µA	V_{IN} = 5.5V
Output Leakage Current	I_{OL}			10	µA	V_{IN} = 5.5V
POWER SUPPLY REQUIREMENTS						
V_{CC} Supply:						
Chip Selected	I_{CC}	-	70	-	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	-	40	-	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	-	385	-	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	-	220	-	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristic	Sym	Max	Typ	Max	Units	Conditions
Input Capacitance	C_I	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_O	-	-	10	pF	V_{OUT} = 0V

FIGURE 1: READ MODE



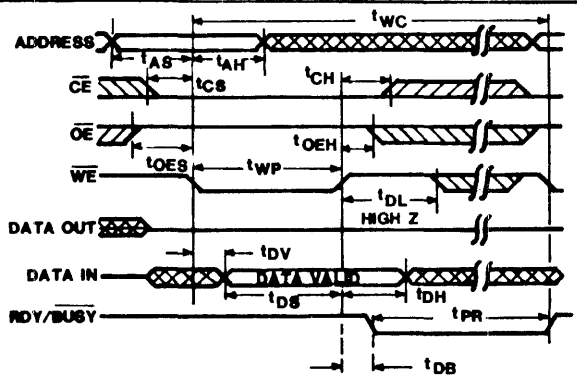
READ MODE	Sym	Min	Typ	Max	Unit	Conditions
Read Cycle Time	t_{RC}	300	-	-	ns	
Chip Enable Access Time	t_{CE}	-	-	300	ns	
Address Access Time	t_{AA}	-	-	300	ns	
Output Enable Access Time	t_{OE}	-	-	100	ns	
Chip Enable to Output Low Z	t_{LZ}	10	-	-	ns	
Chip Disable to Output in High Z	t_{HZ}	10	-	100	ns	
Output Enable to Output in Low Z	t_{OLZ}	50	-	-	ns	
Output Enable to Output in High Z	t_{OHZ}	10	-	100	ns	
Output Hold From Address Change	t_{OH}	20	-	-	ns	

READ MODE

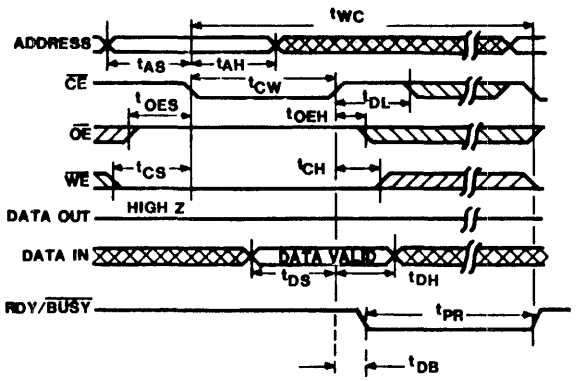
To initiate a read cycle, a valid address must appear on the A0 to A8 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will appear on the data lines D0 to D7 after a time delay t_{CE} measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 300 ns and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$ or an address line. $\overline{WE}$ is held high.

FIGURE 2: PROGRAM MODE

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



PROGRAM MODE	Sym	Min	Typ	Max	Unit	Conditions
Write Cycle Time	t_{WC}	20	-	40	ms	
Address Setup Time	t_{AS}	10	-	-	ns	
Address Hold Time	t_{AH}	70	-	-	ns	
Write Setup Time	t_{CS}	0	-	-	ns	
Write Hold Time	t_{CH}	0	-	-	ns	
Chip Enable to End of Write Input	t_{CW}	150	-	-	ns	
Output Enable Setup Time	t_{OES}	10	-	-	ns	
Output Enable Hold Time	t_{OEH}	10	-	-	ns	
Write Pulse Width	t_{WP}	150	-	-	ns	
Data Latch Time	t_{DL}	50	-	-	ns	
Programming Time	t_{PR}	20	-	40	ms	
Data Setup Time	t_{DS}	50	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
RDY/$\overline{BUSY}$	t_{DB}	-	-	100	ns	

$\overline{WE}$ CONTROLLED PROGRAM MODE

With a stable address and data word presented to the respective inputs of a selected device and $\overline{CE}$ of that device brought low, the $\overline{WE}$ line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$ latches the address inputs and the rising edge latches the data inputs. After a delay t_{DB}, the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

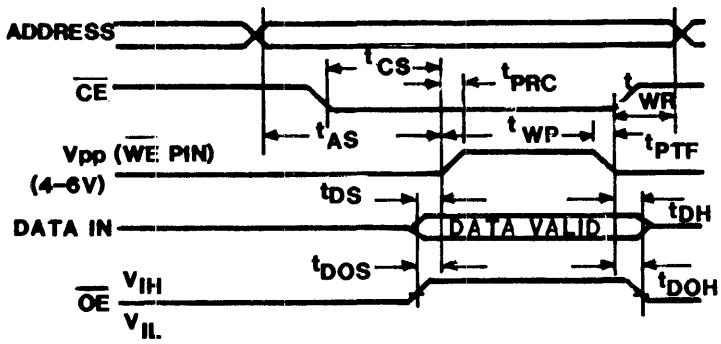
CE CONTROLLED PROGRAM MODE

In this mode, $\overline{WE}$ is brought low prior to selecting the ER5904. The falling and rising edges of the $\overline{CE}$ line will then latch the address and data respectively. A delay t_{DB} is timed from the rising edge of the $\overline{WE}$ line following which the RDY/$\overline{BUSY}$ output will go low and remain there for the duration of the programming cycle.

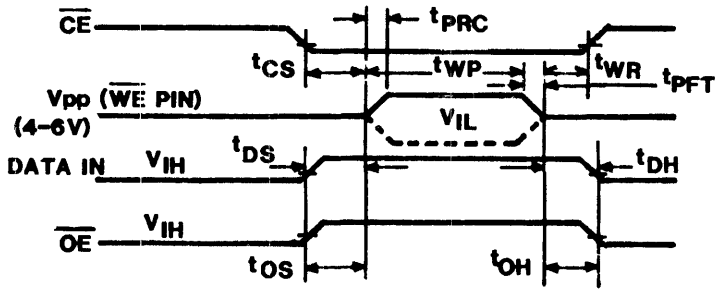
DS20027A-5

FIGURE 3: OPTIONAL HIGH VOLTAGE MODES

BYTE ERASE OR BYTE WRITE CYCLE



CHIP ERASE CYCLE



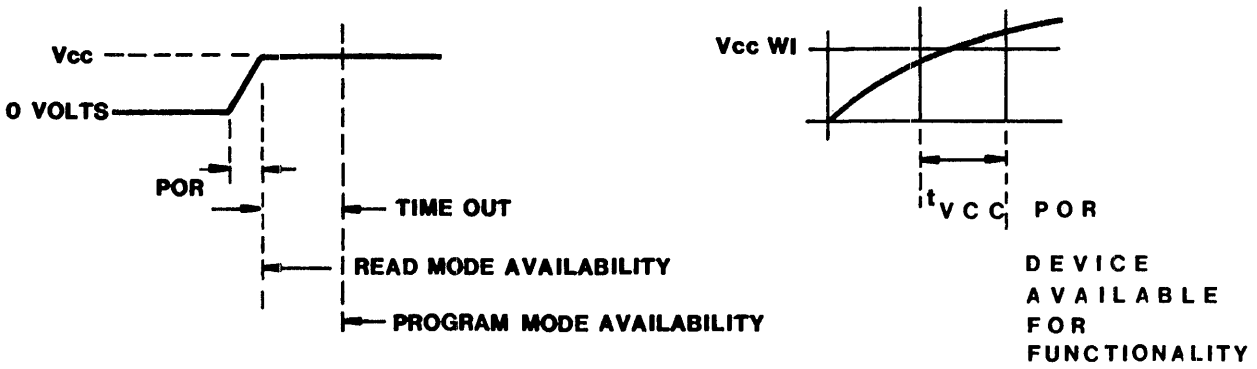
DC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Write/Erase Voltage	V_{PP}	20	-	22	V	
V_{PP} Current (Byte Erase/Write)	I_{PP} (w)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $V_{PP}=22V$
$\overline{OE}$ Voltage (Chip Erase)	V_{OE}	20	-	22	V	$I_{OE}=10\mu A$
V_{PP} Current Inhibit	I_{PP} (i)	-	-	0.01	mA	$\overline{CE}=V_{IH}$, $V_{PP}=22V$
V_{PP} Current (Chip Erase)	I_{PP} (c)	-	-	0.01	mA	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{OE}$, $V_{PP}=22V$

AC CHARACTERISTICS

OPTIONAL HIGH VOLTAGE MODES	Sym	Min	Typ	Max	Unit	Conditions
Add to V_{PP} Setup Time	t_{AS}	10	-	-	ns	
$\overline{CE}$ to V_{PP} Setup Time	t_{CS}	10	-	-	ns	
Data to V_{PP} Setup Time	t_{DS}	0	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	ns	$V_{PP}=6V$
Write Pulse Width	t_{WP}	150ns	-	15ms		
Write Recovery Time	t_{WR}	50	-	-	ns	$V_{PP}=6V$
Chip Erase Setup Time	t_{OS}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
Chip Erase Hold Time	t_{OH}	10	-	-	ns	$V_{PP}=6V$, $V_{OE}=20V$
V_{PP} RC Time Constant	t_{PRC}	-	-	750	µs	
V_{PP} Fall Time	t_{PFT}	-	-	100	us	$V_{PP}=6V$
Byte Erase/Write Setup Time	t_{BOS}	10	-	-	ns	$V_{PP}=6V$
Byte Erase/Write Hold Time	t_{BOH}	10	-	-	ns	$V_{PP}=6V$

FIGURE 4: ON CHIP DATA PROTECTION



ENHANCED ON-CHIP DATA PROTECTION

This protection circuitry minimizes the possibility of erronious program/eral cycles during device power up or down. When the power supply voltage, V_{CC} is below 3.5V, V_{CC} WI, (power up or down), the chip is held in a reset mode inhibiting all erase/write circuitry. On power up, after V_{CC} reaches the 3.5V level, a 10ms time out, t_{VCC}, will start during which the erase/write circuitry remains inhibited. This allows time for setting of inputs to the correct state. Additionally, a low state on $\overline{OE}$ will inhibit erase/write operations.

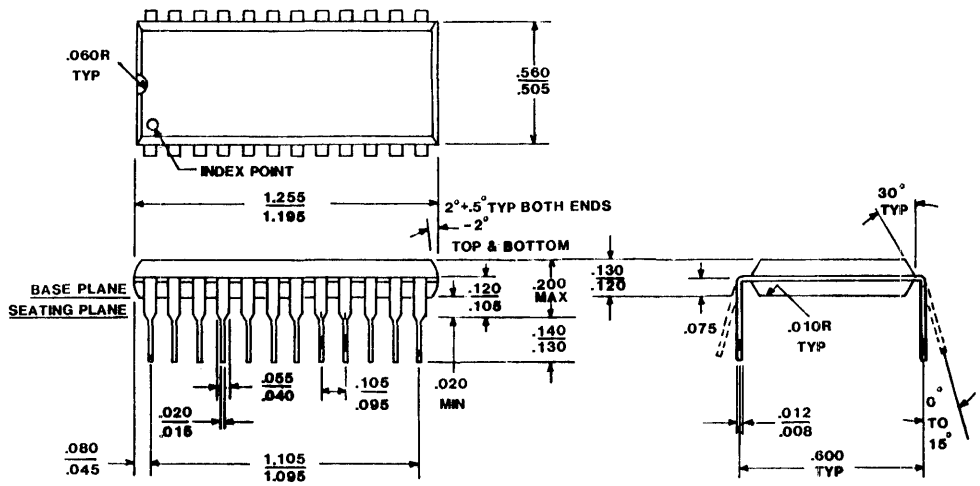
Read operations are not inhibited by the 10ms time out and may occur during this period.

OPTIONAL HIGH VOLTAGE PROGRAMMING AND CHIP ERASE FEATURES

Optional high voltage word erase, word write and 10ms chip erase features are available on the ER5904 (in addition to full +5V only operation) for pin-for-pin and operational compatibility with EEPROMs requiring additional high voltage power supplies.

PACKAGE OUTLINE

24 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

DS20027A-7

GENERAL INSTRUMENT	ER1000

NON-VOLATILE COUNTER

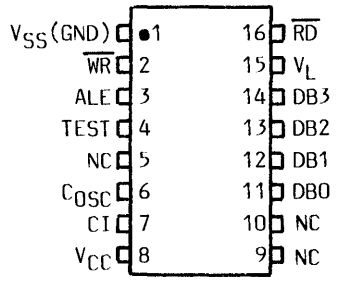
FEATURES

- Single +5 only operation
- 4-bit volatile counter
- 20-bit non-volatile counter - EEPROM
- 16-bit non-volatile scratch pad - EEPROM
- Non-volatile tamper flag - EEPROM
- 16-bit volatile counter
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range

PIN CONFIGURATION

16 LEAD DUAL IN LINE

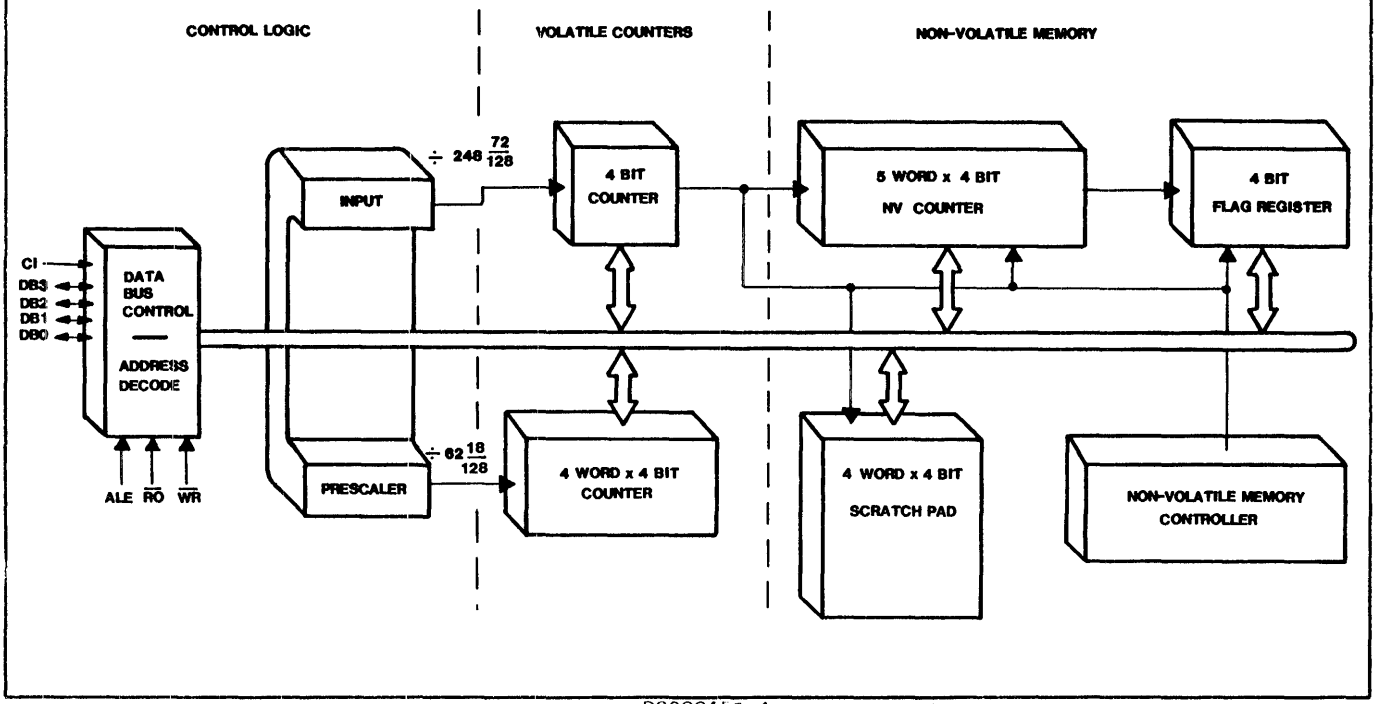
TOP VIEW



OVERVIEW

The ER1000 is a low cost, non-volatile counter manufactured in General Instrument's highly reliable SNOS technology. By incorporating both non-volatile status flags, as well as an additional user-defined, non-volatile scratch pad, the ER1000 presents a wide range of applications including RPM monitoring, determining equipment maintenance periods, measuring gas or electricity consumption in utility meters and monitoring machine on-time. The ER1000 accepts both serial (count) and parallel (scratch pad) data for storage in non-volatile memory. All words may be accessed via a 4-bit data bus.

BLOCK DIAGRAM



DS20015C-1

FUNCTIONAL DESCRIPTION

The ER1000 may be broken down into three major subsystems including two binary counter sections and a non-volatile four-word scratch pad (organized as 4-bit words). One section includes a single-word (4-bits) volatile counter, a five-word (EEPROM backed) non-volatile counter and a non-volatile, tamperproof overflow flag (flag register). The other counter section includes a four-word volatile counter. Both counter sections are incremented via either decoded count input (CI) pulses. The non-volatile, four-word scratch pad may be updated via a 4-bit multiplexed address/data bus (non-volatile scratch pad busy flag is provided). Access to all locations is achieved via this data bus.

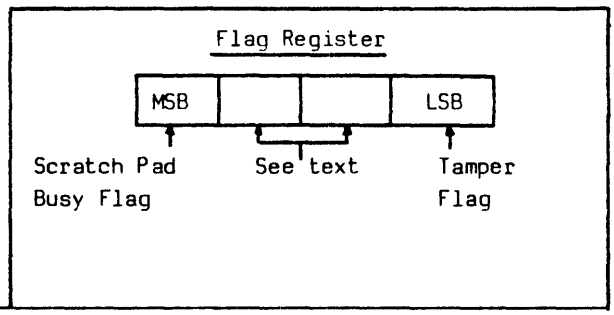
Counter Input: Input pulses occur at a rate of 0 to 1 KHz. The rise time of these transistions is limited externally to a maximum of 1 msec.

Scratch Pad Memory: 16-bits of EEPROM memory, organized 4 x 4, is accessable via the data bus at addresses C, D, E and F.

PIN FUNCTIONS

No.	Name	Comments
1	V_{SS}	System ground
2	$\overline{WR}$	Write data strobe input
3	ALE	Address latch enable input
4	Test Point	Must be left unconnected for normal operation
5	N.C.	No internal connection
6	C_{OSC}	Oscillator external capacitor C=82pf (to GND)
7	CI	Counter input
8	V_{CC}	Supply voltage
9	Test Point	Must be left unconnected for normal operation
10	Test Point	Must be left unconnected for normal operation
11	DB0	Data bus input/output, line 0
12	DB1	Data bus input/output, line 1
13	DB2	Data bus input/output, line 2
14	DB3	Data bus input/output, line 3
15	V_L	Low voltage detect input
16	$\overline{RD}$	Read data strobe input

Flag Register: The flag register is located at address A. The most significant bit is the scratch pad busy flag, which when high denotes that the scratch pad is performing a non-volatile memory programming function and should not be accessed. When the scratch pad busy flag is set and location A or any other location, B through F, are intentionally accessed the data read out will be (1010) HEX A. The least significant bit of the flag register is the tamper flag, which is set by an overflow from the most significant bit of the 20-bit non-volatile counter. However, when the scratch pad busy flag is set, the correct state of the tamper flag may not be read, since a read will always return an A as data. The remaining two bits in the flag register are always low, except when the scratch pad busy flag is set as noted below.



ADDRESS LOCATIONS

HEX	DB3	DB2	DB1	DB0	Register
0	0	0	0	0	4-Bit Volatile Counter
1	0	0	0	1	Word 1 - 20-bit EEPROM Counter
2	0	0	1	0	Word 2 - 20-bit EEPROM Counter
3	0	0	1	1	Word 3 - 20-bit EEPROM Counter
4	0	1	0	0	Word 4 - 20-bit EEPROM Counter
5	0	1	0	1	Word 5 - 20-bit EEPROM Counter
6	0	1	1	0	Word 1 - 16-bit Volatile Counter
7	0	1	1	1	Word 2 - 16-bit Volatile Counter
8	1	0	0	0	Word 3 - 16-bit Volatile Counter
9	1	0	0	1	Word 4 - 16-bit Volatile Counter
A	1	0	1	0	Flag Register - EEPROM
B	1	0	1	1	Used for counter reset-see text
C	1	1	0	0	Word 1 - EEPROM Scratch Pad
D	1	1	0	1	Word 2 - EEPROM Scratch Pad
E	1	1	1	0	Word 3 - EEPROM Scratch Pad
F	1	1	1	1	Word 4 - EEPROM Scratch Pad

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
with respect to ground..... +6V to -0.3V
Storage temperature (unpowered
and without data retention)..... -65°C to +150°C
Soldering temperature of
leads (10 seconds)..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software to the customer.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{CC} = +5V ± 10% V_L = +5V ± 10%
V_{CC} with no loss of volatile memory:
4.0V to 5.5V
V_{CC} with no loss of non-volatile memory:
4.2 to 6.0V
Operating temperature range (T_A):
0°C to +70°C (Commercial)

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V	
Low Level Input Voltage	V_{IL}	0	-	0.8	V	
High Level Output Voltage (open drain)	V_{OH}	V_t-0.5	-	V_t	V	Requires an external pull-up
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA
High Level CI Input Threshold Voltage	V_{TH}	2.4	-	V_{CC}-1.1V	V	Low-to-high Transition
Low Level CI Input Threshold Voltage	V_{TL}	0.8	-	1.8	V	High-to-low Transition
High Level V_L Input Voltage	V_{LH}	4.3	-	V_{CC}+0.3	V	V_{CC} = 4.5V
		5.0	-	V_{CC}+0.3	V	V_{CC} = 5.5V
Low Level V_L Input Voltage	V_{LL}	2.5	-	-	V	
V_{CC} Supply Current	I_{CC}	-	-	4	mA	V_L = 0V, Outputs Open
		-	-	10	mA	V_L = 4.3V, Outputs Open
Input Current V_L Input	I_L	-	-	200	uA	V_L = 2.0V
Input Leakage Current DB0-DB3, WR, RD, ALE, CI	I_{IL}	-	-	±1.0	uA	V_{IN} = 0 to 2.4V
High Level Output Leakage Current, HI-Z	I_{OZH}	-	-	+1.0	uA	V_{OH} = 2.4V
Power Dissipation	P	-	-	55	mW	Output open

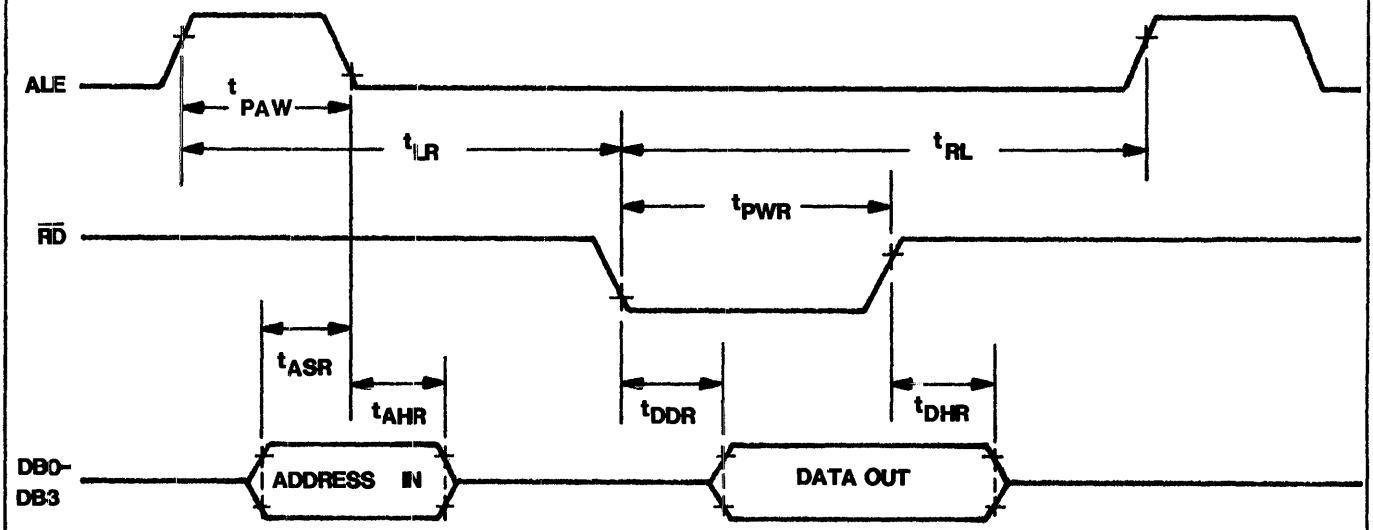
AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance	C_{IN}	-	-	10	pf	
Oscillator Capacitance	C_{osc}	50	-	100	pf	f_{osc} = 2.0MHz

Non-Volatile Counter/ EEPROM Backup: The non-volatile counter is actually a volatile counter backed up by EEPROM memory. The contents of EEPROM memory backup are updated each time an overflow from the 4-bit volatile counter occurs. This update coincides with each time the stored count changes. In order to increase the device's data stability, updates take the form of a dump from non-volatile memory into the counter, incrementing the counter and then restoring the incremented value to non-volatile memory.

Low Voltage Detect Input: Pin 15 (V_L) is an external input which goes low immediately prior to the supply voltage (V_{CC}) falling below its minimum operating voltage of 4.5V. Sufficient external energy storage must be provided to maintain V_{CC} above 4.5V at least 50msec after V_L goes low.

Figure 1: Read Mode



READ MODE	Sym	Min	Typ	Max	Unit	Conditions
ALE and RD Pulse Width	t_{PWR}	300	-	10^8	ns	
ALE to Read Pulse Delay	t_{LR}	1500	-	10^8	ns	
Read Pulse to ALE Delay	t_{RL}	1500	-	10^8	ns	
Address Setup Time	t_{ASR}	250	-	10^8	ns	
Address Hold Time	t_{AHR}	10	-	-	ns	
Data Delay Time	t_{DDR}	-	-	150	ns	
Data Hold Time	t_{DHR}	-	-	50	ns	

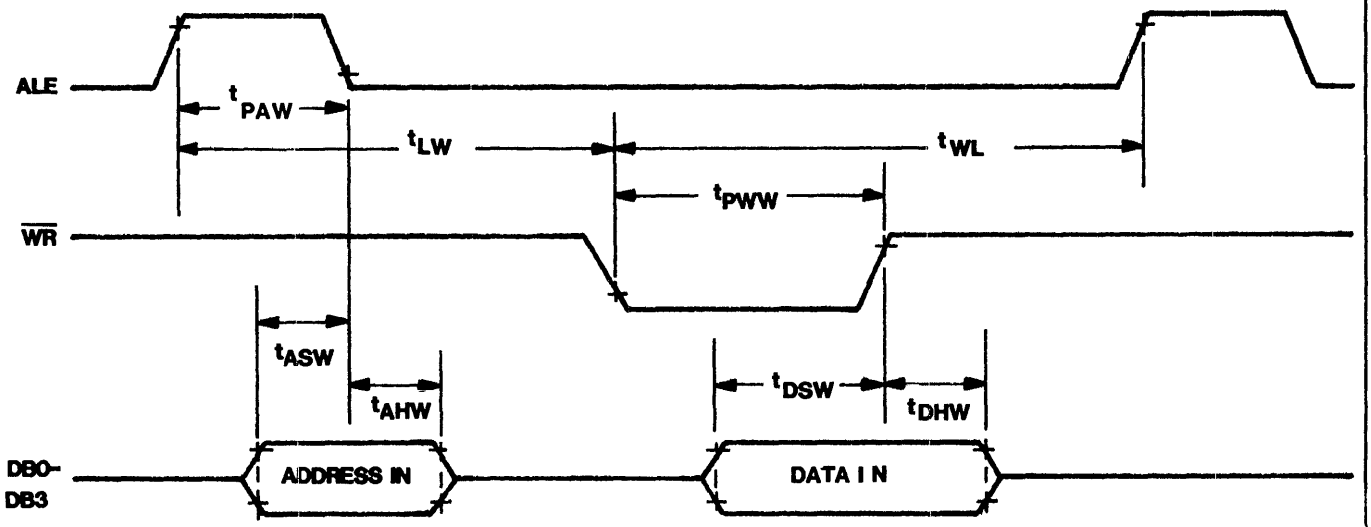
READ MODE PROTOCOL

1. Place the address to be read on the data bus and strobe with ALE.

2. Strobe $\overline{RD}$ (low): Data will be available on the data bus on the rising edge of the $\overline{RD}$ pulse.

An attempt to read address location, Hex B will return 1011 (Hex B) as data. Also, if location Hex A is read while the scratch pad busy flag is set, 1010 (Hex A) will be returned as data.

Figure 2: Write Mode



WRITE MODE	Sym	Min	Typ	Max	Unit	Conditions
ALE and RD Pulse Width	t_{PAW}	300	-	10^8	ns	
Wr Pulse Width	t_{PWW}	500	-	10^8	ns	
ALE to Write Pulse Delay	t_{LW}	1500	-	10^8	ns	
Write Pulse to ALE Delay	t_{WL}	1550	-	10^8	ns	
Address Setup Time	t_{ASW}	250	-	10^8	ns	
Address Hold Time	t_{AHW}	10	-	-	ns	
Data Setup Time	t_{DSW}	120	-	-	ns	
Data Hold Time	t_{DHW}	10	-	-	ns	

WRITE CYCLE PROTOCOL

1. Address location A: place on the data bus and strobe with ALE.

2. Write a 5 to this location: place a 5 on the data bus. This enables the subsequent write and strobe with WR.

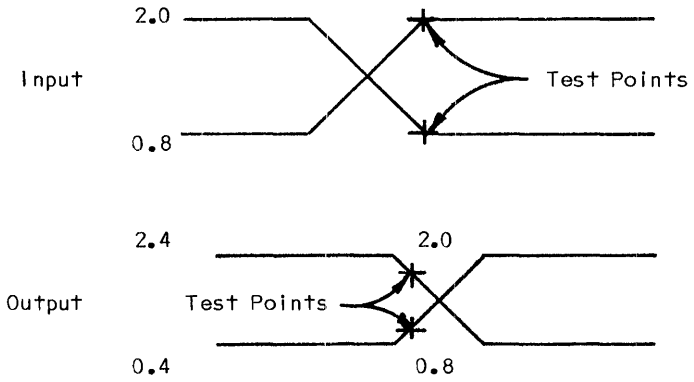
3. Address the desired location: place the location to be written (A, B, C, D, E or F) on the bus and strobe with ALE.

4. Write the desired data: place the desired data on the bus and strobe with WR. The write function is now disabled and must start again at step 1.

Write cycles may only be performed at addresses A through F. If the above sequence is not followed exactly without interruption, the protocol will be terminated. The write function is disabled on power-up.

16-Bit Counter Reset: A reset clears all 16-bits in the volatile counter. This reset is accomplished by following the write protocol and then writing a 4 to address B. If a read operation is performed at address B, a Hex B (1011) will be returned at data.

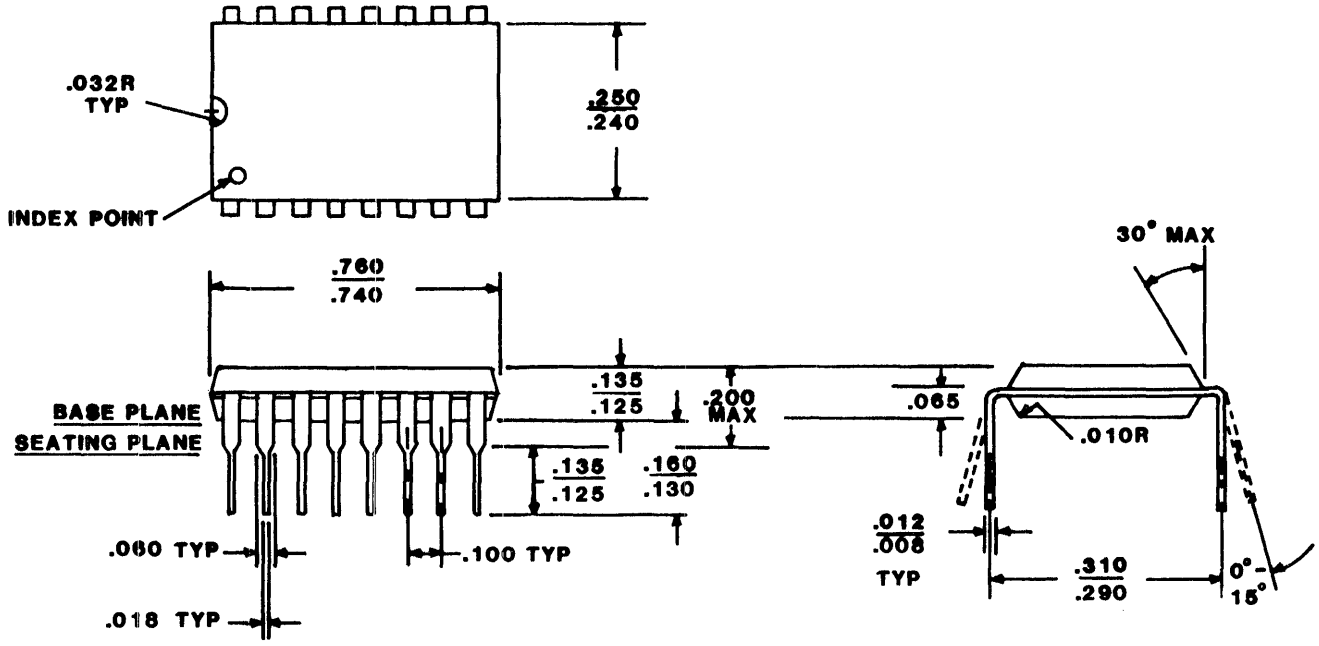
A.C. Testing, Input and Output Waveforms



A.C. Testing: Inputs are driven at 2.0V for an input logic high and 0.8V for an input logic low. Timing measurements of the output waveforms are made at 2.0V for an output logic high and 0.8V for an output logic low.

PACKAGE OUTLINE

16 LEAD DUAL-IN-LINE



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

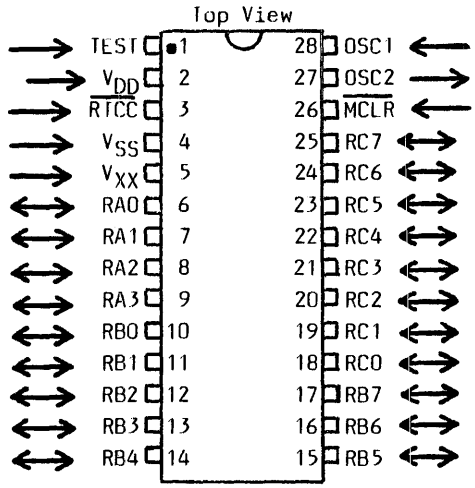
8 BIT SINGLE CHIP MICROCOMPUTER WITH ON BOARD NON-VOLATILE MEMORY

FEATURES:

- 512 x 12 bit program ROM
- 32 x 8 bit RAM registers
- 32 x 8 bit EEPROM (non-volatile) registers
- EEPROM operations include program (erase/write), erase, bulk erase, write and read
- Unlimited read accesses
- 10 years' data retention over the temperature range of -40°C to +85°C
- Arithmetic logic unit
- Real time clock/counter
- 20 bidirectional I/O lines
- 28 pin package
- 2 level pushdown stack for subroutine nesting
- 3μs instruction time
- Open drain option on all I/O lines
- Mask programmable prescaler for RTCC
- Self contained oscillator for crystal or ceramic resonator
- Available in 2 temperature ranges: 0° to 70°C, -40° to 85°C

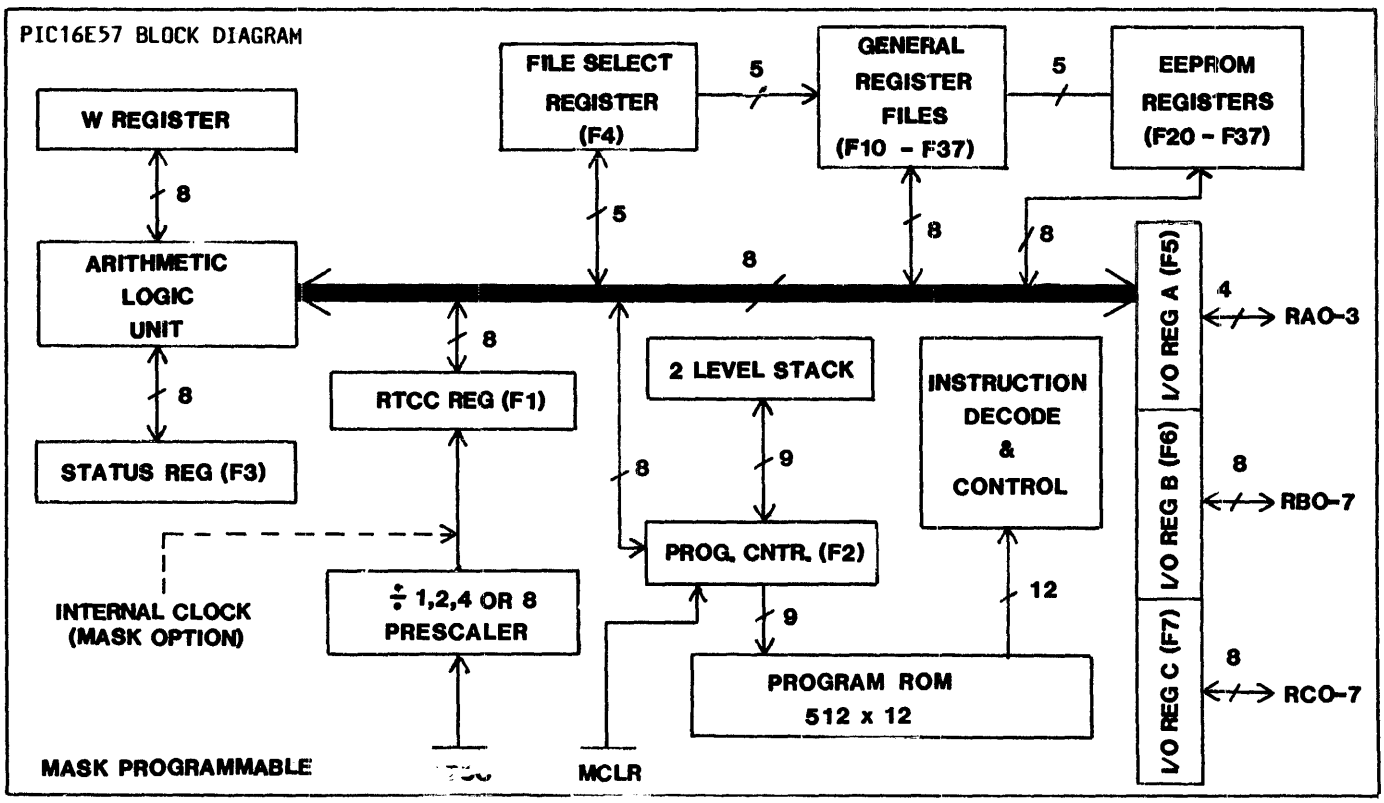
PIN CONFIGURATION

28 Lead Dual In Line



DESCRIPTION

The PIC16E57 microcomputer is an MOS/LSI device containing RAM, I/O and a central processing unit as well as customer-defined ROM on a single chip, with the added feature of non-volatile data storage. This combination produces a low cost solution for applications which require sensing



individual inputs and controlling individual outputs. Keyboard scanning with memory retention, display driving, and other system control functions can be done at the same time due to the powerful 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications.

The PIC16E57 can be used in security applications where the security code may be saved and then changed by the operator. It will also be useful in tuning applications. Favorite stations can be set and changed to suit the consumers needs. In addition, PIC16E57 can be used in automotive applications as electronic odometers or maintenance reminders. The 12-bit instruction word format provides a powerful yet easy to use instruction repetoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC16E57 is fabricated with N-Channel Silicon Gate Nitride (SNOS) technology resulting in a high performance product with proven reliability and production history. Only a single power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal or ceramic resonator to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALB, a powerful macro-assembler. PICALB is available in various versions that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC16E67. The PIC16E67 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD3000E Field Demo System is available containing a PIC16E67 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File (composed of 32 addressable 8-bit registers, and 32 addressable EEPROM registers), an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into three functional groups: operational registers general registers and general EEPROM registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions. The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

DATA MEMORY

Resident data memory is organized as 64 8 bit words addressable in 3 banks. The first eight registers F0-F7 are special purpose and are described in the "File Register Arrangement" on page 6. The file registers are designated F0-F37. F10-F37 are general purpose working registers for program data storage and are addressed when ESEL 1 and ESEL 2 both equal 0 or 1.

The 32 EEPROM registers are addressed as 2 banks of 16 (file registers F20-F37), the first group when ESEL 1 = 1 and ESEL 2 = 0, and the second group when ESEL 1 = 0 and ESEL 2 = 1. Thus F0-F17, which contain the 8 special purpose registers plus 8 general purpose registers, are addressable independent of the ESEL 1 and ESEL 2 bits. This reduces the software "bank switching" to the EEPROM registers when, for example, copying data from general purpose registers to EEPROM registers.

The details of utilizing the 32 non-volatile EEPROM registers are contained in the section titled "Non-Volatile Storage".

NON-VOLATILE STORAGE

Utilization of the 32 non-volatile EEPROM registers has been made as similar as possible to the standard general purpose file registers. What must be done is set the bank select bits to address the EEPROM banks, and then execute the instructions to program (erase/write), erase, write, or read the EEPROM registers. These operations are now described in detail below.

Addressing The EEPROM Registers - There are two EEPROM bank select bits, ESEL 1 and ESEL 2 in the status register, F3. They are bits 3 and 4, respectively. These bits may be read or written to under software control. When both bits are set to 0 or 1, the standard 32 registers are addressed. (See diagram "File Register Arrangement"). When ESEL 1 = 1 and ESEL 2 = 0, the first bank of 16 as EEPROM registers are selected. They are addressed F20-F37. F0-F17, which contain the 8 special purpose registers and 8 general purpose registers, are always directly addressable, independent of the ESEL bits. When ESEL 1 = 0 and ESEL 2 = 1, the second bank of 16 EEPROM registers is specified by addresses F20-F37.

Controlling The EEPROM Registers - The non-volatile registers are different from the standard, volatile registers, in that only a 1 can be written on individual bits. To cause the proper data pattern to be stored, the EEPROM register must first be erased to all 0s, and then a 1 be written to the appropriate bits as desired. This can be accomplished in several ways:

Program - A "program" operation is defined as an erase cycle followed by a write (1's) cycle. This is done automatically when one of the two EEPROM banks is selected (see section titled "Addressing the EEPROM Registers) and a MOVWF instruction is executed on F20-F37. Both erasing and writing take approximately 25 ms. each, but this is done both automatically and transparently to the software. The microcomputer can go off and perform other system functions while programming is taking place. While programming is in progress, the BSY bit in the Status Register (F3, B5) is set to 1. This is a "read-only" bit and should be polled by software to make sure programming is complete (BSY = 0) before attempting to do any operation on another EEPROM register. In the event that the user chooses to ignore the BSY bit and initiate another EEPROM operation, the microcomputer will halt and suspend operation until the programming in progress is complete (BSY = 0), at which time operation of the microcomputer will resume and the new EEPROM register operation will begin. Note that the programmer can avoid this suspension of operation by simply reading the BSY bit and only attempting another EEPROM operation when it is 0. Also the programmer can get a "software free" delay of the program time (approximately 50 ms.) if he wanted to by immediatetly attempting another program while one is already in progress.

Erase - The EEPROM registers can be erased to all 0 individually by selecting one of the two EEPROM banks and executing a CLRF instruction on F20-F37. This operation takes approximately 25 ms.

Bulk Erase - Each bank of EEPROM registers can be erased in a single (aproximately 25 ms.) operation by selecting the bank and executing the ERAL instruction (op code 0025). Both banks can be erased simultaneously by setting ESEL 1 and ESEL 2 both to 1's or both 0's and executing the ERAL instruction. (Any other register instruction executed when ESEL 1 and ESEL 2 are both 1 will function as though they were both 0, resulting in operating on the standard general purpose registers.)

Write - Individual EEPROM registers can be written into by executing an IORWF f,1 instruction on F20-F37 when an EEPROM bank is selected. If the EEPROM register has been previously erased (to 0) then the data in W will correctly be copied to the EEPROM register. Otherwise, since only a 1 can be written into a EEPROM register, a "write" operation is really an "inclusive or" operation. This operation takes approximately 25 ms.

Additionally, a BSF instruction can be used to write (inclusive OR) a 1 to an individual EEPROM register bit.

Read - The EEPROM registers are read by setting the destination designator "d" set to a zero (i.e. MOVF f,0). This is done in one instruction cycle time (t_{CY}).

NOTES:

1. All EEPROM operations (erase, bulk erase, write and read) have the same constraint as the program operation, i.e., if another EEPROM operation is invoked while one is already in progress, the microcomputer will halt and resume when the current EEPROM operation is complete.

2. If any instructions other than the valid EEPROM instructions (MOVWF, MOVF, BSF, IORF, CLRF, BTFSC, BTFSS, ERAL or any other read instruction) are executed on an EEPROM register, they will be NOPED.

PIN FUNCTIONS

SIGNAL	FUNCTION
OSC1 (input), OSC2 (output)	Oscillator pins. These pins are used to derive the internal clock for the chip. A crystal or ceramic resonator may be used in conjunction with OSC1 and OSC2. Additionally, OSC1 may be driven by an external oscillator. The instruction cycle frequency is one-eighth the oscillator frequency. (f_{OSC} = 2.67 MHz gives $t_{CY} \approx 3\mu s$.)
$\overline{RTCC}$ (input)	Real Time Clock/Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter Register increments on falling edges applied to this pin. This register (F1) can be loaded and read by the program. This is a Schmitt trigger input except when a prescaler division ratio of 2, 4, or 8 is selected, in which case the input is TTL compatible. A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock counter register. In this mode, the prescaler is eliminated and transitions in the $\overline{RTCC}$ pin will be disregarded.
RA0-3 (input/output)	User programmable input/output lines. These are controlled by the program to be inputs and/or outputs. The 4 MSBs are always read as logic zeroes.
RB0-7 (input/output)	User programmable input/output lines. These are controlled by the program to be inputs and/or outputs.
RC0-7 (input/output)	User programmable input/output lines. These are controlled by the program to be inputs and/or outputs.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8, set the I/O registers high, and clear the ESEL 1, ESEL 2 and BSY bits. This is a Schmitt Trigger input.
TEST	Used for testing purposes only. Must be connected to V_{SS} or left open circuit for normal operation.
V_{DD}	Power Supply.
V_{SS}	Ground.
V_{XX}	Output buffer power supply voltage. Used to increase the current sinking capability of the I/O pins (for direct LED drive, etc.).

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0-W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data is being stored in the RTCC register simultaneously with a negative transition on the $\overline{RTCC}$ pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction. (Bit 5 is a read only bit).

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	BSY	ESEL 2	ESEL 1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

ESEL 1, ESEL 2: These are the two EEPROM bank select bits. The following table defines their function:

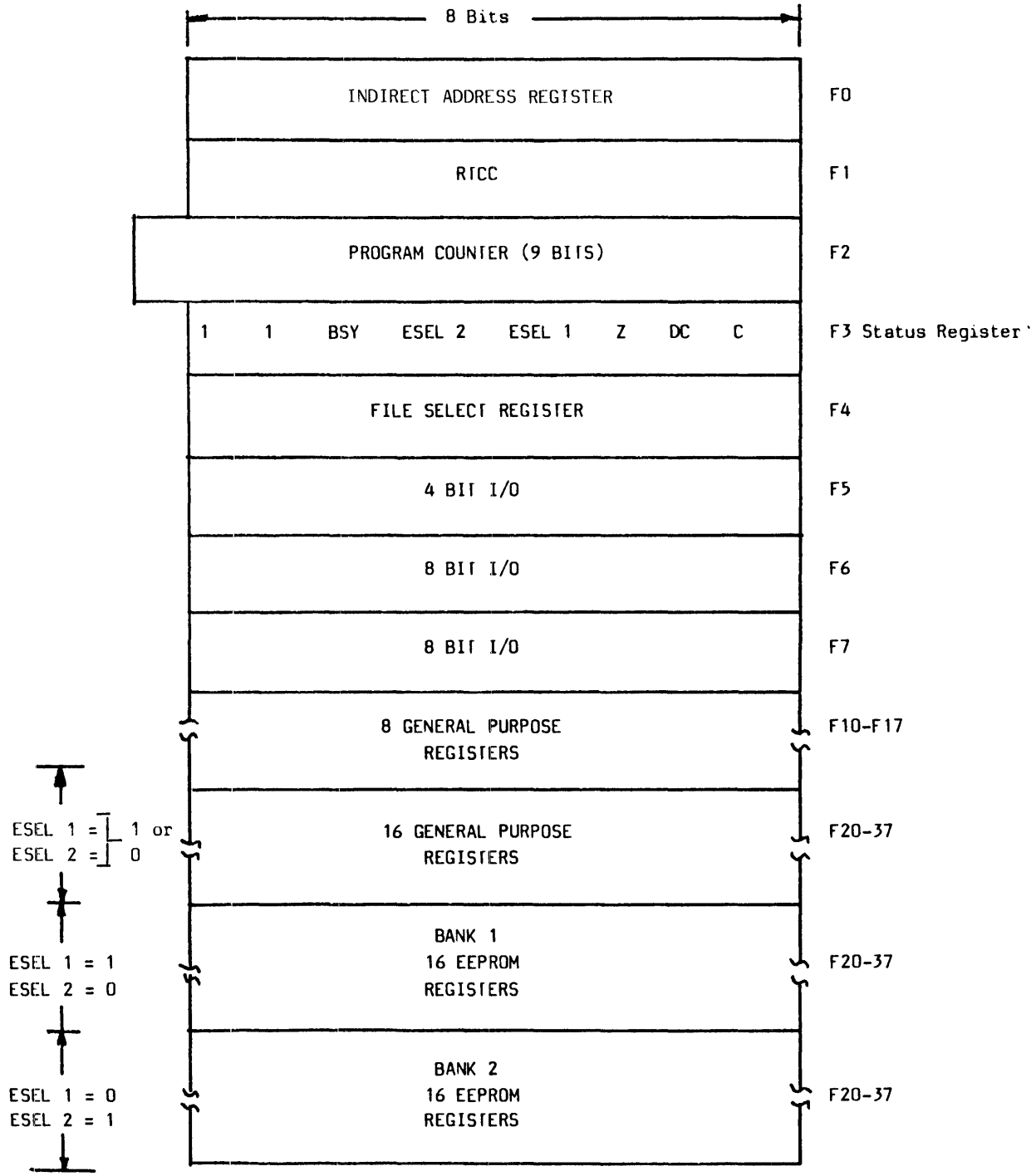
ESEL 2	ESEL 1	SELECTED REGISTERS
0	0	Standard RAM
0	1	EEPROM - Bank 1
1	0	EEPROM - Bank 2
1	1	Standard RAM

BSY: Is set to a one during EEPROM programming. This is a read only bit.

Bits: 6-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A3) (A4-A7 defined as zeros).
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F17	General Purpose Registers
F20-F37	General Purpose or EEPROM Registers (software selectable).

FILE REGISTER ARRANGEMENT



BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 2.67MHz the instruction execution time is 3 usec unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 6 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS (Note 4) (11-6) OP CODE | (5) d | (4-0) f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (if d is omitted, assembler assigns d = 1)

Instruction-Binary (Octal)	Name	Mnemonic	Operands	Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	-	-	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	-	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f,d	f-W→d (f+$\overline{W}$+1→d)	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f,d	f-1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f,d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f,d	W.f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f,d	W+f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f,d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f,d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f,d	f→d	Z
001 010 dff fff (1200)	Increment f	INCF	f,d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f,d	f-1→d, skip of Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f,d	f(n)→d(n-1),f(0)→C,C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f,d	f(n)-d(n+1),f(7)-C,C-d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f,d	f(0-3)⇆f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f,d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS (11-8) OP CODE | (7-5) b(BIT#) | (4-0) f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic	Operands	Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f,b	0—f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f,b	1—f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f,b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f,b	Bit Test f(b): skip if set	None

LITERAL AND CONTROL OPERATIONS (11-8) OP CODE | (7-0) k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic	Operands	Operation	Status Affected
100 0kk kkk kkk (4000)	Return & place Literal in W	RETLW	k	k -W, Stack-PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1—Stack, K—PC	None
101 kkk kkk kkk (5000)	Go to address (k is 9 bits)	GOTO	k	k—PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k—W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW—W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k.W—W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W—W	Z

BYTE-ORIENTED EEPROM FILE REGISTER OPERATIONS (Operational only when ESEL bits are appropriately set)

Instruction-Binary (Octal)	Name	Mnemonic	Operands	Operation	Status Affected
000 000 1ff fff (0040)	Move W to f	MOVWF	f	W → f (EEPROM)	None
001 000 dff fff (1000)	Move f	MOVF	f,d	F (EEPROM → W)	Z
010 1bb bff fff (2400)	Bit Set f	BSF	f,b	1- f(b)	None
011 0bb bff fff (3000)	Bit Test f, skip if clear	BTFSC	f,b	Same as normal mode	None
011 1bb bff fff (3400)	Bit Test, skip if set	BTFSS	f,b	Same as normal mode	None
000 100 dff fff (0400)	Inclusive or W and f	IORWF	f,d	f (EEPROM) VW → d	Z
000 001 1ff fff (0140)	Clear f	CLRF		0 → f (EEPROM)	Z
000 000 010 101 (0025)	Erase all	ERAL		0 → EEPROM file bank	None

Notes:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be related in the low state.
3. See non-volatile storage section for ESEL EEPROM instructions.
4. All instructions, where D=Ø, are legal EEPROM instructions.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assmbler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3,0	-
010 100 000 011 (2403)	Set Carry	SETC	BSF 3,0	-
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3,1	-
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3,1	-
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3,2	-
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3,2	-
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3,0	-
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3,0	-
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3,1	-
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3,1	-
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3,2	-
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3,2	-
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f,1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f,0	Z
001 001 1ff fff (1140)	Negate File	NEGF f,d	COMF f,1	
001 010 dff fff (1200)			INCF f,d	Z
011 000 000 011 (3003)	Add Carry to File	ADDCF f,d	BTFSC 3,0	
001 010 dff fff (1200)			INCF f,d	Z
011 000 000 011 (3003)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0	
000 011 dff fff (0300)			DECF f,d	Z
011 000 100 011 (3043)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1	
001 010 dff fff (1200)			INCF f,d	Z
011 000 100 011 (3043)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1	
000 011 dff fff (0300)			DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	-
011 000 000 011 (3003)	Branch on Carry	BC k	BTFSC 3,0	
101 kkk kkk kkk (5000)			GOTO k	-
011 100 000 011 (3403)	Branch on No Carry	BNC k	BTFSS 3,0	
101 kkk kkk kkk (5000)			GOTO k	-
011 100 100 011 (3043)	Branch on Digit Carry	BDC k	BTFSC 3,1	
101 kkk kkk kkk (5000)			GOTO k	-
011 001 000 011 (3443)	Branch on No Digit Carry	BNDC k	BTFSS 3,1	
101 kkk kkk kkk (5000)			GOTO k	-
011 101 000 011 (3103)	Branch on Zero	BZ k	BTFSC 3,2	
101 kkk kkk kkk (5000)			GOTO k	-
011 101 000 011 (3503)	Branch on No Zero	BNZ k	BTFSS 3,2	
101 kkk kkk kkk (5000)			GOTO k	-

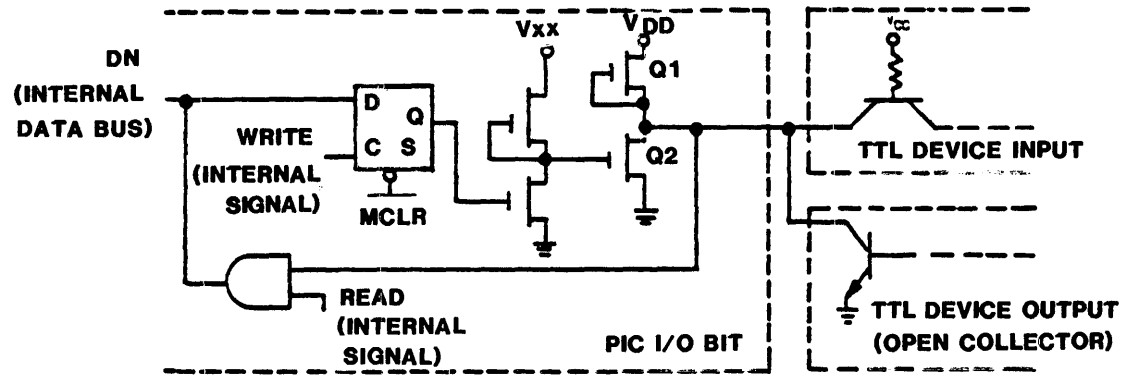
Note: See "Notes" of Non-Volatile Storage for ESEL ELPROM instructions.

I/O INTERFACING

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input.

When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2 allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



PROGRAMMING CAUTIONS

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

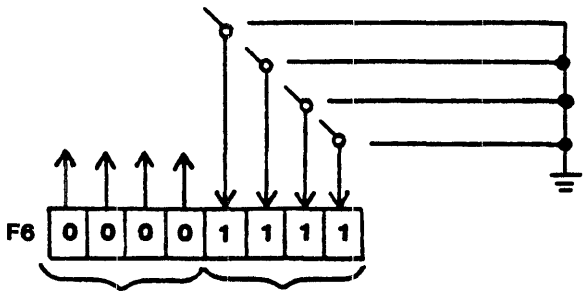
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output latch must be set in the high state. Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F6 (port RC) will cause all eight bits of F6 to be read into the CPU. Then the BSF operation takes place on bit 5 and F6 is re-output to the output latches. If another bit of F6 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programer. Refer to the examples on the next page.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $1/4t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1



OUTPUT INPUT

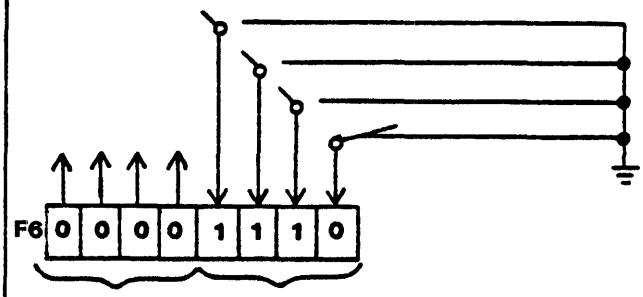
What is thought to be happening:

BSF 6,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F6:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2



OUTPUT INPUT

What could happen if an input were low:

BSF 6,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F6:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

Real Time Clock Counter

The Real Time Clock Counter can be read from and written to under software control. In addition, it can be used to count external events via the $\overline{\text{RTCC}}$ input. A prescaler counter between the $\overline{\text{RTCC}}$ input and the Real TIme Clock Counter can be mask programed to enable the RTCC register to increment every 1, 2, 4, or 8 negative edges of the $\overline{\text{RTCC}}$ input pin.

This allows the maximum frequency of the $\overline{\text{RTCC}}$ input to be (assume an instruction cycle time of 3µs):

Prescaler Division Ratio	Maximum Input Frequency
1	.3125MHz
2	.6250MHz
4	1.2500MHz
8	2.5000MHz

NOTE: The Schmitt trigger input is valid only when a division ratio of 1 is selected. Otherwise, the input is a normal TTL compatible input.

Self-Contained Oscillator

When a crystal or ceramic resonator is connected between the OSC1 and OSC2 pins, the self-contained oscillator will generate a frequency determined by the external components thus allowing an accurate timing reference, a crystal to be used for time base control with a minimum of external parts.

The output of this oscillator is divided down by 8 to give the instruction cycle time of the microcomputer, thus with a 2.67MHz crystal the instruction cycle time is 3µs.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias..... 125°C
Storage Temperature ..... -55°C to + 150°C
Voltage on any Pin with Respect to V_{SS}
(except open drain)..... -0.3V to +9.0V
Voltage on any Pin with Respect to V_{SS}
(open drain)..... -0.3V to +13V
Power Dissipation (Note 1)..... 800mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied--operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (Unless otherwise stated):

DC CHARACTERISTICS: PIC16E57

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ*	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	-	5.5	V	
Primary Supply Current	I_{DD}	-	-	80	mA	All I/O @ V_{DD}
Output Buffer Supply Voltage	V_{XX}	4.5	-	7.0	V	Note 4
Output Buffer Supply Current	I_{XX}	-	-	5	mA	Note 5
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH1}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$, & OSC1)	V_{IH2}	V_{DD}-1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100uA provided by internal pullups (Note 2)
Output Low Voltage (I/O only)	V_{OL}	-	-	0.45	V	I_{OL} = 1.6mA (Note 3), V_{XX} = 4.5V
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	-10	-	+10	µA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain pins)	I_{OL}	-	-	20	µA	$0V \leq V_{PIN} \leq 9V$
Input Low Current (all I/O ports)	I_{IL}	-0.2	-	-1.6	mA	V_{IL} = 0.4V (internal pullup)
Input High Current (all I/O ports)	I_{IH}	-0.1	-0.4	-	mA	V_{IH} = 2.4V

*Typical data is at T_A = 25°C, V_{DD} = 5.0V

NOTES:
1. Total power dissipation for the package is calculated as follows:
$P_D = (V_{DD})\ (I_{DD}) + \sum(V_{DD}-V_{IL})\ (|I_{IL}|) + \sum(V_{DD}-V_{OH})\ (|I_{OH}|) + \sum(V_{OL})\ (I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins must not exceed 125 mA. Maximum I_{OL} per pin must not exceed 15mA.
4. V_{XX} supply drives only the I/O ports.
5. The maximum I_{XX} current will be drawn when all I/O ports are outputting a high.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS: PIC16E57
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	3	-	10	us	0.8MHz - 2.666666MHz external time base (Notes 1 and 2)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}+0.2µs	-	-	-	Note 3
High Pulse Width	t_{RTH}	1/2 t_{RT}	-	-	-	
Low Pulse Width	t_{RTL}	1/2 t_{RT}	-	-	-	

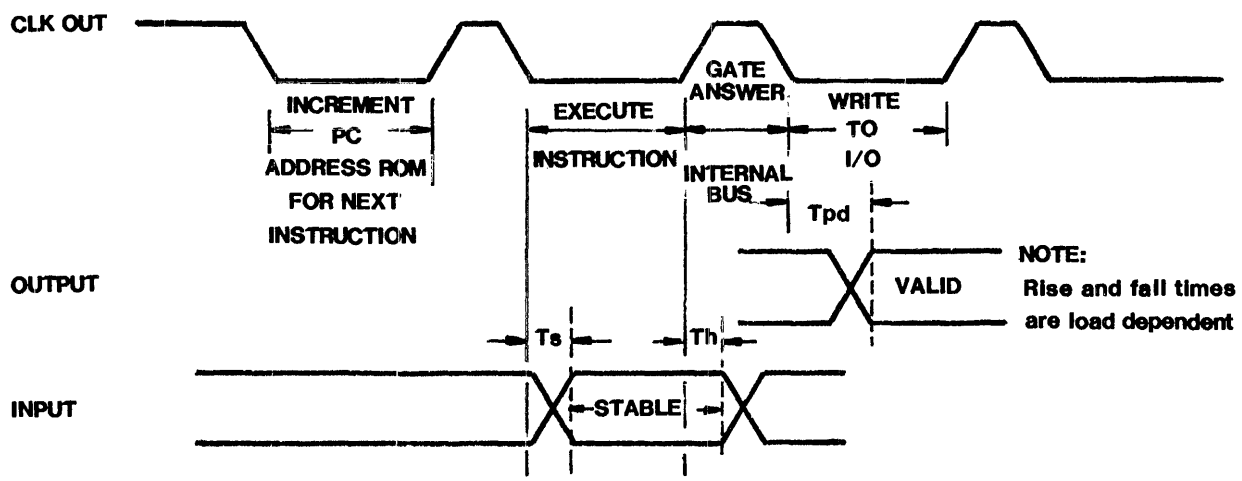
NOTES:
1. Instruction cycle period (t_{CY}) equals eight times the input oscillator time base period.
2. The oscillator frequency may deviate to 2.72MHz to allow for tolerance of a crystal or ceramic resonator time base element.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT(min)}} = \frac{1}{t_{CY(min)}+0.2\mu s}$$

For example:

If t_{CY} = 3µs, $f_{(max)} = \frac{1}{3.2\mu s}$ = .3125MHz

I/O TIMING



some time base elements. Consult the manufacturer of the time base element for specific start-up times.

MICROELECTRONICS DIVISION/GENERAL INSTRUMENT CORPORATION

WORLDWIDE SALES OFFICES

NORTH AMERICA
UNITED STATES:
MICROELECTRONICS DIVISION

NORTHEAST -
36 Commerce Way
Woburn, Massachusetts 01801
Tel: 617-938-5890, TLX: 922540

758 Highway 18, Suite 104
East Brunswick, New Jersey 08816
Tel: 201-254-5024, TWX: 710-480-5469

SOUTHEAST -
1616 Forest Drive
Annapolis, Maryland 21403
Tel: 310-269-6250, TWX: 710-867-8566

19 West Hargett Street
Commerce Bldg., Suite 809E
Raleigh, North Carolina 27601
Tel: 919-828-0317

SOUTH CENTRAL -
4825 LBJ Frwy., Suite 178
Dallas, Texas 75244
Tel: 214-934-1654, TWX: 910-860-9259

CENTRAL -
5511 East 82nd Street, Suite A
Indianapolis, Indiana 46250
Tel: 317-841-9328, TWX: 910-333-2885
ELN: 62774221

2355 S. Arlington Hts. Road,
Suite 408
Arlington Heights, Illinois 60005
Tel: 312-981-0040

SOUTHWEST -
201 Standard Street
El Segundo, California 90245
Tel: 213-322-7745, TWX: 910-348-6296

NORTHWEST -
3080 Olcott Street, Suite 230C Santa
Clara, California 95054
Tel: 408-496-0844, TWX: 910-379-0010

EUROPE
NORTHERN EUROPE
Times House, Ruislip,
Middlesex, HA4 8LE
Tel: (08956), 36141, Telex: 23272

SOUTHERN EUROPE
5-7 Rue De L'Amiral Courbet
94160 Saint Mande, Paris
Tel: (1) 374-1133, Telex: 842-213073

Via Mascheroni 19
20145 Milano
Tel: (2) 498 73 62

CENTRAL EUROPE
GENERAL INSTRUMENT DEUTSCHLAND GmbH
Freischuetzstr. 96
Postfach 810329
8000 Muenchen 81
Tel: (089) 95997-0, Telex: 528054

GENERAL INSTRUMENT

MICROELECTRONICS DIVISION/GENERAL INSTRUMENT CORPORATION

WORLDWIDE SALES OFFICES (continued)

ASIA

HONG KONG:
GENERAL INSTRUMENT HONG KONG LTD.
Room 1104-1107, Tower B
Mandarin Plaza, Science Museun Road
Tsimshatsui East, Kowloon
Hong Kong
Tel: (5) 434360, Telex: 84606+

JAPAN:
GENERAL INSTRUMENT INTERNATIONAL CORP.
Fukide Bldg., 1-13 Toranomon 4-Chome
Minato-ku, Tokyo 105
Tel: (03) 437-0281, Telex: 2423413+

Toyosaki Bldg. 7/F
18-21 Chaya-Machi, Kita-Ku
Osaka 530 Japan
Tel: (06) 375-0606

KOREA:
GENERAL INSTRUMENT MICROELECTRONICS
Room 1004, Keo Yang Bldg.
51-8, Soosong-Dong
Chongro-Ku, Seoul, Korea
Tel: (2) 744-8543,
TLX: K26880 DAEHO

SINGAPORE:
GENERAL INSTRUMENT HONG KONG LTD.
Suite 1914, Shaw Centre
1 Scotts Road, Singapore 0922
Tel: (65) 235-8030,
Telex: GIS'PORE RS 24424

TAIWAN:
GENERAL INSTRUMENT
MICROELECTRONICS TAIWAN
233 Pao Chiao Road, Hsin Tien
Taipei, Taiwan
Tel: (02) 914-6234,
Telex 785-31115

GENERAL INSTRUMENT