July 1994
Edition 2.0

DATA SHEET

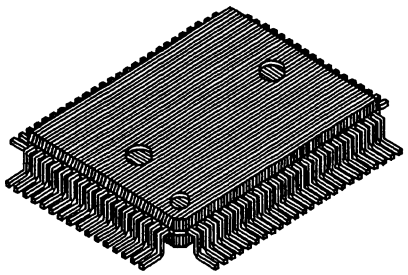
FUJITSU

MB86689A
Address Translation Controller (ATC)

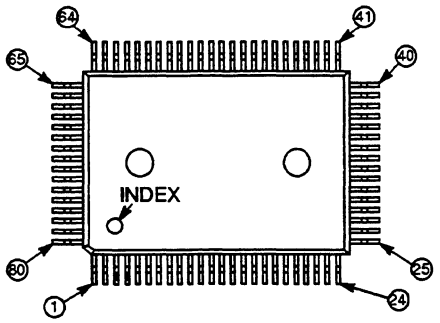
Address Translation Controller

The FUJITSU MB86689A Address Translation Controller provides an autonomous high speed translation function of ATM cell header information in real time at 155Mb/s. The translation supports replacement of ATM virtual path and virtual channel identifiers, and also allows a 24 bit routing tag to be appended. The device is designed to interface directly to the MB86683 Network Termination Controller (NTC), which will be located at ATM switch input/output ports. It also incorporates an 8-bit parallel cell stream interface which facilitates autonomous in-line address translation.

PLASTIC PACKAGE
QFP80



PIN ASSIGNMENT



FEATURES

- 1024 entry content addressable memory.
- Full 28 bit comparison for each entry.
- Selectable VPI and VCI mask for each entry.
- Supports UNI and NNI cell header formats.
- Supports multiple matches (NTC Mode only).
- Supports Flexible tag sizes.
- Supports the provision of translation data suitable for Usage Parameter Control.
- Supports CLP and congestion indication and removal for each entry.
- Multiple ATCs can be cascaded to support larger translation tables (NTC mode only).
- Translation is completed in less than one cell period at 155Mb/s.
- Entries can be updated on-the-fly without affecting the translation process.
- Provides selectable UTOPIA compatibility.
- JTAG pins compatible with IEEE1149.1 are provided.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

TABLE OF CONTENTS

APPENDICES

TABLES

ILLUSTRATIONS

1. OVERVIEW

The Address Translation Controller (ATC) comprises the following major components :-

- Input and output data formatters
- Content addressable memory array
- Output RAM
- Controller
- Microprocessor Interface

Immediately following a power-on reset, the ATC executes an internal initialisation sequence. During this mode of operation, the ATC clears the contents of its CAM Array, thereby disabling all the entries in the CAM table. Match/Translation entries in the CAM Array and Output Ram table are enabled via a control bit in the VPI Match and Control field of Word 3 in Fig 20. See section 4.1.6.

The ATC permits two interface modes of operation, the NTC Interface and the Cell Stream Interface mode. When operating in the NTC interface mode, the ATC receives 28-bit source data from the NTC and will compares the data against each active match entry in the CAM Array. If a match is found, then the ATC will output 54 bits of data which are stored in the output RAM for the associated match location. The maximum time required to read the input data, perform a search, and output the associated RAM data is less than 53 clock cycles, and hence is less than 1 ATM cell period.

If more than 1 match is detected for the same input data, then the ATC will sequentially output associated RAM data for each match (NTC interface mode only). A four wire handshake mechanism is used to control the transfer of data between the ATC and NTC.

Multiple ATCs may be cascaded by using dedicated cascade pins. Multiple matches are supported across multiple ATCs (NTC interface mode only).

In the case of the cell based interface, the ATC will format the output data into a new header and will output the header followed by a re-calculated HEC and the associated cell payload. Cell copying for multiple matches is not supported in the cell based interface mode.

ATC entries may be updated on-the-fly without affecting real-time performance.

2. EXTERNAL INTERFACES

2.1. Logical Outline

A logical view of the ATC's external pins is illustrated in Fig 1, a physical pin assignment diagram is shown in Appendix F , Fig. 31 together with a designated pin table.

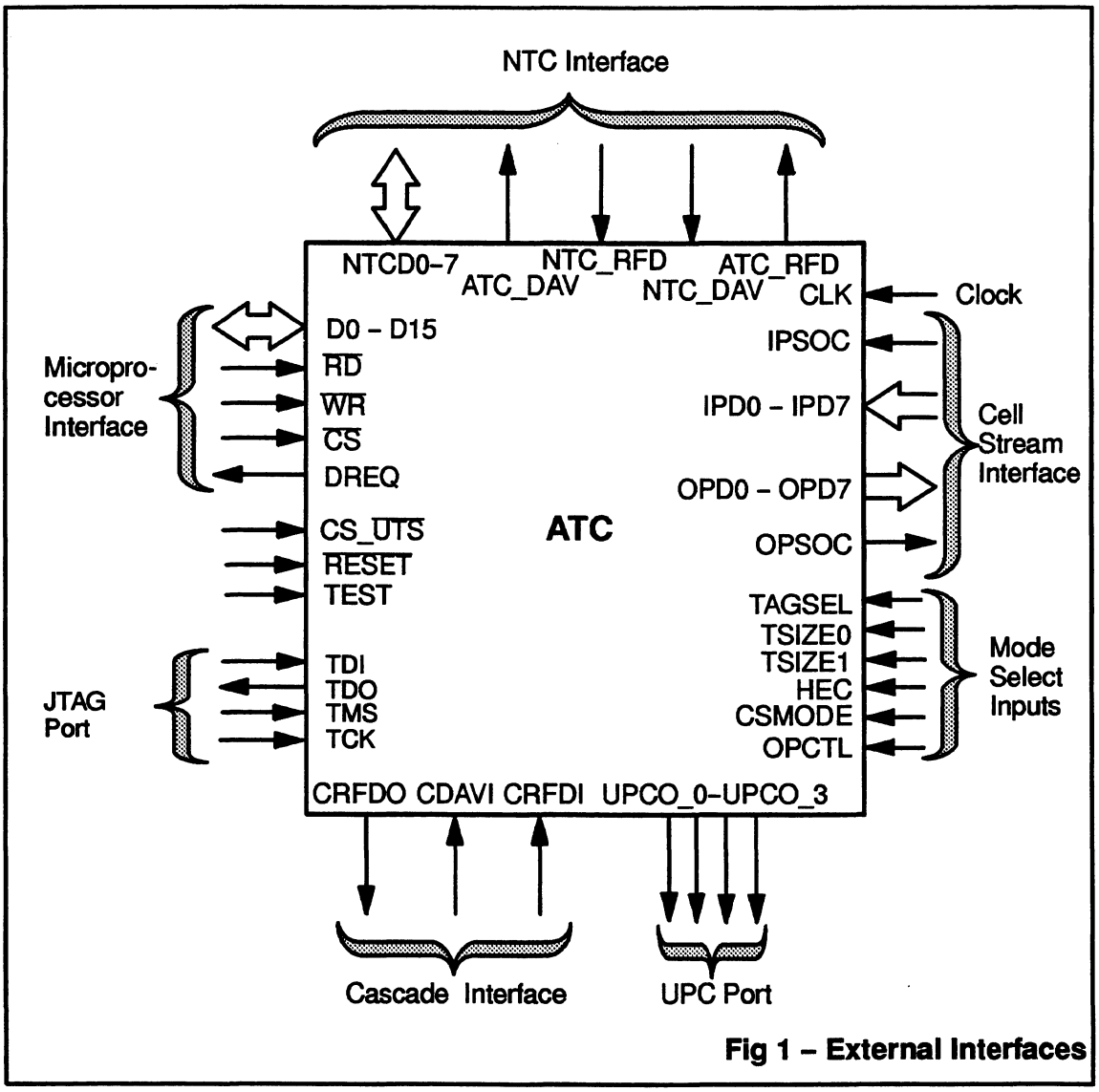


Fig 1 - External Interfaces

2.2. Detailed Description

A brief description of each of the ATC's input and output pins shall now be given.

$\overline{\text{RESET}}$
An active low pulse applied to the $\overline{\text{RESET}}$ input pin shall cause the ATC to enter it's power-up reset state.

CLK
Data present on the input ports IPD0-IPD7, and the bidirectional ports NTCD0-NTCD7 is sampled on the rising edge of the clock signal present on this pin.

2.2.1. Cell Stream Interface

All cell stream interface input / output data comprises 8 data bits together with a Start of Cell (SOC) bit. The data for one cell period comprises a 0 to 3 byte tag field followed by a 52/53 byte ATM cell. The cell stream may be continuous or discontinuous. In both cases the SOC bit marks the first byte associated with a cell period.

IPSOC
This pin indicates the start of an incoming cell and causes the ATC to receive and process the cell. When not in use this pin should be tied to VSS.

IPD0 - IPD7
These pins provide 8-bit parallel input data for the cell stream mode of operation. Data is sampled on the rising edge of CLK.

OPSOC
This pin is used by the ATC to indicate the commencement of cell transmission on the output pins OPD0-OPD7.

The signal pin OPSOC shall remain in it's active high state for the duration of 1 clock cycle and in it's active low state for the transmission of the remainder of the cell.

When operating in the Fujitsu Cell Stream mode, data transitions on the signal pin OPSOC are synchronized to the falling edge of the clock present on the CLK pin.

When operating in the UTOPIA Cell Stream mode, data transitions on the signal pin OPSOC are synchronized to the rising edge of the clock present on the CLK pin.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the OPSOC output pin is driven to it's inactive low state.

OPD0 - OPD7
These pins provide 8-bit parallel output data for the cell stream mode of operation.

When operating in the Fujitsu Cell Stream mode, data transitions on the signal pins OPD0-OPD7 are synchronized to the falling edge of the clock present on the CLK pin.

When operating in the UTOPIA Cell Stream mode, data transitions on the signal pins OPD0-OPD7 are synchronized to the rising edge of the clock present on the CLK pin.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the output pins OPD0-OPD7 are driven low to their logic "0" state.

2.2.2. NTC Interface

This interface is used to transfer data between the NTC and ATC. The interface comprises the following signals:-

NTCD0-NTCD7
8 bit bi-directional data bus between the NTC and ATC.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the bi-directional data bus, NTCD0-NTCD7, is driven to it's inactive high impedance state.

ATC_RFD
The ATC's ready for Data, active high single bit control output pin, ATC_RFD, is used by the ATC to inform the NTC that it is ready to receive any data that may be transferred across the NTC interface data bus pins, NTCD0-NTCD7.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the output pin ATC_RFD is driven to it's active high state.

NTC_DAV
The active high single bit control input pin, NTC_DAV, is used by the ATC to determine the start of data transfer across the NTC interface data bus pins, NTCD0-NTCD7, from the NTC to the ATC.

ATC_DAV
The ATC's Data Available, active high single bit control output pin, ATC_DAV, is used by the ATC to inform the connected NTC that the ATC has found a match and is prepared to commence data transfer across the NTC interface data bus pins, NTCD0-NTCD7.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the output pin ATC_DAV is driven to it's inactive low state.

NTC_RFD
The NTC's Ready for Data, active high single bit control input pin, NTC_RFD, is used by the ATC to initiate the transfer of data across the NTC interface data bus pins, NTCD0-NTCD7, from the ATC to the NTC.

2.2.3. Cascade Interface

This interface facilitates the control of multiple ATCs when they are cascaded to form a larger translation table (ie. more than 1024 entries).

The Cascade interface signals are only applicable when operating in the NTC interface mode of operation.

The ATC provides 3 signals which are dedicated to providing this function. The signals are listed below:-

CRFDI
The Cascade Ready For Data Input pin is used by the ATC to determine whether or not the previous ATC is ready to accept input data.

Consequently when cascading ATCs the CRFDI input pin should connected to the RFD output of the previous ATC.

When not in use CRFDI should be tied to VDD.

CDAVI
The Cascade Data Available Input pin is used by the ATC to determine whether or not the previous ATC has data available for output.

Consequently when cascading ATCs the CDAVI input pin should connected to the DAV output pin of the previous ATC.

When not in use CDAVI should be tied to VSS.

CRFDO
The Cascade Ready For Data Output pin is used by the ATC to inform the ATC Cascaded to it that it is ready to accept input data.

Consequently when cascading ATCs the CRFDO output pin should connected to the RFD input pin of the previous ATC.

Immediately following an active low transition on the $\overline{\text{RESET}}$ pin the output pin CRFDO is driven to it's inactive low state.

2.2.4. ATC mode control signals

The primary function of the ATC mode control signal pins is to provide the user with a number of selectable / flexible interface functions that may be carried out / performed on the translated data and incoming cell.

CSMODE
The Cell stream mode select pin is used by the ATC to select the appropriate active interface mode of operation.

When the CSMODE pin is tied low, this pin shall enable the NTC interface to be selected for cell translation purposes.

When the CSMODE pin is tied high, this pin shall enable the Fujitsu Cell Stream interface to be selected for cell translation purposes.

TAGSEL
The input pin TAGSEL is used by the ATC (only in the NTC mode) to enable / disable the Flexible tag size mode of operation.

When the TAGSEL pin is tied low, the ATC's Flexible tag size mode of operation is enabled permitting variations in the tag size from no tag to a 3 byte tag to be appended to the start of a cell.

When the TAGSEL pin is tied high, the ATC's Flexible tag size mode of operation is disabled permitting only a 3 byte tag to be appended to the start of each cell.

TSIZE0 - TSIZE1
The Tag size select pins TSIZE0–TSIZE1 are used by the ATC to select the length of tag to be appended to the start of each cell.

The two Tag size input pins are interpreted as follows:-

Tsize1	Tsize0	Tag
0	0	no tag
0	1	1 byte tag
1	0	2 byte tag
1	1	3 byte tag

When operating in the NTC interface mode of operation, with the TAGSEL pin tied high, a 3 byte tag is appended to the start of a cell irrespective of the status of the two Tag size input pins.

HEC
The input pin HEC, shall only be used by the ATC when operating in the Cell Stream interface mode of operation

This pin is used by the ATC to determine whether or not to include or exclude an

HEC byte to the ATM Cell header of outgoing ATM cells.

When the HEC pin is tied low, the standard HEC field is assumed to be present on incoming data, and is therefore recalculated on all outgoing data. The recalculated HEC field is internally exclusively "OR"ed with HEX 55 before being appended to the ATM Cell header as recommended in **ITU-T I.432**.

When the HEC pin is tied high, the HEC field is excluded from the ATM Cell header appended to outgoing cells (ie. 52 byte cells).

OPCTL
Output control. This input pin is used by the ATC to determine whether the output pin DREQ and the UPC output port pins UPCO_1 to UPCO_3, are tri-stateable or operate as a normal outputs. For cascade purposes both DREQ and the UPC port pins must be configured as 3-state.

A '0' selects 3-state and a '1' selects normal.

CS_$\overline{UTS}$
This single bit input pin is used by the ATC to select the format of data transmission on the Cell Stream interface output signal pins.

When tied high, the Fujitsu Cell Stream mode of data transmission is selected with all the data present on these output pins being transmitted on the falling edge of the clock present on the CLK input pin.

When tied low, the UTOPIA Cell Stream mode of data transmission is selected, with all the data present on these output pins being transmitted on the rising edge of the clock present on the CLK input pin.

2.2.5. Usage Parameter Control Interface

UPCO_0-UPCO_3
The 4-bit UPC interface output pins are used by the ATC to convey the 10-bit Output Ram address at which a successful translation has occurred and the 2-bit ID code identifying the Cascaded ATC from whence the translation came.

Immediately following a master reset the status of the UPC port pins is dependant on the status of the OPCTL pin.

If the OPCTL pin indicates that normal outputs are to be selected the ATC will drive the UPC port pins to Hex F.

Else the UPC port is driven to it's inactive high impedance state.

2.2.6. Microprocessor Interface

The microprocessor interface is a slave interface which only supports 16-bit word transfers. It comprises the following signals:-

D0-D15
These pins comprise a 16-bit bi-directional data bus that may be used to write data to and read data from the ATC internal registers.

Immediately following an active low transition on the $\overline{RESET}$ pin the bi-directional data bus, D0 - D15, is driven to it's inactive high impedance state.

$\overline{CS}$
The active low Chip select input is used

by the ATC to enable read and write operations to internal ATC registers.

$\overline{RD}$

The active low $\overline{RD}$ input signal is used by the ATC as a Microprocessor bus read signal. A read operation of the ATC's Status register is only permissible when both the $\overline{RD}$ and $\overline{CS}$ input signal pins are active.

$\overline{WR}$

The active low $\overline{WR}$ input signal is used by the ATC as a Microprocessor bus write signal. Write operations to internal ATC registers are only permissible when both the $\overline{WR}$ and $\overline{CS}$ input signal pins are active.

DREQ

The DREQ output pin represents an active high DMA or Microprocessor request signal. This signal pin is used by the ATC to control the rate at which CAM entries may be updated by the host Microprocessor.

Immediately following a master reset the status of the DREQ pin is dependant on the status of the OPCTL pin.

If the OPCTL pin indicates that normal outputs are to be selected DREQ will be driven to its inactive low state.

Else the UPC port is driven to it's inactive high impedance state.

2.2.7. JTAG Interface

TDO

The TDO output pin represents a tri-stateable serial output port through which test instructions and data from the internal test logic may be conveyed.

Changes in the state of the signal driven through TDO shall only occur following the falling edge of TCK.

When no signal is being driven through the TDO port the output pin should revert to it's tri-state condition.

Immediately following an active low transition on the $\overline{RESET}$ pin the output pin TDO is driven to it's inactive high impedance state.

TCK

The TCK input pin provides the clock signal for the internal test logic. Data received on the TDI input pin is sampled on the rising edge of TCK clock signal.

TMS

The TMS input pin is sampled on the rising edge of the TCK clock and decoded by the internal test logic to control test operations.

An External pull-up should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

TDI

The TDI input pin shall provide a port through which JTAG serial test data and instructions may be received by the internal test logic.

An External pull-up should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

TEST

This input pin is used for internal test purposes only and should be permanently tied low by the user via a 2K7 resistor.

3. FUNCTIONAL DESCRIPTION

3.1. General

A block diagram of the ATC is shown in Fig 2.

The ATC is designed to process and translate various fields within an ATM cell header. The format of an ATM cell is illustrated in Fig 3.

The ATC provides two interface modes, the NTC interface mode and the Cell Stream interface mode.

3.2. NTC Interface mode

An ATC may be configured to use it's NTC interface by tie-ing it's CSMODE input pin to VSS. This is known as the NTC mode of operation. The ATC's NTC interface allows the ATC to communicate directly with an NTC (MB86683). In this operational interface mode the transfer of ATM header information across the dedicated bi-directional data bus is controlled via a 4-signal handshake mechanism. During the transfer of data across this interface no cell payload data is transferred.

3.2.1. NTC Mode Input Data

In NTC mode, the input data provided by an NTC comprises the VPI/VCI fields of an ATM cell header only. No cell payload data is transferred across this interface.

The VPI/VCI fields are transferred from the NTC to the ATC in a contiguous 4-byte burst, as shown in Fig 4, via the bi-directional NTC-ATC data bus, NTCD0-D7. The ATC indicates that it is ready to accept these bytes by activating it's ATC_RFD pin. Data transferral from the NTC to the ATC only commences when the NTC activates the NTC_DAV pin.

3.2.2. NTC Mode Output Data

On receiving data across the NTC interface, the ATC commences an internal search. On finding a match for the received VPI/VCI field, the ATC activates it's ATC_DAV pin, as shown in Fig 5.

When the NTC is ready to receive the translated fields it will activate the NTC_RFD pin. On detecting an active NTC_RFD signal the ATC immediately commences the transfer of the translated field data from the ATC to the NTC via the NTC-ATC data bus, NTCD0-D7.

The ATC will drive the bi-directional NTC-ATC data bus when the ATC_DAV and NTC_RFD signal pins are both active.

Depending on the status of the TAGSEL and TSIZE pins the output data from the ATC may comprise anything from between 4 to 7 bytes, which includes 0 to 3 tag bytes together with 4 bytes for VPI/VCI. In conjunction with the aforementioned data the ATC will also transfer CLP and congestion bits as shown in Fig 5. An example of a complete NTC-ATC data transfer is illustrated in Fig 6.

3.2.3. NTC Mode Multiple Match Operation

In normal operation an incoming VPI/VCI should match one unique entry in the CAM. In Cell Stream mode this is the only permitted mode of operation. However, in NTC mode multiple matches are allowed.

In this case the ATC transfers the output data for each match sequentially on to the NTC–ATC data bus in accordance with the timing diagram shown in Fig 7.

The ATC activates it's ATC_DAV pin each time a match is detected, on completing the data transfer on the NTC–ATC data bus, the ATC recommences it's internal search mechanism to determine if any other matches are present. The ATC only activates it's ATC_RFD signal pin when the search is complete and no more matches have been detected. An example of the status of the data transfer handshake pins during a Multiple match operation is illustrated in Fig 7.

3.2.4. NTC Mode Cascade Operation

In NTC mode only, multiple ATCs can be connected together to form a larger translation table. In this case each ATC will search in parallel and hence there will be no overall increase in search time. Cascaded ATCs are also permitted to perform multiple match operations as detailed in section 3.2.3. Cascade operation is controlled by external pins CRFDI, CDAVI, and CFRDO. These pins should be interconnected as shown in Fig 8 if the cascade mode of operation is to be invoked.

3.2.5. NTC mode No match indication.

In NTC mode, the ATC indicates that no match has been detected for a particular VPI/VCI field by keeping it's ATC_DAV signal pin in it's inactive state and by re-activating it's ATC_RFD signal pin as shown in Fig 9.

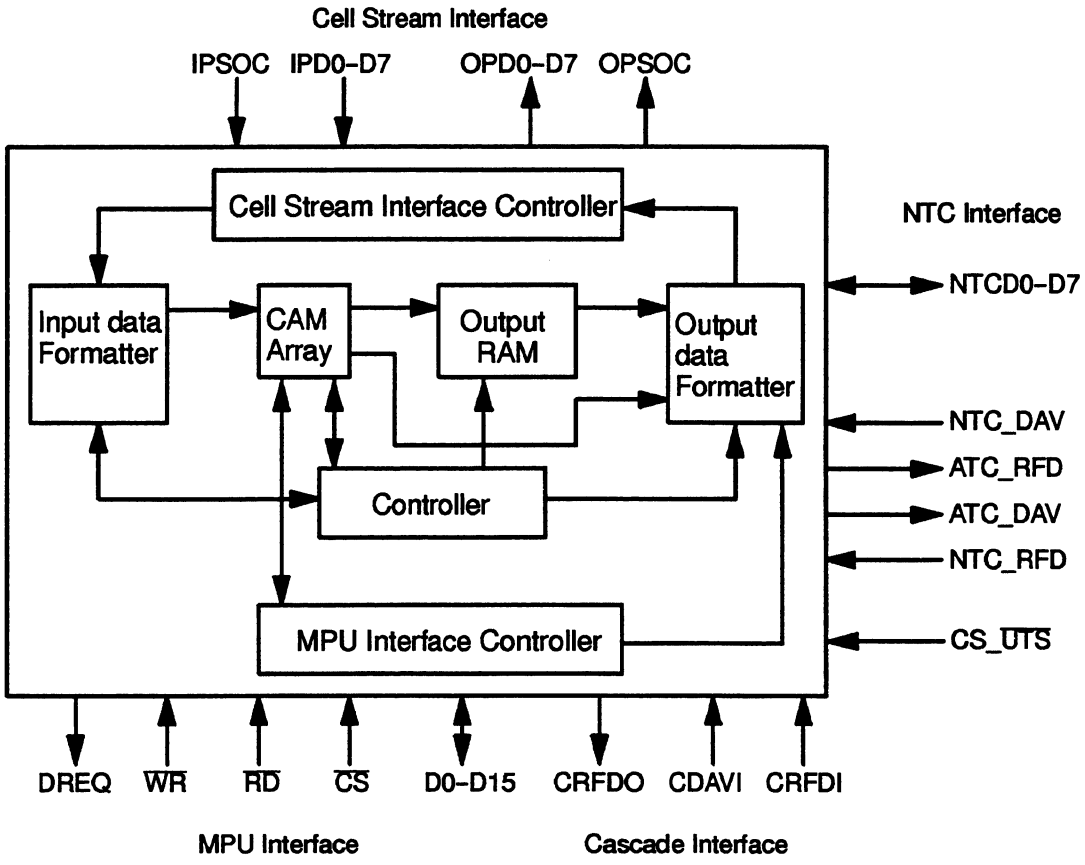


Fig 2 – ATC Block Diagram

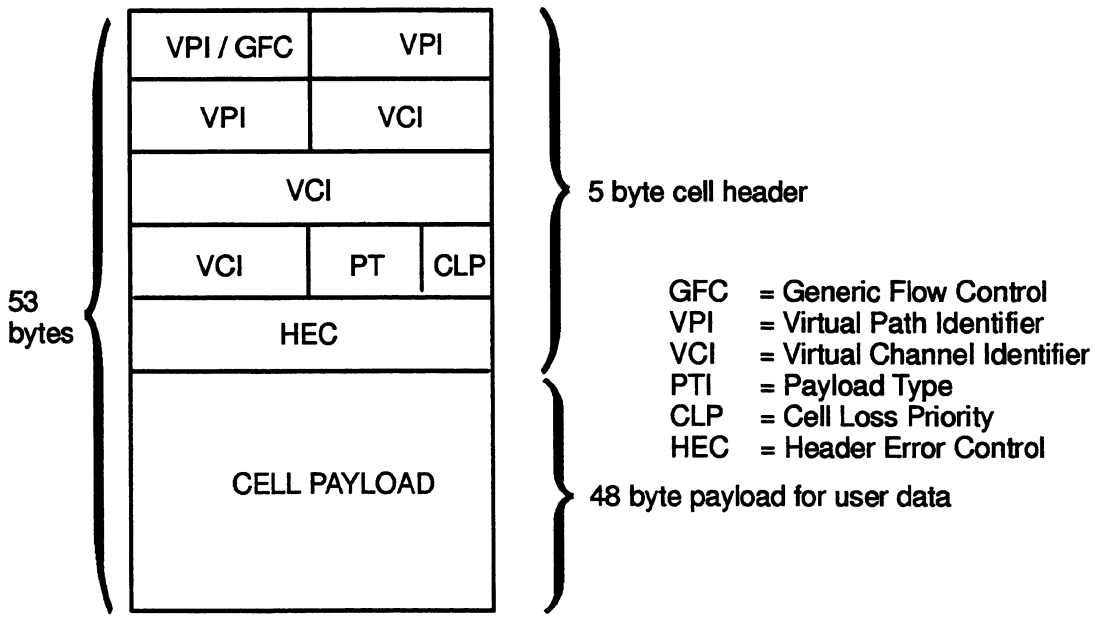


Fig 3 – ATM Cell Format

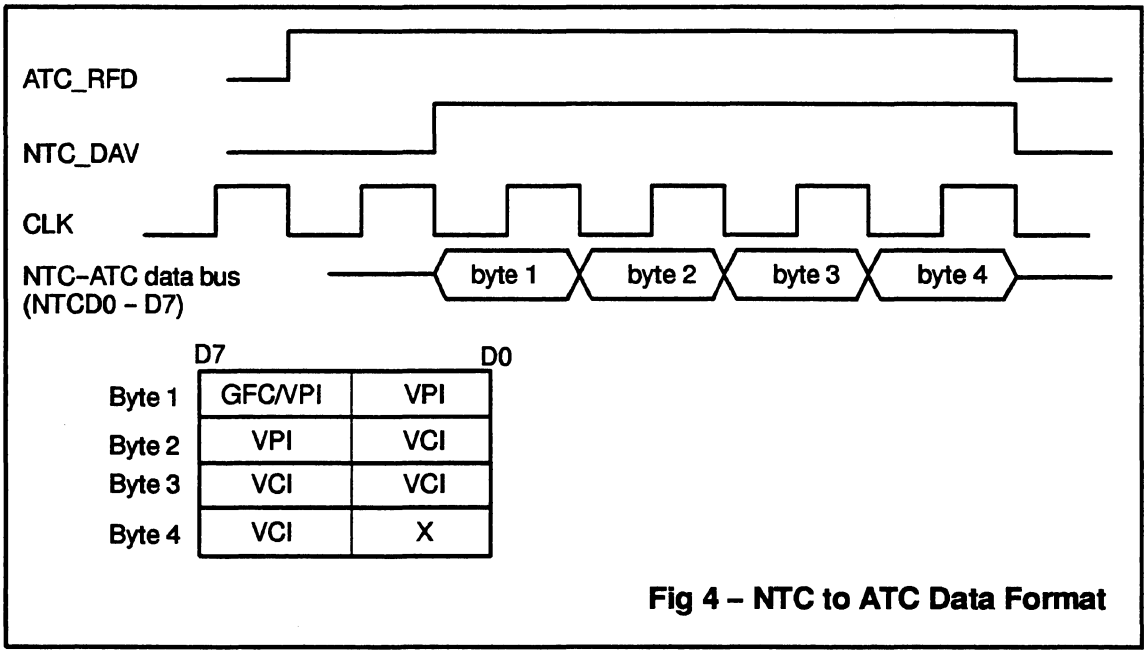


Fig 4 – NTC to ATC Data Format

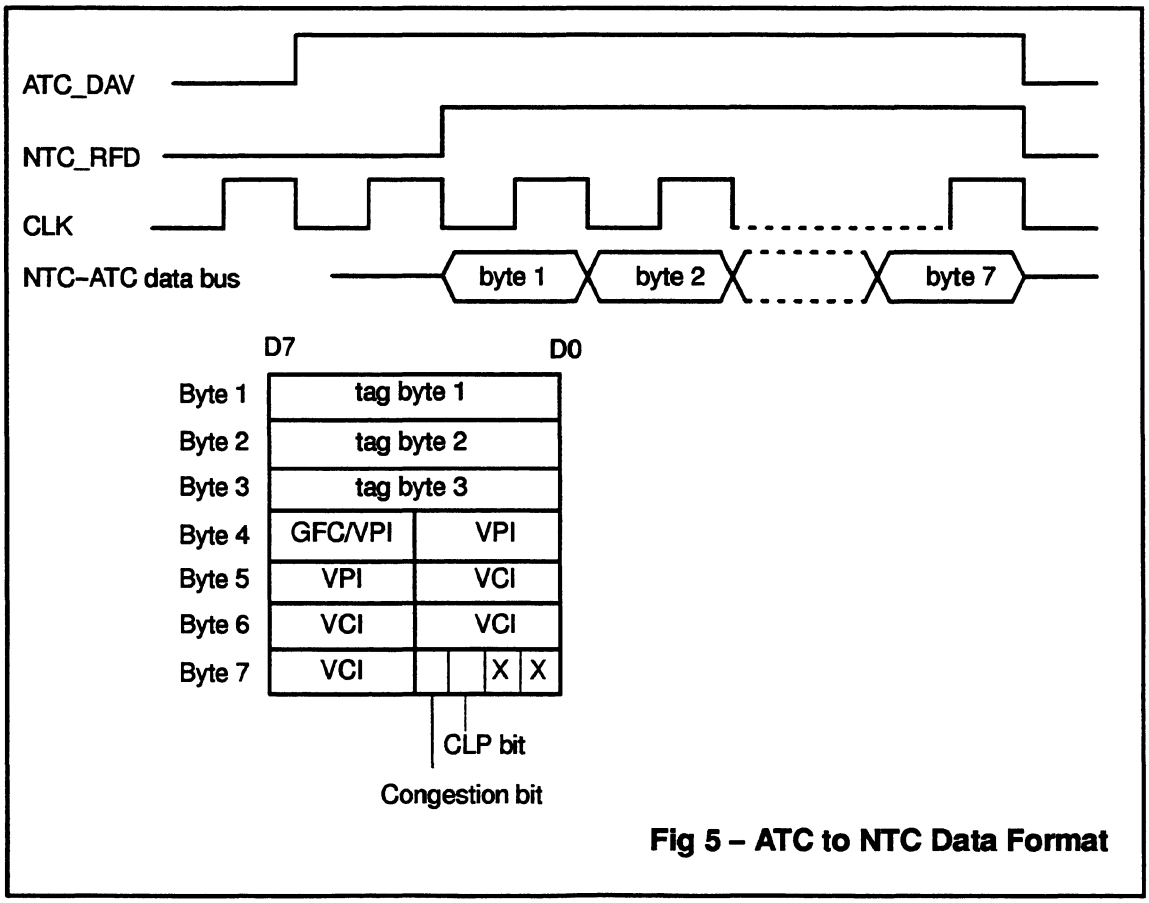


Fig 5 – ATC to NTC Data Format

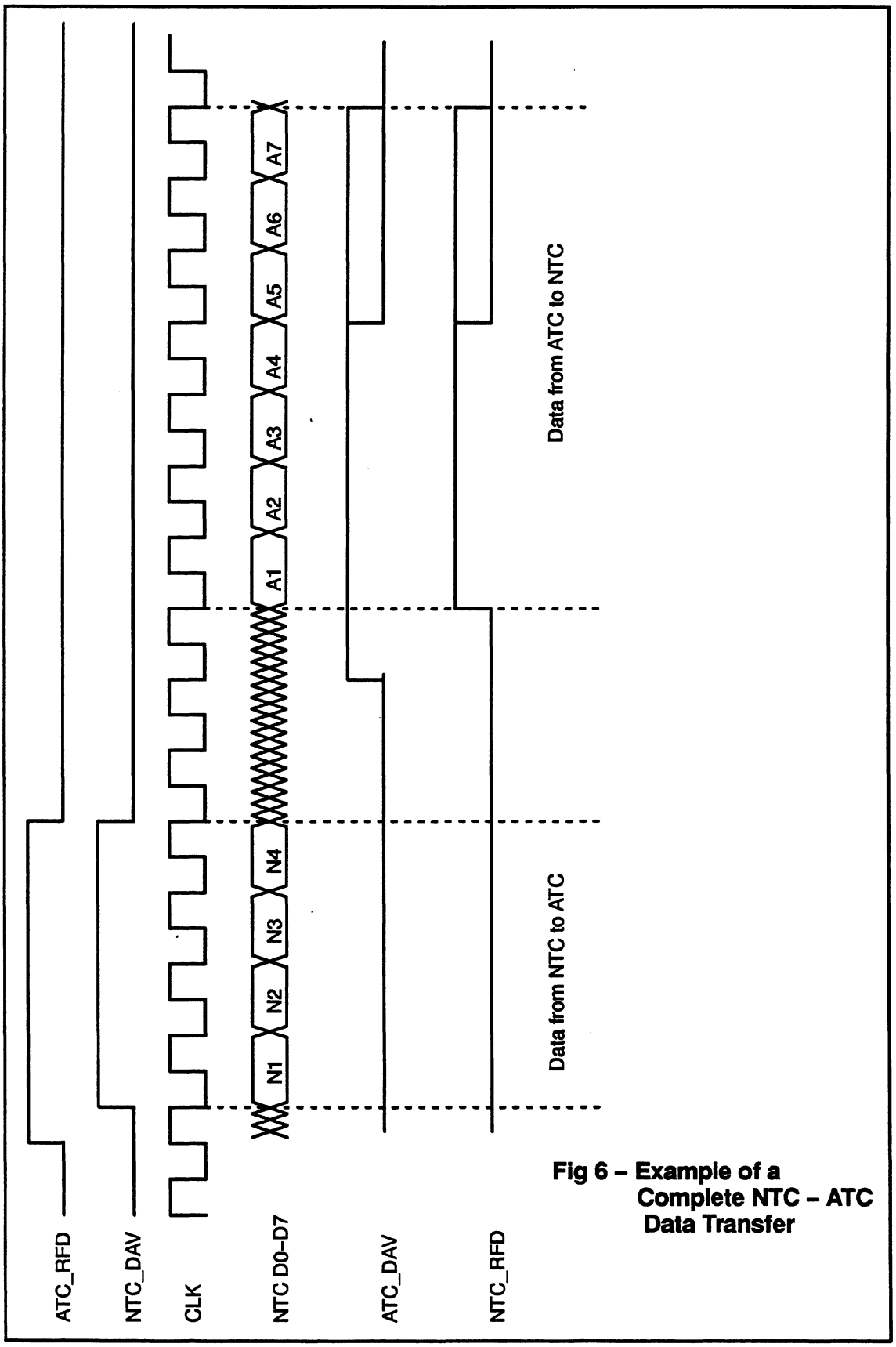


Fig 6 – Example of a Complete NTC – ATC Data Transfer

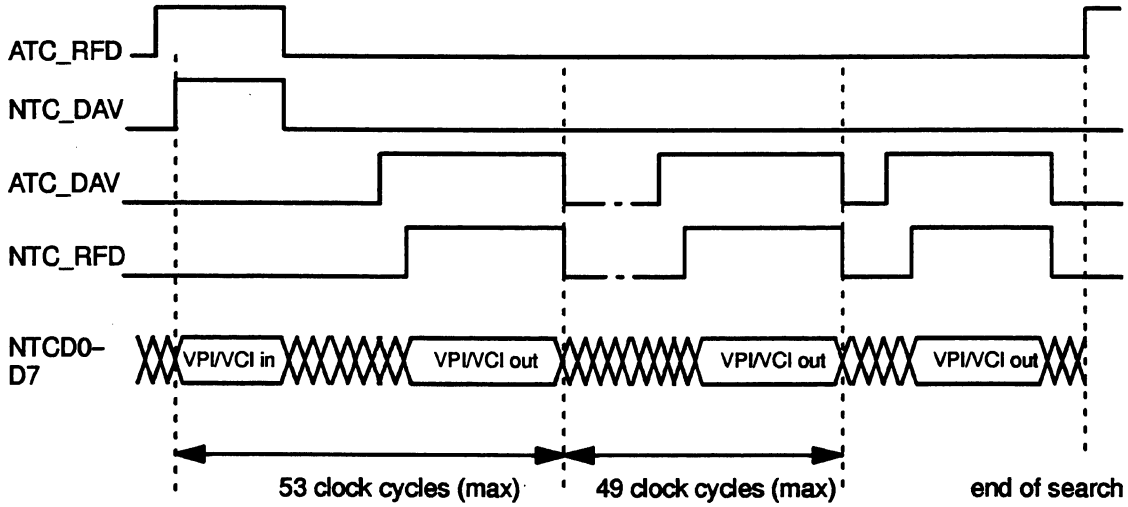


Fig 7 – Multiple Match format

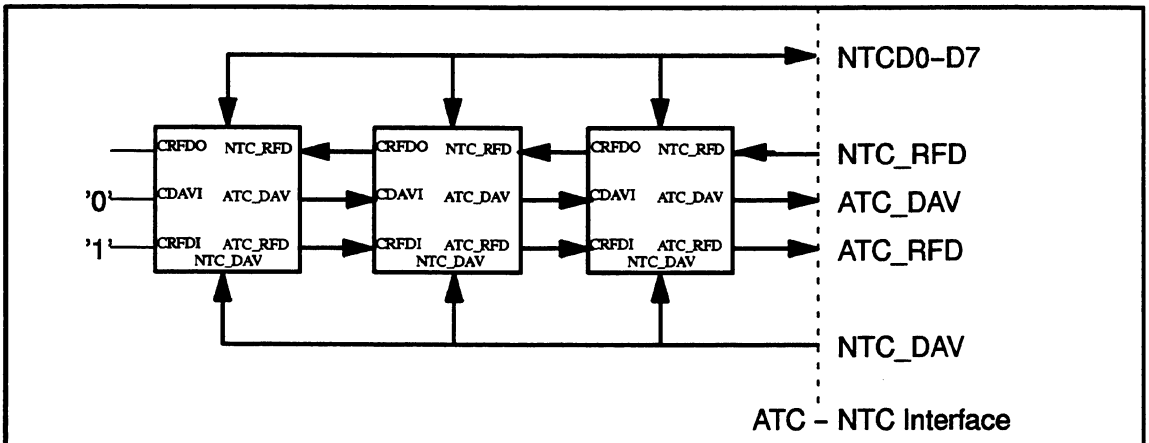


Fig 8 – Cascade Configuration

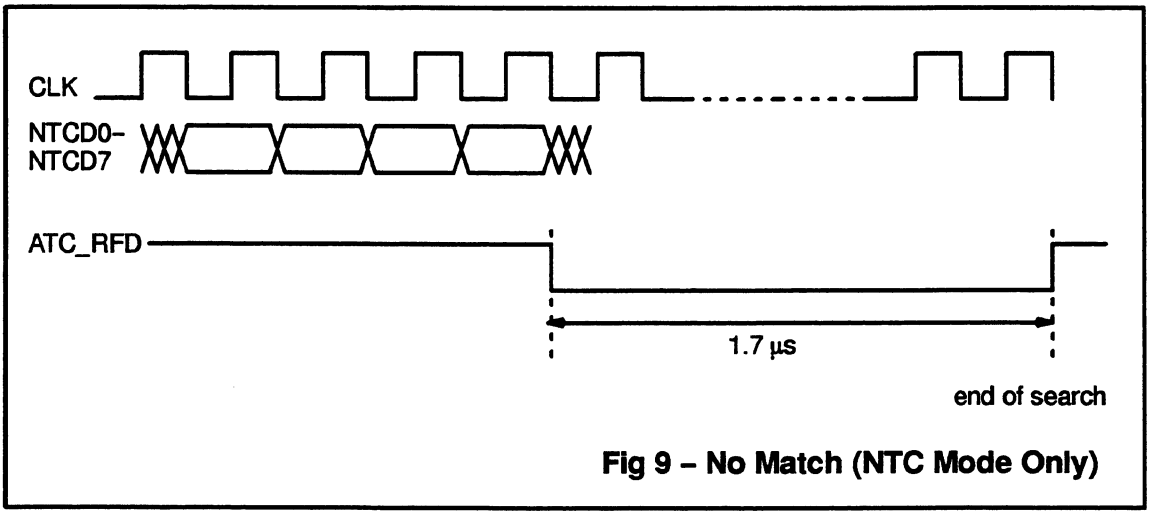


Fig 9 – No Match (NTC Mode Only)

3.3. Cell Stream Interface mode

The ATC's other interface mode, namely the Cell Stream Interface is selected by tie-ing the pin CSMODE to VDD. In Cell Stream Mode, the ATC buffers and processes complete ATM cells received across the 9-bit cell based interface.

In this Cell Stream mode the ATC buffers the payload data of incoming ATM cells, and re-constructs the outgoing cells with appropriately modified headers. In Cell Stream mode ATM cells may include between 0 to 3 tag bytes, and may include or exclude an HEC field.

If an HEC field is included then it will be re-calculated and exclusively "OR"ed with HEX 55 on transmission.

3.3.1. Cell Stream Mode

In Cell Stream mode input data is received on pins IPD0–IPD7, and output data is sent on pins OPD0–OPD7. Input data is sampled on the rising edge of the clock after activation of the IPSOC pin, which indicates the start of an ATM cell.

The first data byte is interpreted as the byte which accompanies the active IPSOC signal. The same protocol is used for data transmission, with OPSOC indicating the start of an outgoing cell.

The number of bytes which are received and transmitted by the ATC's Cell Stream interface, and the way these bytes are interpreted is dependent on the input pins; TSIZE0, TSIZE1, and HEC.

In Cell Stream mode the ATC may be configured to transmit the translated ATM cell on either the rising or the falling edge of the clock depending on the status of the CS_$\overline{\text{UTS}}$ pin. When the CS_$\overline{\text{UTS}}$ pin is tied to VDD, translated Cell Stream data is transmitted by the ATC on the falling edge of the clock. This is defined as Fujitsu Cell Stream mode.

When the CS_$\overline{\text{UTS}}$ pin is tied to VSS, translated Cell Stream data is transmitted by the ATC on the rising edge of the clock. This is defined as the UTOPIA Cell Stream mode.

The timing and format of the cell stream data for both transmission modes are illustrated in Fig 10.

3.3.2. Cell Stream mode No match operation.

The ATC's Cell Stream interface only outputs ATM cells that cause a match. ATM cells that do not cause a match are discarded by the ATC. The Cell Stream interface pins OPSOC and OPD0–D7 remain in their inactive states.

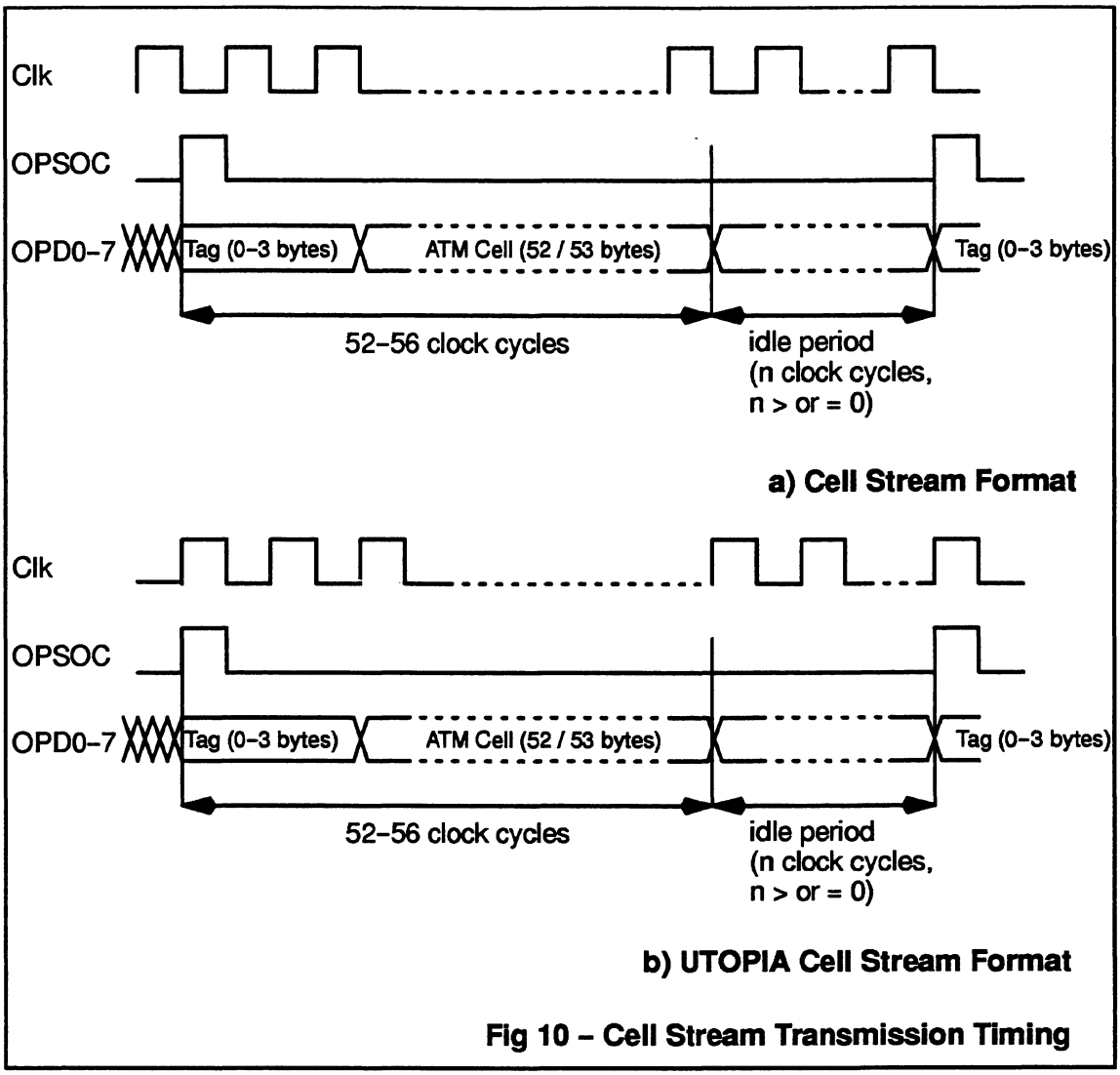


Fig 10 - Cell Stream Transmission Timing

3.4. Basic ATC Translation functions

Irrespective of the selected interface mode the following functions are provided by the ATC:-

- Generation of translated VPI/VCI address fields.
- Generation of the ATM cell routing tag bytes.
- Generation of CLP bit.
- Generation of congestion indication (indicated in PTI field).
- Generation of a 10-bit Output RAM address for UPC.

These functions are realized through a content addressable memory (CAM), together with an output RAM as illustrated in Fig 2. and summarised in Fig 11.

For each cell, the VPI/VCI field is compared against each entry in the CAM. If a match is found, then the match address is used to index the output RAM, which provides new values for the VPI/VCI, together with tag, CLP, and congestion fields.

The CAM and output RAM must be initialised by an external microprocessor, and individual entries may be updated on-the-fly. Hence the device can process a continuous cell stream at 155Mb/s. The maximum time required to complete a search and output the associated information is less than 1 ATM cell period.

Outgoing cell VPI, VCI, and CLP fields are generated directly from data stored in the output RAM. However, the outgoing PT field is formed by a combination of the incoming PT field and the congestion bit from the output RAM.

A more detailed description of the functions mentioned above is now given in the following section.

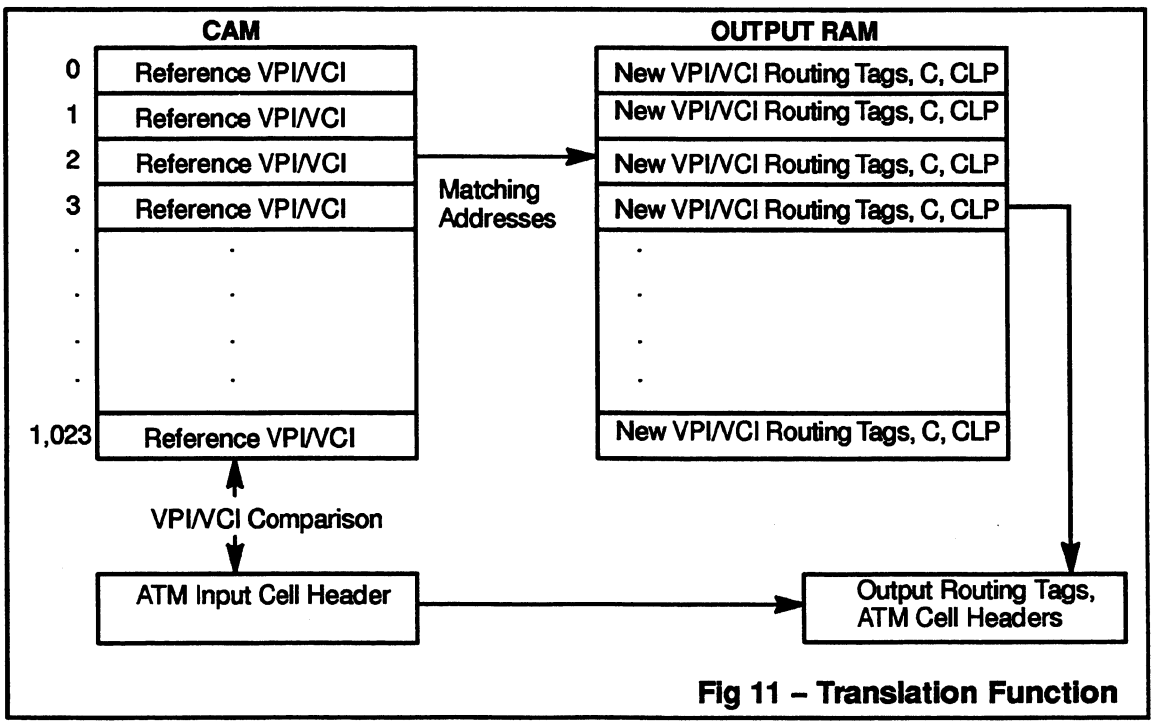


Fig 11 – Translation Function

3.4.1. Generation of translated VPI/VCI address fields

The content addressable memory section of the ATC comprises 1024 28-bit entries, where each entry represents a VPI/VCI address field. Each incoming VPI/VCI is compared against each entry in the CAM. If a match occurs, then the CAM match address will be used to index a 1024 location RAM, which contains the required output parameters.

Various mask facilities are provided, which determine which bits of the incoming VPI/VCI take part in the comparison process. The mask facilities are listed below:-

VP Mask. The first 12 bits of the cell header can be masked on a per entry basis. This allows the entire VP field to be masked and hence allows virtual circuits to be treated in a common way regardless of which VP they are contained in. This facility could be used, for example, for routing signalling VC's to a common destination using a single CAM entry. This is illustrated in Fig 12

VC Mask. The last 16 bits of the VPI/VCI field can be masked on a per entry basis. This allows the entire VC field to be masked and hence allows a complete VP to be routed with a single CAM entry. This is illustrated in Fig 14.

In the case of VP and VC masking, the associated incoming bits are ignored for comparison purposes, but are fed forward and re-combined to form the output VCI/VPI. However, in UNI mode the GFC field is always masked and these bits are not fed forward to the output.

GFC Field Translation. In UNI mode, the GFC field plays no part in the ATC's CAM Array VPI/VCI comparison operation. When operating in UNI mode the received GFC field contents are replaced by the contents of the ATC's output RAM as shown in Fig 13, irrespective of the status of the programmed VPI Mask bit.

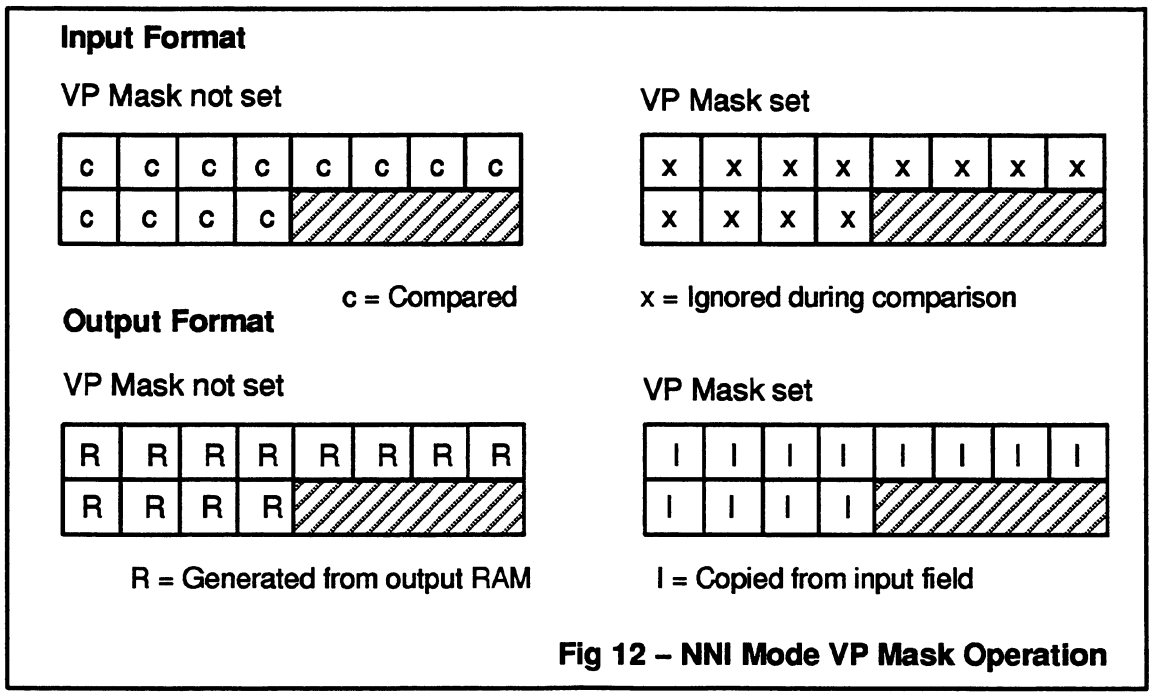


Fig 12 – NNI Mode VP Mask Operation

Input Format

VP Mask not set

(GFC Field)

x	x	x	x	c	c	c	c
c	c	c	c				

c = Compared

VP Mask set

(GFC Field)

x	x	x	x	x	x	x	x
x	x	x	x				

x = Ignored during comparison

Output Format

VP Mask not set

(GFC Field)

R	R	R	R	R	R	R	R
R	R	R	R				

R = Generated from output RAM

VP Mask set

(GFC Field)

R	R	R	R	I	I	I	I
I	I	I	I				

I = Copied from input field

Fig 13 – UNI Mode VP Mask Operation

Input Format

VC Mask not set

				c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c				

c= Compared

VC Mask set

				x	x	x	x
x	x	x	x	x	x	x	x
x	x	x	x				

x= Ignored during comparison

Output Format

VC Mask not set

				R	R	R	R
R	R	R	R	R	R	R	R
R	R	R	R				

R = Generated from output RAM

VC Mask set

				I	I	I	I
I	I	I	I	I	I	I	I
I	I	I	I				

I = Copied from input field

Fig 14 – VC Mask Operation

3.4.2. Generation of the ATM Cell Routing tag

Irespective of the selected interface mode the number of tag bytes appended to the ATM cell header is selectable via the pins TAGSEL, TSIZE0 and TSIZE1.

A maximum of 3 tag bytes may be appended to the ATM cell header and a minimum of 0 tag bytes.

In NTC mode, if TAGSEL is activated i.e by tie-ing it to VDD, the NTC interface will always append a 3 byte routing tag to the translated VPI/VCI data irrespective of the status of the input pins TSIZE0 and TSIZE1.

If the TAGSEL pin is inactive i.e tied to VSS, then irrespective of the interface mode the number of tag bytes appended to the ATM cell header is given by the status of the TSIZE0 and TSIZE1 pins. The order of tag byte transmission with respect to the status of the TSIZE pins is illustrated in Fig 15.

TSIZE1	TSIZE0	Tag byte transmission order
1	1	1 2 3
1	0	2 3
0	1	3
0	0	No Tag bytes transmitted

Fig 15 – Tag byte transmission order

3.4.3. Generation of the ATM Cell Cell Loss Priority (CLP) bit

The ATC permits a per virtual circuit CLP bit to be programmed. The CLP bit is stored in the Output RAM shown in Fig 2 and is interpretted by the ATC in the following manner.

In NTC mode, if the CLP bit for a particular virtual circuit is set to "0" in the Output RAM, then the regenerated CLP bit shown in Fig 5, is set to "0" for each translation carried out on that particular virtual circuit. If the programmed CLP bit is set to "1", then the translated CLP bit shown in Fig 5 is also set to "1".

In Cell Stream mode, if the CLP bit for a particular virtual circuit entry in the Output RAM is set to "0" then the CLP bit in the received ATM cell header is allowed to pass through the ATC untouched. If the programmed CLP bit in the Output RAM is set to "1", then CLP bit in the received ATM cell header is set to "1".

3.4.4. Generation of the ATM Cell Congestion control (C) bit

Like the CLP bit function described in the previous section, the ATC also permits per virtual circuit manipulation of the Congestion control (C) bit of the PT field shown in Fig 3. Like the programmable CLP bit the C bit is also stored in the ATC's Output RAM. Both the ATC's CLP and C bits are configurable via the ATC's microprocessor interface.

Like the CLP bit the C bit has different meanings in the NTC and Cell Stream interface modes of operation.

In NTC mode, the ATC sets the Congestion bit shown in Fig 5 equal to the per virtual circuit programmed C bit.

In Cell Stream mode, if the MSB of the received ATM cell header's PT field is set to "0" then the C bit for the received ATM

cell header's PT field is allowed to pass through the ATC untouched irrespective of the status of the ATC's Output RAM C bit.

If the MSB of the received ATM cell header's PT field is set to "1" then the ATC shall interpret the programmed C bit as follows. If the per virtual circuit programmed C bit in the Output RAM is set to "0", then the C bit for the received ATM cell header's PT field is allowed to pass through the ATC untouched irrespective of the status of the ATC's Output RAM C bit.
If the per virtual circuit programmed C bit in the Output RAM is set to "1", then Congestion bit in the received ATM cell header's PT field is set to "1". Fig 16 summarizes the C bit Cell Stream operations permissable on the received ATM cell header's PT field.

RAM	Incoming PT	Outgoing PT
C=0	P2 P1 P0	P2 P1 P0
C=1	0 P1 P0	0 1 P0
	1 P1 P0	1 P1 P0

Where P1 represents the PT field Congestion bit:
P2, P1, P0 = Incoming 3-bit PT code
C = Congestion bit in O/P RAM

Fig 16 – Cell Stream C bit summary

3.4.5. UPC Port

The 4-bit UPC port may be configured as a tri-state or as a normal output port depending upon the status of the OPCTL pin (see Section 2.2.4.). When configured as a normal output port the ATC will drive the port to Hex F. As shown in Fig 17 one clock cycle after ATC_DAV is asserted, a start nibble, Hex 0 is followed by the ATC code (set up in the Control Register – Word 1) and a 10-bit output RAM address as 3 nibbles.

A 2-bit ATC code (identifies the ATC when multiple ATC's are cascaded to form a translation table of up to 4096 entries) is concatenated with the 2 MSB's of the output RAM address to form the second nibble. The third nibble consists of the next 4 MSB's of the output RAM address and the fourth nibble consists of the remaining 4 bits of the output RAM address. The port then returns to Hex F

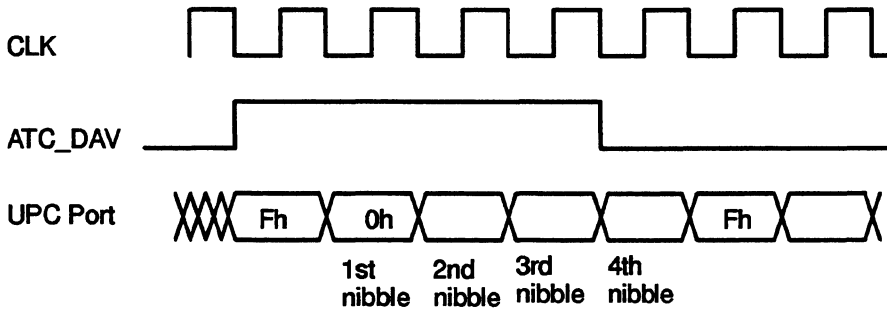


Fig 17 – UPC Port Timing

3.5. JTAG

3.5.1. Introduction

This device now contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This requires the addition of the 4 pins identified below. The JTAG circuitry is internally reset at power on, and hence the optional JTAG reset pin (TRST) is not required.

The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. The test modes are controlled by accessing an internal Test Access Port Controller (TAP), which is in turn controlled from the TAP.

3.5.2. Test Access Port (TAP)

Four pins are dedicated to JTAG:
TDO; TDI; TMS & TCK.
The functions of these signals are described in Section 2 of this datasheet.

3.6. Test Instructions

The following JTAG instructions are implemented :-

BYPASS
SAMPLE/PRELOAD
EXTEST
INTEST

BYPASS

The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows more rapid movement of test data through the components of the board, bypassing the ones that do not need to be tested. The BYPASS operation enables the bypass register, which is a single stage shift register, between TDI and TDO.

1. The binary code for the BYPASS instruction is 11.

2. The BYPASS instruction is forced into the instruction register output latches during the Test_Logic_Reset state. Note the distinction between the "01" content of the instruction shift register and the "11" of the instruction register output latch. Therefore, at the start of the instruction-shift cycle, a "01" pattern will be seen instead of "11".

3. The BYPASS operation does not interfere with the component operation at all. If the TDI input trace to the component is somehow disconnected, the test logic will see a "11" at TDI input during the instruction-shift state. Therefore, no unwarranted interference with the on-chip system logic occurs.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to sample the state of the component pins. The sampled values can be examined by shifting out the data through TDO. This instruction selects the boundary scan-cell output latches with specific values. The preloaded values are then enabled to the output pins by the EXTEST.

1. The binary code for the instruction is 01.

2. The SAMPLE/PRELOAD instruction selects the boundary-scan cells to be connected between TDI and TDO in the Shift_DRTAP controller state.

3. The values of the component pins are sampled on the rising edge of TCK in the Capture_DR TAP controller state.

4. The preload values shifted in the boundary-scan cells are latched into the boundary-scan output latch at the falling edge of TCK in the Update_DR TAP controller state.

EXTEST

EXTEST instruction allows testing of off-chip circuitry and board level interconnections. The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages. Then, the EXTEST instruction enables the preloaded values to the components output pins.

1. The binary code for the instruction is 00.

2. The device outputs the preloaded data to the pins at the falling edge of TCK in the Update_IR TAP controller state at which point the JTAG instruction register is updated with the EXTEST.

3. The EXTEST instruction selects the boundary-scan cells to be connected between TDI and TDO in the SHIFT-DR test logic controller state.

4. Once the EXTEST instruction is effective, the output pins can change at the falling edge of TCK in the Update_DR TAP controller state.

INTEST

This instruction allows testing of the on-chip system logic. Test stimuli are shifted in, one at a time, and applied to the on-chip logic. The test results are captured into the boundary-scan register (BSR) and are examined by subsequent shifting. The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages prior to INTEST being selected.

The binary code for the instruction is 10.

4. DEVELOPERS NOTES

4.1. Programming and Control

4.1.1. Introduction

The ATC provides a 16 bit bi-directional microprocessor interface. The microprocessor permits entries in the ATC's CAM and Output RAM to be updated on the fly without affecting the translation process. The operation of the ATC's processor interface is controlled via 4 single bit pins: $\overline{CS}$, DREQ, $\overline{WR}$ and $\overline{RD}$.

Immediately following an active low transition on the $\overline{RESET}$ pin, the ATC activates an internal initialisation sequence. During this operation the contents of the CAM are completely cleared. The whole operation takes approximately 68 clock cycles and is designated to be complete when the DREQ signal pin becomes active as shown in Fig 18.

On DREQ becoming active the user is now at liberty to configure the ATC's CAM and Output RAM structures as required via the microprocessor interface.

4.1.2. Updating ATC CAM / Output RAM entries

The ATC provides 7 write only control registers to enable the user to configure the ATC's CAM and Output RAM structures.

Individual entries are updated by carrying out 7 write operations to the control registers shown in Appendix B Fig 20. No addressing mechanism is required to carry out this operation since the ATC updates these registers on successive write operations. All write operations must be qualified by the ATC's $\overline{CS}$ pin being in it's active low state.

The ATC is responsive to the seventh write operation and on detecting this operation the ATC will deactivate it's DREQ pin and commence entry update operations in parallel to both the CAM and Output RAM structures simultaneously, thereby minimizing the time required to carry out an update.

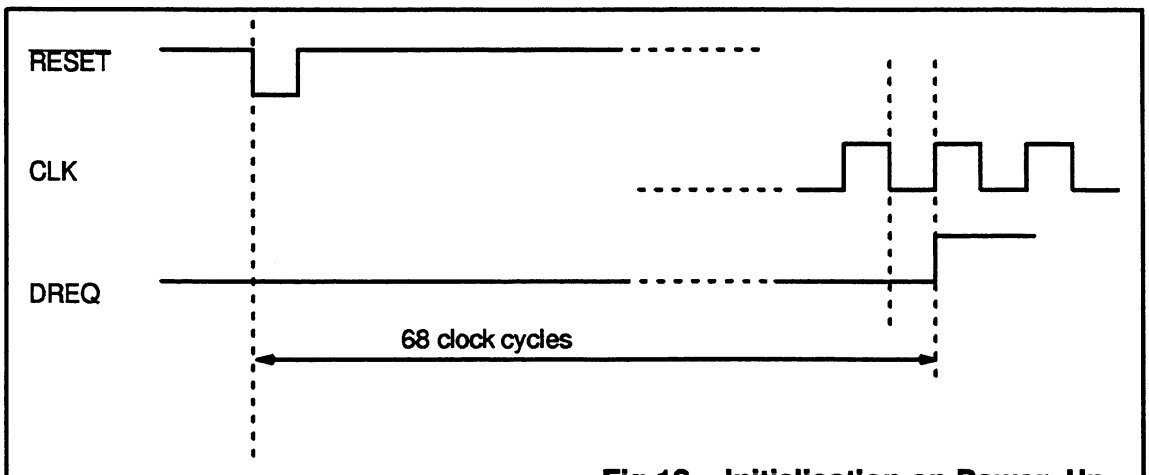


Fig 18 – Initialisation on Power-Up

Update requests are only carried out instantly when no translation processes are currently being activated. In the case where a translation process is currently in progress and an entry update request is received, the ATC will complete it's translation process and then service the update request. During this non service interval the DREQ pin remains in it's inactive low state permitting no more update requests to be carried out until the current one has been serviced. The servicing of an update request by the ATC is signified by the ATC's DREQ pin returning to it's active state.

As shown in Appendix B Fig 20 the CAM Address and control register permits the ATC's CAM and Output RAM structures to be programmed with the same match and translation values for each and every entry. This unique configuration mode is activated by setting the I bit in the CAM Address and control register. On carrying out the seventh write operation the ATC will commence updating all 1024 entry locations in both the CAM and Output RAM simultaneously. Once all 1024 locations have been initialised, the I bit is reset internally by the ATC and the DREQ pin and status bit are both activated.

The format of all the internal control registers is illustrated in Appendix B Fig 20. A description of each register is contained in the following paragraphs.

4.1.3. Status Register

The status register may be used as a means of obtaining the original VPI/VCI. On a match being found the ATC_DAV bit in the status register will be activated indicating that the 10 bit address of the match location is available. This may be used as a pointer to a copy of the CAM table kept in in software external to the ATC. The Status Register format is illustrated in Appendix B Fig 19.

4.1.4. Control Word 1

This register identifies the CAM entry which is to be programmed. Bits A0 through A9 uniquely identify one of 1024 possible locations. In addition, this register includes two control bits, I and NU.

ID Code (ID0–ID1)
The two ID code bits, ID0–ID1, permit the user to identify which ATC is currently carrying out a translation when ATCs are cascaded together as described in section 3.2.4. The two bit ATC ID code is presented at the UPC output port pins when a successful match has been detected and the translation process initiated. The ID code is interpretted as follows :–

ID1	ID0	Translating ATC
0	0	ATC 1
0	1	ATC 2
1	0	ATC 3
1	1	ATC 4.

Initialisation (I bit)
This bit invokes an internal initialisation sequence which will program each entry with the parameters defined in control words 2 through 7. The initialisation sequence will commence after control word 7 is written to the ATC. Completion of the initialisation sequence will be indicated by activation of the DREQ pin / status register bit.

Network/User Select (NU bit)
This bit selects between UNI and NNI ATM cell formats. The only difference between the two is the way in which the

first 4 header bits are processed. In UNI mode (NU=0) the first 4 bits will always be masked, but in NNI mode masking is determined solely by the VPM bit in control word 3.

4.1.5. Control Word 2

This register defines the VCI value which is to be programmed into the CAM at the associated entry address. Incoming VCIs will be compared against the VCI value in each active CAM entry.

4.1.6. Control Word 3

This register defines the VPI value which is to be written into the associated entry address, together with various control information which is to be associated with the entry. The least significant 12 bits define a VPI value, but the most significant 4 bits will automatically be masked in UNI mode and hence will be ignored. Control bit functions are described below.

Enable bit (E)
This bit enables the individual CAM entry. No match will be generated for entries which are not enabled.

Virtual Path Mask (VPM)
This bit controls whether the VP field of the associated entry is to be masked or not. If the VP field is masked then it will be excluded from the comparison process (ie. any VPI will cause a match).

Virtual Channel Mask (VCM)
This bit controls whether the VC field of the associated entry is to be masked or not. If the VC field is masked then it will be excluded from the comparison process (ie. any VCI will cause a match).

4.1.7. Control Word 4

This register defines a new VCI value which will be generated when a match occurs at the associated entry address.

4.1.8. Control Word 5

This register defines a new VPI value which will be generated when a match occurs at the associated entry address.

4.1.9. Control Words 6 and 7

These registers define three tag bytes which may be appended to the start of each cell by the ATC or NTC. The order of transmission is as follows:-

Tag Size	Order
0	not applicable
1	byte 3 only
2	byte 2, byte 3
3	byte 1, byte 2, byte 3

Control word 7 also includes two control bits as described below.

Congestion (C)
This bit may be used to indicate congestion for the associated entry. When this bit is set to '1' the ATC or NTC will modify the PT field in the ATM cell header in order to indicate congestion, see section 3.4.4. for a more complete description on the usage of this control bit.

Cell Loss Priority (CLP)
This bit defines the state of the CLP bit which will be inserted into the outgoing ATM cell header by the ATC or NTC, see section 3.4.3. for a more complete description on the usage of this control bit..

A – REGISTER TABLE

ADDRESS	TYPE	FUNCTION	REF
N/A	RO	Status Register	Fig 19
		Control Registers	Fig 20
N/A	WO	Word 1: CAM Address & Control	
N/A	WO	Word 2: VCI Match	
N/A	WO	Word 3: VPI Match & Control	
N/A	WO	Word 4: VCI Output	
N/A	WO	Word 5: VPI Output	
N/A	WO	Word 6: Tag Output Low	
N/A	WO	Word 7: Tag Output High	

B – REGISTER MAP

Status Register

D15

X	X	X	X	DAVO	MA9	MA8	MA7
MA6	MA5	MA4	MA3	MA2	MA1	MA0	DREQ

D0

Match address (MA0-9) qualified when ATC_DAV goes active

ATC_DAV: Mimics external ATC_DAV pin
0: No match found
1: Match found

DREQ: Mimics external DREQ pin
0: Update in progress
1: Update complete

Fig 19 – Status Register Format

Word 1: CAM Address & Control

D15

X	X	ID1	ID0	I	NU	A9	A8
A7	A6	A5	A4	A3	A2	A1	A0

D0

I: 0 = Normal Operation
1 = Initialise

NU: 0 = UNI Mode
1 = NNI Mode

Word 2: VCI Match

D15

VCI15	VCI14	VCI13	VCI12	VCI11	VCI10	VCI9	VCI8
VCI7	VCI6	VCI5	VCI4	VCI3	VCI2	VCI1	VCI0

D0

Word 3: VPI Match & Control

D15

X	E	VPM	VCM	VPI/GFC
VPI				

D0

E : 0 = Location disabled
1 = Location enabled

VPM : 0 = Not masked
1 = Masked

VCM : 0 = Not masked
1 = Masked

Word 4 VCI Output

D15

VCI15	VCI14	VCI13	VCI12	VCI11	VCI10	VCI9	VCI8
VCI7	VCI6	VCI5	VCI4	VCI3	VCI2	VCI1	VCI0

D0

Word 5: VPI Output

D15

X	X	X	X	VPI/GFC
VPI				

D0

Word 6: Tag Output low

D15

Tag Byte 2
Tag Byte 3

D0

Word 7: Tag Output High

D15

X	X	X	X	X	X	C	CLP
Tag Byte 1							

C = Output Congestion bit CLP = Output CLP bit

D0

Fig 20 – Control Registers and Format

C – RATINGS

C1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Values		Units
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	-0.5	6.0	V
Input Voltage	V_{DIN}	-0.5	$+V_{DD}+0.5$	V
Output Voltage	V_{O1}	-0.5	$+V_{DD}+0.5$	V
Input Current	I_{MAX}	-10.0	10.0	µA
Storage Temperature	T_{STG}	-40	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C2. DC CHARACTERISTICS

Parameter	Symbol	Pin	Test Condition	Value			Units
				Min.	Typ.	Max.	
Positive Supply Voltage	V_{DD}		+4.75	+4.75	+5.0	+5.25	V
Positive Supply Current	$+I_{VS}$		Static no load	-	-	100	µA
Input High Voltage (TTL)	V_{IH}			2.2	-	+VDD	V
Input Low Voltage (TTL)	V_{IL}			0	-	0.8	V
Input Leakage Current	I_L		$0<=V_i<=+V_{DD}$	-10	-	10	µA
Output Low Voltage	V_{OL}		I_{OL}=3.2mA	VSS	-	0.4	V
Output high Voltage	V_{OH}		I_{OH}=-2mA	4.2	-	VDD	V
Output Off Leakage Current	I_{LO}			-10	-	10	µA
Input Pin Capacitance	C_{in}			-	-	8	pF
Output Pin Capacitance	C_{out}			-	-	16	pF
I/O Pin Capacitance	$C_{i/o}$			-	-	21	pF
Operating Temperature	T_A			0	-	+70	°C
Power Dissipation (operating)	P_O		@20MHz		220		mW

D – AC CHARACTERISTICS

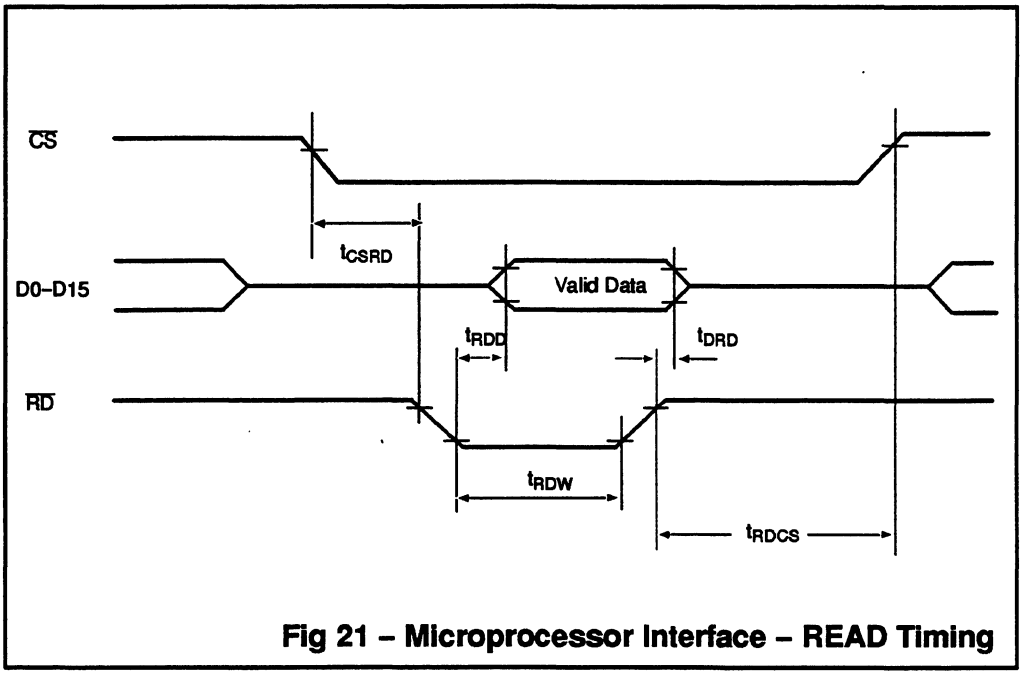


Fig 21 – Microprocessor Interface – READ Timing

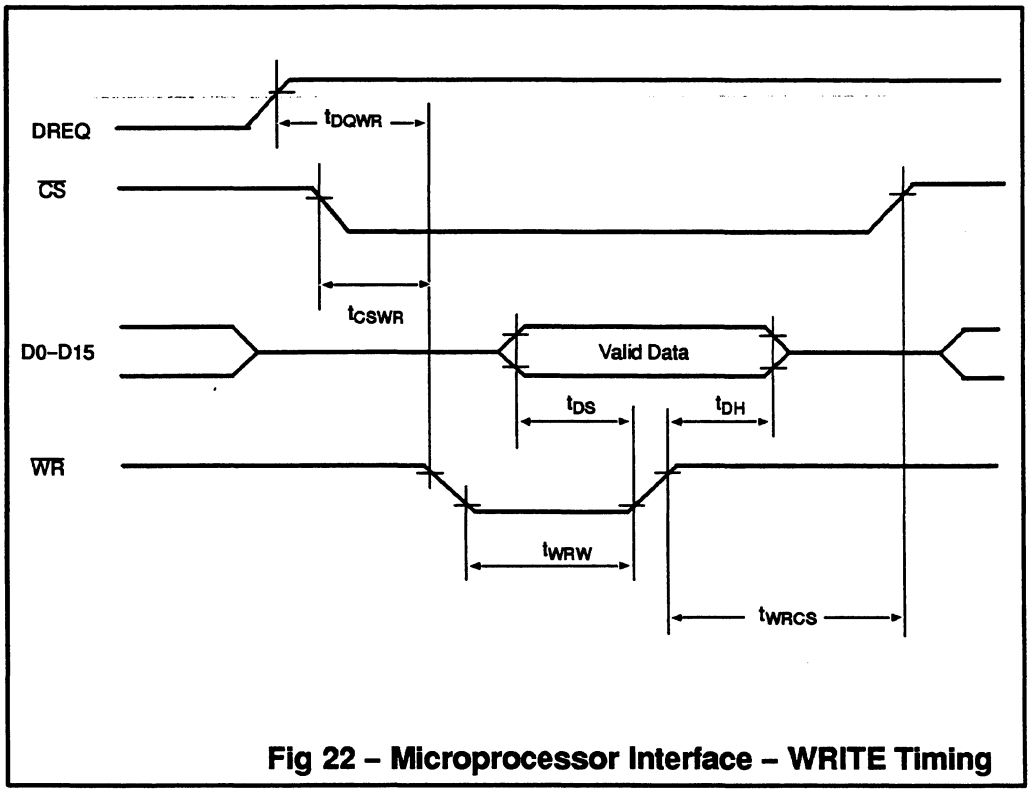


Fig 22 – Microprocessor Interface – WRITE Timing

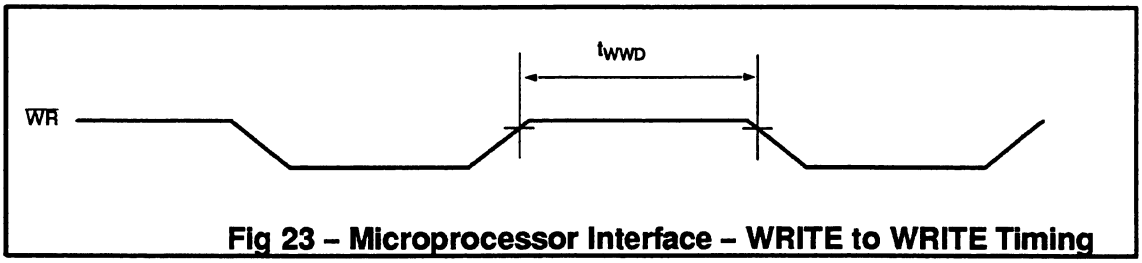


Fig 23 – Microprocessor Interface – WRITE to WRITE Timing

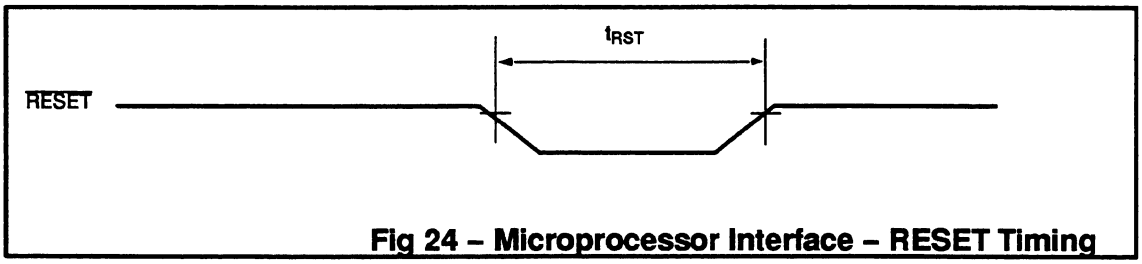


Fig 24 – Microprocessor Interface – RESET Timing

Parameter	Ref Signal	Abrev	Values			Units
			Min	Typical	Max	
Reset Pulse Width	$\overline{RESET}$	t_{RST}	100			ns
Read Pulse Width	$\overline{RD}$	t_{RDW}	30			ns
CS Valid to Read Active	$\overline{RD}$	t_{CSRD}	0			ns
Read Active to Valid Data	$\overline{RD}$	t_{RDD}			20	ns
Read Inactive to Invalid data	$\overline{RD}$	t_{DRD}	5		30	ns
Read Inactive to CS Inactive	$\overline{RD}$	t_{RDCS}	0			ns
DREQ Active to Write Active	$\overline{WR}$	t_{DQWR}	100			ns
Write Pulse Width	$\overline{WR}$	t_{WRW}	30			ns
CS Valid to Write Active	$\overline{WR}$	t_{CSWR}	0			ns
Data Setup Time	$\overline{WR}$	t_{DS}	10			ns
Data Hold Time	$\overline{WR}$	t_{DH}	0			ns
Write Inactive to CS Inactive	$\overline{WR}$	t_{WRCS}	0			ns
Write to Write Delay	$\overline{WR}$	t_{WWD}	30			ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 1 – Microprocessor Interface – AC Timing

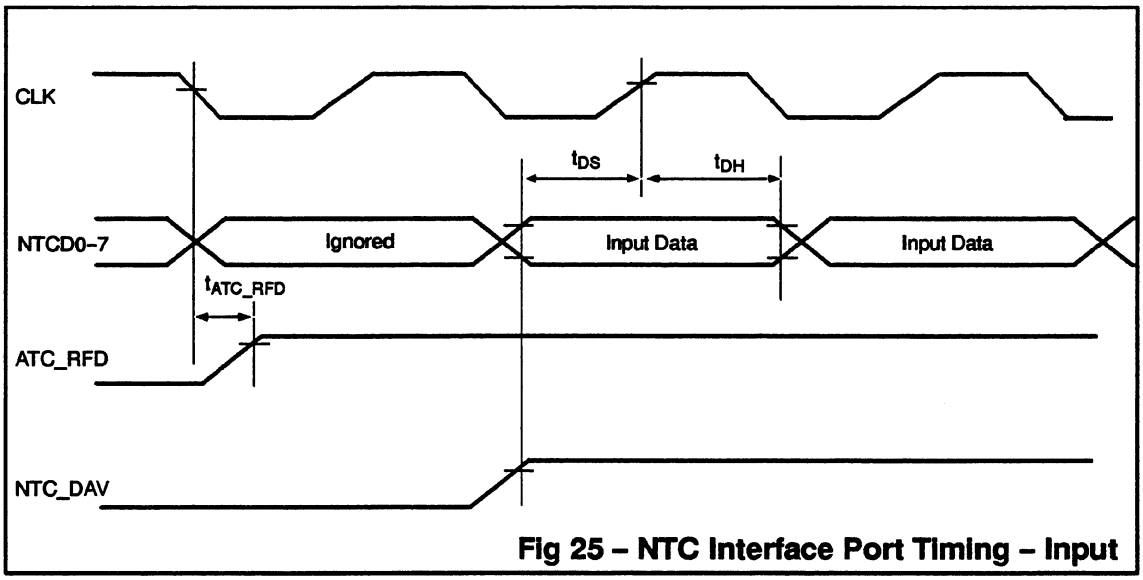


Fig 25 – NTC Interface Port Timing – Input

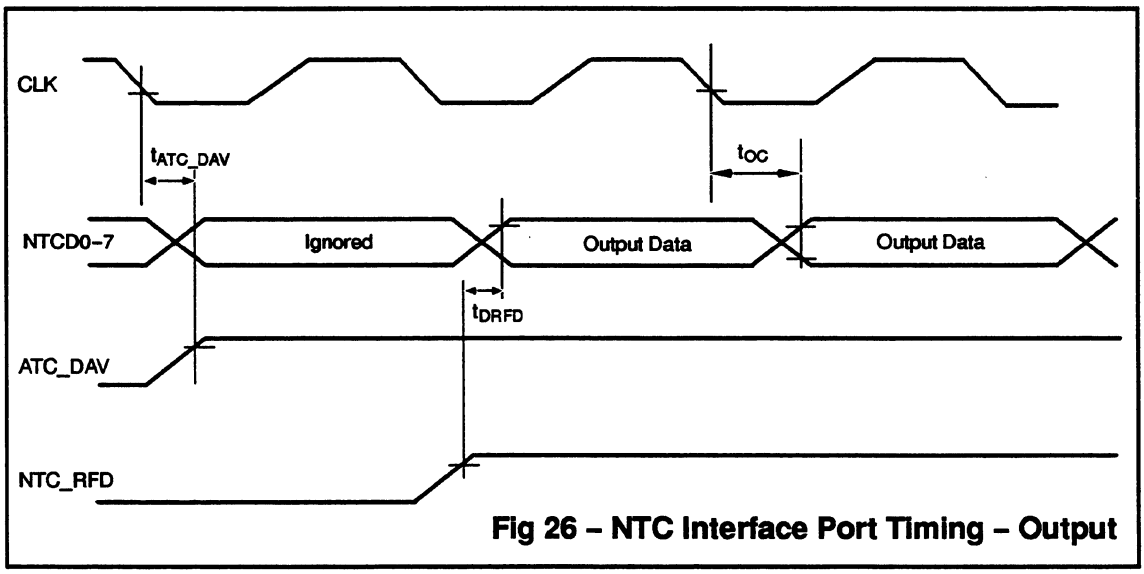


Fig 26 – NTC Interface Port Timing – Output

Parameter	Ref Signal	Abrev	Values			Units
			Min	Typical	Max	
ATC_RFD delay	ATC_RFD	t_{ATC_RFD}	5			ns
Data Setup time	NTCD0-7	t_{DS}				ns
Data Hold Time	NTCD0-7	t_{DH}				ns
DAVO Delay	ATC_DAV	t_{ATC_DAV}	6			ns
Data Out Delay to NTC_RFD	NTCD0-7	t_{DRFD}				ns
Data Out delay to Clock	NTCD0-7	t_{OC}	8			ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 2 – NTC Interface – AC Timing

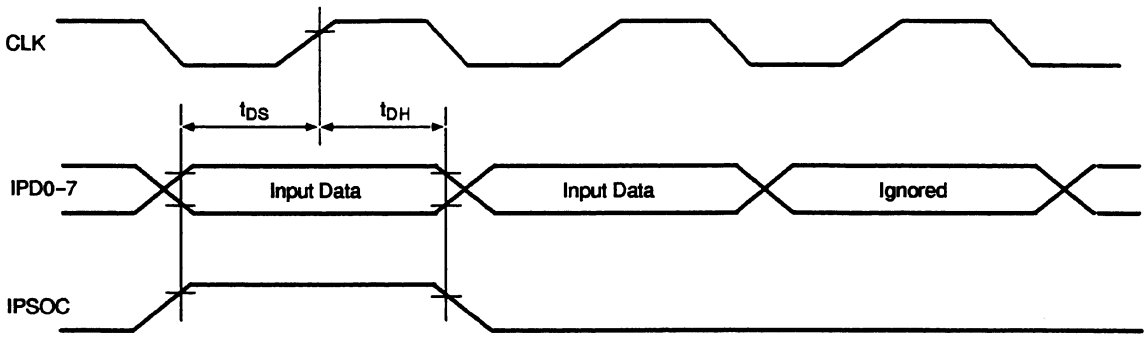


Fig 27 – Cell Stream Interface Transmit Port Timing

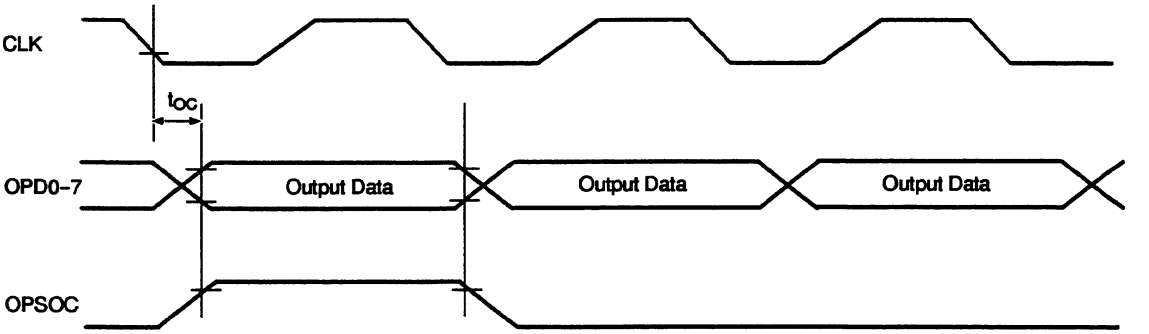


Fig 28 – Cell Stream Interface Receive Port Timing

Parameter	Ref Signal	Abrev	Values			Units
			Min	Typical	Max	
Data Setup Time	IPD0–7	t_{DS}				ns
Data Hold Time	IPD0–7	t_{DH}				ns
Data Out Delay to clock	IPD0–7	t_{OC}	8			ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 3 – Cell Stream Interface – AC Timing

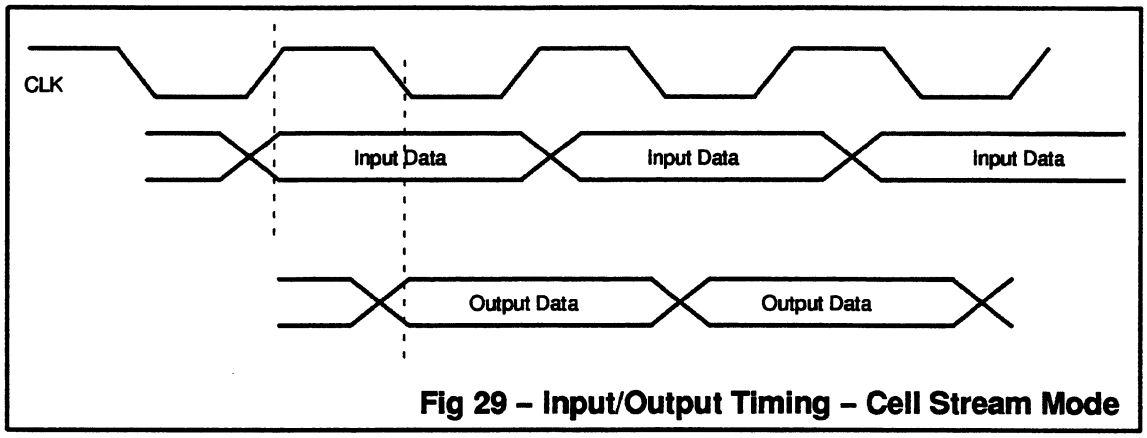


Fig 29 – Input/Output Timing – Cell Stream Mode

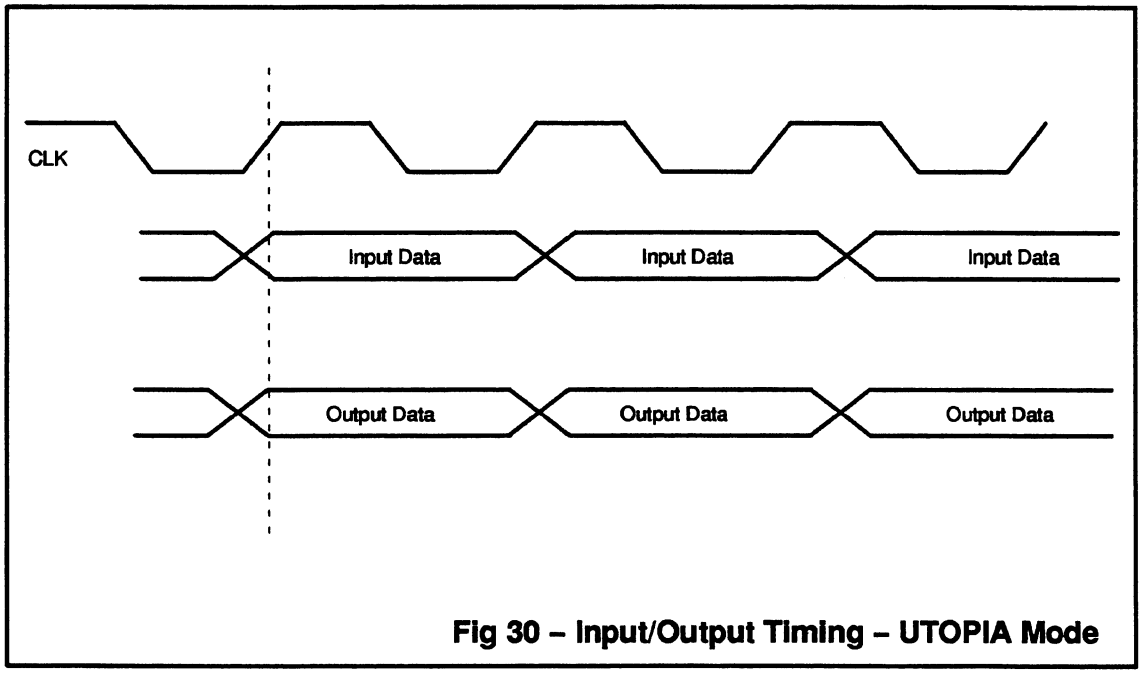


Fig 30 – Input/Output Timing – UTOPIA Mode

E - JTAG

E 1. JTAG Boundary Scan Cells

The Boundary Scan Register (BSR) consists of 95 registers, which form a serial shift register starting from pin 1 (DREQ), moving in an anticlockwise direction around the chip to finish at pin 80 (CLK).

It should be noted that none of the internal D-types which form the BSR are reset,and hence are initially undefined. A valid pattern needs to be shifted into the register prior to any testing. However, while the JTAG TAP controller is reset, the I/O pins are connected through to the system logic.

I / O Pin Type:

I = Input
C = Clock input
O = Output
B = Bidirectional,
T = Tristate
Iu = Input with pull-up resistor.

BSR Cell Type:

BSI1 allows capture of device input pin and control of logic input pin.
BSI3 allows capture of device input pin only.
BSO allows capture of logic output pin and control of device output pin (= BSI1).
BSOE allows control of tristate-able output pin (presettable).
BSDI allows control of bidirectional pin (= BSOE).
BSBI allows capture and control of bidirectional input and output pin (= BSI1 + BSO).

Control Group No.: Denotes a JTAG BSR cell which controls a (group of) tristate-able output(s) or bidirectional pin(s).

Controlled Group No.: Denotes a JTAG BSR cell which connects to a tristate-able output or bidirectional pin which is controlled by the JTAG BSR cell numbered in the previous column.

Pin No.	Pin Name	Pin Type	BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.
1	DREQ	T	1	BSO		1
			2	BSOE	1	
3	D0	B	33 & 34	BSBI		2
4	D1	B	31 & 32	BSBI		2
5	D2	B	29 & 30	BSBI		2
6	D3	B	27 & 28	BSBI		2
7	D4	B	25 & 26	BSBI		2
8	D5	B	23 & 24	BSBI		2
9	D6	B	21 & 22	BSBI		2
10	D7	B	19 & 20	BSBI		2
11	D8	B	17 & 18	BSBI		2
13	D9	B	15 & 16	BSBI		2
14	D10	B	13 & 14	BSBI		2
15	D11	B	11 & 12	BSBI		2
16	D12	B	9 & 10	BSBI		2
17	D13	B	7 & 8	BSBI		2
18	D14	B	5 & 6	BSBI		2
19	D15	B	3 & 4	BSBI		2
			35	BSDI	2	
20	$\overline{RD}$	I	36	BSI1		
21	$\overline{WR}$	I	37	BSI1		
22	$\overline{CS}$	I	38	BSI1		
24	CS_UTS	Iu	39	BSI1		
25	DRFDI	I	40	BSI1		
26	CDAVI	I	41	BSI1		
27	CRFDO	I	42	BSO		
28	RES	Iu				
29	TCK	C				
30	TMS	I				
31	TDI	I				
32	TDO	T				
34	TAGSEL	I	43	BSI1		
35	UPCO_0	T	44	BSO		3
			45	BSOE	3	
36	TEST	I	46	BSI1		
37	NTC_DAV	I	47	BSI1		
38	NTC_RFD	I	48	BSI1		
39	ATC_DAV	O	49	BSO		
40	ATC_RFD	O	50	BSO		
41	$\overline{RESET}$	I	51	BSI1		
43	UPCO_1	T	52	BSO	3	3

44	OPD7	O	53	BSO		
45	OPD6	O	54	BSO		
46	OPD5	O	55	BSO		
47	OPSOC	O	61	BSO		
48	OPD4	O	56	BSO		
49	OPD3	O	57	BSO		
50	OPSD2	O	58	BSO		
51	OPD1	O	59	BSO		
53	OPD0	O	60	BSO		
54	UPCO_2	T	62	BSO	3	3
55	UPCO_3	T	63	BSO	3	3
56	NTCD7	B	64 & 65	BSBI		4
57	NTCD6	B	66 & 67	BSBI		4
58	NTCD5	B	68 & 69	BSBI		4
59	NTCD4	B	70 & 71	BSBI		4
60	NTCD3	B	72 & 73	BSBI		4
61	NTCD2	B	74 & 75	BSBI		4
62	NTCD1	B	76 & 77	BSBI		4
64	NTCD0	B	78 & 79	BSBI		4
			80	BSDI	4	
65	IPD0	I	88	BSI1		
66	IPD1	I	87	BSI1		
67	IPD2	I	86	BSI1		
68	IPD3	I	85	BSI1		
69	IPD4	I	84	BSI1		
70	IPSOC	I	89	BSI1		
71	IPD5	I	83	BSI1		
72	IPD6	I	82	BSI1		
74	IPD7	I	81	BSI1		
75	TSIZE0	I	91	BSI1		
76	TSIZE1	I	90	BSI1		
77	HEC	I	92	BSI1		
78	CSMODE	I	93	BSI1		
79	OPCTL	I	94	BSI1		
80	CLK	C	95	BSI3		
2	VSS					
12	VSS					
23	VSS					
42	VSS					
52	VSS					
63	VSS					
33	VDD					
73	VDD					

F – PHYSICAL PIN DIAGRAM

F 1. Pin Assignment

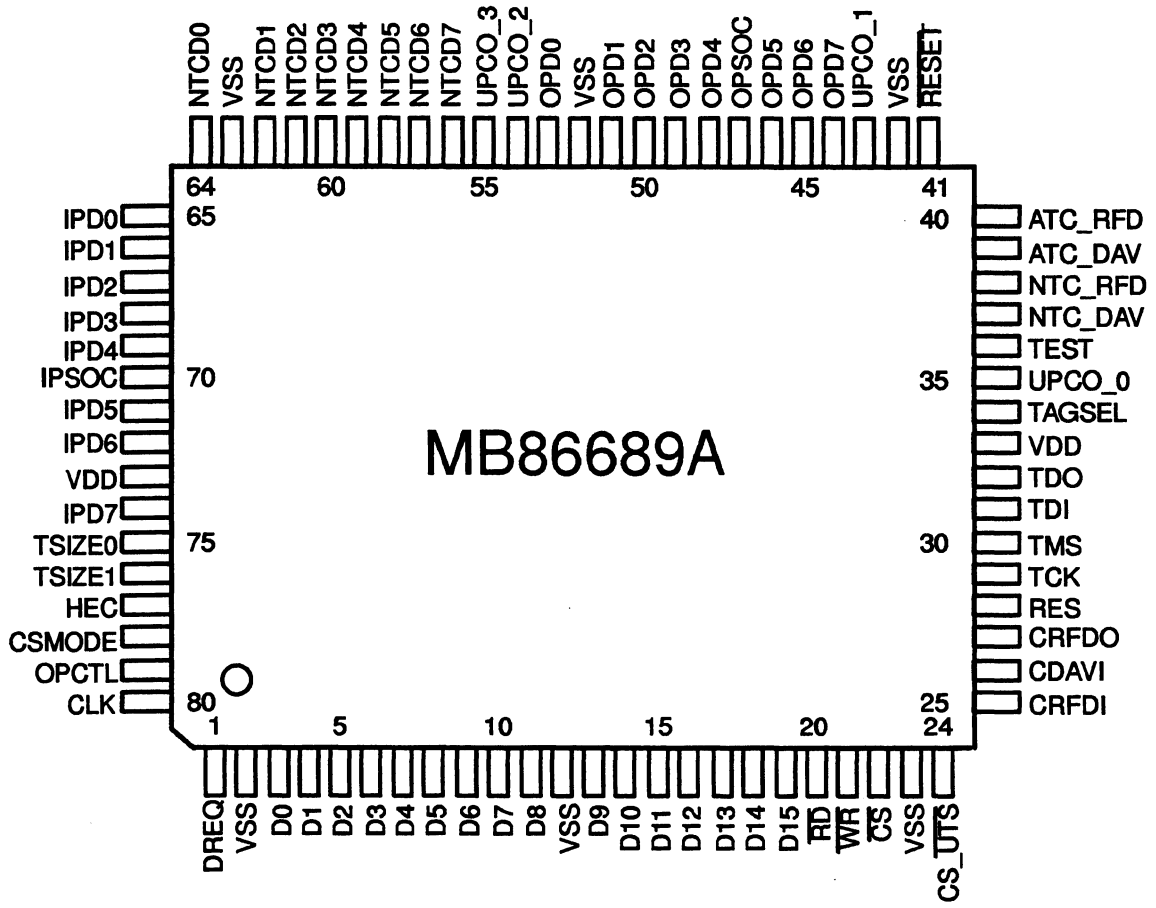


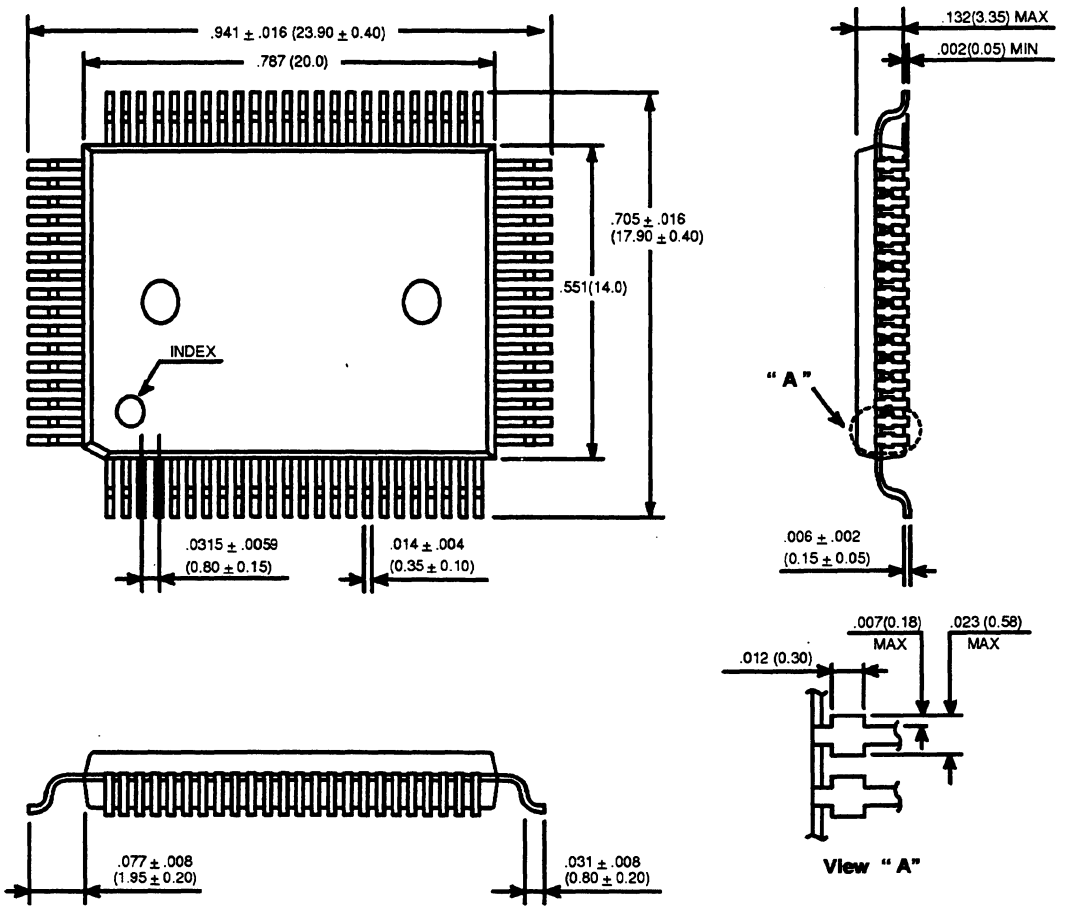
Fig. 31 Pin Assignment

Pin No.	Pin Name	Type	Function
1	DREQ	O	DMA Request signal output
2	VSS	-	
3	D0	I/O	Microprocessor data bus, bit 0
4	D1	I/O	Microprocessor data bus, bit 1
5	D2	I/O	Microprocessor data bus, bit 2
6	D3	I/O	Microprocessor data bus, bit 3
7	D4	I/O	Microprocessor data bus, bit 4
8	D5	I/O	Microprocessor data bus, bit 5
9	D6	I/O	Microprocessor data bus, bit 6
10	D7	I/O	Microprocessor data bus, bit 7
11	D8	I/O	Microprocessor data bus, bit 8
12	VSS	-	
13	D9	I/O	Microprocessor data bus, bit 9
14	D10	I/O	Microprocessor data bus, bit 10
15	D11	I/O	Microprocessor data bus, bit 11
16	D12	I/O	Microprocessor data bus, bit 12
17	D13	I/O	Microprocessor data bus, bit 13
18	D14	I/O	Microprocessor data bus, bit 14
19	D15	I/O	Microprocessor data bus, bit 15
20	$\overline{RD}$	I	Microprocessor Read input
21	$\overline{WR}$	I	Microprocessor Write input
22	$\overline{CS}$	I	Chip Select
23	VSS	-	
24	CS_UTS	I	Cell Stream / Utopia select input
25	CRFD1	I	Cascade RFD in
26	CDAVI	I	Cascade DAV in
27	CRFDO	O	Cascade RFD out
28	RES	I	Reserved. This pin should be left unconnected.
29	TCK	I	JTAG Test Clock
30	TMS	I	JTAG Test Mode Select
31	TDI	I	JTAG Test Data Input
32	TDO	O	JTAG Test Data Output
33	VDD	-	
34	TAGSEL	I	Tag Select input
35	UPCO_0	O	Usage Parameter Control, bit 0
36	TEST	I	Internal test pin, connect to VSS
37	NTC_DAV	I	Data available input from NTC
38	NTC_RFD	I	Ready for data input from NTC
39	ATC_DAV	O	Data available output to NTC
40	ATC_RFD	O	Ready for data output to NTC

Pin No.	Pin Name	Type	Function
41	RESET	I	Master reset input
42	VSS	–	
43	UPCO_1	O	Usage Parameter Control, bit 1
44	OPD7	O	Cell stream output data, bit 7
45	OPD6	O	Cell stream output data, bit 6
46	OPD5	O	Cell stream output data, bit 5
47	OPSOC	O	Cell stream output data sync
48	OPD4	O	Cell stream output data, bit 4
49	OPD3	O	Cell stream output data, bit 3
50	OPD2	O	Cell stream output data, bit 2
51	OPD1	O	Cell stream output data, bit 1
52	VSS	–	
53	OPD0	O	Cell stream output data, bit 0
54	UPCO_2	O	Usage Parameter Control, bit 2
55	UPCO_3	O	Usage Parameter Control, bit 3
56	NTCD7	I/O	NTC-ATC data bus, bit 7
57	NTCD6	I/O	NTC-ATC data bus, bit 6
58	NTCD5	I/O	NTC-ATC data bus, bit 5
59	NTCD4	I/O	NTC-ATC data bus, bit 4
60	NTCD3	I/O	NTC-ATC data bus, bit 3
61	NTCD2	I/O	NTC-ATC data bus, bit 2
62	NTCD1	I/O	NTC-ATC data bus, bit 1
63	VSS	–	
64	NTCD0	I/O	NTC-ATC data bus, bit 0
65	IPD0	I	Cell stream input data, bit 0
66	IPD1	I	Cell stream input data, bit 1
67	IPD2	I	Cell stream input data, bit 2
68	IPD3	I	Cell stream input data, bit 3
69	IPD4	I	Cell stream input data, bit 4
70	IPSOC	I	Cell stream input data sync
71	IPD5	I	Cell stream input data, bit
72	IPD6	I	Cell stream input data, bit
73	VDD	–	
74	IPD7	I	Cell stream input data, bit
75	TSIZE0	I	Tag size select input 0
76	TSIZE1	I	Tag size select input 1
77	HEC	I	HEC/NO HEC select, [0] = HEC
78	CSMODE	I	Cell stream/NTC mode select, [0] = NTC
79	OPCTL	I	Output control for RXD0 - 7 and DREQ
80	CLK	I	Clock input

G – PACKAGE DIMENSIONS

80-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-80P-M06)



Dimensions in
inches (millimeters)

F80010S-2C-2

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ENHANCEMENT SUMMARY

Address Translation Controller (ATC)

MB86689/MB86689A

Edition 1.0, May 1994

MB86689/MB86689A Enhancement Summary Edition 1.0

ERRATA LIST

1) Section 2.3 Fujitsu Cell Stream / UTOPIA Cell Stream Mode

Should read :-

CS/UTS	Cell Stream / UTOPIA (pin 24) (with internal pull-up)
CS/UTS=1	Fujitsu Cell Stream Mode of Operation.
CS/UTS=0	UTOPIA Cell Stream Mode of Operation.

1. INTRODUCTION

1.1. Document Change History

Edition 1.0, initial release, May 25th 1994.

1.2. Purpose of Document

This document details both the hardware and functional changes between the engineering sample version of the Address Translation Controller, MB86689, and the production version, MB86689A.

1.3. Disclosure

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2. HARDWARE CHANGES

2.1. JTAG Test Port

MB86689B now contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). The addition of JTAG functionality simplifies board level testing and requires the additional pins:

TDO - test data output	(pin 32)
TDI - test data input	(pin 31)
TMS - test mode select	(pin 30)
TCK - test clock input	(pin 29)

The Test Access Port (TAP) pins: TDO; TDI; TMS & TCK controls the test modes by accessing the internal Test Access Port Controller. The JTAG instructions BYPASS, SAMPLE/PRELOAD, EXTEST and INTEST are implemented.

The JTAG circuitry is internally reset at power on, and hence the optional JTAG reset pin (TRST) is not required.

2.2. Tag Length Selection

The addition of the TAGSEL pin enables variable tag length in NTC mode.

TAGSEL - tag selection input (pin 34)
(with internal pull up)

2.3. Fujitsu Cell Stream/Utopia Cell Stream Mode

An additional pin is used to select the clock edge on which the outputs are changed.

CS/UTS - Cell Stream/Utopia (pin 24)
(with internal pull down)

2.4. UPC Interface

The addition of the following UPC pins allow transfer of header information to an external policing device.

UPC00 - Bit1 of match address to UPC (pin 35)
UPC01 - Bit2 of match address to UPC (pin 43)
UPC02 - Bit3 of match address to UPC (pin 54)
UPC03 - Bit4 of match address to UPC (pin 55)

3. FUNCTIONAL CHANGES

3.1. Flexible Tag Select

The TAG length is now set by the TSIZE pins in both Cell Stream/Utopia mode and in NTC mode. The additional pin, TAGSEL, is used to determine the TAG length:

TAGSEL=0	TAG length set by TSIZE0 & TSIZE1 pins
TAGSEL=1	(Unconnected) TAG length set to 3.

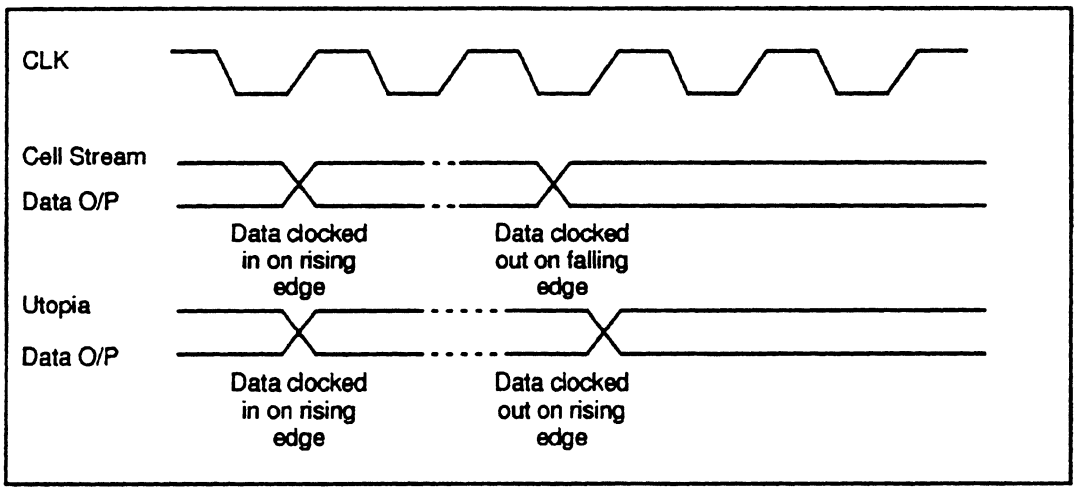
3.2. CS/UTS – Fujitsu Cell Stream or Utopia Cell Stream Mode

Utopia timings have been implemented for interconnection (as an option).

CS/UTS (Pin 24) is used to select the clock edge on which the outputs are changed.

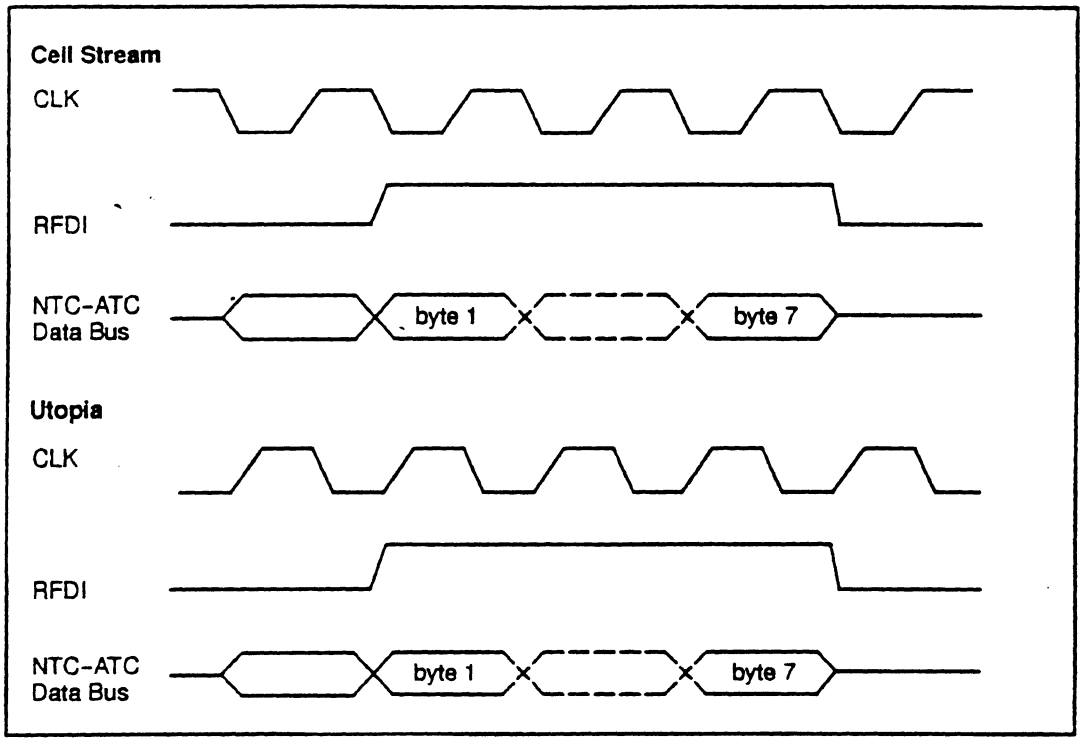
In Utopia Cell Stream mode the data is both clocked out and in on the rising edge whilst in Fujitsu Cell Stream mode data is clocked in on the rising edge but clocked out on the falling edge.

CS Mode of Operation for ATC



NTC Mode is illustrated on the following page.

NTC Mode of Operation for ATC

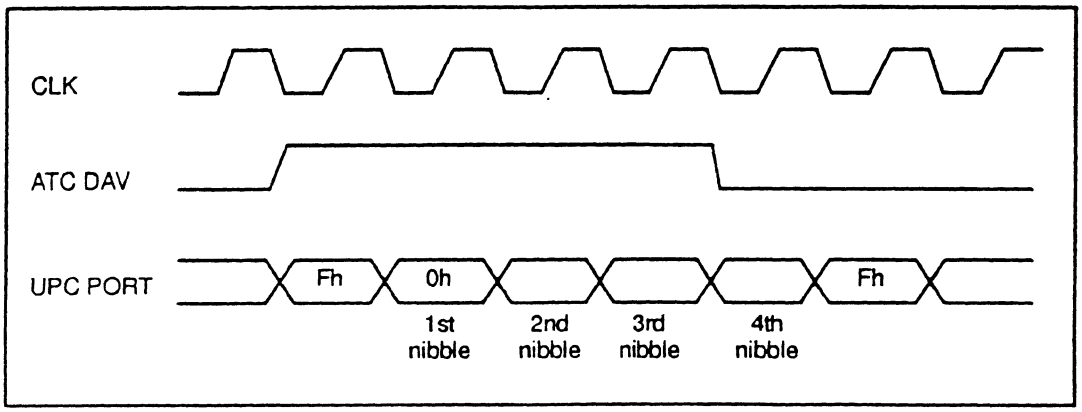


3.3. UPC – Usage Parameter Control

A 4 bit communications port is added to allow transfer of header translation information to an external policing device.

The 4 bit port is normally Hex F. One clock cycle after DAV is asserted a start nibble, Hex 0 is preceded by the ATC code (set up in the Control Register – WORD1) and a 10 bit O/P Ram address as three nibbles.

A 2 bit ATC code is concatenated with the 2 MSBs of the O/P Ram address to form the second nibble. The third nibble consists of the next 4 MSBs of the O/P Ram address and the fourth nibble consists of the remaining 4 bits of the O/P Ram address. The port then returns to Hex F.



1st nibble	-	Indicates Start nibble (Hex 0)
2nd nibble	-	2 bit ATC code + 2 MSBs of O/P Ram address
3rd nibble	-	Next 4 MSBs of O/P Ram address
4th nibble	-	Remaining 4 bits of O/P Ram address

The 2 bit ATC code identifies the ATC when multiple ATCs are cascaded to form a translation table of up to 4096 entries.

3.4. Internal Initialisation

The initialisation sequence is now automatic, previously 7 writes had to be made for each location. All content addressable memory arrays are initialised to '0s' after reset. The completion of this process can be detected by reading the value of DREQ bit in the Status register, or by monitoring the value of the DREQ output pin.

Soft initialisation, as before enables the user to quickly program the RAM with the same 7 words by setting the 'I' bit in the first word.