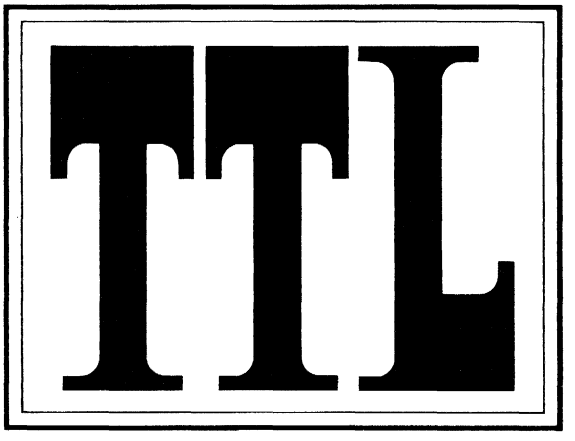
FAIRCHILD SEMICONDUCTOR

LOW POWER SCHOTTKY
AND MACROLOGIC™ TTL

1975

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



FAIRCHILD
SEMICONDUCTOR

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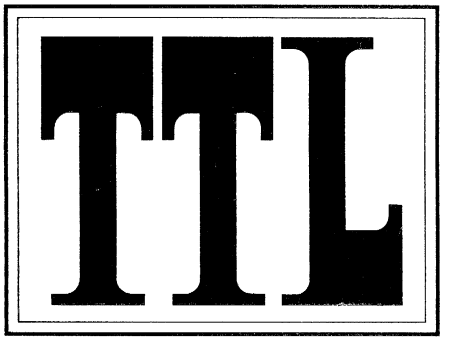


INTRODUCTION

General Description – For many years TTL has been the most popular digital integrated circuit technology, offering a good compromise between cost, speed, power consumption and ease of use. As the price of TTL circuits decreased and the average IC complexity increased to MSI (medium scale integration), the cost and size of the power supply and the difficulty of removing the heat dissipated in the TTL circuits became increasingly important factors. Recent improvements in semiconductor processing have made it possible to not only reduce TTL power consumption significantly, but also to improve the speed over that of standard TTL.

Fairchild's 9LS Low Power Schottky TTL family combines a current and power reduction by a factor 5 (compared to 7400 TTL) with anti-saturation Schottky diode clamping and advanced processing, using shallower diffusions and higher sheet resistivity to achieve circuit performance better than conventional TTL. With a full complement of popular TTL functions available in 9LS and the new, more complex and powerful LSI MACRO-LOGIC™ circuits introduced in 1975, Low Power Schottky is destined to become the dominating TTL logic family.

9LS represents more than just a conventional speed versus power trade-off. This is best illustrated by *Figure 1* which compares 9LS to other TTL technologies. Note that 9LS dissipates eleven times less power than 9S or 74S, suffering a delay increase of only 1.7 times. 9L (Fairchild's Low Power non-Schottky family) by comparison also dissipates eleven times less power than 74H, and 74L dissipates ten times less power than 74N, but both suffer a delay increase of 3.4 times.

The performance of 9LS is not just the result of Schottky clamping. 9LS is four times faster than 9L at the same power dissipation, while 9S and 74S are only two times faster than 74H at the same power. The new and higher level of efficiency exhibited by 9LS is made possible by advanced processing, which provides better switching transistors without any sacrifice in manfacturability.

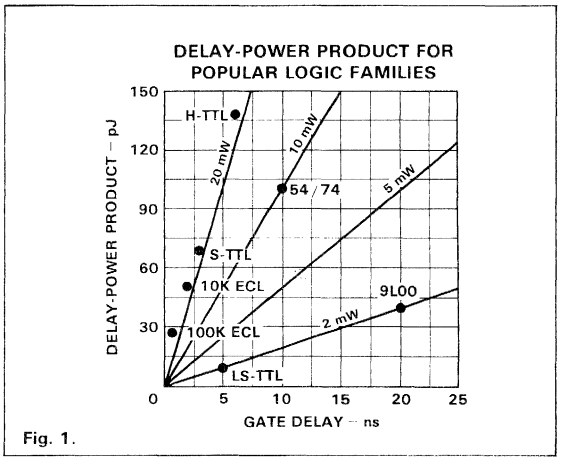


Fig. 1.

To the system designer the advantages of this new TTL family are many:

- Less supply current allows smaller, cheaper power supplies, reducing equipment cost, size and weight.
- Lower power consumption means less heat is generated, which simplifies thermal design. Packing density can be increased or cooling requirements reduced, or perhaps both. The number of cooling fans can be reduced, or slower, quieter ones substituted.
- Reliability is enhanced, since lower dissipation causes less chip temperature rise above ambient; lower junction temperature increases MTBF. Also, lower chip current densities minimizes metal related failure mechanisms.
- Less noise is generated, since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL, which means that fewer or smaller power supply decoupling capacitors are needed. In addition, load currents are only 25% of standard TTL and 20% of HTTL, which means that when a logic transition occurs the current changes along signal lines are proportionately smaller, as are the changes in ground current. Rise and fall times, and thus wiring rules, are the same as for standard TTL and more relaxed than for HTTL or STTL.
- Simplified MOS to TTL interfacing is provided, since the input load current of LSTTL is only 25% of a standard TTL load.
- Ideally suited for CMOS to TTL interfacing. All Fairchild CMOS and most other 4000 or 74C CMOS are designed to drive one 9LS input load at 5.0 V. The 9LS can also interface directly with CMOS operating up to 15 V due to the high voltage Schottky input diodes.
- Best TTL to MOS or CMOS driver. With the modest input current of MOS or CMOS as a load, any 9LS output will rise up to within 1 V of V_{CC}, and can be pulled up to 10 V with an external resistor.
- Interfaces directly with other TTL types, as indicated in the input and output loading tables.
- The functions and pinouts are the same as the familiar 7400/9300 series, which means that no extensive learning period is required to become adept in their use.

Circuit Characteristics

The 9LS circuit features are easiest explained by using the 9LS00 2-input NAND gate as an example. The input/output circuits of all 9LS TTL, including, SSI, MSI and MACROLOGIC are almost identical. While the logic function and the basic structure of 9LS circuits are the same as conventional TTL, there are also significant differences, as explained below:

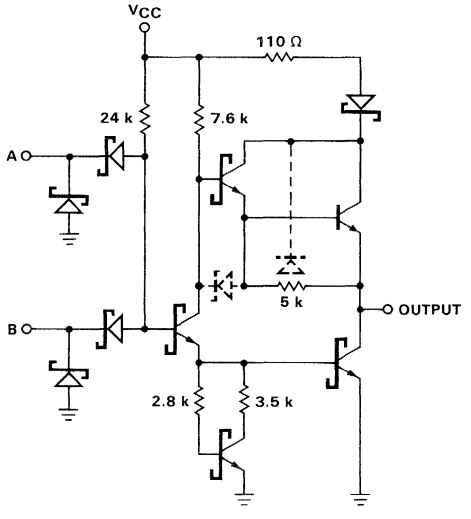


Fig. 2.

Input Configuration

LSTTL is considered part of the TTL family, but it does not use the multi-emitter input structure that originally gave TTL its name. All 9LS TTL, with the exception of some early designs (see Note 1), employ a DTL-type input circuit which uses Schottky diodes to perform the AND function. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage to 15 V. Each input has a Schottky clamping diode which conducts when an input signal goes negative, as indicated by the input characteristic of *Figure 3*. This helps to simplify interfacing with those MOS circuits whose output signal tends to go negative. For a long TTL interconnection, which acts like a transmission line, the clamp diode acts as a termination for a negative-going signal and thus minimizes ringing. Otherwise, ringing could become significant when the finite delay along an interconnection is greater than one-fourth the fall time of the driving signal.

The effective capacitance of an LSTTL input is approximately 3.3 pF. For an input which serves more than one internal function, each additional function adds 1.5 pF.

Note 1. The 9LS03, 05, 22, 74, 109, 112, 113 and 114 use transistor inputs at present, but will be redesigned by the first part of 1976 to incorporate diode inputs.

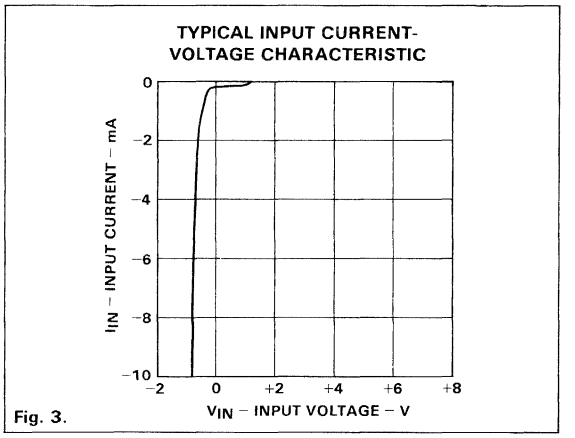


Fig. 3.

Output Configuration

The output circuits of 9LS Low Power Schottky TTL have several features not found in conventional TTL. A few of these features are discussed below.

- The base of the pull-down output transistor is returned to ground through a resistor-transistor network instead of through a simple resistor. This squares up the transfer characteristics since it prevents conduction in the phase-splitter until base current is supplied to the pull-down output transistor. This also improves the propagation delay and transition time. (See *Figure 4*)

- The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5 kΩ resistor to the output terminal. (Unlike 74H and 74S where it is returned to ground, which is a more power consuming configuration). This configuration allows the output to pull-up to one V_{BE} below V_{CC} for low values of output current.

- As a unique feature, the 9LS outputs use a Schottky diode in series with the Darlington collector resistor. This diode allows the output to be pulled substantially higher than V_{CC} (e.g., to +10 V, convenient for interfacing with CMOS). For the same reason the parasistic diode of the base return resistor is connected to the Darlington common collector, not to V_{CC}. Some early 9LS designs – the 9LS00, 02, 04, 10, 11, 20, 32, 74, 109, 112, 113 and 114 – do not have the diode in series with the Darlington collector resistor. These outputs are, therefore, clamped one diode drop above the positive supply voltage (V_{CC}). These older circuits also contain a "speed-up" diode that supplies additional phase splitter current while the output goes from HIGH to LOW and also limits the maximum output voltage to one diode drop above V_{CC}. Since this is the fastest transition even without additional speed-up, this diode is omitted in all new designs.

Output Characteristics

Figure 5 shows the LOW state output characteristics. For low I_{OL} values, the pull-down transistor is clamped out of deep saturation which contributes to speed. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition. This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting edge rate is approximately 0.5 V/ns with a 15 pF load and 0.25 V/ns with a 50 pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$v(t) = V_{OL} + 3.7\,[1 - \exp(-t/T)]$$

where

$T = 8$ ns for $C_L = 15$ pF

$= 16$ ns for $C_L = 50$ pF

The waveform of a falling output signal resembles that part of a cosine wave between angles of 0° and 180°. Fall times from 90% to 10% are approximately 4.5 ns with a 15 pF load and 8.6 ns with a 50 pF load. Equivalent edge rates are approximately 0.8 V/ns and 0.4 V/ns, respectively. For analytical purposes, the falling waveform can be approximated by the following expression.

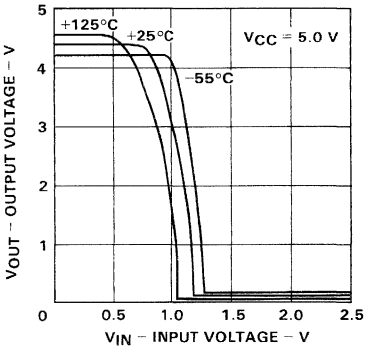


Fig. 4.

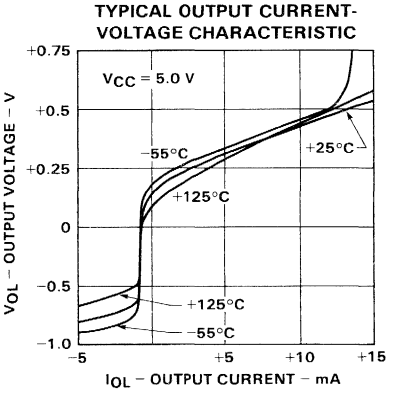


Fig. 5.

$$v(t) = V_{OL} + 1.9\,\mu(t)\,[1 + \cos \omega t] - 1.9\,\mu(t-a)\,[1 + \cos \omega(t-a)]$$

where

$\mu(t) = 0$ for $t < 0$
$= 1$ for $t > 0$

and

$\mu(t-a) = 0$ for $t < a$
$= 1$ for $t > a$

For t in nanoseconds and $C_L = 15$ pF,

$a = 7.5$ ns, $\omega = 0.42$

For $C_L = 50$ pF,

$a = 14$ ns, $\omega = 0.23$

AC Switching Characteristics

The average propagation delay of a Low Power Schottky gate is 5 ns at a load of 15 pF as shown in *Figure 6*. The delay times increase at an average of 0.08 ns/pF for larger values of capacitance load. These delay times are relatively insensitive to variations in power supply and temperature. The average propagation delay time changes less than 1.0 ns over temperature and less than 0.5 ns with V_{CC} for the military temperature and voltage ranges. (See *Figures 8* and *9*).

The power versus frequency characteristics of the 9LS family, as shown in *Figure 7*, indicate that at operating frequencies above 1 MHz the Low Power Schottky devices are more efficient than CMOS for most applications.

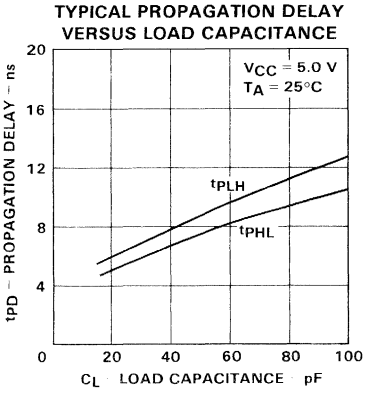


Fig. 6.

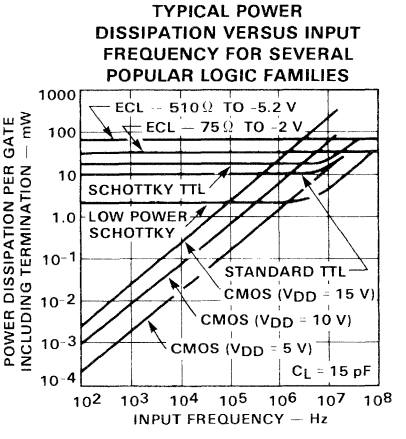


Fig. 7.

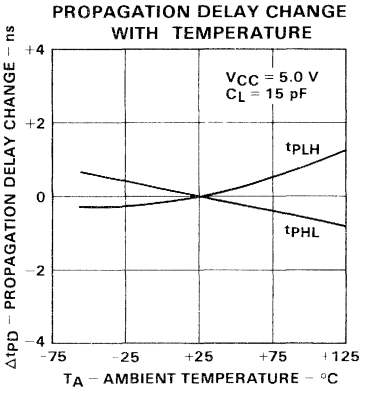


Fig. 8.

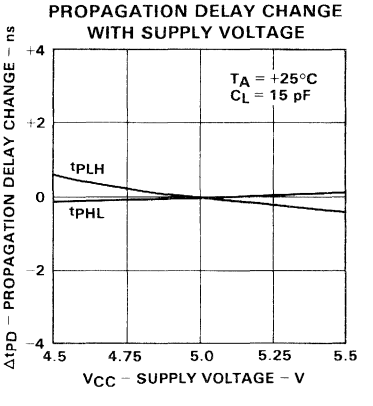


Fig. 9.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} **Input LOW current** – The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} **Output HIGH current** – The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** – The current flowing into an output which is in the LOW state.

I_{OS} **Output short circuit current** – The current flowing out of an output which is in the HIGH state when that output is short circuited to ground (or other specified potential).

I_{OZH} **Output off current HIGH** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, −10 V is greater than −1.0 V).

V_{CC} **Supply voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(MAX)}$ **Input clamp diode voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** – The range of input voltages that represents a logic HIGH in the system.

$V_{IH(MIN)}$ **Minimum input HIGH voltage** – The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** – The range of input voltages that represents a logic LOW in the system.

$V_{IL(MAX)}$ **Maximum input LOW voltage** – The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ **Output HIGH voltage** – The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ **Output LOW voltage** – The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET (Cont'd)

V_{T+} **Positive-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

V_{T-} **Negative-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS

f_{MAX} **Toggle frequency/operating frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse width** – The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.

t_h **Hold time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} **Output disable time (of a 3-state output) from HIGH level** – The time between the 1.3 V level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.

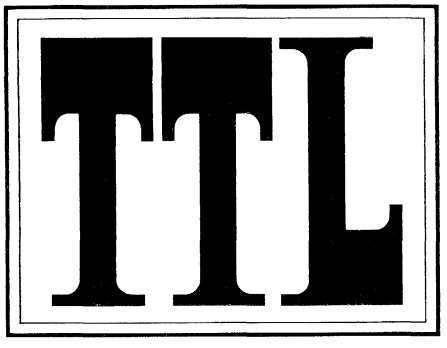
t_{PLZ} **Output disable time (of a 3-state output) from LOW level** – The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.

t_{PZH} **Output enable time (of a 3-state output) to a HIGH level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.

t_{PZL} **Output enable time (of a 3-state output) to a LOW level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.

t_{rec} **Recovery time** – The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



DESIGN CONSIDERATIONS

Supply Voltage and Temperature Range

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 75°C. MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

TTL families may be mixed for optimum system design. The following tables specify the worst case noise immunity in mixed systems.

Worst Case TTL DC Noise Immunity / Noise Margins

Electrical Characteristics

Item	Symbol	Fairchild TTL Families	Military (−55 to +125°C)				Commercial (0 to 75°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL 9000, 9N (54/74)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL 9H (54H/74H)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
8	LPTTL	Low Power TTL, 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
9	STTL	Schottky TTL 9S (54S/74S), 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
10	LSTTL	Low Power Schottky TTL 9LS (54LS/74LS)	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate output levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	300	400	300	mV
HTTL	400	400	300	400	300	mV
LPTTL	500	500	400	500	400	mV
STTL	300	300	200	300	200	mV
LSTTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	500	500	500	500	500	mV
LSTTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	500	500	500	500	500	mV
STTL	300	300	300	300	300	mV
LSTTL	300	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	700	700	700	700	700	mV
LSTTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

Fan-in and Fan-out

In order to simplify designing with Fairchild TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA
in the HIGH state (logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES – INPUT LOAD

1. A 9N00/7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)
2. The 9LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\text{ mA}}{1.6\text{ mA}} \text{ or } 0.5\text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 1\text{ U.L.}$$

3. The 9LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.36\text{ mA}}{1.6\text{ mA}} \text{ or } 0.225\text{ U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 0.5\text{ U.L.}$$

EXAMPLES – OUTPUT DRIVE

1. The output of the 9N00/7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\text{ mA}}{1.6\text{ mA}} = 10\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 20\text{ U.L.}$$

2. The output of the 9LS00XC (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\text{ mA}}{1.6\text{ mA}} \text{ or } 5\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 10\text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in *Table I*.

TABLE I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
9LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
9N00/7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9H00/74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
9S00/74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

Wired-OR Applications

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6\ mA}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(HIGH) \bullet 40\ \mu A}$$

where:

R_X	=	External Pull-up Resistor
N_1	=	Number of Wired-OR Outputs
N_2	=	Number of Input Unit Loads being Driven
$I_{OH} = I_{CEX}$	=	Output HIGH Leakage Current
I_{OL}	=	LOW Level Fan-out Current of Driving Element
V_{OL}	=	Output LOW Voltage Level (0.5 V)
V_{OH}	=	Output HIGH Voltage Level (2.4 V)
V_{CC}	=	Power Supply Voltage

Example: Four 9LS03 gate outputs driving four other 9LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5\ V}{8\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4\ V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1	=	4
$N_2(HIGH)$	=	4 • 0.5 U.L. = 2 U.L.
$N_2(LOW)$	=	4 • 0.25 U.L. = 1 U.L.
I_{OH}	=	100 μA
I_{OL}	=	8 mA
V_{OL}	=	0.5 V
V_{OH}	=	2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

Unused Inputs

For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}. Most 9LS inputs have a breakdown voltage > 15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10 kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

2. Connect the unused input to the output of un unused gate that is forced HIGH.

CAUTION: Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

Interconnection Delays

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, *e.g.,* if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

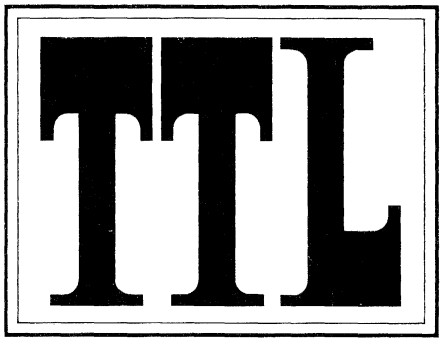
If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-cast situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a circumstance that exists any time a transmission line is terminated by an impedance lower than its characteristic impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



NUMERICAL INDEX OF DEVICES

NUMERICAL INDEX OF DEVICES (Cont'd)

NUMERICAL INDEX OF DEVICES (Cont'd)

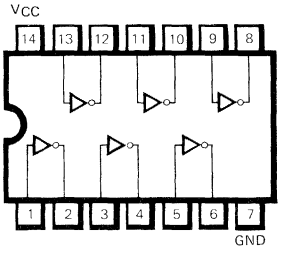
NUMERICAL INDEX OF DEVICES (Cont'd)

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 9N(54/74) 10 ns/10 mW	High Speed 9H(54/74H) 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
NAND Gates						
Hex Inverters	9LS04 (54/74LS04)	9N04 (54/7404)	9H04 (54/74H04)	9S04 (54/74S04) 9S04A	D-1	4-6
Hex Inverts (O.C.)	9LS05 (54/74LS05)	9N05 (54/7405)	9H05 (54/74H05)	9S05 (54/74S05) 9S05A	D-1	4-7
Hex Schmitt Trigger	9LS14 (54/74LS14)	9N14 (54/7414)			D-1	4-12
Quad 2-Input	9LS00 (54/74LS00)	9N00 (54/7400)	9H00 (54/74H00)	9S00 (54/74S00)	D-2	4-3
Quad 2-Input (O.C.)	9LS03 (54/74LS03)	9N03 (54/7403)	9H01 (54/74H01)	9S03 (54/74S03)	D-2	4-5
Quad 2-Input (48 mA)	9LS37 (54/74LS37)	9N37 (54/7437)			D-2	4-21
Quad 2-Input (O.C. 48 mA)	9LS38 (54/74LS138)	9N38 (54/7438)			D-2	4-22
Quad 2-Input Schmitt	9LS132 (54/74LS132)	9N132 (54/74132)		9S132 (54/74S132)	D-2	4-42
Triple 3-Input	9LS10 (54/74LS10)	9N10 (54/7410)	9H10 (54/74H10)	9S10 (54/74S10)	D-3	4-10
Dual 4-Input	9LS20 (54/74LS20)	9N20 (54/7420)	9H20 (54/74H20)	9S20 (54/74S20)	D-4	4-15
Dual 4-Input (O.C.)	9LS22 (54/74LS22)	9N22 (54/7422)	9H22 (54/74H22)	9S22 (54/74S22)	D-4	4-17
Dual 4-Input Buffer	9LS40 (54/74LS40)	9N40 (54/7440)	9H40 (54/74H40)	9S40 (54/74S40)	D-4	4-23
8-Input	9LS30 (54/74LS30)	9N30 (54/7430)	9H30 (54/74H30)	9S30 (54/74S30)	D-5	4-19
NOR Gates						
Quad 2-Input	9LS02 (54/74LS02)	9N02 (54/7402)		9S02 (54/74S02)	D-6	4-4

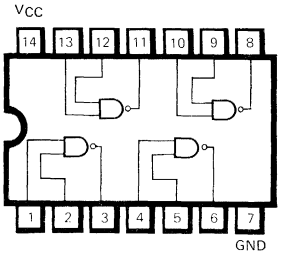
SSI LOGIC SYMBOLS

D1



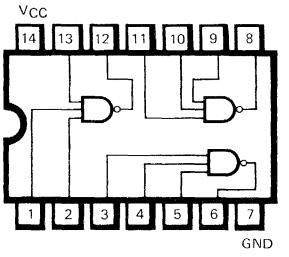
9LS04, 9LS05, 9LS14

D2



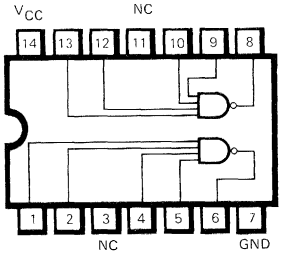
9LS00, 9LS03, 9LS37
9LS38, 9LS132

D3



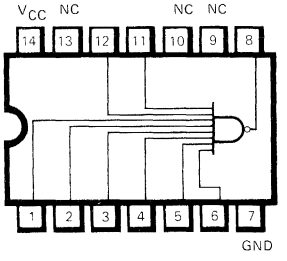
9LS10

D4



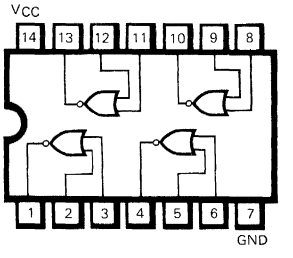
9LS20, 9LS22,
9LS40

D5



9LS30

D6



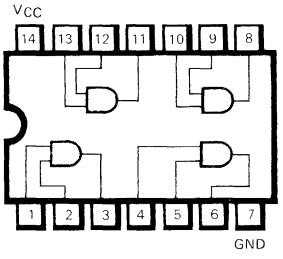
9LS02

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 9N(54/74) 10 ns/10 mW	High Speed 9H(54/74H) 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
AND Gates						
Quad 2-Input	9LS08 (54/74LS08)	9N08 (54/7408)	9H08 (54/74H08)	9S08 (54/74S08)	D-7	4-8
Quad 2-Input (O.C.)	9LS09 (54/74LS09)	9N09 (54/7409)	9H09 (54/74H09)	9S09 (54/74S09)	D-7	4-9
Triple 3-Input	9LS11 (54/74LS11)	9N11 (54/7411)	9H11 (54/74H11)	9S11 (54/74S11)	D-8	4-11
Triple 3-Input (O.C.)	9LS15 (54/74LS15)		9H15 (54/74H15)	9S15 (54/74S15)	D-8	4-14
Dual 4-Input	9LS21 (54/74LS21)	9N21 (54/7421)	9H21 (54/74H21)		D-9	4-16
OR Gates						
Quad 2-Input	9LS32 (54/74LS32)	9N32 (54/7432)		9S32 (54/74S32)	D-10	4-20
Exclusive OR Gate						
Quad 2-Input	9LS86 (54/74LS86)	9N86 (54/7486)		9S86 (54/74S86)	D-11	4-31
Quad 2-Input (O.C)	9LS136 (54/74LS136)				D-11	4-45
Exclusive NOR Gate						
Quad 2-Input (O.C.)	9LS266 (54/74LS266)	9386 (8242)			D-12	4-46
AND-OR-INVERT Gates						
Dual 2-2 Input	9LS51 (54/74LS51)	9N51 (54/7451)	9H51 (54/74H51)	9S51 (54/74S51)	D-13	4-24
2-2-3-3 Input	9LS54 (54/74LS54)				D-14	4-25
4-4 Input	9LS55 (54/74LS55)				D-15	4-26

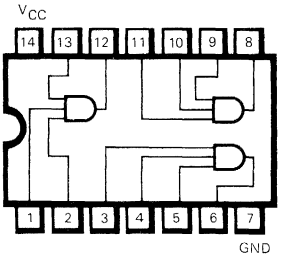
SSI LOGIC SYMBOLS

D7



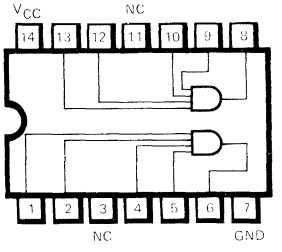
9LS08, 9LS09

D8



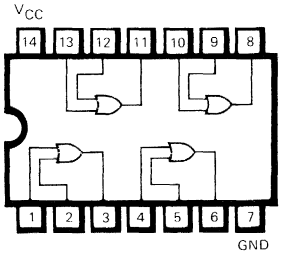
9LS11, 9LS15

D9



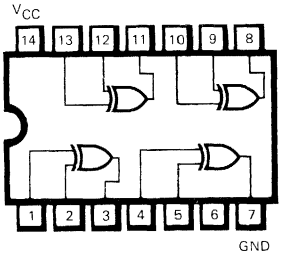
9LS21

D10



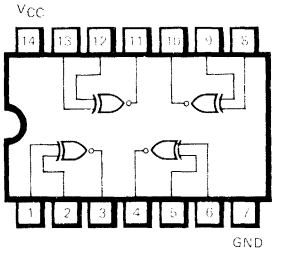
9LS32

D11



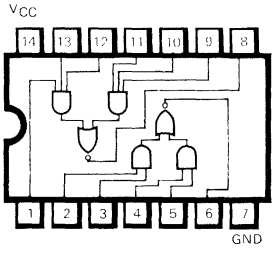
9LS86, 9LS136

D12



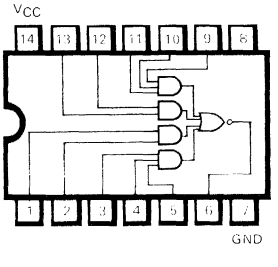
9LS266

D13



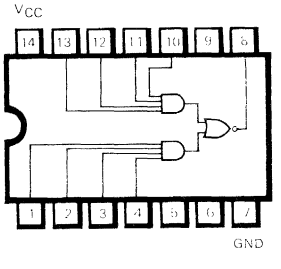
9LS51

D14



9LS54

D15



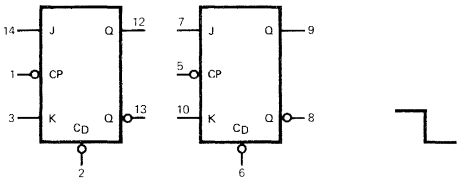
9LS55

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 9N(54/74) 10 ns/10 mW	High Speed 9H(54/74H) 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
Dual Flip-Flops						
Dual JK	9LS73 (54/74LS73)	9N73 (54/7473)	9H73, 103 (55/74H73, 54/74H103)		D-16	4-27
Dual D	9LS74 (54/74LS74)	9N74 (54/7474)	9H74 (54/74H74)	9S74 (54/74S74)	D-17	4-29
Dual $J\overline{K}$	9LS109 (54/74LS109)	9024 (54/74109)		9S109 (54/74S109)	D-18	4-32
Dual JK	9LS112 (54/74LS112)			9S112 (54/74S112)	D-19	4-34
Dual JK	9LS113 (54/74LS113)			9S113 (54/74S113)	D-20	4-36
Dual JK	9LS114 (54/74LS114)			9S114 (54/74S114)	D-21	4-38

SSI FLIP-FLOP LOGIC DIAGRAM

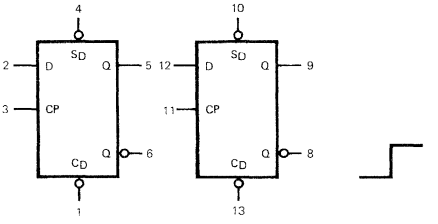
D16



V_{CC} = Pin 4
GND = Pin 11

9LS73

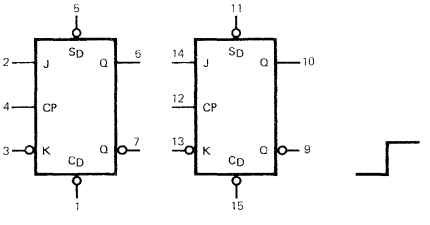
D17



V_{CC} = Pin 14
GND = Pin 7

9LS74

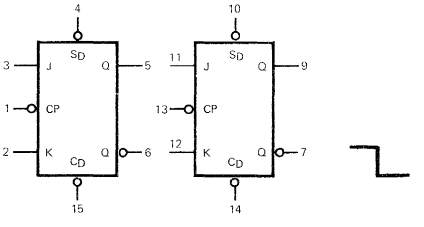
D18



V_{CC} = Pin 16
GND = Pin 8

9LS109

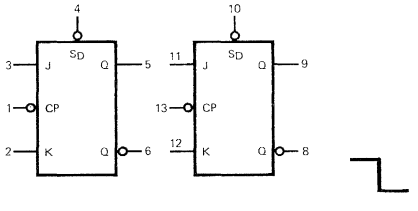
D19



V_{CC} = Pin 16
GND = Pin 8

9LS112

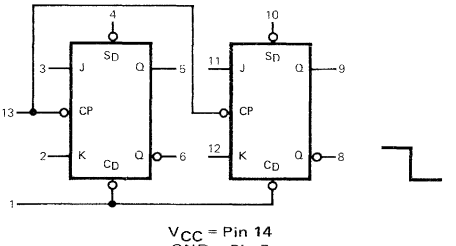
D20



V_{CC} = Pin 14
GND = Pin 7

9LS113

D21



V_{CC} = Pin 14
GND = Pin 7

9LS114

MSI SELECTOR GUIDE BY FUNCTION

Arithmetic and Macrologic Operators
(CLA = Carry Lookahead)

Function	DEVICE NO.	Description	No. of Bits	t_{pd} ns	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Adder	9LS83/ 74LS83	Full Binary 4-Bit w/Carry	4	15	95	5-6
Adder	9LS283/ 74LS283	Full Binary 4-Bit w/Carry	4	15	95	5-109
Arithmetic Logic Unit	9LS181/ 74LS181	ALU with External CLA	4	20	105	5-63
Arith. Logic Reg. Stack	9405	4-Bit ALU, 4-Bit Registers, Ext. CLA	4	70	475	6-24
Data Path Switch	9404	Mut. Arith./Logic Oper.	4	30	350	6-20
Cyclic Redundancy Chk.	9401	CRC Generator Checker	16	30	350	6-3
LIFO P-Stack	9406	Last-In First-Out Memory	64	70	420	6-31
R-Stack	9410	16x4 Random Access Memory w/Output Register	64	50	400	6-48
FIFO	9403	First-In First-Out Memory	64	75	475	6-7

MSI SELECTOR GUIDE BY FUNCTION

Counters

A = Asynchronous S = Synchronous

Function	DEVICE NO.	Modulo	Parallel Load	Clock Transition	Max Clock Rate MHz (typ)	Clock to Q Output Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Asynchronous	9LS90/74LS90	2x5		⌐	50	33	45	5-9
Asynchronous	9LS92/74LS92	2x6		⌐	50	33	45	5-9
Asynchronous	9LS93/74LS93	2x8		⌐	50	46	45	5-9
Asynchronous	9LS196/74LS196	2x5	A	⌐	60	48	60	5-89
Asynchronous	9LS197/74LS197	2x8	A	⌐	70	60	60	5-89
Synchronous	9LS160/74LS160	10 Presettable	S	⌐	45	15	95	5-44
Synchronous	9LS161/74LS161	16 Presettable	S	⌐	45	15	95	5-44
Synchronous	9LS162/74LS162	10 Presettable	S	⌐	45	15	95	5-44
Synchronous	9LS163/74LS163	16 Presettable	S	⌐	45	15	95	5-44
Up/Down	9LS192/74LS192	10	A	⌐	40	30	85	5-75
Up/Down	9LS193/74LS193	16	A	⌐	40	30	85	5-75
Up/Down	9LS190/74LS190	10	A	⌐	40	20	90	5-68
Up/Down	9LS191/74LS191	16	A	⌐	40	20	90	5-68

MSI SELECTOR GUIDE BY FUNCTION

Decoders/Demultiplexers

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	DEVICE NO.	Address Inputs	Active LOW Enable	Active LOW Outputs	Open Collector Output Voltage	Address Delay ns (typ)	Enable Delay ns (typ)	Power Dissipation mW (typ)	Fan-out (UL)	LSTTL Data Sheet Page No.
Dual 1-of-4	9LS139/ 74LS139	2+2	1+1	4+4		22	19	34	5	5-22
Dual 1-of-4	9LS155/ 74LS155	2	2+2	4+4		18	15	30	5	5-34
Dual 1-of-4	9LS156/ 74LS156	2	2+2	4+4	5.5 V	33	26	31	5	5-34
1-Of-8	9LS259/ 74LS259	3	1	8		30	19	60	5	5-108
1-of-8	9LS42/ 74LS42	3	1	8		17	17	35	5	5-3
1-of-8	9LS138/ 74LS138	3	3	8		22	21	34	5	5-19
1-of-10	9LS42/ 74LS42	4 (BCD)		10		17		35	5	5-3

MSI SELECTOR GUIDE BY FUNCTION

Latches/Flip-Flops

Function	DEVICE NO.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/Clock Pulse Width ns (typ)	Enable/Clock to Q Delay ns (typ)	Data to Q Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
4-Bit R-S Latch	9LS279/ 74LS279	4x(RS)	-	-	-	-	14	19	4-47
4-Bit D Latch	9LS196/ 74LS197	4xD	L	1(L)	20	28	24	60	5-89
4-Bit D Latch	9LS197/ 74LS197	4xD	L	1(L)	20	28	24	60	5-89
4-Bit D Flip-Flop	9LS175/ 74LS175	4xD	L	1(⎍)	20	21	-	55	5-60
4-Bit D Flip-Flop	9LS298/ 74LS298	4x2	-	1(⎏)	20	20	-	65	5-121
6-Bit D Flip-Flop	9LS174/ 74LS174	6	L	1(⎍)	20	21	-	80	5-57
8-Bit Add. Latch	9LS259/ 74LS259	1xD	L	1(L) 3 add. bits	11	18	28	70	5-108
4x4 Register File	9LS170/ 74LS170	4xD	-	2	25	-	26	125	5-53
4x4 Register File (3-state)	9LS670/ 74LS670	4xD	-	2	25	-	24	150	5-124

Monostables (One-Shots)

Function	DEVICE NO.	Pulse Width Variation (%)		No. of Inputs		Resettable	Min Output (t_W) ns	Power Dissipation mW (typ)	LSTTL DAta Sheet Page No.
		vs. V_{CC}	vs. Temp	Positive	Negative				
Dual Retriggerable	96L02	±0.4%	±1.5%	1	1	X	110	50	5-129
Dual Retriggerable	96S02	±0.2%	±0.2%	1	1	X	27	250	5-135

MSI SELECTOR GUIDE BY FUNCTION

Multiplexers

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	DEVICE NO.	Enable Inputs	True Output	Complement Output	Select Delay ns (typ)	Enable Delay ns (typ)	Data Delay ns (typ)	Power Dissipation mW (typ)	Fan-Out (UL)	LSTTL Data Sheet Page No.
Quad 2-Input	9LS157/ 74LS157	1	X		18	14	9	49	5	5-38
Quad 2-Input	9LS158/ 74LS158	1		X	16	12	7	24	5	5-41
Quad 2-Input	9LS257/ 74LS257	1	3-State		14	16	12	50	5	5-102
Quad 2-Input	9LS258/ 74LS258	1		3-State	12	16	10	35	5	5-105
Quad 2-Input	9LS298/ 74LS298	Clocked (edge-trigger)	X Latched		-	20	-	65	5	5-121
Dual 4-Input	9LS153/ 74LS153	2	X		18	16	10	31	5	5-31
Dual 4-Input	9LS253/ 74LS253	2	3-State		18	16	10	43	5	5-99
8-Input	9LS151/ 74LS151	1	X	X	28	25	18	30	5	5-25
8-Input	9LS251/ 74LS251	1	3-State	3-State	29	21	18	33	5	5-95
8-Input	9LS152/ 74LS152			X	22	-	11	28	5	5-28

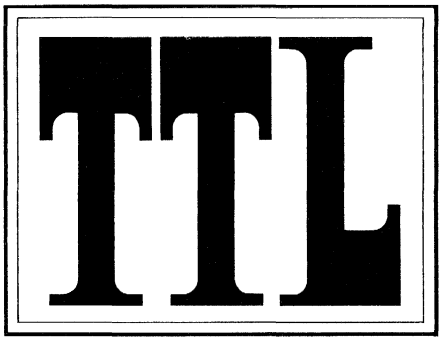
MSI SELECTOR GUIDE BY FUNCTION

Registers

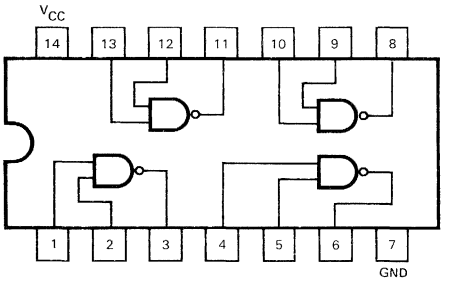
A = Asynchronous S = Synchronous

Function	DEVICE NO.	No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	Max Clock Freq MHz (typ)	Clock to Output Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Parallel-in / Parallel-out Shift Right	9LS95/ 74LS95	4	D	4S	⌝⌞	36	20	65	5-15
Parallel-in / Parallel-out Shift Right	9LS195/ 74LS195	4	J, K	4S	⌟⌜	39	17	70	5-85
Parallel-in / Parallel-out Shift Right	9LS295/ 74LS295	4	D	4S	⌟⌜	28	40	75	5-117
Parallel-in / Parallel-out Bi-Directional	9LS194/ 74LS194	4	DR, DL	4S	⌟⌜	36	16	75	5-81
Serial-in / Parallel-out	9LS164/ 74LS164	8	2D	-	⌟⌜	18	50	95	5-49
Parallel-in / Parallel-out	9LS174/ 74LS174	6	-	6S	⌟⌜	40	21	65	5-57
Parallel-in / Parallel-out	9LS175/ 74LS175	4	-	4S	⌟⌜	40	21	45	5-60
Parallel-in / Parallel-out	9LS298/ 74LS298	4	-	2D MUX	⌝⌞	30	21	65	5-121
Multiport Registers	9LS170/ 74LS170	16	-	4A	⌝⌞	-	25	125	5-53
Multiport Registers	9LS670/ 74LS670	16	-	4A	⌝⌞	-	30	150	5-124

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS00XM/54LS00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS00XC/74LS00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

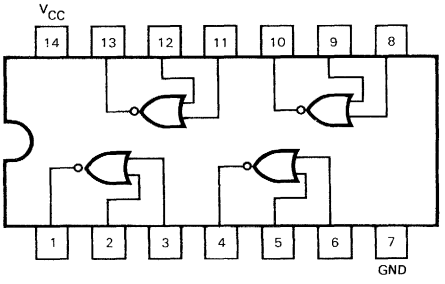
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS02XM/54LS02XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS02XC/74LS02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

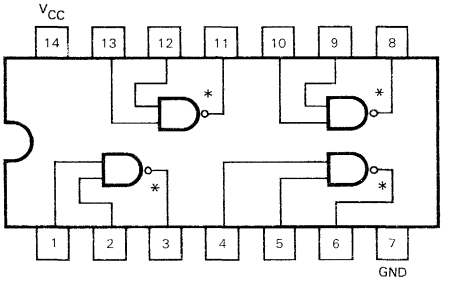
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.6	3.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	5.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS03XM/54LS03XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS03XC/74LS03XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

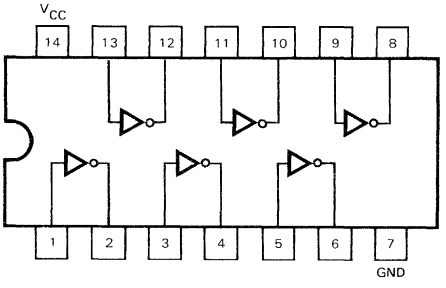
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

HEX INVERTER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS04XM/54LS04XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS04XC/74LS04XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

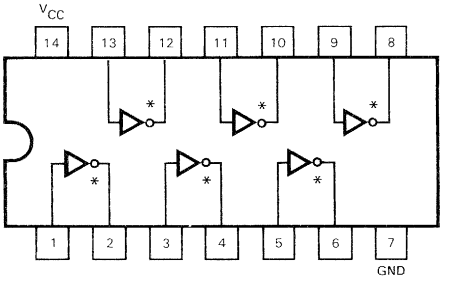
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

HEX INVERTER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS05XM/54LS05XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS05XC/74LS05XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

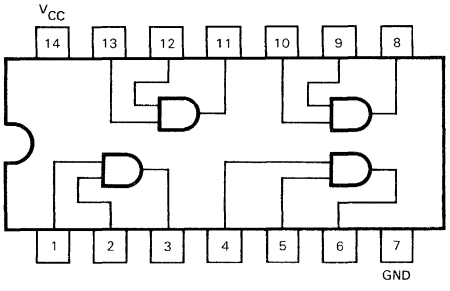
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS08XM/54LS08XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS08XC/74LS08XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

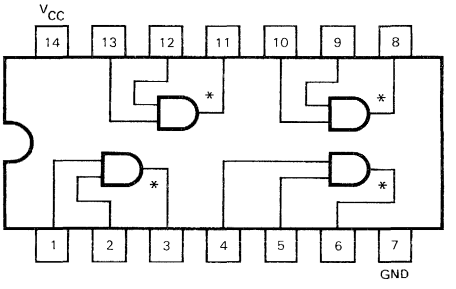
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		7.5	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS09XM/54LS09XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS09XC/74LS09XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

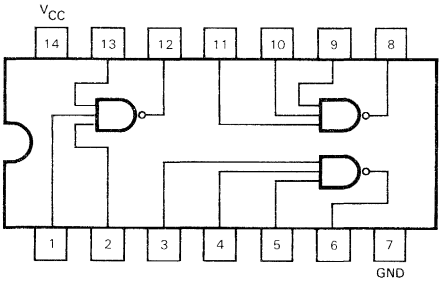
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

TRIPLE 3-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS10XM/54LS10XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS10XC/74LS10XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

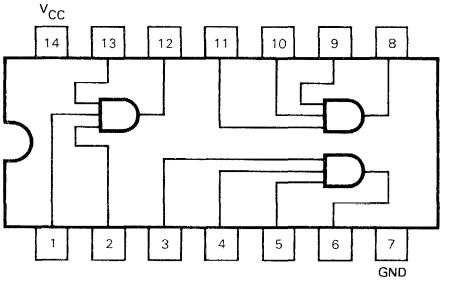
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.6	1.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.8	3.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	6.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	6.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRIPLE 3-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS11XM/54LS11XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS11XC/74LS11XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	4.0	8.5	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.5	11	ns	C_L = 15 pF

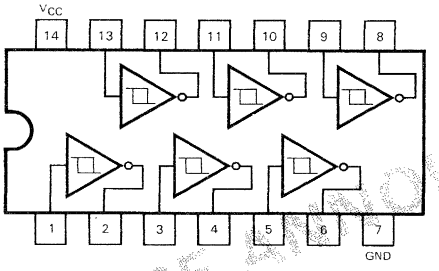
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

HEX SCHMITT TRIGGER INVERTER

DESCRIPTION — The 9LS14 (54LS/74LS14) contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

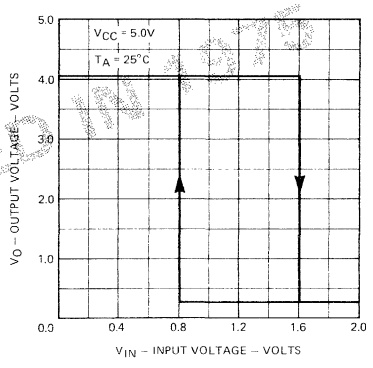


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

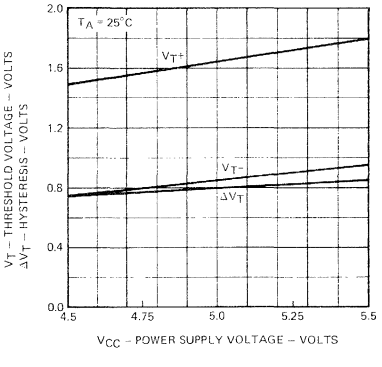


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

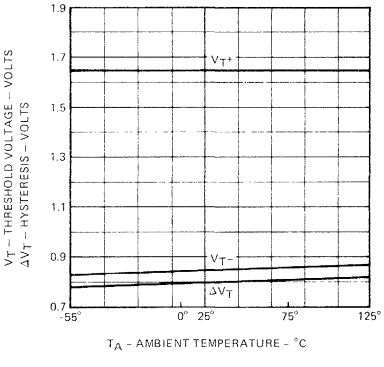


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS14XM/54LS14XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS14XC/74LS14XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

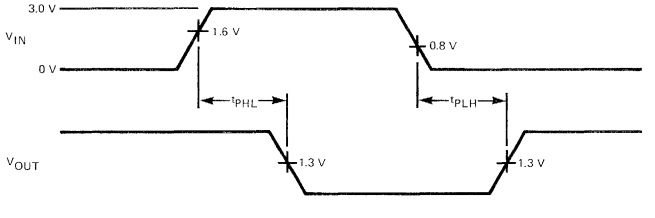
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage			1.6		V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage			0.8		V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			8.6	16	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			12	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V

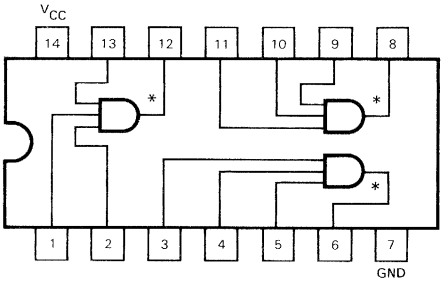
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Propagation Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



TRIPLE 3-INPUT AND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS15XM/54LS15XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS15XC/74LS15XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

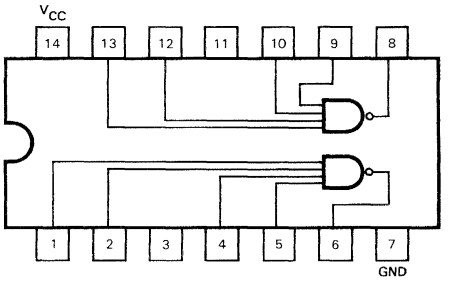
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	7.0	13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	5.0	10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS20XM/54LS20XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS20XC/74LS20XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

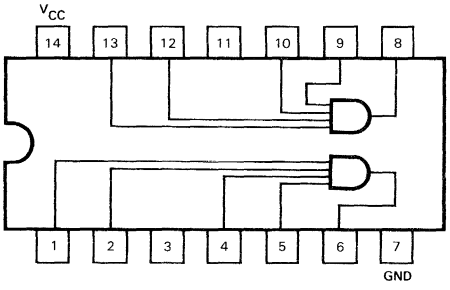
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS21XM/54LS21XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS21XC/74LS21XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

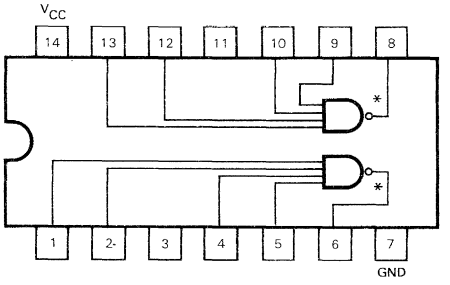
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			2.2	4.4	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS22XM/54LS22XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS22XC/74LS22XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

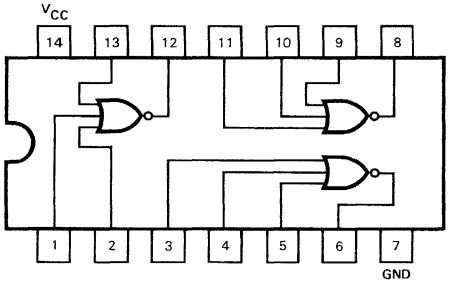
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.

TRIPLE 3-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
9LS27XM/54LS27XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS27XC/74LS27XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

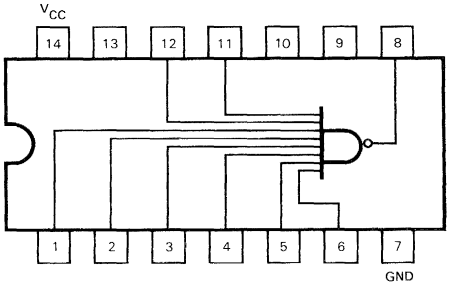
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.0	4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.4	6.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

8-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS30XM/54LS30XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS30XC/74LS30XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

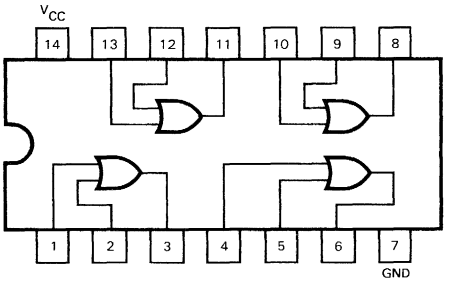
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		7.0	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		9.0	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT OR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS32XM/54LS32XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS32XC/74LS32XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

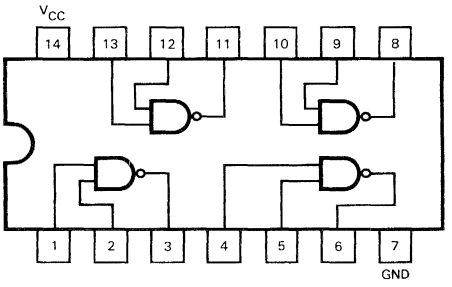
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			3.1	6.2	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.9	9.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS37XM/54LS37XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS37XC/74LS37XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

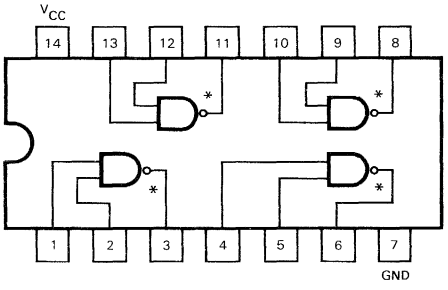
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS38XM/54LS38XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS38XC/74LS38XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

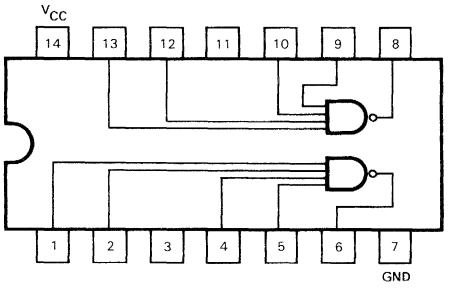
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS40XM/54LS40XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS40XC/74LS40XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

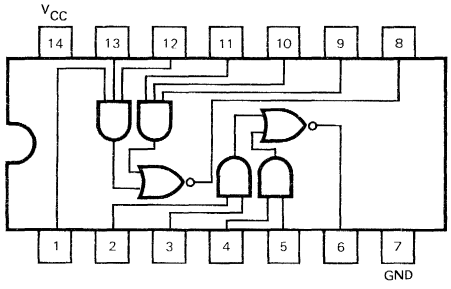
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.45	1.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.0	6.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS51XM/54LS51XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS51XC/74LS51XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

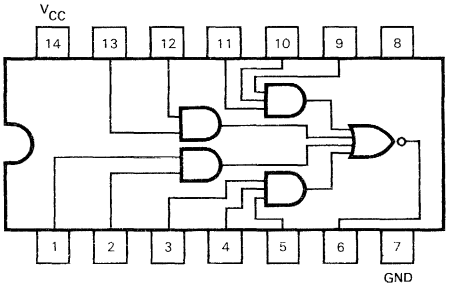
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.4	2.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

3-2-2-3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS54XM/54LS54XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS54XC/74LS54XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

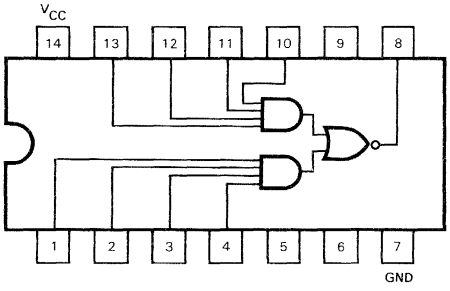
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.0	2.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

2-WIDE 4-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS55XM/54LS55XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS55XC/74LS55XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.7	1.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

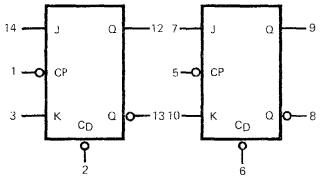
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

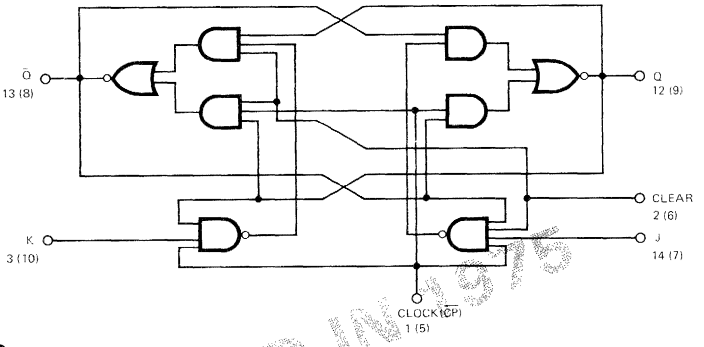
DESCRIPTION — The 9LS73 (54LS/74LS73) offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM
(Each Flip-Flop)



4

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS73XM/54LS73XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS73XC/74LS73XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Clear				60		
	Clock				80		
	J, K				0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
	Clear				0.3		
	Clock				0.4		
I_{IL}	Input LOW Current J, K				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Clear				−0.8		
	Clock				−0.72		
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_W CP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	
$t_W CP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K TO Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

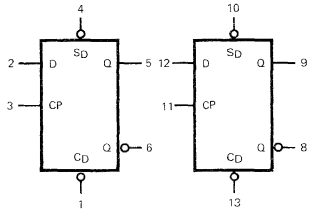
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9LS74 (54LS/74LS74) dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

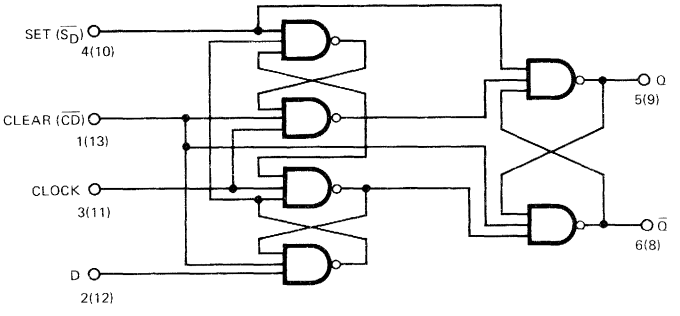
Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS74XM/54LS74XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS74XC/74LS74XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current Data Clock, Set Clear				20 40 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Data Clock, Set Clear				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current Data Clock, Set Clear				−0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

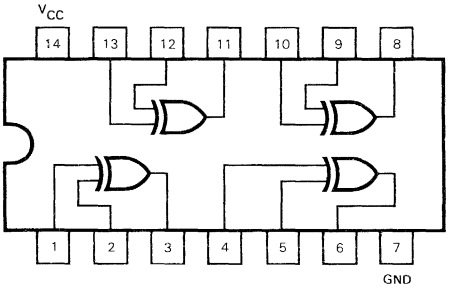
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH}	Propagation Delay,			10	15	ns	Fig. 2	
t_{PHL}	Set or Clear to Output	CP = L		18	24			
t_{PHL}		CP = H		26	35			

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	10	6		ns	Fig. 1	$V_{CC} = 5.0$ V
t_h(H)	Hold Time HIGH, Data to Clock	0	−14		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	14		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−6		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS86XM/54LS86XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS86XC/74LS86XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

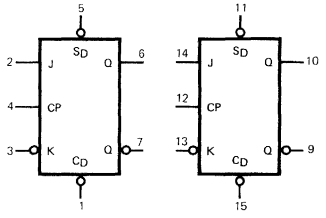
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

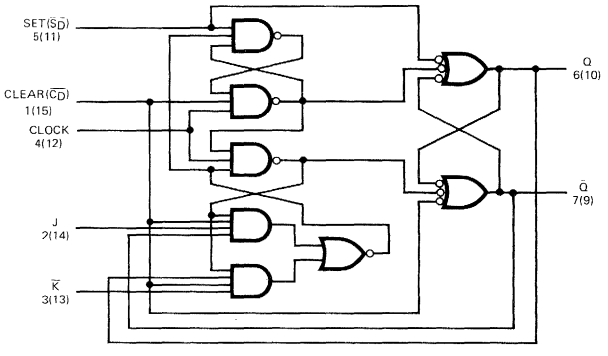
DESCRIPTION — The 9LS109 (54LS/74LS109) consists of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together. The 9LS109 is a pin-for-pin replacement of the 9024 and 9L24.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS109XM/54LS109XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS109XC/74LS109XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Clock, Set Clear				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Clock, Set Clear				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Clock, Set Clear				−0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

4

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	
t_{PLH}	Propagation Delay,			10	15	ns	Fig. 2	
t_{PHL}	Set or Clear to Output	CP = L		18	24			
t_{PHL}		CP = H		26	35			

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

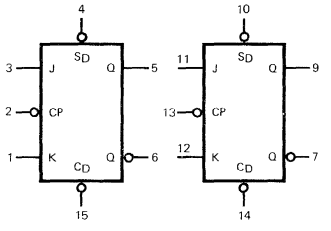
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	18	12		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−13		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	13		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−12		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

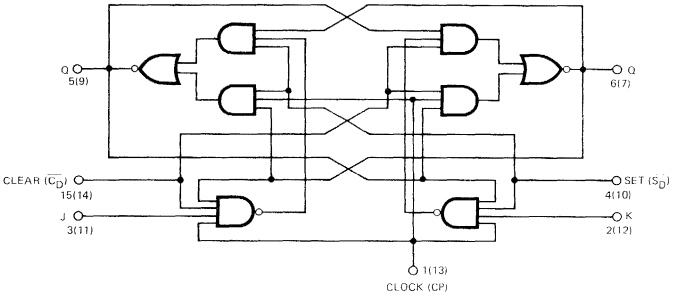
DESCRIPTION — The 9LS112 (54LS/74LS112) dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS112XM/54LS112XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS112XC/74LS112XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Set, Clear Clock				20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set, Clear Clock				−0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

4

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

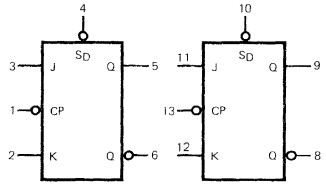
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_W^{CP(H)}$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
$t_W^{CP(L)}$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

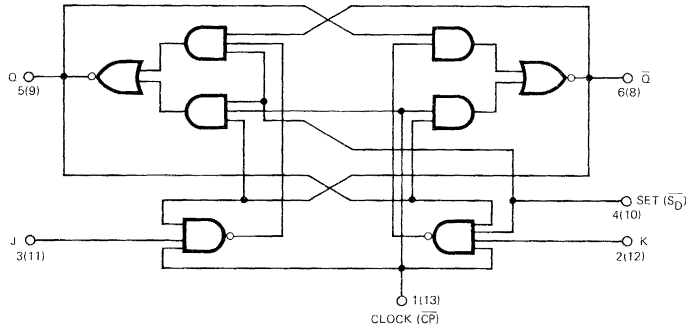
DESCRIPTION — The 9LS113 (54LS/74LS113) offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS113XM/54LS113XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS113XC/74LS113XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clock				20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clock				−0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

4

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

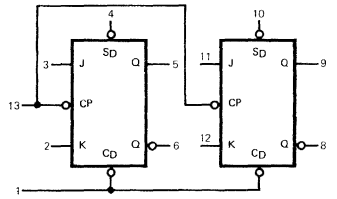
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

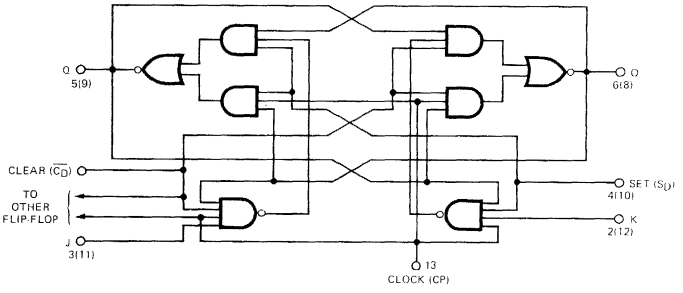
DESCRIPTION — The 9LS114 (54LS114/74LS114) offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS114XM/54LS114XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS114XC/74LS114XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clear Clock				 20 60 120 160	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	 J, K Set Clear Clock				 0.1 0.3 0.6 0.8	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clear Clock				 −0.36 −0.8 −1.6 −1.44	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

4

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

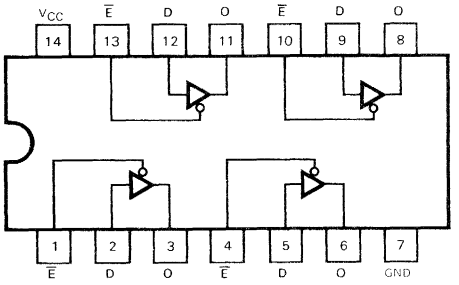
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

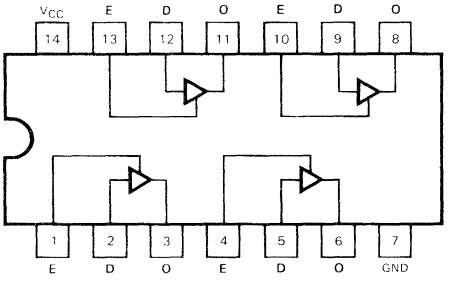
AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES





GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
9LS125XM/54LS125XM 9LS126XM/54LS126XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS125XC/74LS125XC 9LS126XC/74LS126XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW	9LS125			16	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
		9LS126			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V
	Power Supply Current, Outputs Off	9LS125			20	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V
		9LS126			24	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 0 V

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRUTH TABLES

9LS125

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

9LS126

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			10 16	ns	Fig. 2	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	$V_{CC} = 5.0$ V $C_L = 5$ pF $R_L = 667\ \Omega$
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	

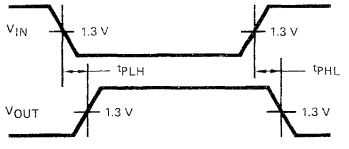


Fig. 1

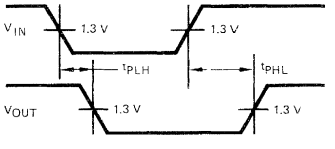


Fig. 2

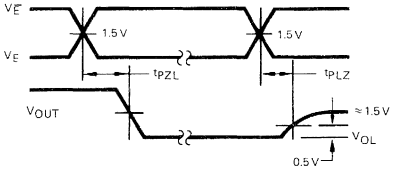


Fig. 3

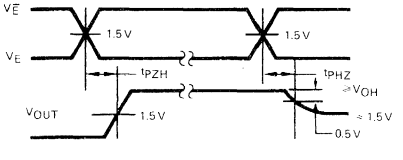
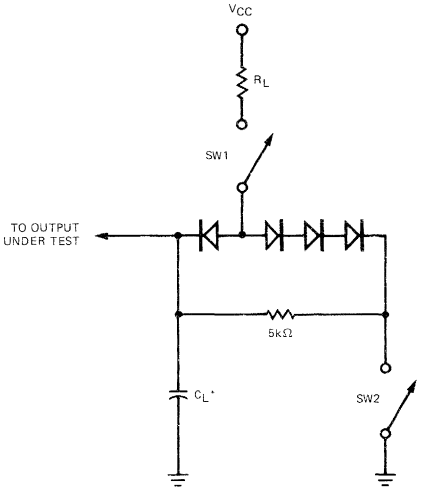


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

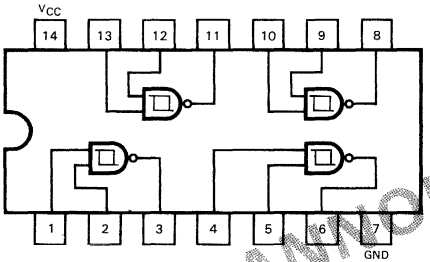
Fig. 5

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

DESCRIPTION – The 9LS132 (54LS/74LS132) contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

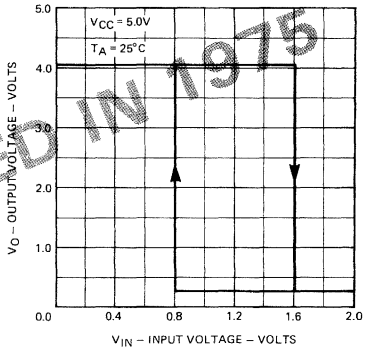


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
POWER SUPPLY VOLTAGE

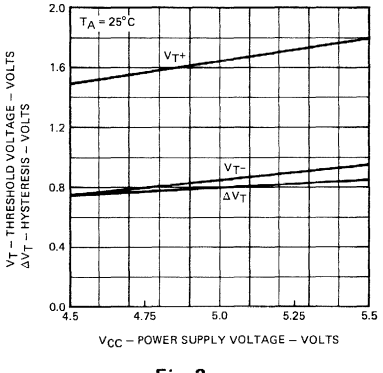


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
TEMPERATURE

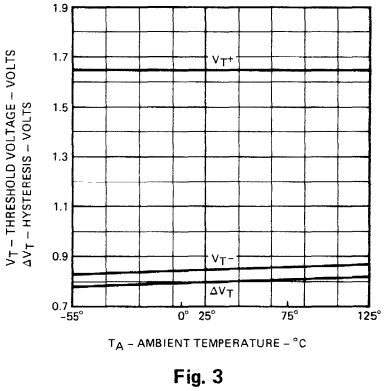


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS132XM/54LS132XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS132XC/74LS132XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

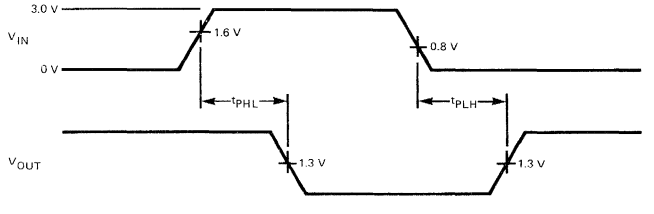
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage			1.6		V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage			0.8		V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			5.9	11	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.2	14	mA	V_{CC} = MAX, V_{IN} = 4.5 V

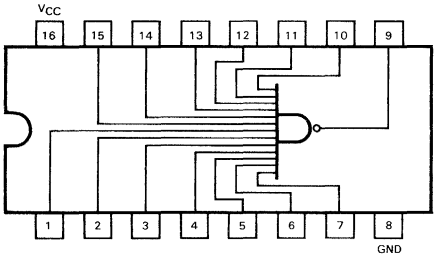
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



13-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
9LS133XM/54LS133XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS133XC/74LS133XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

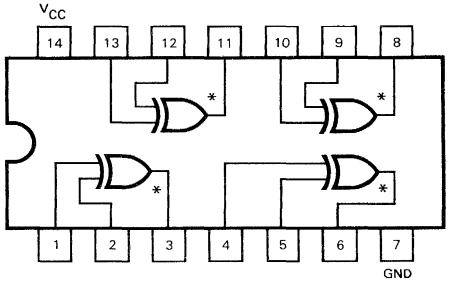
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		17	25	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS136XM/54LS136XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS136XC/74LS136XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

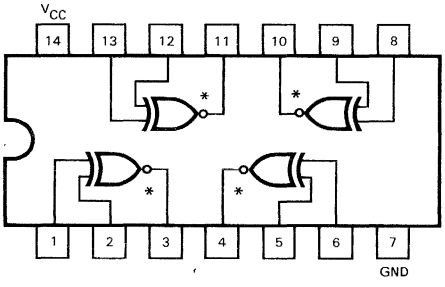
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT EXCLUSIVE NOR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS266XM/54LS266XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS266XC/74LS266XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

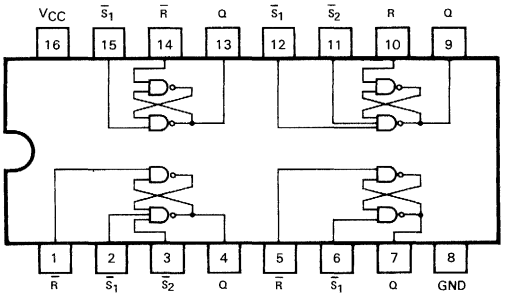
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			8.0	13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD SET-RESET LATCH



TRUTH TABLE

INPUTS			OUTPUT
$\bar{S}_1$	$\bar{S}_2$	$\bar{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
9LS279XM/54LS279XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS279XC/74LS279XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

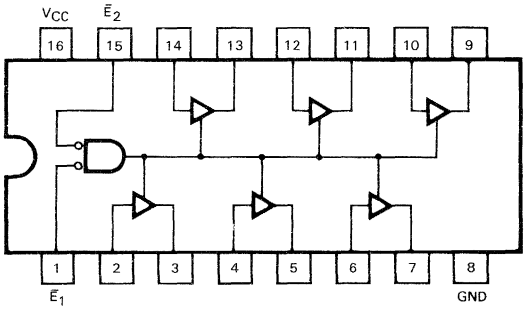
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			3.8	7.0	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, $\bar{S}$ to Output			22	ns	V_{CC} = 5.0 V
t_{PHL}				15		C_L = 15 pF
t_{PHL}	Propagation Delay, $\bar{R}$ to Output			27	ns	

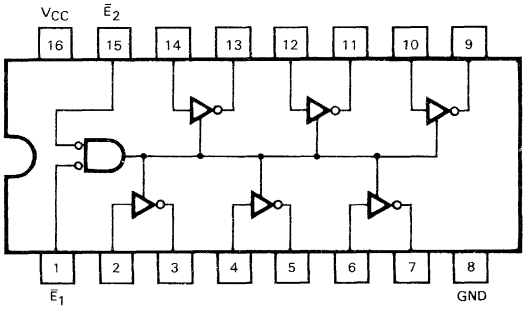
9LS365 (54LS/74LS365)
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

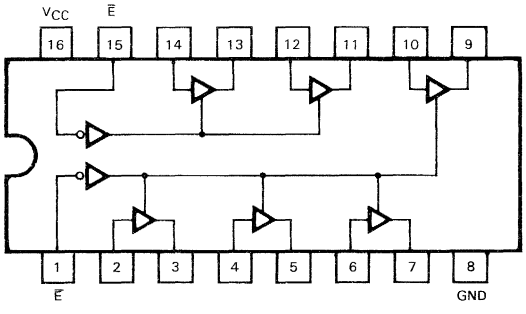
9LS366 (54LS/74LS366)
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

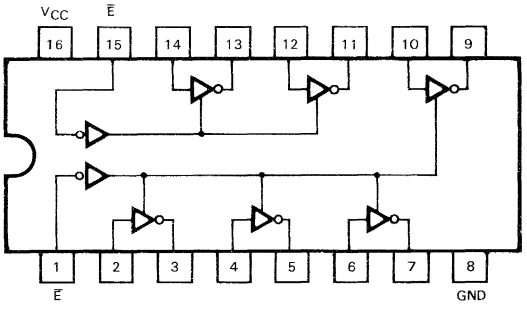
9LS367 (54LS/74LS367)
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

9LS368 (54LS/74LS368)
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

DESCRIPTION — The 9LS365/366/367/368 are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

When the Output Enable Input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
9LS365XM/54LS365XM 9LS366XM/54LS366XM 9LS367XM/54LS367XM 9LS368XM/54LS368XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS365XC/74LS365XC 9LS366XC/74LS366XC 9LS367XC/74LS367XC 9LS368XC/74LS368XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	9LS365/367		13.5	24	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	
		9LS366/368		11.8	21			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

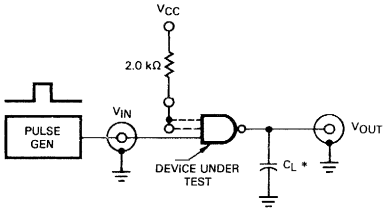
AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 4-41 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (9LS365 • 9LS367)			10 16	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (9LS366 • 9LS368)			10 16	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 667 Ω

AC TEST CIRCUITS AND WAVEFORMS

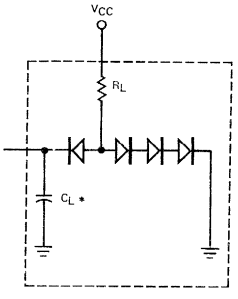
The following test circuits and conditions represent Fairchild's typical AC test procedures. The output loading for standard Low Power Schottky devices is a 15 pF capacitor. Experimental evidence shows that test results using the additional diode-resistor load are within 0.2 ns of the capacitor only load. The capacitor only load also has the advantage of repeatable, easily correlated test results. The input pulse rise and fall times are specified at 6 ns to closely approximate the Low Power Schottky output transitions through the active threshold region. The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

Test Circuit for Standard Output Devices

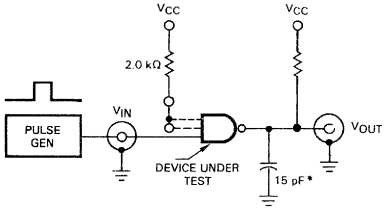


*Includes all probe and jig capacitance

Optional Load (Guaranted – Not Tested)



Test Circuit for Open Collector Output Devices

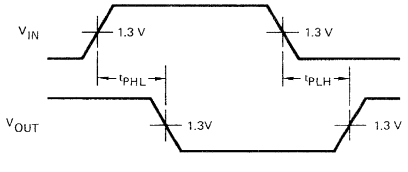


*Includes all probe and jig capacitance

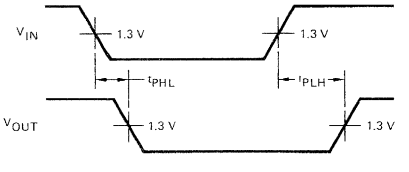
Pulse Generator Settings
(unless otherwise specified)

Frequency = 1 mHz
Duty Cycle = 50%
t_{TLH} (t_r) = 6 ns
t_{THL} (t_f) = 6 ns
Amplitude = 0 to 3 V

Waveform for Inverting Outputs



Waveform for Non-inverting Outputs



WAVEFORMS FOR 9LS73, 9LS74, 9LS109, 9LS112, 9LS113, AND 9LS114

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH

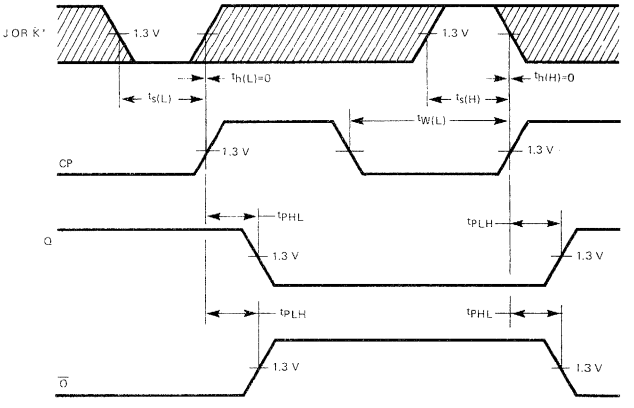


Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS

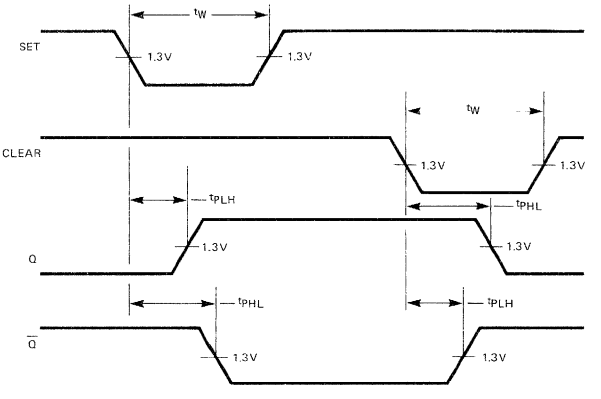
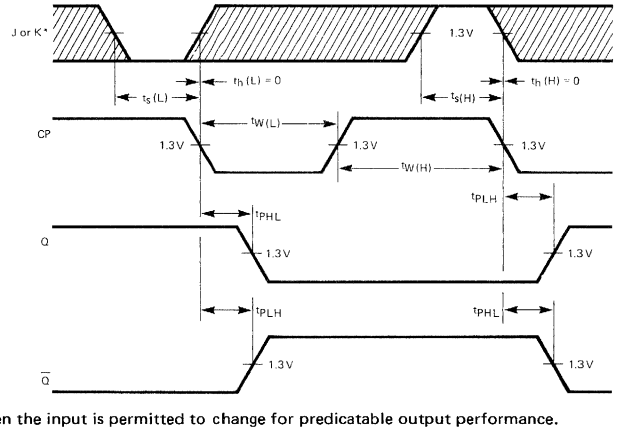
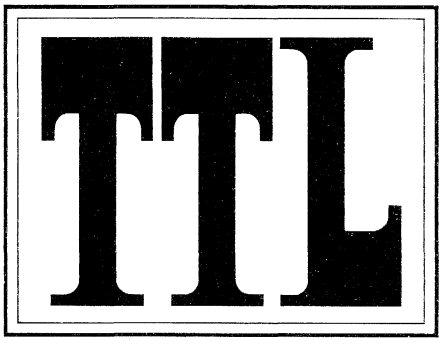


Fig. 3 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



*The shaded areas indicate when the input is permitted to change for predicatable output performance.

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



9LS42 (54LS/74LS42)
ONE-OF-TEN DECODER

DESCRIPTION — The LSTTL/MSI 9LS42 (54LS/74LS42) is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The 9LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

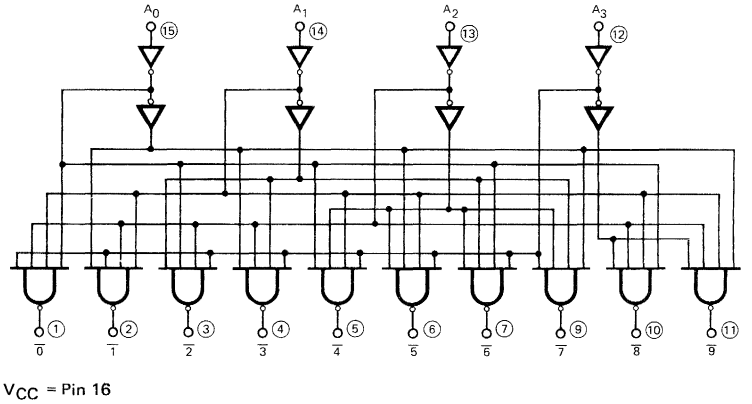
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

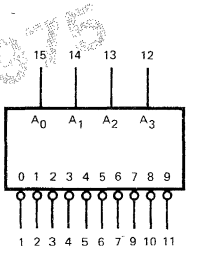
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



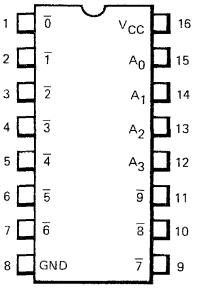
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 9LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the 9LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the 9LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS42XM/54LS42XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS42XC/74LS42XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	12	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

5

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		11 18	18 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		12 19	20 27	ns	Fig. 1	

AC WAVEFORMS

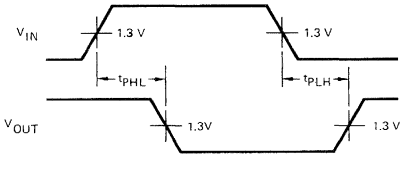


Fig. 1

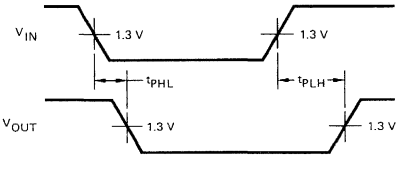


Fig. 2

9LS83 (54LS/74LS83A)

4-BIT BINARY FULL ADDER WITH FAST CARRY

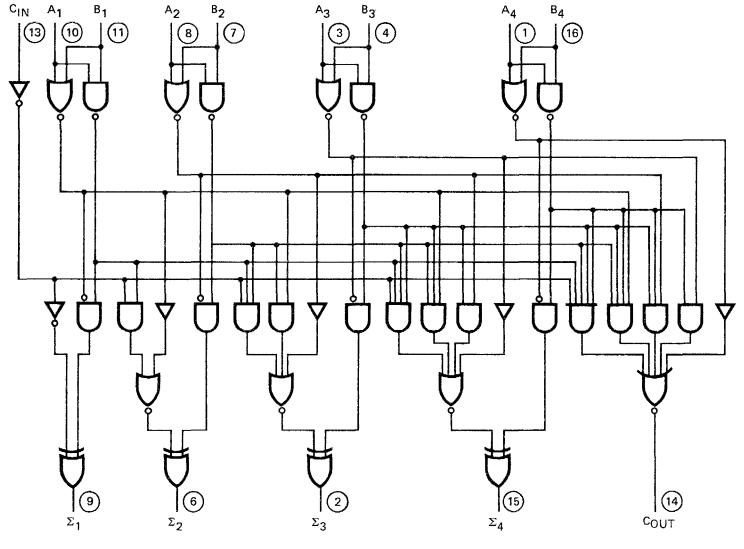
DESCRIPTION — The 9LS83 (54LS/74LS83A) is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The 9LS83 operates with either active HIGH or active LOW operands (positive or negative logic). The 9LS283 (54LS/74LS283) is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

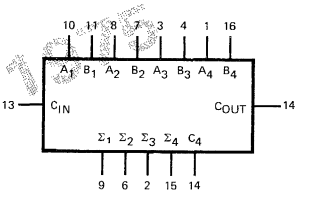
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



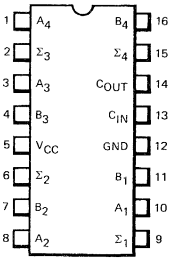
V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS83 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the 9LS83 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

5

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS83XM/54LS83AXM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS83XC/74LS83AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

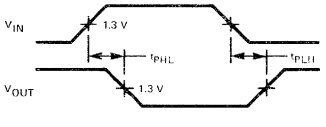


Fig. 1

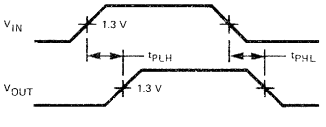


Fig. 2

9LS90 (54LS/74LS90) • 9LS92 (54LS/74LS92)

DECADE COUNTER DIVIDE-BY-TWELVE COUNTER

9LS93 (54LS/74LS93)

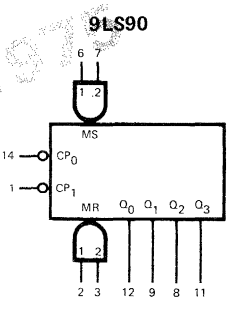
4-BIT BINARY COUNTER

DESCRIPTION — The 9LS90 (54LS/74LS90), 9LS92 (54LS/74LS92) and 9LS93 (54LS/74LS93) are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (9LS90), divide-by-six (9LS92) or divide-by-eight (9LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the 9LS90 also has a 2-input gated Master Set (Preset 9).

- **LOW POWER CONSUMPTION . . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

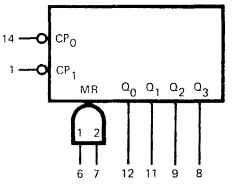
LOGIC SYMBOL

9LS90



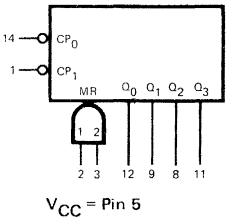
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

9LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

9LS93



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

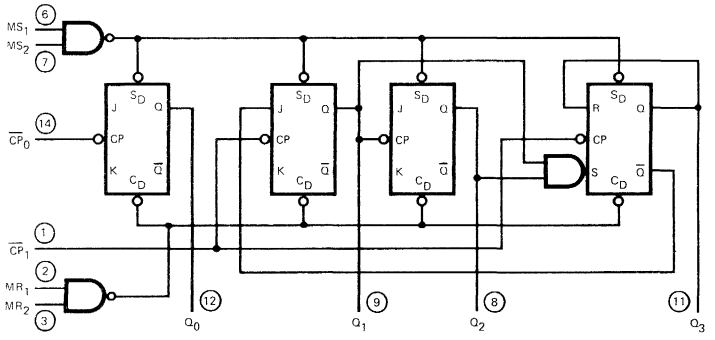
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (9LS90), ÷6 Section (9LS92)	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (9LS93)	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, 9LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (9LS90), ÷6 (9LS92), ÷8 (9LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.

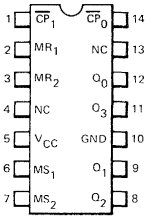
LOGIC DIAGRAM

9LS90



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

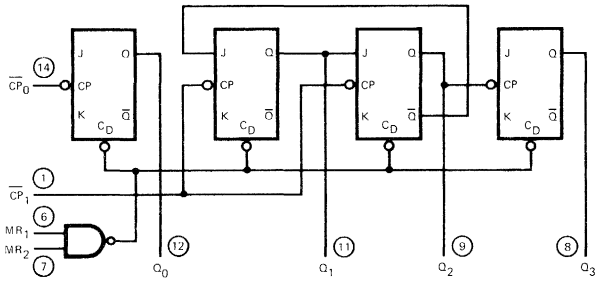


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

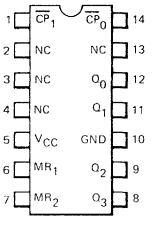
LOGIC DIAGRAM

9LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

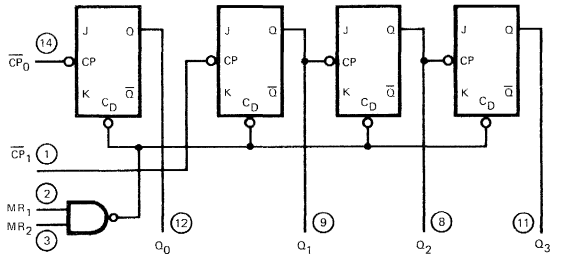


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

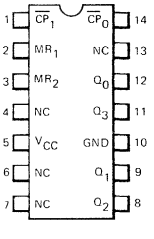
LOGIC DIAGRAM

9LS93



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 9LS90, 9LS92, and 9LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (9LS90), divide-by-six (9LS92), or divide-by-eight (9LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the 9LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

9LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

9LS92

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

9LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

9LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

9LS92 AND 9LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

9LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

9LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input CP_1.

9LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS90XM/54LS90XM 9LS92XM/54LS92XM 9LS93XM/54LS93XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS90XC/74LS90XC 9LS92XC/74LS92XC 9LS93XC/74LS93XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current MS, MR				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_0$				120		
	$\overline{CP}_1$ (LS93)				40		
	$\overline{CP}_1$ (LS90, LS92)				80		
	MS, MR				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_0$, $\overline{CP}_1$ (LS93)				0.4		
	$\overline{CP}_1$ (LS90, LS92)				0.8		
I_{IL}	Input LOW Current MS, MR				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_0$				−2.4		
	$\overline{CP}_1$ (LS93)				−1.6		
	$\overline{CP}_1$ (LS90, LS92)				−3.2		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS						UNITS	
		9LS90		9LS92		9LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		MHz	Fig. 1
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		MHz	Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	ns	Fig. 1
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	ns	
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30					ns	Fig. 3
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40					ns	Fig. 2
t_{PHL}	MR Input to Any Output		40		40		40	ns	Fig. 2

AC SET-UP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS	
		9LS90		9LS92		9LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns	Fig. 1
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns	
t_W	MS Pulse Width	15						ns	Fig. 2, 3
t_W	MR Pulse Width	15		15		15		ns	Fig. 2
t_{rec}	Recovery Time MS to $\overline{CP}$	25						ns	Fig. 2, 3
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns	Fig. 2

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

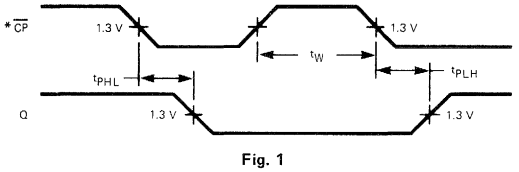


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

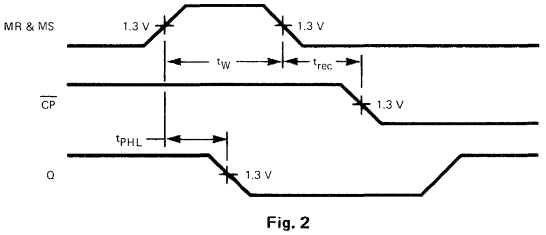


Fig. 2

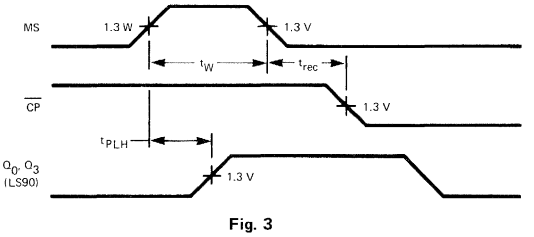


Fig. 3

9LS95 (54LS/74LS95B)

4-BIT SHIFT REGISTER

DESCRIPTION — The 9LS95 (54LS/74LS95B) is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The 9LS95 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

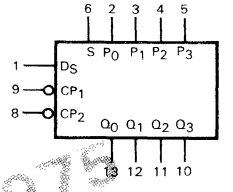
- **SYNCHRONOUS, EXPANDABLE SHIFT RIGHT**
- **SYNCHRONOUS SHIFT LEFT CAPABILITY**
- **SYNCHRONOUS PARALLEL LOAD**
- **SEPARATE SHIFT AND LOAD CLOCK INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

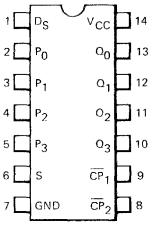
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



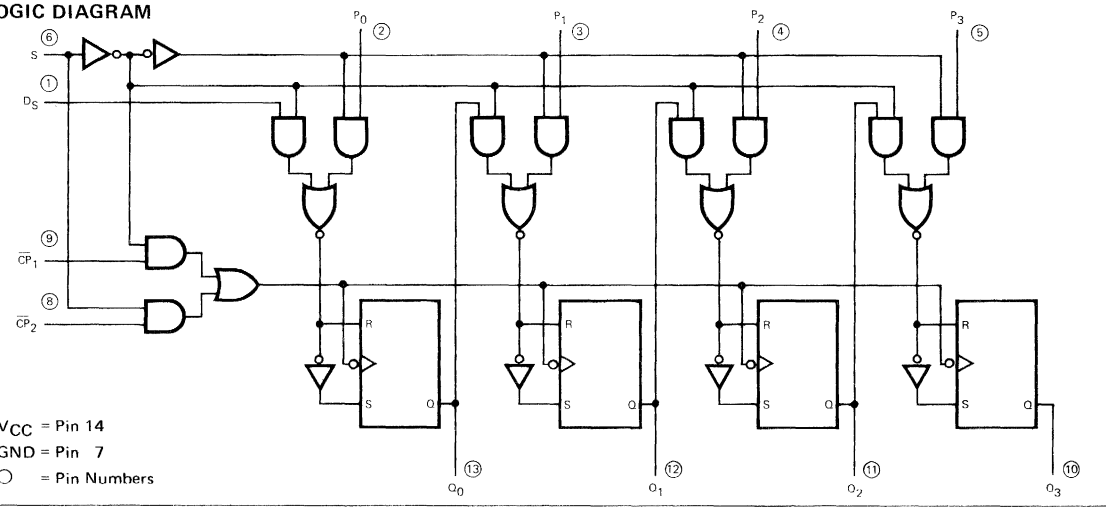
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

5

FUNCTIONAL DESCRIPTION – The 9LS95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel ($P_0 - P_3$) Data inputs and four Parallel Data outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the $P_0 - P_3$ inputs to the $Q_0 - Q_3$ outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the 9LS95 in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	⊓	X	l	X	L	q_0	q_1	q_2
	L	⊓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	⊓	X	p_n	p_0	p_1	p_2	p_3
Mode Change	⊓	L	L	X	X	No Change			
	⊔	L	L	X	X	No Change			
	⊓	H	L	X	X	No Change			
	⊔	H	L	X	X	Undetermined			
	⊓	L	H	X	X	Undetermined			
	⊔	L	H	X	X	No Change			
	⊓	H	H	X	X	Undetermined			
	⊔	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS95XM/54LS95BXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS95XC/74LS95BXC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current S, D_S, P_0, P_1, P_2, P_3				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_1$, $\overline{CP}_2$				40		
	S, D_S, P_0, P_1, P_2, P_3				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_1$, $\overline{CP}_2$				0.2		
I_{IL}	Input LOW Current S, D_S, P_0, P_1, P_2, P_3				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_1$, $\overline{CP}_2$				−0.8		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 18	27 27	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	20			ns	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	10			ns	Fig. 1	
t_{sL}	Set-up Time, LOW Mode Control to Clock	20			ns	Fig. 2	
t_{hL}	Hold Time, LOW Mode Control to Clock	0			ns	Fig. 2	
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			ns	Fig. 2	
t_{hH}	Hold Time, HIGH Mode Control to Clock	0			ns	Fig. 2	

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

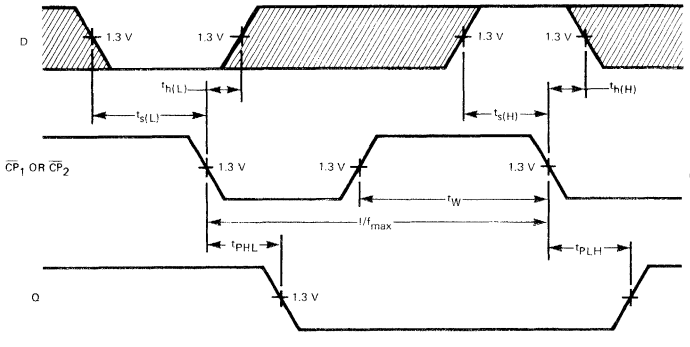


Fig. 1

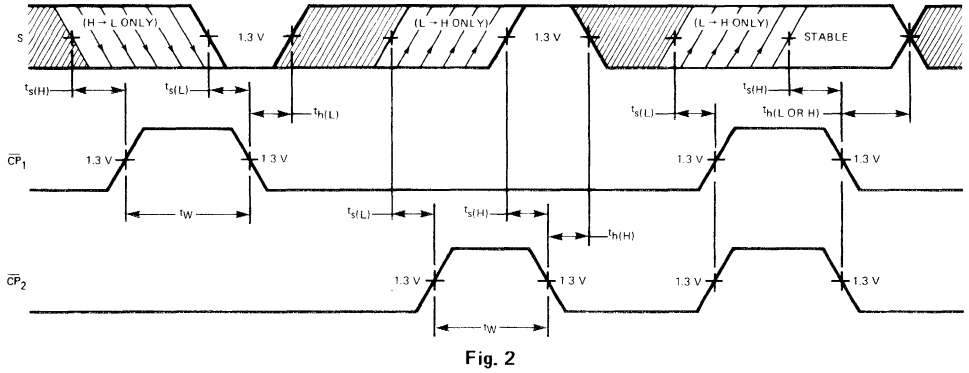


Fig. 2

9LS138 (54LS/74LS138)

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION – The LSTTL/MSI 9LS138 (54LS/74LS138) is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 9LS138 devices or to a 1-of-32 decoder using four 9LS138s and one inverter. The 9LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

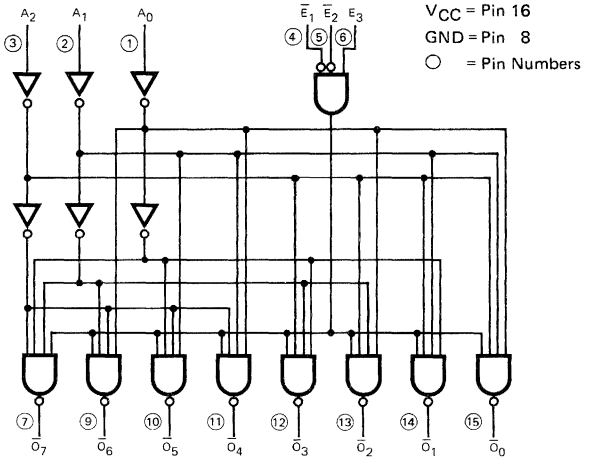
- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- TYPICAL POWER DISSIPATION OF 32 mW
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

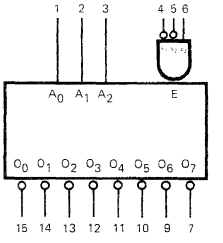
		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM

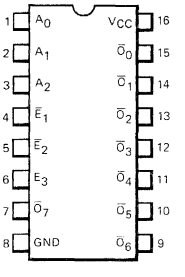


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — The 9LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The 9LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 9LS138s and one inverter. (See Figure a.)

The 9LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

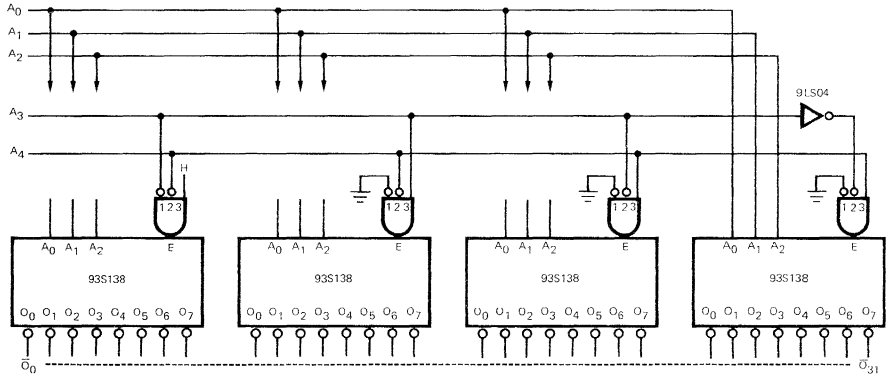


Fig. a.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS138XM / 54LS138XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS138XC/74LS138XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E_1}$ or $\overline{E_2}$ to Output		9.0 17	15 24	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, E_3 to Output		11 20	18 28	ns	Fig. 1	

AC WAVEFORMS

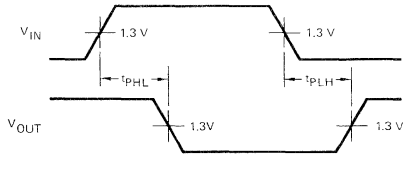


Fig. 1

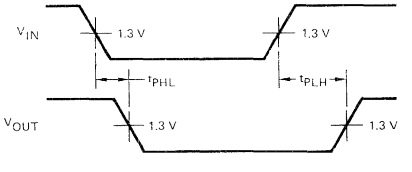


Fig. 2

9LS139 (54LS/74LS139)

DUAL 1-OF-4 DECODER

DESCRIPTION — The LSTTL/MSI 9LS139 (54LS/74LS139) is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 9LS139 can be used as a function generator providing all four minterms of two variables. The 9LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

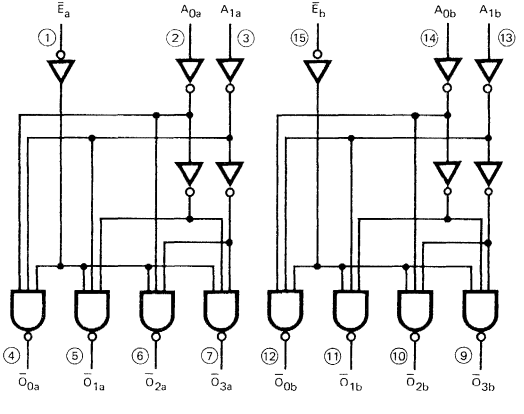
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

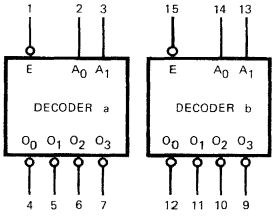
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



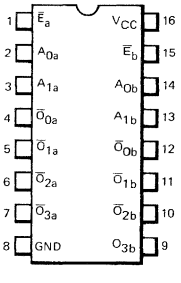
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the 9LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

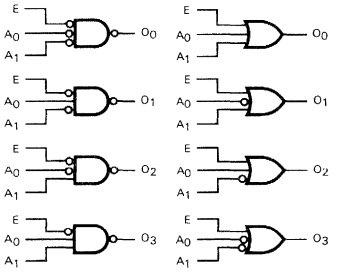


Fig. a

5

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS139XM/54LS139XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS139XC /74LS139XC	4.75 V	5.0 V	5.25 V	0°C to + 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.8	11	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25° C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		9.0 17	15 24	ns	Fig. 2	

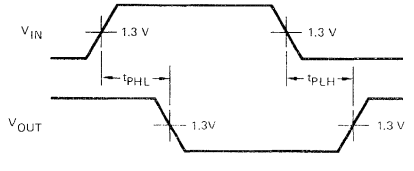


Fig. 1

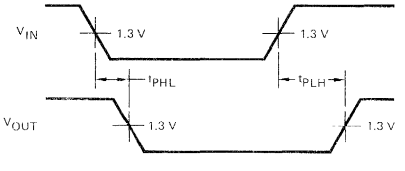


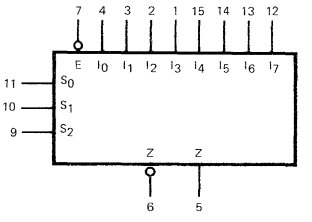
Fig. 2

9LS151 (54LS/74LS151)
8-INPUT MULTIPLEXER

DESCRIPTION – The TTL/MSI 9LS151 (54LS151/74LS151) is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 9LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

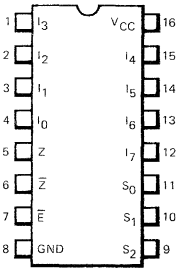
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



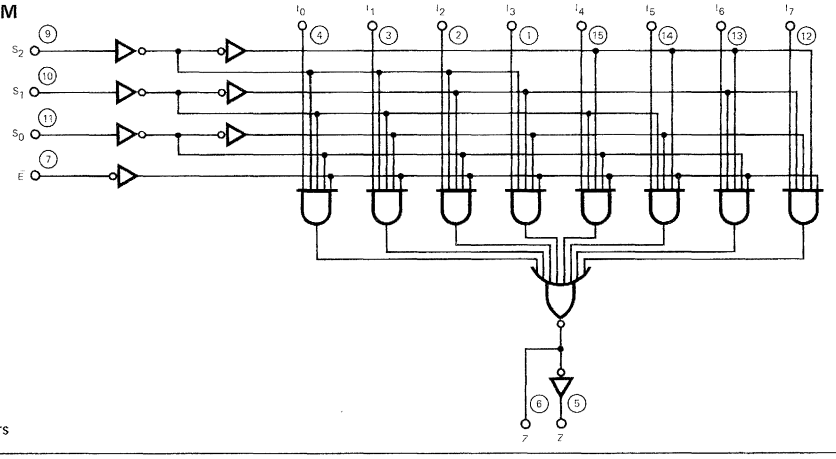
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 9LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS151XM/54LS151XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS151XC/74LS151XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.0	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

5

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	41 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Z}$ Output		13 17	20 26	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Z Output		22 18	33 27	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	26 23	ns	Fig. 2	

AC WAVEFORMS

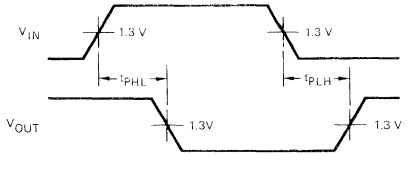


Fig. 1

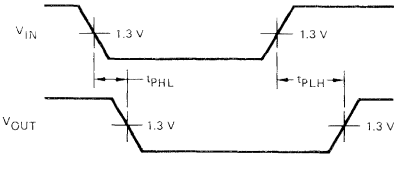


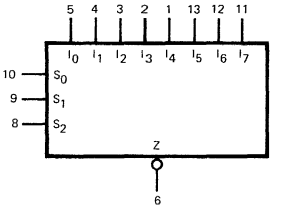
Fig. 2

9LS152 (54LS/74LS152)
8-INPUT MULTIPLEXER

DESCRIPTION – The TTL/MSI 9LS152 (54LS152/74LS152) is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 9LS152 can be used as a universal function generator to generate any logic function of four variables. It is supplied in FLATPAK only; for Dual In-line Package application use the 9LS151.

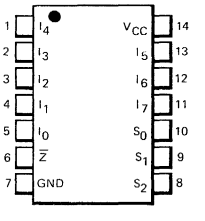
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
FLATPAK (TOP VIEW)



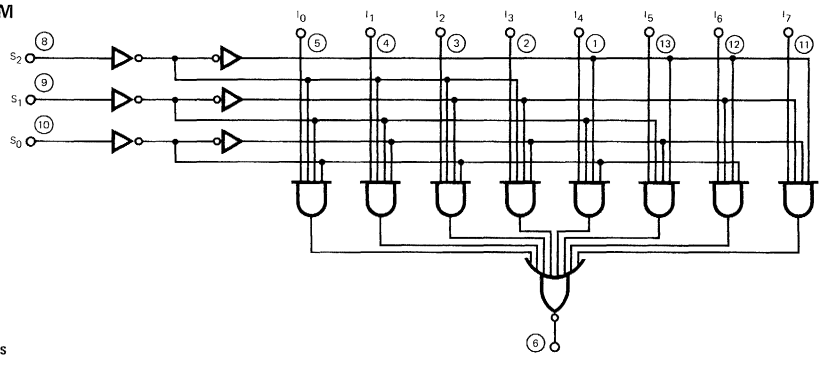
Dot Indicates Pin 1

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 9LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The logic function provided at the output is:

$$\overline{Z} = (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9LS152 provides the ability, in one package, to select from eight sources of data or control information.

TRUTH TABLE

S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$
X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS152XM/54LS152XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS152XC/74LS152XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			5.6	9.0	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		12 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		8.0 10	13 15	ns	Fig. 1	C_L = 15 pF

AC WAVEFORMS

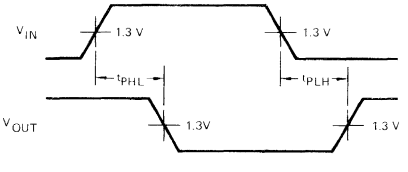


Fig. 1

9LS153 (54LS/74LS153)

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The LSTTL/MSI 9LS153 (54LS/74LS153) is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 9LS153 can generate any two functions of three variables. The 9LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

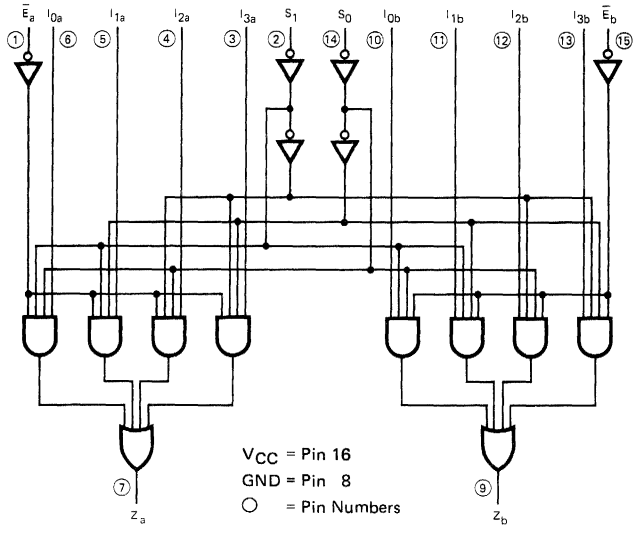
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **SEPARATE ENABLE FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

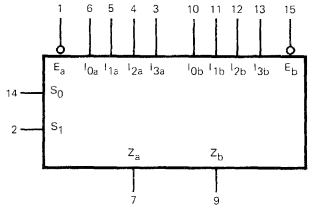
		LOADING (Note a) HIGH	LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM

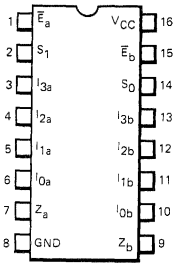


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — The 9LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The 9LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The 9LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The 9LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS153XM/54LS153XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS153XC/74LS153XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		20 16	29 24	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		17 14	24 20	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 2	

AC WAVEFORMS

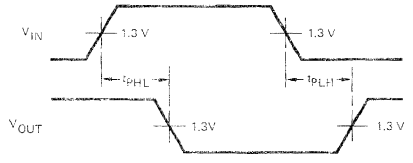


Fig. 1

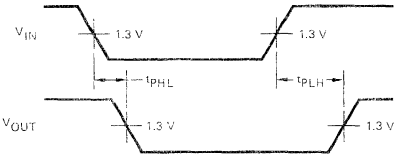


Fig. 2

9LS155 (54LS/74LS155)
9LS156 (54LS/74LS156)

DUAL 1-OF-4 DECODER/DEMULTIPLEXER
(9LS156 HAS OPEN COLLECTOR OUTPUTS)

DESCRIPTION — The LSTTL/MSI 9LS155 (54LS/74LS155) and 9LS156 (54LS/74LS156) are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The 9LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The 9LS155 and 9LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Fairchild TTL families.

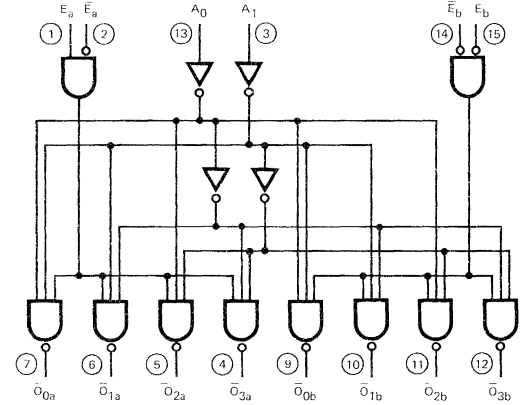
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **COMMON ADDRESS INPUTS**
- **TRUE OR COMPLEMENT DATA DEMULTIPLEXING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a$, $\overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

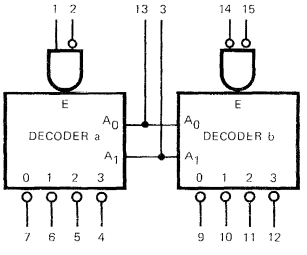
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The HIGH level drive for the 9LS156 must be established by an external resistor.

LOGIC DIAGRAM



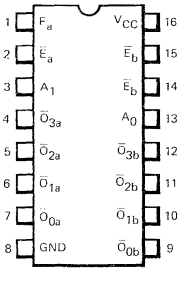
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 9LS155 and 9LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The 9LS155 or 9LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The 9LS155 and 9LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The 9LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

where $E = E_a + \overline{E}_a$; $E = E_b + E_b$

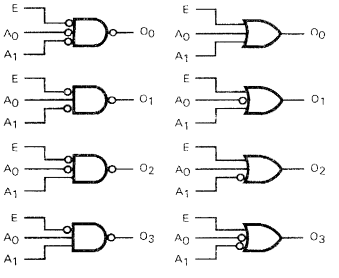


Fig. a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS155XM/54LS155XM 9LS156XM/54LS156XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS155XC/74LS155XC 9LS156XC/74LS156XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
	9LS155 Only	XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OH}	Output HIGH Current 9LS156 Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 9LS155 TYP	LIMITS 9LS155 MAX	LIMITS 9LS156 TYP	LIMITS 9LS156 MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	11 19	18 27	18 23	28 33	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	9.0 17	15 24	16 21	25 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	11 20	18 28	18 24	28 34	ns	Fig. 1	

AC WAVEFORMS

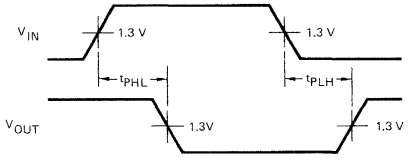


Fig. 1

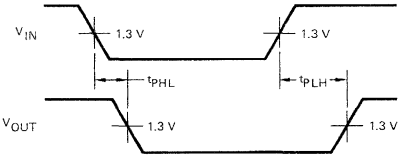


Fig. 2

5

9LS157 (54LS/74LS157)

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The LSTTL/MSI 9LS157 (54LS/74LS157) is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 9LS157 can also be used to generate any four of the 16 different functions of two variables. The 9LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

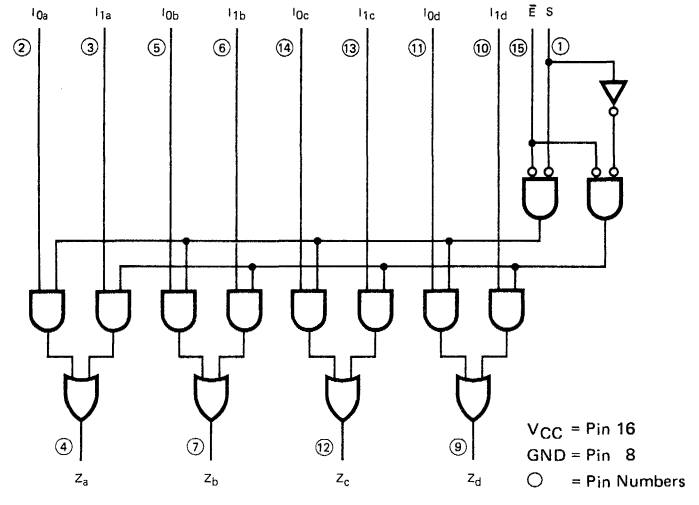
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

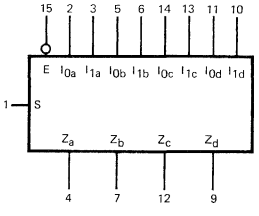
		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM

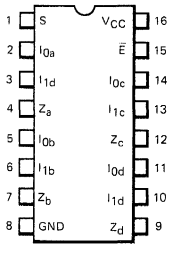


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 9LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The 9LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the 9LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The 9LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS157XM / 54LS157XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9LS157XC / 74LS157XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{I_0}$, I_1 $\overline{E}$, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage $\overline{I_0}$, I_1 $\overline{E}$, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{I_0}$, I_1 $\overline{E}$, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9.7	16	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			26 24	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			25 18	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 2	

AC WAVEFORMS

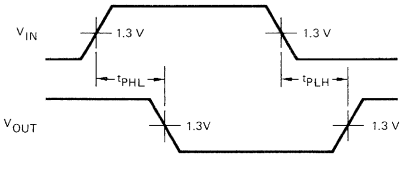


Fig. 1

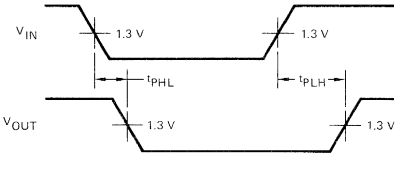


Fig. 2

9LS158 (54LS/74LS158)

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The LSTTL/MSI 9LS158 (54LS/74LS158) is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 9LS158 can also generate any four of the 16 different functions of two variables. The 9LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

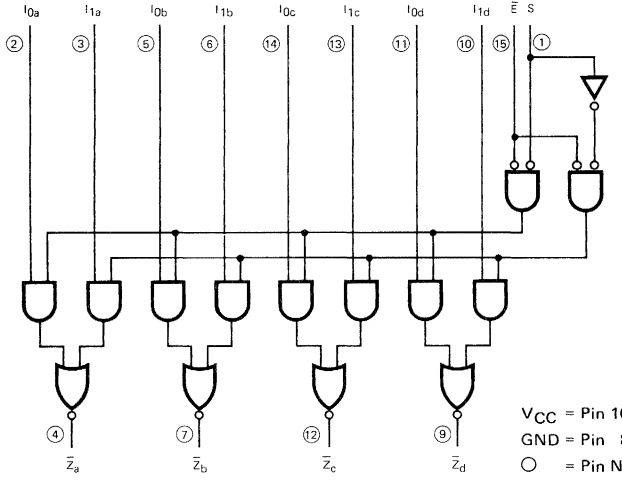
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INVERTED OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

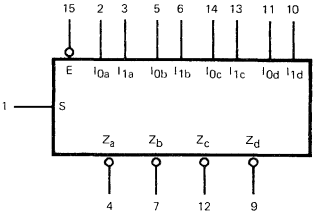
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



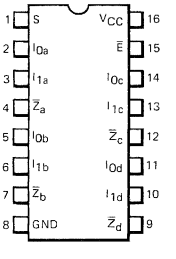
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION – The 9LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The 9LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the 9LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The 9LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS158XM/54LS158XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS158XC/74LS158XC	4.75 V	5.0 V	5.25 V	0°C to + 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current I_0, I_1				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	E, S				40		
	Input HIGH Current at MAX Input Voltage I_0, I_1				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	E, S				0.2		
I_{IL}	Input LOW Current I_0, I_1				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	E, S				−0.8		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.8	8.0	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH}	Propagation Delay			20	ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Select to Output			24			
t_{PLH}	Propagation Delay,			16	ns	Fig. 2	
t_{PHL}	Enable to Output			16			
t_{PLH}	Propagation Delay,			13	ns	Fig. 1	
t_{PHL}	Data to Output			11			

AC WAVEFORMS

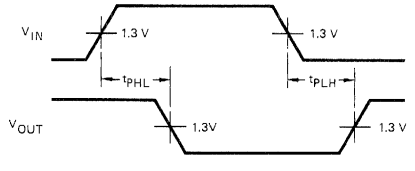


Fig. 1

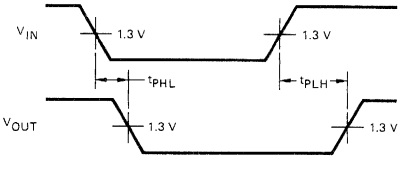


Fig. 2

9LS160(54LS/74LS160) • 9LS161(54LS/74LS161)
9LS162(54LS/74LS162) • 9LS163(54LS/74LS163)

BCD DECADE COUNTERS 4-BIT BINARY COUNTERS

DESCRIPTION — The 9LS160/161/162/163 are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The 9LS160 and 9LS162 count modulo 10 (BCD). The 9LS161 and 9LS163 count modulo 16 (binary.)

The 9LS160 and 9LS161 have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The 9LS162 and 9LS163 have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	9LS160	9LS161
Synchronous Reset	9LS162	9LS163

- **SYNCHRONOUS COUNTING AND LOADING**
- **TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION**
- **TERMINAL COUNT FULLY DECODED**
- **EDGE-TRIGGERED OPERATION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **FULLY TTL AND CMOS COMPATIBLE**

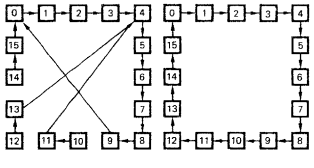
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.6 U.L.	0.3 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.6 U.L.	0.3 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.6 U.L.	0.3 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commerical (XC) Temperature Ranges.

STATE DIAGRAM

9LS160 • 9LS162 **9LS161 • 9LS163**

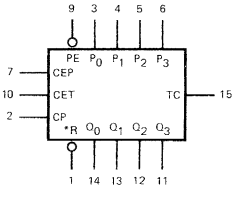


LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for 9LS160 & 9LS162 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for 9LS161 & 9LS163 = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP+ (rising clock edge)
Reset = $\overline{MR}$ (9LS160 & 9LS161)
Reset = $\overline{SR}$ • CP+ (rising clock edge)
(9LS162 & 9LS163)

NOTE:
The 9LS160 and 9LS162 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

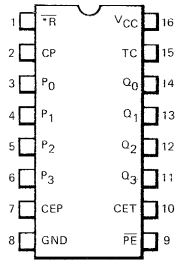
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

*MR for 9LS160 and 9LS161
*SR for 9LS162 and 9LS163

CONNECTION DIAGRAMS
DIP (TOP VIEW)



*$\overline{MR}$ for 9LS160 and 9LS161
*$\overline{SR}$ for 9LS162 and 9LS163

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS160/161/162/163 are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggerd D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the 9LS160 and 9LS161) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs – Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the $\overline{PE}$ held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The 9LS160 and 9LS162 count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The 9LS161 and 9LS163 count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the 9LS160 and 9LS161 is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the 9LS162 and 9LS163 acts as an edge-triggered control input, overriding CET, CEP, and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 9LS162 and 9LS163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Enter Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS160XM/54LS160XM 9LS161XM/54LS161XM 9LS162XM/54LS162XM 9LS163XM/54LS163XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS160XC/74LS160XC 9LS161XC/74LS161XC 9LS162XC/74LS162XC 9LS163XC/74LS163XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA V_{IL} per Truth Table
I_{IH}	Input HIGH Current $P_0 - P_3$, $\overline{MR}$, $\overline{SR}$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PE}$, CEP, CP				24		
	CET				40		
	$P_0 - P_3$, MR, SR, PE, CEP CP				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	CET				0.2		
I_{IL}	Input LOW Current $P_0 - P_3$, $\overline{MR}$, $\overline{SR}$				−0.40	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{PE}$, CEP, CP				−0.48		
	CET				−0.80		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Power Supply Current			18	31	mA	V_{CC} = MAX
I_{CCL}				19	32		

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (These parameters apply to all four devices unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Turn Off Delay CP to Q Turn On Delay CP to Q		13 18	20 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Turn Off Delay CP to TC Turn On Delay CP to TC		15 14	22 21	ns	Fig. 4	
t_{PLH} t_{PHL}	Turn Off Delay CET to TC Turn On Delay CET to TC		9.0 16	14 23	ns	Fig. 3	
t_{PHL}	Turn On Delay $\overline{MR}$ to Q (9LS160 and 9LS161 Only)		18	28	ns	Fig. 2	
f_{count}	Input Count Frequency	25	35		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{rec}	Recovery Time for $\overline{MR}$ (9LS160 and 9LS161 Only)	20			ns	Fig. 2	V_{CC} = 5.0 V
$t_{W\overline{MR}(L)}$	Master Reset Pulse Width (9LS160 and 9LS161 Only)	15	8.0		ns	Fig. 2	
$t_{WCP(H)}$ $t_{WCP(L)}$	Clock Pulse Width (HIGH) Clock Pulse Width (LOW)	15 25	10 18		ns	Fig. 1	
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), Data to Clock Set-Up Time (LOW), Data to Clock	20 20			ns	Fig. 5	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), Data to Clock Hold Time (LOW), Data to Clock	3.0 3.0					
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Set-Up Time (LOW), $\overline{PE}$ or $\overline{SR}$ to Clock	20 20			ns	Fig. 6	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Hold Time (LOW), $\overline{PE}$ OR $\overline{SR}$ to Clock	0 0					
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), CE to Clock Set-Up Time (LOW), CE to Clock	20 20			ns	Fig. 7	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), CE to Clock Hold Time (LOW), CE to Clock	0 0					

DEFINITION OF TERMS:

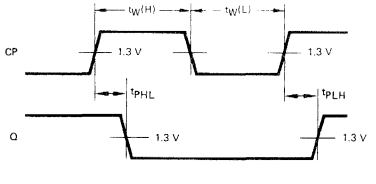
SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

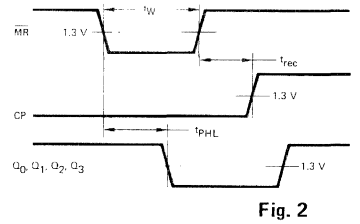
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) state for the 9LS160 and 9LS162 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the 9LS161 and 9LS163.

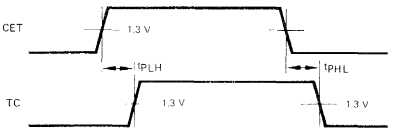


Fig. 3

Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) for the 9LS161 and 9LS163 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the 9LS161 and 9LS163.

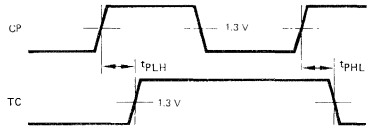


Fig. 4

Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

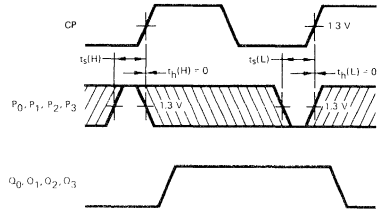


Fig. 5

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

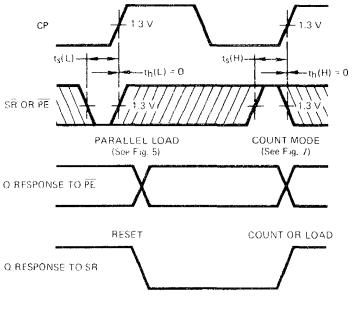
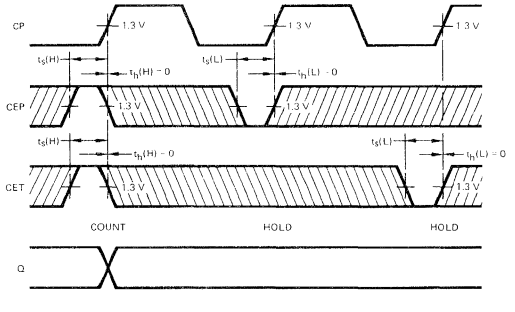


Fig. 6



Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H

Fig. 7

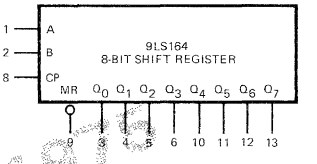
9LS164 (54LS/74LS164)

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION — The 9LS164 (54LS/74LS164) is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL products.

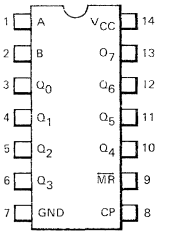
- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



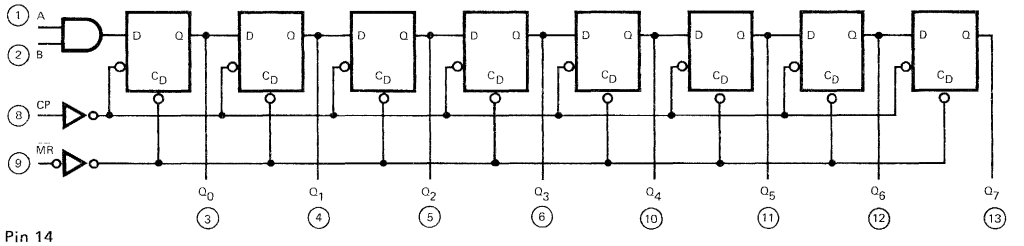
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 9LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A·B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS164XM/54LS164XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS164XC/74LS164XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current (Note 6)			16	27	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.
6. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Fig. 1	V_{CC} = 5 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to Outputs		17 21	27 32	ns	Fig. 1	
t_{PHL}	Propagation Delay, Negative-Going $\overline{MR}$ to Outputs		24	36	ns	Fig. 2	

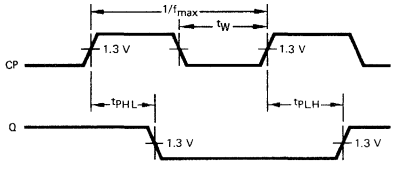
AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			ns	Fig. 3	V_{CC} = 5 V C_L = 15 pF
t_h	Hold Time, A or B Input to Positive-Going CP	5			ns	Fig. 3	
t_WCP(H)	CP Pulse Width (HIGH)	20			ns	Fig. 1	
t_WCP(L)	CP Pulse Width (LOW)	20			ns	Fig. 1	
$t_W\overline{MR}$(L)	$\overline{MR}$ Pulse Width (LOW)	20			ns	Fig. 2	
t_{rec}	Recovery Time, Positive-Going $\overline{MR}$ to Positive-Going CP	20			ns	Fig. 2	

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $\overline{MR}$ = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

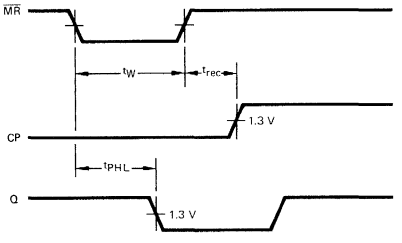


Fig. 2

DATA SET-UP AND HOLD TIMES

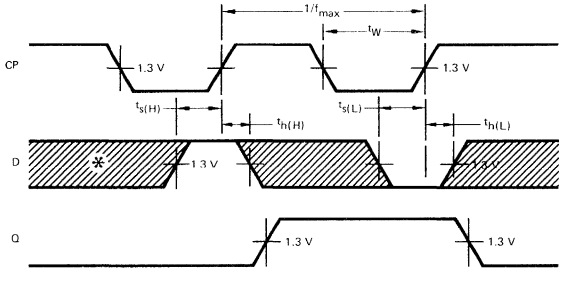


Fig. 3

9LS170 (54LS/74LS170)

4×4 REGISTER FILE (O/C)

DESCRIPTION — The TTL/MSI 9LS170 (54LS/74LS170) is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The 9LS670 (54LS/74LS670) provides a similar function to this device but it features 3-state outputs.

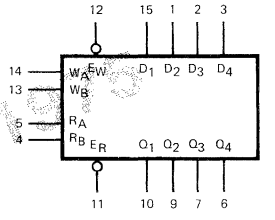
- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_1-Q_4	Outputs (Note b)	Open Collector	5(2.5) U.L.

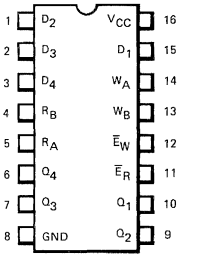
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5.0 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

LOGIC SYMBOL



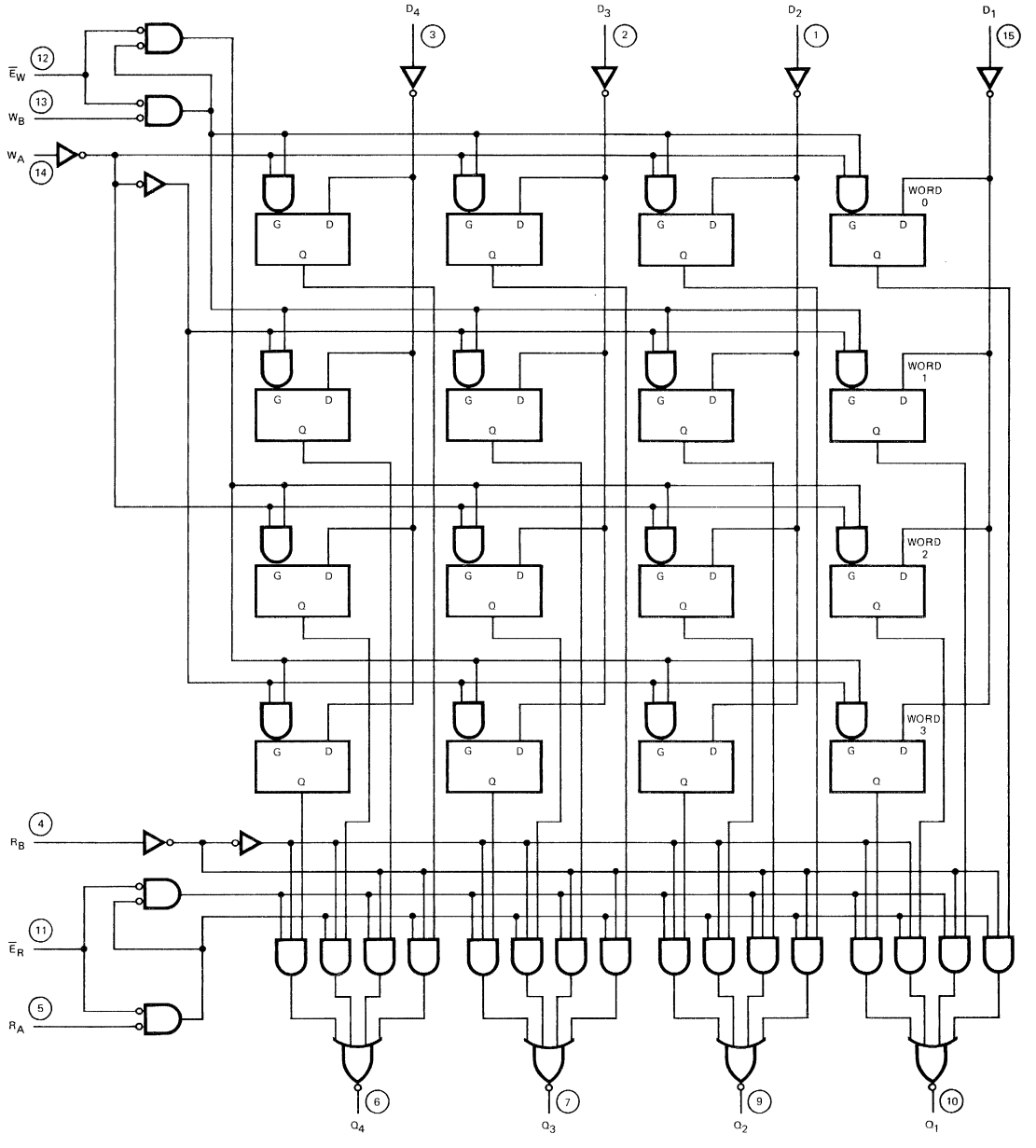
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



◯ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS170XM/54LS170XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS170XC/74LS170XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				20	μA	V_{OH} = 5.5 V, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current Any D, R, or W $\overline{E}_R$ or $\overline{E}_W$				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Any D, R, or W $\overline{E}_R$ or $\overline{E}_W$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_R$ or $\overline{E}_W$				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current (Note 5)			25	40	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_R$ to Q Outputs			30 30	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs			40 40	ns	Fig. 2	$V_{CC} = 5$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_W$ to Q Outputs			45 40	ns	Fig. 1	$R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 35	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 3
t_sD (Note 6)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 8)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:

6. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
7. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
8. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
9. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

AC WAVEFORMS

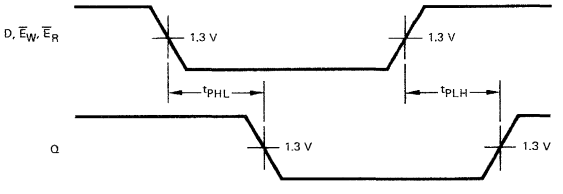


Fig. 1

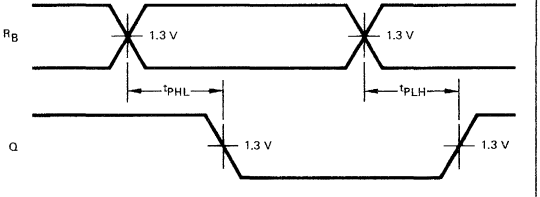


Fig. 2

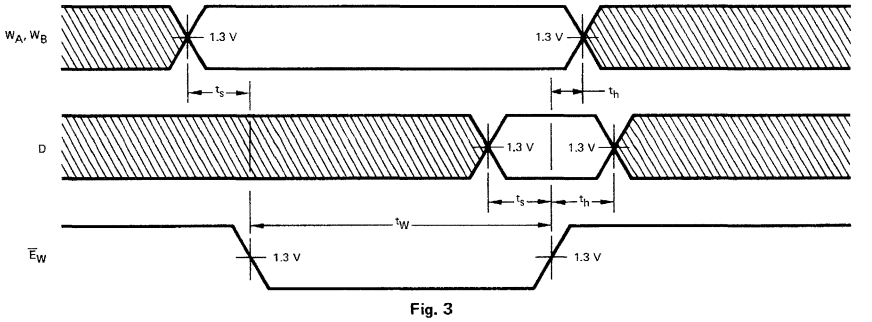


Fig. 3

9LS174 (54LS/74LS174)

HEX D FLIP-FLOP

DESCRIPTION – The LSTTL/MSI 9LS174 (54LS/74LS174) is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The 9LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

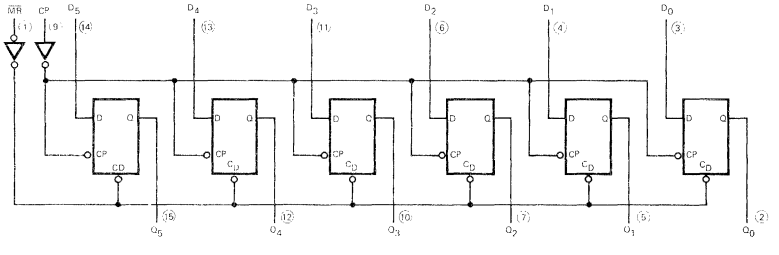
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK
- CLOCK TO OUTPUT DELAYS OF 14 ns
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERNATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

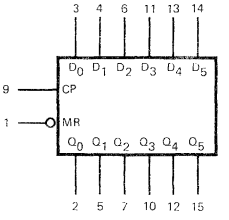
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



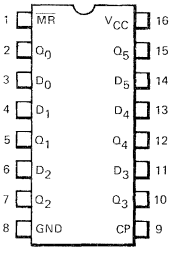
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION – The 9LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 9LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS174XM/54LS174XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS174XC/74LS174XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			16	26	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

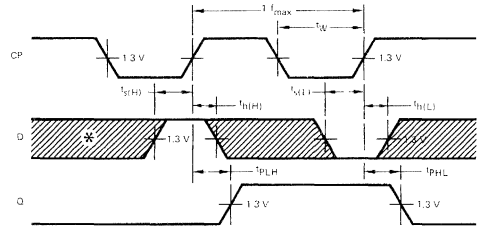
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		20	28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	40	55		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	12	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

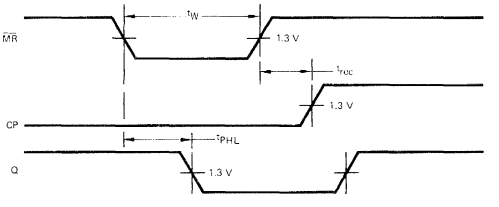


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

9LS175 (54LS/74LS175)

QUAD D FLIP-FLOP

DESCRIPTION — The LSTTL/MSI 9LS175 (54LS/74LS175) is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

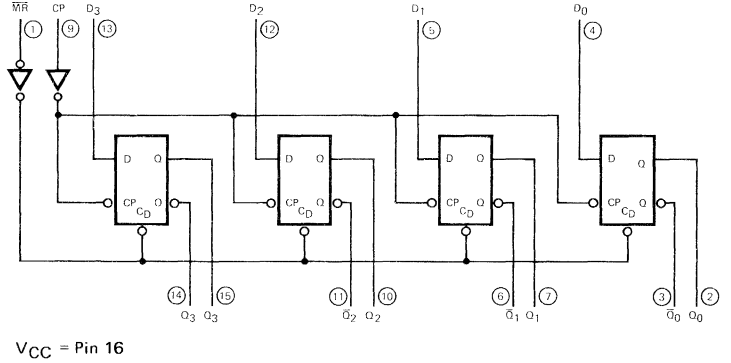
The 9LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 14 ns**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

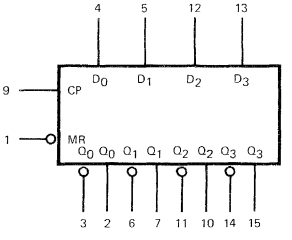
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



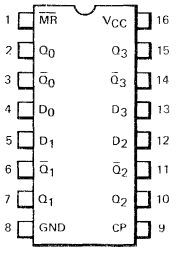
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

The 9LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS175XM/54LS175XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS175XC/74LS175XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = –400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)		–15		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			11	18	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

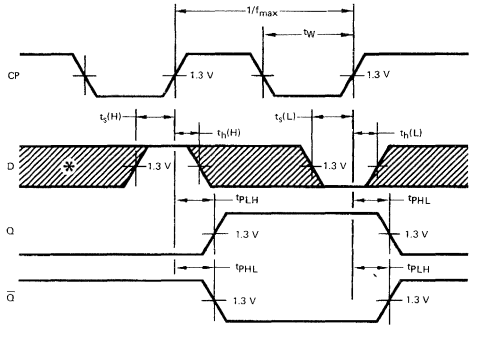
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output		20	28	ns	Fig. 2
t_{PLH}	Propagation Delay, $\overline{MR}$ to $\overline{Q}$ Output		16	24	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	40	55		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	12	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

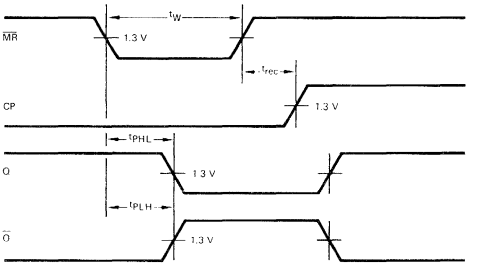


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

9LS181(54LS/74LS181)
4-BIT ARITHMETIC LOGIC UNIT

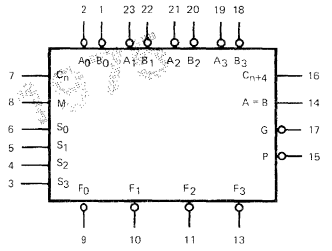
DESCRIPTION — The 9LS181 (54LS/74LS181) is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{A}_0$–$\overline{A}_3$, $\overline{B}_0$–$\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0–S_3	Function – Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C_n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0$–$\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
$\overline{G}$	Carry Generate (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

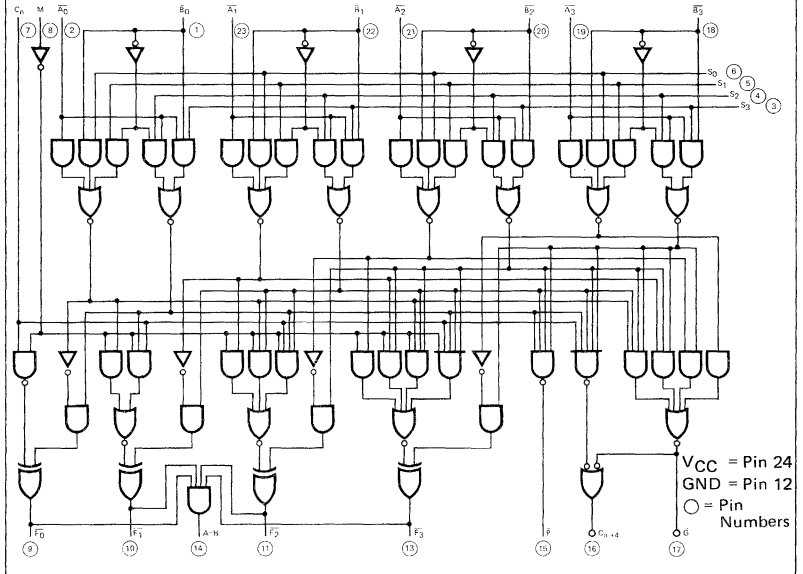
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



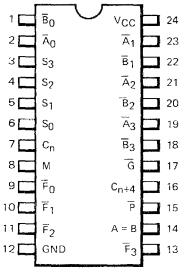
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION – The 9LS181 (54LS/74LS181) is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 9LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the 9LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 9LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 9LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the 9LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{AB}$	$A + \overline{B}$
L	L	H	H	Logical 1	minus 1	Logical 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	$(A + B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus $(A + B)$	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus $(A + B)$	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A*	Logical 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	$(A + B)$ plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level

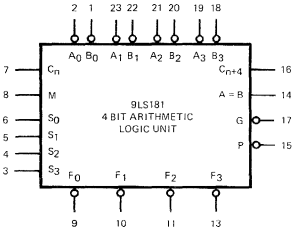
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

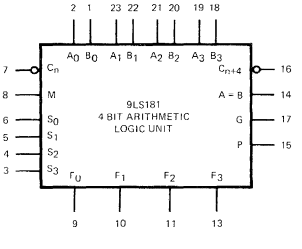
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS181XM/54LS181XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS181XC/74LS181XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
	Any Output except A=B	XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OH}	Output HIGH Current A=B Output Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
	Output LOW Voltage Output $\overline{G}$			0.47	0.7	V	I_{OL} = 16 mA
	Output LOW Voltage Output $\overline{P}$	XM		0.35	0.6	V	I_{OL} = 8.0 mA
		XC		0.35	0.7		
I_{IH}	Input HIGH Current Mode Input				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{A}$ and $\overline{B}$ Inputs				60		
	S Inputs				80		
	Carry Inputs				100		
	Mode Input				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{A}$ and $\overline{B}$ Inputs				0.3		
	S Inputs				0.4		
	Carry Inputs				0.5		
I_{IL}	Input LOW Current Mode Input				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{A}$ and $\overline{B}$ Inputs				−1.08		
	S Inputs				−1.44		
	Carry Inputs				−2.0		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current Condition A (Note 6)	XM		20	32	mA	V_{CC} = MAX
		XC		20	34		
	Power Supply Current Condition B (Note 6)	XM		21	35		
		XC		21	37		

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. With outputs open, I_{CC} is measured for the following conditions:
   A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
   B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND

SYMBOL	PARAMETER	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ Outputs)		26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		32 26	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 23	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{F}$ Outputs)		33 29	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)		50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V, R_L = 2 kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

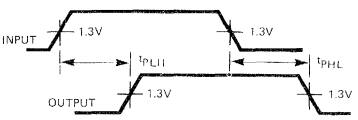


Fig. 4

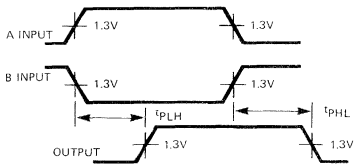


Fig. 5

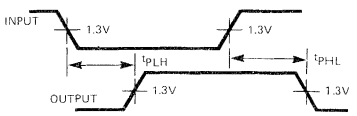


Fig. 6

SUM MODE TEST TABLE I — **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or $C_n + 4$

DIFF MODE TEST TABLE II — **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V

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9LS190 (54LS/74LS190) • 9LS191 (54LS/74LS191)

PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

DESCRIPTION — The 9LS190 (54LS/74LS190) is a synchronous UP/DOWN BCD Decade (8421) Counter and the 9LS191 (54LS/74LS191) is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

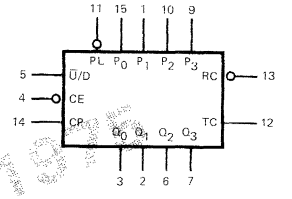
- **LOW POWER . . . 90 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 35 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **COUNT ENABLE AND UP/DOWN CONTROL INPUTS**
- **CASCADABLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}/D$	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{RC}$	Ripple Clock Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

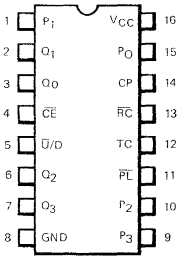
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



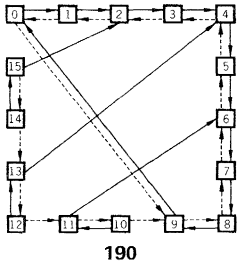
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



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9LS190

UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U/D})$

DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/D})$

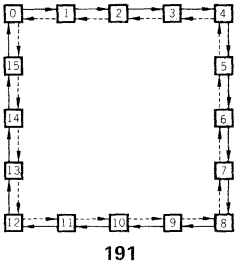
9LS191

UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/D})$

Count Up ——

Count Down ------



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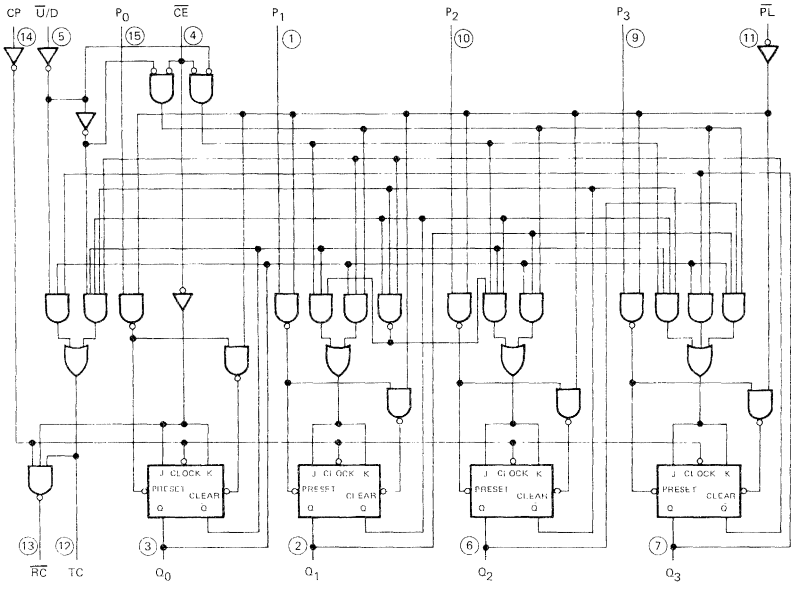
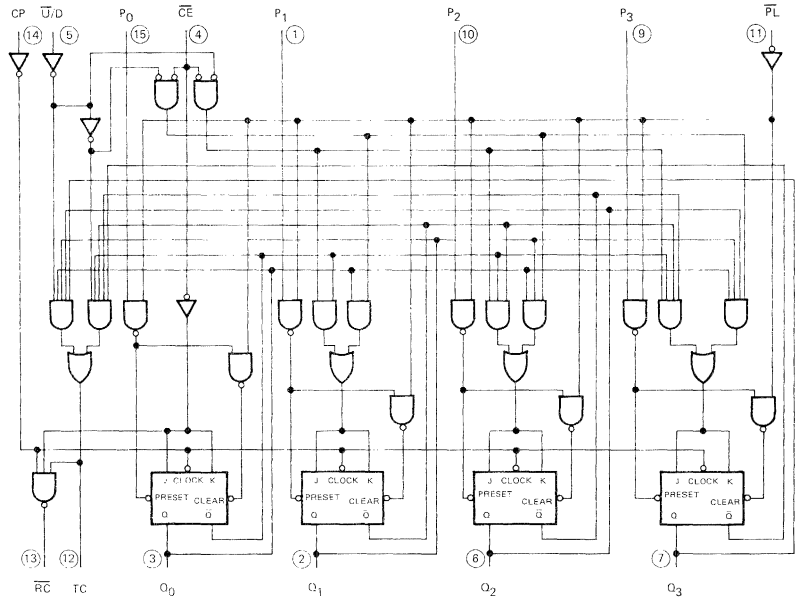
LOGIC DIAGRAMS



DECADE COUNTER
9LS190



BINARY COUNTER
9LS191

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 9LS190 is a synchronous Up/Down BCD Decade Counter and the 9LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the 9LS190 decade counter and the 9LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the 9LS190, 15 for the 9LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{RC}$
$\overline{CE}$	TC*	CP	OUTPUT
L	H	⎍⎍	⎍
H	X	X	H
X	L	X	H

*TC is generated internally

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition
⎍⎍ = LOW Pulse

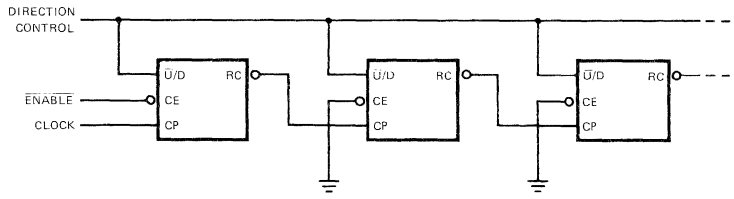


Fig. a) n-stage counter using ripple clock.

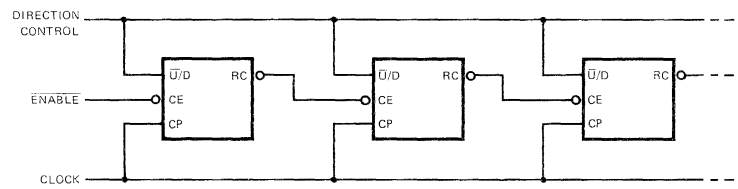


Fig. b) Synchronous n-stage counter using ripple carry/borrow.

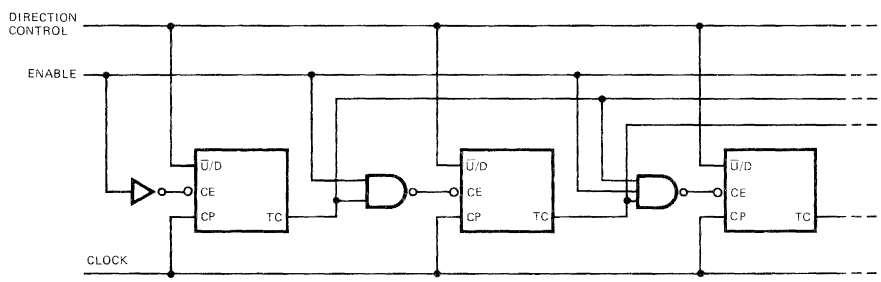


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS190XM/54LS190XM 9LS191XM/54LS191XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS190XC/74LS190XC 9LS191XC/74LS191XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Cermaic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current P_n, $\overline{PL}$, CP, $\overline{U}/D$ $\overline{CE}$				20 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	P_n, $\overline{PL}$, CP, $\overline{U}/D$ $\overline{CE}$				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current P_n, $\overline{PL}$, CP, $\overline{U}/D$ $\overline{CE}$				−0.4 −1.08	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	35	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Count Enable ($\overline{CE}$) and the Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{CE}$ must occur only while the Clock is HIGH for conventional operation.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Max. Input Count Frequency	25	35		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs			24 36	ns	Fig. 1	
t_{PLH} t_{PHL}	CP Input to $\overline{RC}$ Output			20 24	ns	Fig. 2	
t_{PLH} t_{PHL}	CP Input to TC Output			42 52	ns	Fig. 1	
t_{PLH}^* t_{PHL}^*	$\overline{U}/D$ Input to $\overline{RC}$ Output			45 45	ns	Fig. 7	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{U}/D$ Input to TC Output			33 33	ns		
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs to $Q_0 - Q_3$ Outputs			22 50	ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output			33 50	ns	Fig. 4	
t_{PLH}^* t_{PHL}	$\overline{CE}$ Input to $\overline{RC}$ Output			33 33	ns	Fig. 2	

*It is possible to get these timing relationships, but they should not occur during normal operation since the CP would be HIGH.

5

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W	CP Pulse Width	20			ns	Fig. 1	
t_W	$\overline{PL}$ Pulse Width	35			ns	Fig. 4	
t_sL	Set-Up Time LOW, Data to $\overline{PL}$	20			ns	Fig. 6	$V_{CC} = 5.0$ V
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			ns		
t_sH	Set-Up Time HIGH, Data to $\overline{PL}$	20			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP	20			ns	Fig. 5	
t_sL	Set-Up Time LOW, $\overline{CE}$ to Clock	20			ns	Fig. 8	
t_hL	Hold Time LOW, $\overline{CE}$ to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

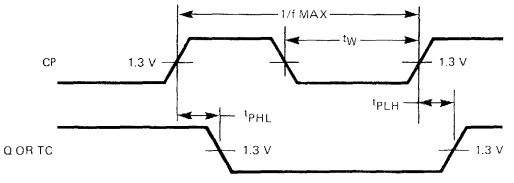


Fig. 1

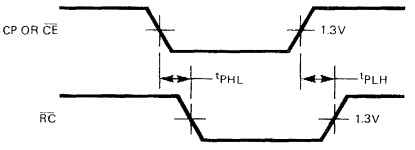
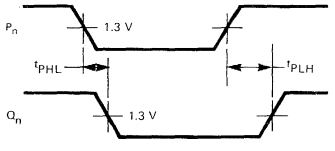


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

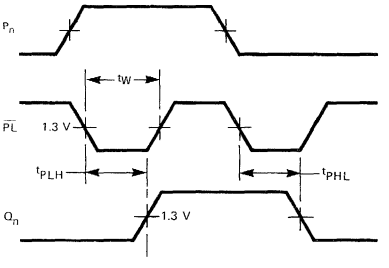


Fig. 4

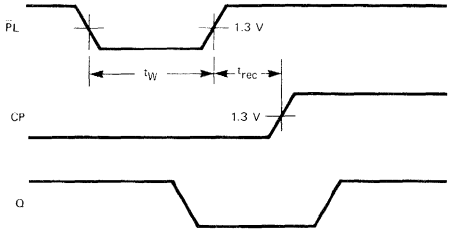
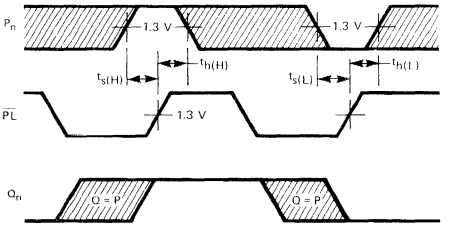


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

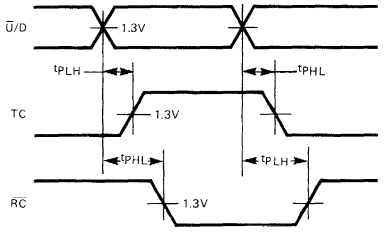


Fig. 7

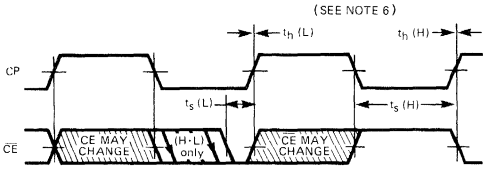


Fig. 8

9LS192 (54LS/74LS192) • 9LS193 (54LS/74LS193)

PRESETTABLE BCD/DECADE UP/DOWN COUNTER

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION — The 9LS192 (54LS/74LS192) is an UP/DOWN BCD Decade (8421) Counter and the 9LS193 (54LS/74LS193) is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

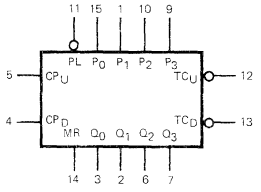
- LOW POWER . . . . 95 mW TYPICAL DISSIPATION
- HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

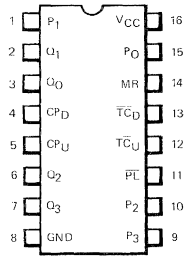
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (XM) and 5 U.L. for COMMERCIAL (XC) Temperature Ranges.

LOGIC SYMBOL



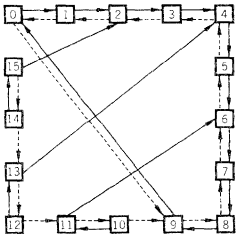
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



9LS192

9LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

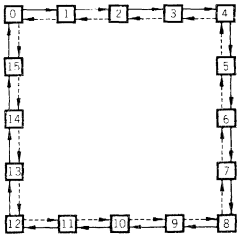
9LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

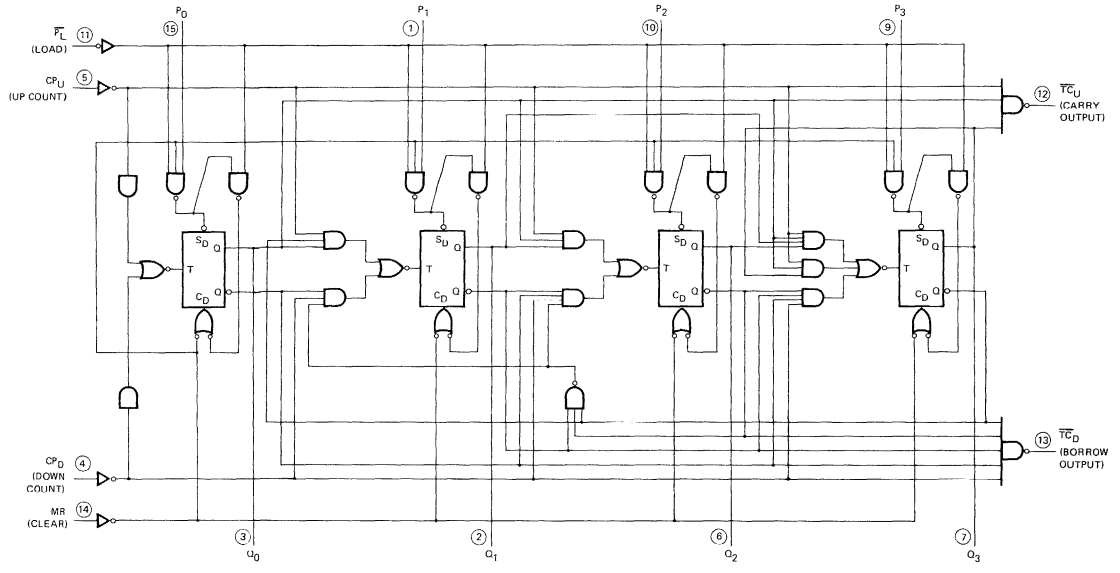
COUNT UP ——

COUNT DOWN ------

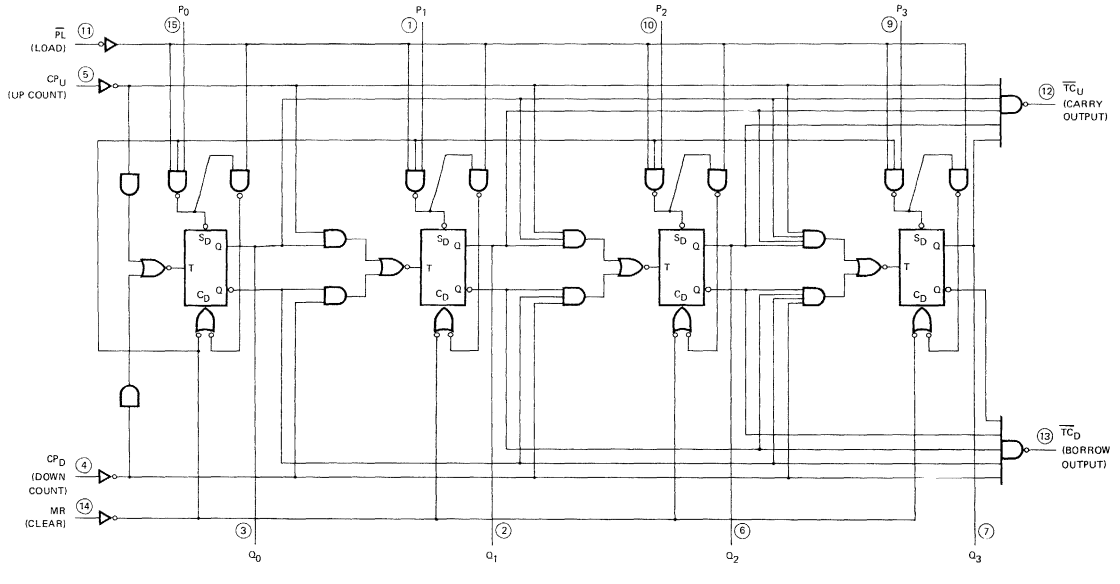


9LS193

LOGIC DIAGRAMS



9LS192



9LS193

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Number

FUNCTIONAL DESCRIPTION — The 9LS192 and 9LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the 9LS192 decade counter and the 9LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the 9LS192, 15 for the 9LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

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MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asnyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0 V
* Input Voltage (dc)	−0.5 V to 15 V
* Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

* Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS192XM/54LS192XM 9LS193XM/54LS193XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS192XC / 74LS192XC 9LS193XC / 74LS193XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			19	34	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, now shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		9LS192			9LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{MAX}	Max Input Count Frequency	30	40		30	40		MHz	Fig. 1	
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		10 14	16 21		10 14	16 21	ns	Fig. 2	
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		10 15	16 22		10 15	16 22	ns		
t_{PLH} t_{PHL}	CP_U or CP_D to Q_n Outputs		22 18	31 28		22 18	31 28	ns		$V_{CC} = 5.0$ V
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs $Q_0 - Q_3$ Outputs							ns	Fig. 3	$C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		23 17	32 25		23 17	32 25	ns	Fig. 4	
t_{PHL}	MR Input to Any Output		17	25		17	25	ns	Fig. 7	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		9LS192			9LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	CP_U Pulse Width	17			17			ns	Fig. 1	
t_W	CP_D Pulse Width	17			17			ns		
t_W	$\overline{PL}$ Pulse Width	15			15			ns	Fig. 4	
t_W	MR Pulse Width	15			15			ns	Fig. 7	
t_sL	Set-up Time LOW, Data to $\overline{PL}$	10			10			ns	Fig. 6	$V_{CC} = 5.0$ V
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			0			ns		
t_sH	Set-up Time HIGH, Data to $\overline{PL}$	10			10			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP							ns	Fig. 5	
t_{rec}	Recovery Time, MR to CP							ns		

5

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transistion from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transistion from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transistion from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

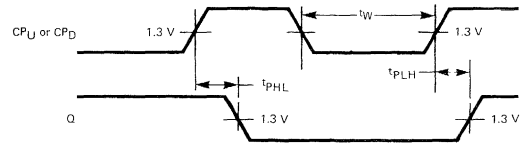


Fig. 1

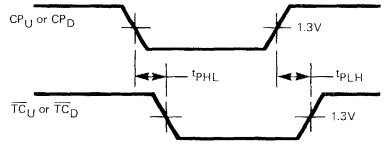
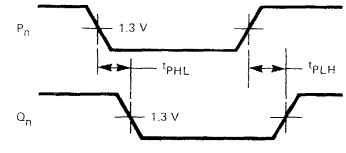


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

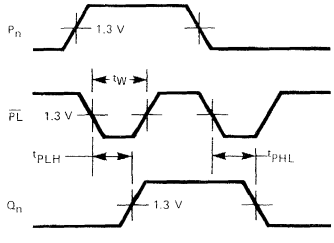


Fig. 4

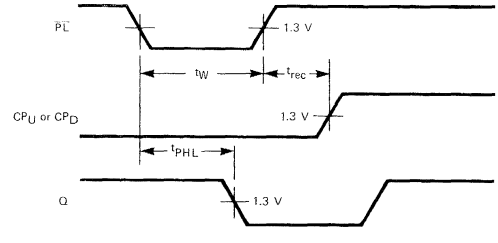
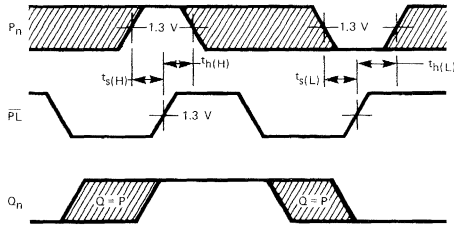


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

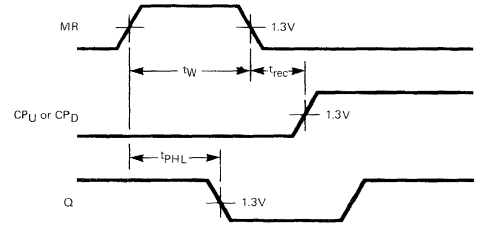


Fig. 7

9LS194(54LS/74LS194A)
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION – The 9LS194 (54LS/74LS194A) is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 9LS194 is similar in operation to the 9LS195 Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL families.

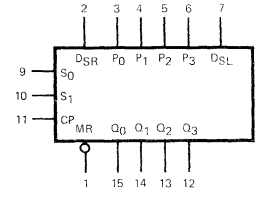
- TYPICAL SHIFT FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

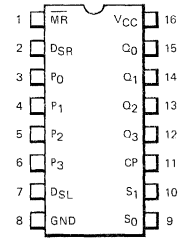
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL

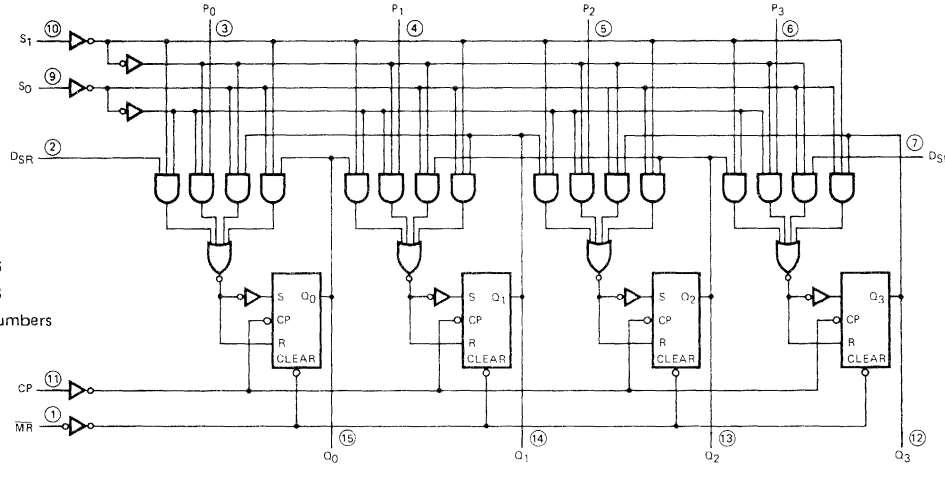


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the 9LS194 4-Bit Bidirectional Shift Register. The 9LS194 is similar in operation to the Fairchild 9LS195 Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the 9LS194 design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

2. D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

L = LOW Voltage Level
H= HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS194XM/54LS194AXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS194XC/74LS194AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			15	23	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			22 15	ns	Fig. 1	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output			18	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	18	12		ns	Fig. 1	$V_{CC} = 5.0$ V
t_s(Data)	Set-up Time, Data to Clock	16			ns	Fig. 3	
t_h(Data)	Hold Time, Data to Clock	0			ns		
t_s(S)	Set-up Time, Mode Control to Clock	20			ns	Fig. 4	
t_h(S)	Hold Time, Mode Control to Clock	0			ns		
t_W(MR)	Master Reset Pulse Width	12			ns	Fig. 2	
t_{rec}(MR)	Recovery Time Master Reset to Clock	18	12		ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

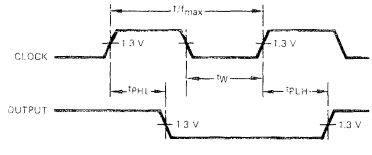
HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

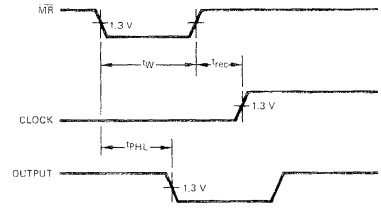
CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH AND f_{max}



OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H

Fig. 1

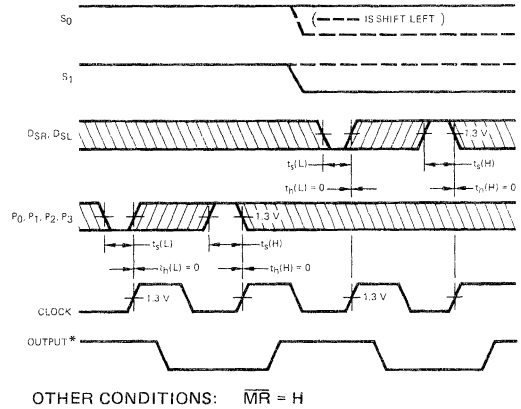
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

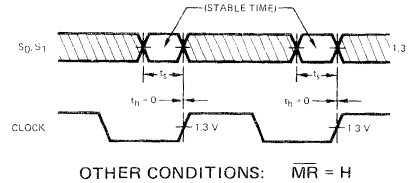


OTHER CONDITIONS: $\overline{MR}$ = H

*D_{SR} set-up time affects Q_0 only
D_{SL} set-up time affects Q_3 only

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 4

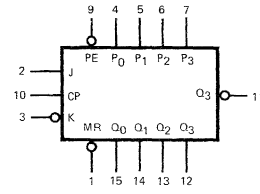
9LS195 (54LS/74LS195A)

UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION — The 9LS195 (54LS/74LS195A) is a high speed 4-Bit Shift Register offering typical shift frequencies of 50 MHz. It is useful for a wide variety of register and counting applications. The 9LS195 is pin and functionally identical to the 9300, 93L00, 93H00 and 54/74195. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL products.

- **TYPICAL SHIFT RIGHT FREQUENCY OF 50 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



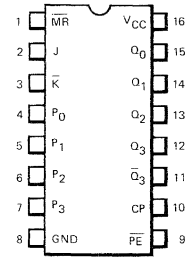
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.	5(2.5) U.L.

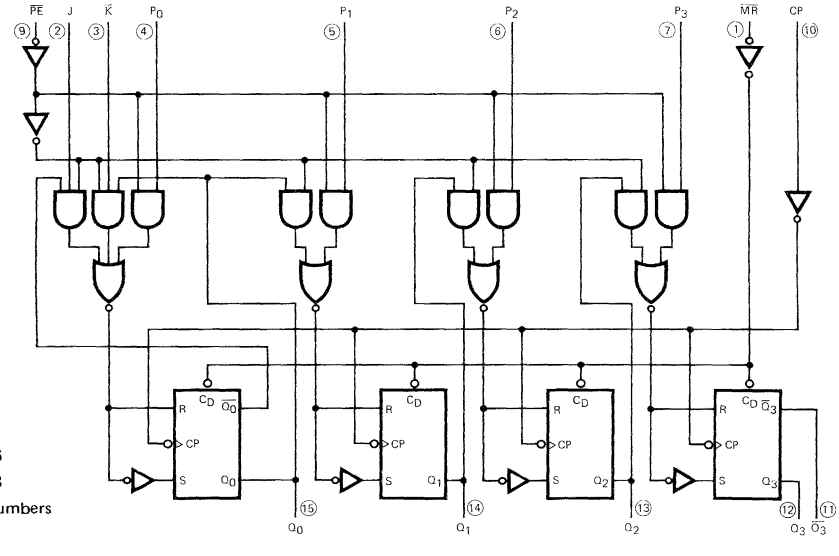
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

5

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the 9LS195 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 9LS195 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins togethers. When the $\overline{PE}$ input is LOW, the 9LS195 appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW to HIGH clock transition. Since the 9LS195 utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation – except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT – TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS195XM/54LS195AXM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS195XC/74LS195AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			14	21	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
5. Not more than one output should be shorted at a time.

5

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		14 13	21 20	ns	Fig. 1	
t_{PHL}	Propagation Delay, MR to Output		13	20	ns	Fig. 3	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	16			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	15	8		ns	Fig. 2	
t_h(Data)	Hold Time, Data to Clock	0	−7		ns		
$t_s(\overline{PE})$	Set-up Time, $\overline{PE}$ Control to Clock	25	18		ns	Fig. 4	
$t_h(\overline{PE})$	Hold Time, $\overline{PE}$ Control to Clock	−10	−17		ns		
$t_{W(\overline{MR})}$	Master Reset Pulse Width	12			ns	Fig. 3	
$t_{rec}(\overline{MR})$	Recovery Time Master Reset to Clock	25			ns		

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

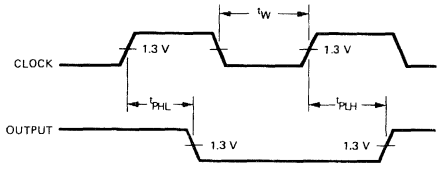
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

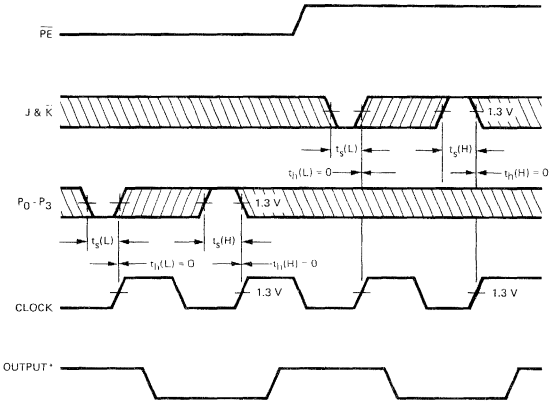
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 1

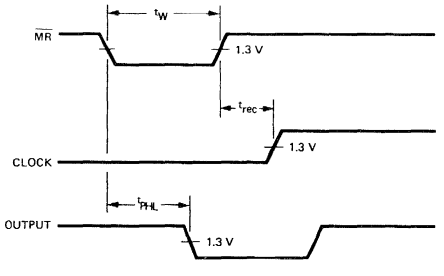
SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



CONDITIONS: $\overline{MR} = H$
*J and $\overline{K}$ set-up time affects Q_0 only

Fig. 2

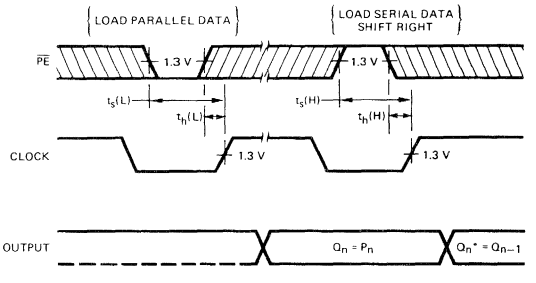
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



CONDITIONS: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



CONDITIONS: $\overline{MR} = H$
*Q_0 state will be determined by J and $\overline{K}$ inputs

Fig. 4

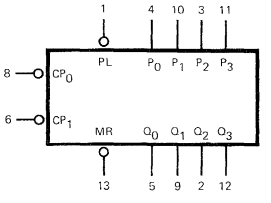
9LS196 (54LS/74LS196)
9LS197 (54LS/74LS197)
4-STAGE PRESETTABLE RIPPLE COUNTERS

DESCRIPTION — The 9LS196 (54LS/74LS196) decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The 9LS197 (54LS/74LS197) contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

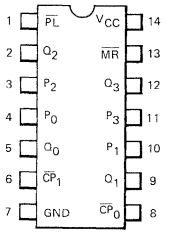
- **LOW POWER CONSUMPTION — TYPICALLY 80 mW**
- **HIGH COUNTING RATES — TYPICALLY 70 MHz**
- **CHOICE OF COUNTING MODES — BCD, BI-QUINARY, BINARY**
- **ASYNCHRONOUS PRESETTABLE**
- **ASYNCHRONOUS MASTER RESET**
- **EASY MULTISTAGE CASCADING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



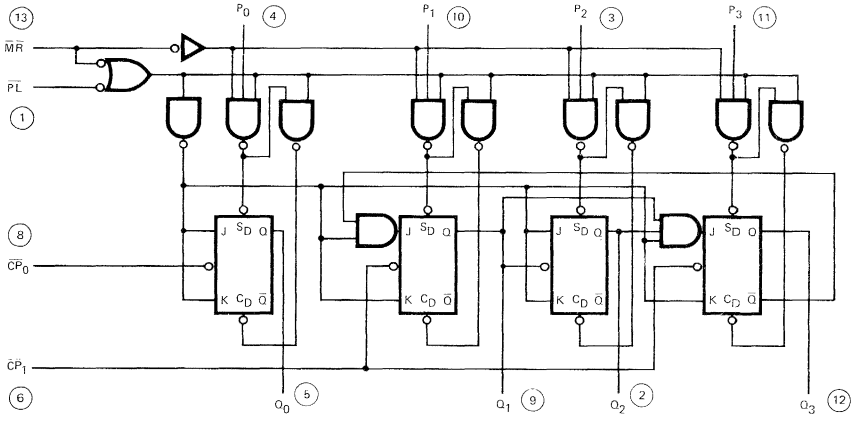
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

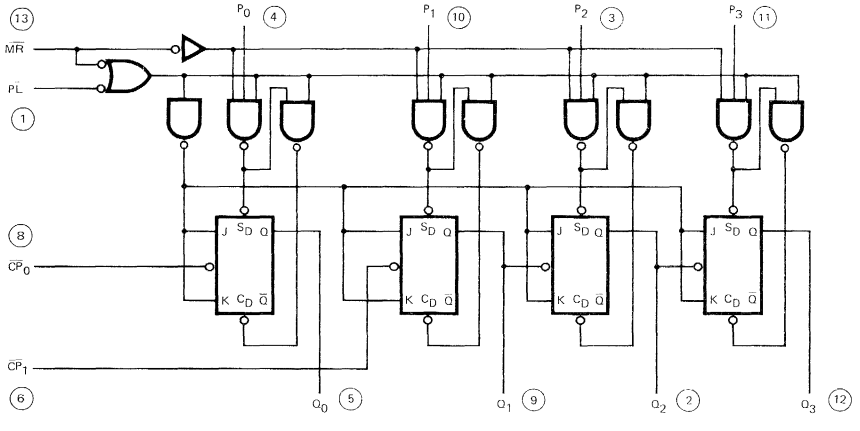
		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	1.0 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Notes b, c)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP}_1$.

LOGIC DIAGRAM



9LS196



9LS197

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 9LS196 and 9LS197 are asynchronously presettable decade and binary ripple counters. The 9LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the 9LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP_0}$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP_1}$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the 9LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

The 9LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The 9LS196 and 9LS197 have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data ($P_0 - P_3$) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

5

Figure 2: 9LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = HIGH to Low Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS196XM/54LS196XM 9LS197XM/54LS197XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS196XC/74LS196XC 9LS197XC/74LS197XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP}_0$ $\overline{CP}_1$ (LS196) $\overline{CP}_1$ (LS197)				−0.36 −0.72 −2.4 −2.8 −1.3	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			12	20	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		9LS196			9LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{max}	Input Count Frequency	45	60		50	75		MHz	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{CP_0}$ Input to Q_0 Output		8.0 8.0	12 12		8.0 8.0	12 12	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_1 Output		9.0 9.0	14 14		9.0 9.0	14 14	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_2 Output		23 21	34 32		26 23	36 34	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_3 Output		12 12	18 18		35 38	50 55	ns		
t_{PLH} t_{PHL}	P_0, P_1, P_2, P_3 Inputs Q_0, Q_1, Q_2, Q_3 Outputs		10 24	15 35		10 24	15 35	ns	Fig. 2	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		15 24	24 35		15 24	24 35	ns	Fig. 3	
t_{PHL}	$\overline{MR}$ Input to Any Output		26	37		26	37	ns	Fig. 4	

5

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		9LS196			9LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	$\overline{CP_0}$ Pulse Width	12			10			ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP_1}$ Pulse Width	24			20			ns		
t_W	$\overline{PL}$ Pulse Width	18			18			ns	Fig. 3	
t_W	$\overline{MR}$ Pulse Width	12			12			ns	Fig. 4	
t_sL	Set-up Time LOW Data to $\overline{PL}$	12			12			ns	Fig. 5	
t_hL	Hold Time LOW Data to $\overline{PL}$	6.0			6.0			ns		
t_sH	Set-up Time HIGH Data to $\overline{PL}$	8.0			8.0			ns		
t_hH	Hold Time HIGH Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}$	16			16			ns	Fig. 4	
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	18			18			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

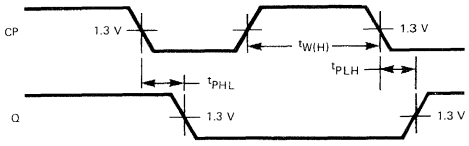
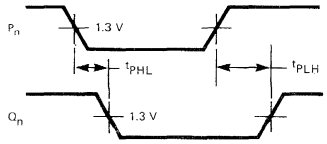


Fig. 1



NOTE: $\overline{PL}$ = LOW

Fig. 2

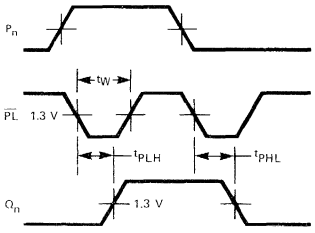


Fig. 3

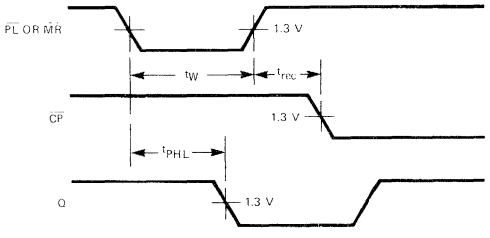
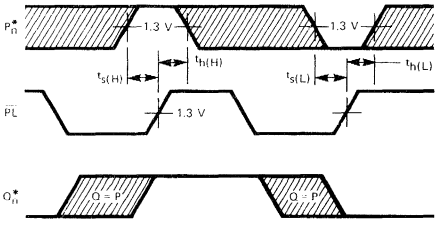


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

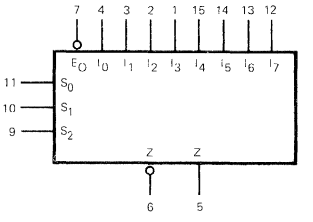
9LS251 (54LS/74LS251)

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The TTL/MSI 9LS251 (54LS251/74LS251) is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 9LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

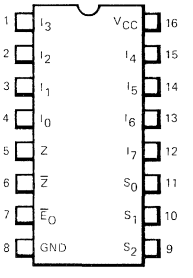
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



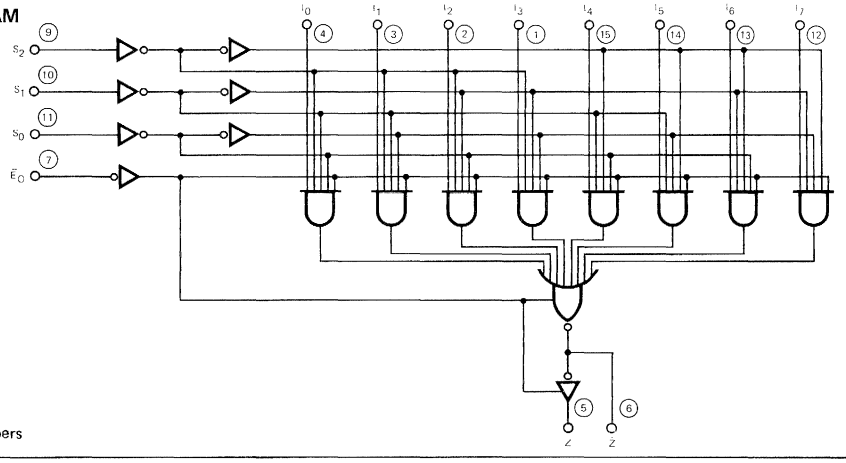
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The 9LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{E}_O$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E}_O \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

$\overline{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS251XM/54LS251XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS251XC/74LS251XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW			6.1	10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs Off			7.1	12	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 33	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	45 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	27 23	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		12	20	ns	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		17	25	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		12	20	ns	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		17	25	ns	Figs. 4, 5	

5

3-STATE AC WAVEFORMS

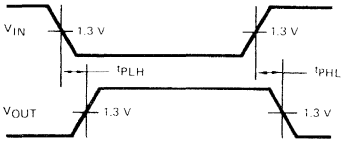


Fig. 1

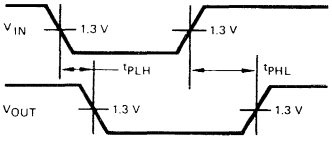


Fig. 2

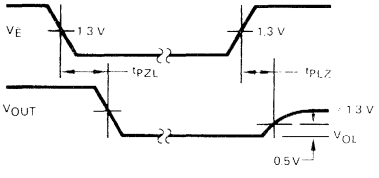


Fig. 3

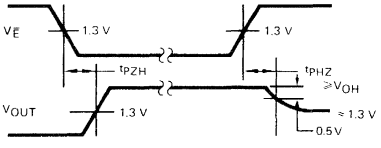
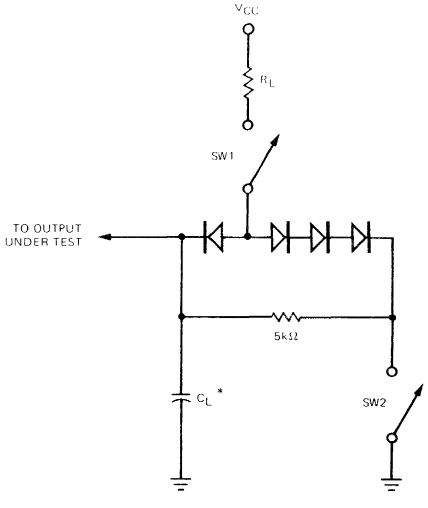


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

9LS253 (54LS/74LS253)

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

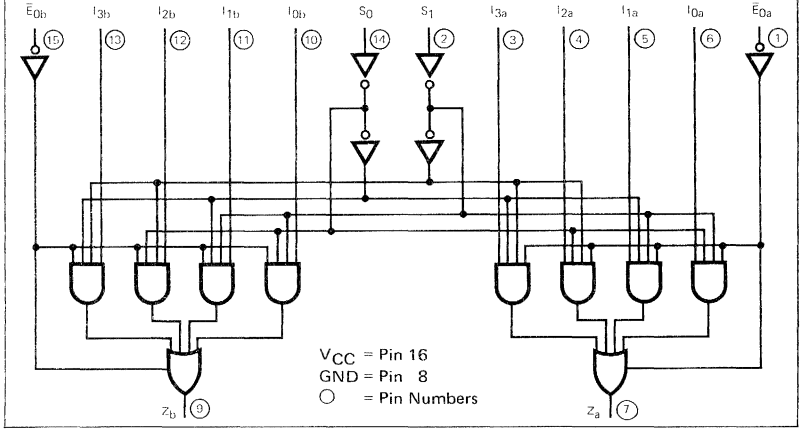
DESCRIPTION — The LSTTL/MSI 9LS253 (54LS/74LS253) is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

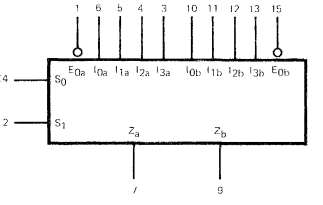
PIN NAMES		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC DIAGRAM

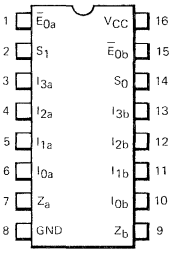


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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FUNCTIONAL DESCRIPTION — The 9LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The 9LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS253XM/54LS253XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS253XC/74LS253XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	29 24	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF, R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	18	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	32	ns	Figs. 3, 5	C_L = 5 pF, R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	18	ns	Figs. 4, 5	

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9LS257 (54LS/74LS257)

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The LSTTL/MSI 9LS257 (54LS/75LS257) is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

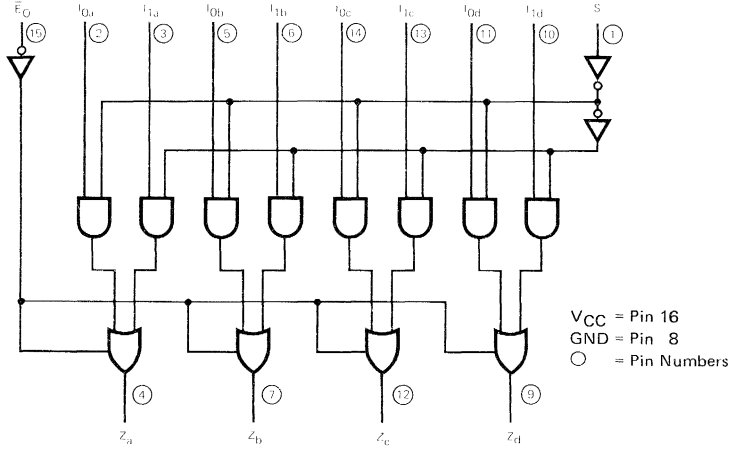
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

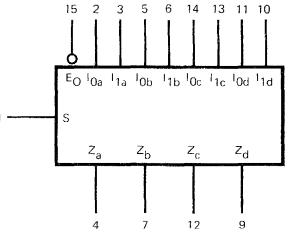
		LOADING (Note a) HIGH	LOW
S	Common Data Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM

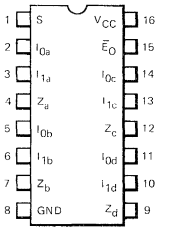


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS257 is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form.

The 9LS257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS257XM/54LS257XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS257XC/74LS257XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	S				40			
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
	S				0.2			
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	S				−0.8			
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				16		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				17		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 14	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level			28	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			24	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			22	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			14	ns	Figs. 4, 5	R_L = 2 kΩ

9LS258 (54LS/74LS258)

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The LSTTL/MSI 9LS258 (54LS/75LS258) is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

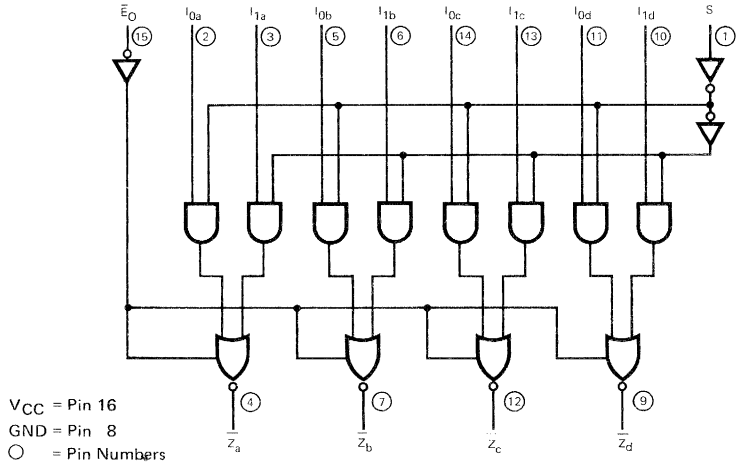
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

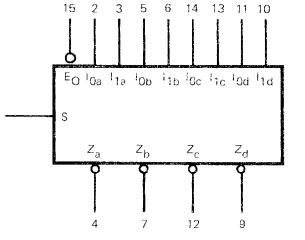
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



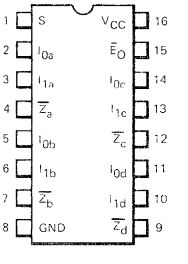
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 9LS258 is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select Input (S). When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in inverted form.

The 9LS258 Quad 2-Input Multiplexer is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad \overline{Z}_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad \overline{Z}_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS258XM/54LS258XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS258XC/74LS258XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	S				40		
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	S				0.2		
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	S				−0.8		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs HIGH				9.0	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs LOW				11	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs OFF				12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level			30	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			16	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			16	ns	Figs. 4, 5	R_L = 2 kΩ

9LS259 (54LS/74LS259)

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The 9LS259 (54LS/74LS259) is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latches.

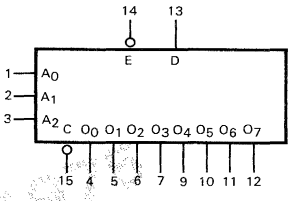
- **SERIAL-TO-PARALLEL CONVERSION**
- **8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL COMPATIBLE**

PRELIMINARY

PIN NAMES

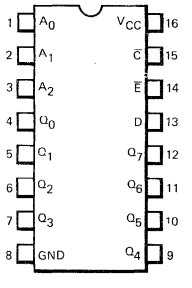
A_0, A_1, A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable (Active LOW) Input
$\overline{C}$	Clear (Active LOW) Input
Q_0 to Q_7	Parallel Latch Outputs

LOGIC SYMBOL

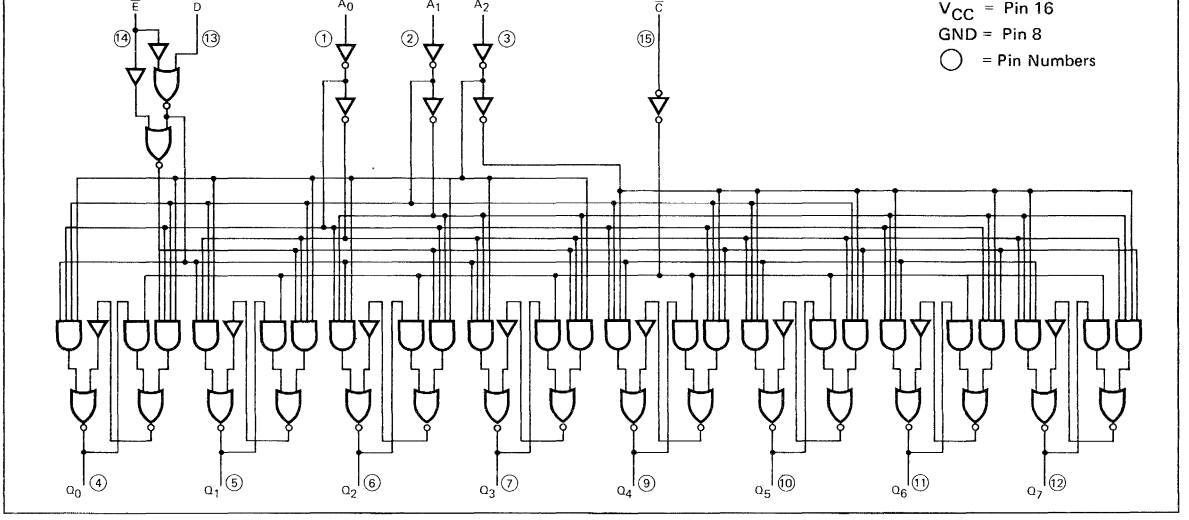


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

9LS283 (54LS/74LS283)

4-BIT BINARY FULL ADDER WITH FAST CARRY

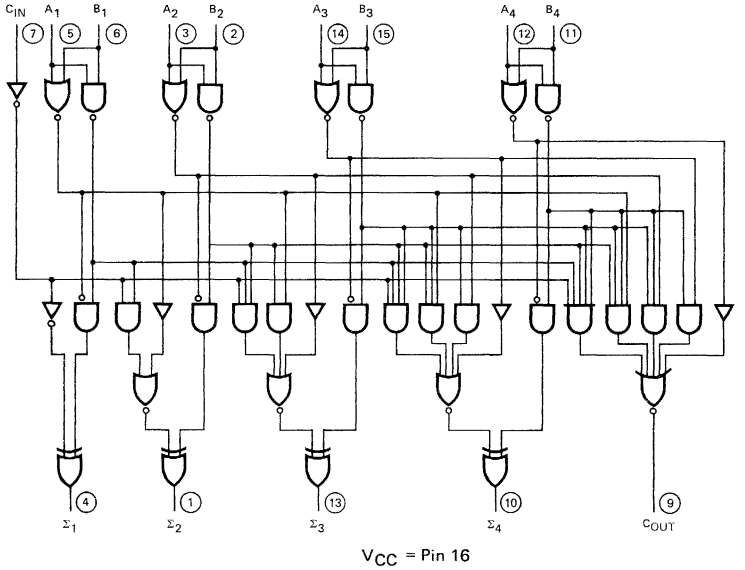
DESCRIPTION — The 9LS283 (54LS/74LS283) is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The 9LS283 operates with either active HIGH or active LOW operands (positive or negative logic). The 9LS283 (54LS/74LS283) is identical in function with 7483A and features corner power pins.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

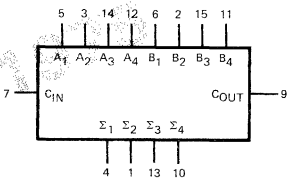
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



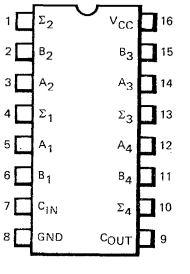
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 9LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the 9LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarity assigned to pins 7, 5 or 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS283XM/54LS283XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
9LS283XC/74LS283XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs = 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

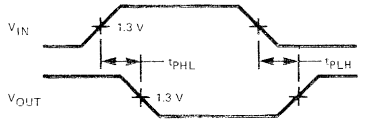


Fig. 1

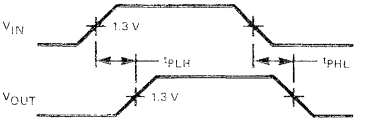


Fig. 2

9LS290 (54LS/74LS290)

DECADE COUNTER

9LS293 (54LS/74LS293)

4-BIT BINARY COUNTER

DESCRIPTION — The 9LS290 (54LS/74LS290) and 9LS293 (54LS/74LS293) are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (9LS290) or divide-by-eight (9LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the 9LS290 also has a 2-input gated Master Set (Preset 9).

- **CORNER POWER PIN VERSIONS OF THE 9LS90 and 9LS93.**
- **LOW POWER CONSUMPTION . . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . . BCD, BI-QUINARY, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷ 2 Section.	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 5 Section (9LS290).	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 8 Section (9LS293).	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, 9LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

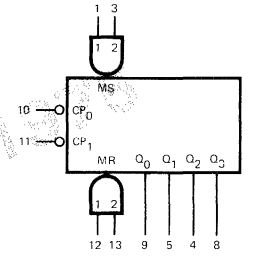
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

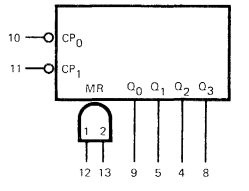
LOGIC SYMBOL

9LS290



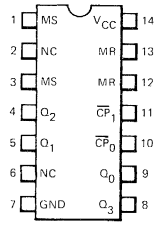
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

9LS293



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

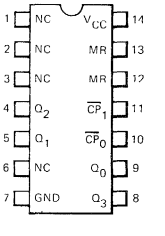
CONNECTION DIAGRAM **9LS290**
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC — No Internal Connection

CONNECTION DIAGRAM **9LS293**
DIP (TOP VIEW)

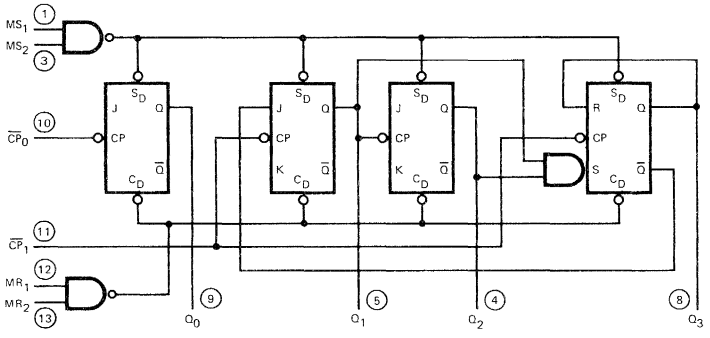


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

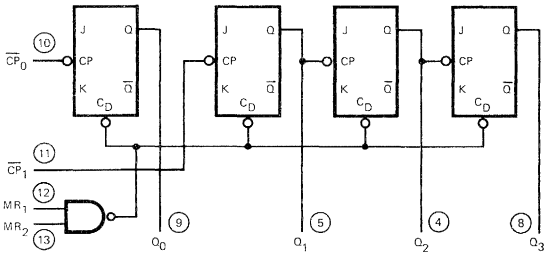
NC — No internal connection

LOGIC DIAGRAMS

9LS290



9LS293



FUNCTIONAL DESCRIPTION — The 9LS290 and 9LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (9LS290) or divide-by-eight (9LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the 9LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

9LS290

A. BCD Decade (8421) Counter — the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

9LS293

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

9LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

9LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

9LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

9LS293
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
9LS290XM/54LS290XM 9LS293XM/54LS293XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS290XC/74LS290XC 9LS293XC/74LS293XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current MS, MR				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_0$				120		
	$\overline{CP}_1$ (LS290)				80		
	$\overline{CP}_1$ (LS293)				40		
	MS, MR				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_0$, $\overline{CP}_1$ (LS293)				0.4		
	$\overline{CP}_1$ (LS290)				0.8		
I_{IL}	Input LOW Current MS, MR				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_0$				−2.4		
	$\overline{CP}_1$ (LS290)				−3.2		
	$\overline{CP}_1$ (LS293)				−1.6		
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 9LS290 MIN	LIMITS 9LS290 MAX	LIMITS 9LS283 MIN	LIMITS 9LS283 MAX	UNITS	TEST CONDITIONS	
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		MHz	Fig. 1	
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		32 35	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		51 51	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		70 70	ns		
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30			ns	Fig. 3	
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40			ns	Fig. 2	
t_{PHL}	MR Input to Any Output		40		40	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 9LS290 MIN	LIMITS 9LS290 MAX	LIMITS 9LS293 MIN	LIMITS 9LS293 MAX	UNITS	TEST CONDITIONS	
t_W	$\overline{CP}_0$ Pulse Width	15		15		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	30		30		ns		
t_W	MS Pulse Width	15				ns	Fig. 2, 3	
t_W	MR Pulse Width	15		15		ns	Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25				ns	Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		ns	Fig. 2	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

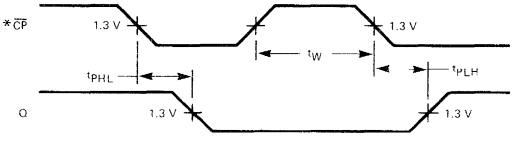


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

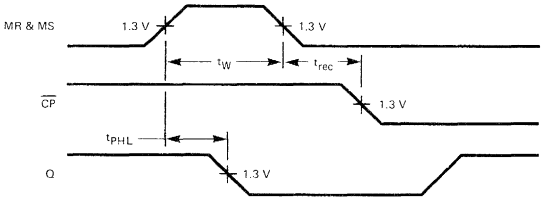


Fig. 2

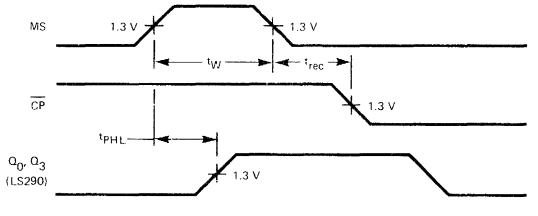


Fig. 3

9LS295 (54LS/74LS295A)

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

DESCRIPTION — The 9LS295 (54LS/74LS295A) is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The 9LS295 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

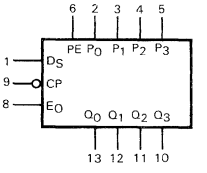
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Input	0.5 U.L.	0.25 U.L.
E_O	Output Enable Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Pulse (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	3-State Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

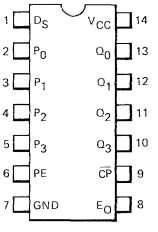
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



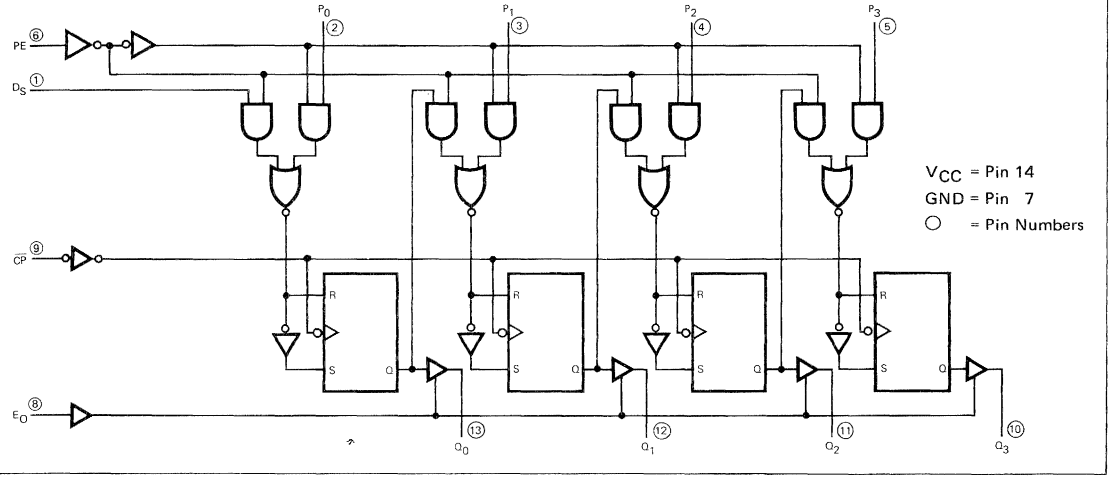
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 9LS295 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data ($P_0 - P_3$) inputs and four parallel 3-State output buffers ($Q_0 - Q_3$). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs ($P_0 - P_3$) into the register synchronous with the HIGH to LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (E_O). When the E_O is HIGH, the four register outputs appear at the $Q_0 - Q_3$ outputs. When E_O is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e., the input transitions on the E_O input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐	l	X	L	q_0	q_1	q_2
	l	⌐	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

L = LOW Voltage Levels
H = HIGH Voltage Levels
X = Don't Care

$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS295XM/54LS295AXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS295XC/74LS295AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.4			I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Output Off Current LOW				20	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs HIGH			14	23	mA	V_{CC} = MAX, V_{CP} = ⎍, V_E = 4.5 V
	Power Supply Current, Outputs Off			15	25	mA	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Propagation Delay, Clock to Output		17	26	ns	Fig. 1	
t_{PHL}			17	26			

AC CHARACTERISTICS: for 3-State Output Buffers (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		12	18	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		12	18	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		12	18	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	20			ns	Fig. 1	
t_s(Data)	Set-up Time, Data to Clock	20			ns	Fig. 1	V_{CC} = 5.0 V
t_h(Data)	Hold Time, Data to Clock	0			ns		C_L = 15 pF
t_s(PE)	Set-up Time, PE to Clock	20			ns	Fig. 2	
t_h(PE)	Hold Time, PE to Clock	0			ns		

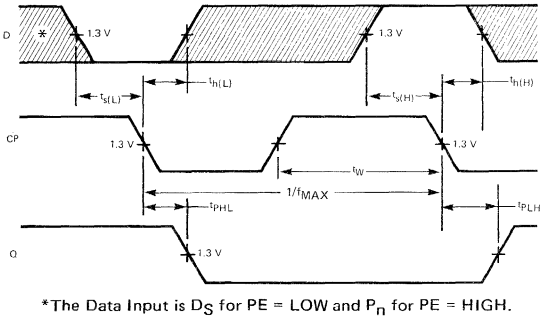
DEFINITION OF TERMS

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1

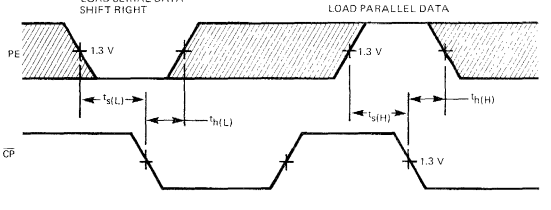


Fig. 2

9LS298 (54LS/74LS298)

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION — The 9LS298 (54LS/74LS298) is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The 9LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Fairchild TTL families.

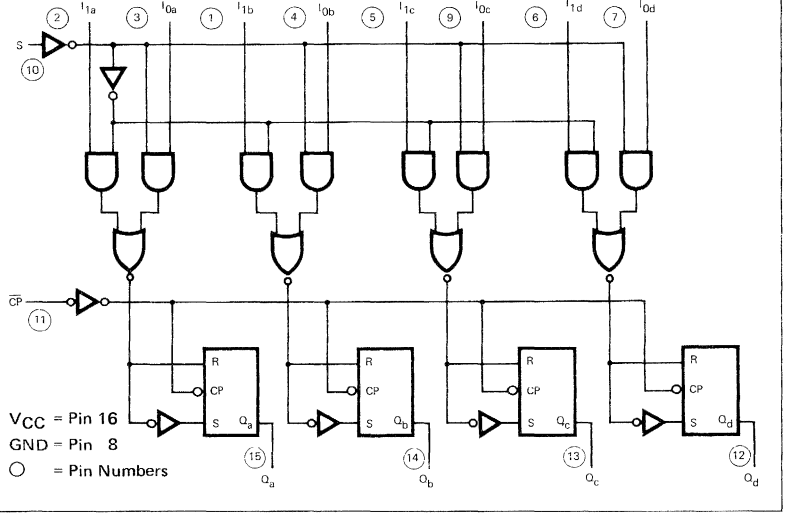
- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

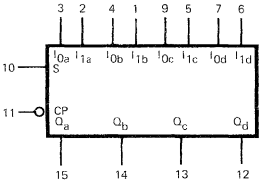
		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
$Q_a - Q_d$	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC OR BLOCK DIAGRAM

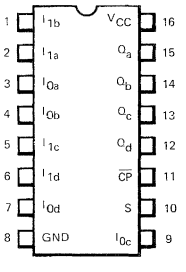


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — The 9LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS298XM/54LS298XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS298XC/74LS298XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		16 16	25 25	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20			ns	Fig. 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clock Pulse Width (LOW)	20			ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	15			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	5.0			ns		
$t_{s(S)}$	Set-up Time, Select to Clock	20			ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0			ns		

5

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

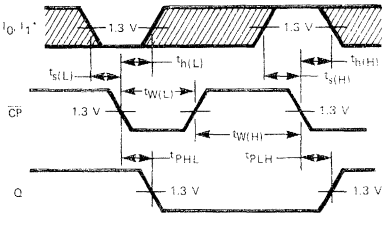


Fig. 1

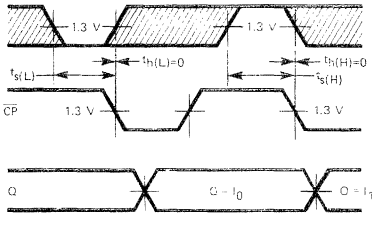


Fig. 2

*The shaded areas indicate when the input is permitted to change for predictable output performance.

9LS670 (54LS/74LS670)

4×4 REGISTER FILE WITH 3-STATE OUTPUTS

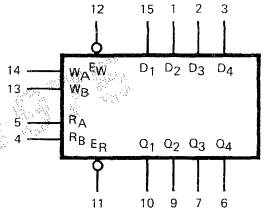
DESCRIPTION — The TTL/MSI 9LS670 (54LS/74LS670) is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The 9LS170 (54LS/74LS170) provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

LOGIC SYMBOL



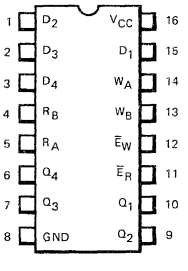
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.5 U.L.	0.75 U.L.
Q_1-Q_4	Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

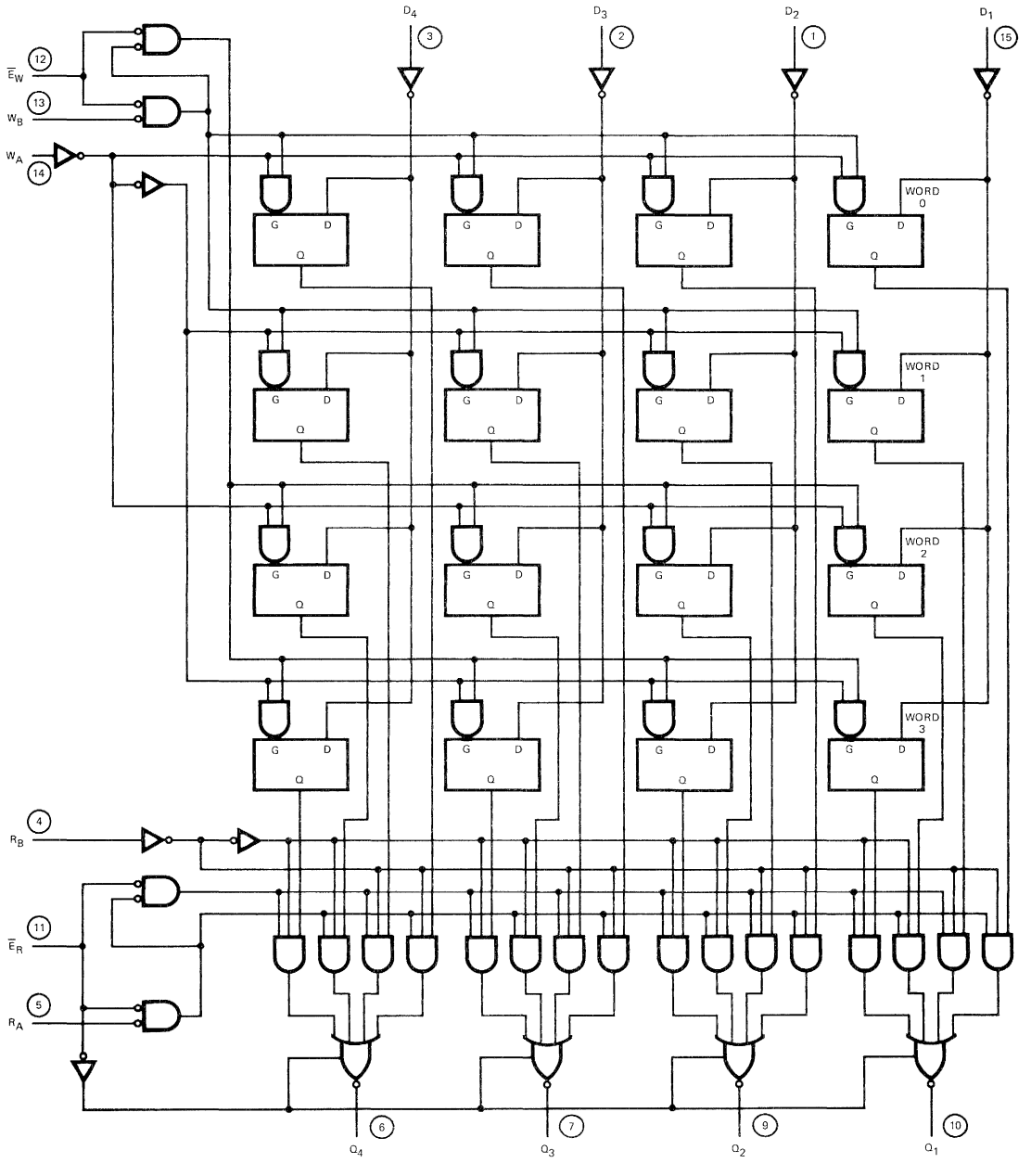
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5.0 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
9LS670XM/54LS670XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
9LS670XC/74LS670XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, V_{IH} = 2 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_{IH} = 2 V
I_{IH}	Input HIGH Current Any D, R or W				20	μA	V_{CC} = MAX, V_{IN} 2.7 V
	$\overline{E}_W$				40	μA	V_{CC} = MAX, V_{IN} 2.7 V
	$\overline{E}_R$				60	μA	V_{CC} = MAX, V_{IN} 2.7 V
	Any D, R or W				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}_W$				0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}_R$				0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Any D, R or W				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}_W$				−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}_R$				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			30	50	mA	V_{CC} = MAX (Note 6)

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay R_A or R_B to Q Outputs			40 45	ns	Fig. 2	$V_{CC} = 5$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs			45 50	ns	Fig. 1	$R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 40	ns	Fig. 1	
t_{PZH}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going HIGH			35	ns	Fig. 4,5	$V_{CC} = 5$ V $C_L = 5.0$ pF $R_L = 2$ kΩ See Page 5-98 for 3-state Waveforms (Figs. 3,4,5)
t_{PZL}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going LOW			40	ns	Fig. 3,5	
t_{PHZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from HIGH			50	ns	Fig. 4,5	
t_{PLZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from LOW			35	ns	Fig. 3,5	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 6 (Note 10)
t_sD (Note 7)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 9)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:
7. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
8. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
9. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
10. The shaded areas indicate when the input are permitted to change for predictable output performance.

AC WAVEFORMS

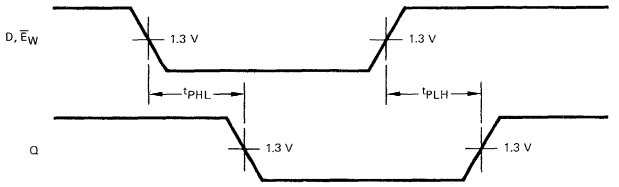


Fig. 1

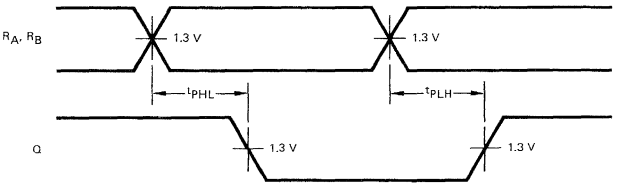


Fig. 2

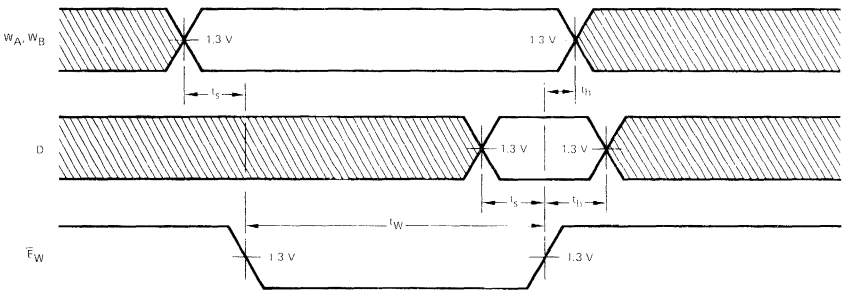


Fig. 6

LPTTL/MONOSTABLE 96L02

LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 96L02 is a low power Dual Retriggerable, Resettable Monostable Multivibrator which provides andoutput pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

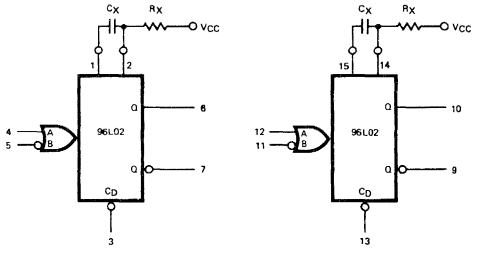
- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100 % DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE-TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

PIN NAMES

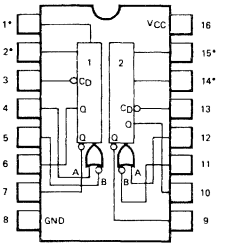
		LOADING HIGH	LOADING LOW
B	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
C_D	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
$\overline{Q}$	Output (Active LOW)	9.0	3.0

1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

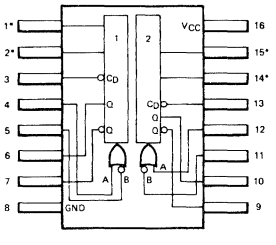


CONNECTION DIAGRAM
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)



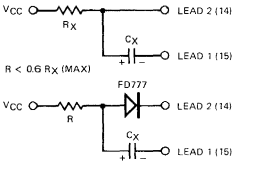
*Pins for ecternal timing.

5

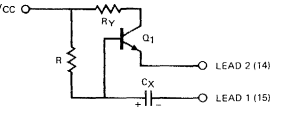
FUNCTIONAL DESCRIPTION – The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset lead to a logic LOW. Active pull ups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active LOW input or the Q output to the active HIGH input.

OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Symbol.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for −55 to 125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:
$$t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right] \text{ (for } C_X > 10^3 \text{ pF)}$$
Where R_X is in kΩ, C_X is in pF, t is in ns, for $C_X < 10^3$ pF, see Fig. 1
5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 μA, and the inverse capacitor leakage at 1.0 V is less than 1.6 μA over the operational temperature range and Rule 3 above is satisfied.



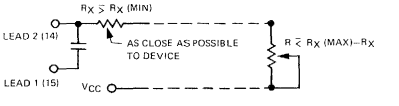
   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.
$$t \approx 0.3\, RC_X$$
   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



$R < R_X\,(0.7)\,(h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
R_X (min) $< R_Y < R_X$ (max)

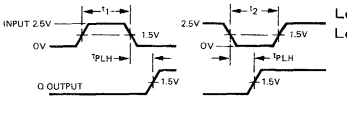
Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962
$$t \approx 0.3\, RC_X$$
This configuration is not recommended with retriggerable operation.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

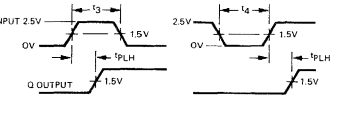


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pick up.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

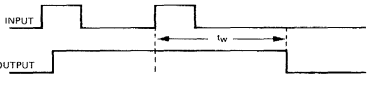
Input to Lead 5 (11)
Lead 4 (12) = LOW
Lead 3 (13) = HIGH
t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
t_2, t_4 = Min. Negative Input Pulse Width > 60 ns



Input to Lead 4 (12)
Lead 5 (11) = HIGH
Lead 3 (13) = HIGH

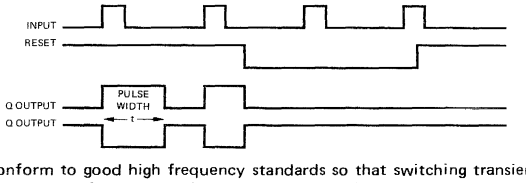


9. The retriggerable pulse width is calculated as shown below:
$$tw = t + t_{PLH} = 0.33\, R_X C_X \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation – An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC}
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
96L02XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip.

5

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 4)	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	V	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	V	V_{CC} = MIN, I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.3 V
I_{SC} I_{OS}	Output Short Circuit Current (Note 5)	−2.0		−13	mA	V_{CC} = MAX, V_{OUT} = 1.0 V
I_{CC}	Supply Current		10	16	mA	V_{CC} = MAX

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
96L02XM						
t_{PLH}	Turn Off Delay, Negative Trigger Input to True Output		55	75	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Turn On Delay, Negative Trigger Input to Complement Output		45	62	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	μs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	$R_X = 39$ kΩ, $C_X = 1000$ pF
96L02XC						
t_{PLH}	Turn Off Delay, Negative Trigger Input to True Output		55	80	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Turn On Delay, Negative Trigger Input to Complement Output		45	65	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	μs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	$R_X = 39$ kΩ, $C_X = 1000$ pF

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X ($C_X \leq 1000$ pF)
(FOR $C_X > 1000$ pF SEE OPERATION RULES 4 AND 5.)

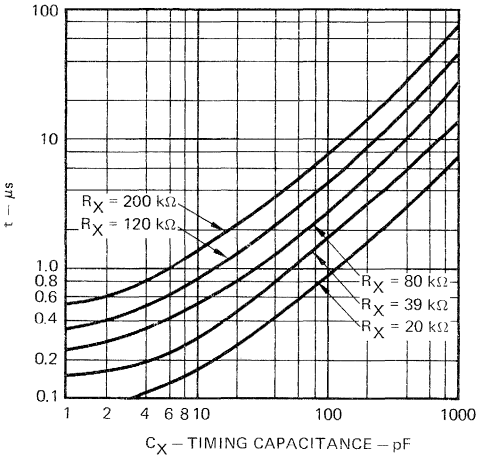
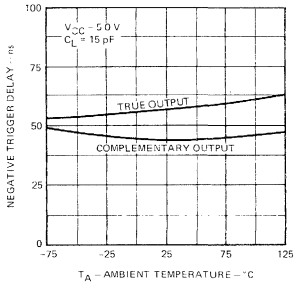


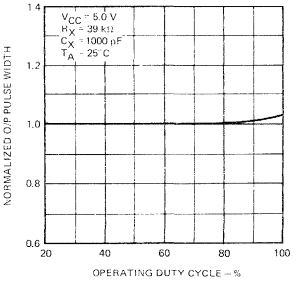
Fig. 1

TYPICAL PULSE CHARACTERISTICS

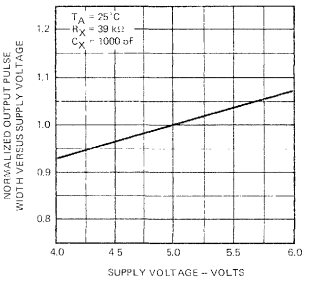
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



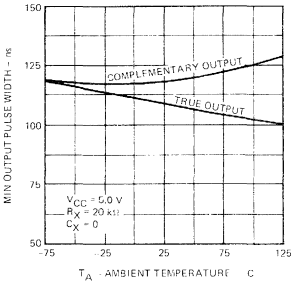
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



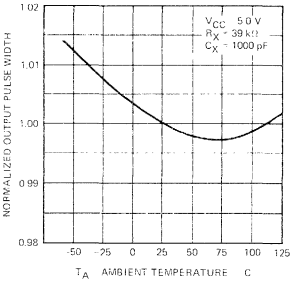
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MIN. OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



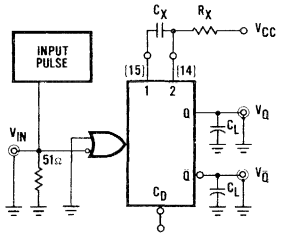
5

TRIGGERING TRUTH TABLE

LEAD NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

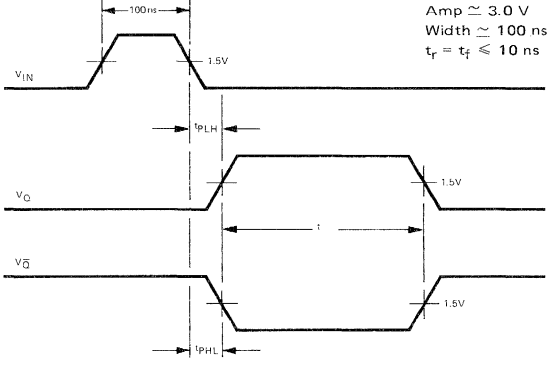
L = LOW Voltage Level
H = HIGH Voltage Level
L → H = LOW to HIGH Voltage Level Transition
H → L = HIGH to LOW Voltage Level Transition
X = Don't Care

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = 16
GND = 8

INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leqslant 10$ ns



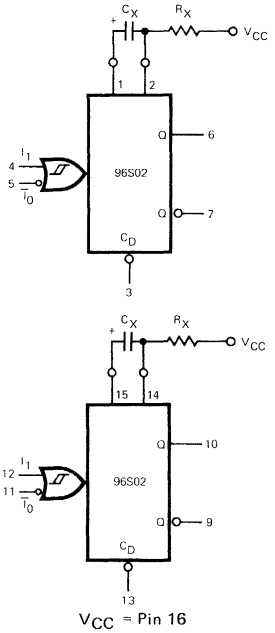
96S02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION– The 96S02 is a Dual Retriggerable and Resettable Monostable which uses Schottky technology to provide wide delay range, stability, prediction accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. The 96S02 may utilize timing resistors to 2 MΩ thus reducing required capacitor values. Hysteresis is provided on the positive-going inputs for increased noise immunity. The 96S02 is fully compatible with all TTL families.

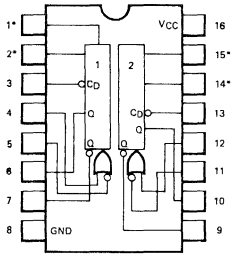
- REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS
- BROAD TIMING RESISTOR RANGE – 1.5 kΩ to 2 MΩ
- OUTPUT PULSE WIDTH IS VARIABLE OVER A 1300:1 RANGE BY RESISTOR CONTROL
- PROPAGATION DELAY OF 12 ns
- OUTPUT PULSE WIDTH STABILITY OF ±0.2% OVER 0°C TO 75°C TEMPERATURE RANGE
- OUTPUT PULSE WIDTH STABILITY OF ±0.3% OVER 4.75 V TO 5.25 V POWER SUPPLY RANGE
- PULSE WIDTH VARIATION OF ±5% FROM UNIT TO UNIT
- 0.3 V HYSTERESIS ON POSITIVE TRIGGER INPUT
- OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE
- 27 ns TO ∞ OUTPUT PULSE WIDTH RANGE
- RESETTABLE IN 9 ns
- SAME PINOUT AS 9602, 96L02

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



*Pins for external timing.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{I}_0$	Trigger (Active LOW) Input	0.5 U.L.	0.625 U.L
I_1	Schmitt Trigger (Active HIGH) Input	0.5 U.L.	0.625 U.L.
$\overline{C}_D$	Clear (Active LOW) Input	0.5 U.L.	0.625 U.L.
Q	Pulse (Active HIGH) Output	25 U.L.	12.5 U.L.
$\overline{Q}$	Pulse (Active LOW) Output	25 U.L.	12.5 U.L.

NOTE:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.

FUNCTIONAL DESCRIPTION – The 96S02 Schottky Dual Retriggerable Resettable Monostable Multivibrator has two dc coupled trigger inputs per function, one active LOW ($\overline{I_0}$) and one active HIGH (I_1). The I_1 input utilizes an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either leading or trailing edge-triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the 96S02 and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I_0}$ or the Q output to I_1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from init to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families. High impedance inputs minimize loading and provide compatibility with low power families such as 9LS/74LS.

OPERATION RULES

TIMING

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.5 kΩ to 2 MΩ.

2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.

3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (–) terminal to pin 2 (14) and R_X. Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle; however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to 2 (14) depending on values of R_X and V_{CC}. For values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVDC or higher should be used when $R_X \geq 10$ kΩ.

4. The output pulse width t_W for $R_X \geq 10$ kΩ and $C_X \geq 100$ pF is determined as follows:

$$\boxed{t_W = 0.5\ R_X C_X}$$

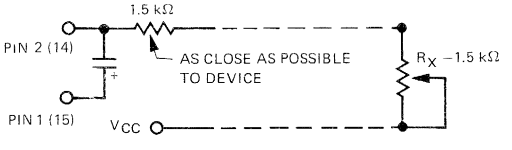
Where R_X is in kΩ, C_X is in pF, t is in ns

OR

R_X is in kΩ, C_X is in μF, t is in ms

5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

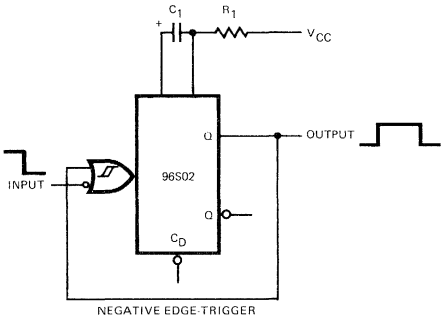


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

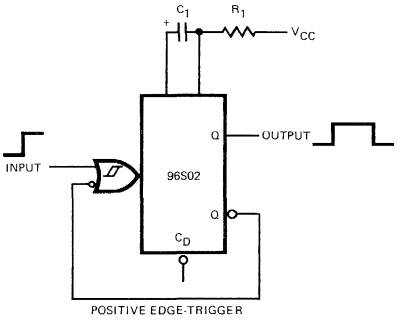
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and ground located near the 96S02 is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I}_0$ is 8 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



NEGATIVE EDGE-TRIGGER



POSITIVE EDGE-TRIGGER

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW to HIGH transition on C_D will *not* trigger the 96S02.

TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	PIN NO'S. 4(12)	PIN NO'S. 3(13)	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Don't Care (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	96S02XC MIN	96S02XC TYP	96S02XC MAX	UNITS
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Operating Free-Air Temperature Range	0	25	75	C
Input Loading for Each Input			0.625	U.L.
Fan-out	12.5			U.L.

X = package type; D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage Except Pins 4 & 12	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage Except Pins 4 & 12			0.8	V	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		−0.65	−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{T+}	Positive-Going Threshold Voltage, Pins 4 & 12		1.7	2.0	V	V_{CC} = 5.0 V, T_A = 25°C
V_{T-}	Negative-Going Threshold Voltage, Pins 4 & 12	0.8	1.4		V	V_{CC} = 5.0 V, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.7	3.2		V	V_{CC} = MIN, I_{OH} = −1.0 mA, V_{IN} = 0.8 V
V_{OL}	Output LOW Voltage		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}
I_{IH}	Input HIGH Current		0.2	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
				0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.6	−1.0	mA	V_{CC} = MAX, V_{IN} = 0.5 V
V_{CX}	Capacitor Voltage, Pin 1 (15) Referenced to Pin 2 (14)	−0.85		3.0	V	R_X = 1.5 kΩ; V_{CC} = 4.75 V to 5.25 V
		−0.5		3.0	V	$R_X \geq$ 10 kΩ; V_{CC} = 4.75 V to 5.25 V
		−0.4		3.0	V	$R_X \geq$ 1 MΩ; V_{CC} = 4.75 V to 5.25 V
I_{OS}	Output Short Circuit Current (Note 3)	−40	−65	−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Quiescent Power Supply Drain		48	70	mA	Inputs Open

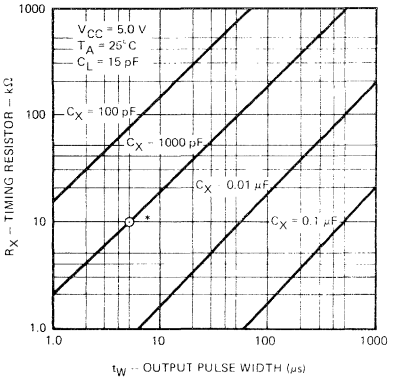
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH}	Negative Trigger Input to True Output		10	15	ns	
t_{PHL}	Negative Trigger Input to Complement Output		12	19	ns	
t_{PLH}	Positive Trigger Input to True Output		12	19	ns	
t_{PHL}	Positive Trigger Input to Complement Output		15	20	ns	
t_{PHL}	Clear Input to True Output		6.5	10	ns	
t_{PLH}	Clear Input to Complement Output		9.0	14	ns	
$t_{W(MIN)}$	Min. Negative Trigger Pulse Width on $\overline{I_0}$		3.0	8.0	ns	
$t_{W(MIN)}$	Min. Positive Trigger Pulse Width on I_1		7.0	12	ns	
$t_{W(MIN)}$	Min. Clear Pulse Width		3.0	7.0	ns	
$t_{W(MIN)}$	Min. True Output Pulse Width	22	27	35	ns	R_X = 1.5 kΩ, C_X = stray capacity only
$t_{W(MIN)}$	Min. True Output Pulse Width	30	38	45	ns	R_X = 1.5 kΩ, C_X = 10 pF including stray and jig capacitance
t_W	True Output Pulse Width	4.9	5.2	5.5	μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	1.5		2000	kΩ	T_A = 0°C to 75°C, V_{CC} = 4.75 V to 5.25 V
Δt	Max. Change in True Output Pulse Width over Temperature Range		0.38	1.0	%	T_A = 0°C to 75°C, V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
Δt	Max. Change in True Output Pulse Width over V_{CC} Range		0.38	1.0	%	T_A = 25°C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF

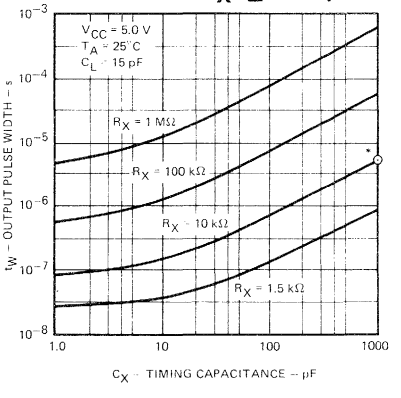
TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR (R_X) AND TIMING CAPACITOR (C_X)



*Guaranteed Limits are 4.9 μs to 5.5 μs.

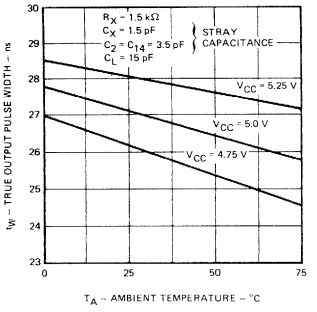
OUTPUT PULSE WIDTH VERSUS TIMING CAPACITANCE FOR LOW VALUES OF C_X (≤ 1000 pF)



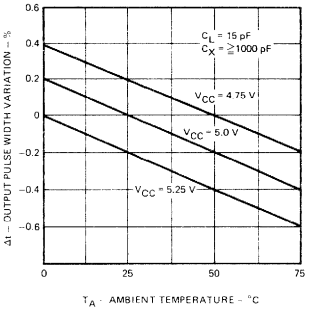
*Guaranteed Limits are 4.9 μs to 5.5 μs.

TYPICAL CHARACTERISTICS (Cont'd)

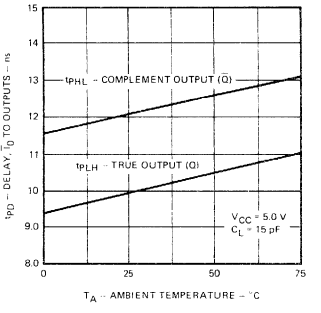
MINIMUM OUTPUT PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE (NO EXTERNAL TIMING CAPACITOR)



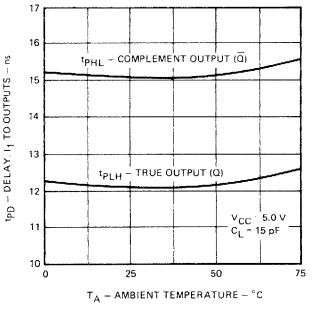
NORMALIZED OUTPUT PULSE WIDTH VARIATION VERSUS AMBIENT TEMPERATURE



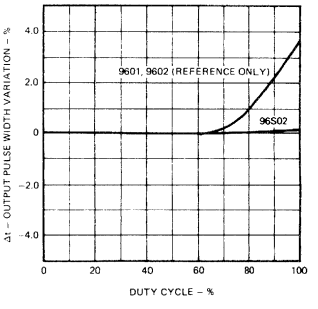
DELAY FROM NEGATIVE TRIGGER INPUT $\overline{I}_0$ TO OUTPUTS VERSUS AMBIENT TEMPERATURE



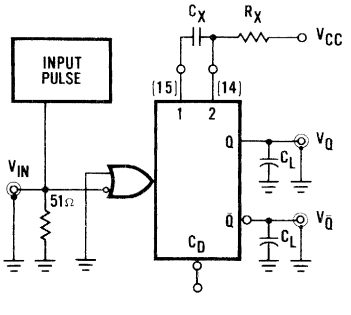
DELAY FROM POSITIVE TRIGGER INPUT I_1 TO OUTPUTS VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VARIATION VERSUS DUTY CYCLE

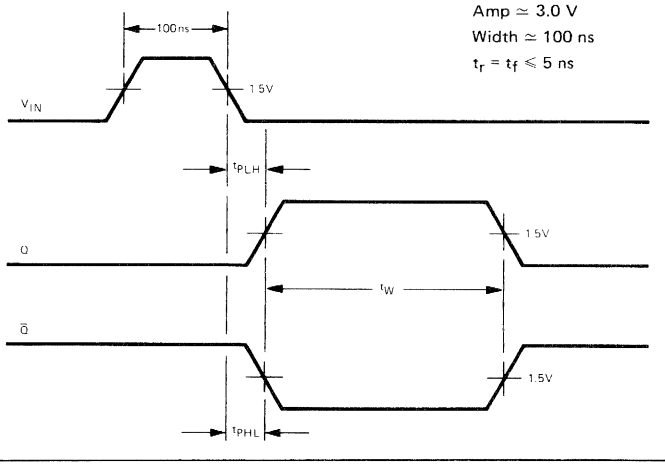


AC CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leqslant 5$ ns



LOW POWER SCHOTTKY AND MACROLOGIC™ TTL

9400 MACROLOGIC™ TTL SERIES

GENERAL DESCRIPTION – Fairchild 9400 MACROLOGIC TTL Series utilizes advanced Schottky technology to provide high performance peripheral and processor oriented LSI. The design of 9400 ensures maximum design flexibility with no performance loss. The MACROLOGIC TTL elements may be used with any bit length, instruction set or organization. Devices may be expanded with little or no extra components. Where applicable, bus oriented, 3-state outputs are provided. A new slim 24-pin package reduces PC board real estate by a third.

- 150–250 GATE COMPLEXITY
- COMPATIBLE WITH ALL TTL FAMILIES
- PERFORMANCE EQUIVALENT TO SCHOTTKY IMPLEMENTATION
- 14, 18 AND SLIM 24-PIN PACKAGES
- INPUTS ABOUT 1/4 NORMAL TTL LOAD, i.e., 360–400 μA
- OUTPUTS DRIVE 16 mA (10U.L.) OR 8mA (5U.L.) DEPENDING ON APPLICATION
- DESIGNED FOR MAXIMUM FLEXIBILITY
- OPERATES OVER COMMERCIAL OR MILITARY TEMPERATURE RANGE

ADVANCED SCHOTTKY PROCESS

The 9400 family uses an advanced Schottky TTL process to obtain the best speed/power product of any commercially available digital bipolar circuitry. Key characteristics are as follows:

- SHALLOW, LOW CAPACITANCE DIFFUSION TO PROVIDE TRANSISTOR f_T OF 2 GHz
- SCHOTTKY DIODES TO ELIMINATE STORAGE TIME
- INTERNAL GATES
  - –30 mils^2 (50 GATES PER mm^2)
  - –5 ns DELAY
  - –6.0 pJ DELAY POWER PRODUCT
- OUTPUT BUFFERS
  - –70 mils^2
  - –6 ns DELAY
  - –10 pJ DELAY POWER PRODUCT

9401

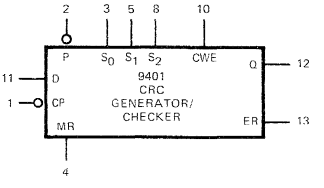
CRC GENERATOR/CHECKER

FAIRCHILD MACROLOGIC™ TTL

DESCRIPTION – The 9401 Cyclic Redundancy Check (CRC) Generator/Checker provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Individual clear and preset inputs are provided for floppy disc and other applications. The Error Output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is a member of Fairchild's MACROLOGIC TTL family and is fully compatible with all TTL families.

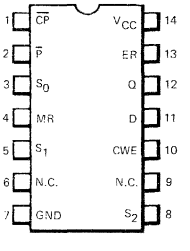
- **GUARANTEED 12 MHz DATA RATE**
- **EIGHT SELECTABLE POLYNOMIALS**
- **ERROR INDICATOR**
- **SEPARATE PRESET AND CLEAR CONTROLS**
- **AUTOMATIC RIGHT JUSTIFICATION**
- **FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES**
- **14-PIN PACKAGE**
- **TYPICAL APPLICATIONS:**
  - **FLOPPY AND OTHER DISC STORAGE SYSTEMS**
  - **DIGITAL CASSETTE AND CARTRIDGE SYSTEMS**
  - **DATA COMMUNICATION SYSTEMS**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

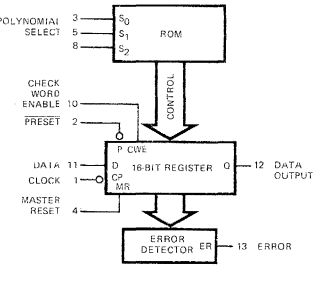
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{CC} = 14
GND = 7

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	0.5 U.L.	0.23 U.L.
$\overline{D}$	Data Input	0.5 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH to LOW Transition) Input	0.5 U.L.	0.23 U.L.
CWE	Check Word Enable Input	0.5 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	0.5 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FUNCTIONAL DESCRIPTION – The 9401 Cyclic Redundancy Check (CRC) Generator/Checker is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the HIGH to LOW transition of the Clock Input ($\overline{CP}$). This data is gated with the most significant Output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWE Input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH to LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH. ER remains valid until the next HIGH to LOW transition of $\overline{CP}$ or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the register. A LOW on the Preset Input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage	XM & XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70	110	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 2)	LIMITS MAX	UNITS	CONDITIONS	
f_{max}	Maximum Clock Frequency	12	20		MHz	Fig. 3, 4, 5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation Delay, Preset to Data Output		40	60	ns		
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR or Preset to Error Output		40	60	ns		

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
$t_w\overline{CP}$ (L)	Clock Pulse Width (LOW)	35			ns	Fig. 2	C_L = 15 pF
t_sD	Set-up Time, Data to Clock		35	55	ns	Fig. 6	
t_sCWE	Set-up Time, CWE to Clock		35	55	ns		
t_h	Hold Time, Data and CWE to Clock		0		ns		
t_wP (L)	Preset Pulse Width (LOW)	35	25		ns	Fig. 4	
t_wMR (H)	Master Reset Pulse Width (HIGH)	35	25		ns	Fig. 6	
t_{rec}	Recovery Time, MR and Preset to Clock		25	35	ns	Fig. 4, 5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

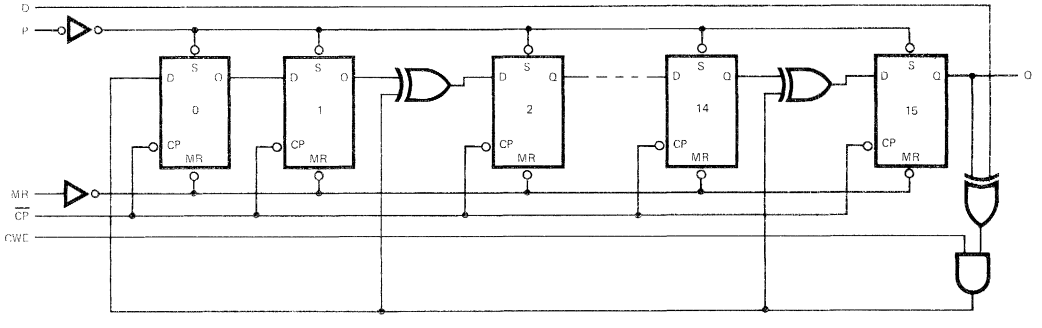
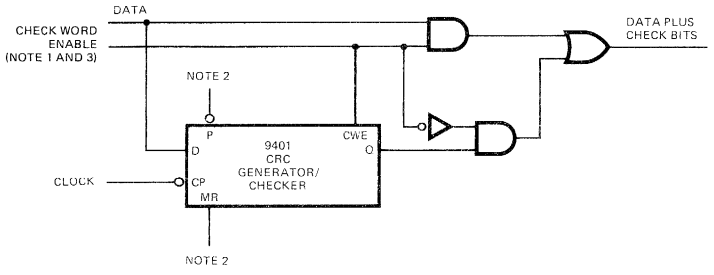


Fig. 1



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Fig. 2
CHECK WORD GENERATION

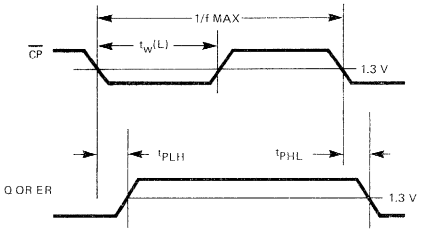


Fig. 3
PROPROPAGATION DELAYS, $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

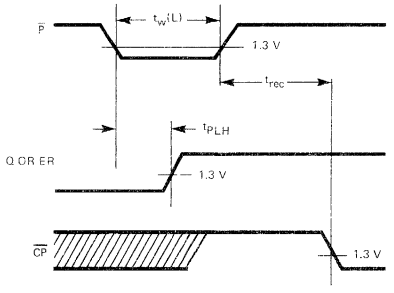


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME P TO $\overline{CP}$

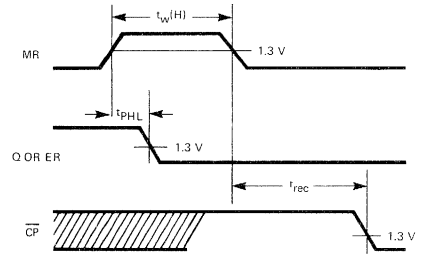


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

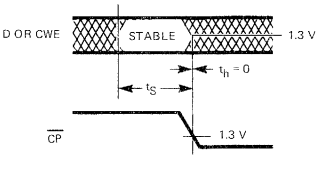


Fig. 6
SET-UP AND HOLD TIMES, D TO $\overline{CP}$ AND CWE TO $\overline{CP}$

9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

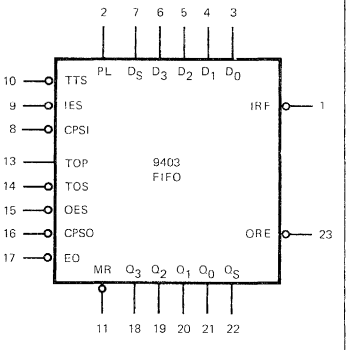
FAIRCHILD MACROLOGIC™ TTL

DESCRIPTION — The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of 4). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility. It is a member of Fairchild's TTL MACROLOGIC family and is fully compatible with all TTL families.

- **12 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **24-PIN PACKAGE**

LOGIC SYMBOL



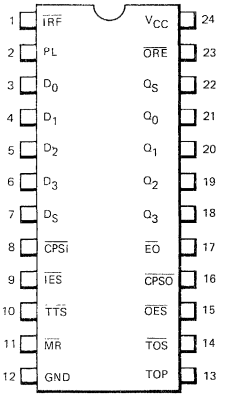
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Parallel Data Inputs	0.5 U.L.	0.23 U.L.
D_S	Serial Data Input	0.5 U.L.	0.23 U.L.
PL	Parallel Load Input	0.5 U.L.	0.23 U.L.
$\overline{CPSI}$	Serial Input Clock (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$\overline{IES}$	Serial Input Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{TTS}$	Transfer to Stack Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{OES}$	Serial Output Enable Input (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)	0.5 U.L.	0.23 U.L.
TOP	Transfer Out Parallel Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CPSO}$	Serial Output Clock Input (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$Q_0 - Q_3$	Parallel Data Outputs (Note b)	130 U.L.	10 U.L.
Q_S	Serial Data Output (Note b)	10 U.L.	10 U.L.
$\overline{IRF}$	Input Register Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{ORE}$	Output Register Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

6

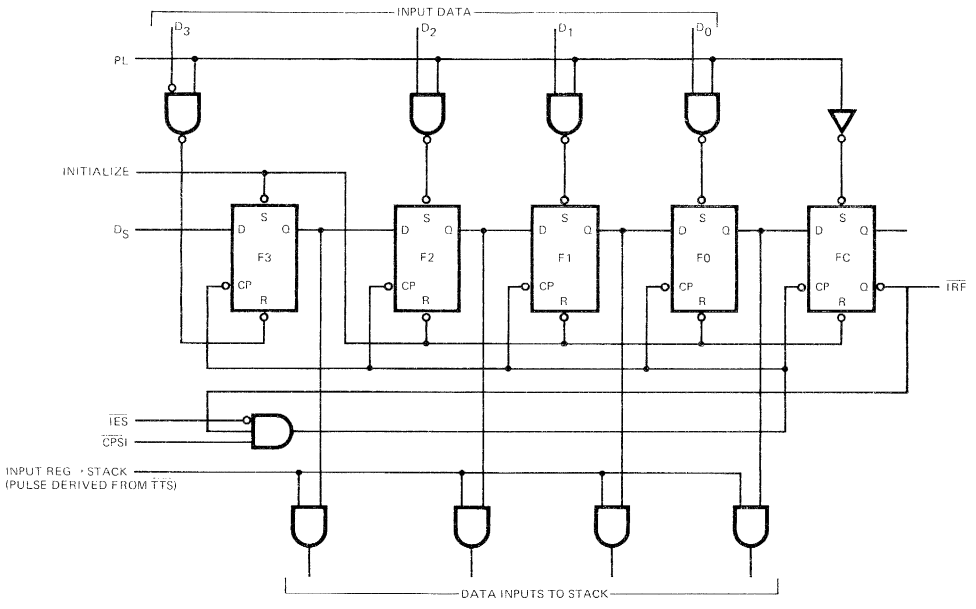


Fig. 1
CONCEPTUAL INPUT SECTION

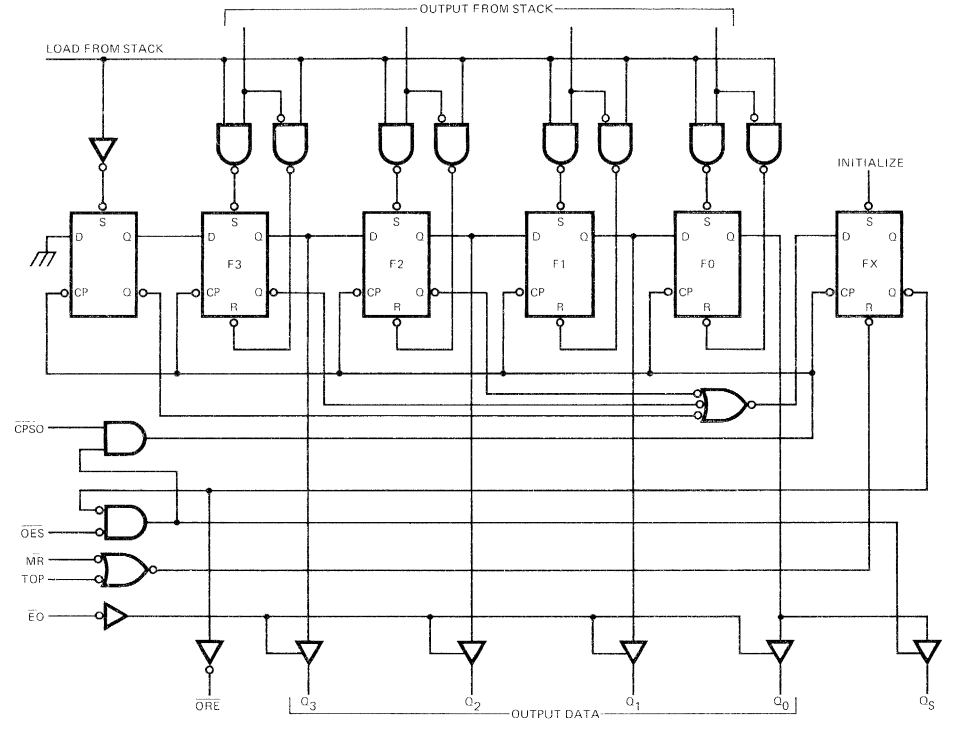
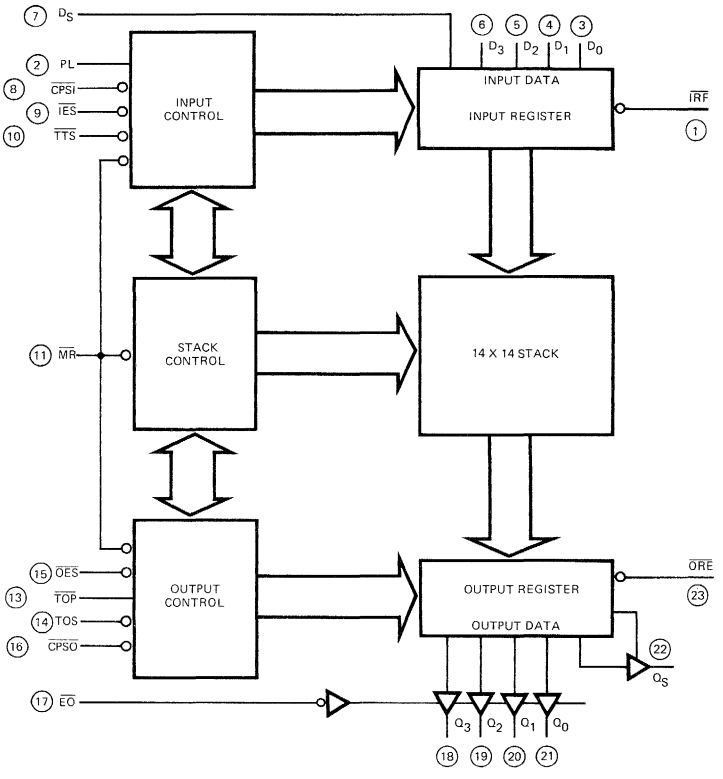


Fig. 2
CONCEPTUAL OUTPUT SECTION

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Numbers

FUNCTIONAL DESCRIPTION — As shown in the Block Diagram the 9403 consists of three parts:

1. An Input Register with Parallel and Serial Data Inputs as well as control inputs and outputs for input handshaking and expansion.

2. A 4-bit wide, 14-word deep Fall-Through Stack with self-contained control logic.

3. An Output Register with Parallel and Serial Data Outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):

The Input Register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the Fall-Through Stack and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 Flip-Flop and resetting the other flip-flops. The $\overline{Q}$ Output of the last Flip-Flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL Input loads the $D_0 - D_3$ Data Inputs into the F0 – F3 Flip-Flops and sets the FC Flip-Flop, which forces $\overline{IRF}$ LOW, indicating "Input Register Full". The D Inputs must be stable while PL is HIGH. During parallel entry, the $\overline{IES}$ Input should be LOW; the $\overline{CPSI}$ Input may be either HIGH or LOW.

SERIAL ENTRY:
Data on the DS Input is serially entered into the F3, F2, F1, F0, FC Shift Register on each HIGH-to-LOW transition of the $\overline{CPSI}$ Clock Input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC Flip-Flop is set, forcing $\overline{IRF}$ LOW (Input Register full) and internally inhibiting further $\overline{CPSI}$ clock pulses. Figure 3 illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B0 is the first bit, B63 the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of Flip-Flops F0 – F3 feed the Stack. A LOW level on the $\overline{TTS}$ Input attempts to initiate a "fall-through" action. If the top location of the Stack is empty, data is loaded into the Stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the Stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the Stack control section and does not clear the data.

OUTPUT REGISTER (DATA EXTRACTION):
The Output Register receives 4-bit data words from the bottom Stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

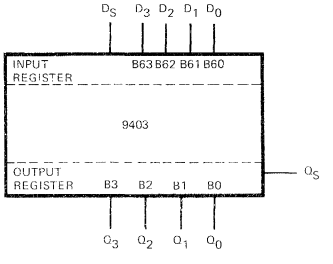


Fig. 3
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

PARALLEL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) Output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) Input is HIGH, and the $\overline{OES}$ Input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction, $\overline{TOS}$, $\overline{CPSO}$, and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial Data Output O_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output O_S. For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the Stack as soon as the previous one has been shifted out.

EXPANSION:

Vertical Expansion – The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does ot sacrifice any of the FIFO's flexibility for serial/parallel input and output.

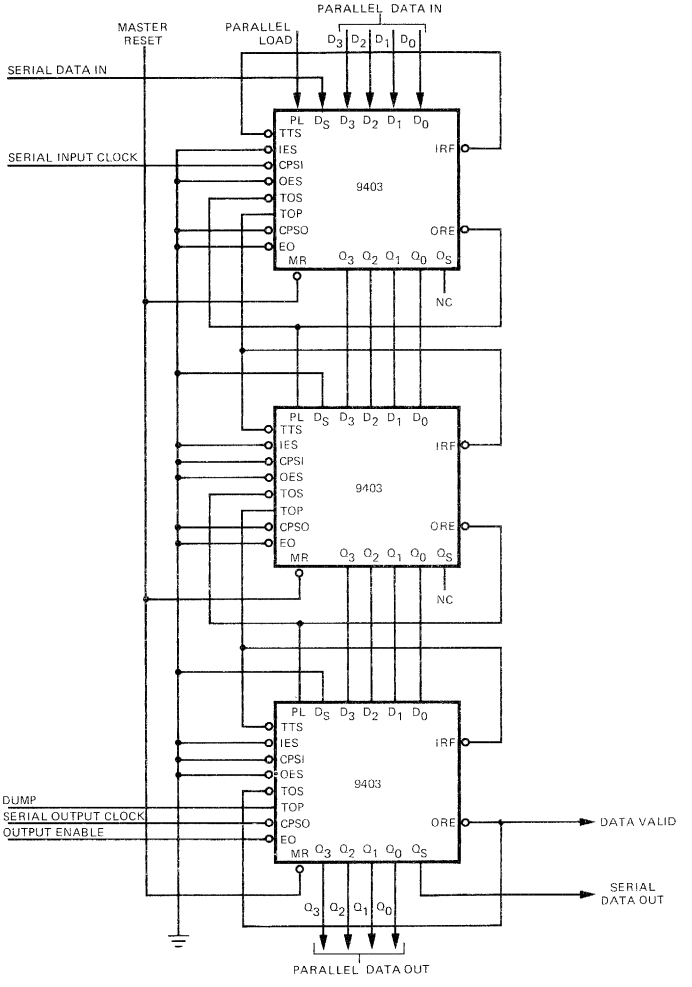


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 may also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 X n bits can be constructed. When expanding in the horizontal direction, it is usual to connect the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs respectively of all devices to the left (less significant devices) to guarantee that no operation is initiated before all devices are ready.

As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the FIFO's flexibility for serial/parallel input and output.

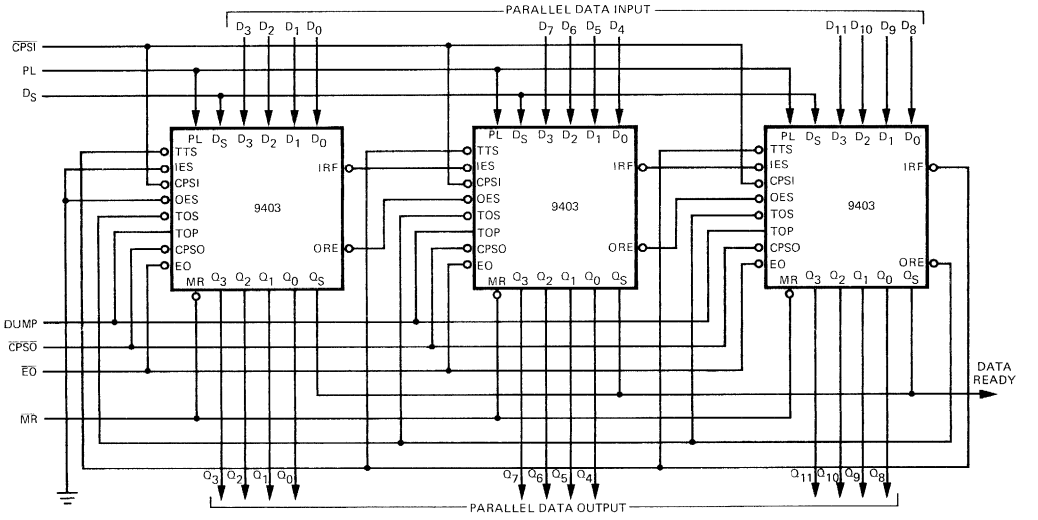


Fig. 5
A HORIZONTAL EXPANSION SCHEME

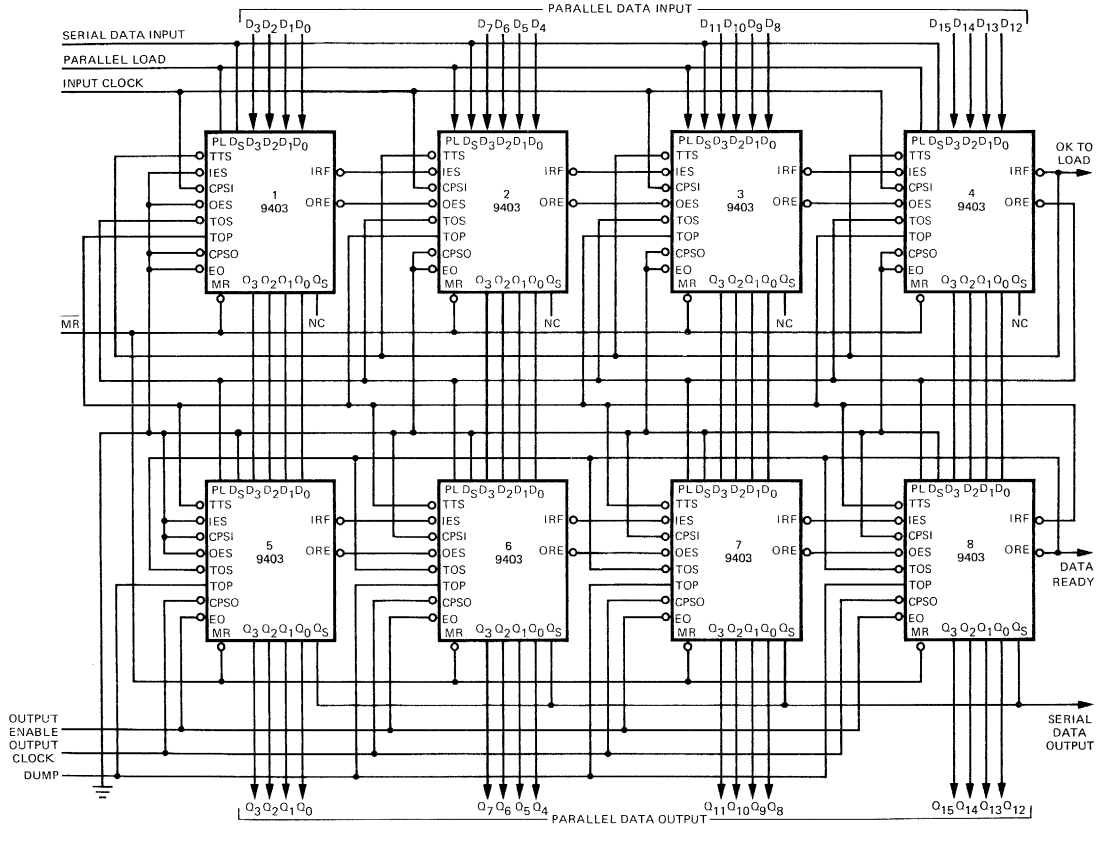


Fig. 6
A 31 X 16 FIFO ARRAY

Horizontal and Vertical Expansion – The 9403 can be expanded in both the horizontal and vertical direction without any external parts and without sacrificing any of the FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of $15n_1 + 1$ words by $4 \times n_2$ bits can be constructed.

Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

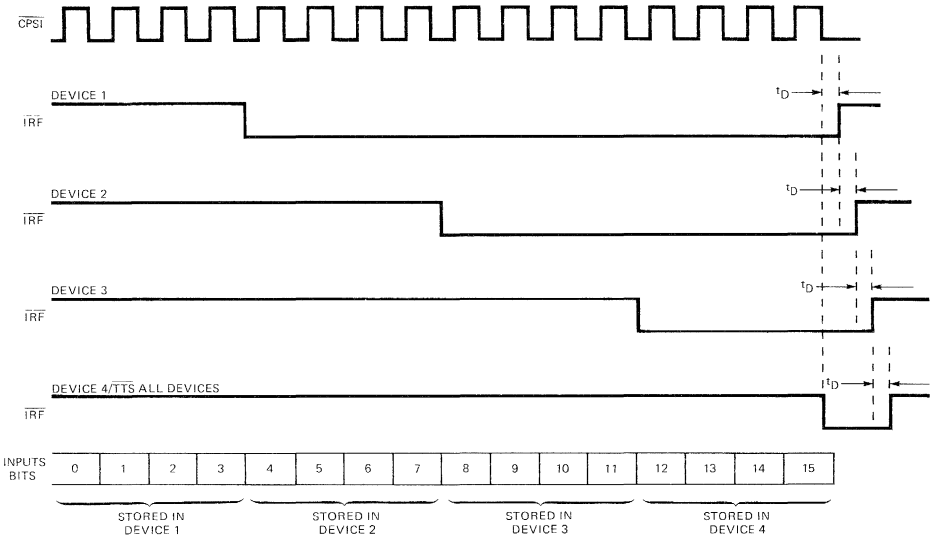


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

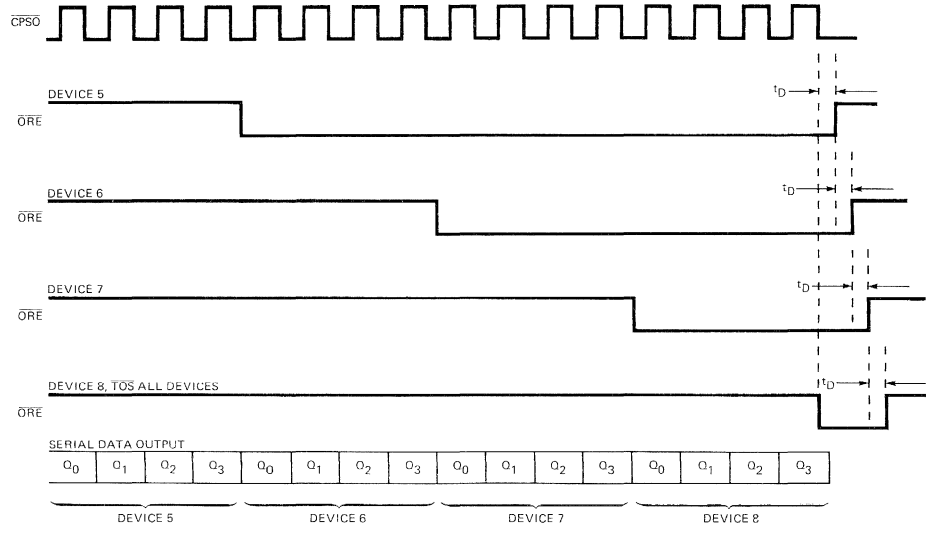


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

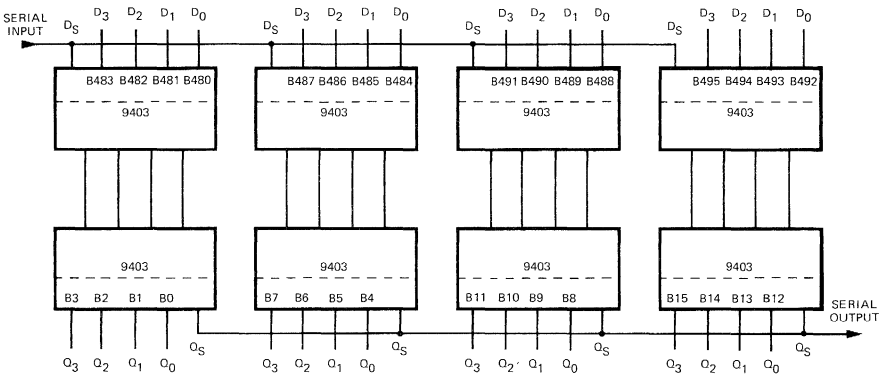


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

INTERLOCKING CIRCUITRY:

Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of Figure 6 devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ input has gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the master latch is set. Whenever $\overline{TTS}$ goes LOW the request initialization flip-flop will be set. If the master latch is HIGH, the input register will be immediately initialized and the request initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE request flip-flop. If the master latch is set, the last Output Register flip-flop is set and $\overline{ORE}$ goes HIGH. If the master latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

TABLE 1

OUTPUT CONDITION	INTERNAL STATE	
	Master Operation — IES LOW when Initialized	Slave Operation — IES HIGH when Initialized
$\overline{IRF}$ LOW	Input Register Full	Input Register Full and IES LOW
$\overline{ORE}$ HIGH	Output Register not Full	Output Register not Full and OES LOW

Table 1 summarizes master/slave status outputs.

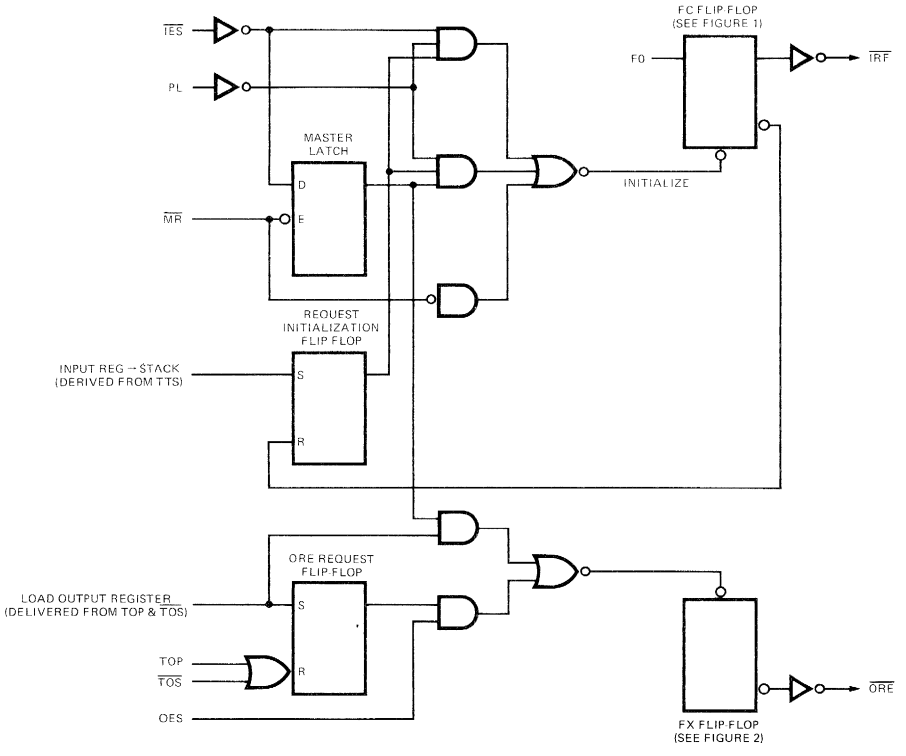


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage Q_S, ORE, OES	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage, Q_0–Q_3	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
V_{OL}	Output LOW Voltage, Q_0–Q_3, Q_S			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{OL}	Output LOW Voltage, ORE, OES			0.25	0.4	V	I_{OL} = 4.0 mA, V_{CC} = MIN
				0.35	0.5		I_{OL} = 8.0 mA, V_{CC} = MIN
I_{OZH}	Output Off Current HIGH, Q_0–Q_3, Q_S				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off Current LOW, Q_0–Q_3, Q_S				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, all except OES				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	OES				−0.86		
IOS	Output Short Circuit Current, ORE, OES		−10		−42	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{OS}	Output Short Circuit Current, Q_0–Q_3, Q_S		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)
I_{CC}	Supply Current			105	160	mA	V_{CC} = MAX, Inputs Open

6

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		18		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		50		ns	
t_{PLH}	Propagation Delay, Negative-Going $\overline{CPSO}$		30		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH, Figures 13 & 14
t_{PHL}	to Q_S Output		20			
t_{PLH}	Propagation Delay, Positive-Going TOP		42		ns	$\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PHL}	to Outputs $Q_0 - Q_3$		32			
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		35		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH, Figures 13 & 14
t_{PLH}	Propagation Delay, Positive-Going $\overline{TOS}$ to $\overline{ORE}$					
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$				ns	Parallel Output, $\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		45			
t_{ft}	Fall Through Time		450		ns	$\overline{TTS}$ connected to IRF TOS connected to $\overline{ORE}$ $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		48		ns	Data in stack, TOP HIGH, Figures 13 & 14
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going IRF		35		ns	Stack not full, Figures 17 & 18

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{CPSI}$ Pulse Width (HIGH)		25		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PWL}	$\overline{CPSI}$ Pulse Width (LOW)		12		ns	
t_{PWH}	PL Pulse Width (HIGH)		30		ns	Stack not full, Figures 17 & 18
t_{PWL}	$\overline{TTS}$ Pulse Width (LOW) Serial or Parallel Mode		6.0		ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{MR}$ Pulse Width (LOW)		15		ns	Figure 16
t_{PWH}	TOP Pulse Width (HIGH)		17		ns	$\overline{CPSO}$ LOW, Data available in stack, Figure 15
t_{PWL}	TOP Pulse Width (LOW)		25		ns	
t_{PWH}	$\overline{CPSO}$ Pulse Width (HIGH)		16		ns	TOP HIGH, Data in stack, Figures 13 & 14
t_{PWL}	$\overline{CPSO}$ Pulse Width (LOW)		20		ns	
t_s	Set-Up Time D_S to Negative $\overline{CPSI}$		20		ns	PL LOW, Figures 11 & 12
t_s	Set-Up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode		0		ns	Figures 11, 12, 17, 18
t_s	Set-Up Time Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$		0		ns	TOP HIGH, Figures 13 & 14
t_{rec}	Recovery Time $\overline{MR}$ to any Input		5.0		ns	Figure 16

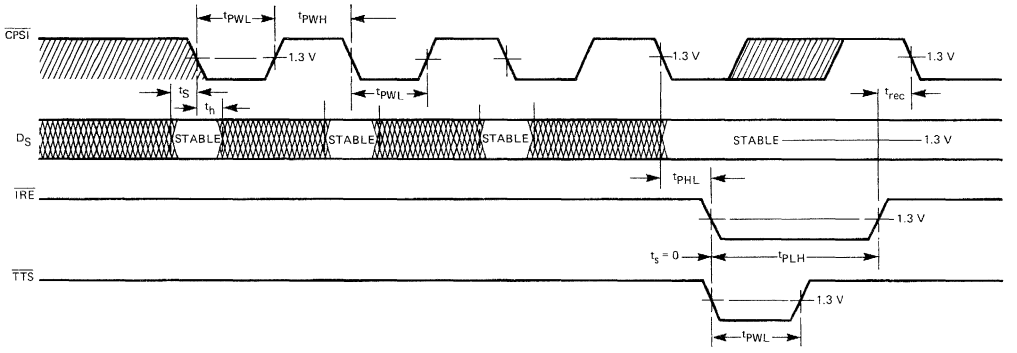


Fig. 11
SERIAL INPUT, UNEXPANDED OR MASTER OPERATION

Conditions: Stack not full, $\overline{IES}$, PL LOW

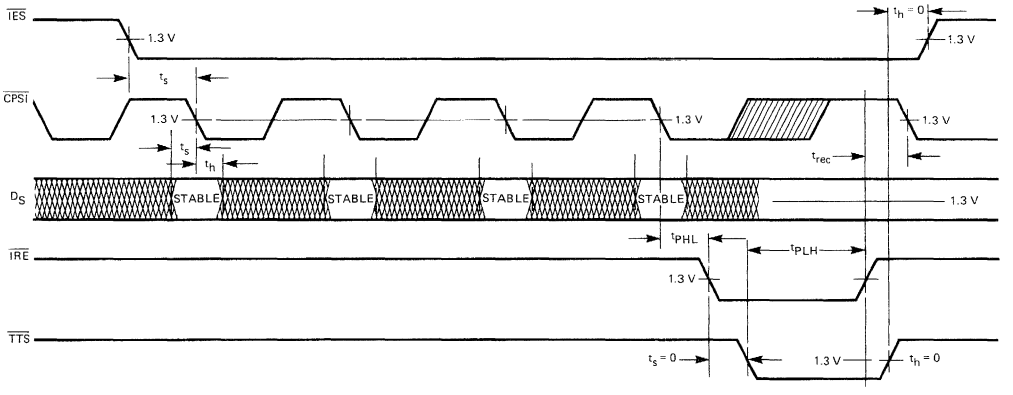


Fig. 12
SERIAL INPUT, EXPANDED SLAVE OPERATION

Conditions: Stack not full, $\overline{IES}$ HIGH when initialized, PL LOW

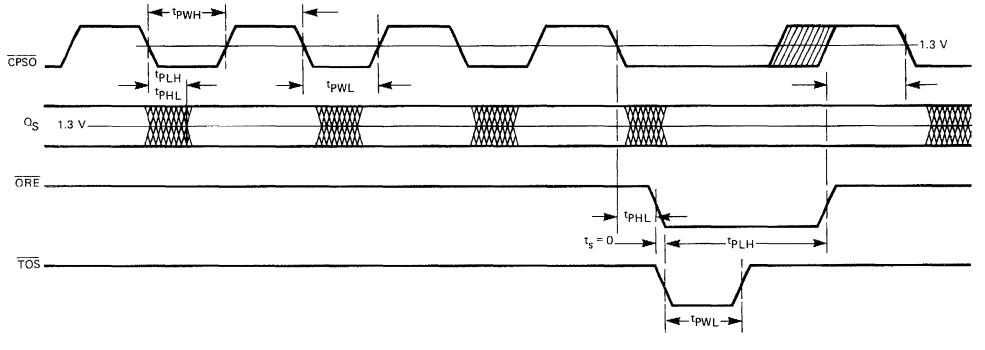


Fig. 13
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION

Conditions: Data in stack, TOP HIGH, $\overline{IES}$ LOW when initialized, $\overline{OES}$ LOW

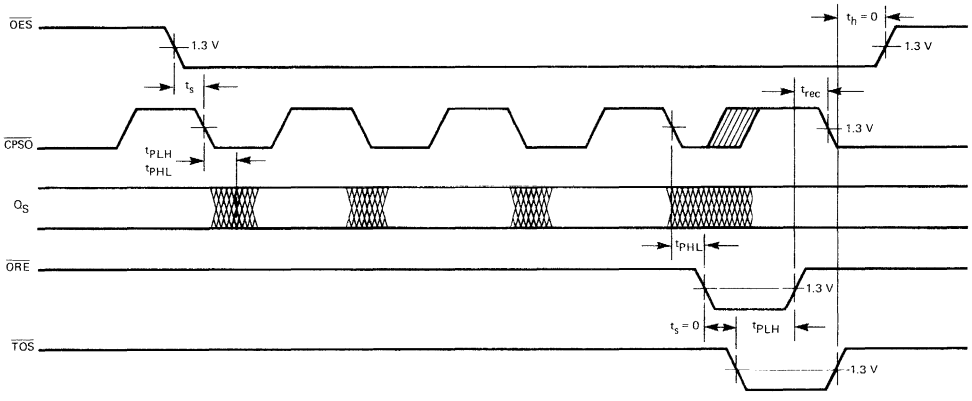


Fig. 14
SERIAL OUTPUT, SLAVE OPERATION

Conditions: Data in stack, TOP HIGH, $\overline{IES}$ HIGH when initialized

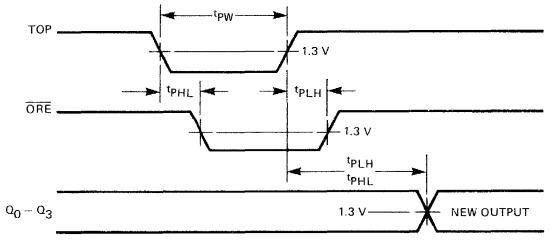


Fig. 15
PARALLEL OUTPUT, 4-BIT WORD OR MASTER IN PARALLEL EXPANSION

Conditions: $\overline{IES}$ LOW when initialized, $\overline{EO}$, $\overline{CPSO}$ LOW. Data available in stack

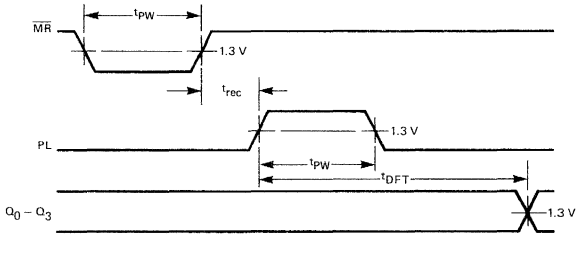
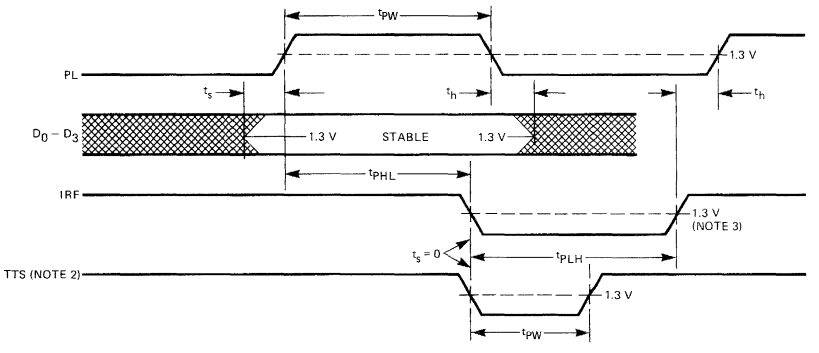


Fig. 16
FALL THROUGH TIME

Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH



NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, IRE will stay LOW.

Fig. 17
PARALLEL LOAD MODE, 4-BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

Conditions: Stack not full, $\overline{IES}$ LOW when initialized

6

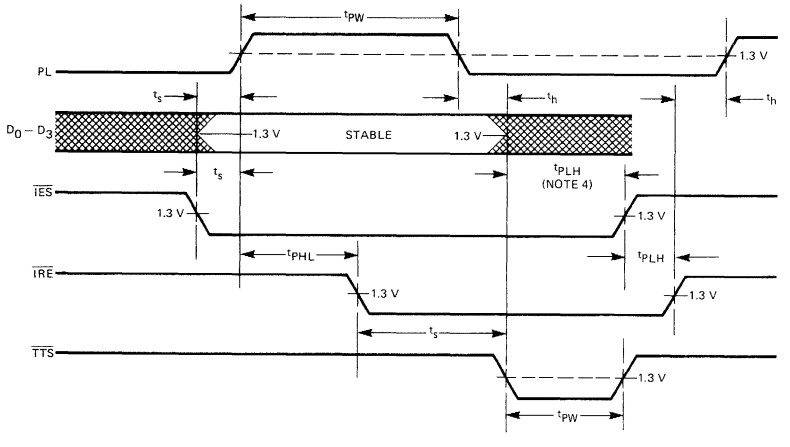


Fig. 18
PARALLEL LOAD, SLAVE MODE

Conditions: Stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

9404
DATA PATH SWITCH
FAIRCHILD MACROLOGIC™ TTL

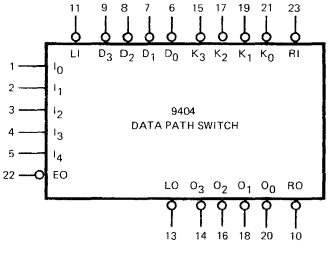
DESCRIPTION – The 9404 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the 9405 (Arithmetic Logic Register Stack). A total of 30 instructions (see Table 1) facilitate logic shifting, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction Word Inputs (I_0-I_4) selects one of the thirty instructions operating on two sets of 4-bit Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$). Left Input ($\overline{LI}$) and Left Output ($\overline{LO}$) and Right Input ($\overline{RI}$) and Right Output ($\overline{RO}$) are available for expansion in 4-bit increments. An active LOW Output Enable Input ($\overline{EO}$) provides 3-state control of the Data Outputs ($\overline{O}_0$-$\overline{O}_3$) for bus oriented applications.

The 9404 is a member of Fairchild's MACROLOGIC TTL family and is fully compatible with all TTL families.

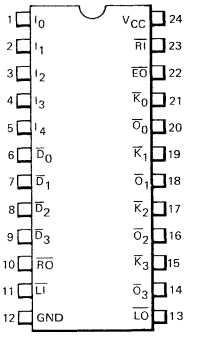
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **20 ns DELAY OVER 16-BIT WORD (EXCEPT SIGN EXTEND FUNCTION)**
- **TWO 4-BIT DATA INPUT BUSSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **PURELY COMBINATORIAL – NO CLOCKS REQUIRED**
- **PACKAGED IN SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)

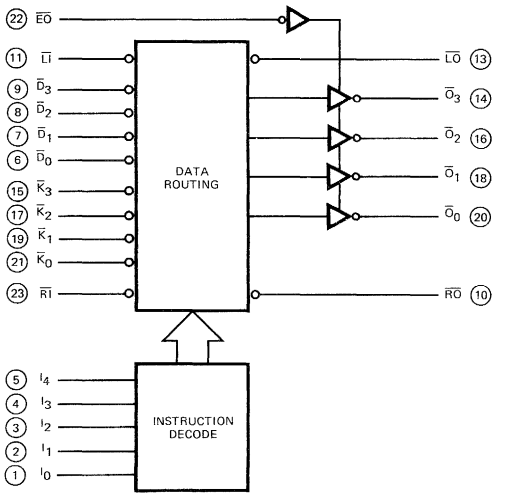


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{D}_0$-$\overline{D}_3$	D-Bus Inputs (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{K}_0$-$\overline{K}_3$	K-Bus Inputs (active LOW)	0.5 U.L.	0.23 U.L.
I_0-I_4	Instruction Word Input	0.5 U.L.	0.23 U.L.
$\overline{LI}$	Shift Left Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{LO}$	Shift Left Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
$\overline{RI}$	Shift Right Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{RO}$	Shift Right Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
$\overline{EO}$	Output Enable Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{O}_0$-$\overline{O}_3$	Data Output (active LOW) (Note b)	130 U.L.	10 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V

BLOCK DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Number

TABLE 1
INSTRUCTION SET FOR THE 9404

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS						FUNCTION
I_4	I_3	I_2	I_1	I_0	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$		I_4	I_3	I_2	I_1	I_0	$\overline{LO}$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	$\overline{RO}$	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)	H	L	L	H	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)	H	L	L	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Sign Extend
L	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	$\overline{RI}$		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask D-Bus	H	L	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	$\overline{RI}$		K-Bus Shift Left
L	L	H	H	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	H	L		$\overline{LI}$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask D-Bus	H	L	H	H	H		$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right Arith(2)
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		$\overline{LI}$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right Arith(2)
L	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Byte Mask K-Bus	H	H	L	H	L		$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		Byte Mask K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask K-Bus
L	H	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined (Reserved)
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined (Reserved)

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

FUNCTIONAL DESCRIPTION — The 9404 Data Path Switch combines the functions of a dual 4-input multiplexer, a true/complement one/zero generator, and a shift left/shift right array.

As shown in Table 1, there are two shift right modes. The arithmetic right shift preserves the sign bit in the most significant position while the logic shift moves all positions. Right shift is defined as a 1-bit shift toward the least significant position.

For half-word arithmetic the 9404 provides instructions which extend the sign bit left through the more significant slices. Shift linkages are available as individual inputs and outputs for complete flexibility.

The 9404 may be used to generate constants +1, 0, −1 and −2 in 2s complement notation.

9404 ARRAYS – Arrays of larger than 4-bit word lengths are easily obtained. Figure 1 illustrates a 16-bit array constructed using four devices; device 1 is the least significant and device 4 is the most significant slice. Within each slice, inputs and outputs with '0' subscript are the least significant bits.

The I_1 through I_4 inputs of all devices are bussed. These four bus lines together with the I_0 inputs of the devices form an 8-bit instruction bus to control the array. In some applications, it may be possible to connect the I_0 inputs of devices 1 & 2 together and the I_0 Inputs of devices 3 & 4 together, so that only six bits are needed to control the arrays. Connecting the $\overline{LO}$ of device 1 to $\overline{RI}$ of device 2, $\overline{LO}$ of device 2 to RI of device 3, etc. provides left shift (i.e., shift towards most significant bit) and sign extension. From Table 1 it can be seen that "sign extend" consists of two adjacent instructions differing only in I_0; one of these instructions connects the most significant bit of the selected input bus (i.e., $\overline{D}_3$ or $\overline{K}_3$) to the $\overline{LO}$ output while the other instruction forces the output bus and $\overline{LO}$ to the $\overline{RI}$ input. In a similar fashion right shift operation is accomplished by connecting the $\overline{LI}$ input of a device to the $\overline{RO}$ of the next more significant device.

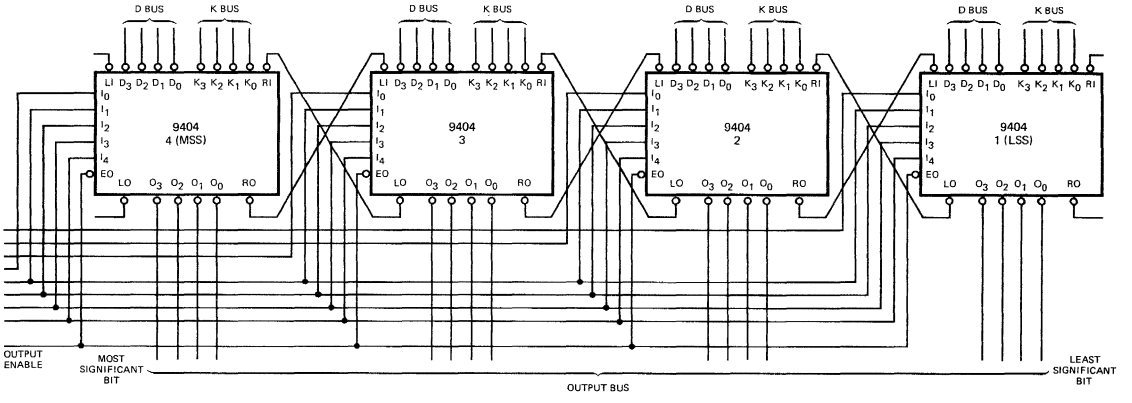


Fig. 1 16-BIT 9404 ARRAY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			–0.9	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage $\overline{LO}$, $\overline{RO}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = –400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $\overline{O}_0$-$\overline{O}_3$	XM	2.4	3.4		V	I_{OH} = –2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = –5.7 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{LO}$, $\overline{RO}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $\overline{O}_0$-$\overline{O}_3$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V
I_{OZL}	Output Off Current LOW				–100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		–30		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			76		mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$) to Output (O_0-O_3)		20		ns	$\overline{EO}$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$) to Shift Outputs ($\overline{LO}$, $\overline{RO}$)		18		ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{RI}$ to $\overline{LO}$		25		ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction Word (I_0-I_5) to Data Outputs ($\overline{O}_0$-$\overline{O}_3$)		22		ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction Word (I_0-I_5) to Shift Outputs ($\overline{RO}$, $\overline{LO}$)		22		ns	
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs ($\overline{O}_0$-$\overline{O}_3$)		12		ns	
t_{PLZ} t_{PHZ}	Disable Delay, EO to Outputs ($\overline{O}_0$-$\overline{O}_3$)		8		ns	

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9405
ARITHMETIC LOGIC REGISTER STACK
FAIRCHILD MACROLOGIC™ TTL

DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement general registers in high performance programmable digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0-A_2). The result of the operation is loaded into the same RAM location and simultaneously, is loaded into the output register making it available at the 3-state output data bus.

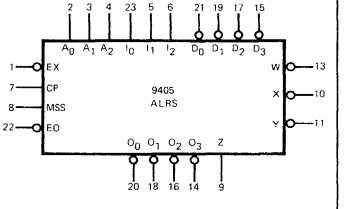
The 9405 operates on four bits of data but features are provided for expansion to longer word lengths. Carry Propagate and Carry Generate Outputs are provided for an external carry lookahead where maximum operating speed is required. In applications where high speed arithmetic is not needed, ripple expansion may also be implemented. The 9405 provides three status signals: Zero, Negative and Overflow. These qualify the result of an operation. The 9405 is a member of Fairchild's MACROLOGIC TTL family and is fully compatible with all TTL families.

- **EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE**
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR LOOKAHEAD CARRY**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES STATUS – ZERO, NEGATIVE, AND OVERFLOW**
- **3-STATE OUTPUTS**
- **24-PIN PACKAGE**

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
A_0-A_2	Address Instruction Inputs	0.5 U.L.	0.23 U.L.
I_0-I_2	ALU Instruction Inputs (Note b)	0.5 U.L.	0.23 U.L.
MSS	Most Significant Slice Input (Active HIGH)	0.5 U.L.	0.23 U.L.
$\overline{CP}$	Clock Input	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
O_0-O_3	Data Outputs (Active LOW)	130 U.L.	10 U.L.
$\overline{W}$	Ripple Carry Output (Active LOW) (Note c)	10 U.L.	5 U.L.
$\overline{X}$	Carry Propagate Output (Note d)	10 U.L.	5 U.L.
$\overline{Y}$	Carry Generate Output (Note e)	10 U.L.	10 U.L.
Z	Zero Status Output (Active HIGH, Open Collector) (Note f)		5 U.L.

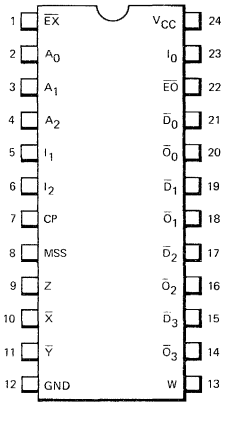
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW (0.5 V).
b) I_0 used also for Carry Input on lesser significant slices.
c) $\overline{W}$ Output also carries instruction information.
d) $\overline{X}$ Output provides Negative Status (active LOW) on most significant slice.
e) $\overline{Y}$ Output provides Overflow Status (active LOW) on most significant slice.
f) An external pull-up resistor is required to supply HIGH level drive capability.

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM

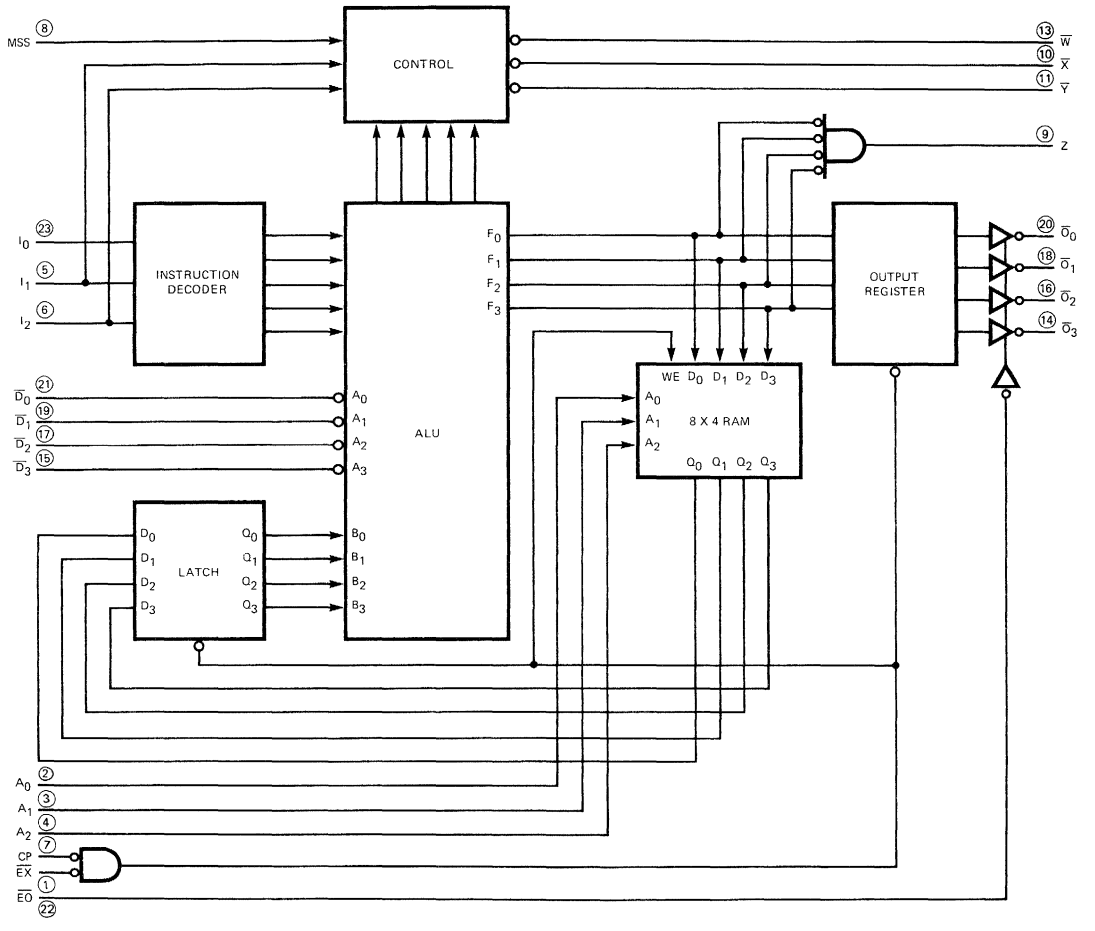


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TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2 I_1 I_0	INTERNAL OPERATION	
L L L	Rx plus D-Bus plus 1 → Rx	Accumulate
L L H	Rx plus D-Bus → Rx	Accumulate
L H L	Rx · D-Bus → Rx	Logic AND
L H H	D-Bus → Rx	Load
H L L	Rx → Output Register	Output
H L H	Rx + D-Bus →	Logic OR
H H L	Rx ⊕ D-Bus → Rx	Exclusive OR
H H H	D-Bus → Rx	Load Complement

NOTES:
1. Rx is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

FUNCTIONAL DESCRIPTION – As shown in the Block Diagram the 9405 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an instruction decode network, control logic and a 4-bit Output Register.

The ALU receives the active LOW input data ($\overline{D}_0$-$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and output register. The active LOW Output Data Bus ($\overline{O}_0$-$\overline{O}_3$) is obtained from the output register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level $\overline{EO}$ disables the buffers (high impedance state).

The instruction bus for the 9405 consists of two fields, A and I; A_0-A_2 specify the desired location of the RAM and I_0-I_2 specify the desired function to be performed. Table 1 lists Instruction Field Code assignments. Thus, the 9405 provides eight registers (R_0-R_7) and eight different operations may be performed on any of these registers. The I_0-I_2 Inputs are decoded by the instruction decode network to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: Carry Out, Carry Propagate, Carry Generate, Negative Status and Overflow Status. The control logic manipulates the status signals as a function of I_0-I_2 and a control input MSS. A HIGH on the MSS Input declares the most significant slice in a 9405 array (the diode-input on MSS allows it to be tied directly to V_{CC}). All devices, except the most significant 9405 should have a LOW level (ground) on the MSS Input. The control logic generates three device outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$ for arrayed operation. An all zero result from the ALU is decoded and presented at the open collector Zero Status (Z) Output.

The I_0 input serves a dual purpose. For arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 9405 expansion schemes.

OPERATION – The 9405 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input active LOW AND gate. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$-$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0-I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. The A lines must obviously be held stable during this time. On the LOW-to-HIGH CP transition, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A Inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

9405 ARRAYS – The 9405 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 9405 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 9405s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, $\overline{CP}$ and $\overline{EO}$ Inputs of all devices. The Z Output is open collector and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four 9405s. The MSS input is tied to V_{CC} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-Field and I-Field. A-Field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 Inputs forms the I-Field for the array. The I_0 Inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ Outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ Output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ Output is the carry output of that slice. In case of non-arithmetic instructions, it assumes the state of the I_0 input. Thus, in Figure 1, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ Output to I_0 Input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 Inputs together to form the I-Field for the array. The $\overline{W}$ Output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ Outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

Thus, $\overline{X}$ Output of device 4 is LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW level on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occured. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by EX or CP. Figure 2 shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 93S42/74S182 in addition to the four 9405s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS Inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-Field for the array instruction bus is obtained by connecting corresponding A Inputs of all four devices. Bussed I_1 and I_2 Inputs together with the I_0 Input of device 1 form the I-Field for the array. The I_0 Inputs for devices 2, 3 and 4 are obtained from the 93S42/74S182 Carry Outputs (Cn+x, Cn+y, and Cn+z

respectively). Also the $\overline{P}$ and $\overline{G}$ Inputs of 93S42/74S182 are connected to $\overline{X}$ and $\overline{Y}$ Outputs of the 9405s as shown. The control logic in the 9405 (see Block Diagram) generates $\overline{X}$ and Y Outputs as a function of I_1, I_2 and MSS Inputs as well as the Carry Generate and Carry Propagate Outputs of the ALU. If the MSS Input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ Output reflects Carry Propagate and $\overline{Y}$ reflects Carry Generate Outputs from that slice. For an arithmetic instruction the I_0 Input is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ Outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ Output of device 4 is the carry output from the array. Also, note that the I_0 Input of device 1 is not only an instruction input but also provides the carry input to the array so the I_0 Input of device 1 must be connected to the appropriate 93S42/74S182 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 9405 forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ Outputs on all except the most significant slice. An examination of the 93S42/74S182 logic reveals that whenever $\overline{P}$ is LOW and $\overline{G}$ is HIGH the associated carry output is the same as the carry input. Thus, in Figure 2 devices 2, 3, and 4 will assume the logic level as that presented to the I_0 Input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion $\overline{X}$ and $\overline{Y}$ Outputs of device 4 represent Negative and Overflow from the array.

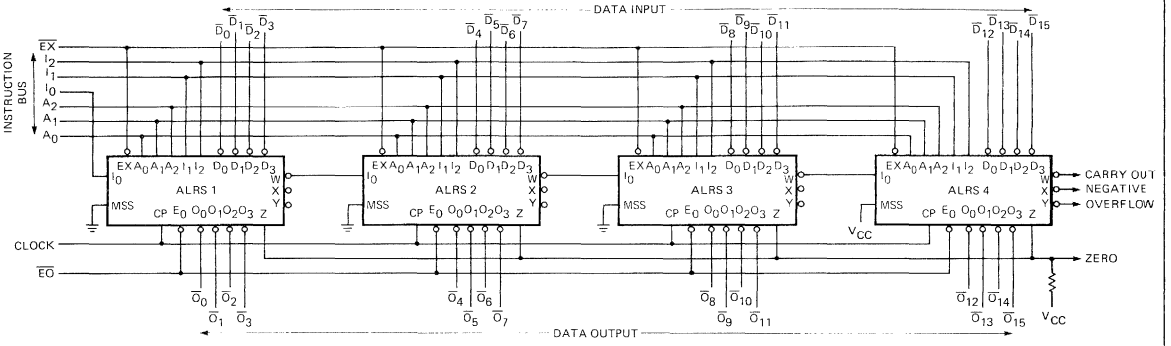

Fig. 1 RIPPLE CARRY EXPANSION

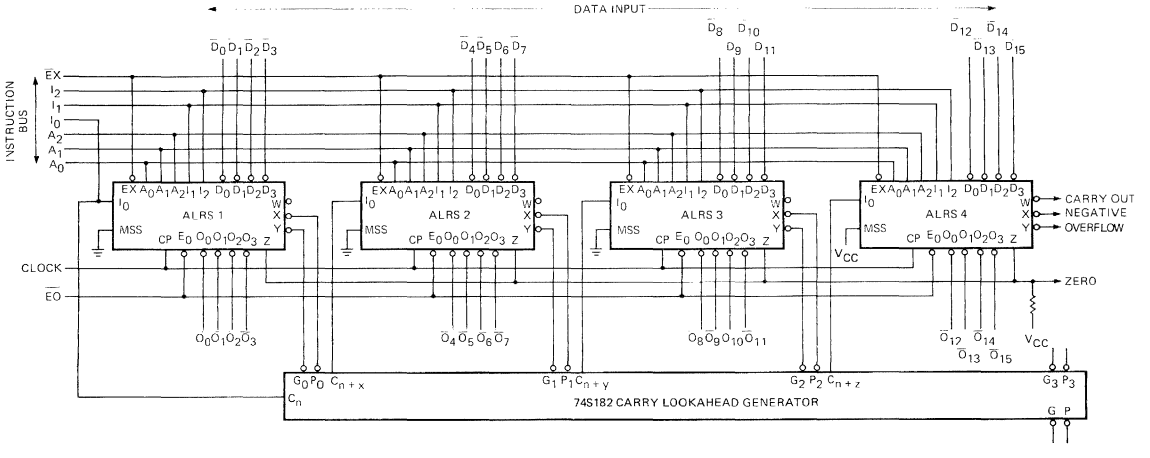

Fig 2. CARRY LOOKAHEAD EXPANSION

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{W}$, $\overline{X}$ Outputs	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA; V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA; V_{CC} = MIN
I_{OH}	Output HIGH Current Z Output				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{W}$, $\overline{X}$, Z			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3, \overline{Y}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			100	160	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{CW}	Clock Period		75		ns	
t_{PWH}	Clock Pulse Width (HIGH)		30			
t_{PWL}	Clock Pulse Width (LOW)		20			
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0			
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0			
t_sA1	Set-Up Time, A_0, A_1, A_2 to Negative Going CP (Note 1)		25		ns	
t_sA2	Set-Up Time, A_0, A_1, A_2 to Positive Going CP (Note 1)		70		ns	$\overline{EX}$ LOW
t_hA	Hold Time, A_0, A_1, A_2 to Positive Going CP		5		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive Going CP		45		ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive Going Clock		−20		ns	
t_sI	Set-Up Time, I_0, I_1, I_2 to Positive Going Clock		50		ns	
t_hI	Hol dTime, I_0, I_1, I_2 to Positive Going Clock		0		ns	

NOTE:
1. Both set-up times must be met simultaneously.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Positive Going CP to $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		25		ns	$\overline{EO}$, $\overline{EX}$ LOW
t_{PLH} t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		15		ns	I_1 or I_2 HIGH
t_{PLH} t_{PHL}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to $\overline{W}$		35		ns	I_1, I_2 LOW
t_{PLH}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to $\overline{X}$, $\overline{Y}$		50		ns	MSS HIGH; I_1, I_2
t_{PHL}			25		ns	MSS LOW; I_1, I_2 LOW
t_{PLH} t_{PHL}	Propagation Delay, I_1 I_2 to $\overline{X}$, $\overline{Y}$		22		ns	MSS LOW
t_{PLH} t_{PHL}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to Z		55		ns	1 kΩ External Load Resistor to V_{CC}
t_{PLH} t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		40		ns	I_1, I_2 LOW
t_{PLH}	Propagation Delay, I_1, I_2 to $\overline{W}$		15		ns	I_1, I_2 LOW
t_{PHL}			40			
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D3}$ to $\overline{X}$		50		ns	I_1, I_2 HIGH MSS HIGH
t_{PLH} t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$, $\overline{Y}$		55		ns	I_1, I_2 LOW MSS LOW
t_{PLH} t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$, $\overline{Y}$		70		ns	I_1, I_2 LOW MSS HIGH
t_{PLH} t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$		70		ns	I_1, I_2 HIGH MSS HIGH
t_{PLH} t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{W}$		55		ns	I_1, I_2 LOW
t_{PLH} t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to Z		70		ns	I_1, I_2 LOW
t_{PLH}	Propagation Delay, I_1, I_2 to $\overline{X}$, $\overline{Y}$		20		ns	I_1, I_2 LOW
t_{PHL}			45		ns	MSS HIGH
t_{PLH} t_{PHL}	Propagation Delay, I_0 to $\overline{X}$, $\overline{Y}$		50		ns	I_1, I_2 LOW MSS HIGH
t_{PLH} t_{PHL}	Propagation Delay, I_1, I_2 to Z		42		ns	I_1, I_2 LOW
t_{PLH} t_{PHL}	Propagation Delay, I_0 to Z		25		ns	I_1, I_2 LOW
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		12		ns	
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}$ to $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		10		ns	

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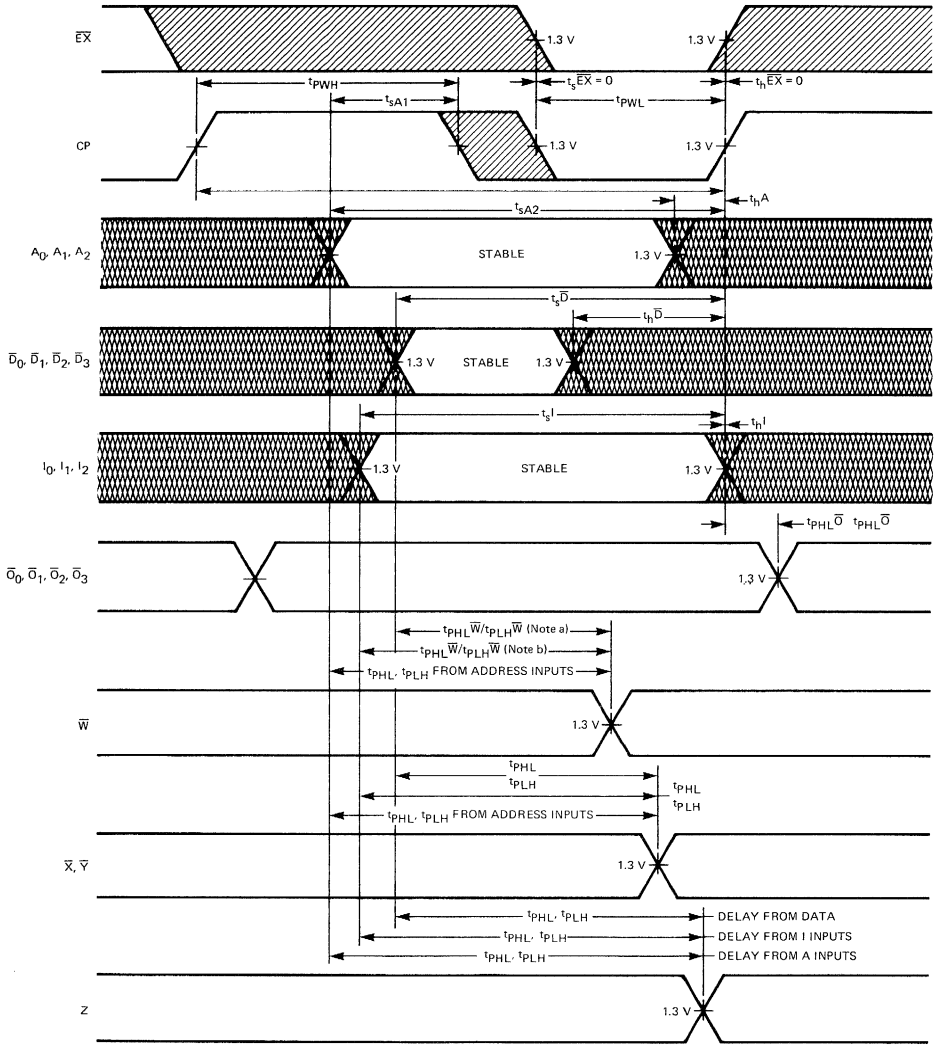


NOTES:

a) Delay for logical operation (I_1 or I_2 HIGH)

b) Delay for arithmetic operation ($I_1 = I_2$ = LOW)

Fig. 3 ALRS TIMING DIAGRAM

9406

PROGRAM STACK

FAIRCHILD MACROLOGIC™ TTL

DESCRIPTION – The 9406 is a 16-word by 4-bit "Push-Down Pop-Up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 9406 executes 4 instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, the Program Counter (PC) is in the top location of the Stack. As a new PC value is "pushed" into the Stack (Call Operation), all previous PC values effectively move down one level. The top location of the Stack is the current PC. Up to 16 PC values can be stored, which gives the 9406 a 15 level nesting capability. "Popping" the Stack (Return Operation) brings the most recent PC to the top of the Stack. The remaining two instructions affect only the top location of the Stack. In the Branch operation a new PC value is loaded into the top location of the Stack from the $\overline{D}_0 - \overline{D}_3$ Inputs. In the Fetch operation, the contents of the top Stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 9406 may be expanded to any word length without additional logic. 3-State output drivers are provided on the 4-bit Address Outputs ($X_0 - X_3$) and Data Outputs, ($\overline{O}_0 - \overline{O}_3$); the X-Bus Outputs are enabled internally during the Fetch instruction while the O-bus Outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 9406 is a member of Fairchild's 9400 MACROLOGIC TTL family, and is fully compatible with all TTL families.

- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **10 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADS FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **24-PIN PACKAGE**
- **3-STATE OUTPUTS**

PIN NAMES

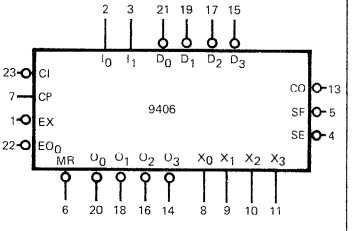
		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
I_0, I_1	Instruction Inputs	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_0$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Output Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{CO}$	Carry Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SF}$	Stack Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SE}$	Stack Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:

a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.

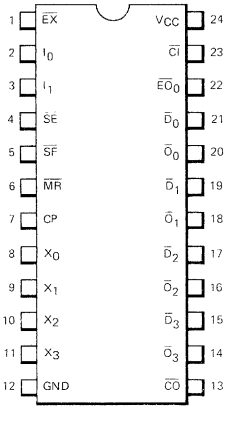
b. Output fan-out with $V_{OL} \leq 0.5$ V.

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – As shown in the Block Diagram, the 9406 consists of an input multiplexer, a 16 X 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 9406 is organized around three 4-bit busses; the Input Data Bus ($\overline{D}_0 - \overline{D}_3$), Output Data Bus ($\overline{O}_0 - \overline{O}_3$) and the Address Bus ($X_0 - X_3$). The 9406 implements four instructions as determined by Inputs I_0 and I_1. (See Table 1). The O-Bus is derived from the RAM output latches and enabled by the active LOW Output Enable ($\overline{EO}_0$) Input. The X-Bus is also derived from the output latches; it is enabled internally during the Fetch instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) Inputs.

FETCH OPERATION – The Fetch Operation places the content of the current Program Counter (PC) on the X-Bus. If the Carry In ($\overline{CI}$) is LOW, the current PC is incremented in preparation for the next Fetch. If $\overline{CI}$ is HIGH, the value of the current program is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The active level LOW Execute ($\overline{EX}$) is normally set up at this time as well. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the input multiplexer. The current PC value is loaded into the latches and is available on the O-Bus if $\overline{EO}_0$ is LOW. When CP is LOW the output latches are disabled from following the RAM output, when both CP and $\overline{EX}$ are LOW, buffers are enabled, applying the current PC to the X-Bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out (CO) is LOW when the contents of the current PC is at its maximum, e.e., all ones and the Carry In ($\overline{CI}$) is LOW. When CP or EX goes HIGH, writing into the RAM is inhibited and the Address Buffers ($X_0 - X_3$) are disabled.

BRANCH OPERATION – During a Branch Operation, the Data Inputs ($\overline{D}_0 - \overline{D}_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. The Stack Pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into the current PC. The X-Bus drivers are not enabled during a Branch Operation.

CALL OPERATION – During a Call Operation the content of the Data Bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The Instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the Stack Pointer value thus incrementing the RAM address. Since the output latches go to the nontransparent or store mode when CP is LOW, the O-Bus outputs will reflect the RAM output at the CP negative-going transition. If EX goes LOW considerably before CP goes LOW, the O-Bus will correspond to the previous contents of the incremented RAM address after CP goes LOW. If CP goes LOW a very short time after EX, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

When CP is LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into this new RAM location. On the LOW-to-HIGH CP transition, the incremented Stack Pointer value is loaded into the Stack Pointer Register and the O-Bus Outputs reflect the newly entered data. When the RAM address is "1111" the Stack Full Output ($\overline{SF}$) is LOW, indicating that no further Call operations should be initiated. If an additional Call Operation is performed SP is incremented to (0000), the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-Bus drivers are not enabled during a Call operation.

RETURN OPERATION – During the Return operation the previous PC is "popped" to become the current PC.

The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the Stack Pointer value, thus decrementing the RAM address. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the new value after $\overline{EX}$ goes LOW. If CP goes LOW a short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

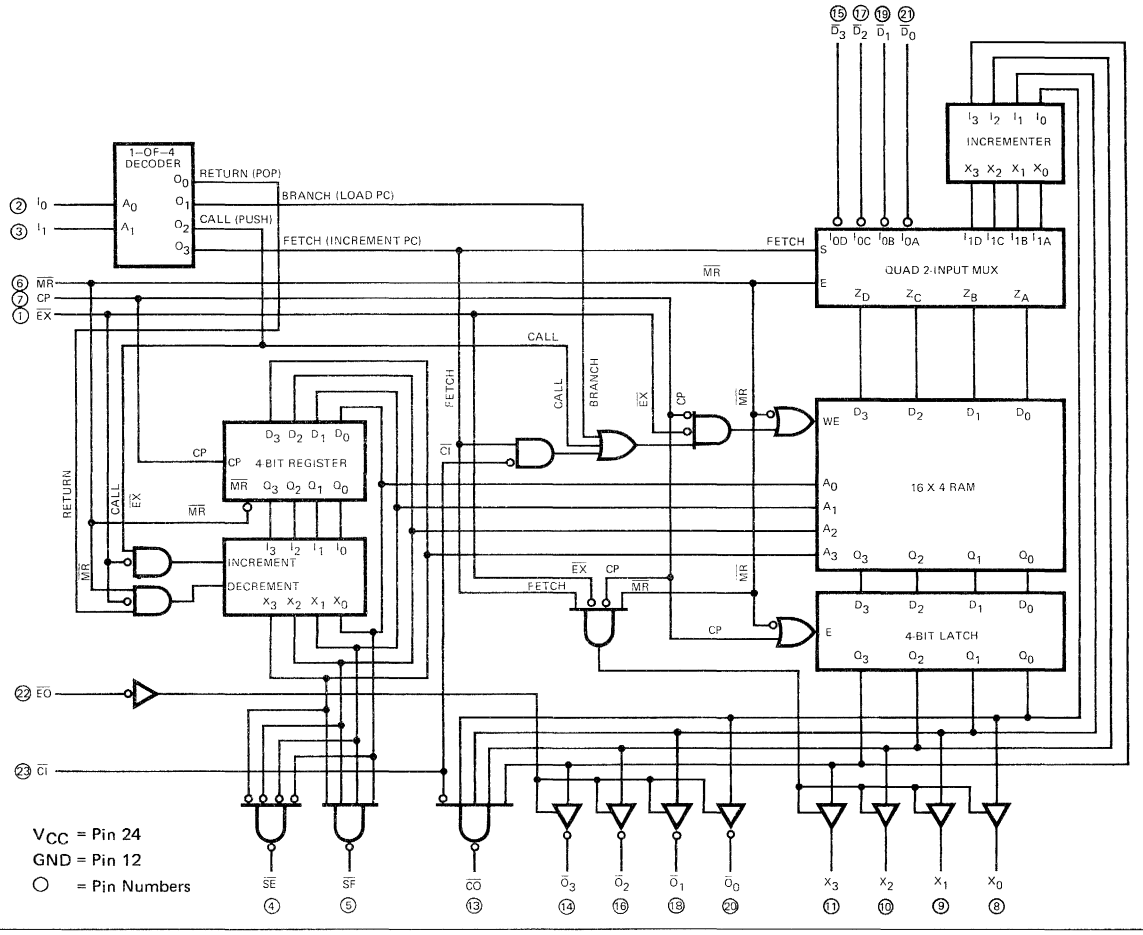
On the LOW-to-HIGH CP transition the decremented Stack Pointer value is loaded into the Stack Pointer Register and the O-Bus Outputs correspond to the new "popped" value.

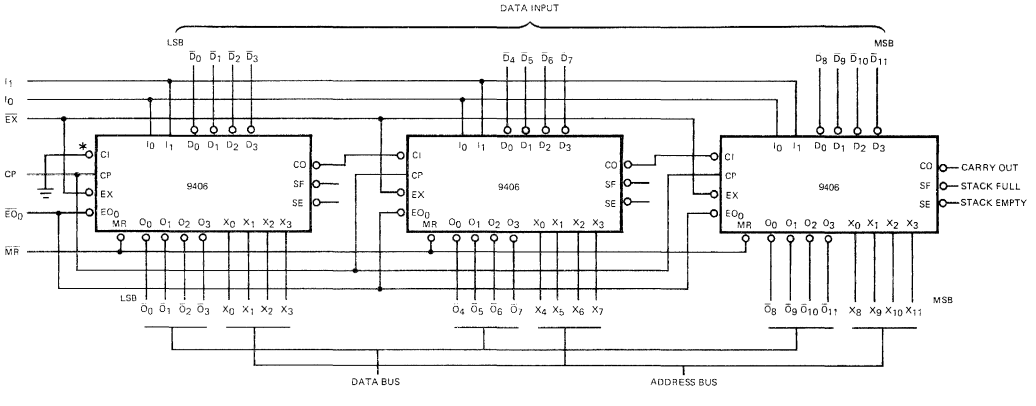
The X-Bus drivers are not enabled during a return operation. When the RAM address is "0000", the Stack Empty Output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full Output ($\overline{SF}$) will go LOW. Operation of the active LOW Master Reset ($\overline{MR}$) causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

MULTIPLE 9406 OPERATION – The 9406 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in Figure 1. Carry In ($\overline{CI}$) and Carry Out (CO) are connected to provide automatic increment of the current program counter during Fetch. The $\overline{CI}$ Input of the least significant 9406 is tied LOW to ground.

If automatic increment during Fetch is not desired, the $\overline{CI}$ Input of the least significant 9406 is held HIGH.

BLOCK DIAGRAM





*Tie to V_{CC} to disable automatic increment.

Fig. 1
9406 EXPANSION A 16 BY 12 PROGRAM STACK

TABLE 1
INSTRUCTION SET FOR THE 9406

I_1 I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH EO_0 LOW)
L L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of EX and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L H	Branch (Load PC)	Load D-Bus into Current Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H L	Call (Push)	Increment Stack Pointer and Load D-Bus into New Program Counter Location	Disabled	Depending on the relative timing of EX and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Figure 9 for details.
H H	Fetch (Increment PC)	Increment Current Program Counter if CI is LOW	Current Program Counter while both CP and EX are LOW, disabled while CP or EX is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level
L = LOW Level

DC CHARACTERISTICS OVER OPERATION TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{CO}$, SE, $\overline{SF}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $X_0 - X_3, \overline{O}_0 - \overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
V_{OL}	Output LOW Voltage $\overline{CO}$, SE, $\overline{SF}$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.35	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $X_0 - X_3, \overline{O}_0 - \overline{O}_3$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.35	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CCH}	Supply Current			100	160	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS – ALL MODES OF OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{CW}	Clock Period		80		ns	
t_{PWH}	Clock Pulse Width (HIGH)		40		ns	
t_{PWL}	Clock Pulse Width (LOW)		30		ns	
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0		ns	Figure 2
t_sI	Set-Up Time, I_0, I_1 to Negative-Going Clock		20		ns	
t_hI	Hold Time, I_0, I_1 to Positive-Going Clock		0		ns	
$t_s\overline{CI}$	Set-Up Time, $\overline{CI}$ to Negative-Going Clock		5		ns	
$t_h\overline{CI}$	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	
t_sD	Set-Up Time, D_0–D_3 to Positive-Going Clock		20		ns	
t_hD	Hold Time, D_0 – D_3 to Positive-Going Clock		0		ns	
$t_{PWL}\overline{MR}$	$\overline{MR}$ Pulse Width (LOW)		40		ns	Figure 3
t_{rec}	$\overline{MR}$ to Negative-Going Clock		30		ns	

REFER TO INDIVIDUAL TIMING DIAGRAMS FOR EACH OPERATION TO DETERMINE OUTPUT RESPONSE

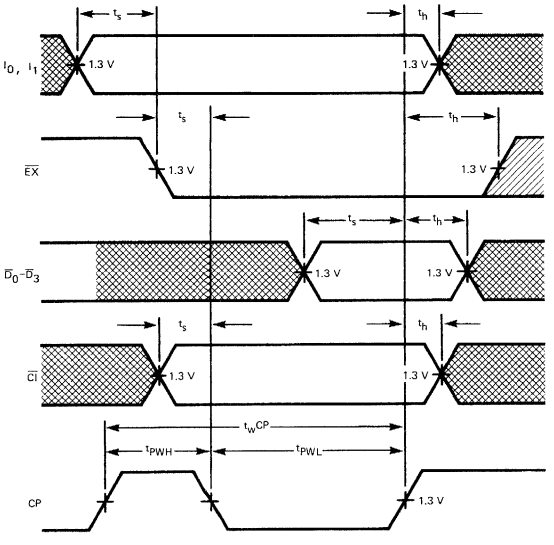


Fig. 2
WAVEFORMS FOR ALL OPERATIONS

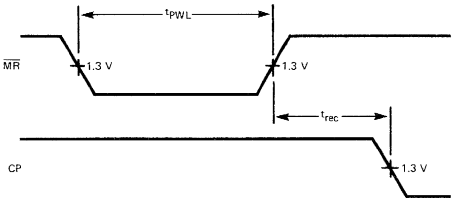


Fig. 3
RESET OPERATION

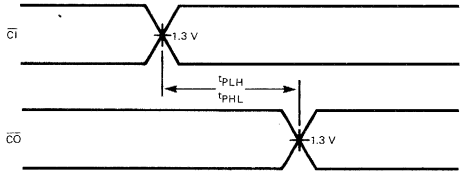


Fig. 4
CARRY-IN TO CARRY-OUT

AC CHARACTERISTICS – ALL MODES OF OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Carry In ($\overline{CI}$) to Carry Out ($\overline{CO}$)		14 10		ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Carry Out ($\overline{CO}$)		34 38		ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Carry Out ($\overline{CO}$)		34 38		ns	Figure 6

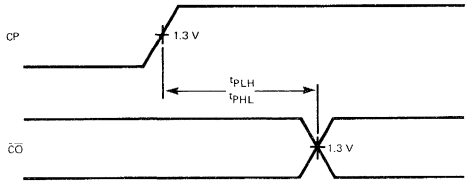


Fig. 5
CLOCK TO CARRY-OUT

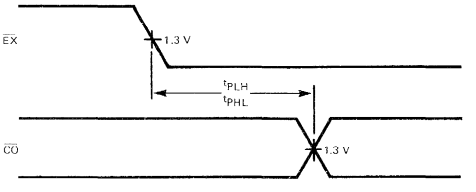


Fig. 6
EXECUTE TO CARRY-OUT

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE BRANCH (LOAD PC) OPERATION:
V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Outputs ($\overline{O}_0 - \overline{O}_3$)		28 36		ns	$\overline{EO}_0$ LOW Figures 7 and 8
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$		20		ns	
t_h	Hold Time I_0, I_1 to Positive-Going $\overline{EX}$		0		ns	$\overline{EX}$ goes HIGH before CP, Figure 8
t_h	Hold Time, I_0, I_1 to Positive-Going CP		0		ns	CP goes HIGH before $\overline{EX}$, Figure 7
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		16		ns	Figures 7 and 8
t_h	Hold Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		0		ns	
t_{PWL}	$\overline{EX}$ Pulse Width		30		ns	$\overline{EX}$ Goes HIGH Before CP, Figure 8

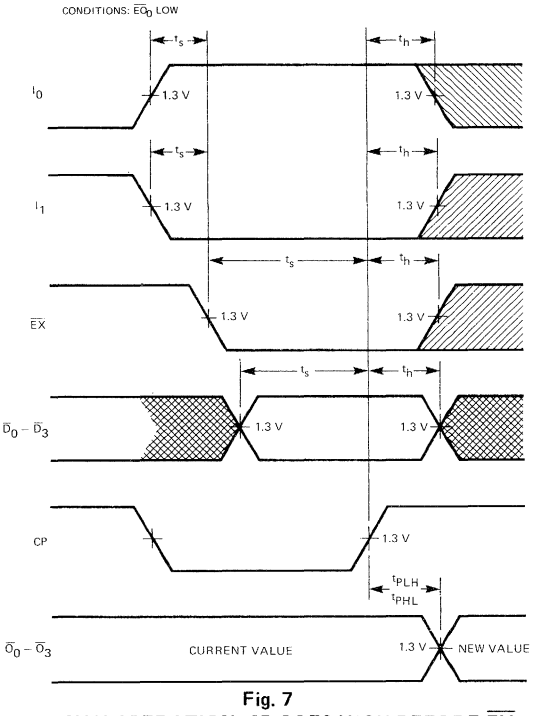


Fig. 7
BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

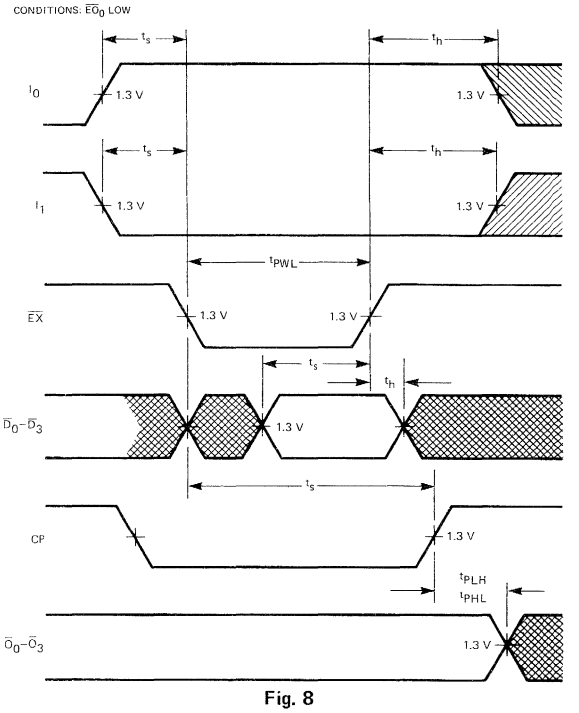


Fig. 8
BRANCH OPERATION, EX GOES HIGH BEFORE CP

6

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE CALL (PUSH) OPERATION:
V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 9)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		35 55		ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Intermediate Value of $\overline{O}_0 - \overline{O}_3$		30 45		ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		20 40		ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1		20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1		0		ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees Intermediate Data on $\overline{O}_0 - \overline{O}_3$ while CP is LOW		45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees no Change in $\overline{O}_0 - \overline{O}_3$ While CP is LOW		0		ns	
$t_h\overline{EX}$	Hold Time, Positive-Going CP to Positive-Going $\overline{EX}$		0		ns	
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		20		ns	
t_h	Hold Time, Positive-Going CP to $\overline{D}_0 - \overline{D}_3$		0		ns	

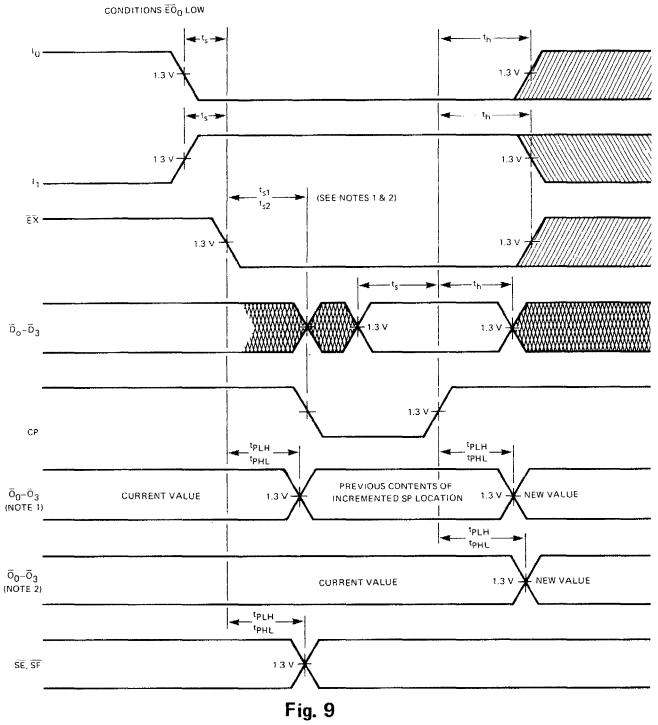


Fig. 9
CALL (PUSH) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW ($t_{S2}\overline{EX}$ is met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE RETURN (POP) OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 10)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		28 55		ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to New Value of $\overline{O}_0 - \overline{O}_3$		30 45		ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		20 40		ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1		20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1		0		ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees the New Value on $\overline{O}_0 - \overline{O}_3$ While CP is LOW		45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP. Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ must be met for Proper Operation		0		ns	
$t_{s3}\overline{EX}$	Set-Up Time, EX to Positive-Going CP. Either $t_{s3}\overline{EX}$ or $t_{s2}\overline{EX}$ (Above) must be met for Proper Operation.		30		ns	

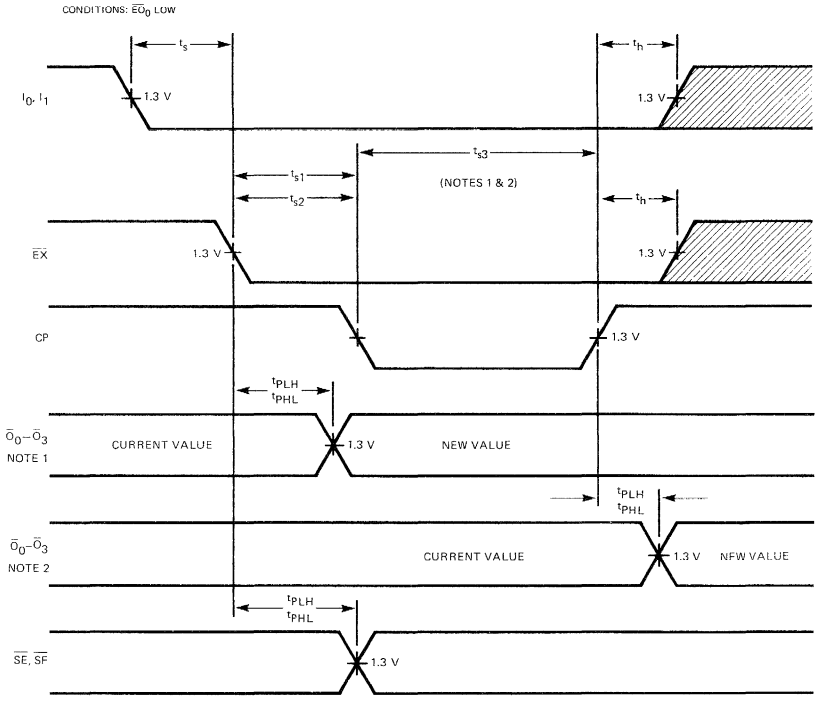


Fig. 10
RETURN (POP) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW (t_{s1} $\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (either t_{s2}EX or $t_{s3}\overline{EX}$ are met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE FETCH OPERATION:
V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay Positive-Going CP to Incremented Value of $\overline{O}_0 - \overline{O}_3$		29 38		ns	$\overline{EO}_0$, $\overline{CI}$ LOW, Figures 13 and 14
t_{PZL} t_{PZH}	Turn-On Delay, from CP or $\overline{EX}$ Whichever goes LOW last to $X_0 - X_3$		15 12		ns	$\overline{EO}_X$ LOW, Figures 11, 12, 13 and 14
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$		20		ns	Figures 11, 12, 13 and 14
t_h	Hold Time , I_0, I_1 to CP or $\overline{EX}$ whichever goes HIGH first		0		ns	
t_s	Set-Up Time, Negative Going $\overline{EX}$ to Positive-Going CP		25		ns	
t_s	Negative-Going $\overline{CI}$ to Positive-Going CP		20		ns	Fetch with Increment, Figures 13 and 14
t_h	Positive-Going $\overline{CI}$ to Negative-Going $\overline{EX}$		0			Iterative Fetch, Figures 11 and 12

CONDITIONS $\overline{EO}_0$ LOW, CP goes HIGH before $\overline{EX}$

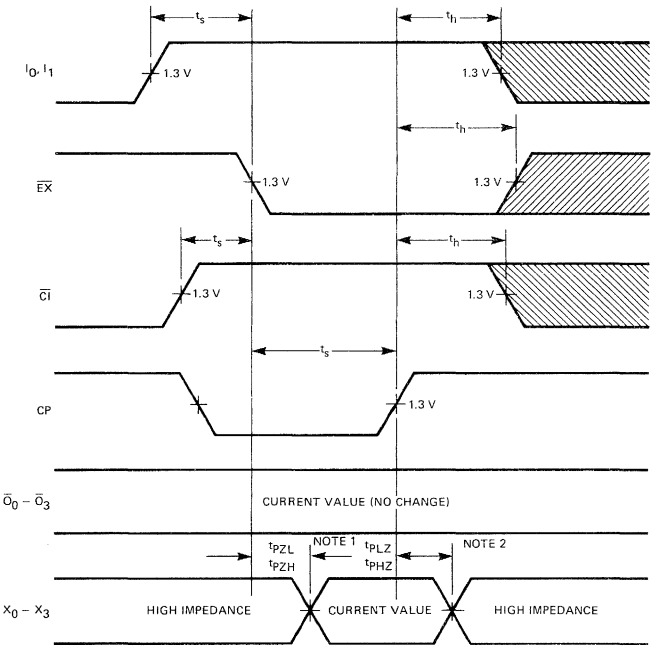


Fig. 11
ITERATIVE FETCH

CONDITIONS $\overline{EO}_0$ LOW, $\overline{EX}$ goes HIGH before CP

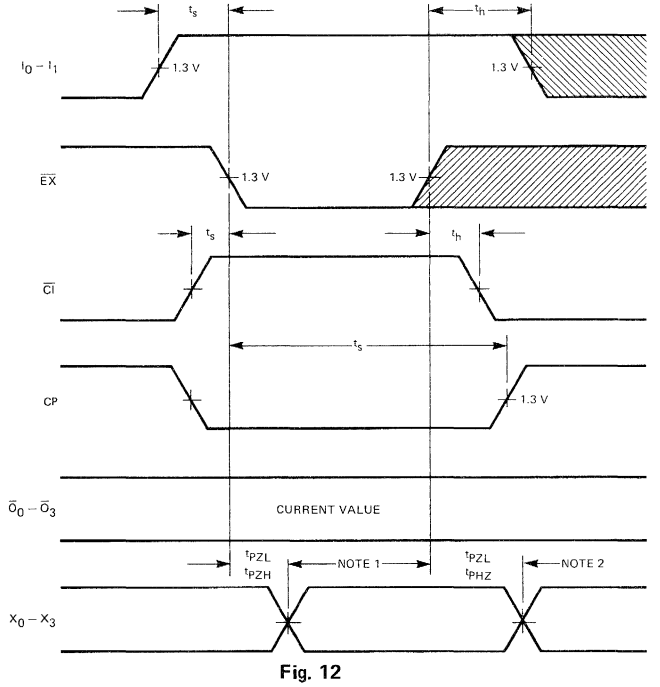


Fig. 12
ITERATIVE FETCH

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

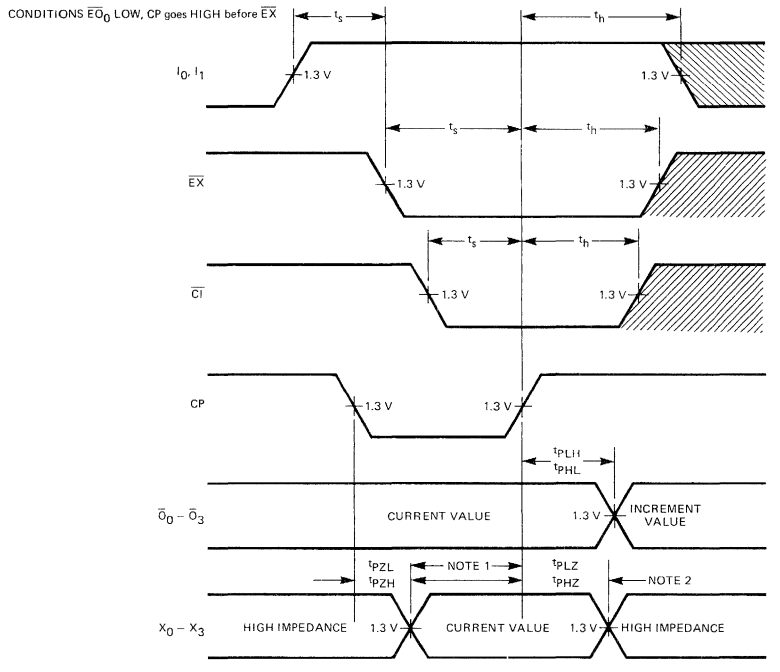


Fig. 13
FETCH WITH INCREMENT PC

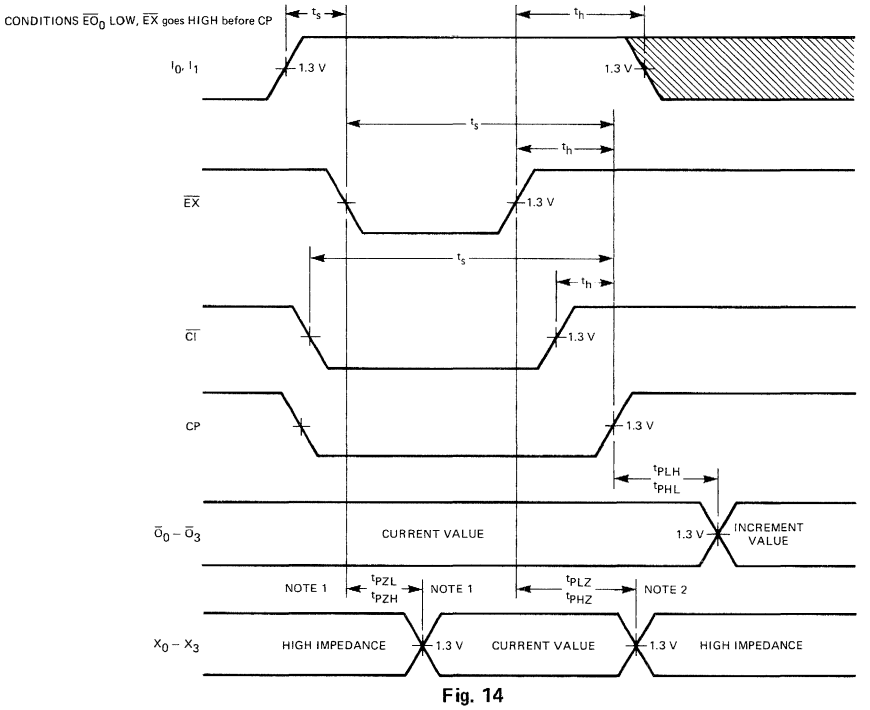


Fig. 14
FETCH OPERATION WITH INCREMENT PC

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

9407

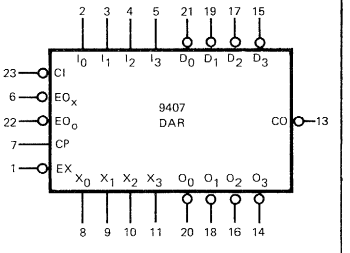
DATA ACCESS REGISTER

FAIRCHILD MACROLOGIC™ TTL

DESCRIPTION – The 9407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1), and Operand Address (R_2). The 9407 implements 16 instructions (see Table 1) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 10 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The 9407 is a member of Fairchild's MACROLOGIC TTL family and is fully compatible with all TTL families.

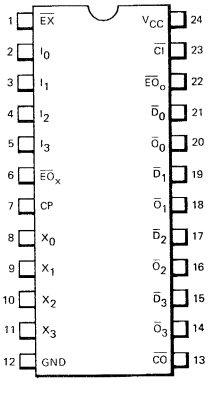
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **THREE 4-BIT REGISTERS**
- **16 INSTRUCTIONS FOR REGISTER MANIPULATION**
- **TWO SEPARATE OUTPUT PORTS, ONE TRANSPARENT**
- **RELATIVE ADDRESSING CAPABILITY**
- **3-STATE OUTPUTS**
- **OPTIONAL PRE OR POST ARITHMETIC**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



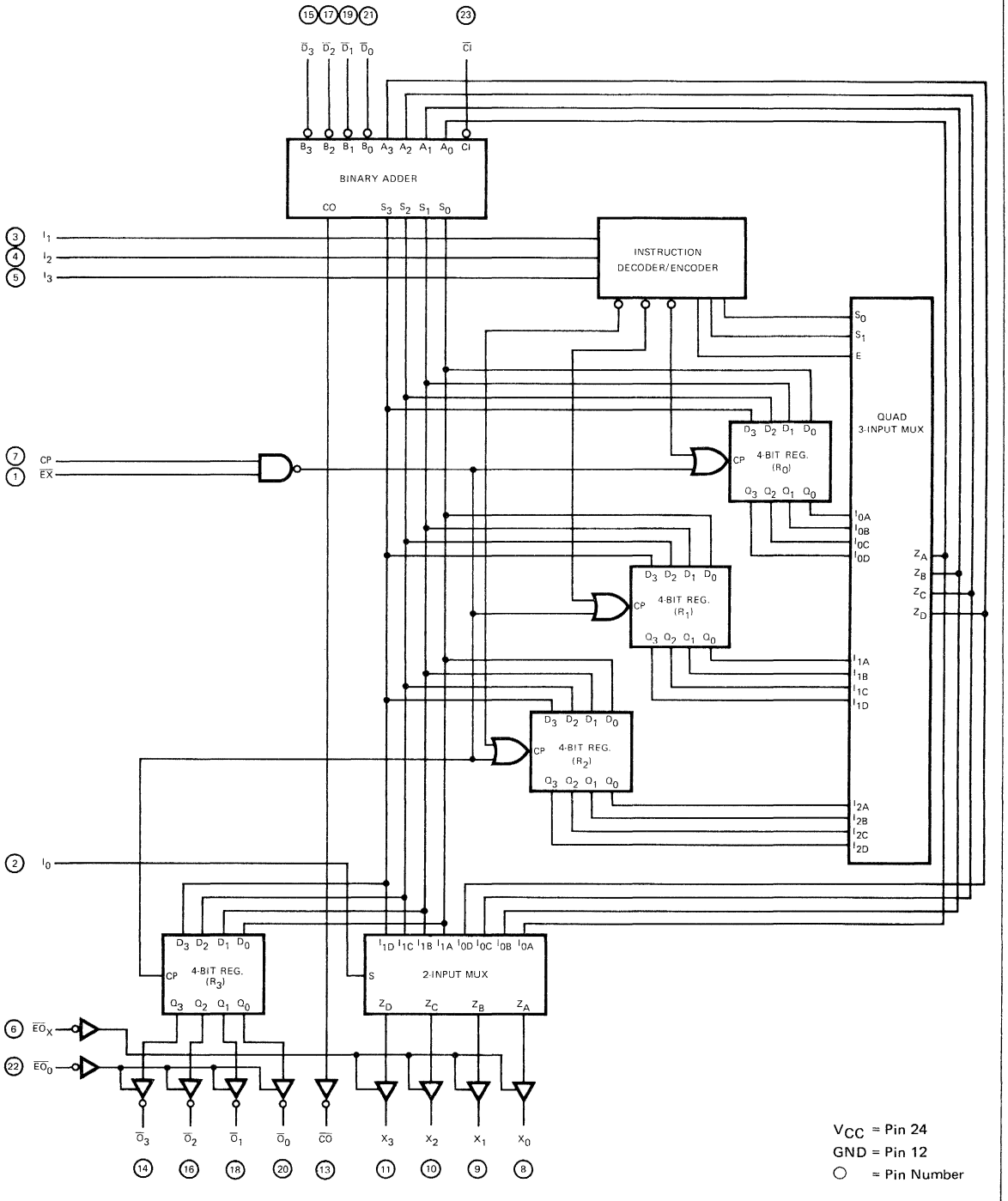
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
$I_0 - I_3$	Instruction Word Inputs	0.5 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW) (Note b)	0.5 U.L.	0.23 U.L.
$\overline{CO}$	Carry Output (Active LOW)	10 U.L.	5 U.L.
CP	Clock Input (L → H Edge-Triggered)	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_X$	Address Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_0$	Data Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output Current measured at V_{OUT} = 0.5 V.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 9407 contains a 4-bit slice of three Registers (R_0–R_2), a 4-Bit Adder, a 3-state Address Output Buffer (X_0–X_3), and a separate Output Register with 3-state buffers ($\overline{O}_0$–$\overline{O}_3$), allowing output of the register contents on the data bus (refer to the Block Diagram). The DAR performs 16 instructions, selected by I_0–I_3, as listed in Table 1.

OPERATION – The 9407 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input, active LOW AND gate. For normal operation $\overline{EX}$ is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data Inputs $\overline{D}_0$–$\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines (I_1,I_2,I_3) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH CP transition writes the result from the Adder into a register (R_0–R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the 3-state Buffer controlling the address bus (X_0–X_3) independent of EX and CP. If I_0 is LOW, the multiplexer routes the output of the selected register directly into the 3-State Buffer controlling the Address Bus (X_0–X_3), independent of $\overline{EX}$ and CP.

9407 ARRAYS – The 9407 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – In a typical application, the register utilization in the DAR may be as follows: R_0 is the program counter (PC), R_1 is the stack pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction Fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC, and loaded into R_2 during the next microcycle.

TABLE 1
INSTRUCTION SET FOR THE 9407

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

L = LOW Level
H = HIGH Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, $\overline{CO}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_1$	XM	2.4	3.4		V	I_{OH} = −2.0 mA V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA
V_{OL}	Output LOW Voltage, $\overline{CO}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			90	145	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

6

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{CW}	Clock Period (Note)		80		ns	
t_{PWH}	Clock Pulse Width (HIGH) (Note)		50			
t_{PWL}	Clock Pulse Width (LOW) (Note)	20				
t_s	Set-Up Time, $I_0 - I_3$ to Negative-Going Clock	20			ns	
t_h	Hold Time, $I_0 - I_3$ to Positive-Going Clock	0			ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	20			ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	0			ns	
t_sI	Set-Up Time, $\overline{CI}$ to Positive-Going Clock	5			ns	
t_hI	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to $\overline{O}_0 - \overline{O}_3$ (Note)		32 22		ns	$\overline{EO}_0$ LOW, Figure 3
t_{PLH} t_{PHL}	Instruction Inputs – $I_1 - I_3$ to $X_0 - X_3$		26 22		ns	$\overline{EO}_X$ LOW, I_0 LOW, Figure 1
t_{PLH} t_{PHL}	Instruction Inputs – $I_1 - I_3$ to $X_0 - X_3$		50 45		ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 1
t_{PLH} t_{PHL}	Positive-Going Clock to $X_0 - X_3$		40 35		ns	$\overline{EO}_X$, I_0 LOW
t_{PLH} t_{PHL}	Positive-Going Clock to $X_0 - X_3$		65 55		ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 2
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to $X_0 - X_3$		30 30		ns	I_0 HIGH, $I_1 - I_3$ Stable, EO LOW, Figure 4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CI}$ to $X_0 - X_3$		24 20		ns	I_0 HIGH, $I_1 - I_3$ Stable, EO_X LOW, Figure 5
t_{PLH} t_{PHL}	Propagation Delay I_0 to $X_0 - X_3$		24 32		ns	$\overline{EO}_X$ LOW, Figure 2
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to $\overline{CO}$		45 58		ns	Figure 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$		13 22		ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs $\overline{D}_0 - \overline{D}_3$ to $\overline{CO}$		13 24		ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Instruction Inputs $I_1 - I_3$ to $\overline{CO}$		30 32		ns	Figure 1
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}_0$ to Outputs $\overline{O}_0 - \overline{O}_3$, $\overline{EO}_X$ to $X_0 - X_3$		13 18		ns	
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}_0$ to $\overline{O}_0$, $\overline{O}$ $\overline{EO}_X$ to $X_0 - X_3$		13 13		ns	

TIMING DIAGRAM

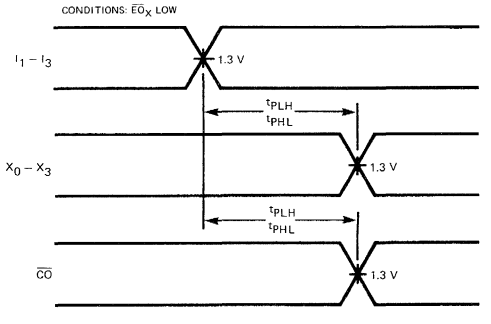
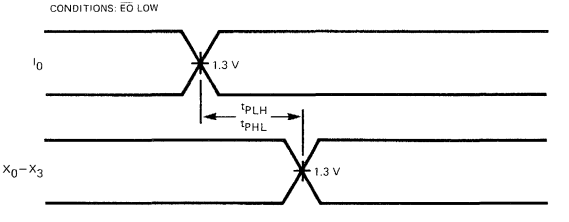


Fig. 1



NOTE:
The internal clock is generated from CP and $\overline{EX}$. The internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW.

Fig. 2

TIMING DIAGRAM

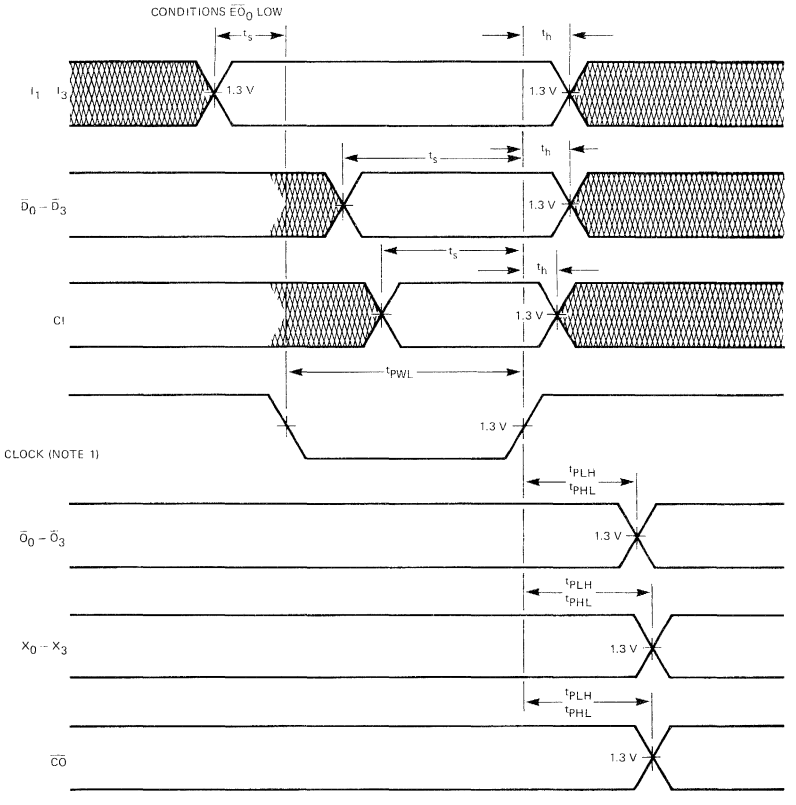


Fig. 3

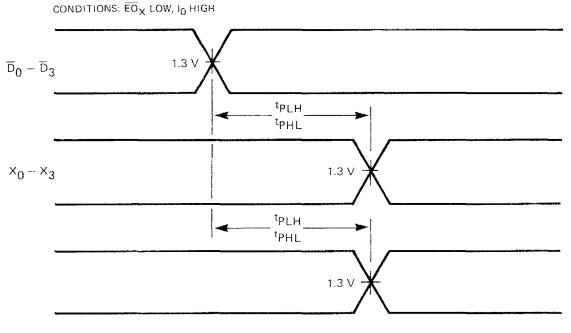


Fig. 4

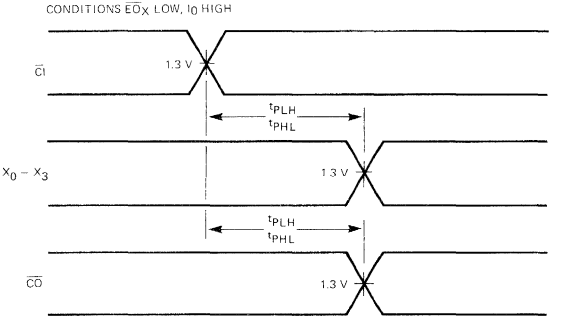


Fig. 5

9410

REGISTER STACK • 16×4 RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD MACROLOGIC™ TTL

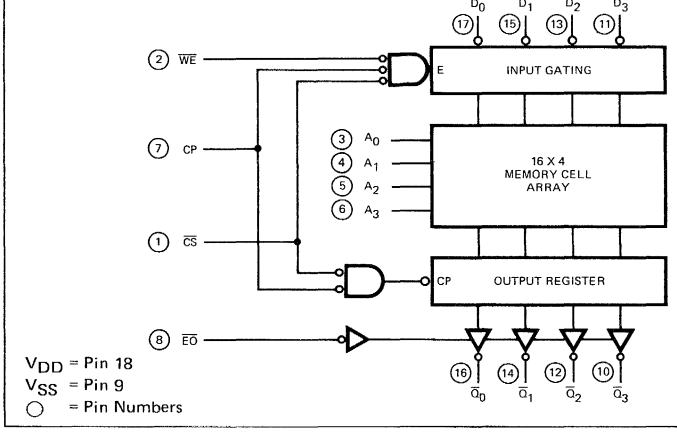
DESCRIPTION — The 9410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 9410 is a member of Fairchild's 9400 MACROLOGIC TTL family and is fully compatible with all TTL families.

- **EDGE TRIGGERED OUTPUT REGISTER**
- **TYPICAL ACCESS TIME OF 35 ns**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **TYPICAL POWER OF 375 mW**
- **18-PIN PACKAGE**

PIN NAMES		LOADING (Note a) HIGH	LOW
A_0-A_3	Address Inputs	0.5 U.L.	0.23 U.L.
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CS}$	Chip Select Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{WE}$	Write Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Input (Outputs Change on LOW to HIGH Transition)	0.5 U.L.	0.23 U.L.
$\overline{Q}_0$-$\overline{Q}_3$	Outputs (Active LOW)	130 U.L.	10 U.L. (Note b)

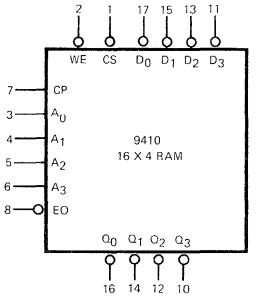
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) 10 LOW Unit Loads measured at 0.5 V.

BLOCK DIAGRAM



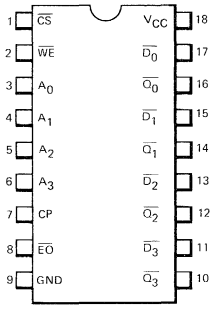
V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION

Write Operation – When the three Control Inputs: Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the Data Inputs ($\overline{D}_0$-$\overline{D}_3$) is written into the memory location selected by the Address Inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

Read Operation – Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the Address Inputs (A_0-A_3) is edge-triggered into the Output Register.

A 3-State Output Enable ($\overline{EO}$) controls the Output Buffers. When $\overline{EO}$ is HIGH the four Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the Outputs are determined by the state of the output register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = −2.0 mA; V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.2 mA; V_{CC} = MIN
V_{OL}	Output LOW Voltage	XM & XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 3 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 3 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CCH}	Supply Current			75	110	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25^\circ C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
READ MODE						
t_{PZH}	Enable Delay, Output Enable to Output		9	14	ns	Figure 2
t_{PZL}			9	14	ns	
t_{PHZ}	Disable Time, Output Enable to Output		5	8	ns	Figure 2
t_{PLZ}			5	8	ns	
t_{PLH}	Propagation Delay, Clock to Output		10	19	ns	Figure 3
t_{PHL}			11	19	ns	
t_sAR	Set-up Time to Read from Address to Clock	45	35		ns	Figure 3
t_hAR	Hold Time to Read from Address to Clock	0		0	ns	Figure 3
WRITE MODE						
t_W	Write Enable, Chip Select, or Clock Pulse Width Required to Write (Note a)	35	20		ns	Figure 4
t_sAW	Set-up Time Address to Write Enable (Note b)	5			ns	Figure 4
t_hAW	Hold Time Address to Write Enable (Note b)	0			ns	Figure 4
t_sDW	Set-up Time Data to Write Enable (Note b)	35	25		ns	Figure 4
t_hDW	Hold Time Data to Write Enable	0			ns	Figure 4

NOTES:

a) Writing occurs when $\overline{WE}$, $\overline{CE}$ and CP are LOW.
b) Assuming $\overline{WE}$ is utilized as Writing Strobe.

READ MODE AC PARAMETERS

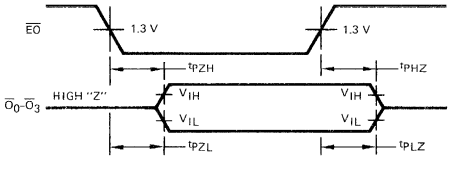
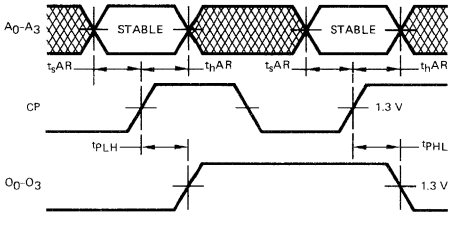


Fig. 2

PROPAGATION DELAY
OUTPUT ENABLE TO DATA OUTPUTS

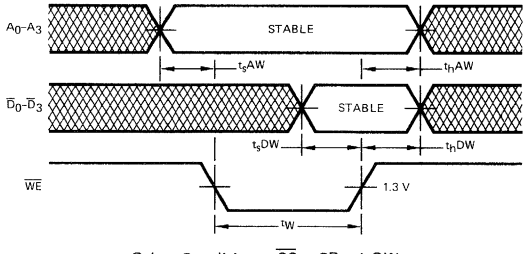


Other Conditions: $\overline{CS} = \overline{OE}$ = LOW

Fig. 3

PROPAGATION DELAY CLOCK
TO DATA OUTPUTS, AND SET-UP
AND HOLD TIMES ADDRESS TO CLOCK TO READ

WRITE MODE AC PARAMETERS

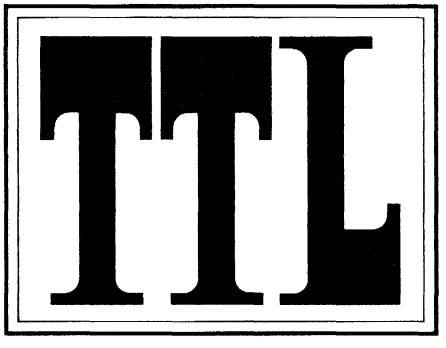


Other Conditions: $\overline{CS}$ = CP = LOW

Fig. 4

WRITE ENABLE PULSE
WIDTH, SET-UP AND HOLD
TIMES ADDRESS AND DATA TO WRITE ENABLE

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL



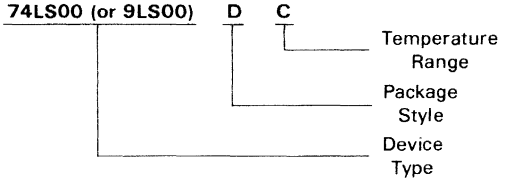
LOW POWER SCHOTTKY ORDERING INFORMATION

Fairchild digital integrated circuits may be ordered using a simplified purchasing code in which the package style and temperature range are defined below. Either the 74LS series number or the 9LS series number may be used when ordering.

TEMPERATURE RANGE
M = Military −55°C to +125°C
C = Commercial 0°C to +75°C

PACKAGE STYLE

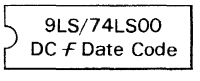
D = Dual In-Line – Ceramic (Hermetic)
P = Dual In-Line – Plastic
F = Flat Package



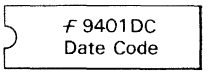
In order to accommodate varying die sizes (SSI, MSI, etc.), numbers of pins (14, 16, 24, etc.), and package outlines, a number of different package forms are required in each of the three package style categories.

The following lists indicate the specific package dimensions currently used for each device type. The detailed outline corresponding to each package code is shown at the end of this section.

LOW POWER SCHOTTKY DEVICE MARKING EXAMPLE



MACROLOGIC TTL DEVICE MARKING EXAMPLE



DEVICE	MILITARY (M) −55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS00	6A	3I	74LS00	6A	9A	3I
54LS02	6A	3I	74LS02	6A	9A	3I
54LS03	6A	3I	74LS03	6A	9A	3I
54LS04	6A	3I	74LS04	6A	9A	3I
54LS05	6A	3I	74LS05	6A	9A	3I
54LS08	6A	3I	74LS08	6A	9A	3I
54LS09	6A	3I	74LS09	6A	9A	3I
54LS10	6A	3I	74LS10	6A	9A	3I
54LS11	6A	3I	74LS11	6A	9A	3I
54LS14	6A	3I	74LS14	6A	9A	3I
54LS15	6A	3I	74LS15	6A	9A	3I
54LS20	6A	3I	74LS20	6A	9A	3I
54LS21	6A	3I	74LS21	6A	9A	3I
54LS22	6A	3I	74LS22	6A	9A	3I
54LS27	6A	3I	74LS27	6A	9A	3I

DEVICE	MILITARY (M) −55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS30	6A	3I	74LS30	6A	9A	3I
54LS32	6A	3I	74LS32	6A	9A	3I
54LS37	6A	3I	74LS37	6A	9A	3I
54LS38	6A	3I	74LS38	6A	9A	3I
54LS40	6A	3I	74LS40	6A	9A	3I
54LS42	6B	4L	74LS42	6B	9B	4L
54LS51	6A	3I	74LS51	6A	9A	3I
54LS54	6A	3I	74LS54	6A	9A	3I
54LS55	6A	3I	74LS55	6A	9A	3I
54LS73	6A	3I	74LS73	6A	9A	3I
54LS74	6A	3I	74LS74	6A	9A	3I
54LS83	6B	4L	74LS83	6B	9B	4L
54LS86	6A	3I	74LS86	6A	9A	3I
54LS90	6A	3I	74LS90	6A	9A	3I
54LS92	6A	3I	74LS92	6A	9A	3I
54LS93	6A	3I	74LS93	6A	9A	3I
54LS95	6A	3I	74LS95	6A	9A	3I
54LS109	6B	4L	74LS109	6B	9B	4L
54LS112	6B	4L	74LS112	6B	9B	4L
54LS113	6A	3I	74LS113	6A	9A	3I
54LS114	6A	3I	74LS114	6A	9A	3I
54LS125	6A	3I	74LS125	6A	9A	3I
54LS126	6A	3I	74LS126	6A	9A	3I
54LS132	6A	3I	74LS132	6A	9A	3I
54LS133	6B	4L	74LS133	6B	9B	4L
54LS136	6A	3I	74LS136	6A	9A	3I
54LS138	6B	4L	74LS138	6B	9B	4L
54LS139	6B	4L	74LS139	6B	9B	4L
54LS151	6B	4L	74LS151	6B	9B	4L
54LS152		3I	74LS152			3I
54LS153	6B	4L	74LS153	6B	9B	4L
54LS155	6B	4L	74LS155	6B	9B	4L
54LS156	6B	4L	74LS156	6B	9B	4L
54LS157	6B	4L	74LS157	6B	9B	4L
54LS158	6B	4L	74LS158	6B	9B	4L
54LS160	6B	4L	74LS160	6B	9B	4L
54LS161	6B	4L	74LS161	6B	9B	4L
54LS162	6B	4L	74LS162	6B	9B	4L
54LS163	6B	4L	74LS163	6B	9B	4L
54LS164	6A	3I	74LS164	6A	9A	3I
54LS170	6B	4L	74LS170	6B	9B	4L
54LS174	6B	4L	74LS174	6B	9B	4L
54LS175	6B	4L	74LS175	6B	9B	4L
54LS181	6N	4M	74LS181	6N	9N	4M
54LS190	6B	4L	74LS190	6B	9B	4L

DEVICE	MILITARY (M) −55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS191	6B	4L	74LS191	6B	9B	4L
54LS192	6B	4L	74LS192	6B	9B	4L
54LS193	6B	4L	74LS193	6B	9B	4L
54LS194	6B	4L	74LS194	6B	9B	4L
54LS195	6B	4L	74LS195	6B	9B	4L
54LS196	6A	3I	74LS196	6A	9A	3I
54LS197	6A	3I	74LS197	6A	9A	3I
54LS251	6B	4L	74LS251	6B	9B	4L
54LS253	6B	4L	74LS253	6B	9B	4L
54LS257	6B	4L	74LS257	6B	9B	4L
54LS258	6B	4L	74LS258	6B	9B	4L
54LS259	6B	4L	74LS259	6B	9B	4L
54LS266	6A	3I	74LS266	6A	9A	3I
54LS279	6B	4L	74LS279	6B	9B	4L
54LS283	6B	4L	74LS283	6B	9B	4L
54LS290	6A	3I	74LS290	6A	9A	3I
54LS293	6A	3I	74LS293	6A	9A	3I
54LS295	6A	3I	74LS295	6A	9A	3I
54LS298	6B	4L	74LS298	6B	9B	4L
54LS365	6B	4L	74LS365	6B	9B	4L
54LS366	6B	4L	74LS366	6B	9B	4L
54LS367	6B	4L	74LS367	6B	9B	4L
54LS368	6B	4L	74LS368	6B	9B	4L
54LS670	6B	4L	74LS670	6B	9B	4L

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9LS00	6A	3I	6A	9A	3I
9LS02	6A	3I	6A	9A	3I
9LS03	6A	3I	6A	9A	3I
9LS04	6A	3I	6A	9A	3I
9LS05	6A	3I	6A	9A	3I
9LS08	6A	3I	6A	9A	3I
9LS09	6A	3I	6A	9A	3I
9LS10	6A	3I	6A	9A	3I
9LS11	6A	3I	6A	9A	3I
9LS14	6A	3I	6A	9A	3I
9LS15	6A	3I	6A	9A	3I
9LS20	6A	3I	6A	9A	3I
9LS21	6A	3I	6A	9A	3I
9LS22	6A	3I	6A	9A	3I
9LS27	6A	3I	6A	9A	3I

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9LS30	6A	3I	6A	9A	3I
9LS32	6A	3I	6A	9A	3I
9LS37	6A	3I	6A	9A	3I
9LS38	6A	3I	6A	9A	3I
9LS40	6A	3I	6A	9A	3I
9LS42	6B	4L	6B	9B	4L
9LS51	6A	3I	6A	9A	3I
9LS54	6A	3I	6A	9A	3I
9LS55	6A	3I	6A	9A	3I
9LS73	6A	3I	6A	9A	3I
9LS74	6A	3I	6A	9A	3I
9LS83	6B	4L	6B	9B	4L
9LS86	6A	3I	6A	9A	3I
9LS90	6A	3I	6A	9A	3I
9LS92	6A	3I	6A	9A	3I
9LS93	6A	3I	6A	9A	3I
9LS95	6A	3I	6A	9A	3I
9LS109	6B	4L	6B	9B	4L
9LS112	6B	4L	6B	9B	4L
9LS113	6A	3I	6A	9A	3I
9LS114	6A	3I	6A	9A	3I
9LS125	6A	3I	6A	9A	3I
9LS126	6A	3I	6A	9A	3I
9LS132	6A	3I	6A	9A	3I
9LS133	6B	4L	6B	9B	4L
9LS136	6A	3I	6A	9A	3I
9LS138	6B	4L	6B	9B	4L
9LS139	6B	4L	6B	9B	4L
9LS151	6B	4L	6B	9B	4L
9LS152		3I			3I
9LS153	6B	4L	6B	9B	4L
9LS155	6B	4L	6B	9B	4L
9LS156	6B	4L	6B	9B	4L
9LS157	6B	4L	6B	9B	4L
9LS158	6B	4L	6B	9B	4L
9LS160	6B	4L	6B	9B	4L
9LS161	6B	4L	6B	9B	4L
9LS162	6B	4L	6B	9B	4L
9LS163	6B	4L	6B	9B	4L
9LS164	6A	3I	6A	9A	3I
9LS170	6B	4L	6B	9B	4L
9LS174	6B	4L	6B	9B	4L
9LS175	6B	4L	6B	9B	4L
9LS181	6N	4M	6N	9N	4M
9LS190	6B	4L	6B	9B	4L

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9LS191	6B	4L	6B	9B	4L
9LS192	6B	4L	6B	9B	4L
9LS193	6B	4L	6B	9B	4L
9LS194	6B	4L	6B	9B	4L
9LS195	6B	4L	6B	9B	4L
9LS196	6A	3I	6A	9A	3I
9LS197	6A	3I	6A	9A	3I
9LS251	6B	4L	6B	9B	4L
9LS253	6B	4L	6B	9B	4L
9LS257	6B	4L	6B	9B	4L
9LS258	6B	4L	6B	9B	4L
9LS259	6B	4L	6B	9B	4L
9LS266	6A	3I	6A	9A	3I
9LS279	6B	4L	6B	9B	4L
9LS283	6B	4L	6B	9B	4L
9LS290	6A	3I	6A	9A	3I
9LS293	6A	3I	6A	9A	3I
9LS295	6A	3I	6A	9A	3I
9LS298	6B	4L	6B	9B	4L
9LS365	6B	4L	6B	9B	4L
9LS366	6B	4L	6B	9B	4L
9LS367	6B	4L	6B	9B	4L
9LS368	6B	4L	6B	9B	4L
9LS670	6B	4L	6B	9B	4L
9401	7A	3I	7A	9A	3I
9403	6Q	4M	6Q	9U	4M
9404	6Q	4M	6Q	9U	4M
9405	6Q	4M	6Q	9U	4M
9406	6Q	4M	6Q	9U	4M
9407	6Q	4M	6Q	9U	4M
9410	7D		7D	9M	
96L02	6B	4L	6B	9B	4L
96S02	6B	4L	6B	9B	4L

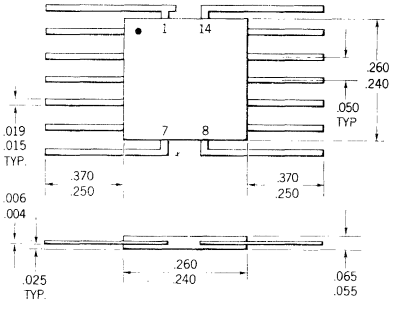
7

PACKAGE OUTLINES

FLATPAK

in accordance with JEDEC (TO-86) outline 14-Pin Cerpak

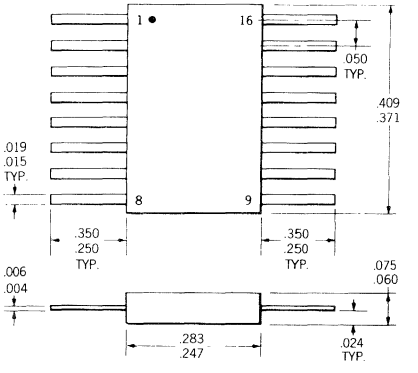
3I



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Lead 1 orientation may be either tab or dot

16-Pin Cerpak

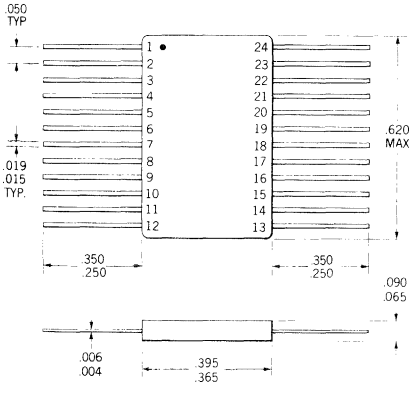
4L



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

24-Pin BeO Cerpak

4M



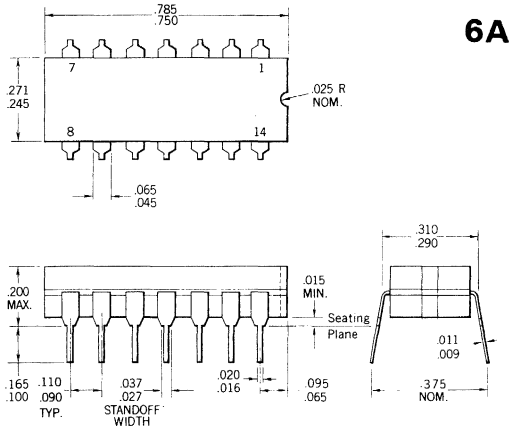
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

PACKAGE OUTLINES

DIP

in accordance with JEDEC (TO-116) outline 14-Pin Ceramic Dual In-Line

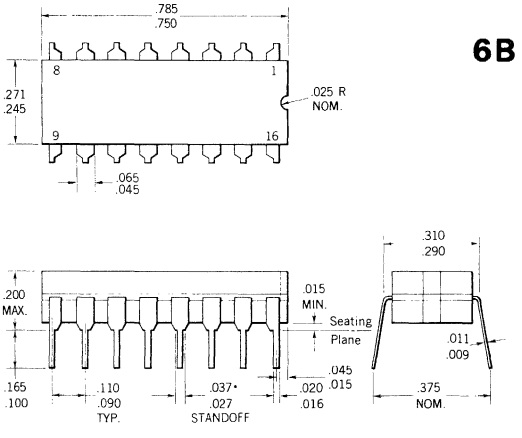
6A



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to faciliate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

16-Pin Ceramic Dual In-Line

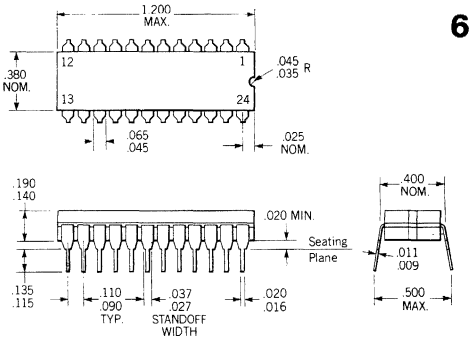
6B



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037 / .027 dimension does not apply to the corner leads

24-Pin Ceramic Dual In-Line

6Q



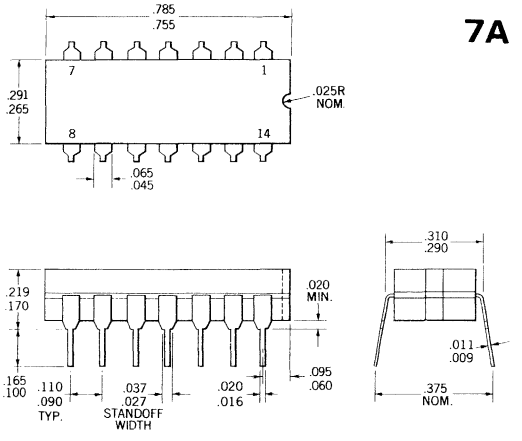
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .400" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

7

PACKAGE OUTLINES

14-Pin Ceramic Dual In-Line

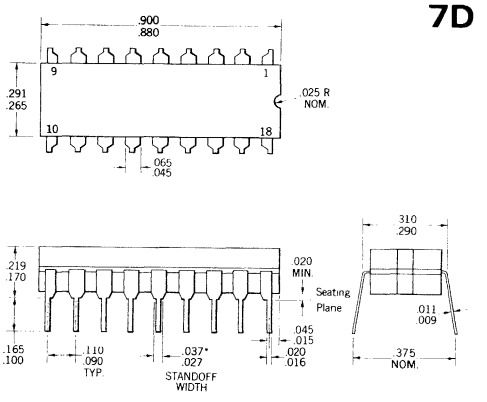
7A



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

18-Pin Ceramic Dual In-Line

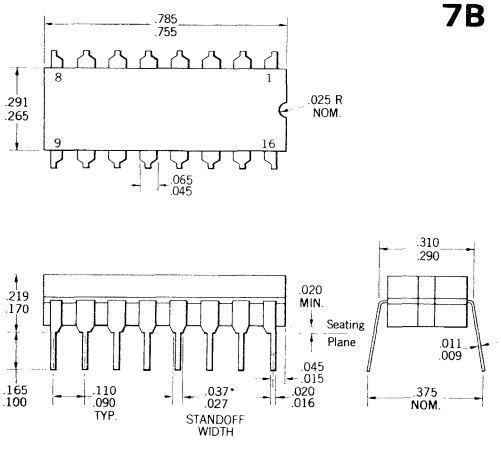
7D



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
*The .037/.027 dimension does not apply to the corner leads

16-Pin Ceramic Dual In-Line

7B

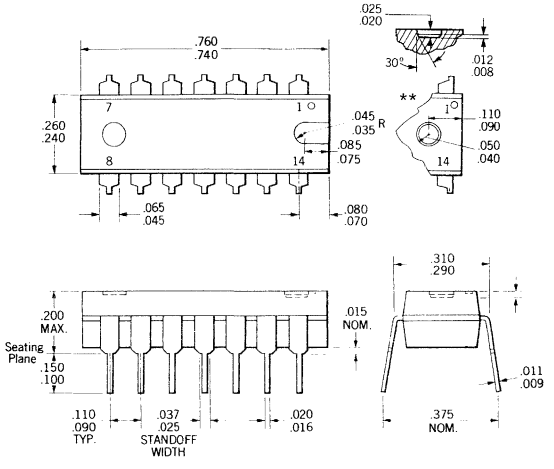


NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

PACKAGE OUTLINES

14-Pin Plastic Dual In-Line

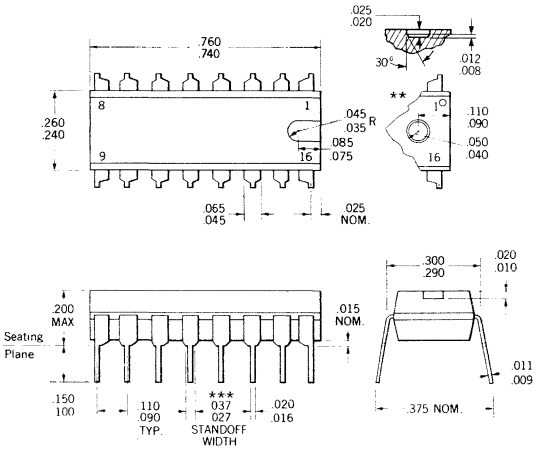
9A



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram

16-Pin Plastic Dual In-Line

9B

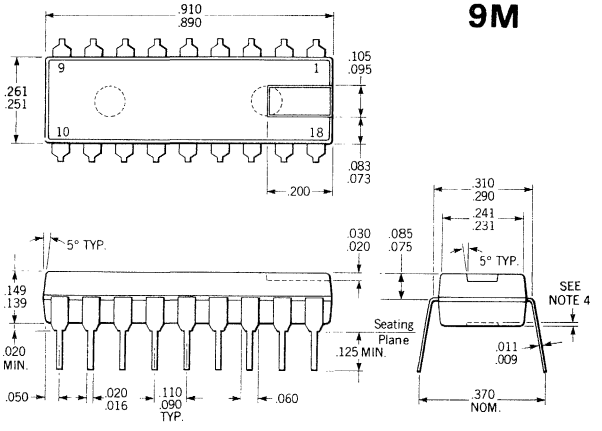


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*The .037/.027 dimensions does not apply to the corner leads

PACKAGE OUTLINES

18-Pin Plastic Dual In-Line

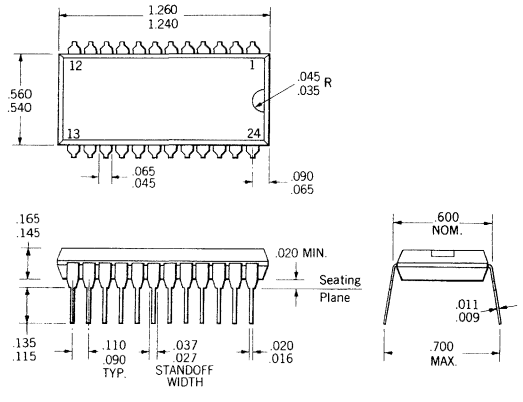
9M



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

24-Pin Plastic Dual In-Line

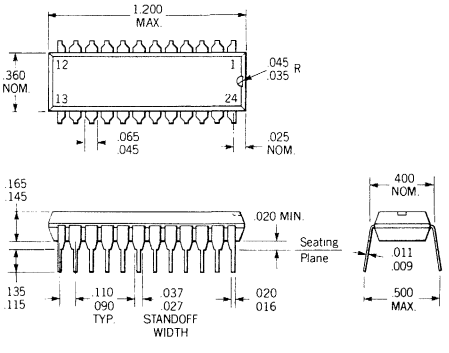
9N



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 2.7 grams

24-Pin Plastic Dual In-Line

9U



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .400" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

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O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666

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Elmhurst Industrial Park
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TWX: None — use 710-332-1201
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Kettering, Ohio 45429
Tel: 513-253-9176 TWX: 810-459-1611

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Cleveland, Ohio 44143
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