HIGH PERFORMANCE DATA BOOK

CYPRESS SEMICONDUCTOR

High Performance Data Book

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How To Use This Book

Overall Organization

This book has been organized by product type, beginning with Product Information. The products are next, starting with SRAMs, then PROMs, EPLDs, FIFOs, Logic, RISC, Modules, ECL, and bus interface products. A section containing military information is next, followed by the Design and Programming Tools section. Quality and Reliability aspects are next, then Thermal Data and Packages. Within each section, data sheets are arranged in order of part number.

Recommended Search Paths

To search by:	Use:
Product line	Table of Contents or flip through the book using the tabs on the right-hand pages.
Size	The Product Selector Guide in section 1.
Numeric part number	Numeric Device Index in section 1. The book is also arranged in order of part number.
Other manufacturer's part number	The Cross Reference Guide in section 1.
Military part number	The Military Selector Guide in section 11.

Key to Waveform Diagrams

 = Rising edge of signal will occur during this time.

 = Falling edge of signal will occur during this time.

 = Signal may transition during this time (don't care condition).

 = Signal changes from high-impedance state to valid logic level during this time.

 = Signal changes from valid logic level to high-impedance state during this time.

Abbreviations

TBD = To Be Determined
N/A = Not Applicable

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Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and was listed on the New York Stock Exchange in October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's products fall into six families: high-speed Static RAMs, PROMS, Programmable Logic Devices, Logic, ECL SRAMs and PLDs, and module products. Members of the CMOS Static RAM family include devices in densities of 64 bits to 256K, and performance from 7 ns to 35 ns. The various organizations—x1, x4, x8, and x9—provide optimal solutions for applications such as large mainframes, high-speed controllers, communications, and graphics display. Cypress's BiCMOS family of 64K and 256K SRAMs in x4 and x8 configurations offers speeds as fast as 6 ns. Cypress's cache RAMs include a 4K x 18 cache tag RAM at 10-ns match, a 32K x 9 cache RAM with a 14-ns access time, and an 64K x 18 cache RAM with a 10-ns access time.

Cypress's programmable products consist of high-speed CMOS PROMs employing an EPROM programming element and Programmable Logic Devices (PLDs) based on CMOS EPROM, CMOS FLASH, and BiCMOS Fuse technology. Like the high-speed Static RAM family, these products are the natural choice to replace older devices because they provide superior performance at one half of the power consumption. PROM densities range from 4 kilobits to 512K in byte-wide and x 16 organizations. PLD products range from 20 pins to 84 pins with performance as fast as 5-ns propagation delay and 156-MHz operational frequency. To provide immediate support for new programmable products, Cypress offers our QuickPro II™ programmer (CY3300). QuickPro II is capable of programming all of Cypress's PLDs and PROMs. It uses an IBM PC's® CPU to implement the silicon programming algorithms and interfaces to the PC via the parallel port. The use of an IBM PC as a host allows updating of the programming software using either floppy disk or modem, thereby providing instantaneous support of all new devices. Cypress also offers *Warp2*™ (CY3120), a powerful design entry synthesis and simulation tool for PLDs and state machine PROMs. *Warp2* uses the IEEE-standard (1076) VHDL design language, which is rapidly emerging as the standard language of choice for behavioral design description. Use of the VHDL language allows users the freedom to also use tools from other vendors for design simulation and synthesis. Cypress is the only programmable logic vendor offering VHDL-based design tools.

Logic products include circuits such as 4-bit and 16-bit slices, 16 x 16 multipliers and 16-bit microprogrammable ALUs, a family of 1K/2K x 8 and 4K/8K x 8 dual-port SRAMs, as well as a family of FIFOs that range from 64 x 4 to 32K x 9. Cypress also offers application-specific FIFOs such as the 2K x 9 bidirectional FIFO and the 512/2K x 9 clocked FIFO. FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed, while the results may be processed or distributed at a speed commensurate with need.

Cypress's Datacom group has developed a family of 300-MHz point-to-point transmitter/receivers. HOTLink™ is compliant with the IBM ESCON™ and Fibre Channel computer network standards, and will also have applications in military, graphics, and instrumentation systems. The Datacom group is also responsible for the Programmable Skew Clock Buffer, which allows designers to compensate for trace delays and load capacitance in high performance systems.

As a result of the acquisition of VTC's manufacturing facility in Minnesota, Cypress has created a VME Bus Interface Products group. Cypress will continue to manufacture VTC's VIC and VAC VME devices on the 0.8-micron CMOS process.

Until 1988, all Cypress products were TTL I/O–compatible. In 1989, Cypress introduced ECL products having access times (propagation delays) of less than 3.5 ns in either of the popular I/O configurations, 100K or 10K/10KH. ECL RAMs include 256 x 4, 1K x 4, and 4K x 4 families with balanced read/write cycles. The ECL PLDs are combinatorial 16P8 and 16P4 devices that can be programmed on QuickPro and other commercially available programming tools. Both the RAMs and PLDs are offered in low-power versions, reducing operating power by 30 percent while achieving 5-ns access times (RAM) and 4-ns t_{PD} (PLD).

The module family consists of both standard and custom modules incorporating circuits from the other six product families. This capability provides a fast, low-risk solution for designs requiring the ultimate in system performance and density. SRAM and FIFO module configurations are available depending on height and board real estate constraints. Modules include Single-In-Line, Dual-In-Line, Dual Single-In-line, Vertical Dual-In-Line, Quad-In-Line, and (Staggered) Zig-Zag-In-Line packages.

Situated in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota, Cypress houses R&D, design, wafer fabrication, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.1 degree Fahrenheit

tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is equally critical. Cypress manufactures 100 percent of our wafers in the United States, at our front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, our largest fab, and Cypress Minnesota, our newest fab, are both Class 1 facilities.

To improve our global competitiveness, we chose to move most of our back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site—Cypress Bangkok.

The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet—a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres—sufficient room for expansion to a number of buildings in a campus-like setting.

Manufacturing at the site since 1990 with a charter to specialize in IC packaging, the Alphatec facility has almost a century of person-years experience working for U.S. semiconductor suppliers. Thoroughly modern, MIL 883-certified, and with fully developed administrative, logistic, and manufacturing systems in place, the facility has earned an exceptional reputation for hermetic assembly and out-going quality.

Cypress San Jose maintains complete management control of Cypress Bangkok's assembly, test, mark, and ship operations within the facility, thus assuring complete continuity of San Jose's back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to it package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

As a result of the acquisition of VTC's manufacturing facility in Minnesota, Cypress has created a VME Bus Interface Products group. Cypress will continue to manufacture VTC's VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees . . . all striving to make the best CMOS, BiCMOS, and bipolar products.

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Eraseable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most advanced production processes in the world. The drive to maintain leadership in process technology has not stopped with the 0.8-micron devices. Cypress introduced a 0.65-micron process in 1991. A 0.5-micron process is currently in the works.

Although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2-, 0.8-, 0.65-, and 0.5-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching, and 100-percent stepper technology with the world's most advanced equipment.

A wholly owned subsidiary of Cypress, Aspen Semiconductor, has developed a BiCMOS technology to augment the capabilities of the Cypress CMOS processes. The new BiCMOS technology is based on the Cypress 0.8-micron CMOS process for enhanced manufacturability. Like CMOS, the process is scalable, to take advantage of finer line lithography. Where speed is critical, Cypress BiCMOS allows increased transistor performance. It also allows reduced power in the non-speed critical sections of the design to optimize the speed/power balance. The BiCMOS

process makes memories and logic operating up to 400 MHz possible.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

Ordering Information

In general, the valid ordering codes for all products (except modules and VMEbus products) follow the format below; e.g., CY7C128–45DMB, PALC16R8L–35PC

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	–25 P C	PAL 20
PAL C	16R8	L–35 P C	LOW POWER PAL 20
PAL C	22V10	–25 W C	PAL 24 VARIABLE PRODUCT TERMS
PLD C	20G10	–25 W C	GENERIC PLD 24
CY	7C330	–33 P C	PLD SYNCHRONOUS STATE MACHINE

RAM, PROM, FIFO, µP, ECL

PREFIX	DEVICE	SUFFIX	FAMILY
CY	7C128	–45 D M B	CMOS SRAM
CY	7B185	–15 V C	BiCMOS SRAM
CY	7C245	L–35 P C	PROM
CY	7C404	–25 D M B	FIFO
CY	7C9101	–30 P C	µP
CY	10E422	–3 K C	10K ECL SRAM
CY	100E422	–3 K C	100K ECL SRAM

B = BiCMOS
C = CMOS

PROCESSING

B = MIL-STD-883C FOR MILITARY PRODUCT
= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT
T = SURFACE-MOUNTED DEVICES TO BE TAPE AND REELED
R = LEVEL 2 PROCESSING ON TAPE AND REELED DEVICES

TEMPERATURE RANGE

C = COMMERCIAL (0°C TO +70°C)
I = INDUSTRIAL (–40°C TO +85°C)
M = MILITARY (–55°C TO +125°C)

PACKAGE

B = PLASTIC PIN GRID ARRAY (PPGA)
D = CERAMIC DUAL IN-LINE PACKAGE (CERDIP)/BRAZED DIP
E = TAPE AUTOMATED BONDING (TAB)
F = FLATPACK (SOLDER-SEALED FLAT PACKAGE)
G = PIN GRID ARRAY (PGA)
H = WINDOWED LEADED CHIP CARRIER
J = PLASTIC LEADED CHIP CARRIER (PLCC)
K = CERPACK (GLASS-SEALED FLAT PACKAGE)
L = LEADLESS CHIP CARRIER (LCC)
N = PLASTIC QUAD FLATPACK (PQFP)
P = PLASTIC DUAL IN-LINE (PDIP)
Q = WINDOWED LEADLESS CHIP CARRIER (LCC)
R = WINDOWED PIN GRID ARRAY (PGA)
S = SOIC (GULL WING)
T = WINDOWED CERPACK
U = CERAMIC QUAD FLATPACK (CQFP)
V = SOIC (J LEAD)
W = WINDOWED CERAMIC DUAL IN-LINE PACKAGE (CERDIP)
X = DICE (WAFFLE PACK)
Y = CERAMIC LEADED CHIP CARRIER

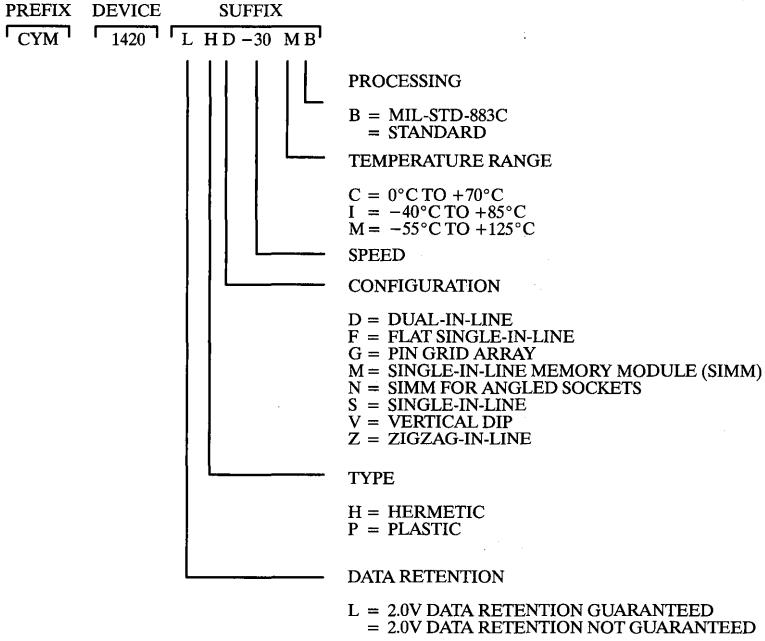
SPEED (ns or MHz)

L = LOW-POWER OPTION
A, B, C = REVISION LEVEL

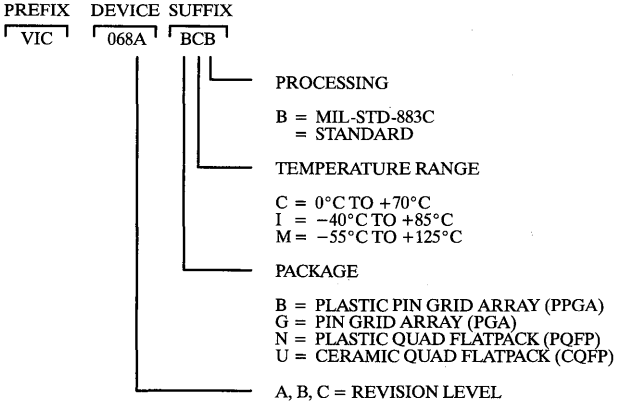
Cypress FSCM #65786

The codes for module and VMEbus products follow the the formats below.

Modules



VMEbus Products



Cypress FSCM #65786

Datasheets Available Upon Request

Datasheets listed here are not in this catalog but can be obtained from a Cypress representative.

Static RAMs (Random Access Memory)

Device Number	Description
CY2147	4096 x 1 Static R/W RAM
CY2148/CY21L48/CY2149/CY21L49	1024 x 4 Static R/W RAM
CY6116	2048 x 8 Static R/W RAM
CY6116A/CY6117A	2048 x 8 Static R/W RAM
CY7C122	256 x 4 Static R/W RAM Separate I/O
CY7C128	2048 x 8 Static R/W RAM
CY7C147	4096 x 1 Static RAM
CY7C167	16,384 x 1 Static R/W RAM
CY7C168/CY7C169	4096 x 4 Static RAM
CY7C170	4096 x 4 Static R/W RAM
CY7C171/CY7C172	4096 x 4 Static R/W RAM Separate I/O
CY7C183/CY7C184	2 x 4096 x 16 Cache RAM
CY7C186	8K x 8 Static RAM
CY7C189/CY7C190	16 x 4 Static R/W RAM
CY7C198	32K x 8 Static R/W RAM
CY74S189/CY27LS03/CY27S03/CY27S07	16 x 4 Static R/W RAM
CY93L422A/CY93422/CY93L422	256 x 4 Static R/W RAM

FIFOs

Device Number	Description
CY3341	64 x 4 Serial Memory FIFO

Logic

Device Number	Description
CY2901C	CMOS 4-Bit Slice
CY2909/11	CMOS Microprogram Sequencers
CY2910	CMOS Microprogram Controller
CY7C510	16 x 16 Multiplier Accumulator
CY7C516/7	16 x 16 Multiplier
CY7C901	CMOS 4-Bit Slice
CY7C909/11	CMOS Microprogram Sequencers
CY7C910	CMOS Microprogram Controller

Modules

Device Number	Description
CYM1240	256K x 4 Static RAM Module
CYM1422	128K x 8 Static RAM Module
CYM1423	128K x 8 Static RAM Module
CYM1460	512K x 8 Static RAM Module
CYM1461	512K x 8 Static RAM Module
CYM1466	512K x 8 Static RAM Module
CYM1540	256K x 9 Buffered Static RAM Module with Separate I/O
CYM1610	16K x 16 Static RAM Module
CYM1611	16K x 16 Static RAM Module
CYM1620	64K x 16 Static RAM Module
CYM1621	64K x 16 Static RAM Module
CYM1624	64K x 16 Static RAM Module
CYM1641	256K x 16 Static RAM Module
CYM1822	16K x 32 Static RAM Module with Separate I/O

Modules (continued)

Device Number	Description
CYM1830	64K x 32 Static RAM Module
CYM1841	256K x 32 Static RAM Module
CYM1843	256K x 32 Static RAM Module
CYM1910	16K x 68 Static RAM Module
CYM1911	16K x 68 Static RAM Module
CYM4210/CYM4220	Cascadeable 8K x 9 FIFO
CYM4241	64K x 9 FIFO
CY7M194	64K x 4 Static RAM Module
CY7M199	32K x 8 Static RAM Module

Cypress Semiconductor Bulletin Board System (BBS)

Cypress Semiconductor supports a 24-hour electronic Bulletin Board System (BBS) that allows Cypress Applications to better serve our customers by allowing them to transfer files to and from the BBS.

The BBS is set up to serve in multiple ways. One of its purposes is to allow customers to receive the most recent versions of the QuickPro programming software. Another is to allow the customers to send PLD programming files that they are having trouble with to the BBS. Cypress Applications can then find the errors in the files, correct them, and place them back on the BBS for the customer to download. The customer may also ask questions in our open forum message area. The sysop (system operator) will forward these questions to the appropriate applications engineer for an answer. The answers then get posted back into the forum. The BBS also allows the customer to communicate with their local FAE electronically, and to download both application notes and the latest versions of selected datasheets.

Communications Set-Up

The BBS is attached to a USRobotics HST Dual Standard modem capable of 14.4-Kbaud rates without compression and rates upwards of 19.2-Kbaud with compression. It is compatible with CCITT V.32 bis, V.32, V.22 (2400-baud), Bell 212A (1200-baud), CCITT V.42, and CCITT V.42 bis. It also handles MNP levels 2, 3, 4, and 5.

To call the BBS, set your communication package parameters as follows:

Baud Rate: 1200 baud to 19.2 Kbaud. Max. is determined by your modem.
Data Bits: 8
Parity: None (N)
Stop Bits: 1

In the U.S. the phone number for the BBS is (408) 943−2954. In Japan the BBS number is 81−423−69−8220. In Europe the BBS number is 49−810−62−2675. These numbers are for transmitting data only.

If the line is busy, please retry at a later time. When you access the BBS, an initial screen with the following statement will appear:

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Rybbs Bulletin Board
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After you choose the graphics format you want to use, the system will ask for your first and last name. If you are a first-time user, you will be asked a few questions for the purposes of registration. Otherwise you will be asked for your password, and then you will be logged onto the BBS, which is menu driven.

Downloading Application Notes and Datasheets

A complete listing of files that may be downloaded is included on the BBS. Application notes and selected datasheets are available for downloading in two formats, PCL and Postscript. An "hp" in front of the file name indicates it is a PCL file and can be downloaded to Hewlett-Packard LaserJets. Files without the hp preceding them are in Postscript and can be downloaded to any Postscript printer.

If you have any problems or questions regarding the BBS, please contact Cypress Applications at (408) 943−2821 (voice).

Contact a Cypress representative or use the Cypress Bulletin Board System to get copies of the application notes listed here.

General Information

I/O Characteristics of Cypress Products
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Using the CY7C361 as an Mbus Arbiter
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Glossary - '91
Glossary - '93

tatic RAMs

ize	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
4	16x4—Inverting	16	CY7C189	t_{AA} = 15, 25	55 @ 25	D, P	Now
4	16x4—Non-Inverting	16	CY7C190	t_{AA} = 15, 25	55 @ 25	L, P	Now
4	16x4—Inverting	16	CY74S189	t_{AA} = 35	90 @ 35	D, P	Now
4	16x4—Inverting	16	CY27S03A	t_{AA} = 25, 35	90 @ 25	D, P	Now
4	16x4—Non-Inverting	16	CY27S07A	t_{AA} = 25, 35	90 @ 25	D, P	Now
4	16x4—Inverting Low Power	16	CY27LS03M	t_{AA} = 65	38 @ 65	D,	Now
K	256x4	22	CY7C122	t_{AA} = 15, 25, 35	60 @ 25	D, L, P, S	Now
K	256x4	24S	CY7C123	t_{AA} = 7, 9, 10, 12, 15	120 @ 7	D, L, P, V	Now
K	256x4	22	CY9122/91L22	t_{AA} = 25, 35, 45	120 @ 25	D, P	Now
K	256x4	22	CY93422A/93L422A	t_{AA} = 35, 45, 60	80 @ 45	D, L, P	Now
K	4Kx1—CS Power-Down	18	CY7C147	t_{AA} = 25, 35, 45	80/10 @ 35	D, P	Now
K	4Kx1—CS Power-Down	18	CY2147/21L47	t_{AA} = 35, 45, 55	125/25 @ 35	D, P	Now
K	1Kx4—CS Power-Down	18	CY7C148	t_{AA} = 25, 35, 45	80/10 @ 35	D, P	Now
K	1Kx4—CS Power-Down	18	CY2148/21L48	t_{AA} = 35, 45, 55	120/20 @ 35	D, P	Now
K	1Kx4	18	CY7C149	t_{AA} = 25, 35, 45	80 @ 35	D, L, P	Now
K	1Kx4	18	CY2149/21L49	t_{AA} = 35, 45, 55	120 @ 35	D, P	Now
K	1Kx4—Separate I/O, Reset	24S	CY7C150	t_{AA} = 10, 12, 15, 25, 35	90 @ 12	D, P, S	Now
K	1Kx8—Dual Port Master	48	CY7C130	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, L, P	Now
K	1Kx8—Dual Port Slave	48	CY7C140	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, L, P	Now
K	1Kx8—Dual Port Master	52	CY7C131	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N	Now
K	1Kx8—Dual Port Slave	52	CY7C141	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N	Now
6K	2Kx8—CS Power-Down	24	CY7C128A	t_{AA} = 15, 20, 25, 35, 45, 55	90/20 @ 55	D, L, P, V	Now
6K	2Kx8—CS Power-Down	24	CY6116A	t_{AA} = 20, 25, 35, 45, 55	80/20 @ 55	D, L	Now
6K	2Kx8—CS Power-Down	32	CY6117A	t_{AA} = 20, 25, 35, 45, 55	80/20 @ 55	L	Now
6K	16Kx1—CS Power-Down	20	CY7C167A	t_{AA} = 15, 20, 25, 35, 45	50/15 @ 45	D, P, V	Now
6K	4Kx4—CS Power-Down	20	CY7C168A	t_{AA} = 15, 20, 25, 35, 45	70/15 @ 45	D, P, V	Now
6K	4Kx4	20	CY7C169A	t_{AA} = 15, 20, 25, 35, 45	70 @ 45	P, V	Now
6K	4Kx4—Output Enable	22S	CY7C170A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	D, P, V	Now
6K	4Kx4—Separate I/O	24S	CY7C171A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P, V	Now
6K	4Kx4—Separate I/O	24S	CY7C172A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P, V	Now
6K	2Kx8—Dual Port Master	48	CY7C132	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, L, P	Now
6K	2Kx8—Dual Port Slave	48	CY7C142	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, L, P	Now
6K	2Kx8—Dual Port Master	52	CY7C136	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N	Now
6K	2Kx8—Dual Port Slave	52	CY7C146	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N	Now
2K	4Kx8—Dual Port, No Arbitration	48	CY7B134	t_{AA} = 20, 25, 35	240	D, L, P	Now
2K	4Kx8—Dual Port, w/Semaph	52	CY7B1342	t_{AA} = 20, 25, 35	240	J, L	Now
2K	4Kx8—Dual Port, No Arbitration	52	CY7B135	t_{AA} = 20, 25, 35	240	J, L	Now
2K	4Kx8—Dual Port, w/ Semaph, Busy, Int	68	CY7B138	t_{AA} = 15, 25, 35	260	G, J, L	Now
2K	4Kx9—Dual Port, w/ Semaph, Busy, Int	68	CY7B139	t_{AA} = 15, 25, 35	260	G, J, L	Now
4K	8Kx8—Dual Port, w/ Semaph, Busy, Int	68	CY7B144	t_{AA} = 15, 25, 35	260	G, J, L	Now
4K	8Kx9—Dual Port, w/ Semaph, Busy, Int	68	CY7B145	t_{AA} = 15, 25, 35	260	G, J, L	Now
4K	8Kx8—CS Power-Down	28S	CY7B185	t_{AA} = 9, 10, 12, 15	150/50 @ 9	D, P, V	Now
4K	8Kx8—CS Power-Down	28S	CY7C185	t_{AA} = 15, 20, 25, 35, 45	120/20 @ 15	P, V	Now
4K	8Kx8—CS Power-Down	28S	CY7C185A	t_{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L	Now
4K	8Kx8—CS Power-Down	28	CY7C186A	t_{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L	Now
4K	8Kx8—CS Power-Down	28	CY7C186	t_{AA} = 20, 25, 35, 45	120/20 @ 15	P	Now
4K	64Kx1—CS Power-Down	22S	CY7C187A	t_{AA} = 15, 20, 25, 35, 45	80/40 @ 25	D, L	Now
4K	64Kx1—CS Power-Down	22S	CY7C187	t_{AA} = 15, 20, 25, 35, 45	90/40 @ 15	P, V	Now
4K	16Kx4—CS Power-Down	22S	CY7B164	t_{AA} = 8, 10, 12	140/50 @ 8	D, P, V	Now
4K	16Kx4—CS Power-Down	22S	CY7C164	t_{AA} = 15, 20, 25, 35, 45	115/40 @ 15	P, V	Now
4K	16Kx4—Output Enable	24S	CY7B166	t_{AA} = 8, 10, 12	140/50 @ 8	D, P, V	Now
4K	16Kx4—Output Enable	24S	CY7C166	t_{AA} = 15, 20, 25, 35, 45	115/40 @ 15	P, V	Now
4K	16Kx4—Separate I/O, Transparent Write	28S	CY7B161	t_{AA} = 8, 10, 12	140/50 @ 8	D, P, V	Now
4K	16Kx4—Separate I/O	28S	CY7B162	t_{AA} = 8, 10, 12	140/50 @ 8	D, P, V	Now
4K	16Kx4—Separate I/O, Transparent Write	28S	CY7C161	t_{AA} = 15, 20, 25, 35, 45	115/40 @ 15	P, V	Now

Static RAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
64K	16K x 4—Separate I/O	28S	CY7C162	t_{AA} = 15, 20, 25, 35, 45	115/40 @ 15	P, V	Now
64K	16K x 4—Separate I/O, Transparent Write	28S	CY7C161A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L	Now
64K	16K x 4—Separate I/O	28S	CY7C162A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L	Now
64K	16K x 4—CS Power-Down	22S	CY7C164A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L	Now
64K	16K x 4—Output Enable	24S	CY7C166A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L	Now
72K	8K x 9	28S	CY7C182	t_{AA} = 25, 35, 45, 55	140/35 @ 25	P, V	Now
72K	4K x 18—Cache Tag, Multiprocessing	68	CY7B180	t_{MATCH} = 10, 12, 15, 20	340 @ 10	J, N	Now
72K	4K x 18—Cache Tag, Uniprocessing	68	CY7B181	t_{MATCH} = 10, 12, 15, 20	340 @ 10	J, N	Now
128K	8K x 16—Addresses Latched except A12	52	CY7C183	t_{AA} = 25, 35, 45	220 @ 25	J	Now
128K	8K x 16—Addresses Latched	52	CY7C184	t_{AA} = 25, 35, 45	220 @ 25	J	Now
256K	16K x 16—SPARC Cache RAM	52	CY7C157	t_{AA} = 18, 20, 24, 33	250	J	Now
256K	32K x 8—CS Power-Down	28	CY7C198	t_{AA} = 25, 35, 45	160/35 @ 25	D, L, P	Now
256K	32K x 8—CS Power-Down	28S	CY7C199	t_{AA} = 12, 15, 20, 25, 35, 45, 55	170/30 @ 25	D, L, P, V	Now
256K	32K x 8—CS Power-Down	28S	CY7B199	t_{AA} = 10, 12	185/30 @ 10	D, P, V	Now
256K	32K x 8—CS Power-Down (3.3V)	28S	CY7C1399	t_{AA} = 20, 25, 35	60/25 @ 20	P, V	Q393
256K	64K x 4—CS Power-Down	24S	CY7C194	t_{AA} = 12, 15, 20, 25, 35, 45	160/30 @ 25	D, L, P, V	Now
256K	64K x 4—CS Power Down with OE	28S	CY7C196	t_{AA} = 12, 15, 20, 25, 35, 45	160/30 @ 25	D, L, P, V	Now
256K	64K x 4—Separate I/O, Transparent Write	28S	CY7C191	t_{AA} = 12, 15, 20, 25, 35, 45	120/30 @ 25	D, P, V	Now
256K	64K x 4—Separate I/O	28S	CY7C192	t_{AA} = 12, 15, 20, 25, 35, 45	120/30 @ 25	D, L, P, V	Now
256K	64K x 4—Separate I/O, Transparent Write	28S	CY7B191	t_{AA} = 10, 12	170/30 @ 10	D, P, V	Now
256K	64K x 4—Separate I/O	28S	CY7B192	t_{AA} = 10, 12	170/30 @ 10	D, P, V	Now
256K	64K x 4—CS Power-Down	24S	CY7B194	t_{AA} = 10, 12	170/30 @ 10	D, P, V	Now
256K	64K x 4—CS Power-Down w/ OE	28S	CY7B195	t_{AA} = 10, 12	170/30 @ 10	D, P, V	Now
256K	64K x 4—CS Power-Down w/ OE, Second CS	28S	CY7B196	t_{AA} = 10, 12	170/30 @ 10	D, P, V	Now
256K	64K x 4—CS Power-Down w/ OE	28S	CY7C195	t_{AA} = 12, 15, 20, 25, 35	160/30 @ 25	D, L, P, V	Now
256K	256K x 1—CS Power-Down	24S	CY7B197	t_{AA} = 10, 12	140/30 @ 10	D, P, V	Now
256K	256K x 1—CS Power-Down	24S	CY7C197	t_{AA} = 12, 15, 20, 25, 35, 45	105/30 @ 25	D, P, V	Now
288K	32K x 9—CS Power-Down	32S	CY7C188	t_{AA} = 12, 15, 20, 25, 35	160/40 @ 12	P, V	Q194
288K	32K x 9—CS Power-Down (3.3V)	32S	CY7C1388	t_{AA} = 20, 25, 35	60/40 @ 20	P, V	Q194
1M	64K x 18—Burst	52	CY7C1031	t_{AA} = 10, 12, 14 (@ 85 pF)	265 @ 10	J	Q393
1M	64K x 18—Burst	52	CY7C1032	t_{AA} = 10, 12, 14 (@ 85 pF)	265 @ 10	J	Q393
1M	64K x 18—Burst (3.3V)	52	CY7C1331	t_{AA} = 14, 18, 21 (@ 85 pF)	180 @ 14	J	Q493
1M	64K x 18—Burst (3.3V)	52	CY7C1332	t_{AA} = 14, 18, 21 (@ 85 pF)	180 @ 14	J	Q493
1M	128K x 8—CS Power-Down	32	CY7C1009	t_{AA} = 12, 15, 20, 25	185 @ 12	D, L, P, V	Q493
1M	128K x 8—CS Power-Down	32	CY7C109A	t_{AA} = 12, 15, 20, 25, 35	185 @ 12	D, L, P, V	Q194
1M	256K x 4—CS Power-Down	28	CY7C1006	t_{AA} = 12, 15, 20, 25	165 @ 12	D, P, V	Q493
1M	256K x 4—CS Power-Down w/ OE	28	CY7C106A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, P, V	Q493
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C1001	t_{AA} = 12, 15, 20, 25	165 @ 12	D, P, V	Q493
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C101A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, L, P, V	Q493
1M	256K x 4—Separate I/O	32	CY7C1002	t_{AA} = 12, 15, 20, 25	165 @ 12	D, L, P, V	Q493
1M	256K x 4—Separate I/O	32	CY7C102A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, L, P, V	Q493
1M	1M x 1—CS Power-Down	28	CY7C1007	t_{AA} = 12, 15, 20, 25	150 @ 12	D, L, P, V	Q493
1M	1M x 1—CS Power-Down	28	CY7C107A	t_{AA} = 12, 15, 20, 25, 35	150 @ 12	D, L, P, V	Q493

ECL SRAMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{EE}	Packages	Availability
1K	256 x 4—10K/10 KH	24.4	CY10E422	t_{AA} = 4, 5	220	D, K, L	Now
1K	256 x 4—10K/10 KH	24.4	CY10E422L	t_{AA} = 5, 7	150	D, J, K, L	Now
1K	256 x 4—100K	24.4	CY100E422	t_{AA} = 3.5, 5	220	D, K, L	Now
1K	256 x 4—100K	24.4	CY100E422L	t_{AA} = 5, 7	150	D, J, K, L	Now

CL SRAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{EE}	Packages	Availability
K	4Kx1—10K	18.3	CY10E470	t_{AA} = 5, 7	200	D	Now
K	4Kx1—100K	18.3	CY100E470	t_{AA} = 5, 7	200	D	Now
K	1024x4—10K/10 KH	24.4	CY10E474	t_{AA} = 4,5	275	D, K, L	Now
K	1024x4—10K/10 KH	24.4	CY10E474L	t_{AA} = 5,7	190	D, J, K, L	Now
K	1024x4—100K	24.4	CY100E474	t_{AA} = 3.5,5	275	D, K, L	Now
K	1024x4—100K	24.4	CY100E474L	t_{AA} = 5,7	190	D, J, K, L	Now
6K	4Kx4—10K/10KH	28.4	CY10E484	t_{AA} = 4,5	320	D, K, Y	Now
6K	4Kx4—10K/10KH	28.4	CY10E484L	t_{AA} = 7, 10	200	D, J, K, V	Now
6K	4Kx4—100K	28.4	CY100E484	t_{AA} = 4,5	320	D, K, V, Y	Now
6K	4Kx4—100K	28.4	CY100E484L	t_{AA} = 7, 10	200	D, J, K, V	Now
6K	4Kx4—100K	28.4	CY101E484	t_{AA} = 4,5	320	D, K, Y	Now
6K	4Kx4—100K	28.4	CY101E484L	t_{AA} = 7,10	200	D, J, K, V	Now

RAM Modules

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
12K	16Kx32—JEDEC	64	CYM1821	t_{AA} = 12, 15 t_{AA} = 20, 25, 30, 35, 45	960@12 720@25	PM, PZ PM, PZ	Now Now
68K	32Kx24	56	CYM1720	t_{AA} = 15, 20, 25, 30, 35	330@25	PZ	Now
M	32Kx32	66	CYM1828	t_{AA} = 25, 30, 35, 45, 55, 70	400@45	HG	Now
M	64Kx16	40	CYM1622	t_{AA} = 25, 30, 35, 45	400@25	PV	Now
M	i486 Secondary Cache	128	CYM7485	t_{freq} = 33 MHz	1500	PM	Now
.5M	64Kx24	56	CYM1730	t_{AA} = 25, 30, 35	510@25	PZ	Now
M	256Kx8—JEDEC	60	CYM1441	t_{AA} = 25, 35, 45	960@25	PZ	Now
M	64Kx32	60	CYM1830	t_{AA} = 25, 30, 35, 45, 55	880@25	HD	Now
M	64Kx32—JEDEC	64	CYM1831	t_{AA} = 20, 25, 30, 35, 45	720@20	PM, PN, PZ	Now
M	64Kx32	60	CYM1832	t_{AA} = 25, 35, 45, 55	980@25	PZ	Now
M	512Kx8—JEDEC	32	CYM1464	t_{AA} = 20, 25, 30, 35, 45, 55, 70	300@35	PD	Now
M	512Kx8—JEDEC	32	CYM1465	t_{AA} = 70, 85, 100, 120, 150	110@85	PD	Now
M	128Kx32	64	CYM1836	t_{AA} = 20, 25, 30, 35, 45	480@20	PM, PZ	Now
M	128Kx32	66	CYM1838	t_{AA} = 25, 30, 35	720@25	HG	Now
M	256Kx32	60	CYM1840	t_{AA} = 20, 25, 30, 35, 45, 55	1120@25	PD	Now
M	256Kx32—JEDEC	64	CYM1841	t_{AA} = 20, 25, 30, 35, 45, 55	960@25	PM, PN, PZ	Now
M	1Mx8	36	CYM1471	t_{AA} = 85, 100, 120	110@85	PS	Now
M	1Mx9	44	CYM1560	t_{AA} = 30, 35, 45	1200@30	PS	Now
6M	2Mx8	36	CYM1481	t_{AA} = 85, 100, 120	110@85	PF, PS	Now
2M	1Mx32	72	CYM1851	t_{AA} = 25, 30, 35	1250@30	PM, PN, PZ	Now

ROMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA@ns)	Packages	Availability
K	512x8—Registered	24S	CY7C225	$t_{SA/CO}$ = 25/12, 30/15, 35/20, 40/25	90	D, J, L, P	Now
K	512x8—Registered	24S	CY7C225A	$t_{SA/CO}$ = 25/12, 30/15, 35/20, 40/25	90	D, J, L, P	Q393
K	1024x8—Registered	24S	CY7C235	$t_{SA/CO}$ = 25/12, 30/15, 40/20	90	D, J, K, L, P	Now
K	1024x8—Registered	24S	CY7C235A	$t_{SA/CO}$ = 25/12, 30/15, 40/20	90	D, J, K, L, P	Q393
K	1Kx8	24S	CY7C281	t_{AA} = 30, 45	90@45, 100@30	D, J, K, P	Now
K	1Kx8	24S	CY7C281A	t_{AA} = 30, 45	90@45, 100@30	D, J, K, P	Q393
K	1Kx8	24	CY7C282	t_{AA} = 30, 45	90@45, 100@30	D, P	Now
K	1Kx8	24	CY7C282A	t_{AA} = 30, 45	90@45, 100@30	D, P	Q393
6K	2Kx8—Registered	24S	CY7C245/L	$t_{SA/CO}$ = 25/12, 35/15, 45/25	90, 60	D, J, L, P, Q, S, T, W	Now
6K	2Kx8—Registered	24S	CY7C245A/L	$t_{SA/CO}$ = 15/10, 25/12, 35/15 45/25	120@15, 90, 60@25	D, J, L, P, Q, S, T, W	Now
6K	2Kx8	24S	CY7C291/L	t_{AA} = 35, 50	90, 60	D, J, L, P, Q, S, T, W	Now

PROMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
16K	2Kx8	24S	CY7C291A/L	t_{AA} = 20, 25, 35, 50	120 @ 20, 90, 60 @ 25	D, J, L, P, Q, S, T, W	Now
16K	2Kx8	24	CY7C292/L	t_{AA} = 35, 50	90, 60	D, P	Now
16K	2Kx8	24	CY7C292A/L	t_{AA} = 20, 25, 35, 50	120 @ 20, 90 @ 25, 90, 60 @ 35	D, P	Now
16K	2Kx8—CS Power-Down	24S	CY7C293A/L	t_{AA} = 20, 25, 35, 50	120/40 @ 20, 90/30 @ 25 60/15 @ 35	D, L, Q, P, W	Now
32K	2Kx16—Reprogrammable State Machine Prom	28S	CY7C258	t_{AA} = 10, 12, 15	170	H, J, L, P, Q, W	Now
32K	2Kx16—Reprogrammable State Machine Prom	44	CY7C259	t_{AA} = 10, 12, 15	170	H, J, L, Q	Now
64K	8Kx8—CS Power-Down	24S	CY7C261	t_{AA} = 20, 25, 35, 45, 55	120/40 @ 20, 100/30 @ 35	D, J, L, P, Q, T, W	Now
64K	8Kx8	24S	CY7C263	t_{AA} = 20, 25, 35, 45, 55	120 @ 20, 100 @ 35	D, J, L, P, Q, T, W	Now
64K	8Kx8	24	CY7C264	t_{AA} = 20, 25, 35, 45, 55	120 @ 20, 100 @ 35	D, P, W	Now
64K	8Kx8—Registered	28S	CY7C265	$t_{SA/CO}$ = 15/12, 25/15, 40/20 50/25	120 @ 15, 100 @ 40 80 @ 50	D, J, L, P, Q, W	Now
64K	8Kx8—EPROM Pinout	28	CY7C266	t_{AA} = 20, 25, 35, 45	120/15 @ 20, 100/15 @ 35	D, L, P, Q, W	Now
64K	8Kx8—Registered, Diagnostic	28S	CY7C269	$t_{SA/CO}$ = 15/12, 25/15, 40/20, 50/25	120 @ 15, 100 @ 40, 80 @ 50	D, J, L, P, Q, W	Now
128K	16Kx8—CS Power-Down	28S	CY7C251	t_{AA} = 45, 55, 65	100/30	D, L, P, Q, W	Now
128K	16Kx8	28	CY7C254	t_{AA} = 45, 55, 65	100/30	D, P, Q, W	Now
256K	32Kx8—Asynchronous	28	CY7C256	t_{AA} = 45, 55	95	D, J, P, W	Q493
256K	Processor-Intelligent PROM	44	CY7C270	$t_{AA/CKB}$ = 25/11, 28/12, 35/15	175	H, J, Q	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	t_{AA} = 30, 35, 45, 55	120/30	D, J, K, L, P, Q, T, W	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	t_{AA} = 30, 35, 45, 55	120/30	D, J, K L, P, Q, T, W	Now
256K	32Kx8—Registered	28S	CY7C277	$t_{SA/CO}$ = 30/15, 40/20, 50/25	120	D, J, K L, P, Q, T, W	Now
256K	16Kx16	44	CY7C276	t_{AA} = 25, 30, 35	175	H, J, Q	Now
256K	32Kx8—Register/Latch	28S	CY7C279	t_{AA} = 35, 45, 55	120	J, W	Now
512K	64Kx8	28	CY7C286	t_{AA} = 50, 60, 70, 80	120/40 @ 50, 90/30 @ 70	D, L, P, Q, W	Now
512K	64Kx8—Registered	28S	CY7C287	$t_{AS/CO}$ = 45/15, 55/20, 65/25	120	D, L, P, Q, W	Now
512K	64Kx8 with ALE	28S	CY7C285	t_{AA} = 65/20, 75/25, 85/35	180	D, L, P, Q, W	Now

PLDs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
PAL20	16L8	20	PAL16L8	t_{PD} = 4.5/5/7	180	D, J, P	Now
PAL20	16R8	20	PAL16R8	$t_{S/CO}$ = 2.5/4.5, 2.5/5, 3.5/6	180	D, J, P	Now
PAL20	16R6	20	PAL16R6	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, P	Now
PAL20	16R4	20	PAL16R4	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, P	Now
PAL20	16L8	20	PALC16L8/L	t_{PD} = 20	70, 45	D, L, P, Q, V, W	Now
PAL20	16R8	20	PALC16R8/L	$t_{S/CO}$ = 15/12	70, 45	D, L, P, Q, V, W	Now
PAL20	16R6	20	PALC16R6/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
PAL20	16R4	20	PALC16R4/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
PLD20	18G8—Generic	20	PLDC18G8	$t_{PD/S/CO}$ = 12/8/10	90/70	D, J, L, P, Q, V, W	Now

LDs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
'LD24	22V10—Macrocell	24S	PALC22V10/L	$t_{PD/S/CO}$ = 25/15/15, 20/12/12	90, 55	D, J, K, L, P, Q, W	Now
'LD24	22V10—Macrocell	24S	PALC22V10B	$t_{PD/S/CO}$ = 15/10/10	90	D, H, J, K, L, P, Q, W	Now
'LD24	22V10—Macrocell	24S	PAL22V10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P	Now
'LD24	22VP10—Macrocell	24S	PAL22VP10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P	Now
'AL24	22V10—Macrocell	24	PALC22V10D	t_{PD} = 7.5, 10, 15	130/90/90	D, J, L, P	Now
LD24	20G10—Generic	24S	PLDC20G10	$t_{PD/S/CO}$ = 25/15/15	55	D, J, L, P, Q, W	Now
LD24	20G10—Generic	24S	PLDC20G10B	$t_{PD/S/CO}$ = 15/12/10	70	D, H, J, L, P, Q, W	Now
LDB24	20G10—Generic	24S	PLD20G10C	$t_{PD/S/CO}$ = 7.5/3/6.5, 10/3.6/7.5	190	D, J, L, P	Now
LD24	20RA10—Asynchronous	24S	PLD20RA10	$t_{PD/S/CO}$ = 15/10/15	80	D, H, J, L, P, Q, W	Now
LD24	7B326—16 Macrocell	24S	PLD610	t_{PD} = 10	130	D, J, K, L, P, Y	Now
LD28	7C330—State Machine	28S	CY7C330	$f_{MAX.}$, t_{IS}, t_{CO} = 66 MHz/3ns/12ns	130 @ 50 MHz	D, H, J, L, P, Q, W	Now
LD28	7C331—Asynchronous, Registered	28S	CY7C331	$t_{PD/S/CO}$ = 20/12/20	120@25 ns	D, H, J, L, P, Q, W	Now
LD28	7C332—Input Registered, Combinatorial	28S	CY7C332	t_{PD} = 15	120@20ns	D, H, J, L, P, Q, W	Now
LD28	7B333B—16 Macrocell	28S	CY7B333B	$t_{PD/S/CO}$ = 10/8/8	130	D, J, K, L, P, Y	Now
LD28	7C335—Universal Synchronous	28S	CY7C335	f_{MAX}/t_{IS} = 100 MHz/2ns, 83 MHz/2ns	140	D, H, J, L, P, Q, W	Now
LD28	7C361—32-Macrocell State Machine	28S	CY7C361	f_{MAX} = 125 MHz	140	D, H, J, L, P, Q, W	Now
'AX28	7C344—32 Macrocell	28S	CY7C344	$t_{PD/S/CO}$ = 20/12/12	200/150	D, H, J, L, P, Q, W	Now
'AX44	7C343—64 Macrocell	44	CY7C343	$t_{PD/S/CO}$ = 20/12/12	135/125	H, J	Now
'AX68	7C342—128 Macrocell	68	CY7C342/B	$t_{PD/S/CO}$ = 25/15/14, 15/10/10	250/225	G, H, J, L, R	Now
'AX84	7C341—192 Macrocell	84	CY7C341/B	$t_{PD/S/CO}$ = 25/20/16, 15/10/10	380/360	H, J	Now
7X-44	7C371—32-Macrocell Flash CPLD	44S	CY7C371	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/7.5 ns/7.5 ns	150/TBD	J	Q393
7X-44	7C372—64-Macrocell Flash CPLD	44S	CY7C372	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/9 ns/9 ns	180/TBD	J	Q493
7X-84	7C373—64-Macrocell Flash CPLD	84S	CY7C373	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/9 ns/9 ns	180/TBD	J	Q493
7X-84	7C374—128-Macrocell Flash CPLD	84S	CY7C374	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/9 ns/9 ns	300/TBD	J	Q393
7X-164	7C375—128-Macrocell Flash CPLD	164S	CY7C375	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/9 ns/9 ns	300/TBD	N	Q393
ASIC-1	CMOS 1K Gate FPGA	68S	CY7C382	−0, −1, −2	I_{SB} = 10	J	Q293
ASIC-2	CMOS 2K Gate FPGA	84S	CY7C384	−0, −1, −2	I_{SB} = 10	J	Q293
ASIC-4	CMOS 4K Gate FPGA	84S	CY7C385	−0, −1, −2	I_{SB} = 10	J	Q493
ASIC-4	CMOS 4K Gate FPGA	144S	CY7C386	−0, −1, −2	I_{SB} = 10	N	Q293

CL PLDs

Organization	Pins	Part Number	Speed (ns)	I_{EE} (mA @ ns)	Packages	Availability
6P8—10 KH	24	CY10E301	t_{PD} = 4	240	D, Y	Now
6P8—10 KH	24	CY10E301L	t_{PD} = 6	170	J, P	Now
6P8—100K	24	CY100E301	t_{PD} = 4	240	D, Y	Now
6P8—100K	24	CY100E301L	t_{PD} = 6	170	J, P	Now
6P4—10 KH	24	CY10E302	t_{PD} = 3, 4	220	D, Y	Now
6P4—10 KH	24	CY10E302L	t_{PD} = 4	170	J, P	Now
6P4—100K	24	CY100E302	t_{PD} = 3, 4	220	D, Y	Now
6P4—100K	24	CY100E302L	t_{PD} = 4	170	J, P	Now

FIFOs

Organization	Pins	Part Number	Speed	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
64x4	16	CY3341	1.2, 2 MHz	45	D, P	Now
64x4	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P	Now
64x4—w/OE	16	CY7C403	10, 15, 25 MHz	75	D, L, P	Now
64x5	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P	Now
64x5—w/OE	18	CY7C404	10, 15, 25 MHz	75	D, L, P	Now
64x8—w/OE and Almost Flags	28S	CY7C408A	15, 25, 35 MHz	120	D, L, P, V	Now
64x9—w/Almost Flags	28S	CY7C409A	15, 25, 35 MHz	120	D, L, P, V	Now
512x9—w/Half Full Flag	28	CY7C420	20, 25, 30, 40, 65	142/30	D, P	Now
512x9—w/Half Full Flag	28S	CY7C421	20, 25, 30, 40, 65	142/30	D, J, L, P, V	Now
512x9—w/Half Full Flag	28S	CY7C421A	10, 15	180	J, P	Now
512 x 9—Clocked	28S	CY7C441	14, 20, 30*	180	D, J, L, P, V	Now
512 x 9—Clocked w/ Prog. Flags	32	CY7C451	14, 20, 30*	180	D, J, L	Now
512x18—Clocked w/Prog. Flags	48	CY7C445	14, 20, 30*	120	P, D	Q194
512x18—Clocked w/Prog. Flags	52	CY7C455	14, 20, 30*	120	J, L	Now
1Kx9—w/ Half Full Flag	28	CY7C424	20, 25, 30, 40, 65	142/30	D, P	Now
1Kx9—w/ Half Full Flag	28S	CY7C425	20, 25, 30, 40, 65	142/30	D, J, L, P	Now
1Kx9—w/ Half Full Flag	28S	CY7C425A	10, 15	180	J, P	Now
1Kx18—Clocked w/Prog. Flags	48	CY7C446	14, 20, 30*	120	D, P	Q194
1Kx18—Clocked w/Prog. Flags	52	CY7C456	14, 20, 30*	120	J, L	Now
2Kx9—w/ Half Full Flag	28	CY7C428	20, 25, 30, 40, 65	142/30	D, P	Now
2Kx9—w/ Half Full Flag	28S	CY7C429	20, 25, 30, 40, 65	142/30	D, J, L, P, V	Now
2Kx9—w/ Half Full Flag	28S	CY7C429A	10, 15	180	J, P	Now
2Kx9—Bidirectional	28S	CY7C439	30, 40, 65	140/40	D, J, L, P, V	Now
2K x 9—Clocked	28S	CY7C443	14, 20, 30*	180	D, J, L, P, V	Now
2K x 9—Clocked w/ Prog. Flags	32	CY7C453	14, 20, 30*	180	D, J, L	Now
2Kx18—Clocked w/Prog. Flags	48	CY7C447	14, 20, 30*	120	D, P	Q194
2Kx18—Clocked w/Prog. Flags	52	CY7C457	14, 20, 30*	120	J, L	Now
4Kx9—w/ Half Full Flag	28	CY7C432	25, 30, 40, 65	142/25	D, P	Now
4Kx9—w/Half Full Flag	28S	CY7C433	25, 30, 40, 65	142/25	D, J, L, P, V	Now
4Kx9—w/Half Full Flag	28S	CY7C433A	10, 15	180	J, P	Now
8K x 9—Module	28	CYM4210	30, 40, 50, 65	540/120	HD	Now
8K x 9—w/ Half Full Flag	28	CY7C460	15, 25, 40	180	D, J, L, P	Now
8K x 9—w/ Prog. Flags	28	CY7C470	15, 25, 40	180	D, J, L, P	Now
16K x 9—w/ Half Full Flag	28	CY7C462	15, 25, 40	180	D, J, L, P	Now
16K x 9—w/ Prog. Flags	28	CY7C472	15, 25, 40	180	D, J, L, P	Now
16K x 9—Module	28	CYM4220	30, 40, 50, 65	540/120	HD	Now
32K x 9—w/ Half Full Flag	28	CY7C464	15, 25, 40	180	D, J, L, P	Now
32K x 9—w/ Prog. Flags	28	CY7C474	15, 25, 40	180	D, J, L, P	Now
64K x 9—Module	28	CYM4208	25, 30, 40	640/120	HD	Now
128K x 9—Module	28	CYM4209	25, 30, 40	640/120	HD	Now

* Clocked FIFO [CY7C44x/45x] times are cycle times.

Logic

Organization	Pins	Part Number	Speed	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
Programmable Skew Clock Buffer (TTL Output)	32	CY7B991	15-80 MHz	65	J, L	Now
Programmable Skew Clock Buffer (CMOS Output)	32	CY7B992	15-80 MHz	65	J, L	Now
2901—4-Bit Slice	40	CY7C901	t_{CLK} = 23, 31 ns	70	D, J, L, P	Now
2901—4-Bit Slice	40	CY2901	C	140	D, P	Now
4x2901—16-Bit Slice	64	CY7C9101	t_{CLK} = 30, 40 ns	60	D, J, L, P	Now
2909—Sequencer	28	CY7C909	t_{CLK} = 30, 40 ns	55	D, J, L, P	Now
2911—Sequencer	20	CY7C911	t_{CLK} = 30, 40 ns	55	D, J, L, P	Now
ECL/TTL Translator—10KH	84	CY10E383	t_{PD} = 2.5/3 ns	270	J, N	Now
ECL/TTL Translator—100K	84	CY101E383	t_{PD} = 2.5/3 ns	270	J, N	Now
ECL/TTL Translator—10KH	28S	CY10E384L	t_{PD} = 3 ns	110	V	Now
2909—Sequencer	28	CY2909	A	70	D, P	Now

Logic (continued)

Organization	Pins	Part Number	Speed	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
2911—Sequencer	20	CY2911	A	70	D, P	Now
2910—Controller (17-word Stack)	40	CY7C910	t_{CLK} = 40, 50, 93 ns	100	D, J, L, P	Now
2910—Controller (9-word Stack)	40	CY2910	A	170	D, J, L, P	Now
16 x 16 Multiplier	64	CY7C516	t_{MC} = 38, 45, 55, 75 ns	100 @ 10 MHz	D, G, J, L, P	Now
16 x 16 Multiplier	64	CY7C517	t_{MC} = 38, 45, 55, 75 ns	100 @ 10 MHz	D, G, J, L, P	Now
16 x 16 Multiplier/Accumulator	64	CY7C510	t_{MC} = 45, 55, 65, 75 ns	100 @ 10 MHz	D, G, J, L, P	Now

Design and Programming Tools

Part Name	Type	Part Number
QuickPro II	Programmer	CY3300
MAX+PLUS®	Design Tool	CY3201
QP2—MAX® PLD Programmer	Programmer	CY3202
MAX+PLUS PLS-EDIF	Design tool	CY3210
Warp2	VHDL Compiler	CY3120

RISC

Desc.	Organization	Pins	Part Number	Freq. (MHz)	I_{CC}/I_{SB} (mA @ 40 MHz)	Packages	Availability
IU	SPARC 32-bit Integer Unit	207	CY7C601A	40, 33, 25	675	G	Now
FPU	Floating-Point Unit (Controller and Processor)	143	CY7C602A	40, 33, 25	350	G	Now
CMU	Cache-Controlled Memory Management Unit	243	CY7C604A	40, 33, 25	750	G	Now
CMU-MP	Cache Controller and Multiprocessing Memory Management Unit	243	CY7C605A	40, 33, 25	850	G	Now
IU	SPARC 32-bit Integer Unit for Embedded Control	160	CY7C611A	25	600	U	Now
CSU	SPARC Cache Storage Unit	52	CY7C157A	40	250	J	Now
CPU	Complete Uniprocessor SPARC CPU	MBus 100	CYM6001K	40	2600		Now
CPU	Complete Multiprocessor SPARC Dual CPU	MBus 100	CYM6002K	40	5200		Now
CPU	Complete Multiprocessor SPARC Single CPU	MBus 100	CYM6003K	40	2800		Now
M2MC	MBus Memory Controller	160	CY7C613	40	280	N	Now
M2SX	MBus Peripheral I/O Controller	208	CY7C614	40	280	N	Now
INT/T	Interrupt Controller/Timer	100	CY7C615	40	230	N	Now
M2S	MBus-to-SBus Interface Controller	208	CY7C616	40	280	N	Now
M2V	MBus Graphics Controller	208	CY7C617	40	280	N	Now
SBus-DMA	Sbus DMA Controller	120	CY7C618	40	280	N	Now
CPU	Complete Multiprocessing SPARC Single-CPU 128K Cache	MBus 100	CYM6221K	55, 66	3200		Now
CPU	Complete Multiprocessing SPARC Single-CPU 256K Cache	MBus 100	CYM6224K	55, 66	3300		Now
CPU	Complete Multiprocessing SPARC Dual-CPU 256K Cache	MBus 100	CYM6226K	55, 66	6400		Now
CPU	Complete Uniprocessor SPARC CPU	256	CYM6111	40	2600	MCM	Now

VMEbus Interface Products

Organization	Pins	Part Number	Speed (MHz)	I_{CC} (mA)	Packages	Availability
VME Interface Controller	144/160	VIC068A	64	250	B, G, N, U	Now
VME Address Controller	144/160	VAC068A	50	150	B, G, N, U	Now
64-Bit VIC	144/160	VIC64	64	300	B, G, N, U	Now
Bus Interface Logic Circuit	64	CY7C964	N/A	120	N, U	Now

Communication Products

Organization	Pins	Part Number	Speed (MHz)	I_{CC} (mA)	Packages	Availability
HOTLink Transmitter	28	CY7B923	160-330	70	D, J, L, P	1Q93
HOTLink Receiver	28	CY7B933	160-330	100	D, J, L, P	1Q93

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C. Military temperature range (−55°C to +125°C) product processed to MIL-STD-883 Revision C is also available for most products. Speed and power selections may vary from those above. Contact your local sales office for more information.

Commercial grade product is available in plastic, cerDIP, or LCC. Military grade product is available in cerDIP, LCC, or PGA. F, K, and T packages are special order only.

All power supplies are V_{CC} = 5V ± 10% (V_{CC} = 5V ± 5% for RISC).

22S, 24S, 28S stands for 300 mil. 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

PLCC, SOJ, and SOIC packages are available on some products.

F, K, and T packages are special order only.

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Package Code:

B = Plastic Pin Grid Array
D = CerDIP
E = Tape Automated Bond (TAB)
F = Flatpack
G = Pin Grid Array (PGA)
H = Windowed Hermetic LCC
J = PLCC
K = Cerpack
L = Leadless Chip Carrier (LCC)
N = Plastic Quad Flatpack
P = Plastic
Q = Windowed LCC
R = Windowed PGA
S = SOIC
T = Windowed Cerpack
U = Ceramic Quad Flatpack
V = SOJ
W = Windowed CerDIP
X = DICE
HD = Hermetic DIP
HV = Hermetic Vertical DIP
PF = Plastic Flat SIP
PS = Plastic SIP
PZ = Plastic ZIP
Y = Ceramic LCC

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CYPRESS	CYPRESS
2147-35C	7C147-35C
2147-45C	2147-35C
2147-45C	7C147-45C
2147-45M+	7C147-45M+
2147-55C	2147-45C
2147-55M	2147-45M
2148-35C	21L48-35C
2148-35C	7C148-35C
2148-35M	7C148-35M
2148-45C	2148-35C
2148-45C	21L48-45C
2148-45M	2148-35M
2148-45M+	7C148-45M+
2148-55C	2148-45C
2148-55C	21L48-55C
2148-55M	2148-45M
2149-35C	21L49-35C
2149-35C	7C149-35C
2149-35M	7C149-35M
2149-45C	21L49-45C
2149-45M	2149-35M
2149-45M	7C149-45M
2149-55C	2149-45C
2149-55C	21L49-55C
2149-55M	2149-45M
21L48-35C	7C148-35C
21L48-45C	21L48-35C
21L48-45C	7C148-45C
21L48-55C	21L48-45C
21L49-35C	7C149-25C
21L49-45C	21L49-35C
21L49-45C	7C149-45C
21L49-55C	21L49-45C
7S03AC	7C189-25C
7S03AM	7C189-25M
7S03C	27S03AC
7S03C	74S189C
7S03M	27S03AM
7S03M	54S189M
7S07AC	7C190-25C
7S07AM	7C190-25M
7S07C	27S07AC
7S07M	27S07AM
7S07M	7C190-25M
901CC	7C901-31C
901CM	7C901-32M
909AC	7C909-40C
909AM	7C909-40M
910AC	7C910-50C
910AM	7C910-51M
910C	2910AC
910M	2910AM
911AC	7C911-40C
911AM	7C911-40M
341-2C	7C401-5C+
341-2M	7C401-10M
341C	3341-2C
341M	3341-2M
4S189M	27S03M
6116A-45C	6116A-35C
6116A-55C	6116A-45C
6116A-55M	6116A-45M

CYPRESS	CYPRESS
74S189C	27S03C
7C122-25C	7C122-15C+
7C122-35C	7C122-25C
7C122-35M	7C122-25M
7C123-12C	7C123-7C
7C128A-35C	7C128A-25C
7C128A-45C	7C128A-35C
7C128A-45M	7C128A-35M+
7C128A-55C	7C128A-45C+
7C128A-55M	7C128A-45M+
7C130-45C	7C130-35C
7C130-55C	7C130-45C
7C130-55M	7C130-45M
7C131-45C	7C131-35C
7C131-55C	7C131-45C
7C131-55M	7C131-45M
7C132-45C	7C132-35C
7C132-55C	7C132-45C
7C132-55M	7C132-45M
7C136-45C	7C136-35C
7C136-55C	7C136-45C
7C136-55M	7C136-45M
7C140-35C	7C140-25C
7C140-45C	7C140-35C
7C140-55C	7C140-45C
7C141-35C	7C141-25C
7C141-45C	7C141-35C
7C141-55C	7C141-45C
7C147-35C	7C147-25C+
7C147-45C	7C147-35C
7C148-35C	7C148-25C+
7C148-45C	7C148-35C
7C149-35C	7C149-25C+
7C149-45C	7C149-35C
7C149-45M	7C149-35M
7C150-25C	7C150-15C
7C150-35C	7C150-25C
7C150-35M	7C150-25M
7C167A-35C	7C167A-25C
7C167A-45M	7C167A-35M+
7C168A-35C	7C168A-25C
7C168A-45M	7C168A-35M+
7C169A-35C	7C169A-25C
7C169A-40M	7C169A-35M+
7C170A-35C	7C170A-25C
7C170A-45C	7C170A-35C
7C170A-45M	7C170A-35M
7C171A-35C	7C171A-25C
7C171A-45M	7C171A-35M+
7C172A-35C	7C172A-25C
7C172A-45M	7C172A-35M+
7C186L-45M	7C186-45M
7C189-25C	7C189-15C+
7C190-25C	7C190-15C+
7C191-45M	7C191-35M
7C192-45M	7C192-35M
7C194-35C	7C194-25C
7C194-45C	7C194-35C+
7C194-45M	7C194-35M
7C196-35C	7C196-25C
7C196-45C	7C196-35C+
7C197-35C	7C197-25C

CYPRESS	CYPRESS
7C197-45C	7C197-35C+
7C197-45M	7C197-35M
7C198-45C	7C198-35C
7C198-55C	7C198-45C+
7C198-55M	7C198-45M
7C199-45C	7C199-35C
7C199-55C	7C199-45C+
7C199-55M	7C199-45M
7C225-30C	7C225-25C
7C225-30M	7C225-25M
7C225-40C	7C225-30C
7C225-40M	7C225-35M
7C235-40C	7C235-30C
7C245-35C	7C245-25C
7C245-45C	7C245-35C
7C245-45M	7C245-35M
7C245A-25C	7C245A-18C
7C245A-35C	7C245AL-35C
7C245A-35M	7C245A-25M
7C245AL-35C	7C245A-25C+
7C245L-35C	7C245-35C+
7C245L-45C	7C245L-35C
7C251-55C	7C251-45C
7C251-65C	7C251-55C
7C251-65C	7C251-55C
7C251-65M	7C251-55M
7C253-65M	7C253-55M
7C254-55C	7C254-45C
7C254-65C	7C254-55C
7C254-65M	7C254-55M
7C261-45C	7C261-35C
7C261-55C	7C261-45C
7C261-55M	7C261-45M
7C263-45C	7C263-35C
7C263-55C	7C263-45C
7C263-55M	7C263-45M
7C264-45C	7C264-35C
7C264-55C	7C264-45C
7C264-55M	7C264-45M
7C269-50C	7C269-40C+
7C269-60C	7C269-50C
7C269-60M	7C269-50M+
7C281-45C	7C281-30C
7C282-45C	7C282-30C+
7C291-35C	7C291-25C+
7C291-50C	7C291-35C
7C291-50M	7C291-35M
7C291A-35C	7C291AL-35C
7C291A-35M	7C291A-30M
7C291A-50C	7C291AL-50C
7C291A-50M	7C291A-35M
7C291AL-35C	7C291A-25C+
7C291AL-50C	7C291AL-35C
7C291L-35C	7C291-35C+
7C291L-50C	7C291L-35C
7C292-35C	7C292-25C+
7C292-50C	7C292-35C
7C292L-35C	7C292-35C+
7C292L-50C	7C292L-35C
7C293A-35C	7C293AL-35C
7C293A-35M	7C293A-30M
7C293A-50C	7C293AL-50C

CYPRESS	CYPRESS
7C293A–50M	7C293A–35M
7C293AL–35C	7C293A–20C+
7C293AL–50C	7C293AL–35C
7C401–10C	7C401–15C
7C401–10M	7C401–15M
7C401–5C	7C401–10C
7C402–10C	7C402–15C
7C402–10M	7C402–15M
7C402–5C	7C402–10C
7C403–10C	7C403–15C
7C403–10M	7C403–15M
7C403–15C	7C403–25C
7C403–15M	7C403–25M
7C404–10C	7C404–15C
7C404–10M	7C404–15M
7C404–15C	7C404–25C
7C404–15M	7C404–25M
7C408–15C	7C408–25C
7C408–15M	7C408–25M
7C408–25C	7C408–35C
7C409–15C	7C409–25C
7C409–15M	7C409–25M
7C409–25C	7C409–35C
7C420–40C	7C420–30C
7C420–40M	7C420–30M
7C420–65C	7C420–40C
7C420–65M	7C420–40M
7C421–40C	7C421–30C
7C421–40M	7C421–30M
7C421–65C	7C421–40C
7C421–65M	7C421–40M
7C424–40C	7C424–30C
7C424–40M	7C424–30M
7C424–65C	7C424–40C
7C424–65M	7C424–40M
7C425–40C	7C425–30C
7C425–40M	7C425–30M
7C425–65C	7C425–40C
7C425–65M	7C425–40M
7C428–40C	7C428–30C
7C428–40M	7C428–30M
7C428–65C	7C428–40C
7C428–65M	7C428–40M
7C429–40C	7C429–30C
7C429–40M	7C429–30M
7C429–65C	7C429–40C
7C429–65M	7C429–40M
7C510–55C	7C510–45C
7C510–65C	7C510–55C
7C510–65M	7C510–55M
7C510–75C	7C510–65C
7C510–75M	7C510–65M
7C516–45C	7C516–38C
7C516–55C	7C516–45C
7C516–55M	7C516–42M
7C516–75C	7C516–55C
7C516–75M	7C516–55M
7C517–45C	7C517–38C
7C517–55C	7C517–45C
7C517–55M	7C517–42M
7C517–75C	7C517–55C
7C517–75M	7C517–55M

CYPRESS	CYPRESS
7C901–31C	7C901–23C+
7C901–32M	7C901–27M
7C909–40C	7C909–30C
7C909–40M	7C909–30M
7C910–50C	7C910–40C
7C910–51M	7C910–46M
7C910–93C	7C910–50C
7C910–99M	7C910–51M
7C9101–40C	7C9101–30C
7C9101–45M	7C9101–35M
7C911–40C	7C911–30C
7C911–40M	7C911–30M
9122–25C	7C122–15C
9122–25C	91L22–25C
9122–35C	9122–25C
9122–35C	91L22–35C
9122–45C	93L422C
91L22–25C	7C122–25C
91L22–35C	7C122–35C
91L22–45C	93L422AC
93422AC	7C122–35C
93422AC	9122–35C
93422AM	7C122–35M
93422C	93L422AC
93422M	93422AM
93422M	93L422AM
93L422AC	7C122–35C
93L422AC	91L22–45C
93L422AM	7C122–35M
93L422C	93L422AC
93L422M	93L422AM
PALC16L8–25C	PALC16L8L–25C
PALC16L8–30M	PALC16L8–20M
PALC16L8–35C	PALC16L8–25C
PALC16L8–40M	PALC16L8–30M
PALC16L8L–35C	PALC16L8L–25C
PALC16R4–25C	PALC16R4L–25C
PALC16R4–30M	PALC16R4–20M
PALC16R4–35C	PALC16R4–25C
PALC16R4–40M	PALC16R4–30M
PALC16R4L–35C	PALC16R4L–25C
PALC16R6–25C	PALC16R6L–25C
PALC16R6–30M	PALC16R6–20M
PALC16R6–35C	PALC16R6–25C
PALC16R6–40M	PALC16R6–30M
PALC16R6L–35C	PALC16R6L–25C
PALC16R8–25C	PALC16R8L–25C
PALC16R8–30M	PALC16R8–20M
PALC16R8–35C	PALC16R8–25C
PALC16R8–40M	PALC16R8–30M
PALC16R8L–35C	PALC16R8L–25C
PALC22V10–35C	PALC22V10–25C
PALC22V10–40M	PALC22V10–30M
PALC22V10L–25C	PALC22V10–25C
PALC22V10L–35C	PALC22V10L–25C
PLDC20G10–35C	PLDC20G10–25C
PLDC20G10–40M	PLDC20G10–30M

ALTERA	CYPRESS
PREFIX:EPM	PREFIX:CY
PREFIX:EP	PREFIX:PLD
5032DC	7C344–25WC

ALTERA	CYPRESS
5032DC–2	7C344–20WC
5032DC–15	Call Factory
5032DC–17	Call Factory
5032DC–20	7C344–20WC
5032DC–25	7C344–25WC
5032DM	7C344–25WMB
5032DM–25	7C344–25WMB
5032JC	7C344–25HC
5032JC–2	7C344–20HC
5032JC–15	Call Factory
5032JC–17	Call Factory
5032JC–20	7C344–20HC
5032JC–25	7C344–25HC
5032JI–20	7C344–20HI
5032JM	7C344–25HMB
5032JM–25	7C344–25HMB
5032LC	7C344–25JC
5032LC–2	7C344–20JC
5032LC–15	Call Factory
5032LC–17	Call Factory
5032LC–20	7C344–20JC
5032LC–25	7C344–25JC
5032PC	7C344–25PC
5032PC–2	7C344–20PC
5032PC–15	Call Factory
5032PC–17	Call Factory
5032PC–20	7C344–20PC
5032PC–25	7C344–25PC
5064JC	7C343–35HC
5064JC–1	7C343–25HC
5064JC–2	7C343–30HC
5064JI	7C343–35HI
5064JM	7C343–35HMB
5064LC	7C343–35JC
5064LC–1	7C343–25JC
5064LC–2	7C343–30JC
5128GC	7C342–35RC
5128GC–1	7C342–25RC
5128GC–2	7C342–30RC
5128GM	7C342–35RMB
5128JC	7C342–35HC
5128JC–1	7C342–25HC
5128JC–2	7C342–30HC
5128JI–2	7C342–30HI
5128JM	7C342–35HMB
5128LC	7C342–35JC
5128LC–1	7C342–25JC
5128LC–2	7C342–30JC
5128LI–2	7C342–30HI
5192GC	7C341–35RC
5192GC–1	7C341–25RC
5192GC–2	7C341–30RC
5192JC	7C341–35HC
5192JC–1	7C341–25HC
5192JC–2	7C341–30HC
5192JI	7C341–35HI
610A–15C	610–15C

AMD	CYPRESS
PREFIX:Am	PREFIX:CY
PREFIX:SN	PREFIX:CY
SUFFIX:B	SUFFIX:B

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

AMD	CYPRESS
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
2130-100C	7C130-55C
2130-120C	7C130-55C
2130-55C	7C130-45C
2130-55C	7C130-55C
2130-70C	7C130-55C
2130-70/BC	7C130-55MB
2140-55C	7C140-45C
2140-55C	7C140-55C
2140-70C	7C140-55C
2140-70/BC	7C140-55MB
2147-35C	2147-35C
2147-45C	2147-45C
2147-45M	2147-45M
2148-35C	2148-35C
2148-35M	2148-35M
2148-45C	2148-45C
2148-45M	2148-45M
2149-35C	2149-35C
2149-45C	2149-45C
2149-45M	2149-45M
21L47-55C	7C147-45C
21L49-45C	21L49-45C
27C256-55C	7C274-55C
27C256-70C	7C274-55C
27C64-55C	7C266-55C
27C64-70C	7C266-55C
27H256-35C	7C274-35C
27H256-45C	7C274-45C
27H256-45M	7C274-45M
27H256-55C	7C274-55C
27H256-55M	7C274-55M
27H256-70C	7C274-55M
27C512-75C	7C286-70C
27C512L-75C	7C286-70C
27LS291M	7C291-35M
27PS191AC	7C292-50C
27PS191AM	7C292-50M+
27PS191C	7C292-50C
27PS191M	7C292-50M+
27PS291AC	7C293-50C
27PS291AM	7C293-50M+
27PS291C	7C293-50C
27PS291M	7C293-50M+
27S03AC	27S03AC
27S03AM	27S03AM
27S03C	27S03C
27S03M	27S03M
27S07AC	27S07AC
27S07AM	27S07AM
27S07C	27S07C
27S07M	27S07M,
27S181AC	7C282-30C
27S181AM	7C282-45M
27S181C	7C282-45C
27S181M	7C282-45M
27S191AC	7C292A-35C
27S191AM	7C292A-50M
27S191C	7C292A-50C

AMD	CYPRESS
27S191M	7C292A-50M
27S191SAC	7C292A-25C
27S191SAM	7C292A-30M
27S25AC	7C225-30C
27S25AM	7C225-35M
27S25SAM	7C225-30M
27S25C	7C225-40C
27S25M	7C225-40M
27S25SAC	7C225-25C
27S281AC	7C281-30C
27S281AM	7C281-45M
27S281C	7C281-45C
27S281M	7C281-45M
27S291AC	7C291A-35C
27S291AM	7C291A-50M
27S291C	7C291A-50C
27S291M	7C291A-50M
27S291SAC	7C291A-25C
27S291SAM	7C291A-30M
27S35AC	7C235-30C
27S35AM	7C235-40M
27S35C	7C235-40C
27S35M	7C235-40M
27S45AC	7C245-35C
27S45AM	7C245-45M
27S45C	7C245-45C
27S45M	7C245-45M
27S45SAC	7C245-25C
27S45SAM	7C245A-25M-
27S49A	7C263/4-40C
27S49AM	7C263/4-55M
27S49C	7C263/4-55C
27S49M	7C263/4-55M
27S49SAC	7C263/4-25C
27S49SAM	7C263/4-25M
2841AC	3341C
2841AM	3341M
2841C	3341C
2841M	3341M
2901BC	2901CC
2901BM	2901CM
2901CC	2901CC
2901CM	2901CM
2909AC	2909AC
2909AM	2909AM
2909C	2909AC
2909M	2909M
2910-1C	2910C
2910-1M	2910M
2910AC	2910AC
2910AM	2910AM
2910C	2910C
2910M	2910M
2911AC	2911AC
2911AM	2911AM
2911C	2911AC
2911M	2911M
29510C	7C510-75C
29510M	7C510-75M
29516AM	7C516-55M
29516C	7C516-55C
29516M	7C516-55M

AMD	CYPRESS
29517AC	7C517-38C
29517C	7C517-55C
29517M	7C517-55M
29701C	27S07C
29701M	27S07M
29C01-1C	7C901-23C+
29C01BA	7C901-32M
29C01BC	7C901-31C
29C01C	7C901-31C
29C01CC	7C901-31C
29C10-1C	7C910-40C
29C101C	7C9101-40C
29C101M	7C9101-35M
29C10ABA	7C910-51M
29C10AC	7C910-50C
29C10AC	7C910-93C
29L510C	7C510-75C
29L510M	7C510-75M
29L516C	7C516-75C
29L516M	7C516-75M
29L517C	7C517-75C
29L517M	7C517-75M
3341C	3341C
3341M	3341M
67C401-10	7C401-10
67C401-15	7C401-15
67C401-25	7C401-25
67C402-10	7C402-10
67C402-15	7C402-15
67C402-25	7C402-25
67C4023-10	7C404-10
67C4023-15	7C404-15
67C403-10	7C403-10
67C403-15	7C403-15
67C403-25	7C403-25
7201-25	7C420-25
7201-35	7C420-30
7201-50	7C420-40
7201-65	7C420-65
7201-80	7C420-65
7201-25R	7C421-25
7201-35R	7C421-30
7201-50R	7C421-40
7201-65R	7C421-65
7201-80R	7C421-65
7202A-15	7C425A-15
7202A-25	7C424-25
7202A-35	7C424-30
7202A-50	7C424-40
7202A-65	7C424-65
7202A-80	7C424-65
7202A-25R	7C425-25
7202A-35R	7C425-30
7202A-50R	7C425-40
7202A-65R	7C425-65
7202A-80R	7C425-65
7203A-15	7C429A-15
7203A-25	7C428-25
7203A-35	7C428-30
7203A-50	7C428-40
7203A-65	7C428-65
7203A-80	7C428-65

AMD	CYPRESS
7203A–25R	7C429–25
7203A–35R	7C429–30
7203A–50R	7C429–40
7203A–65R	7C429–65
7203A–80R	7C429–65
7204A–15	7C433A–15
7204A–25	7C432–25
7204A–35	7C432–30
7204A–50	7C432–40
7204A–65	7C432–65
7204A–80	7C432–65
7205A–15	7C460–15
7205A–25	7C460–25
74S189C	74S189C
9122–25C	9122–25C
9122–35C	9122–35C
9122–35M	7C122–35M
9128–100C	6116A–55C
9128–120M	6116A–55M
9128–150C	6116A–55C
9128–150M	6116A–55M
9128–200C	6116A–55C
9128–200M	6116A–55M
9128–70C	6116A–55C
9128–90M	6116A–55M
9150–20C	7C150–15C
9150–25C	7C150–25C
9150–25M	7C150–25M
9150–35C	7C150–35C
9150–35M	7C150–35M
9150–45C	7C150–35C
9150–45M	7C150–35M
91L22–35C	91L22–35C
91L22–35M	7C122–35M
91L50–25C	7C150–25C
91L50–35C	7C150–35C
93422AC	93422AC
93422AM	93422AM
93422C	93422C
93422M	93422M
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
PAL16L8A–4C	PALC16L8L–35C
PAL16L8A–4M	PALC16L8–40M
PAL16L8AC	PALC16L8–25C
PAL16L8ALC	PALC16L8–25C
PAL16L8ALM	PALC16L8–30M
PAL16L8AM	PALC16L8–30M
PAL16L8BM	PALC16L8–20M
PAL16L8C	PALC16L8–35C
PAL16L8LC	PALC16L8–35C
PAL16L8LM	PALC16L8–40M
PAL16L8M	PALC16L8–40M
PAL16L8QC	PALC16L8L–35C
PAL16L8QM	PALC16L8–40M
PAL16R4A–4C	PALC16R4L–35C
PAL16R4A–4M	PALC16R4–40M
PAL16R4ALC	PALC16R4–25C
PAL16R4ALM	PALC16R4–30M
PAL16R4AM	PALC16R4–30M

AMD	CYPRESS
PAL16R4BM	PALC16R4–20M
PAL16R4C	PALC16R4–35C
PAL16R4LC	PALC16R4–35C
PAL16R4LM	PALC16R4–40M
PAL16R4M	PALC16R4–40M
PAL16R4QC	PALC16R4L–35C
PAL16R4QM	PALC16R4–40M
PAL16R6A–4C	PALC16R6L–35C
PAL16R6A–4M	PALC16R6–40M
PAL16R6AC	PALC16R6–25C
PAL16R6ALC	PALC16R6–25C
PAL16R6ALM	PALC16R6–30M
PAL16R6AM	PALC16R6–30M
PAL16R6BM	PALC16R6–20M
PAL16R6C	PALC16R6–35C
PAL16R6LC	PALC16R6–35C
PAL16R6LM	PALC16R6–40M
PAL16R6M	PALC16R6–40M
PAL16R6QC	PALC16R6L–35C
PAL16R6QM	PALC16R6–40M
PAL16R8A–4C	PALC16R8L–35
PAL16R8A–4M	PALC16R8–40M
PAL16R8AC	PALC16R8–25C
PAL16R8ALC	PALC16R8–25C
PAL16R8ALM	PALC16R8–30M
PAL16R8AM	PALC16R8–30M
PAL16R8BM	PALC16R8–20M
PAL16R8C	PALC16R8–35C
PAL16R8LC	PALC16R8–35C
PAL16R8LM	PALC16R8–40M
PAL16R8M	PALC16R8–40M
PAL16R8QC	PALC16R8L–35
PAL16R8QM	PALC16R8–40M
PAL22V10–7JC	PALC22V10D–7JC
PAL22V10–7PC	PALC22V10D–7PC
PAL22V10–10DC	PALC22V10D-10DC
PAL22V10–10JC	PALC22V10D-10JC
PAL22V10–10PC	PALC22V10D-10PC
PAL22V10–12/B3A	PALC22V10B –10LMB
PAL22V10–12/BLA	PALC22V10B –10DMB
PAL22V10–15DC	PALC22V10B-15DC
PAL22V10–15JC	PALC22V10B-15JC
PAL22V10–15PC	PALC22V10B-15PC
PAL22V10–20/B3A	PALC22V10B –20LMB
PAL22V10–20/BLA	PALC22V10B –20DMB
PAL22V10/B3A	PALC22V10-35LMB
PAL22V10/BLA	PALC22V10-35DMB
PAL22V10A/B3A	PALC22V10-25LMB
PAL22V10A/BLA	PALC22V10-25DMB
PAL22V10ADC	PALC22V10–25DC
PAL22V10AJC	PALC22V10–25JC
PAL22V10APC	PALC22V10–25PC
PAL22V10DC	PALC22V10–35DC
PAL22V10JC	PALC22V10–35JC
PAL22V10PC	PALC22V10–35PC
PALCE16V8H–15C	PLDC18G8–12C
PALCE16V8H–15C	PLDC18G8–15C
PALCE16V8H–20/B	PLDC18G8–15MB
PALCE16V8H–20/B	PLDC18G8–20MB

AMD	CYPRESS
PALCE16V8H–25/B	PLDC18G8–20MB
PALCE16V8H–25C	PLDC18G8–20C
PALCE22V10H-10JC	PALC22V10D-10JC
PALCE22V10H-10PC	PALC22V10D-10PC
PALCE22V10H -15/B3A	PALC22V10D -15LMB
PALCE22V10H -15/BLA	PALC22V10D -15DMB
PALCE22V10H-15JC	PALC22V10D-15JC
PALCE22V10H-15PC	PALC22V10D-15PC
PALCE22V10H -20/B3A	PALC22V10D -20LMB
PALCE22V10H -20/BLA	PALC22V10D -20DMB
PALCE22V10H -25/B3A	PALC22V10D -25LMB
PALCE22V10H -25/BLA	PALC22V10D -25DMB
PALCE22V10H-25JC	PALC22V10D-25JC
PALCE22V10H-25PC	PALC22V10D-25PC
PALCE22V10H -30/B3A	PALC22V10D -25LMB
PALCE22V10H -30/BLA	PALC22V10D -25DMB

ANALOG DEV	CYPRESS
PREFIX:ADSP	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:E	SUFFIX:L
SUFFIX:F	SUFFIX:F
SUFFIX:G	SUFFIX:G
1010A	7C510–65C+
1010J	7C510–75C+
1010K	7C510–75C+
1010S	7C510–75M+
1010T	7C510–75M+
7C901–27M	7C910–32M
7C901–32M	2901CM

AT&T	CYPRESS
7C116–20	6116A–20C
7C116–25	6116A–25C
7C166–10	7B166–10C
7C166–12	7B166–12C
7C166–15	7C166–15C
7C166–20	7C166–20C
7C166–25	7C166–25C
7C185–10	7B185–10C
7C185–12	7C185–12C
7C185–15	7C185–15C
7C185–20	7C185–20C
7C185–25	7C185–25C
7C194–15	7C194–12C
7C194–15	7C194–15C
7C194–20	7C194–20C
7C194–25	7C194–25C
7C199–12	7C199–12C
7C199–15	7C199–15C
7C199–20	7C199–20C
7C199–25	7C199–25C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

ATMEL	CYPRESS
PREFIX:AT	PREFIX:CY
27HC256R−55C	7C274−55C
27HC256R−70C	7C274−55C
27HC256R−70M	7C274−55M
27HC642−35C	7C261−35C
27HC642−45C	7C261−45C
27HC642−45M	7C261−45M
27HC642−55C	7C261−55C
27HC642−55M	7C261−55M
27HC642−70C	7C261−55C
22V10	PALC22V10
22V10−15	PALC22V10B

CATALYST	CYPRESS
CAT27HC256L/LI-55	CY7C274−55C/I
CAT27HC256L/LI-70	CY7C274−55C/I

DALLAS	CYPRESS
PREFIX:DS	PREFIX:CY
2009	7C421−25C
2010	7C425−2C
2011	7C429−25C

DENSEPAK	CYPRESS
PREFIX:DPS	PREFIX:CYM
16X17−25C	1611HV−25C
16X17−25C	1611HV−25C
16X17−35C	1611HV−35C
16X17−35C	1611HV−35C
16X17−45C	1611HV−45C
16X17−45C	1611HV−45C
16X17−55C	1611HV−55C
1432−45C	1830HD−45C
1432−55C	1830HD−55C
1432−55C	1830HD−55C
1M624−100C	1623HD−85C
1M624−85C	1623HD−100C

EDI	CYPRESS
PREFIX:ED	PREFIX:CYM
116H16C−25	1611HV−25C
116H16C−35	1611HV−35C
116H16C−45	1611HV−45C
1464C−45	7C194−45
1F32256CXXMZC	M1841PZ−XXC
1F3264CXXMZC	M1831PZ−XXC
1F8512CXXBC	1465PC−XXC
1F8512LPXXB6C	1465LPD−XXC
F8512PXXB6C	1465LPD−XXC
1M16256C−25C9C	1641HD−25C
1M16256C−30C9C	1641HD−30C
1M16256C−35C9C	1641HD−35C
1M16256C−45C9C	1641HD−45C
1M16256C−55C9C	1641HD−55C
1M16256C−70C9C	1641HD−55C
M16256C−30C9MB	1641HD−30MB
M16256C−35C9MB	1641HD−35MB
M16256C−45C9MB	1641HD−45MB
M16256C−55C9MB	1641HD−55MB
M16256C−70C9MB	1641HD−55MB
M32256CXXC6B	M1840HD−XXMB
M32256CXXC6B	M1840HD−XXC

EDI	CYPRESS
8M3264CXXC6B	M1830HD−XXMB
8M3264CXXC6C	M1830HD−XXC
8M8128C−100	1421HD−85C
8M8128C−100CB	1420HD−55MB
8M8128C−60CB	1420HD−55MB
8M8128C−60CC	1420HD−55C
8M8128C−70	1421HD−70C
8M8512CXXC6B	1466HD−XXMB
8M8512CXXC6C	1466HD−XXC
8M8512CXXM6C	1464PD−XXC
8M8512LPXXC6B	1466LHD−XXMB
8M8512PXXC6B	1466LHD−XXMB
H816H16C−25CC−	1611HV−25C
H816H16C−35CC−	1611HV−35C
H816H16C−45CC−	1611HV−45C
H816H16C−55CC−	1611HV−45C

FUJITSU	CYPRESS
PREFIX:MB	PREFIX:CY
PREFIX:MBM	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:M	SUFFIX:P
SUFFIX:Z	SUFFIX:D
100422A−5C	100E422−5C
100422A−7C	100E422L−7C
100422AC	100E422L−7C
100470A−7	100E470−7C
100470A−10	100E470−7C
100470A−15	100E470−7C
100474A−3C	100E474−3.5C
100474A−5C	100E474−5C
100474A−7C	100E474L−7C
100474AC	100E474L−7C
100484A−10	100E484L−7C
100484A−8	100E484L−7C
100484−15	100E484L−7C
101A484−5	101E484−5C
10422A−5C	10E422−5C
10422A−7C	10E422L−7C
10422AC	10E422L−7C
10470A−7	10E470−7C
10470A−10C	10E470−7C
10470A−15C	10E470−7C
10470A−20C	10E470−7C
10474A−3C	10E474−4C
10474A−5C	10E474−5C
10474A−7C	10E474L−7C
10474AC	10E474L−7C
10484−15	10E484L−7C
10484A−8	10E484L−7C
10484A−10	10E484L−7C
10484A−5	10E484−5C
2147H−35	2147−35C
2147H−45	2147−45C
2147H−55	2147−55C
2148−55L	21L48−55C
2149−45	2149−45C
2149−55L	21L49−55C
7132E	7C282−45C
7132E−SK	7C281−45C
7132E−W	7C282−45M
7132H	7C282−45C

FUJTISU	CYPRESS
7132H−SK	7C281−45C
7132L−70	7C281/2−45C
7132Y	7C282−30C
7132Y−SK	7C281−30C
7138Y−35	7C291/2A−35C
7138H−45	7C291/2A−35C
7138E−55	7C291/2A−50C
7138E−W	7C291/2A−50M
7144E	7C264−55C
7144E−W	7C264−55M
7144H	7C264−55C
71A38−25	7C291/2A−25C
71A38−35	7C291/2A−35C
71C44−35	7C264−35C
71C44−45	7C264−45C
71C46−45	7C254−45C
7226RA/S−25	7C225−25C
7232RA−25	7C235−25C
7238RA−20	7C245A−18C
7238RA−20−W	7C245A−18M
7238RA−25	7C245A−25C
7238RA−25−W	7C245A−25M
8128−10	7C128A−55C
8128−15	7C128A−55C
8167−70W	7C167A−45M
8167A−55	7C167A−45C
8167A−70	7C167A−45C
8168−55	7C168A−45C
8171−55	7C187−45C
8171−70	7C187−45C
81C67−35	7C167A−35C
81C67−45	7C167A−45C
81C67−55W	7C167A−45M
81C68−45	7C168A−45C
81C68−55W	7C168A−45M+
81C71−45	7C187−45C
81C71−55	7C187−45C
81C74−25	7C164−25C
81C74−35	7C164−35C+
81C74−45	7C164−45C
81C75−25	7C166−25C
81C75−35	7C166−35C
81C78−45	7C186−45C
81C78−55	7C186−55C
81C81A−35	7C197−35
81C81A−45	7C197−45
81C84A−35	7C194−35
81C84A−45	7C194−45
81C86−70	7C192−45C+
8287−35	7C199−35
8299	7C188
8287−45	7C199−45
8464L−100	7C185−55C+
8464L−70	7C185−45C+

HARRIS	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HPL	PREFIX:CY
SUFFIX:8	SUFFIX:B
PREFIX:1	SUFFIX:D
PREFIX:9	SUFFIX:F
PREFIX:4	SUFFIX:L

HARRIS	CYPRESS
PREFIX:3	SUFFIX:P
16LC8–5	PALC16L8L–35C
16LC8–8	PALC16L8–40M
16LC8–9	PALC16L8–40M
16RC4–5	PALC16R4L–35C
16RC4–8	PALC16R4–40M
16RC4–9	PALC16R4–40M
16RC6–5	PALC16R6L–35C
16RC6–8	PALC16R6–40M
16RC6–9	PALC16R6–40M
16RC8–5	PALC16R8L–35C
16RC8–8	PALC16R8–40M
16RC8–9	PALC16R8–40M
6–76161–2	7C291–50M
6–76161–5	7C291–50C
6–76161A–2	7C291–50M
6–76161A–5	7C291–50C
6–76161B–5	7C291–35C
6–7681–5	7C281–45C
6–7681A–5	7C281–45C
76161–2	7C292–50M
76161A–2	7C292–50M
76161A–5	7C292–50C
76161B–5	7C292–35C
76641–2	7C264–55M
76641–5	7C264–55C
76641A–5	7C264–45C
7681–2	7C282–45M
7681–5	7C282–45C
7681A–5	7C282–45C

HITACHI	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HN	PREFIX:CY
SUFFIX:CG	SUFFIX:L
SUFFIX:G	SUFFIX:D
SUFFIX:P	SUFFIX:P
100422C	100E422L–7C
100474–10C	100E474L–7C
100474–8C	100E474L–7C
100474C	100E474L–7C
10422C	10E422L–7C
10474–10C	100E474L–7C
10474–8C	10E474L–7C
10474C	10E474L–7C
25089	7C282–45C
25089S	7C282–45C
25169S	7C292–50C
27C256GHG–70C	7C274–55C
27C256GHG–85C	7C274–55C
4847	2147–55C
4847–2	2147–45C
4847–3	2147–55C
6116ALS–12	6116A–55C*
6116ALS–15	6116A–55C*
6116ALS–20	6116A–55C*
6116AS–12	6116A–55C+
6116AS–15	6116A–55C+
6116AS–20	6116A–55C+
6147	7C147–45C*
6147–3	7C147–45C*
6147H–35	7C147–35C+

HITACHI	CYPRESS
6147H–45	7C147–45C+
6147H–55	7C147–45C+
6147HL–35	7C147–35C*
6147HL–45	7C147–45C*
6147HL–55	7C147–55C*
6148	7C148–45C
6148H–35	21L48–35C
6148H–45	7C148–45C+
6148H–55	7C14845C+
6148HL–35	21L48–35C*
6148HL–45	7C148–45C*
6148HL–55	7C148–45C*
6148L	7C148–45C*
6167–6	7C167A–45C+
6167–8	7C167A–45C+
6167H–55	7C167A–45C
6167H–70	7C167A–45C
6167HL–55	7C167A–45C*
6167HL–70	7C167A–45C*
6167L–6	7C167A–45C*
6167L–8	7C167A–45C*
6168H–45	7C168A–45C+
6168H–55	7C168A–45C+
6168H–70	7C168A–45C+
6168HL–45	7C168A–45C*
6168HL–55	7C168A–45C*
6168HL–70	7C168A–45C*
6207P–35	7C197–35
6207P–45	7C197–45
6208P–35	7C194–35
6208P–45	7C194–45
62256	7C198*
6264–10	7C186–55C+
6264–12	7C186–55C+
6264–15	7C186–55C+
6267–35	7C167A–35C+
6267–45	7C167A–45C
6268–25	7C168A–25C
6268–35	7C168A–35C
62832H	7C199+
62832	7C199
6287–45	7C187–45C
6287–55	7C187–45C
6287–70	7C187–45C
6288–35	7C164–35C
6288–45	7C164–45C
6288–55	7C164–45C
62932	7C188
6707–20	7C197–20C
6707–25	7C197–25C
6707A–15	7C197–15C
6707A–20	7C197–20C
6707A–25	7C197–25C
6708–20	7C194–20C
6708–25	7C194–25C
6708A–15	7C194–15C
6708A–20	7C194–20C
6708A–25	7C194–25C
6709–20	7C195–20C
6709–25	7C195–25C
6709A–15	7C195–15C
6709A–20	7C195–20C

HITACHI	CYPRESS
6709A–25	7C195–25C
6716–25	7C128A–25C
6716–30	7C128A–25C
6787–30	7C187–25C
6788–25	7C164–25C
6788–30	7C164–25C
6788HA–12	7B164–12C
6789HA–12	7B166–12C

ICT	CYPRESS
27CX256–35C	CY7C274–35C
27CX256–45C	CY7C274–45C
27CX256–55C	CY7C274–55C

IDT	CYPRESS
PREFIX:IDT	PREFIX:CY
PREFIX:IDT	PREFIX:CYM
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
100484S7	100E484L–7C
101484S7	100E484L–7C
10484S7	10E484L–7C
39C01CB	7C901–32M+
39C01CC	2901CC+
39C01CM	2901CM+
39C01DB	7C901–27M+
39C01DC	7C901–23C+
39C09A	7C909–40C+
39C09AB	7C909–40M+
39C10B	7C910–50C–
39C10BB	7C910–51M
39C11A	7C911–40C+
39C11AB	7C911–40M+
6116SA120B	7C128A–55MB
6116SA25	7C128A–25C
6116SA35	7C128A–35C
6116SA35	6116A–35C
6116SA35B	7C128A–35MB
6116SA35B	6116A–35MB
6116SA45	7C128A–45C
6116SA45	6116A–45C
6116SA45B	7C128A–45MB
6116SA45B	6116A–45MB
6116SA55B	7C128A–55MB
6116SA55B	6116A–55MB
6116SA70B	7C128A–55MB
61298SA25	7C196–25C
61298SA25B	7C196–25MB
61298SA35	7C196–35C
61298SA35B	7C196–35MB
61298SA45	7C196–45C
61298SA45B	7C196–45MB
61298SA55	7C196–45
61298SA55B	7C196–45MB
61298SA70B	7C196–45MB
6167SA100B	7C167A–45MB
6167SA25	7C167A–25C
6167SA35	7C167A–35C
6167SA35B	7C167A–35MB

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* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

IDT	CYPRESS
5167SA45B	7C167A–45MB
5167SA55B	7C167A–45MB
5167SA70B	7C167A–45MB
5167SA85B	7C167A–45MB
5168SA100B	7C168A–45MB
5168SA15	7C168A–15C
5168SA20	7C168A–20C
5168SA25	7C168A–25C
5168SA25B	7C168A–25MB
5168SA35	7C168A–35C
5168SA35B	7C168A–35MB
5168SA45B	7C168A–45MB
5168SA55B	7C168A–45MB
5168SA70B	7C168A–45MB
5168SA90B	7C168A–45MB
7197SA25	7C170A–25C
7197SA35	7C170A–35C
7197SA35B	7C170A–35MB
7197SA45B	7C170A–45MB
7197SA55	7C170A–45C
7197SA55B	7C170A–45MB
7198SA15	7C166–15C
7198SA19	7C166–15C
7198SA20	7C166–20C
7198SA20B	7C166–A20MB
7198SA25	7C166–25C
7198SA25B	7C166–A25MB
7198SA30	7C166–25C
7198SA30B	7C166–A25MB
7198SA45	7C166–45C
7198SA45B	7C166–A45MB
7198SA55B	7C166–A45MB
7198SA70B	7C166–A45MB
7198SA85B	7C166–A45MB
71B298S12	7C195–12C
71B298S15	7C195–15C
71B298S20	7C195–20C
71B298S15B	7C195–15MB
71B298S20B	7C195–20MB
7005S35	7B144–25C
7005S35	7B144–35C
7005S45B	7B144–35MB
71256SA100B	7C198–55MB
71256SA15	7C199–15C
71256SA20	7C199–20C
71256SA20B	7C199–20MB
71256SA25	7C198–25C
71256SA30	7C198–25C
71256SA30B	7C198–25MB
71256SA35	7C198–35C
71256SA35B	7C198–35MB
71256SA45	7C198–45C
71256SA45B	7C198–45MB
71256SA55	7C198–55C
71256SA55B	7C198–55MB
71256SA70	7C198–55C
71256SA70B	7C198–55MB
71256SA85B	7C198–55MB
71257SA25	7C197–25C
71257SA25B	7C197–25MB
71257SA35	7C197–35C
71257SA35B	7C197–35MB

IDT	CYPRESS
71257SA45	7C197–45C
71257SA45B	7C197–45MB
71257SA55	7C197–45C
71257SA55B	7C197–45MB
71257SA70B	7C197–45MB
71258SA25	7C194–25C
71258SA25B	7C194–25MB
71258SA35	7C194–35C
71258SA35B	7C194–35MB
71258SA45	7C194–45C
71258SA45B	7C194–45MB
71258SA55	7C194–45C
71258SA55B	7C194–45MB
71258SA70B	7C194–45MB
71259	7C188
71281SA25	7C191–25C
71281SA25B	7C191–25MB
71281SA35	7C191–35C
71281SA35B	7C191–35MB
71281SA45	7C191–45C
71281SA45B	7C191–45MB
71281SA55	7C191–45C
71281SA55B	7C191–45MB
71281SA70B	7C191–45MB
71282SA	7C192–25C
71282SA	7C192–25MB
71282SA	7C192–35C
71282SA	7C192–35MB
71282SA	7C192–45C
71282SA	7C192–45MB
71282SA	7C192–45C
71282SA	7C192–45MB
71282SA	7C192–45MB
7130LA25	7C130–25C
7130LA25J	7C131–25JC
7130LA30	7C130–30C
7130LA30J	7C131–30JC
7130LA35	7C130–35C
7130LA35B	7C130–35MB
7130LA35J	7C131–35JC
7130LA35LB	7C130–35LMB
7130LA45	7C130–45C
7130LA45B	7C131–45MB
7130LA45J	7C131–45JC
7130LA45LB	7C130–45LMB
7130LA55	7C130–55C
7130LA55B	7C131–55MB
7130LA55J	7C131–55JC
7130LA55L52B	7C130–55LMB
7130LA70	7C130–55C
7130LA70B	7C131–55MB
7130LA70J	7C131–55JC
7130LA70LB	7C130–55LMB
7130LA90LB	7C131–55LMB
7130SA100	7C130–55C
7130SA100B	7C130–55MB
7130SA100LB	7C131–55LMB
7130SA25	7C130–25C
7130SA30	7C130–25C
7130SA25J	7C131–25JC
7130SA30J	7C131–30JC
7130SA35	7C130–35C

IDT	CYPRESS
7130SA35B	7C130–35MB
7130SA35J	7C131–35JC
7130SA35LB	7C131–35LMB
7130SA45	7C130–45C
7130SA45B	7C130–45MB
7130SA45J	7C131–45JC
7130SA45LB	7C131–45LMB
7130SA55	7C130–55C
7130SA55B	7C130–55M
7130SA55J	7C131–55JC
7130SA55LB	7C131–55LMB
7130SA70	7C130–55C
7130SA70B	7C130–55MB
7130SA70J	7C131–55JC
7130SA70LB	7C131–55LMB
7130SA90	7C130–55C
7130SA90B	7C130–55MB
7130SA90J	7C131–55JC
7130SA90LB	7C131–55LMB
71321LA25	7C136–25C
71321LA30	7C136–30C
71321LA35	7C136–35C
71321LA35B	7C136–35MB
71321LA45	7C136–45C
71321LA45B	7C136–45MB
71321LA55	7C136–55C
71321LA55B	7C136–55MB
71321LA70	7C136–55C
71321LA70B	7C136–55MB
71321LA90	7C136–55C
71321LA90B	7C136–55MB
71321SA25	7C136–25C
71321SA30	7C136–30C
71321SA35	7C136–35C
71321SA35B	7C136–35MB
71321SA45	7C136–45C
71321SA45B	7C136–45MB
71321SA55	7C136–55C
71321SA55B	7C136–55MB
71321SA70	7C136–55C
71321SA70B	7C136–55MB
71321SA90	7C136–55C
71321SA90B	7C136–55MB
7132LA25	7C132-25C
7132LA30	7C132-30C
7132LA35	7C132-35C
7132LA35B	7C132-35MB
7132LA45	7C132-45C
7132LA45B	7C132-45MB
7132LA55	7C132–55C*
7132LA55B	7C132-55MB
7132LA70	7C132–55C*
7132LA70B	7C132–55M*
7132LA90	7C132–55C*
7132LA90B	7C132–55M*
7132LA100	7C132–55C*
7132LA100B	7C132–55M*
7132LA120B	7C132–55M*
7132SA100	7C132–55C+
7132SA100B	7C132–55M+
7132SA120B	7C132–55M+
7132SA25	7C132–25C

IDT	CYPRESS
7132SA30	7C132–30C
7132SA35	7C132–35C
7132SA35B	7C132–35MB
7132SA45	7C132–45C
7132SA45B	7C132–45MB
7132SA55B	7C132–55MB
7132SA55	7C132–55C+
7132SA70	7C132–55C+
7132SA70B	7C132–55M+
7132SA90	7C132–55C+
7132SA90B	7C132–55M+
71342S35	7C1342–25C
71342S35	7C1342–35C
71342S45B	7C1342–35MB
7134S35	7B134–25C
7134S35	7B134–35C
7134S35J52	7B135–25JC
7134S35J52	7B135–35JC
7134S35L52	7B135–25LC
7134S35L52	7B135–35LC
7134S45B	7B134–35MB
7134S45L52B	7B135–35LMB
7140LA25	7C140–25C
7140LA25J	7C141–25JC
7140LA30	7C140–30C
7140LA30J	7C141–30JC
7140LA30L52	7C141–30LC
7140LA35	7C140–35C
7140LA35B	7C140–35MB
7140LA35J	7C141–35JC
7140LA35LB	7C141–35LMB
7140LA45	7C140–45C
7140LA45B	7C140–45MB
7140LA45J	7C141–45JC
7140LA45LB	7C141–45LMB
7140LA55	7C140–55C
7140LA55B	7C140–55MB
7140LA55J52	7C141–55JC
7140LA55LB	7C141–55LMB
7140LA70	7C140–55C
7140LA70B	7C140–55MB
7140LA70J	7C141–55JC
7140LA70LB	7C141–55LMB
7140LA90J	7C141–55JC
7140LA90LB	7C141–55LMB
7140SA100	7C140–55C
7140SA100B	7C140–55MB
7140SA100L	7C141–55C
7140SA100LB	7C141–55MB
7140SA25	7C140–25C
7140SA25J	7C141–25JC
7140SA30	7C140–30C
7140SA30J	7C141–30JC
7140SA35	7C140–35C
7140SA35B	7C140–35MB
7140SA35J	7C141–35JC
7140SA35LB	7C141–35LMB
7140SA45	7C140–45C
7140SA45B	7C140–45MB
7140SA45J	7C141–45JC
7140SA45LB	7C141–45LMB
7140SA55	7C140–55C

IDT	CYPRESS
7140SA55B	7C140–55MB
7140SA55J	7C141–55JC
7140SA55LB	7C141–55LMB
7140SA70	7C140–55C
7140SA70B	7C140–55MB
7140SA70J	7C141–55JC
7140SA70LB	7C141–55LMB
7140SA90	7C140–55C
7140SA90B	7C140–55MB
7140SA90J	7C141–55JC
7140SA90LB	7C141–55LMB
71421LA25	7C146–25C
71421LA30	7C146–30C
71421LA35	7C146–35C
71421LA35B	7C146–35MB
71421LA45	7C146–45C
71421LA45B	7C146–45MB
71421LA55	7C146–55C
71421LA55B	7C146–55MB
71421LA70	7C146–55C
71421LA70B	7C146–55MB
71421LA90	7C146–55C
71421LA90B	7C146–55MB
71421SA25	7C146–25C
71421SA30	7C146–30C
71421SA35	7C146–35C
71421SA35B	7C146–35MB
71421SA45	7C146–45C
71421SA45B	7C146–45MB
71421SA55	7C146–55C
71421SA55B	7C146–55MB
71421SA70	7C146–55C
71421SA70B	7C146–55MB
71421SA90	7C146–55C
71421SA90B	7C146–55MB
7142LA25	7C142–25C
7142LA30	7C142–30C
7142LA35	7C142–35C
7142LA35B	7C142–35MB
7142LA45	7C142–45C
7142LA45B	7C142–45MB
7142LA55	7C142–55C
7142LA55B	7C142–55MB
7142LA70	7C142–55C
7142LA70B	7C142–55MB
7142SA25	7C142–25C
7142SA30	7C142–30C
7142SA35	7C142–35C
7142SA35B	7C142–35MB
7142SA45	7C142–45C
7142SA45B	7C142–45MB
7142SA55	7C142–55C
7142SA55B	7C142–55MB
7142SA70	7C142–55C
7142SA70B	7C142–55MB
7164SA20	7C185–20C
7164SA20P	7C186–20C
7164SA25	7C185–25C
7164SA25B	7C185A–25MB
7164SA25P	7C186–25C
7164SA25PB	7C186A–25MB
7164SA30	7C185–25C

IDT	CYPRESS
7164SA30B	7C185A–25MB
7164SA30P	7C186–25C
7164SA30PB	7C186A–25MB
7164SA35	7C185–35C
7164SA35B	7C185A–35MB
7164SA35P	7C186–35C
7164SA35PB	7C186A–35MB
7164SA45	7C185–45C
7164SA45B	7C185A–45MB
7164SA45P	7C186–45C
7164SA45PB	7C186A–45MB
7164SA55B	7C185A–55MB
7164SA55BP	7C185A–55MB
7164SA70B	7C186A–55MB
7164SA70BP	7C186A–55MB
7164SA85B	7C185A–55MB
7164SA85BP	7C185A–55MB
71681SA100B	7C171A–45MB
71681SA25	7C171A–25C
71681SA25B	7C171A–25MB
71681SA35	7C171A–35C
71681SA35B	7C171A–35MB
71681SA45	7C171A–45C
71681SA45B	7C171A–45MB
71681SA55B	7C171A–45MB
71681SA70B	7C171A–45MB
71681SA85B	7C171A–45MB
71682SA100B	7C172A–45MB
71682SA25	7C172A–25C
71682SA25B	7C172A–25MB
71682SA35	7C172A–35C
71682SA35B	7C172A–35MB
71682SA45	7C172A–45C
71682SA45B	7C172A–45MB
71682SA55B	7C172A–45MB
71682SA70B	7C172A–45MB
71682SA85B	7C172A–45MB
7187SA15	7C187–15C
7187SA20	7C187–20C
7187SA25	7C187–25C
7187SA25B	7C187A–25MB
7187SA30	7C187–25C
7187SA30B	7C187A–25MB
7187SA35	7C187–35C
7187SA35B	7C187A–35MB
7187SA45	7C187–45C
7187SA45B	7C187A–45MB
7187SA55B	7C187A–45MB
7187SA70B	7C187A–45MB
7187SA85B	7C187A–45MB
7188SA15	7C164–15C
7188SA20	7C164–20C
7188SA20B	7C164A–20MB
7188SA25	7C164–25C
7188SA25B	7C164A–25MB
7188SA30	7C164–25C
7188SA35	7C164–35C
7188SA35B	7C164A–35MB
7188SA45	7C164–45C
7188SA45B	7C164A–45MB
7188SA55B	7C164A–45MB
7188SA70B	7C164A–45MB

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

IDT	CYPRESS
7188SA85B	7C164A–45MB
71981S35	7C161–35C
71981S35B	7C161A–35M
71981S45	7C161–45C
71981S45B	7C161A–45M
71981S55	7C161–45C
71981S55B	7C161A–45M
71981S70	7C161–45C
71981S70B	7C161A–45M
71981S85B	7C161A–45M
71982S35	7C162–35C
71982S35B	7C162A–35M
71982S45	7C162–45C
71982S45B	7C162A–45M
71982S55	7C162–45C
71982S55B	7C162A–45M
71982S70	7C162–45C
71982S70B	7C162A–45M
71982S85B	7C162A–45M
7198S35	7C166–35C
7198S35B	7C166A–35M
7198S45	7C166–45C
7198S45B	7C166A–45M
7198S55	7C166–45C
7198S55B	7C166A–45M
7198S70	7C166–45C
7198S70B	7C166A–45M
7198S85B	7C166A–45M
1B256A12	7C199–12C
1B256S12	7B199–12C
1B256S15	7B199–15C
1B256S20	7C199–20C
1B256S20B	7B199–20MB
1B258S12	7B194–12C
1B258S15	7B194–15C
1B258S20	7C194–20C
1B258S15B	7B194–15MB
1B258S20B	7B194–20MB
201LA120	7C420–65C+
201LA120B	7C420–65MB+
201LA15	7C421A–15
201LA20	7C420–20C
201LA20T	7C421–20C
201LA25	7C420–25C
201LA25T	7C421–25C
201LA30B	7C420–30MB
201LA30TB	7C421–30MB
201LA35	7C420–30C+
201LA35T	7C421–30C
201LA40B	7C420–40MB+
201LA40TB	7C421–40MB
201LA50	7C420–40C+
201LA50B	7C420–40MB+
201LA50T	7C421–40C
201LA50TB	7C421–40MB
201LA65	7C420–65C+
201LA65B	7C420–65MB+
201LA65T	7C421–65C
201LA65TB	7C421–65MB
201LA80	7C420–65C+
201LA80B	7C420–65MB+
201SA120	7C420–65C

IDT	CYPRESS
7201SA120B	7C420–65MB
7201SA15	7C421A–15
7201SA20	7C420–20C
7201SA20T	7C421–20C
7201SA25	7C420–25C
7201SA25T	7C421–25C
7201SA30B	7C420–30MB
7201SA30TB	7C421–30MB
7201SA35	7C420–30C
7201SA35T	7C421–30C
7201SA40B	7C420–40MB
7201SA40TB	7C421–40MB
7201SA50	7C420–40C
7201SA50B	7C420–40MB
7201SA50T	7C421–40C
7201SA50TB	7C421–40MB
7201SA65	7C420–65C
7201SA65B	7C420–65MB
7201SA65T	7C421–65C
7201SA65TB	7C421–65MB
7201SA80	7C420–65C
7201SA80B	7C420–65MB
7202LA120	7C424–65C+
7202LA120B	7C424–65MB+
7202LA15	7C425A–15
7202LA20	7C424–20C
7202LA20T	7C425–20C
7202LA25	7C424–25C
7202LA25T	7C425–25C
7202LA30B	7C424–30MB
7202LA30TB	7C425–30MB
7202LA35	7C424–30C+
7202LA35T	7C425–30C
7202LA40B	7C424–40MB+
7202LA40TB	7C425–40MB
7202LA50	7C424–40C+
7202LA50B	7C424–40MB+
7202LA50T	7C425–40C
7202LA50TB	7C425–40MB
7202LA65	7C424–65C+
7202LA65B	7C424–65MB+
7202LA65T	7C425–65C
7202LA65TB	7C425–65MB
7202LA80	7C424–65C+
7202LA80B	7C424–65MB+
7202SA120	7C424–65C
7202SA120B	7C424–65MB
7202SA15	7C425A–15
7202SA20	7C424–20C
7202SA20T	7C425–20C
7202SA25	7C424–25C
7202SA25T	7C425–25C
7202SA30B	7C424–30MB
7202SA30TB	7C425–30MB
7202SA35	7C424–30C
7202SA35T	7C425–30C
7202SA40B	7C424–40MB
7202SA40TB	7C425–40MB
7202SA50	7C424–40C
7202SA50B	7C424–40MB
7202SA50T	7C425–40C
7202SA50TB	7C425–40MB

IDT	CYPRESS
7202SA65	7C424–65C
7202SA65B	7C424–65MB
7202SA65T	7C425–65C
7202SA65TB	7C425–65MB
7202SA80	7C424–65C
7202SA80B	7C424–65MB
7203L20	7C428–20C
7203L20T	7C429–20C
7203L25	7C428–25C
7203L25B	7C428–25MB
7203L25T	7C429–25C
7203L25TB	7C429–25MB
7203L30	7C428–30C
7203L30T	7C429–30C
7203L35B	7C428–30MB
7203L35TB	7C429–30MB
7203L40	7C428–40C
7203L40T	7C429–40C
7203L55B	7C428–40MB
7203L55TB	7C429–40MB
7203L65	7C428–65C
7203L65B	7C428–65MB
7203L65T	7C429–65C
7203L65TB	7C429–65MB
7203L80	7C428–65C
7203L80B	7C428–65MB
7203L80T	7C429–65C
7203L80TB	7C429–65MB
7203S20	7C428–20C
7203S20T	7C429–20C
7203S25	7C428–25C
7203S25B	7C428–25MB
7203S25T	7C429–25C
7203S25TB	7C429–25MB
7203S30	7C428–30C
7203S30T	7C429–30C
7203S35B	7C428–30MB
7203S35TB	7C429–30MB
7203S40	7C428–40C
7203S40T	7C429–40C
7203S55B	7C428–40MB
7203S55TB	7C429–40MB
7203S65	7C428–65C
7203S65B	7C428–65MB
7203S65T	7C429–65C
7203S65TB	7C429–65MB
7203S80	7C428–65C
7203S80B	7C428–65MB
7203S80T	7C429–65C
7203S80TB	7C429–65MB
7204S25	7C432–25C
7204S25T	7C433–25C
7204S30	7C432–30C
7204S30T	7C433–30C
7204S35B	7C432–30MB
7204S35TB	7C433–30MB
7204S40	7C432–40C
7204S40T	7C433–40C
7204S55B	7C432–40MB
7204S55TB	7C433–40MB
7204S65	7C432–65C
7204S65B	7C432–65MB

Product Line Cross Reference

IDT	CYPRESS
7204S65T	7C433–65C
7204S65TB	7C433–65MB
7204S80B	7C432–65MB
7204S80TB	7C433–65MB
7205L20	7C460–15C
7205L25	7C460–25C
7205L30B	7C460–15MB
7205L30B	7C460–25MB
7205L35	7C460–25C
7205L50	7C460–40C
7205L50B	7C460–40MB
7206–20	7C462–20
7206–25	7C462–25
7210–120B	7C510–75M
7210–200B	7C510–75M+
7210–55B	7C510–55M
7210–65B	7C510–65M
7210–75B	7C510–75M
7210–85B	7C510–75M
7210L–45	7C510–45C+
7210L100	7C510–75C+
7210L165	7C510–75C+
7210L55	7C510–55C+
7210L65	7C510–65C+
7210L75	7C510–75C+
7216L120B	7C516–75M+
7216L140	7C516–75C+
7216L185B	7C516–75M+
7216L55	7C516–55C+
7216L55B	7C516–55M+
7216L65	7C516–65C+
7216L65B	7C516–65M
7216L75	7C516–75C+
7216L75B	7C516–75M
7216L90	7C516–75C+
7216L90B	7C516–75M+
7217L120B	7C517–75M+
7217L140	7C517–75C+
7217L185B	7C517–75M+
7217L45	7C517–45C+
7217L55	7C517–55C+
7217L55	7C517–55C+
7217L55B	7C517–55M
7217L65	7C517–65C+
7217L65B	7C517–65M
7217L75	7C517–75C+
7217L75B	7C517–75M
7217L90	7C517–75C+
7217L90B	7C517–75M+
72401L10	7C401–10C
72401L10B	7C401–10MB
72401L15	7C401–15C
72401L15B	7C401–15MB
72401L25	7C401–25C
72401L25B	7C401–25MB
72401L35	7C401–25C
72401L35B	7C401–25MB
72401L45	7C401–25C
72402L10	7C402–10C
72402L10B	7C402–10MB
72402L15	7C402–15C
72402L15B	7C402–15MB

IDT	CYPRESS
72402L25	7C402–25C
72402L25B	7C402–25MB
72402L35	7C402–25C
72402L35B	7C402–25MB
72402L45	7C402–25C
72403L10	7C403–10C
72403L10B	7C403–10MB
72403L15	7C403–15C
72403L15B	7C403–15MB
72403L25	7C403–25C
72403L25B	7C403–25MB
72403L35	7C403–25C
72403L35B	7C403–25MB
72403L45	7C403–25C
72404L10	7C404–10C
72404L10B	7C404–10MB
72404L15	7C404–15C
72404L15B	7C404–15MB
72404L25	7C404–25C
72404L25B	7C404–25MB
72404L35	7C404–25C
72404L35B	7C404–25MB
72404L45	7C404–25C
7M4016S25C	1641HD–25C
7M4016S35C	1641HD–35C
7M4016S35CB	1641HD–35MB
7M4016S45C	1641HD–45C
7M4016S45CB	1641HD–45MB
7M4016S55C	1641HD–55C
7M4016S55CB	1641HD–55MB
7M4016S70CB	1641HD–55MB
7M4017S40C	1830HD–35C
7M4017S50C	1830HD–45C
7M4017S50CB	1830HD–45MB
7M4017S55C	1830HD–55C
7M4017S60C	1830HD–55C
7M4017S60CB	1830HD–55MB
7M4017S70C	1830HD–55C
7M4017S70CB	1830HD–55MB
7M4048SXXC	M1466HD–XXC
7M4048SXXCB	M1466HD–XXMB
7M4048SXXP	M1464PD–XXC
7MB4048SXXP	M1464PD–XXC
7MC4005S20CV	1611HV–20C
7MC4005S25CV	1611HV–25C
7MC4005S25CVB	1611HV–25MB
7MC4005S30CV	1611HV–30C
7MC4005S30CVB	1611HV–30MB
7MC4005S35CV	1611HV–35C
7MC4005S35CVB	1611HV–35MB
7MC4005S45CV	1611HV–45C
7MC4005S45CVB	1611HV–45MB
7MC4005S55CV	1611HV–45C
7MC4005S55CVB	1611HV–45MB
7MC4032S20CV	1822HV–20C
7MC4032S25CV	1822HV–25C
7MC4032S30CV	1822HV–30C
7MC4032S40CV	1822HV–35C
7MC4032S50CV	1822HV–45C
7MP4008L100S	1461PS–100C
7MP4008L70S	1461PS–70C
7MP4008L85S	1461PS–85C

IDT	CYPRESS
7MP4008S35S	1460PS–35C
7MP4008S45S	1460PS–45C
7MP4008S55S	1460PS–55C
7MP4008S70S	1460PS–70C
7MP4031SXX	M1821PZ–XXC
7MP4036SXX	M1831PZ–XXC
7MP4045SXX	M1841PZ–XXC
7N4017S45C	1830HD–45C
8M624S100CB	1620HD–55MB
8M624S35C	1620HD–35C
8M624S40C	1620HD–35C
8M624S45C	1620HD–45C
8M624S50C	1620HD–45C
8M624S50CB	1620HD–45MB
8M624S60C	1620HD–55C
8M624S60CB	1620HD–55MB
8M624S70C	1620HD–55C
8M824L100C	1421HD–85C
8M824L100N	1421HD–85C
8M824S100CB	1420HD–55MB
8M824S35C	1420HD–35C
8M824S40C	1420HD–35C
8M824S45C	1420HD–45C
8M824S45CB	1420HD–45MB
8M824S45N	1423PD–45C
8M824S50C	1420HD–45C
8M824S50CB	1420HD–45MB
8M824S50N	1423PD–45C
8M824S60C	1420HD–55C
8M824S60CB	1420HD–55MB
8M824S60N	1423PD–55C
8M824S70CB	1420HD–55MB
8M824S70N	1423PD–70C
8M824S85CB	1420HD–55MB
8M824S85N	1421HD–85C
8MP824S40S	1422PS–35C
8MP824S45S	1422PS–45C
8MP824S50S	1422PS–45C
8MP824S60S	1422PS–55C
8MP824S70S	1422PS–55C
8N624S70CB	1620HD–55MB
8N624S85CB	1620HD–55MB

INTEL	CYPRESS
PREFIX:85C	PREFIX:CY
PREFIX:85C	PREFIX:PLD
PREFIX:D	SUFFIX:D
PREFIX:L	SUFFIX:L
PREFIX:P	SUFFIX:P
SUFFIX:/B	SUFFIX:B
060–10	610–10C
1223–35	7C148–35C
1223–45	7C148–45C
1223M–35	7C148–25M+
1223M–45	7C148–45M+
1400–35	7C167A–35C
1400–45	7C167A–45C
1400–55	7C167A–45C
1400M–45	7C167A–45M
1400M–55	7C167A–45M
1400M–70	7C167A–45M
1403–25	7C167A–25C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

INTEL	CYPRESS
1403−35	7C167A−35C+
1403−45	7C167A−45C+
1403−55	7C167A−45C+
1403LM−35	7C167A−35M*
1403M−35	7C167A−35M+
1403M−45	7C167A−45M+
1403M−55	7C167A−45M+
1403M−70	7C167A−45M+
1420−45	7C168A−35C
1420−55	7C168A−45C
1420M−55	7C168A−45M+
1420M−70	7C168A−45M
1421C−40	7C169A−40C
1423−25	7C168A−25C+
1423−35	7C168A−35C+
1423−40	7C168A−45C+
1423M−35	7C168A−35M*
1423M−45	7C168A−45M*
1423M−55	7C168A−45M*
1433−30	7C128A−25C+
1433−35	7C128A−35C+
1433−45	7C128A−45C+
1433−55	7C128A−55C+
1433M−35	7C128A−35M+
1433M−45	7C128A−45M+
1433M−55	7C128A−55M+
22V10−10C	PALC22V10D−7C
22V10−10C	PALC22V10D−10C
22V10−10C	PAL22V10C−7C+
22V10−10C	PAL22V10C−10C+
22V10−15C	PALC22V10B−15C
22V10−15C	PALC22V10D−15C

LATTICE	CYPRESS
PREFIX:EE	PREFIX:CY
PREFIX:GAL	PREFIX:CY
PREFIX:ST	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
GAL22V10−25LJ	PALC22V10D-25JC
GAL22V10−25LP	PALC22V10D-25PC
GAL22V10B−7LJ	PALC22V10D−7JC
GAL22V10B−7LP	PALC22V10D−7PC
GAL22V10B−10LJ	PALC22V10D-10JC
GAL22V10B−10LP	PALC22V10D-10PC
GAL22V10B−15LD /883	PALC22V10D− 15DMB
GAL22V10B−15LJ	PALC22V10D-15JC
GAL22V10B−15LJI	PALC22V10D-15JI
GAL22V10B−15LP	PALC22V10D-15PC
GAL22V10B−15LPI	PALC22V10D-15PI
GAL22V10B−15LR /883	PALC22V10D− 15LMB
GAL22V10B−20LJI	PALC22V10D-15JI
GAL22V10B−20LD /883	PALC22V10D− 15DMB
GAL22V10B−20LPI	PALC22V10D-15PI
GAL22V10B−20LR /883	PALC22V10D− 15LMB
GAL22V10B−25LD /883	PALC22V10D− 25DMB

LATTICE	CYPRESS
GAL22V10B−25LJ	PALC22V10D-25JC
GAL22V10B−25LJI	PALC22V10D-25JI
GAL22V10B−25LP	PALC22V10D-25PC
GAL22V10B−25LPI	PALC22V10D-25PI
GAL22V10B−25LR /883	PALC22V10D− 25LMB
GAL22V10B−30LD /883	PALC22V10D− 25DMB
GAL22V10B−30LR /883	PALC22V10D− 25LMB

MICROCHIP	CYPRESS
27HC64−40C	CY7C266−35C
27HC64−45C	CY7C266−45C
27HC64−55C	CY7C266−55C
27HC64−70C	CY7C266−55C
27HC191−35C	CY7C292A−35C
27HC191−40C	CY7C292A−35C
27HC191−45C	CY7C292A−35C
27HC191−55C	CY7C292A−50C
27HC291−35C	CY7C291A−35C
27HC291−40C	CY7C291A−35C
27HC291−45C	CY7C291A−35C
27HC291−55C	CY7C291A−50C
27HC256−55C	CY7C274−55
27HC256−70C	CY7C274−55C
27HC641−40C	CY7C261−40C
27HC641−45C	CY7C261−45C
27HC641−55C	CY7C261−55C
27HC641−70C	CY7C261−55C

MICRON PREFIX:MT	CYPRESS PREFIX:CY
52C4K9A1−15	7C433A−15
52C4K9A1−25	7C433−25
52C4K9A1−35	7C433−35
52C9005−15	7C421A−15
52C9005−20	7C421−20
52C9005−25	7C421−25
52C9010−15	7C425A−15
52C9010−20	7C425−20
52C9010−25	7C425−25
52C9020−15	7C429A−15
52C9020−20	7C429−20
52C9020−25	7C429−25
56C0816−25C	7C183−25C
56C0816−35C	7C183−35C
56C3816−25C	7C184−25C
56C3816−35C	7C184−35C
5C1001−25C	7C107A−25C
5C1601−15	7C167A−15C
5C1601−20C	7C167A−20C
5C1601−25C	7C167A−25C
5C1601−30	7C167A−25C
5C1601−35C	7C167A−35C
5C1604−15	7C168A−15C
5C1604−20C	7C168A−20C
5C1604−25C	7C168A−25C
5C1604−30	7C168A−25C
5C1604−35C	7C168A−35C
5C1605−15	7C170A−15C
5C1605−20C	7C170A−20C
5C1605−25C	7C170A−25C

MICRON	CYPRESS
5C1605−30	7C170A−25C
5C1605−35C	7C170A−35C
5C1606−15	7C171A−15C
5C1606−20C	7C171A−20C
5C1606−25C	7C171A−25C
5C1606−30	7C171A−25C
5C1606−35C	7C171A−35C
5C1607−15	7C172A−15C
5C1607−20C	7C172A−20C
5C1607−25C	7C172A−25C
5C1607−30	7C172A−25C
5C1607−35C	7C172A−35C
5C1608−15	7C128A−15C
5C1608−20C	7C128A−20C
5C1608−30	7C128A−25C
5C1608−30M	7C128A−25M
5C1608−25C	7C128A−25C
5C1608−25M	7C128A−25M
5C1608−35C	7C128A−35C
5C1608−35M	7C128A−35M
5C2561−12	7C197−12
5C2561−15	7C197−15
5C2561−20	7C197−20
5C2561−25	7C197−25C
5C2561−25M	7C197−25MB
5C2561−30	7C197−25C
5C2561−35	7C197−35C
5C2561−35M	7C197−35MB
5C2561−45	7C197−45C
5C2561−45M	7C197−45MB
5C2564−12	7C194−12
5C2564−15	7C194−15
5C2564−20	7C194−20
5C2564−25	7C194−25C
5C2564−25M	7C194−25MB
5C2564−30	7C194−25C
5C2564−35	7C194−35C
5C2564−35M	7C194−35MB
5C2564−45	7C194−45C
5C2564−45M	7C194−45MB
5C2565−12	7C195−12
5C2565−15	7C195−15
5C2565−20	7C195−20
5C2565−25	7C195−25C
5C2565−30	7C195−25C
5C2565−35	7C195−35C
5C2565−45	7C195−45C
5C2568−12	7C199−12
5C2568−15	7C199−15
5C2568−20	7C199−20
5C2568−25	7C199−25C
5C2568−25M	7C199−25MB
5C2568−30	7C199−25C
5C2568−35	7C199−35C
5C2568−35M	7C199−35MB
5C2568−45	7C199−45C
5C2568−45B	7C199−45MB
5C2568CW−25	7C198−25C
5C2568CW−25M	7C198−25MB
5C2568CW−30	7C198−25C
5C2568CW−35	7C198−35C
5C2568CW−35M	7C198−35MB

MICRON	CYPRESS
5C2568CW–45	7C198–45C
5C2568CW–45B	7C198–45MB
5C2568W–25	7C198–25C
5C2568W–25M	7C198–25MB
5C2568W–30	7C198–25C
5C2568W–35	7C198–35C
5C2568W–35M	7C198–35MB
5C2568W–45	7C198–45C
5C2568W–45B	7C198–45MB
5C2889	7C188
5C6401–15	7C187–15C
5C6401–20	7C187–20C
5C6401–20C	7C187–20C
5C6401–20M	7C187A–20MB
5C6401–25	7C187–25C
5C6401–25C	7C187–25C
5C6401–25M	7C187A–25MB
5C6401–30	7C187–25C
5C6401–30M	7C187A–25MB
5C6401–35	7C187–35C
5C6401–35C	7C187–35C
5C6401–35M	7C187A–35MB
5C6401–45C	7C187–45C
5C6404–12C	7B164–12C
5C6404–15	7C164–15C
5C6404–20	7C164–20C
5C6404–20M	7C164A–20MB
5C6404–25	7C164–25C
5C6404–25M	7C164A–25MB
5C6404–30	7C164–25C
5C6404–30M	7C164A–25MB
5C6404–35	7C164–35C
5C6404–35M	7C164A–35MB
5C6405–12C	7B166–12C
5C6405–15	7C166–15C
5C6405–20C	7C166–20C
5C6405–25C	7C166–25C
5C6405–30	7C166–25C
5C6405–35C	7C166–35C
5C6406–12C	7B161–12C
5C6406–15	7C161–15C
5C6406–20	7C161–20C
5C6406–25	7C161–25C
5C6406–30	7C161–25C
5C6406–35	7C161–35C
5C6407–12C	7B162–12C
5C6407–15	7C162–15C
5C6407–20	7C162–20C
5C6407–25	7C162–25C
5C6407–30	7C162–25C
5C6407–35	7C162–35C
5C6408–12	7B185–12C
5C6408–15	7C185–15C
5C6408–20C	7C185–20C
5C6408–20M	7C185A–20MB
5C6408–25C	7C185–25C
5C6408–25M	7C185A–25M
5C6408–30	7C185–25C
5C6408–30M	7C185A–25MB
5C6408–35C	7C185–35C
5C6408–35M	7C185A–35MB
85C1664–30C	1620HD–30C
85C1664–35C	1620HD–35C
85C1664–45C	1620HD–45C
85C3216–20	M1821PZ–20C
85C3216–25	M1821PZ–25C
85C3216–35	M1821PZ–35C
85C3264–20	M1831PZ–20C
85C3264–25	M1831PZ–25C
85C3264–35	M1831PZ–35C
85C8128–25	M1420PD–25C
85C8128–35	M1420PD–35C
85C8128–30C	1420HD–30C
85C8128–35C	1420HD–35C
85C8128–45C	1420HD–45C
85C8128–45C	1423PD–45C
8S1632Z–20	M1821PZ–20C
8S1632Z–25	M1821PZ–25C
8S1632Z–35	M1821PZ–35C
8S6432Z–20	M1831PZ–20C
8S6432Z–25	M1831PZ–25C
8S6432Z–35	M1831PZ–35C

MITSUBISHI	CYPRESS
PREFIX:M5L	PREFIX:CY
PREFIX:M5M	PREFIX:CY
SUFFIX:AP	SUFFIX:L
SUFFIX:FP	SUFFIX:F
SUFFIX:K	SUFFIX:D
SUFFIX:P	SUFFIX:P
21C67P–35	7C167A–35C
21C67P–45	7C167A–45C
21C67P–55	7C167A–45C
21C68P–35	7C168A–35C
21C68P–45	7C168A–45C
21C68P–55	7C168A–45C
5165L–100	7C186–55C+
5165L–120	7C186–55C+
5165L–70	7C186–55C+
5165P–100	7C186–55C+
5165P–120	7C186–55C+
5165P–70	7C186–55C+
5178P–45	7C186–45C+
5178P–55	7C186–55C+
5187P–25	7C187–25C
5187P–35	7C187–35C
5187P–45	7C187–45C
5187P–55	7C187–45C
5188P–25	7C164–25C
5188P–35	7C164–35C
5188P–45	7C164–45C
5188P–55	7C164–45C
5257J–35	7C197–35C
5257J–45	7C197–45C
5257P–35	7C197–35C
5257P–45	7C197–45C
5258J–45	7C194–45C
5258P–35	7C194–35C
5258P–45	7C194–45C
52B79P/J	7C188

MMI/AMD	CYPRESS
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:SHRP	SUFFIX:B
PAL12L10C	PLDC20G10–35C
PAL12L10M	PLDC20G10–40M
PAL14L8C	PLDC20G10–35C
PAL14L8M	PLD20G10–40M
PAL16L6C	PLD20G10–35C
PAL16L6M	PLDC20G10–40M
PAL16L8A–2C	PALC16L8–35C
PAL16L8A–2M	PALC16L8–40M
PAL16L8A–4C	PALC16L8L–35C
PAL16L8A–4M	PALC16L8–40M
PAL16L8AC	PALC16L8–25C
PAL16L8AM	PALC16L8–30M
PAL16L8B–2C	PALC16L8–35C
PAL16L8B–2M	PALC16L8–30M
PAL16L8B–4C	PALC16L8L–35C
PAL16L8B–4M	PALC16L8–40M
PAL16L8BM	PALC16L8–20M
PAL16L8C	PALC16L8–35C
PAL16L8D–4C	PALC16L8L–25C
PAL16L8D–4M	PALC16L8–30M
PAL16L8M	PALC16L8–40M
PAL16R4A–2C	PALC16R4–35C
PAL16R4A–2M	PALC16R4–40M
PAL16R4A–4C	PALC16R4L–35C
PAL16R4A–4M	PALC16R4–40M
PAL16R4AC	PALC16R4–25C
PAL16R4AM	PALC16R4–30M
PAL16R4B–2C	PALC16R4–25C
PAL16R4B–2M	PALC16R4–30M
PAL16R4B–4C	PALC16R4L–35C
PAL16R4B–4M	PALC16R4–40M
PAL16R4BM	PALC16R4–20M
PAL16R4C	PALC16R4–35C
PAL16R4D–4C	PALC16R4L–25C
PAL16R4M	PALC16R4–40M
PAL16R6A–2C	PALC16R6–35C
PAL16R6A–2M	PALC16R6–40M
PAL16R6A–4C	PALC16R6L–35C
PAL16R6A–4M	PALC16R6–40M
PAL16R6AC	PALC16R6–25C
PAL16R6AM	PALC16R6–30M
PAL16R6B–2C	PALC16R6–25C
PAL16R6B–2M	PALC16R6–30M
PAL16R6B–4C	PALC16R6L–35C
PAL16R6B–4M	PALC16R6–40M
PAL16R6BM	PALC16R6–20M
PAL16R6C	PALC16R6–35C
PAL16R6D–4C	PALC16R6L–25C
PAL16R6M	PALC16R6–40M
PAL16R8A–2C	PALC16R8–35C
PAL16R8A–2M	PALC16R8–40M
PAL16R8A–4C	PALC16R8L–35C
PAL16R8A–4M	PALC16R8–40M
PAL16R8AC	PALC16R8–25C
PAL16R8AM	PALC16R8–30M
PAL16R8B–2C	PALC16R8–25C
PAL16R8B–2M	PALC16R8–30M
PAL16R8B–4C	PALC16R8L–35C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

MMI/AMD	CYPRESS
PAL16R8B-4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8D-4C	PALC1648L-25C
PAL16R8M	PALC16R8-40M
PAL18L4C	PLDC20G10-35C
PAL18L4M	PLDC20G10-40M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20L2C	PLDC20G10-35C
PAL20L2M	PLDC20G10-40M
PAL20L8A-2C	PLDC20G10-35C
PAL20L8A-2M	PLDC20G10-40M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4A-2C	PLDC20G10-35C
PAL20R4A-2M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6A-2C	PLDC20G10-35C
PAL20R6A-2M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8A-2C	PLDC20G10-35C
PAL20R8A-2M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M
PALC22V10/A	PALC22V10-35C

MOSAIC	CYPRESS
PREFIX:MS	PREFIX:SYM
128SC-100	1420HD-85C
128SC-100	1421HD-85C
128SC-45	1420HD-45C
128SC-55	1420HD-55C
128SC-70	1420HD-70C
128SC-70	1421HD-70C

MOTOROLA	CYPRESS
PREFIX:MCM	PREFIX:CY
UFFIX:BXAJC	SUFFIX:MB
UFFIX:P	SUFFIX:P
UFFIX:S	SUFFIX:D
UFFIX:Z	SUFFIX:L
0422-10C	10E422-7C
423-45	7C168A-45C+
016H-45	6116A-45C
016H-55	6116A-55C
016H-70	6116A-55C
018-35	7C128A-35C
018-45	7C128A-45C
167H-35	7C167A-35C

MOTOROLA	CYPRESS
2167H-45	7C167A-45C
2167H-55	7C167A-45C
6164-45	7C186-45C
6168-35	7C168A-35C+
6168-45	7C168A-45C+
61L64-45	7C186-45C
6205C	7C188
6206C-15	7C199-15
6206C-20	7C199-20
6206C-25	7C199-25
6206C-35	7C199-35C
6207C-15	7C197-15
6207C-20	7C197-20
6207C-25	7C197-25
6207C-35	7C197-35
6208C-20	7C194-20
6208C-25	7C194-25
6208C-25	7C194-25C
6208C-35	7C194-35
62486FN14	7B173-14C
62486FN19	7B173-18C
62486FN24	7B173-21C
6264-15C	7B185-15C
6264-25	7C185-25C
6264-25	7C186-25C
6264-30	7C185-25C
6264-30	7C186-25C
6264-35	7C185-35C
6264-35	7C186-35C
6264-45	7C185-45C
6264-45	7C186-45C
6268P20	7C168A-20C
6268P25	7C168A-25C
6268P35	7C168A-35C
6268P40	7C168A-40C
6268P45	7C168A-45
6268P45	7C168A-45C
6269P20	7C169A-20C
6269P25	7C169A-25C
6269P35	7C169A-35C
6270-20	7C170A-20C
6270-25	7C170A-25C
6270-35	7C170A-35C
6270-45	7C170A-45C
6287-15	7C187-15C
6287-20	7C187-20C
6287-25	7C187-25C
6287-35	7C187-35C
6288-12	7B164-12C
6288-15	7C164-15C
6288-25	7C164-25C
6288-30	7C164-25C
6288-35	7C164-35C
6290-12	7B166-12C
6290-15	7C166-15C
6290-20	7C166-20C
6290-25	7C166-25C
6290-35	7C166-35C
62940FN14	7B174-14C
62940FN19	7B174-18C
62940FN24	7B174-21C
62V06D-20	7C1399-20C

MOTOROLA	CYPRESS
6706C-12	7C199-12C
6708C-12	7C194-12C
6709C-12	7C195-12C

NATIONAL	CYPRESS
PREFIX:DM	PREFIX:CY
PREFIX:GAL	PREFIX:None
PREIFX:IDM	PREFIX:CY
PREFIX:NM	PREFIX:CY
PREFIX:NMC	PREFIX:CY
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
100422-10C	100E422L-7C
100422-5C	100E422-5C
100422A-7C	100E422L-7C
100422AC	100E422L-7C
100474A-10C	100E474L-7C
100474A-8C	100E474L-7C
10422-10C	10E422L-7C
10422-5C	10E422-5C
10422A-7C	10E422L-7C
10422AC	10E422L-7C
10474A-8C	10E474L-7C
1047A-10C	10E474L-7C
12L10C	PLDC20G10-35C
14L8C	PLDC20G10-35C
14L8M	PLDC20G10-40M
16L6C	PLDC20G10-35C
16L6M	PLDC20G10-40M
16V8A-12LC	PLDC18G8-12C
16V8A-12C	PLDC18G8-12C
16V8A-15LC	PLDC18G8-15C
16V8A-15C	PLDC18G8-15C
16V8A-15LM	PLDC18G8-15MB
16V8A-15M	PLDC18G8-15MB
16V8A-20LM	PLDC18G8-20MB
16V8A-20M	PLDC18G8-20MB
18L4C	PLDC20G10-35C
18L4M	PLDC20G10-40M
20L2M	PLDC20G10-40M
2147H	2147-55C
2147H	2147-55M
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147H-3	2147-55M
2147H-3L	7C147-45C
2148H	2148-55C
2148H	7C148-C
2148H	2148-C
2148H	21L48-C
2148H-2	2148-45C
2148H-3	2148-55C
2148H-3L	21L48-55C
2148HL	21L48-55C
2901A-1C	7C901-31C
2901A-1M	7C901-32M
2901A-2C	7C901-31C
2901A-2M	7C901-32M
2901AC	7C901-31C
2901AM	7C901-32M
2909AC	2909AC

NATIONAL	CYPRESS
2909AM	2909M
2911AC	2911AC
2911AM	2911M
54S189	74S189M
54S189	7C189–M
54S189	27S03A–M
54S189	27LS03A–M
54S189A	74S189M
54S189A	7C189–25M
54S189A	7C189–M
74S189	7C189–C
74S189A	7C189–C
74S289A	7C189–C
75S07	7C190–25M
77LS181	7C282–45M
77S181	7C282–45M
77S181A	7C282–45M
77S281	7C281–45M
77S281A	7C281–45M
77S401	7C401–10M
77S401A	7C401–10M
77S402	7C402–10M
77S402A	7C402–10M
77SR181	7C235–40M
77SR476B	7C225–40M–
77SR476	7C225–40M–
85S07A	7C128–45C+
87LS181	7C282–45C
87S181	7C282–45C
87S281	7C281–45C
87S281A	7C281–45C
87S401	7C401–10C
87S401A	7C401–15C
87S402	7C402–10C
87S402A	7C402–15C
87SR181	7C235–40C
87SR476	7C225–40C
87SR476B	7C225–30C
93L422A	7C122–C
NMF512X9–15	7C421A–15
NMF512X9–25	7C421–25
NMF2048X9–20	7C429–20
NMF4096X9A–25	7C433–25
PAL10016P4–4C	100E302L–4C
PAL10016P4–6C	100E302L–4C
PAL10016P8–4C	100E301–4C
PAL10016P8–6C	100E301L–6C
PAL1016P4–4C	10E302L–4C
PAL1016P4–6C	10E302L–4C
PAL1016P8–4C	10E301–4C
PAL1016P8–6C	10E301L–6C
PAL164A2M	PALC16R4–40M
PAL16L8A2C	PALC16L8–35C
PAL16L8A2M	PALC16L8–40M
PAL16L8AC	PALC16L8–25C
PAL16L8AM	PALC16L8–30M
PAL16L8B2C	PALC16L8–25C
PAL16L8B2M	PALC16L8–30M
PAL16L8B4C	PALC16L8L–35C
PAL16L8B4M	PALC16L8–40M
PAL16L8BM	PALC16L8–20M
PAL16L8C	PALC16L8–35C

NATIONAL	CYPRESS
PAL16L8M	PALC16L8–40M
PAL16R4A2C	PALC16R4–35C
PAL16R4AC	PALC16R4–25C
PAL16R4AM	PALC16R4–30M
PAL16R4B2C	PALC16R4–25C
PAL16R4B2M	PALC16R4–30M
PAL16R4B4C	PALC16R4L–35C
PAL16R4B4M	PALC16R4–40M
PAL16R4BM	PALC16R4–20M
PAL16R4C	PALC16R4–35C
PAL16R4M	PALC16R4–40M
PAL16R6A2C	PALC16R6–35C
PAL16R6A2M	PALC16R6–40M
PAL16R6AC	PALC16R6–25C
PAL16R6AM	PALC16R6–30M
PAL16R6B2C	PALC16R6–25C
PAL16R6B2M	PALC16R6–30M
PAL16R6B4C	PALC16R6L–35C
PAL16R6B4M	PALC16R6–40M
PAL16R6BM	PALC16R6–20M
PAL16R6C	PALC16R6–35C
PAL16R6M	PALC16R6–40M
PAL16R8A2C	PALC16R8–35C
PAL16R8A2M	PALC16R8–40M
PAL16R8AC	PALC16R8–25C
PAL16R8AM	PALC16R8–30M
PAL16R8B2C	PALC16R8–25C
PAL16R8B2M	PALC16R8–30M
PAL16R8B4C	PALC16R8L–35C
PAL16R8B4M	PALC16R8–40M
PAL16R8BM	PALC16R8–20M
PAL16R8C	PALC16R8–35C
PAL16R8M	PALC16R8–40M
PAL20L10B2C	PLDC20G10–25C
PAL20L10B2M	PLDC20G10–30M
PAL20L10C	PLDC20G10–35C
PAL20L10M	PLDC20G10–40M
PAL20L2C	PLDC20G10–35C
PAL20L8AC	PLDC20G10–25C
PAL20L8AM	PLDC20G10–30M
PAL20L8BC	PLDC20G10–25C
PAL20L8BM	PLDC20G10–30M
PAL20L8C	PLDC20G10–35C
PAL20L8M	PLDC20G10–40M
PAL20R4AC	PLDC20G10–25C
PAL20R4AM	PLDC20G10–30M
PAL20R4BC	PLDC20G10–25C
PAL20R4BM	PLDC20G10–30M
PAL20R4C	PLDC20G10–35C
PAL20R4M	PLDC20G10–40M
PAL20R6AC	PLDC20G10–25C
PAL20R6AM	PLDC20G10–30M
PAL20R6BC	PLDC20G10–25C
PAL20R6BM	PLDC20G10–30M
PAL20R6C	PLDC20G10–35C
PAL20R6M	PLDC20G10–40M
PAL20R8AC	PLDC20G10–25C
PAL20R8AM	PLDC20G10–30M
PAL20R8BC	PLDC20G10–25C
PAL20R8BM	PLDC20G10–30M
PAL20R8C	PLDC20G10–35C
PAL20R8M	PLDC20G10–40M

NEC	CYPRESS
PREFIX:uPD	PREFIX:CY
SUFFIX:C	SUFFIX:P
SUFFIX:D	SUFFIX:D
SUFFIX:K	SUFFIX:L
SUFFIX:L	SUFFIX:F
100422–10C	100E422L–7C
100422–7C	100E422L–7C
100470–10C	100E470–7C
100470–15C	100E470–7C
100474–10C	100E474L–7C
100474–4.5	100E474–3.5C
100474–6	100E474–5C
100474–8C	100E474L–7C
100474A–5	100E474L–5C
100474A–6	100E474L–5C
100474E–4	100E474–3.5C
100484–10	100E484L–7C
100484–15	100E484L–7C
100A484–5	100E484–5C
100A484–7	100E484L–7C
10422–10C	10E422L–7C
10422–7C	10E422L–7C
10470–10C	10E470–7C
10470–15C	10E470–7C
10474–10C	10E474L–7C
10474–8C	10E474L–7C
10474A–5	10E474L–5C
10474A–6	10E474L–5C
10474E–4	10E474–4C
10484–10	10E484L–7C
10484–15	10E484L–7C
10A484–5	10E484–5C
10A484–7	10E484L–7C
2147–2	2147–55C
2147–3	2147–55C
2147A–25	7C147–25C
2147A–35	2147–35C
2147A–45	2147–45C
2149	2149–55C
2149–1	2149–45C
2149–2	2149–35C
2167–2	7C167A–45C
2167–3	7C167A–45C
27HC65–25	7C263/4–25C
27HC65–35	7C263/4–35C
27HC65–45	7C263/4–45C
4311–45	7C167A–45C
4311–55	7C167A–45C
43254C–35	7C194–35
43254C–45	7C194–45
4361–40	7C187–35C
4361–45	7C187–45C
4361–55	7C187–45C
4361–70	7C187–45C
4362–45	7C164–45C
4362–55	7C164–45C
4362–70	7C164–45C
4363–45	7C166–45C
4363–55	7C166–45C
4363–70	7C166–45C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

PARADIGM	CYPRESS
PREFIX:PDM	PREFIX:CY
41251L	7C191–C
41251LB	7C191–MB*
41251S	7C191–C
41251SB	7C191–MB
41252L	7C192–C
41252LB	7C192–MB*
41252S	7C192–C
41252SB	7C192–MB
41256L	7C199/8–C*
41256LB	7C199/8–MB*
41256S	7C199/8–C
41256SB	7C199/8–MB
41258L	7C194–C*
41258LB	7C194–B*
41258S	7C194–C
41258SB	7C194–B

PERFORMANCE	CYPRESS
PREFIX:P	PREFIX:CY
SUFFIX:L	SUFFIX:L
SUFFIX:S	SUFFIX:S
1256–35	7C199–35
1256–45	7C199–45
C1256–25	7C199–25
C1256–35	7C199–35
C1256–45	7C198–45
C1257–25	7C197–25
C1257–35	7C197–35
C1257–45	7C197–45
C1258–25	7C194–25
C1258–35	7C194–35
C1258–45	7C194–45
C150–12C	7C150–12C
C150–15C	7C150–15C
C150–15M	7C150–15M
C150–20C	7C150–15C
C150–20M	7C150–15M
C150–25C	7C150–25C
C150–25M	7C150–25M
C150–35M	7C150–35M
C164DW–20C	7C186–20C
C164DW–25C	7C186–25C
C164DW–25M	7C186A–25M
C164DW–35C	7C186–35C
C164DW–35M	7C186A–35M
C164DW–45C	7C186–45C
C164DW–45M	7C186A–45M
C164DW–55C	7C186–55C
C164DW–55M	7C186A–55M
C164P–20C	7C185–20C
C164P–25C	7C185–25C
C164P–25M	7C185A–25M
C164P–35C	7C185–35C
C164P–35M	7C185A–35M
C164P–45C	7C185–45C
C164P–45M	7C185A–45M
C164P–55C	7C185–55C
C164P–55M	7C185A–55M
C1681–25C	7C171A–25C
C1681–35C	7C171A–35C
C1681–35M	7C171A–35M

PERFORMANCE	CYPRESS
4C1681–45C	7C171A–45C
4C1681–45M	7C171A–45M
4C1682–25C	7C172A–25C
4C1682–35C	7C172A–35C
4C1682–35M	7C172A–35M
4C1682–45C	7C172A–45C
4C1682–45M	7C172A–45M
4C169–25C	7C169A–25C
4C169–30C	7C169A–25C
4C169–35C	7C169A–35C
4C169–35M	7C169A–35M
4C169–45M	7C169A–45M
4C187–20C	7C187–20C
4C187–25C	7C187–25C
4C187–25M	7C187A–25M
4C187–35M	7C187A–35M
4C188–20C	7C164–20C
4C188–25C	7C164–25C
4C188–25M	7C164A–25M
4C188–35C	7C164–35C
4C188–35M	7C164A–35M
4C188–45M	7C164A–45M
4C198–20C	7C166–20C
4C198–25C	7C166–25C
4C198–25M	7C166A–25M
4C198–35C	7C166–35C
4C198–35M	7C166A–35M
4C198–45M	7C166A–45M
4C1981–20C	7C161–20C
4C1981–25C	7C161–25C
4C1981–25M	7C161A–25M
4C1981–35C	7C161–35C
4C1981–35M	7C161A–35M
4C1981–45M	7C161A–45M
4C1981–55M	7C161A–55M
4C1982–20C	7C162–20C
4C1982–25C	7C162–25C
4C1982–25M	7C162A–25M
4C1982–35C	7C162–35C
4C1982–35M	7C162A–35M
4C1982–45M	7C162A–45M
4C1982–55M	7C162A–55M
93U422–35C	7C122–15C
93U422–35C	7C122–25C
93U422–35C	7C122–35C
93U422–35M	7C122–25M
93U422–35M	7C122–35M

QUICKLOGIC	CYPRESS
PREFIX:QL	PREFIX:CY
12X16–0XX68C	7C383–0C
12X16–0XX68I	7C383–0I
12X16–0XX84C	7C384–0C
12X16–0XX84I	7C384–0I
12X16–1XX68C	7C383–1C
12X16–1XX68I	7C383–1I
12X16–1XX84C	7C384–1C
12X16–1XX84I	7C384–1I
12X16–2XX68C	7C383–2C
12X16–2XX84C	7C384–2C
8X12–0XX44C	7C381–0C
8X12–0XX44I	7C381–0I

QUICKLOGIC	CYPRESS
8X12–0XX68C	7C382–0C
8X12–0XX68I	7C382–0I
8X12–1XX44C	7C381–1C
8X12–1XX44I	7C381–1I
8X12–1XX68C	7C382–1C
8X12–1XX68I	7C382–1I
8X12–2XX44C	7C381–2C
8X12–2XX68C	7C382–2C

SAMSUNG	CYPRESS
PREFIX:KM	PREFIX:CY
61257A–25	7C197–25C
61257A–35	7C197–35C
61257A–45	7C197–45C
64257A–25	7C194–25C
64257A–35	7C194–35C
64257A–45	7C194–45C
75C01A–15	7C421A–15
75C01A–20	7C421–20C
75C01A–25	7C421–25C
75C01A–35	7C421–30C
75C01A–50	7C421–40C
75C01A–80	7C421–65C
75C01AP–20	7C420–20C
75C01AP–25	7C420–25C
75C01AP–35	7C420–35C
75C01AP–50	7C420–50C
75C01AP–80	7C420–80C
75C02A–15	7C425A–15
75C02A–20	7C425–20C
75C02A–25	7C425–25C
75C02A–35	7C425–30C
75C02A–50	7C425–40C
75C02A–80	7C425–65C
75C02AP–20	7C424–20C
75C02AP–25	7C424–25C
75C02AP–35	7C424–30C
75C02AP–50	7C424–40C
75C02AP–80	7C424–65C
75C03A–15	7C429A–15
75C03A–20	7C429–20C
75C03A–25	7C429–25C
75C03A–35	7C429–30C
75C03A–50	7C429–40C
75C03A–80	7C429–65C
75C03AP–20	7C428–20C
75C03AP–25	7C428–25C
75C03AP–35	7C428–30C
75C03AP–50	7C428–40C
75C03AP–80	7C428–65C
75C102A–20	7C425–20C
75C102A–25	7C425–25C
75C102A–35	7C425–25C
75C102A–80	7C425–65C

SHARP	CYPRESS
PREFIX:LH	PREFIX:CY
52251–35	7C197–35C
52251–45	7C197–45C
52252–35	7C194–35C
52252–45	7C194–45C
52254D–25	7C199–25C

SHARP	CYPRESS
52254D-35	7C199-35C
52254D-45	7C199-45C
52259	7C188
5481-15	7C408A-15C
5481-25	7C408A-25C
5481-35	7C408A-35C
5491-15	7C409A-15C
5491-25	7C409A-25C
5491-35	7C409A-35C
5496-20	7C420-20C
5496-35	7C420-30C
5496-50	7C420-40C
5496D-15	7C421A-15
5496D-20	7C421-20C
5496D-35	7C421-30C
5496D-50	7C421-40C
5497-20	7C424-20C
5497-35	7C424-30C
5497-50	7C424-40C
5497D-15	7C425A-15
5497D-20	7C425-20C
5497D-35	7C425-30C
5497D-50	7C425-40C
5498-20	7C428-20C
5498-35	7C428-30C
5498-50	7C428-40C
5498D-15	7C429A-15
5498D-20	7C429-20C
5498D-35	7C429-30C
5498D-50	7C429-40C
5499-35	7C432-30C
5499-50	7C432-40C
5499D-15	7C433A-15
5499D-35	7C433-30C
5499D-50	7C433-40C
5749/J-55	7C263/4-55C
5749/J-70	7C263/4-55C

SIGNETICS	CYPRESS
SUFFIX:G	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:R	SUFFIX:F
100422BC	100E422-7C
100422CC	100E422-7C
100474AC	100E474-7C
10422BC	10E422-7C
10422CC	10E422-7C
10474AC	10E474-7C
27HC641-45C	7C263/4-45C
27HC641-55C	7C263/4-55C
N74S189	74S189C
N82HS641	7C263/4-55C
N82HS641A	7C263/4-45C
N82HS641B	7C263/4-35C
N82HS641C	7C263/4-25C
N82LHS191-3	7C291A-35C
N82LHS191-6	7C292A-35C
N82S181	7C281/2-45C
N82S181A	7C281/2-45C
N82S181C	7C281/2-30C
N82S191-3	7C291A-50C
N82S191-6	7C292A-50C

SIGNETICS	CYPRESS
N82S191A-3	7C291A-50C
N82S191A-6	7C292A-50C
N82S191C-3	7C291A-35C
N82S191C-6	7C292A-35C
S82HS641	7C263/4-55M
S82LS181	7C282-45M
S82S181	7C282-45M
S82S181A	7C282-45M
S82S191-3	7C291A-50M
S82S191-6	7C292A-50M
S82S191A-3	7C291A-50M
S82S191A-6	7C292A-50M
S82S191B-3	7C291A-50M
S82S191B-6	7C292A-50M

SONY	CYPRESS
PREFIX:CXK	PREFIX:CY
51256P-35	7C197-35
51256P-45	7C197-45
54256P-35	7C194-35
54256P-45	7C194-45
58255AJ-25	7C199-25
58255AP-25	7C199-25
58258P-35	7C198-35
58258P-45	7C198-45
58258SP-35	7C199-35
58258SP-45	7C199-45

TI	CYPRESS
PREFIX:JBP	PREFIX:CY
PREFIX:PAL	SUFFIX:P
PREFIX:SM	PREFIX:CY
PREFIX:SMJ	PREFIX:CY
PREFIX:SN	PREFIX:CY
PREFIX:TBP	PREFIX:CY
PREFIX:TIB	PREFIX:CY
PREFIX:TMS	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:L
SUFFIX:N	SUFFIX:D
10016P8-6C	100E301L-6C
10H16P8-6C	10E301L-6C
22V10AC	PALC22V10-25C
22V10AM	PALC22V10-30M
54HC189	7C189-25M
54HCT189	7C189-25M
54LS189A	27LS03M
54LS219A	7C190-25M+
54S189A	74S189M
61CD256-35	7C197-35M
61CD256-45	7C197-45M
64C256-35	7C194-35M
64C256-45	7C194-45M
68CE256-35	7C198-35M
68CE256-45	7C198-45M
7489	7C189-25C
74ACT29116	7C9116AC
74ACT29116-1	7C9116AC
74HC189	7C189-25C
74HC219	7C190-25C
74HCT189	7C189-25C
74LS189A	27LS03C

TI	CYPRESS
74LS219A	27S07C+
74S189A	74S189C
74S189B	7C189-25C
HCT9510E	7C510-75C+
HCT9510E-10	7C510-75C+
HCT9510M	7C510-75M+
PAL16L8-20M	PALC16L8-20M
PAL16L8-25C	PALC16L8-25C
PAL16L8-30M	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16R4-20M	PALC16R4-20M
PAL16R4-25C	PALC16R4-25C
PAL16R4-30M	PALC16R4-30M
PAL16R4A-2C	PALC16R4-25C
PAL16R4A-2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R6-20M	PALC16R6-20M
PAL16R6-25C	PALC16R6-25C
PAL16R6-30M	PALC16R6-30M
PAL16R6A-2C	PALC16R6-25C
PAL16R6A-2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R8-20M	PALC16R8-20M
PAL16R8-25C	PALC16R8-25C
PAL16R8-30M	PALC16R8-30M
PAL16R8A-2C	PALC16R8-25C
PAL16R8A-2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL20L10A-2C	PLDC20G10-25C
PAL20L10A-2M	PLDC20G10-30M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L8A-2C	PLDC20G10-25C
PAL20L8A-2M	PLDC20G10-30M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20R4A-2C	PLDC20G10-25C
PAL20R4A-2M	PLDC20G10-30M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R6A-2C	PLDC20G10-25C
PAL20R6A-2M	PLDC20G10-30M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R8A-2C	PLDC20G10-25C
PAL20R8A-2M	PLDC20G10-30M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL22V10-7C	PALC22V10D-7C
PAL22V10-7C	PAL22V10C-7C
PAL22V10-15C	PALC22V10B-15C
PAL22V10-20M	PALC22V10B-20M
PAL22V10AC	PALC22V10-25C
PAL22V10AC	PALC22V10L-25C
PAL22V10AM	PALC22V10-25M
PAL22V10AM	PALC22V10-30M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

TI	CYPRESS
PAL22V10C	PALC22V10-35C
PAL22V10C	PALC22V10L-35C
SN74ACT7201LA15	7C421A-15
SN74ACT7201LA25	7C421-25
SN74ACT7202LA15	7C425A-15
SN74ACT7202LA25	7C425-25
SN74ACT7203L15	7C429A-15
SN74ACT7203L25	7C429-25
SN74ACT7204L15	7C433A-15
SN74ACT7204L25	7C433-25

TOSHIBA	CYPRESS
PREFIX:P	SUFFIX:P
PREFIX:TC	PREFIX:CY
PREFIX:TMM	PREFIX:CY
SUFFIX:D	SUFFIX:D
2015A-10	7C128A-55C+
2015A-12	7C128A-55C+
2015A-15	7C128A-55C+
2015A-90	7C128A-55C+
2018-25	7C128A-25C
2018-35	7C128A-35C
2018-45	7C128A-45C
2018-55	7C128A-55C+
2018AP-35	7C128A-35C
2018AP-45	7C128A-45C
2068-25	7C168A-25C
2068-35	7C168A-35C
2068-45	7C168A-45C
2068-55	7C168A-45C
2069-35	7C169A-35C
2078-35	7C170A-35C
2078-45	7C170A-45C
2078-55	7C170A-45C
2088-35	7C186-35C
2088-45	7C186-45C
2088-55	7C186-55C
2115	2147-55C
2115-1	2147-55C
25187T-25	7C183-25C
25187T-30	7C183-25C
25188T-25	7C184-25C
25188T-30	7C184-25C
25257-10	7C199-55C
25257-12	7C199-55C
25257-70	7C199-55C
25257-85	7C199-55C
25328-17	7C199-15C
25328-20	7C199-20C
25328-25	7C199-25C
25328-35	7C199-35C
25328P/J-25	7C199-25C
25328P/J-35	7C199-35C
25329P/J	7C188
25416-35	7C164-35C
25416-45	7C164-45C
25417-25	7C166-25C
25417-35	7C166-35C
25417-45	7C166-45C
25417P/J-15	7C166-15C
25417P/J-20	7C166-20C
25417P/J-25	7C166-25C

TOSHIBA	CYPRESS
55417P/J-35	7C166-35C
55464-17	7B194-15C
55464-20	7C194-20C
55464-25	7C194-25C
55464-35	7C194-35C
55464P/J-25	7C194-25C
55464P/J-35	7C194-35C
55465-17	7B196-15C
55465-20	7C196-20C
55465-25	7C196-25C
55465-35	7C196-35C
55465P/J-25	7C195-25C
55465P/J-35	7C195-35C
5561-45	7C187-45C+
5561-55	7C187-45C+
5561-70	7C187-45C+
5561P/J-45	7C187-45C
5561P/J-55	7C187-35C
5561P/J-70	7C187-45C
5562-35	7C187-35C
5562-45	7C187-45C
5562-55	7C187-45C
5562P/J-35	7C187-45C
5562P/J-45	7C187-45C
5562P/J-55	7C187-45C
5563-10	7C185-55C
5563-12	7C185-55C
5563-15	7C185-55C
5565-10	7C186-55C
5565-12	7C186-55C
5565-15	7C186-55C
5588P/J-20	7C185-20C
5588P/J-25	7C185-25C
5589P/J-25	7C182-25C
55B328-12	7B199-12C
55B328-15	7B199-15C
55B464-12	7B194-12C
55B464-15	7B194-15C
55B465-12	7B196-12C
55B465-15	7B196-15C

VTI (VLSI)	CYPRESS
PREFIX:VL	PREFIX:CY
PREFIX:VT	PREFIX:CY
2010-65	7C510-65C
2010-70	7C510-65C
2010-90	7C510-75C
2130-10C	7C130-55C
2130-12C	7C130-55C
2130-15C	7C130-55C
7132-55	7C132-55C
7132-55C	7C132-55C
7132-70	7C132-55C
7132-70C	7C132-55C
7132-90C	7C132-55C
7132A-25C	7C132-25C
7132A-30C	7C132-25C
7132A-35	7C132-35C
7132A-35C	7C132-35C
7132A-45	7C132-45C
7132A-45C	7C132-45C
7142-55	7C142-55C

VTI (VLSI)	CYPRESS
7142-55C	7C142-55C
7142-70	7C142-55C
7142-70C	7C142-55C
7142-90C	7C142-55C
7142A-25C	7C142-25C
7142A-30C	7C142-25C
7142A-35	7C142-35C
7142A-35C	7C142-35C
7142A-45	7C142-45C
7142A-45C	7C142-45C

WSI	CYPRESS
PREFIX:WS	PREFIX:CY
SUFFIX:C	PREFIX:CY
SUFFIX:D	PREFIX:CY
SUFFIX:M	SUFFIX:P
SUFFIX:P	PREFIX:CY
29C01C	7C901-31C
57C45-25C	7C245A-25C
57C45-25M	7C245A-25M
57C45-35C	7C245A-35C
57C45-35M	7C245A-35M
57C45-45C	7C245A-45C
57C45-45M	7C245A-45M
57C49B-35C	7C263/4-35C
57C49B-45C	7C263/4-45C
57C49B-45M	7C263/4-45C
57C49B-55C	7C263/4-55C
57C49B-55M	7C263/4-55C
57C49B-70C	7C263/4-55C
57C49B-70M	7C263/4-55C
57C49C-25C	7C263/4-25C
57C49C-35C	7C263/4-35C
57C49C-45C	7C263/4-45C
57C49C-45M	7C263/4-45C
57C49C-55C	7C263/4-55C
57C49C-55M	7C263/4-55C
57C49C-70C	7C263/4-55C
57C49C-70M	7C263/4-55C
57C51C-45C	7C251/4-45C
57C51C-45M	7C251/4-45M
57C51C-55C	7C251/4-55C
57C51C-55M	7C251/4-55M
57C51C-70C	7C251/4-55M
57C51C-70M	7C251/4-55M
57C71C-35C	7C271-35C
57C71C-45C	7C271-45C
57C71C-55C	7C271-55C
57C71C-55M	7C271-55M
57C71C-70C	7C271-55M
57C71C-70M	7C271-55M
57C191B-35C	7C292-35C
57C191B-35M	7C292-35M
57C191B-45C	7C292-35C
57C191B-45M	7C292-35M
57C191B-50M	7C292A-50M
57C191B-55C	7C292A-50C
57C191B-55M	7C292A-50M
57C191C-25C	7C292A-25C
57C191C-35C	7C292A-35C
57C191C-45C	7C292-35C
57C191C-45M	7C292-35M

WSI	CYPRESS
57C191C–55C	7C292–50C
57C191C–55M	7C292–50M
57C256F–35C	7C274–35C
57C256F–45C	7C274–45C
57C256F–55C	7C274–55C
57C256F–55M	7C274–55M
57C291B–35C	7C291–35C
57C291B–35M	7C291–35M
57C291B–45C	7C291–35C
57C291B–45M	7C291–35M
57C291B–50M	7C291–50M
57C291B–55C	7C291–50C
57C291B–55M	7C291–50M
57C291C–25C	7C291A–25C
57C291C–35C	7C291A–35C
57C291C–45C	7C291–35C
57C291C–45M	7C291–35M
57C291C–55C	7C291–50C
57C291C–55M	7C291–50M
57C64F–55C	7C266–55C
5901C	2901CC+
5901M	2901CM+
5910AC	7C910–40C
5910AM	7C910–46M
59510	7C510
59516	7C516–45C
59517	7C517–45C

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Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}

* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}

– = functionally equivalent

† = SOIC only

‡ = 32-pin LCC crosses to the 7C198M

CYPRESS SEMICONDUCTOR

Section Contents

Static RAMs (Random Access Memory)

Static RAMs (Random Access Memory) (continued)

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C101A
CY7C102A

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Transparent write (7C101A)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 μW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C101A and CY7C102A are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

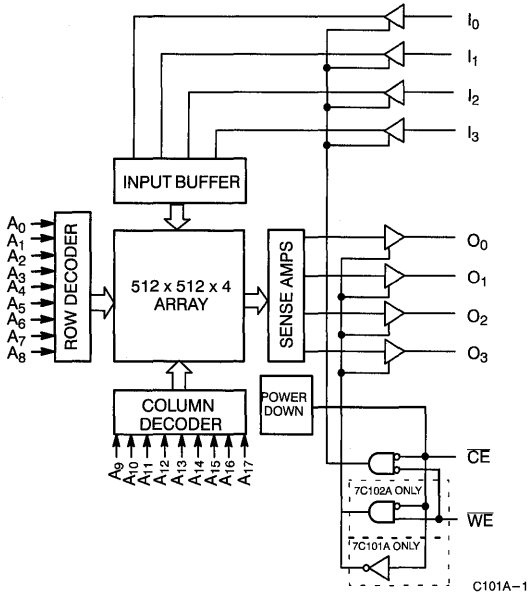
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

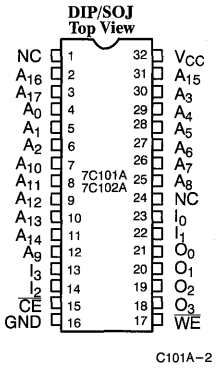
The data output pins on the CY7C101A and the CY7C102A are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C102A's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C101A, the output pins will carry the same data as the inputs after a specified delay.

The CY7C101A and CY7C102A are available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C101A–12 7C102A–12	7C101A–15 7C102A–15	7C101A–20 7C102A–20	7C101A–25 7C102A–25	7C101A–35 7C102A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C101A−12 7C102A−12 Min.	7C101A−12 7C102A−12 Max.	7C101A−15 7C102A−15 Min.	7C101A−15 7C102A−15 Max.	7C101A−20 7C102A−20 Min.	7C101A−20 7C102A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+1	− 1	+1	− 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 5	+5	− 5	+5	− 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140	mA
			Mil				165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Electrical Characteristics Over the Operating Range[3] (continued)

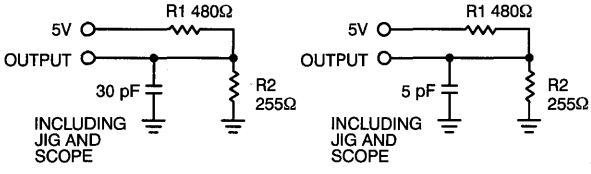
Parameter	Description	Test Conditions		7C101A–25 7C102A–25 Min.	7C101A–25 7C102A–25 Max.	7C101A–35 7C102A–35 Min.	7C101A–35 7C102A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+ 1	− 1	+ 1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 5	+ 5	− 5	+ 5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		130		125	mA
			Mil		140		135	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

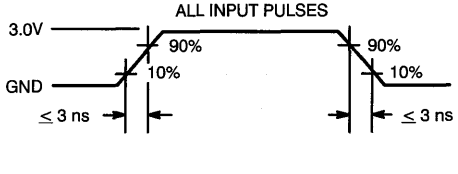
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

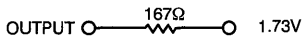
Notes:
1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C101A–12 7C102A–12		7C101A–15 7C102A–15		7C101A–20 7C102A–20		7C101A–25 7C102A–25		7C101A–35 7C102A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{ADV}	Data Valid to Output Valid (7C101A)		12		15		20		25		35	ns

Notes:

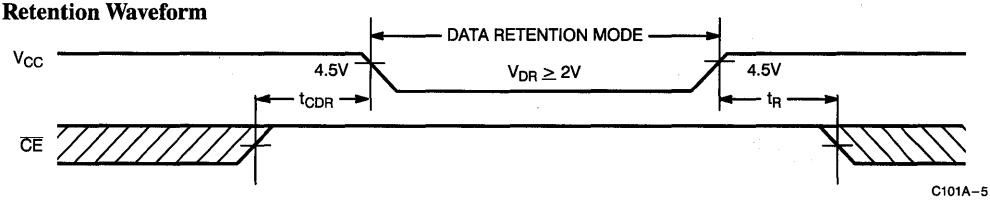
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	μA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

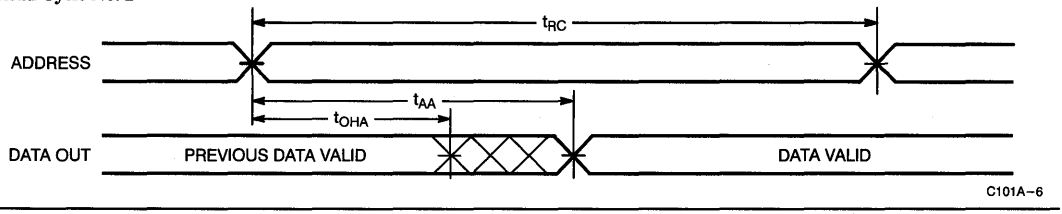
Note:
10. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

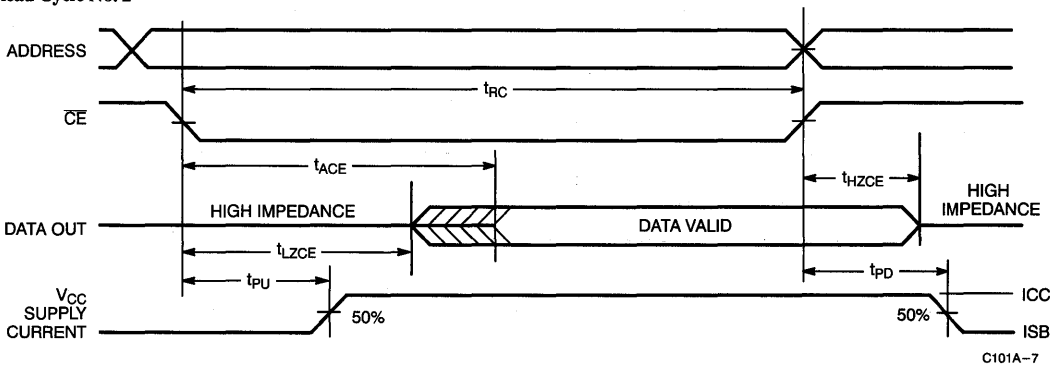


Switching Waveforms

Read Cycle No. 1[11, 12]

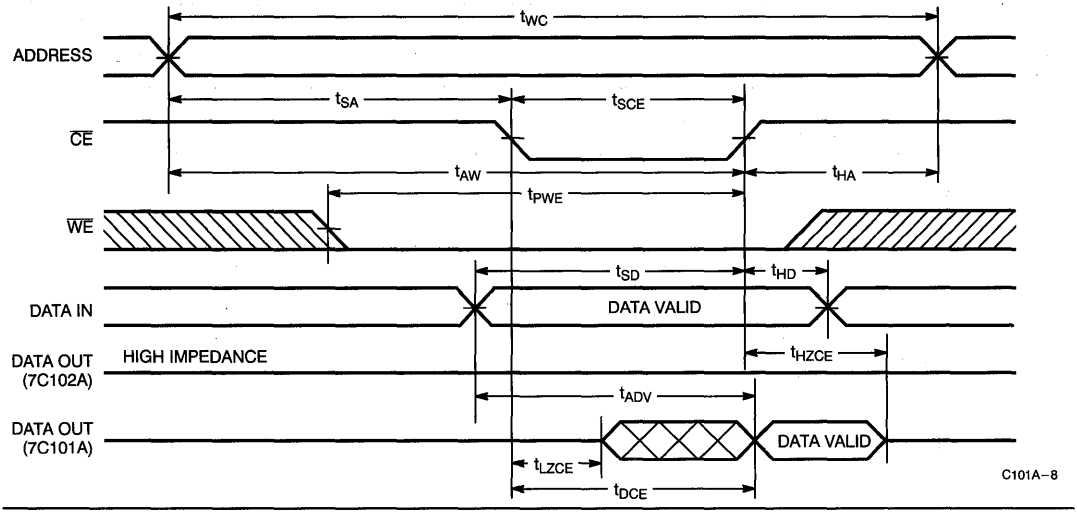


Read Cycle No. 2[12, 13]

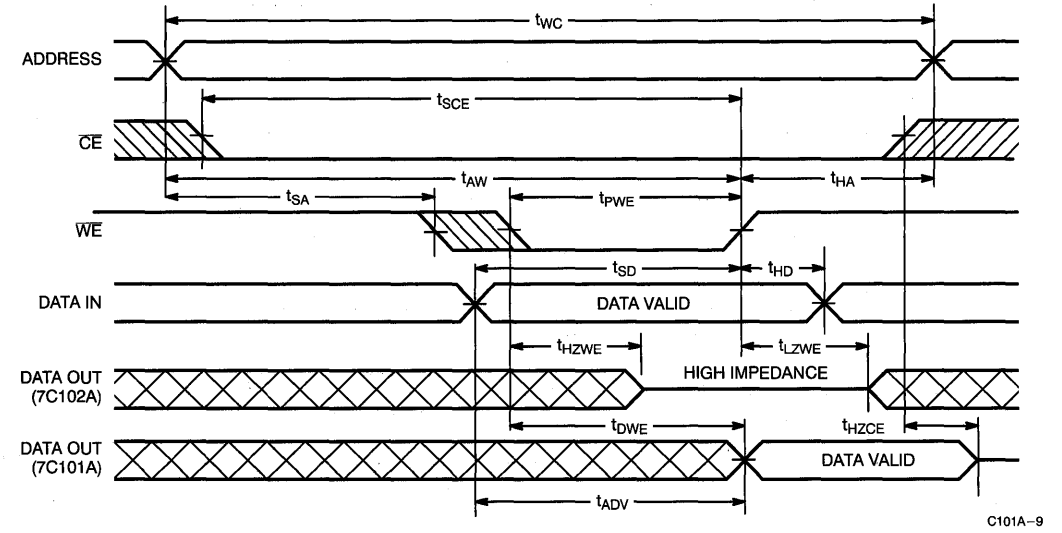


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Notes:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C102A only).

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C102A: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C101A: Transparent Write[15]	Active (I_{CC})

Note:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	PackageType	Operating Range
12	CY7C101A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C101A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C101A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C101A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C101A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C102A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C102A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C102A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C102A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C102A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}[16]	7, 8, 9, 10, 11

Note:
16. 7C101A only.

Document #: 38−00231

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C106A**

256K x 4 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C106A is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

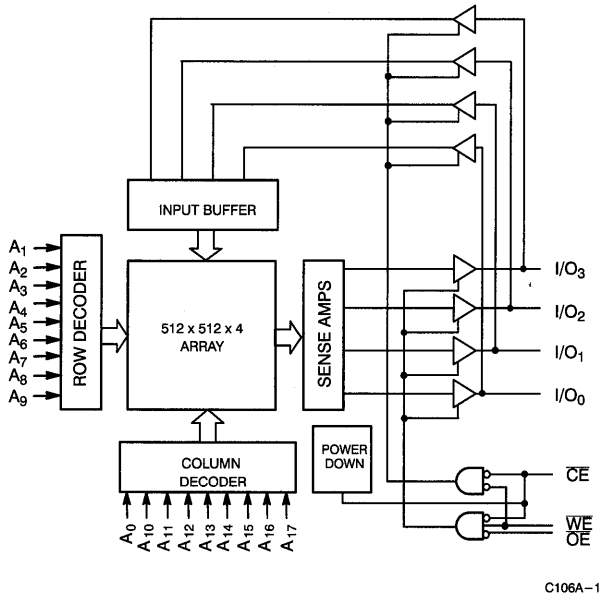
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

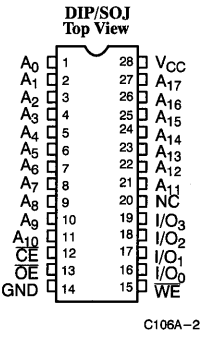
The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C106A is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C106A–12	7C106A–15	7C106A–20	7C106A–25	7C106A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C106A–12 Min.	7C106A–12 Max.	7C106A–15 Min.	7C106A–15 Max.	7C106A–20 Min.	7C106A–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 1	+1	– 1	+1	– 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	– 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300		– 300	mA
I_{CC}	V_{CC} Operating SupplyCurrent	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140	mA
			Mil				165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Notes:

1. V_{IL} (min.) = – 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3]

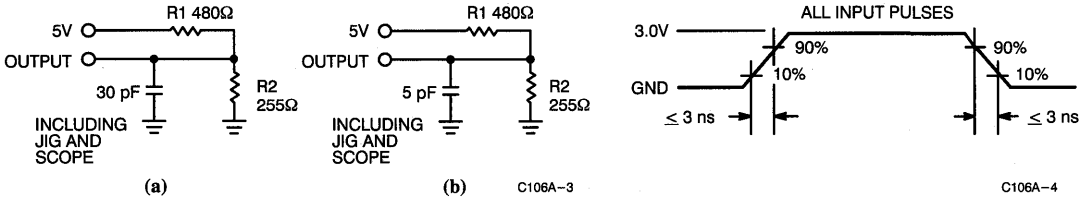
Parameter	Description	Test Conditions		7C106A–25 Min.	7C106A–25 Max.	7C106A–35 Min.	7C106A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	– 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300	mA
I_{CC}	V_{CC} Operating SupplyCurrent	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		130		125	mA
			Mil		140		135	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

Capacitance[5]

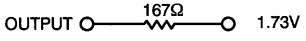
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3,6]

Parameter	Description	7C106A–12		7C106A–15		7C106A–20		7C106A–25		7C106A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9,10]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]		6		7		8		10		10	ns

Notes:

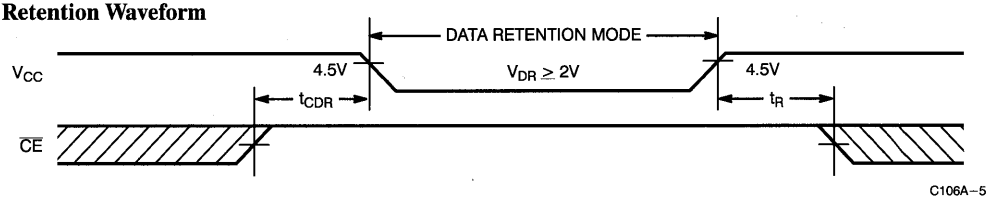
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

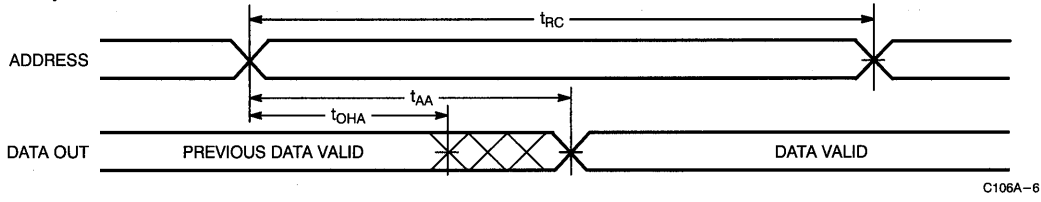
Note:
11. No input may exceed V_{CC} +0.5V.

Data Retention Waveform

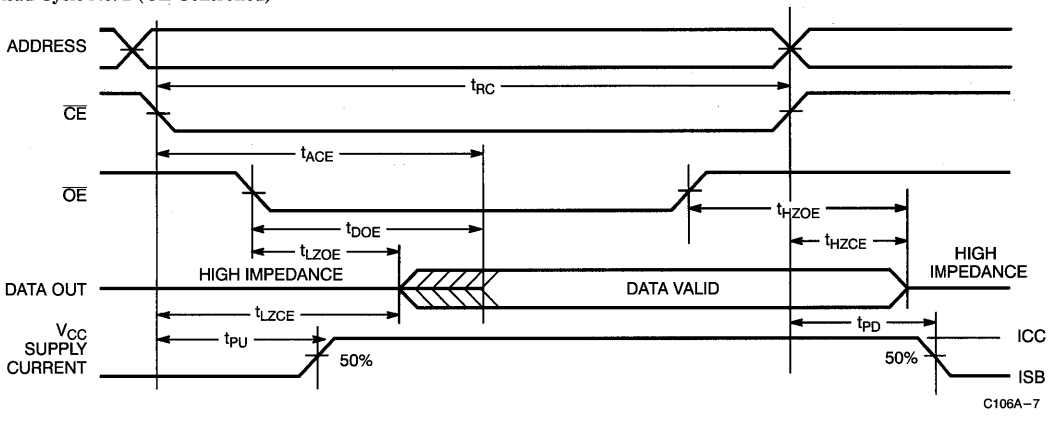


Switching Waveforms

Read Cycle No. 1[12, 13]

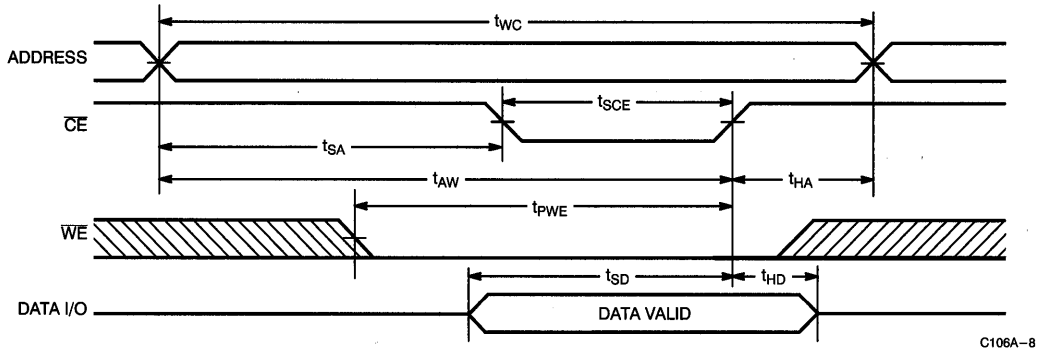


Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]

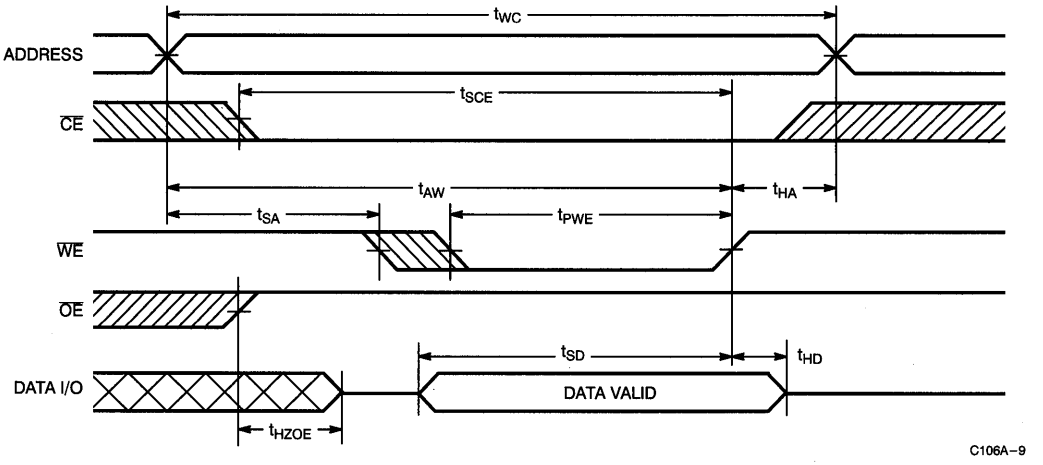


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

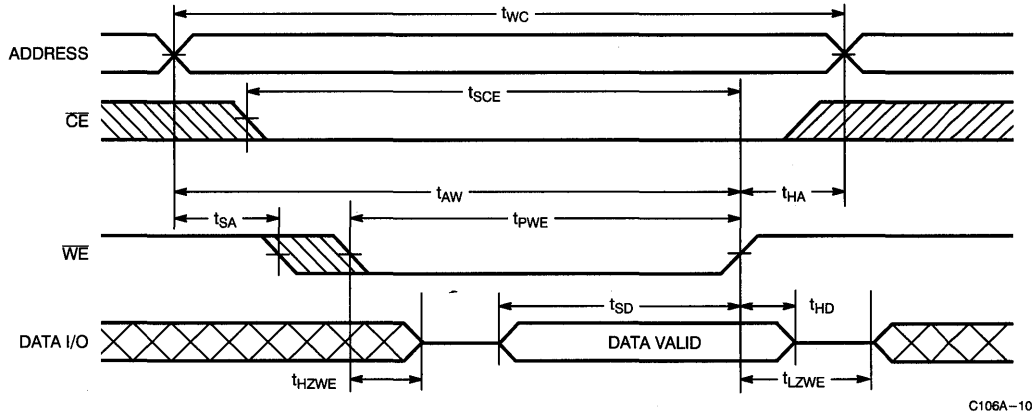


Notes:

12. Device is continuously selected, $\overline{OE}$ and $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C106A–12PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–12VC	V28	28-Lead (400-Mil) Molded SOJ	
15	CY7C106A–15PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–15VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–15DMB	D42	28-Lead (400-Mil) CerDIP	Military
20	CY7C106A–20PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–20VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–20DMB	D42	28-Lead (400-Mil) CerDIP	Military
25	CY7C106A–25PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–25VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–25DMB	D42	28-Lead (400-Mil) CerDIP	Military
35	CY7C106A–35PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–35VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–35DMB	D42	28-Lead (400-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00230

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C107A**

1M x 1 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 825 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C107A is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

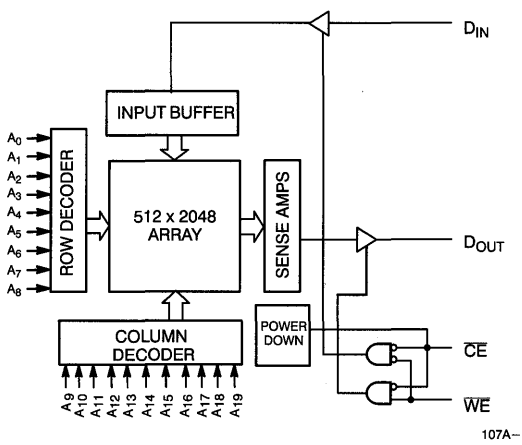
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C107A is available in standard 400-mil-wide DIPs and SOJs.

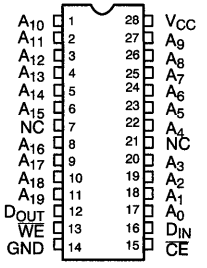
Logic Block Diagram



107A–1

Pin Configuration

DIP/SOJ
Top View



107A–2

Selection Guide

		7C107A–12	7C107A–15	7C107A–20	7C107A–25	7C107A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	150	135	125	120	110
	Military		145	135	130	120
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics[3] Over the Operating Range

Parameter	Description	Test Conditions		7C107A−12 Min.	7C107A−12 Max.	7C107A−15 Min.	7C107A−15 Max.	7C107A−20 Min.	7C107A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+1	− 1	+1	− 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 5	+5	− 5	+5	− 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		135		125	mA
			Mil				145		135	
I_{SB1}	Automatic CE Power-Down Current − TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Electrical Characteristics[3] Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C107A–25 Min.	7C107A–25 Max.	7C107A–35 Min.	7C107A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 1	+1	– 1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		120		110	mA
			Mil		130		120	
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

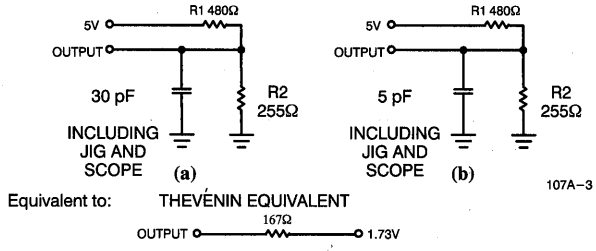
Capacitance[5]

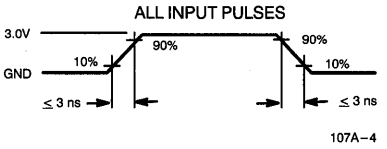
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics[3,6] Over the Operating Range

Parameter	Description	7C107A–12		7C107A–15		7C107A–20		7C107A–25		7C107A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns

Notes:

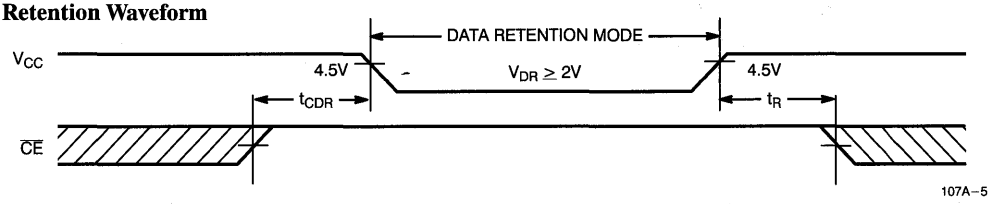
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

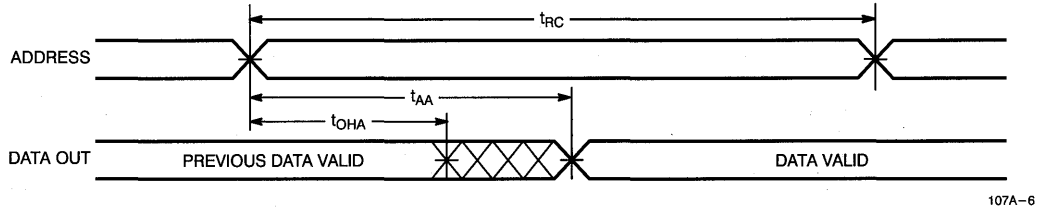
Note:
10. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

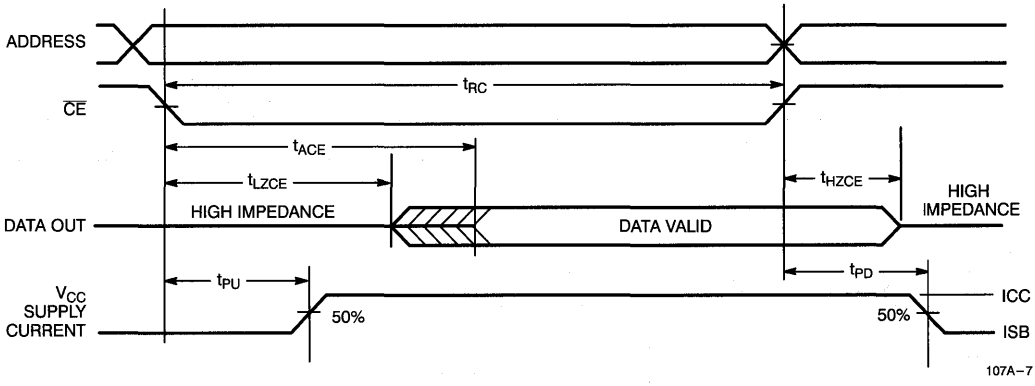


Switching Waveforms

Read Cycle No. 1[11, 12]



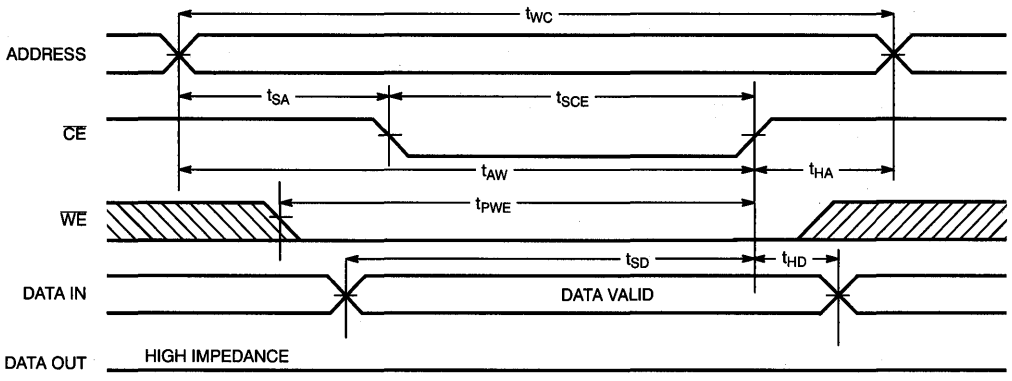
Read Cycle No. 2[12, 13]



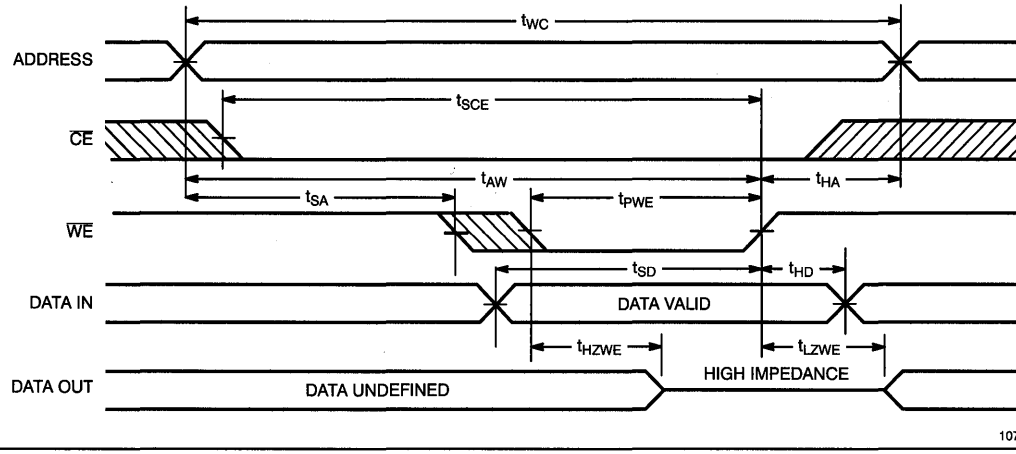
Notes:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C107A–12PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–12VC	V28	28-Lead (400-Mil) Molded SOJ	
15	CY7C107A–15PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–15VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–15DMB	D42	28-Lead (400-Mil) CerDIP	Military
20	CY7C107A–20PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–20VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–20DMB	D42	28-Lead (400-Mil) CerDIP	Military
25	CY7C107A–25PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–25VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–25DMB	D42	28-Lead (400-Mil) CerDIP	Military
35	CY7C107A–35PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–35VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–35DMB	D42	28-Lead (400-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C109A**

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Low standby power**
  - **— 250 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C109A is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

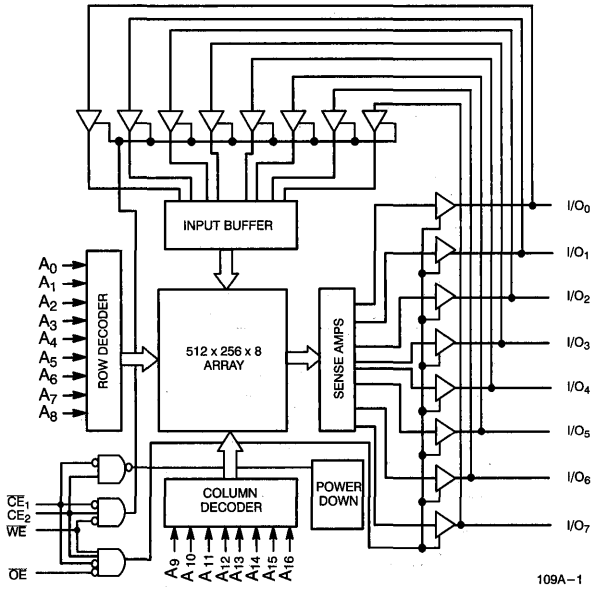
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

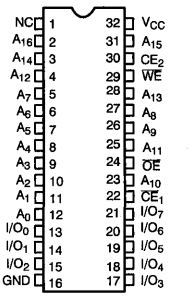
The CY7C109 is available in standard 400-mil-wide DIPs and SOJs and a leadless chip carrier.

Logic Block Diagram



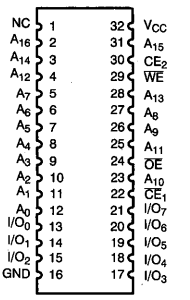
Pin Configurations

DIP/SOJ
Top View



109A–2

LCC
Top View



109A–3

Selection Guide

		7C109A–12	7C109A–15	7C109A–20	7C109A–25	7C109A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	185	170	155	145	140
	Military		180	170	160	150
Maximum Standby Current (mA)	Commercial	45	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] . – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C109A–12 Min.	7C109A–12 Max.	7C109A–15 Min.	7C109A–15 Max.	7C109A–20 Min.	7C109A–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		155	mA
			Mil				180		170	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		45		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C109A–25 Min.	7C109A–25 Max.	7C109A–35 Min.	7C109A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		145		140	mA
			Mil		160		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

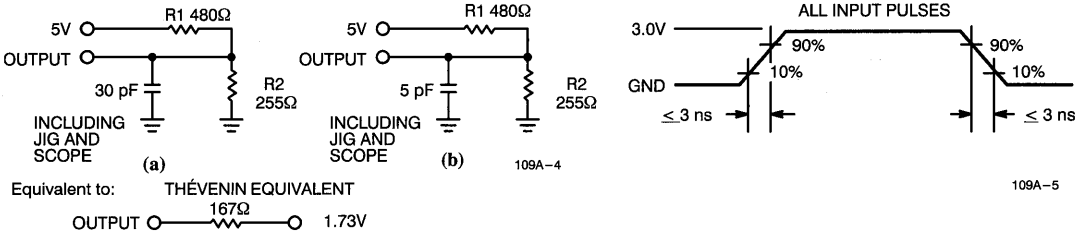
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics[3,6] Over the Operating Range

Parameter	Description	7C109A–12		7C109A–15		7C109A–20		7C109A–25		7C109A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Min.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7,8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to PowerDown		12		15		20		25		35	ns
WRITE CYCLE[9,10]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]		6		7		8		10		10	ns

Notes:

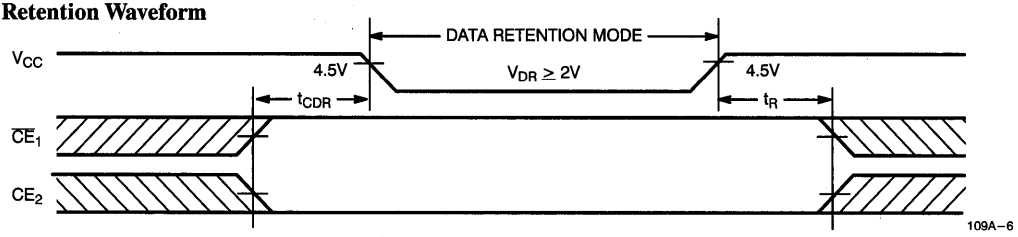
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

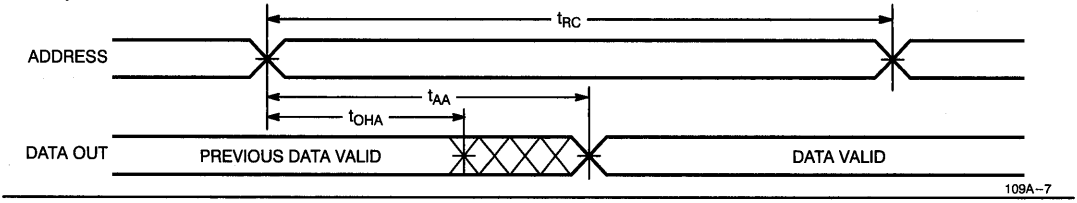
Note:
11. No input may exceed V_{CC} +0.5V.

Data Retention Waveform

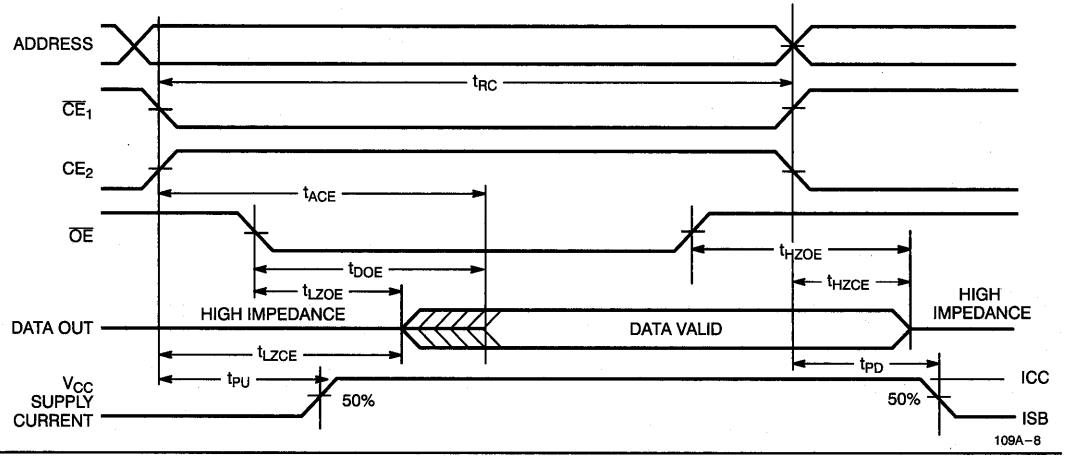


Switching Waveforms

Read Cycle No. 1[12, 13]



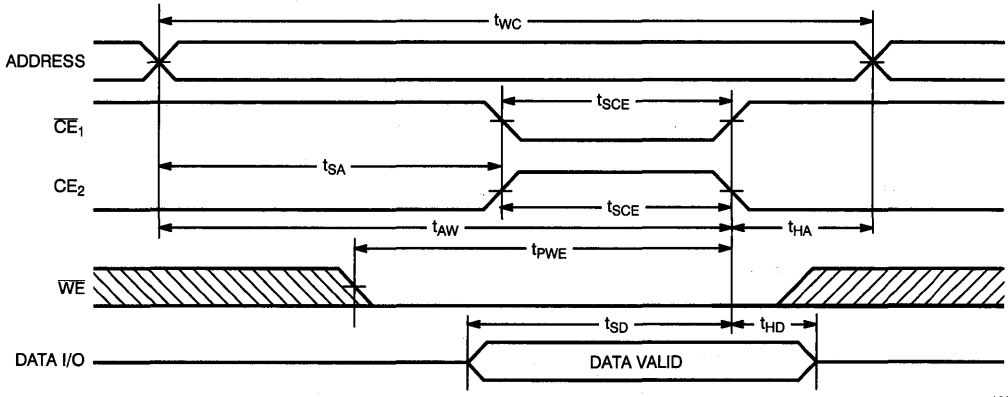
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



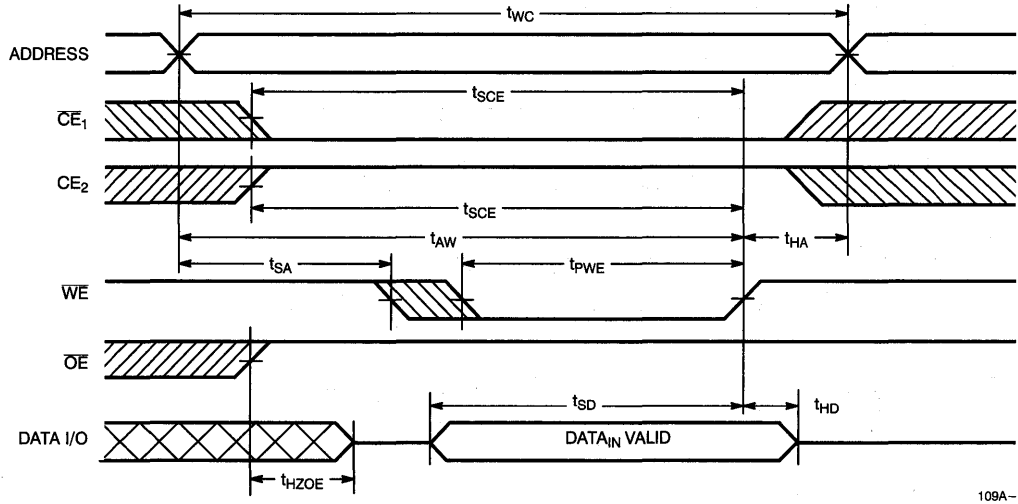
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)[15, 16]

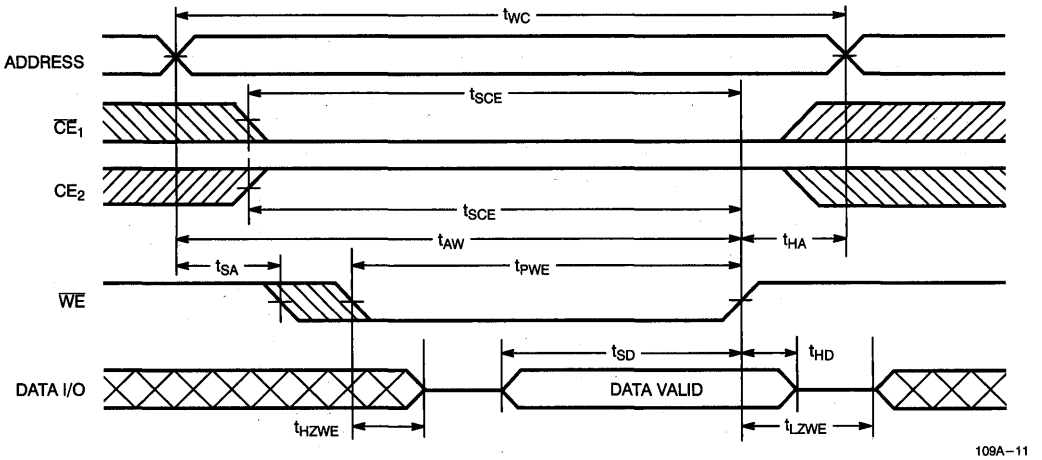


Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Notes:
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C109A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C109A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–15LMB	L75	32-Pin Leadless Chip Carrier	
20	CY7C109A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–20LMB	L75	32-Pin Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C109A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–25LMB	L75	32-Pin Leadless Chip Carrier	
35	CY7C109A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–35LMB	L75	32-Pin Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00233

CYPRESS SEMICONDUCTOR

CY7C123

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 7 ns (commercial)**
  - **— 10 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 825 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance both commercial and military**
- **TTL-compatible inputs and outputs**
- **24 pins**
- **300-mil package**

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

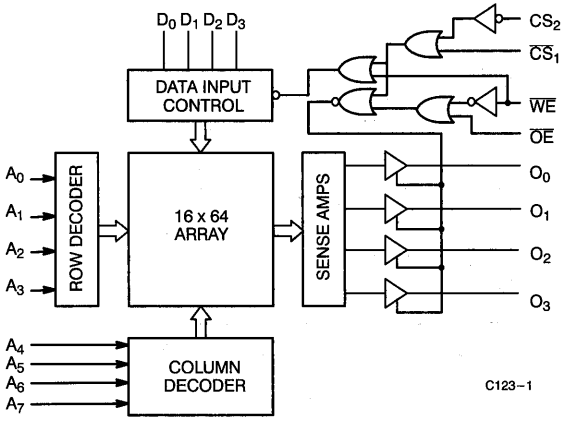
Writing to the device is accomplished when the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one ($\overline{CS_1}$) and output enable ($\overline{OE}$) inputs LOW, while the write enable ($\overline{WE}$) and chip select two ($\overline{CS_2}$) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

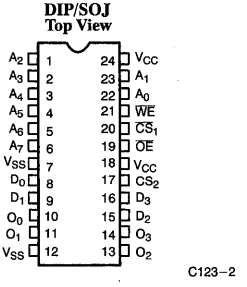
The output pins remain in high-impedance state when chip select one ($\overline{CS_1}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip select two ($\overline{CS_2}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C123-7	7C123-9	7C123-10	7C123-12	7C123-15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pins 24 and 18 to Pins 7 and 12)[1] ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C123−7 7C123−9 Min.	7C123−7 7C123−9 Max.	7C123−10 7C123−15 Min.	7C123−10 7C123−15 Max.	7C123−12 Min.	7C123−12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.8	+0.8	− 0.8	+0.8	− 0.8	+0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Current (High Z)	$V_{SS} \le V_{OUT} \le V_{CC}$, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Commercial		120				120	mA
			Military				150		150	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

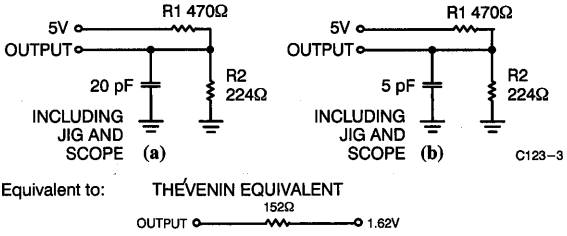
Logic Table[5]

Input					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	$D_0 - D_3$		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

Notes:

1. V_{IL} (min.) = −3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. H = High Voltage, L = Low Voltage, X = Don't Care, and High Z = High Impedance.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3]

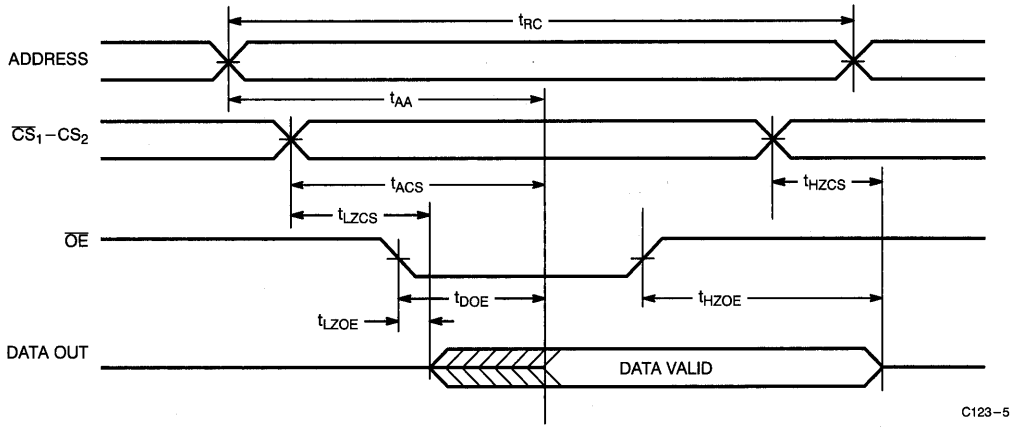
Parameter	Description	7C123–7		7C123–9		7C123–10		7C123–12		7C123–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	7		9		10		12		15		ns
t_{AA}	Address to Data Valid		7		9		10		12		15	ns
t_{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8		8		10	ns
t_{HZCS}	Chip Select to High Z[6, 7]		5		6		6		6.5		8	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		5		6		6		6.5		8	ns
t_{LZCS}	Chip Select to Low Z[7]	2		2		2		2		2		ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		2		2		2		ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	7		9		10		12		15		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		5.5		6		6		7		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	5		6.5		7		8		11		ns
t_{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t_{HD}	Data Hold from Write End	1		1		1		1		1		ns
t_{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t_{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	5		6.5		7		8		11		ns
t_{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:

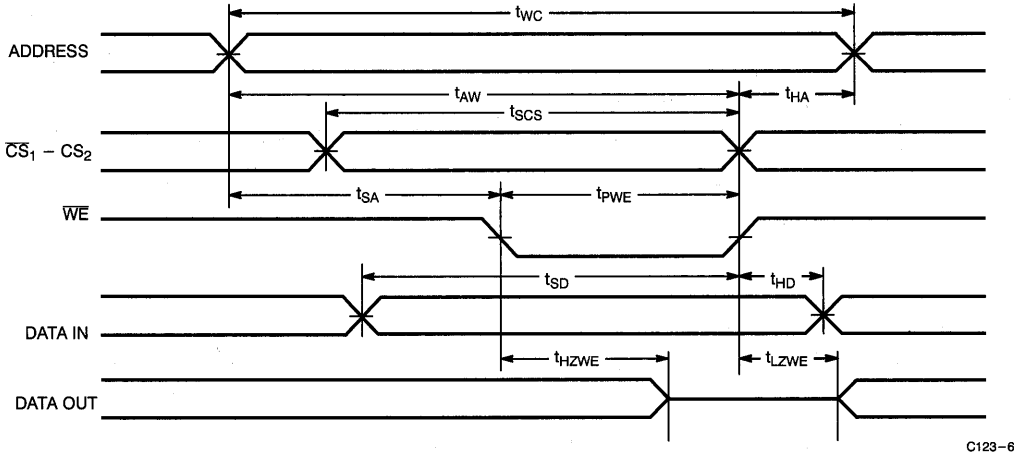
6. Transition is measured at steady-state HIGH level − 500 mV or steady-state LOW level +500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

Switching Waveforms

Read Cycle [8, 9]



Write Cycle [7, 8]

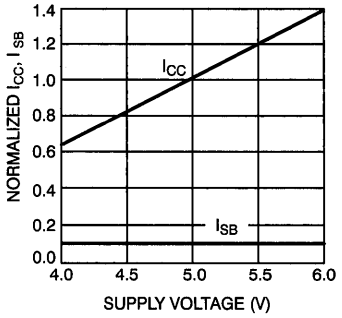


Notes:

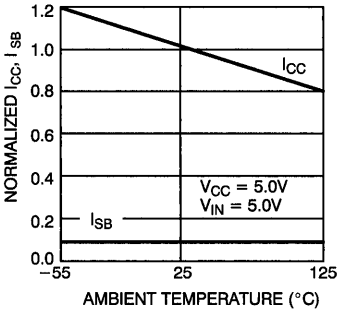
8. Measurements are referenced to 1.5V unless otherwise stated.
9. Timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in varous applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

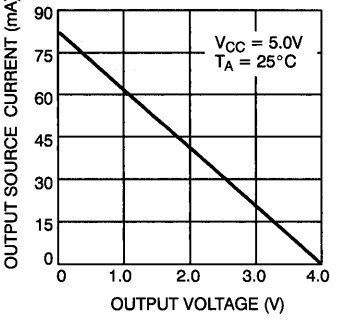
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



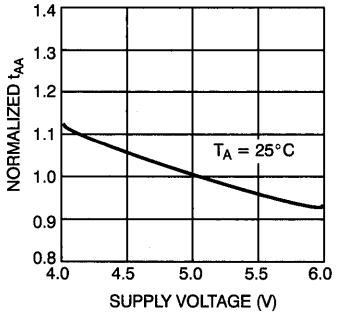
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



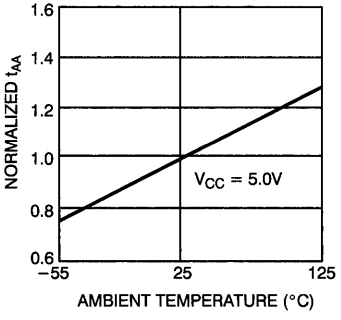
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



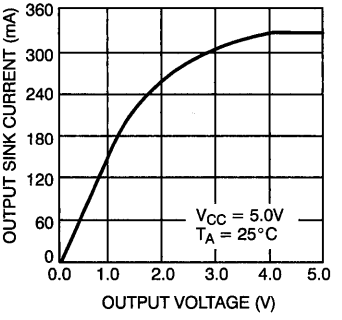
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



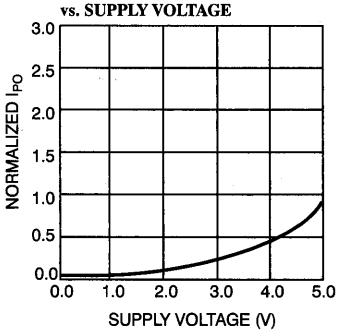
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



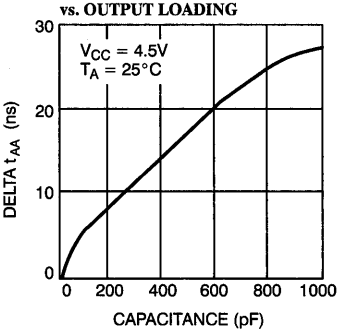
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



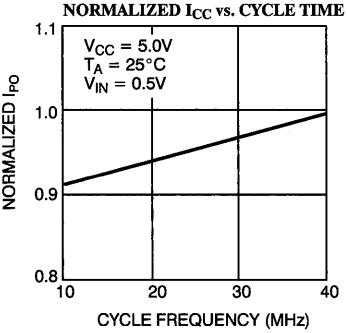
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TOTAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C123–7PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–7VC	V13	24-Lead Molded SOJ	
9	CY7C123–9PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–9VC	V13	24-Lead Molded SOJ	
10	CY7C123–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
12	CY7C123–12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C123–15DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

CY7C128A

2K x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 550 mW (military)**
- **Low standby power**
  - **— 110 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

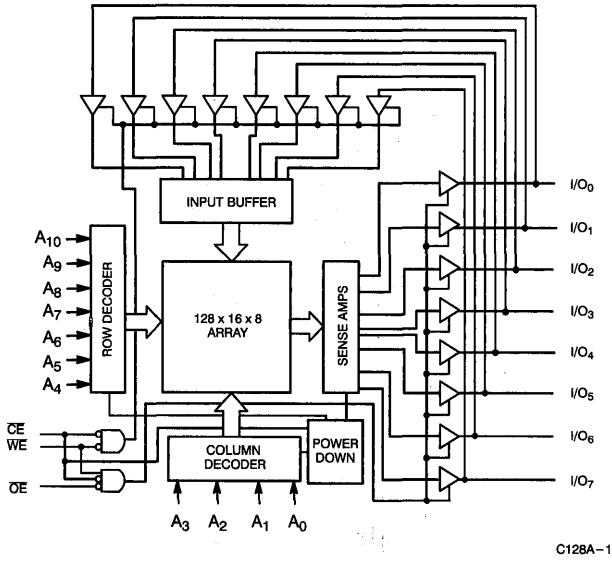
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C128A utilizes a die coat to insure alpha immunity.

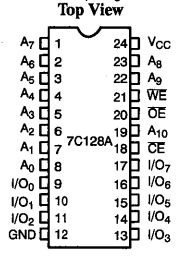
Logic Block Diagram



C128A–1

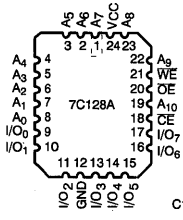
Pin Configurations

DIP/SOJ
Top View



C128A–2

LCC
Top View



C128A–3

Selection Guide

		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	120	100	100	100	
	Military		125	125	100	100
Maximum Standby Current (mA)	Commercial	40/40	40/20	20	20	
	Military		40/20	40	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to + 150°C

Ambient Temperature with Power Applied ..... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to + 7.0V

DC Input Voltage ..... − 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C128A-15 Min.	7C128A-15 Max.	7C128A-20 Min.	7C128A-20 Max.	7C128A-25 Min.	7C128A-25 Max.	7C128A-35, 45 Min.	7C128A-35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120		100		100		100	mA
			Mil				125		125		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Com'l		40		40		20		20	mA
			Mil				40		40		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V	Com'l		40		20		20		20	mA
			Mil				20		20		20	

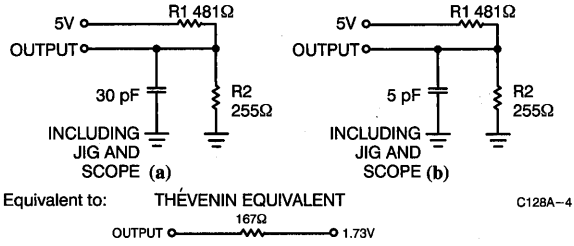
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

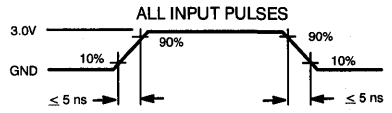
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C128A–4



C128A–5

Switching Characteristics Over the Operating Range[2,6]

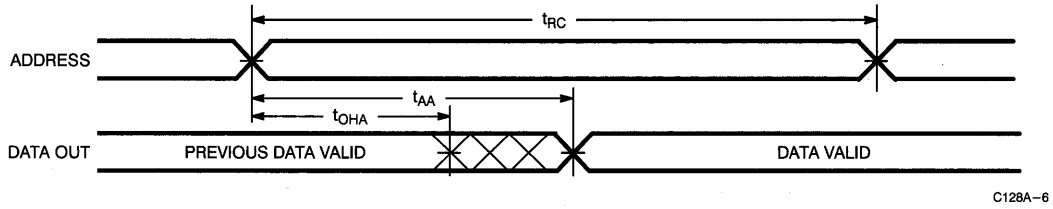
Parameter	Description	7C128A-15		7C128A-20		7C128A-25		7C128A-35		7C128A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Note:

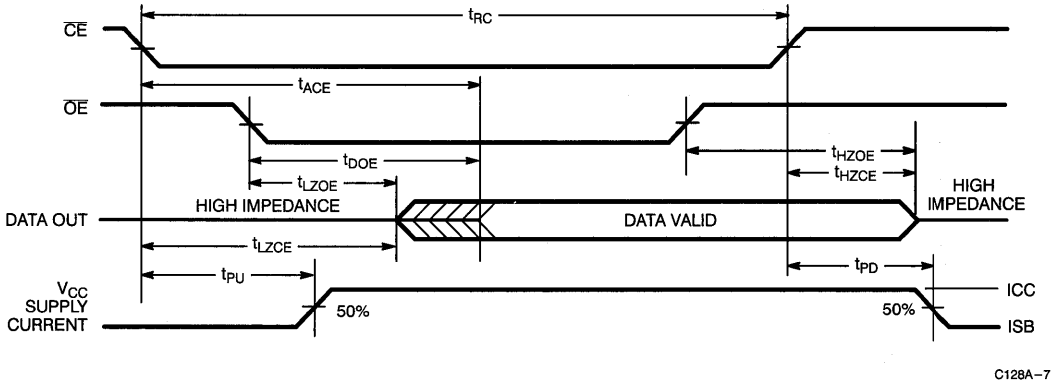
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

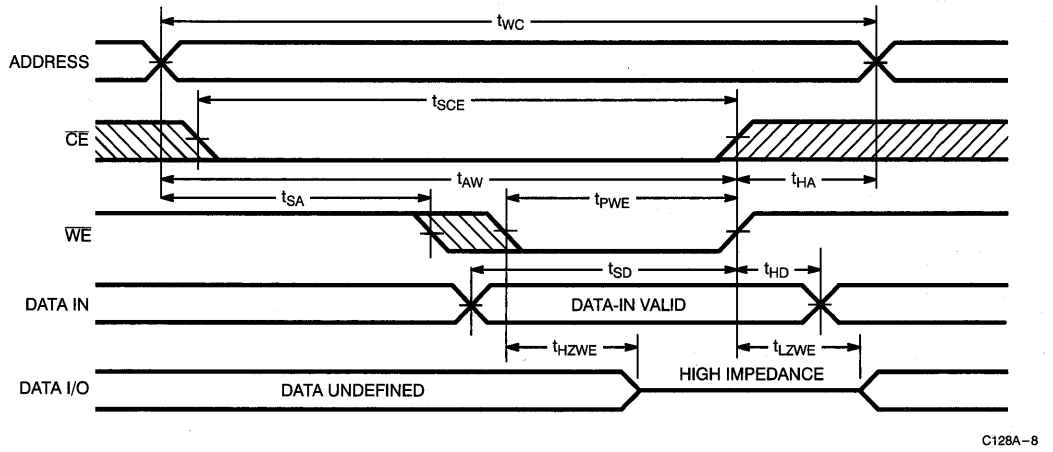
Read Cycle No. 1[10,11]



Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]

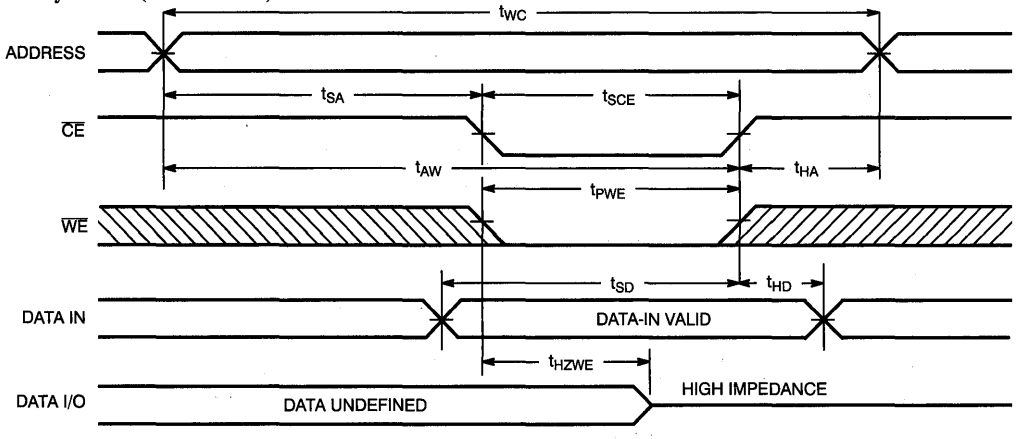


Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

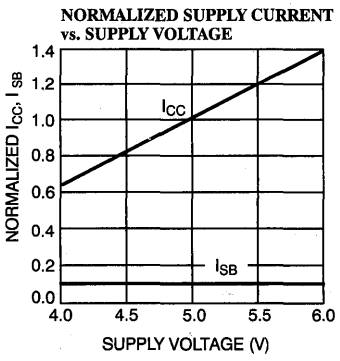
Switching Waveforms (continued)

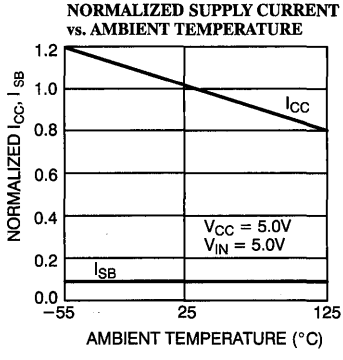
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 12, 14]

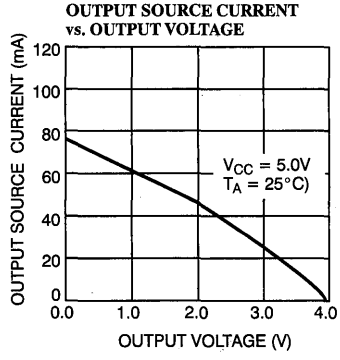


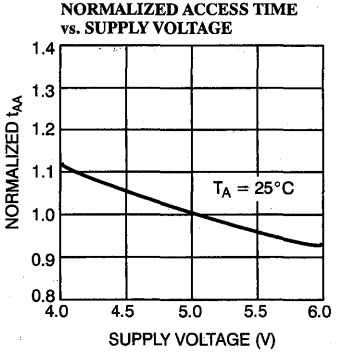
C128A–9

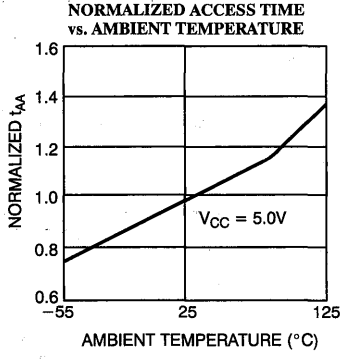
Typical DC and AC Characteristics

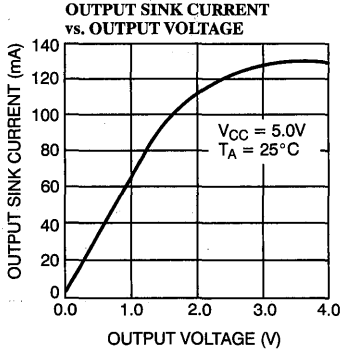






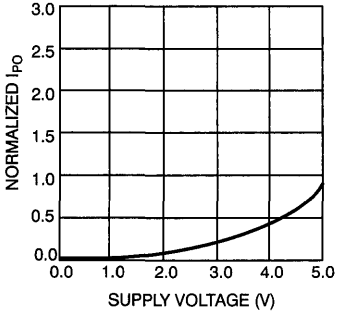




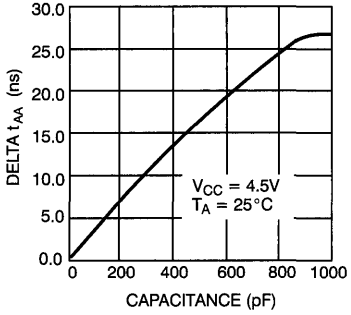


Typical DC and AC Characteristics (continued)

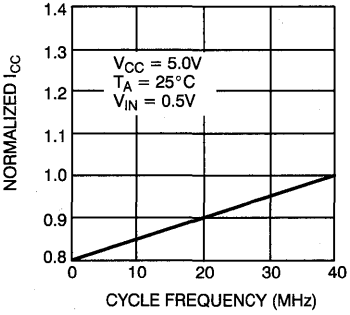
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C128A–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–15VC	V13	24-Lead Molded SOJ	
20	CY7C128A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–20VC	V13	24-Lead Molded SOJ	
	CY7C128A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–20LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
25	CY7C128A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–25VC	V13	24-Lead Molded SOJ	
	CY7C128A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–25LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C128A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–35VC	V13	24-Lead Molded SOJ	
	CY7C128A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–35LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C128A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–45LMB	L53	24-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00094–B

CYPRESS SEMICONDUCTOR

1K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**

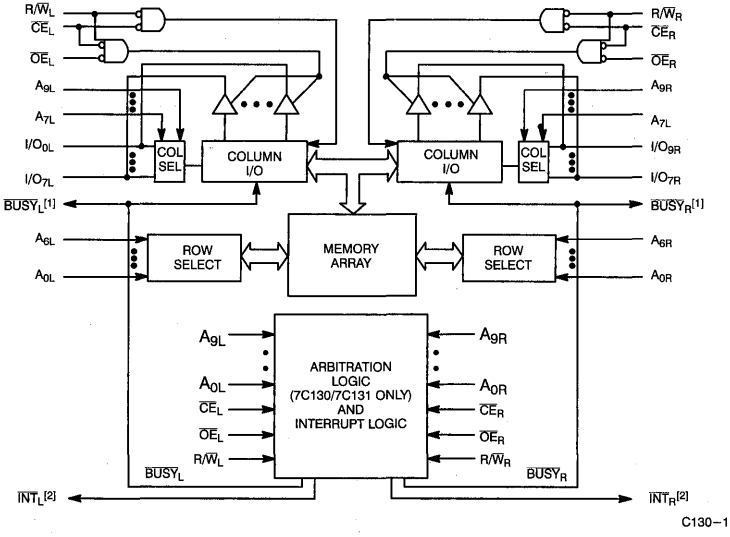
Functional Description

The CY7C130/CY7C131/CY7C140/CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in both 52-pin LCC and PLCC.

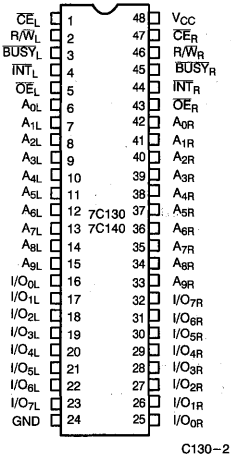
Logic Block Diagram



C130–1

Pin Configurations

DIP
Top View

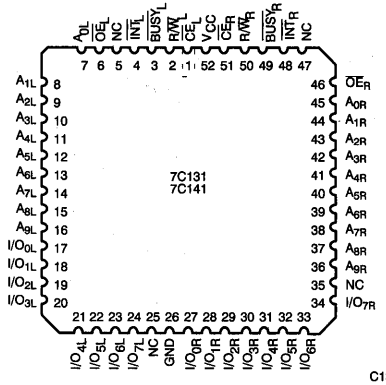


C130–2

Notes:
1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required.

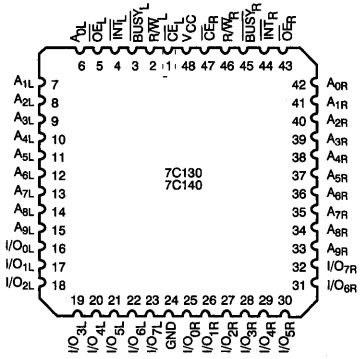
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C130–3

48-Pin LCC/QFP
Top View



C130–4

Selection Guide

		7C130–25[3] 7C131–25 7C140–25 7C141–25	7C130–30 7C131–30 7C140–30 7C141–30	7C130–35 7C131–35 7C140–35 7C141–35	7C130–45 7C131–45 7C140–45 7C141–45	7C130–55 7C131–55 7C140–55 7C141–55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150 °C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[4]	– 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/LCC packages.

4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C130–25, 30[3] 7C131–25,30 7C140–25,30 7C141–25,30 Min.	Max.	7C130–35 7C131–35 7C140–35 7C141–35 Min.	Max.	7C130–45,55 7C131–45,55 7C140–45,55 7C141–45,55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		– 5	+5	– 5	+5	– 5	+5	μA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		– 5	+5	– 5	+5	– 5	+5	μA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = GND			– 350		– 350		– 350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[9]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[9]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		105		85		70	mA
			Mil				105		85	

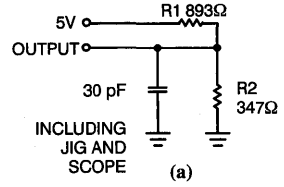
Capacitance[8]

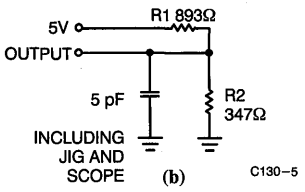
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

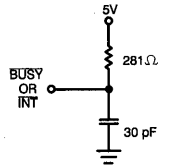
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters.
9. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.
10. AC Test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
11. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
12. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
13. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
14. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
15. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms



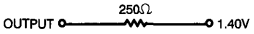


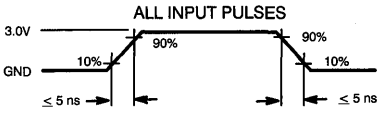


BUSY Output Load (CY7C130/CY7C131 ONLY)

C130–6

Equivalent to: THEVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5,11]

Parameter	Description	7C130–25[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[12]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[12]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[12]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[13]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13, 14]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[13, 14]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[15]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5,11] (continued)

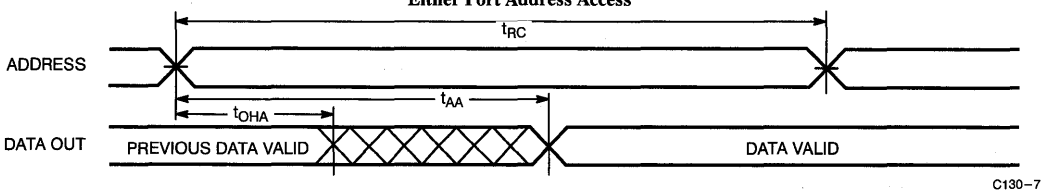
Parameter	Description	7C130–25[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[16]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[16]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[17]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18		Note 18		Note 18	ns
t_{WDD}	Write Pulse to Data Delay		Note 18		Note 18		Note 18		Note 18		Note 18	ns
INTERRUPT TIMING												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[16]		25		25		25		35		45	ns

Notes:

16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. CY7C140/CY7C141 only.
18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address is toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

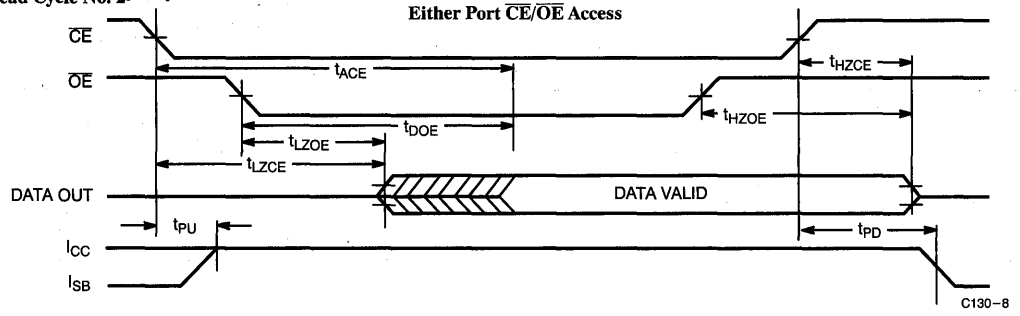
Switching Waveforms

Read Cycle No. 1[19, 20]

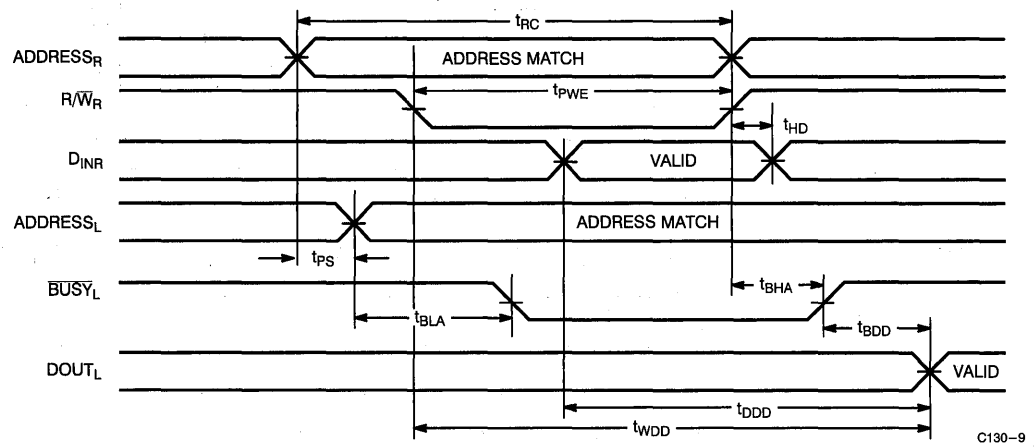


Switching Waveforms (continued)

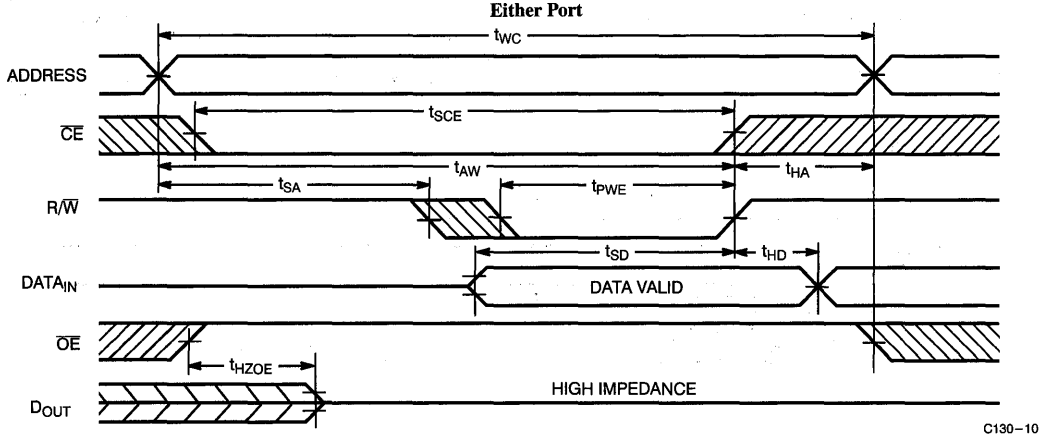
Read Cycle No. 2[19,21]



Read Cycle No. 3[20]

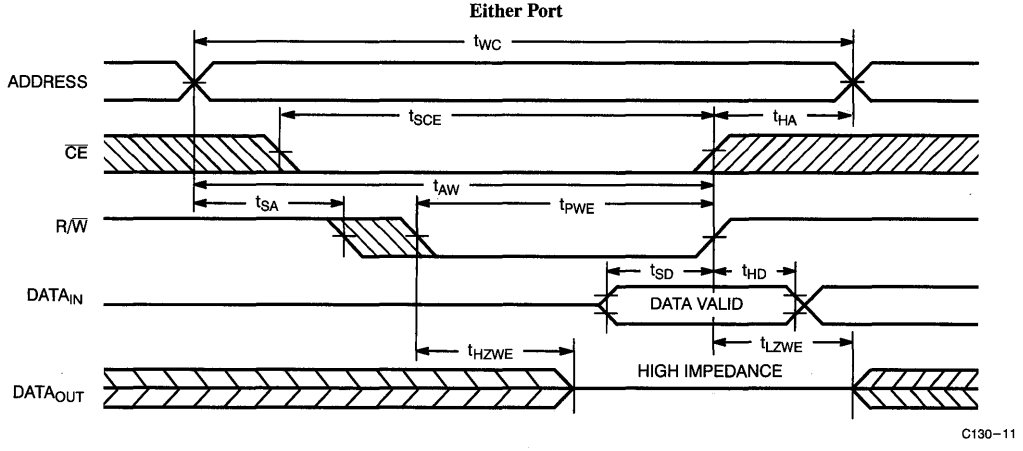


Write Cycle No.1 (OE Tri-States Data I/Os – Either Port)[15,22]



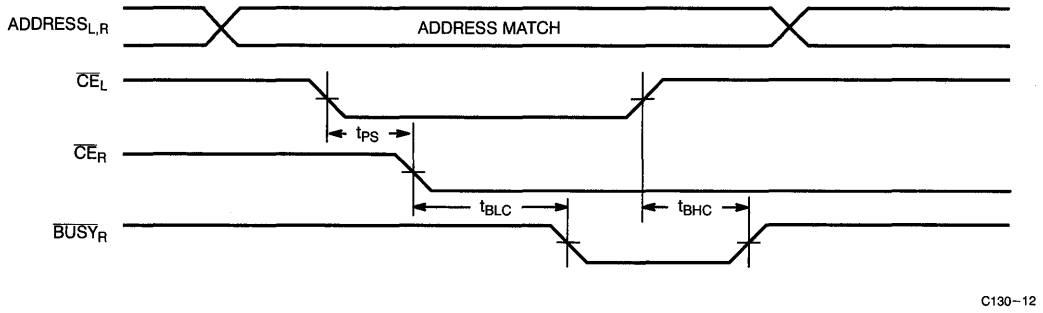
Switching Waveforms (continued)

Write Cycle No. 2 ($R/\overline{W}$ Tri-States Data I/Os – Either Port)[15,23]

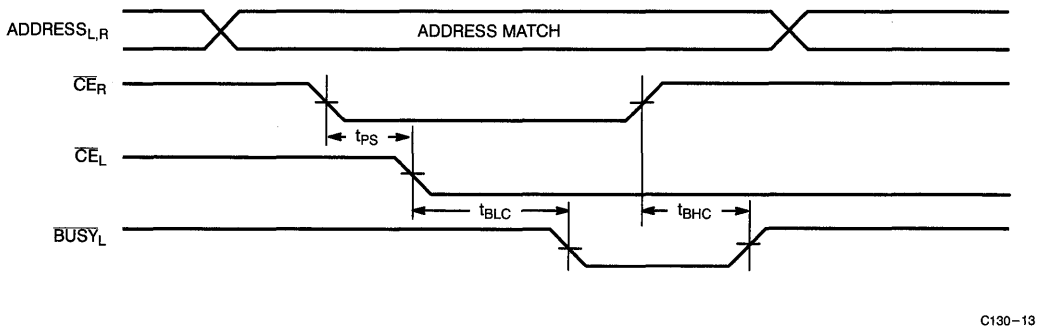


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



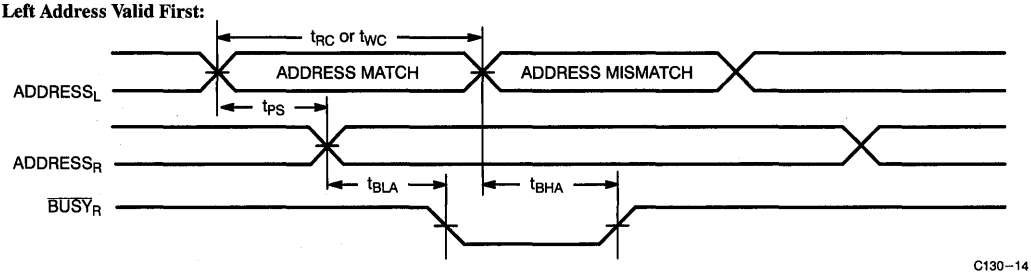
$\overline{CE}_R$ Valid First:



Switching Waveforms (continued)

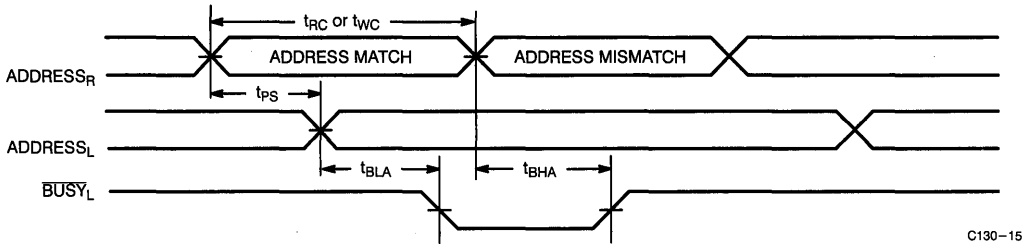
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C130–14

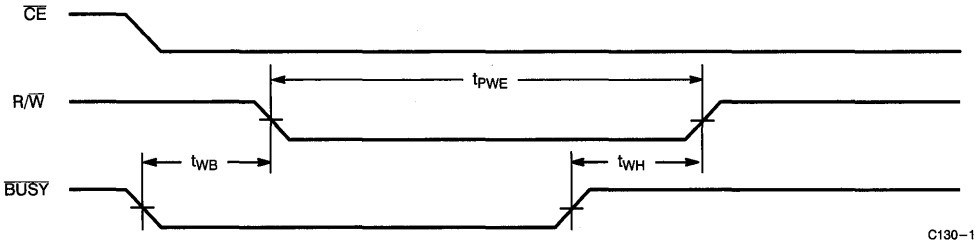
Right Address Valid First:



C130–15

Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave: CY7C140/CY7C141)

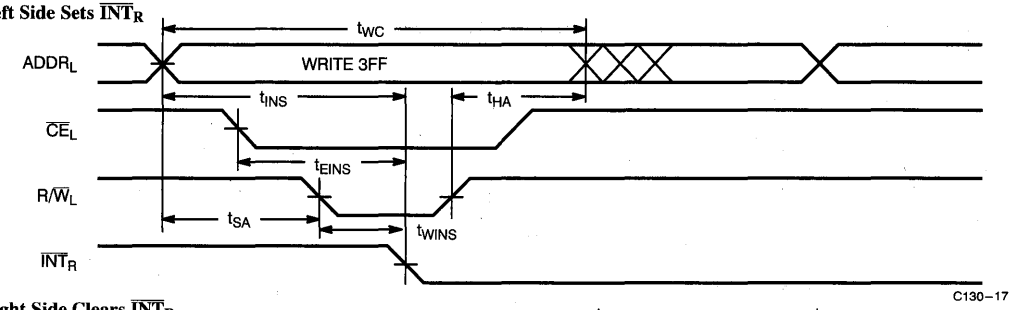


C130–16

Switching Waveforms (continued)

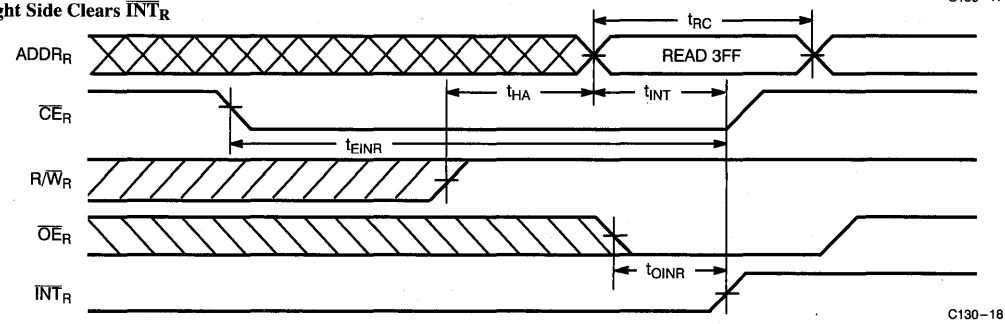
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$



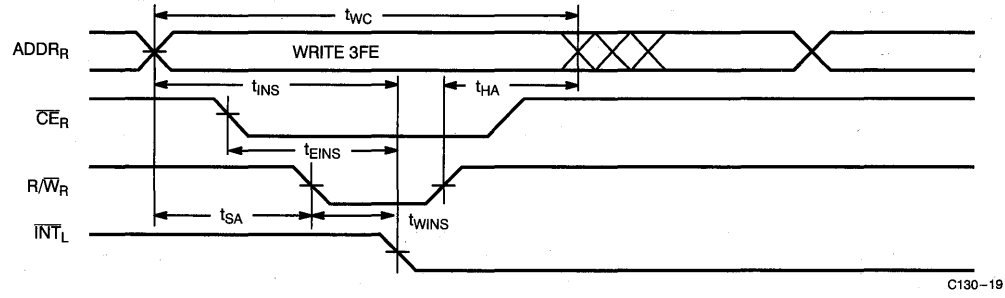
C130–17

Right Side Clears $\overline{INT}_R$



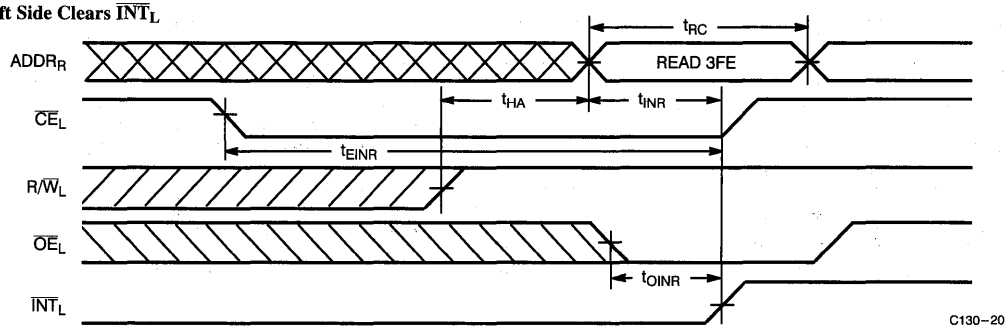
C130–18

Right Side Sets $\overline{INT}_L$



C130–19

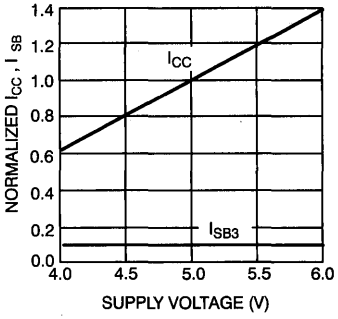
Left Side Clears $\overline{INT}_L$



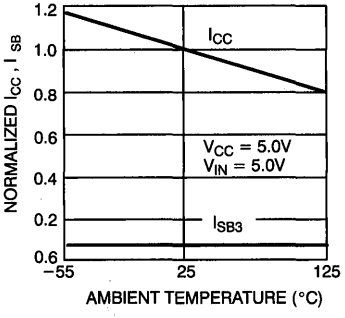
C130–20

Typical DC and AC Characteristics

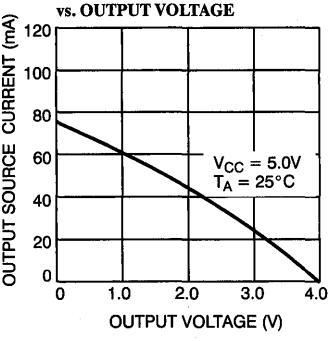
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



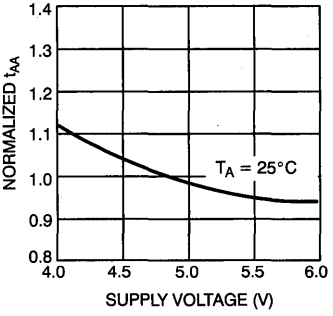
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



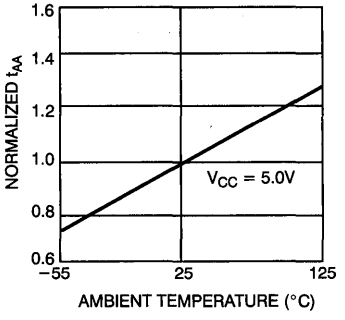
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



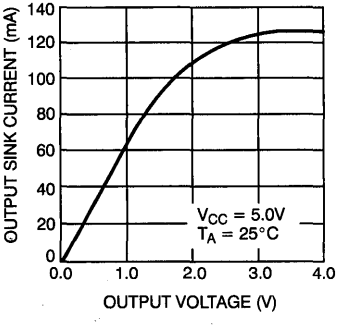
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



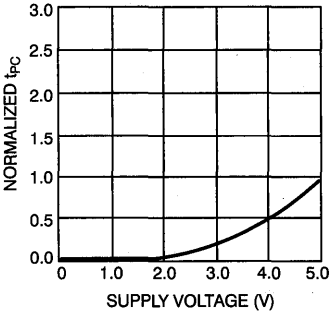
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



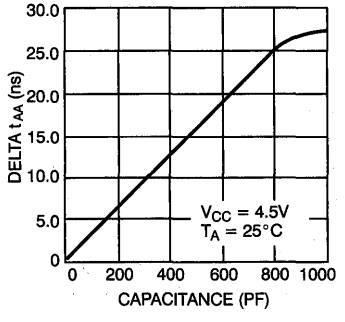
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



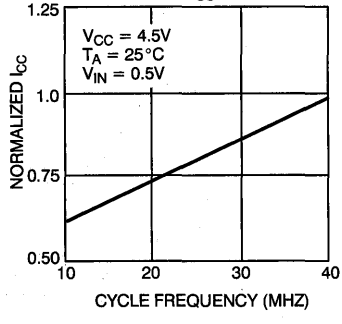
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130–35PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130–35FMB	F78	48-Lead Quad Flatpack	
	CY7C130–35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C130–45PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130–45FMB	F78	48-Lead Quad Flatpack	
	CY7C130–45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C130–55PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C130–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C130–55FMB	F78	48-Lead Quad Flatpack	
	CY7C130–55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C131–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C131–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–35FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131–35LMB	L69	52-Square Leadless Chip Carrier	
45	CY7C131–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–45FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131–45LMB	L69	52-Square Leadless Chip Carrier	
55	CY7C131–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–55FMB	F78	48-Lead Quad Flatpack	Military
	CY7C131–55MB	L69	52-Square Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140–35FMB	F78	48-Lead Quad Flatpack	
	CY7C140–35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C140–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140–45FMB	F78	48-Lead Quad Flatpack	
	CY7C140–45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C140–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C140–55FMB	F78	48-Lead Quad Flatpack	
	CY7C140–55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C141–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–35FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141–35LMB	L69	52-Square Leadless Chip Carrier	
45	CY7C141–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–45FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141–45LMB	L69	52-Square Leadless Chip Carrier	
55	CY7C141–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–55FMB	F78	48-Lead Quad Flatpack	Military
	CY7C141–55LMB	L69	52-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C140/CY7C141 only.

Document #: 38-00027-I

CY7C132/CY7C136
CY7C142/CY7C146

CYPRESS SEMICONDUCTOR

2K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146**
- **$\overline{BUSY}$ output flag on CY7C132/CY7C136; $\overline{BUSY}$ input on CY7C142/CY7C146**
- **$\overline{INT}$ flag for port-to-port communication (52-pin LCC/PLCC versions)**

Functional Description

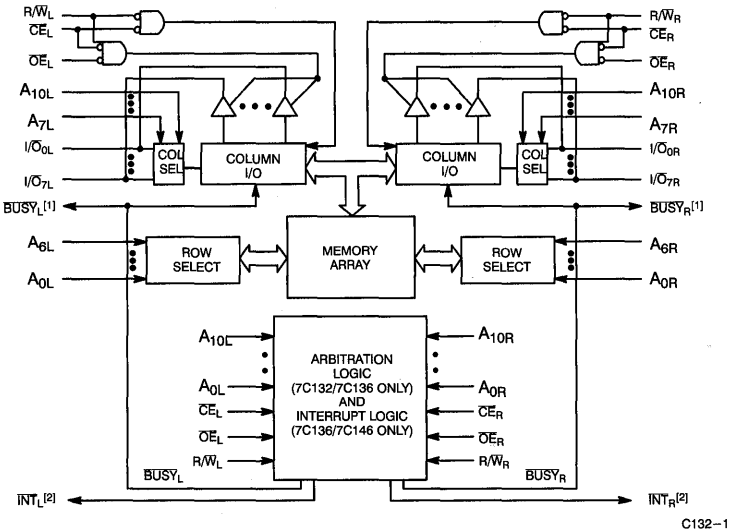
The CY7C132/CY7C136/CY7C142/CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ flags are provided on each port. In addition, an interrupt flag ($\overline{INT}$) is provided on each port of the 52-pin LCC and PLCC versions. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC.

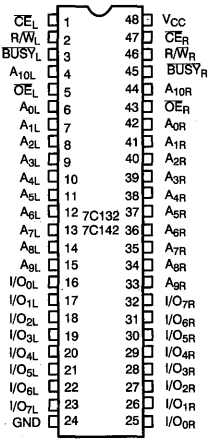
Logic Block Diagram



C132–1

Pin Configuration

DIP
Top View

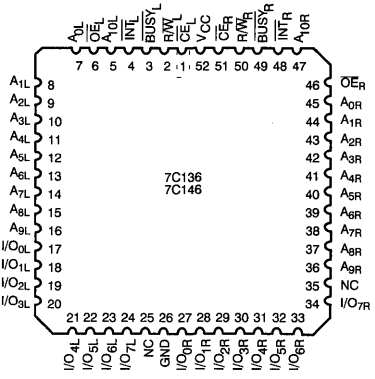


C132–2

Notes:
1. CY7C132/CY7C136 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
   CY7C142/CY7C146 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs; pull-up resistor required.

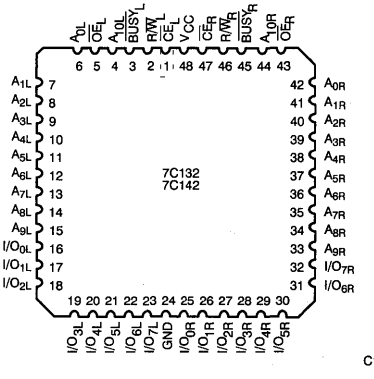
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C132-3

48-Pin LCC
Top View



C132-4

Selection Guide

		7C132-25[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military[4]	− 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in LCC and PLCC packages only.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C132–25, 30[3] 7C136–25,30 7C142–25,30 7C146–25,30 Min.	Max.	7C132–35 7C136–35 7C142–35 7C146–35 Min.	Max.	7C132–45,55 7C136–45,55 7C142–45,55 7C146–45,55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 5	+5	– 5	+5	– 5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	– 5	+5	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND			– 350		– 350		– 350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		105		85		70	mA
			Mil				105		85	

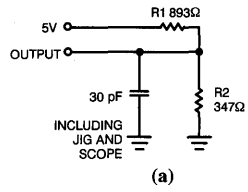
Capacitance[9]

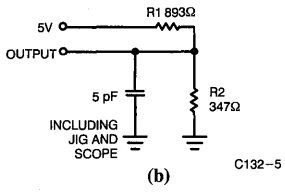
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

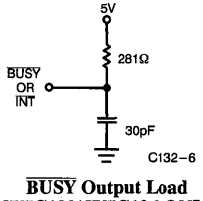
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

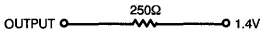


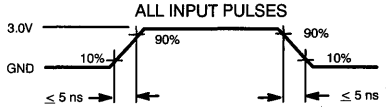




$\overline{BUSY}$ Output Load (CY7C132/CY7C136 ONLY)

Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5,10]

Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5,10] (continued)

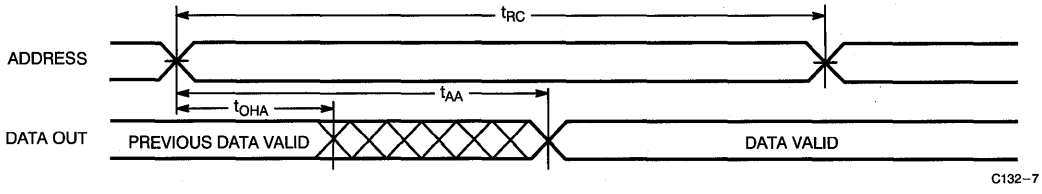
Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING[18]												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. 52-pin LCC/PLCC versions only.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

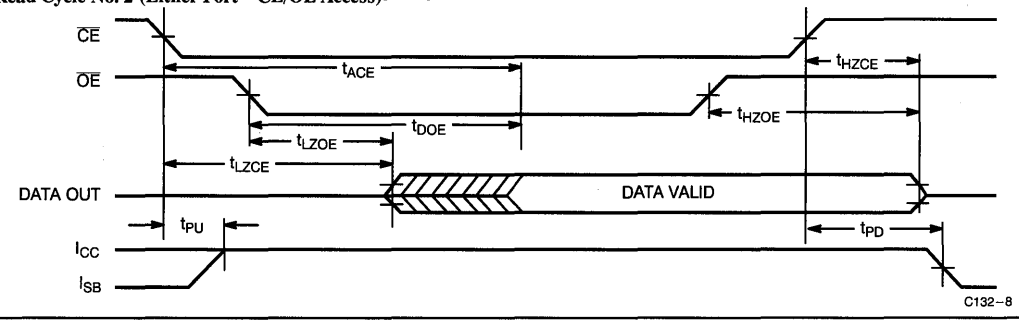
Switching Waveforms

Read Cycle No. 1 (Either Port—Address Access)[19, 20]

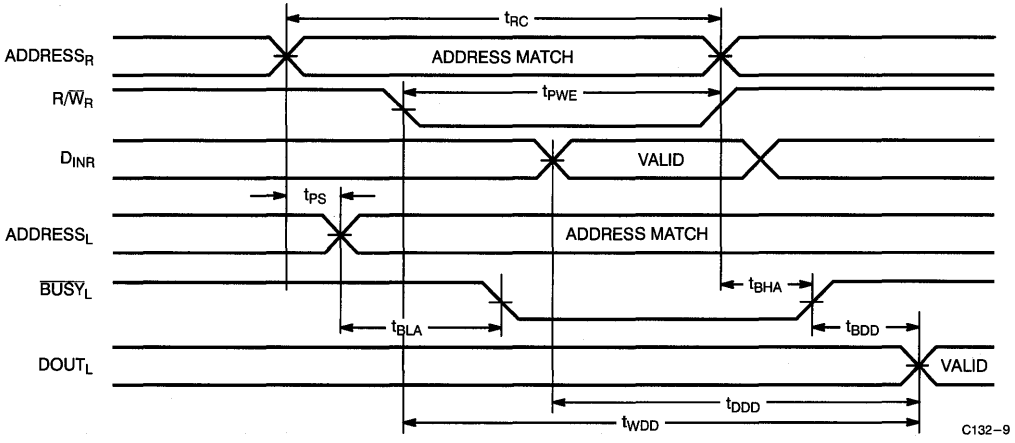


Switching Waveforms (continued)

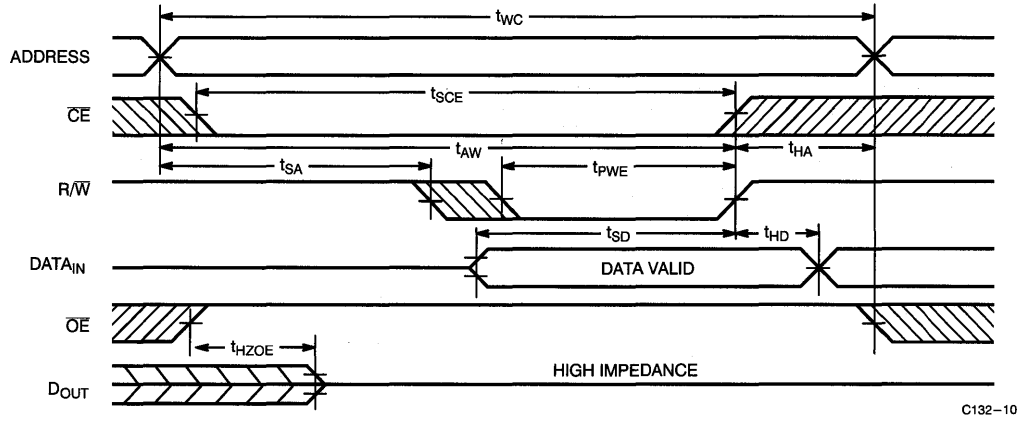
Read Cycle No. 2 (Either Port—$\overline{CE}$/$\overline{OE}$ Access)[19, 21]



Read Cycle No. 3 (Read with $\overline{BUSY}$ Master: CY7C132 and 7C136)[20]

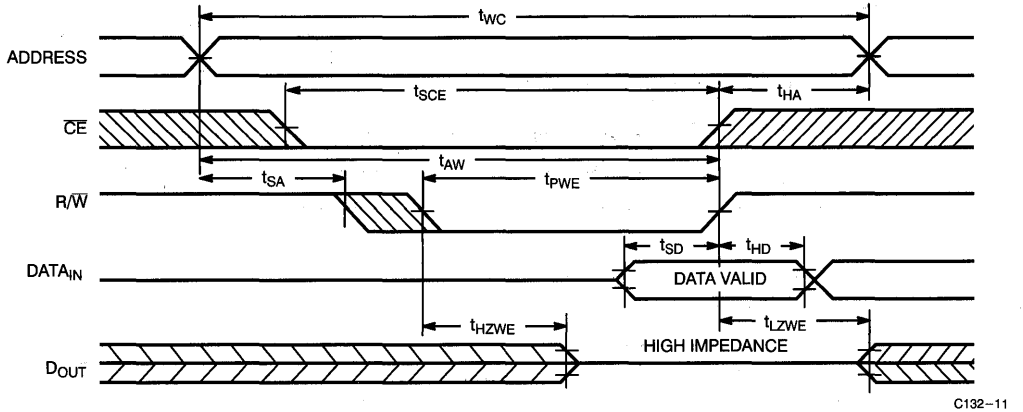


Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os—Either Port) [14,22]



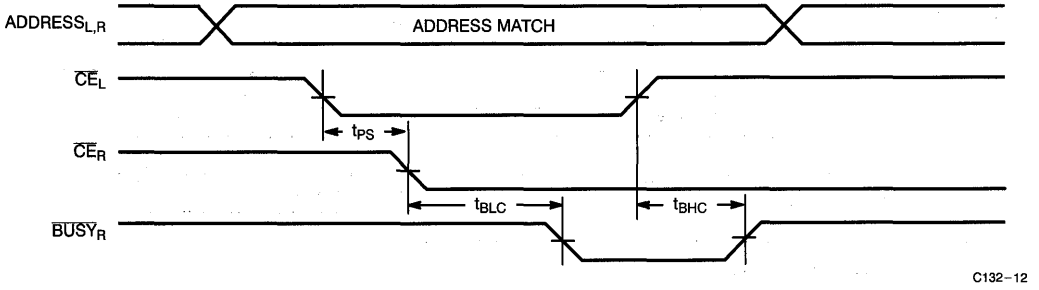
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os—Either Port)[14,23]

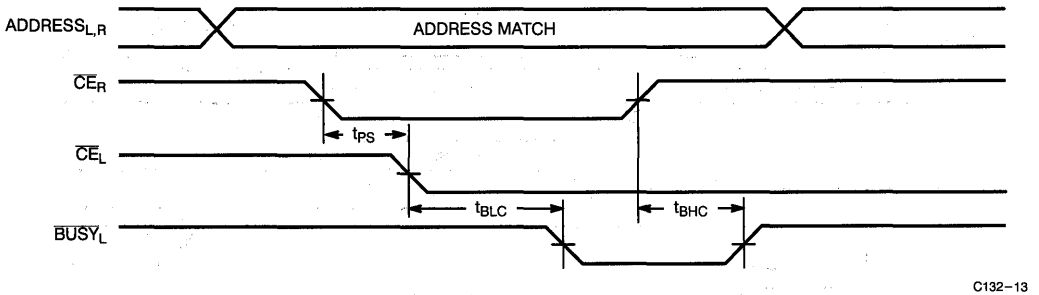


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



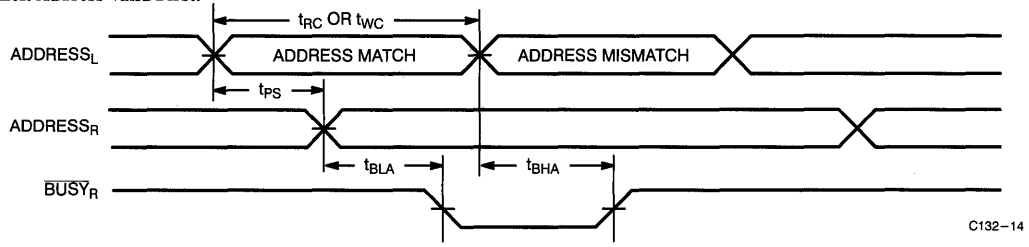
$\overline{CE}_R$ Valid First:



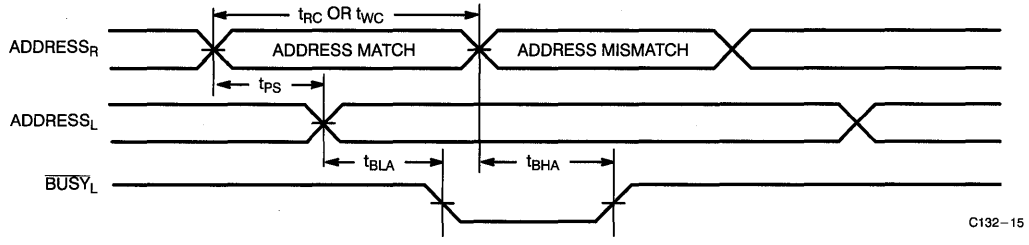
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

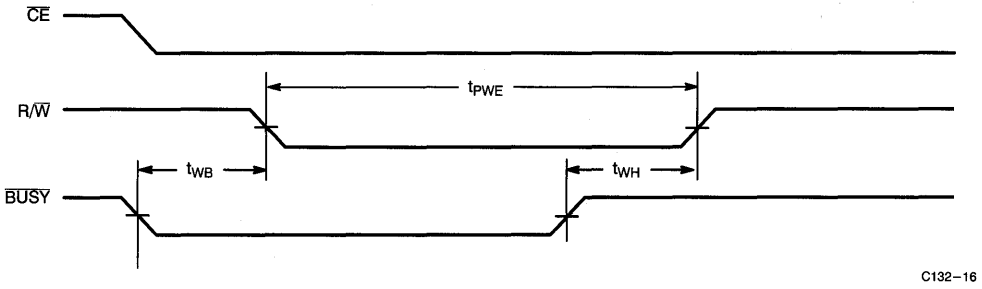
Left Address Valid First:



Right Address Valid First:

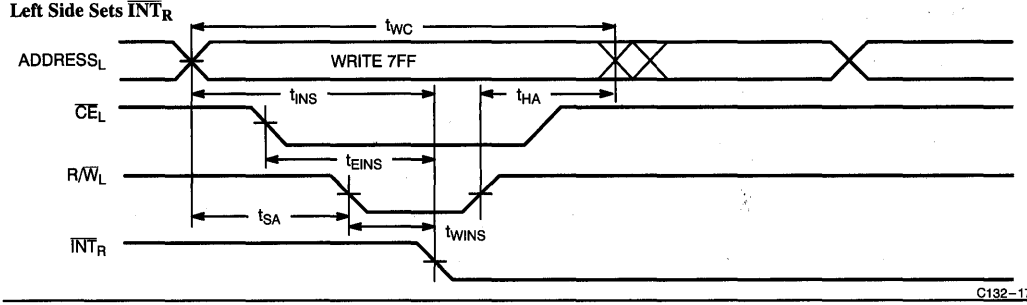


Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7C142/CY7C146)

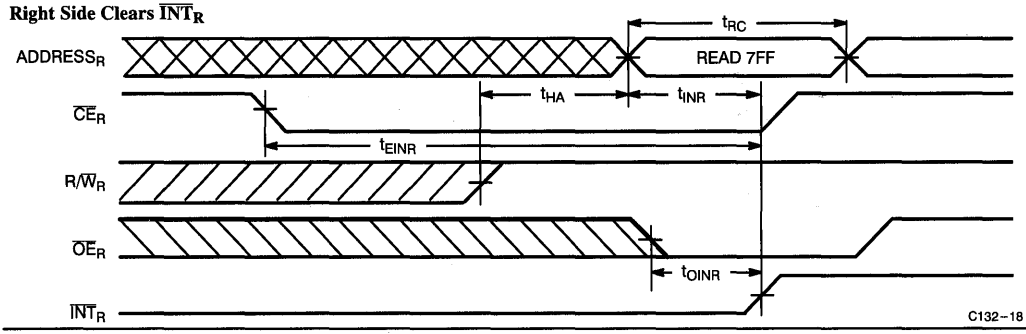


Interrupt Timing Diagrams[18]

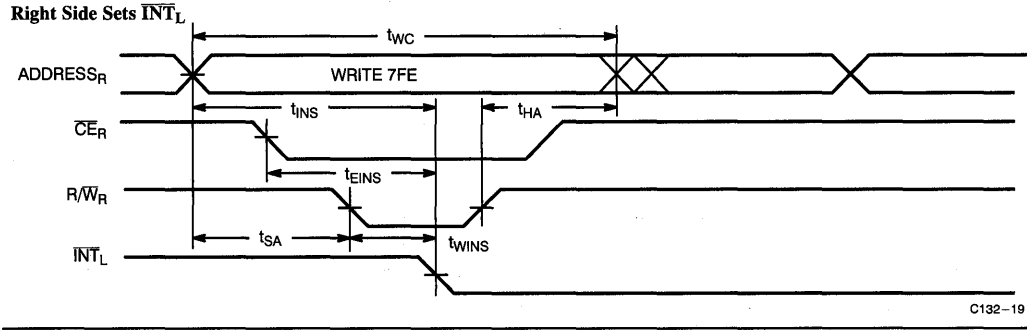
Left Side Sets $\overline{INT}_R$



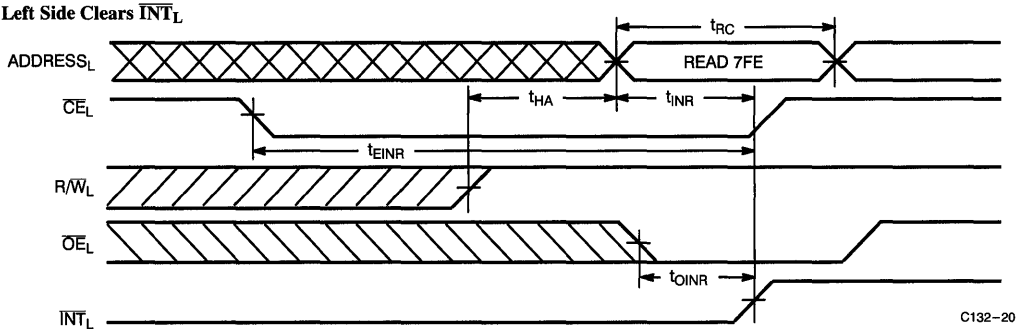
Right Side Clears $\overline{INT}_R$



Right Side Sets $\overline{INT}_L$

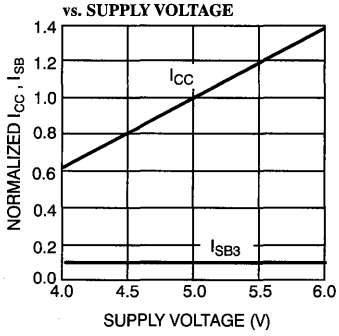


Left Side Clears $\overline{INT}_L$

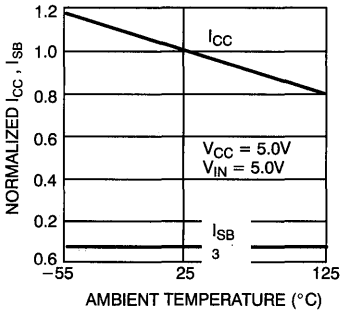


Typical DC and AC Characteristics

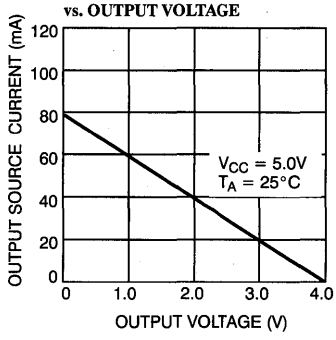
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



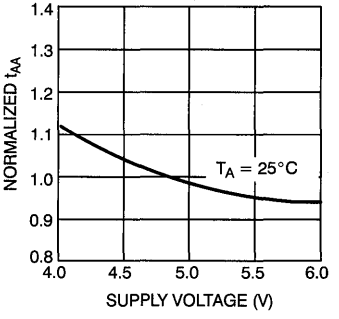
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



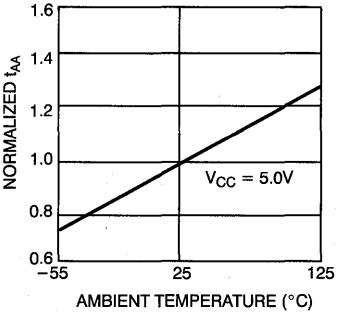
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



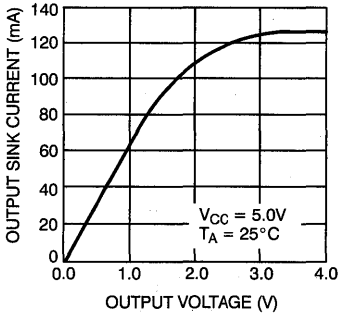
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



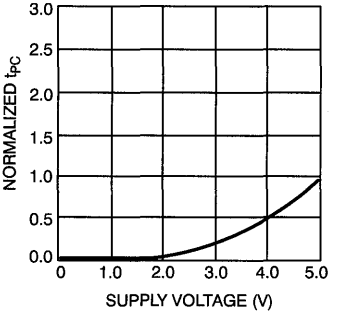
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



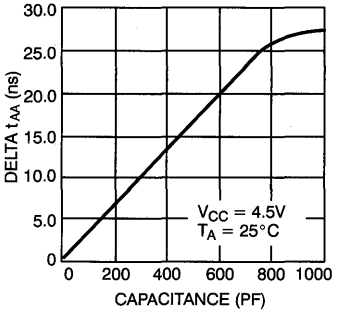
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



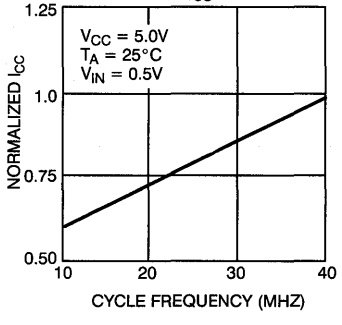
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C132–35FMB	F78	48-Lead Quad Flatpack	
	CY7C132–35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C132–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C132–45FMB	F78	48-Lead Quad Flatpack	
	CY7C132–45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C132–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C132–55FMB	F78	48-Lead Quad Flatpack	
	CY7C132–55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C136–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C142–35FMB	F78	48-Lead Quad Flatpack	
	CY7C142–35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C142–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C142–45FMB	F78	48-Lead Quad Flatpack	
	CY7C142–45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C142–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7C142–55FMB	F78	48-Lead Quad Flatpack	
	CY7C142–55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C146–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C146–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–55LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C142/CY7C146 only.

Document #: 38-00061-H

CYPRESS SEMICONDUCTOR

4K x 8 Dual-Port Static RAMs and 4K x 8 Dual-Port Static RAM with Semaphores

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **7B1342 includes semaphores**
- **7B134 available in 48-pin DIP, 48-pin LCC**
- **7B135/7B1342 available in 52-pin LCC/PLCC**

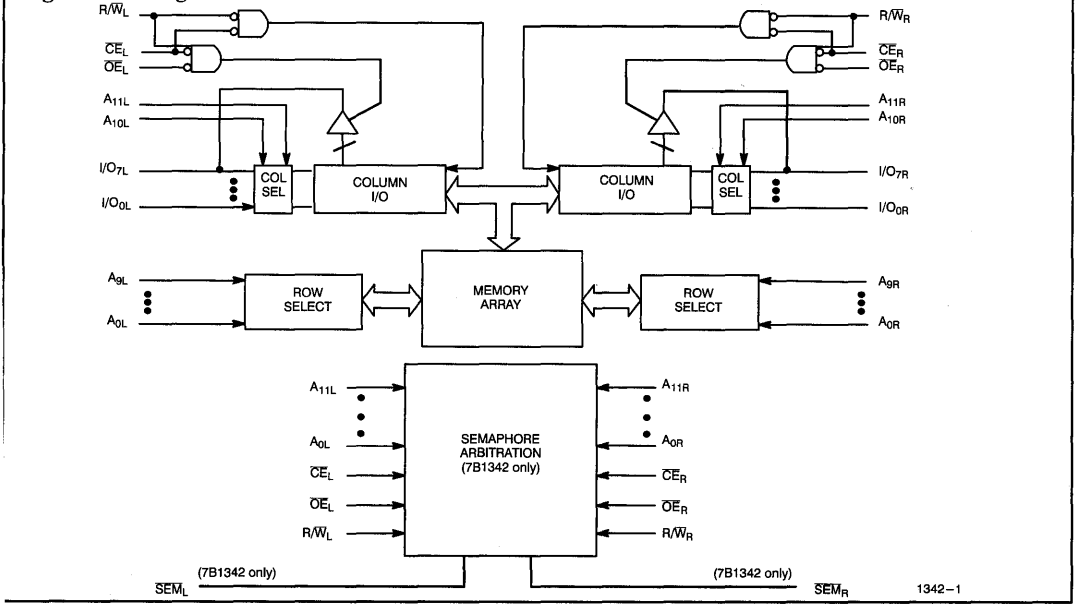
Functional Description

The CY7B134, CY7B135, and CY7B1342 are high-speed BiCMOS 4K x 8 dual-port static RAMs. The CY7B1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). The CY7B134/135 are suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7B1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7B1342 only).

The CY7B134 is available in 48-pin DIP and 48-pin LCC. The CY7B135 and CY7B1342 are available in 52-pin LCC/PLCC.

Logic Block Diagram

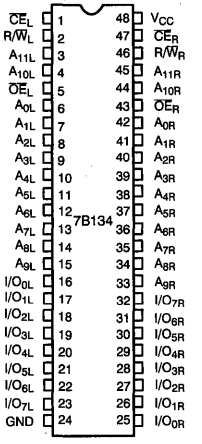


Selection Guide

		7B134–20 7B135–20 7B1342–20	7B134–25 7B135–25 7B1342–25	7B134–35 7B135–35 7B1342–35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	240	220	210
	Military		260	250
Maximum Standby Current (mA)	Commercial	80	75	70
	Military		80	75

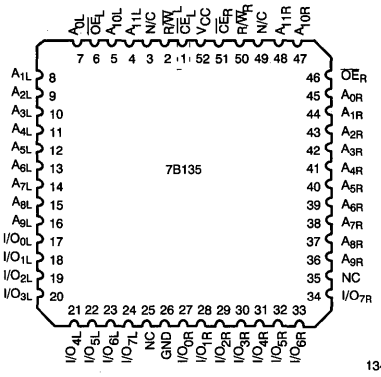
Pin Configurations

DIP
Top View



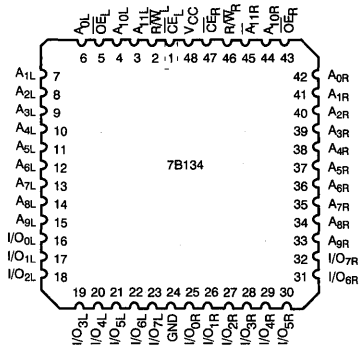
1342-2

LCC/PLCC
Top View



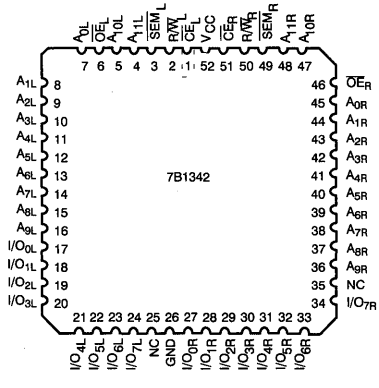
1342-3

LCC
Top View



1342-4

LCC/PLCC
Top View



1342-5

Pin Definitions

Left Port	Right Port	Description
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7B1342 only)	$\overline{SEM}_R$ (CY7B1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage[1] ..... – 3.0V to +7.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[2]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B134–20 7B135–20 7B1342–20 Min.	Max.	7B134–25 7B135–25 7B1342–25 Min.	Max.	7B134–35 7B135–35 7B1342–35 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2..4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		240		220		210	mA
			Mil				260		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		80		75		70	mA
			Mil				80		75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		150		140		130	mA
			Mil				170		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		25		25		25	mA
			Mil				30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		130		120		110	mA
			Mil				150		130	

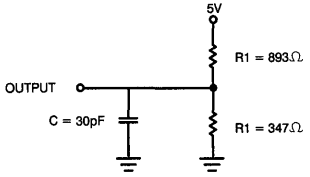
Capacitance[5]

Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

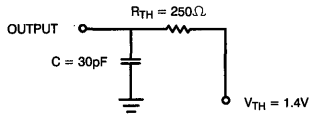
1. Pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 meas no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For all packages except DIP and cerDIP (D26, P25), which have maximums of C_{IN} = 15 pF, C_{OUT} = 15 pF.

AC Test Loads and Waveforms



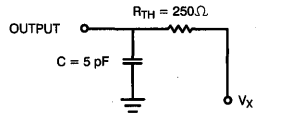
(a) Normal Load (Load 1)

1342–6



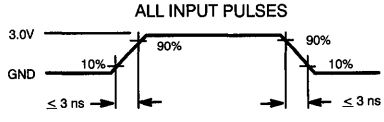
(b) Thevenin Equivalent (Load 1)

1342–7



(c) Three-State Delay (Load 3)

1342–8



1342–9

Switching Characteristics Over the Operating Range[7,8]

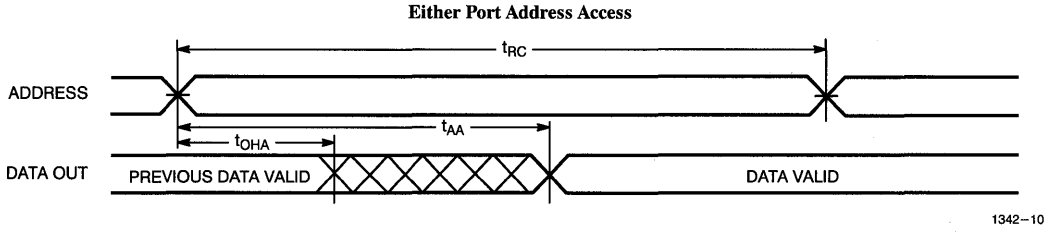
Parameter	Description	7B134–20 7B135–20 7B1342–20		7B134–25 7B135–25 7B1342–25		7B134–35 7B135–35 7B1342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		15		20	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z		13		15		20	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z		13		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	15		20		30		ns
t_{AW}	Address Set-Up to Write End	15		20		30		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		13		15		20	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns

Switching Characteristics Over the Operating Range[7,8] (continued)

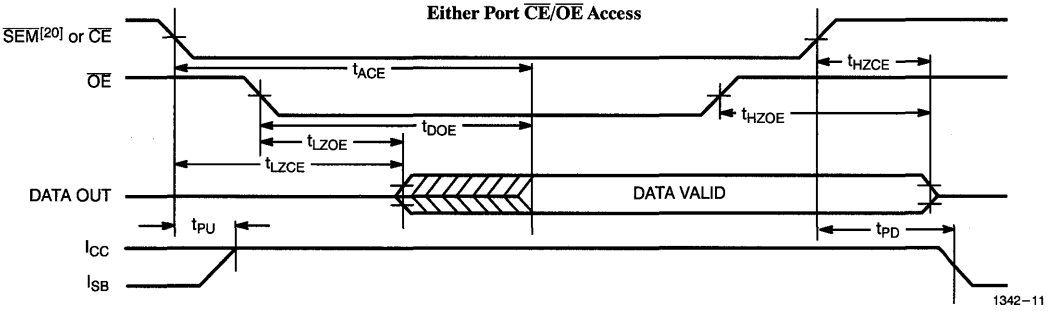
Parameter	Description	7B134–20 7B135–20 7B1342–20		7B134–25 7B135–25 7B1342–25		7B134–35 7B135–35 7B1342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE (continued)								
t_{WDD}[11]	Write Pulse to Data Delay		40		50		60	ns
t_{DDD}[11]	Write Data Valid to Read Data Valid		30		30		35	ns
SEMAPHORE TIMING[12]								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns

Switching Waveforms

Read Cycle No. 1[13,14]



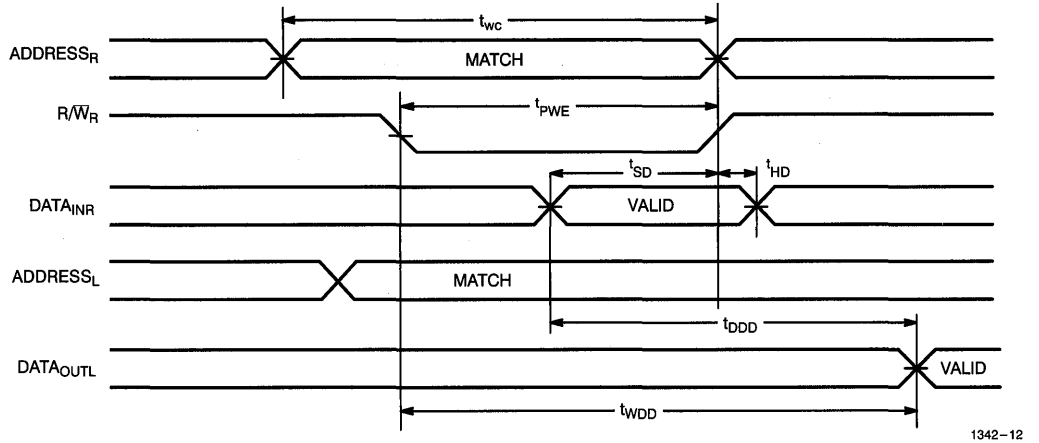
Read Cycle No. 2[13,15]



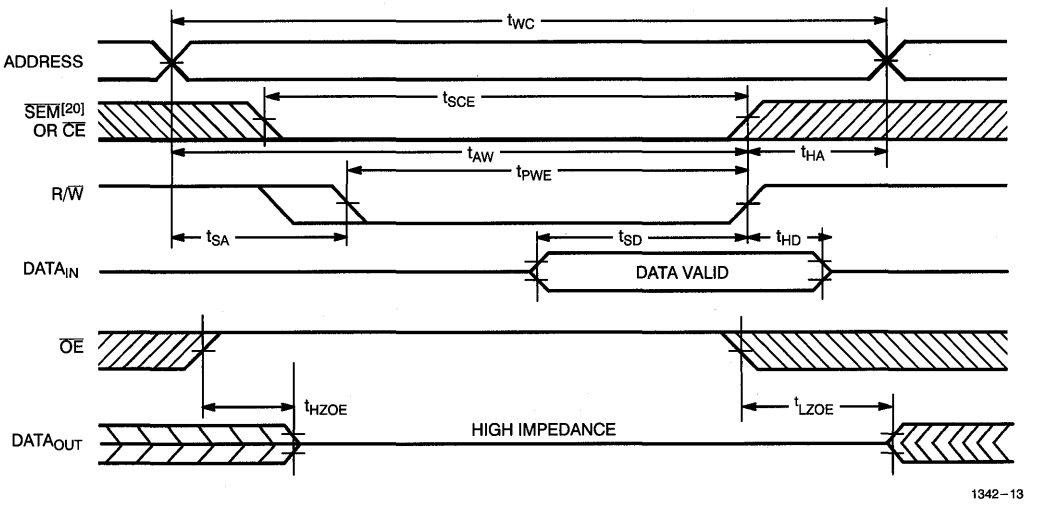
Notes:
7. See the last page of this specification for Group A subgroup testing information.
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-toPort Delay waveform.
12. Semaphore timing applies only to CY7B1342.
13. R/$\overline{W}$ is HIGH for read cycle.
14. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

Read Timing with Port-to-Port Delay[16]



Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[17,18,19]

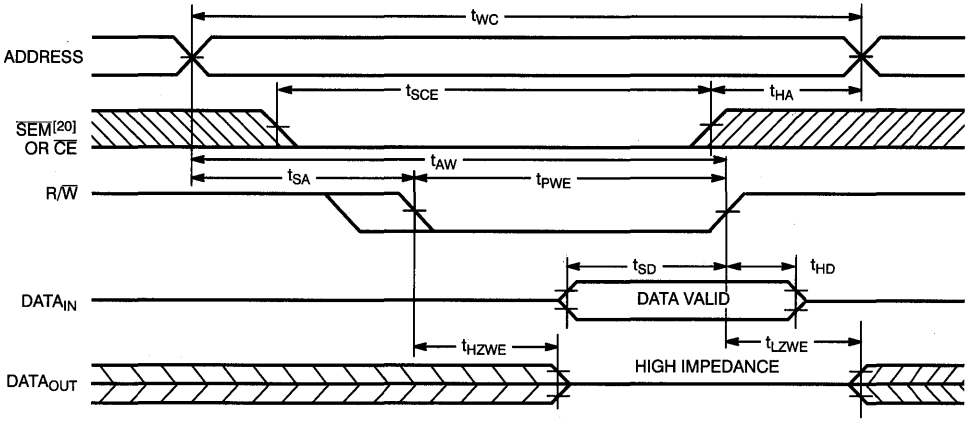


Notes:

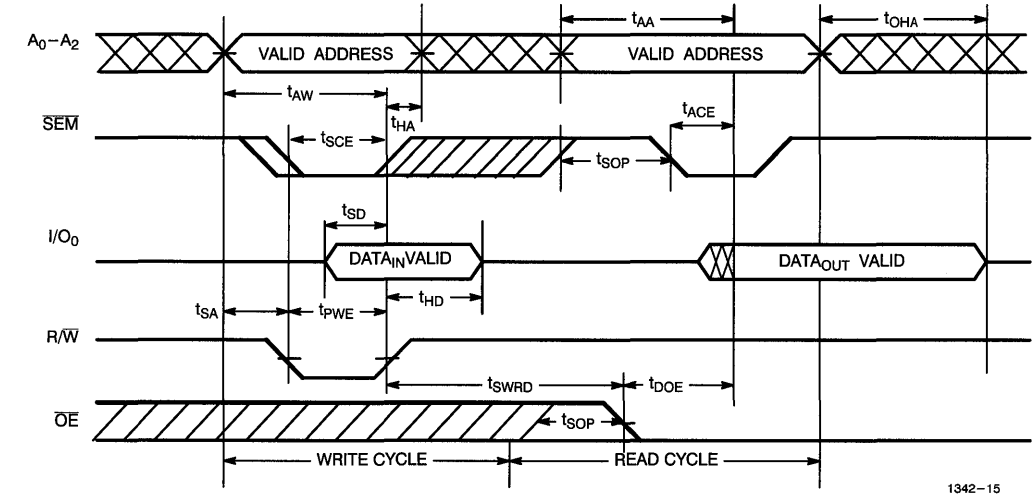
16. $\overline{CE}_L = \overline{CE}_R$ =LOW; $R/\overline{W}_L$ = HIGH
17. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and $R/\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. $R/\overline{W}$ must be HIGH during all address transactions.
19. If $\overline{OE}$ is LOW during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a $R/\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
20. $\overline{SEM}$ only applies to CY7B1342.

Switching Waveforms (continued)

Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[18,21]



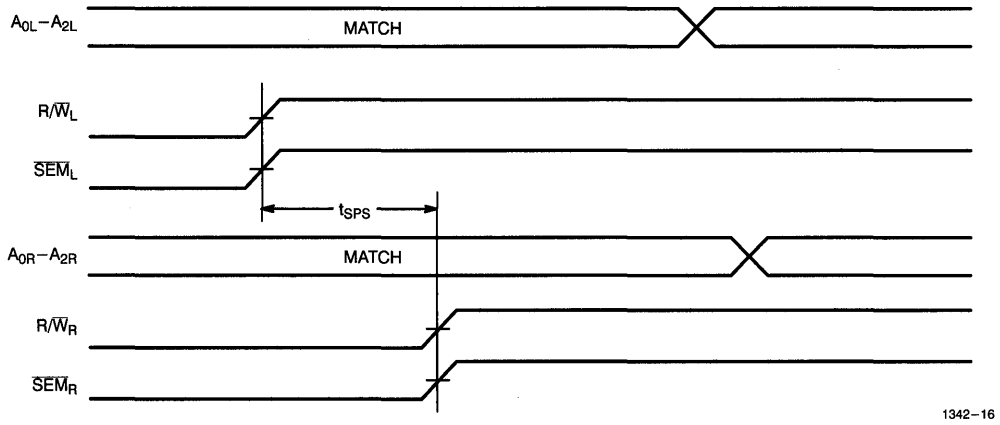
Semaphore Read After Write Timing, Either Side (CY7B1342 only)[22]



Notes:
21. Data I/O pins enter high-impedance when $\overline{OE}$ is held LOW during write.
22. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued)

Timing Diagram of Semaphore Contention (CY7B1342 only)[23,24,25]



Notes:
23. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
24. Semaphores are reset (available to both ports) at cycle start.
25. If t_{SPS} is violated, it is gauranteed that only one side will gain access to the semaphore.

Architecture

The CY7B134 and CY7B135 consist of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/W). Two semaphore control pins exist for the CY7B1342 ($\overline{SEM}_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. Since there is no on-chip arbitration, the user must be sure that a specific location will not be accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 timing diagram) or the R/$\overline{W}$ pin (see Write Cycle No. 2 timing diagram). Data can be written t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for write operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B1342 wishes to access a semaphore, the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin. Required inputs for read operations are summarized in *Table 1*.

Semaphore Operation

The CY7B1342 provides eight semaphore latches which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches. $\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. *Table 2* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side will gain access to the semaphore.

Table 1. Non-contending Read/Write

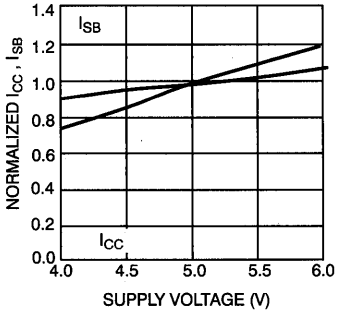
Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read $Data_{IN}$ Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Semaphore Operation Example

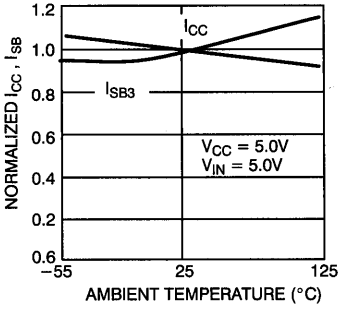
Function	I/O_0 Left	I/O_0 Right	Status
No Action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to Semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

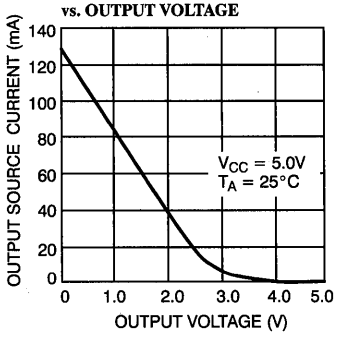
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



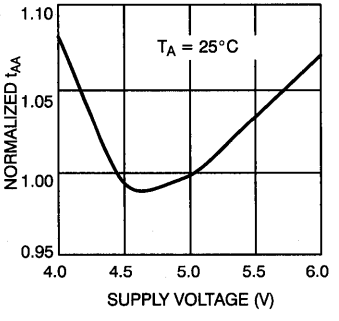
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



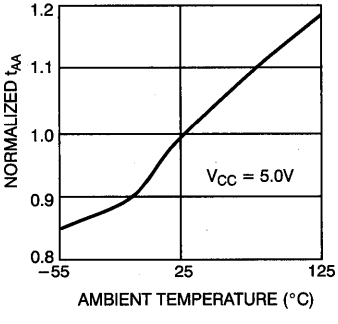
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



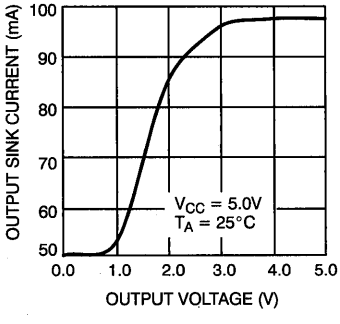
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



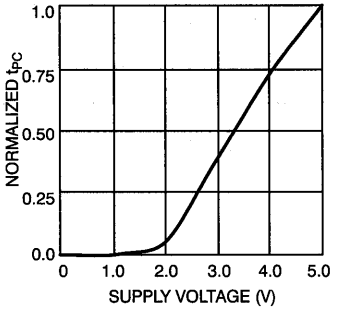
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



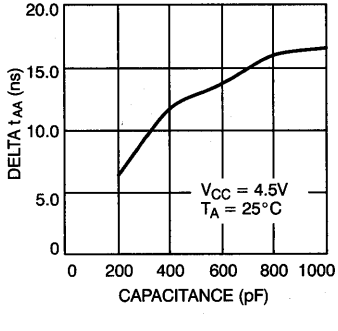
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



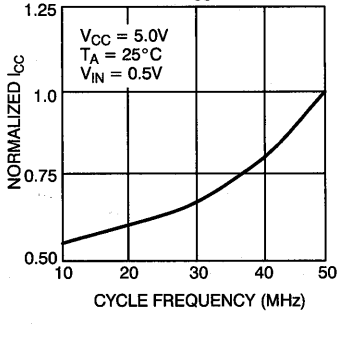
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7B134–20PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
25	CY7B134–25PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–25PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–25DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7B134–25LMB	L68	48-Square Leadless Chip Carrier	
35	CY7B134–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
	CY7B134–35LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7B135-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B135-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B135-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135-35LMB	L69	52-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7B1342-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B1342-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B1342-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342-35LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
SEMAPHORE CYCLE	
t_{SOD}	7, 8, 9, 10, 11
t_{SWRD}	7, 8, 9, 10, 11
t_{SPS}	7, 8, 9, 10, 11

Document #: 38−00161−B

CYPRESS SEMICONDUCTOR

4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (com'l)**
  - **— 25 ns (mil)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC/PGA**
- **TTL compatible**

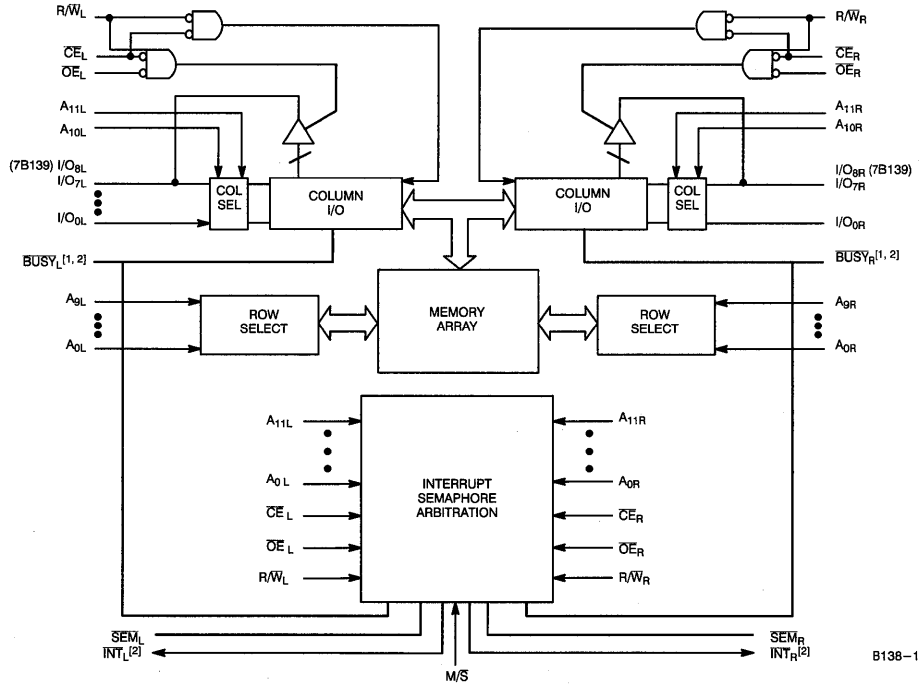
Functional Description

The CY7B138 and CY7B139 are high-speed BiCMOS 4K x 8 and 4K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B138/9 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B138/9 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B138 and CY7B139 are available in 68-pin LCCs, PLCCs, and PGAs.

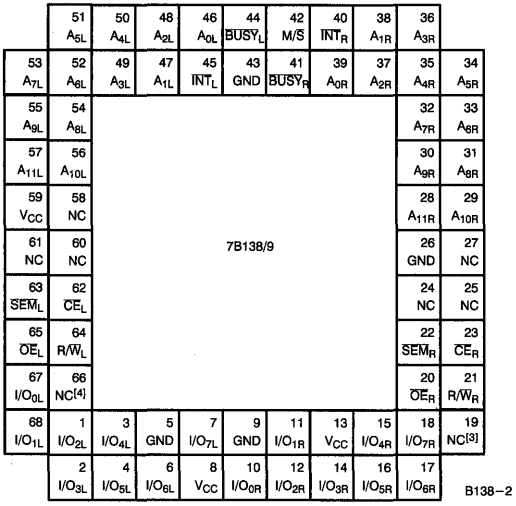
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

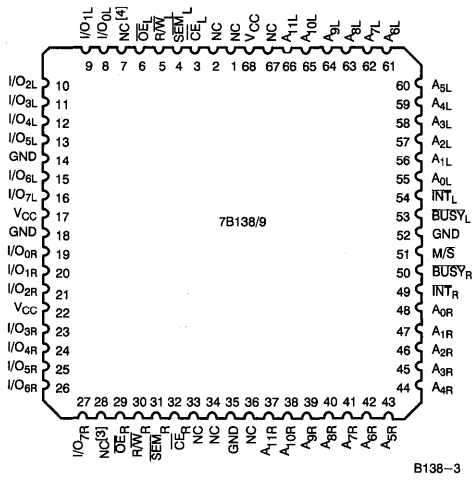
Pin Configurations

68-Pin PGA
Top View



B138–2

68-Pin LCC/PLCC
Top View



B138–3

Notes:
3. I/O_{8R} on the CY7B139.
4. I/O_{8L} on the CY7B139.

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location FFE and is cleared when left port reads location FFE. $\overline{INT}_R$ is set when left port writes location FFF and is cleared when right port reads location FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B138–15 7B139–15	7B138–25 7B139–25	7B138–35 7B139–35
Maximum Access Time (ns)		15	25	35
Maximum Operating Current (mA)	Commercial	260	220	210
	Military		280	250
Maximum Standby Current for I_{SB1}(mA)	Commercial	90	75	70
	Military		80	75

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage[5] ..... – 0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	−40°C to + 85°C	5V ± 10%
Military[6]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B138–15 7B139–15 Min.	7B138–15 7B139–15 Max.	7B138–25 7B139–25 Min.	7B138–25 7B139–25 Max.	7B138–35 7B139–35 Min.	7B138–35 7B139–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2..4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		260		220		210	mA
			Mil/Ind				280		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		75		70	mA
			Mil/Ind				80		75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		160		140		130	mA
			Mil/Ind				180		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		25		25		25	mA
			Mil/Ind				30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		140		120		110	mA
			Mil/Ind				150		130	

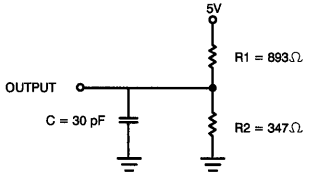
Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

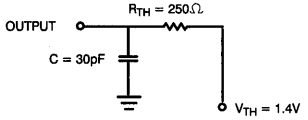
5. Pulse width < 20 ns.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



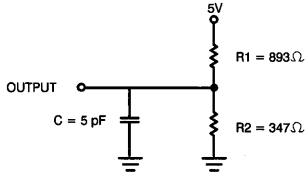
(a) Normal Load (Load 1)

B138–4



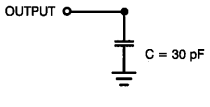
(b) Thevenin Equivalent (Load 1)

B138–5



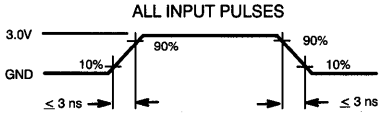
(c) Three-State Delay (Load 3)

B138–6



Load (Load 2)

B138–7



B138–8

Switching Characteristics Over the Operating Range[10,11]

Parameter	Description	7B138–15 7B139–15		7B138–25 7B139–25		7B138–35 7B139–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{AA}	Address to Data Valid		15		25		35	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20	ns
t_{LZOE}[12, 13]	$\overline{OE}$ Low to Low Z	3		3		3		ns
t_{HZOE}[12, 13]	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCE}[12, 13]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[12, 13]	$\overline{CE}$ HIGH to High Z		10		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		ns
t_{AW}	Address Set-Up to Write End	12		20		30		ns
t_{HA}	Address Hold From Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold From Write End	0		0		0		ns
t_{HZWE}[13]	R/$\overline{W}$ LOW to High Z		10		15		20	ns
t_{LZWE}[13]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns
t_{WDD}[14]	Write Pulse to Data Delay		30		50		60	ns
t_{DDD}[14]	Write Data Valid to Read Data Valid		25		30		35	ns

Switching Characteristics Over the Operating Range[10, 11] (continued)

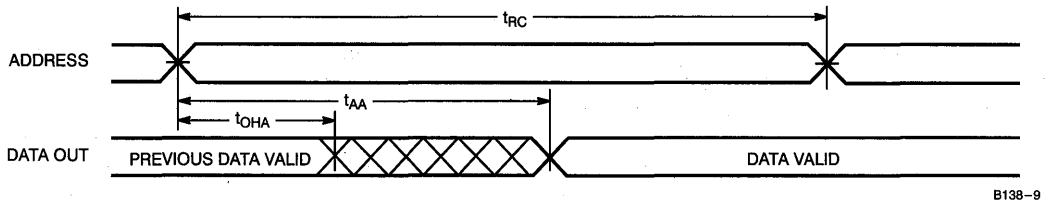
Parameter	Description	7B138–15 7B139–15		7B138–25 7B139–25		7B138–35 7B139–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING[15]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20	ns
t_{PS}	Port Set-Up for Priority		5		5		5	ns
t_{WB}	$\overline{WE}$ LOW after $\overline{BUSY}$ LOW		0		0		0	ns
t_{WH}	$\overline{WE}$ HIGH after $\overline{BUSY}$ HIGH		13		20		30	ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35	ns
INTERRUPT TIMING[15]								
t_{INS}	$\overline{INT}$ Set Time		15		25		25	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25	ns
SEMAPHORE TIMING								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns

Notes:

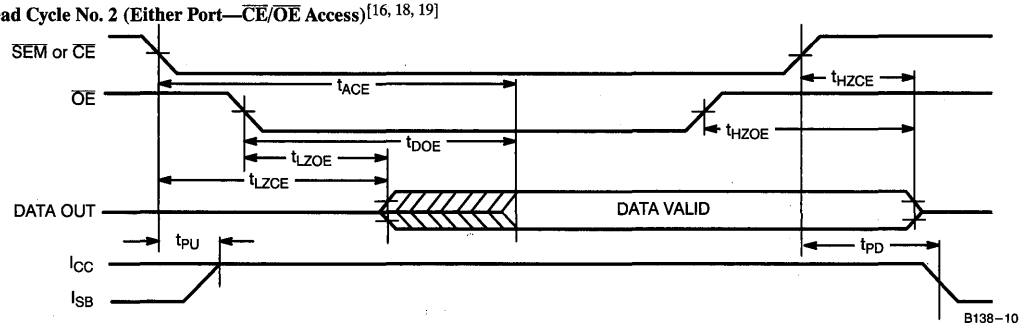
10. See the last page of this specification for Group A subgroup testing information.
11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. Test conditions used are Load 3.
14. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
15. Test conditions used are Load 2.

Switching Waveforms

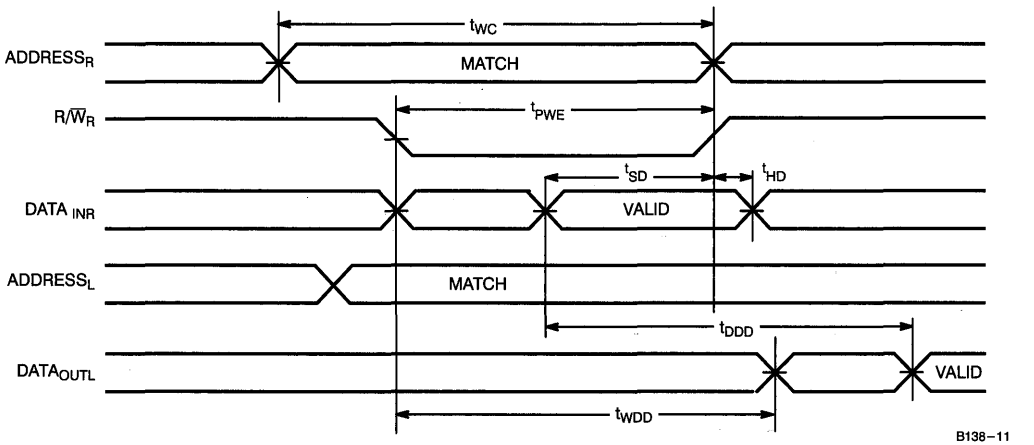
Read Cycle No. 1 (Either Port—Address Access)[16, 17]



Read Cycle No. 2 (Either Port—$\overline{CE}/\overline{OE}$ Access)[16, 18, 19]



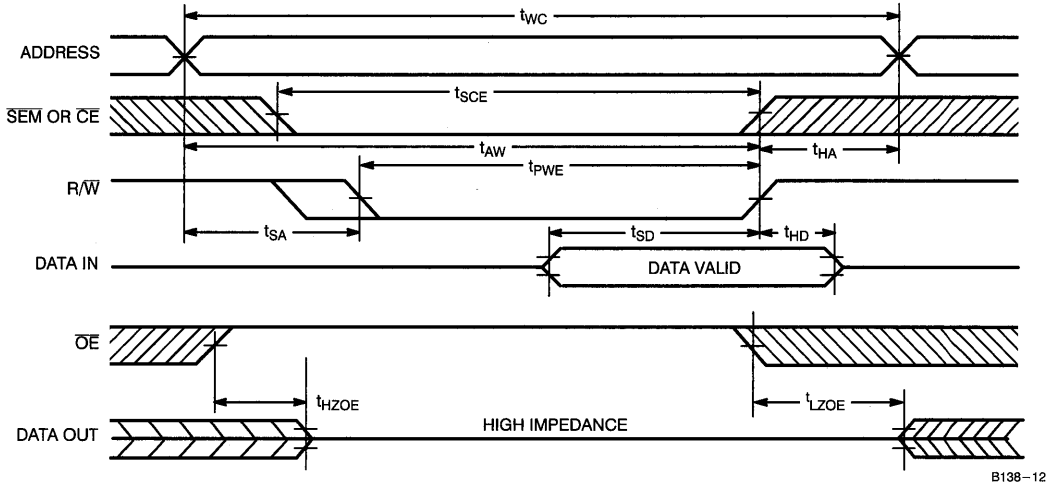
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[20, 21]



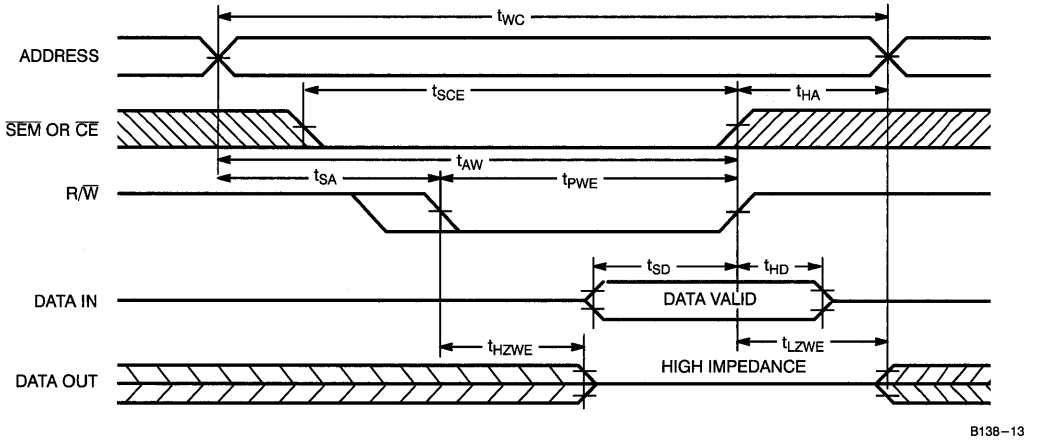
Notes:
16. R/$\overline{W}$ is HIGH for read cycle.
17. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
20. $\overline{BUSY}$ = HIGH for the writing port.
21. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[22, 23, 24]



Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[22, 24, 25]

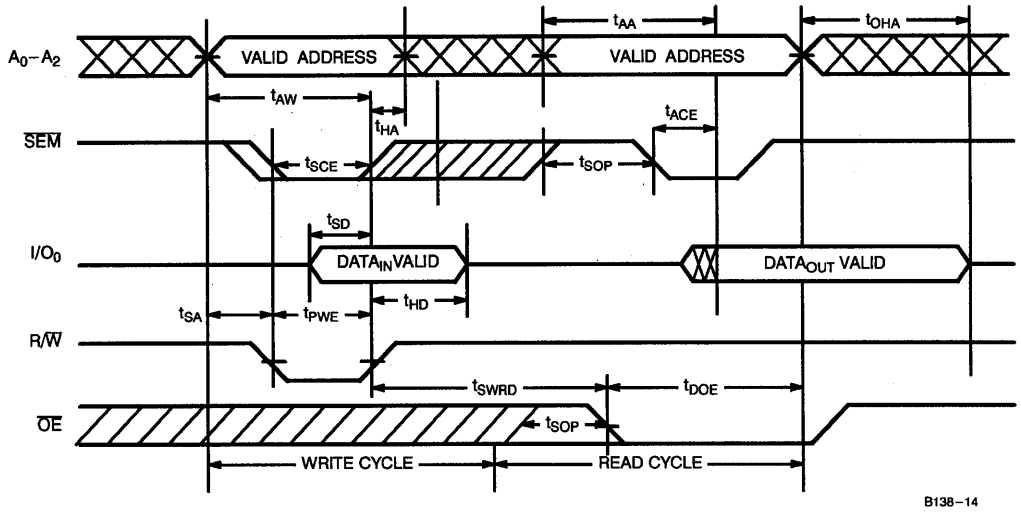


Notes:

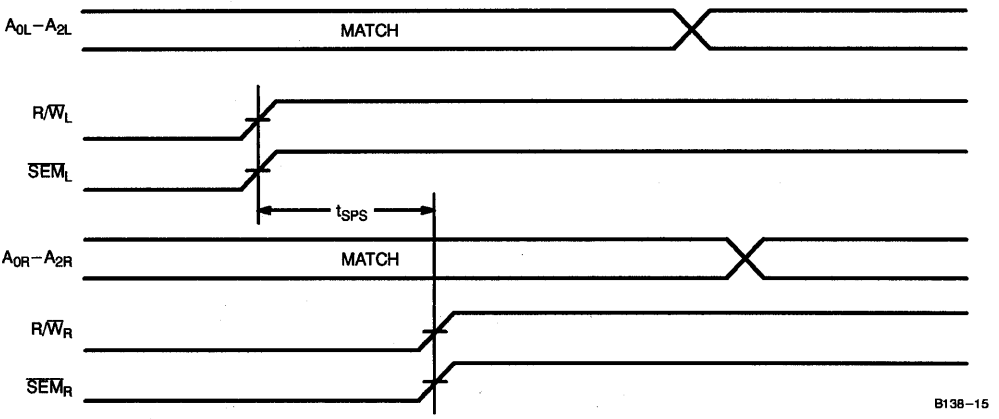
22. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
24. R/$\overline{W}$ must be HIGH during all address transitions.
25. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[26]



Timing Diagram of Semaphore Contention[27, 28, 29]

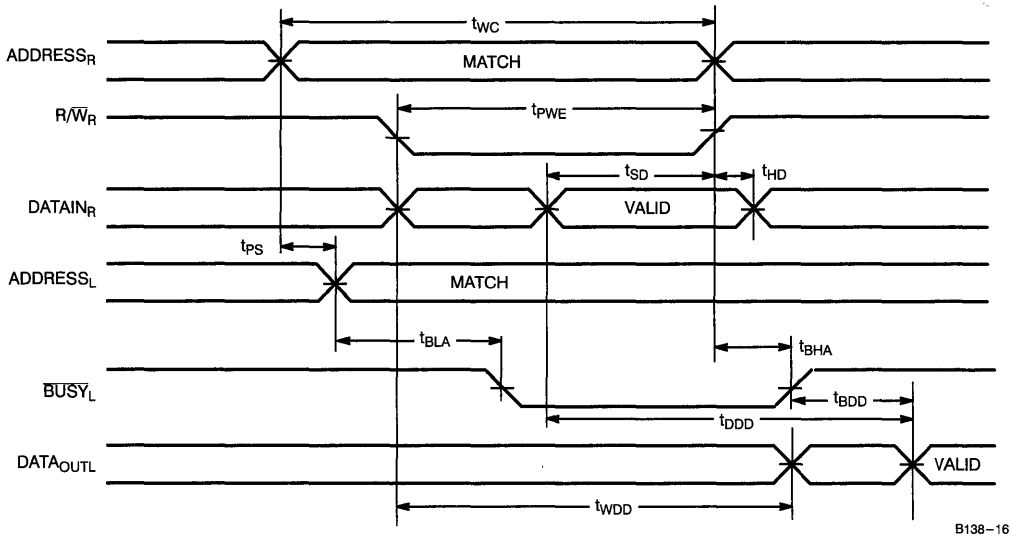


Notes:

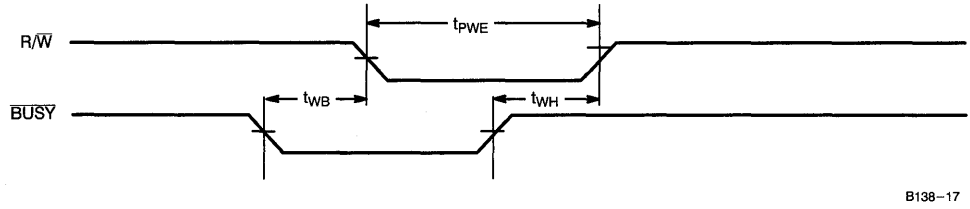
26. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
27. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
28. Semaphores are reset (available to both ports) at cycle start.
29. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[21]



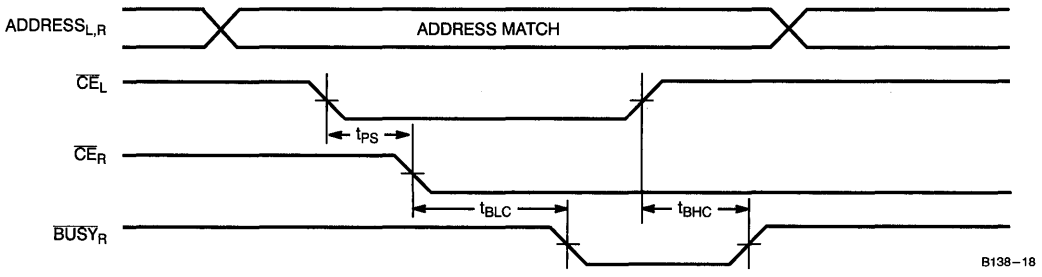
Write Timing with Busy Input (M/$\overline{S}$=LOW)



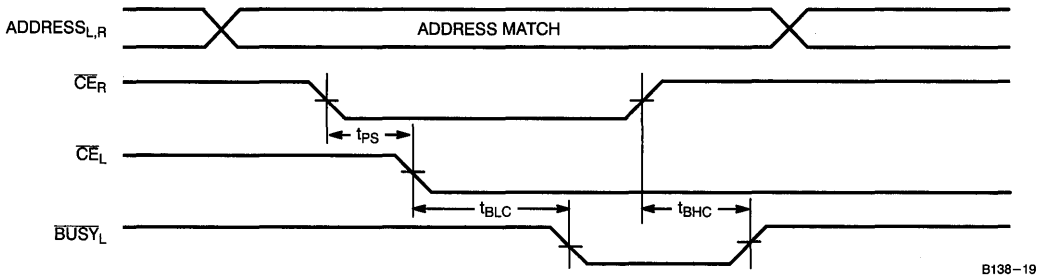
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[30]

$\overline{CE}_L$ Valid First:

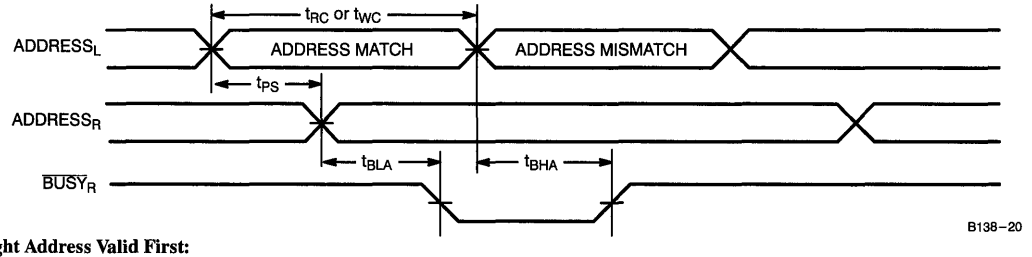


$\overline{CE}_R$ Valid First:

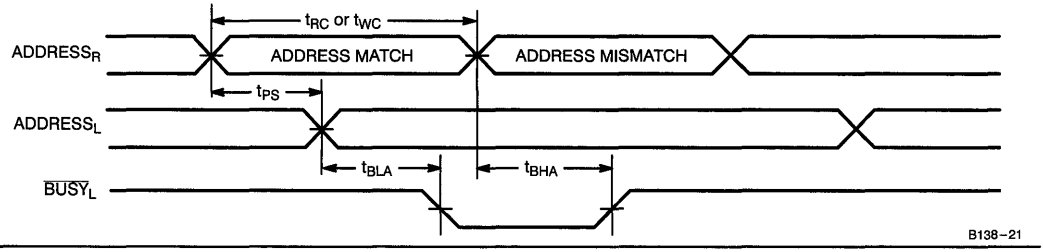


Busy Timing Diagram No. 2 (Address Arbitration)[30]

Left Address Valid First:



Right Address Valid First:

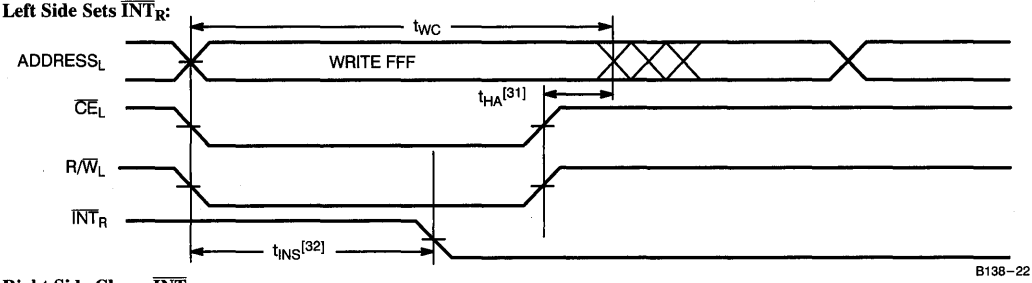


Note:
30. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

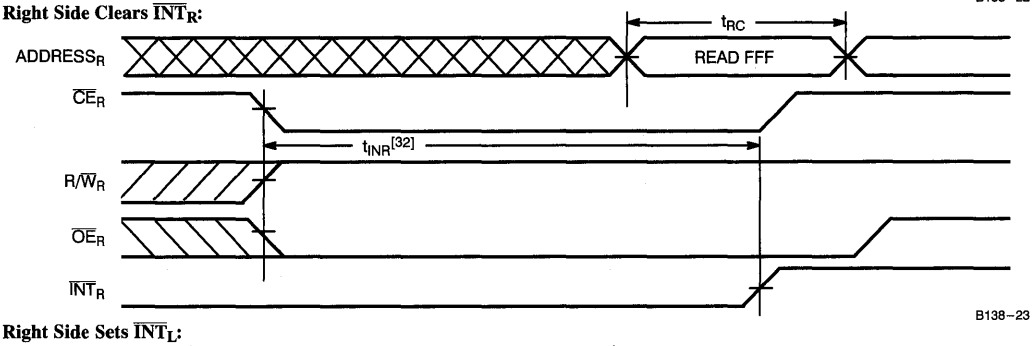
Switching Waveforms (continued)

Interrupt Timing Diagrams

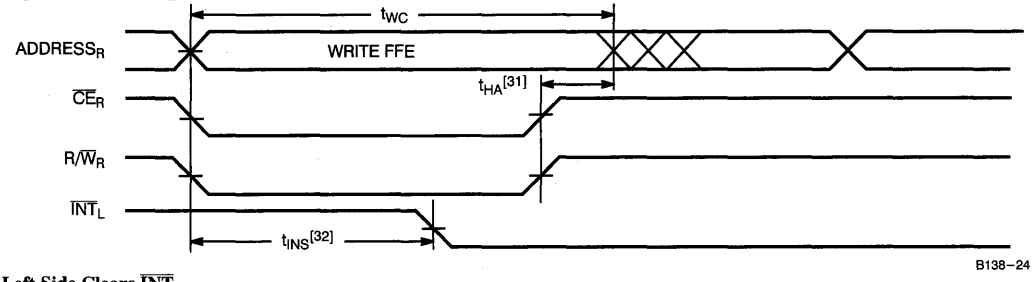
Left Side Sets $\overline{INT}_R$:



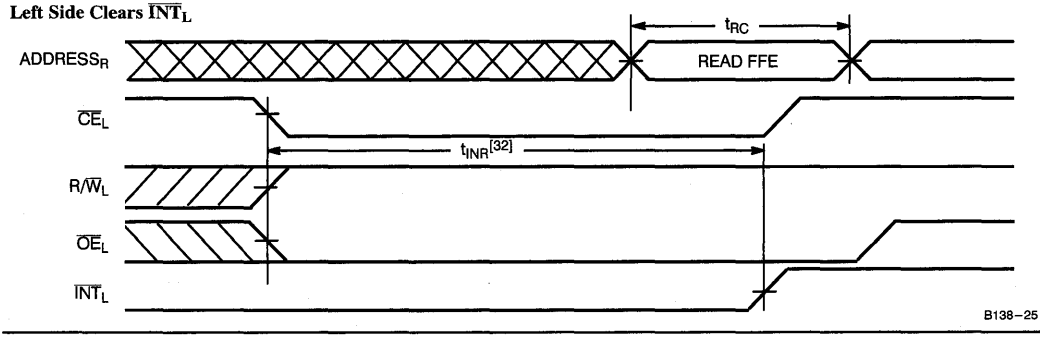
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Notes:

31. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
32. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7B138/9 consists of an array of 4K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B138/9 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B138/9 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7B138/9 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B138/9 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B138/9 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the a semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

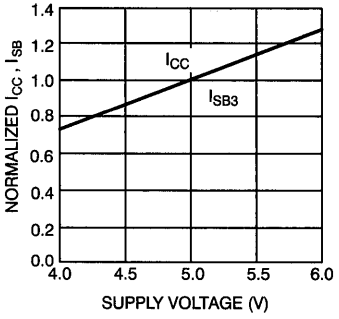
	Left Port					Right Port				
Function	**R/$\overline{W}$**	**$\overline{CE}$**	**$\overline{OE}$**	**A_{0-11}**	**$\overline{INT}$**	**R/$\overline{W}$**	**$\overline{CE}$**	**$\overline{OE}$**	**A_{0-11}**	**$\overline{INT}$**
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	FFE	X
Reset Left $\overline{INT}$	X	L	L	FFE	H	X	X	X	X	X
Set Right $\overline{INT}$	L	L	X	FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	FFF	H

Table 3. Semaphore Operation Example

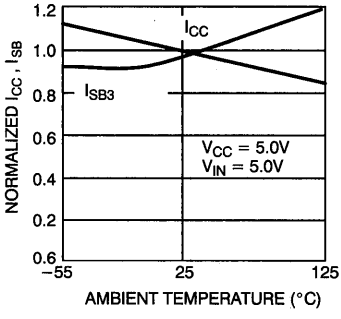
Function	I/O 0 Left	I/O 0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

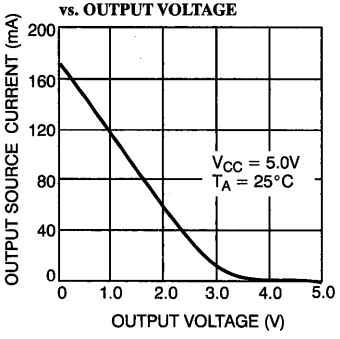
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



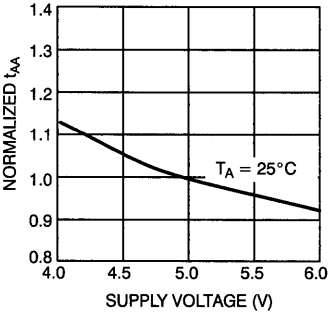
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



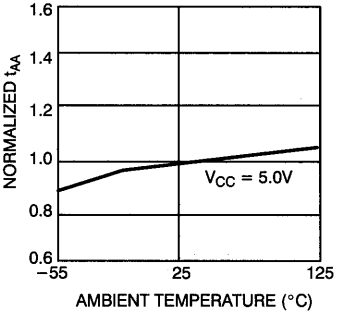
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



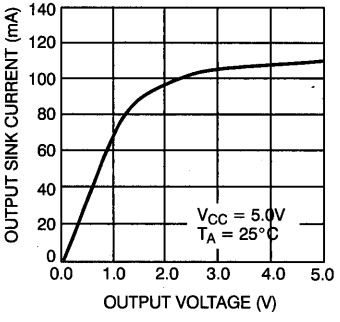
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



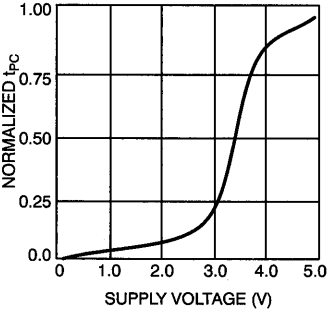
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



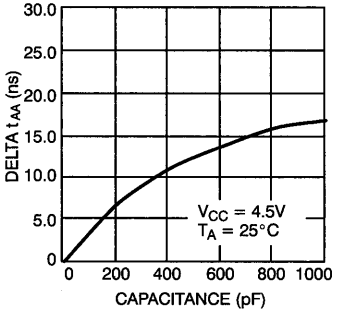
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



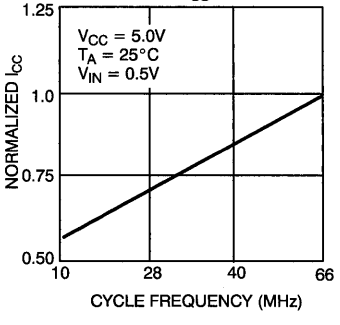
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B138–15GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B138–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B138–25GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B138–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B138–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B138–35GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B138–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B138–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–35LMB	L81	68-Square Leadless Chip Carrier	Military

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15	CY7B139–15GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B139–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B139–25GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B139–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B139–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B139–35GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B139–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B139–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–35LMB	L81	68-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38–00162–E

CYPRESS SEMICONDUCTOR

8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC/PGA**
- **TTL compatible**

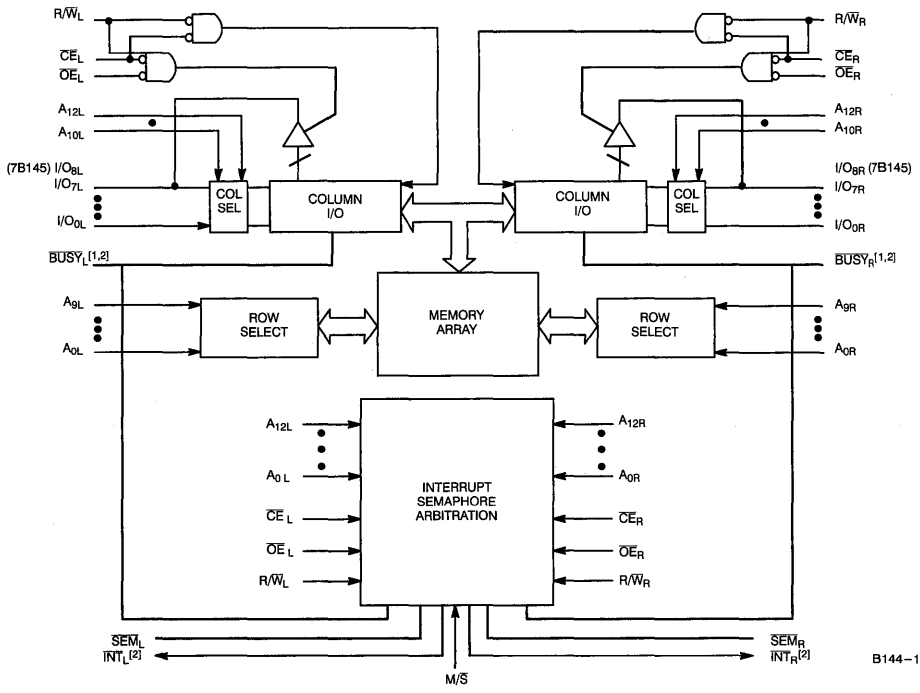
Functional Description

The CY7B144 and CY7B145 are high-speed BiCMOS 8K x 8 and 8K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B144/5 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B144/5 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B144 and CY7B145 are available in 68-pin LCCs, PLCCs, and PGAs.

Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

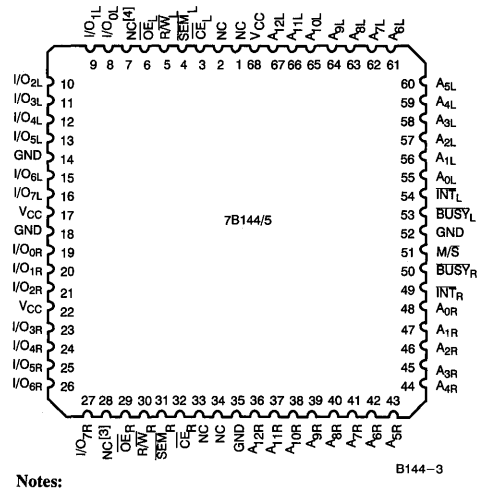
Pin Configurations

68-Pin PGA
Top View

	51 A_{5L}	50 A_{4L}	48 A_{2L}	46 A_{0L}	44 $\overline{BUSY}_L$	42 M/$\overline{S}$	40 $\overline{INT}_R$	38 A_{1R}	36 A_{3R}	
53 A_{7L}	52 A_{6L}	49 A_{3L}	47 A_{1L}	45 $\overline{INT}_L$	43 GND	41 $\overline{BUSY}_R$	39 A_{0R}	37 A_{2R}	35 A_{4R}	34 A_{5R}
55 A_{9L}	54 A_{8L}								32 A_{7R}	33 A_{6R}
57 A_{11L}	56 A_{10L}								30 A_{9R}	31 A_{8R}
59 V_{CC}	58 A_{12L}								28 A_{11R}	29 A_{10R}
61 NC	60 NC				7B144/5				26 GND	27 A_{12R}
63 $\overline{SEM}_L$	62 $\overline{CE}_L$								24 NC	25 NC
65 $\overline{OE}_L$	64 R/$\overline{W}_L$								22 $\overline{SEM}_R$	23 $\overline{CE}_R$
67 I/O_{0L}	66 NC[4]								20 $\overline{OE}_R$	21 R/$\overline{W}_R$
68 I/O_{1L}	1 I/O_{2L}	3 I/O_{4L}	5 GND	7 I/O_{7L}	9 GND	11 I/O_{1R}	13 V_{CC}	15 I/O_{4R}	18 I/O_{7R}	19 NC[3]
	2 I/O_{3L}	4 I/O_{5L}	6 I/O_{6L}	8 V_{CC}	10 I/O_{0R}	12 I/O_{2R}	14 I/O_{3R}	16 I/O_{5R}	17 I/O_{6R}	

B144-2

68-Pin LCC/PLCC
Top View



B144-3

Notes:
3. I/O_{8R} on the CY7B145.
4. I/O_{8L} on the CY7B145.

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data bus Input/Output
A_{0L-12L}	A_{0R-12R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B144-15 7B145-15	7B144-25 7B145-25	7B144-35 7B145-35
Maximum Access Time (ns)		15	25	35
Maximum Operating Current (mA)	Commercial	260	220	210
	Military		280	250
Maximum Standby Current for I_{SB1} (mA)	Commercial	90	75	70
	Military		80	75

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[5] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[6]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B144−15 7B145−15 Min.	7B144−15 7B145−15 Max.	7B144−25 7B145−25 Min.	7B144−25 7B145−25 Max.	7B144−35 7B145−35 Min.	7B144−35 7B145−35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2..4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		260		220		210	mA
			Mil/Ind				280		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		75		70	mA
			Mil/Ind				80		75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		160		140		130	mA
			Mil/Ind				180		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		25		25		25	mA
			Mil/Ind				30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		140		120		110	mA
			Mil/Ind				150		130	

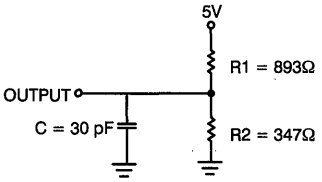
Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

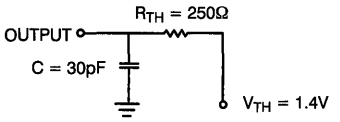
5. Pulse width < 20 ns.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



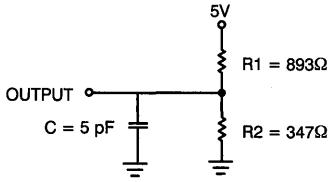
(a) Normal Load (Load 1)

B144–4



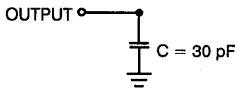
(b) Thévenin Equivalent (Load 1)

B144–5



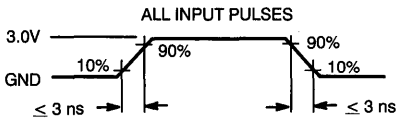
(c) Three-State Delay (Load 3)

B144–6



Load (Load 2)

B144–7



B144–8

Switching Characteristics Over the Operating Range[10,11]

Parameter	Description	7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{AA}	Address to Data Valid		15		25		35	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20	ns
t_{LZOE}[12, 13]	$\overline{OE}$ Low to Low Z	3		3		3		ns
t_{HZOE}[12, 13]	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCE}[12, 13]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[12, 13]	$\overline{CE}$ HIGH to High Z		10		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		ns
t_{AW}	Address Set-Up to Write End	12		20		30		ns
t_{HA}	Address Hold From Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold From Write End	0		0		0		ns
t_{HZWE}[13]	R/$\overline{W}$ LOW to High Z		10		15		20	ns
t_{LZWE}[13]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns
t_{WDD}[14]	Write Pulse to Data Delay	30			50		60	ns
t_{DDD}[14]	Write Data Valid to Read Data Valid	25			30		35	ns

Switching Characteristics Over the Operating Range[10,11] (continued)

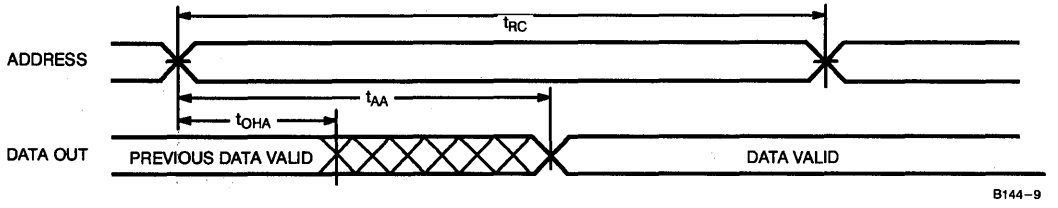
Parameter	Description	7B144–15 7B145–15		7B144–25 7B145–25		7B144–35 7B145–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING[15]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20	ns
t_{PS}	Port Set-Up for Priority		5		5		5	ns
t_{WB}	$\overline{WE}$ LOW after $\overline{BUSY}$ LOW		0		0		0	ns
t_{WH}	$\overline{WE}$ HIGH after $\overline{BUSY}$ HIGH		13		20		30	ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35	ns
INTERRUPT TIMING[15]								
t_{INS}	$\overline{INT}$ Set Time		15		25		25	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25	ns
SEMAPHORE TIMING								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns

Notes:

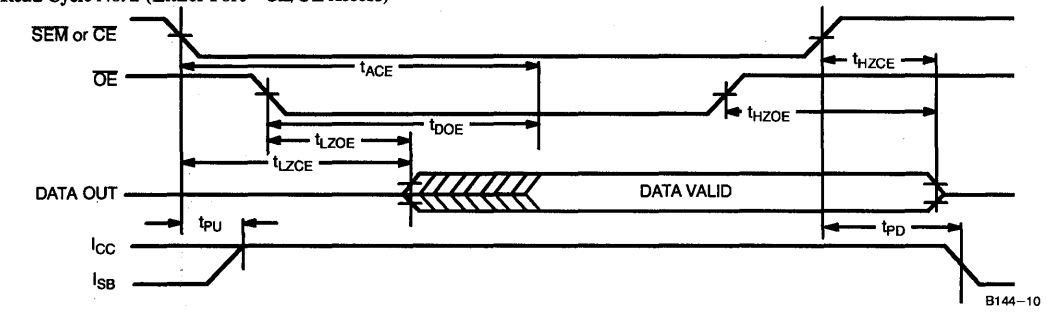
10. See the last page of this specification for Group A subgroup testing information.
11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. Test conditions used are Load 3.
14. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
15. Test conditions used are Load 2.

Switching Waveforms

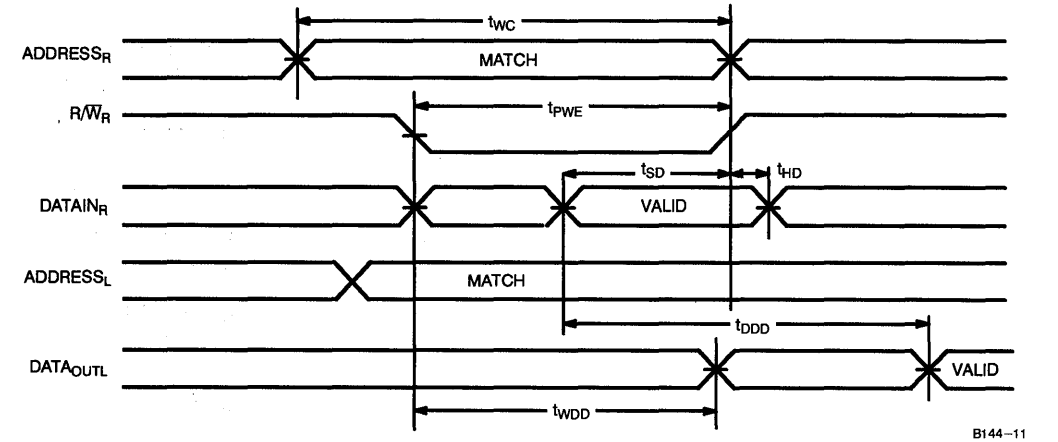
Read Cycle No. 1 (Either Port—Address Access)[16, 17]



Read Cycle No. 2 (Either Port—$\overline{CE}/\overline{OE}$ Access)[16, 18, 19]



Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[20, 21]

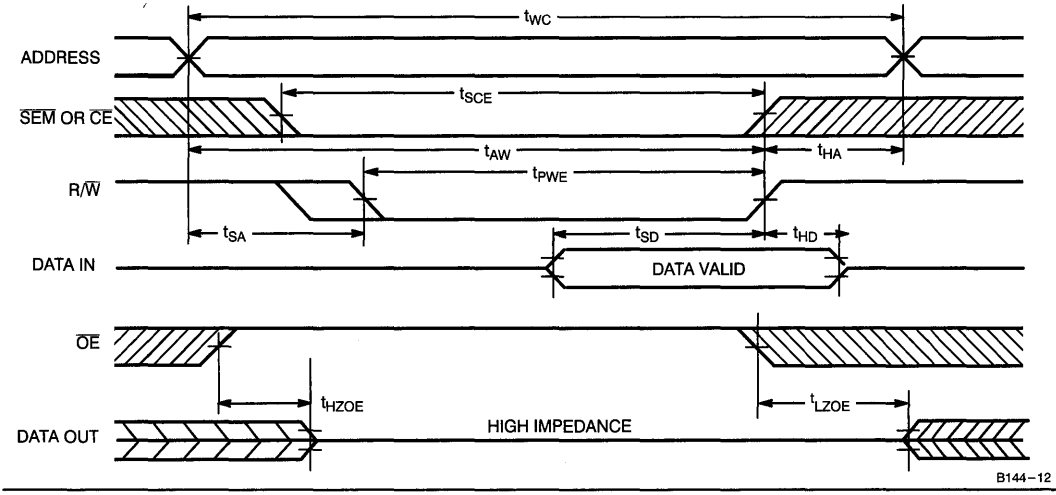


Notes:

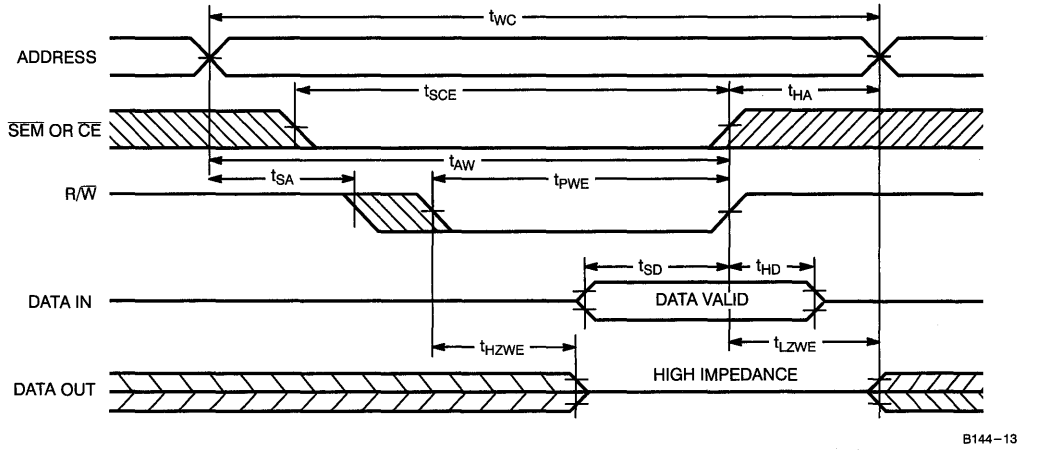
16. $R/\overline{W}$ is HIGH for read cycle.
17. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
20. $\overline{BUSY}$ = HIGH for the writing port.
21. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[22, 23,24]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[22, 24, 25,]

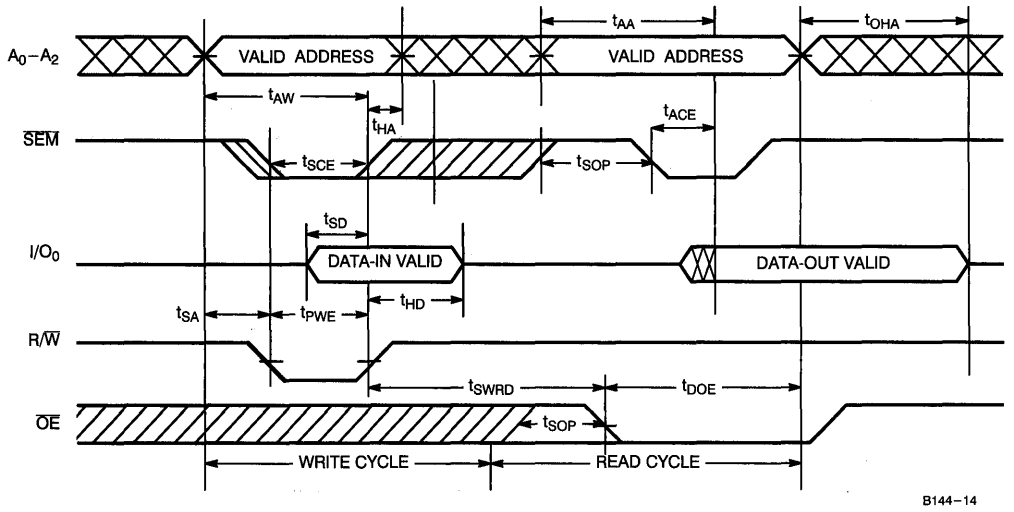


Notes:

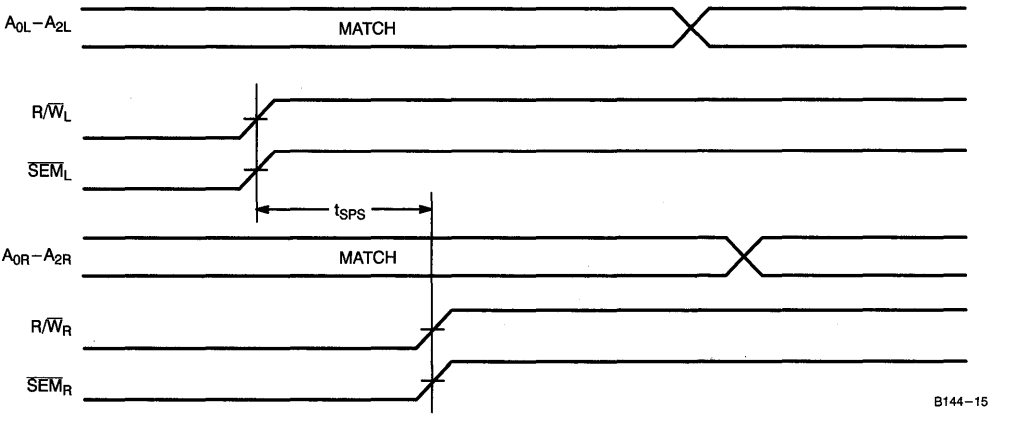
22. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
24. R/$\overline{W}$ must be HIGH during all address transitions.
25. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[26]



Semaphore Contention[27, 28, 29]

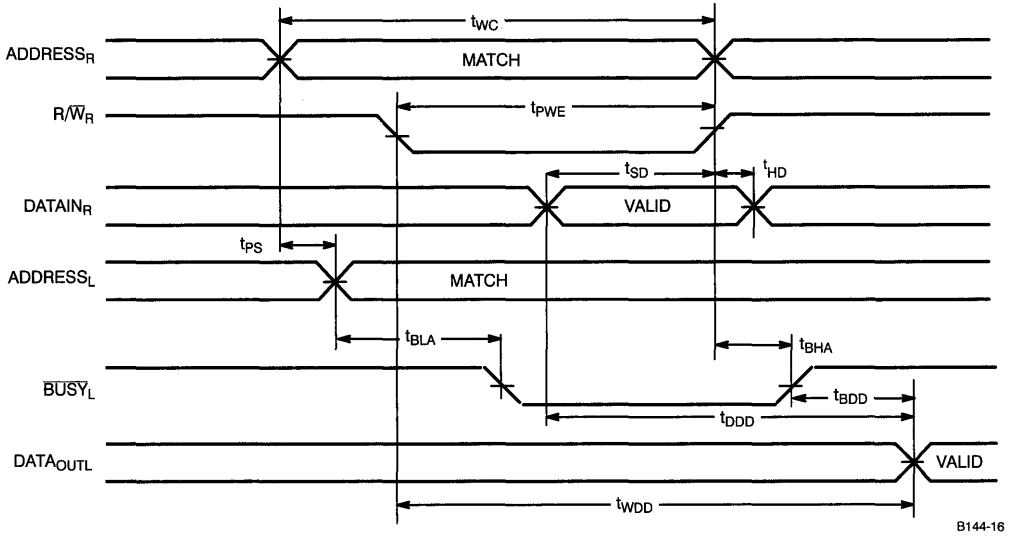


Notes:

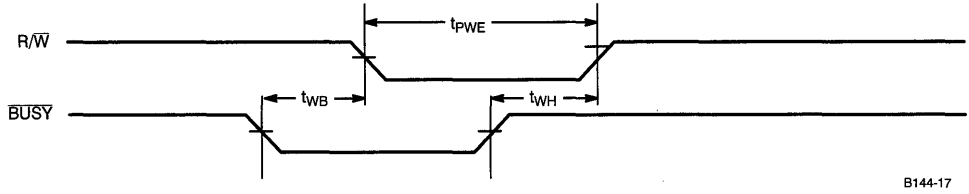
26. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
27. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
28. Semaphores are reset (available to both ports) at cycle start.
29. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[21]



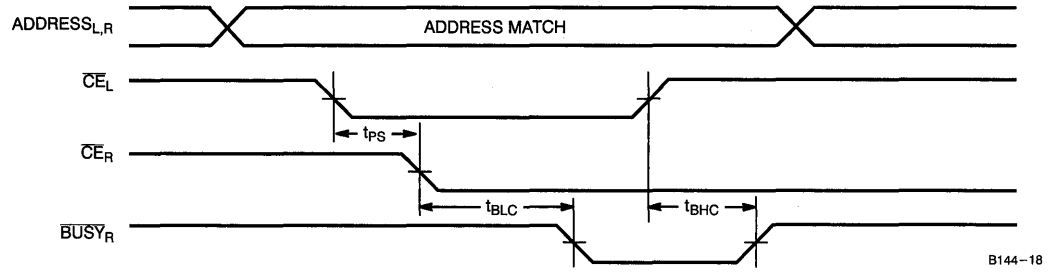
Write Timing with Busy Input (M/$\overline{S}$=LOW)



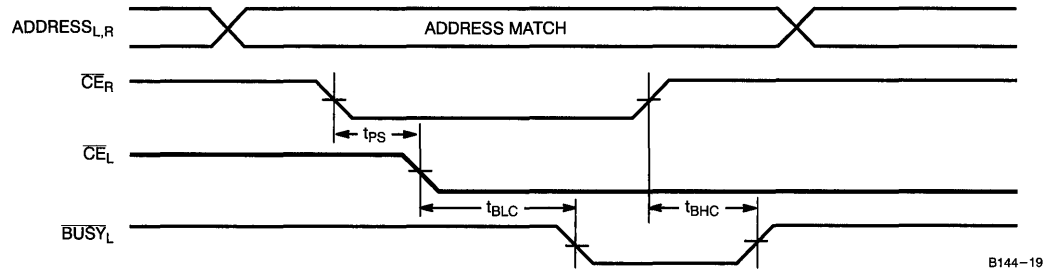
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[30]

$\overline{CE}_L$ Valid First:

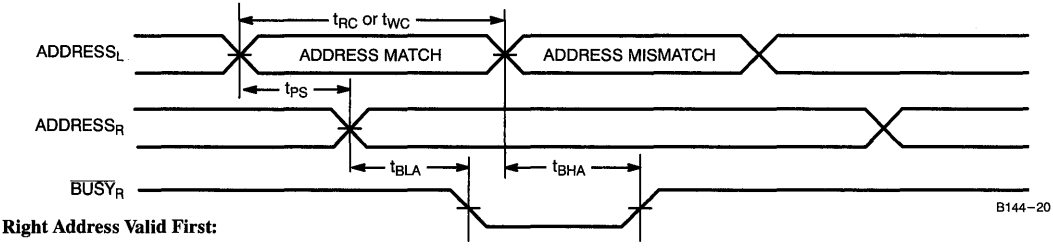


$\overline{CE}_R$ Valid First:

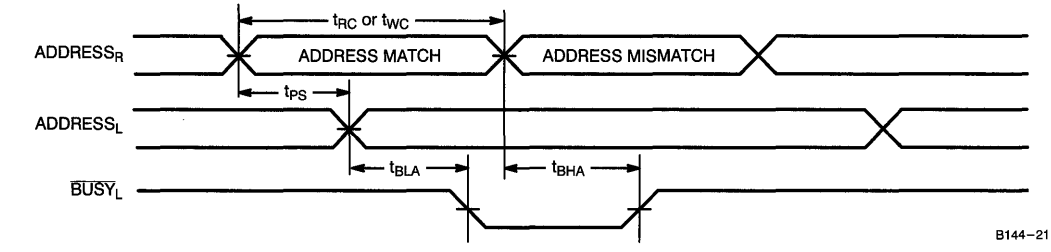


Busy Timing Diagram No. 2 (Address Arbitration)[30]

Left Address Valid First:



Right Address Valid First:



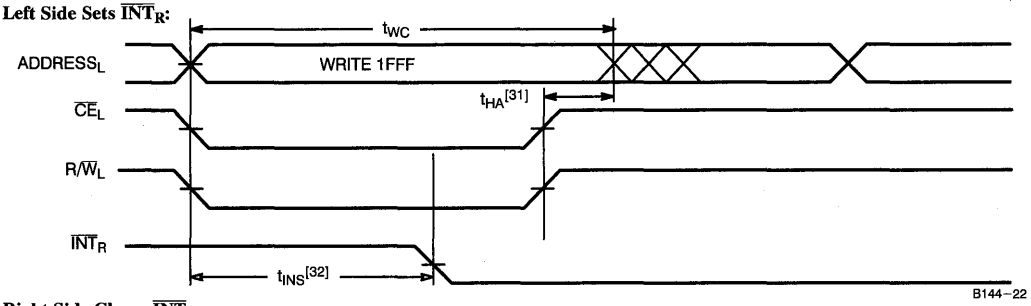
Note:

30. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted
31. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
32. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

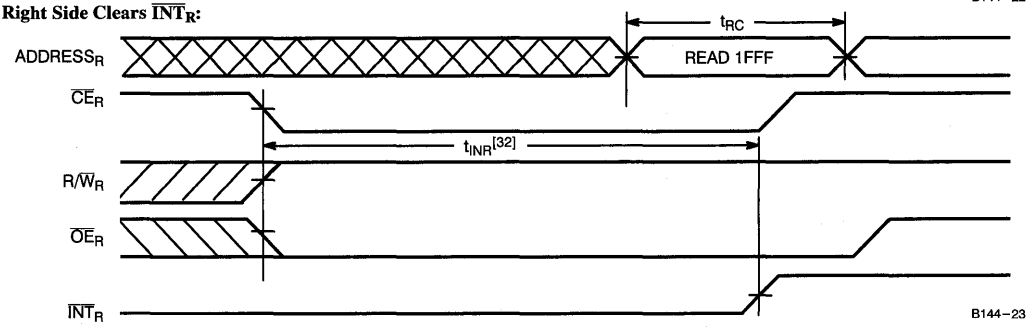
Switching Waveforms (continued)

Interrupt Timing Diagrams

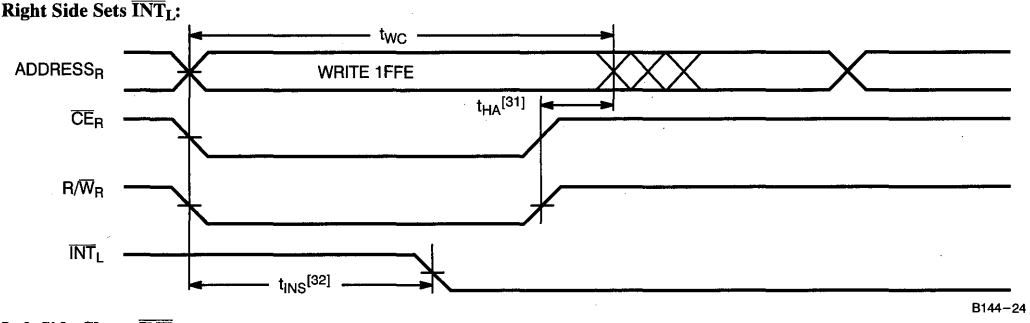
Left Side Sets $\overline{INT}_R$:



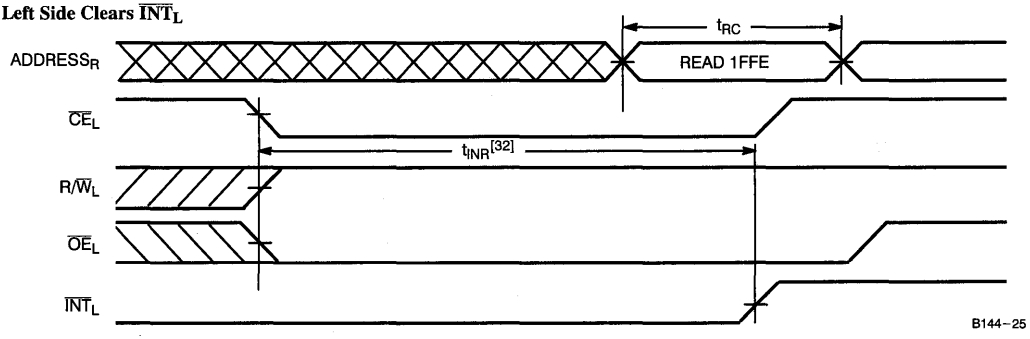
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Architecture

The CY7B144/5 consists of a an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B144/5 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B144/5 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B144/5 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

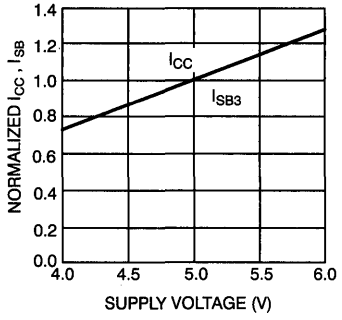
	Left Port					Right Port				
Function	**R/$\overline{W}$**	**$\overline{CE}$**	**$\overline{OE}$**	**A_{0-12}**	**$\overline{INT}$**	**R/$\overline{W}$**	**$\overline{CE}$**	**$\overline{OE}$**	**A_{0-12}**	**$\overline{INT}$**
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset Left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 3. Semaphore Operation Example

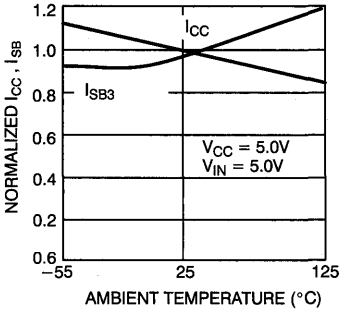
Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

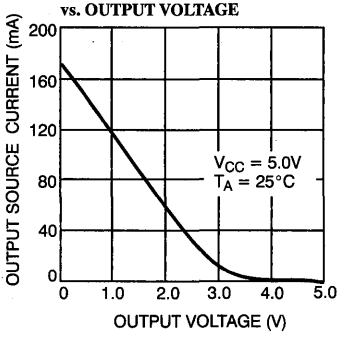
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



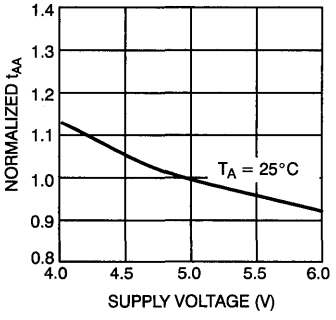
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



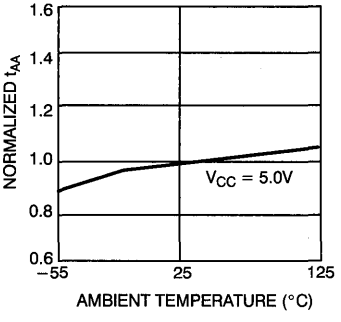
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



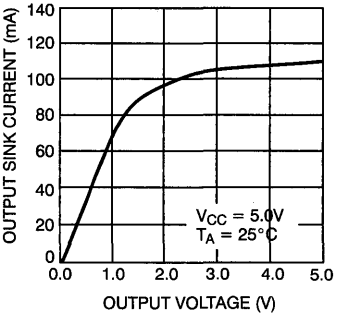
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



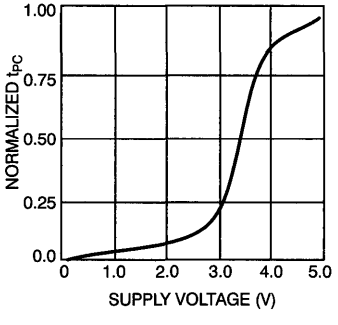
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



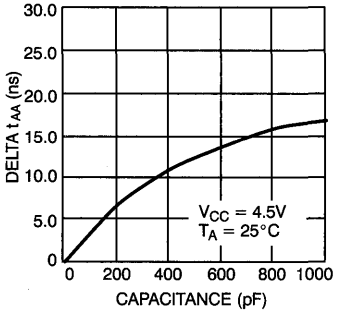
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



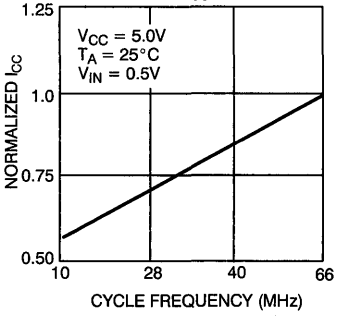
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B144–15GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B144–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B144–25GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B144–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B144–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B144–35GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B144–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B144–35LMB	L81	68-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B145–15GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B145–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B145–25GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B145–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B145–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B145–35GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7B145–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B145–35LMB	L81	68-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38-00163-E

CY7C148
CY7C149

CYPRESS SEMICONDUCTOR

1K x 4 Static RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25-ns access time**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power (7C148)**
  - **— 82.5 mW (25-ns version)**
  - **— 55 mW (all others)**
- **5-volt power supply ± 10% tolerance, both commercial and military**
- **TTL-compatible inputs and outputs**

Functional Description

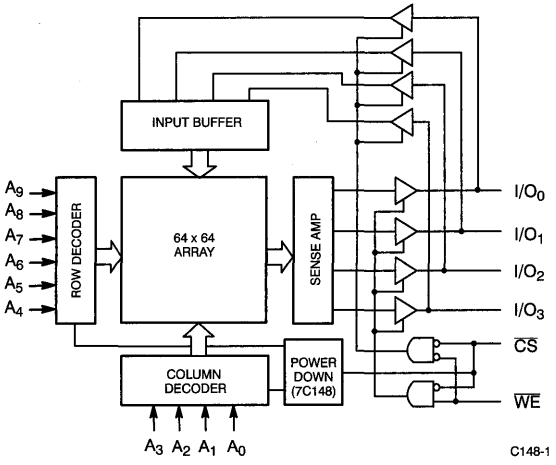
The CY7C148 and CY7C149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the memory locations specified on the address pins (A_0 through A_9).

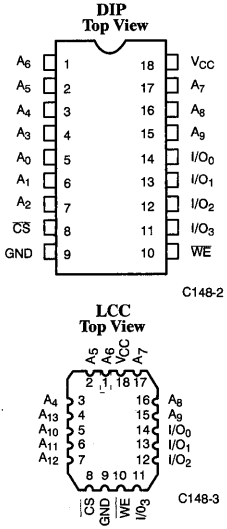
Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

The I/O pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C148–25	7C148–35	7C148–45	7C149–25	7C149–35	7C149–45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C148/9−25 Min.	7C148/9−25 Max.	7C148/9−35,45 Min.	7C148/9−35,45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled			−50	50	−50	50	µA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS}$ ≤ V_{IL}, Output Open		Com'l		90		80	mA
				Mil				110	
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{OS}	Output Short Circuit Current[4]	GND ≤ V_O ≤ V_{CC}		Com'l		±275		±275	mA
				Mil				±350	

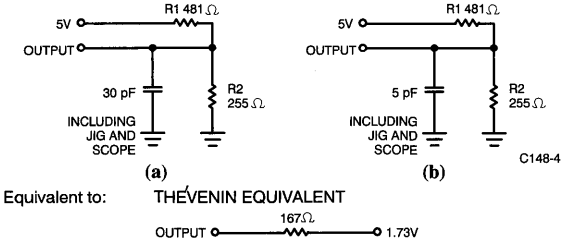
Capacitance[5]

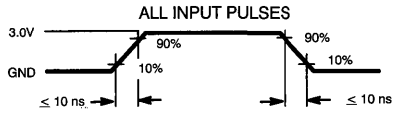
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
4. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[2]

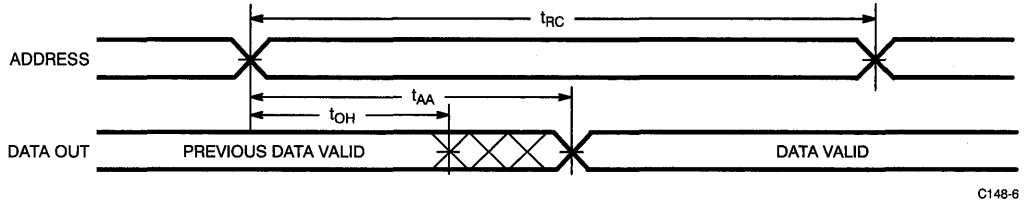
Parameter	Description		7C148-25 7C149-25 Min.	7C148-25 7C149-25 Max.	7C148-35 7C149-35 Min.	7C148-35 7C149-35 Max.	7C148-45 7C149-45 Min.	7C148-45 7C149-45 Max.	Unit
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1} t_{ACS2}	Chip Select LOW to Data Out Valid (7C148 only)			25[6]		35		45	ns
				30[7]		35		45	ns
t_{ACS}	Chip Select LOW to Data Out Valid (7C149 only)			15		15		20	ns
t_{LZ}[8]	Chip Select LOW to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[8]	Chip Select HIGH to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable to Output in High Z		0	8	0	8	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		20		30		40		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

Notes:

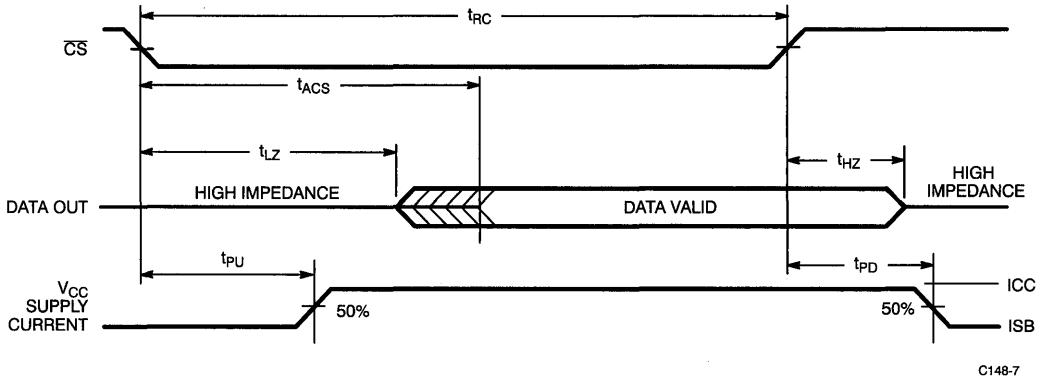
6. Chip deselected greater than 25 ns prior to selection.
7. Chip deselected less than 25 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady-state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to intiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

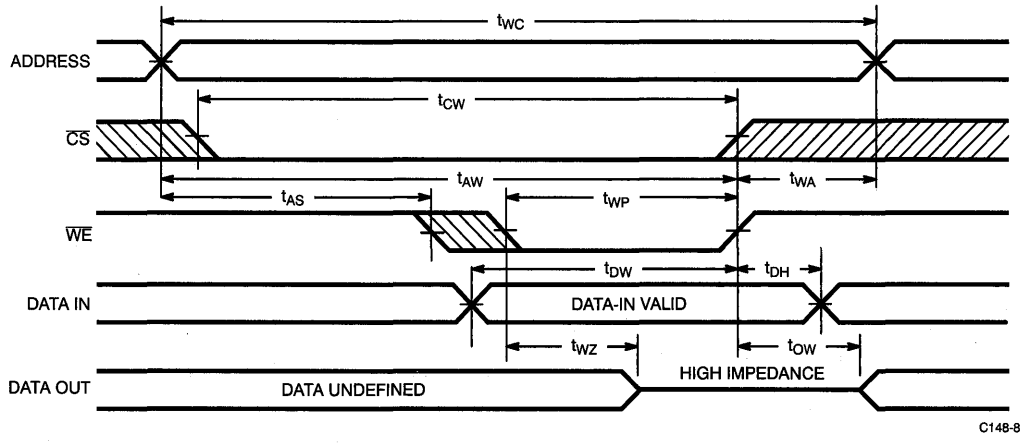
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



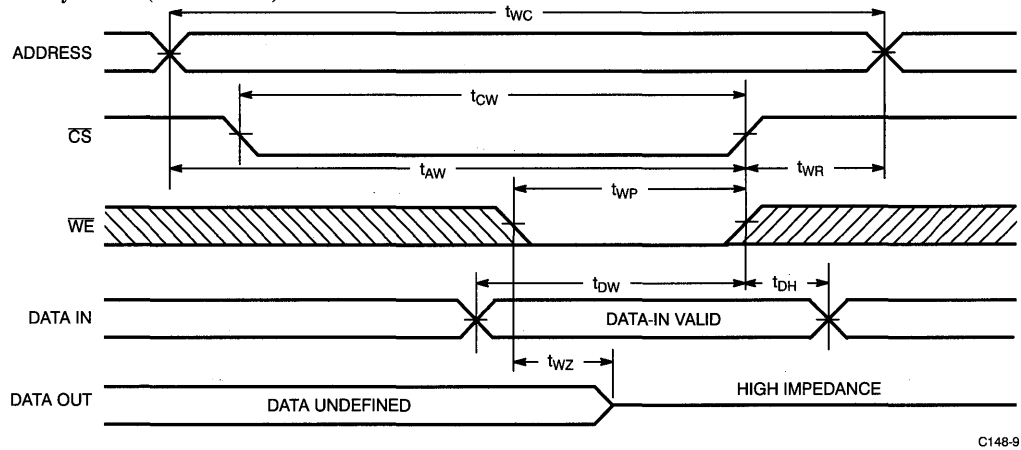
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

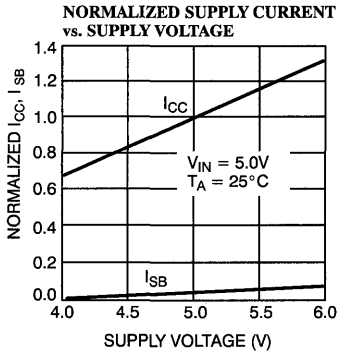
Switching Waveforms (continued)

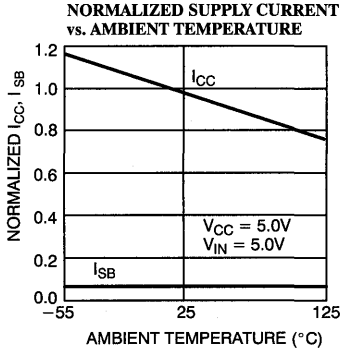
Write Cycle No. 2 ($\overline{CS}$ Controlled)[13]

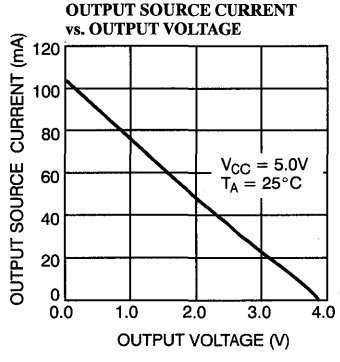


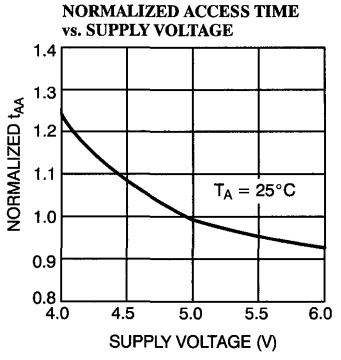
Notes:
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

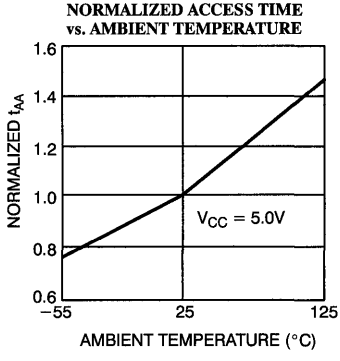
Typical DC and AC Characteristics

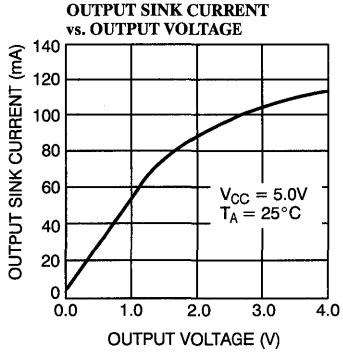






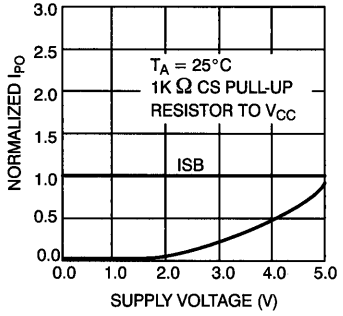




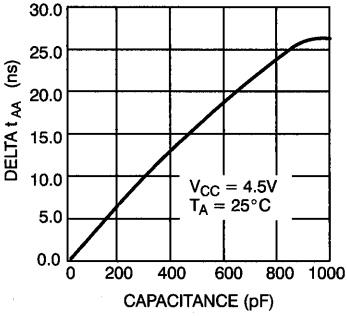


Typical DC and AC Characteristics

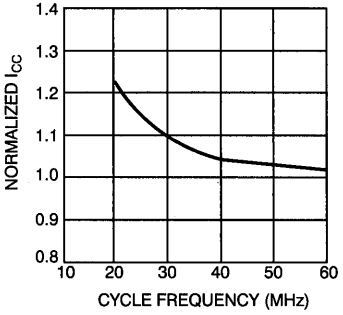
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. ACCESS TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C148–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C148–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
45	CY7C148–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–45DMB	D4	18-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C149–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C149–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–35LMB	L50	18-Pin Rectangular Leadless Chip Carrier	
45	CY7C149–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–45DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–45LMB	L50	18-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[14]	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[14]	7, 8, 9, 10, 11
t_{ACS2}[14]	7, 8, 9, 10, 11
t_{ACS}[15]	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{DW}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Notes:
14. 7C148 only.
15. 7C149 only.

Document #: 38−00031−C

CYPRESS SEMICONDUCTOR

CY7C150

1K x 4 Static R/W RAM

Features

- **Memory reset function**
- **1024 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 10 ns (commercial)**
  - **— 12 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 550 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance in both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C150 is a high-performance CMOS static RAM designed for use in cache memory, high-speed graphics, and data-acquisition applications. The CY7C150 has a memory reset feature that allows the entire memory to be reset in two memory cycles.

Separate I/O paths eliminates the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are tri-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS}$ = LOW) and taking the reset ($\overline{RS}$) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

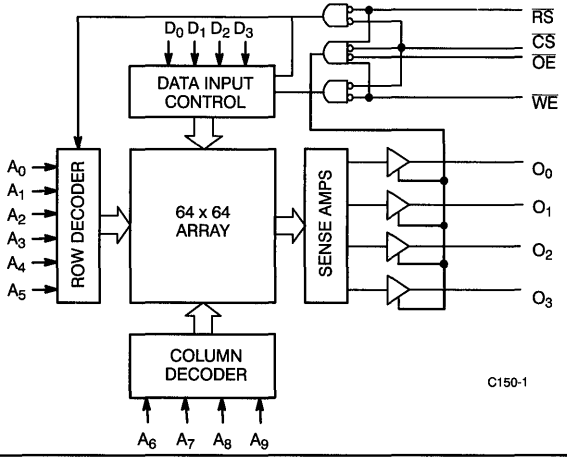
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0–D_3) is written into the memory location specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

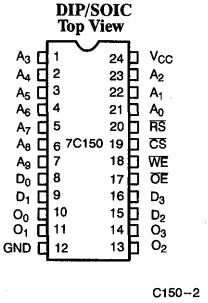
The output pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or reset ($\overline{RS}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C150–10	7C150–12	7C150–15	7C150–25	7C150–35
Maximum Access Time (ns)	Commercial	10	12	15	25	
	Military		12	15	25	35
Maximum Operating Current (mA)	Commercial	90	90	90	90	90
	Military		100	100	100	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

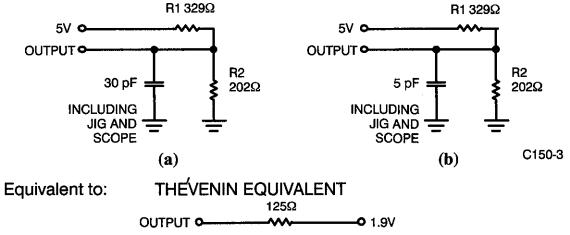
Electrical Characteristics Over the Operating Range[2]

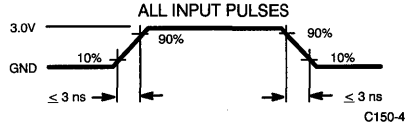
Parameter	Description	Test Conditions		7C150 Min.	7C150 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 0.4 mA		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 12 mA			0.4	V
V_{IH}	Input HIGH Level			2.0	V_{CC}	V
V_{IL}	Input LOW Level			− 3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Current (High Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90	mA
			Military		100	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 5]

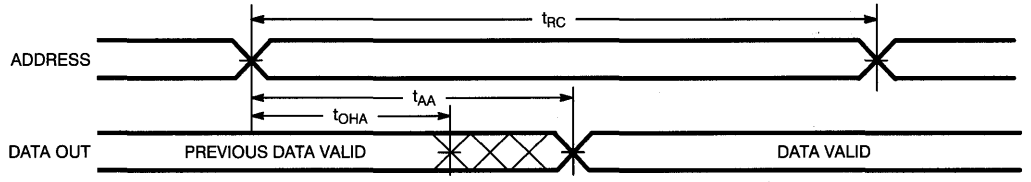
Parameter	Description	7C150–10		7C150–12		7C150–15		7C150–25		7C150–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	10		12		15		25		35		ns
t_{AA}	Address to Data Valid		10		12		15		25		35	ns
t_{OHA}	Output Hold from Address Change	2		2		2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		8		10		12		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		6		8		11		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		8		9		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	10		12		15		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	6		8		11		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		13		20		30		ns
t_{HA}	Address Hold from Write End	2		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		8		11		15		20		ns
t_{SD}	Data Set-Up to Write End	6		8		11		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		8		12		20		25	ns
RESET CYCLE												
t_{RRC}	Reset Cycle Time	20		24		30		50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		0		0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		0		0		ns
t_{PRS}	Reset Pulse Width	10		12		15		20		30		ns
t_{HCSR}	Chip Select Hold After End of Reset	0		0		0		0		0		ns
t_{HWER}	Write Enable Hold After End of Reset	8		12		15		30		40		ns
t_{HAR}	Address Hold After End of Reset	10		12		15		30		40		ns
t_{LZRS}	Reset HIGH to Output in Low Z[6]	0		0		0		0		0		ns
t_{HZRS}	Reset LOW to Output in High Z[6, 7]		6		8		12		20		25	ns

Notes:

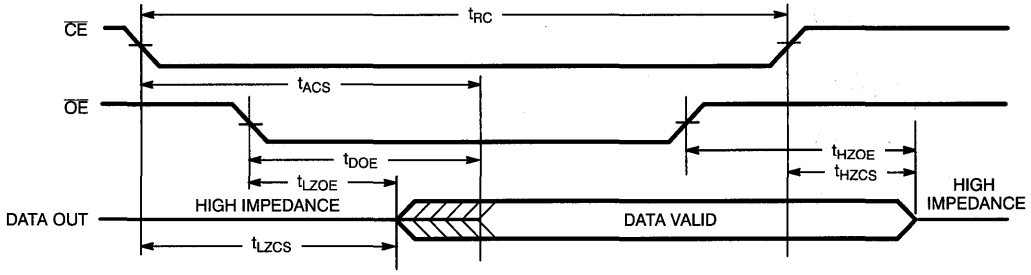
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCS}, t_{HZOE}, t_{HZR}, and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

Switching Waveforms

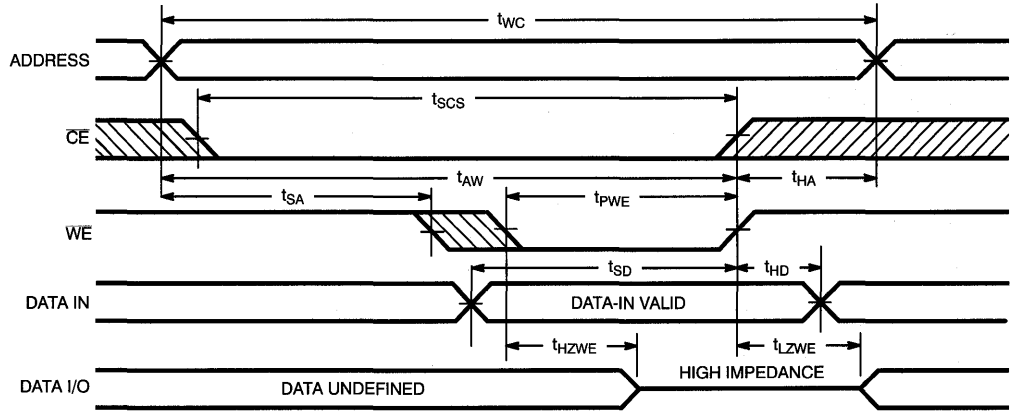
Read Cycle No. 1[9, 10]



Read Cycle No. 2[10, 11]



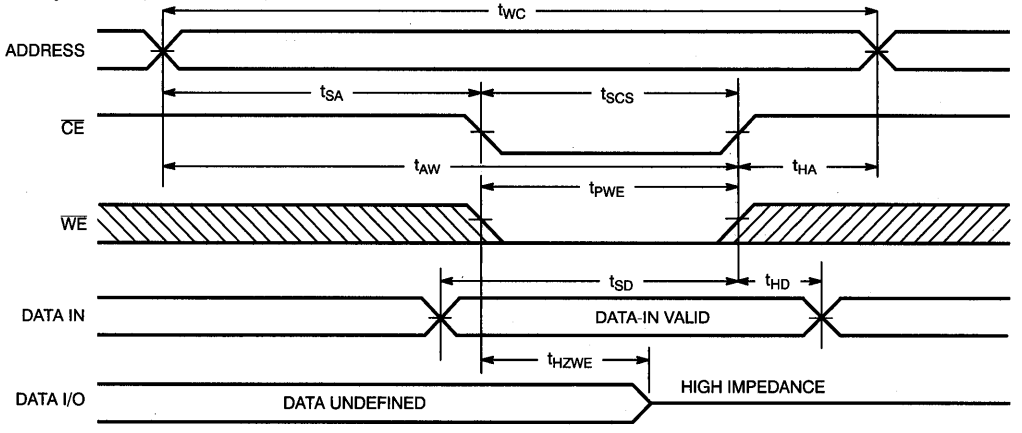
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



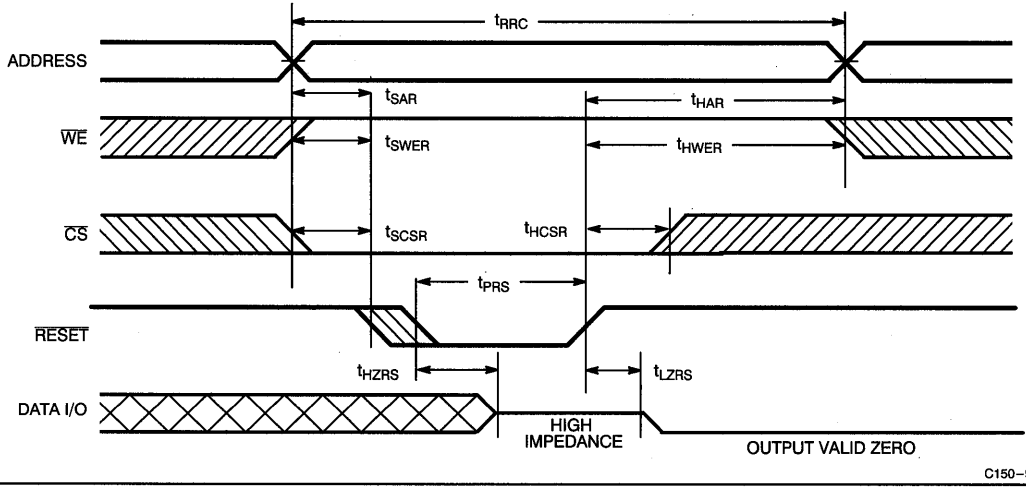
Notes:
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ and $\overline{OE}$ = V_{IL}.
11. Address prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[8, 12]



Reset Cycle[13]

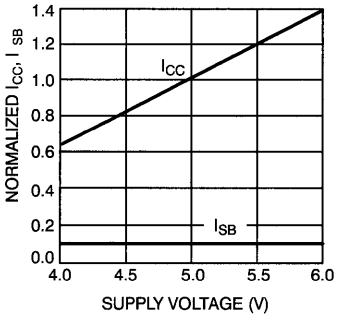


Notes:

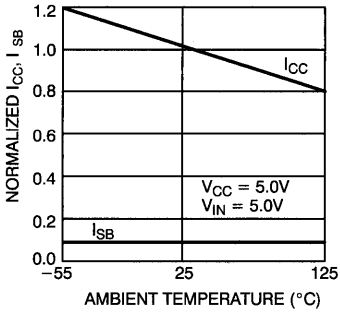
12. If $\overline{CS}$ goes HIGH with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
13. Reset cycle is defined by the overlap of $\overline{RS}$ and $\overline{CS}$ for the minimum reset pulse width.

Typical DC and AC Characteristics

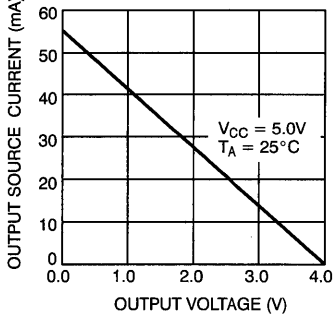
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



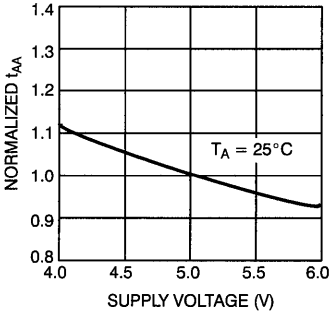
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



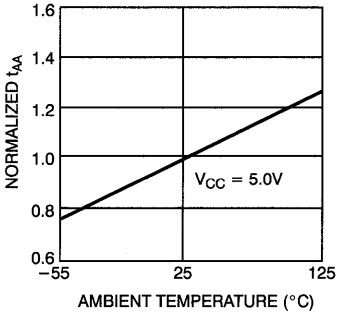
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



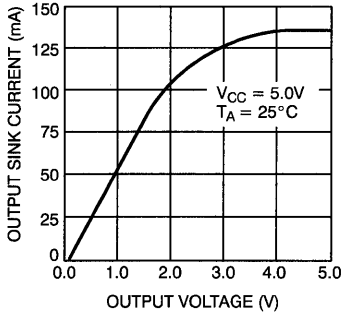
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



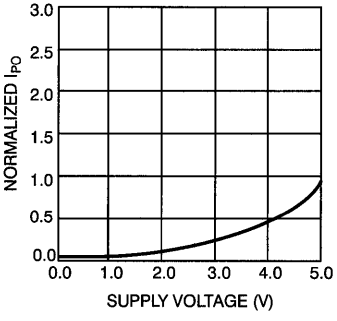
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



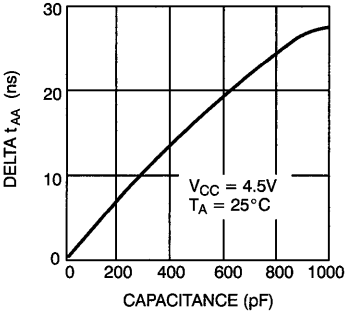
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



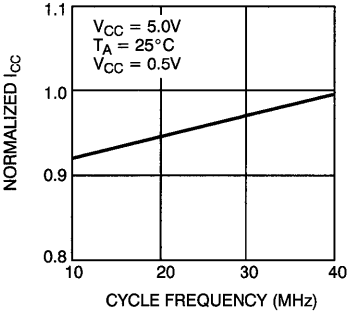
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

Inputs				Outputs	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{RS}$		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0-O_3	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C150–10PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–10SC	S13	24-Lead Molded SOIC	
12	CY7C150–12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–12SC	S13	24-Lead Molded SOIC	
	CY7C150–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C150–15PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–15SC	S13	24-Lead Molded SOIC	
	CY7C150–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C150–25PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–25SC	S13	24-Lead Molded SOIC	
	CY7C150–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C150–35DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
RESET CYCLE	
t_{RRC}	7, 8, 9, 10, 11
t_{SAR}	7, 8, 9, 10, 11
t_{SWER}	7, 8, 9, 10, 11
t_{SCSR}	7, 8, 9, 10, 11
t_{PRS}	7, 8, 9, 10, 11
t_{HCSR}	7, 8, 9, 10, 11
t_{HWER}	7, 8, 9, 10, 11
t_{HAR}	7, 8, 9, 10, 11

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CY7B161
CY7B162

16K x 4 Static RAM Separate I/O

Features

- **Ultra high speed**
  - **— 8 ns t_{AA}**
- **Low active power**
  - **— 700 mW**
- **Low standby power**
  - **— 250 mW**
- **Transparent write (7B161)**
- **BiCMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

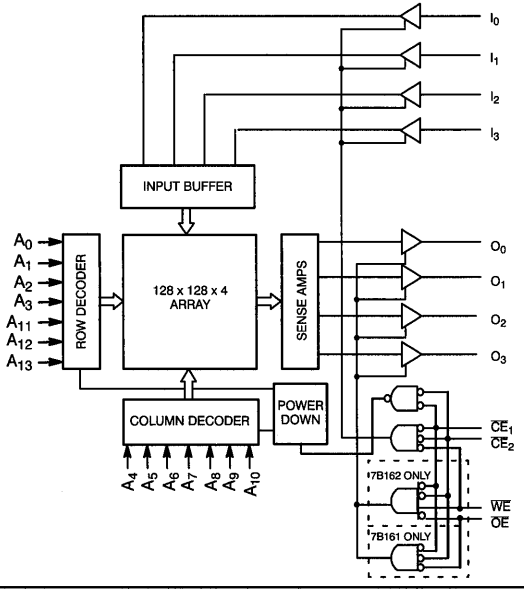
The CY7B161 and CY7B162 are high-performance BiCMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have a $\overline{CE}$ power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are all LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and $\overline{OE}$ LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

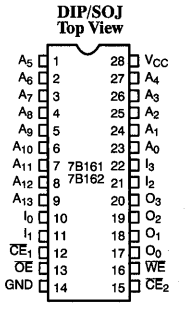
The output pins remain in high-impedance state when write enable ($\overline{WE}$) is LOW (7B162 only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) is HIGH, or $\overline{OE}$ is HIGH.

Logic Block Diagram

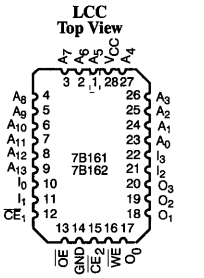


B161-1

Pin Configurations



B161-2



B161-3

Selection Guide

		7B161–8 7B162–8	7B161–10 7B162–10	7B161–12 7B162–12	7B161–15 7B162–15
Maximum Access Time (ns)		8	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	120	
	Military		145	140	135
Maximum Standby Current (mA)	Commercial	50	40	40	
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Latch-Up Current ..... > 200 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}	
		−8	−10, −12
Commercial	0°C to +70°C	5V ± 5%	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%	

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7B161−8 7B162−8 Min.	7B161−8 7B162−8 Max.	7B161−10 7B162−10 Min.	7B161−10 7B162−10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{max}.		Com'l		140		130	mA
				Mil				145	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3 V, I_{OUT} = 0 mA, Other Inputs = <0.8 or >3V, V_{CC}=Max.		Com'l		50		40	mA
				Mil				60	

Shaded area contains preliminary information.

Parameter	Description	Test Conditions			7B161−12 7B162−12 Min.	7B161−12 7B162−12 Max.	7B161−15 7B162−15 Min.	7B161−15 7B162−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{max}.		Com'l		120			mA
				Mil		140		135	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT}=0mA, Other Inputs = <0.8 or >3V, V_{CC}=Max.		Com'l		40			mA
				Mil		55		50	

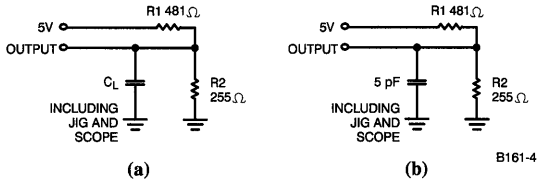
Capacitance[4]

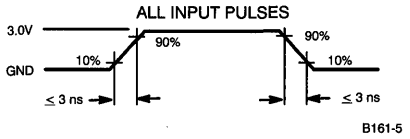
Parameter	Description	Test Conditions	Max.[5]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

Notes:

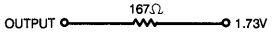
1. V_{IL} (min.) = − 3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CerDIP (D22), which has maximums of C_{IN} = 9.5 pF and C_{OUT} = 9 pF.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6, 7]

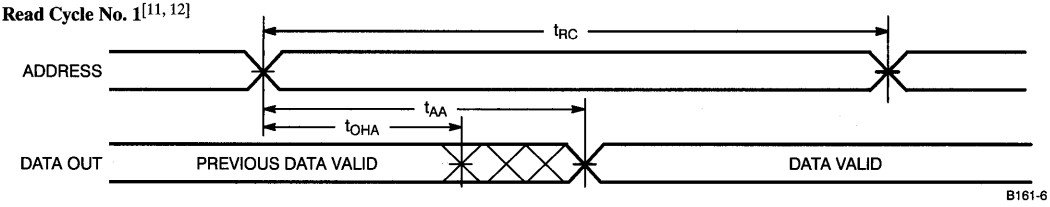
Parameter	Description	7B161–8 7B162–8		7B161–10 7B162–10		7B161–12 7B162–12		7B161–15 7B162–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Output Hold from Address Change	2.5		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4.2		5		6		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	1.5		2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	2		2		2		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		4		5		6		7	ns
WRITE CYCLE[10]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		8		10		ns
t_{AW}	Address Set-Up to Write End	7		8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6.5		8		8		10		ns
t_{SD}	Data Set-Up to Write End	4		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8] (7B162)	2		2		2		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9] (7B162)		4		5		6		7	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7B161)		8		10		12		15	ns
t_{ADV}	Data Valid to Output Valid (7B161)		8		10		12		15	ns

Notes:

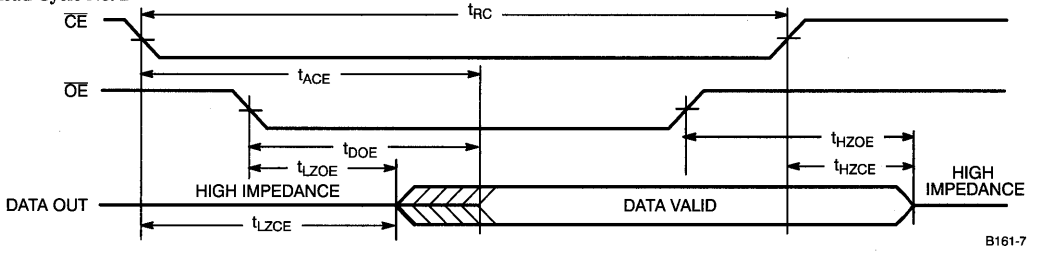
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and C_L = 20 pF.
7. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms section.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. This parameter is guaranteed and not 100% tested.
9. t_{HZCE}, t_{HZOE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage. This parameter is guaranteed and not 100% tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[7]

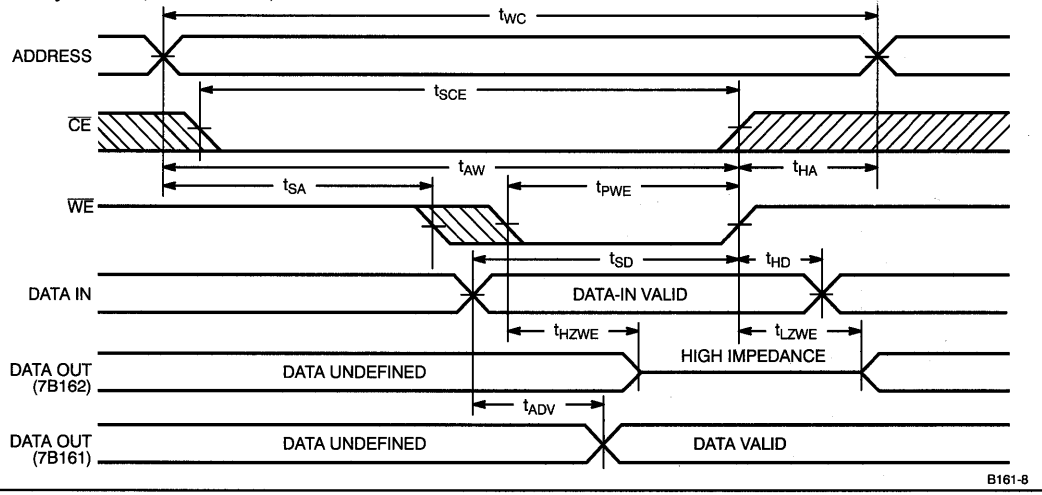
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



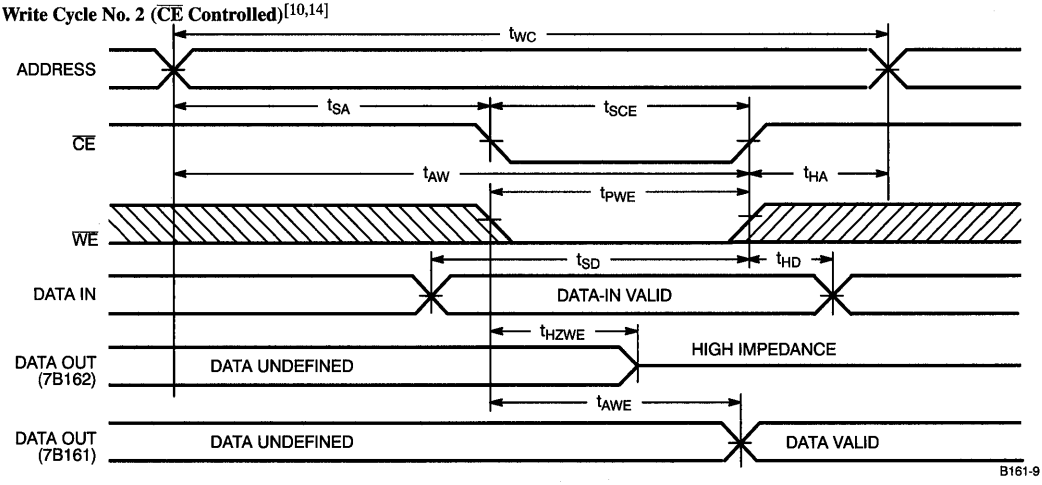
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2 \leq V_{IL}$. $\overline{OE} \leq V_{IL}$ also.
13. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.

Switching Waveforms[7] (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10,14]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7B162 only).

7B161 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Output	Input	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	L	Data In	Data In	Write
L	L	L	H	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

7B162 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Output	Input	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	X	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B161–8VC	V21	28-Lead Molded SOJ	
10	CY7B161–10DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B161–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B161–10VC	V21	28-Lead Molded SOJ	
	CY7B161–10DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B161–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B161–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B161–12VC	V21	28-Lead Molded SOJ	
	CY7B161–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B161–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B162–8VC	V21	28-Lead Molded SOJ	
10	CY7B162–10DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B162–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B162–10VC	V21	28-Lead Molded SOJ	
	CY7B162–10DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B162–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B162–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B162–12VC	V21	28-Lead Molded SOJ	
	CY7B162–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B162–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. 7B161 only.

Document #: 38-A-00014-E

CY7C161
CY7C162

16K x 4 Static RAM Separate I/O

Features

- **High speed**
  - **15-ns**
- **Transparent write (7C161)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **633 mW**
- **Low standby power**
  - **220 mW**
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

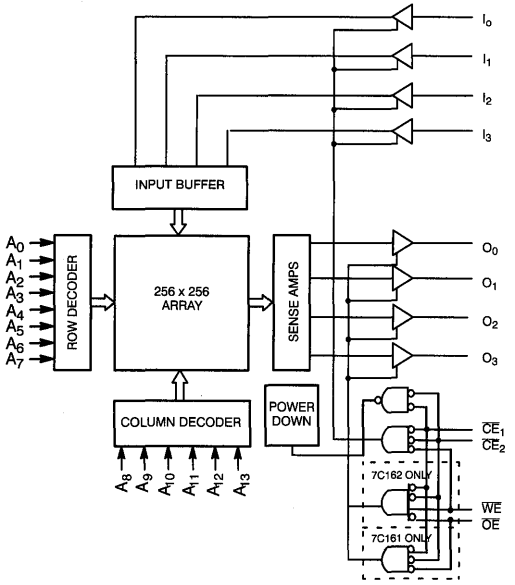
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

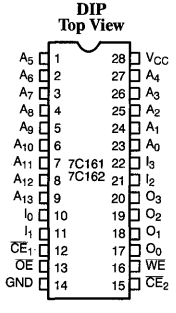
The output pins stay in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C162 only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide[1]

	7C161–12 7C162–12	7C161–15 7C162–15	7C161–20 7C162–20	7C161–25 7C162–25	7C161–35 7C162–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded areas indicate advanced information.

Note:
1. For military specifications, see the CY7C161A/CY7C162A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... − 0.5V to +7.0V

DC Input Voltage[2] ..... − 0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C161−12 7C162−12		7C161−15 7C162−15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		− 0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		− 350		− 350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		115	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} Min. Duty Cycle = 100%		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20	mA

Shaded areas indicate advanced information.

Electrical Characteristics Over the Operating Range (continued)

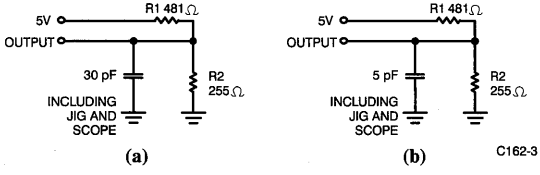
Parameter	Description	Test Conditions	7C161–20 7C162–20		7C161–25,35 7C162–25,35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		− 350		− 350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		80		70	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} Min. Duty Cycle = 100%		40		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20	mA

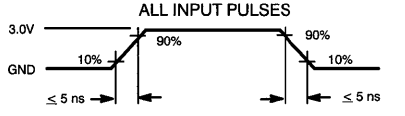
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

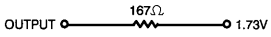
Notes:
2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	7C161–12 7C162–12		7C161–15 7C162–15		7C161–20 7C162–20		7C161–25 7C162–25		7C161–35 7C162–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		7		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	8		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		15		20		ns
t_{SD}	Data Set-Up to Write End	6		10		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7] (7C162)	3		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8] (7C162)		6		7		7		7		10	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161)		12		15		20		25		30	ns
t_{ADV}	Data Valid to Output Valid (7C161)		12		15		20		20		30	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns

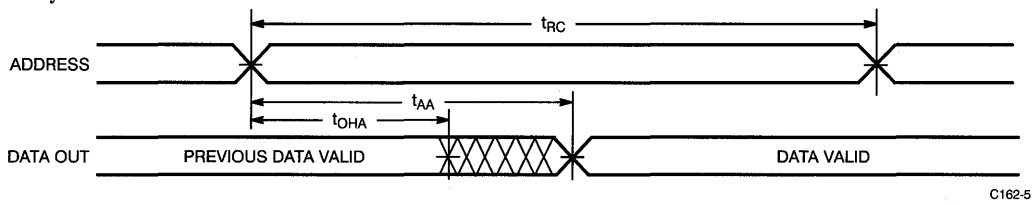
Shaded areas indicate advanced information.

Notes:

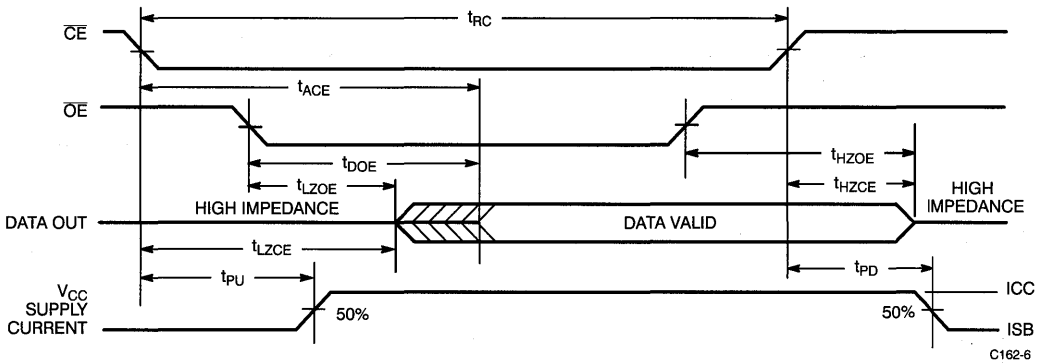
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[8]

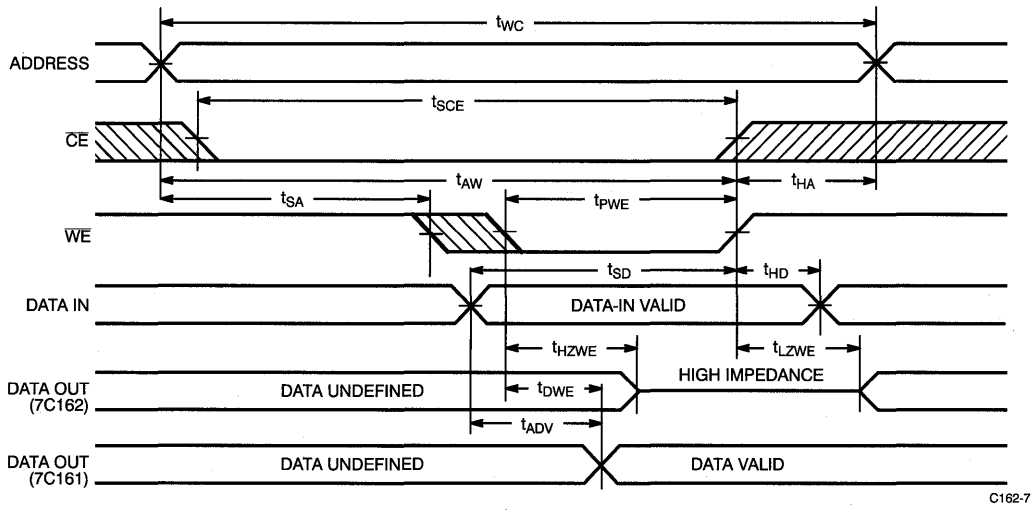
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



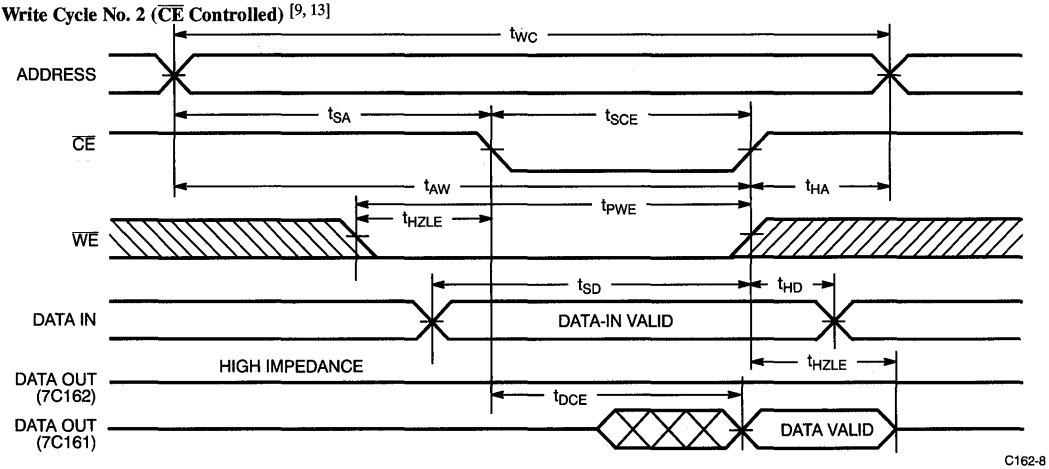
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.

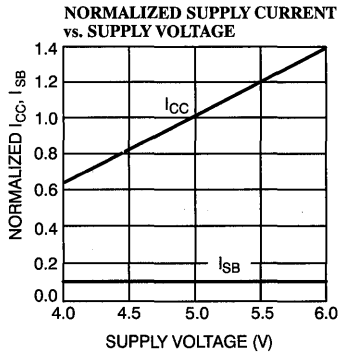
Switching Waveforms[8] (continued)

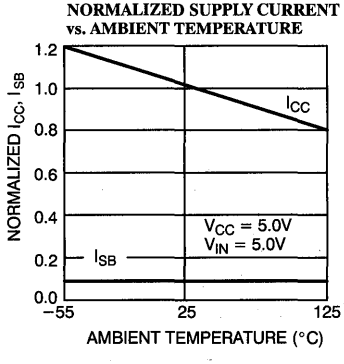
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]

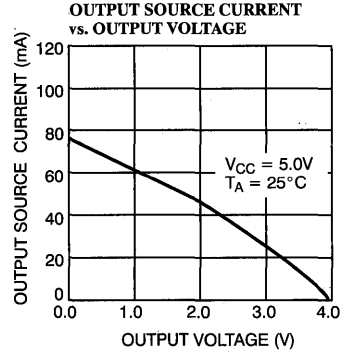


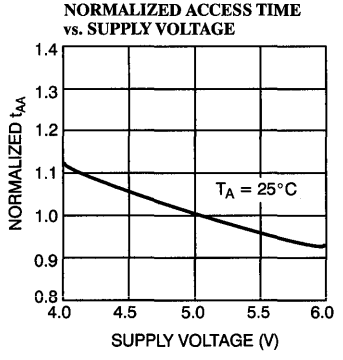
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162 only).

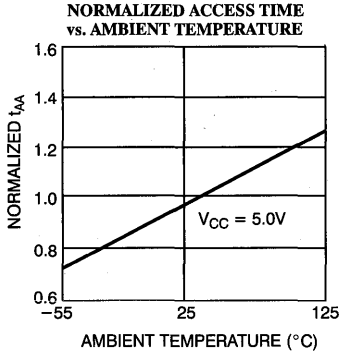
Typical DC and AC Characteristics

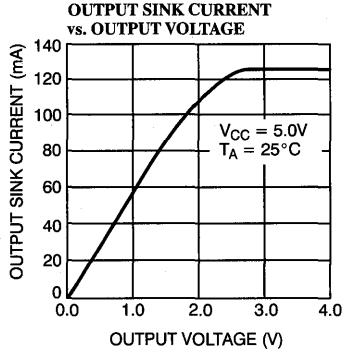






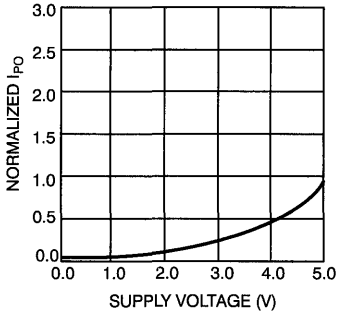




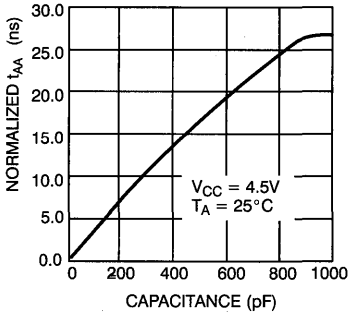


Typical DC and AC Characteristics (continued)

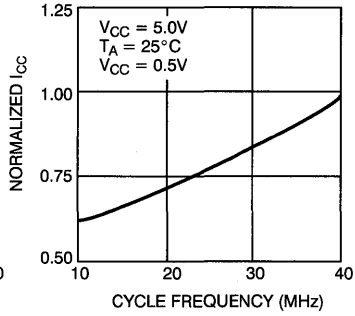
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Nsme	Package Type	Operating Range
12	CY7C161-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-12VC	V21	28-Lead Molded SOJ	
15	CY7C161-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-15VC	V21	28-Lead Molded SOJ	
20	CY7C161-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-20VC	V21	28-Lead Molded SOJ	
25	CY7C161-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-25VC	V21	28-Lead Molded SOJ	
35	CY7C161-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-35VC	V21	28-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C162-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-12VC	V21	28-Lead Molded SOJ	
15	CY7C162-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-15VC	V21	28-Lead Molded SOJ	
20	CY7C162-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-20VC	V21	28-Lead Molded SOJ	
25	CY7C162-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-25VC	V21	28-Lead Molded SOJ	
35	CY7C162-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-35VC	V21	28-Lead Molded SOJ	

Shaded areas indicate advanced information.

Document #: 38-00029-H

CY7C161A
CY7C162A

16K x 4 Static RAM Separate I/O

Features

- **High speed**
  - **— 20 ns t_{AA}**
- **CMOS for optimum speed/power**
- **Transparent write (7C161A)**
- **Low active power**
  - **— 550 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organizes as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

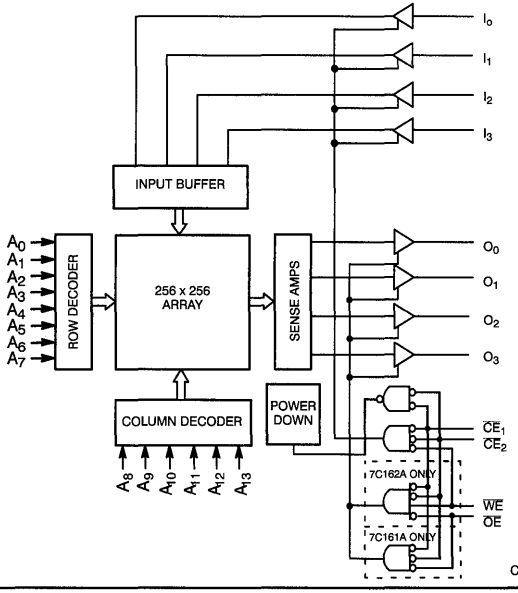
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

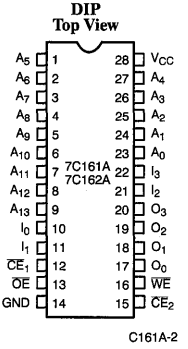
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162A only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

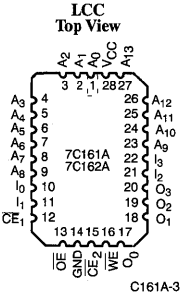
A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations





Selection Guide[1]

		7C161A–15 7C162A–15	7C161A–20 7C162A–20	7C161A–25 7C162A–25	7C161A–35 7C162A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains advanced information.

Note:
1. For commercial specifications, see the CY7C161/CY7C162 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to +7.0V

DC Input Voltage[2] ..... – 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C161A–15 7C162A–15 Min.	7C161A–15 7C162A–15 Max.	7C161A–20 7C162A–20 Min.	7C161A–20 7C162A–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 10	+10	– 10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			– 350		– 350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Military		160		100	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

Shaded area contains advanced information.

Notes:

2. Minimum voltage is equal to –3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[4] (continued)

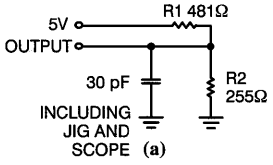
Parameter	Description	Test Conditions		7C161A–25 7C162A–25 Min.	7C161A–25 7C162A–25 Max.	7C161A–35 7C162A–35 Min.	7C161A–35 7C162A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		100		100	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Military		20		20	mA

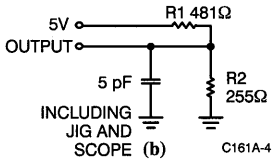
Capacitance[6]

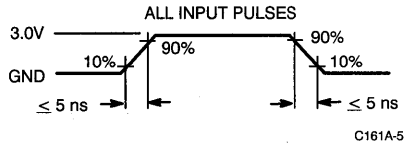
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

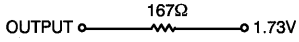
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 7, 8]

Parameter	Description	7C161A–15 7C162A–15		7C161A–20 7C162A–20		7C161A–25 7C162A–25		7C161A–35 7C162A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9] (7C162A)	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10] (7C162A)		7		7		7		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C161A)		15		20		25		30	ns
t_{ADV}	Data Valid to Output Valid (7C161A)		15		20		20		30	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C161A)		15		20		25		35	ns

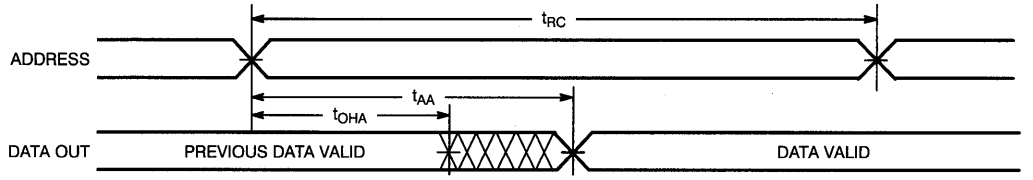
Shaded area contains advanced information.

Notes:

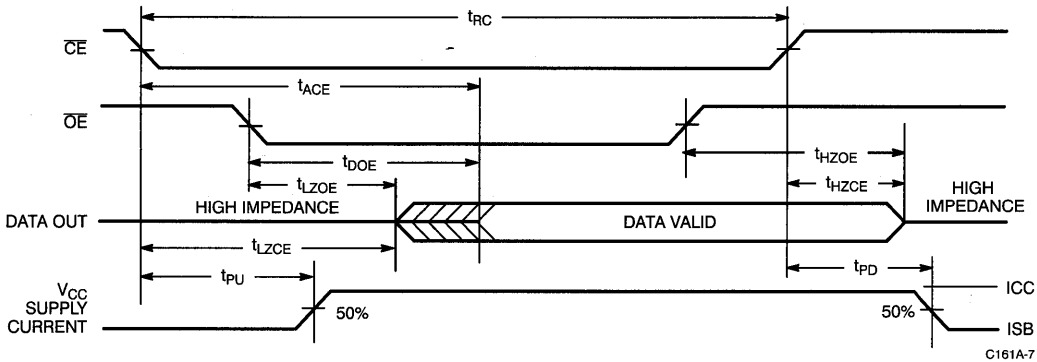
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
9. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[8]

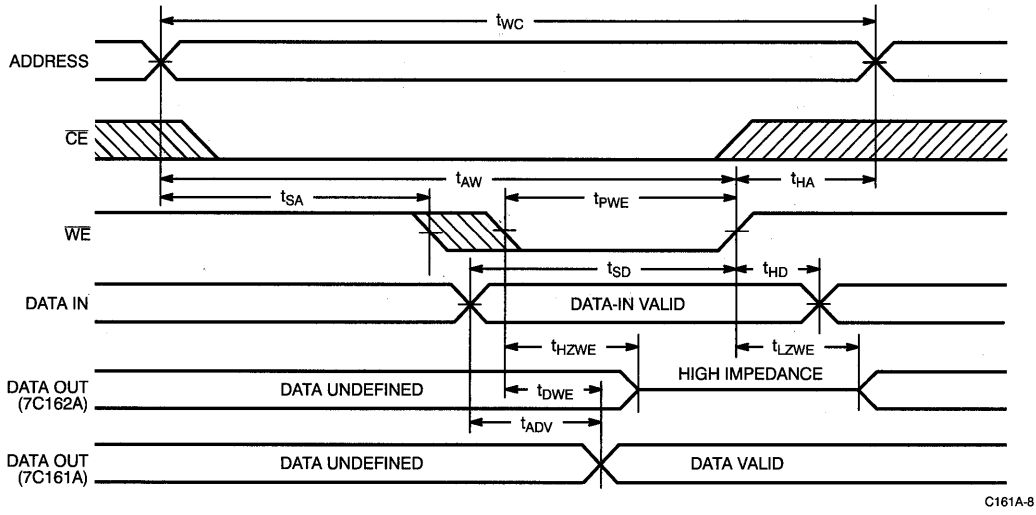
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



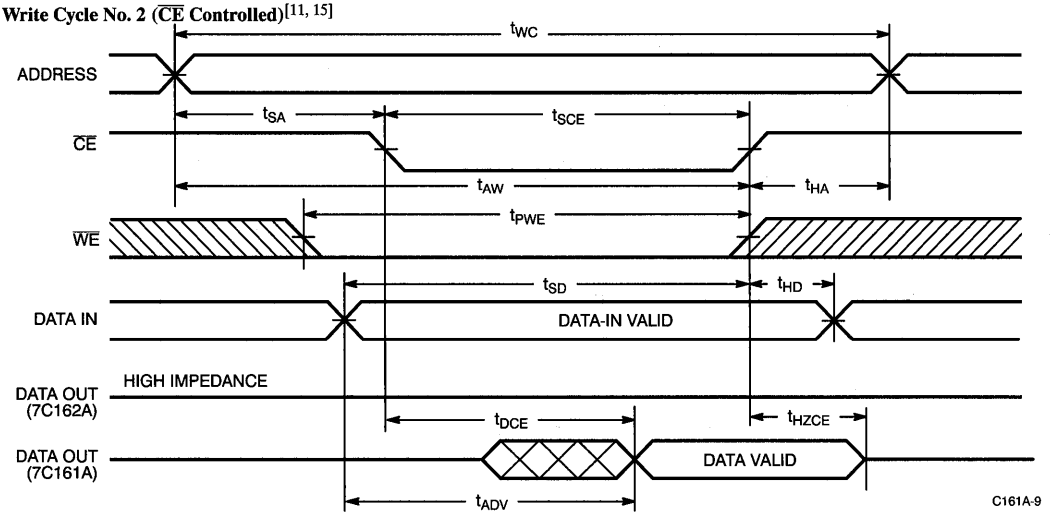
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
14. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.

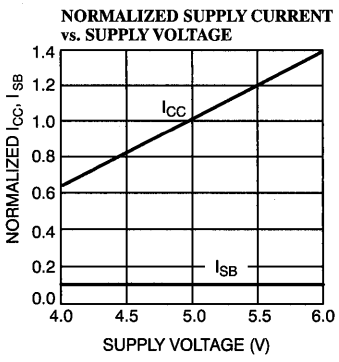
Switching Waveforms (continued)

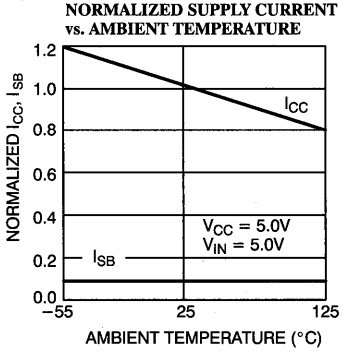
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15]

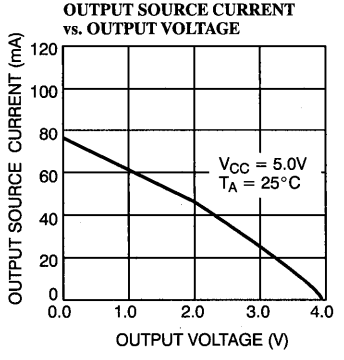


Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162A only).

Typical DC and AC Characteristics

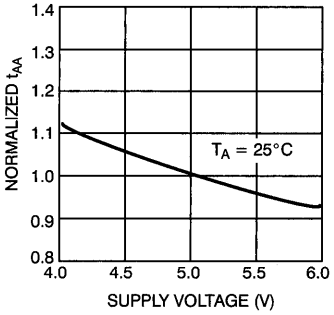




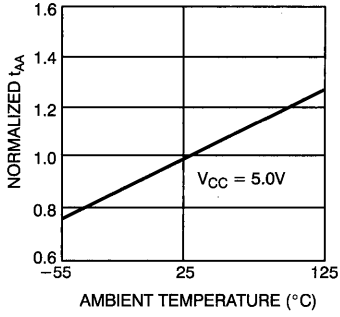


Typical DC and AC Characteristics (continued)

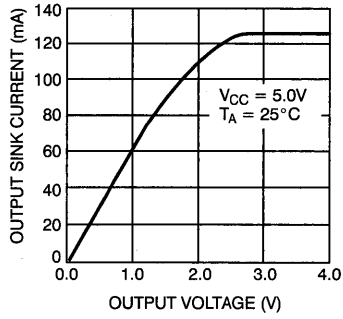
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



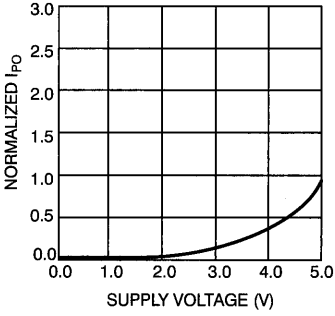
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



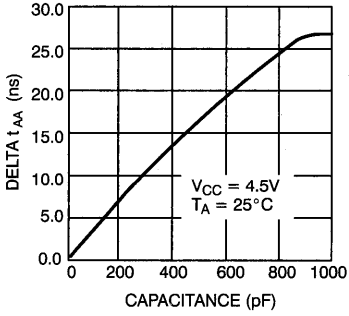
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



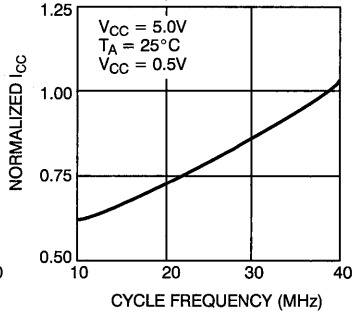
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C161A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C161A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C161A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C161A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C161A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C161A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C161A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C161A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C162A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C162A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C162A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C162A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}	7, 8, 9, 10, 11

Notes:
16. 7C161A only.

Document #: 38–00116–B

CYPRESS SEMICONDUCTOR

CY7B164
CY7B166

16K x 4 Static R/W RAM

Features

- **Ultra high speed**
  - **— t_{AA} = 8 ns**
- **Low active power**
  - **— 700 mW**
- **Low standby power**
  - **— 250 mW**
- **BiCMOS for optimum speed/power**
- **Output enable ($\overline{OE}$) feature (7B166)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

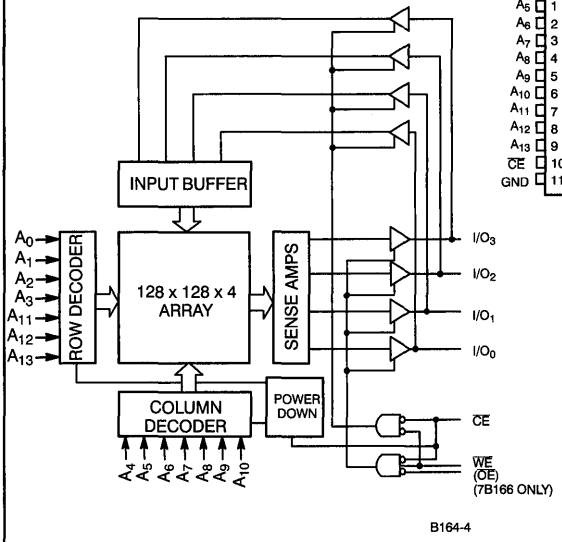
The CY7B164 and CY7B166 are high-performance BiCMOS static RAMs organized as 16,384 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7B166 has an active LOW output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7B166) while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

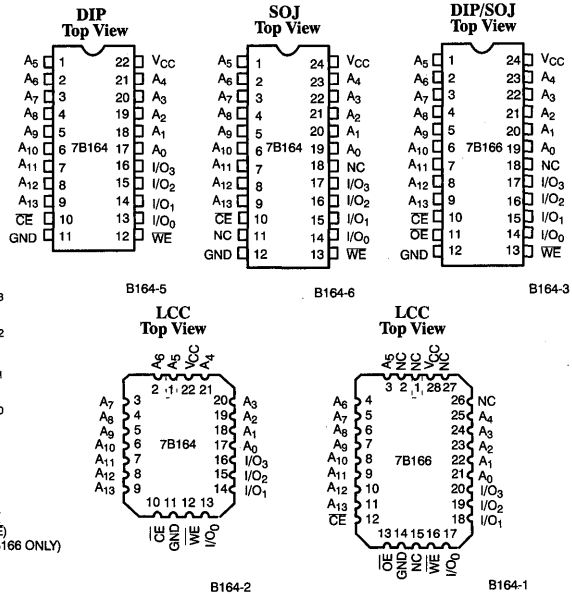
The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW (or output enable ($\overline{OE}$) is HIGH for 7B166).

Logic Block Diagram



B164-4

Pin Configurations



Selection Guide

		7B164–8 7B166–8	7B164–10 7B166–10	7B164–12 7B166–12	7B164–15 7B166–15
Maximum Access Time (ns)		8	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	120	
	Military		145	140	135
Maximum Operating Current (mA)	Commercial	50	40	40	
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to + 150°C

Ambient Temperature with Power Applied ..... − 55°C to + 125°C

Supply Voltage to Ground Potential ..... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to + 7.0V

DC Input Voltage[1] ..... − 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	
Commercial	0°C to + 70°C	−8	5V ±5%
		−10, −12	5V ±10%
Military[2]	− 55°C to + 125°C	5V ±10%	

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B164−8 7B166−8 Min.	7B164−8 7B166−8 Max.	7B164−10 7B166−10 Min.	7B164−10 7B166−10 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil					
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		140		130	mA
				Mil				145	
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT} = 0 mA Other Inputs ≤ 0.8V or >3V, V_{CC} = Max.		Com'l		50		40	mA
				Mil				60	

Parameters	Description	Test Conditions			7B164−12 7B166−12 Min.	7B164−12 7B166−12 Max.	7B164−15 7B166−15 Min.	7B164−15 7B166−15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil					
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		120			mA
				Mil		140		135	
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT} = 0 mA Other Inputs ≤ 0.8V or >3V, V_{CC} = Max.		Com'l		40			mA
				Mil		55		50	

Shaded area contains preliminary information.

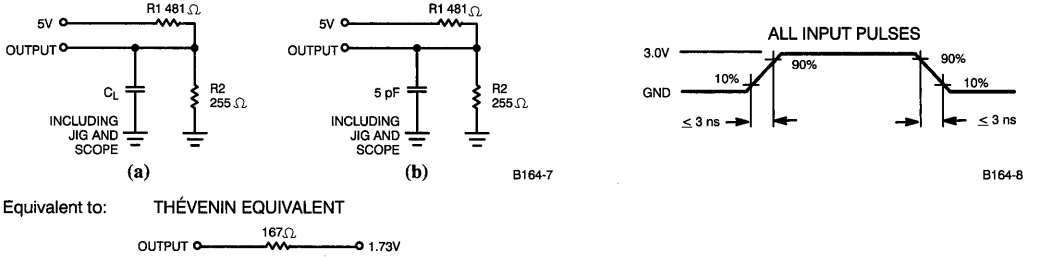
Notes:

1. V_{IL} (min.) = −3.0V for pulse width <20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3, 6]

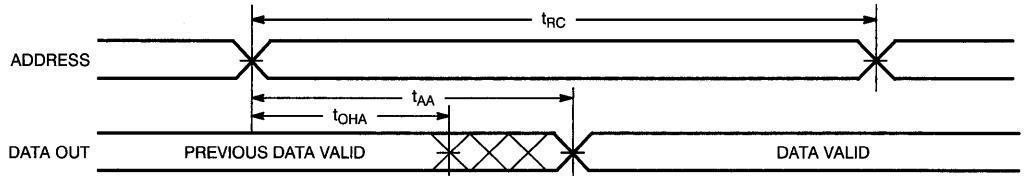
Parameters	Description		7B164–8 7B166–8 Min.	7B164–8 7B166–8 Max.	7B164–10 7B166–10 Min.	7B164–10 7B166–10 Max.	7B164–12 7B166–12 Min.	7B164–12 7B166–12 Max.	7B164–15 7B166–15 Min.	7B164–15 7B166–15 Max.	Units
READ CYCLE											
t_{RC}	Read Cycle Time		8		10		12		15		ns
t_{AA}	Address to Data Valid			8		10		12		15	ns
t_{OHA}	Output Hold from Address Change		2.5		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7B166		4.2		5		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7B166	1.5		2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]	7B166		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		2		2		2		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			4		5		6		7	ns
WRITE CYCLE[9]											
t_{WC}	Write Cycle Time		8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		7		8		8		10		ns
t_{AW}	Address Set-Up to Write End		7		8		8		10		ns
t_{HA}	Address Hold from Write End		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		6.5		8		8		10		ns
t_{SD}	Data Set-Up to Write End		4		5		6		7		ns
t_{HD}	Data Hold from Write End		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		2		2		2		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]			4	0	5	0	6	0	7	ns

Notes:

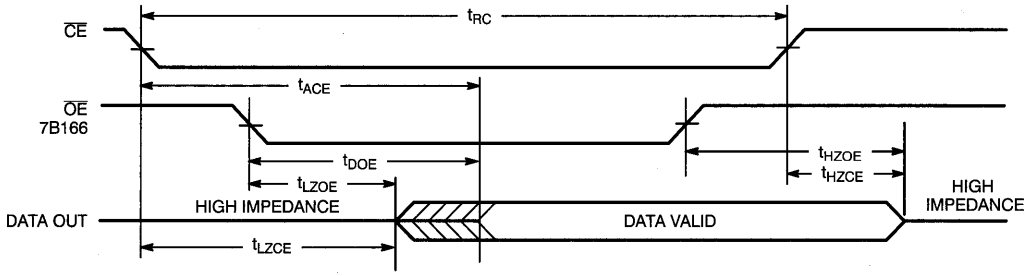
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except cerDIP (D10, D14), which has maximums of C_{IN} = 9.5 pF, C_{OUT} = 8 pF.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
7. t_{HZCE}, t_{HZWE}, and t_{HZOE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±200 mV from steady state voltage. This parameter is guaranteed and not 100% tested.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

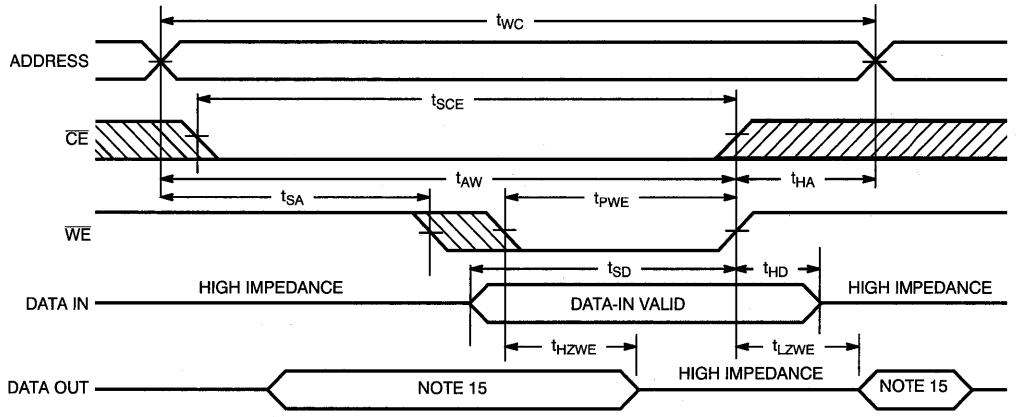
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



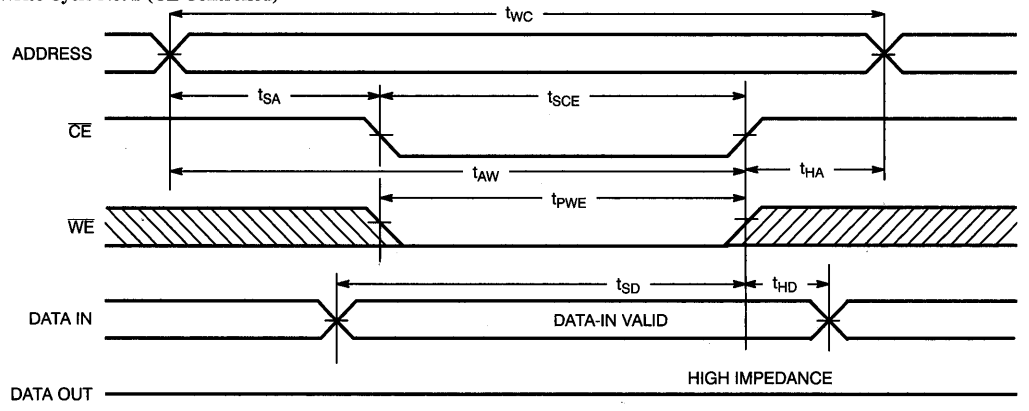
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13, 14]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7B166: $\overline{OE}$ = V_{IL} also).
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. 7B166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period the I/O pins are in the output state, and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13, 14, 16]



Note:
16. If the $\overline{CE}$ LOW transition occurs after the WE transition, the output remains in a high-impedance state.

7B164 Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7B166 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B164–8VC	V13	32-Lead (400-Mil) Molded SOJ	Commercial
10	CY7B164–10DC	D10	22-Lead (300-Mil) CerDIP	Commercial
	CY7B164–10PC	P9	22-Lead (300-Mil) Molded DIP	
	CY7B164–10VC	V13	32-Lead (400-Mil) Molded SOJ	
	CY7B164–10DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–10LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
12	CY7B164–12DC	D10	22-Lead (300-Mil) CerDIP	Commercial
	CY7B164–12PC	P9	22-Lead (300-Mil) Molded DIP	
	CY7B164–12VC	V13	32-Lead (400-Mil) Molded SOJ	
	CY7B164–12DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–12LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
15	CY7B164–15DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B166–8VC	V13	24-Lead Molded SOJ	Commercial
10	CY7B166–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B166–10PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B166–10VC	V13	24-Lead Molded SOJ	
	CY7B166–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B166–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B166–12PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B166–12VC	V13	24-Lead Molded SOJ	
	CY7B166–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B166–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

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Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[17]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
17. 7B166 only.

CY7C164
CY7C166

CYPRESS SEMICONDUCTOR

16K x 4 Static RAM

Features

- **High speed**
  - **— 15 ns**
- **Output enable ($\overline{OE}$) feature (7C166)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 633 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

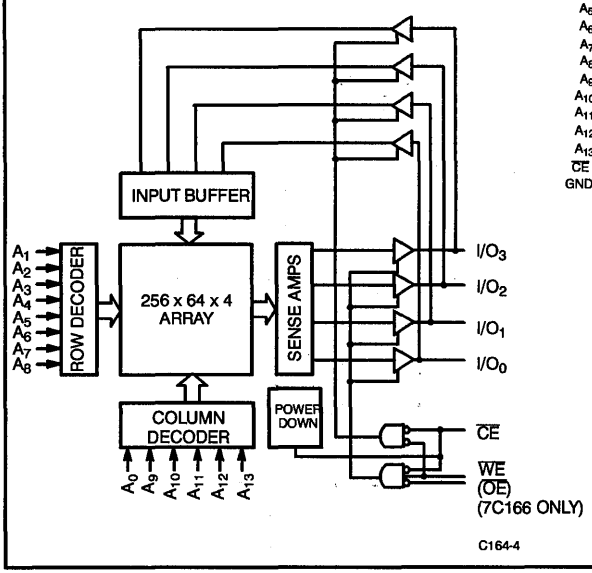
The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166 has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when chip enable ($\overline{CE}$) is HIGH (or output enable ($\overline{OE}$) is HIGH for 7C166). A die coat is used to insure alpha immunity.

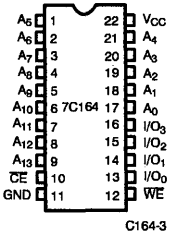
Logic Block Diagram



C164-4

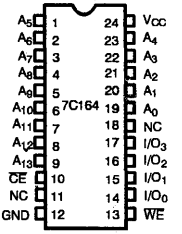
Pin Configurations

DIP
Top View



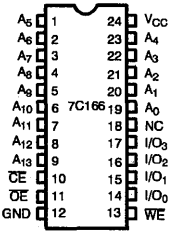
C164-3

SOJ
Top View



C164-2

DIP/SOJ
Top View



C164-1

Selection Guide[1]

	7C164–12 7C166–12	7C164–15 7C166–15	7C164–20 7C166–20	7C164–25 7C166–25	7C164–35 7C166–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded area contains advanced information.

Note:
1. For military specifications, see the CY7C164A/CY7C166A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to +7.0V

DC Input Voltage[2] ..... – 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C164–12 7C166–12		7C164–15 7C166–15		7C164–20 7C166–20		7C164–25, 35 7C166–25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		–0.5	0.8	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–350		–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		115		80		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%		40		40		40		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V		20		20		20		20	mA

Shaded area contains advanced information.

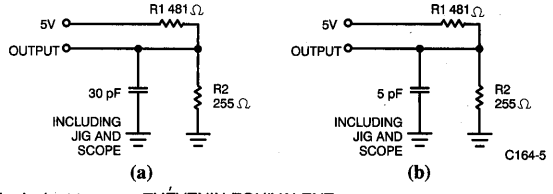
Capacitance[5]

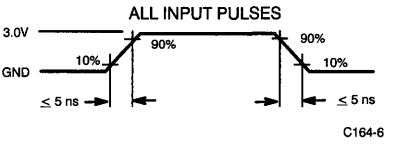
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. Minimum voltage is equal to –3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C164–12 7C166–12 Min.	7C164–12 7C166–12 Max.	7C164–15 7C166–15 Min.	7C164–15 7C166–15 Max.	7C164–20 7C166–20 Min.	7C164–20 7C166–20 Max.	7C164–25 7C166–25 Min.	7C164–25 7C166–25 Max.	7C164–35 7C166–35 Min.	7C164–35 7C166–35 Max.	Unit
READ CYCLE													
t_{RC}	Read Cycle Time		12		15		20		25		35		ns
t_{AA}	Address to Data Valid			12		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change		3		3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C166		6		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7C166	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	7C166		7		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]		3		3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			7		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			12		15		20		20		20	ns
WRITE CYCLE[9]													
t_{WC}	Write Cycle Time		12		15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		8		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End		9		12		15		20		25		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		8		12		15		15		20		ns
t_{SD}	Data Set-Up to Write End		6		10		10		10		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		3		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]			6		7		7		7		10	ns

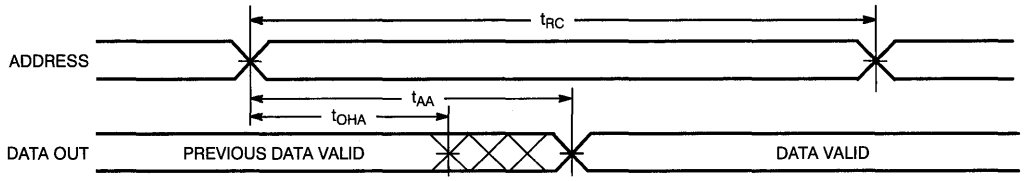
Shaded area contains advanced information.

Notes:

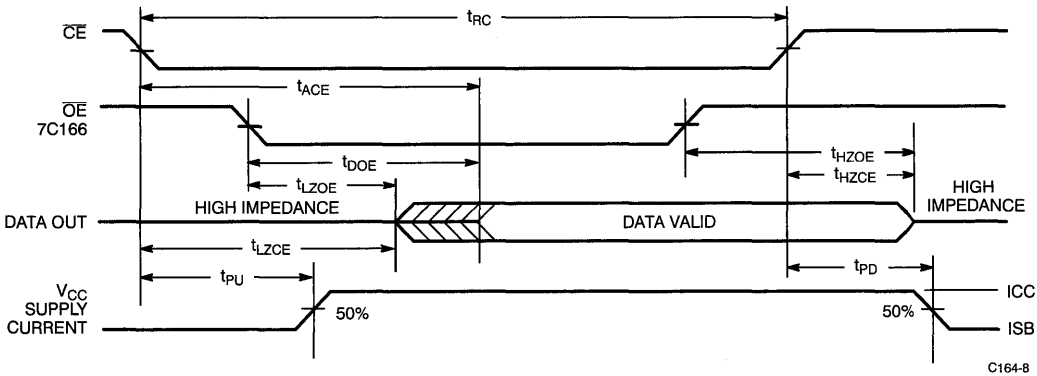
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

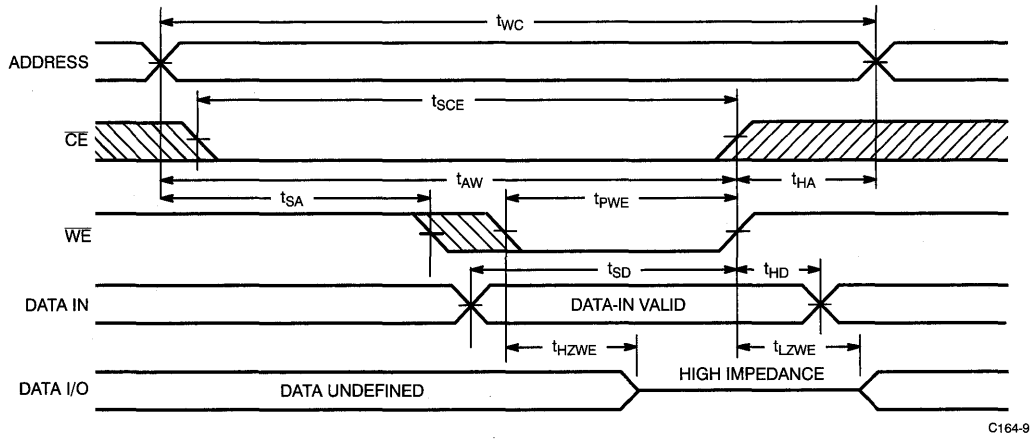
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



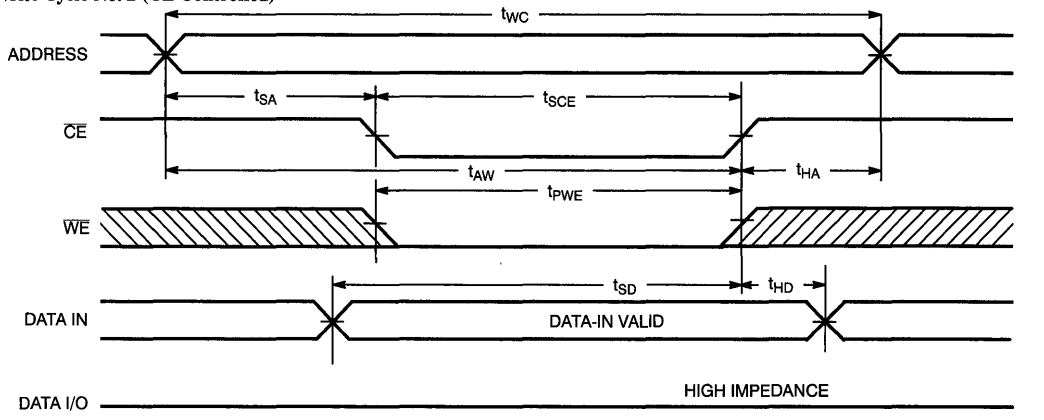
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7C166: $\overline{OE}$ = V_{IL} also).
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. 7C166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

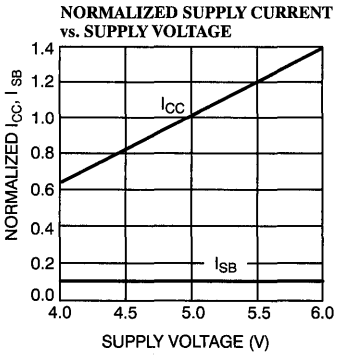
Switching Waveforms (continued)

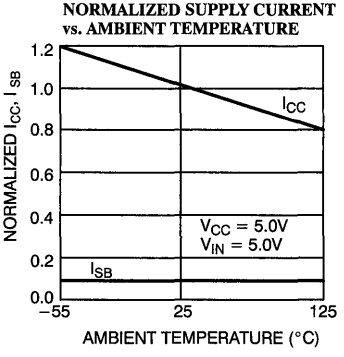
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9,13,14]

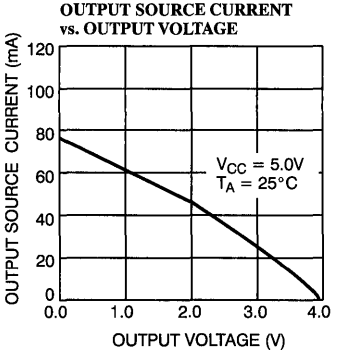


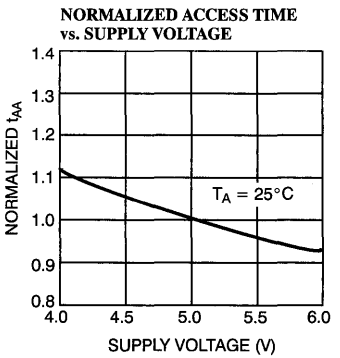
C164-10

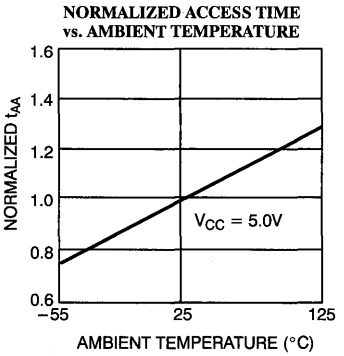
Typical DC and AC Characteristics

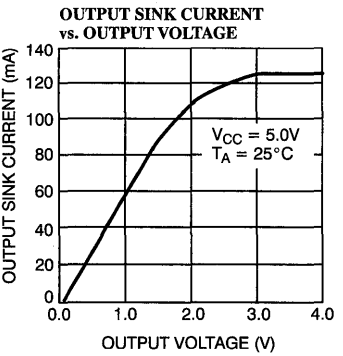






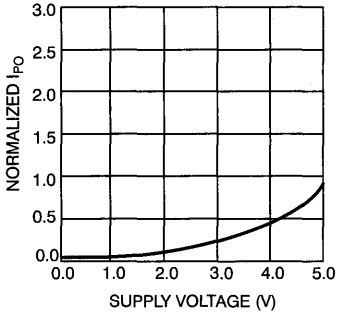




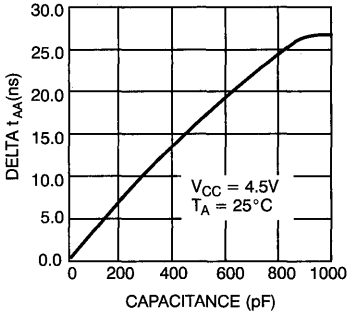


Typical DC and AC Characteristics (continued)

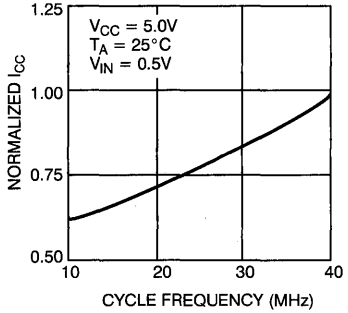
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



CY7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	H	Data In	Write
L	H	H	High Z	Write

Address Designators

Address Name	Address Function	CY 7C164 Pin Number	CY7C166 Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C164–12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164–12VC	V13	24-Lead Molded SOJ	
15	CY7C164–15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164–15VC	V13	24-Lead Molded SOJ	
20	CY7C164–20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164–20VC	V13	24-Lead Molded SOJ	
25	CY7C164–25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164–25VC	V13	24-Lead Molded SOJ	
35	CY7C164–35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164–35VC	V13	24-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C166–12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166–12VC	V13	24-Lead Molded SOJ	
15	CY7C166–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166–15VC	V13	24-Lead Molded SOJ	
20	CY7C166–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166–20VC	V13	24-Lead Molded SOJ	
25	CY7C166–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166–25VC	V13	24-Lead Molded SOJ	
35	CY7C166–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166–35VC	V13	24-Lead Molded SOJ	

Shaded areas contain advanced information.

Document #: 38–00032–H

CY7C164A
CY7C166A

CYPRESS SEMICONDUCTOR

16K x 4 Static RAM

Features

- **High speed**
  — 20 ns
- **Output enable ($\overline{OE}$) feature (7C166A)**
- **CMOS for optimum speed/power**
- **Low active power**
  — 550 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166A has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

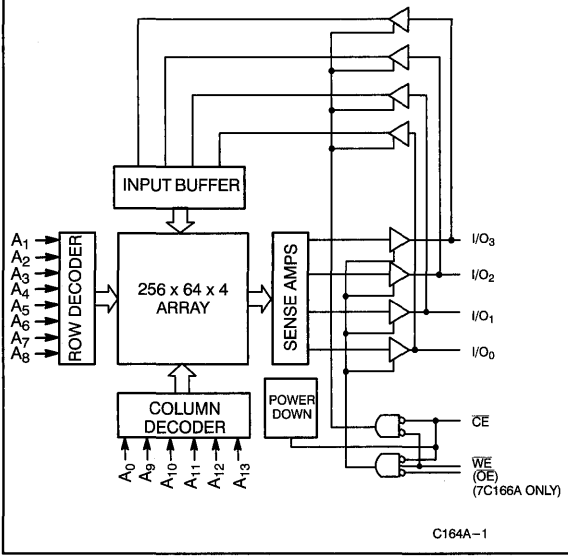
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166A). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166A), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or output enable ($\overline{OE}$) is HIGH for 7C166A).

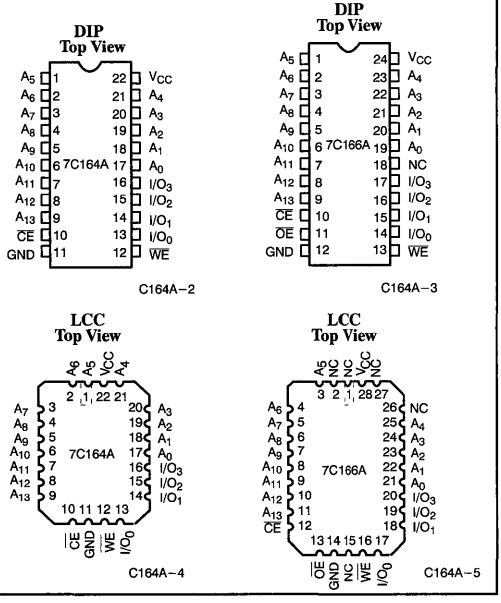
A die coat is used to insure alpha immunity.

Logic Block Diagram



C164A–1

Pin Configurations



Selection Guide[1]

		7C164A–15 7C166A–15	7C164A–20 7C164A–20	7C164A–25 7C166A–25	7C164A–35 7C166A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C164/CY7C166 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... − 0.5V to +7.0V

DC Input Voltage[2] ..... − 0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C164A−15 7C166A−15 Min.	7C164A−15 7C166A−15 Max.	7C164A−20 7C166A−20 Min.	7C164A−20 7C166A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		160		100	mA
I_{SB1}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

Shaded area contains advanced information.

Notes:

2. Minimum voltage is equal to − 3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.;
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range [4](continued)

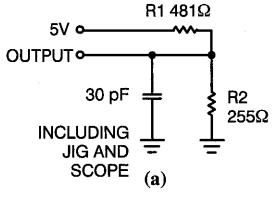
Parameter	Description	Test Conditions		7C164A–25 7C166A–25 Min.	7C164A–25 7C166A–25 Max.	7C164A–35 7C166A–35 Min.	7C164A–35 7C166A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		100		100	mA
I_{SB1}	Automatic $\overline{CE}$ [6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ [6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

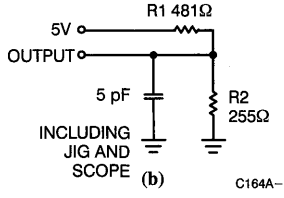
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

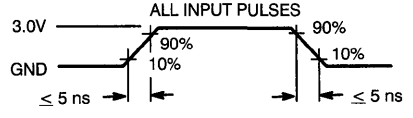
Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



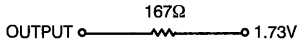


C164A–6



C164A–7

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 8]

Parameter	Description	7C164A–15 7C166A–15		7C164A–20 7C166A–20		7C164A–25 7C166A–25		7C164A–35 7C166A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid (7C166A)		7		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z (7C166A)	0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z (7C166A)		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7		7		10	ns

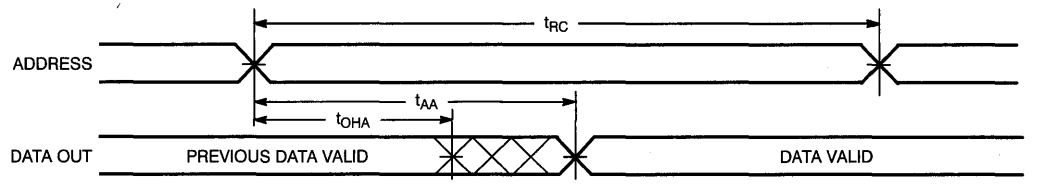
Shaded area contains advanced information.

Notes:

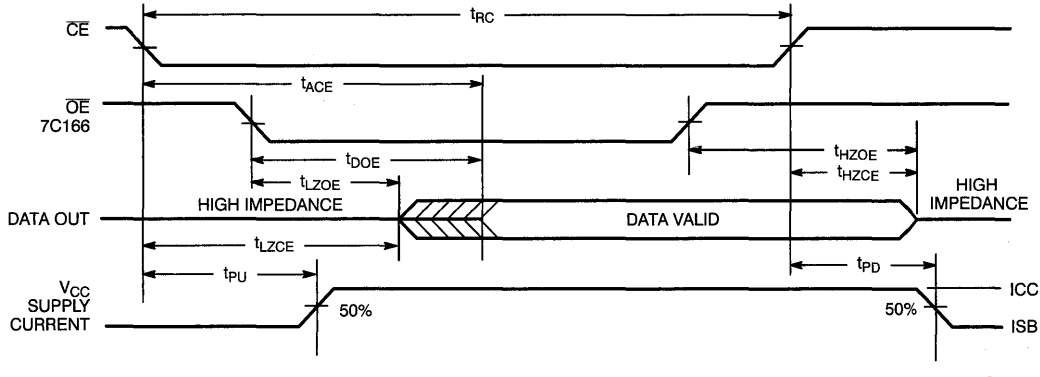
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
10. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

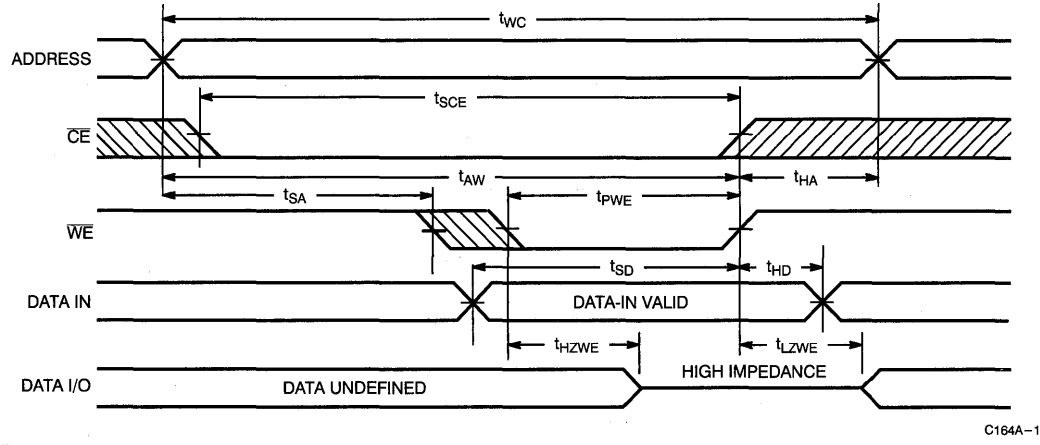
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



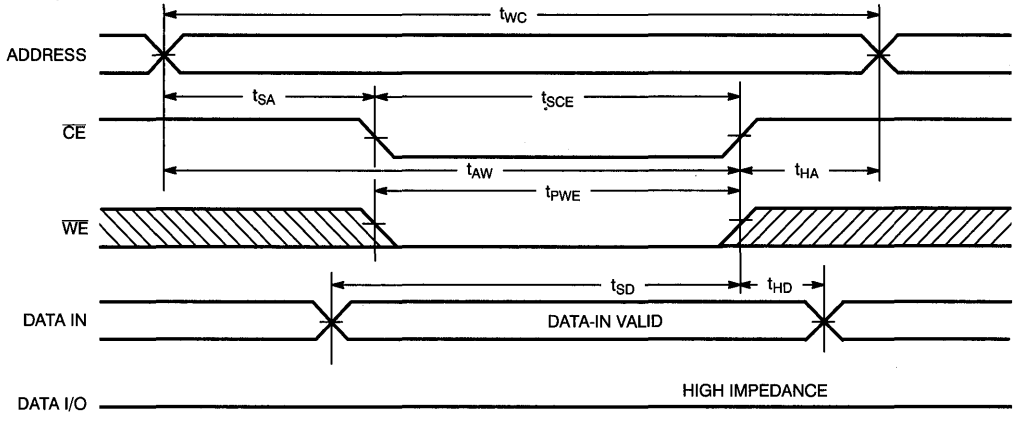
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11, 15]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7C166A $\overline{OE}$ = V_{IL} also).
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. 7C166A only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

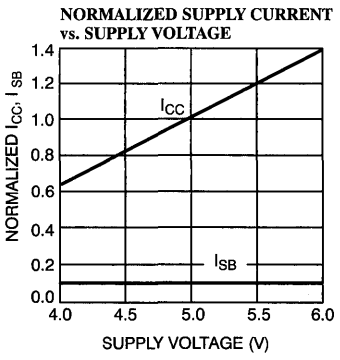
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15, 16]

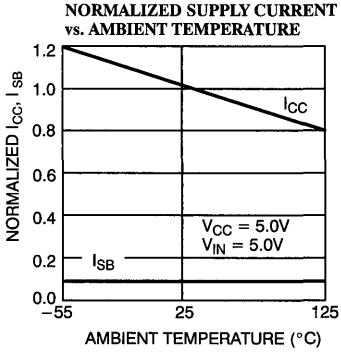


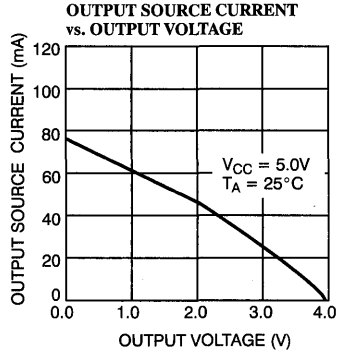
C164A–11

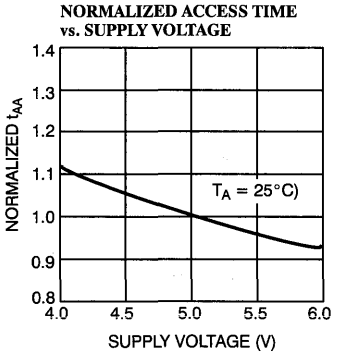
Note:
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

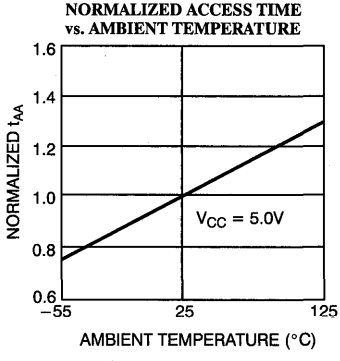
Typical DC and AC Characteristics

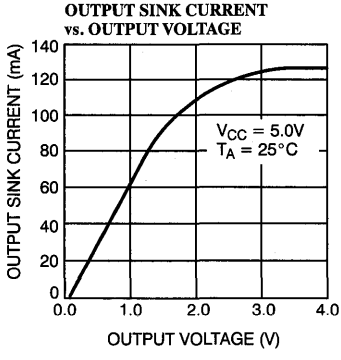






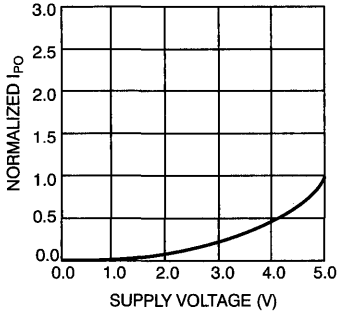




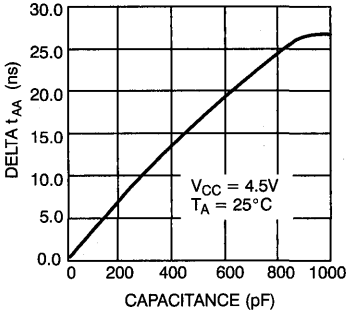


Typical DC and AC Characteristics (continued)

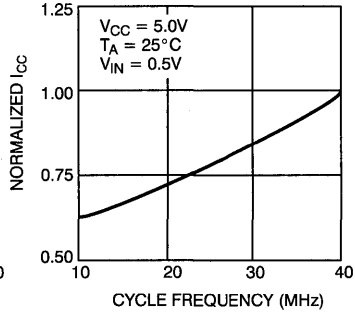
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



CY7C164A Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166A Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	CY7C164A Pin Number	CY7C166A Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C164A–15DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7C164A–15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
20	CY7C164A–20DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7C164A–20LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
25	CY7C164A–25DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7C164A–25LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
35	CY7C164A–35DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7C164A–35LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C166A–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C166A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C166A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C166A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C166A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C166A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C166A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C166A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[17]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
17. 7C166A only.

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  — 15 ns
- **Low active power**
  — 275 mW
- **Low standby power**
  — 83 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C167A is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

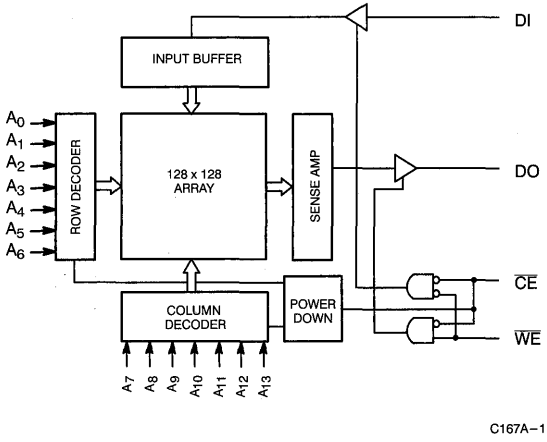
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these condintions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

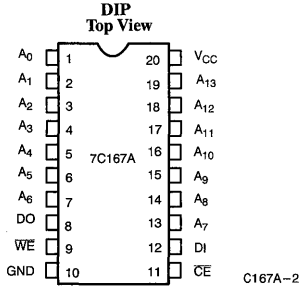
A die coat is used to insure alpha immunity.

Logic Block Diagram



C167A–1

Pin Configuration



C167A–2

Selection Guide

		7C167A–15	7C167A–20	7C167A–25	7C167A–35	7C167A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	60	60	
	Military		80	70	60	50

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C167A−15 Min.	7C167A−15 Max.	7C167A−20 Min.	7C167A−20 Max.	7C167A−25 Min.	7C167A−25 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		80		60	mA
			Mil				80		70	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40		20	mA
			Mil				40		20	

Parameter	Description	Test Conditions		7C167A−35 Min.	7C167A−35 Max.	7C167A−45 Min.	7C167A−45 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		60		50	mA
			Mil		60		50	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20			mA
			Mil		20		20	

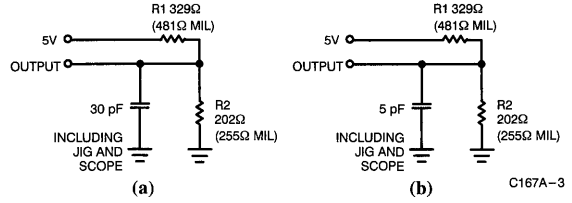
Notes:

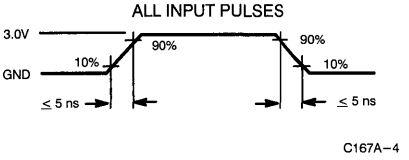
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Capacitance[6]

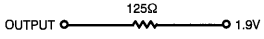
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF
C_{CE}	Chip Enable Capacitance		6	pF

AC Test Loads and Waveforms

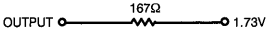




Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

Switching Characteristics Over the Operating Range[2, 7]

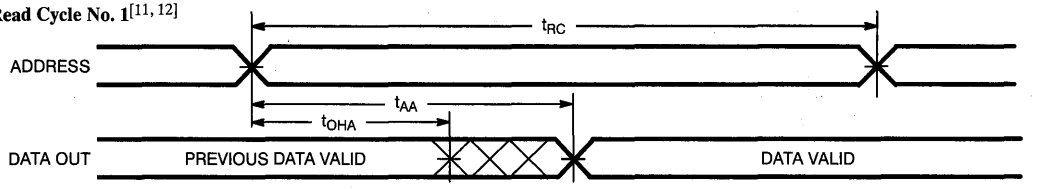
Parameter	Description		7C167A–15		7C167A–20		7C167A–25		7C167A–35		7C167A–45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE													
t_{RC}	Read Cycle Time	Com'l	15		20		25		30				ns
		Mil			20		25		35		40		ns
t_{AA}	Address to Data Valid	Com'l		15		20		25		30			ns
		Mil				20		25		35		40	ns
t_{OHA}	Data Hold from Address Change		5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE[10]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]			7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]		5		5		5		5		5		ns

Notes:

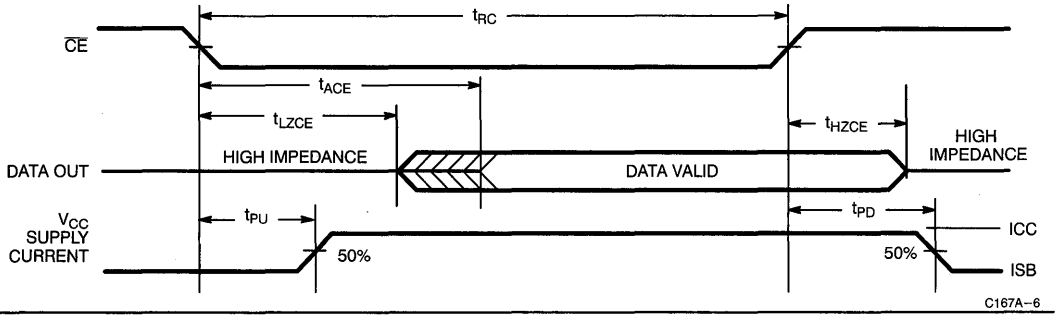
6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

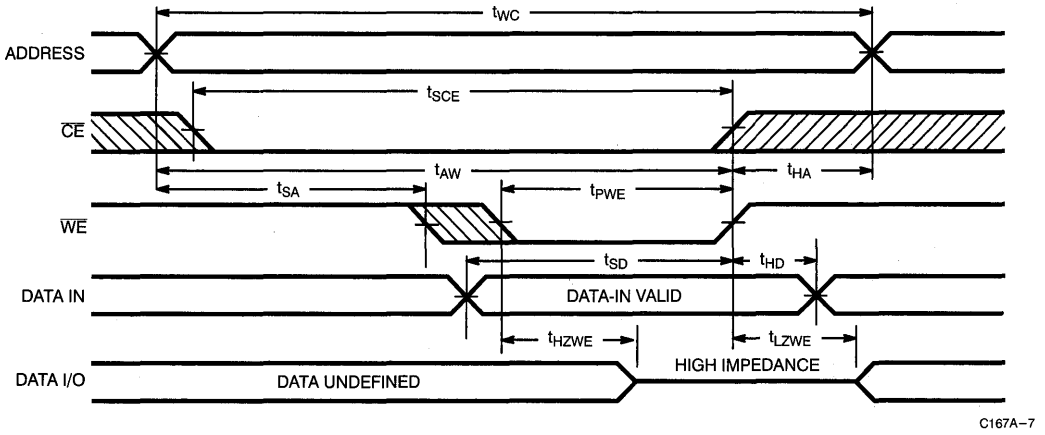
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]

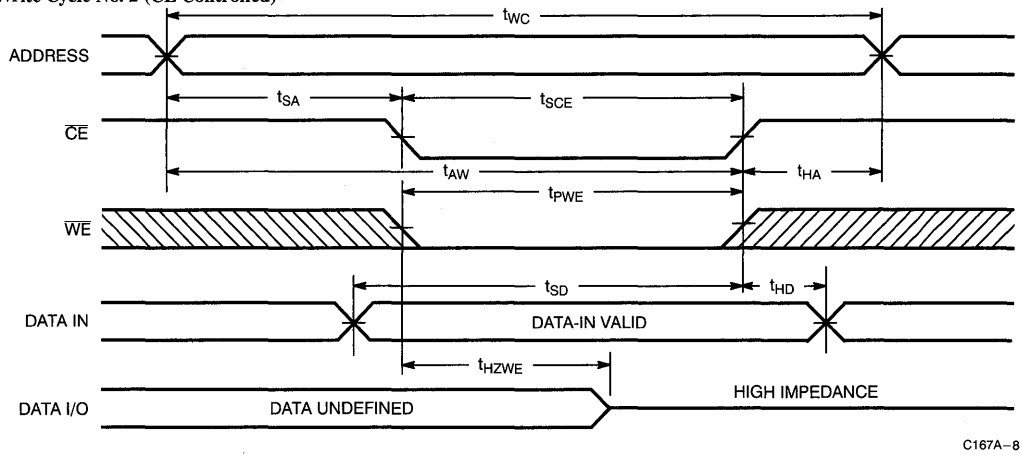


Notes:

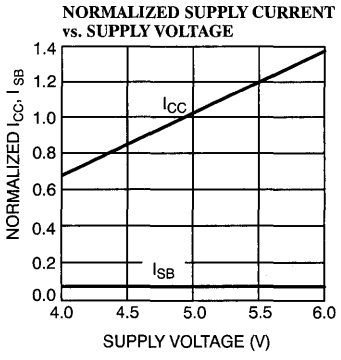
11. $\overline{WE}$ is high for read cycle.
12. Device is continuously selected, $\overline{CE} = V_{IL}$.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

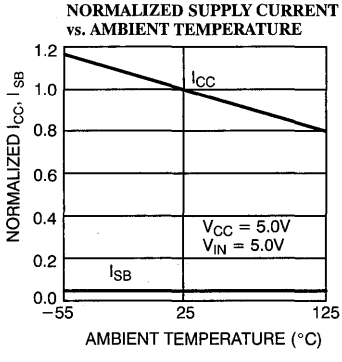
Switching Waveforms (continued)

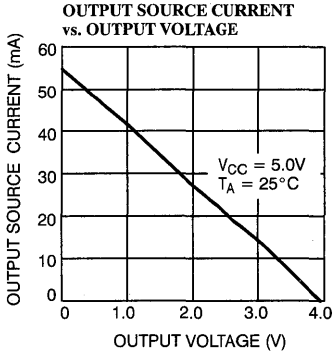
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

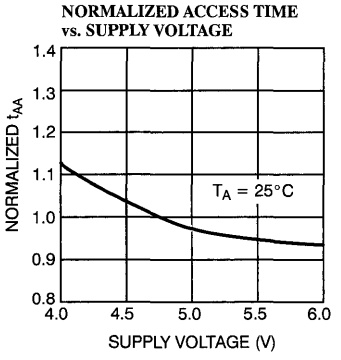


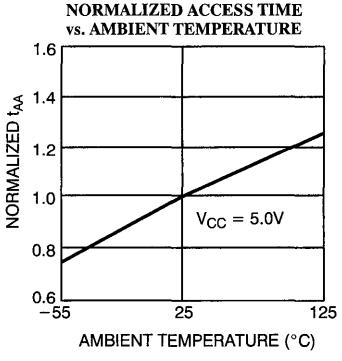
Typical DC and AC Characteristics

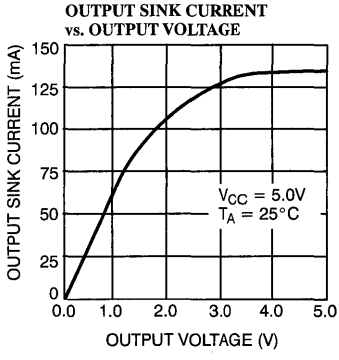






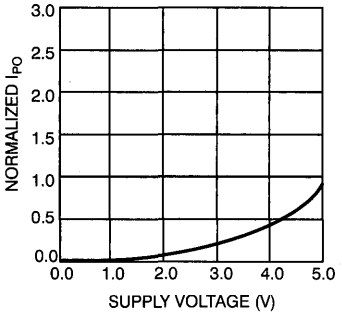




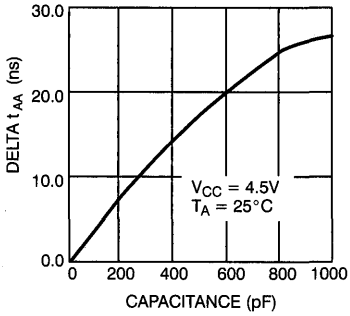


Typical DC and AC Characteristics (continued)

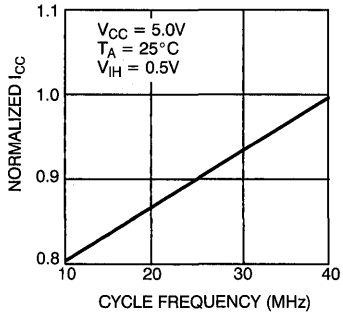
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	80	CY7C167A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–15VC	V5	20-Lead Molded SOJ	
20	80	CY7C167A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–20VC	V5	20-Lead Molded SOJ	
		CY7C167A–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	60	CY7C167A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–25VC	V5	20-Lead Molded SOJ	
		CY7C167A–25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	60	CY7C167A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–35VC	V5	20-Lead Molded SOJ	
		CY7C167A–35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	50	CY7C167A–45DMB	D6	20-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

CY7C168A
CY7C169A

CYPRESS SEMICONDUCTOR

4K x 4 R/W RAM

Features

- **Automatic power-down when deselected (7C168A)**
- **CMOS for optimum speed/power**
- **High speed**
  - **t_{AA} = 15 ns**
  - **t_{ACE} = 10 ns (7C169A)**
- **Low active power**
  - **385 mW**
- **Low standby power (7C168)**
  - **83 mW**
- **TTL-compatible inputs and outputs**
- **V_{IH} of 2.2V**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C168A and CY7C169A are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

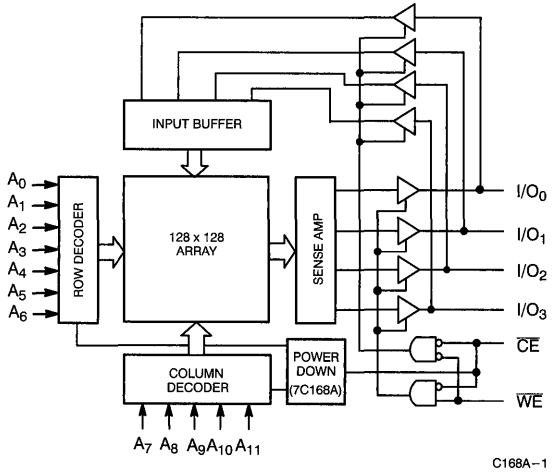
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable is HIGH or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

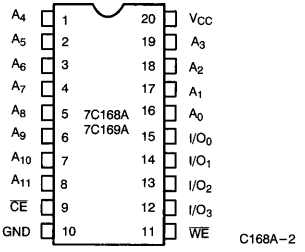
Logic Block Diagram



C168A–1

Pin Configurations

DIP/SOJ
Top View



C168A–2

Selection Guide

		7C168A–15 7C169A–15	7C168A–20 7C169A–20	7C168A–25 7C169A–25	7C168A–35 7C169A–35	7C168A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	70	70	
	Military		90	80	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C168A−15 7C169A−15 Min.	7C168A−15 7C169A−15 Max.	7C168A−20 7C169A−20 Min.	7C168A−20 7C169A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				90	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40	mA
			Mil				40	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ VCC −0.3 V	Com'l		20		20	mA
			Mil				20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

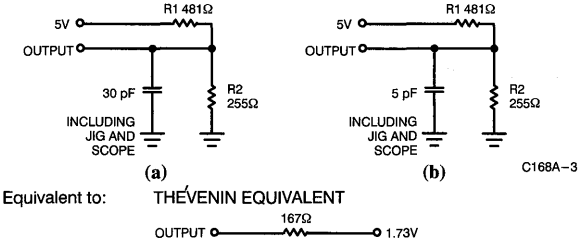
Electrical Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Test Conditions		7C168A–25 7C169A–25 Min.	7C168A–25 7C169A–25 Max.	7C168A–35 7C169A–35 Min.	7C168A–35 7C169A–35 Max.	7C168A–45 Min.	7C168A–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−50	50	−50	50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70			mA
			Mil		80		70		70	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20		20			mA
			Mil		20		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ VCC −0.3 V	Com'l		20		20			mA
			Mil		20		20		20	

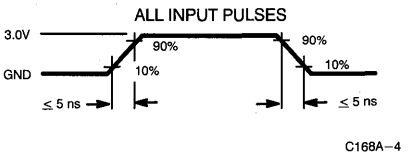
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description		7C168A–15 7C169A–15 Min.	7C168A–15 7C169A–15 Max.	7C168A–20 7C169A–20 Min.	7C168A–20 7C169A–20 Max.	7C168A–25 7C169A–25 Min.	7C168A–25 7C169A–25 Max.	Unit
READ CYCLE									
t_{RC}	Read Cycle Time		15		20		25		ns
t_{AA}	Address to Data Valid			15		20		25	ns
t_{OHA}	Output Hold from Address Change		5		5		5		ns
t_{ACE}	Power Supply Current	7C168A		15		20		25	ns
		7C169A		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7, 8]		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 9]			8		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)			15		20		20	ns
t_{RCS}	Read Command Set-Up		0		0		0		ns
t_{RCH}	Read Command Hold		0		0		0		ns
WRITE CYCLE[10]									
t_{WC}	Write Cycle Time		15		20		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		ns
t_{AW}	Address Set-Up to Write End		12		15		20		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		ns
t_{SD}	Data Set-Up to Write End		10		10		10		ns
t_{HD}	Data Hold from Write End		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		7		7		7		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]			5		5		5	ns

Notes:

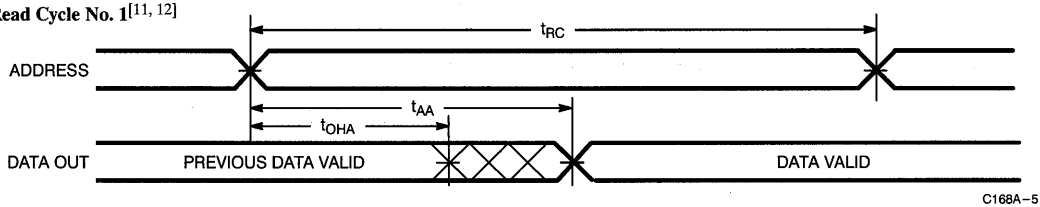
7. At any given temperature and voltage condition, T_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
8. 3-ns minimum for the CY7C169A.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition low.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Characteristics Over the Operating Range[3, 6] (continued)

Parameter	Description		7C168A–35 7C169A–35 Min.	7C168A–35 7C169A–35 Max.	7C168A–45 Min.	7C168A–45 Max.	Unit
READ CYCLE							
t_{RC}	Read Cycle Time		35		45		ns
t_{AA}	Address to Data Valid			35		45	ns
t_{OHA}	Output Hold from Address Change		5		5		ns
t_{ACE}	Power Supply Current	7C168A		35		45	ns
		7C169A		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7, 8]		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 9]			15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)			20		25	ns
t_{RCS}	Read Command Set-Up		0		0		ns
t_{RCH}	Read Command Hold		0		0		ns
WRITE CYCLE[10]							
t_{WC}	Write Cycle Time		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		30		ns
t_{AW}	Address Set-Up to Write End		25		30		ns
t_{HA}	Address Hold from Write End		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		20		20		ns
t_{SD}	Data Set-Up to Write End		15		15		ns
t_{HD}	Data Hold from Write End		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]			10		15	ns

Switching Waveforms

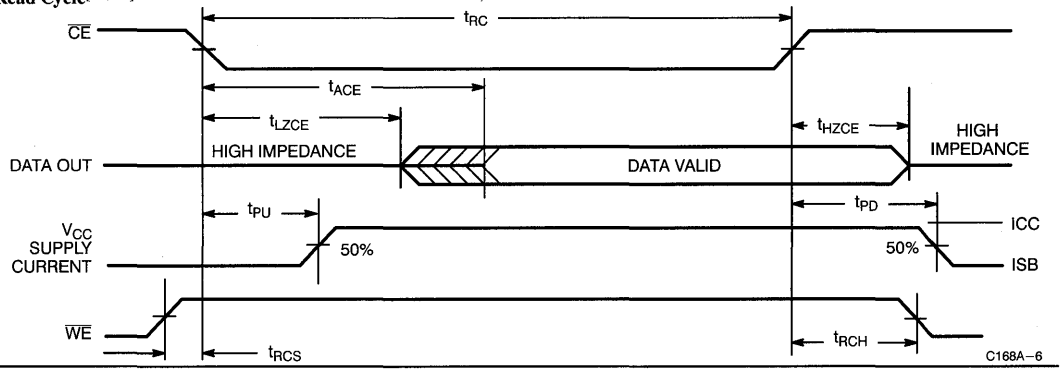
Read Cycle No. 1[11, 12]



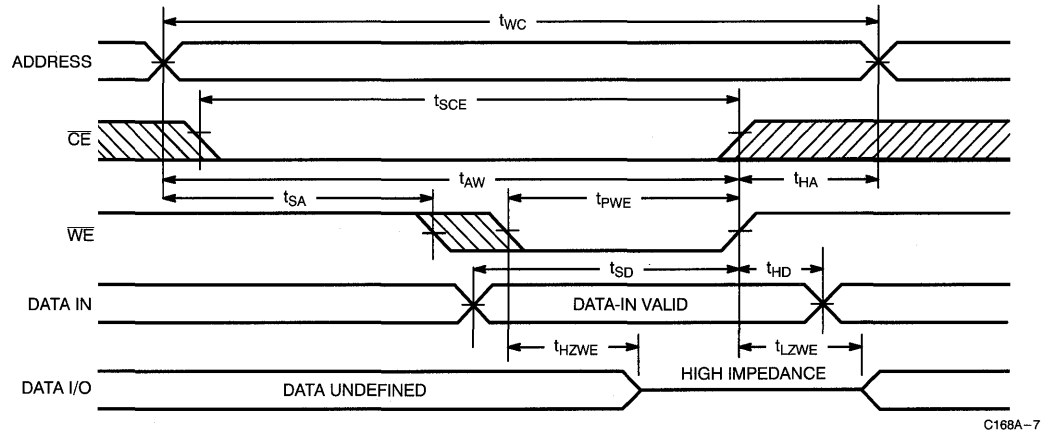
C168A–5

Switching Waveforms (continued)

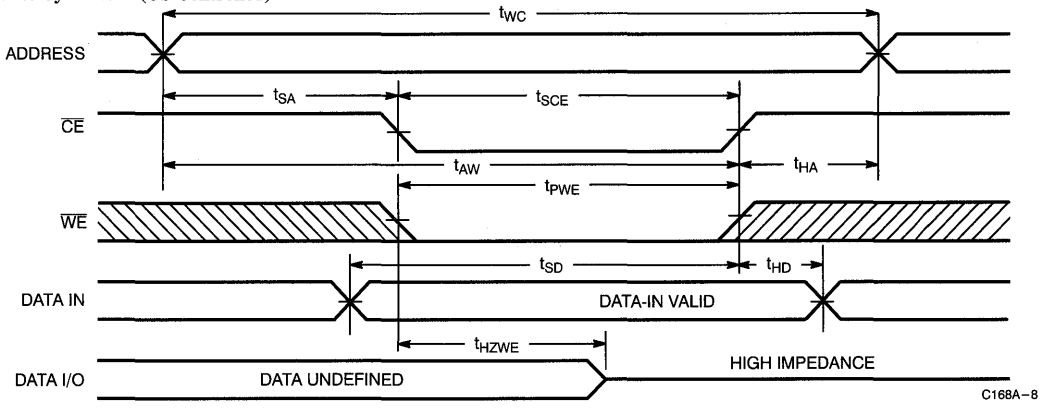
Read Cycle[11, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]

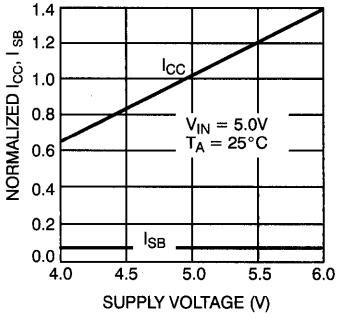


Write Cycle No. 2 ($\overline{CS}$ Controlled) [10, 14]

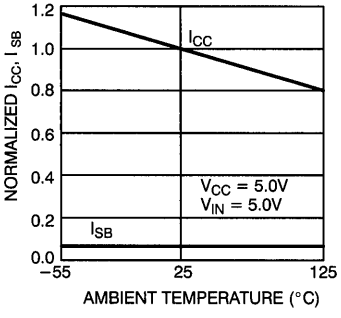


Typical DC and AC Characteristics

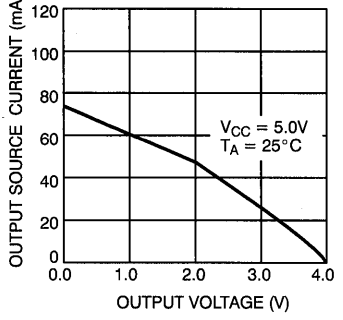
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



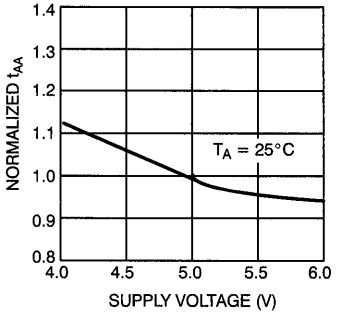
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



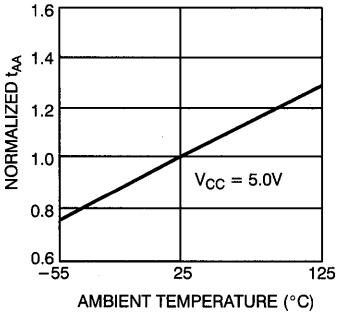
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



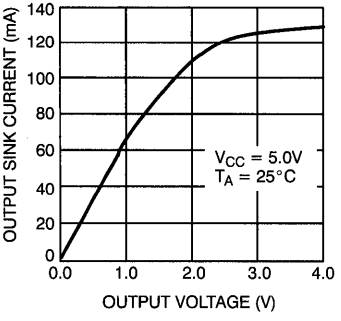
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



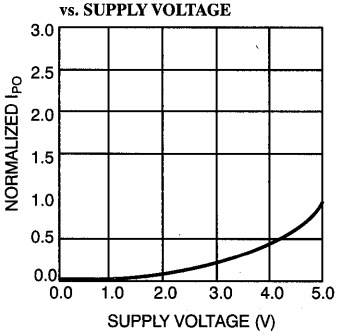
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



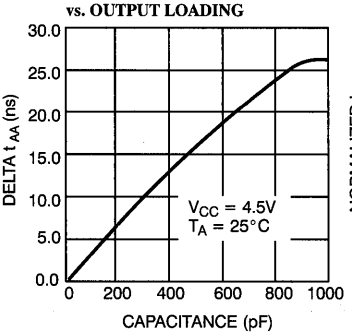
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



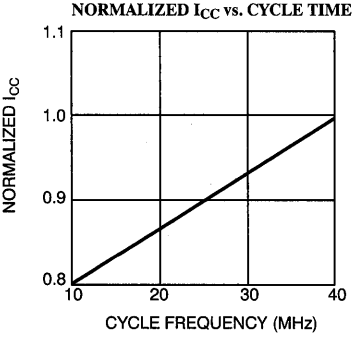
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C168A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–15VC	V5	20-Lead Molded SOJ	
20	90	CY7C168A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–20VC	V5	20-Lead Molded SOJ	
		CY7C168A–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	70	CY7C168A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–25VC	V5	20-Lead Molded SOJ	
	80	CY7C168A–25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	70	CY7C168A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–35VC	V5	20-Lead Molded SOJ	
		CY7C168A–35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	70	CY7C168A–45DMB	D6	20-Lead (300-Mil) CerDIP	Military

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C169A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–15VC	V5	20-Lead Molded SOJ	
20	90	CY7C169A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–20VC	V5	20-Lead Molded SOJ	
25	70	CY7C169A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–25VC	V5	20-Lead Molded SOJ	
35	70	CY7C169A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–35VC	V5	20-Lead Molded SOJ	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}[15]	1, 2, 3
I_{SB2}[15]	1, 2, 3

Note:
15. 7C168 only.

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CY7C170A

4K x 4 Static R/W RAM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 15 ns**
  - **— t_{ACS} = 10 ns**
- **Low active power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Output enable**
- **V_{IH} of 2.2V**

Functional Description

The CY7C170A is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$) and three-state drivers.

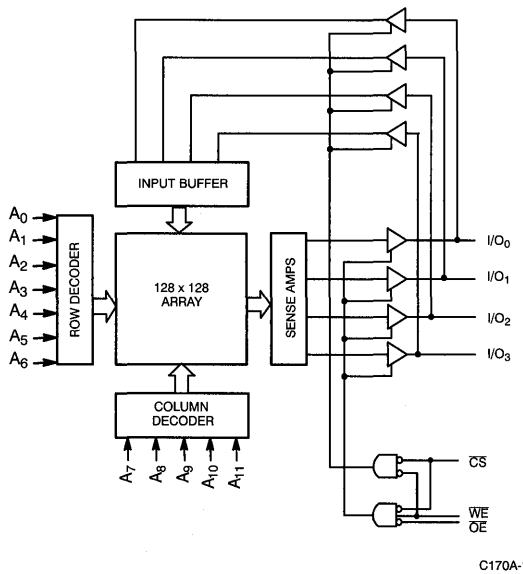
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

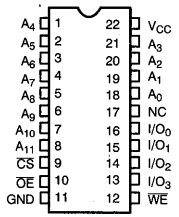
Logic Block Diagram



C170A-1

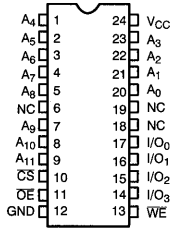
Pin Configurations

DIP
Top View



C170A-2

SOJ
Top View



C170A-3

Selection Guide

		7C170A–15	7C170A–20	7C170A–25	7C170A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Commercial	115	90	90	90
	Military			120	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 21) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C170A−15 Min.	7C170A−15 Max.	7C170A−20, 25, 35, 45 Min.	7C170A−20, 25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				120	mA

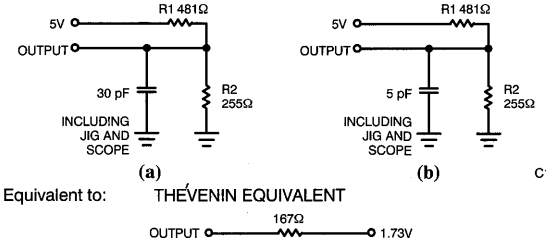
Capacitance[4]

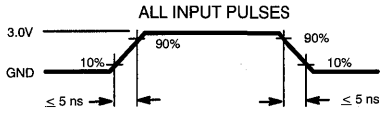
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[1, 5]

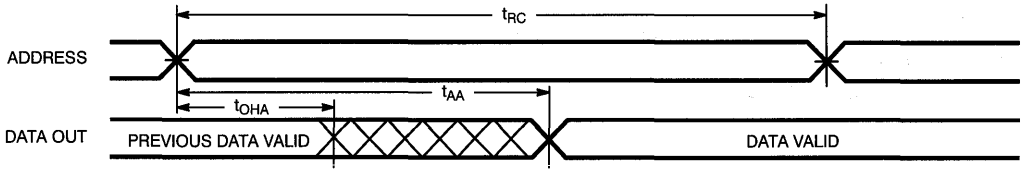
Parameter	Description	7C170A–15		7C170A–20		7C170A–25		7C170A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		10		15		15		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		8		8		10		12	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		8		8		10		15	ns
WRITE CYCLE[8]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z		7		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
11. Data I/O will be high-impedance if $\overline{OE}$ = V_{IH}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1[9, 10]



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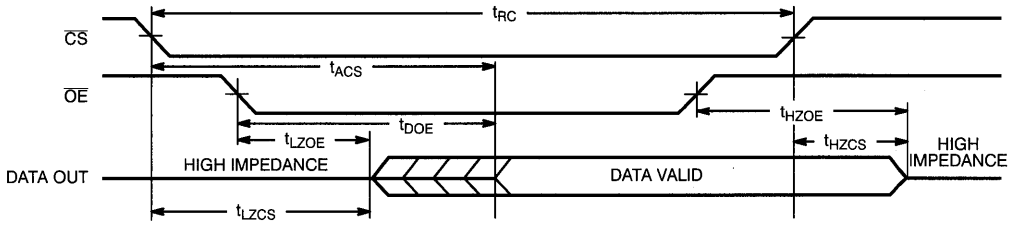
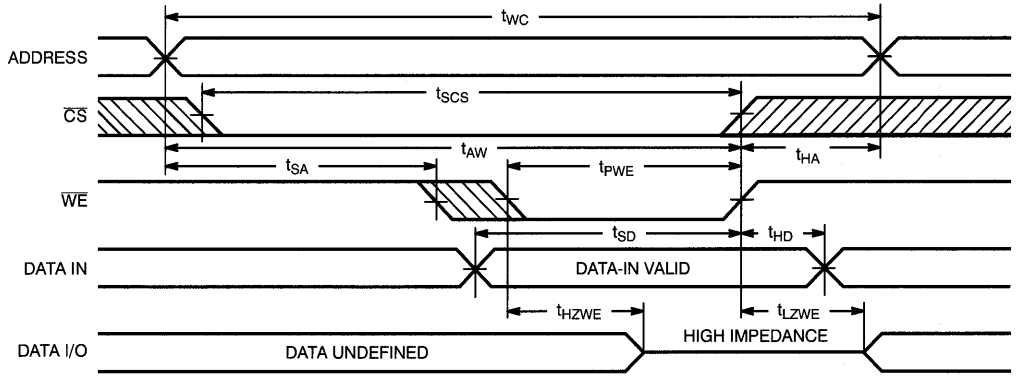
Switching Waveforms (continued)

Read Cycle No. 2[9, 11]



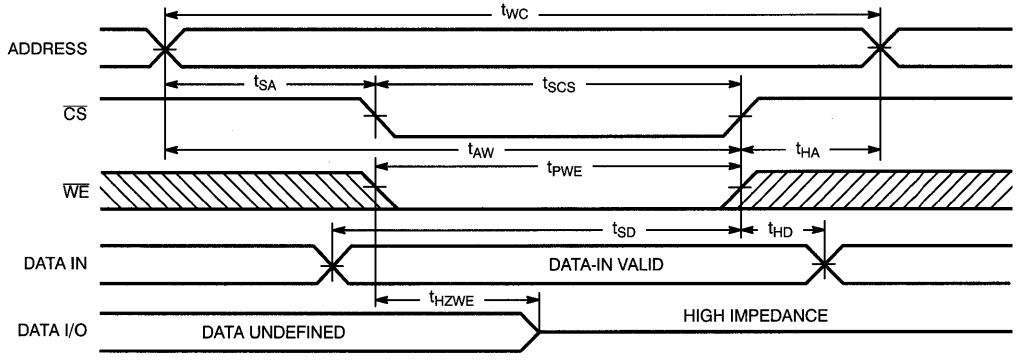
C170A-7

Write Cycle No. 1[8, 12]



C170A-8

Write Cycle No. 2[8, 12, 13]



C170A-9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C170A–15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–15VC	V13	24-Lead Molded SOJ	
20	CY7C170A–20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–20VC	V13	24-Lead Molded SOJ	
25	CY7C170A–25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–25VC	V13	24-Lead Molded SOJ	
	CY7C170A–25DMB	D10	22-Lead (300-Mil) CerDIP	Military
35	CY7C170A–35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–35VC	V13	24-Lead Molded SOJ	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

CY7C171A
CY7C172A

4K x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 15 ns**
- **Transparent write (7C171A)**
- **Low active power**
  - **— 375 mW**
- **Low standby power**
  - **— 93 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

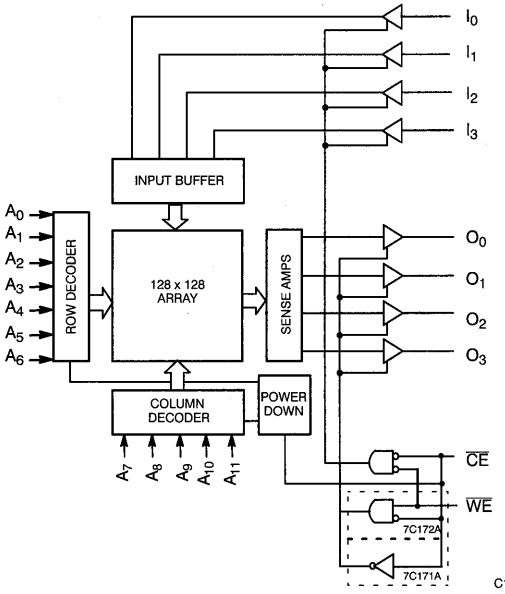
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

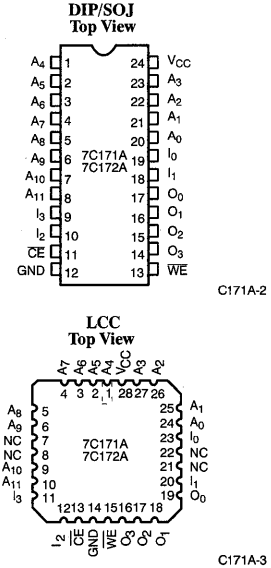
The output pins remain in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C172A only), or chip enable is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C171A–15 7C172A–15	7C171A–20 7C172A–20	7C171A–25 7C172A–25	7C171A–35 7C172A–35	7C171A–45 7C172A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	80	70	70	
	Military		90	80	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C171A−15 7C172A−15 Min.	7C171A−15 7C172A−15 Max.	7C171A−20 7C172A−20 Min.	7C171A−20 7C172A−20 Max.	7C171A−25 7C172A−25 Min.	7C171A−25 7C172A−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		80		70	mA
			Mil				90		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		40		40		20	mA
			Mil				40		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20		20	mA
			Mil				20		20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

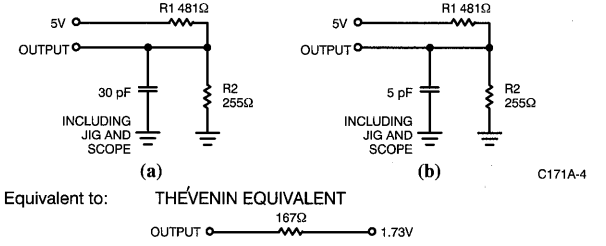
Parameter	Description	Test Conditions		7C171A–35 7C172A–35 Min.	7C171A–35 7C172A–35 Max.	7C171A–45 7C172A–45 Min.	7C171A–45 7C172A–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		70			mA
			Mil		70		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		20			mA
			Mil		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20			mA
			Mil		20		20	

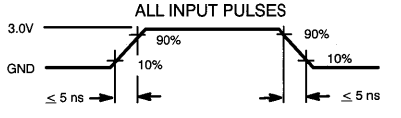
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
4. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[2,5]

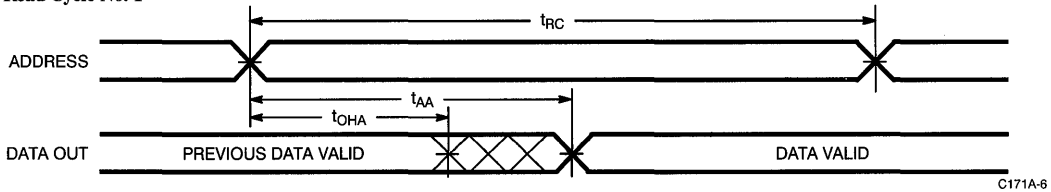
Parameter	Description	7C171A–15 7C172A–15		7C171A–20 7C172A–20		7C171A–25 7C172A–25		7C171A–35 7C172A–35		7C171A–45 7C172A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to LOW Z[6]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to HIGH Z[6, 7]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		20		20		25	ns
t_{RCS}	Read Command Set-Up	0		0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		0		ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C172A)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7] (7C172A)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C171A)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171A)		15		20		25		30		35	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C172A).

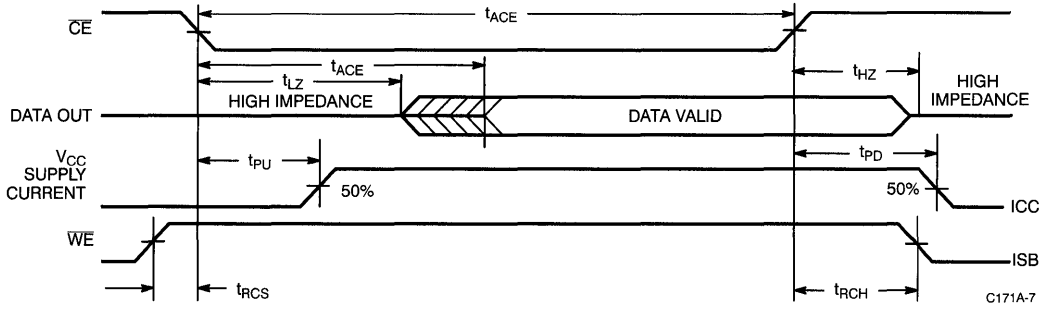
Switching Waveforms

Read Cycle No. 1[9, 10]

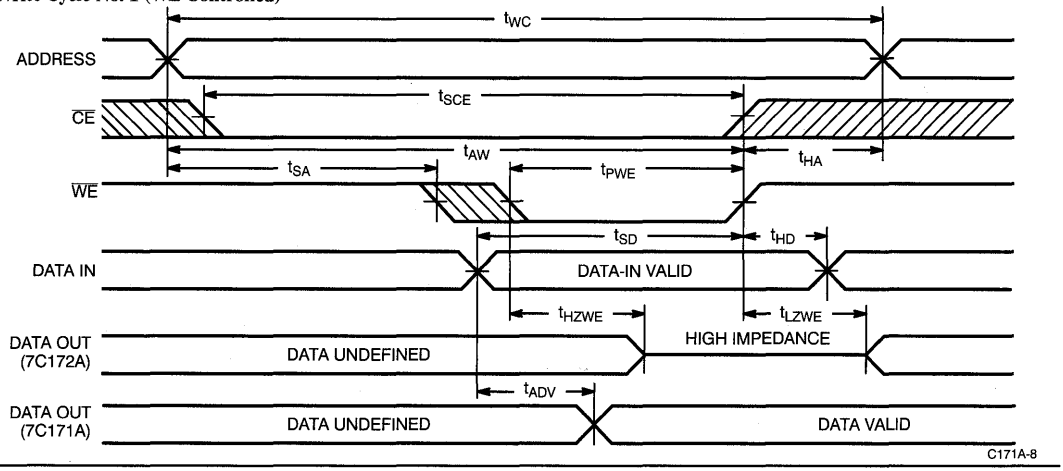


Switching Waveforms

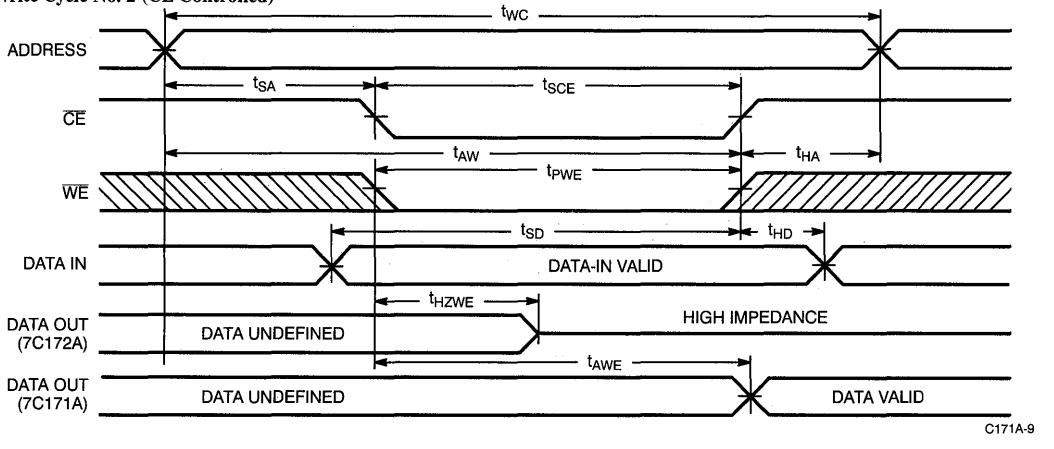
Read Cycle No. 2[9, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]

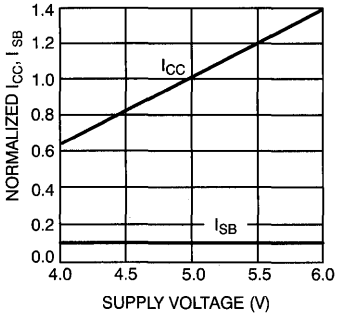


Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12]

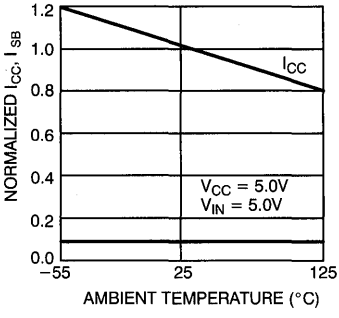


Typical DC and AC Characteristics

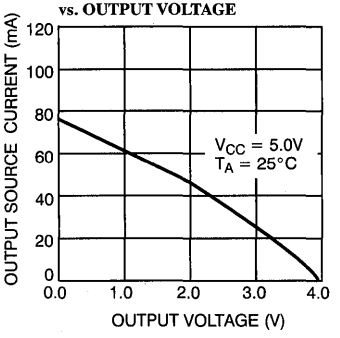
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



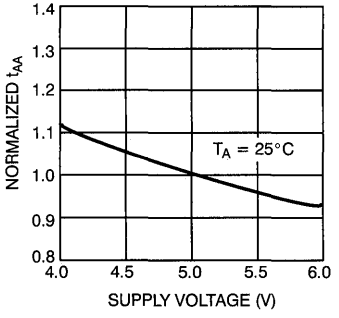
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



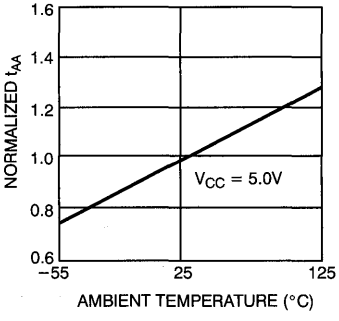
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



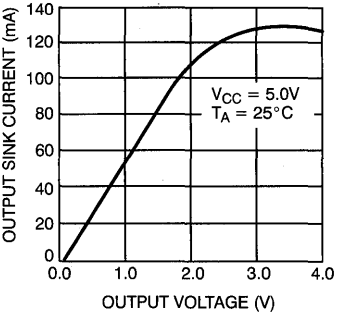
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



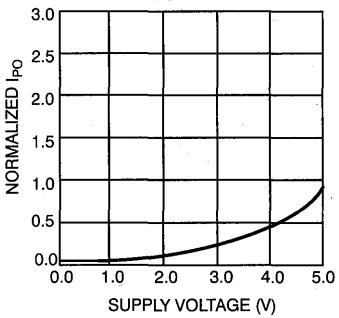
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



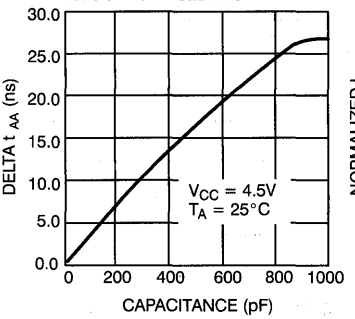
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



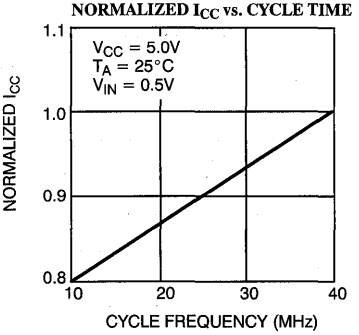
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C171A–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C171A–15VC	V13	24-Lead Molded SOJ	
20	CY7C171A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C171A–20VC	V13	24-Lead Molded SOJ	
	CY7C171A–DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C171A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C171A–25VC	V13	24-Lead Molded SOJ	
	CY7C171A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C171A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C171A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C171A–35VC	V13	24-Lead Molded SOJ	
	CY7C171A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C171A–35LMB	L64	28-Square Leadless Chip Carrier	
45	CY7C171A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C171A–45LMB	L64	28-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C172A–5PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–15VC	V13	24-Lead Molded SOJ	
20	CY7C172A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–20VC	V13	24-Lead Molded SOJ	
	CY7C172A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C172A–20LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C172A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–25VC	V13	24-Lead Molded SOJ	
	CY7C172A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C172A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C172A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C172A–35LMB	L64	28-Square Leadless Chip Carrier	
45	CY7C172A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C171A only.

Document #: 38−00104−C

CY7B173
CY7B174

32K x 9 Synchronous Cache R/W RAM

Features

- **Supports 50-MHz cache systems**
- **32K by 9 common I/O**
- **BiCMOS for optimum speed/power**
- **14-ns access delay (clock to output)**
- **Two-bit wraparound counter supporting the 486 burst sequence (7B173)**
- **Two-bit wraparound counter supporting the linear burst sequence (7B174)**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Two complementary synchronous chip selects**
- **Asynchronous output enable**

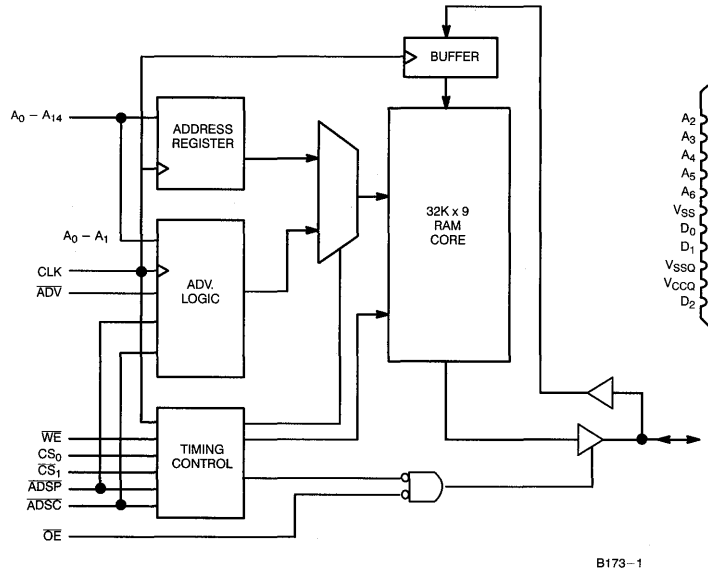
Functional Description

The CY7B173 and CY7B174 are 32K by 9 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 14 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

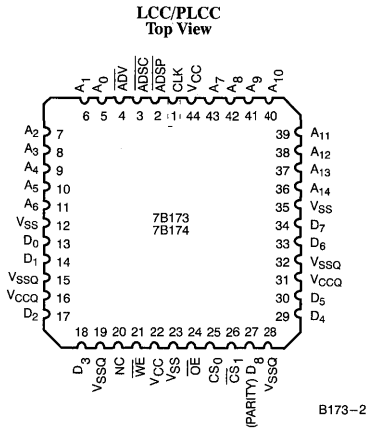
The CY7B173 is designed for Intel i486-based systems; its counter follows the burst sequence of the i486. The CY7B174 is architected for other processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. Two complementary synchronous chip select inputs are provided to support two banks of memory (256 Kbytes) with no external logic. These signals, in conjunction with the asynchronous output enable ($\overline{OE}$) signal, greatly simplify memory bank selection.

Logic Block Diagram



Pin Configurations



Selector Guide

		7B173–14 7B174–14	7B173–18 7B174–18	7B173–21 7B174–21
Maximum Access Time (ns)		14	18	21
Maximum Operating Current (mA)	Commercial	210	210	210
	Military		230	230

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) CS_0 = 1 and $\overline{CS_1}$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B173 and CY7B174 will be pulled LOW before the next clock rise.

If $\overline{WE}$ is LOW at the next clock rise, information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Because the CY7B173 and CY7B174 are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) CS_0 = 1 and $\overline{CS_1}$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$ trigger accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. Information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Since the CY7B173 and CY7B174 are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CS_0 = 1 and $\overline{CS_1}$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at D_0 through D_8 a maximum of 14 ns after clock rise.

Burst Sequences

The CY7B173 provides a 2-bit wraparound counter implementing the Intel 80486 sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

Table 1. Counter Implementation for the Intel 80486 Sequence

First Address		Second Address		Third Address		Fourth Address	
A_X + 1	A_X	A_X + 1	A_X	A_X + 1	A_X	A_X + 1	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

The CY7B174 provides a two-bit wraparound counter implementing a linear sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address		Second Address		Third Address		Fourth Address	
A_X + 1	A_X	A_X + 1	A_X	A_X + 1	A_X	A_X + 1	A_X
0	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	1	1	0

Application Example

Figure 1 shows a 128-Kbyte secondary cache for the i486 using four CY7B173 cache RAMs and a CY7B181 cache tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 12 ns.

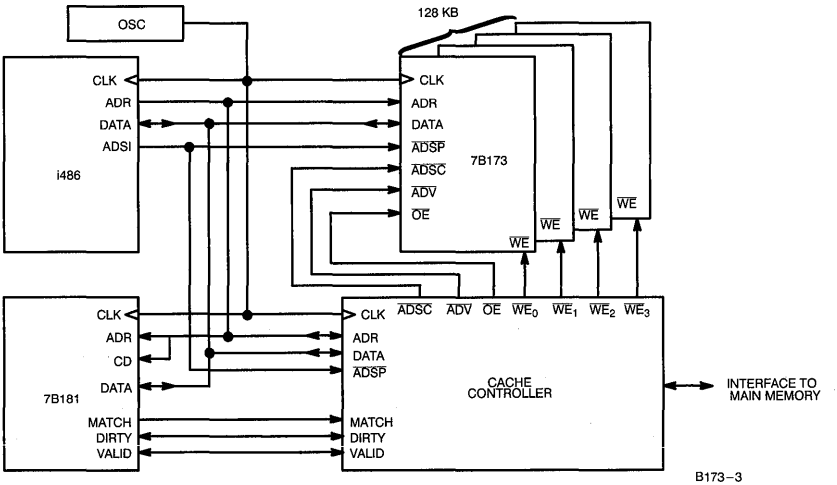


Figure 1. Cache Using Four CY7B173s

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{14}$	I	Address Inputs
CLK	I	Clock
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable
CS_0, $\overline{CS_1}$	I	Chip Select
$\overline{ADV}$	I	Address Advance
$\overline{ADSP}$	I	Processor Address Strobe
$\overline{ADSC}$	I	Cache Controller Address Strobe
$D_0 - D_8$	I/O	Data I/O
V_{CC}	–	+5V Power Supply
V_{SS}	–	Ground
V_{CCQ}	–	Output Buffer (Driver) Power Supply
V_{SSQ}	–	Output Buffer (Driver) Ground
RESV	–	Reserved

Pin Descriptions

Input Signals	
CLK	Clock signal used as the reference for most on-chip operations.
$\overline{ADSP}$	Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at A_0 through A_{14} will be loaded into the address register and the address advancement logic. The write signal, $\overline{WE}$, is ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$\overline{ADSC}$	Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B173/4. The write signal, $\overline{WE}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$A_0 - A_{14}$	Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations.
$\overline{WE}$	Write Enable: This signal is sampled at the rising edge of the clock signal. If $\overline{WE}$ = 0, a self-timed write operation will be initiated and data on $D_0 - D_8$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$ and $\overline{WE}$ are LOW at clock rise. In this case, the write signal is ignored.
$\overline{ADV}$	Address Advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B173, LOW at this input will advance the address in the advancement logic according to the Intel 80486 burst sequence. In the case of the CY7B174, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW).
$CS_0 - \overline{CS_1}$	Chip Select inputs: CS_0 is active HIGH and $\overline{CS_1}$ is active LOW. Both inputs are sampled at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The RAM is selected if CS_0 = 1 and $\overline{CS_1}$ = 0.
$\overline{OE}$	Output Enable: $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B173/4 is a common I/O device and three-state conflict may occur at the data pins.
NC	No Connect: This input can be left floating or tied to V_{SS} or V_{CC}.
Bidirectional Signals	
$D_0 - D_8$	Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WE}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B173−14 7B174−14 Min.	7B173−14 7B174−14 Max.	7B173−18, 21 7B174−18, 21 Min.	7B173−18, 21 7B174−18, 21 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 100	+100	− 100	+100	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		210		210	mA
			Mil				230	

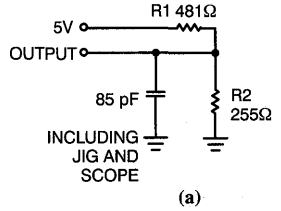
Capacitance[4]

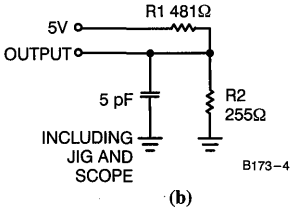
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4.5	pF
C_{IN}: Other Inputs			6	pF
C_{OUT}	Output Capacitance		13	pF

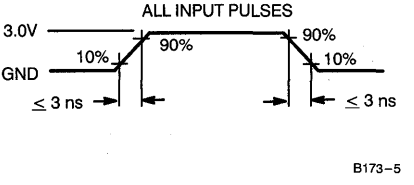
Notes:

1. V_{IL} (min.) = − 1.5V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

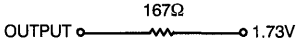
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5]

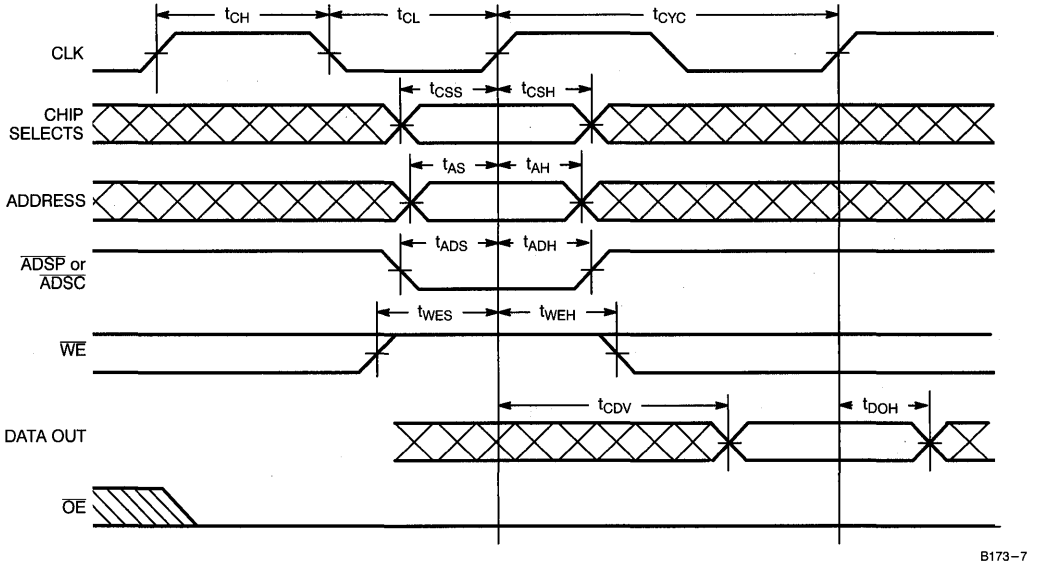
Parameter	Description	7B173–14 7B174–14		7B173–18 7B174–18		7B173–21 7B173–21		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20		25		30		ns
f_{MAX}	Maximum Frequency		50		40		33	MHz
t_{CH}	Clock HIGH	8		10		12		ns
t_{CL}	Clock LOW	8		10		12		ns
t_{AS}	Address Set-Up Before CLK Rise	2		4		5		ns
t_{AH}	Address Hold After CLK Rise	2		3		4		ns
t_{CDV}	Data Output Valid After CLK Rise		14		18		21	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	2		3		4		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	3		4		5		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	2		3		4		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	2		3		4		ns
t_{DS}	Data Input Set-Up Before CLK Rise	3		4		5		ns
t_{DH}	Data Input Hold After CLK Rise	2		3		4		ns
t_{CSS}	Chip Select Set-Up	3		4		5		ns
t_{CSH}	Chip Select Hold After CLK Rise	2		3		4		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[6, 7]		10		12		14	ns
t_{CSOV}	Chip Select Sampled to Output Valid	3	14	3	18	3	21	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]		7		9		11	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		7		9		11	ns
t_{WEOZ}	$\overline{WE}$ Sampled LOW to Output High Z[6]		10		12		14	ns
t_{WEOV}	$\overline{WE}$ Sampled HIGH to Output Valid	3	14	3	18	3	21	ns

Notes:

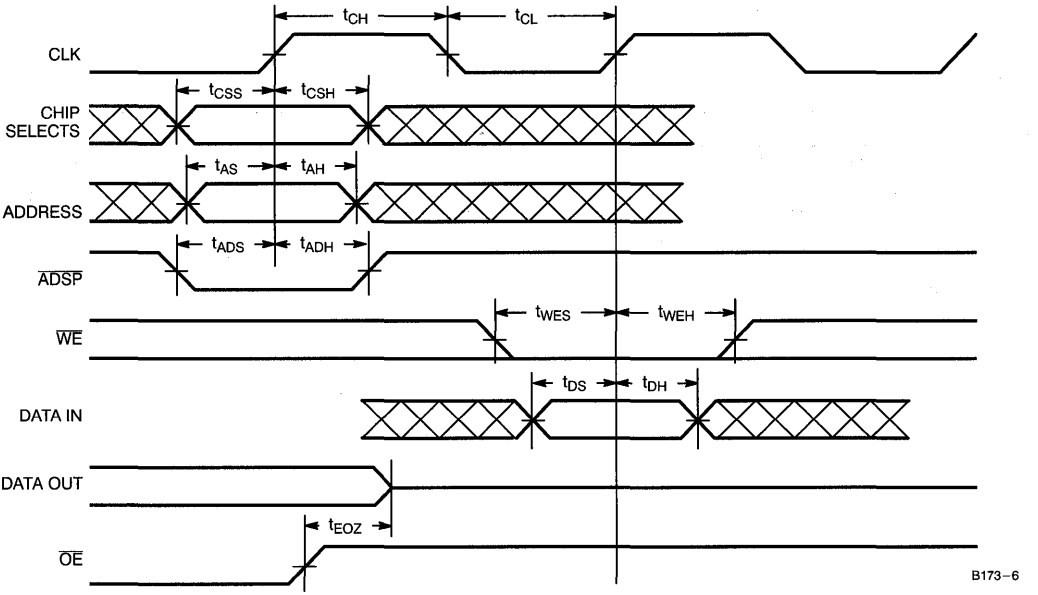
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
6. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given voltage and temperature, t_{CSOZ} (t_{WEOZ}) min. is less than t_{CSOV} (t_{WEOV}) min.

Switching Waveforms

Single Read

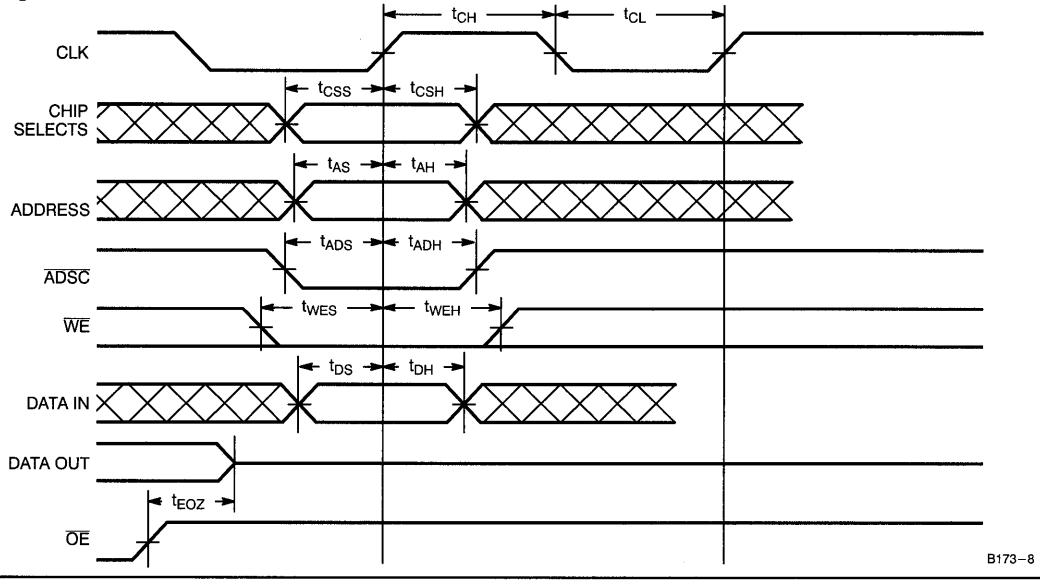


Single 486 Write

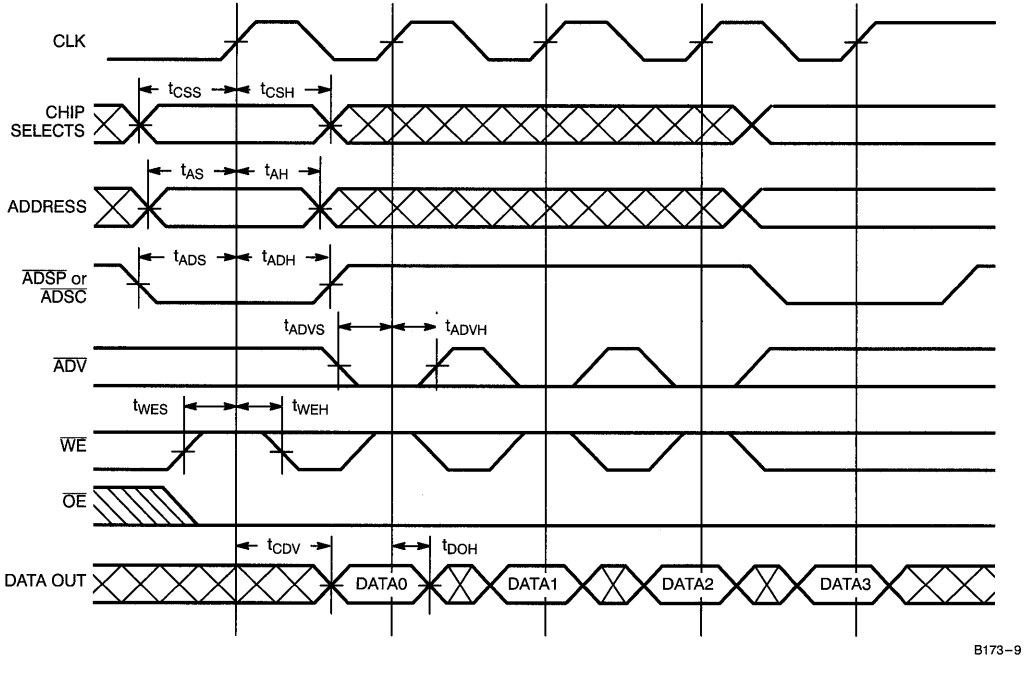


Switching Waveforms (continued)

Single Cache Controller Write

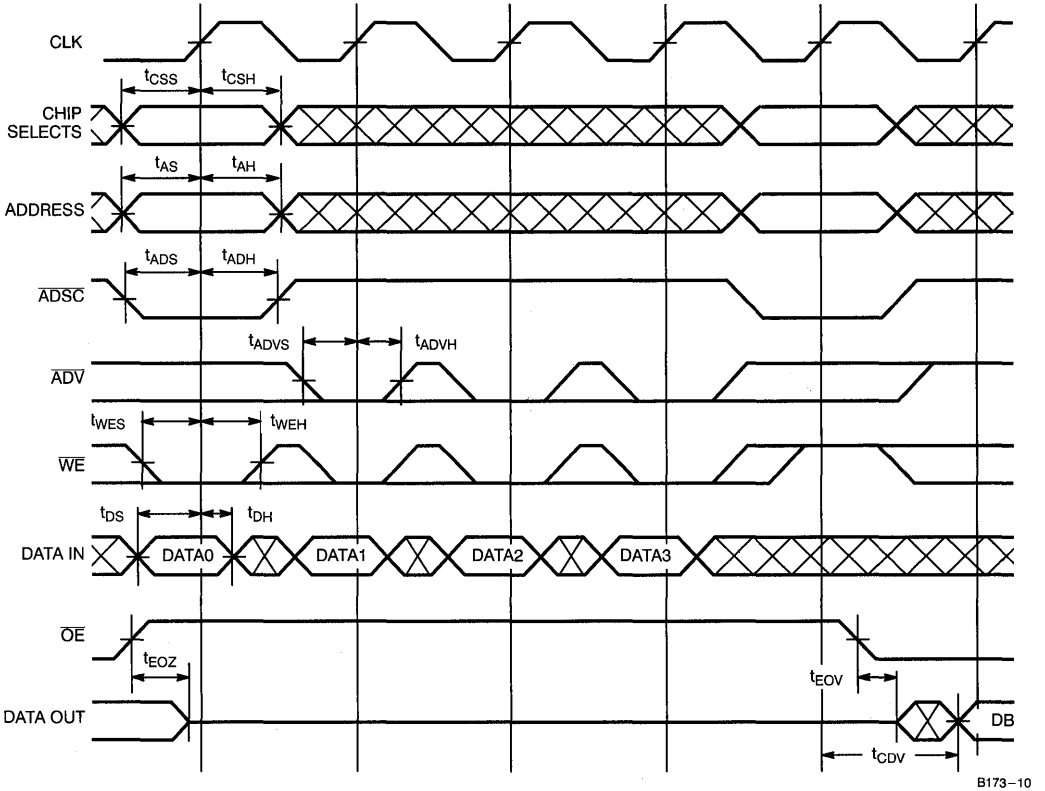


Burst Read Sequence with Four Accesses

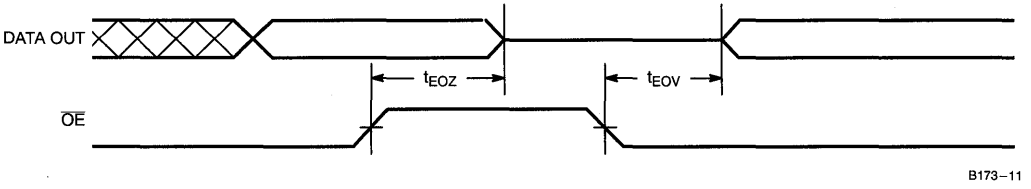


Switching Waveforms (continued)

Cache Controller Burst Write Sequence with Four Accesses Followed by a Single Read Cycle

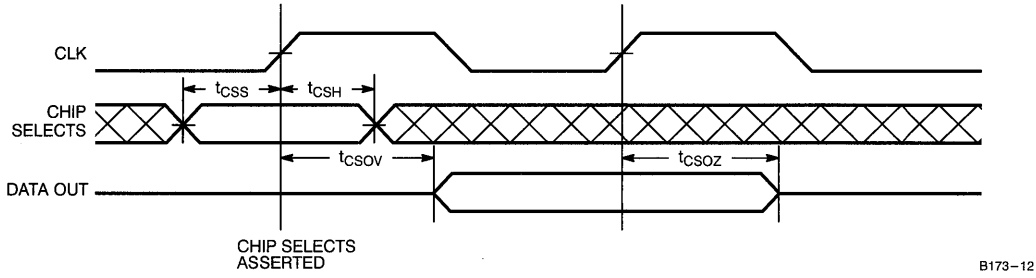


Output (Controlled by $\overline{OE}$)

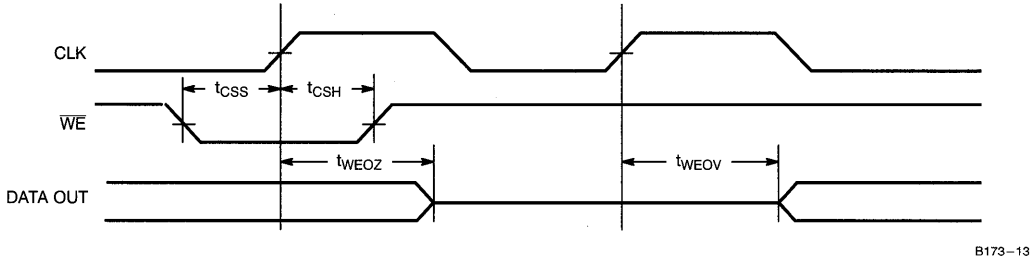


Switching Waveforms (continued)

Output Timing (Controlled by CS)



Output Timing (Controlled by $\overline{WE}$)



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7B173–14JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
18	CY7B173–18JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B173–18LC	L67	44-Square Leadless Chip Carrier	
	CY7B173–18LMB	L67	44-Square Leadless Chip Carrier	Military
21	CY7B173–21JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B173–21LC	L67	44-Square Leadless Chip Carrier	
	CY7B173–21LMB	L67	44-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7B174–14JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
18	CY7B174–18JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B174–18LC	L67	44-Square Leadless Chip Carrier	
	CY7B174–18LMB	L67	44-Square Leadless Chip Carrier	Military
21	CY7B174–21JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B174–21LC	L67	44-Square Leadless Chip Carrier	
	CY7B174–21LMB	L67	44-Square Leadless Chip Carrier	Military

Document #: 38–00154–B

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7B173A
CY7B174A

32K x 9 Synchronous Cache R/W RAM

Features

- **Supports 66-MHz Pentium™ CPU cache systems**
- **Available in standard PLCC/LCC**
- **BiCMOS for optimum speed/power**
- **7.5-ns access delay (clock to output) with 0 pF**
- **9-ns access delay (clock to output) with 85 pF**
- **Two-bit wraparound counter supporting the i486/Pentium microprocessor burst sequence (7B173A)**
- **Two-bit wraparound counter supporting the linear burst sequence (7B174A)**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Internal clamp diodes**
- **Direct interface with the processor and external cache controller**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable**
- **JEDEC-standard 44-pin PLCC pinout**

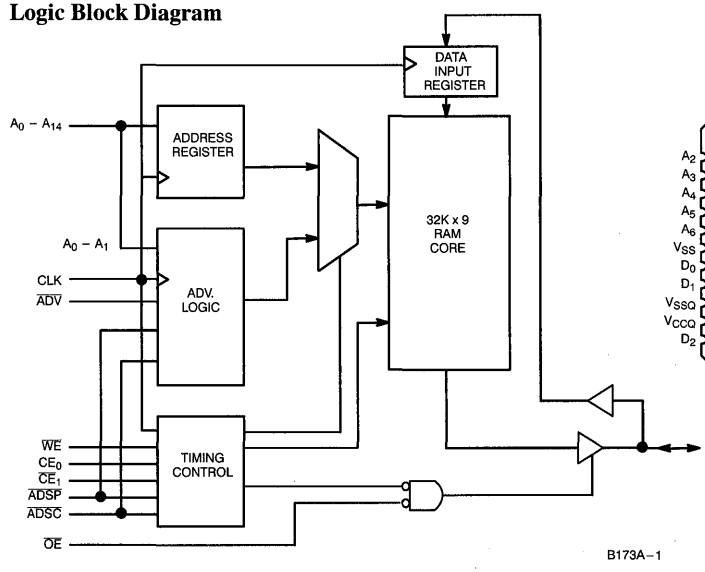
Functional Description

The CY7B173A and CY7B174A are 32K by 9 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. A two-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7B173A is designed for Intel i486 and Pentium microprocessor–based systems; its counter follows the burst sequence of the i486 and Pentium microprocessors. The CY7B174A is architected for other processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

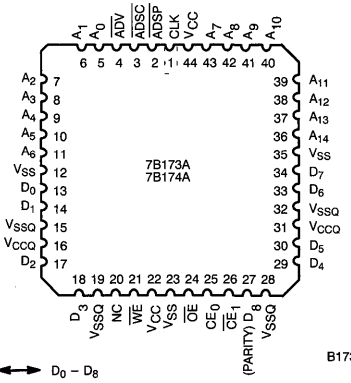
A synchronous self-timed write mechanism is provided to simplify the write interface. Two complementary synchronous chip select inputs are provided to support two banks of memory (256 Kbytes) with no external logic. These signals, in conjunction with the asynchronous output enable ($\overline{OE}$) signal, greatly simplify memory bank selection. The I/O and ADDR pins have internal clamp diodes to prevent overshoot and undershoot. The part is available in PLCC/LCC packages.

Logic Block Diagram



Pin Configuration

LCC/PLCC
Top View



Selector Guide

		7B173A–9 7B174A–9	7B173A–10 7B174A–10	7B173A–14 7B174A–14
Maximum Access Time (ns)		7.5	8.5	11.5
Maximum Operating Current (mA)	Commercial	210	210	180
	Military			250

Pentium is a trademark of Intel Corporation.

Functional Description (continued)

Single-Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE}_1$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B173A and CY7B174A will be pulled LOW before the next clock rise.

If $\overline{WE}$ is LOW at the next clock rise, information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Because the CY7B173A and CY7B174A are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single-Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at the rising edge of the clock: (1) CE_0 = 1 and $\overline{CE}_1$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$-triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. Information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Since the CY7B173A and CY7B174A are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

Single-Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE}_1$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at D_0 through D_8 a maximum of 14 ns after clock rise.

Burst Sequences

The CY7B173A provides a two-bit wraparound counter implementing the Intel 80486/Pentium sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

Table 1. Counter Implementation for the Intel 80486/Pentium Sequence

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

The CY7B174A provides a two-bit wraparound counter implementing a linear sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	1	1	0

Application Example

Figure 1 shows a 128-Kbyte secondary cache for the i486 using four CY7B173A cache RAMs and a CY7B181 cache tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 10 ns. This same arrangement can be used with the Pentium processor.

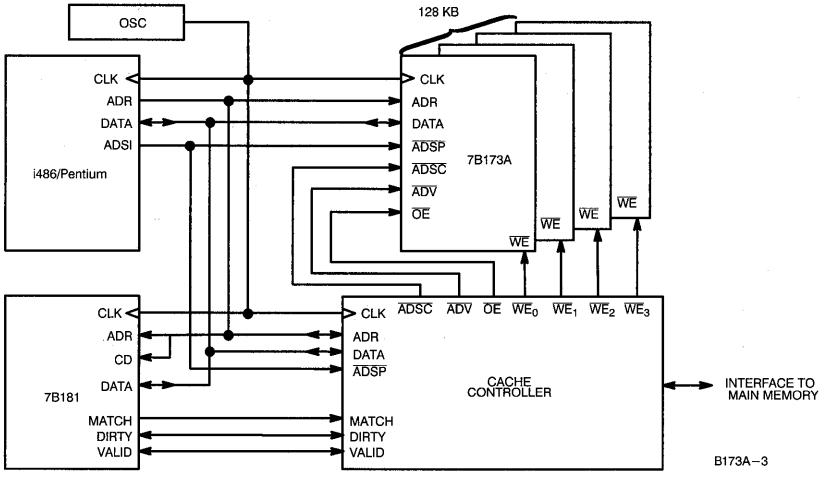


Figure 1. Cache Using Four CY7B173As

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{14}$	I	Address Inputs
CLK	I	Clock
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable
CE_0, $\overline{CE_1}$	I	Chip Enables
$\overline{ADV}$	I	Address Advance
$\overline{ADSP}$	I	Processor Address Strobe
$\overline{ADSC}$	I	Cache Controller Address Strobe
$D_0 - D_8$	I/O	Data I/O
V_{CC}	–	+5V Power Supply
V_{SS}	–	Ground
V_{CCQ}	–	Output Buffer (Driver) Power Supply
V_{SSQ}	–	Output Buffer (Driver) Ground
NC	–	Not Connected Internally

Pin Descriptions

Input Signals	
CLK	Clock signal used as the reference for most on-chip operations.
$\overline{ADSP}$	Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at A_0 through A_{14} will be loaded into the address register and the address advancement logic. The write signal, $\overline{WE}$, is ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$\overline{ADSC}$	Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B173A/4A. The write signal, $\overline{WE}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$A_0 - A_{14}$	Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations.
$\overline{WE}$	Write Enable: This signal is sampled at the rising edge of the clock signal. If $\overline{WE}$ = 0, a self-timed write operation will be initiated and data on $D_0 - D_8$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$ and $\overline{WE}$ are LOW at clock rise. In this case, the write signal is ignored.
$\overline{ADV}$	Address Advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B173A, LOW at this input will advance the address in the advancement logic according to the Intel 80486 burst sequence. In the case of the CY7B174A, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW).
$CE_0 - \overline{CE_1}$	Chip Enable inputs: CE_0 is active HIGH and $\overline{CE_1}$ is active LOW. Both inputs are sampled at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The RAM is selected if CE_0 = 1 and $\overline{CE_1}$ = 0.
$\overline{OE}$	Output Enable: $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B173A/4A is a common I/O device and three-state conflict may occur at the data pins.
NC	Not connected internally: Can be left open or tied to V_{SS} or V_{CC}.
Bidirectional Signals	
$D_0 - D_8$	Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WE}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B173A−9, 10 7B174A−9, 10 Min.	7B173A−9, 10 7B174A−9, 10 Max.	7B173A−14 7B174A−14 Min.	7B173A−14 7B174A−14 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+1	− 1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		210		180	mA
			Mil				250	
I_{SB1}	AC Standby Current	CE_0, $\overline{CE_1}$ = V_{IH}, I_{OUT} = 0 mA, All Inputs= V_{IL} or V_{IH}, V_{IL}=0.0V and V_{IH} ≥ 3.0V, Cycle Time ≥ t_{CYC} Min.			50		40	mA
I_{SB2}	CMOS Standby Current	CE_0, $\overline{CE_1}$ ≥ V_{CC} −0.2V, All Inputs=V_{CC} −0.2V or ≤ 0.2V, Cycle Time ≥ t_{CYC} Min.			40		30	mA

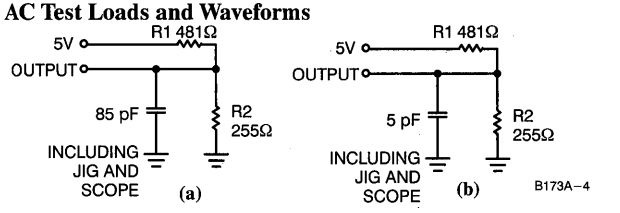
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	3.5	pF
C_{IN}: Other Inputs			4	pF
C_{OUT}	Output Capacitance		5.5	pF

Notes:

1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

AC Test Loads and Waveforms



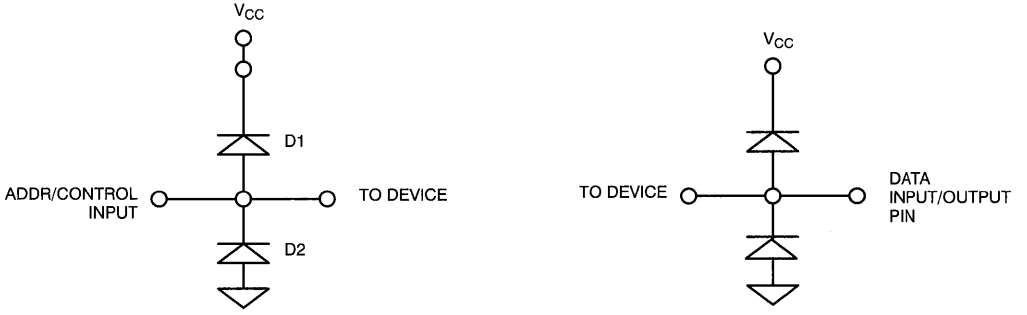
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7B173A–9 7B174A–9		7B173A–10 7B174A–10		7B173A–14 7B173A–14		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		16.6		20		ns
f_{MAX}	Maximum Frequency		66		60		50	MHz
t_{CH}	Clock HIGH	4		5		7		ns
t_{CL}	Clock LOW	4		5		7		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		1		ns
t_{CDV1}	Data Output Valid After CLK Rise (0-pF Load)		7.5		8.5		11.5	ns
t_{CDV2}	Data Output Valid After CLK Rise (85-pF Load)		9		6		13.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CES}	Chip Enable Set-Up	2.5		2.5		3		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		1		ns
t_{CEOZ}	Chip Enable Sampled to Output High Z[6, 7]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		6		6		7	ns
t_{WEOZ}	$\overline{WE}$ Sampled LOW to Output High Z[6]		6		6		7	ns
t_{WEOV}	$\overline{WE}$ Sampled HIGH to Output Valid		9		9		13.5	ns

Notes:

5. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
6. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given voltage and temperature, t_{CSOZ} (t_{WEOZ}) min. is less than t_{CSOV} (t_{WEOV}) min.

Input/Output ESD and Clamp Diode Protection

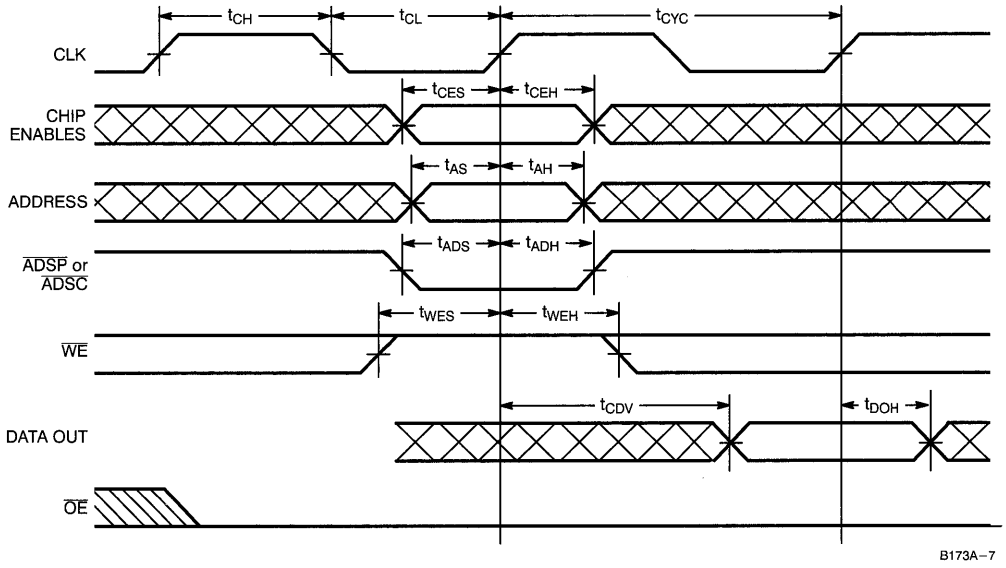


(a) Input ESD and Clamp Diode **(b) Input/Output ESD and Clamp Diode**

B173A–6

Switching Waveforms

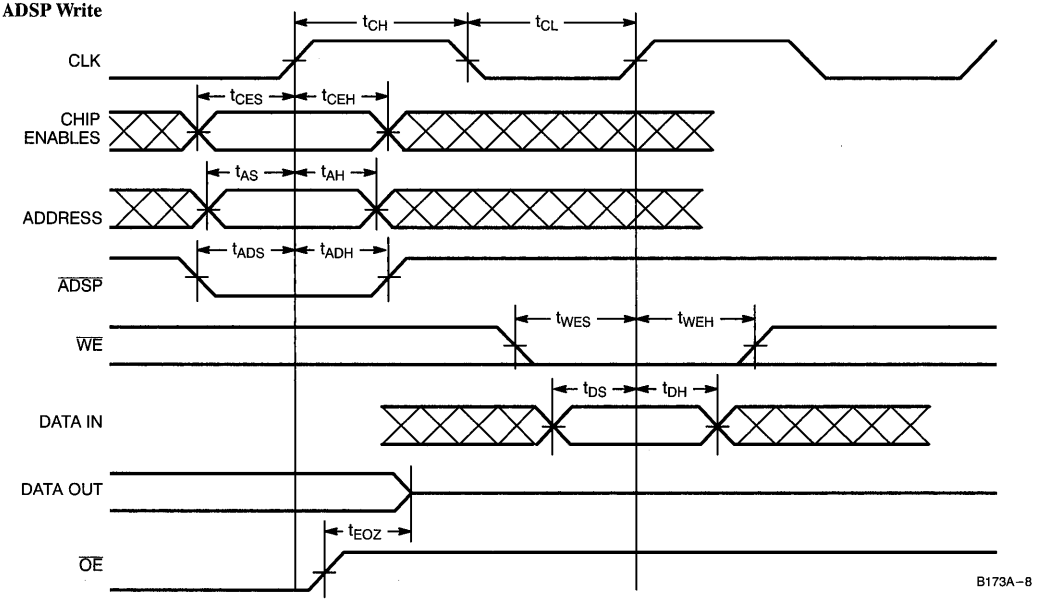
Single Read



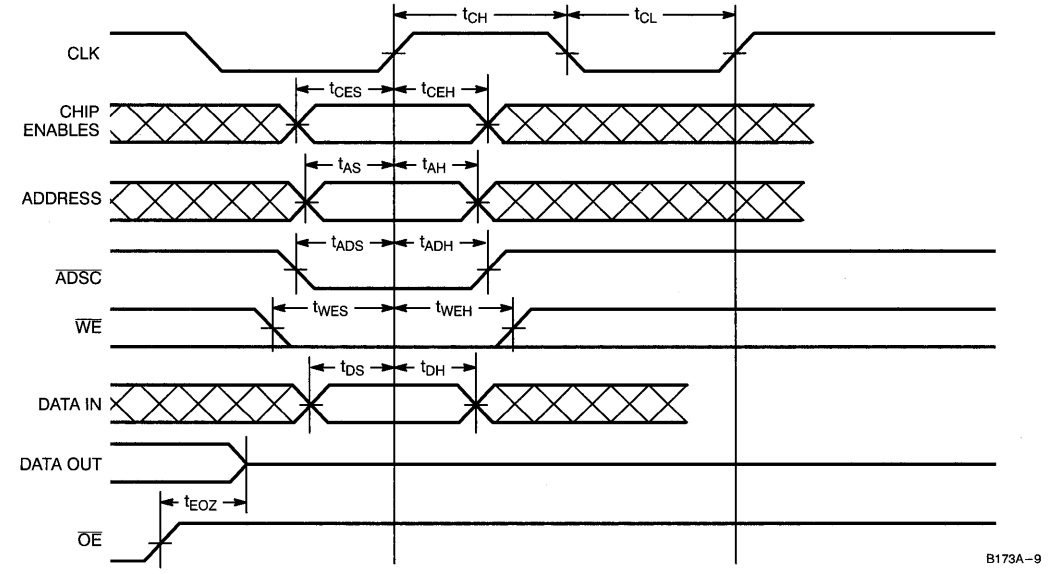
B173A–7

Switching Waveforms (continued)

ADSP Write

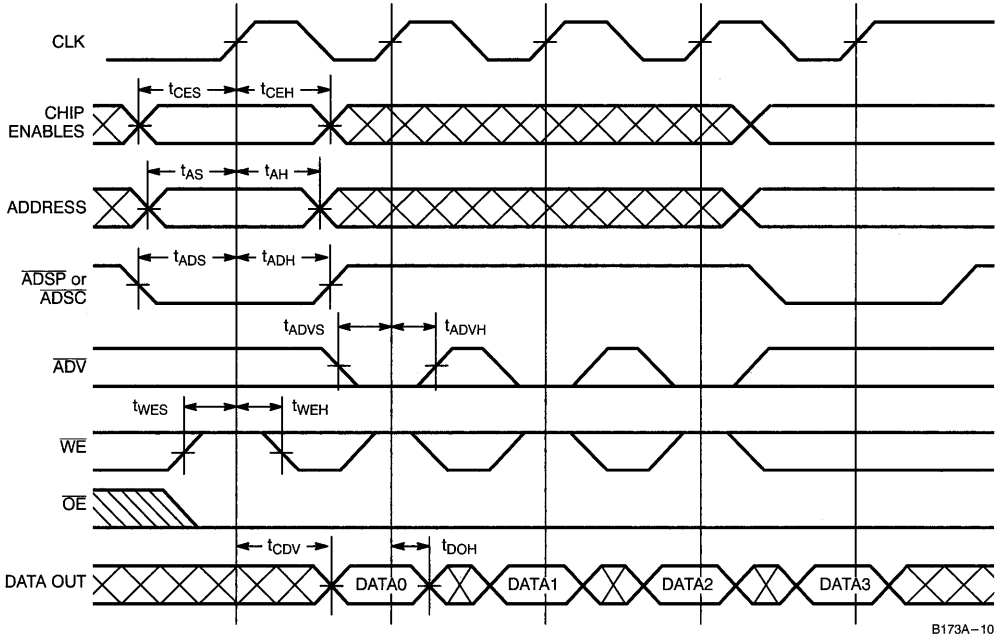


Single Cache Controller Write



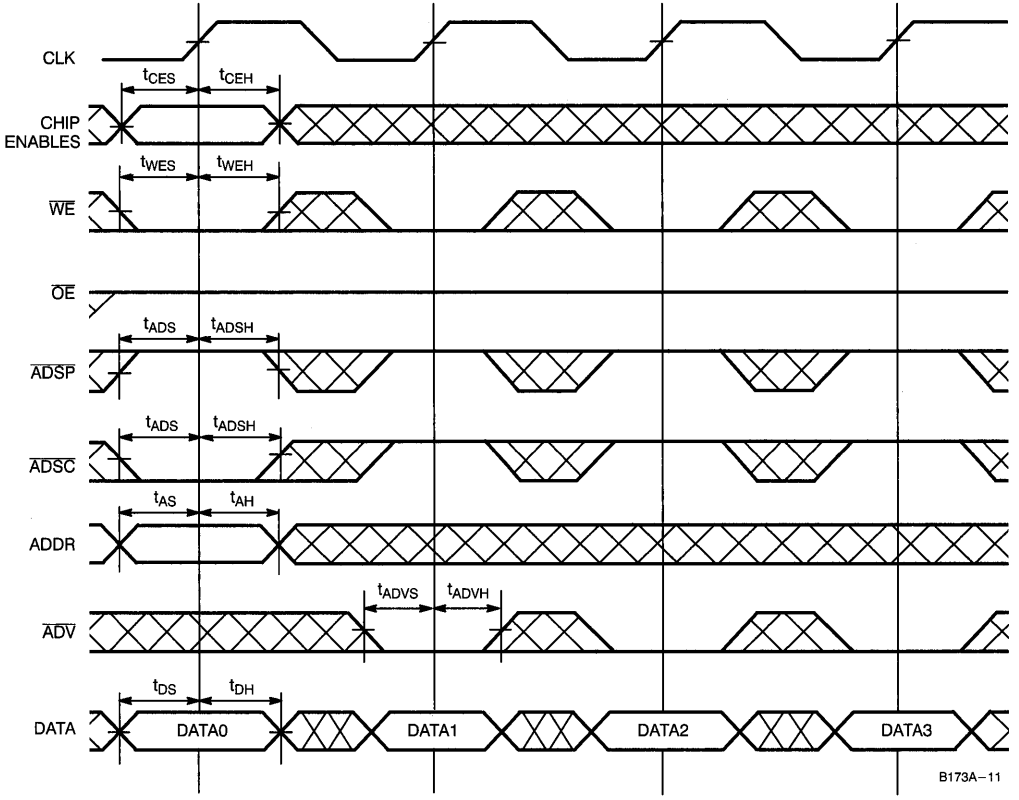
Switching Waveforms (continued)

Burst Read Sequence with Four Accesses

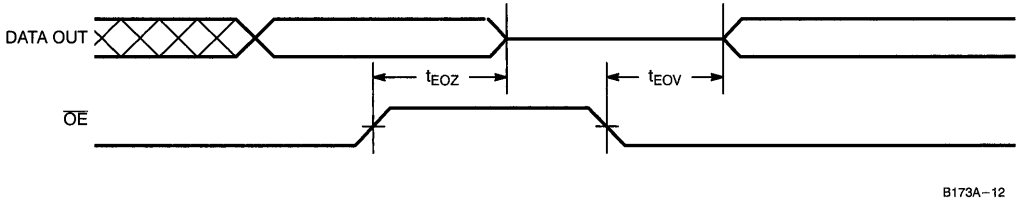


Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSC}$

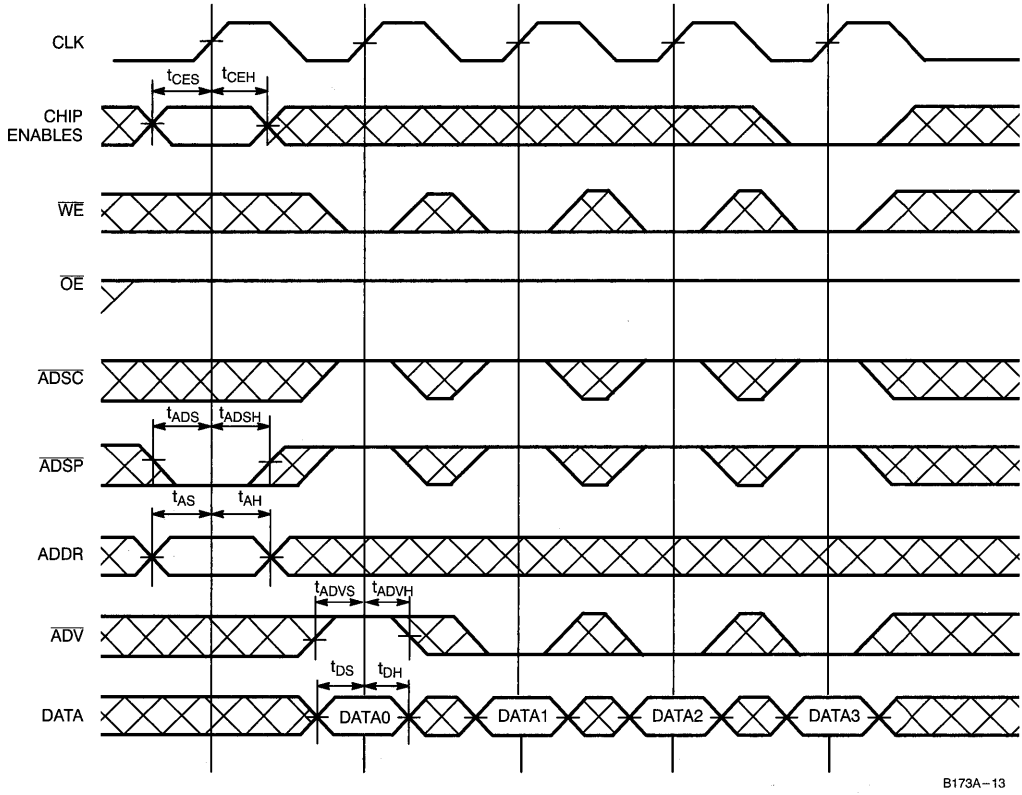


Output (Controlled by $\overline{OE}$)



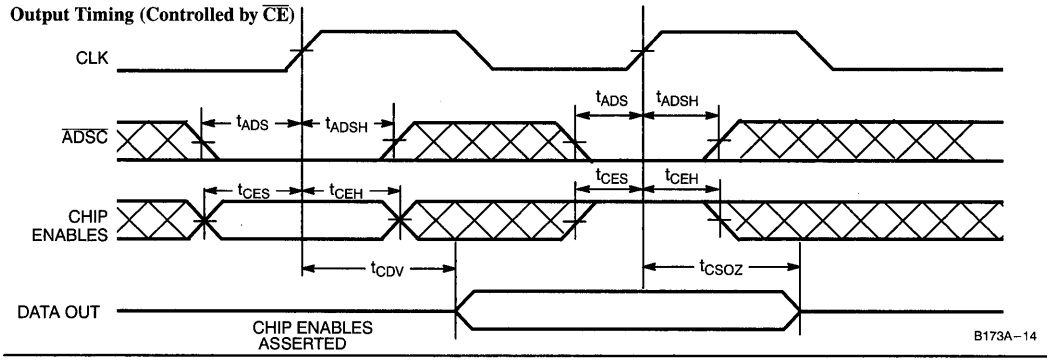
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

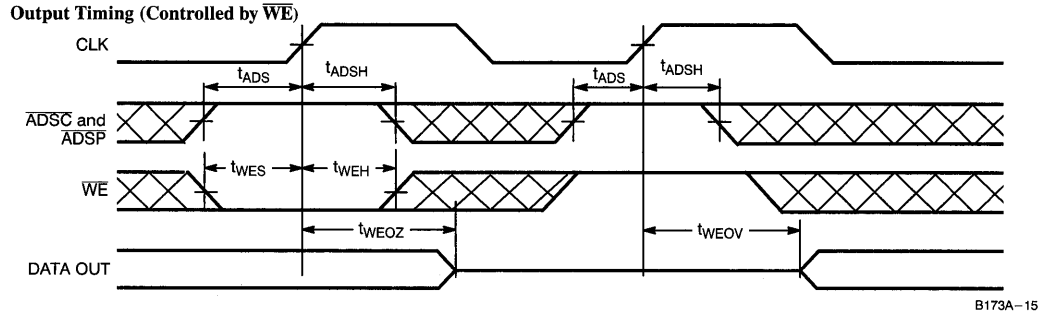


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CE}$)



Output Timing (Controlled by $\overline{WE}$)



Synchronous Truth Table[8, 9, 10, 11]

Inputs						Address	Mode
E	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K		
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

Asynchronous Truth Table[8, 12]

$\overline{E}$ Input	Input/Output	Mode
L	Data Out (DQ_0 – DQ_8)	Read
H	High Z	Read
X	High Z, Data In (DQ_0 – DQ_8)	Write
X	High Z	Deselected

Notes:

8. X means Don't Care.
9. All inputs except $\overline{E}$ must meet set-up and hold times for the low-to-high transition of clock (K).
10. E represents CE_0 and $\overline{CE}_1$. T inplies $\overline{CE}_1$ = L and CE_0 = H; F implies $\overline{CE}_1$ = H or CE_0 = L.
11. Wait states are inserted by suspending burst.
12. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time and held HIGH through the input data hold time.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
9	CY7B173A–9JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
10	CY7B173A–10JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
14	CY7B173A–14JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B173A–14LC	L67	44-Square Leadless Chip Carrier	
	CY7B173A–14LMB	L67	44-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
9	CY7B174A–9JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
10	CY7B174A–10JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
14	CY7B174A–14JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B174A–14LC	L67	44-Square Leadless Chip Carrier	
	CY7B174A–14LMB	L67	44-Square Leadless Chip Carrier	Military

Document #: 38–00042–B

CYPRESS SEMICONDUCTOR

32K x 9 Synchronous Pentium™ CPU Cache R/W RAM

Features

- **Supports 66-MHz Pentium CPU cache systems**
- **Supports zero-wait-state performance**
- **7.5-ns access delay (clock to output) with 0 pF**
- **9-ns access delay (clock to output) with 85 pF**
- **Allows Pentium CPU address pipelining**
- **Available in PQFP with 25-Mil lead pitch and standard PLCC/LCC**
- **BiCMOS for optimum speed/power**
- **Two-bit wraparound counter supporting the Pentium microprocessor burst sequence**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Internal clamp diodes**
- **Direct interface with the processor and external cache controller**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable**
- **JEDEC-standard 44-pin PLCC pinout**

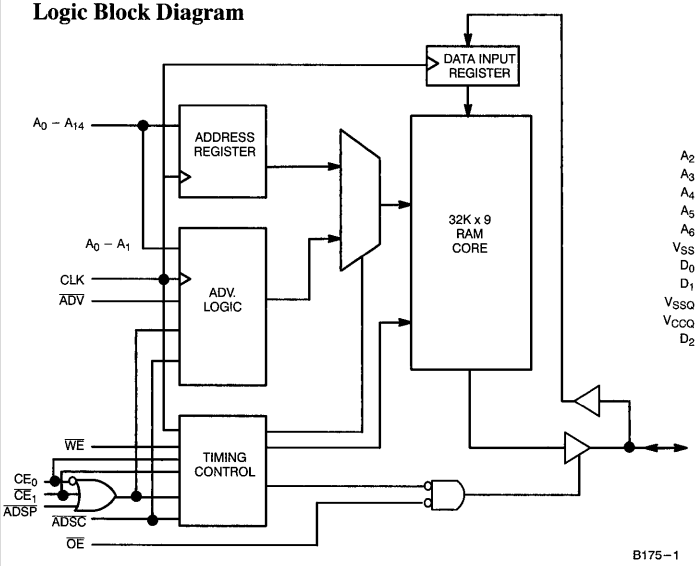
Functional Description

The CY7B175 is a 32K by 9 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. A two-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7B175 is designed for Intel Pentium microprocessor–based systems; its counter follows the burst sequence of the Pentium microprocessor. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

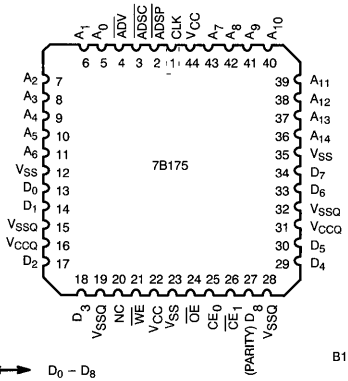
A synchronous self-timed write mechanism is provided to simplify the write interface. Two complementary synchronous chip select inputs are provided to support two banks of memory (256 Kbytes) with no external logic. These signals, in conjunction with the asynchronous output enable ($\overline{OE}$) signal, greatly simplify memory bank selection. The I/O and ADDR pins have internal clamp diodes to prevent overshoot and undershoot. The part is available in the very small outline plastic quad flat pack (PQFP) and PLCC/LCC packages.

Logic Block Diagram



Pin Configuration

LCC/PLCC/PQFP
Top View



Selector Guide

		7B175–7	7B175–8	7B175–11
Maximum Access Time (ns)		7.5	8.5	11.5
Maximum Operating Current (mA)	Commercial	210	210	210
	Military			250

Pentium is a trademark of Intel Corporation.

Functional Description (continued)

Single-Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE_1}$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B175 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if CE_0 = 0 or $\overline{CE_1}$ = 1.

If $\overline{WE}$ is LOW at the next clock rise, information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Because the CY7B175 is a common I/O device, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single-Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at the rising edge of the clock: (1) CE_0 = 1 and $\overline{CE_1}$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$-triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. Information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Since the CY7B175 is a common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

Single-Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE_1}$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at D_0 through D_8 a maximum of 14 ns after clock rise. $\overline{ADSP}$ is ignored if CE_0 = 0 or $\overline{CE_1}$ = 1.

Burst Sequences

The CY7B175 provides a two-bit wraparound counter implementing the Intel Pentium sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

Table 1. Counter Implementation for the Intel Pentium Sequence

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

Application Example

Figure 1 shows a 256-Kbyte secondary cache for the Pentium microprocessor using eight CY7B175 cache RAMs and a CY7B181 cache tag. Address from the Pentium CPU is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 10 ns.

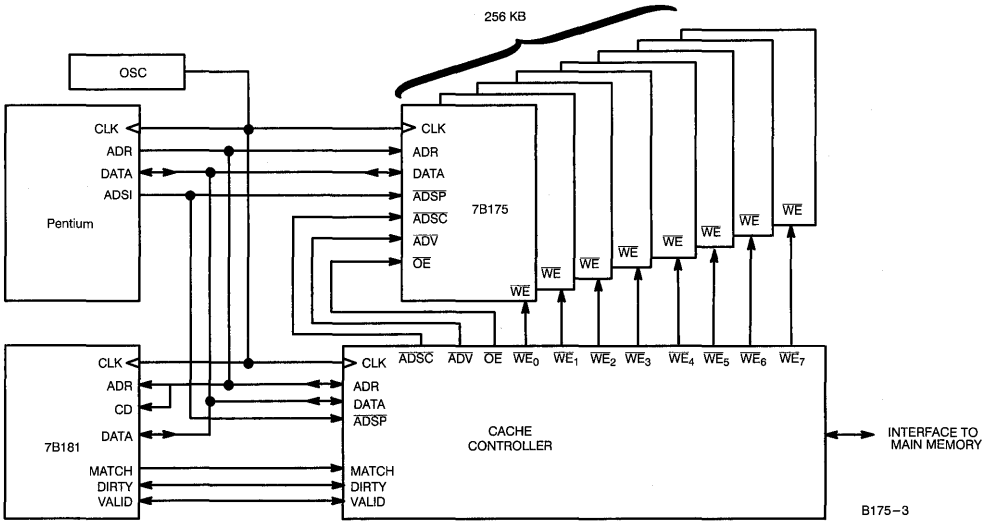


Figure 1. Cache Using Eight CY7B175s

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{14}$	I	Address Inputs
CLK	I	Clock
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable
CE_0, $\overline{CE_1}$	I	Chip Enables
$\overline{ADV}$	I	Address Advance
$\overline{ADSP}$	I	Processor Address Strobe
$\overline{ADSC}$	I	Cache Controller Address Strobe
$D_0 - D_8$	I/O	Data I/O
V_{CC}	–	+5V Power Supply
V_{SS}	–	Ground
V_{CCQ}	–	Output Buffer (Driver) Power Supply
V_{SSQ}	–	Output Buffer (Driver) Ground
NC	–	Not Connected Internally

Pin Descriptions

Input Signals	
CLK	Clock signal used as the reference for most on-chip operations.
$\overline{ADSP}$	Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at A_0 through A_{14} will be loaded into the address register and the address advancement logic. The write signal, $\overline{WE}$, is ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized. $\overline{ADSP}$ is ignored when $CE_0 = 0$ or $\overline{CE_1} = 1$.
$\overline{ADSC}$	Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B175/4A. The write signal, $\overline{WE}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$A_0 - A_{14}$	Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations.
$\overline{WE}$	Write Enable: This signal is sampled at the rising edge of the clock signal. If $\overline{WE} = 0$, a self-timed write operation will be initiated and data on $D_0 - D_8$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$ and $\overline{WE}$ are LOW at clock rise. In this case, the write signal is ignored.
$\overline{ADV}$	Address Advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B175, LOW at this input will advance the address in the advancement logic according to the Intel 80486 burst sequence. In the case of the CY7B174A, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW).
$CE_0 - \overline{CE_1}$	Chip Enable inputs: CE_0 is active HIGH and $\overline{CE_1}$ is active LOW. If $CE_0 = 0$, $\overline{CE_1} = 1$ and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $CE_0 = 1$, $\overline{CE_1} = 0$ and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $CE_0 = 0$ or $\overline{CE_0} = 1$, $\overline{ADSP}$ is ignored.
$\overline{OE}$	Output Enable: $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B175/4A is a common I/O device and three-state conflict may occur at the data pins.
NC	Not connected internally: Can be left open or tied to V_{SS} or V_{CC}.
Bidirectional Signals	
$D_0 - D_8$	Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WE}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B175−7, 8 Min.	7B175−7, 8 Max.	7B175−11 Min.	7B175−11 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1.0	+1.0	− 1.0	+1.0	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		210		210	mA
			Mil				250	
I_{SB1}	AC Standby Current	CE_0, $\overline{CE_1}$ = V_{IH}, I_{OUT} = 0 mA, All Inputs= V_{IL} or V_{IH}, V_{IL}=0.0V and V_{IH}≥3.0V, Cycle Time ≥ t_{CYC} Min.			50		50	mA
I_{SB2}	CMOS Standby Current	CE_0, $\overline{CE_1}$ ≥ V_{CC} −0.2V, All Inputs=V_{CC} −0.2V or ≤ 0.2V, Cycle Time ≥ t_{CYC} Min.			40		40	mA

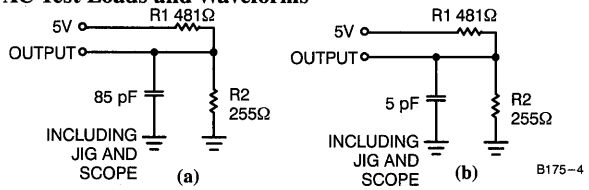
Capacitance[4]

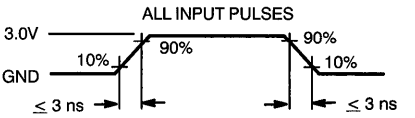
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	3.5	pF
C_{IN}: Other Inputs			4	pF
C_{OUT}	Output Capacitance		5.5	pF

Notes:

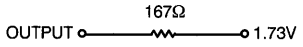
1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



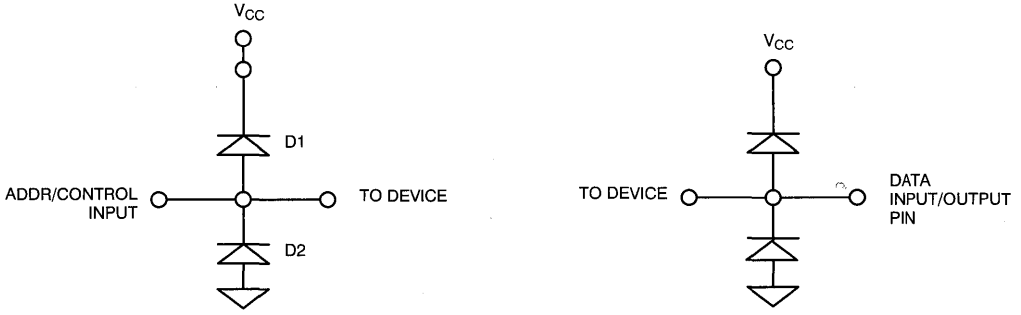
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7B175–7		7B175–8		7B175–11		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		16.6		20		ns
f_{MAX}	Maximum Frequency		66		60		50	MHz
t_{CH}	Clock HIGH	4		5		7		ns
t_{CL}	Clock LOW	4		5		7		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV1}	Data Output Valid After CLK Rise (0-pF Load)		7.5		8.5		11.5	ns
t_{CDV2}	Data Output Valid After CLK Rise (85-pF Load)		9		10		13.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CES}	Chip Enable Set-Up	2.5		2.5		3		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		1		ns
t_{CEOZ}	Chip Enable Sampled to Output High Z[6, 7]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		6		6		6	ns
t_{WEOZ}	$\overline{WE}$ Sampled LOW to Output High Z[6]		6		6		7	ns
t_{WEOV}	$\overline{WE}$ Sampled HIGH to Output Valid		9		10		13.5	ns

Notes:

5. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
6. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given voltage and temperature, t_{CSOZ} (t_{WEOZ}) min. is less than t_{CSOV} (t_{WEOV}) min.

Input/Output ESD and Clamp Diode Protection

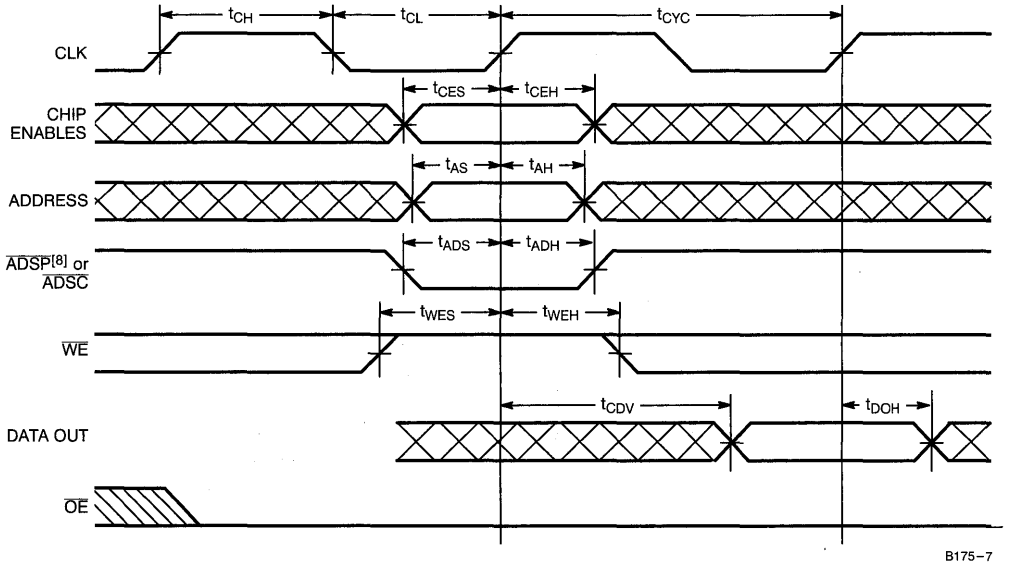


(a) Input ESD and Clamp Diode **(b) Input/Output ESD and Clamp Diode**

B175–6

Switching Waveforms

Single Read

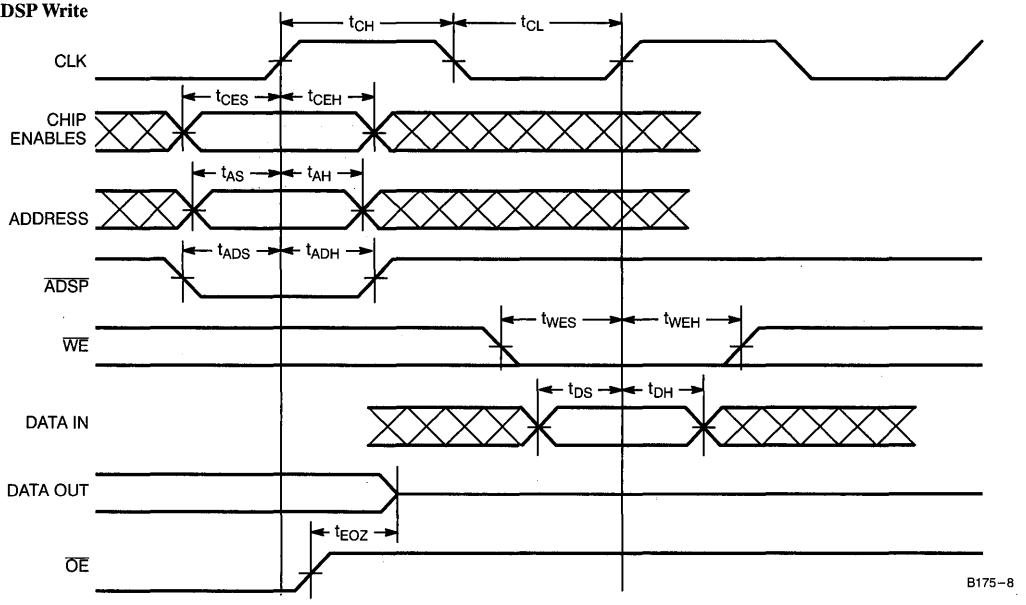


B175–7

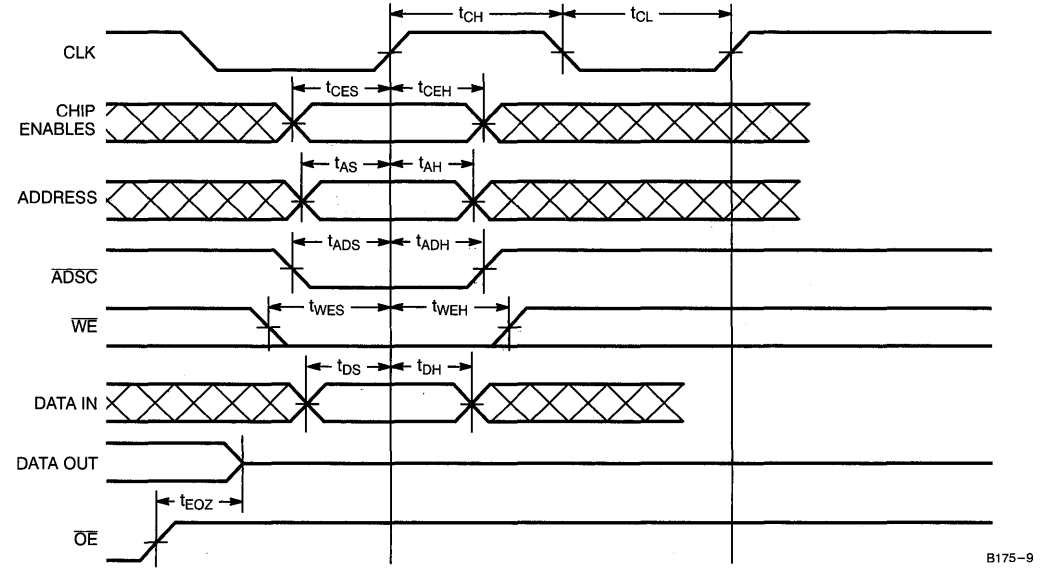
Note:
8. If $\overline{ADSP}$ is asserted while $CE_0 = 0$ or $\overline{CE}_0 = 1$, $\overline{ADSP}$ will be ignored.

Switching Waveforms (continued)

ADSP Write

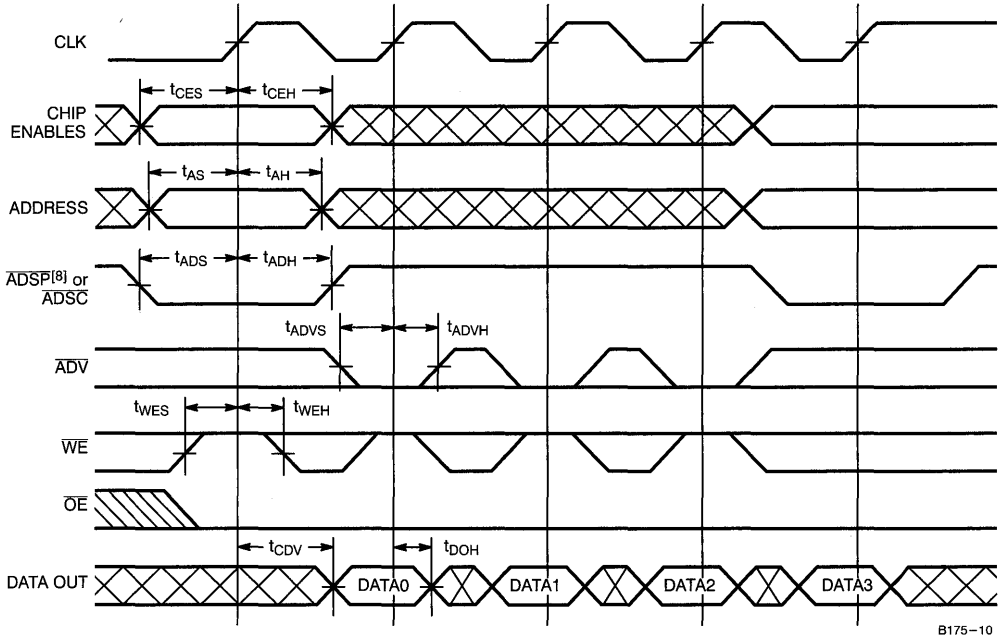


Single Cache Controller Write



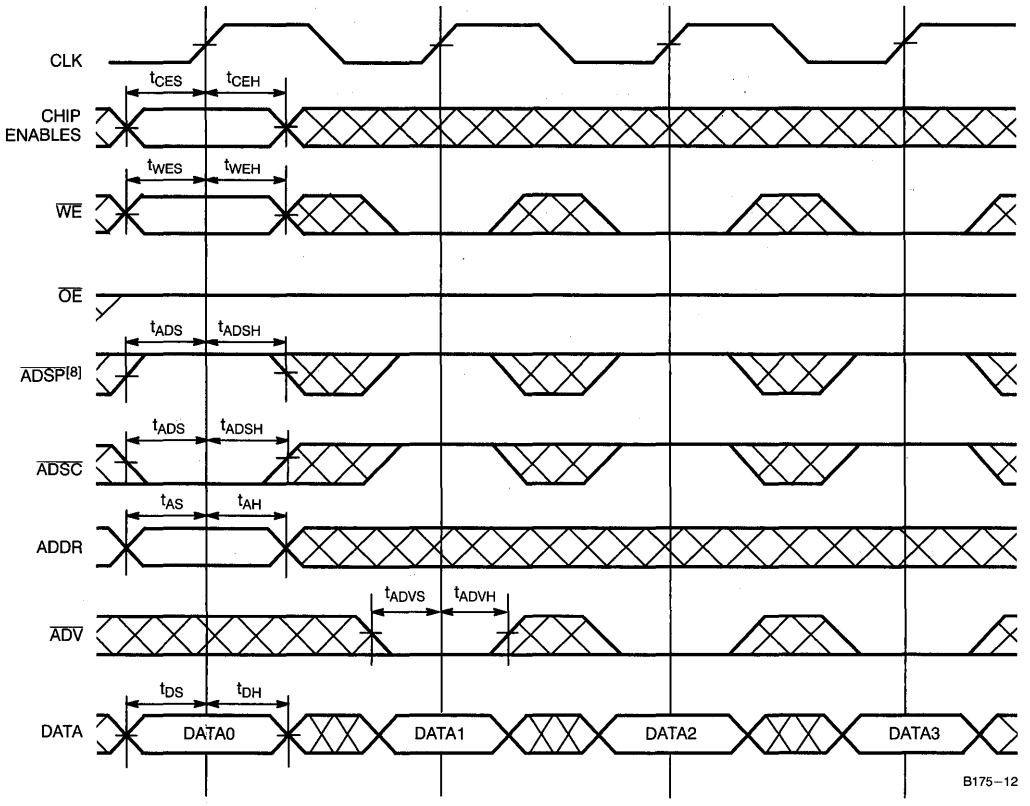
Switching Waveforms (continued)

Burst Read Sequence with Four Accesses

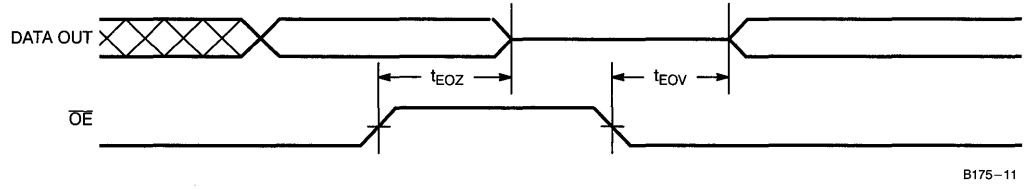


Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSC}$

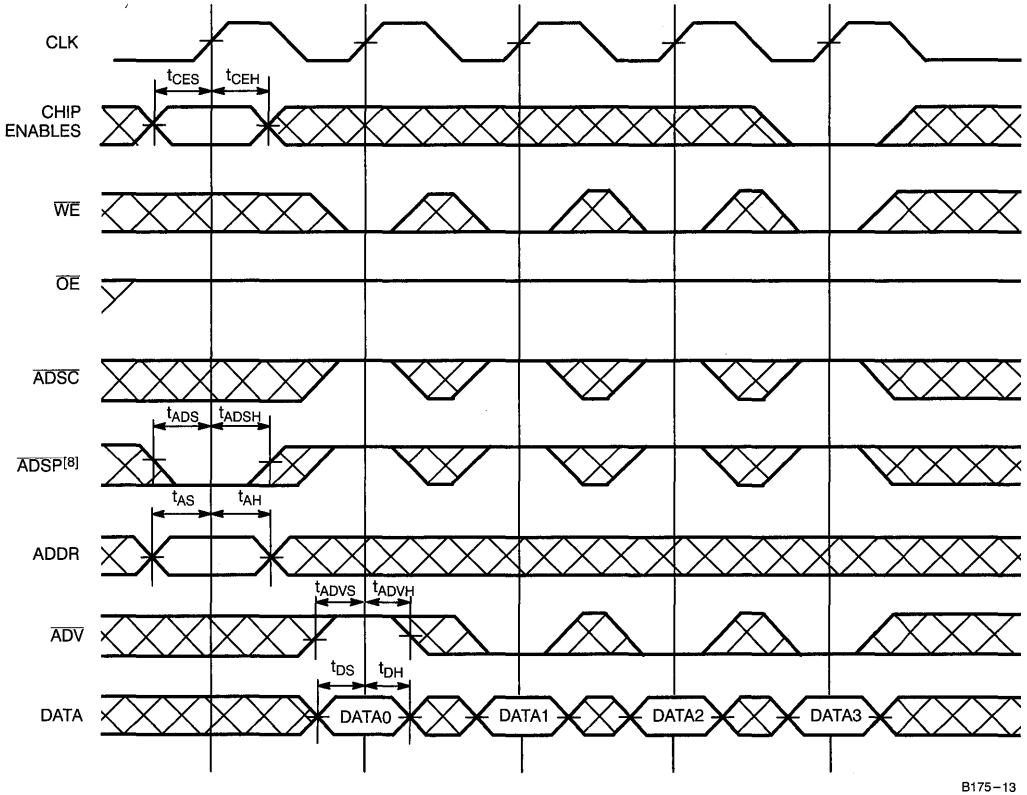


Output (Controlled by $\overline{OE}$)

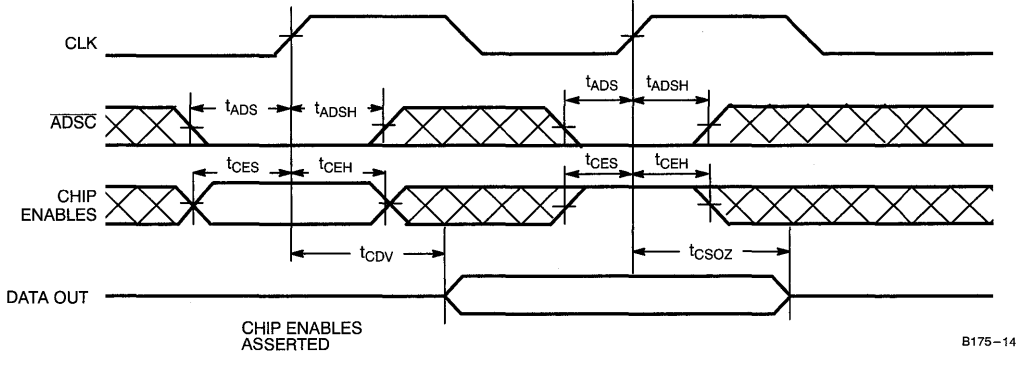


Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

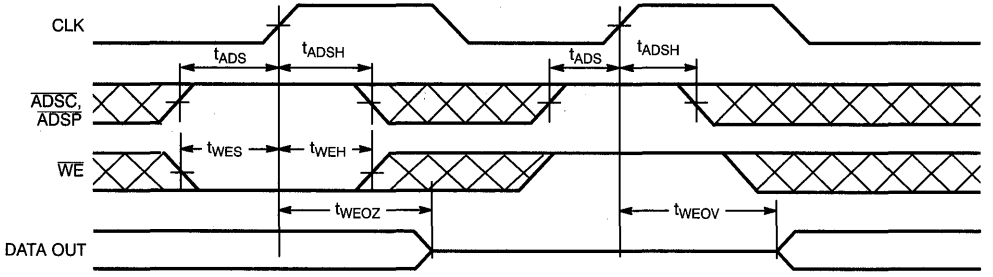


Output Timing (Controlled by CE_0 and $\overline{CE_1}$)



Switching Waveforms (continued)

Output Timing (Controlled by $\overline{WE}$)



Synchronous Truth Table[9, 10, 11, 12]

Inputs						Address	Mode
E	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K		
F	X	L	X	X	L-H	N/A	Deselected
F	L	H	H	H	L-H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
F	L	H	L	H	L-H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
F	L	H	H	L	L-H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
F	L	H	L	L	L-H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
T	L	X	X	X	L-H	External address	Read cycle, begin burst
T	H	L	X	L	L-H	External address	Write cycle, begin burst
T	H	L	X	H	L-H	External address	Read cycle, begin burst
X	H	H	L	L	L-H	Next address	Write cycle, continue burst
X	H	H	L	H	L-H	Next address	Read cycle, continue burst
X	H	H	H	L	L-H	Current address	Write cycle, suspend burst
X	H	H	H	H	L-H	Current address	Read cycle, suspend burst

Asynchronous Truth Table[9, 11, 13]

E	Input/Output	Mode
T	Data Out (DQ_0 – DQ_8)	Read
F	High Z	Read
X	High Z, Data In (DQ_0 – DQ_8)	Write
X	High Z	Deselected

Notes:

9. X means Don't Care.
10. All inputs except $\overline{E}$ must meet set-up and hold times for the low-to-high transition of clock (K).
11. E represents CE_0 and $\overline{CE}_1$. T inplies $\overline{CE}_1$ = L and CE_0 = H; F implies $\overline{CE}_1$ = H or CE_0 = L.
12. Wait states are inserted by suspending burst.
13. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time and held high through the input data hold time.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7.5	CY7B175–7JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–7NC	N67	TBD	
8.5	CY7B175–8JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–8NC	N67	TBD	
11.5	CY7B175–11JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–11NC	N67	TBD	
	CY7B175–11LC	L67	44-Square Leadless Chip Carrier	
	CY7B175–11LMB	L67	44-Square Leadless Chip Carrier	Military

Document #: 38–A–00043

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C178
CY7C179

32K x 18 Synchronous Cache RAM

Features

- **Supports 66-MHz Pentium™ microprocessor cache systems with zero wait states**
- **32K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 8.5 ns with 0-pF load**
  - **— 10 ns with 85-pF load**
- **Two-bit wraparound counter supporting Pentium and 486 burst sequence (7C178)**
- **Two-bit wraparound counter supporting linear burst sequence (7C179)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **I/Os capable of 3.3V operation**
- **Industry-standard pinout**
- **52-pin PLCC and PQFP**

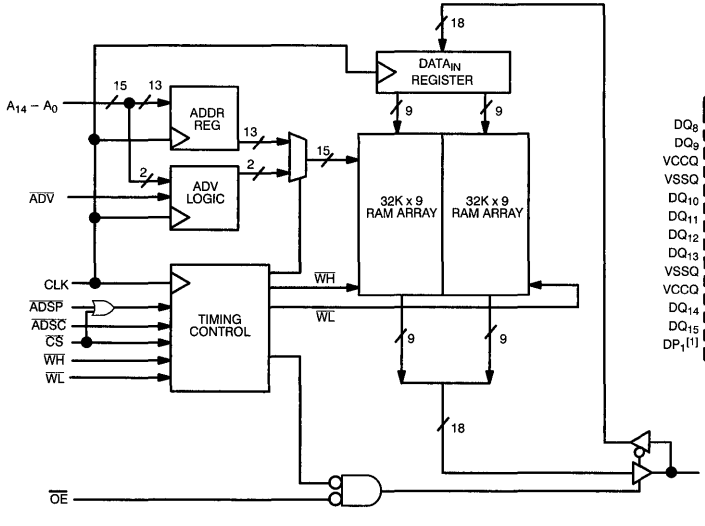
Functional Description

The CY7C178 and CY7C179 are 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C178 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C179 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



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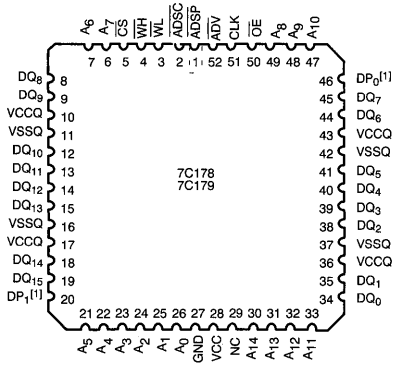
Pin Configuration

PLCC
Top View



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Selector Guide

		7C178–8 7C179–8	7C178–10 7C179–10	7C178–12 7C179–12
Maximum Access Time (ns) (0-pF Load)		8.5	10.5	12.5
Maximum Operating Current (mA)	Commercial	295	265	215
	Military			220

Shaded area contains advanced information.
Pentium is a trademark of Intel Corporation.

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_x.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C178 and CY7C179 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C178 and CY7C179 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. Since the CY7C178 and the CY7C179 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data and parity lines. As a safety precaution, the appropriate data and parity lines are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ are sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

Burst Sequences

The CY7C178 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor's address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C179 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 256-Kbyte secondary cache for the Pentium microprocessor using four CY7C178 cache RAMs.

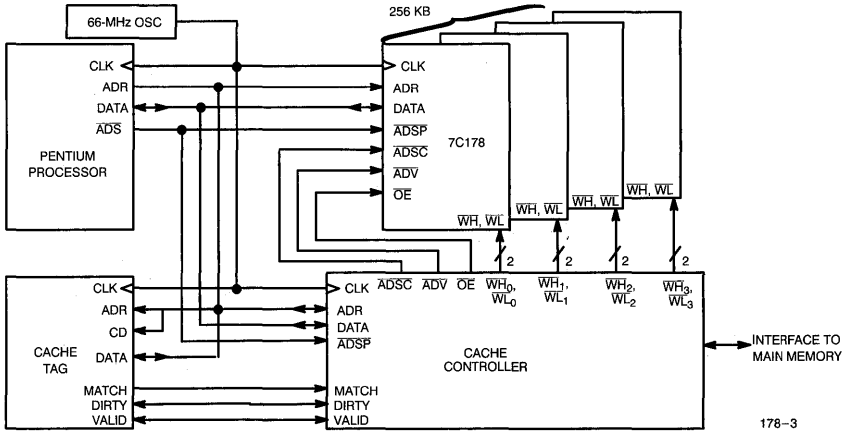


Figure 1. Cache Using Four CY7C178s

Pin Definitions

Signal Name	Type	# of Pins	Description
VCC	Input	1	+5V Power
VCCQ	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
VSSQ	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{14} - A_0$	Input	15	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CS}$, $\overline{WH}$, $\overline{WL}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A_{14}–A_0	I	Fifteen address lines used to select one of 32K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{14} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{14} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect of $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C179, the address will be incremented linearly. In the CY7C178, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$.. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ_{15}-DQ_0	I/O	Sixteen bidirectional data I/O lines. $DQ_{15} - DQ_8$ are inputs to and outputs from the high-order half of the RAM array, while $DQ_7 - DQ_0$ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. $DQ_{15} - DQ_8$ and $DQ_7 - DQ_0$ are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, is sampled LOW at clock rise.
DP_1–DP_0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as $DQ_{15} - DQ_0$, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}	V_{CCQ}
Com'l	0°C to +70°C	5V ± 5%	3.0V – 5.5V
Mil	– 55°C to +125°C	5V ± 5%	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	7C178–8 7C179–8		7C178–10 7C179–10		7C178–12 7C179–12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	1	–1	1	–1	1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	5	–5	5	–5	5	µA

Notes:

2. Minimum voltage equals – 2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page for Group A subgroup testing information.

Electrical Characteristics (continued)

Parameter	Description	Test Conditions		7C178–8 7C179–8 Min.	7C178–8 7C179–8 Max.	7C178–10 7C179–10 Min.	7C178–10 7C179–10 Max.	7C178–12 7C179–12 Min.	7C178–12 7C179–12 Max.	Unit
I_{OS}	Output Short Circuit Current [5]	V_{CC}=Max., V_{OUT}=GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX} =1/t_{RC}	Com'l		295		265		215	mA
			Mil						250	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		60		50		40	mA
			Mil						50	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f=0[6]	Com'l		20		20		20	mA
			Mil						20	

Shaded areas contain advanced information

Capacitance[7]

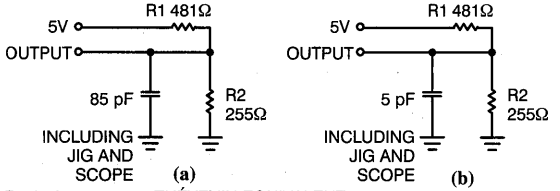
Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	Com'l	4	pF
			Mil	6	
C_{IN}: Other Inputs			Com'l	6	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	6	pF
			Mil	8	

Shaded areas contain advanced information

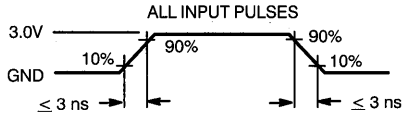
Notes:

5. Not more than one output should be shortened at one time. Duration of the short circuit should not exceed 30 seconds.
6. Clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

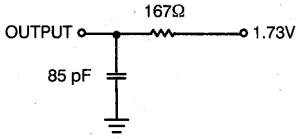


178–4



178–5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[8]

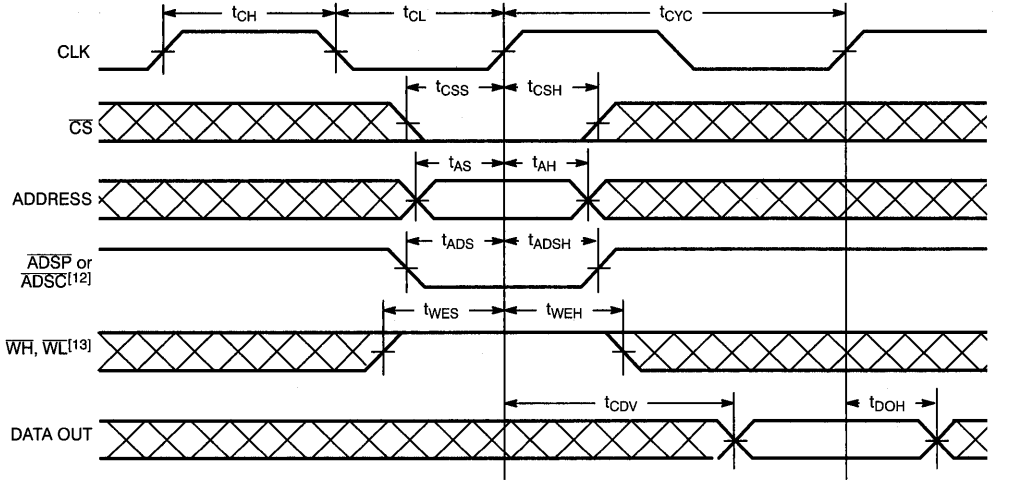
Parameter	Description	7C178–8 7C179–8		7C178–10 7C179–10		7C178–12 7C179–12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	12.5		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		1		ns
t_{CDV1}	Data Output Valid After CLK Rise, 0-pF Load		8.5		10.5		12.5	ns
t_{CDV2}	Data Output Valid After CLK Rise, 85-pF Load		10		12		14	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		3		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		1		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[9,10]		6		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[10]		10		12		14	ns

Notes:

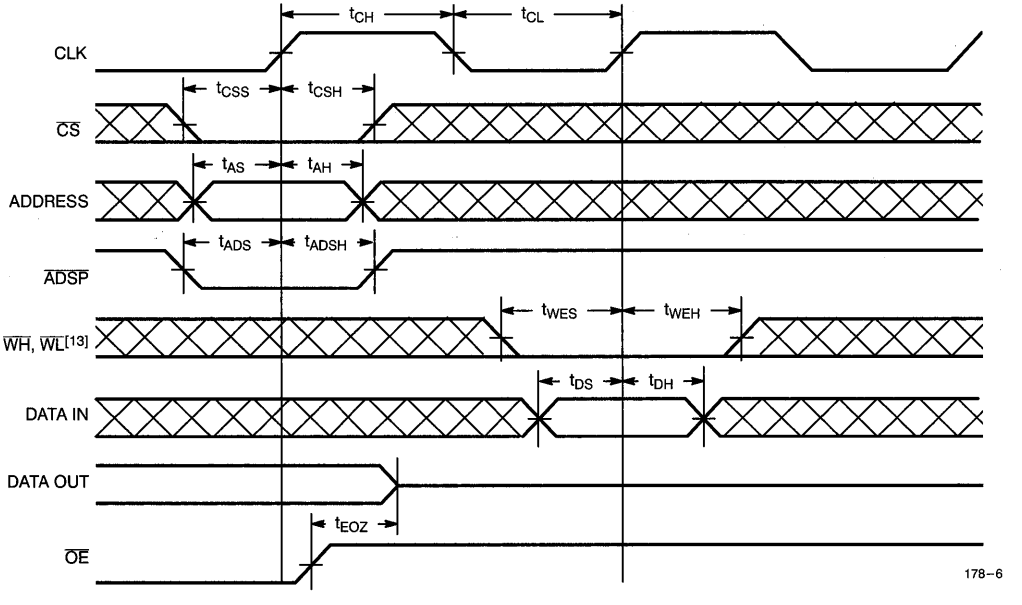
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[11]



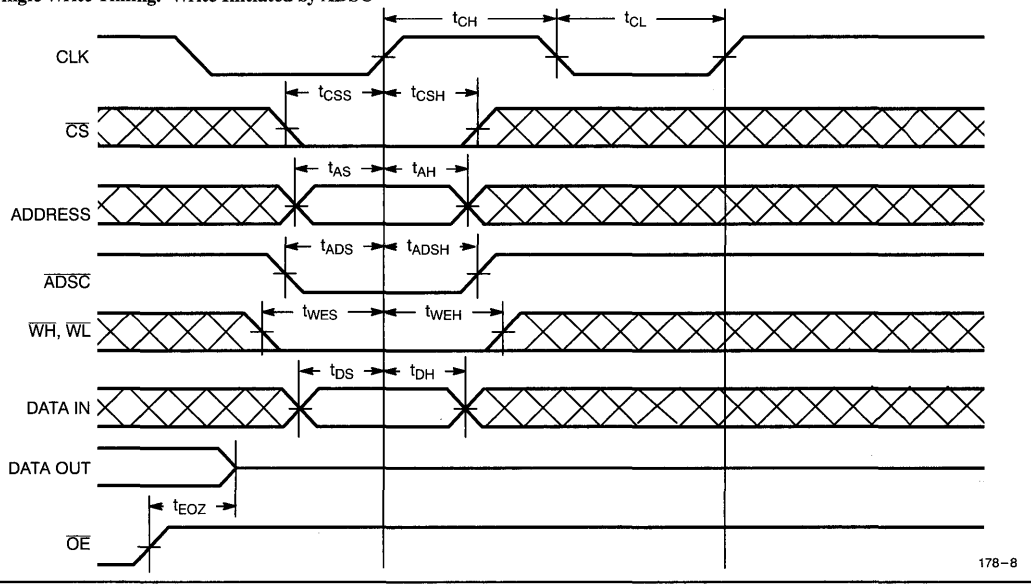
Single Write Timing: Write Initiated by $\overline{ADSP}$



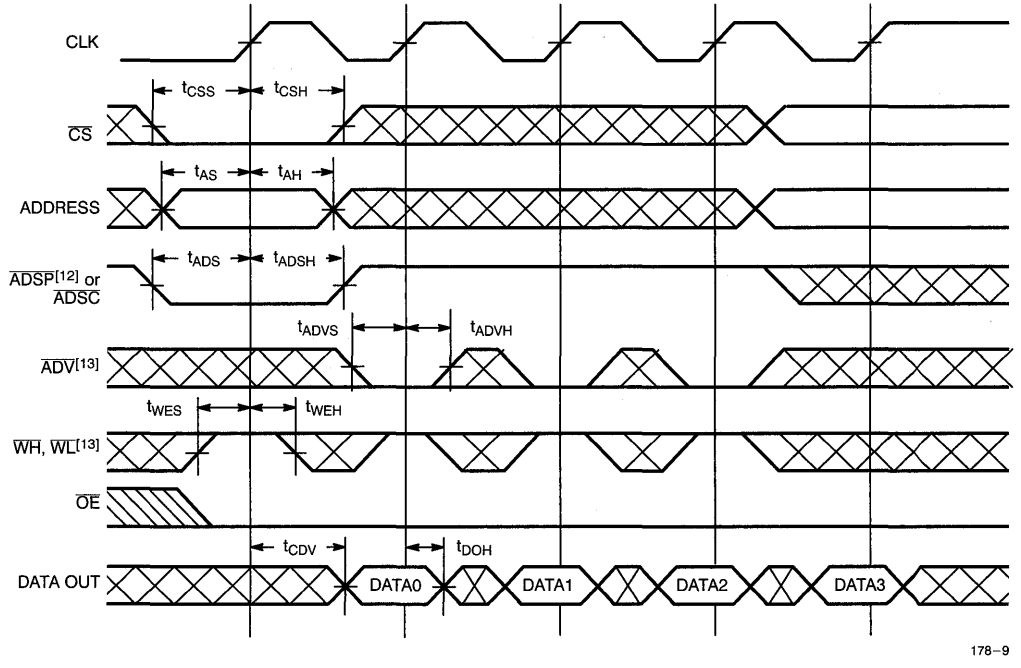
Notes:
11. $\overline{OE}$ is LOW throughout this operation.
12. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
13. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WH}$, and $\overline{WL}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

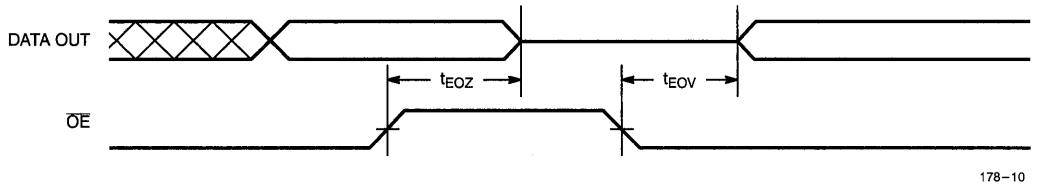


Burst Read Sequence with Four Accesses

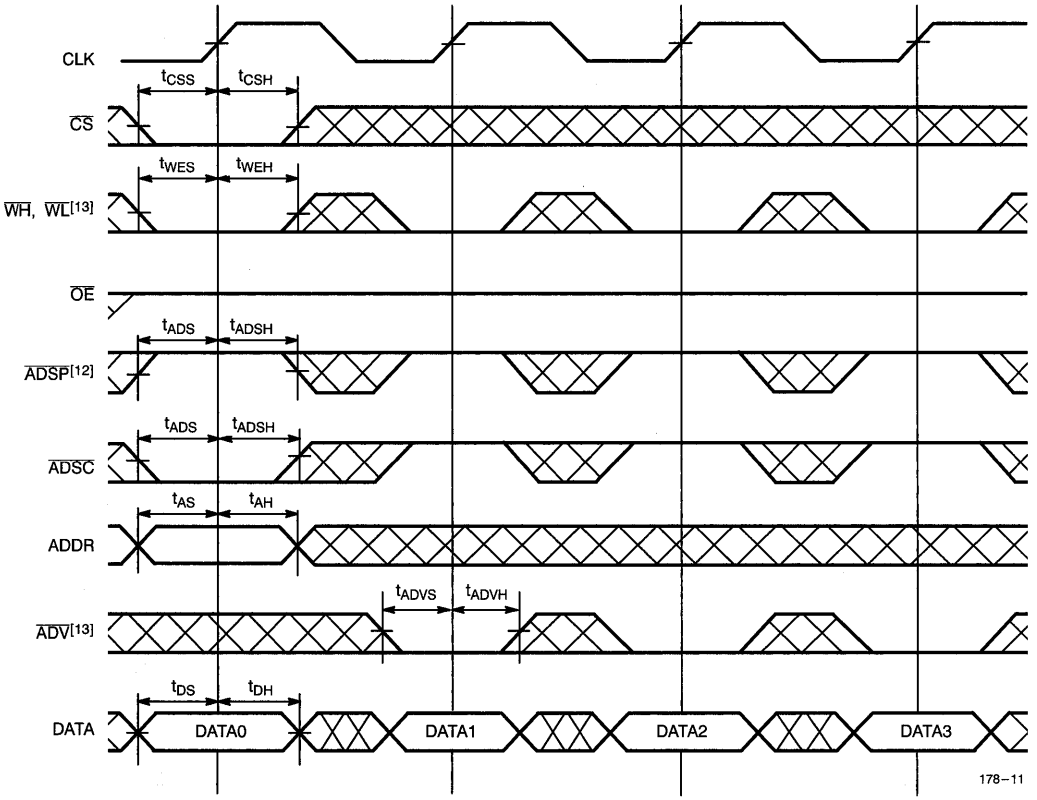


Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)

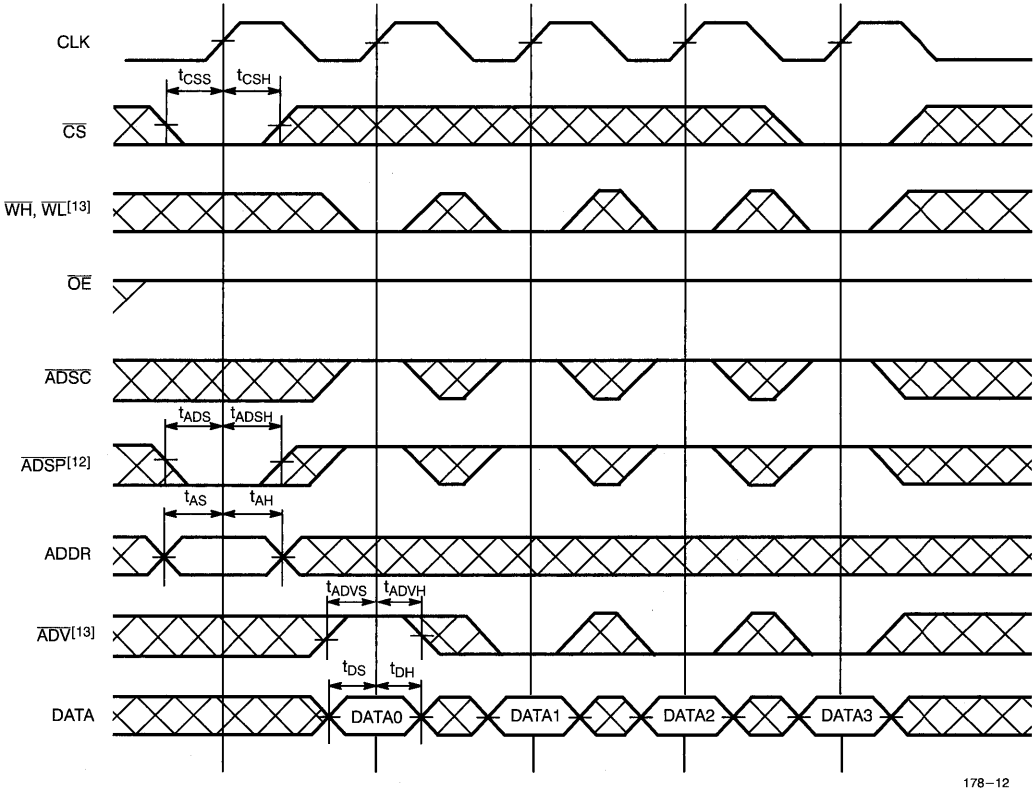


Write Burst Timing: Write Initiated by $\overline{ADSC}$



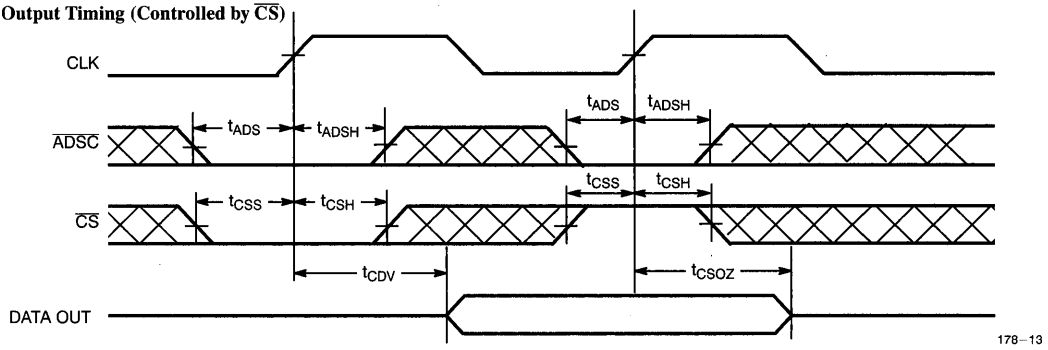
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

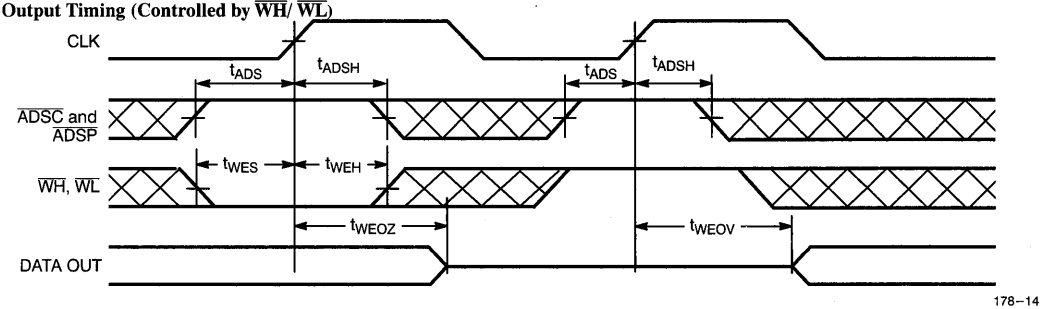


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}$/ $\overline{WL}$)



Truth Table

Input						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	L	H	H	H	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, read cycle
H	L	H	L	H	L→H	Incremented burst address	$\overline{ADSP}$ ignored, read cycle in burst sequence
H	L	H	H	L	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, write cycle
H	L	H	L	L	L→H	Incremented burst address	$\overline{ADSP}$ ignored, write cycle in burst sequence
H	X	L	X	X	L→H	N/A	Chip deselected
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C178–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C178–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C178–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–10NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C178–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C179–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C179–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C179–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C179–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

Document #: 38–00243

CY7B180
CY7B181

CYPRESS SEMICONDUCTOR

4K x 18 Cache Tag

Features

- **Supports 66-MHz cache for all major high-speed processors**
- **4K x 18 tag organization**
- **BiCMOS for optimum speed/power**
- **High speed**
  - **— 10-ns match delay**
  - **— 13-ns tag SRAM access**
- **Selectable clock and latch modes**
- **Input address and data latches**
- **Supports multiprocessing (CY7B180) with two cache status bits per entry**
- **Supports dirty and valid bits (CY7B181)**
  - **— Dirty-bit set on write hit**
  - **— Two cycles to invalidate entire tag array**
  - **— Match qualified by valid bit**
- **Write output to cache RAM asserted during write hit**
- **Cascadeable**
  - **— up to four cache tags with no external logic**
- **Can be used as 4K x 18 SRAM**

Functional Description

The CY7B180 and CY7B181 are high-performance BiCMOS cache tag RAMs organized as 4096 words by 18 bits. Each word contains a 16-bit address tag field and a 2-bit status field. Because the CY7B180 is optimized for multiprocessor applications where cache coherency is important, the two status bits are unassigned and can be used to store multiprocessing cache status information. Uniprocessor applications implementing write-through or copy-back cache policies are best supported by the CY7B181. The two status bits are assigned as the valid bit and the dirty bit. To simplify the cache controller logic, the dirty bit is set automatically during a write hit. The tag field and the status field can be loaded separately via a dedicated I/O data port.

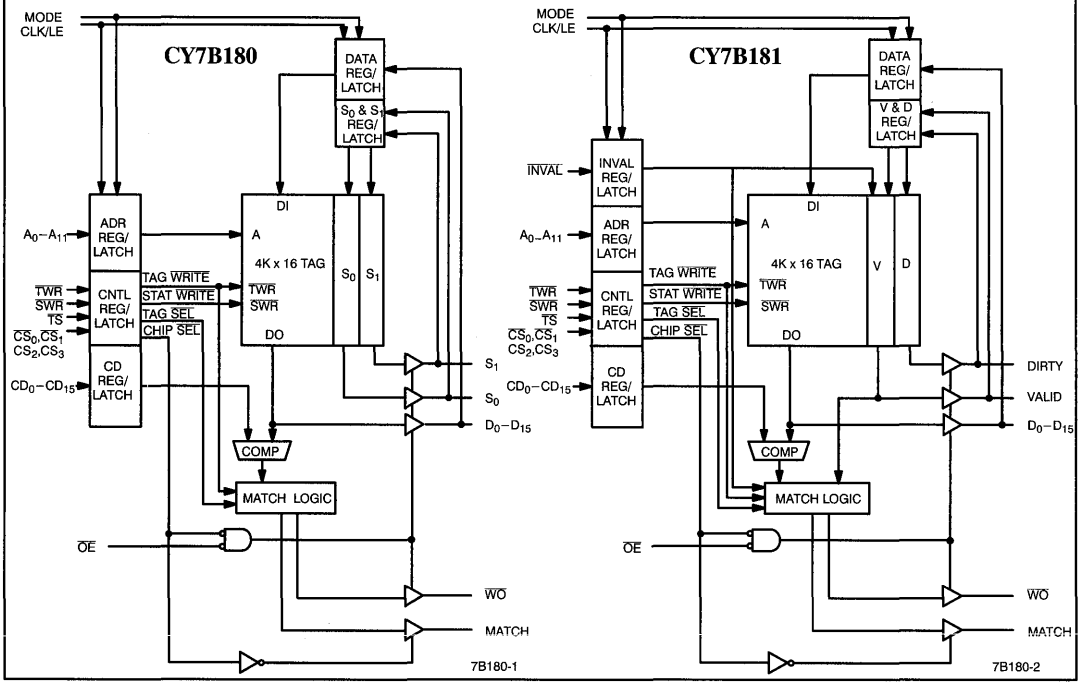
The twelve address lines select one of the 4096 words in the tag RAM. The 16-bit tag address is matched against data presented at the Compare Data inputs. In the CY7B181, the match output is qualified by the valid bit of the chosen word. Match is asserted only if the comparison is successful and the valid bit is set. The contents of the tag and status fields in the selected entry are available to external logic as direct output pins.

In many cache systems, generating the write signal to the cache RAMs is a time-consuming process because the write signal must be qualified with the match signal from the cache tag. The CY7B180/CY7B181 incorporates this function on-chip by asserting the write output ($\overline{WO}$) whenever a write hit is detected.

Tag invalidation in the CY7B181 is controlled by the $\overline{INVAL}$ input. Holding this input low for two consecutive cycles will invalidate the entire tag RAM. Individual entries can be invalidated by writing a zero into the valid bit of that entry.

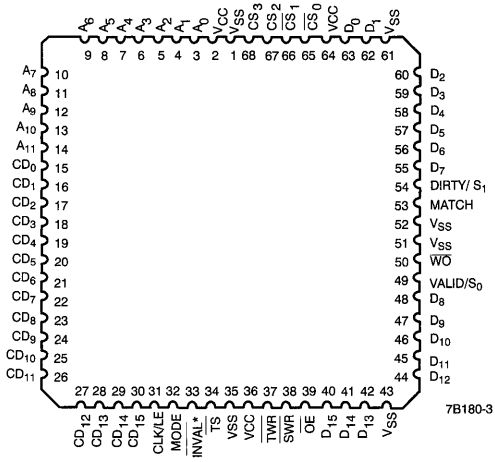
With a match delay of 10 ns and selectable clock or latch mode, the CY7B180 and CY7B181 can be used with all major high-speed microprocessors currently offered. The 13-ns address access of these parts also allows them to be used as 4K by 18 cache data RAMs.

Logic Block Diagrams



Pin Configurations

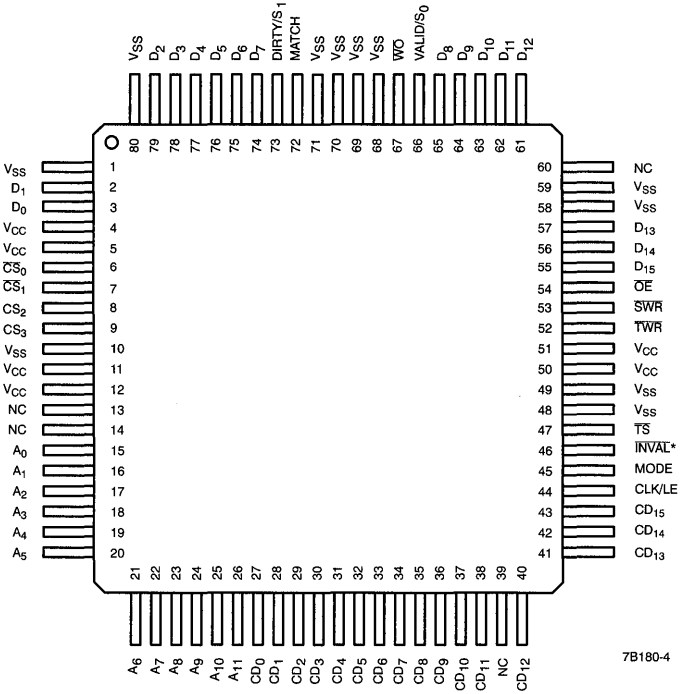
LCC & PLCC
Top View



* The INVAL input is only available on the CY7B181

Pin Configurations (continued)

PQFP
Top View



* Note: INVAL not supported in CY7B180.

Selection Guide

		7B180–10 7B181–10	7B180–12 7B181–12	7B180–15 7B181–15	7B180–20 7B181–20
Match Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	340	325	315	
	Military			390	390

Shaded area contains preliminary information.

Functional Description (continued)

Clock Mode

The CLOCK mode is selected when the MODE input is LOW. The address, compare data, chip select, and tag select are sampled at the rising edge of CLK. Write data is sampled on the falling edge of CLK. The tag write and status write inputs are different in that they are level sampled by CLK. If CLK is HIGH, the input latches associated with the tag write and status write inputs are transparent, and these inputs are allowed to ripple into the CY7B180/CY7B181. These inputs are latched when CLK goes LOW.

Latch Mode

The LATCH mode is selected when the MODE input is HIGH. All inputs are level sampled by LE. If LE is high, the input latches are transparent and the inputs are allowed to ripple into the CY7B180/CY7B181. When LE goes LOW, the inputs are latched and are no longer sampled. However, $\overline{LE}$ must still be strobed low to initiate a self-timed write.

Tag Storage

The CY7B180/CY7B181 provides 4096 cache tag entries. Each 7B181 entry contains a 16-bit cache tag address, a valid (V) bit, and a dirty (D) bit. The same two bits in the CY7B180 are generic status bits, and their meanings must be interpreted and controlled by the external processor.

On the CY7B181, the valid bit specifies the validity of the tag entry. A match is detected only when the 16-bit tag of the selected entry matches the 16 compare inputs and the valid bit is set. The dirty bit on the CY7B181 indicates whether the cache line associated with the tag entry has been modified and its value is available to external logic as the DIRTY output. The D bit in a selected entry on the CY7B181 is set if the current access is a write and a hit is detected. The valid bit in the selected entry is also available as the VALID output so that external logic can determine the cause of a miss:

- If the V bit is HIGH, then the miss is caused by tag mismatch.
- If the V bit is LOW, then the miss is caused by either a tag mismatch or an invalid, or both.

The cache tag entry format is shown in *Figure 1*.

Tag Compare

A tag compare cycle is initiated if tag select ($\overline{TS}$) is HIGH. $\overline{TS}$ is sampled at the rising edge of CLK (in the clock mode) or captured by the positive level of LE (in the latch mode). Once a tag entry is selected by A_0 through A_{11}, its 16-bit tag address is compared against CD_0 through CD_{15}. The compare result is delivered to the match logic.

The match output of the CY7B180 is driven HIGH if the compare is successful. For the CY7B181, the compare result is qualified by the state of the valid (V) bit in the selected entry. MATCH is driven HIGH only when the compare is successful and the valid bit is set.

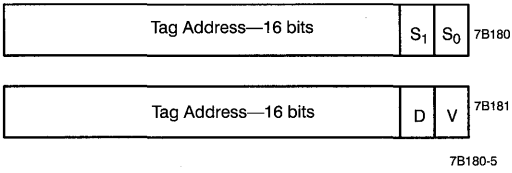


Figure 1. Cache Tag Entry Format

In addition, the write output ($\overline{WO}$) of the CY7B180/CY7B181 is asserted whenever a match is detected in a CPU write cycle ($\overline{TS}$ = 1 and $\overline{TWR}$ = 0). In some applications, this signal may be connected directly to the write input of the cache RAM.

Tag Access

The tag access cycle is initiated by asserting the tag select ($\overline{TS}$) input. Reading and writing is controlled by the tag write ($\overline{TWR}$) and status write ($\overline{SWR}$) inputs. In both clock and latch modes, the state of $\overline{TWR}$ and $\overline{SWR}$ are captured by the positive level of the CLK/LE input. The MATCH and $\overline{WO}$ outputs remain HIGH during tag access cycles.

If $\overline{TWR}$ is HIGH, the tag address field of the selected entry is driven onto data lines D_0 through D_{15} provided output enable ($\overline{OE}$) is LOW. For the CY7B180, the state of the two generic status bits are available at the S_0 and S_1 outputs if $\overline{SWR}$ is HIGH. For the CY7B181, the valid and dirty bits of the chosen entry are driven onto the valid and dirty outputs if $\overline{SWR}$ is HIGH.

Changing the tag content is accomplished by asserting the $\overline{TWR}$ and $\overline{SWR}$ inputs. $\overline{TWR}$ controls the loading of the tag address field while $\overline{SWR}$ controls the loading of the status field (S_0, S_1 in the CY7B180, valid and dirty in the CY7B181). Because the CY7B180/CY7B181 are common I/O devices, $\overline{OE}$ must be driven HIGH before data is placed on the data inputs and the status inputs.

Cascade Operation

Up to four CY7B180/CY7B181s can be used in a system by connecting appropriate address lines to the four chip select inputs. A cache tag is selected only if $\overline{CS_0} = \overline{CS_1} = 0$ and $CS_2 = CS_3 = 1$. Once selected, the CY7B180/CY7B181 will either execute a tag comparison cycle or a tag access cycle (depending on the state of the $\overline{TS}$ input). If a cache tag is deselected, it disables the comparison logic and three-states match, valid, dirty, $\overline{WO}$, and D_{15} through D_0 outputs.

The four chip selects are sampled at the positive edge of CLK (in clock mode) or sampled by the positive level of LE (in latch mode). By connecting the chip selects to the appropriate address bits or logic levels (see *Table 1* and *Figure 2*), four CY7B180/1s can be cascaded to provide 16,384 tag entries with no external logic.

Pin Descriptions

The cache tag RAM is packaged in a 68-pin PGA, PLCC, and LCC and in an 80-pin PQFP. The following sections are brief descriptions of the pin functions:

Supplies

V_{CC}—3 pins, connected to the +5V power supply (6 in the PQFP package).

GND—6 pins, connected to ground (11 in the PQFP package).

Input Signals

A_{11} – A_0—Address from the processor, 12 pins. These inputs are registered/latched and are controlled by CLK/LE. In the clock mode, the register is positive-edge triggered. In the LATCH mode, the latch is positive-level triggered. While in LATCH mode, if the LE input is HIGH, the latch is transparent and the addresses are allowed to ripple into the CY7B180/CY7B181 to start a new access. These 12 address inputs are used to select one of the 4096 cache tag entries.

Table 1. Chip Select Connections for Cascading Four Cache Tags

Tag 1				Tag 2			
CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$	CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$
H	H	Adr X+1	Adr X	H	Adr X	L	Adr X+1
Tag 3				**Tag 4**			
CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$	CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$
H	Adr X+1	L	Adr X	Adr X+1	Adr X	L	L

Tag 1 is selected when Adr X+1, Adr X = LL
Tag 2 is selected when Adr X+1, Adr X = LH
Tag 3 is selected when Adr X+1, Adr X = HL
Tag 4 is selected when Adr X+1, Adr X = HH

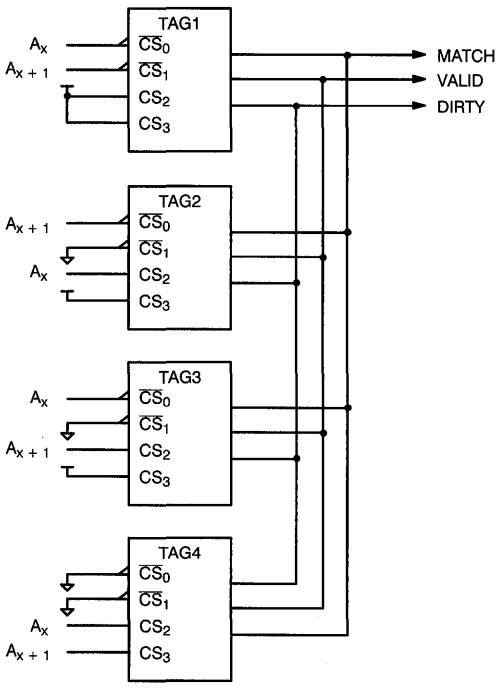


Figure 2. Cascading the CY7B180 and CY7B181

Pin Summary

Signal	Dir.	# of Pins	Description
V_{CC}		3	+5V
GND		6	Ground
$A_{11} - A_0$	I	12	Tag Address
CLK/LE	I	1	Clock/Latch
MODE	I	1	Mode Select
$CD_{15} - CD_0$	I	16	Compare Data
$\overline{CS_1} - \overline{CS_0}$	I	2	Chip Selects 1 & 0
$CS_3 - CS_2$	I	2	Chip Selects 3 & 2
$\overline{TS}$	I	1	Tag Select
$\overline{TWR}$	I	1	Tag Write Signal
$\overline{SWR}$	I	1	Status Write Signal
$\overline{INVAL}$	I	1	Tag Invalidate (CY7B181 only)
MATCH	O	1	Cache Match
$\overline{WO}$	O	1	Cache Write Match
VALID/S_0	I/O	1	Valid/Status Bit 0
DIRTY/S_1	I/O	1	Dirty/Status Bit 1
$D_{15} - D_0$	I/O	16	Processor Data
$\overline{OE}$	I	1	Output Enable

Pin Descriptions (continued)

MODE—Mode select, 1 pin. The clock mode is selected by strapping the MODE input LOW. The latch mode is selected by strapping this input HIGH.

CLK/LE—Clock/Latch input, 1 pin. This input controls all input registers and latches.

$CD_{15} - CD_0$—Compare data, 16 pins. These inputs are registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if the LE input is HIGH, the latch is transparent and the compare data is allowed to ripple into the CY7B180/CY7B181 to the comparison logic. The contents of the compare register/latch are compared with the 16-bit tag address in the selected tag entry.

$\overline{CS_0} - \overline{CS_1}$—Chip select 0 – 1, active LOW, 2 pins. These inputs are registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the LATCH mode, the latch is positive-level triggered. While in the LATCH mode, if the LE input is HIGH, the latch is transparent and the chip select inputs are allowed to ripple into the CY7B180/CY7B181. If $\overline{CS_1}$, $\overline{CS_0}$ are LOW and CS_2, CS_3 are HIGH, the comparison logic and output drivers are enabled, otherwise, the comparison logic will be disabled and all output drivers will be three-stated.

CS_2, CS_3—Chip select 2 – 3, active HIGH, 2 pins. These inputs are registered/latched CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if the LE input is HIGH, the latch is transparent and the chip select inputs are allowed to ripple into the CY7B180/CY7B181. If CS_2, CS_3 are HIGH and $\overline{CS_1}$, $\overline{CS_0}$

are LOW, the comparison logic and output drivers are enabled, otherwise, the comparison logic will be disabled and all output drivers will be three-stated.

$\overline{TS}$—Tag select, active LOW, 1 pin. This input is registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if LE is HIGH, the latch is transparent and the $\overline{TS}$ is allowed to ripple into the CY7B180/CY7B181. If $\overline{TS}$ is LOW, external logic is allowed to modify (read or write) the tag entries. If $\overline{TS}$ is HIGH, the tag entries are available only for address comparisons.

$\overline{TWR}$—Tag write indicator, active LOW, 1 pin. This input is latched and is controlled by CLK/LE. In both the clock and latch modes, the latch is positive-level triggered. While CLK/LE is HIGH, the latch is transparent and $\overline{TWR}$ is allowed to ripple into the CY7B180/CY7B181. $\overline{TWR}$ is handled according to the access mode: tag access mode or tag compare mode. In the tag access mode ($\overline{TS}$ = 0), $\overline{TWR}$ controls the access direction of the tag: a HIGH indicates a read while a LOW indicates a write. Assertion of $\overline{TWR}$ will store data on D_{15} through D_0 into the 16-bit tag address field of the selected entry. In the tag compare mode ($\overline{TS}$ = 1) of the CY7B181, $\overline{TWR}$ determines the setting of the dirty bit in the selected tag entry; the D bit is set if a tag match is detected and $\overline{TWR}$ is LOW. The $\overline{TWR}$ input of the CY7B180 is ignored in the tag compare mode; the status bits S_0 and S_1 are not modified.

$\overline{SWR}$—Status write indicator, active LOW, 1 pin. This input is latched by CLK/LE. In both the clock and latch modes, the latch is positive-level triggered. While CLK/LE is HIGH, the latch is transparent and $\overline{SWR}$ is allowed to ripple into the CY7B180/CY7B181. $\overline{SWR}$ is handled according to the access mode: tag access mode or tag compare mode. In the tag access mode ($\overline{TS}$ = 0), $\overline{SWR}$ controls the access direction of the status bits in the selected tag: a HIGH indicates a read while a LOW indicates a write. Assertion of $\overline{SWR}$ will store the data presented at the status inputs into the status bits of the selected entry. In the tag compare mode ($\overline{TS}$ = 1), the state of $\overline{SWR}$ is ignored.

$\overline{INVAL}$—Tag invalidate input, active LOW, 1 pin. This input is only available in the CY7B181. It is registered at the rising edge of CLK/LE. Assertion of $\overline{INVAL}$ overrides all other operations and clears all of the valid bits in the tag storage. The CY7B181 does not have to be selected to do an invalidation. An invalidation requires two cycles to complete; therefore, the $\overline{INVAL}$ input must be held for two rising edges of the CLK or LE signal. If the $\overline{INVAL}$ input is asserted, MATCH is forced LOW, $\overline{WO}$ is forced HIGH, VALID is forced LOW, DIRTY goes to an unknown state, and the data outputs (D_0 through D_{15}) go to an unknown state. The $\overline{INVAL}$ input must be asserted during power-up to ensure that all of the valid bits in the tag are cleared. The contents of the tag may be modified as a result of invalidation.

$\overline{OE}$—Output enable, 1 pin. When $\overline{OE}$ is HIGH, all outputs except match will be placed in a three-state condition. This pin must be asserted before the beginning of a tag write cycle to allow the external processor to drive data into the CY7B180/CY7B181.

Output Signals

MATCH—Cache match signal, active HIGH, 1 pin. A HIGH at this pin indicates a cache hit while a LOW indicates a cache miss. This output is HIGH during all tag access cycles ($\overline{TS}$ = 0), except on the CY7B181 when the $\overline{INVAL}$ input is asserted. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the match output is forced LOW. Match is placed in a three-state condition when the tag is deselected via the chip select signals. $\overline{OE}$ has no effect on the match output.

$\overline{WO}$—Cache write match signal, active LOW, one pin. A LOW at this pin indicates a cache hit during a memory write. A HIGH indicates a cache miss during a memory write. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the $\overline{WO}$ output is forced HIGH. This output is HIGH during all tag access cycles ($\overline{TS}$ = 0). $\overline{WO}$ is placed in a three-state condition when the tag is deselected via the chip select signals or when $\overline{OE}$ is HIGH.

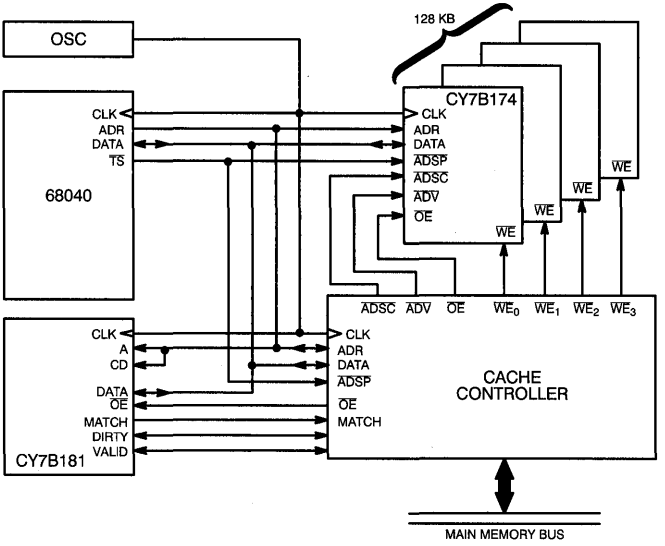
Input/Output Signals

D_{15}–D_0—Data lines to/from the processor, 16 pins. These pins are used during both tag access ($\overline{TS}$ = 0) and tag compare ($\overline{TS}$ = 1) cycles. During tag reads or tag compares, the tag address field of the selected tag entry is driven onto these lines. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the data outputs will go to an unknown state. During tag writes, the $\overline{OE}$ input must be deasserted to three-state the output drivers so that these pins may be driven by the external processor. The data inputs are registered/latched by the CY7B180/CY7B181. In the clock mode, the register is negative edge triggered. In the latch mode, the latch is positive level triggered. While in the latch mode, if LE is HIGH, the latch is transparent and the data is allowed to ripple into the CY7B180/CY7B181. All 16 outputs will be placed in a three-state condition if the $\overline{OE}$ input is deasserted (HIGH) or when the cache tag is deselected via the four chip select inputs.

VALID/S_0—Valid bit (active HIGH) in CY7B181, status bit S_0 in CY7B180, 1 pin. During tag comparison and status read cycles, this pin reflects the state of the Valid bit (in CY7B181) or status bit S_0 (in CY7B180) of the selected entry. During status write cycles ($\overline{TS}$ and $\overline{SWR}$ LOW), data presented at this pin is registered/latched. In the clock mode, the register is negative-edge triggered. In the latch mode, the latch is positive-level triggered. This pin can be placed in a three-state condition via the chip select and output enable signals. If the $\overline{INVAL}$ input of the CY7B181 is asserted, the VALID output is forced LOW.

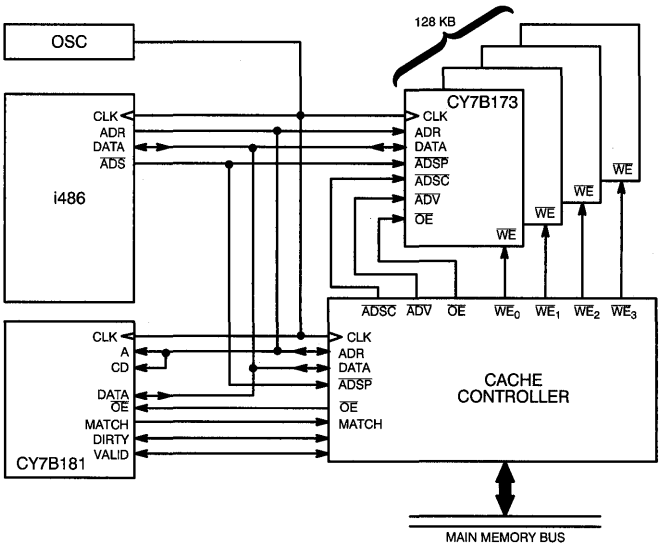
DIRTY/S_1—Dirty bit (active HIGH) in CY7B181, status bit S_1 in CY7B180, 1 pin. During tag comparison and status read cycles, this pin reflects the state of the Dirty bit (in CY7B181) or status bit S_1 (in CY7B180) of the selected entry. In copy-back caches using the CY7B181, the cache controller can examine this output to determine whether the cache line to be replaced should be copied back to the main memory. During status write cycles ($\overline{TS}$ and $\overline{SWR}$ LOW), data presented at this pin is registered/latched. In the clock mode, the register is negative-edge triggered. In the latch mode, the latch is positive-level triggered. This pin can be placed in a three-state condition via the chip select and output enable signals. If the $\overline{INVAL}$ input of the CY7B181 is asserted, the Dirty output will enter an unknown state.

Application Examples



7B180-7

A 128-Kbyte cache for a single 68040 using four CY7B174 cache RAMs and a CY7B181 cache tag. The complexity of the cache controller is reduced because the CY7B181 generates the write enable signal to the RAM automatically during write hits.



7B180-6

A 128-Kbyte secondary cache for a single i486 using four CY7B173 cache RAMs and a CY7B181 Cache Tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match result is delivered to the cache controller after 10 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to +V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B180−10 7B181−10 Min.	7B180−10 7B181−10 Max.	7B180−12 7B181−12 Min.	7B180−12 7B181−12 Max.	7B180−15, 20 7B181−15, 20 Min.	7B180−15, 20 7B181−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage[1]			− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 2.0		− 2.0		− 2.0		mA
I_{OL}	Output LOW Current	V_{CC} = Max., V_{OL} = 0.4V		4.0		4.0		4.0		mA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max, V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current[4]	V_{CC} = Max., I_{OUT} MATCH= 0 mA, $\overline{OE}$ HIGH, f = f_{MAX} = $1/t_{CYC}$	Com'l		340		325		315	mA
			Mil						390	

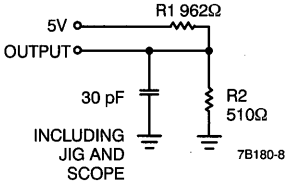
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	6.5	pF
C_{OUT}	Output Capacitance		10	pF

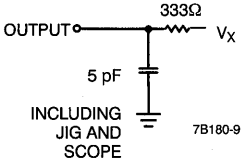
Notes:

1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
2. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Assumes 67% read cycles and 33% write cycles (50% cache hit rate).
5. Tested initially and after any design or process changes that may affect these parameters.

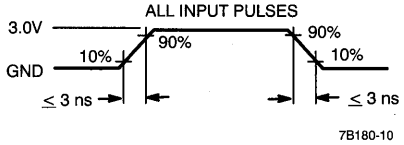
AC Test Loads and Waveforms



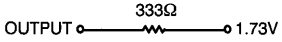
(a)



(b) Three-State Delay Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[6]

Parameter	Description	7B180–10 7B181–10 Min.	7B180–10 7B181–10 Max.	7B180–12 7B181–12 Min.	7B180–12 7B181–12 Max.	7B180–15 7B181–15 Min.	7B180–15 7B181–15 Max.	7B180–20 7B181–20 Min.	7B180–20 7B181–20 Max.	Unit
t_{CYC}	Clock Cycle Time	15		20		24		33		ns
t_{CH}	Clock HIGH	7		8		10		13		ns
t_{CL}	Clock LOW	7		8		10		13		ns
t_{OEDZ}	$\overline{OE}$ HIGH to Output High Z[7]		6		7		9		12	ns
t_{OEDV}	$\overline{OE}$ LOW to Output Valid[8]		8		9		11		13	ns
CLOCK MODE (RE = Rising Edge, FE = Falling Edge)										
t_{MCH}	Match Valid After CLK RE		10		12		15		20	ns
t_{MHLD}	Match Hold After CLK RE	2		2		2		2		ns
t_{CSD}	Status Valid After CLK RE		10		12		15		20	ns
t_{SHLD}	Status Hold After CLK RE	2		2		2		2		ns
t_{TWRWO}	Write Output Valid After $\overline{TWR}$ LOW		8		9		11		13	ns
t_{WO}	Write Output Valid After CLK RE		10		12		15		20	ns
t_{WOHLD}	Write Match Hold After CLK RE	2		2		2		2		ns
t_{AD}	Access Delay from CLK RE		13		15		18		25	ns
t_{DOH}	Output Data Hold After CLK RE	3		3		3		3		ns
t_{DIS}	Input Data Set-Up Before CLK FE	4		4		5		6		ns
t_{DIH}	Input Data Hold After CLK FE	2		2		3		4		ns
t_{TSS}	$\overline{TS}$ Set-Up Before CLK RE	3		3		4		5		ns
t_{TSH}	$\overline{TS}$ Hold After CLK RE	3		3		4		5		ns
t_{AS}	Address Set-Up Before CLK RE	3		3		4		5		ns
t_{AH}	Address Hold After CLK RE	3		3		4		5		ns
t_{CDS}	Compare Data Set-Up Before CLK RE	3		3		4		5		ns
t_{CDH}	Compare Data Hold After CLK RE	3		3		4		5		ns
t_{CSS}	Chip Select Set-Up Before CLK RE	3		3		4		5		ns
t_{CSH}	Chip Select Hold After CLK RE	3		3		4		5		ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7B180–10 7B181–10		7B180–12 7B181–12		7B180–15 7B181–15		7B180–20 7B181–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CSHZ}	Output High Z After CLK RE (chip deselected via CS inputs)[7, 9]		8		9		11		13	ns
t_{CSLZ}	Output Low Z After CLK RE (chip deselected via CS inputs)[8, 9]	2		2		2		2		ns
t_{WRS}	$\overline{WR}$ Set-Up Before CLK FE	3		3		4		5		ns
t_{WRH}	$\overline{WR}$ Hold After CLK FE	3		3		4		5		ns
t_{INVS1}	$\overline{INVAL}$ Set-Up Before CLK RE	3		3		4		5		ns
t_{INVH1}	$\overline{INVAL}$ Hold After CLK RE	3		3		4		5		ns
t_{MCHL1}	MATCH LOW After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
t_{WOH1}	$\overline{WO}$ HIGH After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
t_{VALL1}	VALID LOW After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
LATCH MODE										
t_{LRLR}	LE Rise to Next LE Rise	15		20		24		33		ns
t_{LW}	Width of LE Pulse	5		5		6		8		ns
t_{LFLR}	LE Fall to LE Rise	8		8		10		13		ns
t_{ASLC}	Address Set-Up Before Latch Close	3		3		4		5		ns
t_{AHLC}	Address Hold After Latch Close	3		3		4		5		ns
t_{CSLC}	Chip Select Set-Up Before Latch Close	3		3		4		5		ns
t_{CHLC}	Chip Select Hold After Latch Close	3		3		4		5		ns
t_{TSLC}	Tag Select Set-Up Before Latch Close	3		3		4		5		ns
t_{THLC}	Tag Select Hold After Latch Close	3		3		4		5		ns
t_{WSLC}	Write Set-Up Before Latch Close	3		3		4		5		ns
t_{WHLC}	Write Hold After Latch Close	3		3		4		5		ns
t_{CDSLC}	Comp Data Set-Up Before Latch Close	3		3		4		5		ns
t_{CDHLC}	Comp Data Hold After Latch Close	3		3		4		5		ns
t_{DSLC}	Data In Set-Up Before Latch Close	4		4		5		6		ns
t_{DHLC}	Data In Hold After Latch Close	2		2		3		4		ns
t_{CDMCH}	Comp Data Valid to Match Valid		10		12		15		20	ns
t_{TSMCH}	Tag Select Valid to Match Valid		10		12		15		20	ns
t_{CSMCH}	Chip Select Valid to Match Valid		10		12		15		20	ns
t_{AMCH}	Address Valid to Match Valid		10		12		15		20	ns
t_{LOMCH}	Latch Open to Match Valid		10		12		15		20	ns
t_{LOMX}	Latch Open to Match Change	2		2		2		2		ns
t_{TSSV}	Tag Select Valid to Status Valid		10		12		15		20	ns
t_{CSSV}	Chip Select Valid to Status Valid		10		12		15		20	ns
t_{ASV}	Address Valid to Status Valid		10		12		15		20	ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7B180–10 7B181–10		7B180–12 7B181–12		7B180–15 7B181–15		7B180–20 7B181–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LOSV}	Latch Open to Status Valid		10		12		15		20	ns
t_{LOSX}	Latch Open to Status Change	2		2		2		2		ns
t_{TWRWO}	$\overline{TWR}$ VALID to $\overline{WO}$ Valid		8		9		11		13	ns
t_{CDWO}	Comp Data Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{TSWO}	Tag Select Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{CSWO}	Chip Select Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{AWO}	Address Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{LOWO}	Latch Open to $\overline{WO}$ Valid		10		12		15		20	ns
t_{LOWOX}	Latch Open to $\overline{WO}$ Change	2		2		2		2		ns
t_{CSDV}	Chip Select Valid to Data Out Valid		13		15		18		25	ns
t_{ADV}	Address Valid to Data Out Valid		13		15		18		25	ns
t_{LODV}	Latch Open to Data Out Valid		13		15		18		25	ns
t_{LODX}	Latch Open to Data Out Change	2		2		2		2		ns
t_{TSLMH}	Tag Select LOW to Match HIGH		8		9		11		13	ns
t_{TSLWOH}	Tag Select LOW to $\overline{WO}$ HIGH		8		9		11		13	ns
t_{CSHZ}	Output High Z After the Tag is Deselected via Chip Select Inputs[7, 9]		8		9		11		13	ns
t_{CSLZ}	Output Low Z After the Tag is Selected via Chip Select Inputs[8, 9]	2		2		2		2		ns
t_{INVS2}	$\overline{INVAL}$ Set-Up Before LE RE	3		3		4		5		ns
t_{INVH2}	$\overline{INVAL}$ Hold After LE RE	3		3		4		5		ns
t_{MCHL2}	MATCH LOW After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns
t_{WOH2}	$\overline{WO}$ HIGH After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns
t_{VALL2}	VALID LOW After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns

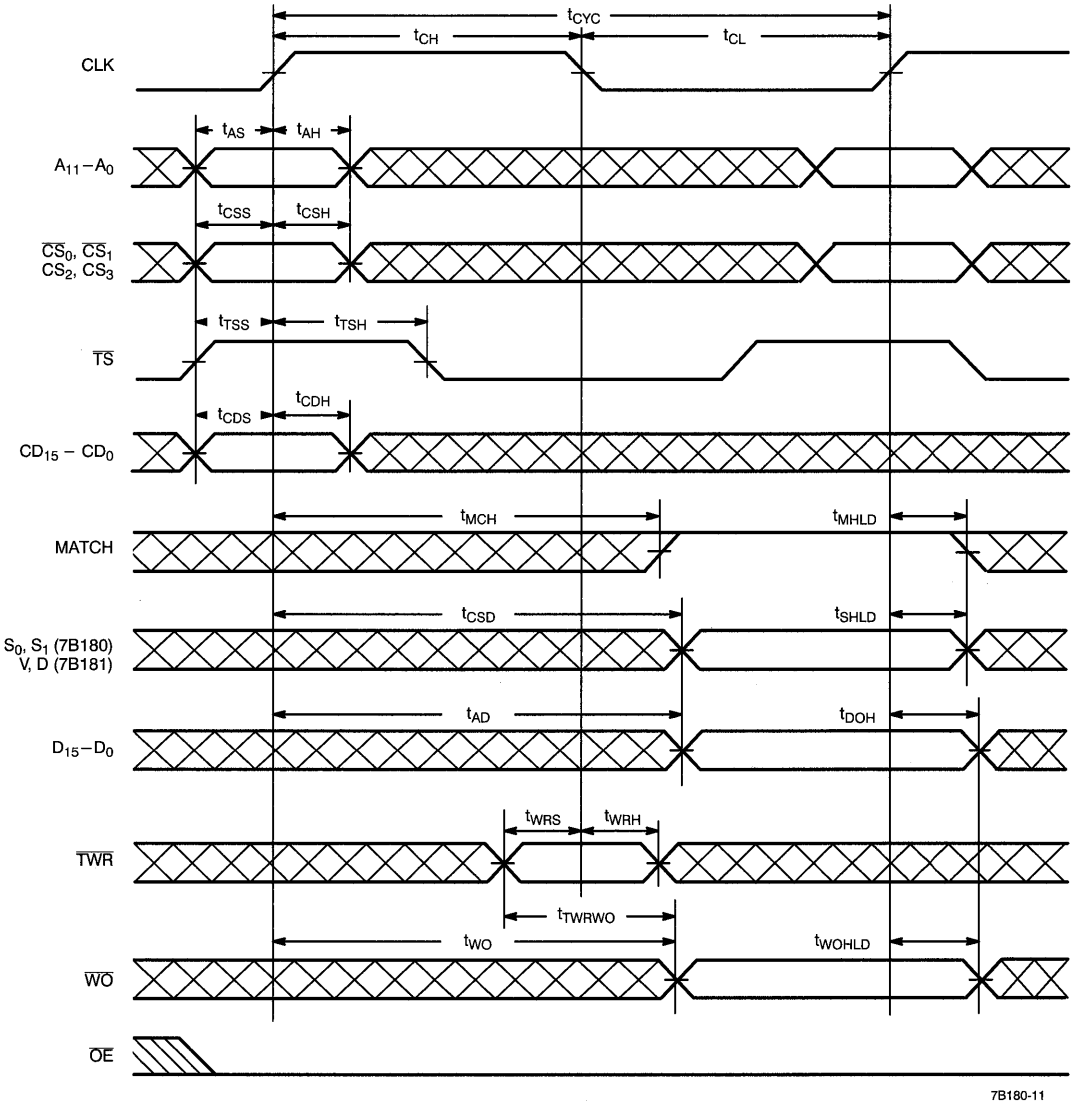
Shaded area contains preliminary information.

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 35-pF load capacitance, as in part (a) of AC Test Loads and Waveforms, unless otherwise specified.
7. t_{OEDZ} and t_{CSHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured at ±500 mV from steady-state voltage. This parameter is sampled and not 100% tested.
8. t_{OEDV} and t_{CSLZ} are tested using part (a) of AC Test Loads and Waveforms. This parameter is sampled and not 100% tested.
9. At any voltage and temperature combination, t_{CSHZ} max. is guaranteed to be smaller than t_{CSLZ} min. for a given device.

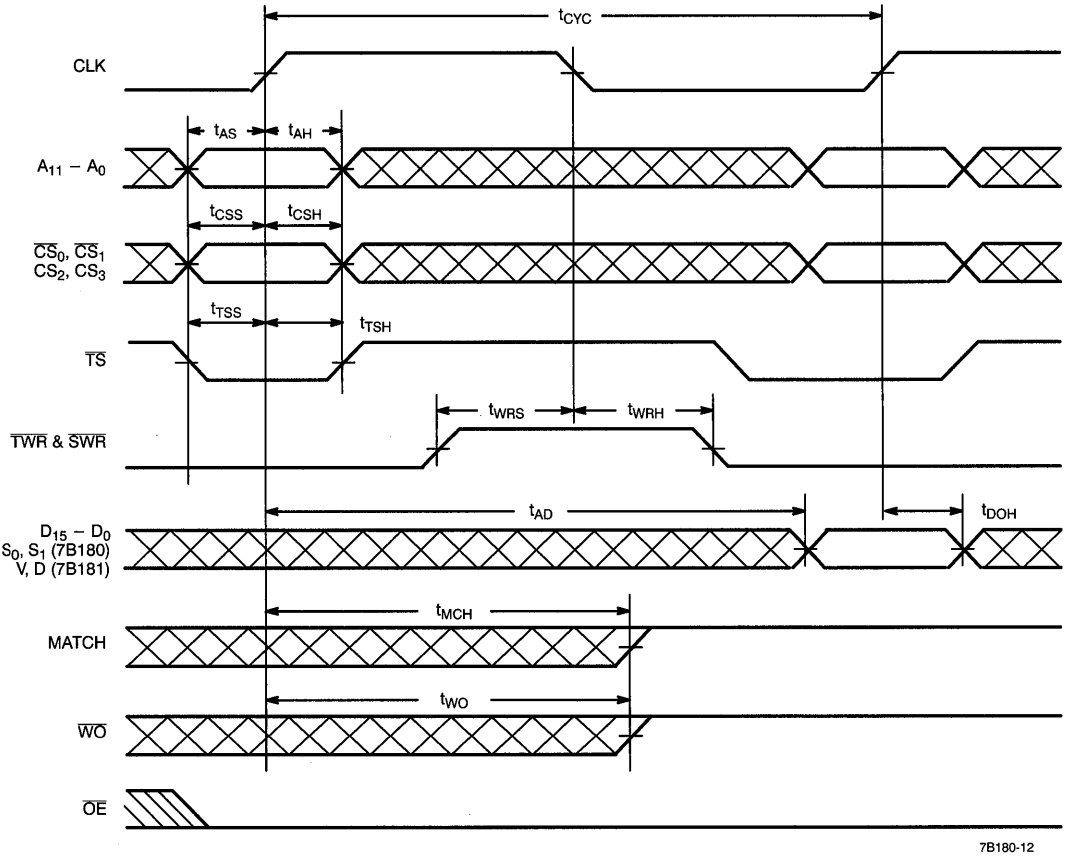
Switching Waveforms

Tag Match Timing in Clock Mode (Showing a Hit)



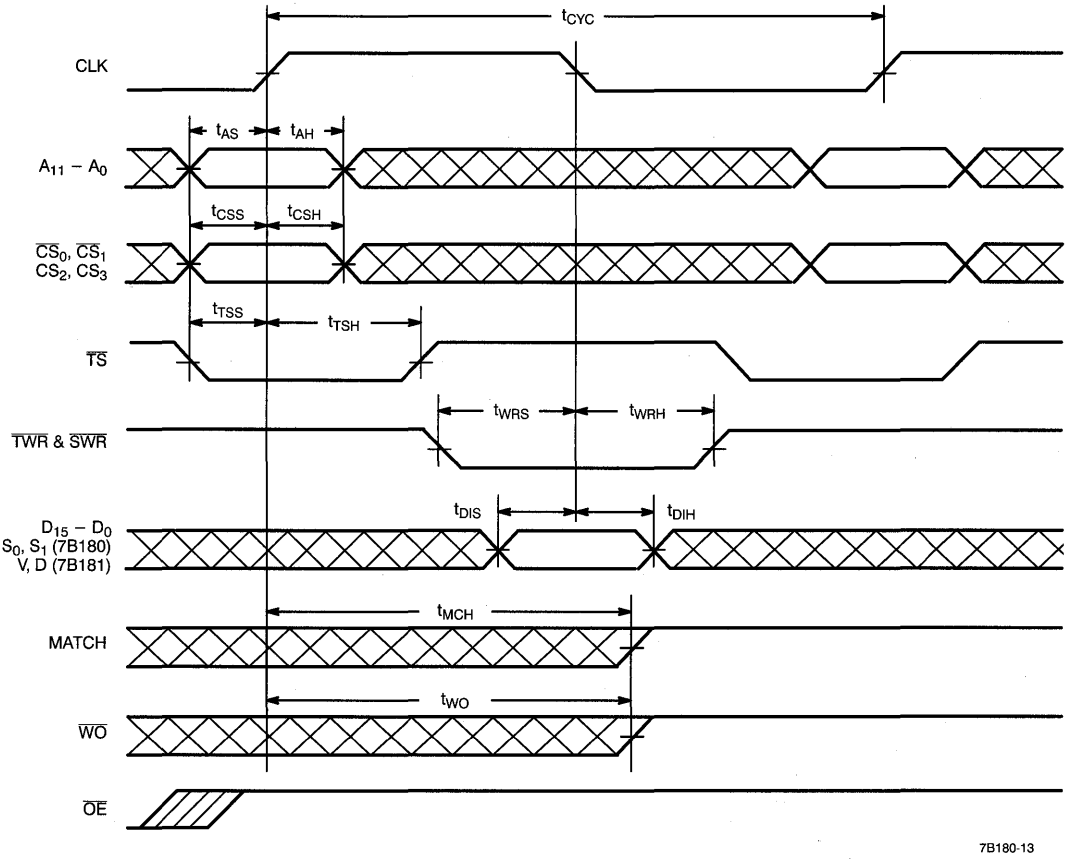
Switching Waveforms (continued)

Tag Read Timing in Clock Mode



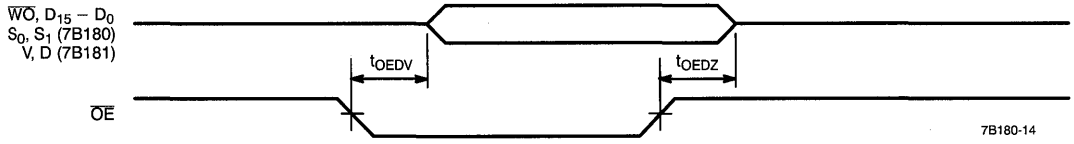
Switching Waveforms (continued)

Tag Write Timing in Clock Mode

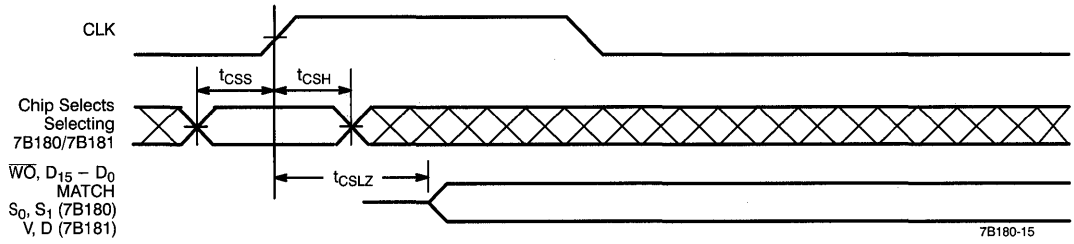


Switching Waveforms (continued)

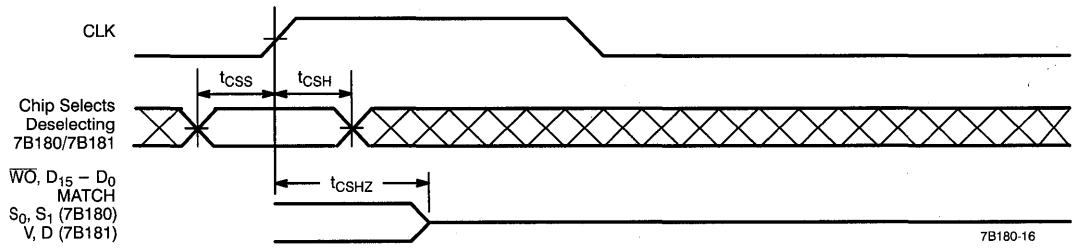
Output Enable Timing



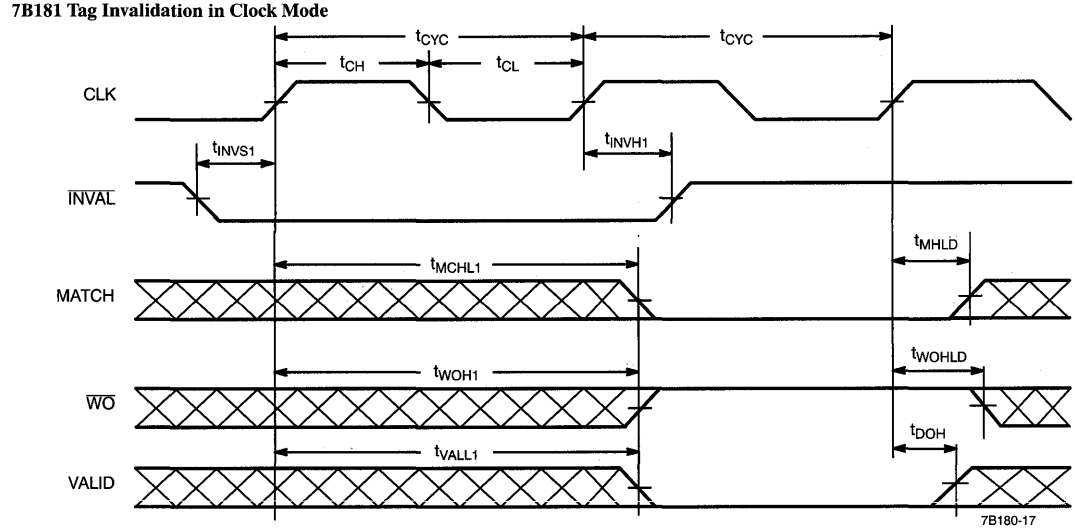
Chip Select Timing in Clock Mode



Chip Deselect Timing in Clock Mode

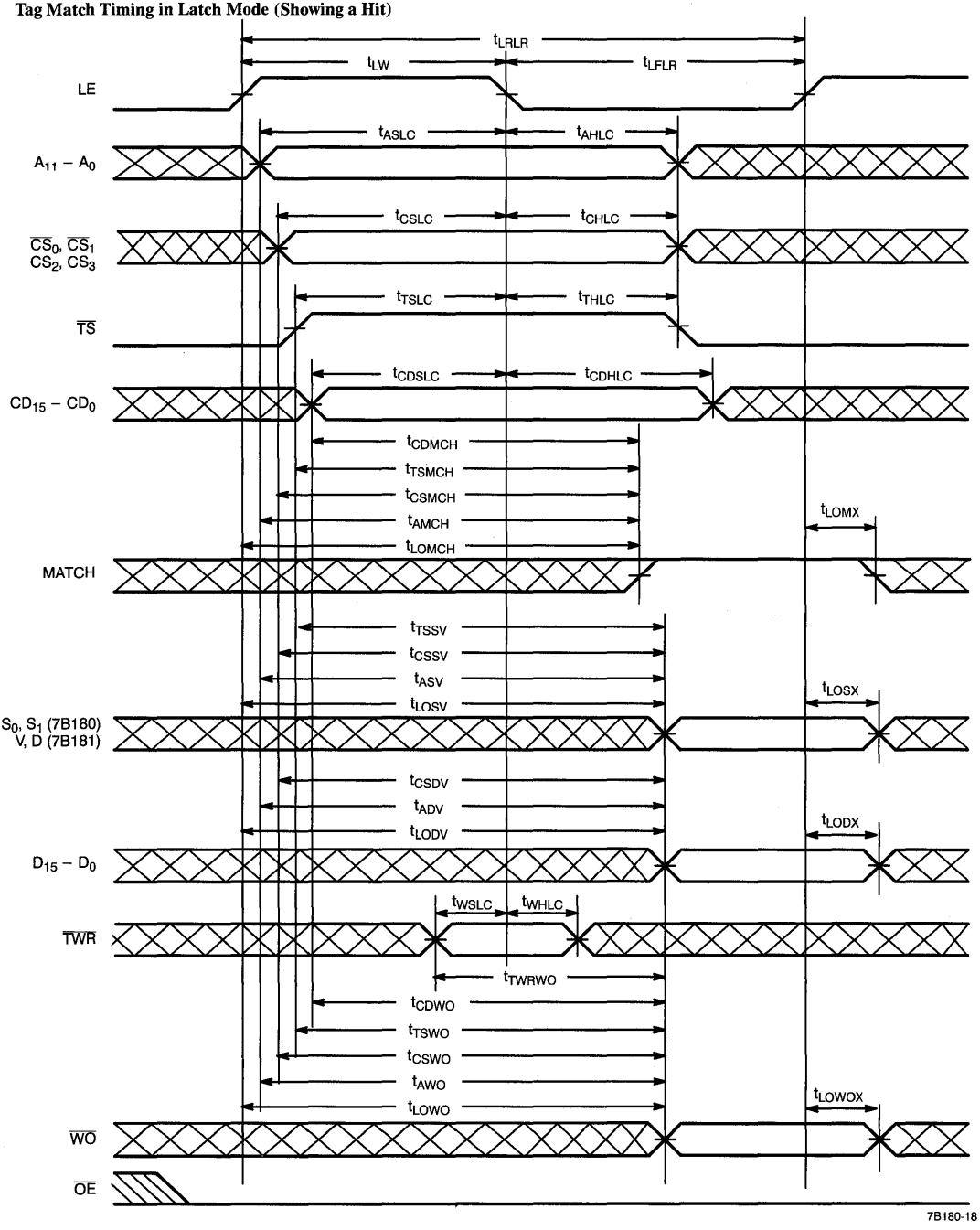


7B181 Tag Invalidation in Clock Mode



Switching Waveforms (continued)

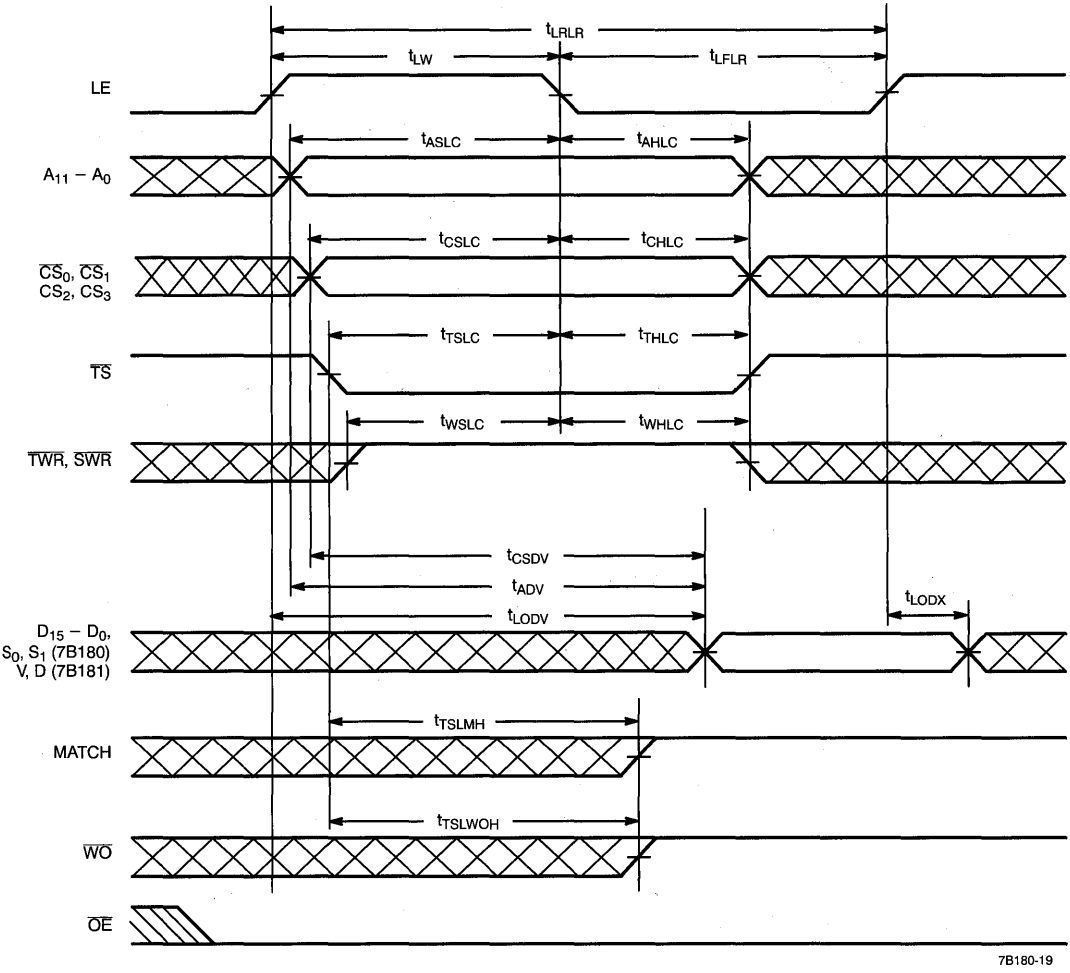
Tag Match Timing in Latch Mode (Showing a Hit)



7B180-18

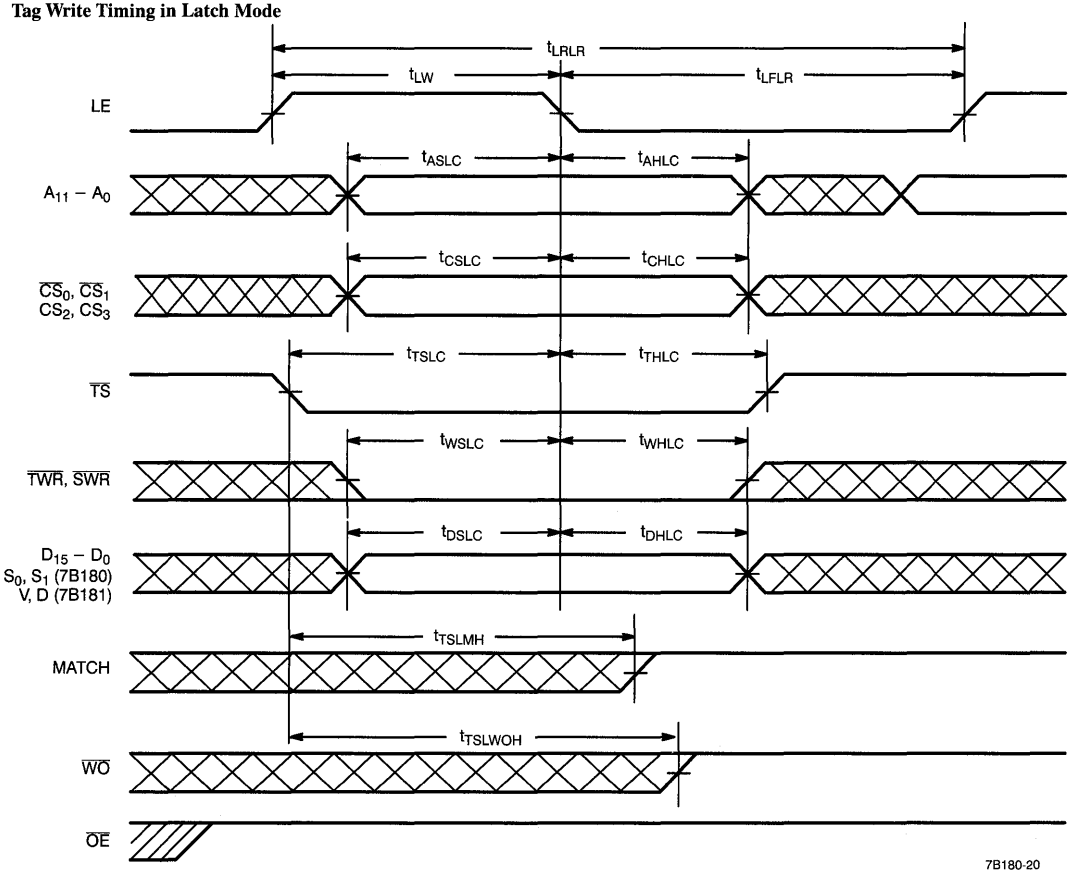
Switching Waveforms (continued)

Tag Read Timing in Latch Mode



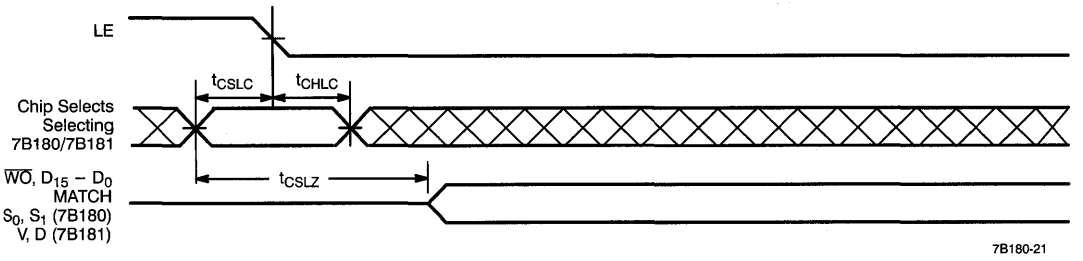
Switching Waveforms (continued)

Tag Write Timing in Latch Mode

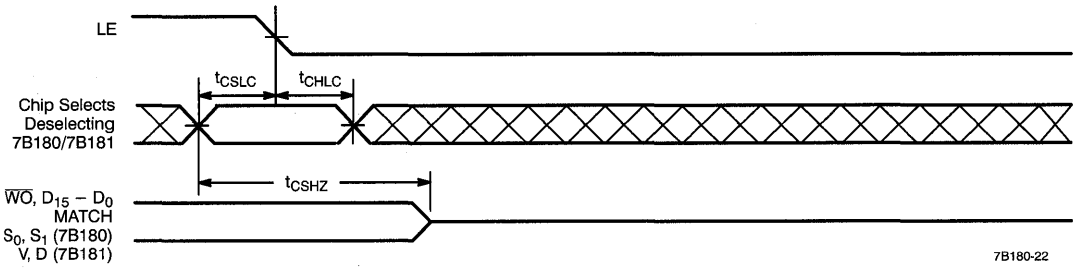


Switching Waveforms (continued)

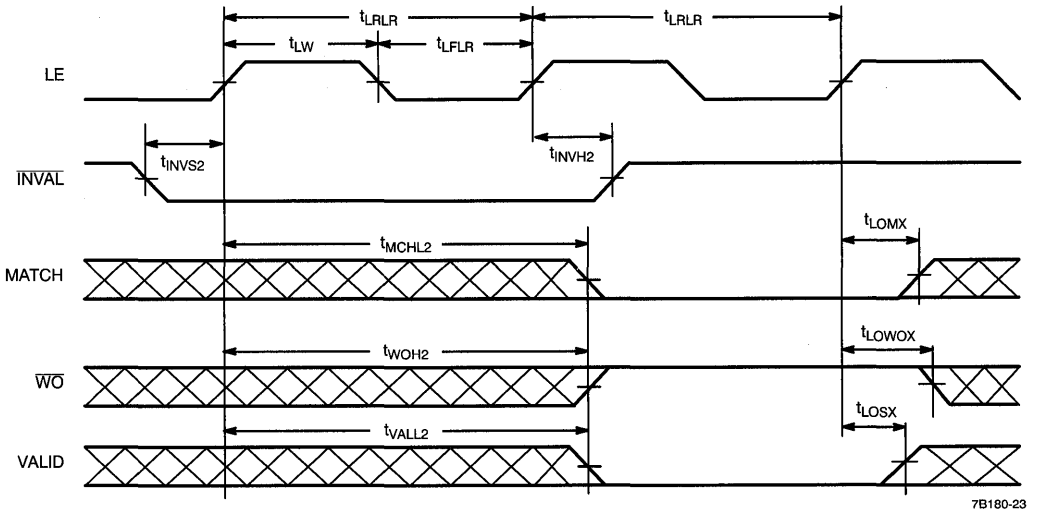
Chip Select Timing in Latch Mode



Chip Deselect Timing in Latch Mode



7B181 Tag Invalidation in Latch Mode



Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7B180–10JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–10NC	N80	80-Lead Plastic Quad Flatpack	
12	CY7B180–12JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–12NC	N80	80-Lead Plastic Quad Flatpack	
15	CY7B180–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–15NC	N80	80-Lead Plastic Quad Flatpack	
	CY7B180–15LMB	L81	68-Square Leadless Chip Carrier	Military
20	CY7B180–20LMB	L81	68-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7B181–10JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–10NC	N80	80-Lead Plastic Quad Flatpack	
12	CY7B181–12JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–12NC	N80	80-Lead Plastic Quad Flatpack	
15	CY7B181–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–15NC	N80	80-Lead Plastic Quad Flatpack	
	CY7B181–15LMB	L81	68-Square Leadless Chip Carrier	Military
20	CY7B181–20LMB	L81	68-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.

Document #: 38–00155–D

CYPRESS SEMICONDUCTOR

CY7C182

8K x 9 Static R/W RAM

Features

- **High speed**
  — t_{AA} = 25 ns
- **x9 organization is ideal for cache memory applications**
- **CMOS for optimum speed/power**
- **Low active power**
  — 770 mW
- **Low standby power**
  — 195 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, $\overline{OE}$ options**

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 770 mW.

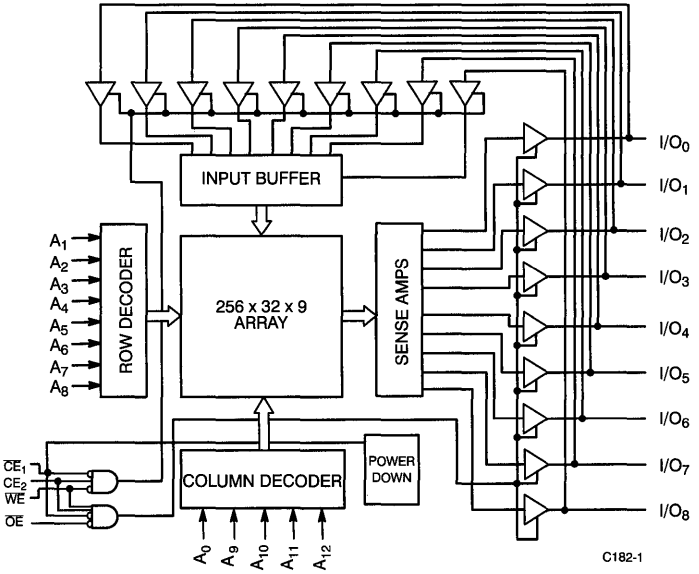
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by more than 70% when the circuit is deselected. Easy memory expansion is provided by an active-LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and three-state drivers.

An active-LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, ($\overline{CE}_1$ and $\overline{OE}$ active LOW and CE_2 active HIGH), while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

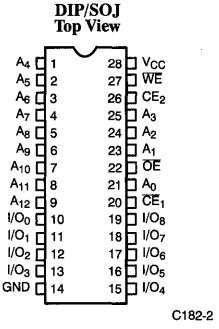
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C182–20	7C182–25	7C182–35	7C182–45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating Current (mA)	Com'l	150	140	140	140
Maximum Standby Current (mA)		35	35	35	35

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential[1] ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C182−20		7C182−25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} Min., I_{OH} = − 4.0 mA.	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}, GND < V_{OUT} < V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Circuit Current	V_{CC} Max., Output Current = 0 mA, f = Max., V_{IN} = V_{CC} or GND		150		140	mA
I_{SB1}	Automatic Power-Down Current — TTL Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		35		35	mA
I_{SB2}	Automatic Power-Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0		20		20	mA

Shaded area contains advanced information.

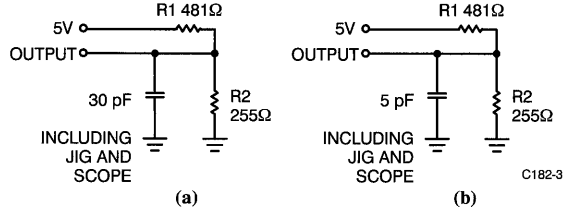
Capacitance[3]

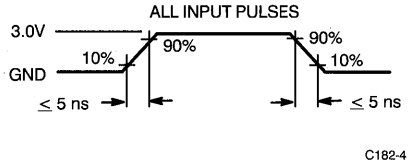
Parameter	Description	Test Conditions	Max.	Unit
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{IN}	Input Capacitance		10	pF

Notes:

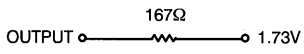
1. $V_{IL\,(min.)}$ = − 3.0V for pulse durations of less than 20 ns.
2. Duration of the short circuit should not exceed 30 seconds. Not more than one output should be shorted at one time.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	7C182–20		7C182–25		7C182–35		7C182–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[4]										
t_{RC}	Read Cycle Time	20		25		35		45		ns
t_{AA}	Address to Data Valid		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ Access Time		20		25		35		45	ns
t_{ACE2}	CE_2 Access Time		20		25		35		45	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z	5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	5		5		5		5		ns
t_{HZCE1}	$\overline{CE}_1$ HIGH to High Z[5]		15		18		20		25	ns
t_{HZCE2}	CE_2 LOW to High Z[5]		15		18		20		25	
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25	ns
t_{DOE}	$\overline{OE}$ Access Time		15		18		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		15		18		20		25	ns
WRITE CYCLE[6]										
t_{WC}	Write Cycle Time	20		25		35		45		ns
t_{SA}	Address Set-Up Time	0		0		0		0		ns
t_{AW}	Address Valid to End of Write	15		20		30		40		ns
t_{SD}	Data Set-Up Time	10		15		20		25		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		30		40		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		30		ns
t_{HA}	Address Hold from End of Write	0		0		0		0		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{LZWE}	Write HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	Write LOW to High Z[5,7,8]		13		13		15		20	ns

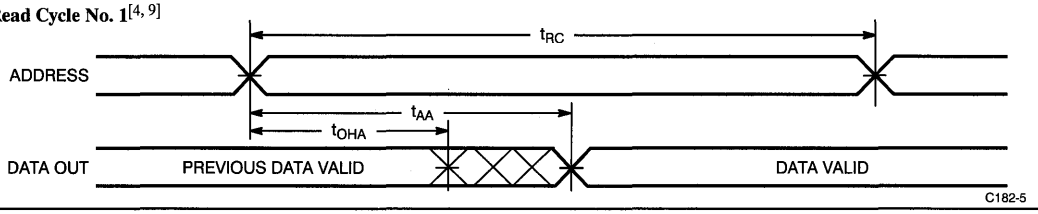
Shaded area contains advanced information.

Notes:

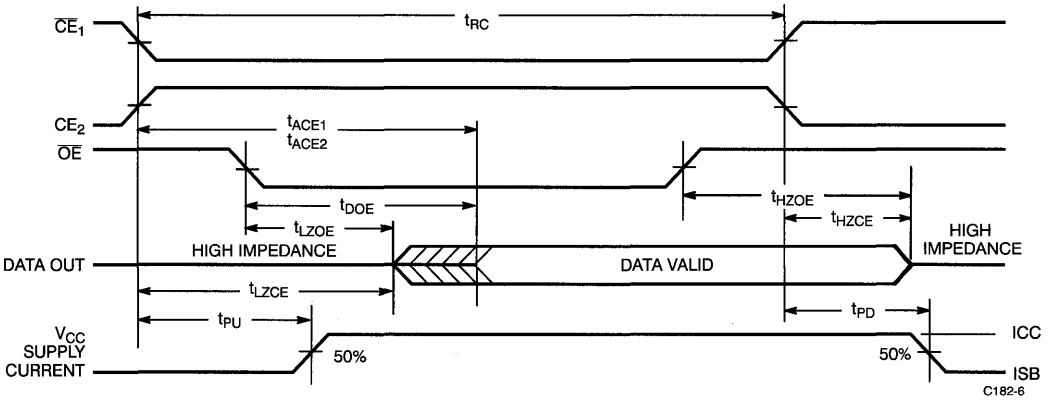
4. $\overline{WE}$ is HIGH for read cycle.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF. Transition is measured ± 500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms

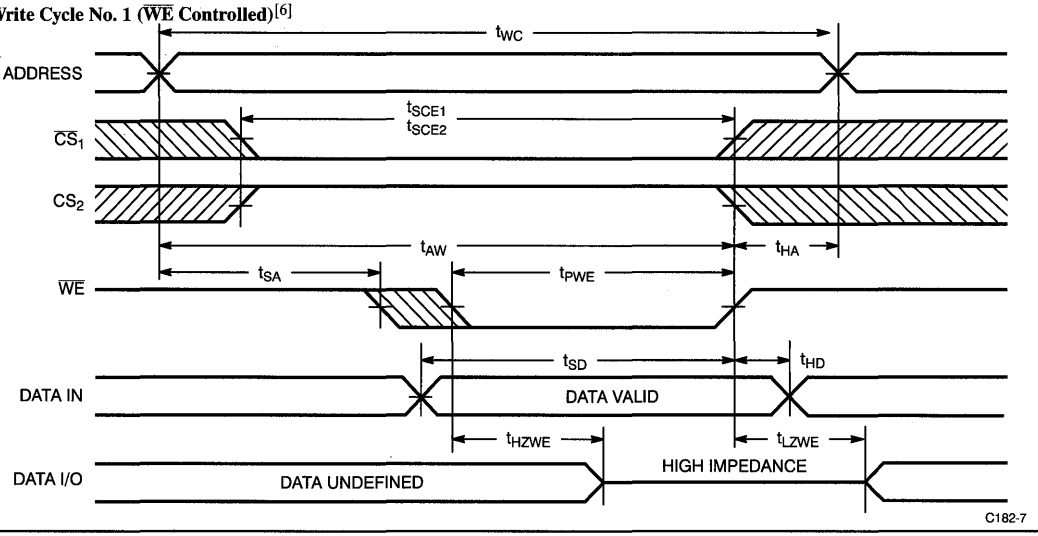
Read Cycle No. 1[4, 9]



Read Cycle No. 2[4, 10]



Write Cycle No. 1 (WE Controlled)[6]

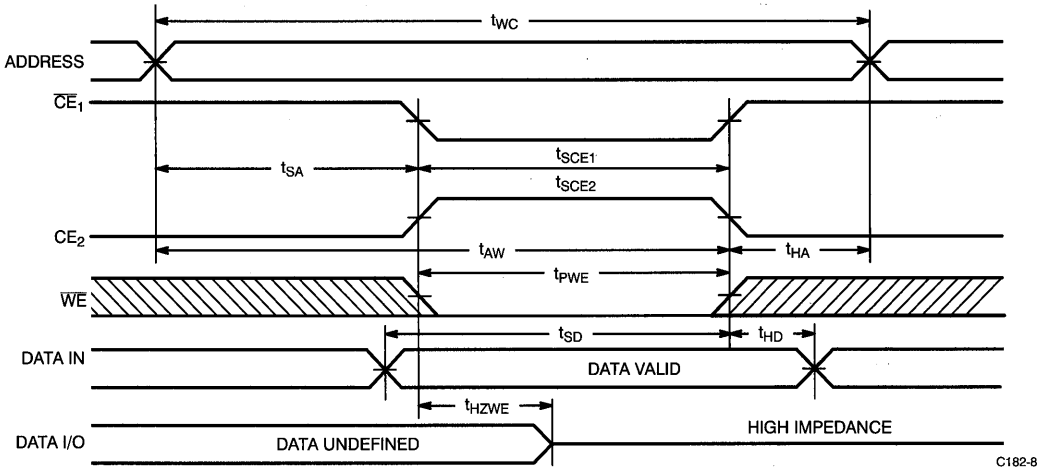


Notes:

9. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}. CE_2 = V_{IH}.
10. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[6, 10]



Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Data In	Data Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C182–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–20VC	V21	28-Lead Molded SOJ	
25	CY7C182–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–25VC	V21	28-Lead Molded SOJ	
35	CY7C182–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–35VC	V21	28-Lead Molded SOJ	
45	CY7C182–45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–45VC	V21	28-Lead Molded SOJ	

Shaded area contains advanced information.

Document #: 38–00110–E

CYPRESS SEMICONDUCTOR

CY7B185

8K x 8 Static RAM

Features

- **BiCMOS for optimum speed/power**
- **Ultra high speed**
  —9 ns
- **Low active power**
  —750 mW
- **Low standby power**
  —250 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

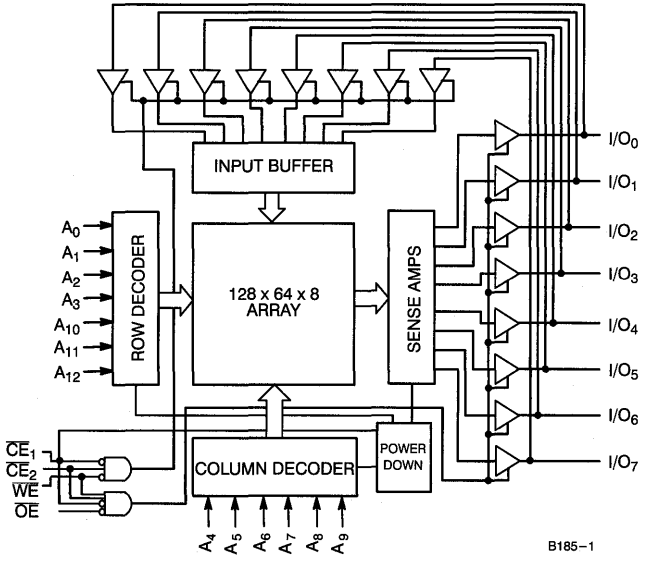
Functional Description

The CY7B185 is a high-performance BiCMOS static RAM organized as 8K words by 8 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have a power-down feature ($\overline{CE}_1$) that reduces the power consumption by 67% when deselected. The CY7B185 is in the space saving 300-mil-wide DIP and SOJ package and leadless chip carrier.

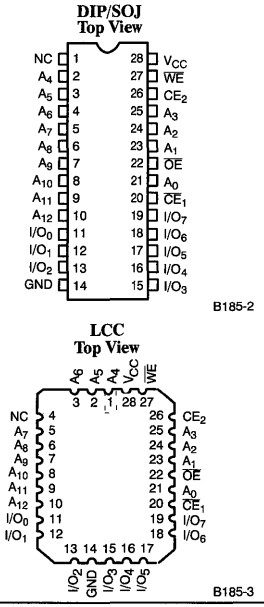
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configurations



Selection Guide

		7B185–9	7B185–10	7B185–12	7B185–15
Maximum Access Time (ns)		9	10	12	15
Maximum Operating Current (mA)	Commercial	150	145	140	135
	Military		155	150	145
Maximum Standby Current (mA)	Commercial	50	45	40	40
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

Input Voltage[1] ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7B185−9 Min.	7B185−9 Max.	7B185−10 Min.	7B185−10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		150		145	mA
				Mil				155	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ 3V, I_{OUT}=0mA, Other Inputs = <0.8V or >3V, V_{CC}=Max.		Com'l		50		45	mA
				Mil				60	mA

Parameter	Description	Test Conditions			7B185−12 Min.	7B185−12 Max.	7B185−15 Min.	7B185−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		140		135	mA
				Mil		150		145	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ 3V, I_{OUT}=0mA, Other Inputs = <0.8V or >3V, V_{CC}=Max		Com'l		40		40	mA
				Mil		55		50	mA

Shaded area contains preliminary information.

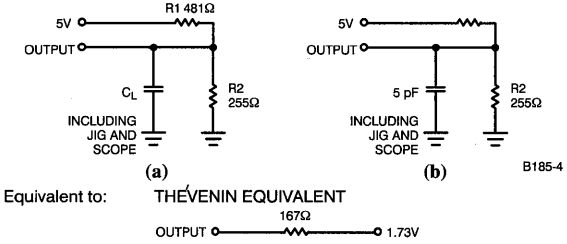
Capacitance[4]

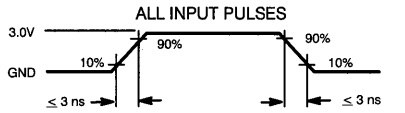
Parameter	Description	Test Conditions	Max.[5]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

Notes:

1. V_{IL} (min.) = − 3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CERDIP (D22), which has maximums of C_{IN} = 9.5 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[3,6]

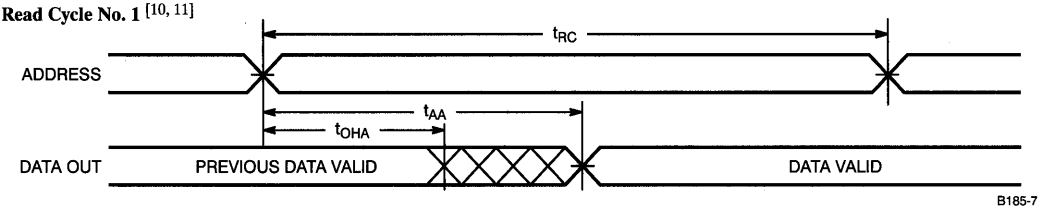
Parameter	Description	7B185–9		7B185–10		7B185–12		7B185–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	9		10		12		15		ns
t_{AA}	Address to Data Valid		9		10		12		15	ns
t_{OHA}	Data Hold from Address Change	2.5		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		9		10		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		9		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4.5		5		6		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1.5		2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		4		5		6		7	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[8]	2		2		2		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z[8]	2		2		2		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[7, 8] CE_2 LOW to High Z		4		5		6		7	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	9		10		12		15		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		8		8		10		ns
t_{SCE2}	CE_2 HIGH to Write End	8		8		8		10		ns
t_{AW}	Address Set-Up to Write End	8		8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		8		10		ns
t_{SD}	Data Set-Up to Write End	4.5		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]	0	4	0	5	0	6	0	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		3		ns

Notes:

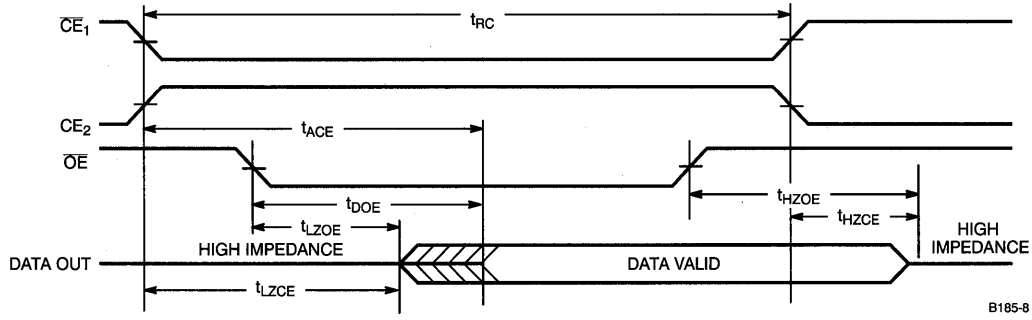
6. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage. This parameter is guaranteed and not 100% tested.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. This parameter is guaranteed and not 100% tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

Switching Waveforms

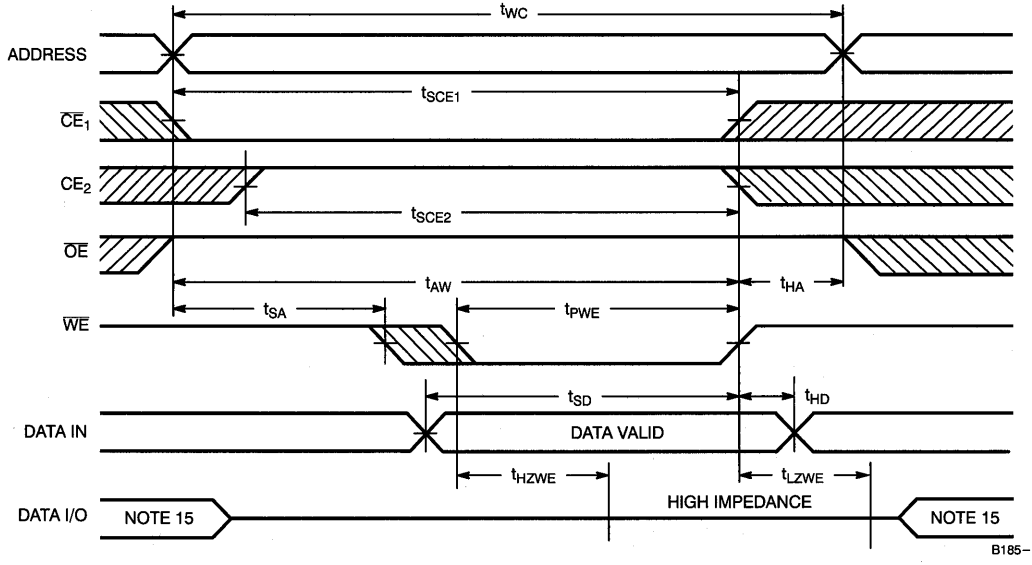
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [10, 11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [8, 13, 14]

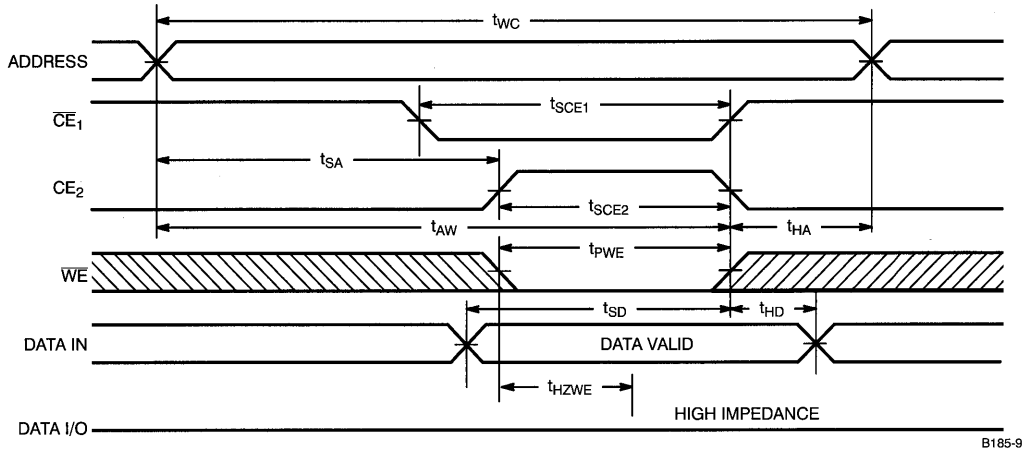


Notes:

10. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}. CE_2 = V_{IH}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
14. When data input is applied to the device I/O, the device output should be in the high-impedance state.
15. During this period, the I/Os are in the output state and input signals should not be applied.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 12, 14, 16]



Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
9	CY7B185–9VC	V21	28-Lead (300-Mil) Molded SOJ	
10	CY7B185–10DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B185–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B185–10VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B185–10DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B185–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B185–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B185–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B185–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B185–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B185–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B185–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B185–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B185–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B185–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B185–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-A-00016-F

CYPRESS SEMICONDUCTOR

CY7C185

8K x 8 Static RAM

Features

- **High speed**
  - **— 15 ns**
- **Fast t_{DOE}**
- **Low active power**
  - **— 715 mW**
- **Low standby power**
  - **— 220 mW**
- **CMOS for optimum speed/power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

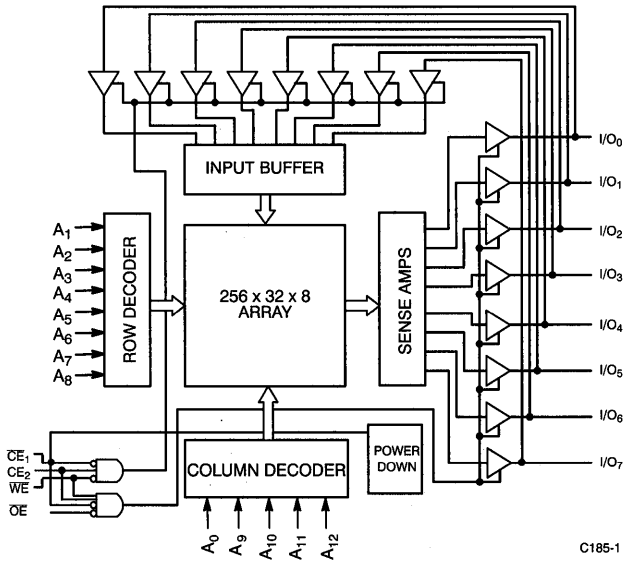
Functional Description

The CY7C185 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP and SOJ package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

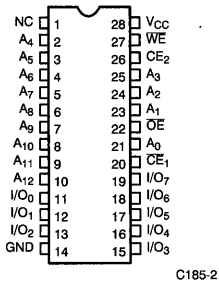
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration

DIP/SOJ
Top View



Selection Guide[1]

	7C185–12	7C185–15	7C185–20	7C185–25	7C185–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	140	130	110	100	100
Maximum Standby Current (mA)	40/15	40/15	20/15	20/15	20/15

Shaded areas contain advanced information.

Note:
1. For military specifications, see the CY7C185A/CY7C186A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to +7.0V

DC Input Voltage[2] ..... – 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C185–12		7C185–15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		140		130	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V		15		15	mA

Shaded areas contain advanced information.

Notes:

2. Minimum voltage is equal to –3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C185–20		7C185–25, 35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		110		100	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		20		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		15		15	mA

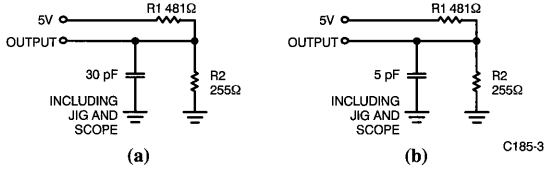
Capacitance[4]

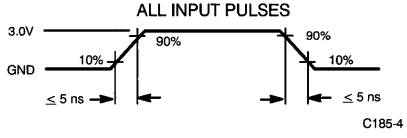
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

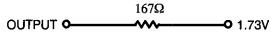
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C185–12		7C185–15		7C185–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		12		15		20	ns
t_{ACE2}	CE_2 HIGH to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		6		7		8	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[7]	3		3		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[6, 7] CE_2 LOW to High Z		6		7		8	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		12		15		ns
t_{SCE2}	CE_2 HIGH to Write End	8		12		15		ns
t_{AW}	Address Set-Up to Write End	9		12		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		ns
t_{SD}	Data Set-Up to Write End	6		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		6		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		ns

Shaded areas contain advanced information.

Notes:

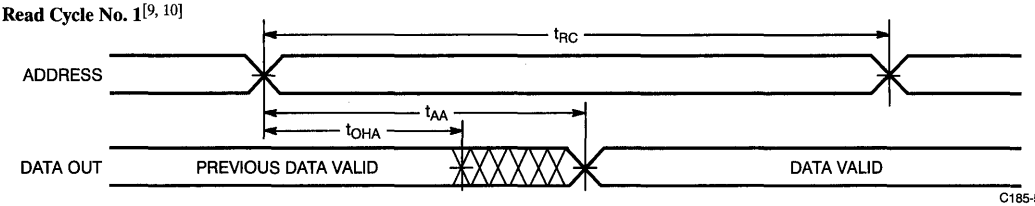
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[5] (continued)

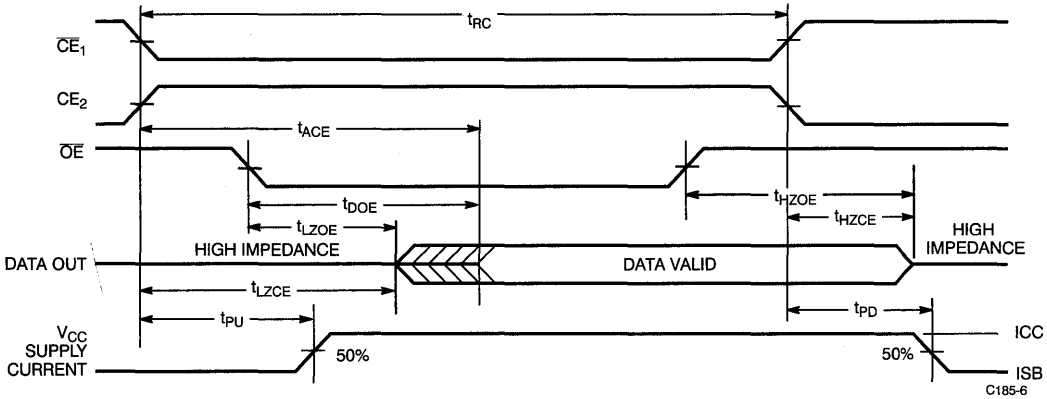
Parameter	Description	7C185–25		7C185–35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		25		35	ns
t_{ACE2}	CE_2 HIGH to Data Valid		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		10		10	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[7]	5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[6,7] CE_2 LOW to High Z		10		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20	ns
WRITE CYCLE[8]						
t_{WC}	Write Cycle Time	25		35		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	20		20		ns
t_{SCE2}	CE_2 HIGH to Write End	20		20		ns
t_{AW}	Address Set-Up to Write End	20		25		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		12		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		7		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		ns

Switching Waveforms

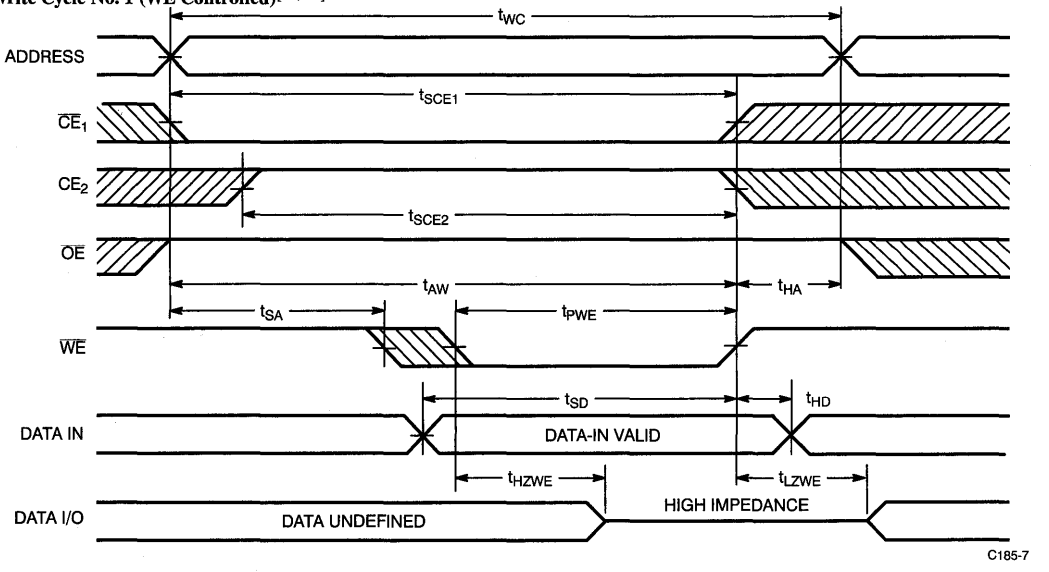
Read Cycle No. 1[9, 10]



Read Cycle No. 2[11, 12]



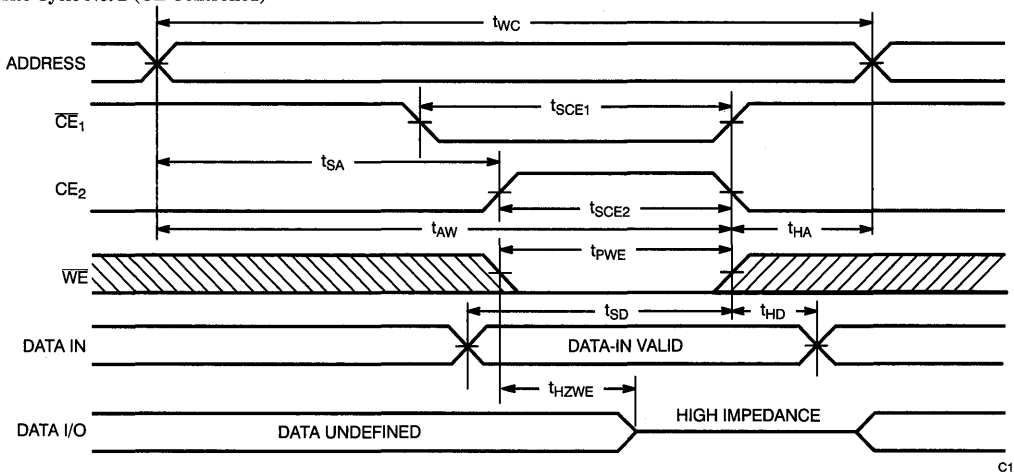
Write Cycle No. 1 (WE Controlled)[10, 12]



Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. $\overline{WE}$ is HIGH for read cycle.
12. Data I/O is High Z if $\overline{OE}$ = V_{IH}, $\overline{CE_1}$ = V_{IH}, or $\overline{WE}$ = V_{IL}.

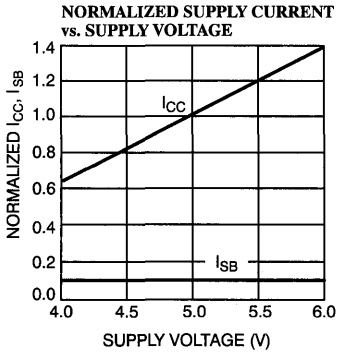
Switching Waveforms (continued)

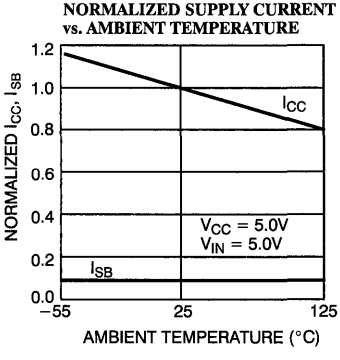
Write Cycle No. 2 ($\overline{CE}$ Controlled) [10, 12, 13]

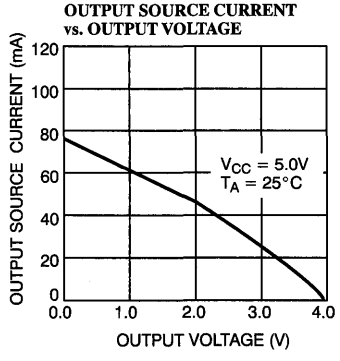


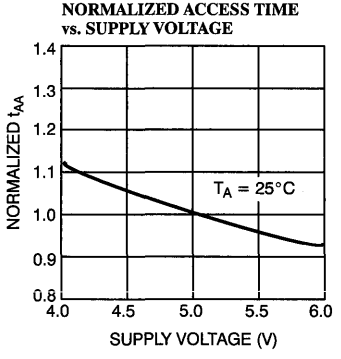
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

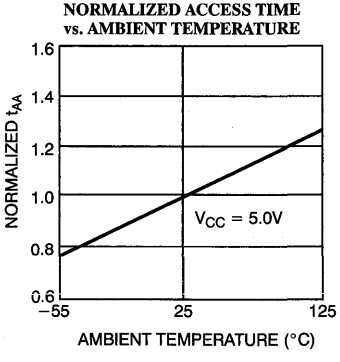
Typical DC and AC Characteristics

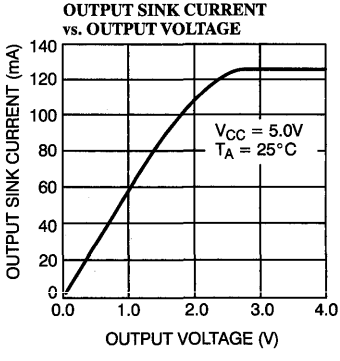






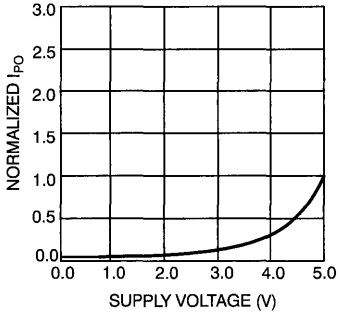




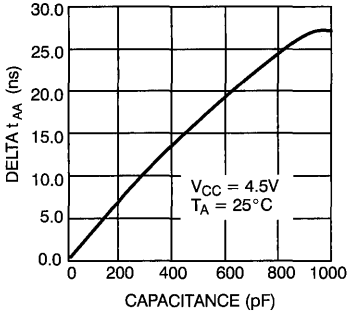


Typical DC and AC Characteristics (continued)

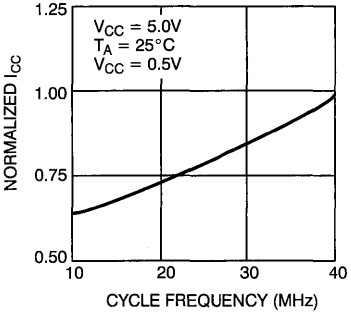
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C185–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–12VC	V21	28-Lead Molded SOJ	
15	CY7C185–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–15VC	V21	28-Lead Molded SOJ	
20	CY7C185–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–20VC	V21	28-Lead Molded SOJ	
25	CY7C185–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–25VC	V21	28-Lead Molded SOJ	
35	CY7C185–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–35VC	V21	28-Lead Molded SOJ	

Shaded areas contain advanced information.

Document #: 38–00037-I

CYPRESS SEMICONDUCTOR

CY7C185A

8K x 8 Static RAM

Features

- **High speed**
  - **20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **743 mW**
- **Low standby Power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**

Functional Description

The CY7C185A is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 70% when deselected. The CY7C185A is in the standard 300-mil-wide DIP package and leadless chip carrier.

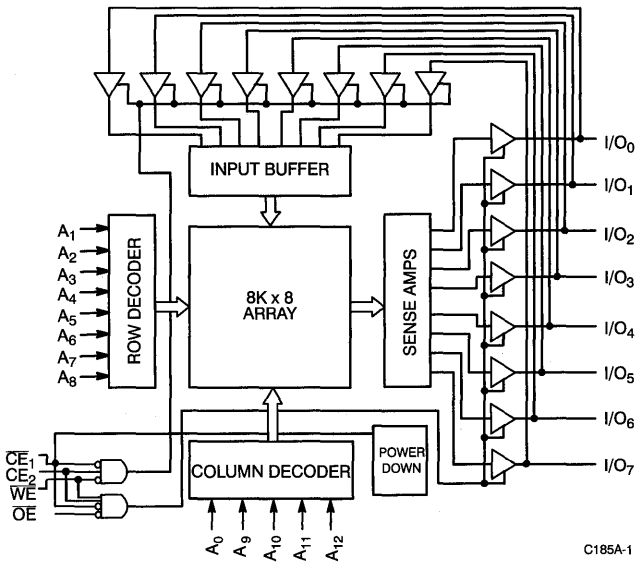
Writing to the device is accomplished when the chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

Reading the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in a high-impedance state when chip enable one ($\overline{CE}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

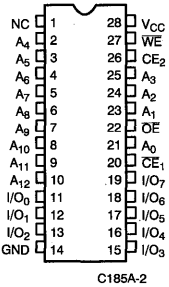
A die coat is used to insure alpha immunity.

Logic Block Diagram

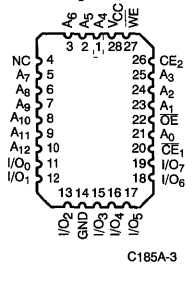


Pin Configurations

DIP
Top View



LCC
Top View



Selection Guide[1]

		7C185A–15	7C185A–20	7C185A–25	7C185A–35	7C185A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Military	170	135	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C185 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[4] ..... − 0.5V to +7.0V

DC Input Voltage[4] ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C185A−15 Min.	7C185A−15 Max.	7C185A−20 Min.	7C185A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[4]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Military		170		135	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

Shaded area contains advanced information.

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V (min.) = − 3.0V for pulse durations less than 30 ns.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

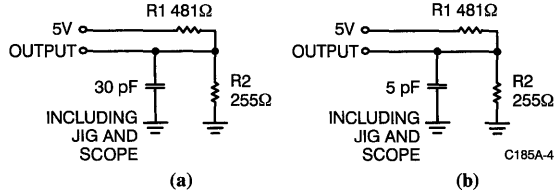
Parameter	Description	Test Conditions		7C185A–25 Min.	7C185A–25 Max.	7C185A–35, 45 Min.	7C185A–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[4]			– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 10	+10	– 10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		125		125	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC} $\overline{CE}_1$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

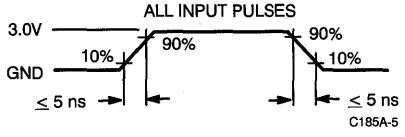
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

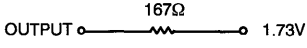
Note:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 7]

Parameter	Description	7C185A–15		7C185A–20		7C185A–25		7C185A–35		7C185A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		15		20		25		35		45	ns
t_{ACE2}	CE_2 HIGH to Data Valid		15		20		25		35		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8]		8		8		10		12		15	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[9]	3		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[8, 9] CE_2 LOW to High Z		8		8		10		15		15	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	10		15		20		25		30		ns
t_{SCE2}	CE_2 HIGH to Write End	10		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		7		7		7		10		15	ns

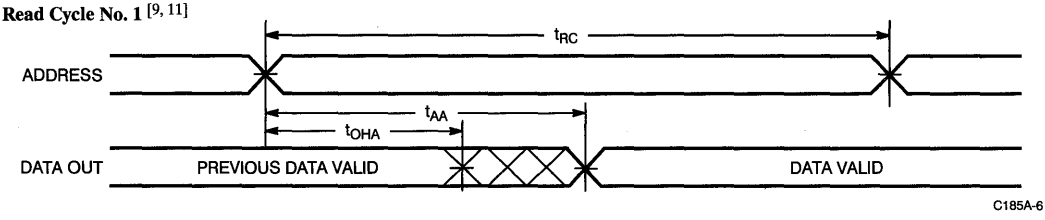
Shaded area contains advanced information.

Notes:

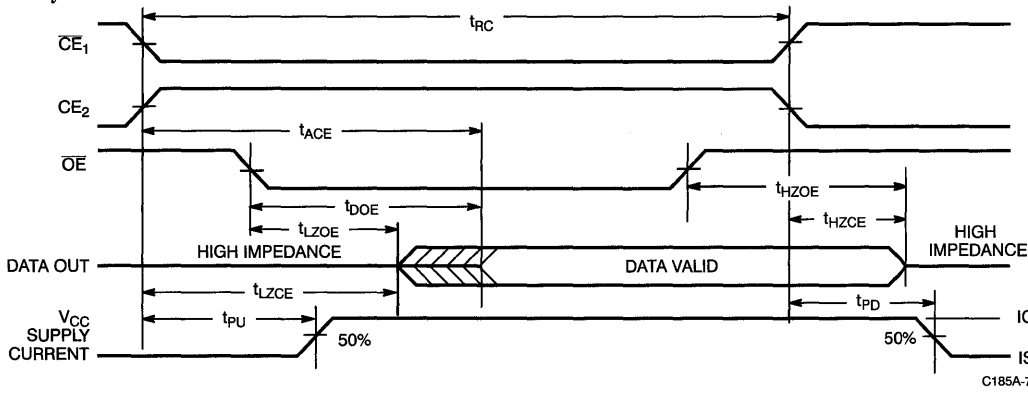
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.

Switching Waveforms

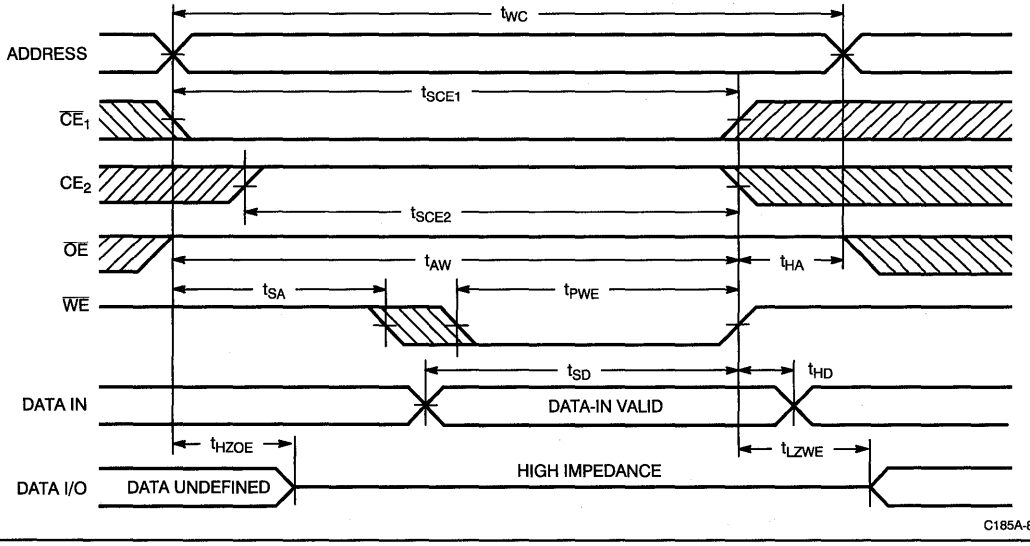
Read Cycle No. 1 [9, 11]



Read Cycle No. 2 [11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [13, 14]

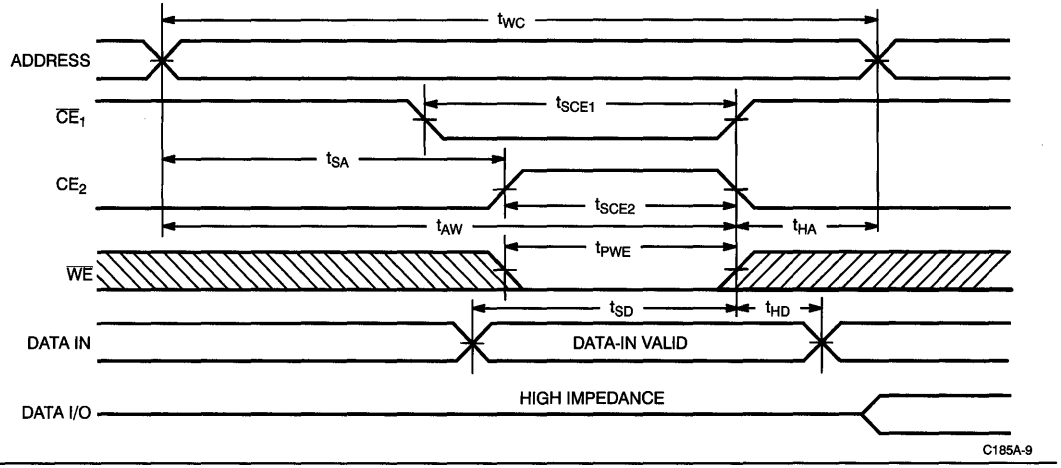


Notes:

11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. $\overline{WE}$ is HIGH for read cycle.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

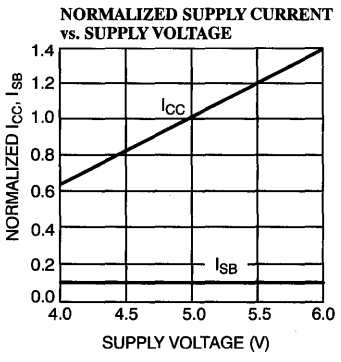
Switching Waveforms (continued)

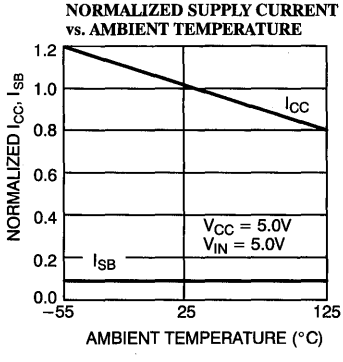
Write Cycle No. 2 ($\overline{CE}$ Controlled) [13, 14, 15]

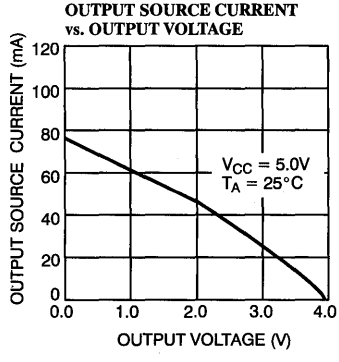


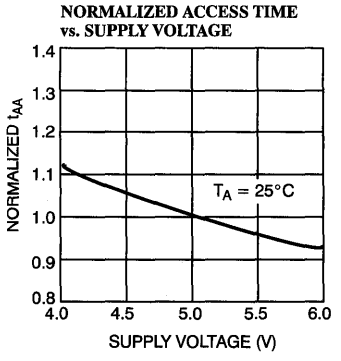
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

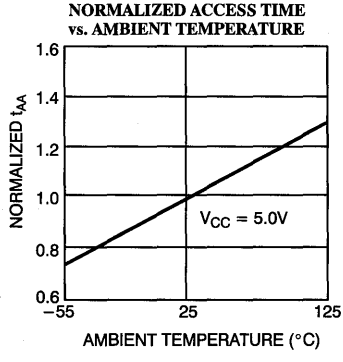
Typical DC and AC Characteristics

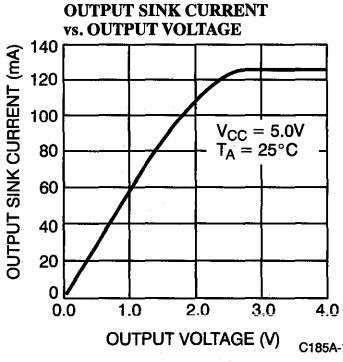




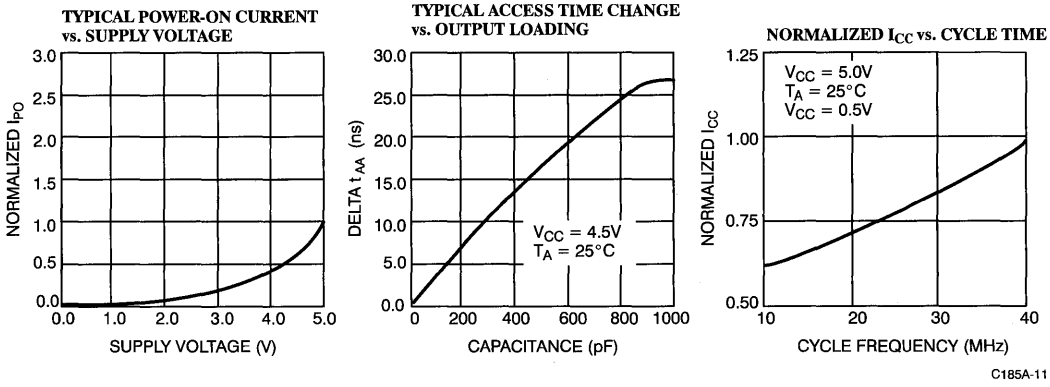








Typical DC and AC Characteristics (continued)



C185A-11

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C185A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C185A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C185A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C185A–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE1}	7, 8, 9, 10, 11
t_{ACE2}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE1}	7, 8, 9, 10, 11
t_{SCE2}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00114–B

Features

- **High speed**
  — **15 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  — **495 mW**
- **Low standby power**
  — **220 mW**
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

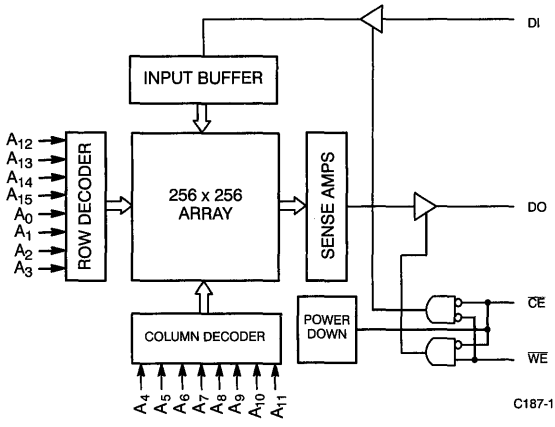
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

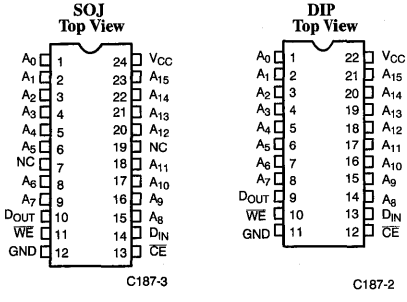
The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C187 utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide[1]

	7C187–12	7C187–15	7C187–20	7C187–25	7C187–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	90	80	70	70
Maximum Standby Current (mA)	40/40	40/20	40/20	20/20	20/20

Shaded area indicates advanced information.

Note:
1. For military specifications, see the CY7C187A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... − 0.5V to +7.0V

DC Input Voltage[2] ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C187−12		7C187−15		7C187−20		7C187−25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		− 0.5	0.8	− 0.5	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	− 10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	− 10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		90		80		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		40		40		40		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20		20		20	mA

Shaded area indicates advanced information.

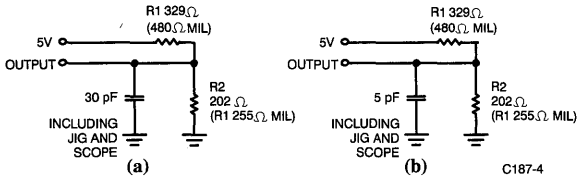
Capacitance[5]

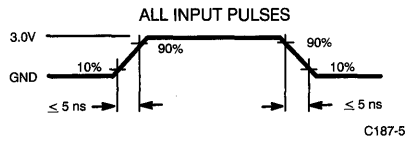
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

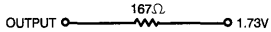
2. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

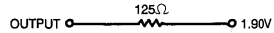




Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

Switching Characteristics Over the Operating Range[6]

Parameters	Description	7C187–12		7C187–15		7C187–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Output Hold from Address Change	3		3		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		7		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		12		15		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		12		15		ns
t_{AW}	Address Set-up to Write End	9		12		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		ns
t_{SD}	Data Set-up to Write End	6		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		6		7		7	ns

Shaded area indicates advanced information.

Notes:

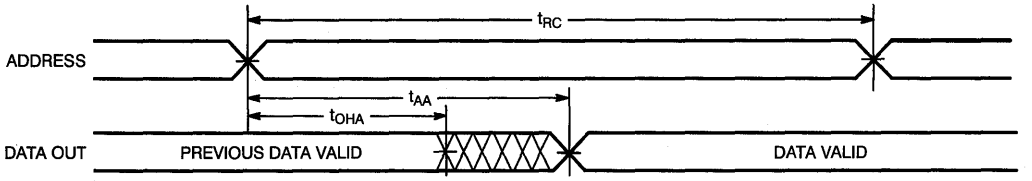
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.

Switching Characteristics Over the Operating Range[6] (continued)

Parameters	Description	7C187–25		7C187–35		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20	ns
WRITE CYCLE[9]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		ns
t_{AW}	Address Set-Up to Write End	20		25		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low[9]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		10	ns

Switching Waveforms

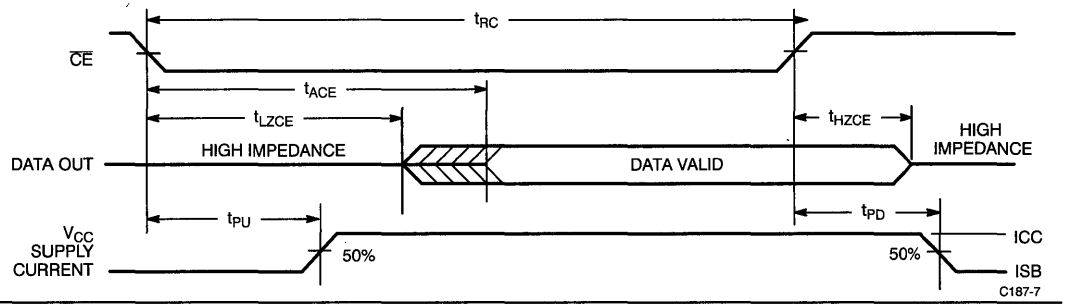
Read Cycle No. 1[10, 11]



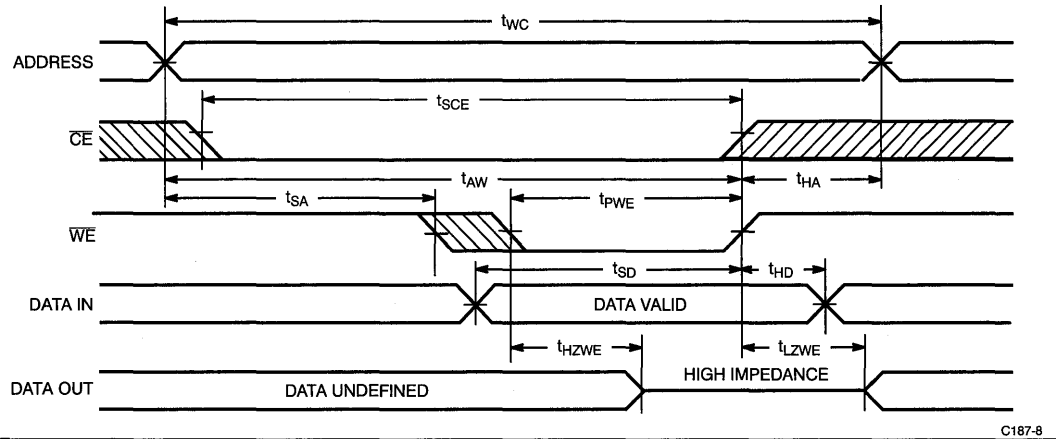
Note:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms

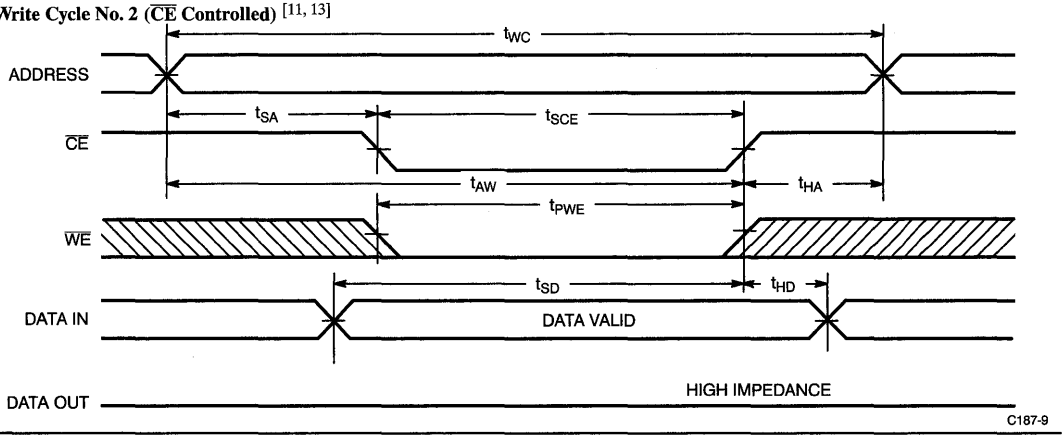
Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Write Cycle No. 2 ($\overline{CE}$ Controlled) [11, 13]

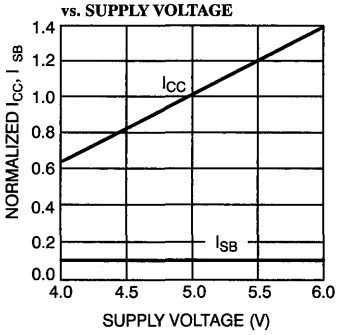


Note:

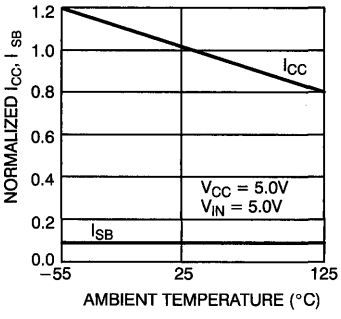
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

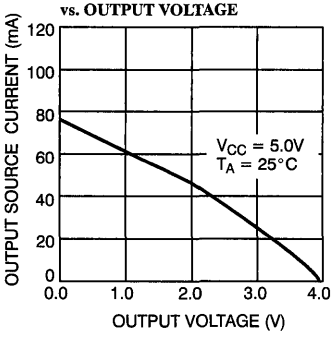
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



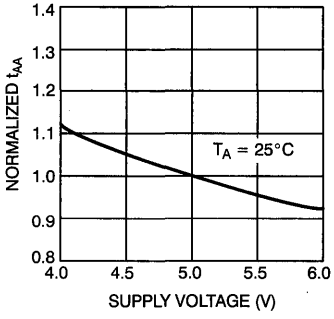
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



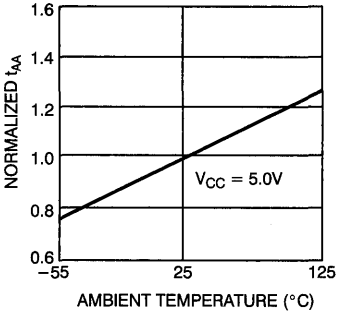
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



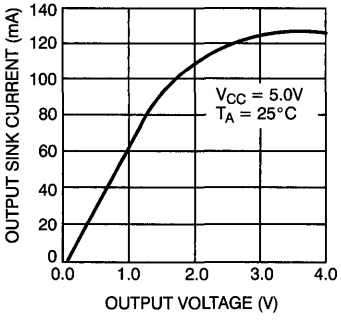
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



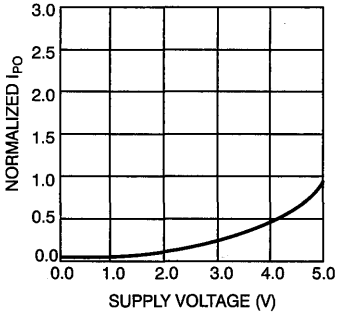
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



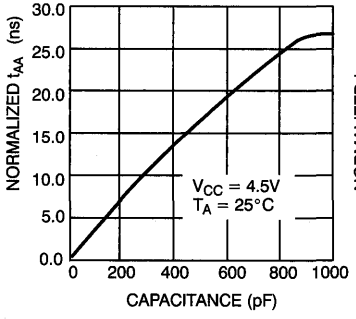
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



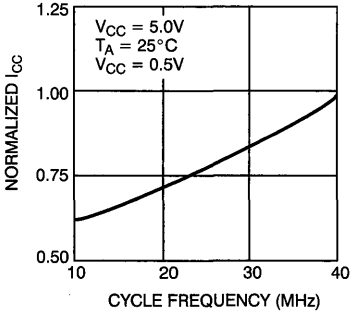
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information[14]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C187–12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187–12VC	V13	24-Lead Molded SOJ	
15	CY7C187–15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187–15VC	V13	24-Lead Molded SOJ	
20	CY7C187–20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187–20VC	V13	24-Lead Molded SOJ	
25	CY7C187–25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187–25VC	V13	24-Lead Molded SOJ	
35	CY7C187–35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187–35VC	V13	24-Lead Molded SOJ	

Shaded area contains advanced information.

Note:
14. For military variations, see the CY7C187A datasheet.

Document #: 38–00038–I

CYPRESS SEMICONDUCTOR

CY7C187A

64K x 1 Static R/W RAM

Features

- **High speed**
  - **20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **495 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 55% when deselected.

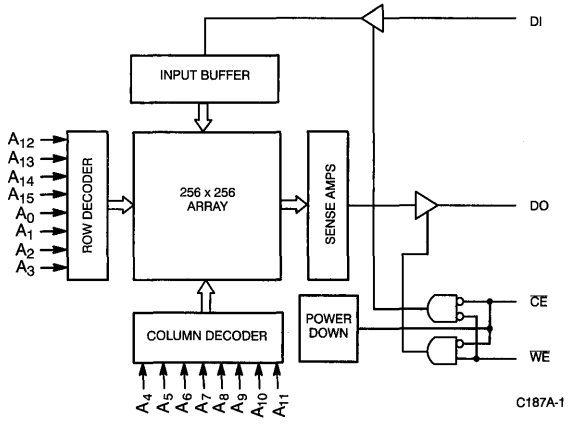
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

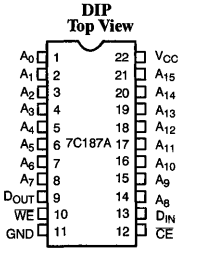
The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

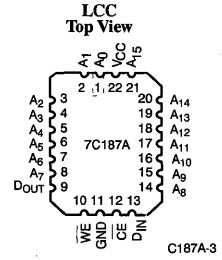
The 7C187A utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations





Selection Guide[1]

		7C187A–15	7C187A–20	7C187A–25	7C187A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	90	80	80
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see CY7C187 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... − 0.5V to +7.0V

DC Input Voltage[2] ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C187A−15 Min.	7C187A−15 Max.	7C187A−20 Min.	7C187A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		160		90	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Mil		40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Mil		20		20	mA

Shaded area contains advanced information.

Notes:

2. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range[4] (continued)

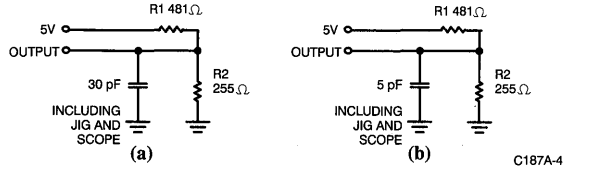
Parameter	Description	Test Conditions		7C187A–25 Min.	7C187A–25 Max.	7C187A–35 Min.	7C187A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		80		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current[6]	Max. V_{CC}, $\overline{CE} \ge V_{IH}$	Mil		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power Down Current[6]	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$	Mil		20		20	mA

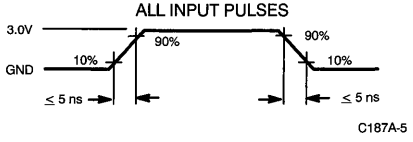
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

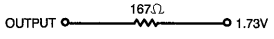
Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 8]

Parameter	Description	7C187A–15		7C187A–20		7C187A–25		7C187A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7		7		10	ns

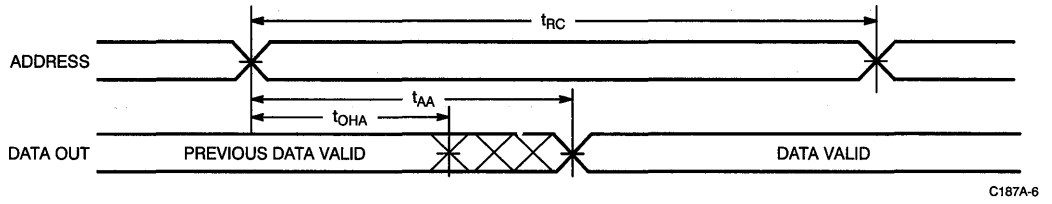
Shaded area contains advanced information.

Notes:

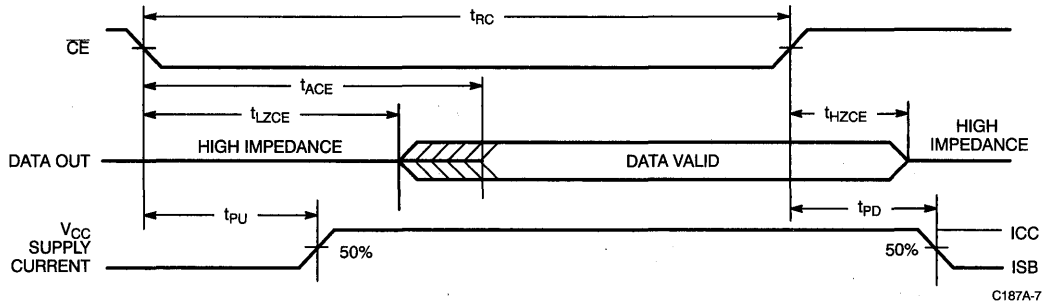
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

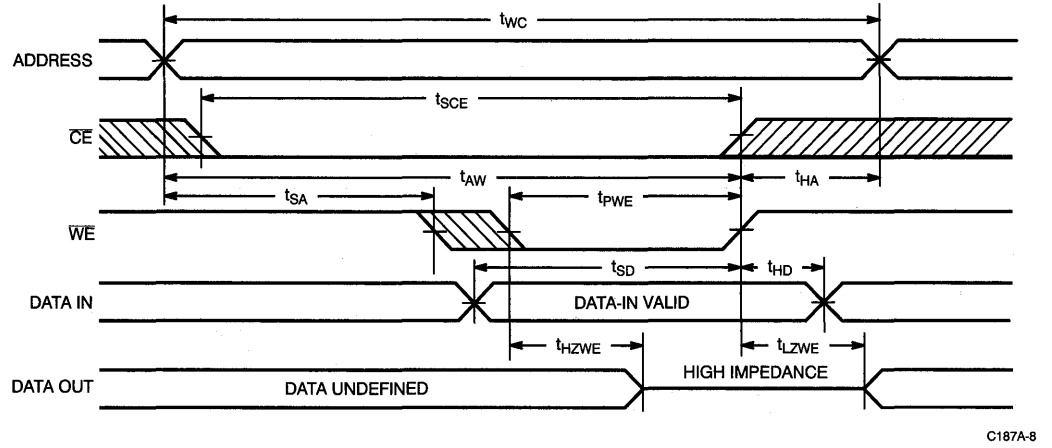
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



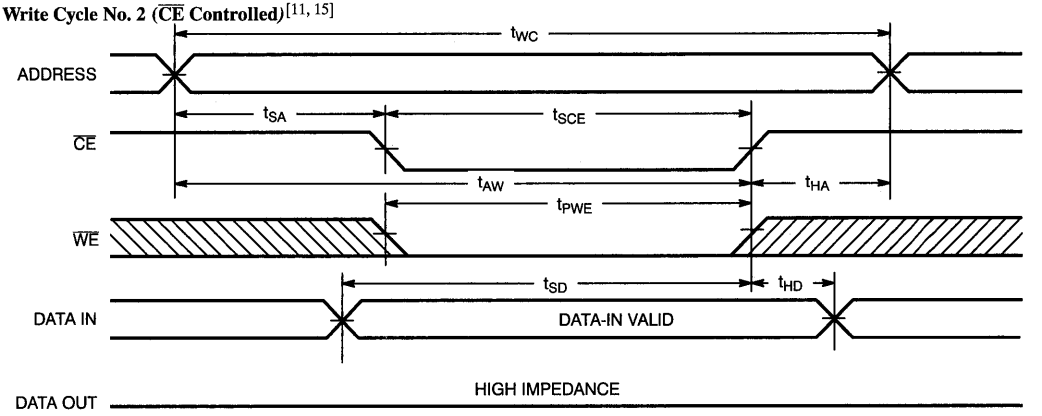
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE} = V_{IL}$.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

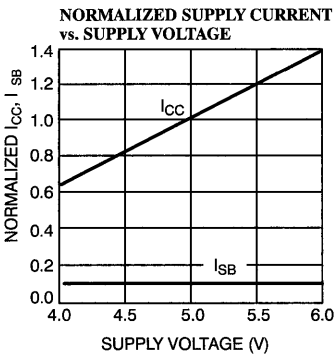
Switching Waveforms (continued)

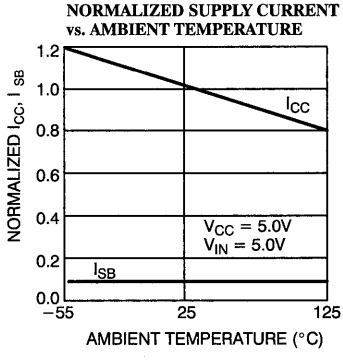
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15]

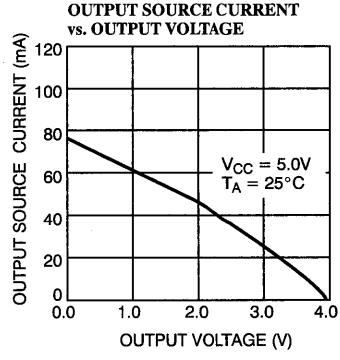


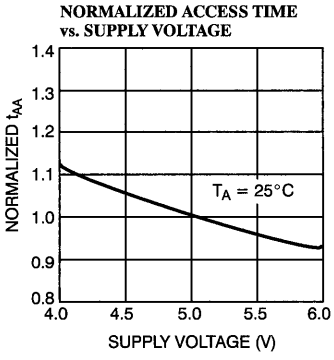
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

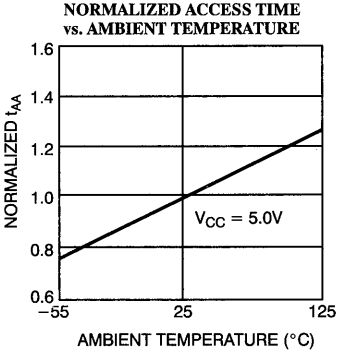
Typical DC and AC Characteristics

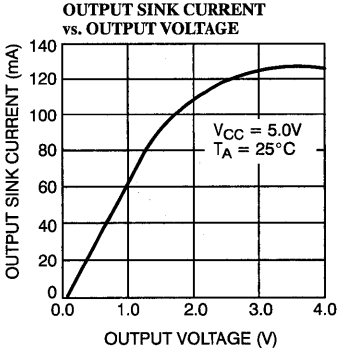






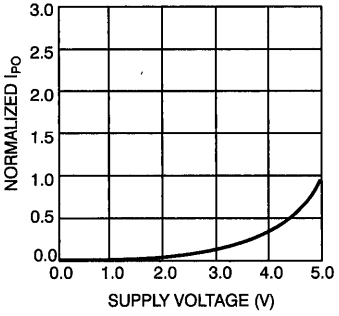




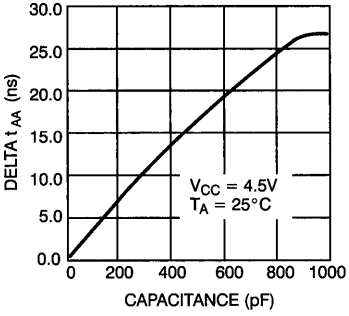


Typical DC and AC Characteristics (continued)

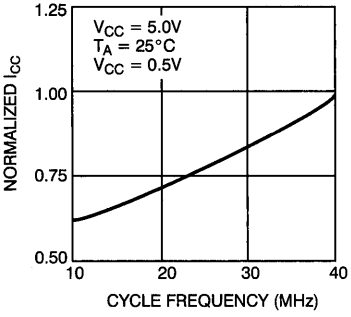
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C187A–15DMB	D10	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
20	CY7C187A–20DMB	D10	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–20LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
25	CY7C187A–25DMB	D10	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–25LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
35	CY7C187A–35DMB	D10	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–35LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00115–C

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C188**

32K x 9 Static RAM

Features

- **High speed**
  — 12 ns
- **Automatic power-down when deselected**
- **Low active power**
  — 965 mW
- **Low standby power**
  — 220 mW
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**

Functional Description

The CY7C188 is a high-performance CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is provided by an active-LOW chip enable ($\overline{CE}_1$), an active-HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking $\overline{CE}_1$ and write enable ($\overline{WE}$) inputs LOW and CE_2 input HIGH. Data on the nine I/O pins (I/O_0 – I/O_8) is then written into the location specified on the address pins (A_0 – A_{14}).

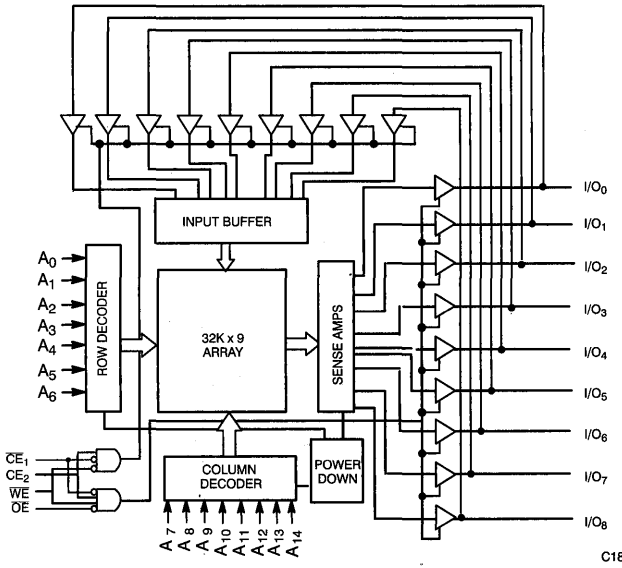
Reading from the device is accomplished by taking $\overline{CE}_1$ and $\overline{OE}$ LOW while forcing $\overline{WE}$ and CE_2 HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins (I/O_0 – I/O_8) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C188 is available in standard 300-mil-wide DIPs and SOJs.

A die coat is used to ensure alpha immunity.

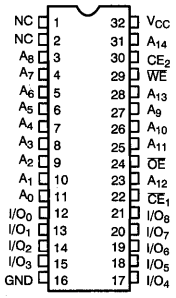
Logic Block Diagram



C188–1

Pin Configuration

DIP/SOJ
Top View



C188–2

Selection Guide

		7C188–12	7C188–15	7C188–20	7C188–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	175	165	155	145
	Military		185	170	165
Maximum Standby Current (mA)		40	40	40	35

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND (Pin 32 to Pin 16) ..... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C188−12 Min.	7C188−12 Max.	7C188−15 Min.	7C188−15 Max.	7C188−20 Min.	7C188−20 Max.	7C188−25 Min.	7C188−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+1	− 1	+1	− 1	+1	− 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	− 300		mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		175		165		155		145	mA
			Mil				185		170		165	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		40		40		40		35	mA
			Mil				40		40		35	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ −0.3V or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V or $V_{IN} \leq$ 0.3V, f = 0	Com'l		10		10		10		10	mA
			Mil				15		15		15	mA

Shaded areas contain advanced information.

Notes:

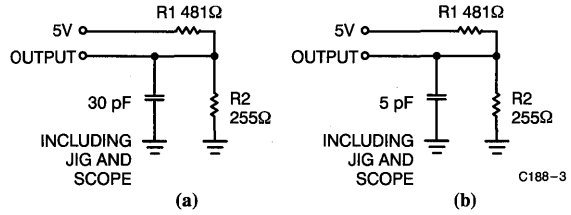
1. Minimum voltage is equal to −2.0V for pulse durations less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

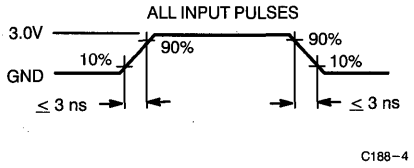
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{IN}: Controls			8	pF
C_{OUT}	Output Capacitance		8	pF

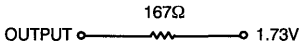
Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[6, 7]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

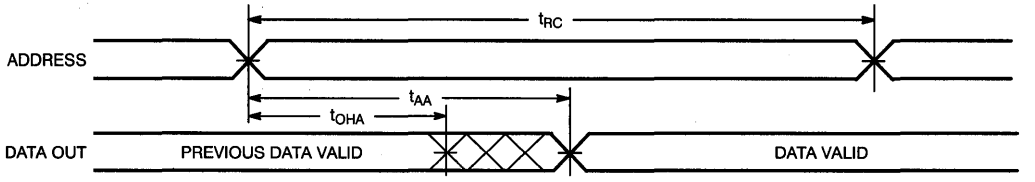
Parameter	Description	7C188–12		7C188–15		7C188–20		7C188–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Data Valid		12		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		7		7	ns
t_{LZCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[7, 8]		6		7		8		8	ns
t_{PU}	$\overline{CE}_1$ LOW or CE_2 HIGH to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-Down		12		15		20		25	ns
WRITE CYCLE[9, 10]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Write End	9		10		12		15		ns
t_{AW}	Address Set-Up to Write End	9		10		12		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	9		10		12		15		ns
t_{SD}	Data Set-Up to Write End	8		9		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7, 8]	3		3		3		3		ns

Notes:

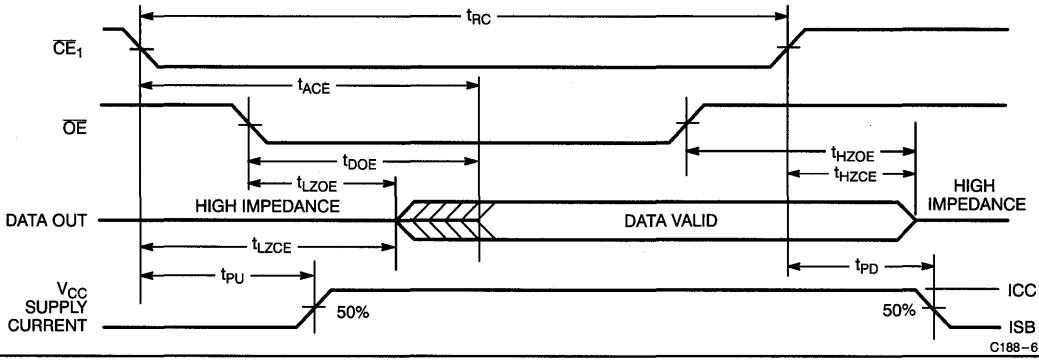
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

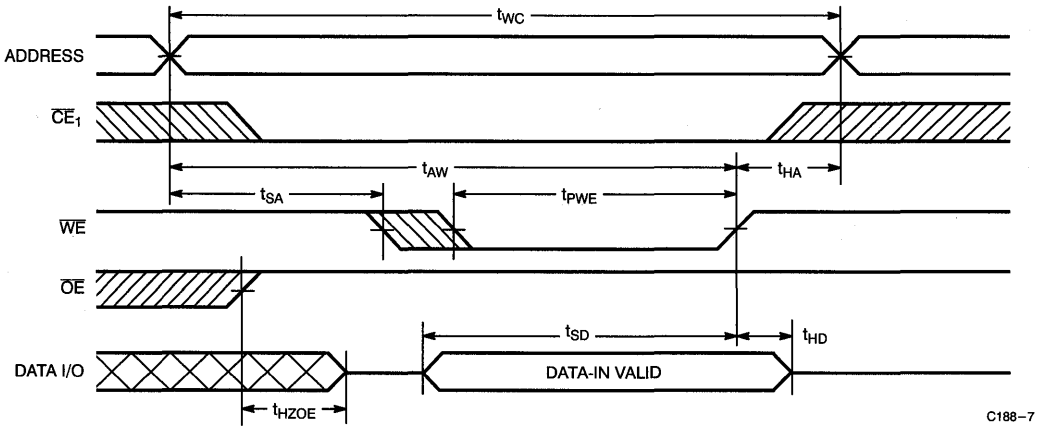
Read Cycle No. 1[11, 12]



Read Cycle No. 2 (Chip-Enable Controlled)[12, 13, 14]



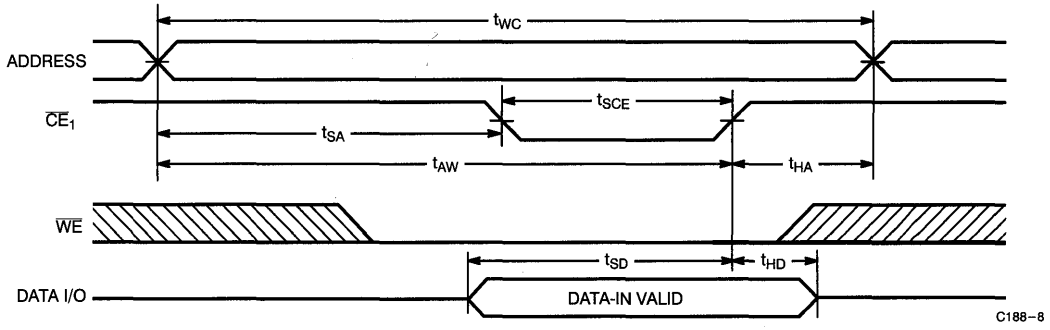
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 14, 15, 16]



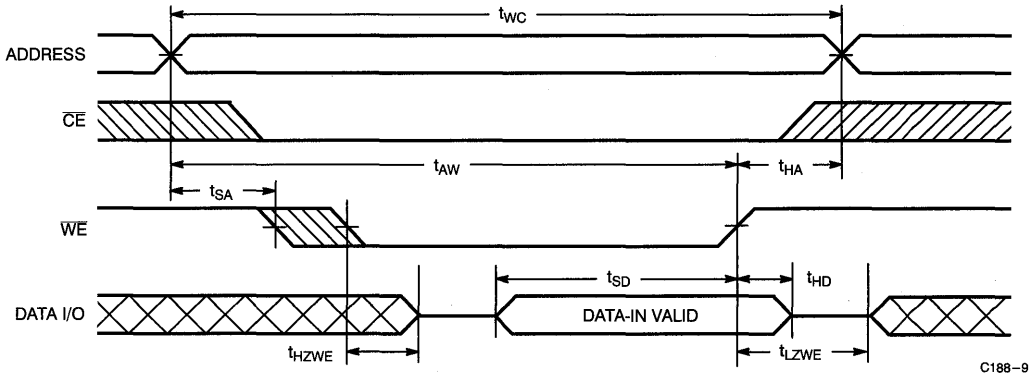
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Timing parameters are the same for all chip enable signals ($\overline{CE}_1$ and CE_2), so only the timing for $\overline{CE}_1$ is shown.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 14, 15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 14, 16]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C188-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C188-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C188-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C188-25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00220-B

CY7B191
CY7B192

64K x 4 Static R/W RAM with Separate I/O

Features

- **High speed**
  - **— 10 ns t_{AA}**
- **Automatic power-down when deselected**
- **Transparent write (7B191)**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 850 mW**
- **Low standby power**
  - **— 200 mW**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B191 and CY7B192 are high-performance BiCMOS static RAMs organized as 64K words by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 60% when deselected.

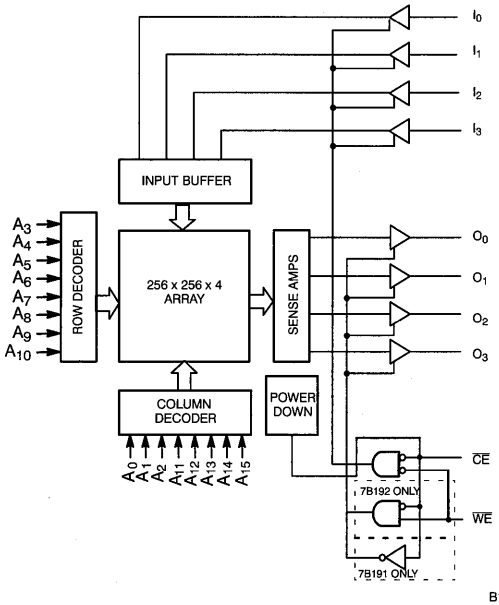
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data output pins.

The four output pins (O_0 through O_3) are in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). During a write operation ($\overline{WE}$ and $\overline{CE}$ LOW), the outputs of the 7B192 are in a high-impedance state and the outputs of the 7B191 track the inputs after a specified delay.

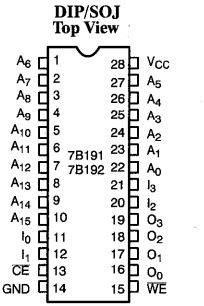
The CY7B191 and CY7B192 are available in space-saving 300-mil-wide DIPs and SOJs.

Logic Block Diagram



B191–1

Pin Configuration



B191–2

Selection Guide

		7B191–10 7B192–10	7B191–12 7B192–12	7B191–15 7B192–15	7B191–20 7B192–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	170	160	150	
	Military		170	160	160
Maximum Standby Current (mA)	Commercial	40	35	30	
	Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		.7B191−10 7B192−10 Min.	.7B191−10 7B192−10 Max.	7B191−12 7B192−12 Min.	7B191−12 7B192−12 Max.	7B191−15, 20 7B192−15, 20 Min.	7B191−15, 20 7B192−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		170		160		150	mA
			Mil				170		160	
I_{SB}	Automatic CE Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		40		35		30	mA
			Mil				40		40	

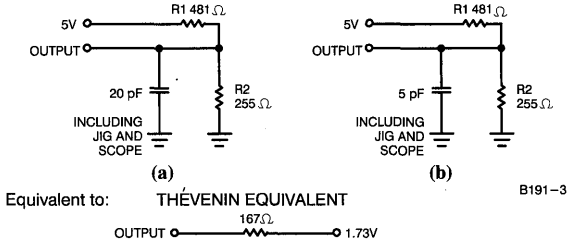
Capacitance[5]

Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}, $C_{I/O}$	Output Capacitance		8	pF

Notes:

1. $V_{IL\,(min.)}$ = − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For PDIP (P21) and CDIP (D22), C_{IN}=C_{OUT}=10pF.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics[3,7] Over the Operating Range

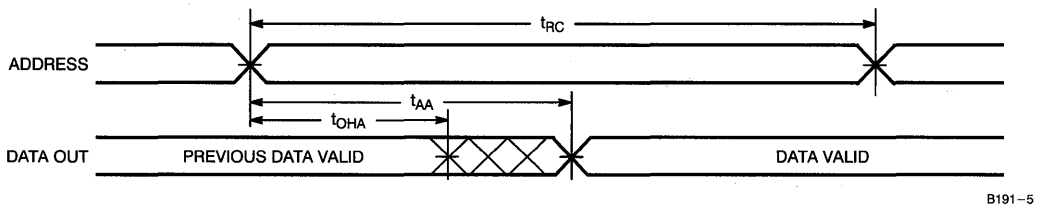
Parameter	Description	7B191-10 7B192-10		7B191-12 7B192-12		7B191-15 7B192-15		7B191-20 7B191-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[10]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8,9]		6		7		7		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7B191)		10		12		15		20	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7B191)		10		12		15		20	ns
t_{ADV}	Data Valid to Output Valid (7B191)		10		12		15		20	ns

Notes:

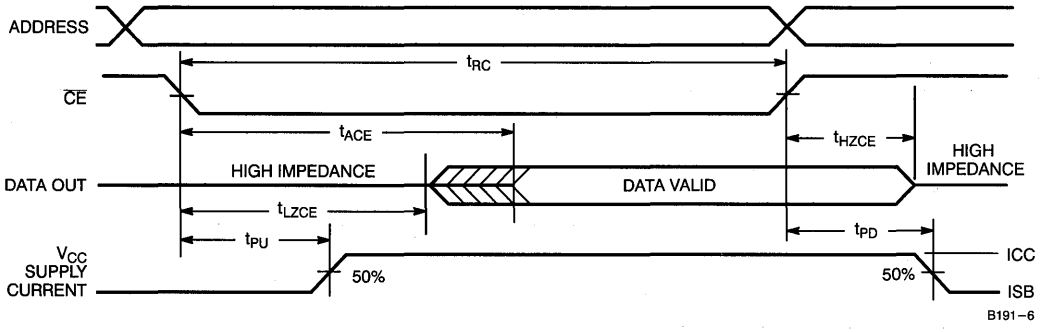
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
9. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

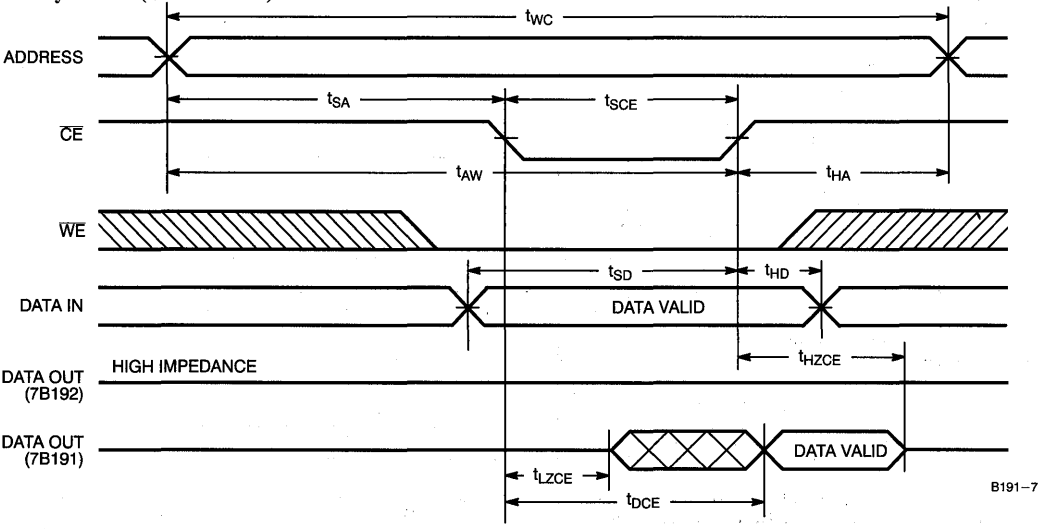
Read Cycle No. 1[11,12]



Read Cycle No. 2[12,13]



Write Cycle No. 1 ($\overline{CE}$ Controlled)[14]

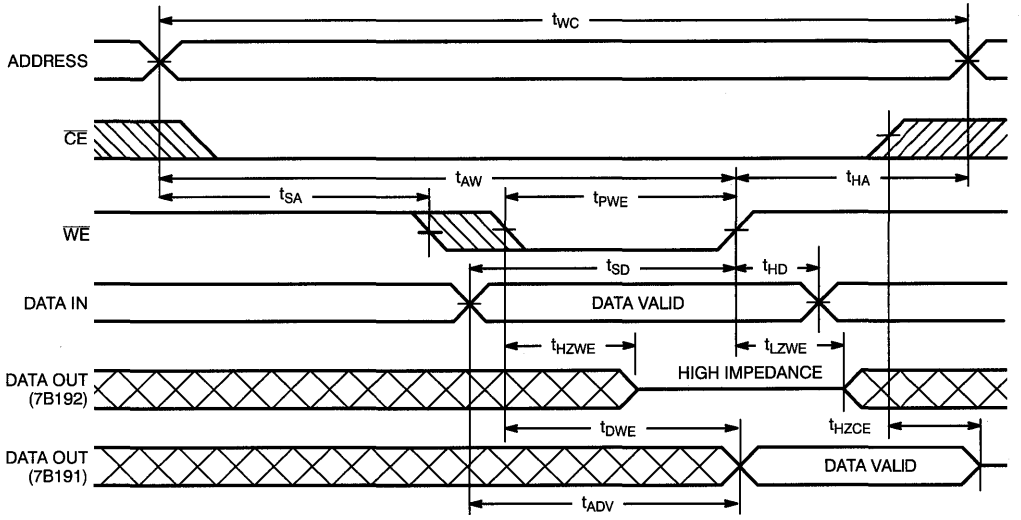


Notes:

11. Device is continuously selected. $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



B191-8

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7B192: Standard Write	Active (I_{CC})
L	L	Data In	7B191: Transparent Write[15]	Active (I_{CC})

Notes:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B191-10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B191-10VC	V21	28-Lead Molded SOJ	
12	CY7B191-12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B191-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B191-12VC	V21	28-Lead Molded SOJ	
	CY7B191-12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B191-15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B191-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B191-15VC	V21	28-Lead Molded SOJ	
	CY7B191-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B191-20DMB	D22	28-Lead (300-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B192–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–10VC	V21	28-Lead Molded SOJ	
12	CY7B192–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B192–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–12VC	V21	28-Lead Molded SOJ	
	CY7B192–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B192–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B192–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B192–15VC	V21	28-Lead Molded SOJ	
	CY7B192–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B192–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}	7, 8, 9, 10, 11

Note:
16. 7B191 only.

Document #: 38–00156–C

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C191
CY7C192

64K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **— 12 ns**
- **Transparent write (7C191)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C191 and CY7C192 are high-performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

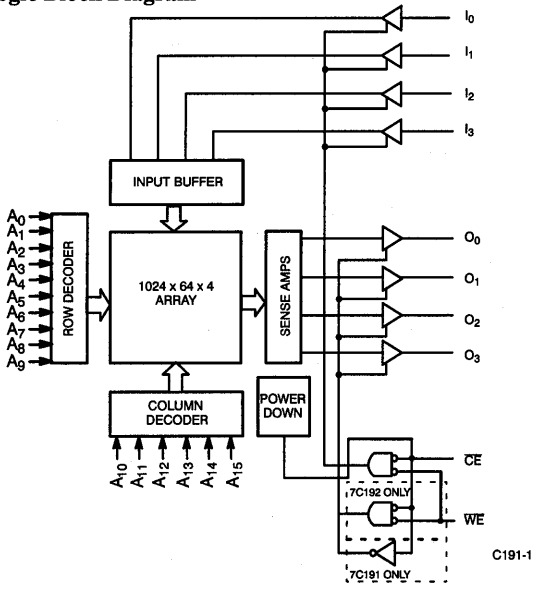
Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

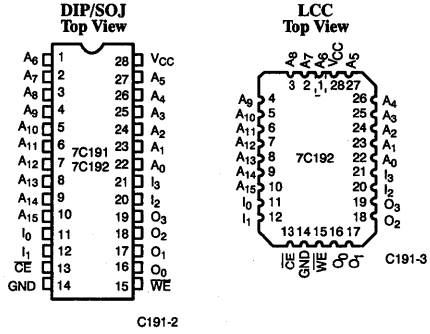
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (CY7C192 only), or chip enable ($\overline{CE}$) is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C191–12 7C192–12	7C191–15 7C192–15	7C191–20 7C192–20	7C191–25 7C192–25	7C191–35 7C192–35	7C191–45 7C192–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	115	
	Military		160	150	125	125	125
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C191–12 7C192–12 Min.	7C191–12 7C192–12 Max.	7C191–15 7C192–15 Min.	7C191–15 7C192–15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}	Com'l		160		150	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10	mA
			Mil				15	

Shaded area contains advanced information.

Notes:

1. Minimum voltage is equal to – 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

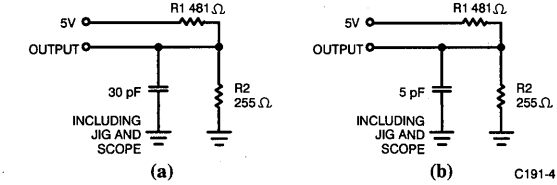
Parameter	Description	Test Conditions		7C191–20 7C192–20 Min.	7C191–20 7C192–20 Max.	7C191–25, 35, 45 7C192–25, 35, 45 Min.	7C191–25, 35, 45 7C192–25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		115	mA
			Mil		150		125	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≤ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15	mA

Shaded area contains advanced information.

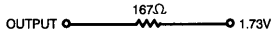
Capacitance[5]

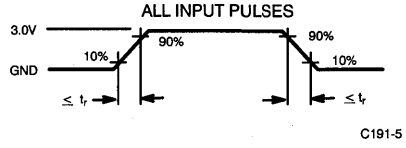
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[6]



Equivalent to: THÉVENIN EQUIVALENT





Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3,7]

Parameter	Description	7C191–12 7C192–12		7C191–15 7C192–15		7C191–20 7C192–20		7C191–25 7C192–25		7C191–35 7C192–35		7C192–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		5		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE[10]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		18		22		22		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		18		22		22		ns
t_{SD}	Data Set-Up to Write End	8		9		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z (7C192)[8]	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z (7C192)[8,9]		7		7		10		11		15		15	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C191)		12		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		12		15		20		20		30		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C191)		12		15		20		25		35		45	ns

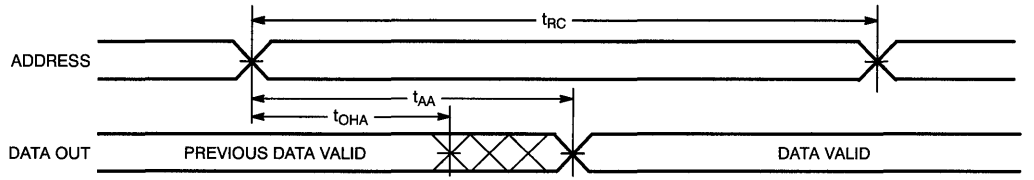
Shaded area contains advanced information.

Notes:

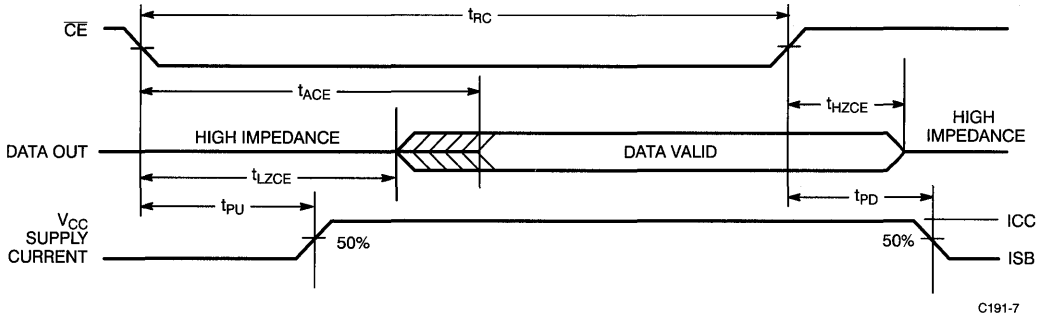
7. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 through −45 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed and not 100% tested.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

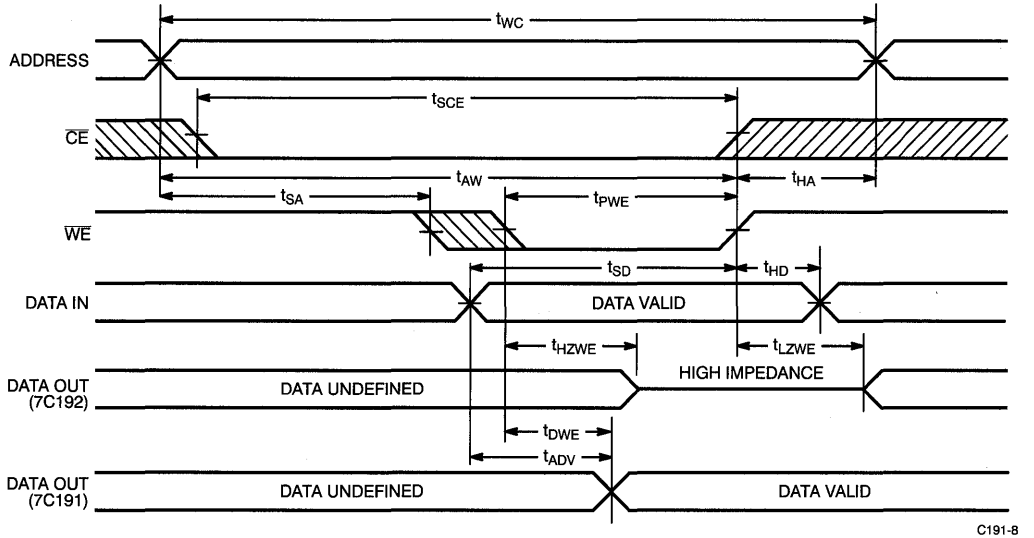
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



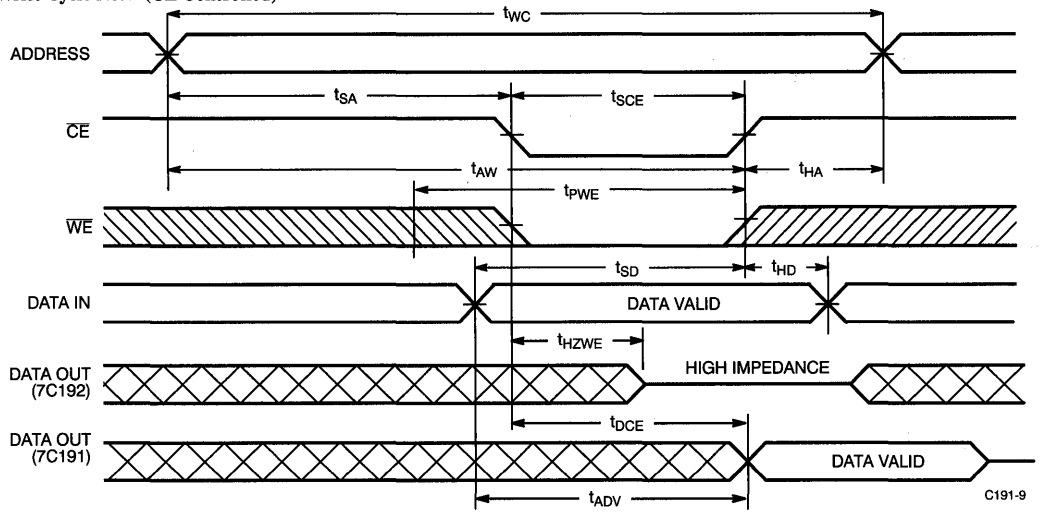
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE} = V_{IL}$.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C192 only).

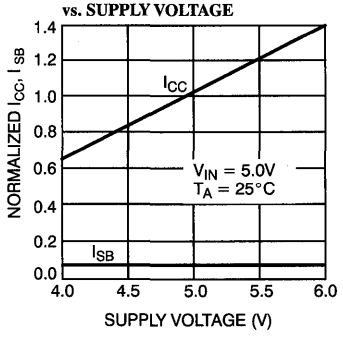
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

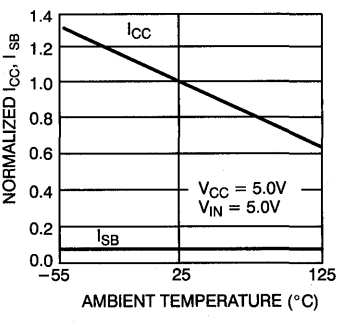


Typical DC and AC Characteristics

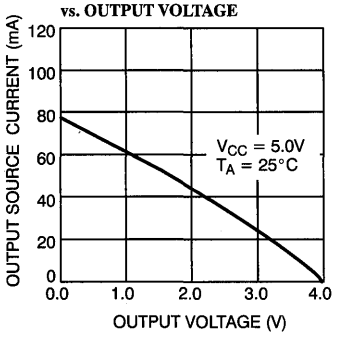
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



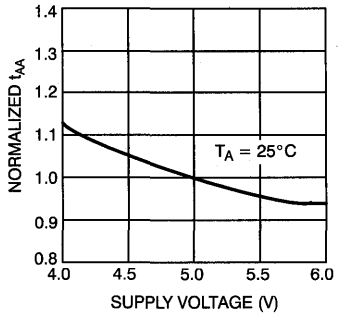
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



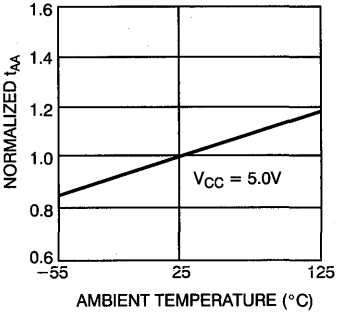
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



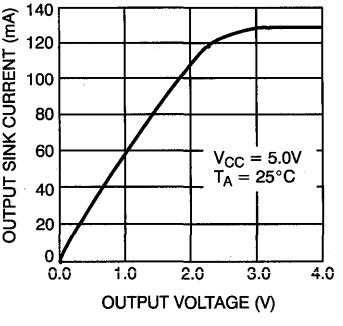
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

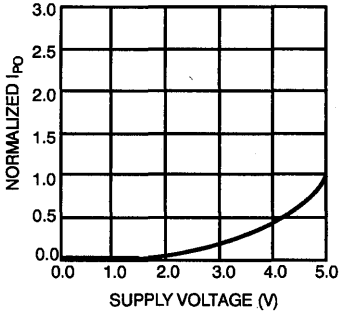


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

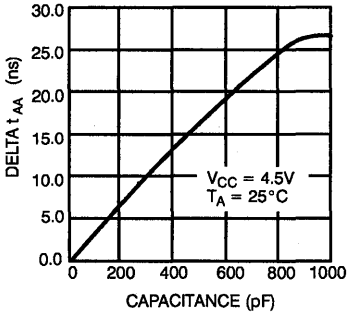


Typical DC and AC Characteristics (continued)

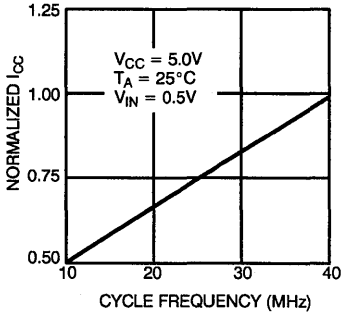
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C191-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191-12VC	V21	28-Lead Molded SOJ	
15	CY7C191-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191-15VC	V21	28-Lead Molded SOJ	
20	CY7C191-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191-20VC	V21	28-Lead Molded SOJ	
25	CY7C191-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191-25VC	V21	28-Lead Molded SOJ	
35	CY7C191-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191-35VC	V21	28-Lead Molded SOJ	

Shaded area contains advanced information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C192–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–12VC	V21	28-Lead Molded SOJ	
15	CY7C192–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–15VC	V21	28-Lead Molded SOJ	
	CY7C192–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C192–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–20VC	V21	28-Lead Molded SOJ	
	CY7C192–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C192–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–25VC	V21	28-Lead Molded SOJ	
	CY7C192–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C192–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–35VC	V21	28-Lead Molded SOJ	
	CY7C192–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C192–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. CY7C191 only

CY7B194
CY7B195
CY7B196

CYPRESS SEMICONDUCTOR

64K x 4 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 850 mW**
- **Low standby power**
  - **— 160 mW**
- **Automatic power-down when deselected**
- **Output enable ($\overline{OE}$) feature (CY7B195 and CY7B196 only)**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B194, CY7B195, and CY7B196 are high-performance BiCMOS static RAMs organized as 65,536 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active LOW chip enable ($\overline{CE}_2$, CY7B196 only), an active LOW output enable ($\overline{OE}$, CY7B195 and CY7B196 only), and three-state drivers. Both devices have an automatic power-down feature that reduces power consumption by more than 75% when deselected.

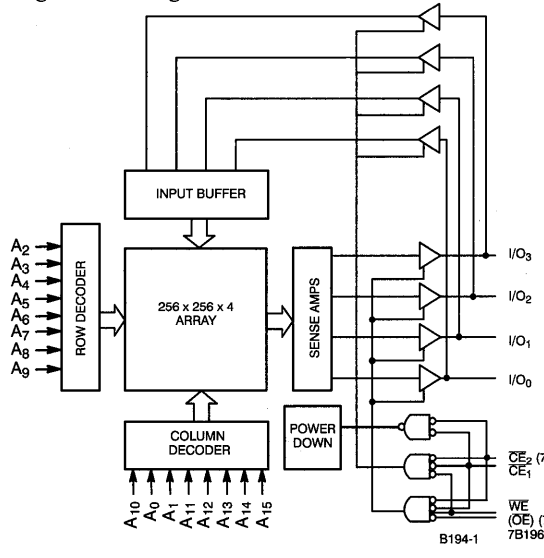
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two ($\overline{CE}_2$, CY7B196 only) input LOW. Data on the I/O pin (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$), chip enable two ($\overline{CE}_2$, CY7B196 only), and output enable ($\overline{OE}$) LOW, while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

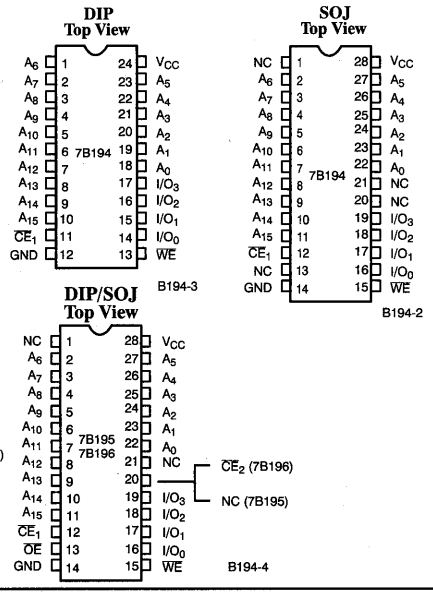
The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH, or $\overline{CE}_2$ HIGH, CY7B196 only), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ CY7B196 only, and $\overline{WE}$ LOW).

The CY7B194, CY7B195, and CY7B196 are available in 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configurations



Selection Guide

		7B194–10 7B195–10 7B196–10	7B194–12 7B195–12 7B196–12	7B194–15 7B195–15 7B196–15	7B194–20 7B195–20 7B196–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	170	160	150	
	Military		170	160	160
Maximum Standby Current (mA)	Commercial	40	35	30	
	Military		40	40	40

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B194−10 7B195−10 7B196−10 Min.	7B194−10 7B195−10 7B196−10 Max.	7B194−12 7B195−12 7B196−12 Min.	7B194−12 7B195−12 7B196−12 Max.	7B194−15, 20 7B195−15, 20 7B196−15, 20 Min.	7B194−15, 20 7B195−15, 20 7B196−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		170		160		150	mA
			Mil				170		160	
I_{SB}	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		40		35		30	mA
			Mil				40		40	

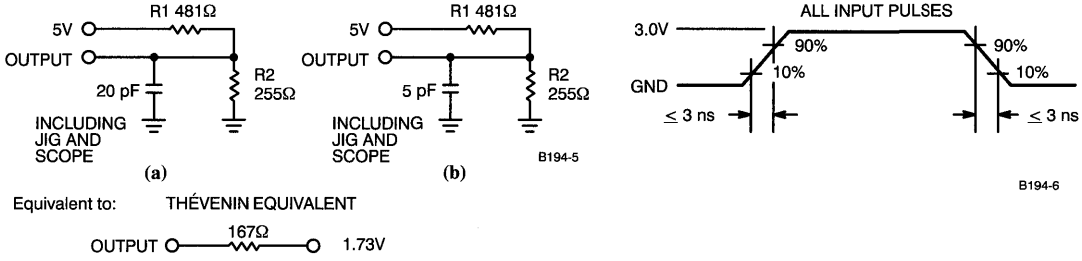
Capacitance[5]

Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}, $C_{I/O}$	Output Capacitance		8	pF

Notes:

1. $V_{IL\,(min.)}$ = − 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For PDIP (P13, P21) AND CDIP (D14, D22), C_{IN} = C_{OUT} = 10 pF.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 7]

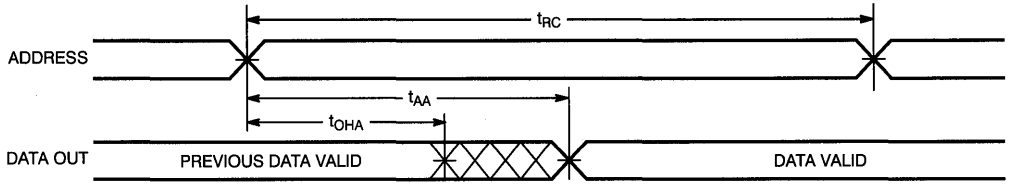
Parameter	Description	7B194–10 7B195–10 7B196–10		7B194–12 7B195–12 7B196–12		7B194–15 7B195–15 7B196–15		7B194–20 7B195–20 7B196–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		6		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	2		2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[10, 11]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		6		7		7		10	ns

Notes:

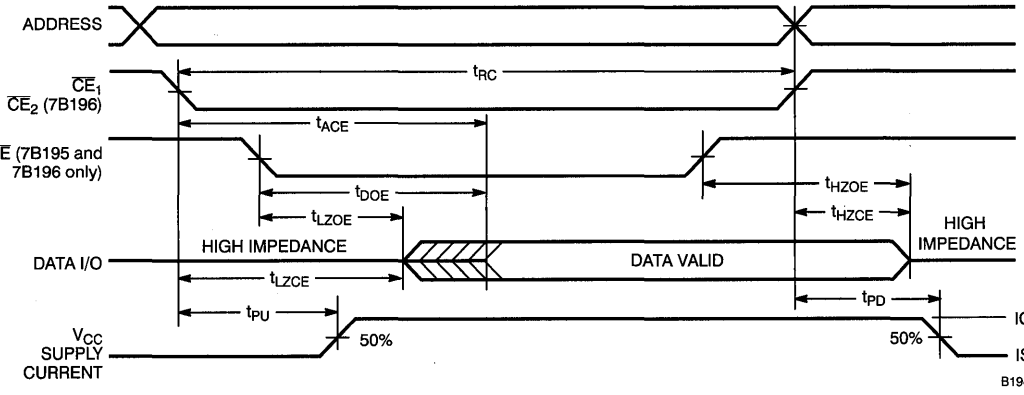
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

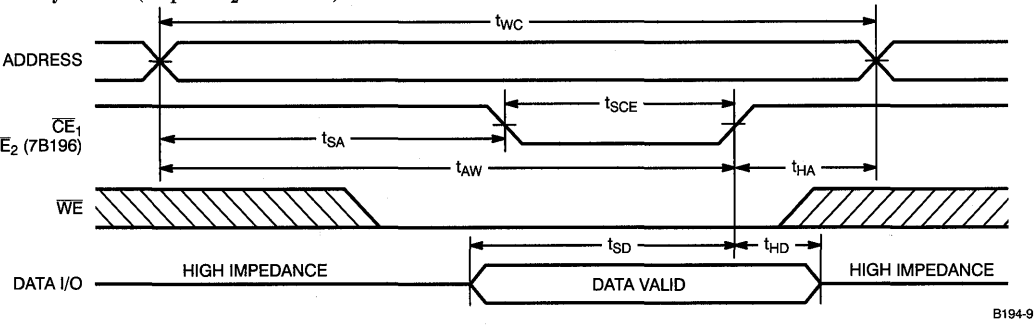
Read Cycle No. 1[12, 13]



Read Cycle No. 2[13, 14]



Write Cycle No. 1 ($\overline{CE_1}$ or $\overline{CE_2}$ Controlled)[15, 16]

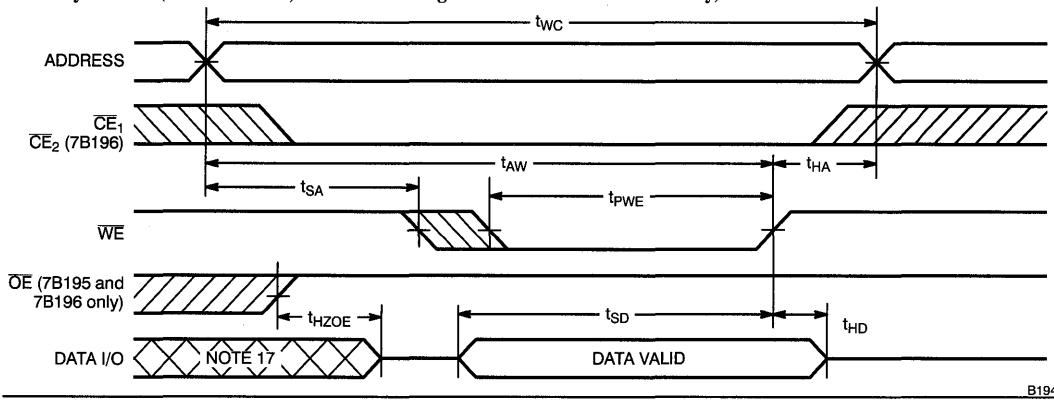


Notes:

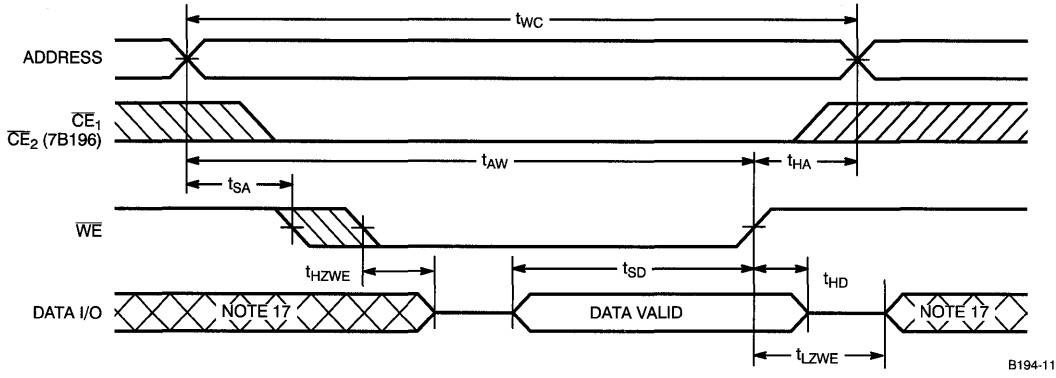
12. Device is continuously selected. $\overline{CE_1}$ ($\overline{OE}$: 7B195 and 7B196, $\overline{CE_2}$: 7B196 only) = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE_1}$ and $\overline{CE_2}$ transition LOW.
15. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE_1}$ ($\overline{CE_1}$ or $\overline{CE_2}$ on the 7B196) goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7B195 and 7B196 only)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Note:
17. During this period, the I/Os are in the output state and input signals should not be applied.

CYPRESS SEMICONDUCTOR

7B194 Truth Table

$\overline{CE_1}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7B195 Truth Table

$\overline{CE_1}$	$\overline{WE}$	$\overline{OE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

7B196 Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B194–10PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7B194–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B194–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B194–12PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B194–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B194–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7B194–15DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B194–15PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B194–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B194–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7B194–20DMB	D14	24-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B196–10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B196–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B196–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B196–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B196–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B196–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B196–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B196–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B196–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B196–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B196–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B195–10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B195–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B195–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B195–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B195–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B195–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B195–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B195–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B195–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B195–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B195–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CY7C194
CY7C195
CY7C196

CYPRESS SEMICONDUCTOR

64K x 4 Static RAM

Features

- **High speed**
  - **12 ns**
- **Output enable ($\overline{OE}$) feature (7C195 and 7C196)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **880 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

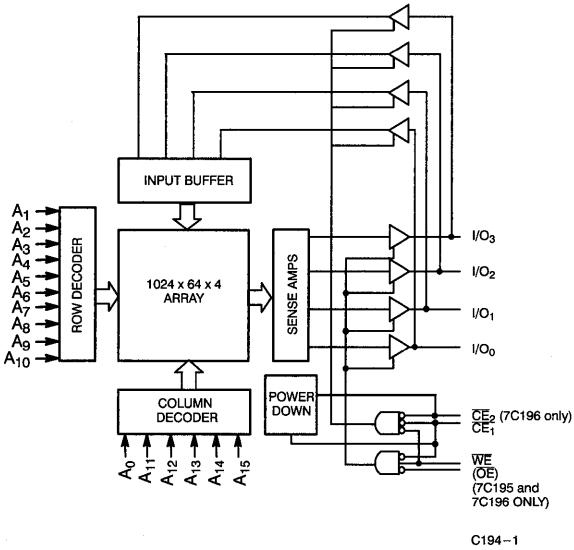
The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

A die coat is used to ensure alpha immunity.

Logic Block Diagram



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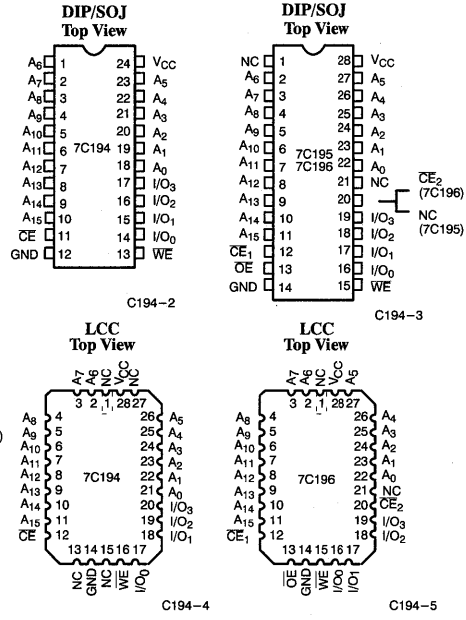
Pin Configurations



Selection Guide

		7C194–12 7C195–12 7C196–12	7C194–15 7C195–15 7C196–15	7C194–20 7C195–20 7C196–20	7C194–25 7C195–25 7C196–25	7C194–35 7C195–35 7C196–35	7C194–45 7C196–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	115	
	Military		160	150	125	125	125
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains preliminary information.

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C194−12 7C195−12 7C196−12 Min.	7C194−12 7C195−12 7C196−12 Max.	7C194−15 7C195−15 7C196−15 Min.	7C194−15 7C195−15 7C196−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}[1]	Input LOW Voltage			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		160		145	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10	mA
			Mil				15	

Shaded area contains preliminary information.

Notes:

1. Minimum voltage is equal to −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range[3] (continued)

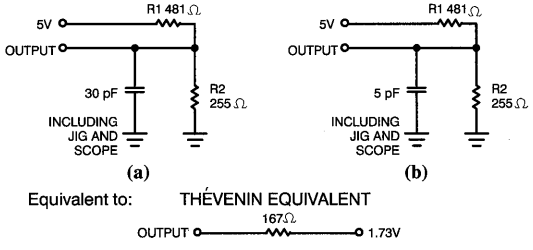
Parameter	Description	Test Conditions		7C194–20 7C195–20 7C196–20 Min.	7C194–20 7C195–20 7C196–20 Max.	7C194–25, 35,45 7C195–25, 35 7C196–25, 35,45 Min.	7C194–25, 35,45 7C195–25, 35 7C196–25, 35,45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		115	mA
			Mil		150		125	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15	mA

Shaded area contains preliminary information.

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7]



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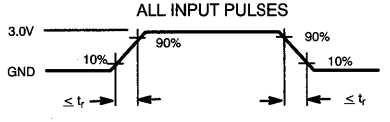


C194–7

Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

CYPRESS SEMICONDUCTOR

Switching Characteristics Over the Operating Range[3,8]

Parameter	Description		7C194–12 7C195–12 7C196–12		7C194–15 7C195–15 7C196–15		7C194–20 7C195–20 7C196–20		7C194–25 7C195–25 7C196–25		7C194–35 7C195–35 7C196–35		7C194–45 7C196–45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
t_{RC}	Read Cycle Time		12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid			12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		3		3		ns
t_{ACE1}, t_{ACE2}	$\overline{CE}$ LOW to Data Valid			12		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C195, 7C196		5		7		9		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7C195, 7C196	0		0		0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10]	7C195, 7C196		5		7		9		11		15		15	ns
t_{LZCE1}, t_{LZCE2}	$\overline{CE}$ LOW to Low Z[9]		3		3		3		3		3		3		ns
t_{HZCE1}, t_{HZCE2}	$\overline{CE}$ HIGH to High Z[9,10]			5		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			12		15		20		25		35		45	ns
WRITE CYCLE[11]															
t_{WC}	Write Cycle Time		12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		9		10		15		18		22		22		ns
t_{AW}	Address Set-Up to Write End		9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		8		9		15		18		22		22		ns
t_{SD}	Data Set-Up to Write End		8		9		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]		3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 8]			7		7		10	0	13	0	15	0	20	ns

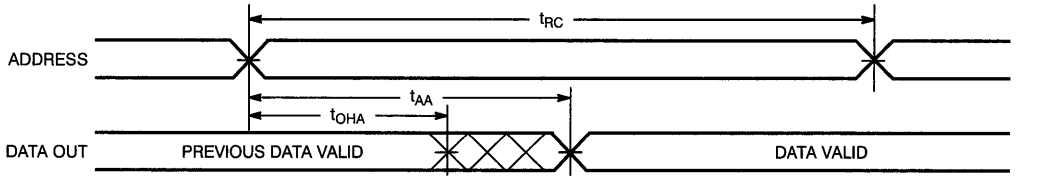
Shaded area contains preliminary information.

Notes:

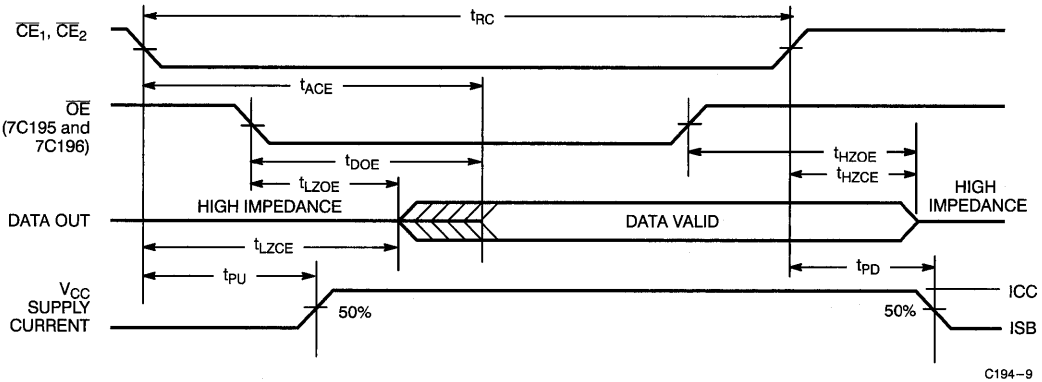
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

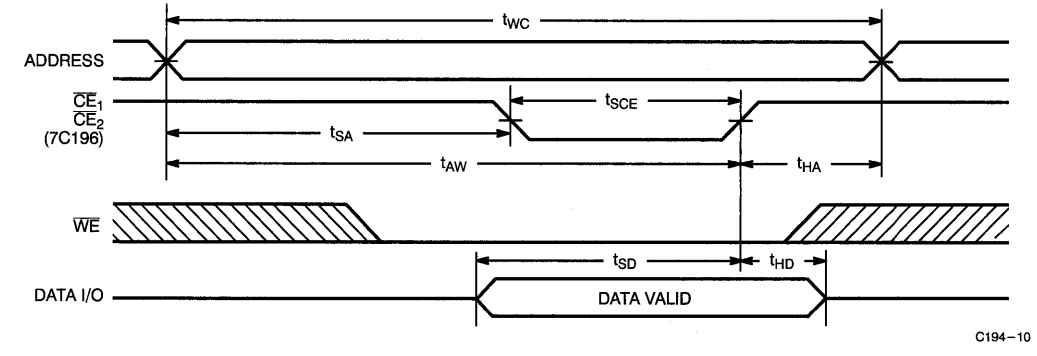
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



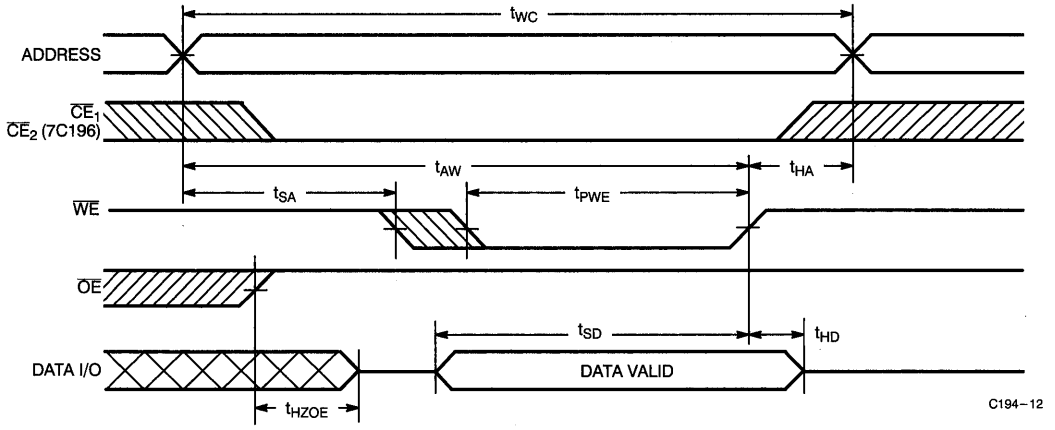
Write Cycle No. 1 ($\overline{CE}$ Controlled)[11, 15, 16]



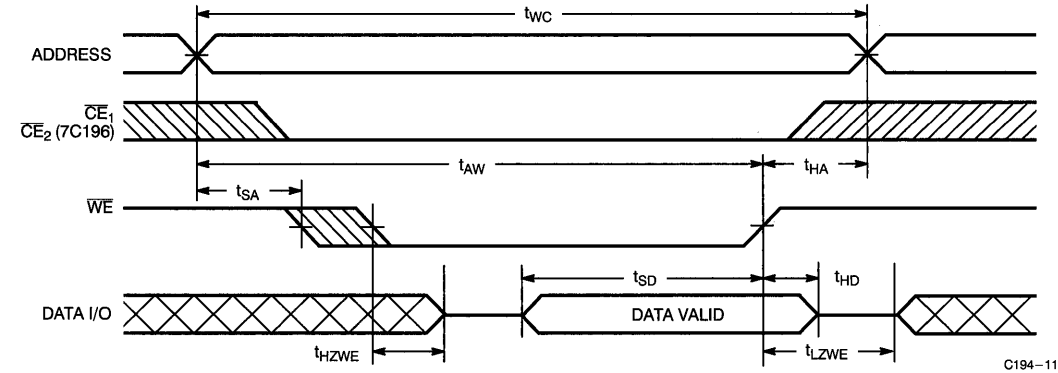
Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected: $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IL}$ (7C196), and $\overline{OE} = V_{IL}$ (7C195 and 7C196).
14. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.
15. Data I/O will be high impedance if $\overline{OE} = V_{IH}$ (7C195 and 7C196).
16. If any $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

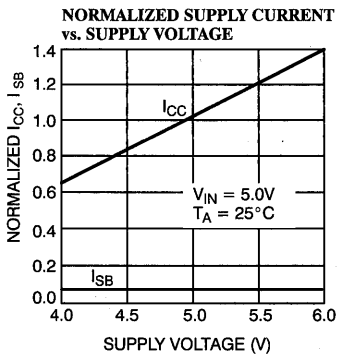
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7C195 and 7C196 only)[11, 15, 16]

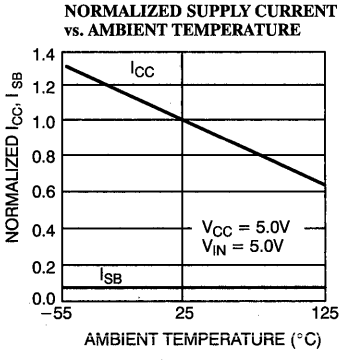


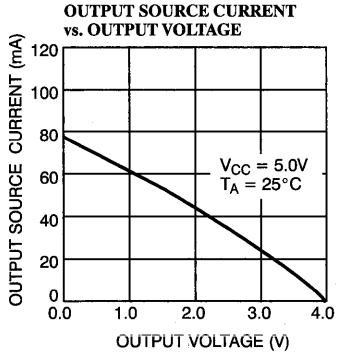
Write Cycle No. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ LOW)[16, 17]



Typical DC and AC Characteristics

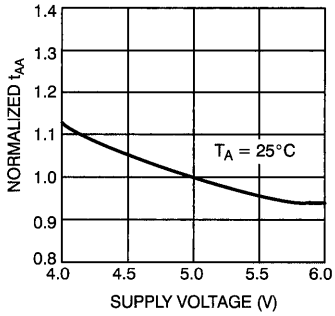




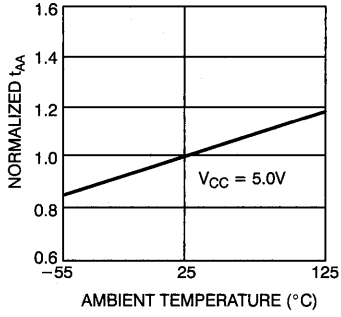


Typical DC and AC Characteristics (continued)

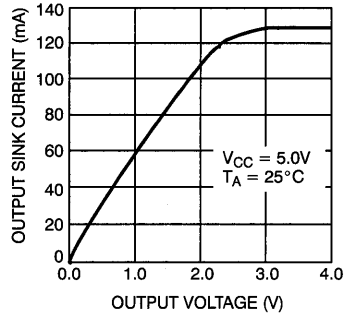
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



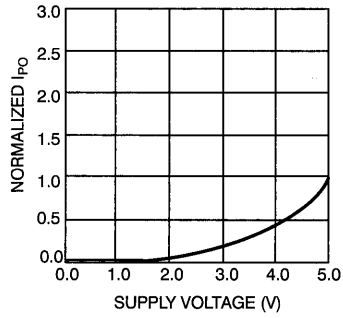
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



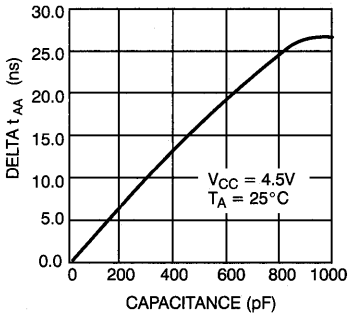
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



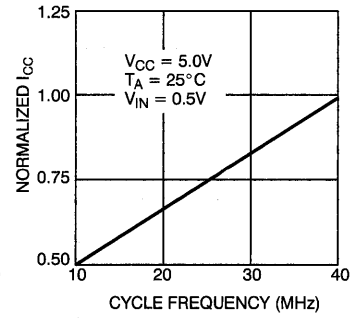
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C194 Truth Table

$\overline{CE}$	$\overline{WE}$	Data I/O	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7C195 Truth Table

$\overline{CE_1}$	$\overline{WE}$	$\overline{OE}$	Data I/O	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect	Active (I_{CC})

7C196 Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	Data I/O	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	H	X	X			
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Deselect	Active (I_{CC})

CYPRESS SEMICONDUCTOR

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194–12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–12VC	V13	24-Lead Molded SOJ	
15	CY7C194–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–15VC	V13	24-Lead Molded SOJ	
	CY7C194–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C194–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–20VC	V13	24-Lead Molded SOJ	
	CY7C194–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C194–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–25VC	V13	24-Lead Molded SOJ	
	CY7C194–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C194–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–35VC	V13	24-Lead Molded SOJ	
	CY7C194–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C194–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–12VC	V21	28-Lead Molded SOJ	
15	CY7C195–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–15VC	V21	28-Lead Molded SOJ	
20	CY7C195–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–20VC	V21	28-Lead Molded SOJ	
25	CY7C195–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–25VC	V21	28-Lead Molded SOJ	
35	CY7C195–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–35VC	V21	28-Lead Molded SOJ	

Shaded areas contain preliminary information.

CYPRESS SEMICONDUCTOR

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C196–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–12VC	V21	28-Lead Molded SOJ	
15	CY7C196–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–15VC	V21	28-Lead Molded SOJ	
	CY7C196–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
20	CY7C196–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–20VC	V21	28-Lead Molded SOJ	
	CY7C196–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C196–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–25VC	V21	28-Lead Molded SOJ	
	CY7C196–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
35	CY7C196–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–35VC	V21	28-Lead Molded SOJ	
	CY7C196–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
45	CY7C196–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}, $_{ACE2}$	7, 8, 9, 10, 11
t_{DOE}[18]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
18. 7C195 and 7C196 only.

Document #: 38–00081–I

CYPRESS SEMICONDUCTOR

CY7C197

256K x 1 Static R/W RAM

Features

- **High speed**
  - **— 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible imputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

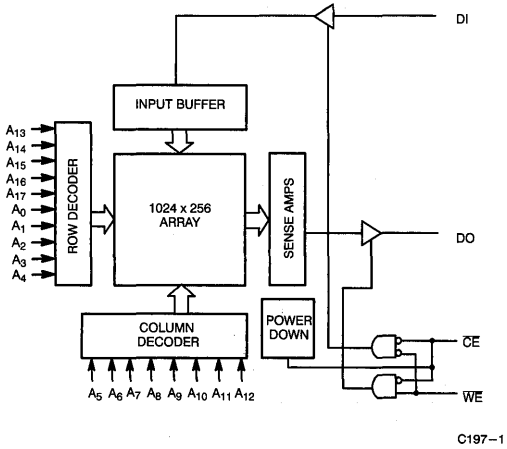
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

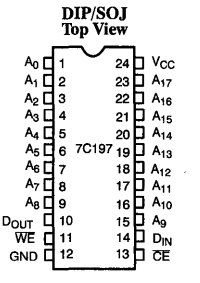
The 7C197 utilizes a die coat to insure alpha immunity.

Logic Block Diagram

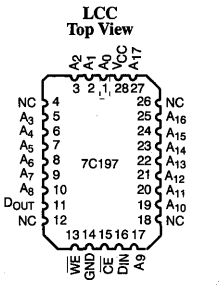


C197–1

Pin Configurations



C197–2



C197–3

Selection Guide

		7C197-12	7C197-15	7C197-20	7C197-25	7C197-35	7C197-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	150	140	135	95	95	
	Military			150	105	105	105
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7C197−12 Min.	7C197−12 Max.	7C197−15 Min.	7C197−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
			I_{OL} = 8.0 mA	Mil				0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 5	+5	− 5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			− 5	+5	− 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		160		150	mA
				Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V		Com'l		10		10	mA
				Mil				15	

Shaded area contains preliminary information.

Notes:

1. $V_{(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range[3] (continued)

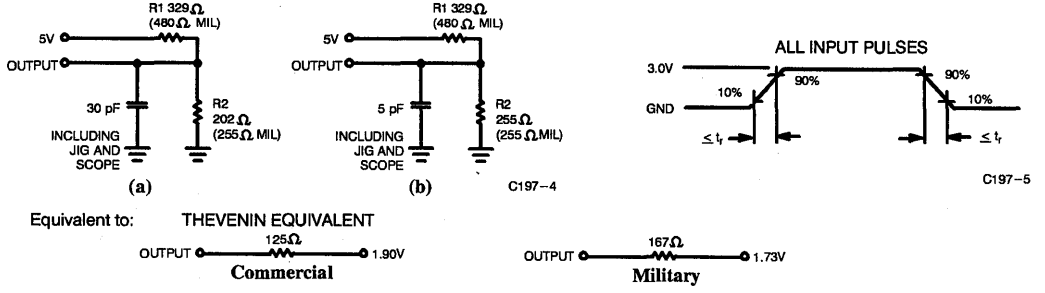
Parameter	Description	Test Conditions			7C197–20 Min.	7C197–20 Max.	7C197–25, 35, 45 Min.	7C197–25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Mil		0.4		0.4	V
			I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		135		95	mA
				Mil		150		105	
I_{SB1}	Automatic $\overline{CE}$ PowerDown Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V				15		15	mA

Shaded area contains preliminary information.

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7]



Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3,8]

Parameter	Description	7C197–12		7C197–15		7C197–20		7C197–25		7C197–35		7C197–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		5		7	0	9	0	11	0	15	0	15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		25		30	ns
WRITE CYCLE[11]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		20		30		40		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	8		9		10		15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	2		2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7	0	10	0	11	0	15	0	15	ns

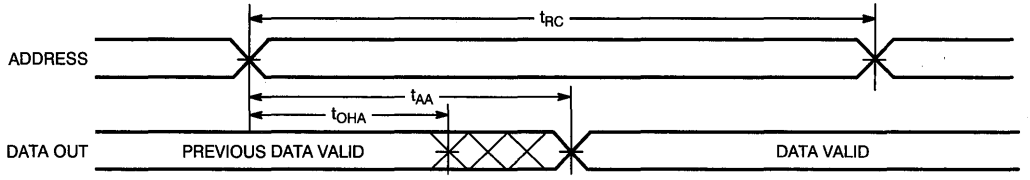
Shaded area contains preliminary information.

Notes:

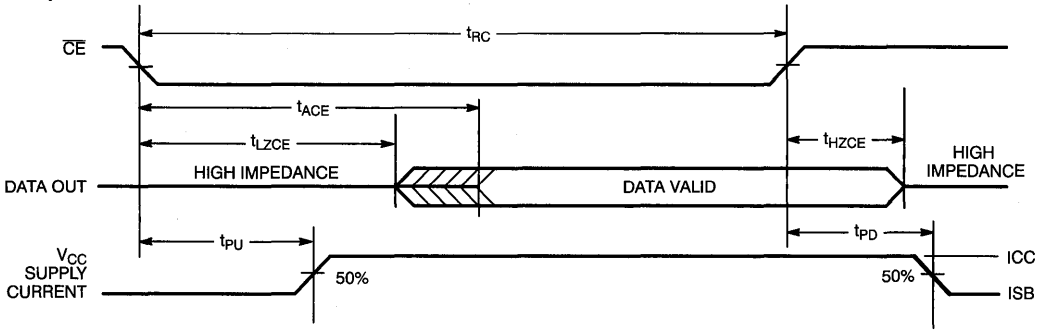
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

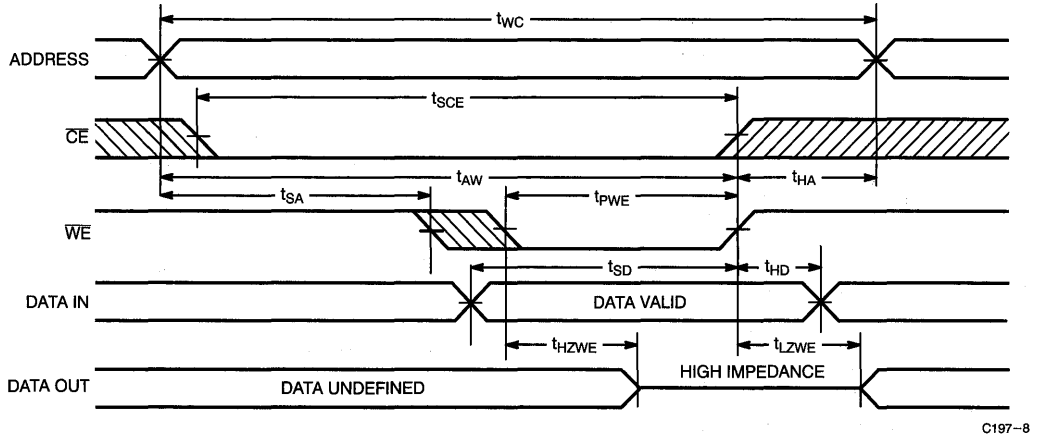
Read Cycle No. 1[12, 13]



Read Cycle No. 2[13]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[12]

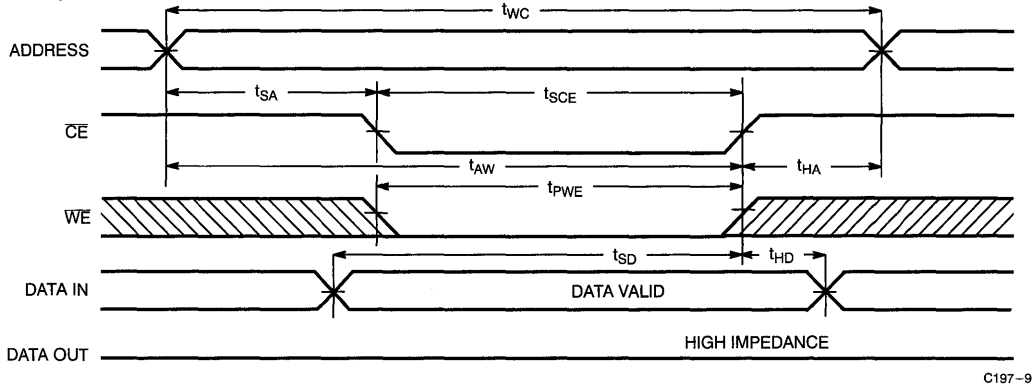


Notes:

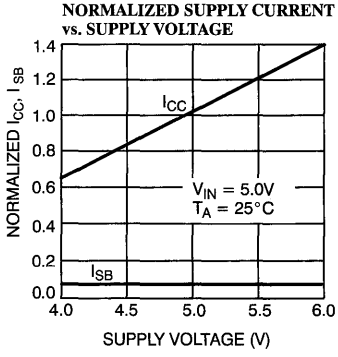
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

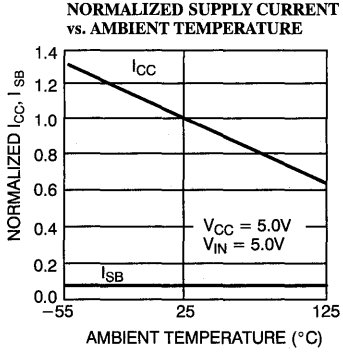
Switching Waveforms (continued)

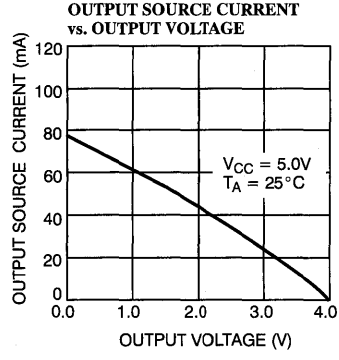
Write Cycle No. 2 ($\overline{CE}$ Controlled) [12, 14]

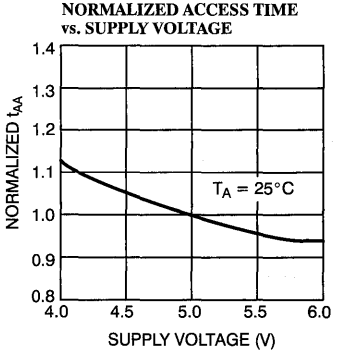


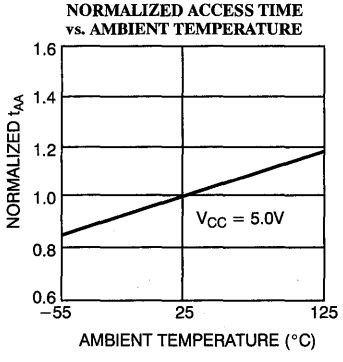
Typical DC and AC Characteristics

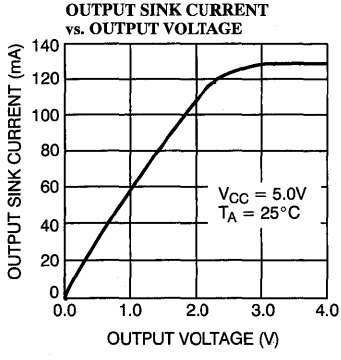






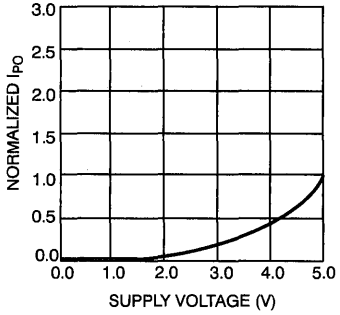




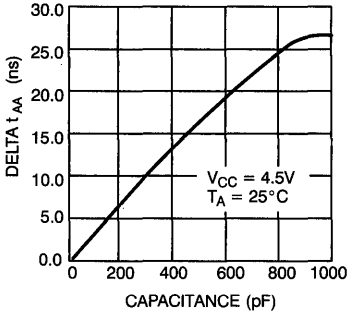


Typical DC and AC Characteristics (continued)

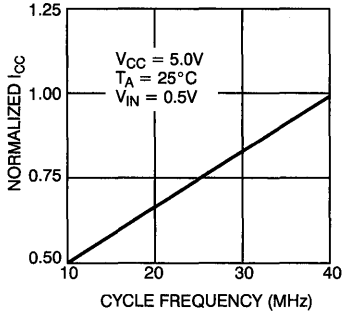
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C197 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C197–12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–12VC	V13	24-Lead Molded SOJ	
15	CY7C197–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–15VC	V13	24-Lead Molded SOJ	
	CY7C197–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7C197–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–20VC	V13	24-Lead Molded SOJ	
	CY7C197–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C197–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–25VC	V13	24-Lead Molded SOJ	
	CY7C197–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–25LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C197–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–35VC	V13	24-Lead Molded SOJ	
	CY7C197–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–35LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C197–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–45LMB	L54	24-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00078-K

CYPRESS SEMICONDUCTOR

CY7B199

32K x 8 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 925 mW**
- **Low standby power**
  - **— 60 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B199 is a high-performance BiCMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 75% when deselected.

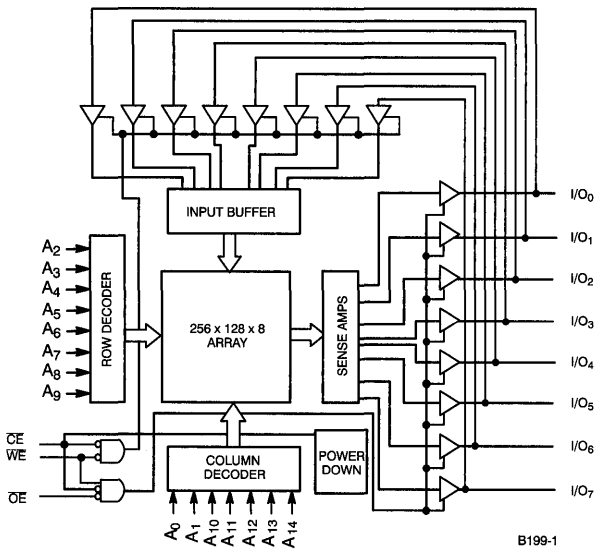
An active LOW write enable signal ($\overline{WE}$) controls the writing operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location specified on the address pins is present on the eight data input/output pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{WE}$ LOW).

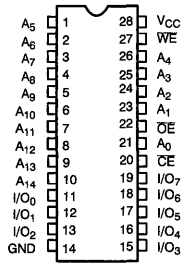
The CY7B199 is available in space-saving 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration

DIP/SOJ
Top View



Selection Guide

		7B199–10	7B199–12	7B199–15	7B199–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	185	170	170	
	Military		170	170	170
Maximum Standby Current (mA)	Commercial	40	35	30	
	Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B199−10 Min.	7B199−10 Max.	7B199−12 Min.	7B199−12 Max.	7B199−15, 20 Min.	7B199−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		170	mA
			Mil				170		170	
I_{SB}	Automatic CE Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		40		35		30	mA
			Mil				40		40	

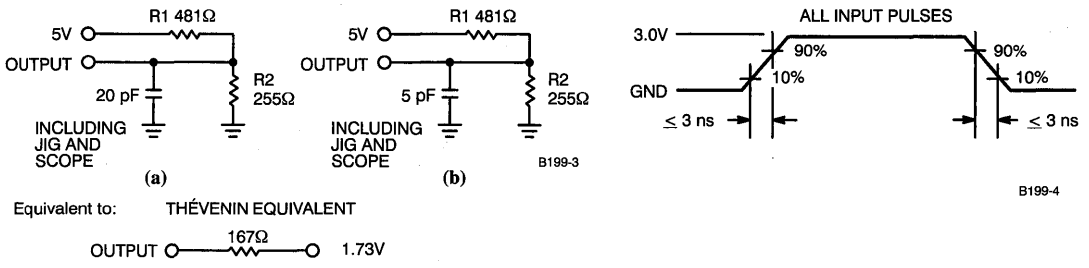
Capacitance[5]

Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}, $C_{I/O}$	Output Capacitance		8	pF

Notes:

1. $V_{IL\,(min.)}$ = − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For PDIP (P21) and CDIP (D22), C_{IN}=C_{OUT}=10 pF.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 7]

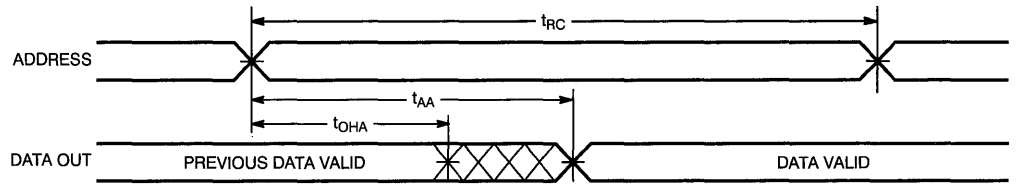
Parameter	Description	7B199–10		7B199–12		7B199–15		7B199–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		6		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	2		2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[10, 11]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		6		7		7		10	ns

Notes:

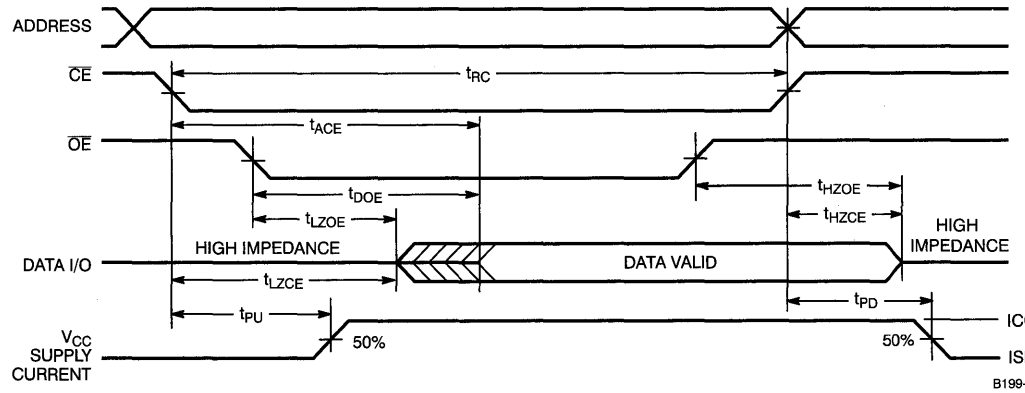
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

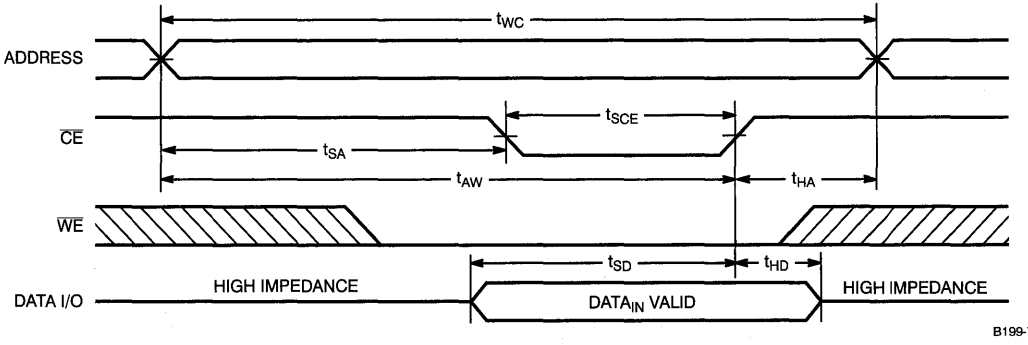
Read Cycle No. 1[12, 13]



Read Cycle No. 2[13, 14]



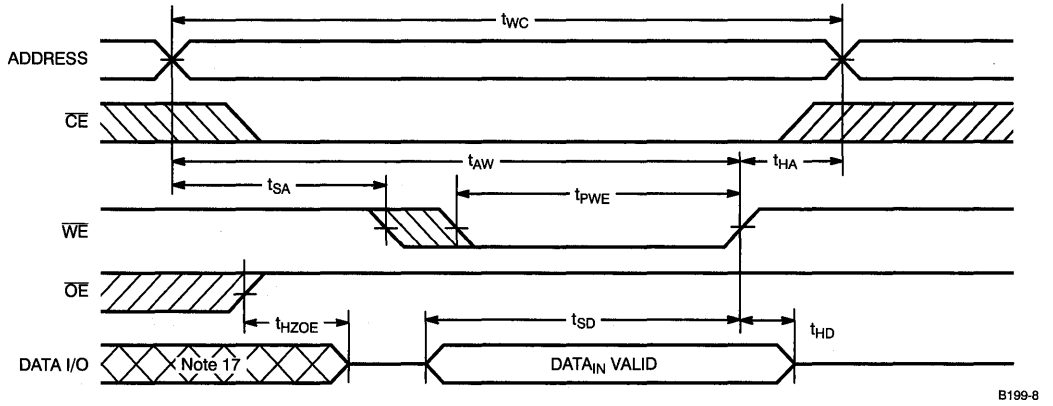
Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



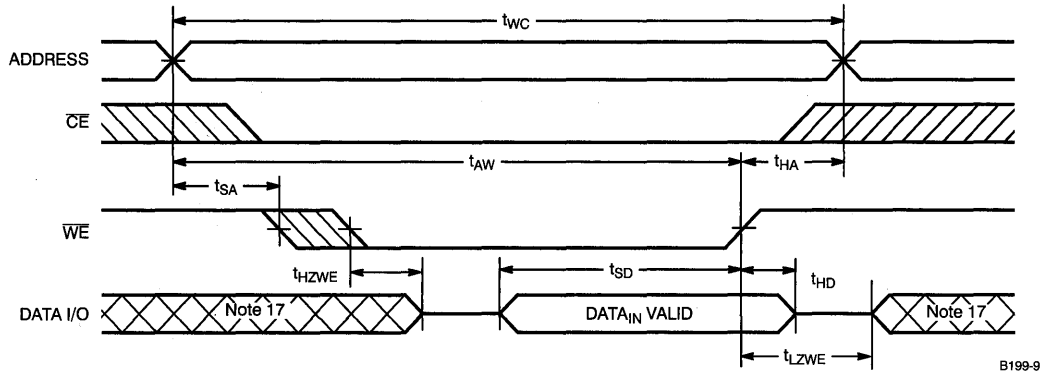
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Notes:
17. During this period, the I/Os are in the output state and input signals should not be applied.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B199–10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B199–10VC	V21	28-Lead Molded SOJ	
12	CY7B199–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B199–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B199–12VC	V21	28-Lead Molded SOJ	
	CY7B199–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B199–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B199–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B199–15VC	V21	28-Lead Molded SOJ	
	CY7B199–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B199–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00160–D

CYPRESS SEMICONDUCTOR

CY7C199

32K x 8 Static RAM

Features

- **High speed**
  - **— 12 ns**
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 165 mW**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

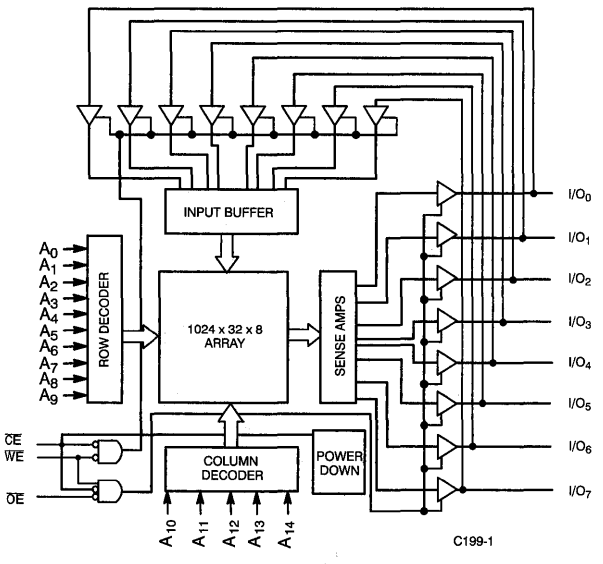
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ and LCC packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

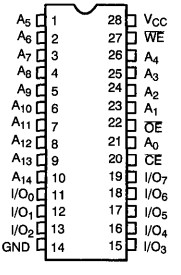
Logic Block Diagram



C199-1

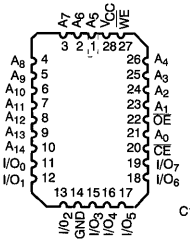
Pin Configurations

DIP/SOJ
Top View



C199-2

LCC
Top View



C199-3

Selection Guide

		7C199–12	7C199–15	7C199–20	7C199–25	7C199–35	7C199–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	160	155	150	150	140	
	Military		180	170	150	150	150
Maximum Standby Current (mA)		30	30	30	30	25	25

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C199−12 Min.	7C199−12 Max.	7C199−15 Min.	7C199−15 Max.	7C199−20 Min.	7C199−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		160		155		150	mA
			Mil				180		170	
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30		30	mA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10		15	mA
			Mil				15		15	

Shaded area contains preliminary information.

Notes:

1. $V_{IL(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

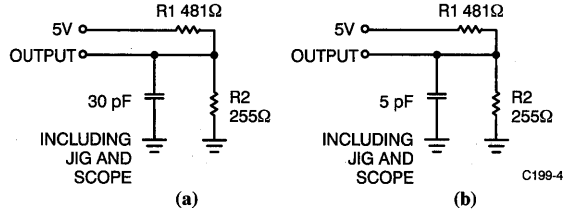
Parameter	Description	Test Conditions		7C199–25 Min.	7C199–25 Max.	7C199–35, 45 Min.	7C199–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		140	mA
			Mil		150		150	
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		25	mA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0			15		15	mA

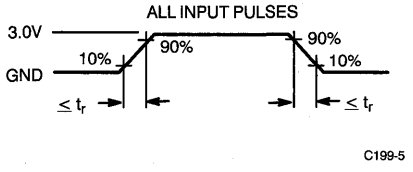
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

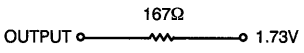
Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT



Note:
6. t_r ≤ 3 ns for the −12 and −15 speeds. t_r ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7C199–12		7C199–15		7C199–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		5		7		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		5		7		9	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		ns
t_{AW}	Address Set-Up to Write End	9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		ns
t_{SD}	Data Set-Up to Write End	8		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9]		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns

Shaded area contains preliminary information.

Notes:

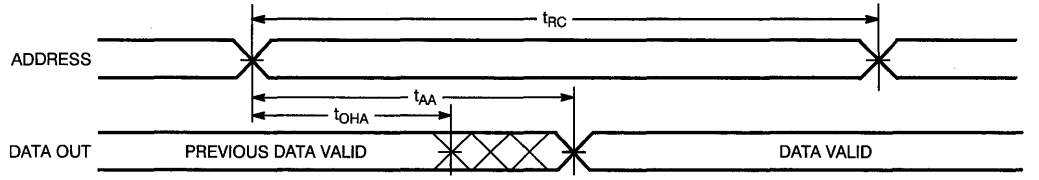
7. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[3, 7] (continued)

Parameter	Description	7C199–25		7C199–35		7C199–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		11		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9]		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns

Switching Waveforms

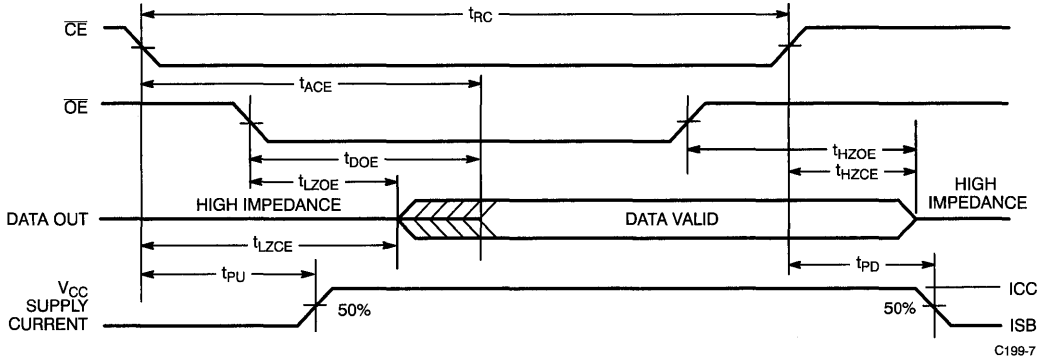
Read Cycle No. 1[12, 13]



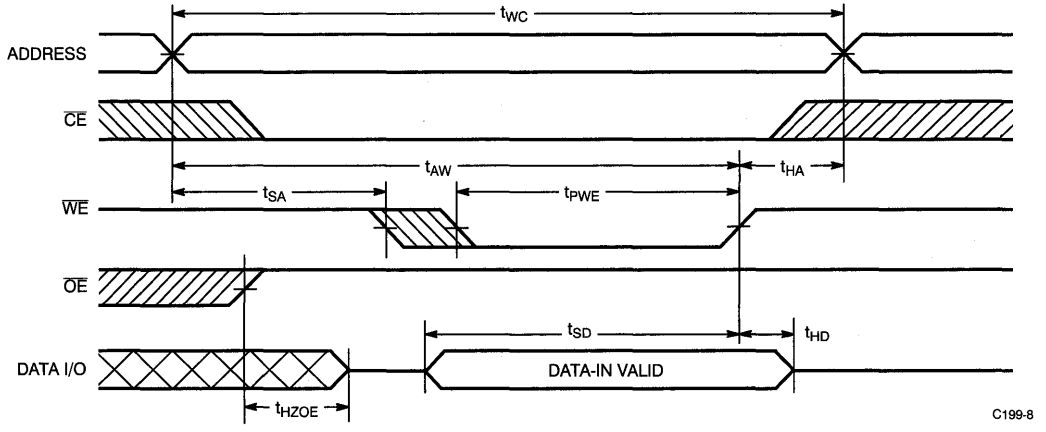
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

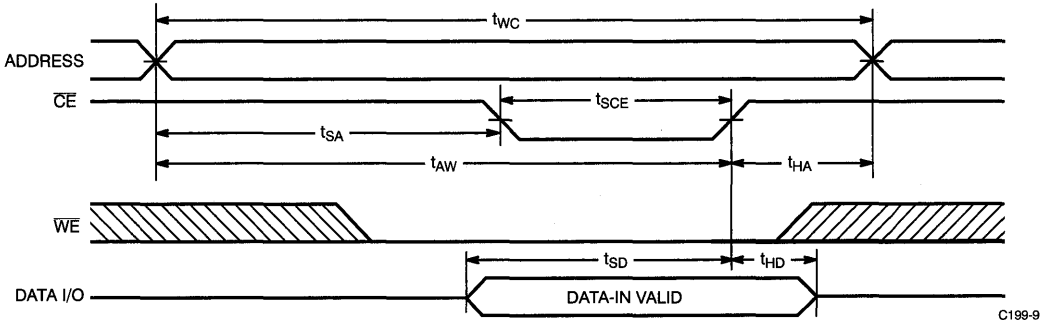
Read Cycle No. 2[13, 14]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 15, 16]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 15, 16]

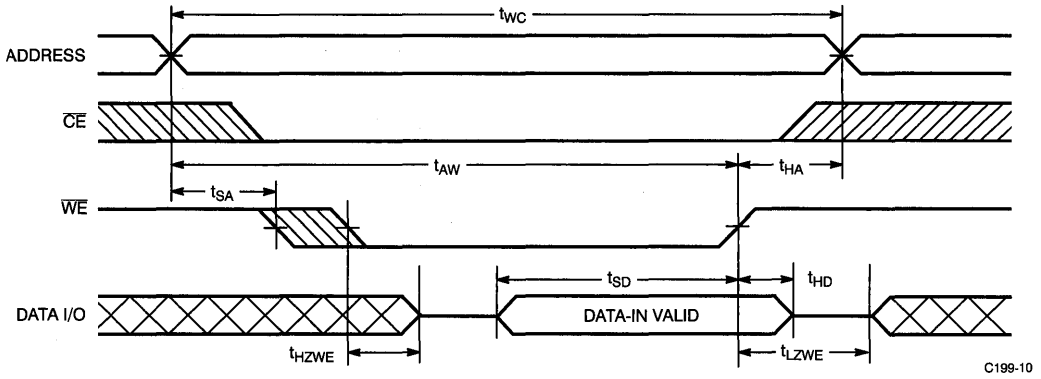


Notes:

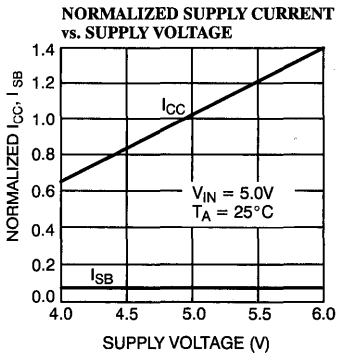
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

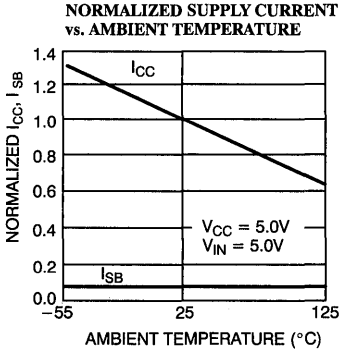
Switching Waveforms (continued)

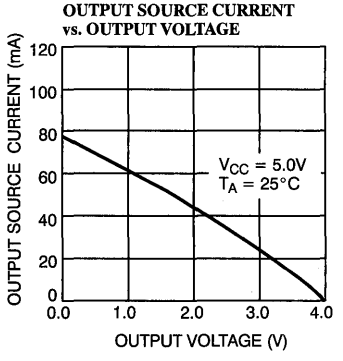
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]

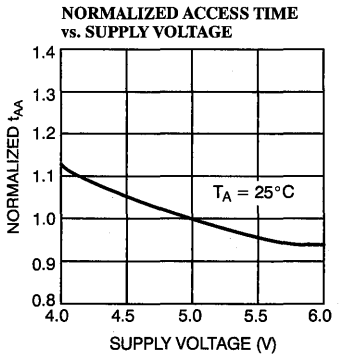


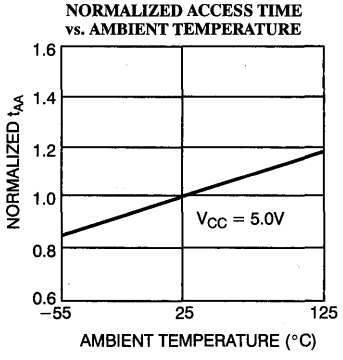
Typical DC and AC Characteristics

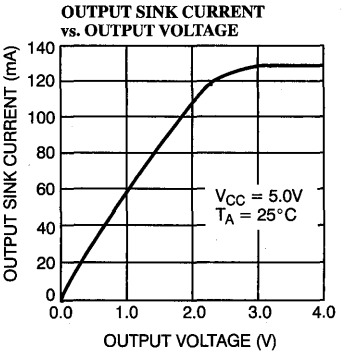






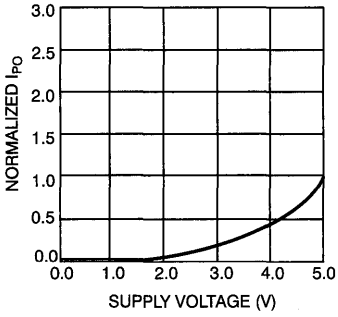




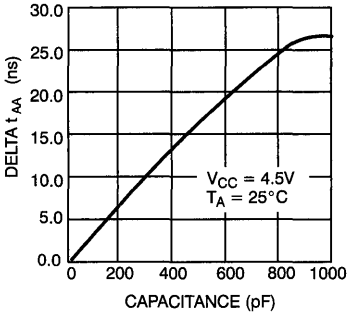


Typical DC and AC Characteristics (continued)

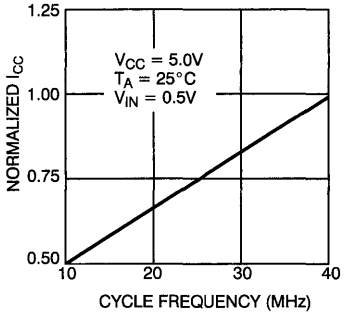
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C199–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199–12VC	V21	28-Lead Molded SOJ	
15	CY7C199–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199–15VC	V21	28-Lead Molded SOJ	
	CY7C199–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199–20VC	V21	28-Lead Molded SOJ	
	CY7C199–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199–25VC	V21	28-Lead Molded SOJ	
	CY7C199–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199–35VC	V21	28-Lead Molded SOJ	
	CY7C199–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00239–A

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C1001
CY7C1002

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Transparent write (7C1001)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1001 and CY7C1002 are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

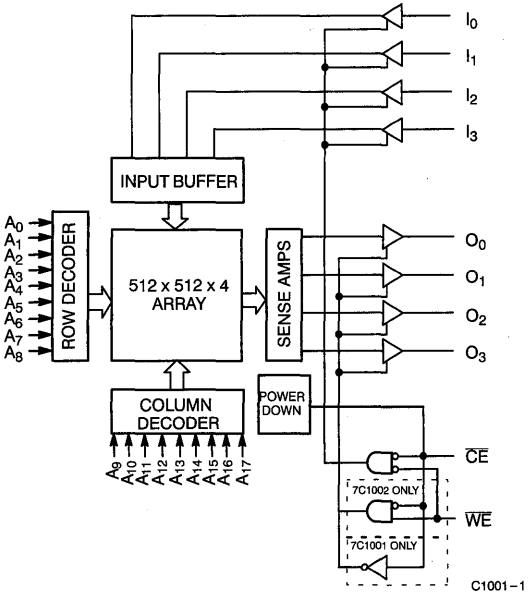
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

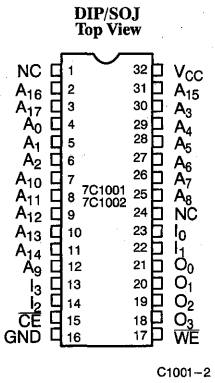
The data output pins on the CY7C1001 and the CY7C1002 are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C1002's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C1001, the output pins will carry the same data as the inputs after a specified delay.

The CY7C1001 and CY7C1002 are available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1001–12 7C1002–12	7C1001–15 7C1002–15	7C1001–20 7C1002–20	7C1001–25 7C1002–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1001−12 7C1002−12 Min.	7C1001−12 7C1002−12 Max.	7C1001−15 7C1002−15 Min.	7C1001−15 7C1002−15 Max.	7C1001−20 7C1002−20 Min.	7C1001−20 7C1002−20 Max.	7C1001−25 7C1002−25 Min.	7C1001−25 7C1002−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 1	+1	− 1	+1	− 1	+1	− 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 5	+5	− 5	+5	− 5	+5	− 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140		130	mA
			Mil				165		150		140	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

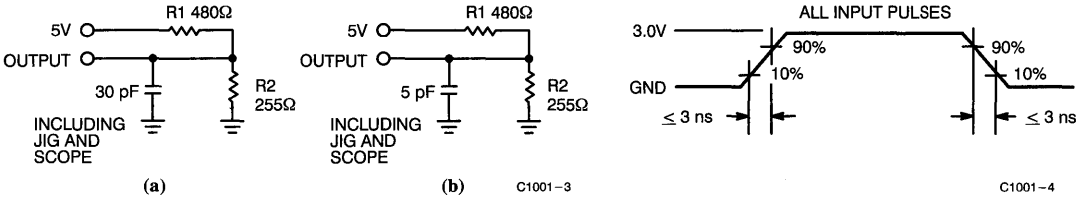
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

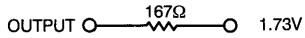
Notes:

1. $V_{IL\,(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C1001–12 7C1002–12 Min.	7C1001–12 7C1002–12 Max.	7C1001–15 7C1002–15 Min.	7C1001–15 7C1002–15 Max.	7C1001–20 7C1002–20 Min.	7C1001–20 7C1002–20 Max.	7C1001–25 7C1002–25 Min.	7C1001–25 7C1002–25 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t_{ADV}	Data Valid to Output Valid (7C1001)		12		15		20		25	ns

Notes:

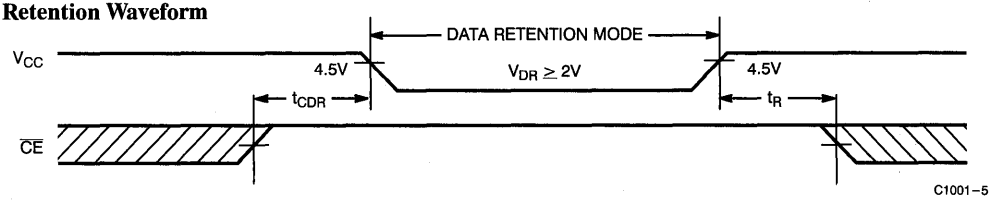
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range

Parameters	Description	Conditions[10]	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

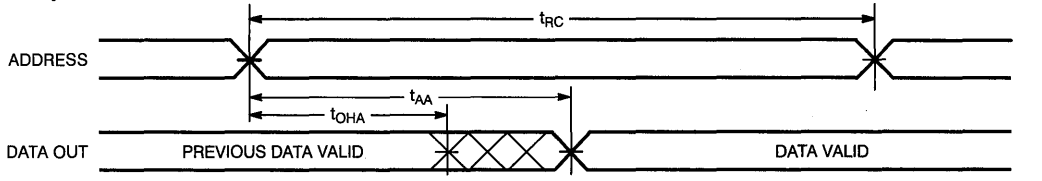
Note:
10. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

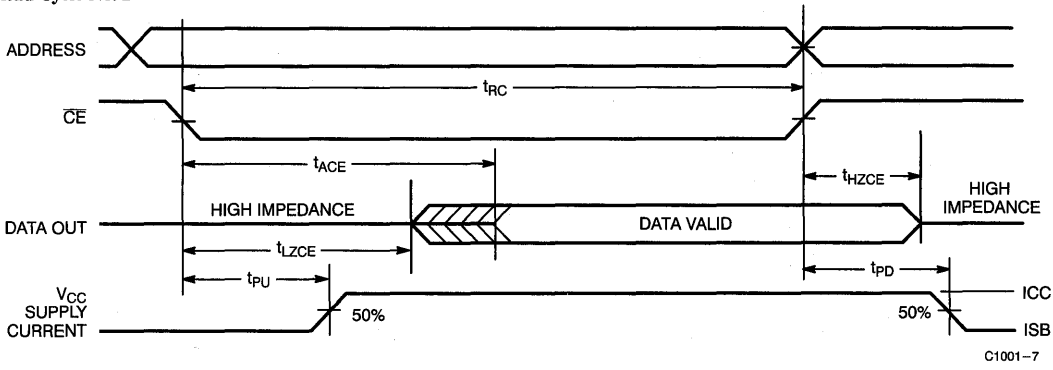


Switching Waveforms

Read Cycle No. 1[11, 12]

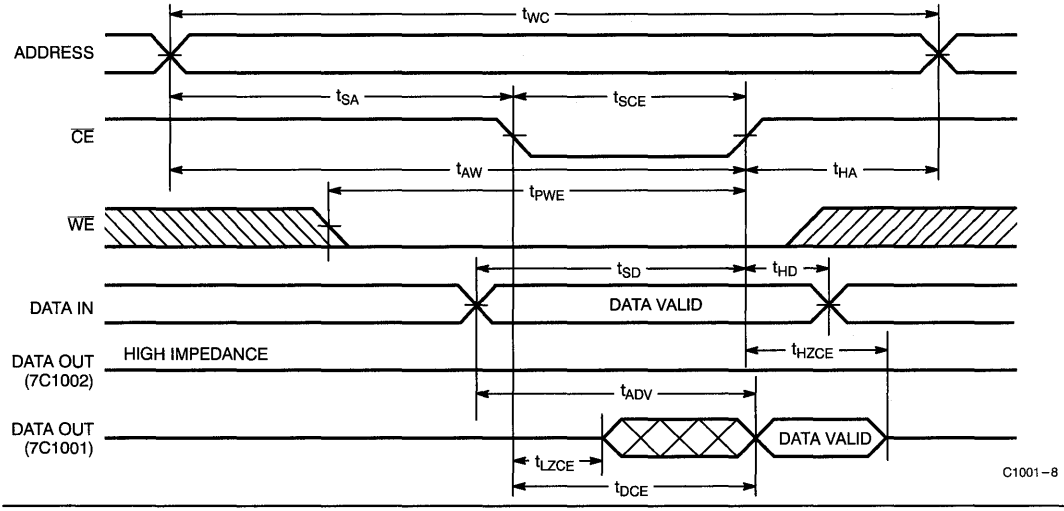


Read Cycle No. 2[12, 13]

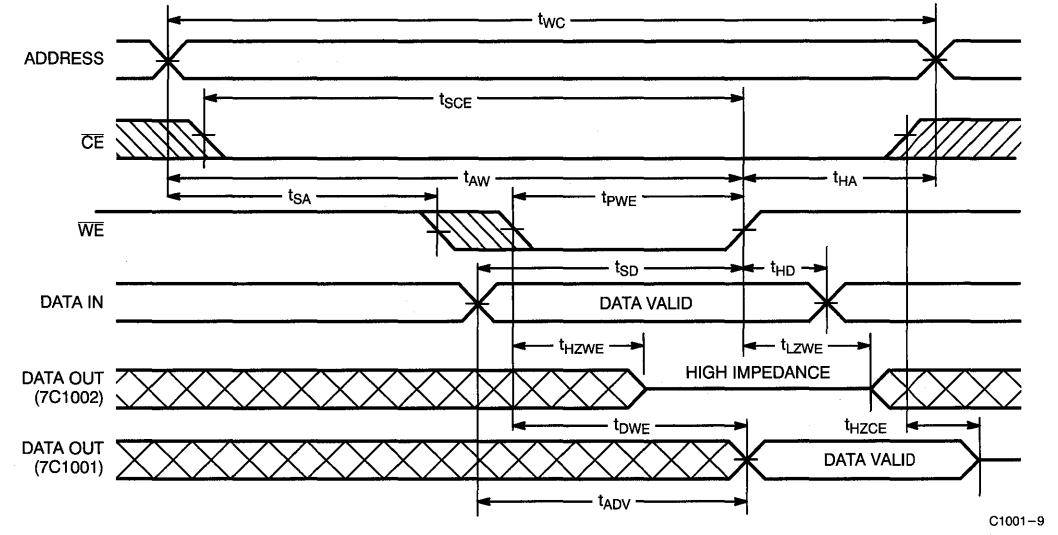


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Notes:
11. Device is continuously selected, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C1002 only).

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C1002: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C1001: Transparent Write[15]	Active (I_{CC})

Note:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1001–12PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1001–12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1001–15PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1001–15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001–15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1001–20PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1001–20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1001–25DC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1001–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001–25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1002–12PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1002–12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1002–15PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1002–15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002–15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1002–20PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1002–20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1002–25PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1002–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002–25DMB	D32	32-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}[16]	7, 8, 9, 10, 11

Note:
16. 7C1001 only.

Document #: 38–00200–A

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C1006**

256K x 4 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1006 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

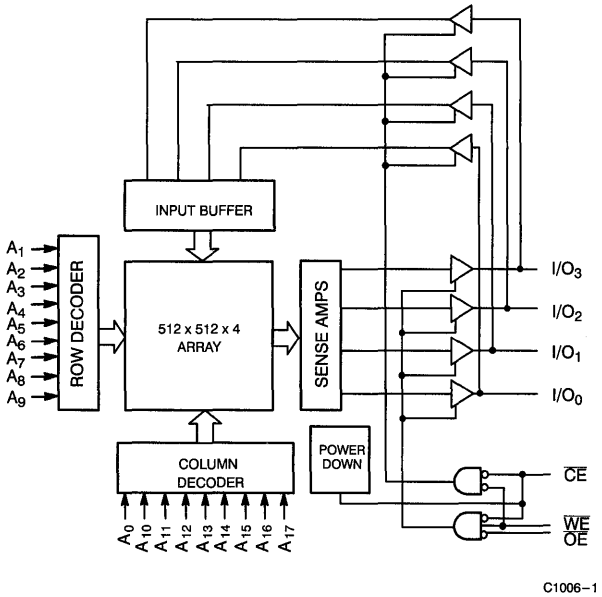
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1006 is available in standard 300-mil-wide DIPs and SOJs.

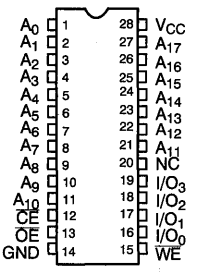
Logic Block Diagram



C1006–1

Pin Configuration

DIP/SOJ
Top View



C1006–2

Selection Guide

		7C1006–12	7C1006–15	7C1006–20	7C1006–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1006–12 Min.	7C1006–12 Max.	7C1006–15 Min.	7C1006–15 Max.	7C1006–20 Min.	7C1006–20 Max.	7C1006–25 Min.	7C1006–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 1	+1	– 1	+1	– 1	+1	– 1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	– 5	+5	– 5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300		– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140		130	mA
			Mil				165		150		140	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

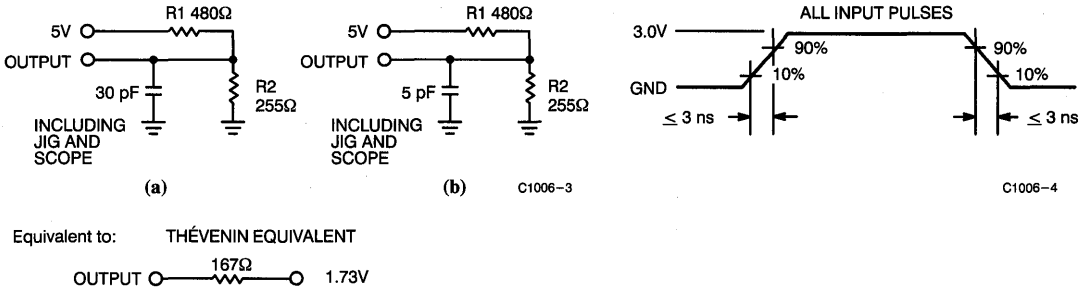
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. $V_{IL\,(min.)}$ = – 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C1006-12		7C1006-15		7C1006-20		7C1006-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9, 10]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

Notes:

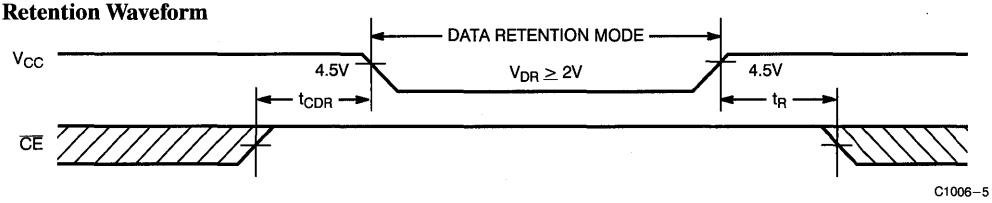
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

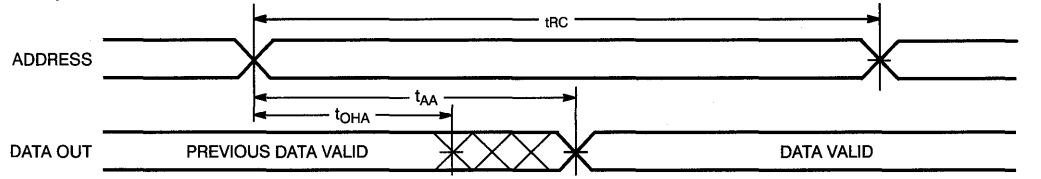
Notes:
11. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

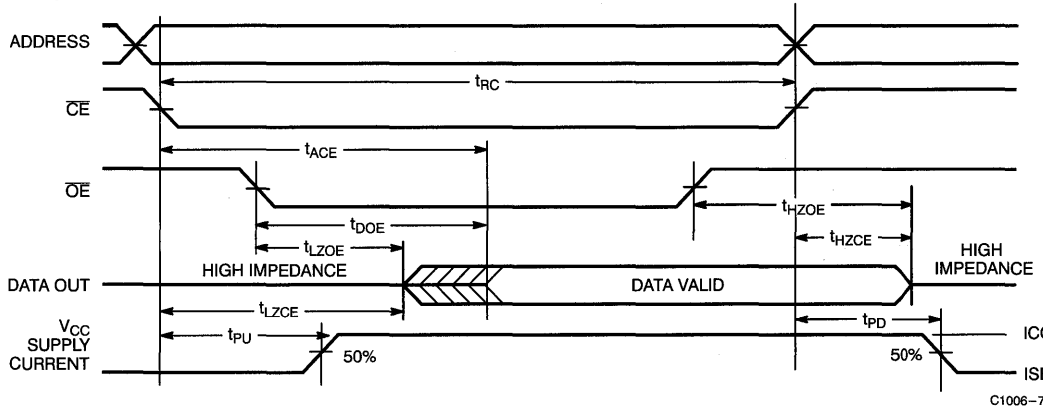


Switching Waveforms

Read Cycle No. 1[12, 13]

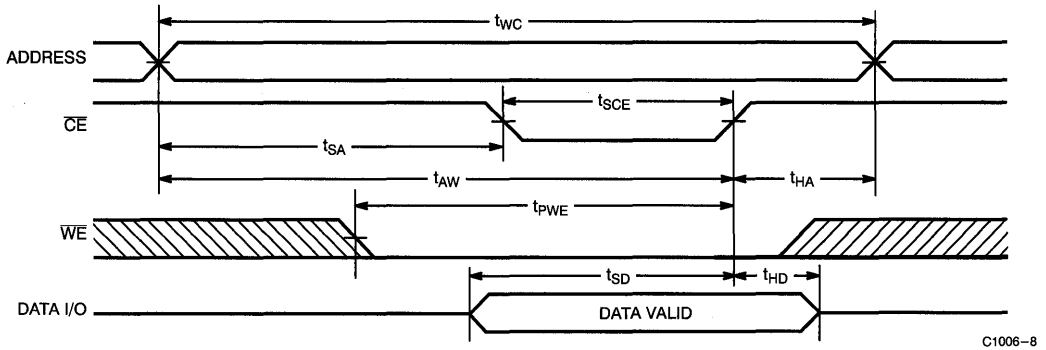


Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]

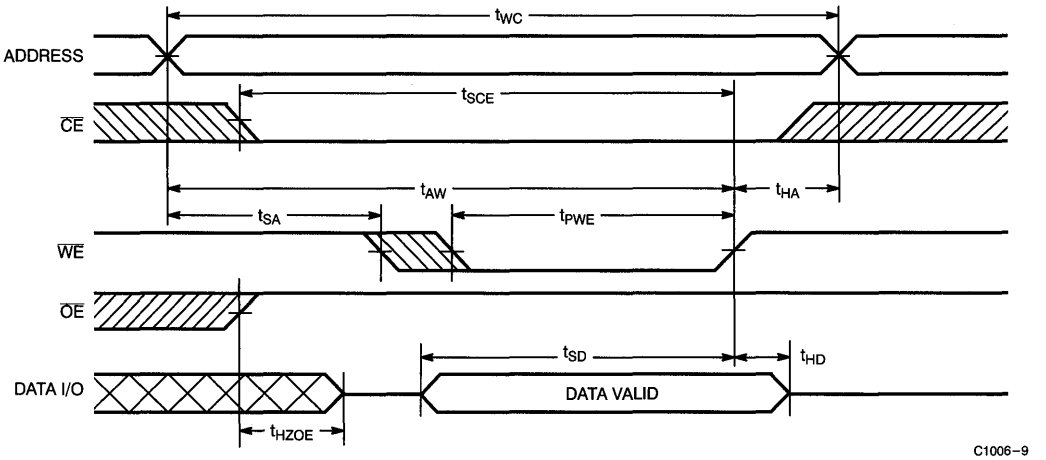


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

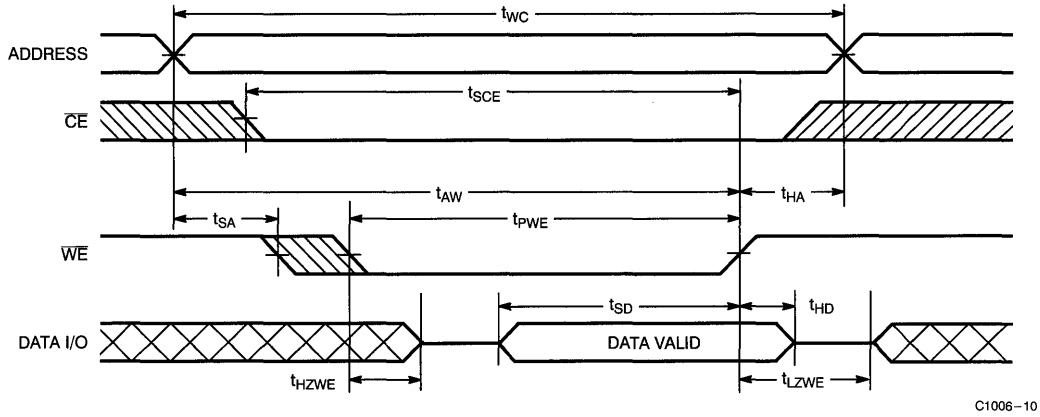


Notes:

12. Device is continuously selected, $\overline{OE}$ and $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1006–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–12VC	V21	28-Lead Molded SOJ	
15	CY7C1006–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–15VC	V21	28-Lead Molded SOJ	
	CY7C1006–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1006–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–20VC	V21	28-Lead Molded SOJ	
	CY7C1006–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1006–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–25VC	V21	28-Lead Molded SOJ	
	CY7C1006–25DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

1M x 1 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 825 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1007 is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

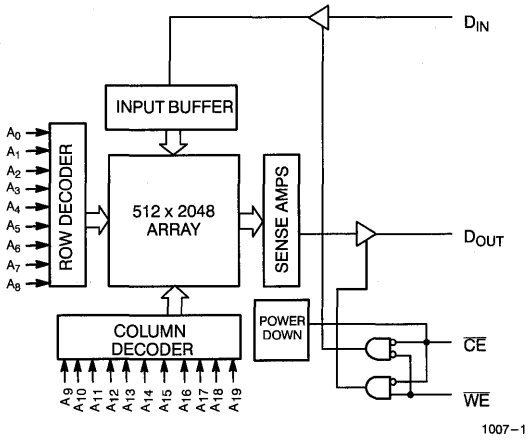
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

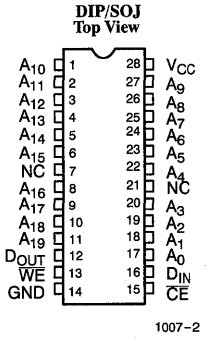
The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1007 is available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1007–12	7C1007–15	7C1007–20	7C1007–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	150	135	125	120
	Military		145	135	130
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics[3] Over the Operating Range

Parameter	Description	Test Conditions		7C1007–12 Min.	7C1007–12 Max.	7C1007–15 Min.	7C1007–15 Max.	7C1007–20 Min.	7C1007–20 Max.	7C1007–25 Min.	7C1007–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 1	+1	– 1	+1	– 1	+1	– 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 5	+5	– 5	+5	– 5	+5	– 5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300		– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		135		125		120	mA
			Mil				145		135		130	
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

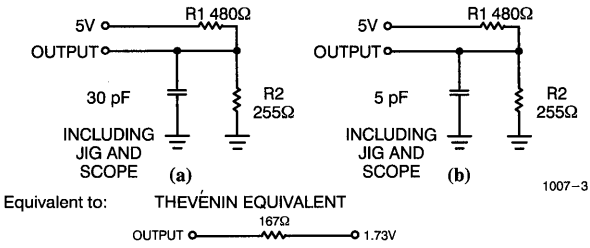
Capacitance[5]

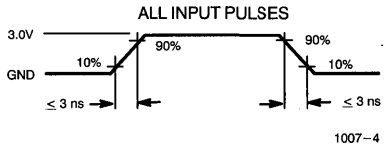
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. $V_{IL\,(min.)}$ = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C1007–12		7C1007–15		7C1007–20		7C1007–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

Notes:

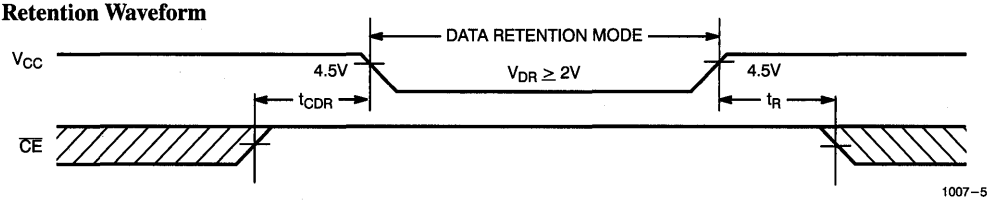
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

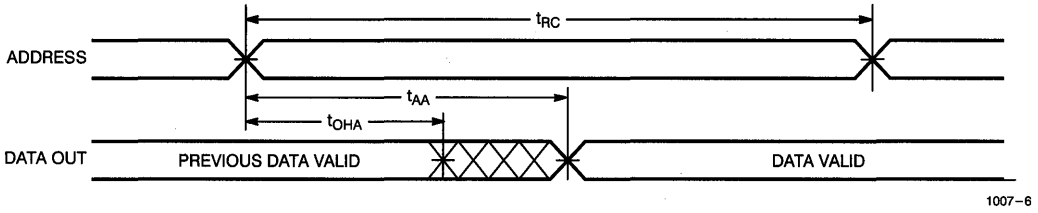
Note:
10. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

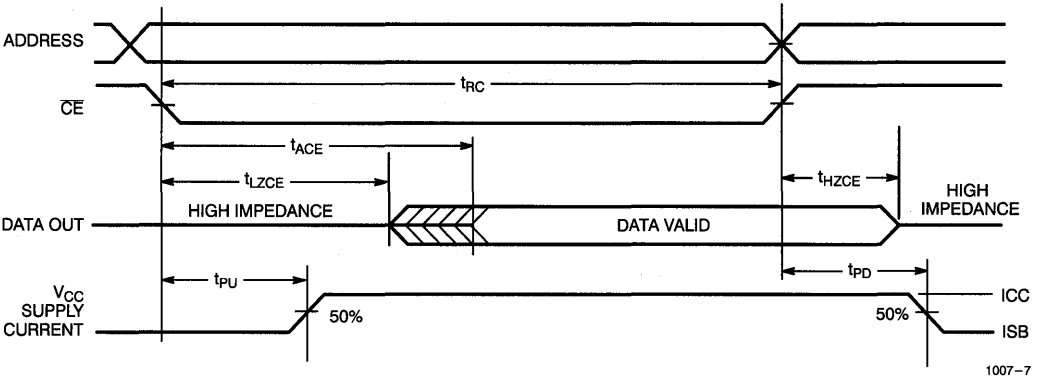


Switching Waveforms

Read Cycle No. 1[11, 12]



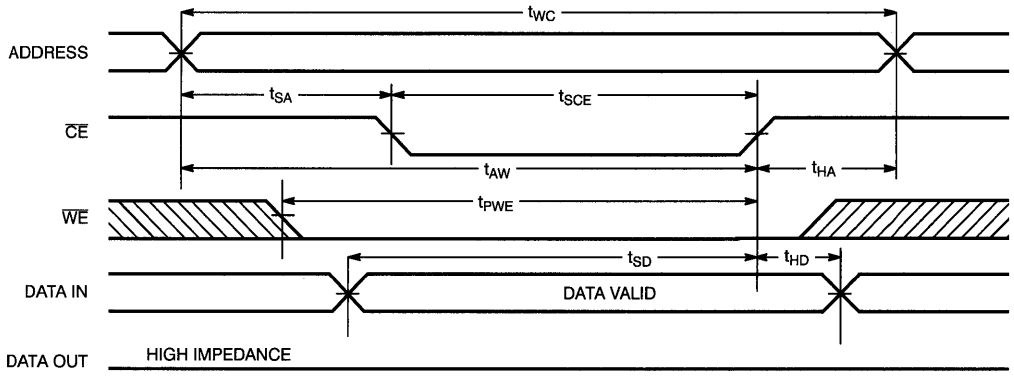
Read Cycle No. 2[12, 13]



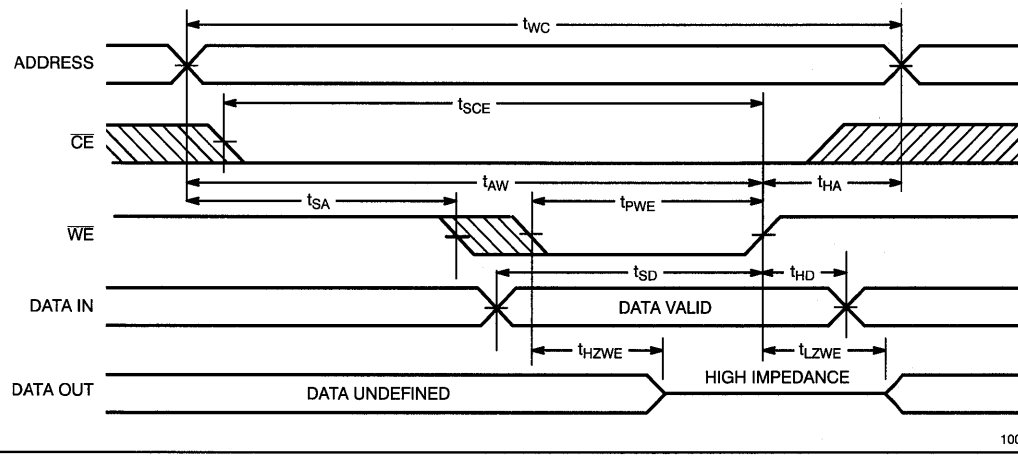
Notes:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1007–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–12VC	V21	28-Lead Molded SOJ	
15	CY7C1007–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–15VC	V21	28-Lead Molded SOJ	
	CY7C1007–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1007–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–20VC	V21	28-Lead Molded SOJ	
	CY7C1007–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1007–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–25VC	V21	28-Lead Molded SOJ	
	CY7C1007–25DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C1009**

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Low standby power**
  - **— 250 mW**
- **2.0V data retention**
  - **— 100 µW**
- **Available in 450 x 550-mil LCC**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C1009 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

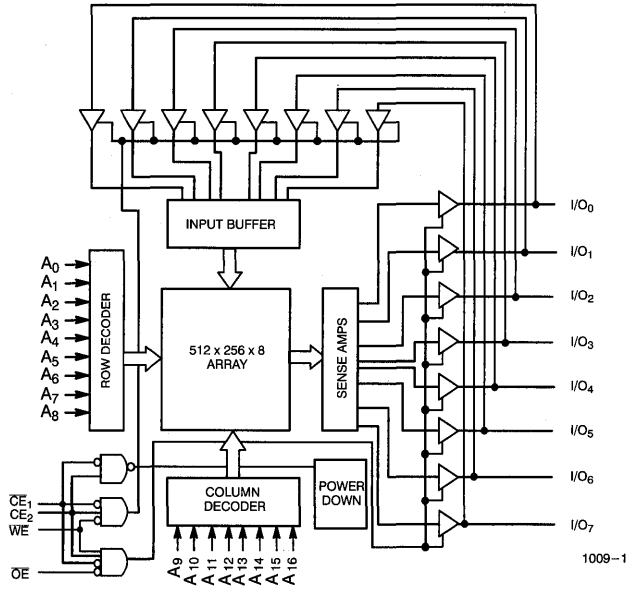
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

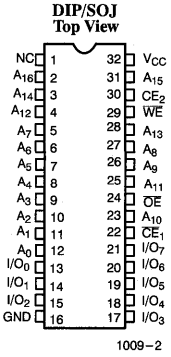
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

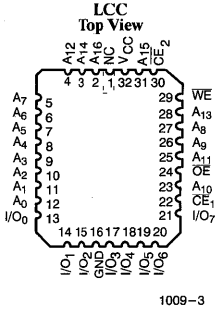
The CY7C1009 is available in standard 300-mil-wide DIPs, SOJs and a small footprint 450 x 550-mil leadless chip carrier.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C1009–12	7C1009–15	7C1009–20	7C1009–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	185	170	155	145
	Military		180	170	160
Maximum Standby Current (mA)	Commercial	45	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] . – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1009–12		7C1009–15		7C1009–20		7C1009–25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		155		145	mA
			Mil				180		170		160	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		45		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

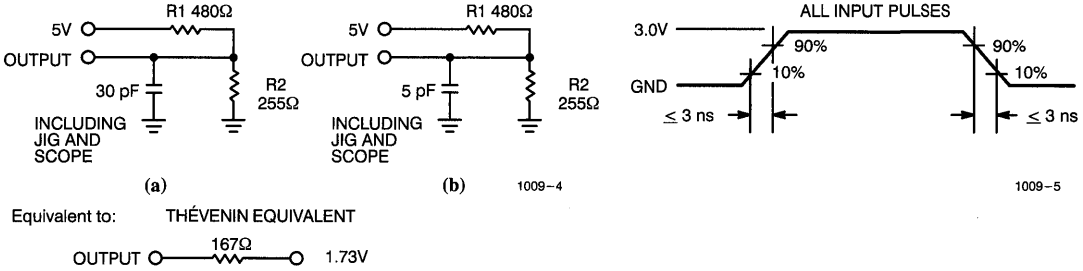
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Address	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C1009-12		7C1009-15		7C1009-20		7C1009-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		12		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to PowerDown		12		15		20		25	ns
WRITE CYCLE[9, 10]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

Notes:

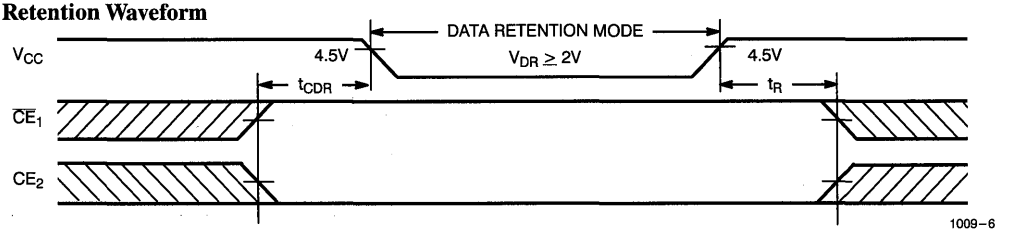
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	μA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

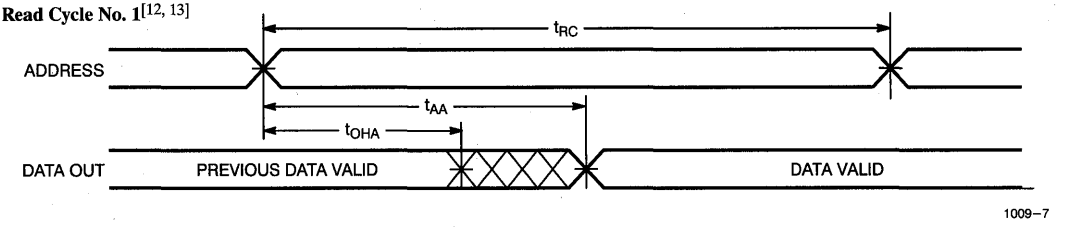
Note:
11. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

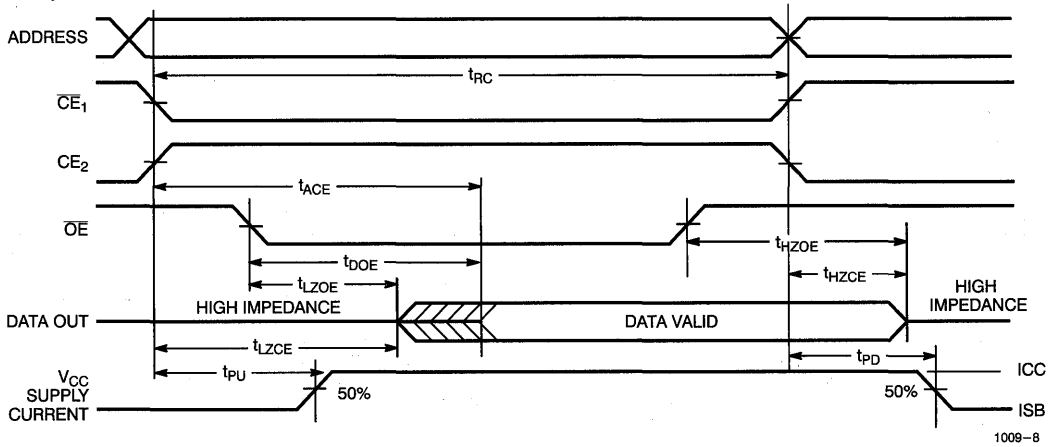


Switching Waveforms

Read Cycle No. 1[12, 13]



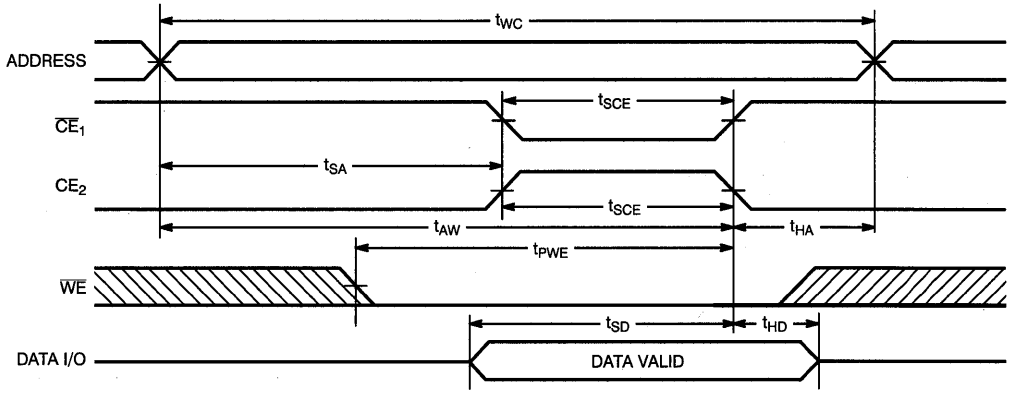
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



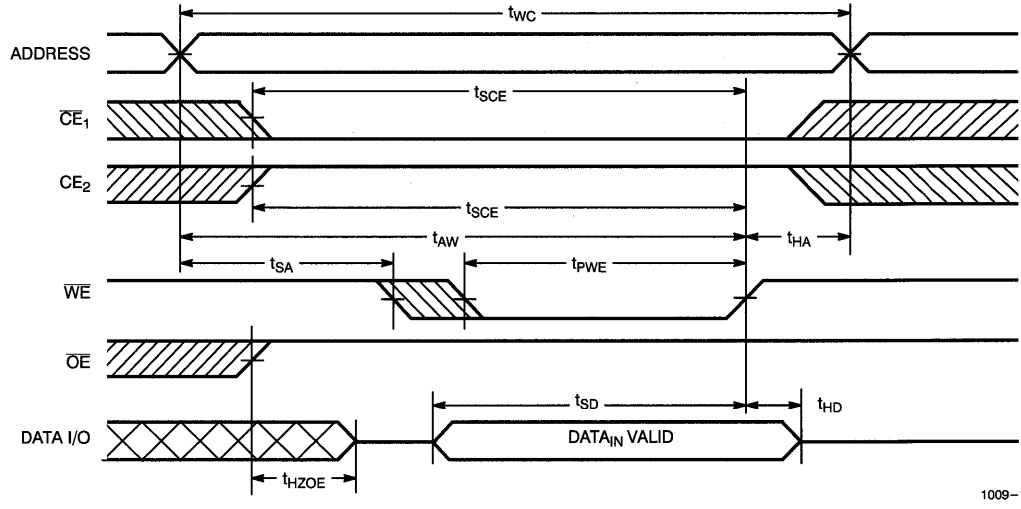
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

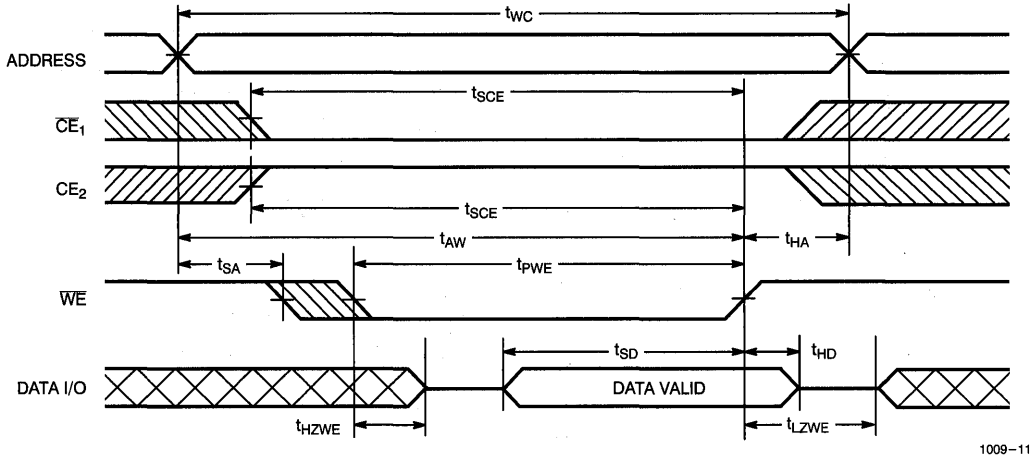


Notes:

15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1009–12PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1009–12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1009–15PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1009–15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–15DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C1009–20PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1009–20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C1009–25PC	P31	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C1009–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–25DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C1031
CY7C1032

64K x 18 Synchronous Cache RAM

Features

- **Supports 66-MHz Pentium™ microprocessor cache systems with zero wait states**
- **64K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 8.5 ns with 0-pF load**
  - **— 10 ns with 85-pF load**
- **Two-bit wraparound counter supporting Pentium microprocessor and 486 burst sequence (7C1031)**
- **Two-bit wraparound counter supporting linear burst sequence (7C1032)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **I/Os capable of 3.3V operation**
- **JEDEC-standard pinout**
- **52-pin PLCC and PQFP packaging**

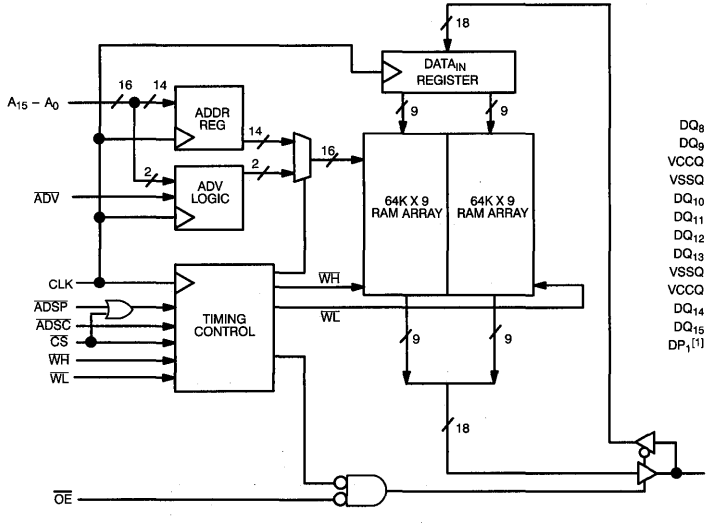
Functional Description

The CY7C1031 and CY7C1032 are 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C1031 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1032 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

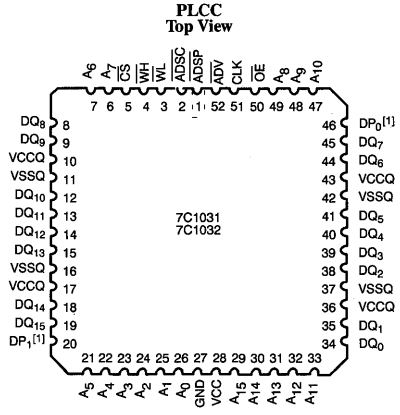
A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration

PLCC
Top View



Selection Guide

		7C1031–8 7C1032–8	7C1031–10 7C1032–10	7C1031–12 7C1032–12
Maximum Access Time (ns) (0-pF load)		8.5	10.5	12.5
Maximum Operating Current (mA)	Commercial	295	265	215
	Military			220

Shaded area contains advanced information.

Pentium is a trademark of Intel Corporation.

Note:

1. DP_0 and DP_1 are functionally equivalent to DQ_x.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1031 and CY7C1032 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C1031 and CY7C1032 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. Since the CY7C1031 and the CY7C1032 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data and parity lines. As a safety precaution, the appropriate data and parity lines are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ are sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

Burst Sequences

The CY7C1031 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor's address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1032 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 512-Kbyte secondary cache for the Pentium microprocessor using four CY7C1031 cache RAMs.

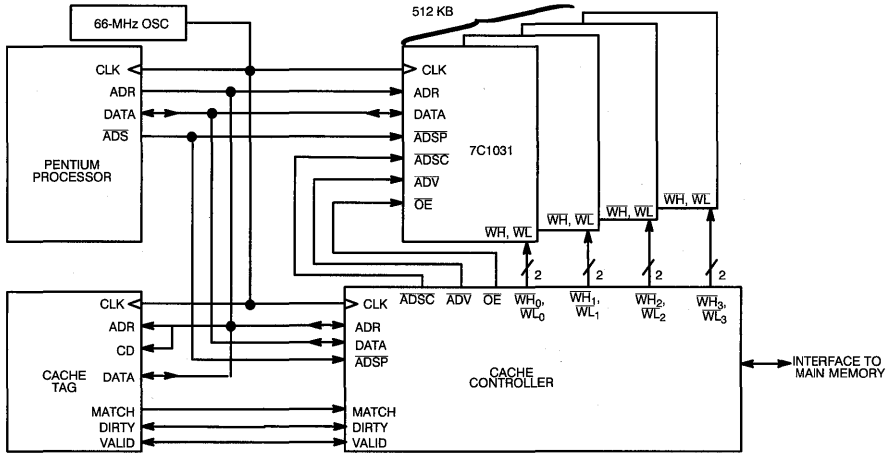


Figure 1. Cache Using Four CY7C1031s

Pin Definitions

Signal Name	Type	# of Pins	Description
VCC	Input	1	+5V Power
VCCQ	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
VSSQ	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{15} - A_0$	Input	16	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CS}$, $\overline{WH}$, $\overline{WL}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A15–A0	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C1032, the address will be incremented linearly. In the CY7C1031, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ15-DQ0	I/O	Sixteen bidirectional data I/O lines. $DQ_{15} - DQ_8$ are inputs to and outputs from the high-order half of the RAM array, while $DQ_7 - DQ_0$ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. $DQ_{15} - DQ_8$ and $DQ_7 - DQ_0$ are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, is sampled LOW at clock rise.
DP1–DP0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as $DQ_{15} - DQ_0$, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}	V_{CCQ}
Com'l	0°C to +70°C	5V ± 5%	3.0V – 5.5V
Mil	– 55°C to +125°C	5V ± 5%	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	7C1031–8 7C1032–8		7C1031–10 7C1032–10		7C1031–12 7C1032–12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	1	–1	1	–1	1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	5	–5	5	–5	5	µA

Notes:

2. Minimum voltage equals – 2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page for Group A subgroup testing information.

Electrical Characteristics (continued)

Parameter	Description	Test Conditions		7C1031–8 7C1032–8 Min.	7C1031–8 7C1032–8 Max.	7C1031–10 7C1032–10 Min.	7C1031–10 7C1032–10 Max.	7C1031–12 7C1032–12 Min.	7C1031–12 7C1032–12 Max.	Unit
I_{OS}	Output Short Circuit Current [5]	V_{CC}=Max., V_{OUT}=GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX} =1/t_{RC}	Com'l		295		265		215	mA
			Mil						250	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		60		50		40	mA
			Mil						50	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V, f=0[6]	Com'l		20		20		20	mA
			Mil						20	

Shaded areas contain advanced information

Capacitance[7]

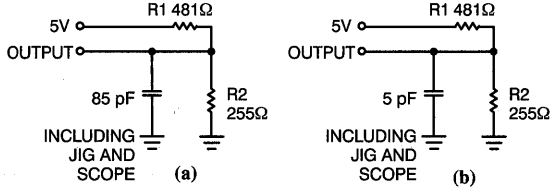
Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	Com'l	4	pF
			Mil	6	
C_{IN}: Other Inputs			Com'l	6	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	6	pF
			Mil	8	

Shaded areas contain advanced information

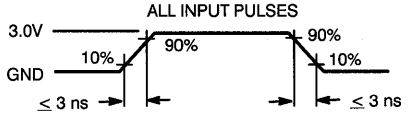
Notes:

5. Not more than one output should be shortened at one time. Duration of the short circuit should not exceed 30 seconds.
6. Clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

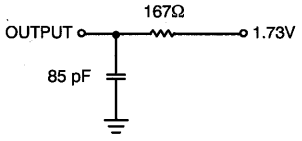


1031-3



1031-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[8]

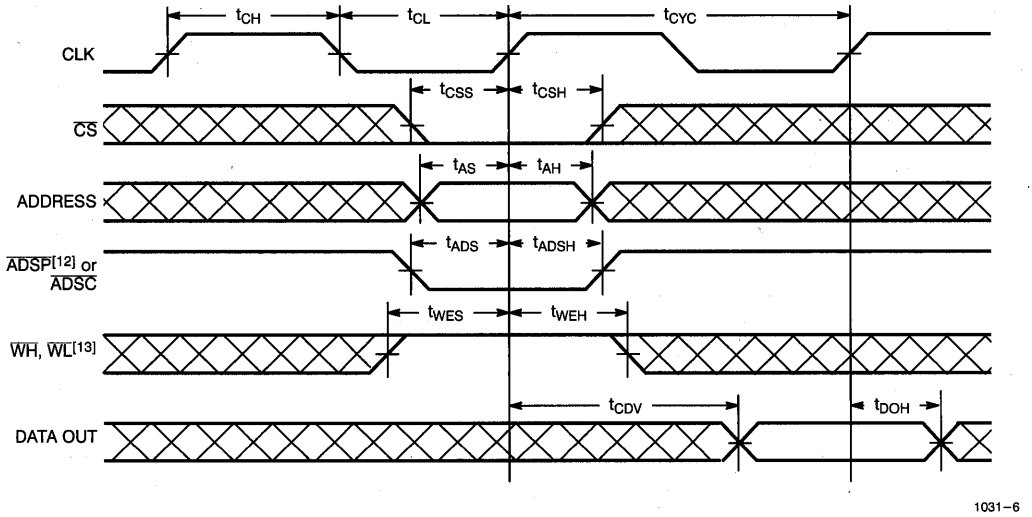
Parameter	Description	7C1031–8 7C1032–8		7C1031–10 7C1032–10		7C1031–12 7C1032–12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	12.5		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		1		ns
t_{CDV1}	Data Output Valid After CLK Rise, 0-pF Load		8.5		10.5		12.5	ns
t_{CDV2}	Data Output Valid After CLK Rise, 85-pF Load		10		12		14	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		3		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		1		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[9,10]		6		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[10]		10		12		14	ns

Notes:

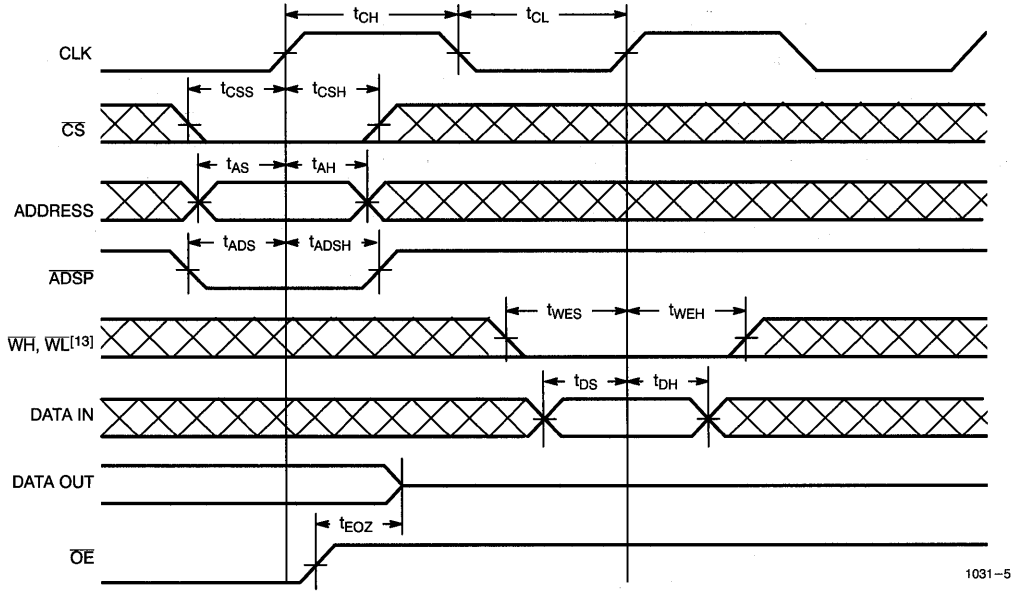
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[11]



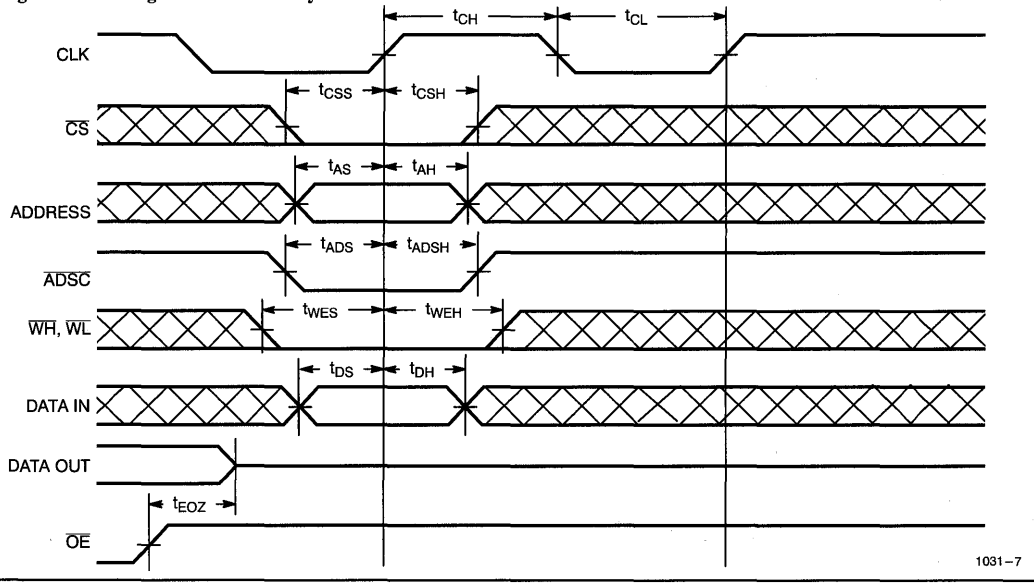
Single Write Timing: Write Initiated by $\overline{ADSP}$



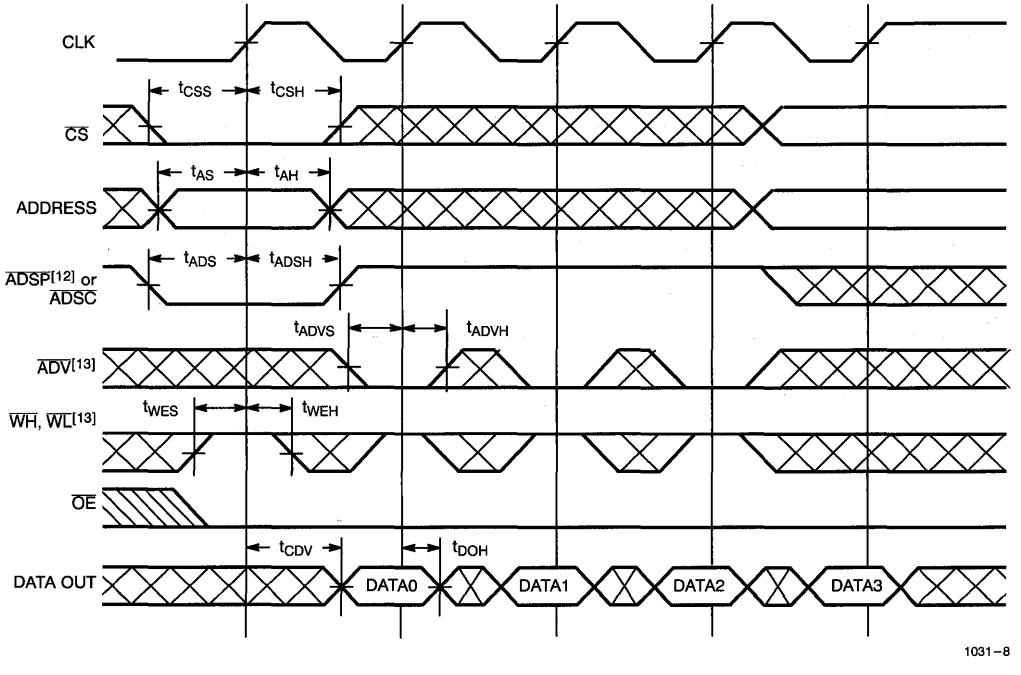
Notes:
11. $\overline{OE}$ is LOW throughout this operation.
12. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
13. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WL}$, and $\overline{WH}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

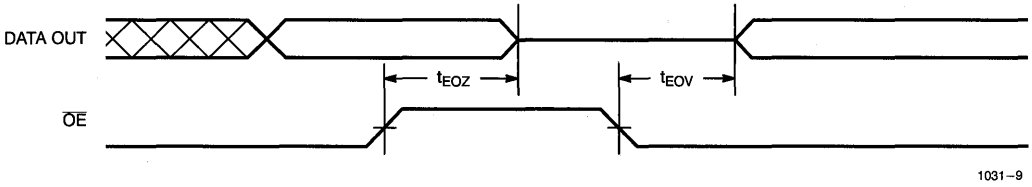


Burst Read Sequence with Four Accesses

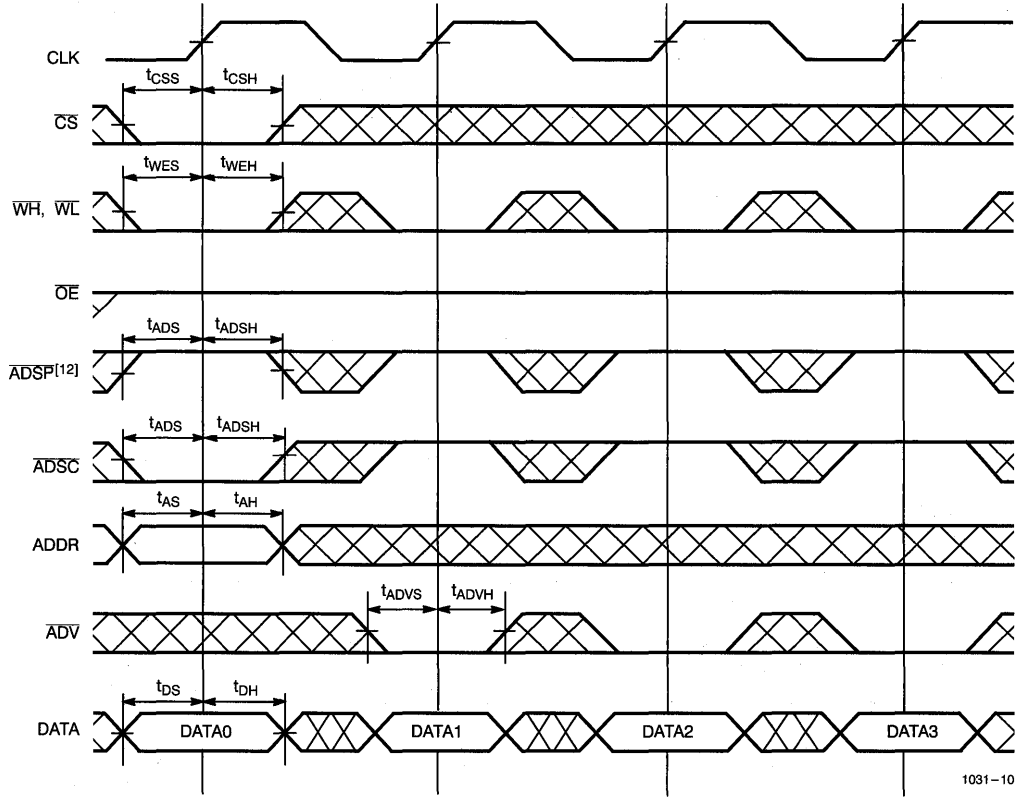


Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)

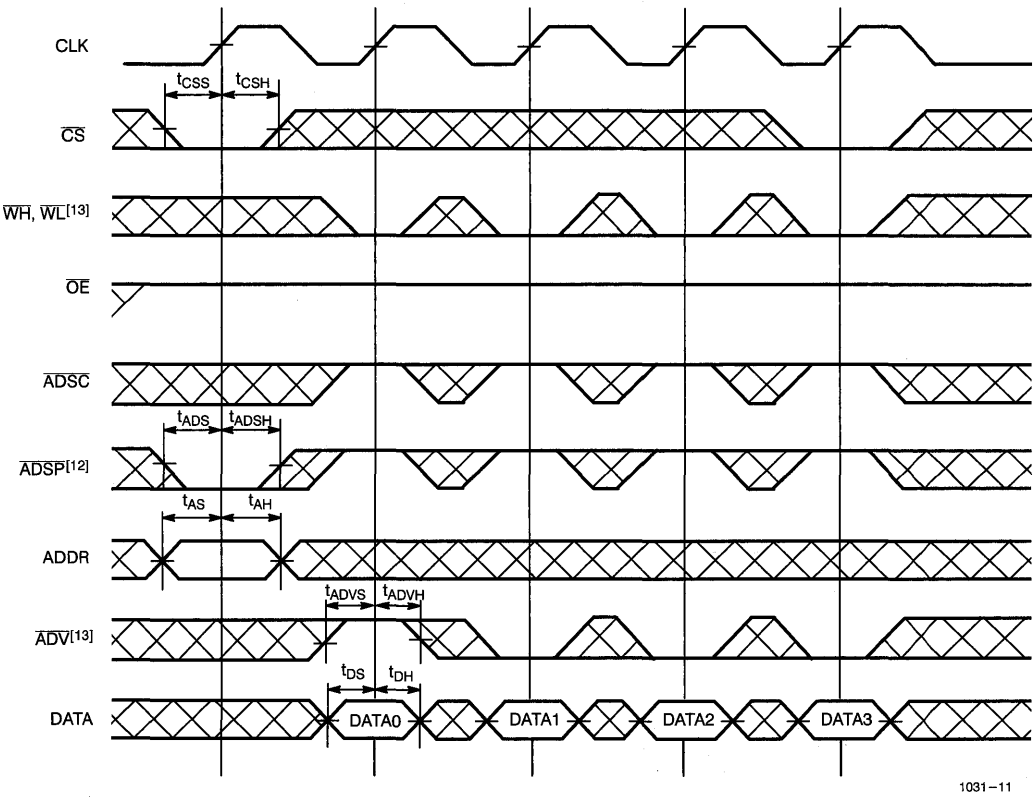


Write Burst Timing: Write Initiated by $\overline{ADSC}$



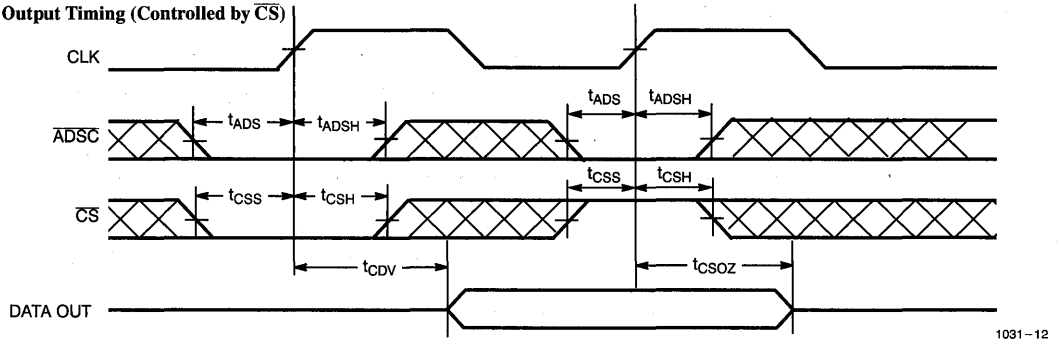
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

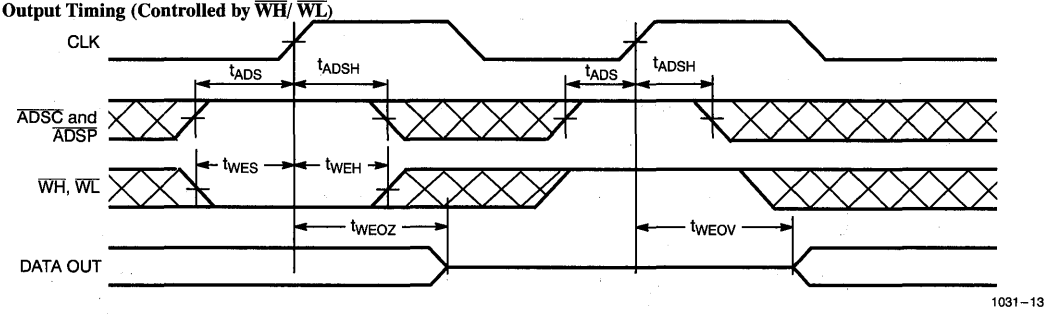


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}$/ $\overline{WL}$)



Truth Table

Input						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1031–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C1031–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C1031–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031–12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C1031–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1032–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C1032–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C1032–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032–12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C1032–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

Document #: 38–00219–A

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7B1051
CY7B1061

64K x 18 and 128K x 18 Synchronous Pipelined Cache R/W RAM

Features

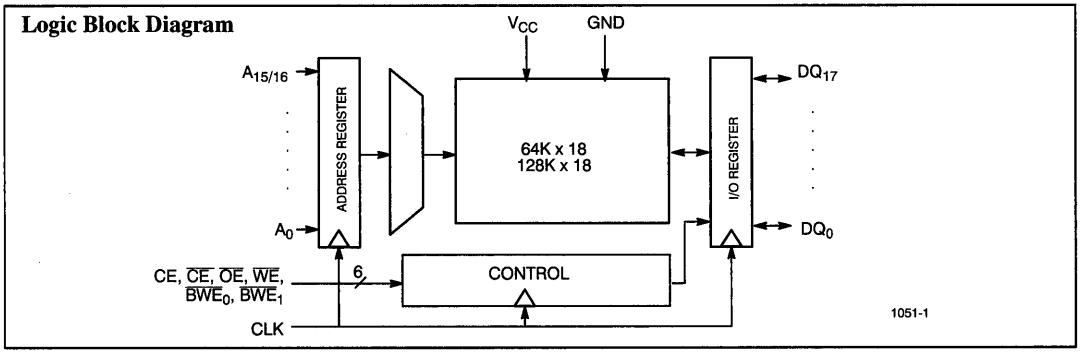
- **Supports 200-MHz cache systems**
- **64K by 18 (7B1051) and 128K by 18 (7B1061) common I/O**
- **BiCMOS for optimum speed/power**
- **3-ns access delay (clock to output)**
- **5-ns cycle time (input to output)**
- **3.3V power supply**
- **3.3V GTL-capable I/O logic levels**
- **Write-through and byte-write capability**
- **Synchronous self-timed write**
- **Direct interface with the processor**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable option**

Functional Description

The CY7B1051 and CY7B1061 are 3.3V devices with the 5-ns t_{CYC} and 3-ns t_{CO} needed to run at 200-MHz clock speeds. Since Pentium™ (P5) and the new RISC processors have 64-bit and wider data buses with ECC and parity, x9, x18, and x36 wide parts will be necessary to trade off between cache depth and width to satisfy both low-end and high-end systems (see the and CY7B1055/65 datasheet). The I/O is designed for GTL-capable signal swings to achieve maximum speed with minimal noise. C_{IN} on all inputs except DQ is 5 pF max. and $DQ_0 - DQ_{17}$ is 7 pF to provide less loading on the processor outputs. A pipelined architecture is implemented by placing registers at both the data inputs and data outputs of the device. The advantage of this architecture is that it allows the designer to minimize the cycle time for the device by equalizing the delays through each segment of the pipeline. The devices are completely synchronous, therefore all the registers in the CY7B1051 and CY7B1061 (including the address and control registers) operate off the same clock. A consequence of these features is a one-clock latency between address and data. In other words, when an address is registered at a clock rise, the data corresponding to that address will be delivered to the data outputs following the next rising edge of the clock. Also, the control signals (write enable, output enable, and chip enable) follow a similar pipelined path to insure that the proper control accompanies the appropriate access. The write operations are greatly simplified by the self-timed write mechanism. An asynchronous output enable ($\overline{OE}$) option is available as well as a control pin to disable the output register to allow for flow-through operation where latency needs to be avoided. The CY7B1051 and CY7B1061 are packaged in 100-pin PBGAs (plastic ball grid array) and PGAs.

Pipelined SRAMs have architectures such that the propagation delays through the device are divided by a technique of registering information at intermediate states with a common clock signal. In this manner, each of the processes may be done concurrently. In a pipelined SRAM, the registers are inserted in two locations, between the address/control/data inputs and the memory cell and also between the memory cells and the data outputs. In this arrangement, the address, control, and data in (in case of a write) of the current access are clocked into the RAM while the data from the previous access is clocked out to the I/O pins. A write pass-through mode is included. In this mode, when chip enable ($\overline{CE}$) is deasserted while write ($\overline{WE}$) is asserted, the values registered at the data inputs are routed around the core to the output registers and presented at the data output pins on the next clock. This mode requires that the $\overline{OE}$ pin be asserted during the same cycle that the write is asserted.

Logic Block Diagram



Selection Guide

		7B1051–5 7B1061–5	7B1051–7 7B1061–7
Maximum Cycle Time (ns)		5	7
Maximum Operating Current (mA)	Commercial	TBD	TBD
	Military		TBD

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Document #: 38–A–00038

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7B1055
CY7B1065

32K x 36 and 64K x 36 Synchronous Pipelined Cache R/W RAM

Features

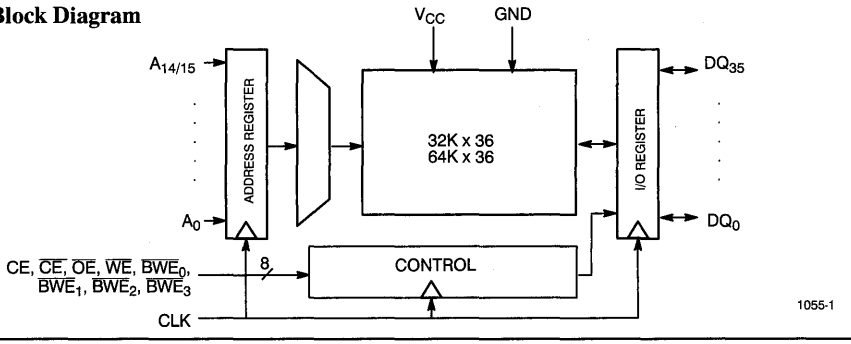
- **Supports 200-MHz cache systems**
- **32K by 36 (7B1055) and 64K by 36 (7B1065) common I/O**
- **BiCMOS for optimum speed/power**
- **3-ns access delay (clock to output)**
- **5-ns cycle time (input to output)**
- **3.3V power supply**
- **3.3V GTL-capable I/O logic levels**
- **Write-through and byte-write capability**
- **Synchronous self-timed write**
- **Direct interface with the processor**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable option**

Functional Description

The CY7B1055 and CY7B1065 are 3.3V devices with the 5-ns t_{CYC} and 3-ns t_{CO} needed to run at 200-MHz clock speeds. Since Pentium™ (P5) and the new RISC processors have 64-bit and wider data buses with ECC and parity, x9, x18, and x36 wide parts will be necessary to trade off between cache depth and width to satisfy both low-end and high-end systems (see the CY7B1051/61 datasheet). The I/O is designed for GTL-capable signal swings to achieve maximum speed with minimal noise. C_{IN} on all inputs except DQ is 5 pF max. and DQ_0 – DQ_{35} is 7 pF to provide less loading on the processor outputs. A pipelined architecture is implemented by placing registers at both the data inputs and data outputs of the device. The advantage of this architecture is that it allows the designer to minimize the cycle time for the device by equalizing the delays through each segment of the pipeline. The devices are completely synchronous, therefore all the registers in the CY7B1055 and CY7B1065 (including the address and control registers) operate off the same clock. A consequence of these features is a one-clock latency between address and data. In other words, when an address is registered at a clock rise, the data corresponding to that address will be delivered to the data outputs following the next rising edge of the clock. Also, the control signals (write enable, output enable, and chip enable) follow a similar pipelined path to insure that the proper control accompanies the appropriate access. The write operations are greatly simplified by the self-timed write mechanism. An asynchronous output enable ($\overline{OE}$) option is available as well as a control pin to disable the output register to allow for flow-through operation where latency needs to be avoided. The CY7B1055 and CY7B1065 are packaged in 100-pin PBGAs (plastic ball grid array) and PGAs.

Pipelined SRAMs have architectures such that the propagation delays through the device are divided by a technique of registering information at intermediate states with a common clock signal. In this manner, each of the processes may be done concurrently. In a pipelined SRAM, the registers are inserted in two locations, between the address/control/data inputs and the memory cell and also between the memory cells and the data outputs. In this arrangement, the address, control, and data in (in case of a write) of the current access are clocked into the RAM while the data from the previous access is clocked out to the I/O pins. A write pass-through mode is included. In this mode, when chip enable ($\overline{CE}$) is deasserted while write ($\overline{WE}$) is asserted, the values registered at the data inputs are routed around the core to the output registers and presented at the data output pins on the next clock. This mode requires that the $\overline{OE}$ pin be asserted during the same cycle that the write is asserted.

Logic Block Diagram



Selection Guide

		7B1055–5 7B1065–5	7B1055–7 7B1065–7
Maximum Cycle Time (ns)		5	7
Maximum Operating Current (mA)	Commercial	TBD	TBD
	Military		TBD

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Document #: 38–A–00039

CY7B1094
CY7B1095
CY7B1096

PRELIMINARY

CYPRESS SEMICONDUCTOR

64K x 4 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 6 ns**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 900 mW**
- **Low standby power**
  - **— 350 mW**
- **Automatic power-down when deselected**
- **Output enable ($\overline{OE}$) feature**
- **Both 5V and 3.3V TTL-compatible inputs and outputs**

Functional Description

The CY7B1094, CY7B1095, and CY7B1096 are high-performance BiCMOS static RAMs organized as 65,536 words by 4 bits. All devices have a revolutionary center power/ground configuration. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active LOW chip enable ($\overline{CE}_2$, CY7B1096 only), an active LOW output enable ($\overline{OE}$), and three-state drivers. All devices have an automatic power-down feature that reduces power consumption by more than 54% when deselected. Also, for 3.3V systems, V_{OH} is limited to 3.3V max.

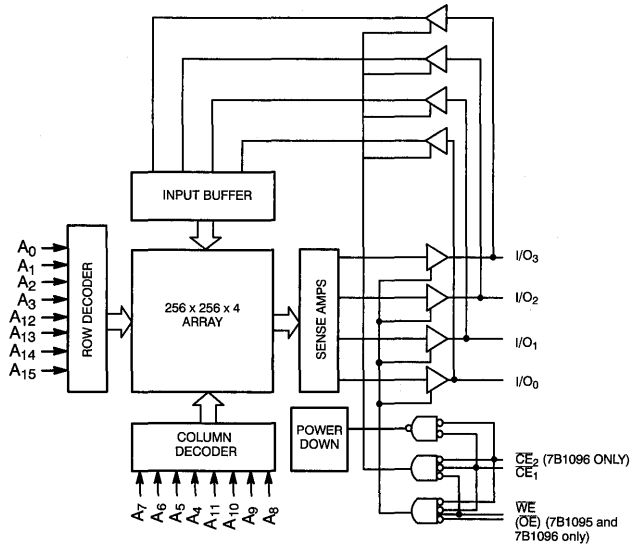
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs and chip enable two ($\overline{CE}_2$, CY7B1096 only) LOW. Data on the I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$), chip enable two ($\overline{CE}_2$, CY7B1096 only), and output enable ($\overline{OE}$) LOW, while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ HIGH for the CY7B1096), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ for the CY7B1096, and $\overline{WE}$ all LOW).

The CY7B1094, CY7B1095, and CY7B1096 are available in leadless chip carriers, 300-mil-wide center power/ground DIPs, and SOJs.

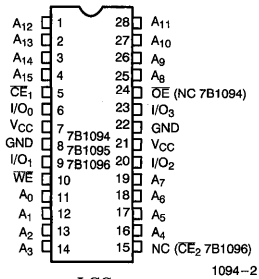
Logic Block Diagram



1094–1

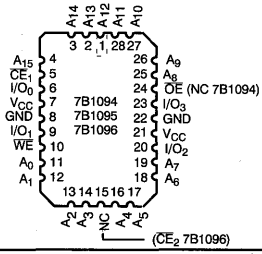
Pin Configurations

DIP/SOJ
Top View



1094–2

LCC
Top View



1094–3

Selection Guide

		7B1094–6 7B1095–6 7B1096–6	7B1094–8 7B1095–8 7B1096–8	7B1094–9 7B1095–9 7B1096–9
Maximum Access Time (ns)		6	8	9
Maximum Operating Current (mA)	Commercial	180	180	
	Military		180	180
Maximum Standby Current (mA)	Commercial	70	70	
	Military		80	80

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to +7.0V

DC Input Voltage[1] ..... – 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B1094–6 7B1095–6 7B1096–6 Min.	7B1094–6 7B1095–6 7B1096–6 Max.	7B1094–8, 9 7B1095–8, 9 7B1096–8, 9 Min.	7B1094–8, 9 7B1095–8, 9 7B1096–8, 9 Max.	Unit
V_{OH}[4]	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4	3.3	2.4	3.3	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 10	+10	– 10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		180		180	mA
			Mil				180	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} f = f_{MAX} = $1/t_{RC}$	Com'l		70		70	mA
			Mil				80	
I_{SB2}[4]	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		20		20	mA
			Mil				30	

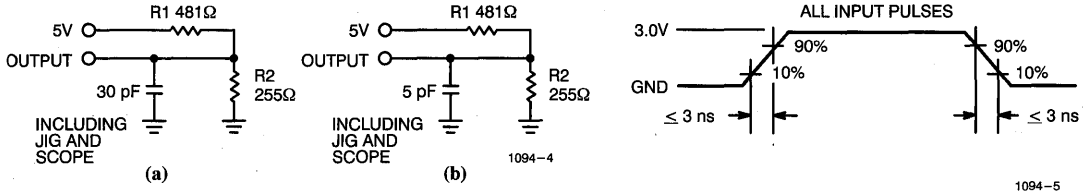
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

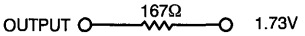
Notes:

1. $V_{IL\,(min.)}$ = – 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V_{OH} maximum is limited by internal temperature-compensated bandgap reference. The output will not go above 3.3V unless externally pulled to above 3.3V.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



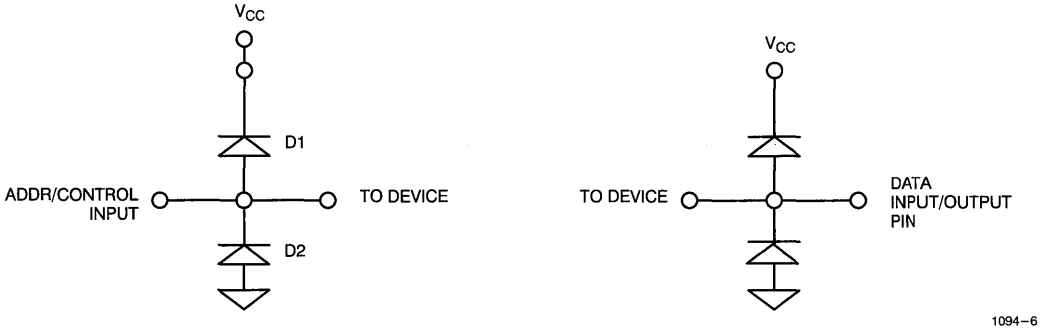
Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B1094–6 7B1095–6 7B1096–6 Min.	7B1094–6 7B1095–6 7B1096–6 Max.	7B1094–8 7B1095–8 7B1096–8 Min.	7B1094–8 7B1095–8 7B1096–8 Max.	7B1094–9 7B1095–9 7B1096–9 Min.	7B1094–9 7B1095–9 7B1096–9 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	6		8		9		ns
t_{AA}	Address to Data Valid		6		8		9	ns
t_{OHA}	Data Hold from Address Change	2.5		2.5		2.5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		6		8		9	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		3.5		4		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		6		10		12	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	6		8		9		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	5		6		7		ns
t_{AW}	Address Set-Up to Write End	4		6		7		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	4		6		7		ns
t_{SD}	Data Set-Up to Write End	3		4		5		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]	0	3	0	4	0	4.5	ns

Notes:

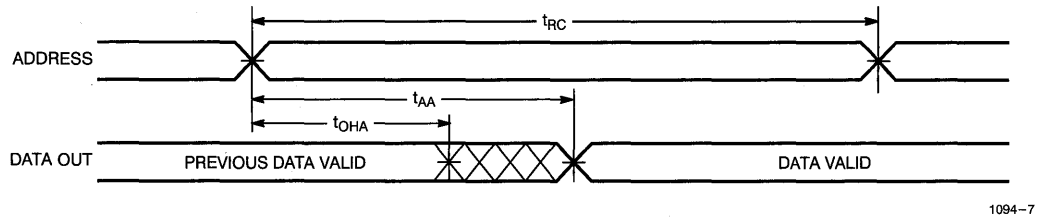
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Input/Output ESD and Clamp Diode Protection

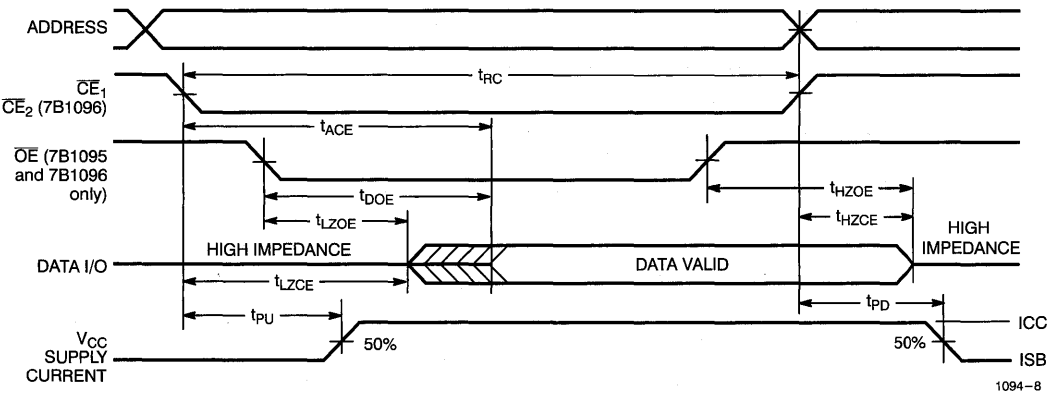


Switching Waveforms

Read Cycle No. 1[12, 13]



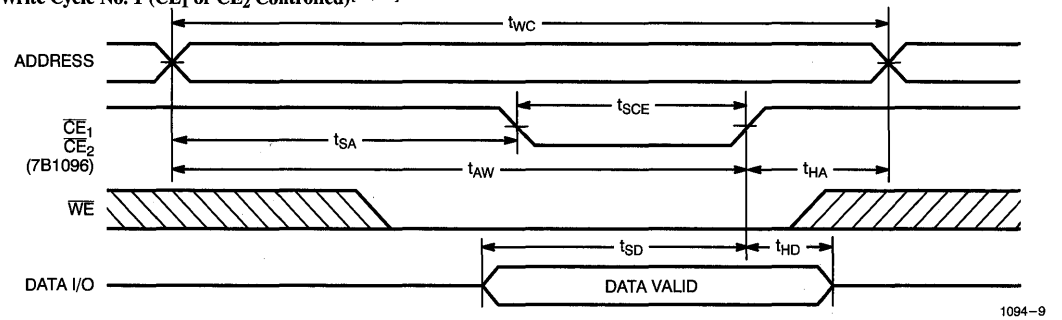
Read Cycle No. 2[13, 14]



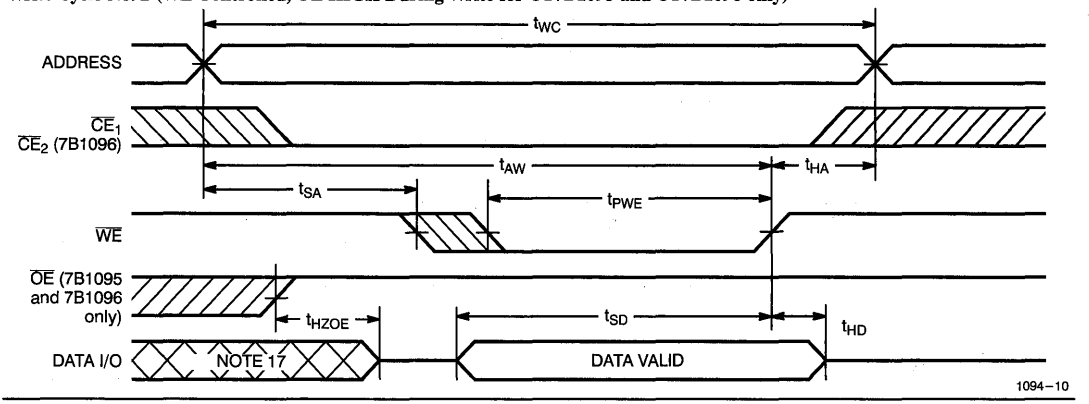
Notes:
12. Device is continuously selected. $\overline{CE}$ and $\overline{OE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

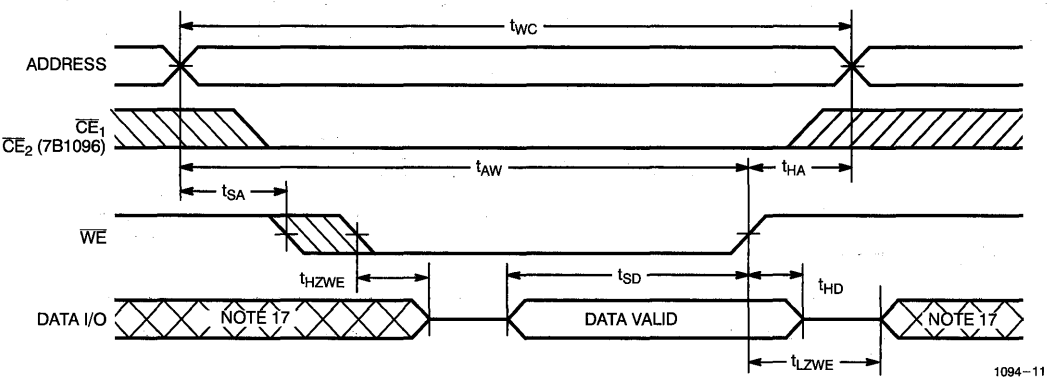
Write Cycle No. 1 ($\overline{CE}_1$ or $\overline{CE}_2$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for CY7B1095 and CY7B1096 only)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this time the I/Os are in the output mode and input signals must be applied.

7B1094 Truth Table

$\overline{CE}_1$	$\overline{WE}$	Input/Output	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7B1095 Truth Table

$\overline{CE}_1$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

7B1096 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1094–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1094–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1094–8VC	V21	28-Lead Molded SOJ	
	CY7B1094–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1094–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1094–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1094–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1095–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1095–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1095–8VC	V21	28-Lead Molded SOJ	
	CY7B1095–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1095–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1095–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1095–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1096–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1096–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1096–8VC	V21	28-Lead Molded SOJ	
	CY7B1096–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1096–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1096–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1096–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7B1099**

32K x 8 Static R/W RAM

Features

- **High speed**
  — t_{AA} = 6 ns
- **BiCMOS for optimum speed/power**
- **Low active power**
  — 900 mW
- **Low standby power**
  — 350 mW
- **Automatic power-down when deselected**
- **Output enable ($\overline{OE}$) feature**
- **Both 5V and 3.3V TTL-compatible inputs and outputs**

Functional Description

The CY7B1099 is a high-performance BiCMOS static RAM organized as 32,768 words by 8 bits. The CY7B1099 has a revolutionary center power/ground configuration. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 56% when deselected. Also, for 3.3V systems, V_{OH} is limited to 3.3V max.

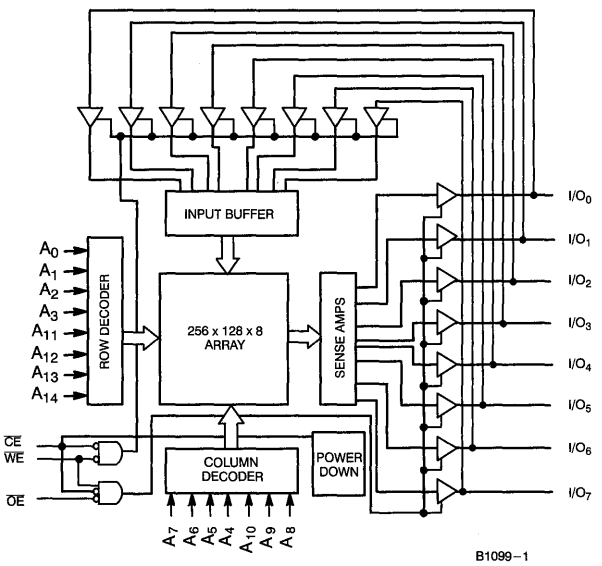
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7B1099 is available in leadless chip carriers, and 300-mil-wide center power/ground SOJs.

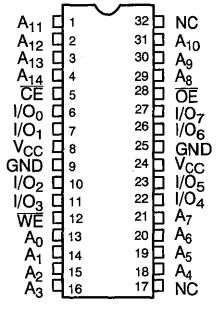
Logic Block Diagram



B1099–1

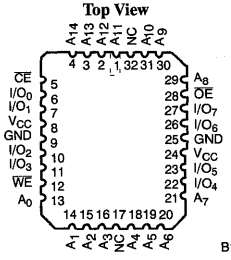
Pin Configurations

SOJ
Top View



B1099–2

LCC
Top View



B1099–3

Selection Guide

		7B1099–6	7B1099–8	7B1099–9
Maximum Access Time (ns)		6	8	9
Maximum Operating Current (mA)	Commercial	180	180	
	Military		180	180
Maximum Standby Current (mA)	Commercial	70	70	
	Military		80	80

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B1099−6 Min.	7B1099−6 Max.	7B1099−8, 9 Min.	7B1099−8, 9 Max.	Unit
V_{OH}[4]	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4	3.3	2.4	3.3	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		180		180	mA
			Mil				180	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} f = f_{MAX} = $1/t_{RC}$	Com'l		70		70	mA
			Mil				80	
I_{SB2}[4]	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		20		20	mA
			Mil				30	

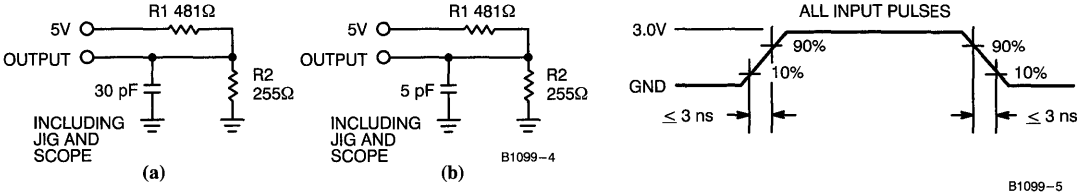
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

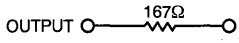
Notes:

1. $V_{IL\,(min.)}$ = − 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V_{OH} maximum is limited by internal temperature-compensated bandgap reference. The output will not go above 3.3V unless externally pulled to above 3.3V.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



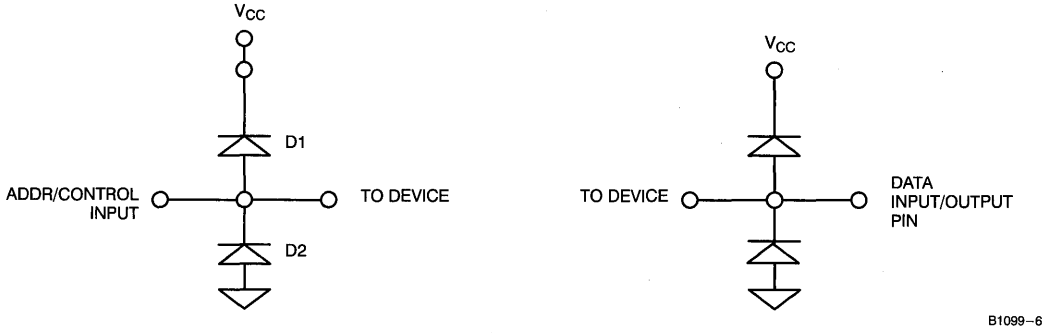
Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B1099–6		7B1099–8		7B1099–9		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	6		8		9		ns
t_{AA}	Address to Data Valid		6		8		9	ns
t_{OHA}	Data Hold from Address Change	2.5		2.5		2.5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		6		8		9	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		3.5		4		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		6		10		12	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	6		8		9		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	5		6		7		ns
t_{AW}	Address Set-Up to Write End	4		6		7		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	4		6		7		ns
t_{SD}	Data Set-Up to Write End	3		4		5		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]	0	3	0	4	0	4.5	ns

Notes:

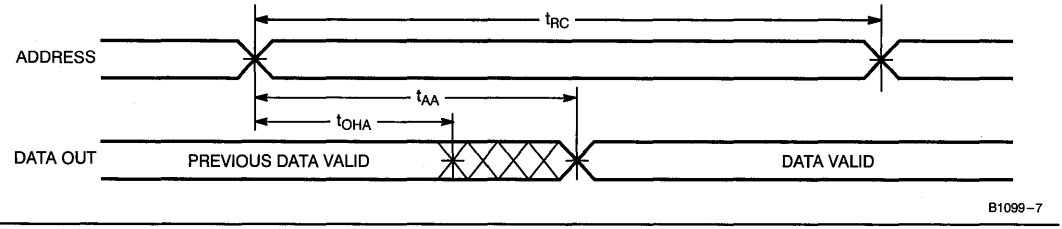
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Input/Output ESD and Clamp Diode Protection

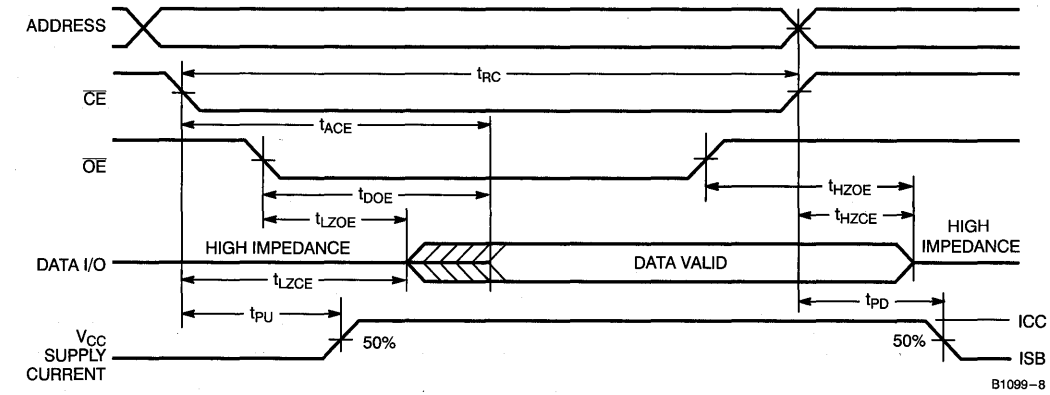


Switching Waveforms

Read Cycle No. 1[12, 13]



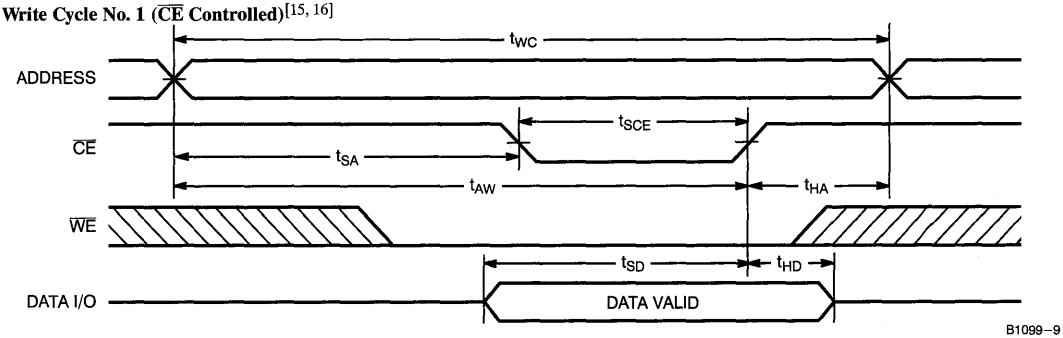
Read Cycle No. 2[13, 14]



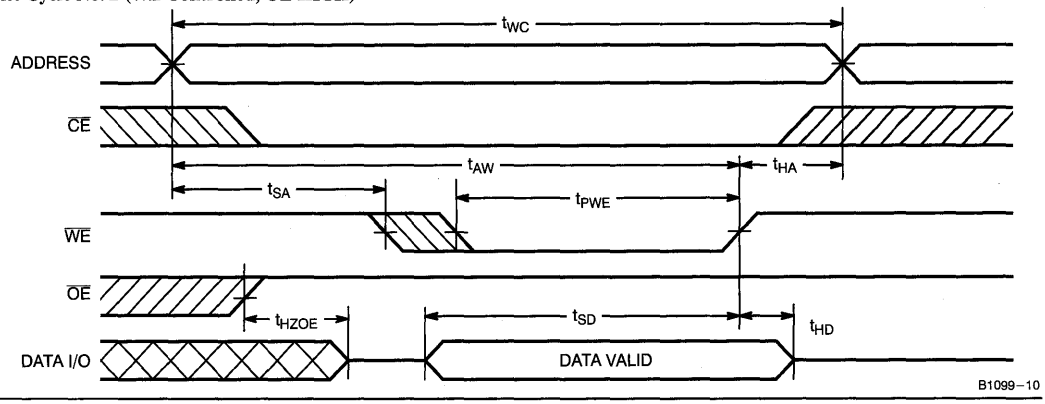
Notes:
12. Device is continuously selected. $\overline{CE}$ and $\overline{OE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

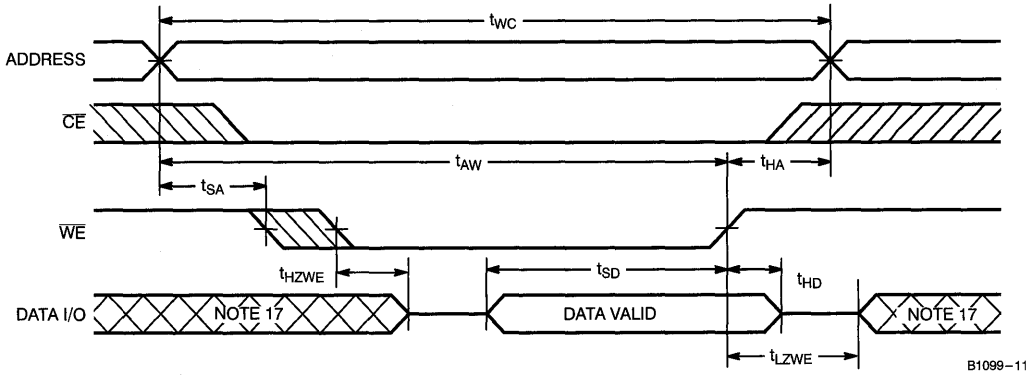
Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Notes:

15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this time the I/Os are in the output mode and input signals must not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1099–6VC	V32	32-Lead Molded SOJ	Commercial
8	CY7B1099–8VC	V32	32-Lead Molded SOJ	Commercial
	CY7B1099–8LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
9	CY7B1099–9LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7C1331
CY7C1332

64K x 18 Synchronous Cache 3.3V RAM

Features

- **Supports 50-MHz Pentium™ processor cache systems with zero wait states**
- **64K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 12.5 ns with 0-pF load**
  - **— 14 ns with 85-pF load**
- **Two-bit wraparound counter supporting the Pentium and 486 burst sequence (7C1331)**
- **Two-bit wraparound counter supporting linear burst sequence (7C1332)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **JEDEC-standard pinout**
- **52-pin PLCC and PQFP packaging**

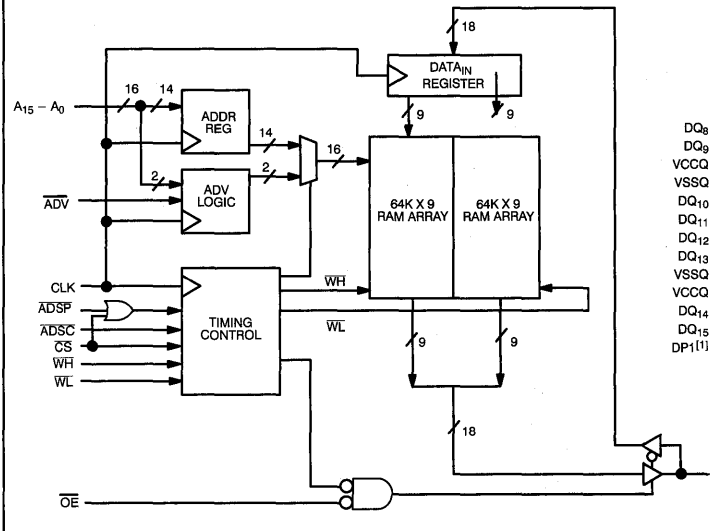
Functional Description

The CY7C1331 and CY7C1332 are 3.3V 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 12.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

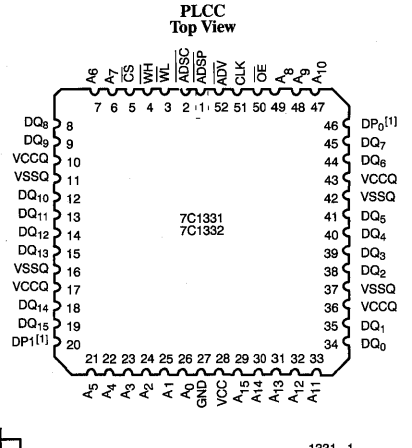
The CY7C1331 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1332 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1331–12 7C1332–12	7C1331–16 7C1332–16	7C1331–19 7C1332–19
Maximum Access Time (ns) (0-pF load)		12.5	16.5	19.5
Maximum Operating Current (mA)	Commercial	180	160	150
	Military			170

Pentium is a trademark of Intel Corporation.

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_X.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1331 and CY7C1332 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C1331 and CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Since the CY7C1331 and the CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data lines. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 12.5 ns after clock rise.

Burst Sequences

The CY7C1331 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1332 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure1 shows a 512-Kbyte secondary cache for a hypothetical 3.3V, 50-MHz Pentium or i486 processor using four CY7C1331 cache RAMs.

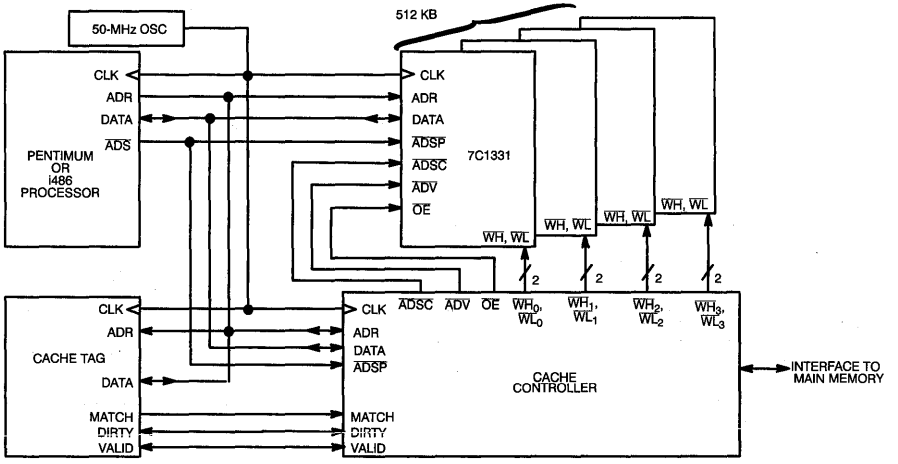


Figure 1. Cache Using Four CY7C1331s

Pin Definitions

Signal Name	Type	# of Pins	Description
VCC	Input	1	+3.3V Power
VCCQ	Input	4	+3.3V (Outputs)
GND	Input	1	Ground
VSSQ	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{15} - A_0$	Input	16	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{WH}$, $\overline{WL}$, $\overline{CS}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A15–A0	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the two-bit on-chip auto-address-increment counter. In the CY7C1332, the address will be incremented linearly. In the CY7C1331, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three–stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ15-DQ0	I/O	Sixteen bidirectional data I/O lines. $DQ_{15} - DQ_8$ are inputs to and outputs from the high-order half of the RAM array, while $DQ_7 - DQ_0$ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. $DQ_{15} - DQ_8$ and $DQ_7 - DQ_0$ are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, are sampled LOW at clock rise.
DP1–DP0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as $DQ_{15} - DQ_0$, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... – 0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[2] ..... – 0.5V to V_{CC} + 0.3V

DC Input Voltage[2] ..... – 0.5V to V_{CC} + 0.3V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}, V_{CCQ}
Com'l	0°C to +70°C	3.3V ± 0.3V
Mil	– 55°C to +125°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C1331–12 7C1332–12 Min.	7C1331–12 7C1332–12 Max.	7C1331–16 7C1332–16 Min.	7C1331–16 7C1332–16 Max.	7C1331–19 7C1332–19 Min.	7C1331–19 7C1332–19 Min.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Ciruit Current[5]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX}=1/t_{RC}	Com'l		180		160		150	mA
			Mil						170	

Notes:

2. Minimum voltage equals – 2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

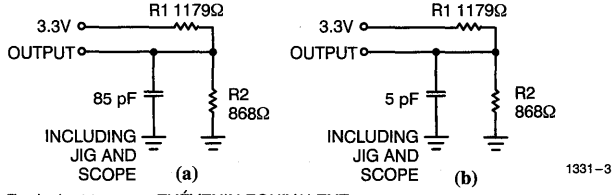
Electrical Charaterictics (continued)

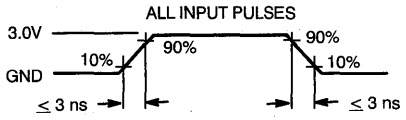
Parameter	Description	Test Conditions		7C1331–12 7C1332–12 Min.	7C1331–12 7C1332–12 Max.	7C1331–16 7C1332–16 Min.	7C1331–16 7C1332–16 Max.	7C1331–19 7C1332–19 Min.	7C1331–19 7C1332–19 Min.	Unit
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		30		30		30	mA
			Mil						30	
I_{SB2}	Automatic CE Power-Down Current –CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ –0.3V, $V_{IN} \geq V_{CC}$ –0.3V or $V_{IN} \leq$ 0.3V, f=0 [6]	Com'l		10		10		10	mA
			Mil						10	

Capacitance[7]

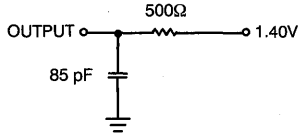
Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	Com'l	4	pF
			Mil	6	
C_{IN}: Other Inputs	Input Capacitance		Com'l	6	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	6	pF
			Mil	8	

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:

6. Clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[8]

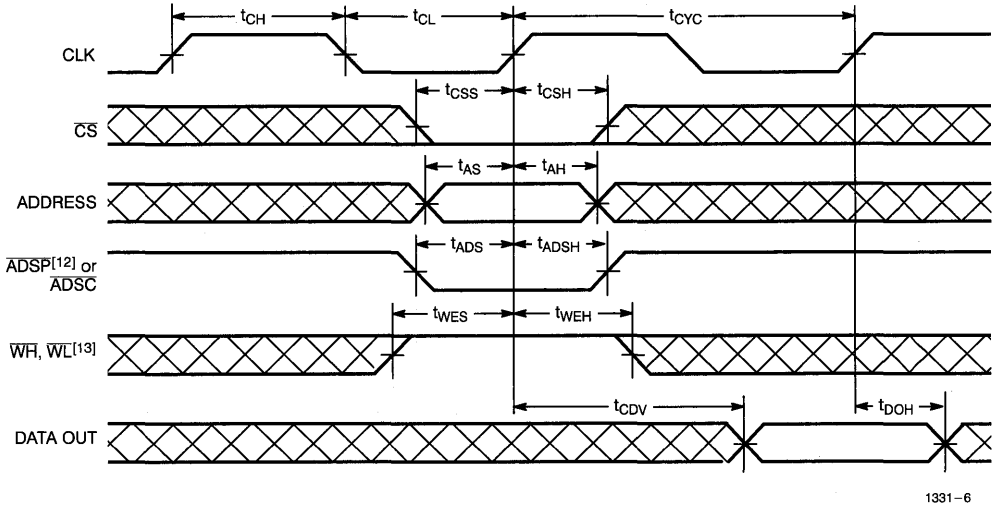
Parameter	Description	7C1331–12 7C1331–12		7C1331–16 7C1331–16		7C1331–19 7C1332–19		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20		25		30		ns
t_{CH}	Clock HIGH	8		9		12		ns
t_{CL}	Clock LOW	8		9		12		ns
t_{AS}	Address Set-Up Before CLK Rise	3		4		5		ns
t_{AH}	Address Hold After CLK Rise	1		2		3		ns
t_{CDV1}	Data Output Valid After CLK Rise, 0-pF Load		12.5		16.5		19.5	
t_{CDV2}	Data Output Valid After CLK Rise		14		18		21	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	1		2		3		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	3		4		5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	1		2		3		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	1		2		3		ns
t_{DS}	Data Input Set-Up Before CLK Rise	3		4		5		ns
t_{DH}	Data Input Hold After CLK Rise	1		2		3		ns
t_{CSS}	Chip Select Set-Up	3		4		5		ns
t_{CSH}	Chip Select Hold After CLK Rise	1		2		3		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[9]	2	7	2	8	2	11	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[9]	2	7	2	8	2	11	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		6		7		8	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[9,10]		7		8		11	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[10]		14		18		21	ns

Notes:

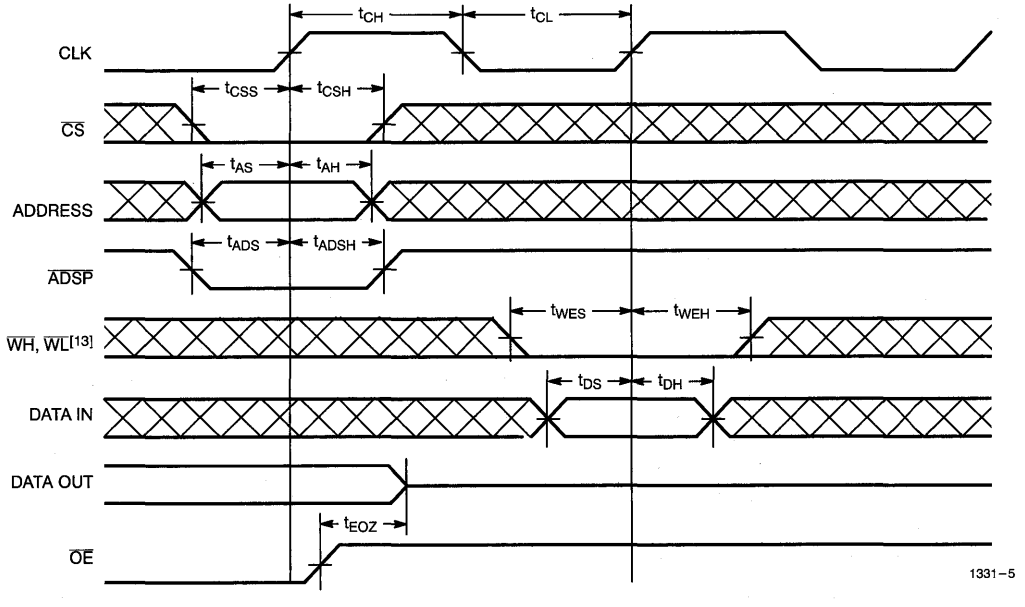
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[11]



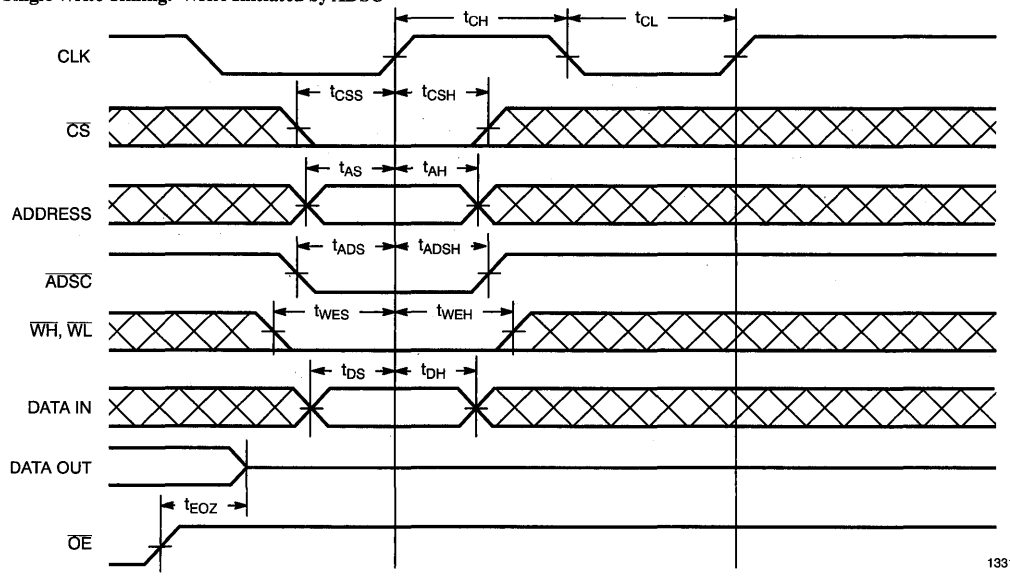
Single Write Timing: Write Initiated by $\overline{ADSP}$



Notes:
11. $\overline{OE}$ is LOW throughout.
12. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
13. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WH}$, and $\overline{WL}$ if $\overline{CS}$ is HIGH.

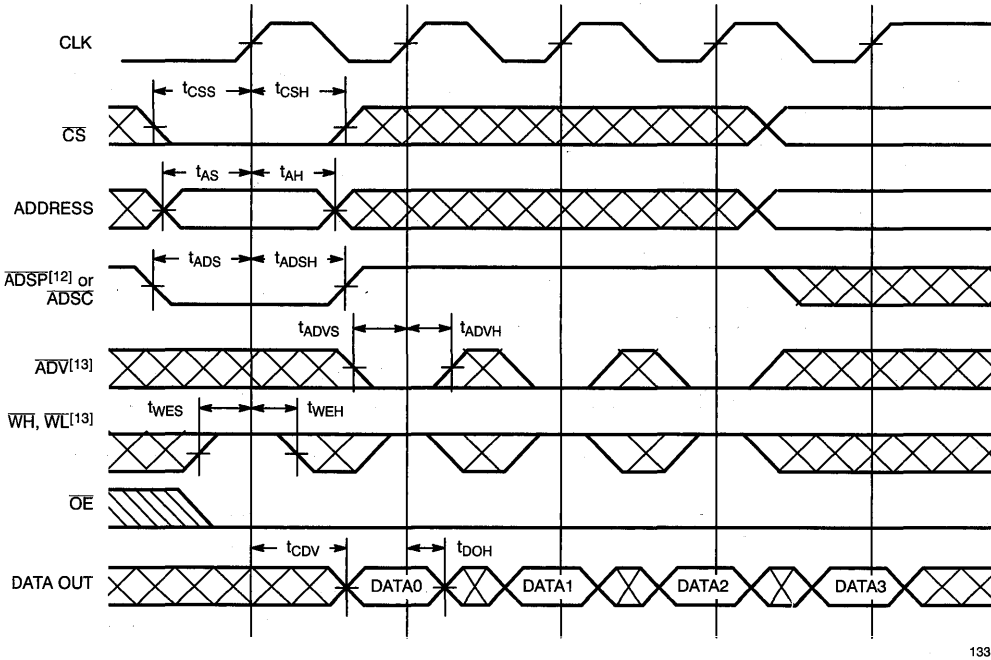
Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$



1331–7

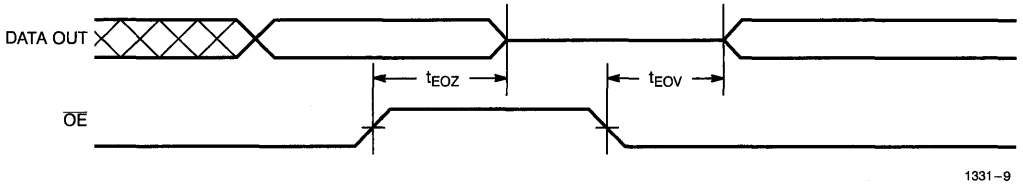
Burst Read Sequence with Four Accesses



1331–8

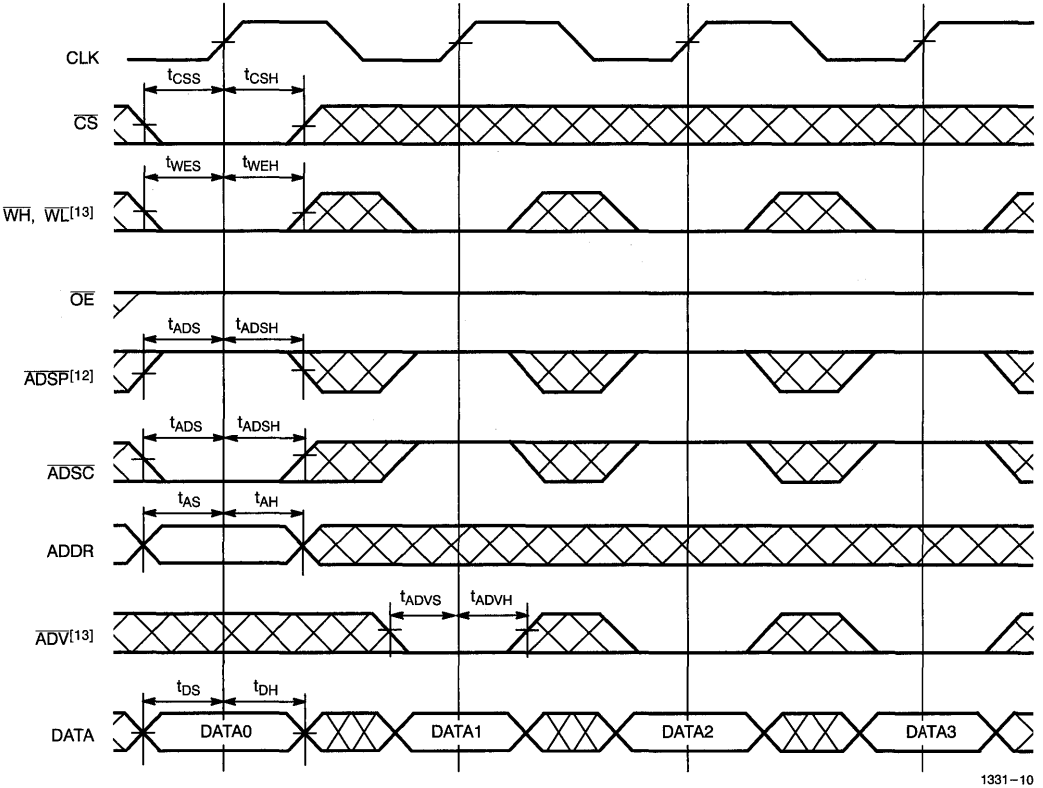
Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)



1331–9

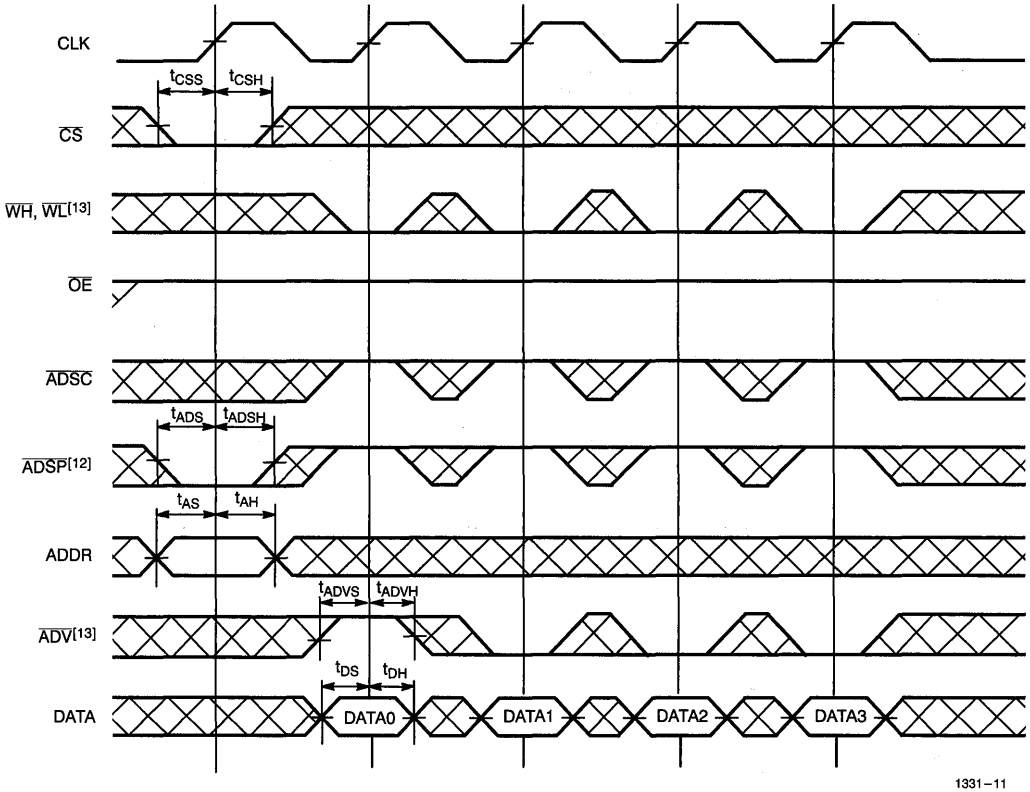
Write Burst Timing: Write Initiated by $\overline{ADSC}$



1331–10

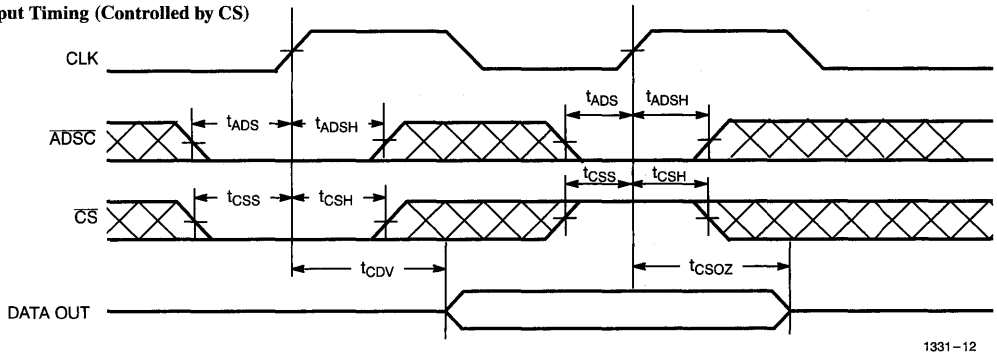
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$



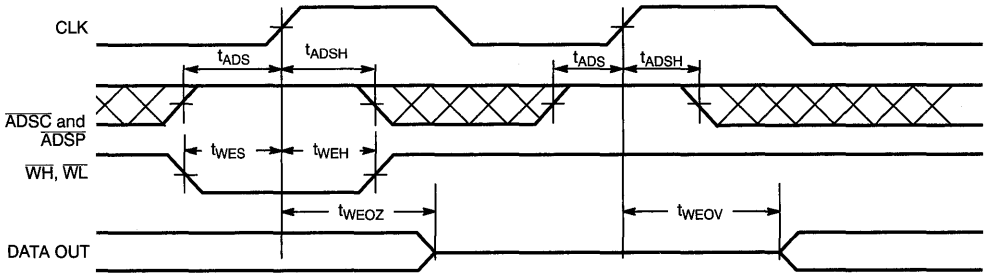
Switching Waveforms (continued)

Output Timing (Controlled by CS)



1331–12

Output Timing (Controlled by $\overline{WH}/\overline{WL}$)



1331–13

Truth Table

Inputs						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, begin burst
X	H	H	L	H	L→H	Incremented burst address	Read cycle, begin burst
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1331–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–12NC	TBD	52-Lead Plastic Quad Flatpack	
16	CY7C1331–16JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–16NC	TBD	52-Lead Plastic Quad Flatpack	
19	CY7C1331–19JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–16NC	TBD	52-Lead Plastic Quad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1332–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–12NC	TBD	52-Lead Plastic Quad Flatpack	
16	CY7C1332–16JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–16NC	TBD	52-Lead Plastic Quad Flatpack	
19	CY7C1332–19JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–19NC	TBD	52-Lead Plastic Quad Flatpack	

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CY7C1378
CY7C1379

CYPRESS SEMICONDUCTOR

32K x 18 Synchronous Cache 3.3V RAM

Features

- **Supports 50-MHz Pentium™ processor cache systems with zero wait states**
- **32K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 12.5 ns with 0-pF load**
  - **— 14 ns with 85-pF load**
- **Two-bit wraparound counter supporting the Pentium™ and 486 burst sequence (7C1378)**
- **Two-bit wraparound counter supporting the linear burst sequence (7C1379)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **Industry-standard pinout**
- **52-pin PLCC and PQFP packaging**

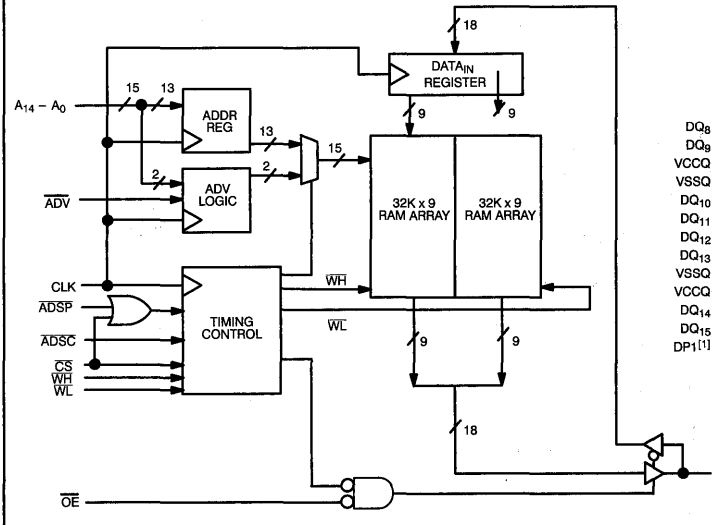
Functional Description

The CY7C1378 and CY7C1379 are 3.3V 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 12.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

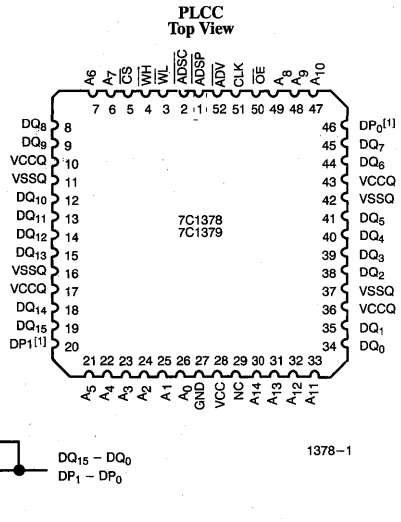
The CY7C1378 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1379 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1378–12 7C1379–12	7C1378–16 7C1379–16	7C1378–19 7C1379–19
Maximum Access Time (ns) (0-pF Load)		12.5	16.5	19.5
Maximum Operating Current (mA)	Commercial	180	160	150
	Military			170

Pentium is a trademark of Intel Corporation.

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_x.

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION **CY7C1388**

3.3V 32K x 9 Static RAM

Features

- **Single 3.3 ± 0.3V power supply**
- **High speed**
  - **— 20 ns**
- **Low active power**
  - **— 235 mW**
- **Low standby power**
  - **— 90 mW**
- **2.0V data retention**
  - **— 100 μW**
- **Ideal for low-voltage cache memory applications**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **CMOS for optimum speed/power**
- **Automatic power-down when deselected**

Functional Description

The CY7C1388 is a high-performance 3.3V CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 60% when deselected.

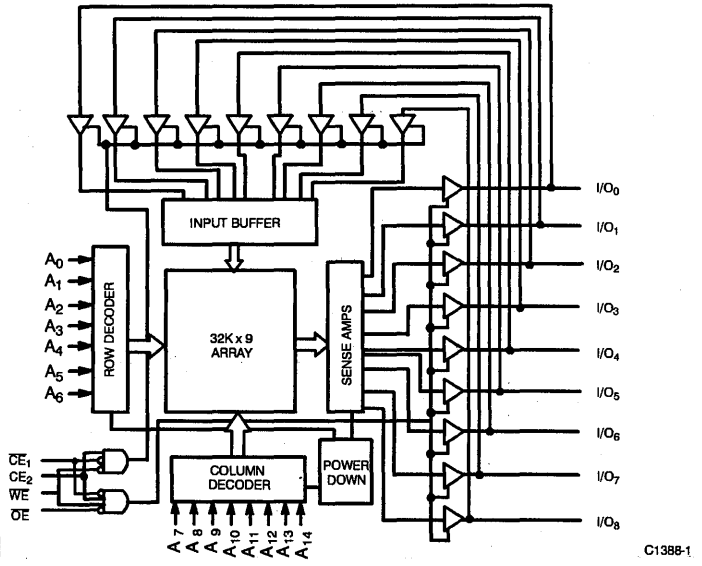
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the nine I/O pins (I/O_0 through I/O_8) is then written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins (I/O_0 through I/O_8) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

THe CY7C1388 is available in standard 300-mil-wide DIPs and SOJs. A die coat is used to ensure alpha immunity.

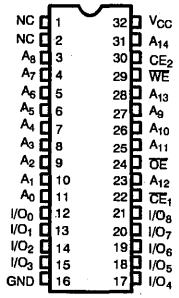
Logic Block Diagram



C1388-1

Pin Configuration

DIP/SOJ
Top View



C1388-2

Selection Guide

	7C1388–20	7C1388–25	7C1388–35
Maximum Access Time (ns)	20	25	35
Maximum Operating Current (mA)	65	60	55
Maximum Standby Current (mA)	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} to Relative GND ... − 0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.3V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	7C1388−20		7C1388−25		7C1388−35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[1]		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	−2	+2	−2	+2	−2	+2	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC}=Max., V_{OUT}=GND		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, $f=f_{MAX}=1/t_{RC}$		65		60		55	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		25		25		25	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ −0.3V or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq 0.3V$, f=0		500		500		500	µA

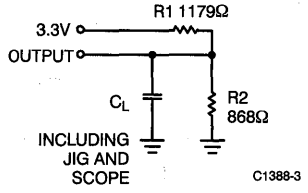
Capacitance[4]

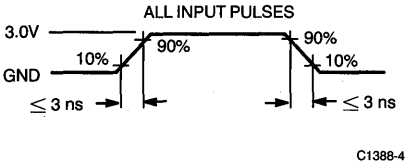
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
C_{IN}: Controls			8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

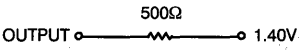
1. Minimum voltage is equal to −2.0 for pulse durations of less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[5, 6]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 5]

Parameter	Description	7C1388–20		7C1388–25		7C1388–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE_1}$ LOW or CE_2 HIGH to Data Valid		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		9		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		7		7		7	ns
t_{LZCE}	$\overline{CE_1}$ LOW or CE_2 HIGH to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE_1}$ HIGH or CE_2 LOW to High Z[6, 7]		8		8		8	ns
t_{PU}	$\overline{CE_1}$ LOW or CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE_1}$ HIGH or CE_2 LOW to Power-Down		20		25		35	ns
WRITE CYCLE[8, 9]								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCE}	$\overline{CE_1}$ LOW or CE_2 HIGH to Write End	12		15		20		ns
t_{AW}	Address Set-Up to Write End	12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		20		ns
t_{SD}	Data Set-Up to Write End	10		11		12		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns

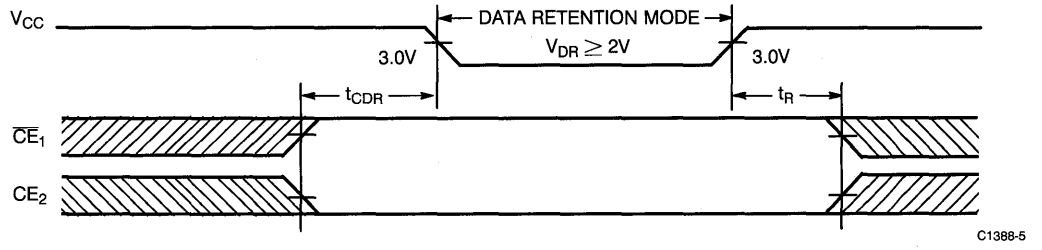
Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance C_L = 30 pF.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

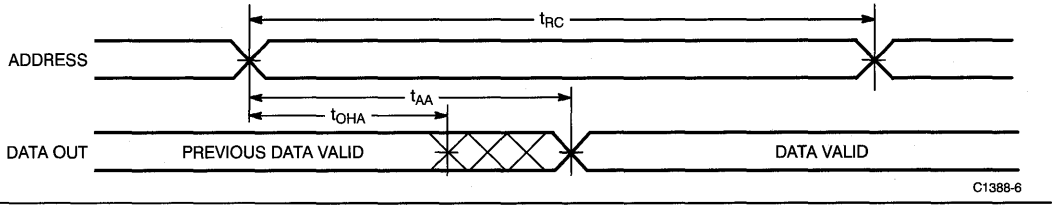
Parameter	Description	Conditions[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC}=V_{DR}=2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50	μA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[4]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

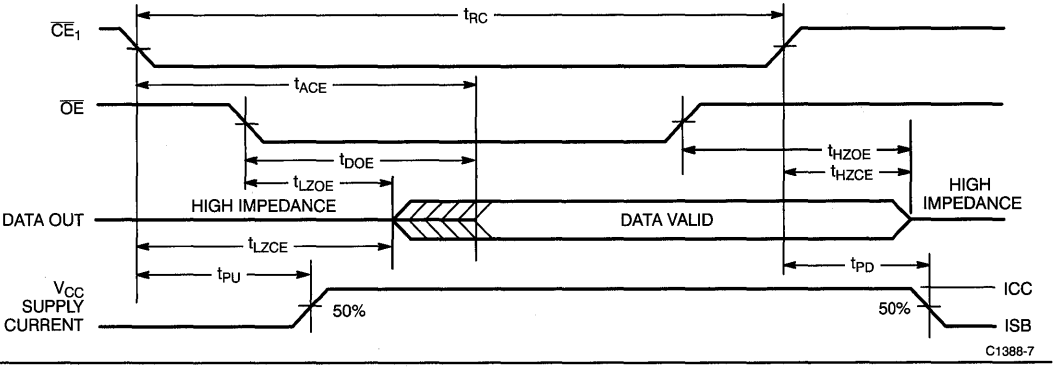


Switching Waveforms

Read Cycle No. 1[11, 12]



Read Cycle No. 2 (Chip Enable Controlled)[12, 13, 14]

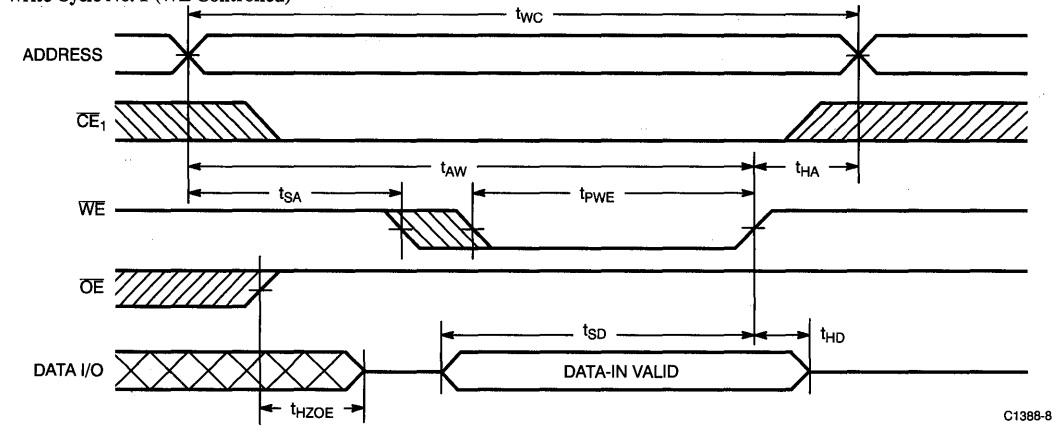


Notes:

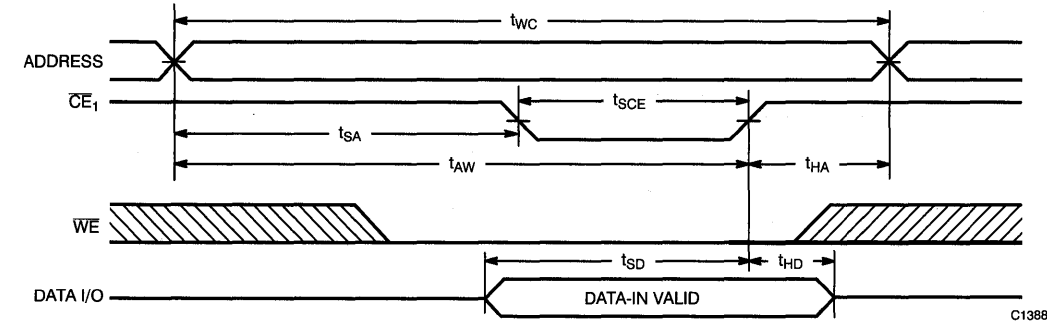
10. No input may exceed V_{CC} +0.3V.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Timing parameters are the same for all chip-enable signals ($\overline{CE_1}$ and CE_2). Only the timing for $\overline{CE_1}$ is shown.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

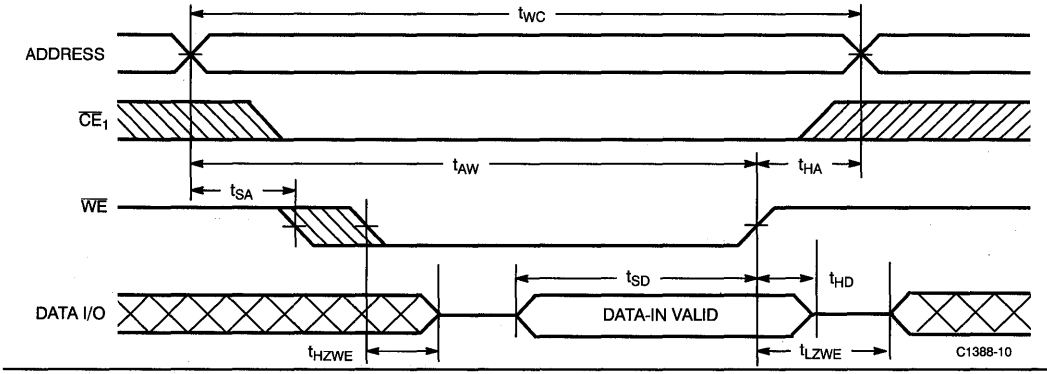
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 13, 15, 16]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 16]



Notes:

15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C1388–20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1388–20VC	V32	32-Lead (300-Mil) Molded SOJ	
25	CY7C1388–25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1388–25VC	V32	32-Lead (300-Mil) Molded SOJ	
35	CY7C1388–35PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1388–35VC	V32	32-Lead (300-Mil) Molded SOJ	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00221–A

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C1399**

3.3V 32K x 8 Static RAM

Features

- **Single 3.3 ± 0.3V power supply**
- **High speed**
  - **— 15 ns**
- **Low active power**
  - **— 255 mW**
- **Low standby power**
  - **— 90 mW**
- **2.0V data retention**
  - **— 100 μW**
- **Ideal for low-voltage cache memory applications**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **CMOS for optimum speed/power**
- **Automatic power-down when deselected**

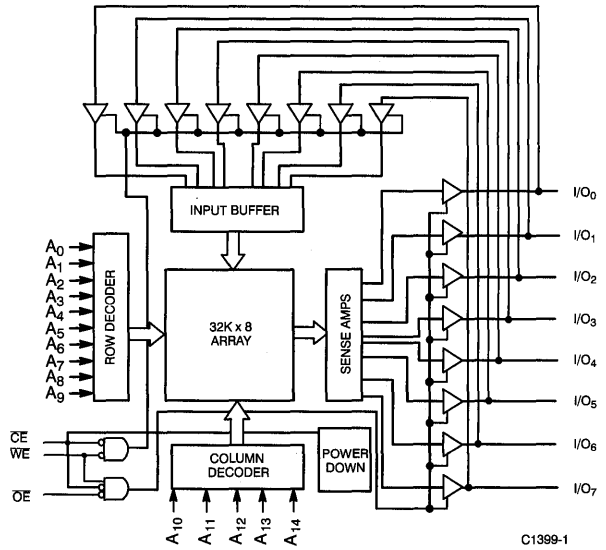
Functional Description

The CY7C1399 is a high-performance 3.3V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 60% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. The CY7C1399 is available in standard 300-mil-wide DIP and SOJ packages. A die coat is used to ensure alpha immunity.

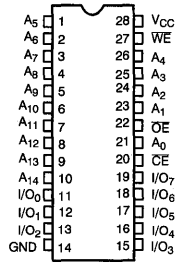
Logic Block Diagram



C1399-1

Pin Configuration

DIP/SOJ
Top View



C1399-2

Selection Guide

	7C1399–15	7C1399–20	7C1399–25	7C1399–35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	70	65	60	55
Maximum Standby Current (mA)	25	25	25	25

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] . − 0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to V_{CC} + 0.3V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3 ± 0.3V

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	7C1399−15		7C1399−20		7C1399−25		7C1399−35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current		− 1	+1	− 1	+1	− 1	+1	− 1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	− 5	+5	− 5	+5	− 5	+5	− 5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		− 300		− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		70		65		60		55	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$, or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$, or $V_{IN} \leq V_{IL}$, f = f_{MAX}		25		25		25		25	mA
I_{SB2}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$, 0.3V or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq$ 0.3V, f=0		500		500		500		500	µA

Shaded area contains advanced information.

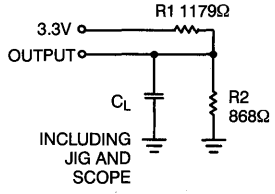
Capacitance[4]

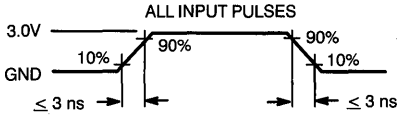
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
C_{IN}: Controls			8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

1. Minimum voltage is equal to − 2.0V for pulse durations of less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

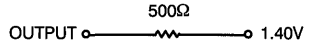
AC Test Loads and Waveforms





C1399-3

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 5]

Parameter	Description	7C1399–15		7C1399–20		7C1399–25		7C1399–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		9		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		7		7		7		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		8		8		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		25		35	ns
WRITE CYCLE[8, 9]										
t_{WC}	Write Cycle Time	15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	9		10		11		12		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		8		8		8		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns

Shaded area contains advanced information.

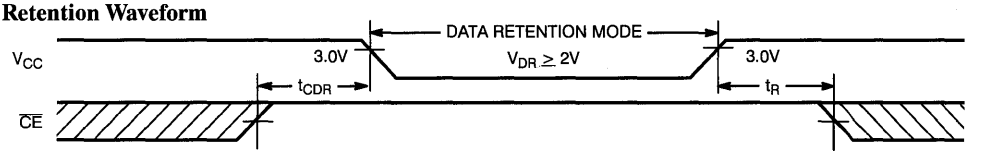
Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[4]	Operation Recovery Time		t_{RC}		ns

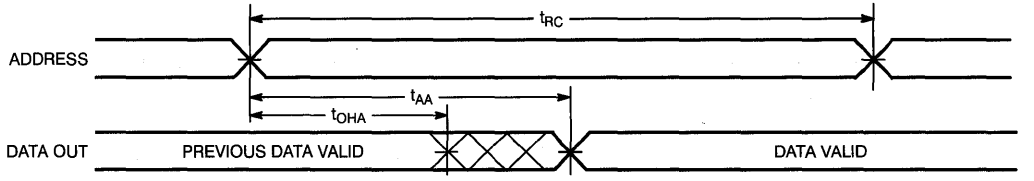
Data Retention Waveform



C1399-4

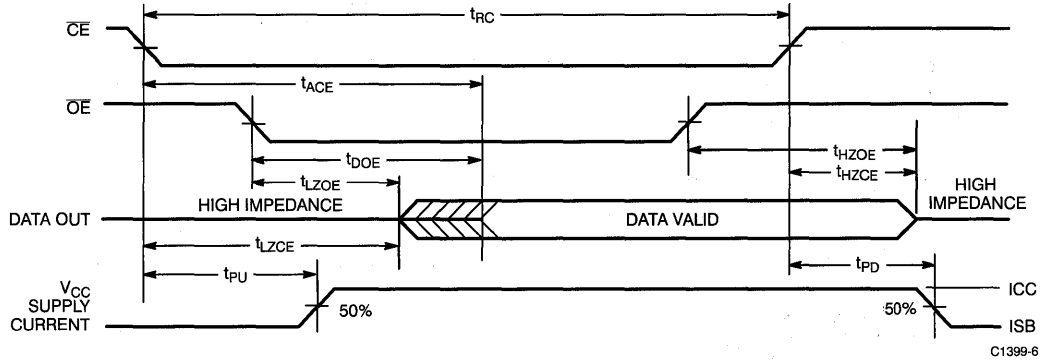
Switching Waveforms

Read Cycle No. 1[11, 12]



C1399-5

Read Cycle No. 2[12, 13]

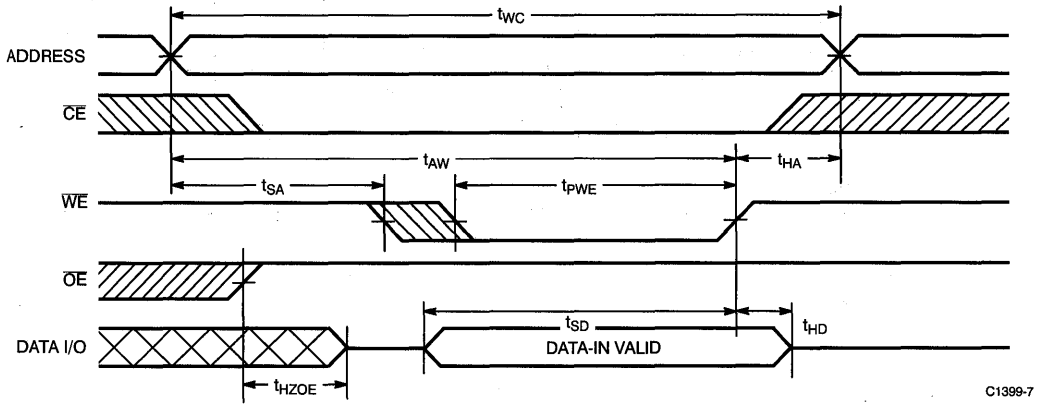


C1399-6

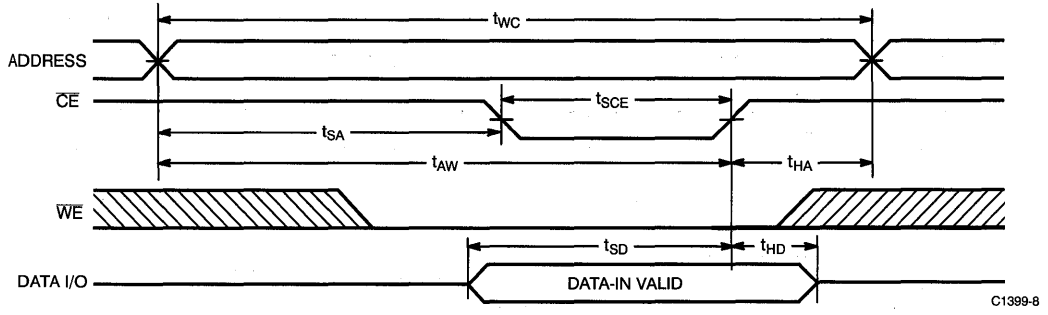
Notes:
10. No input may exceed V_{CC} + 0.3V.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

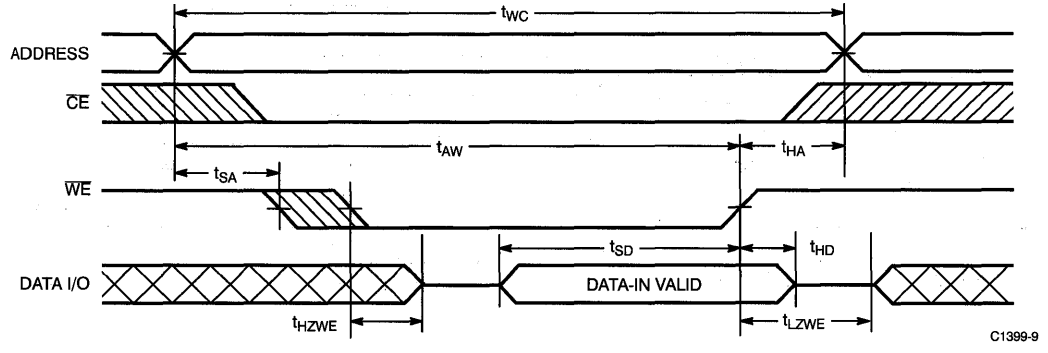
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 14, 15]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 14, 15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 15]



Notes:

14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C1399–15PC	P21	Commercial
	CY7C1399–15VC	V21	
20	CY7C1399–20PC	P21	Commercial
	CY7C1399–20VC	V21	
25	CY7C1399–25PC	P21	Commercial
	CY7C1399–25VC	V21	
35	CY7C1399–35PC	P21	Commercial
	CY7C1399–35VC	V21	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00222–B

CYPRESS SEMICONDUCTOR

Section Contents

PROMs (Programmable Read Only Memory)

Introduction to CMOS PROMs

Product Line Overview

The Cypress CMOS family of high-performance byte-wide and word-wide (x16) PROMs spans 4-kilobit to 512-kilobit densities and three functional configurations. Products are typically available as EPROMs (Erasable, Programmable ROMs) in 300- and 600-mil windowed cerDIP packages, leadless chip carriers (LCCs), leaded chip carriers (CLCC, PLCC) and flatpacks. They are also available as PROMs in similarly configured plastic and opaque hermetic packages. With the exception of the 4K PROMs (registered only), all densities are available in both registered and non-registered versions. The registered devices operate in either synchronous or asynchronous modes and may have an INITIALIZATION feature to preload the pipeline register, which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at or above the speed level of their bipolar counterparts with the advantage of lower power consumption inherent in CMOS technology. They operate with 10% power supply tolerances and can withstand 2000 volts of electrostatic discharge.

Technology Introduction

Cypress PROMs are executed in N-well CMOS EPROM processes that provide basic gate delays of 235 picoseconds for a fan-out of one with a power consumption of 45 femto-joules. These processes provide the basis for the development of Cypress LSI products, which outperform the fastest bipolar equivalents.

Historically, CMOS static RAMs have challenged bipolar RAMs for speed, while CMOS PROMs have been slower than the fused bipolar devices because (1) the typical single transistor CMOS cell is slow compared to any "fuse," and (2) CMOS technologies were optimized for programmability and density at the expense of speed. Innovative Cypress EPROM technology overcomes both of these historical limitations. A substrate bias generator is employed in an EPROM technology to improve performance and raise latch-up immunity to greater than 200 mA. The result is a CMOS EPROM technology that outperforms bipolar fuse technology for both density and speed, particularly at higher densities. Limitations of devices implemented in the bipolar fuse technology such as programming yield, power dissipation and higher-density performance are eliminated or greatly reduced using Cypress CMOS EPROM technology.

Programming

Differential Memory Cells

Cypress PROMs are programmed a byte at a time by applying V_{PP} ($\sim$12V) to the programming pin and the desired logic levels to input pins. Both logic 1 and logic 0 are programmed into the differential cell. A bit is programmed by applying V_{PP} on the control gate and 9 volts on the drain of the floating-gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate, thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts, resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is the corrected logic state. Because an unprogrammed cell has neither a 1 nor a 0 in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference, which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual bits allowing the monitoring of the quality of programming during the manufacturing operation.

Single-Ended Memory Cells

The programming mechanism of the EPROM transistor in a single-ended memory cell is the same as its counterpart in a double-ended memory cell. The difference is that only 1s are programmed in a single-ended cell. A 1 applied to the I/O pin during programming causes an erased EPROM transistor to be programmed, while a 0 allows the EPROM transistor to remain unprogrammed.

Erasability

This is available for devices in windowed packages, both registered and non-registered. Wavelengths of light less than 4000 Angstroms begin to erase Cypress PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mV/cm^2 power rating, the exposure time would be approximately 35 minutes.

The PROM needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. The recommended maximum dosage is 7258 Wsec/cm^2.

Some devices are sensitive to photo-electric effects during programming. Cypress recommends covering the windows of reprogrammable devices during programming.

Reliability

The CMOS EPROM approach to PROMs has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed an erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each CMOS PROM contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged, thus assuring the user that not only will every cell program, but that the product performs to the specification.

General Testing Information

Incoming test procedures on these devices should be carefully planned, taking into account the high-performance and output drive capabilities of the parts. The following notes may be useful:

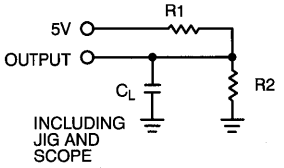
- Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
- All device test loads should be located within 2″ of device outputs.
- Do not leave any inputs disconnected (floating) during any tests.
- Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capaci-

tances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

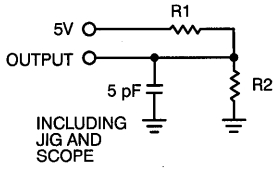
- V_{OH} and V_{OL} are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- Capacitance is tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the Cypress PROM Products are insensitive to − 3V dc input levels and − 5V undershoot pulses of less than 10 ns (measured at 50%).

Switching Tests

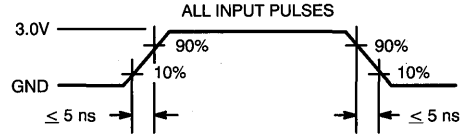
AC Test Loads and Waveforms



(a) Normal Load

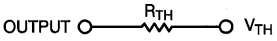


(b) High Z Load



INTRO-1 INTRO-2

Equivalent to: THÉVENIN EQUIVALENT



Load circuit (a) is used to test all switching characteristics except High Z parameters. Load circuit (b) is used to test High Z parameters. R1 is a resistor connected from the output to V_{CC} and R2 is connected between the output and ground for testing purposes.

Values of R1 and R2 are given in the individual datasheet for each product. Speed is measured at 1.5V reference levels except for delay to output High Z.

Document #: 38−00234

CYPRESS SEMICONDUCTOR

CY7C225

512 x 8 Registered PROM

Features

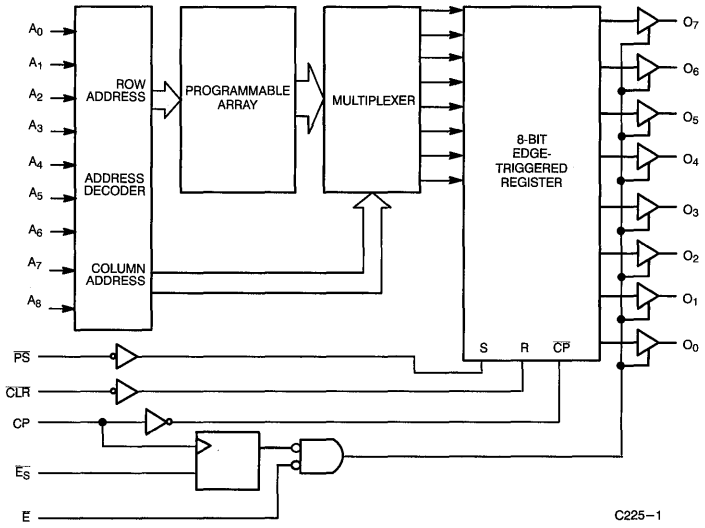
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 1500V static discharge**

Functional Description

The CY7C225 is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

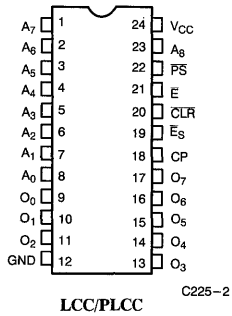
Logic Block Diagram



C225–1

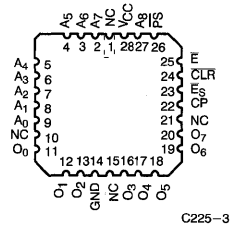
Pin Configurations

DIP
Top View



C225–2

LCC/PLCC
Top View



C225–3

Selection Guide

		7C225-25	7C225-30	7C225-35	7C225-40
Maximum Set-Up Time (ns)		25	30	35	40
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90		90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled[5]		– 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		– 20	– 90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.[7]	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			13	14	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

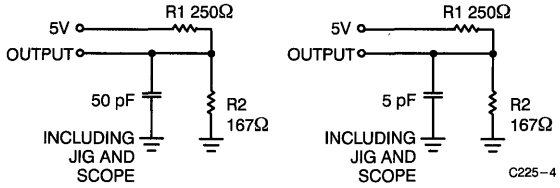
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

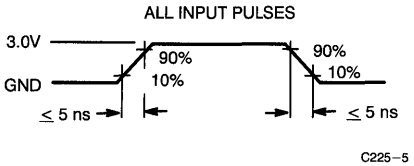
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Due to the design of the differential cell in this device, I_{CC} can only be accurately measured on a programmed array.

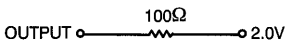
AC Test Loads and Waveforms[4]



(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

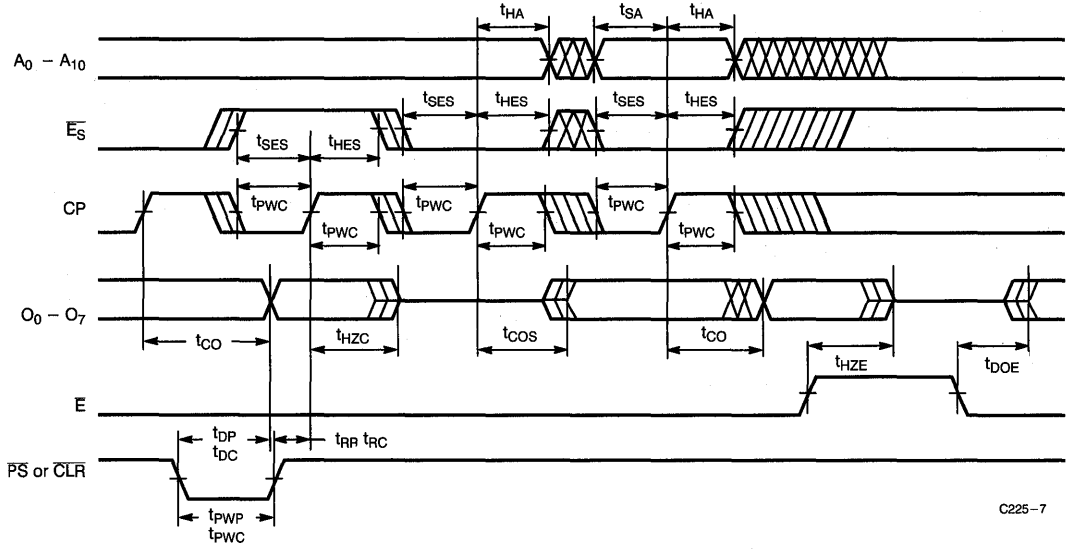
The CY7C225 has buffered asynchronous $\overline{CLEAR}$ and $\overline{PRESET}$ inputs. Applying a LOW to the $\overline{PRESET}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{CLEAR}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C225–25		7C225–30		7C225–35		7C225–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	10		10		10		10		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	0		5		5		5		ns
t_{DB} t_{DC}	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to Valid Output		20		20		20		20	ns
t_{RB} t_{RC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWB} t_{PWC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width	15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[8]		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[8]		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		20		20		25		30	ns

Switching Waveforms[4]



Note:
8. Applies only when the synchronous ($\overline{E}_S$) function is used.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[9]						
	Read or Output Disable	$A_8 - A_0$	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	$O_7 - O_0$
	Other	$A_8 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	$D_7 - D_0$
Read		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_8 - A_0$	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_8 - A_0$	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
Clear		$A_8 - A_0$	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
Preset		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Program Verify		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_8 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Blank Check Ones		$A_8 - A_0$	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	Ones
Blank Check Zeros		$A_8 - A_0$	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	Zeros

Note:
9. X = "don't care" but not to exceed V_{CC} ±5%.

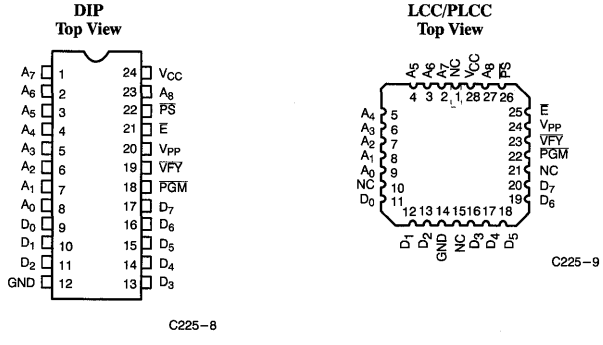
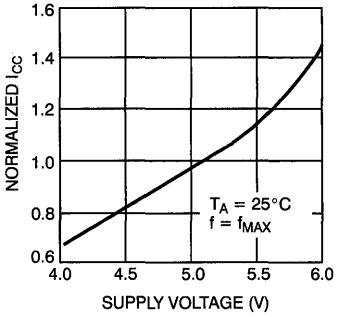


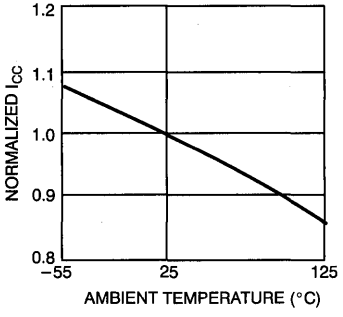
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

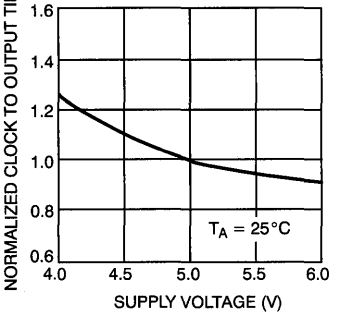
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



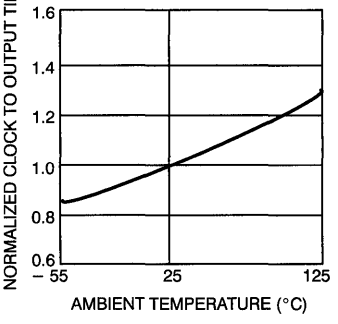
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



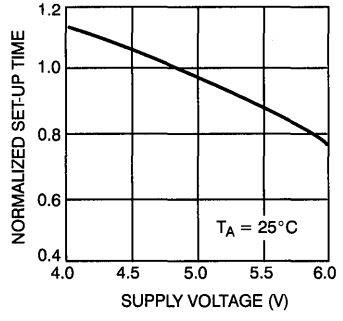
CLOCK TO OUTPUT TIME vs. V_{CC}



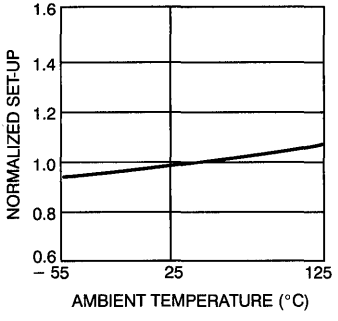
CLOCK TO OUTPUT TIME vs. TEMPERATURE



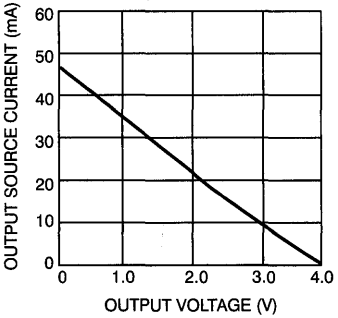
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



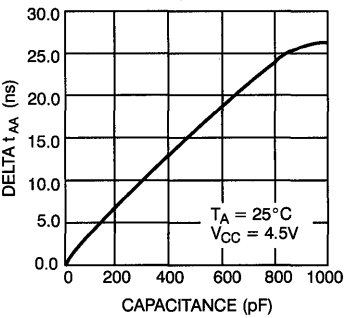
NORMALIZED SET-UP TIME vs. TEMPERATURE



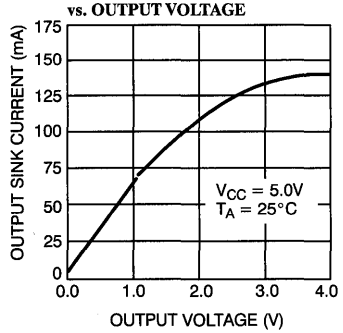
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C225–10

Ordering Information[10]

Speed (ns) t_{SA}	Speed (ns) t_{CO}	Ordering Code	Package Name	Package Type	Operating Range
25	12	CY7C225–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–25PC	P13	24-Lead (300-Mil) Molded DIP	
30	15	CY7C225–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DP}	7, 8, 9, 10, 11
t_{RP}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88518	01LX	CY7C225–30DMB
5962–88518	013X	CY7C225–30LMB
5962–88518	02LX	CY7C225–35DMB
5962–88518	023X	CY7C225–35LMB
5962–88518	03LX	CY7C225–40DMB
5962–88518	033X	CY7C225–40LMB

Document #: 38–00002–E

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C225A**

512 x 8 Registered PROM

Features

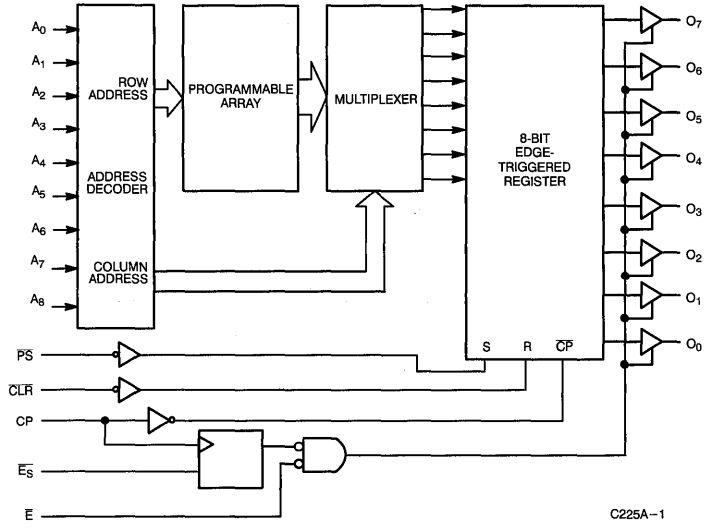
- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

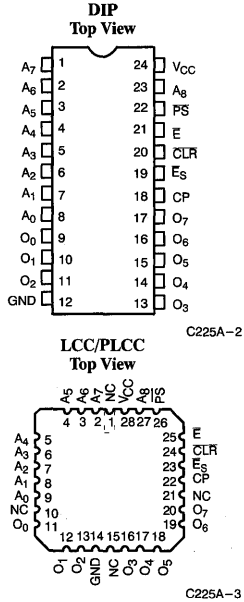
The CY7C225A is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225A replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C225A–18	7C225A–25	7C225A–30	7C225A–35	7C225A–40
Maximum Set-Up Time (ns)		18	25	30	35	40
Maximum Clock to Output (ns)		12	12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90	90		90
	Military		120	120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		– 10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		– 20	– 90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

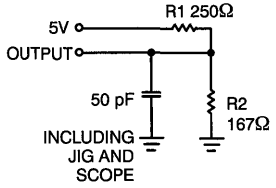
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

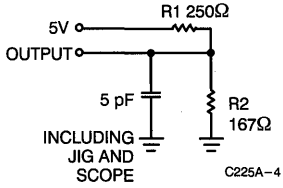
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[4]

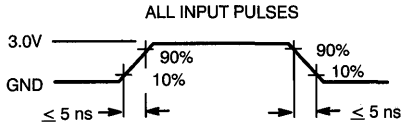


(a) Normal Load



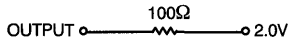
C225A–4

(b) High Z Load



C225A–5

Equivalent to: THÉVENIN EQUIVALENT



C225A–6

Operating Modes

The CY7C225A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

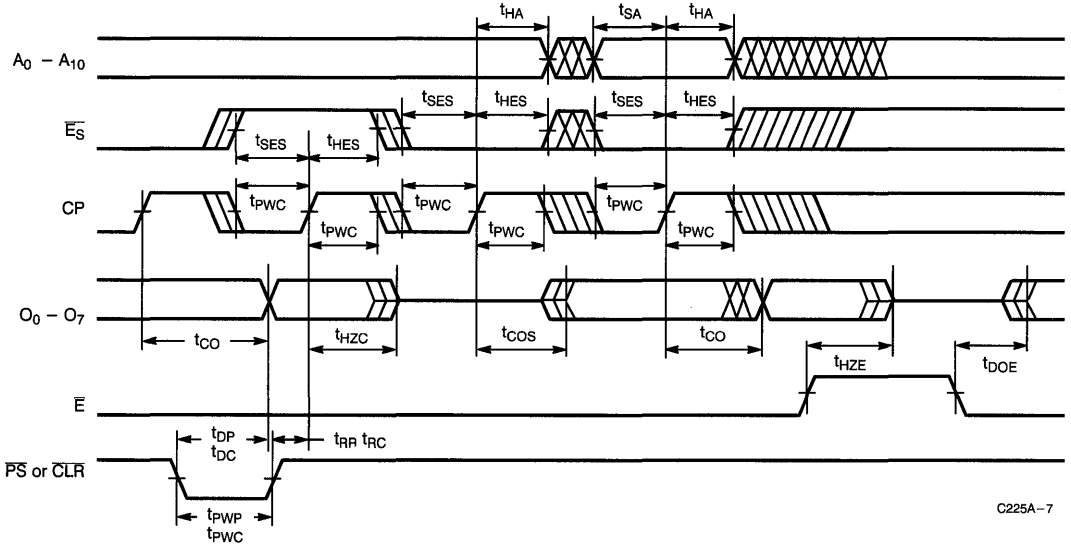
The CY7C225A has buffered asynchronous $\overline{CLEAR}$ and $\overline{PRESET}$ inputs. Applying a LOW to the $\overline{PRESET}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{CLEAR}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C225A–18		7C225A–25		7C225A–30		7C225A–35		7C225A–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		10		10		10		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	0		0		5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to Valid Output		20		20		20		20		20	ns
t_{RP}, t_{RC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery to Clock HIGH	15		15		20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width	15		15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25		30	ns

Switching Waveforms[4]



Note:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]						
	Read or Output Disable	$A_8 - A_0$	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	$O_7 - O_0$
	Other	$A_8 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	$D_7 - D_0$
Read		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_8 - A_0$	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_8 - A_0$	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
Clear		$A_8 - A_0$	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
Preset		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Program Verify		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_8 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Blank Check		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

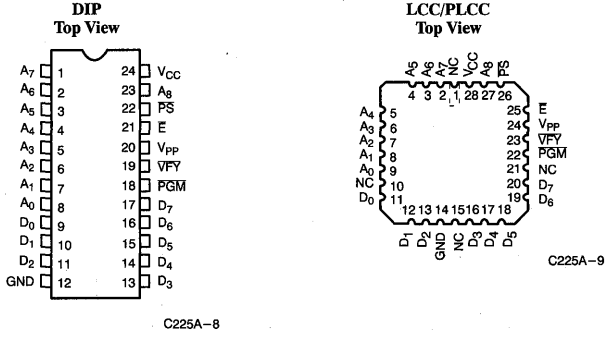
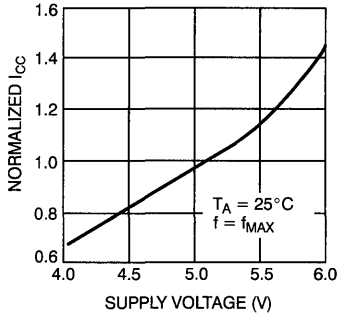


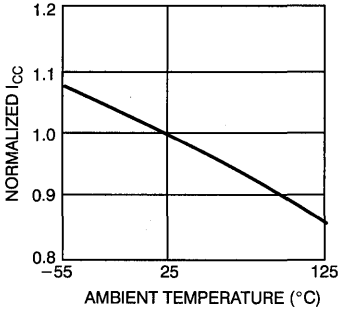
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

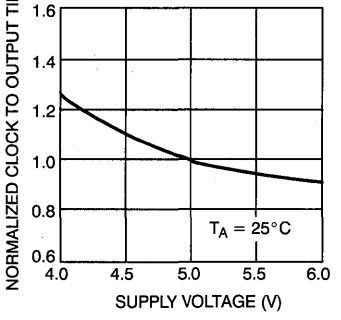
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



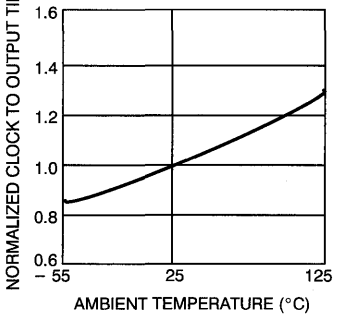
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



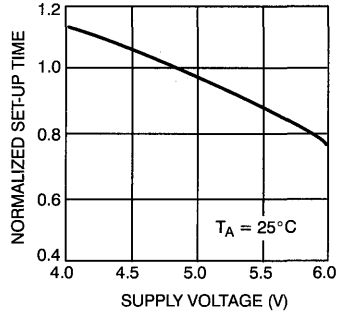
CLOCK TO OUTPUT TIME vs. V_{CC}



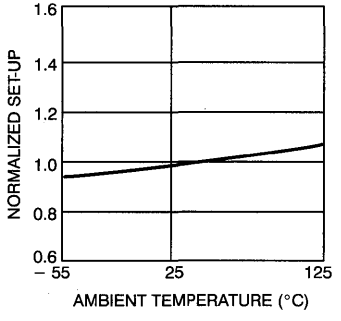
CLOCK TO OUTPUT TIME vs. TEMPERATURE



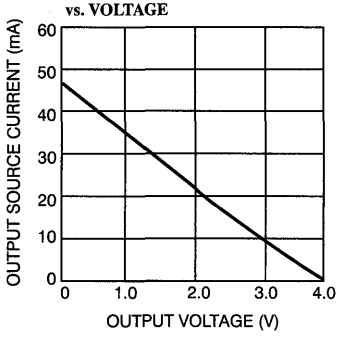
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



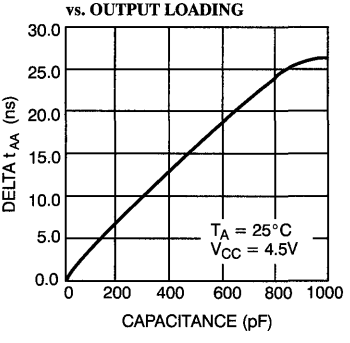
NORMALIZED SET-UP TIME vs. TEMPERATURE



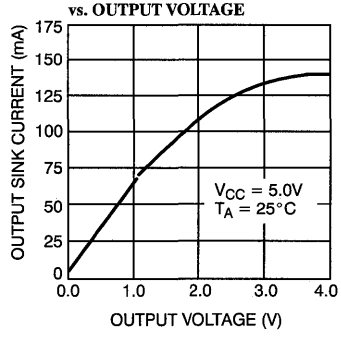
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C225A–10

Ordering Information[9]

Speed (ns)		Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}				
18	12	CY7C225A–18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C225A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C225A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225A–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DP}	7, 8, 9, 10, 11
t_{RP}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88518	01LX	CY7C225A–30DMB
5962–88518	013X	CY7C225A–30LMB
5962–88518	02LX	CY7C225A–35DMB
5962–88518	023X	CY7C225A–35LMB
5962–88518	03LX	CY7C225A–40DMB
5962–88518	033X	CY7C225A–40LMB

Document #: 38–00228–A

CY7C235

1K x 8 Registered PROM

Features

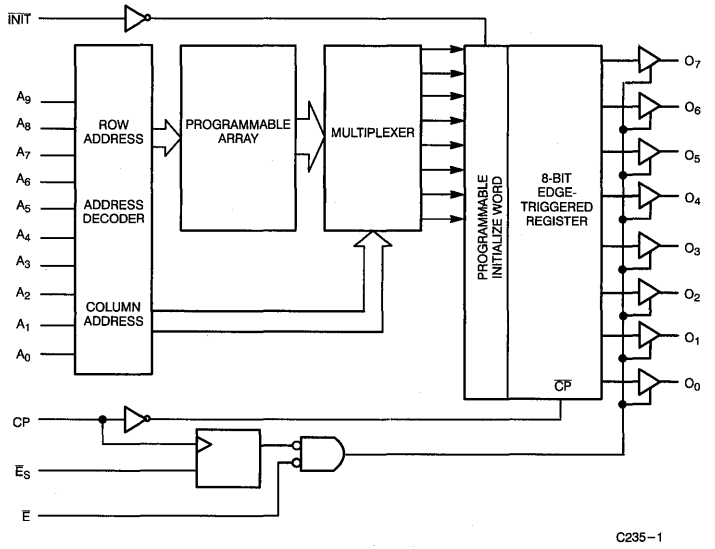
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous registers ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 1500V static discharge**

Functional Description

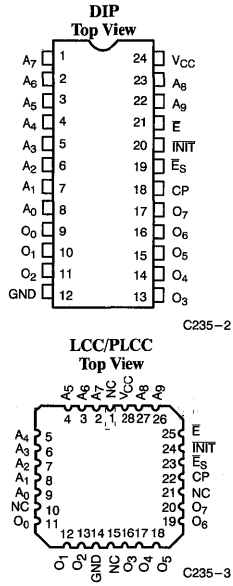
The CY7C235 is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 13.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C235–25	7C235–30	7C235–40
Maximum Set-Up Time (ns)		25	30	40
Maximum Clock to Output (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20 for DIP) 14.0V

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[5]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	mA
I_{CC}	Power Supply Current[7]	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			13	14	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

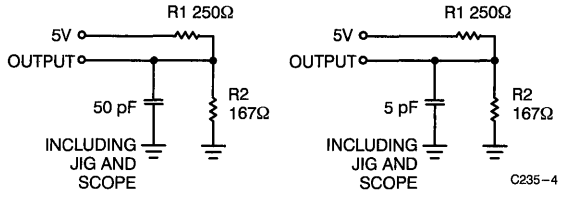
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} =5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

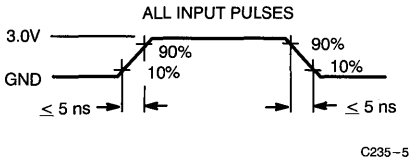
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Due to the design of the differential cell in this device, I_{CC} can only be accurately measured on a programmed array.

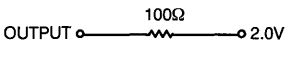
AC Test Loads and Waveforms[5]



(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C235 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{INIT}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

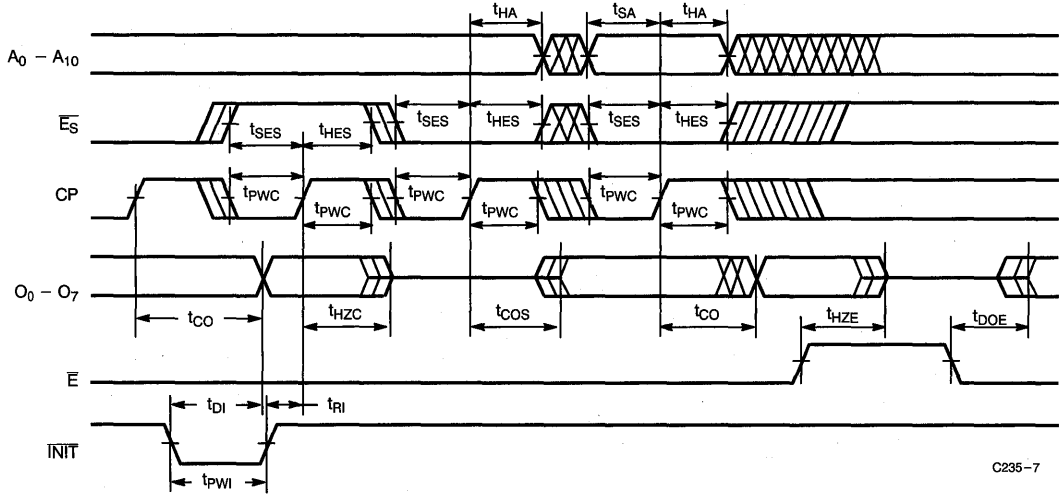
When the asynchronous initialize input, $\overline{INIT}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Characteristics Over Operating Range[3, 5]

Parameter	Description	7C235–25		7C235–30		7C235–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		25		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	20		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH[8]		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[8]		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		20		20		25	ns

Note:
8. Applies only when the synchronous ($\overline{E}_S$) function is used.

Switching Waveforms[5]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[9]							
	Read or Output Disable	$A_0, A_3 - A_9$	A_1	A_2	CP	$\overline{E}_S$	$\overline{E}$	$\overline{INIT}$	$O_7 - O_0$
	Other	$A_0, A_3 - A_9$	A_1	A_2	$\overline{PGM}$	$\overline{VFY}$	$\overline{E}$	V_{PP}	$D_7 - D_0$
Read		$A_0, A_3 - A_9$	A_1	A_2	X	V_{IL}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_0, A_3 - A_9$	A_1	A_2	X	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_0, A_3 - A_9$	A_1	A_2	X	X	V_{IH}	V_{IH}	High Z
Initialize		$A_0, A_3 - A_9$	A_1	A_2	X	X	V_{IL}	V_{IL}	Init Byte
Program		$A_0, A_3 - A_9$	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_0, A_3 - A_9$	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_0, A_3 - A_9$	A_1	A_2	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_0, A_3 - A_9$	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize Byte		$A_0, A_3 - A_9$	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check Ones		$A_0, A_3 - A_9$	A_1	A_2	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		$A_0, A_3 - A_9$	A_1	A_2	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	Zeros

Note:
9. X = "don't care" but not to exceed V_{CC} ±5%.

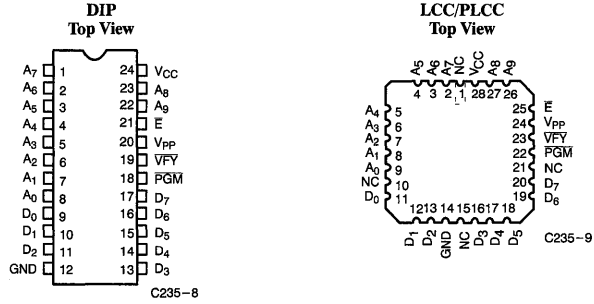
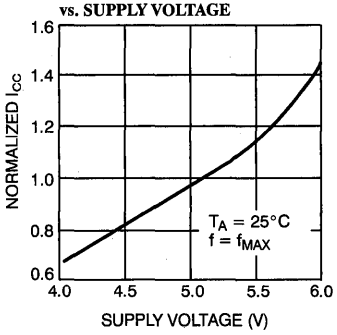


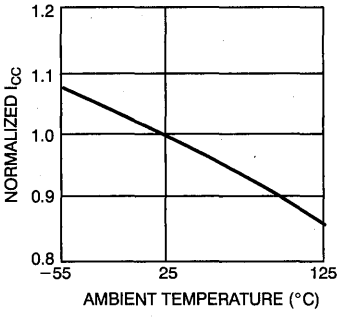
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

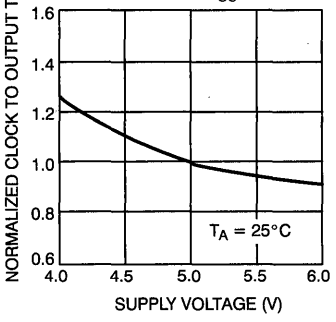
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



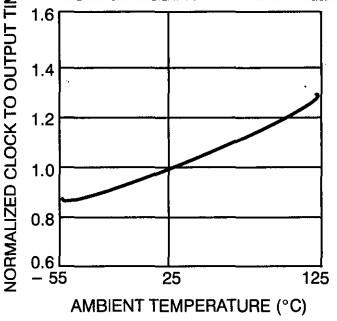
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



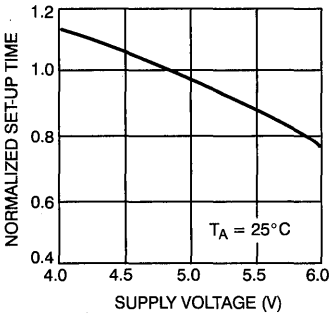
NORMALIZED CLOCK TO OUTPUT TIME vs. V_{CC}



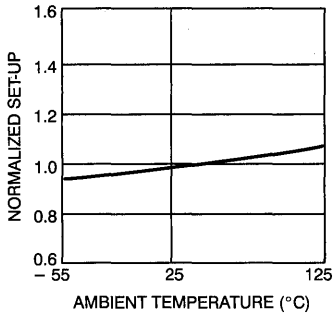
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



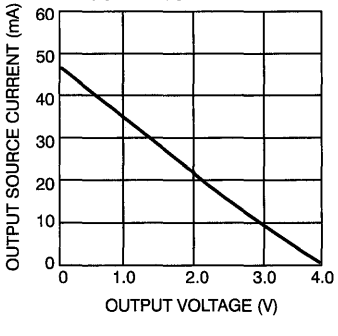
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



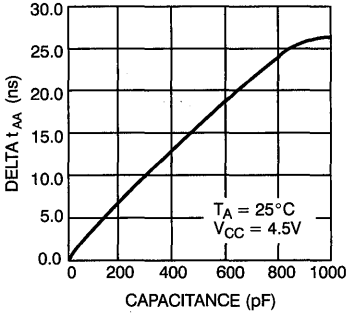
NORMALIZED SET-UP TIME vs. TEMPERATURE



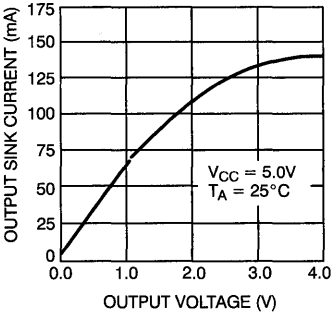
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C235–10

Ordering Information[10]

Speed (ns)		Ordering Code	Package Name	Package Type	Operating Range
t_{SA}	t_{CO}				
25	12	CY7C235–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235–25PC	P13	24-Lead (300-Mil) Molded DIP	
30	15	CY7C235–30DC	D14	24-Lead (300-Mil) CerDIP	
		CY7C235–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235–30KMB	K73	24-Lead Rectangular Cerpack	
		CY7C235–30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235–40KMB	K73	24-Lead Rectangular Cerpack	
		CY7C235–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88636	01KX	CY7C235–40KMB
5962–88636	01LX	CY7C235–40DMB
5962–88636	013X	CY7C235–40LMB
5962–88636	02KX	CY7C235–30KMB
5962–88636	02LX	CY7C235–30DMB
5962–88636	023X	CY7C235–30LMB

Document #: 38–00003–E

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C235A**

1K x 8 Registered PROM

Features

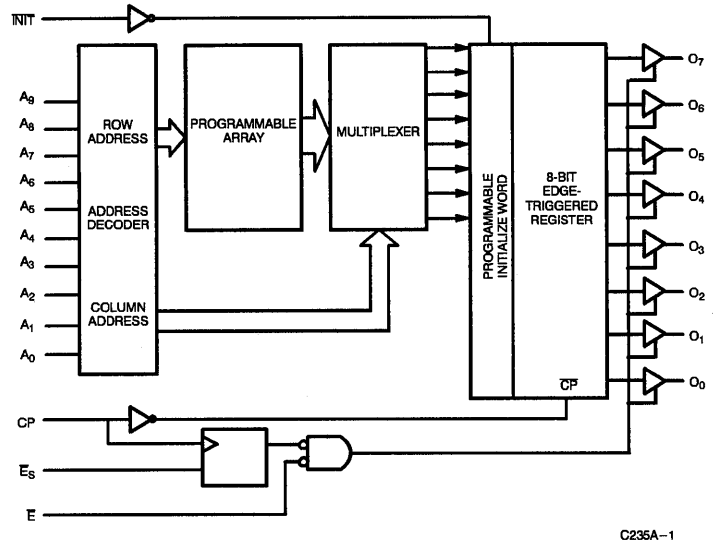
- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous registers ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C235A is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235A replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.

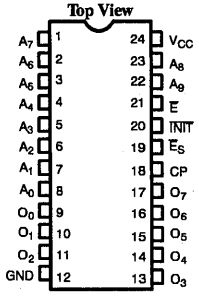
Logic Block Diagram



C235A–1

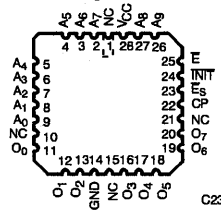
Pin Configurations

DIP
Top View



C235A–2

LCC/PLCC
Top View



C235A–3

Selection Guide

		7C235A–18	7C235A–25	7C235A–30	7C235A–40
Maximum Set-Up Time (ns)		18	25	30	40
Maximum Clock to Output (ns)		12	12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90	90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20 for DIP) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled[4]		−10	+10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

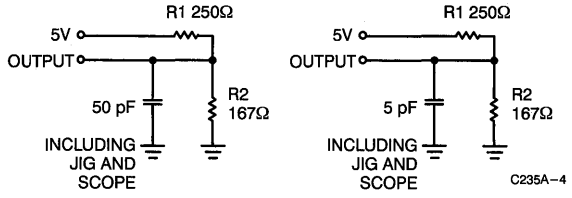
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

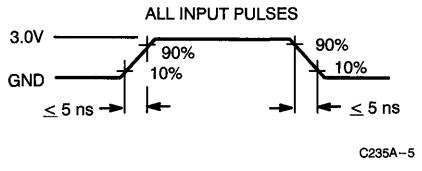
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

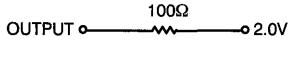
AC Test Loads and Waveforms[5]



(a) Normal Load **(b) High Z Load**



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C235A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{INIT}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

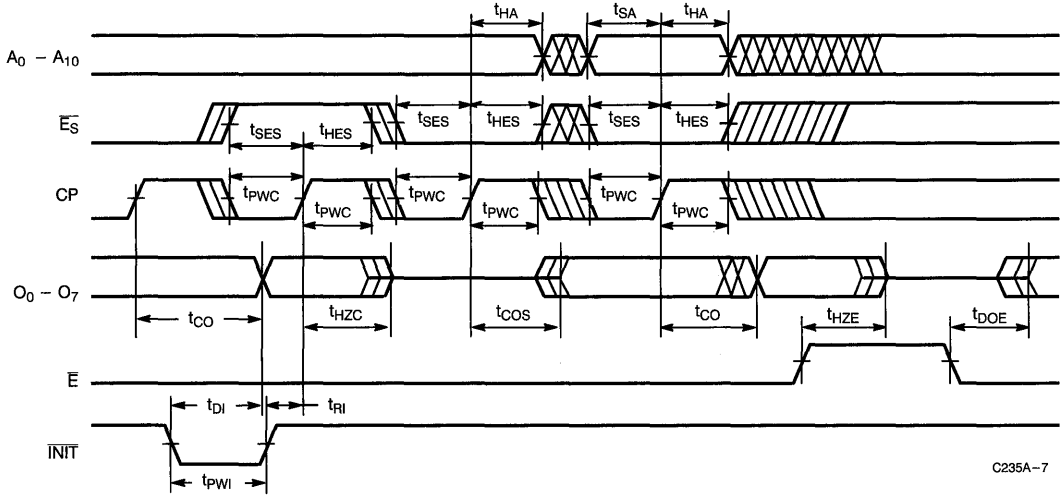
When the asynchronous initialize input, $\overline{INIT}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Characteristics Over Operating Range[3, 5]

Parameter	Description	7C235A–18		7C235A–25		7C235A–30		7C235A–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		12		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		10		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		20		25		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	15		20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH[7]		15		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25	ns

Note:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.

Switching Waveforms[5]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]							
	Read or Output Disable	$A_0, A_3 - A_9$	A_1	A_2	CP	$\overline{E}_S$	$\overline{E}$	$\overline{INIT}$	$O_7 - O_0$
	Other	$A_0, A_3 - A_9$	A_1	A_2	$\overline{PGM}$	$\overline{VFY}$	$\overline{E}$	V_{PP}	$D_7 - D_0$
Read		$A_0, A_3 - A_9$	A_1	A_2	X	V_{IL}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_0, A_3 - A_9$	A_1	A_2	X	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_0, A_3 - A_9$	A_1	A_2	X	X	V_{IH}	V_{IH}	High Z
Initialize		$A_0, A_3 - A_9$	A_1	A_2	X	X	V_{IL}	V_{IL}	Init Byte
Program		$A_0, A_3 - A_9$	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_0, A_3 - A_9$	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_0, A_3 - A_9$	A_1	A_2	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_0, A_3 - A_9$	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize Byte		$A_0, A_3 - A_9$	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check		$A_0, A_3 - A_9$	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

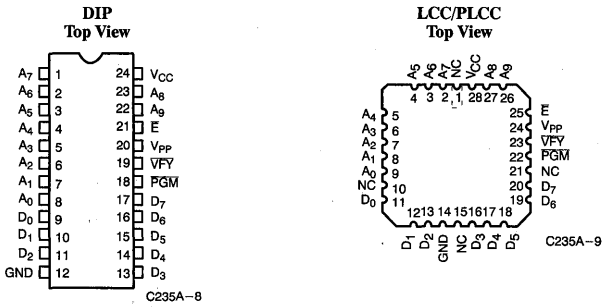
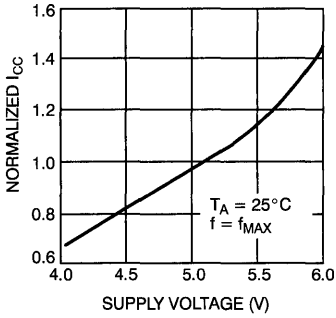


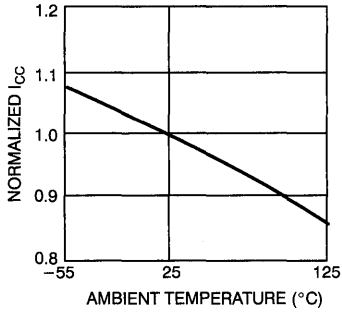
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

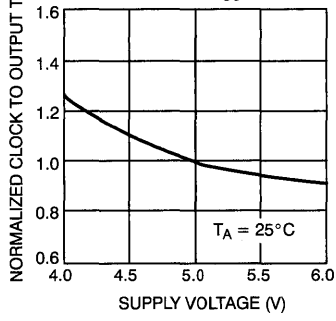
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



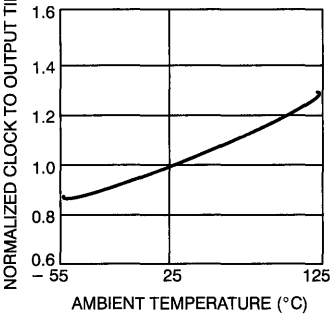
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



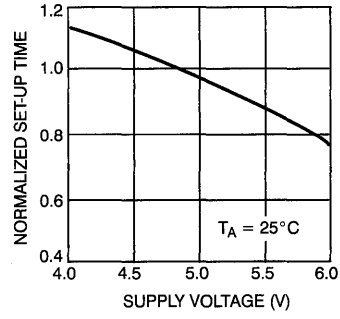
NORMALIZED CLOCK TO OUTPUT TIME vs. V_{CC}



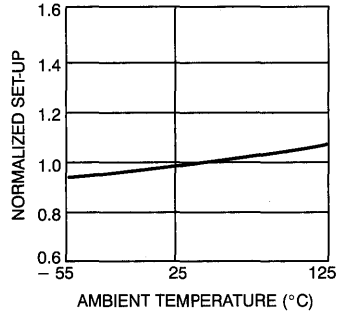
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



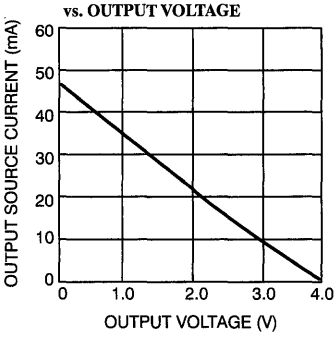
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



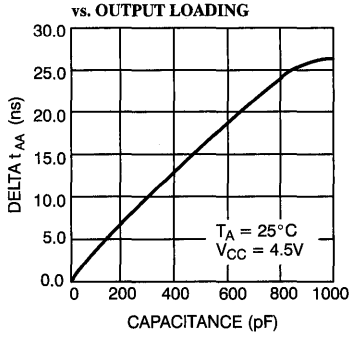
NORMALIZED SET-UP TIME vs. TEMPERATURE



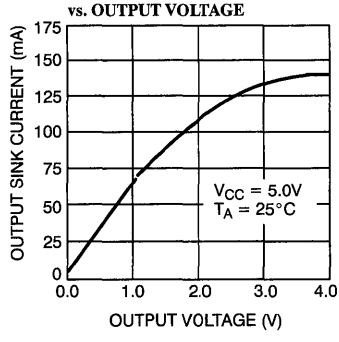
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C235A–10

Ordering Information[9]

Speed (ns) t_{SA}	Speed (ns) t_{CO}	Ordering Code	Package Name	Package Type	Operating Range
18	12	CY7C235A–18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–18JC	J64	24-Lead Plastic Leaded Chip Carrier	
		CY7C235A–18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C235A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–25JC	J64	24-Lead Plastic Leaded Chip Carrier	
		CY7C235A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C235A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–30JC	J64	24-Lead Plastic Leaded Chip Carrier	
		CY7C235A–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235A–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–40JC	J64	24-Lead Plastic Leaded Chip Carrier	
		CY7C235A–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88636	01KX	CY7C235A–40KMB
5962–88636	01LX	CY7C235A–40DMB
5962–88636	013X	CY7C235A–40LMB
5962–88636	02KX	CY7C235A–30KMB
5962–88636	02LX	CY7C235A–30DMB
5962–88636	023X	CY7C235A–30LMB

Document #: 38–00229–A

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the CY7C245A.

CY7C245

CYPRESS SEMICONDUCTOR

Reprogrammable 2K x 8 Registered PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 330 mW (commercial) for −35 ns, −45 ns**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

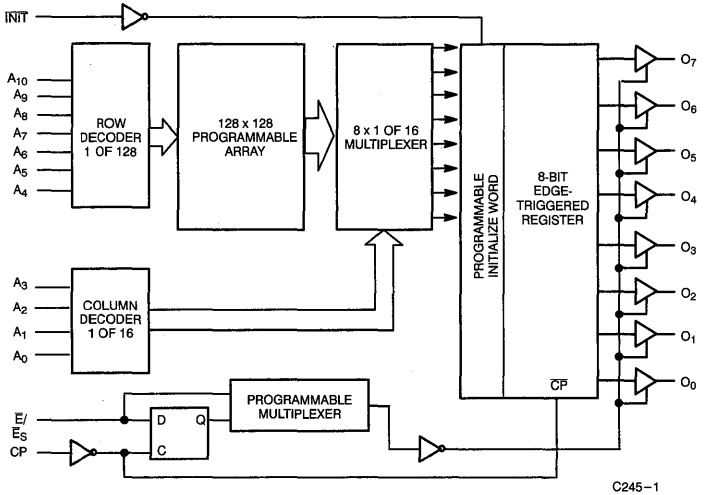
Product Characteristics

The CY7C245 is a high-performance 2048-word by 8-bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

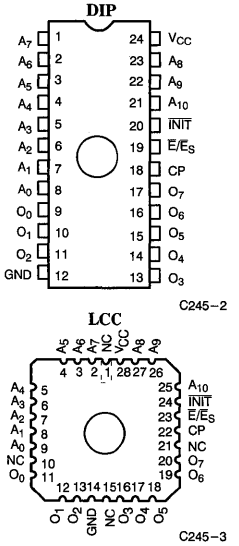
The CY7C245 replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word, or may be used as a PRESET or CLEAR function on the outputs. $\overline{INIT}$ is triggered by a LOW level, not an edge.

Logic Block Diagram



Pin Configurations



Selection Guide

			7C245–25	7C245–35	7C245–45
Maximum Set-up Time (ns)			25	35	40
Maximum Clock to Output (ns)			12	15	25
Maximum Operating Current (mA)	STD	Commercial	90	90	90
		Military		120	120
	L	Commercial		60	60

CYPRESS SEMICONDUCTOR

CY7C245A

Reprogrammable 2K x 8 Registered PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15-ns max set-up**
  - **— 10-ns clock to output**
- **Low power**
  - **— 330 mW (commercial) for −25 ns**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

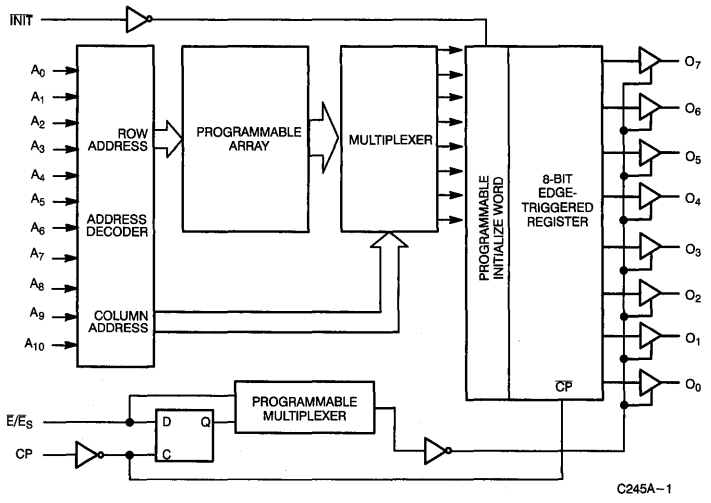
Functional Description

The CY7C245A is a high-performance 2048-word by 8-bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C245A replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow gang programming. The EPROM cells allow each memory location to be tested 100%, because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

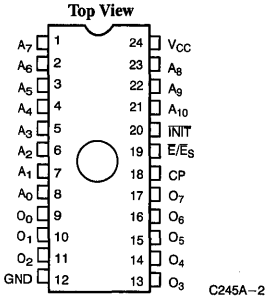
The CY7C245A has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word, or may be used as a PRESET or CLEAR function on the outputs. $\overline{INIT}$ is triggered by a low level, not an edge.

Logic Block Diagram

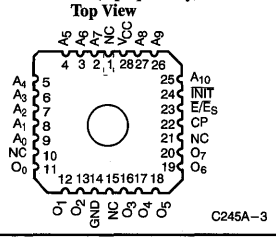


Pin Configurations

DIP
Top View



LCC/PLCC (Opaque only)
Top View



Selection Guide

			7C245A−15	7C245A−25 7C245AL−25	7C245A−35 7C245AL−35	7C245A−45 7C245AL−45
Maximum Set-Up Time (ns)			15	25	35	45
Maximum Clock to Output (ns)			10	12	15	25
Maximum Operating Current (mA)	Standard	Commercial	120	90	90	90
		Military		120	120	120
	L	Commercial		60	60	60

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C245A−15 Min.	7C245A−15 Max.	7C245A−25 7C245A−35 7C245A−45 Min.	7C245A−25 7C245A−35 7C245A−45 Max.	7C245AL−25 7C245AL−35 7C245AL−45 Min.	7C245AL−25 7C245AL−35 7C245AL−45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4								
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled[5]		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		90		60	mA
			Mil		120		120			
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

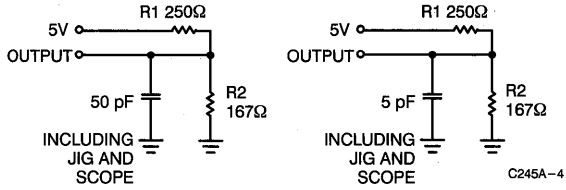
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

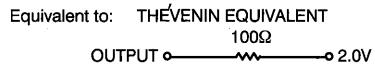
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[3, 4]



(a) Normal Load (b) High Z Load



Switching Characteristics Over Operating Range[3, 4]

Parameter	Description	7C245A-15		7C245A-25 7C245AL-25		7C245A-35 7C245AL-35		7C245A-45 7C245AL-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	15		25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		10		12		15		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		15		20		20		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	10		15		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	10		15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[8]		12		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[8]		15		15		20		30	ns

Notes:

7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

Operating Modes

The CY7C245A is a CMOS electrically programmable read only memory organized as 2048 words x 8 bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{INIT}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high-impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs ($A_0 - A_{10}$) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

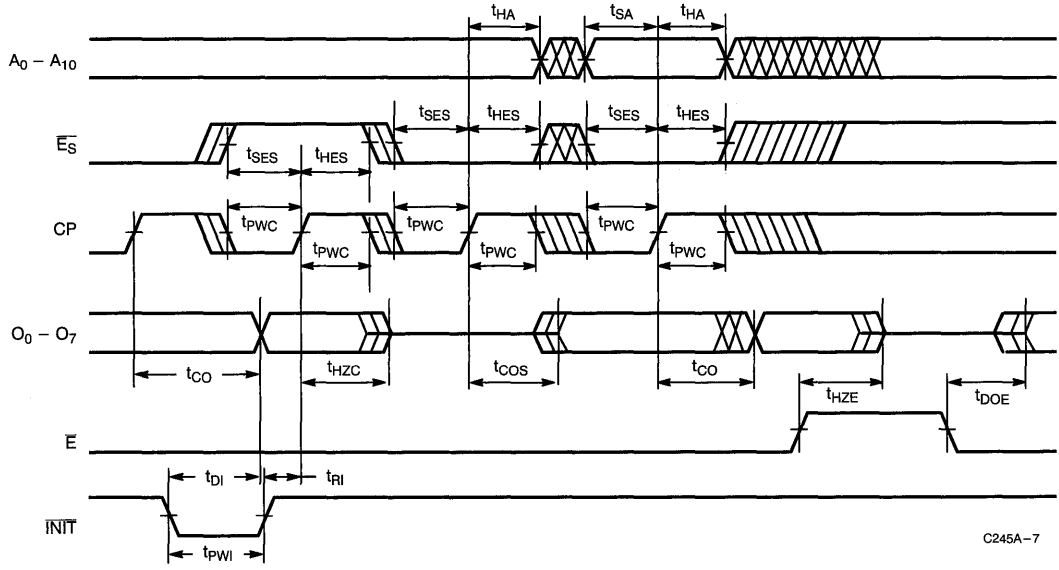
Operating Modes (continued)

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
.	.	.
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Control Byte

00 Asynchronous output enable (default state)
01 Synchronous output enable

Table 1. Mode Selection

Mode		Pin Function[9]							
	Read or Output Disable	**$A_{10} - A_4$**	**A_3**	**$A_2 - A_1$**	**A_0**	**CP**	**$\overline{E}, \overline{E}_S$**	**$\overline{INIT}$**	**$O_7 - O_0$**
	Other	**$A_{10} - A_4$**	**A_3**	**$A_2 - A_1$**	**A_0**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IL}/V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	X	V_{IH}	V_{IH}	High Z
Initialize		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	X	V_{IL}	V_{IL}	Init. Byte
Program		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Synchronous Enable		$A_{10} - A_4$	V_{IHP}	$A_2 - A_1$	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Initialization Byte		$A_{10} - A_4$	V_{ILP}	$A_2 - A_1$	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check Zeros		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Note:
9. X = "don't care" but not to exceed V_{CC} +5%.

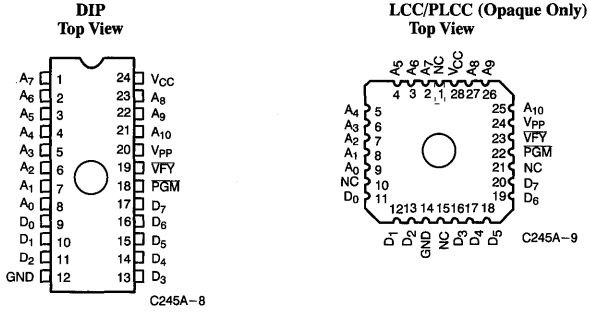
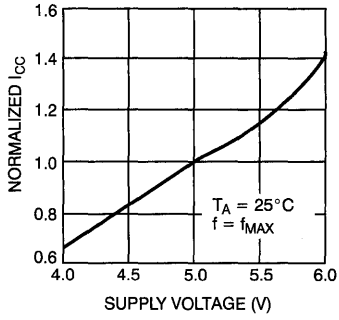


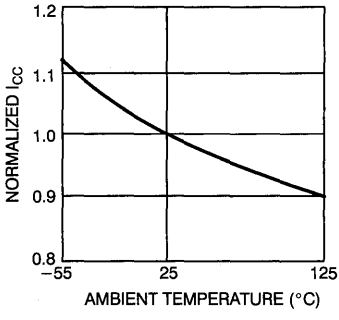
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

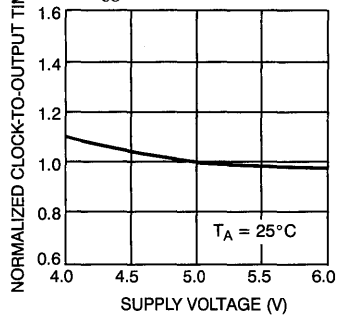
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



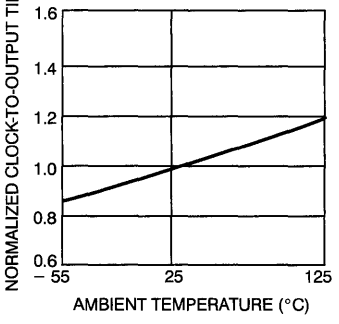
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



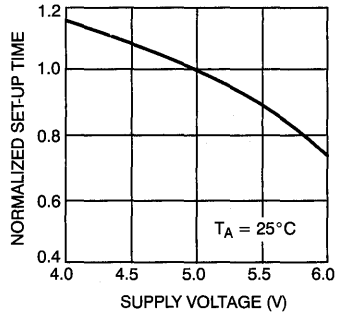
CLOCK TO OUTPUT TIME vs. V_{CC}



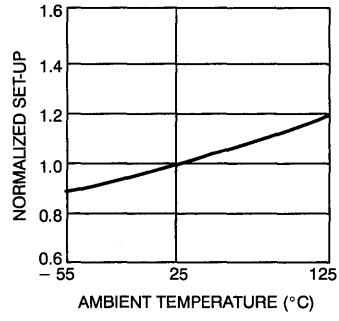
CLOCK TO OUTPUT TIME vs. TEMPERATURE



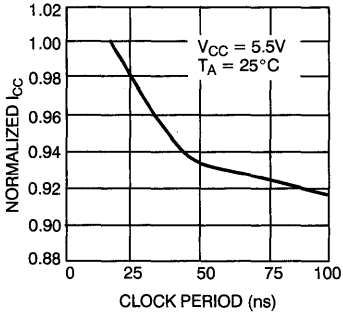
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



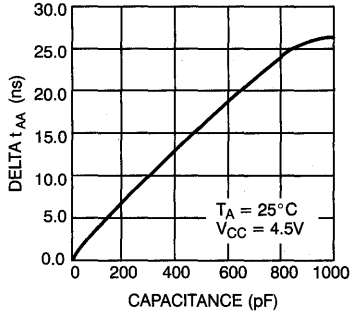
NORMALIZED SET-UP TIME vs. TEMPERATURE



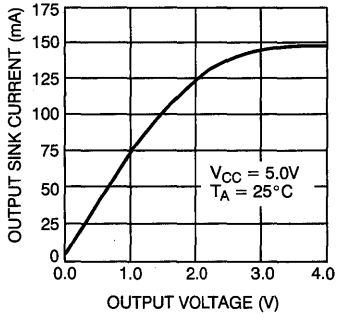
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C245A–10

Ordering Information[10]

Speed (ns)		I_{CC} (mA)	Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}					
15	10	120	CY7C245A–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A–15PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
			CY7C245A–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–15LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–15TMB	T73	24-Lead Windowed Cerpack T73	
			CY7C245A–15WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
25	15	60	CY7C245AL–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
			CY7C245AL–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		90	CY7C245A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–25PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–25SC	S13	24-Lead Molded SOIC	
			CY7C245A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–25LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–25TMB	T73	24-Lead Windowed Cerpack T73	
			CY7C245A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	20	60	CY7C245AL–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
			CY7C245AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		90	CY7C245A–35JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–35PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–35SC	S13	24-Lead Molded SOIC	
			CY7C245A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–35LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–35TMB	T73	24-Lead Windowed Cerpack T73	
			CY7C245A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	25	60	CY7C245A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A–45PC	P13	24-Lead (300-Mil) Molded DIP	
		90	CY7C245A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–45PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–45SC	S13	24-Lead Molded SOIC	
			CY7C245A–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–45LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–45TMB	T73	24-Lead Windowed Cerpack T73	
			CY7C245A–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88735	01KX	CY7C245A–45KMB
5962–88735	01LX	CY7C245A–45DMB
5962–88735	013X	CY7C245A–45LMB
5962–88735	02KX	CY7C245A–35KMB
5962–88735	02LX	CY7C245A–35DMB
5962–88735	023X	CY7C245A–35LMB
5962–88735	03KX	CY7C245A–35KMB
5962–88735	03LX	CY7C245A–35DMB
5962–88735	033X	CY7C245A–25LMB
5962–88735	04KX	CY7C245A–25KMB
5962–88735	04LX	CY7C245A–25DMB
5962–88735	043X	CY7C245A–25LMB
5962–87529	01KX	CY7C245A–45TMB
5962–87529	01LX	CY7C245A–45WMB
5962–87529	013X	CY7C245A–45QMB
5962–87529	02KX	CY7C245A–35TMB
5962–87529	02LX	CY7C245A–35WMB
5962–87529	023X	CY7C245A–35QMB
5962–89815	01LX	CY7C245A–35WMB
5962–89815	01KX	CY7C245A–35TMB
5962–89815	013X	CY7C245A–35QMB
5962–89815	02LX	CY7C245A–25WMB
5962–89815	02KX	CY7C245A–25TMB
5962–89815	023X	CY7C245A–25QMB
5962–89815	03LX	CY7C245A–18WMB
5962–89815	03KX	CY7C245A–18TMB
5962–89815	033X	CY7C245A–18QMB

Document #: 38–00074–F

CYPRESS SEMICONDUCTOR

CY7C251
CY7C254

16K x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C251)**
  - **— Less than 165 mW when deselected**
  - **— Fast access: 50 ns**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding > 2001V static discharge**

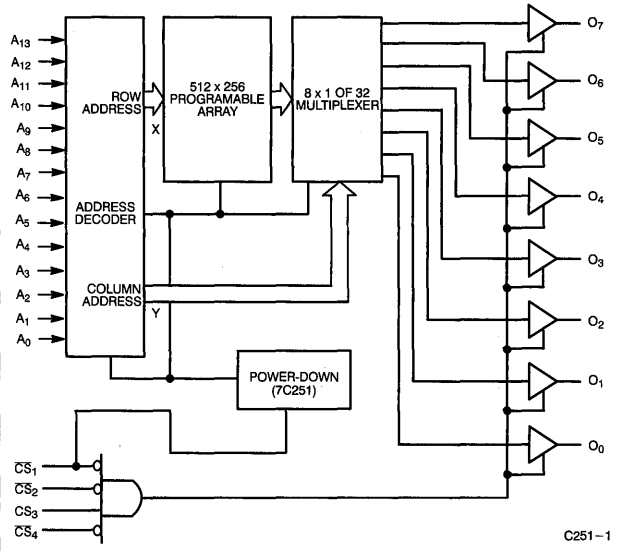
Functional Description

The CY7C251 and CY7C254 are high-performance 16,384-word by 8-bit CMOS PROMs. When deselected, the CY7C251 automatically powers down into a low-power stand-by mode. It is packaged in a 300-mil-wide package. The 7C254 is packaged in a 600-mil-wide package and does not power down when deselected. The 7C251 and 7C254 are available in reprogrammable packages equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C251 and CY7C254 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

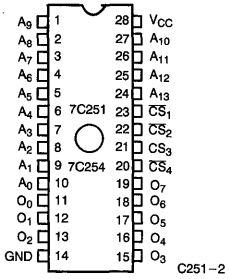
Reading is accomplished by placing all four chip selects in their active states. The contents of the memory location addressed by the address lines (A_0 – A_{13}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram

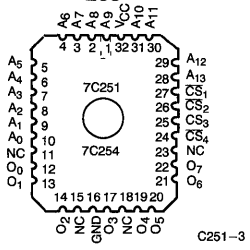


Pin Configurations

DIP/Flatpack



LCC



Selection Guide

		7C251–45, 7C254–45	7C251–55, 7C254–55	7C251–65, 7C254–65
Maximum Access Time (ns)		45	55	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	120	120	120
Standby Current (mA) (7C251 only)	Commercial	30	30	30
	Military	35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pin 22) 13.5V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

3 PROMs

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C251−45, 55, 65 7C254−45, 55, 65 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100	mA
			Mil		120	
I_{SB}	Standby Supply Current (7C251)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, I_{OUT} = 0 mA	Com'l		30	mA
			Mil		35	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

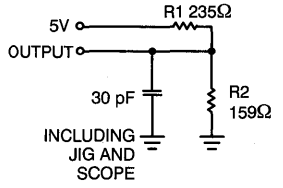
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

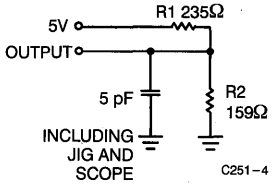
Notes:

1. Contact a Cypress representative regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

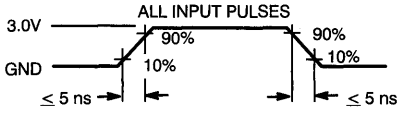
AC Test Loads and Waveforms[4]



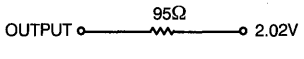
(a) Normal Load



(b) High Z Load



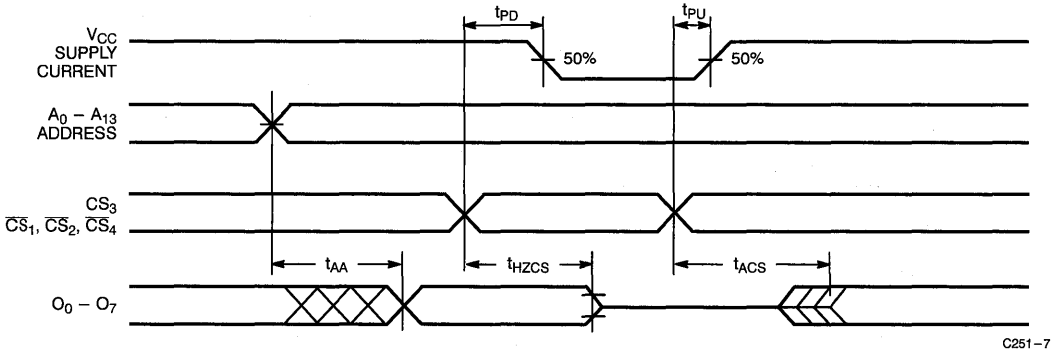
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 4]

Parameter	Description	7C251-45 7C254-45		7C251-55 7C254-55		7C251-65 7C254-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		65	ns
t_{HZCS1}	Chip Select Inactive to High Z[6]		25		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C251, $\overline{CS}_1$ Only)		50		60		70	ns
t_{ACS1}	Chip Select Active to Output Valid[6]		25		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C251, $\overline{CS}_1$ Only)		50		60		70	ns
t_{PU}	Chip Select Active to Power Up (7C251)	0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C251)[7]		50		60		70	ns

Switching Waveform[4, 7]



Notes:

6. t_{HZCS1} and t_{ACS1} refers to 7C254 (all chip selects); and 7C251 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).
7. Power-down controlled by 7C251 $\overline{CS}_1$ only.

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C251 and 7C254 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C251 or 7C254 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{VFY}$ toggles on each address), sequencing through all memory address locations, where all the data read will be zeros.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]					
	Read or Output Disable	**$A_{13} - A_0$**	**$\overline{CS_4}$**	**CS_3**	**$\overline{CS_2}$**	**$\overline{CS_1}$**	**$O_7 - O_0$**
	Other	**$A_{13} - A_0$**	**NA**	**$\overline{VFY}$**	**V_{PP}**	**$\overline{PGM}$**	**$D_7 - D_0$**
Read		$A_{13} - A_0$	V_{IL}	V_{IH}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{13} - A_0$	X	X	X	V_{IH}	High Z
Output Disable		$A_{13} - A_0$	X	X	V_{IH}	X	High Z
Output Disable		$A_{13} - A_0$	X	V_{IL}	X	X	High Z
Output Disable		$A_{13} - A_0$	V_{IH}	X	X	X	High Z
Program		$A_{13} - A_0$	X	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Program Verify		$A_{13} - A_0$	X	V_{ILP}	V_{PP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_{13} - A_0$	X	V_{IHP}	V_{PP}	V_{IHP}	High Z
Blank Check		$A_{13} - A_0$	X	V_{ILP}	V_{PP}	V_{IHP}	$O_7 - O_0$

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

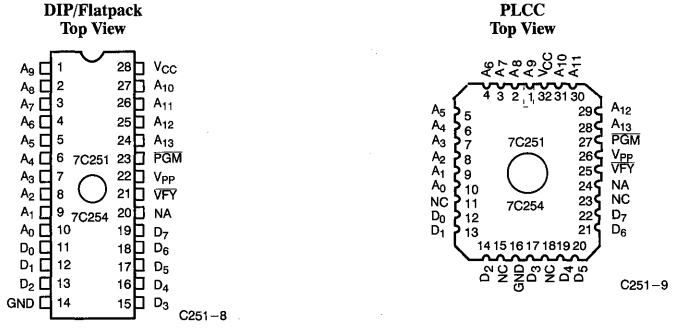
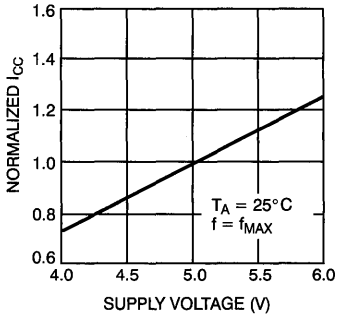


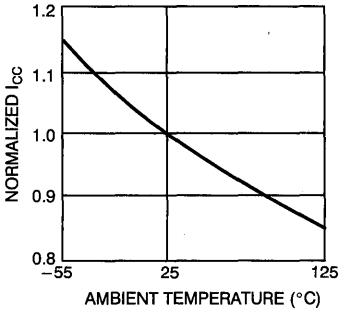
Figure 1. Programming Pinout

Typical DC and AC Characteristics

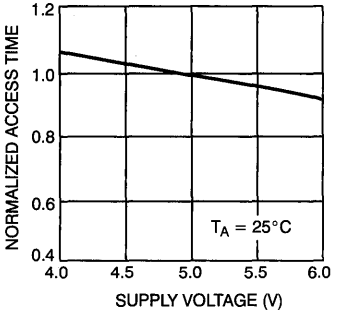
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



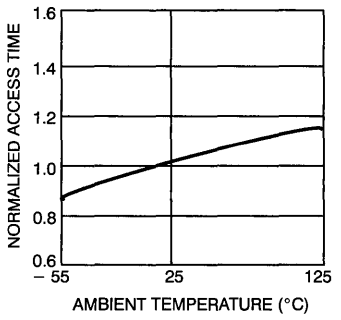
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



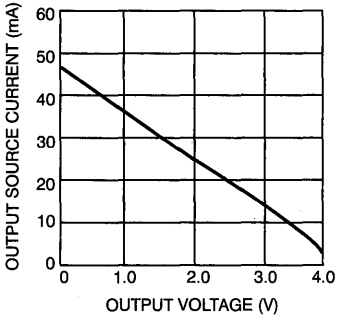
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



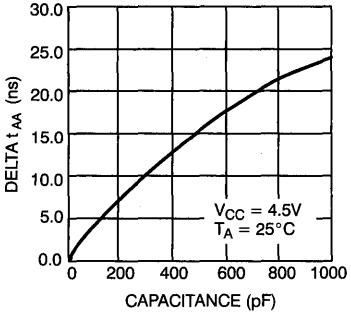
NORMALIZED ACCESS TIME vs. TEMPERATURE



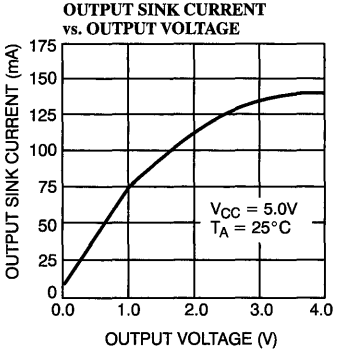
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C251–45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C251–55PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C251–65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251–65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C254–45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C254–55PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
65	CY7C254–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–65WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–65DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254–65WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[10]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[11]	7, 8, 9, 10, 11
t_{ACS2}[10]	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–8953701	YX	CY7C251–65WMB
5962–8953701	ZX	CY7C251–65TMB
5962–8953701	VX	CY7C251–65QMB
5962–8953702	YX	CY7C251–55WMB
5962–8953702	ZX	CY7C251–55TMB
5962–8953702	VX	CY7C251–55QMB
5962–8953801	XX	CY7C254–65WMB
5962–8953801	ZX	CY7C254–65TMB
5962–8953801	VX	CY7C254–65QMB
5962–8953802	XX	CY7C254–55WMB
5962–8953802	ZX	CY7C254–55TMB
5962–8953802	VX	CY7C254–55QMB

Notes:
10. 7C251 ($\overline{CS}_1$ only).
11. 7C254 and 7C251 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).

Document #: 38–00056–G

CYPRESS SEMICONDUCTOR

32K x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns (commercial)**
  - **— 55 ns (military)**
- **Low power**
  - **— 250 mW (commercial)**
  - **— 300 mW (military)**
- **Super low standby power**
  - **— Less than 75 mW when deselected**
- **EPROM technology 100% programmable**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

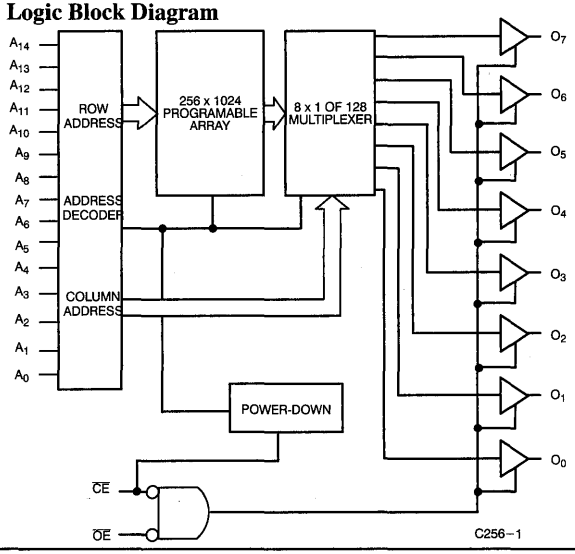
Functional Description

The CY7C256 is a high-performance 32,768-word by 8-bit CMOS PROM. When disabled ($\overline{CE}$ HIGH), the CY7C256 automatically powers down into a low-power stand-by mode. The CY7C256 is packaged in the industry standard 600-mil package. The CY7C256 is available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C256 offers the advantage of lower power and superior performance and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

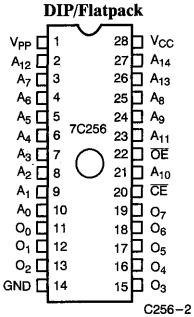
Reading the CY7C256 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram

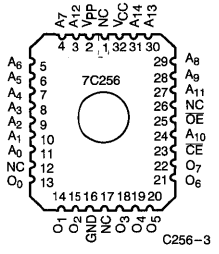


Pin Configurations

DIP/Flatpack



LCC/PLCC (Opaque Only)[1]



Selection Guide

		7C256–45	7C256–55
Maximum Access Time (ns)		45	55
Maximum Operating Current (mA)[2]	Commercial	50	50
	Military	60	60
Standby Current (mA)	Commercial	15	15
	Military	20	20
Chip Select Time (ns)		45	55
Output Enable (ns)		15	20

Notes:

1. For PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They must therefore be DU (don't use) for the PLCC package.
2. Add 2 mA/MHz for AC power component.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[3]	−40°C to +85°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C256−45, 55 Min.	7C256−45, 55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA[6]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	Power Supply Current[2]	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA, $\overline{CE}$=V_{IL}, $\overline{OE}$ = V_{IH}	Commercial		50	mA
			Military		60	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Commercial		15	mA
			Military		20	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

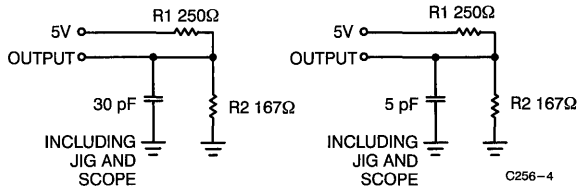
Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

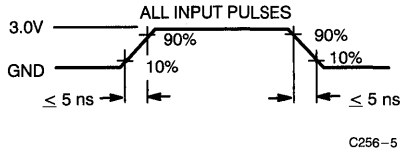
Notes:

3. Contact a Cypress representative for information on industrial temperature range specifications.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.
6. I_{OL}=12.0 mA for military devices.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. See Introduction to CMOS PROMs in this Data Book for general information on testing.

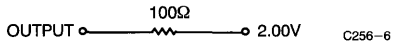
AC Test Loads and Waveforms[8]



(a) Normal Load **(b) High Z Load**



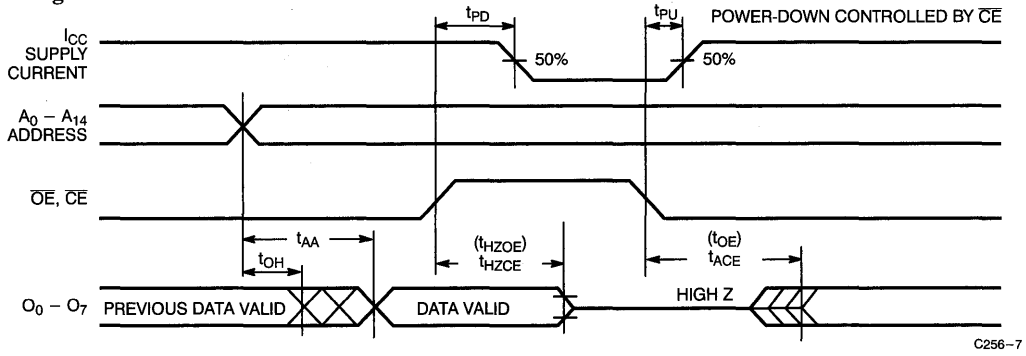
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5, 8]

Parameter	Description	7C256–45		7C256–55		Unit
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55	ns
t_{HZOE}	Output Enable Inactive to High Z		15		20	ns
t_{OE}	Output Enable Active to Output Valid		15		20	ns
t_{HZCE}	Chip Enable Inactive to High Z		45		55	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55	ns
t_{PU}	Chip Enable Active to Power Up	0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C256 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C256 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C256 Mode Selection

Mode		Pin Function[9]				
	Read or Output Disable	**$A_{14} - A_0$**	**$\overline{OE}$**	**$\overline{CE}$**	**V_{PP}**	**$O_7 - O_0$**
	Other	**$A_{14} - A_0$**	**$\overline{VFY}$**	**$\overline{PGM}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{14} - A_0$	V_{IL}	V_{IL}	Note 10	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Power Down		$A_{14} - A_0$	X	V_{IH}	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z

Notes:

9. X can be V_{IL} (V_{ILP}) or V_{IH} (V_{IHP}).
10. V_{PP} should not exceed V_{CC} in read mode.

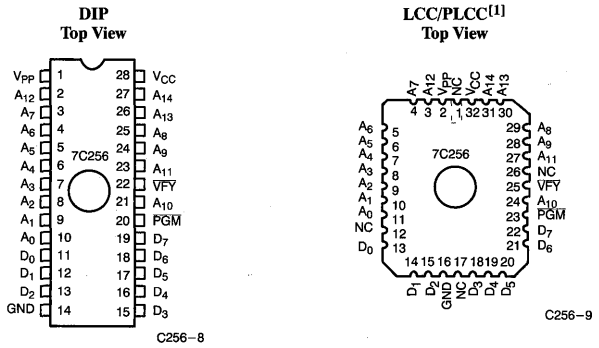


Figure 1. Programming Pinouts

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C256–45JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY7C256–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C256–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C256–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C256–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C256–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C256–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C256–55JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY7C256–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C256–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C256–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C256–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C256–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C256–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:
11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Document #: 38–00245

CY7C258
CY7C259

CYPRESS SEMICONDUCTOR

2K x 16 Reprogrammable State Machine PROM

Features

- **High speed: 100-MHz operation**
  - **t_{CP} = 10 ns**
  - **t_{CKO} = 8 ns**
  - **t_{AS} = 2 ns**
- **16-bit-wide state word**
- **Can be programmed as asynchronous PROM t_{AA} = 18 ns**
- **Optimum speed/ power**
- **Individually bypassable input and output registers**
- **Individually programmable address/ feedback muxes**
- **Synchronous and asynchronous chip select**
- **Synchronous and asynchronous $\overline{INIT}$ and programmable initialize word**
- **16 outputs (CY7C259)**
- **Software support**
- **CY7C258 available in 28-pin, 300-mil plastic and ceramic DIP, LCC, PLCC**
- **CY7C259 available in 44-pin LCC and PLCC**
- **Reprogrammable in windowed packages**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C258 and CY7C259 are 2K x 16 CMOS PROMs specifically designed for use in state machine applications.

State machines are one of the most common applications for registered PROMs. The CY7C258 and CY7C259 feature internal state feedback and a variety of programmable features to support 100-MHz state machines with as many as 2,048 distinct states.

It is easy to use a PROM as a state machine. Each array location contains output data as well as information fed back to select the next state. Note that a PROM is only limited by the number of array inputs. If a given state machine can be implemented in the number of inputs/ feedbacks available (11 on the CY7C258/259), then it will always fit in the device. No software minimization is required.

Among the programmable features of the CY7C258/CY7C259 are individually bypassable input and output registers. The registers run off the same clock for pipeline capability. Each individual register can be programmed to capture data at the rising edge of the clock or to be transparent.

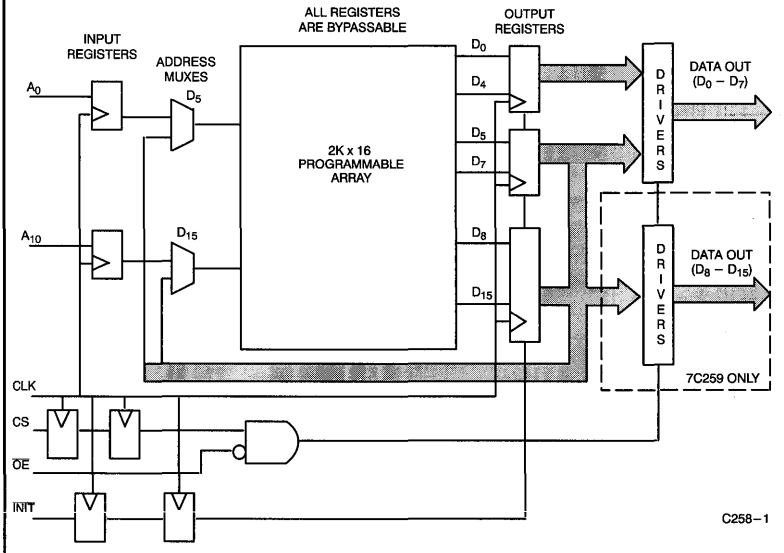
The registers at the inputs are useful for signals that require short set-up times (t_{AS} = 2 ns). The input register does introduce a cycle of latency, however. For signals that directly affect the next state of the machine, each input register can be bypassed. Note that the cycle time remains the same (10-ns min.), even if the inputs are bypassed.

Registers at the output are used to hold both state information and output data. These registers are also bypassable for maximum flexibility. Occasionally, an individual output cannot wait for the next clock edge. These outputs are sometimes called Mealy outputs, and can be created by bypassing the appropriate output register.

Since the CY7C258 and CY7C259 contain a 2K array, they each require 11 inputs. Each of these inputs can come from an input pin or from internal output register feedback. Eleven individually programmable address muxes allow the user to select the ratio of pin input and state feedback.

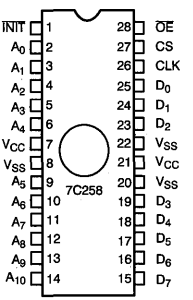
These devices have both an asynchronous output ($\overline{OE}$) and a synchronous chip select (CS). The CS input is polarity programmable and registered twice. Each of

Logic Block Diagram



Pin Configurations

DIP
Top View



C258–2

Functional Description (continued)

the CS registers can be bypassed in the same manner as the address input and output registers.

A separately controllable $\overline{INIT}$ input is included for user resets. If $\overline{INIT}$ is sampled LOW on the rising edge of CLK, the user programmable initialization word will appear at the outputs after the next CLK cycle. Each of the $\overline{INIT}$ registers can be bypassed in the same manner as the address input and output registers.

The difference between the CY7C258 and CY7C259 is in the packaging. The CY7C258 has three different types of outputs. $D_4 - D_0$ are dedicated outputs that do not feed back to the input muxes. $D_5 - D_7$ appear on the output pins and are fed back to the input muxes. Finally, $D_8 - D_{15}$ are dedicated feedback lines that do not appear at the output pins. The dedicated feedback allows the CY7C258 to be packaged in 28-pin packages. The CY7C258 is available in 28-pin LCC, PLCC, and slim 300-mil DIP packages.

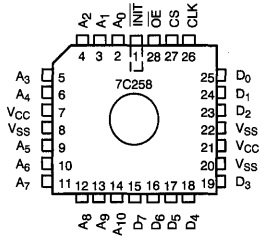
On the CY7C259, all 16 array outputs are available at the pins. Outputs $D_4 - D_0$ remain as dedicated outputs while $D_5 - D_{15}$ appear at the pins and are also fed back to the input muxes. This organization allows the user maximum flexibility in selecting the ratio of outputs to state feedback. The availability of state information at pins also improves testability. The CY7C259 is packaged in 44-pin LCC and PLCC packages.

Several third-party programmers will feature support for PROMs as state machines, including Data I/O (ABEL), ISDATA (LOG/iC), and CUPL. The devices are also supported on the Cypress *Warp2* development software.

The CY7C258 and CY7C259 offer the advantage of low power, superior performance, and programming yield. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

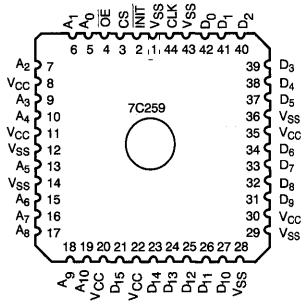
Pin Configurations (continued)

LCC/PLCC(Opaque Only)
Top View



C258-3

LCC/PLCC (Opaque Only)
Top View



C258-4

Selection Guide

	Commercial	Commercial and Military		
	7C258-10 7C259-10	7C258-12 7C259-12	7C258-15 7C259-15	Unit
Minimum Cycle Time	10	12	15	ns
Registered Input Set-Up/Hold[1]	2/2 or 5/0	3/3 or 7/0	4/4 or 8/1	ns
Bypassed Input Set-Up/Hold	10/0	12/0	15/0	ns
Clock-to-Output	8	9	11	ns

Note:
1. This parameter is programmable.

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	− 40°C to +85°C	5V ± 10%
Military[3]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA	Commercial		0.4	V
		V_{CC} = Min., I_{OL} = 6 mA	Military		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0	6.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		− 3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	Active Current [7]	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		70	mA
		V_{CC} = Max., I_{OUT} = 0 mA	Military		90	mA

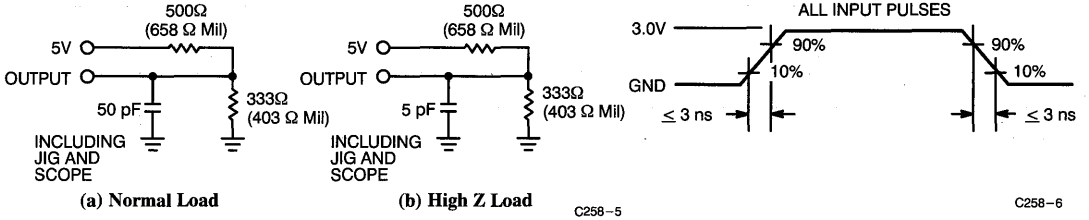
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

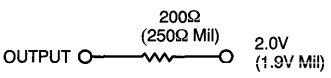
Notes:

2. Contact a Cypress representative for industrial temperature range specification.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Add 1 mA/MHz for AC power component.

AC Test Loads and Waveforms[4]



Equivalent to: THÉVENIN EQUIVALENT

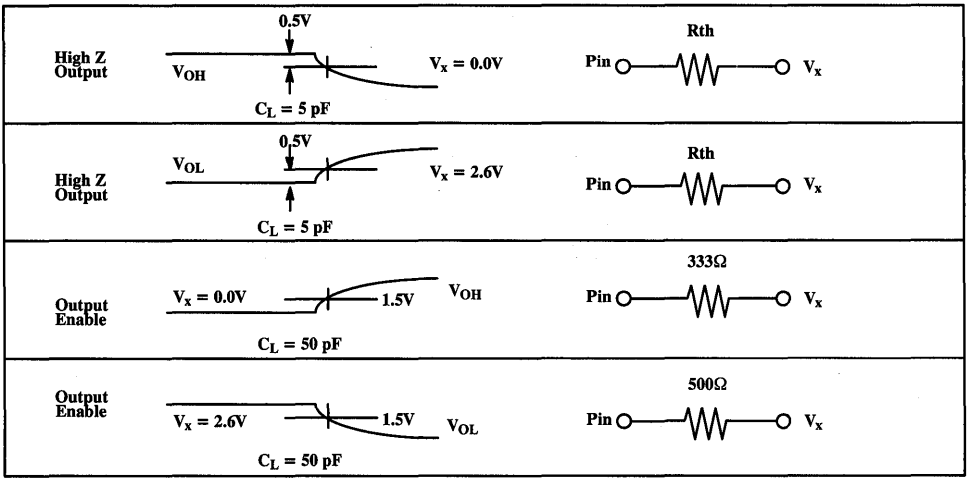


Switching Characteristics Over the Operating Range[3,4]

Parameter	Description	Commercial		Commercial and Military				Unit
		7C258–10 7C259–10		7C258–12 7C259–12		7C258–15 7C259–15		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	10		12		15		ns
t_{CH}	Clock HIGH	4		5		6.5		ns
t_{CL}	Clock LOW	4		5		6.5		ns
t_{AS}/t_{AH}	Register Input Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{ABS}	Address Set-Up to CLK with Input Bypassed	10		12		15		ns
t_{ABH}	Address Hold from CLK with Input Bypassed	0		0		0		ns
t_{CSS}/t_{CSH}	Chip Select Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{IPD}	Asynchronous $\overline{INIT}$ to Output Valid with Output Bypassed		21		21		25	ns
t_{CKO1}	Output CLK to Registered Output Valid		8		9		11	ns
t_{CKO2}	Output CLK to Output Valid with Output Bypassed		18		18		21	ns
t_{DH}	Data Hold from CLK	2		2		2		ns
t_{COV}	CLK to Output Valid[8]		8		9		11	ns
t_{COZ}	CLK to High Z Output[8]		8		9		11	ns
t_{CSV}	CS to Output Valid with Input Bypassed[8]		10		12		15	ns
t_{CSZ}	CS to High Z Output with Input Bypassed [8]		10		12		15	ns
t_{OEV}	$\overline{OE}$ to Output Valid[8]		8		9		11	ns
t_{OEZ}	$\overline{OE}$ to High Z Output[8]		8		9		11	ns
t_{IS}/t_{IH}	$\overline{INIT}$ Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{IBS}	$\overline{INIT}$ Set-Up to CLK with Input Bypassed	10		12		15		ns
t_{IBH}	$\overline{INIT}$ Hold from CLK with Input Bypassed	0		0		0		ns
t_{PD}	Propagation Delay with Input and Output Bypassed		18		18		21	ns
t_{ICO}	CLK to Output Valid with Output Bypassed		18		18		21	ns
t_{IW}	Asynchronous $\overline{INIT}$ Pulse Width	10		12		15		ns
t_{IDV}	Asynchronous $\overline{INIT}$ to Data Valid		10		12		15	ns
t_{ICR}	Asynchronous $\overline{INIT}$ Recovery to Clock	10		12		15		ns

Note:
8. See Output Waveform—Measurement Level.

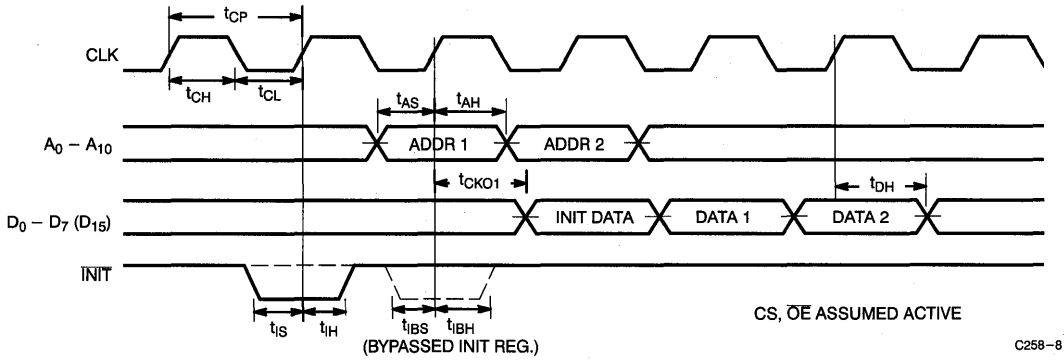
Output Waveform—Measurement Level



C258-7

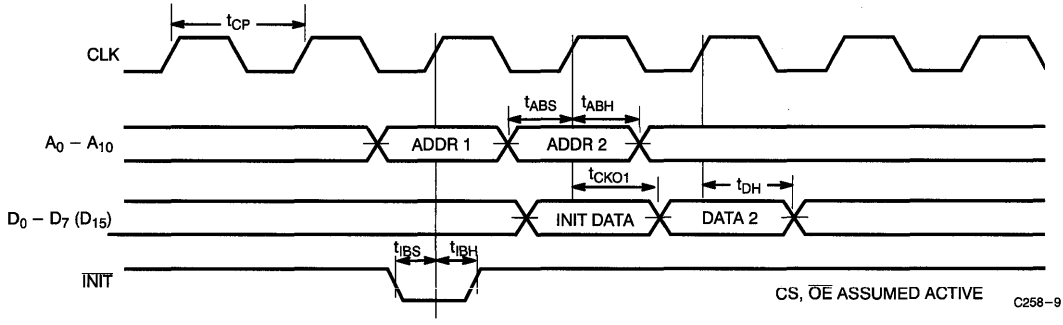
Switching Waveforms

Registered Input and Output (combined with $\overline{INIT}$)



C258-8

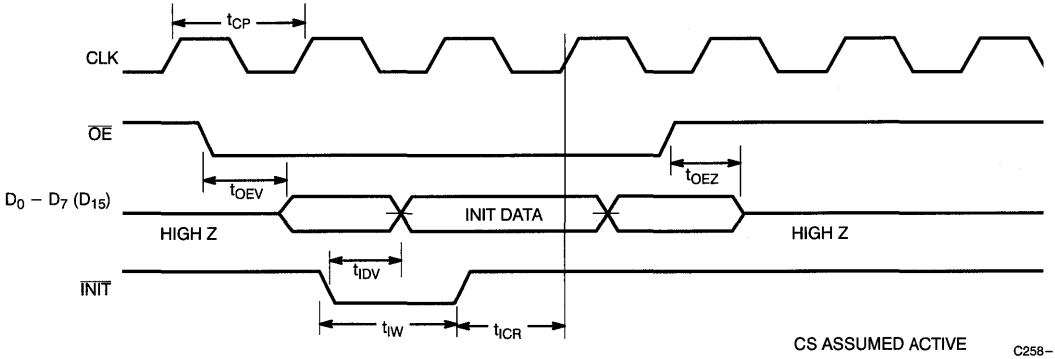
Bypassed Address and $\overline{INIT}$ Registers



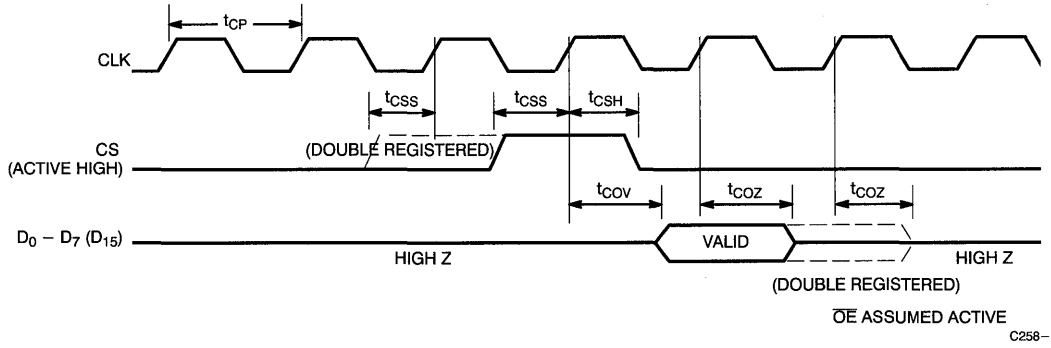
C258-9

Switching Waveforms (continued)

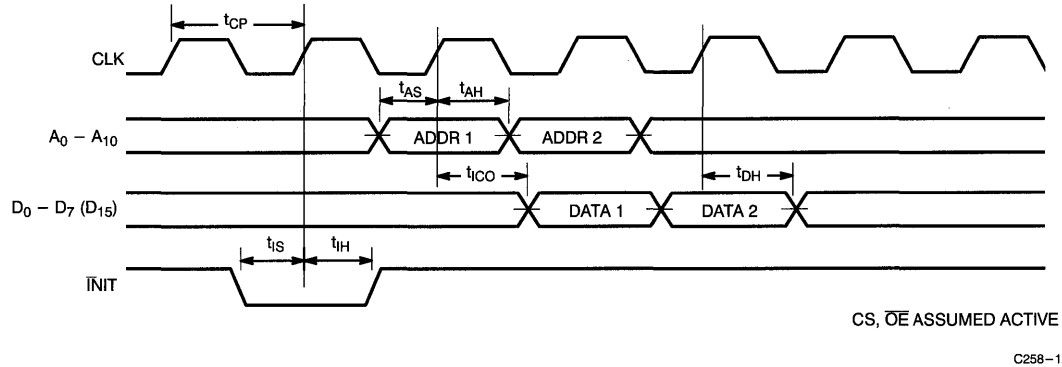
Asynchronous $\overline{INIT}$ and $\overline{OE}$



Single- and Double-Registered Chip Select



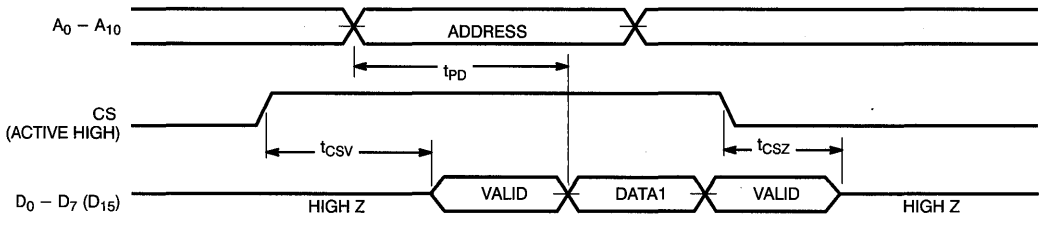
Bypassed Output Register[9]



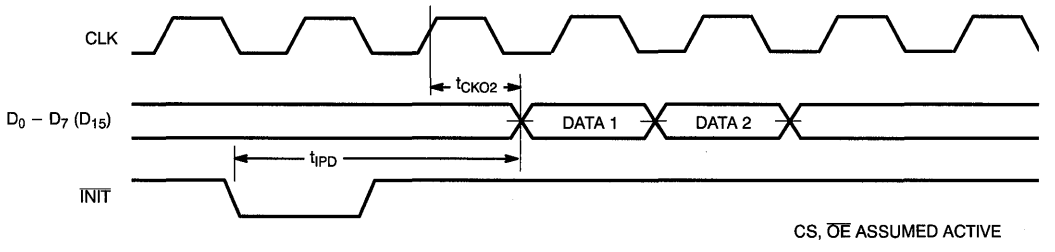
Note:
9. Even though the register is bypassed, $\overline{INIT}$ continues to set the output register (for feedback purposes).

Switching Waveforms

Bypassed Input and Output Register (CS and Address)



Asynchronous $\overline{INIT}$ and Bypassed Output Register[10]



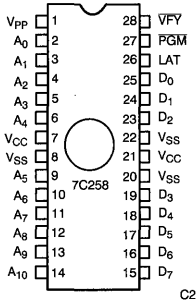
Note:
10. Output registers configured as feedback to the array and bypassed with respect to the output.

Mode Table

Mode	LAT (7C258–CLK)	$\overline{VPP}$ ($\overline{INIT}$)	$\overline{PGM}$ (CS)	$\overline{VFY}$ ($\overline{OE}$)	D_0–D_{15} (259) D_0–D_7 (258)
Latch High Byte	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Inhibit	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	HI–Z
Program Enable	V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Verify	V_{ILP}	V_{PP}	V_{IHP}	V_{ILP}	V_{OHP}/V_{OLP}

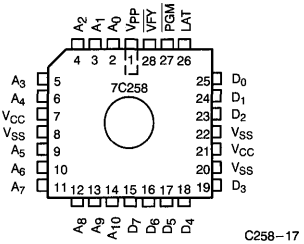
Programming Pinouts

DIP



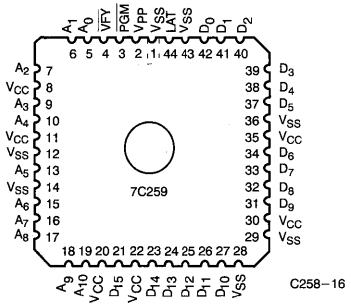
C258–15

LCC/PLCC (Opaque Only)



C258–17

LCC/PLCC (Opaque Only)



C258–16

Programming Information

This datasheet provides some but not all the of programming information necessary for on-board programming of the CY7C258 and CY7C259. For more information about on-board programming of Cypress PROMs contact your local Cypress Field Sales Engineer or Field Applications Engineer.

7C258 Bitmap[11]

Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C258	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	. . . Array Data . . .
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1=Bypassed Register)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2049	801	Array Input Select (1= Feedback)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2050	802	Output Register Select (1= Bypassed Register)	X X X X X X X X D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1= INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	X X X X X X X X SH C_1 C_2 CP IB IA X X

Note:
11. All configurable bits default to 0.

7C259 Bitmap[11]

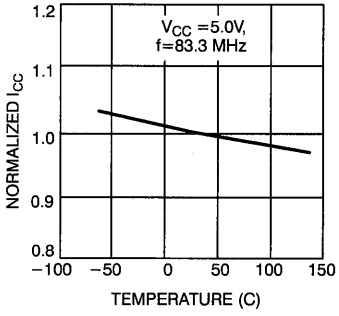
Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C259	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	Array Data
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1 = Bypassed Register)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2049	801	Array Input Select (1 = Feedback)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2050	802	Output Register Select (1 = Bypassed Register)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1 = INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	SH C_1 C_2 CP IB IA X X X X X X X X X X

Architecture Word

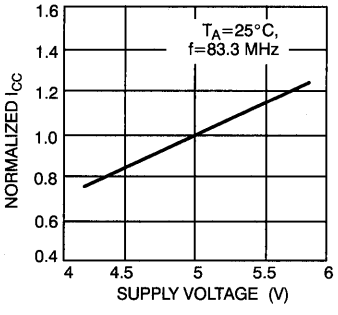
Control Option	Control Word			Function
	Bit (258)	Bit (259)	Programmed level	
IA (INIT Async)	D_2	D_{10}	0 = Default 1 = Programmed	Synchronous INIT Asynchronous INIT
IB (INIT Bypass)	D_3	D_{11}	0 = Default 1 = Programmed	INIT Registered Bypass INIT Register
CP (CS Polarity)	D_4	D_{12}	0 = Default 1 = Programmed	CS Active LOW CS Active HIGH
C2 (CS Bypass) (Buried Register)	D_5	D_{13}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
C1 (CS Bypass) (Input Register)	D_6	D_{14}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
SH (Set-Up/Hold)	D_7	D_{15}	0 = Default 1 = Programmed	Set-Up/Hold = 2/2 ns Set-Up/Hold = 5/0 ns

Typical DC and AC Characteristics

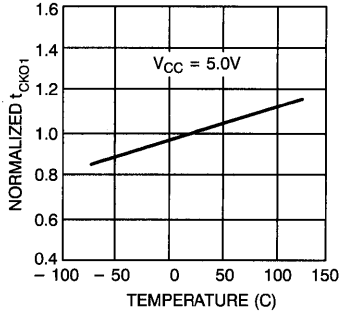
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



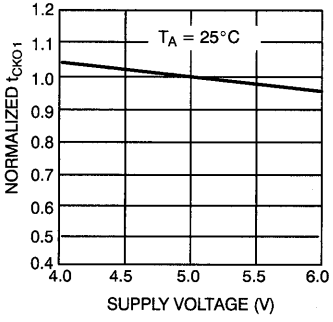
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



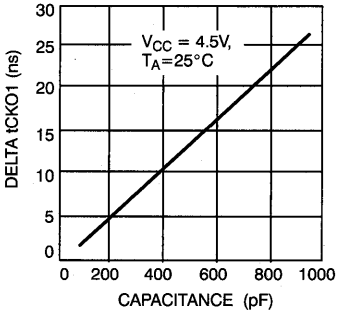
NORMALIZED t_{CKO1} vs. AMBIENT TEMPERATURE



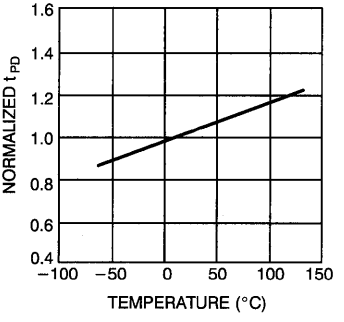
NORMALIZED t_{CKO1} vs. SUPPLY VOLTAGE



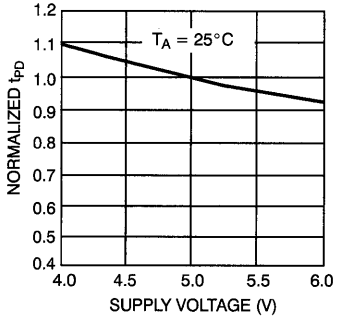
TYPICAL t_{CKO1} CHANGE vs. OUTPUT LOADING



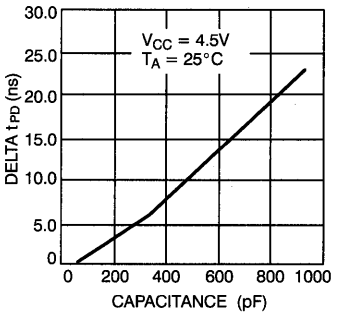
NORMALIZED t_{PD} vs. AMBIENT TEMPERATURE



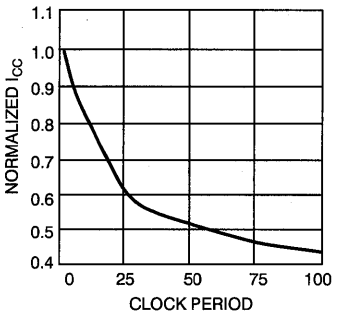
NORMALIZED t_{PD} vs. SUPPLY VOLTAGE



DELTA t_{PD} vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CLOCK PERIOD



Ordering Information[12]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C258–10HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–10WC	W22	28-Lead (300-Mil) Windowed CerDIP	
12	CY7C258–12HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–12WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C258–12HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
	CY7C258–12LMB	L64	28-Square Leadless Chip Carrier	
	CY7C258–12QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C258–12WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
15	CY7C258–15HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–15JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C258–15HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
	CY7C258–15LMB	L64	28-Square Leadless Chip Carrier	
	CY7C258–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C258–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C259–10HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–10JC	J67	44-Lead Plastic Leaded Chip Carrier	
12	CY7C259–12HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–12JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C259–12HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C259–12LMB	L67	44-Square Leadless Chip Carrier	
	CY7C259–12QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
15	CY7C259–15HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–15JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C259–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C259–15LMB	L67	44-Square Leadless Chip Carrier	
	CY7C259–15QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

Note:
12. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3,
V_{OL}	1, 2, 3,
V_{IH}	1, 2, 3,
V_{IL}	1, 2, 3,
I_{IX}	1, 2, 3,
I_{OZ}	1, 2, 3,
I_{CC}	1, 2, 3,

Switching Characteristics

Parameter	Subgroups
t_{CP}	7, 8, 9, 10, 11
t_{CH}	7, 8, 9, 10, 11
t_{CL}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{ABS}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{IPD}	7, 8, 9, 10, 11
t_{CKO1}	7, 8, 9, 10, 11
t_{CKO2}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11
t_{CSV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{IBS}	7, 8, 9, 10, 11
t_{IBH}	7, 8, 9, 10, 11
t_{PD}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{IW}	7, 8, 9, 10, 11
t_{IDV}	7, 8, 9, 10, 11
t_{ICR}	7, 8, 9, 10, 11

Document #: 38–00173–E

CY7C261
CY7C263/CY7C264

8K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **Super low standby power (7C261)**
  - **— Less than 220 mW when deselected**
  - **— Fast access: 20 ns**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ± 10% V_{CC}, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**

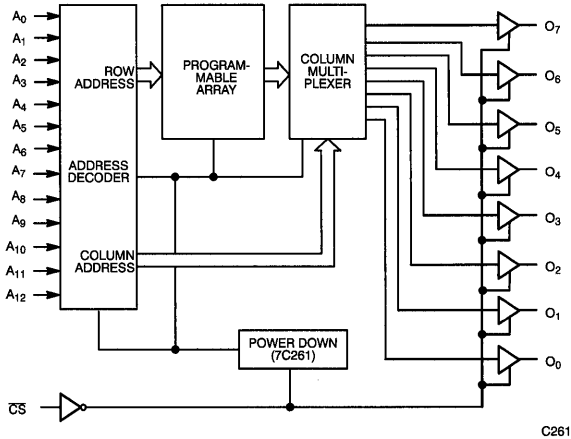
Functional Description

The CY7C261, CY7C263, and CY7C264 are high-performance 8192-word by 8-bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low-power standby mode. It is packaged in a 300-mil-wide package. The 7C263 and 7C264 are packaged in 300-mil-wide and 600-mil-wide packages respectively, and do not power down when deselected. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263, and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Read is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address line (A_0 – A_{12}) will become available on the output lines (O_0 – O_7).

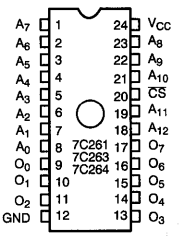
Logic Block Diagram



C261–1

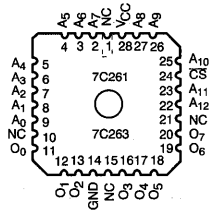
Pin Configurations

DIP/Flatpack Top View



C261–2

LCC/PLCC (Opaque Only) Top View



C261–3

Selection Guide

		7C261–20 7C263–20 7C264–20	7C261–25 7C263–25 7C264–25	7C261–35 7C263–35 7C264–35	7C261–45 7C263–45 7C264–45	7C261–55 7C263–55 7C264–55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	100	100	100
	Military		140	120	120	120
Maximum Standby Current (mA) (7C261 only)	Commercial	40	40	30	30	30
	Military		40	30	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to + 7.0V

DC Program Voltage (Pin 19 DIP, Pin 23 LCC) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial[1]	− 40°C to + 85°C	5V ± 10%
Military[2]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C261−20, 25 7C263−20, 25 7C264−20, 25		7C261−35, 45, 55 7C263−35, 45, 55 7C264−35, 45, 55		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4				V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA				2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA (6 mA Mil)			0.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA					0.4	V
V_{IH}	Input HIGH Level			2.0		2.0		V
V_{IL}	Input LOW Level				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	− 10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		Note 4		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		− 40	+40	− 40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	− 20	− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V	Com'l		120		100	mA
			Mil		140		120	
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Com'l		40		30	mA
			Mil		40		30	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Capacitance[4]

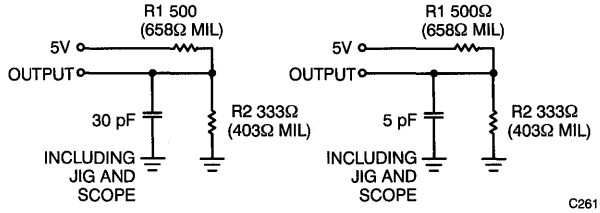
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

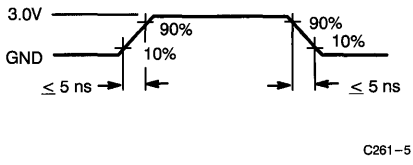
1. See the Ordering Information section regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[4]

Test Load for −20 through −30 speeds

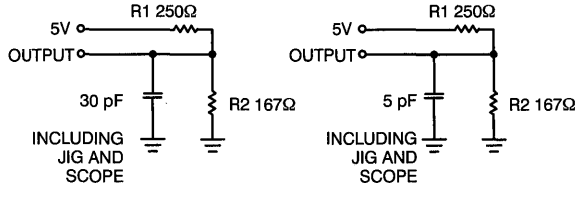


(a) Normal Load (b) High Z Load



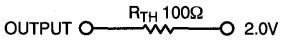
Equivalent to: THEVENIN EQUIVALENT

Test Load for −35 through −55 speeds



(c) Normal Load (d) High Z Load

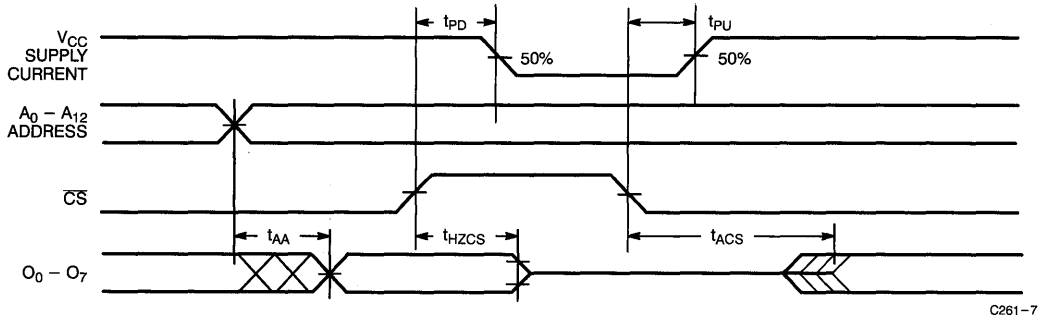
Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3, 4]

Parameter	Description	7C261−20 7C263−20 7C264−20		7C261−25 7C263−25 7C264−25		7C261−35 7C263−35 7C264−35		7C261−45 7C263−45 7C264−45		7C261−55 7C263−55 7C264−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z		12		12		20		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)		20		25		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid		12		12		20		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		20		25		35		45		55	ns
t_{PU}	Chip Select Active to Power-Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C261)		20		25		35		45		55	ns

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 45 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13-bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

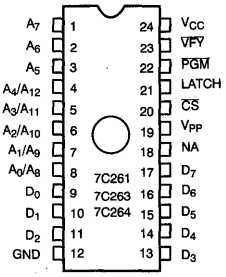
These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP} In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The verify mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the program inhibit mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. Program inhibit is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Table 1. Mode Selection

Mode		Pin Function[6,7]						
	Read or Output Disable	A_{12}	A_{11}	A_{10}	A_9	A_8	$\overline{CS}$	$O_7 - O_0$
	Program	**NA**	V_{PP}	**LATCH**	$\overline{PGM}$	$\overline{VFY}$	$\overline{CS}$	$D_7 - D_0$
Read		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IL}	$O_7 - O_0$
Output Disable		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IH}	High Z
Program		V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	$D_7 - D_0$
Program Inhibit		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	High Z
Program Verify		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	$O_7 - O_0$
Blank Check		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	$O_7 - O_0$

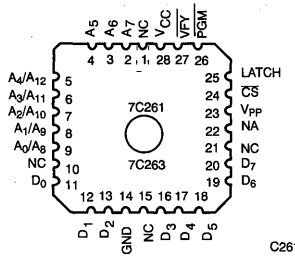
Notes:
6. X = "don't care" but not to exceed V_{CC} ±5%.
7. Addresses $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in programming modes.

DIP/Flatpack
Top View



C261-8

LCC/PLCC (Opaque only)
Top View



C261-9

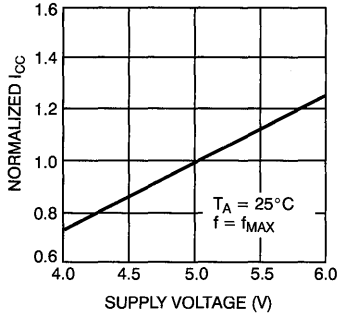
Figure 1. Programming Pinouts

Programming Information

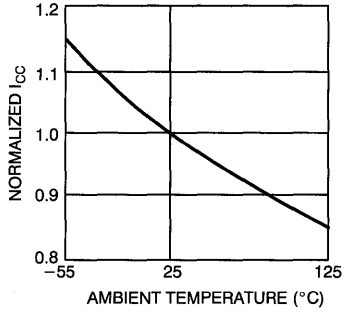
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics

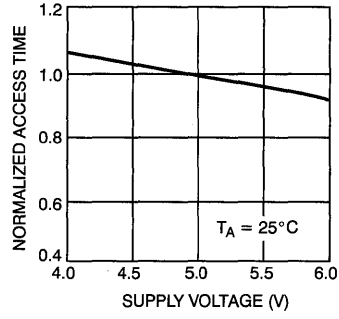
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



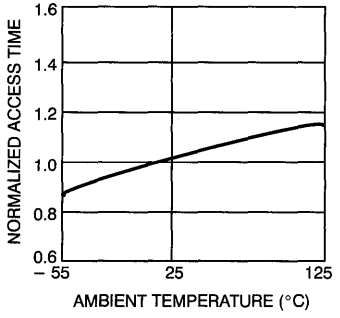
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



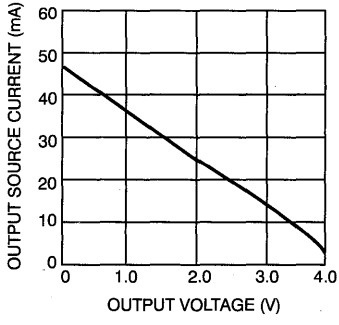
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



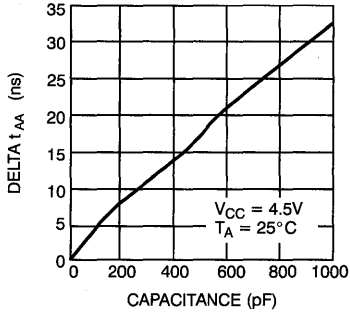
NORMALIZED ACCESS TIME vs. TEMPERATURE



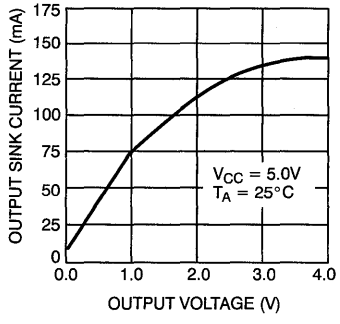
OUTPUT SOURCE CURRENT vs. VOLTAGE



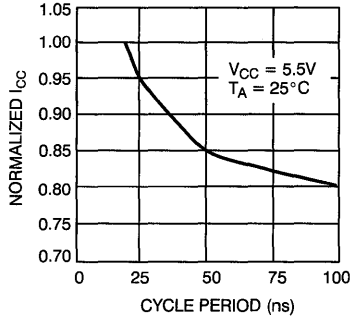
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C261-20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C261-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-25TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C261-35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-35TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C261-45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-45TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C261-55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261-55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261-55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261-55TMB	T73	24-Lead Windowed Cerpack	
	CY7C261-55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[8] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C263–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C263–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–25TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C263–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–35TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C263–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–45TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C263–55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–55TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C264–20DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–20PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–20WC	W12	24-Lead (600-Mil) Windowed CerDIP	
25	CY7C264–25DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–25PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–25WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–25DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–25WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
35	CY7C264–35DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–35PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–35WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–35DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–35WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
45	CY7C264–45DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–45PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–45WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–45DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
55	CY7C264–55DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–55PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–55WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–55DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–55WMB	W12	24-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[9]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[10]	7, 8, 9, 10, 11
t_{ACS2}[10]	7, 8, 9, 10, 11

Notes:
9. 7C261 only.
10. 7C263 and 7C264 only.

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–87515	05KX	CY7C261–45TMB
5962–87515	05LX	CY7C261–45WMB
5962–87515	053X	CY7C261–45QMB
5962–87515	06KX	CY7C261–55TMB
5962–87515	06LX	CY7C261–55WMB
5962–87515	063X	CY7C261–55QMB
5962–90803	01MKX	CY7C261–55KMB
5962–90803	01MLX	CY7C261–55DMB
5962–90803	01M3X	CY7C261–55LMB
5962–90803	02MKX	CY7C261–45KMB
5962–90803	02MLX	CY7C261–45DMB
5962–90803	02M3X	CY7C261-45LMB
5962–90803	03MKX	CY7C261-35KMB
5962–90803	03MLX	CY7C261-35DMB
5962–90803	03M3X	CY7C261-35LMB
5962–90803	04MKX	CY7C261-25KMB
5962–90803	04MLX	CY7C261-25DMB
5962–90803	04M3X	CY7C261-25LMB
5962–90803	05MJX	CY7C264-55DMB
5962–90803	05MKX	CY7C263-55KMB
5962–90803	05MLX	CY7C263-55DMB
5962–90803	05M3X	CY7C263-55LMB
5962–90803	06MJX	CY7C264-45DMB
5962–90803	06MKX	CY7C263-45KMB
5962–90803	06MLX	CY7C263-45DMB
5962–90803	06M3X	CY7C263-45LMB
5962–90803	07MJX	CY7C264-35DMB
5962–90803	07MKX	CY7C263-35KMB
5962–90803	07MLX	CY7C263-35DMB
5962–90803	07M3X	CY7C263-35LMB
5962–90803	08MJX	CY7C264-25DMB
5962–90803	08MKX	CY7C263-25KMB
5962–90803	08MLX	CY7C263-25DMB
5962–90803	08M3X	CY7C263-25LMB

Document #: 38–00005–I

CYPRESS SEMICONDUCTOR

CY7C265

8K x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed (commercial and military)**
  - **— 15 ns max. set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **On-chip edge-triggered registers**
  - **— Ideal for pipelined microprogrammed systems**
- **EPROM technology**
  - **— 100% programmable**
  - **— Reprogrammable (7C265W)**
- **5V ±10% V_{CC}, commercial and military**
- **Capable of withstanding >2001V static discharge**
- **Slim 28-pin, 300-mil plastic or hermetic DIP**

Functional Description

The CY7C265 is a 8192 x 8 registered PROM. It is organized as 8,192 words by 8 bits wide, and has a pipeline output register. In addition, the device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM and its value is programmed at the time of use.

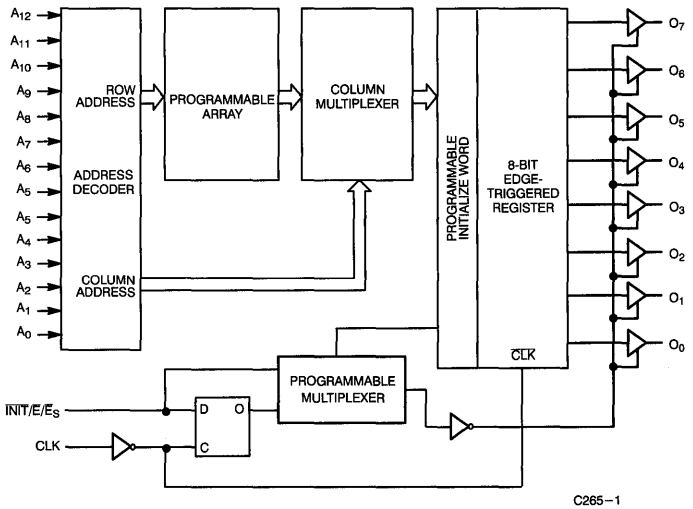
Packaged in 28 pins, the PROM has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/I$ (enable or initialize), and CLOCK.

CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the enable or the initialize function.

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

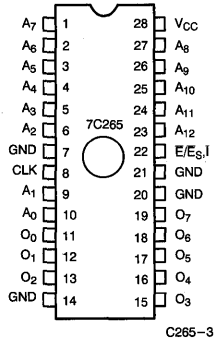
Logic Block Diagram



C265–1

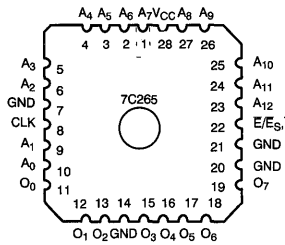
Pin Configurations

DIP/Flatpack
Top View



C265–3

LCC/PLCC (Opaque Only)
Top View



C265–2

Functional Description (continued)

If the $\overline{E}/I$ pin is used for $\overline{INIT}$ (asynchronous), then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences, and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register clear (all outputs LOW). If all the bits of the initialize word are programmed to be a 1, activating $\overline{INIT}$ performs a register preset (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The $\overline{INIT}$ LOW disables clock and must return HIGH to enable clock independent of all other inputs, including the clock.

Selection Guides

		7C265–15	7C265–25	7C265–40	7C265–50
Maximum Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Com'l	120	120	100	80
	Mil	140	140		120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	– 40°C to +85°C	5V ±10%
Military[2]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C265–15, 25 Min.	7C265–15, 25 Max.	7C265–40 Min.	7C265–40 Max.	7C265–50 Min.	7C265–50 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4						V
		V_{CC} = Min., I_{OH} = – 4.0 mA				2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4					V
		V_{CC} = Min., I_{OL} = 12.0 mA					0.4		0.4	
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4					
		V_{CC} = Min., I_{OL} = 8.0 mA					0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+40	–40	+40	–40	+40	µA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100		80	mA
			Mil		140				120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

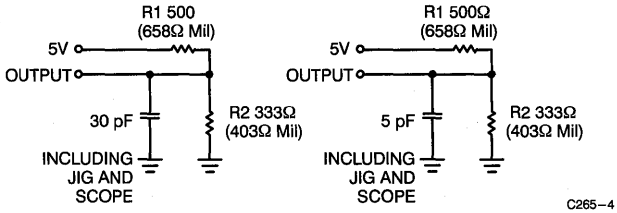
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

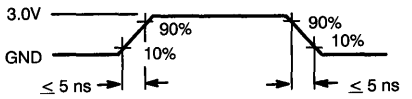
Note:
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

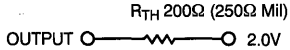
Test Load for −15 through −25 speeds



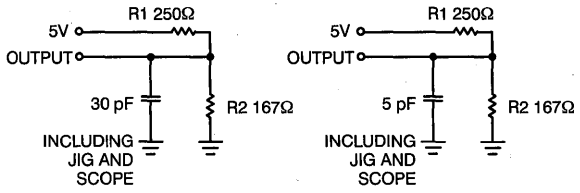
(a) Normal Load **(b) High Z Load**



Equivalent to: THÉVENIN EQUIVALENT

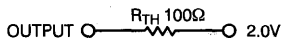


Test Load for −40 through −50 speeds



(c) Normal Load **(d) High Z Load**

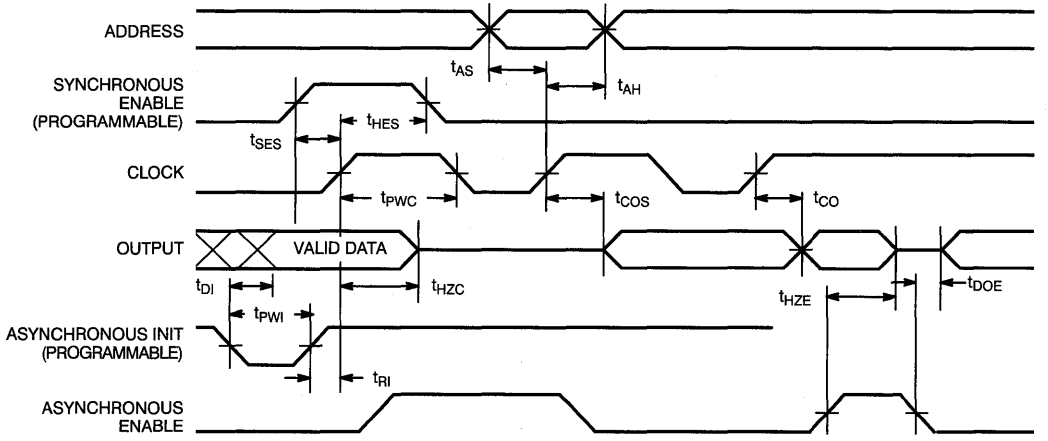
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 5]

Parameter	Description	7C265–15		7C265–25		7C265–40		7C265–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{HA}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PW}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Switching Waveform



C265–7

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity • exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C265 needs to be within one inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	INIT Byte
8193	2001	Control Byte

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

Programming Modes

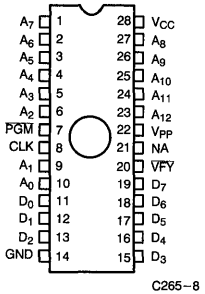
The 7C265 offers a limited selection of programmed architectures. Programming these features should be done with a single 10-ms-wide pulse in place of the intelligent algorithm, mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture, V_{PP} is applied to pins 3, 9, and 22. The choice of a particular mode depends on the states of the other pins during programming, so it is important that the condition of the other pins be met as set forth in the mode table. The considerations that apply with respect to power-up and power-down during intelligent programming also apply during architecture programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{PGM}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

Table 1. Mode Selection

Mode	Read or Output Disable / Other	Pin Function						
	Read or Output Disable	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**
	Other	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}
Program Initialize		V_{ILP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}
Program Initial Byte		A_{12}	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}

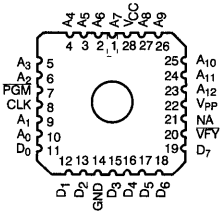
Mode	Read or Output Disable / Other	Pin Function						
	Read or Output Disable	**A_1**	**A_0**	**GND**	**CLK**	**GND**	**$\overline{E}, \overline{I}$**	**$O_7 - O_0$**
	Other	**A_1**	**A_0**	**$\overline{PGM}$**	**CLK**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Asynchronous Enable Read		A_1	A_0	V_{IL}	V_{IL}	GND	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_1	A_0	V_{IL}	V_{IL}/V_{IH}	GND	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_1	A_0	V_{IL}	V_{IL}	GND	V_{IL}	$O_7 - O_0$
Program Memory		A_1	A_0	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_1	A_0	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_1	A_0	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$

DIP/Flatpack



C265-8

LCC/PLCC (Opaque Only)



C265-9

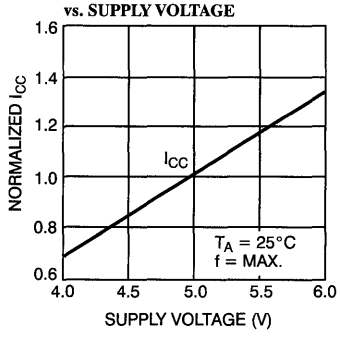
Figure 1. Programming Pinout

Programming Information

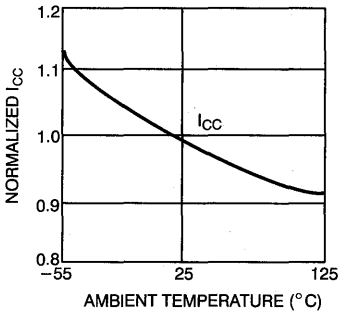
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics

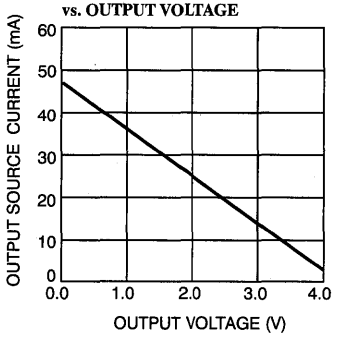
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



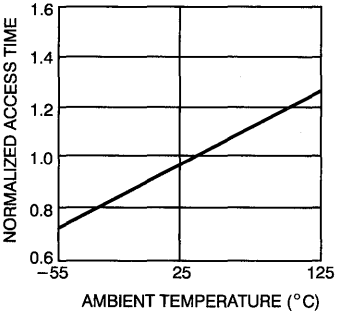
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



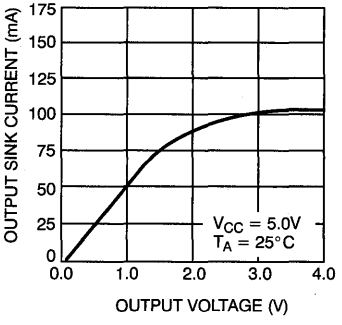
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



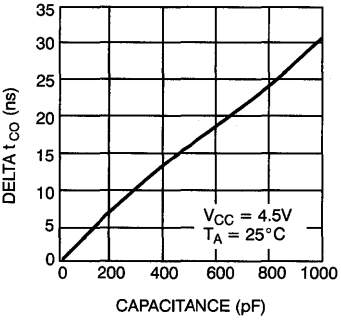
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



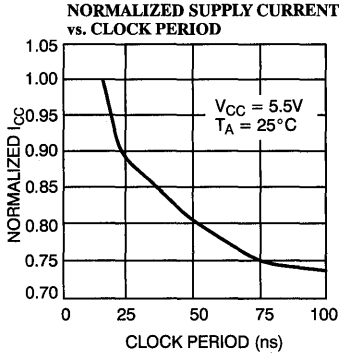
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



Typical DC and AC Characteristics (continued)



Ordering Information[6]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C265–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–15PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–15LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C265–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–25PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	100	CY7C265–40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C265–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C265–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Notes:
6. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Document #: 38–00084–E

CYPRESS SEMICONDUCTOR

CY7C266

8K x 8 PROM Power-Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for 27C64 EPROMs**

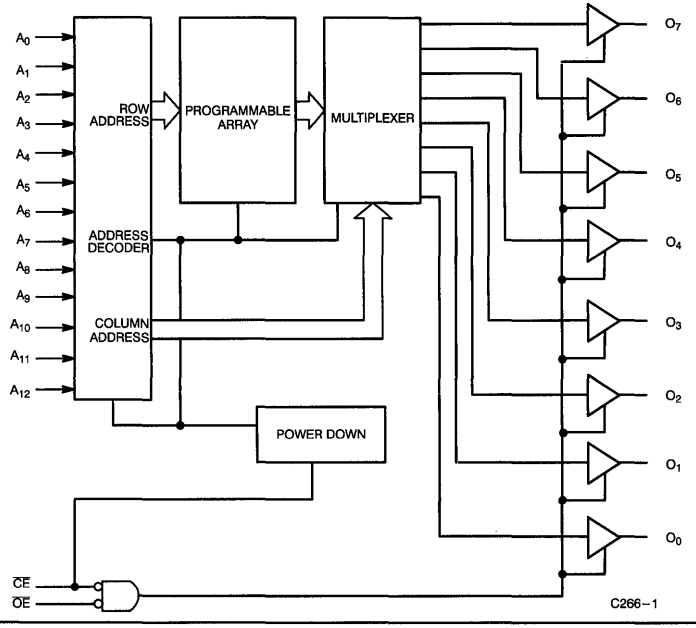
Functional Description

The CY7C266 is a high-performance 8192 word by 8 bit CMOS PROM. When deselected, the CY7C266 automatically powers down into a low-power standby mode. It is packaged in a 600-mil-wide package. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

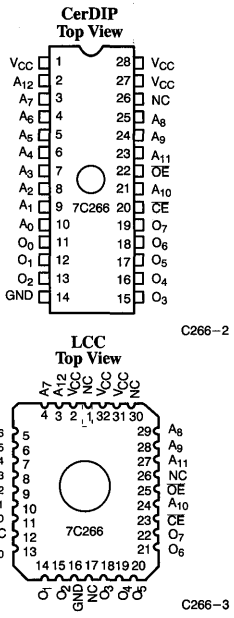
The CY7C266 is a plug-in replacement for EPROM devices. The EPROM cell requires only 12.5V for the super voltage and low-current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 through A_{12}) will become available on the output lines (O_0 through O_7).

Logic Block Diagram



Pin Configurations



Selection Guide

		7C266–20	7C266–25	7C266–35	7C266–45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating Current (mA)	Commercial	120	120	100	100
	Military		140		120
Maximum Standby Current (mA)	Commercial	15	15	15	15
	Military		15		15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C266−20 Min.	7C266−20 Max.	7C266−25 Min.	7C266−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA	Com'l	2.4		2.4		V
			Mil			2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil				0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	− 10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		− 40	+40	− 40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	− 20	− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA	Com'l		120		120	mA
			Mil				140	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE}$ ≥ V_{IH}, I_{OUT} = 0 mA	Com'l		15		15	mA
			Mil				15	

Notes:

1. Contact a Cypress representative regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3, 4] (continued)

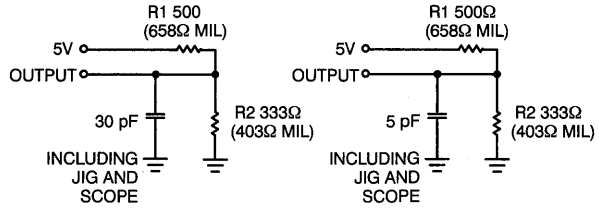
Parameter	Description	Test Conditions		7C266–35 Min.	7C266–35 Max.	7C266–45 Min.	7C266–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$		– 10	+10	– 10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled		– 10	+10	– 10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		– 20	– 90	– 20	– 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA	Com'l		100		100	mA
			Mil				120	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE} \ge V_{IH}$, I_{OUT} = 0 mA	Com'l		15		15	mA
			Mil				15	

Capacitance[4]

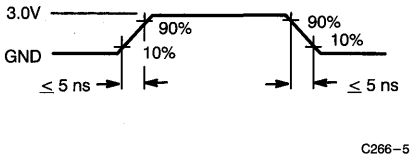
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms

Test Load for −20 through −25 speeds

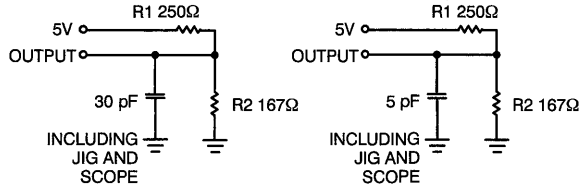


(a) **Normal Load** (b) **High Z Load** C266−4



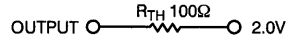
Equivalent to: THEVENIN EQUIVALENT

Test Load for −35 through −55 speeds



(c) **Normal Load** (d) **High Z Load** C266−6

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[1, 2, 4]

Parameter	Description	7C266−20		7C266−25		7C266−35		7C266−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45	ns
t_{HZCE}	Chip Enable Inactive to High Z		25		30		40		45	ns
t_{HZOE}	Output Enable Inactive to High Z		12		12		20		25	ns
t_{AOE}	Output Enable Active to Output Valid		12		12		20		25	ns
t_{ACE}	Chip Enable Active to Output Valid		25		30		40		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{PU}	Chip Enable Active to Power-Up		25		30		40		45	ns
t_{PD}	Chip Enable Inactive to Power-Down		25		30		40		45	ns

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C266 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[6, 7]							
	Normal Operation	**A_8**	**A_9**	**A_{10}**	**A_{11}**	**A_{12}**	**$\overline{CE}$**	**$\overline{OE}$**	**$D_7 - D_0$**
	Program	**$\overline{VFY}$**	**$\overline{PGM}$**	**LAT**	**NA**	**NA**	**$\overline{CE}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IL}	$O_7 - O_0$
Standby		X	X	X	X	X	V_{IH}	X	Three-Stated
Output Disable		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IH}	Three-Stated
Program		V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	Three-Stated
Blank Check		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:

6. X = "don't care" but must not exceed V_{CC} + 5%.
7. Address $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in Programming modes.

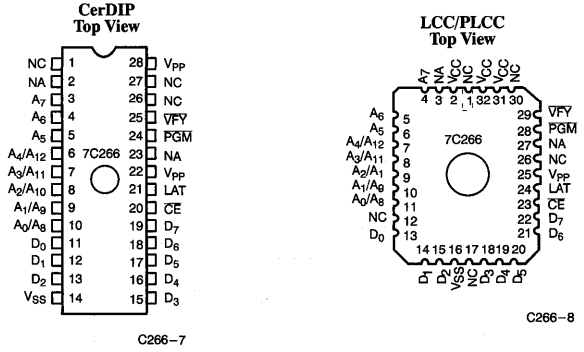
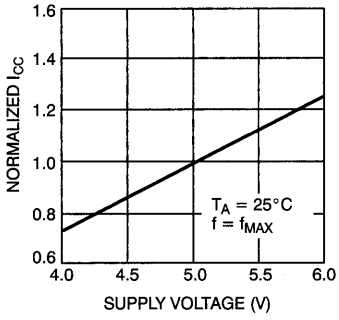


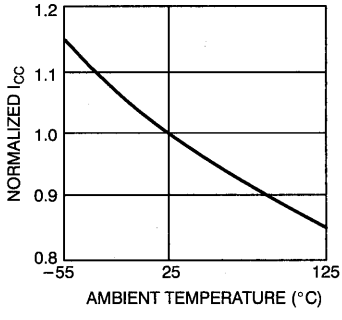
Figure 1. Programming Pinout

Typical DC and AC Characteristics

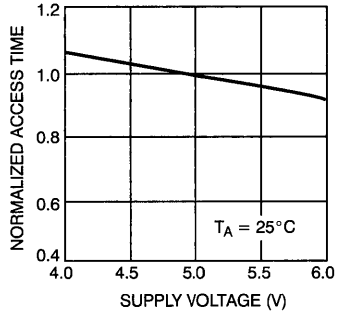
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



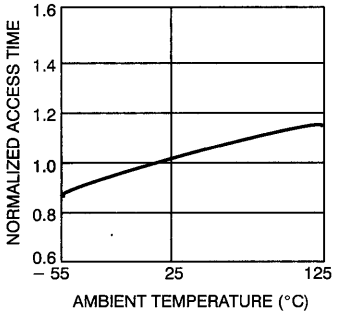
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



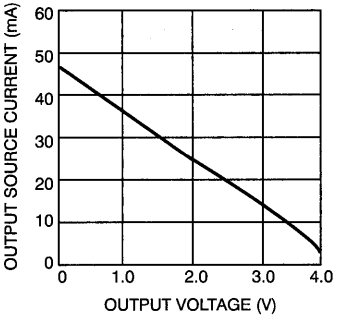
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



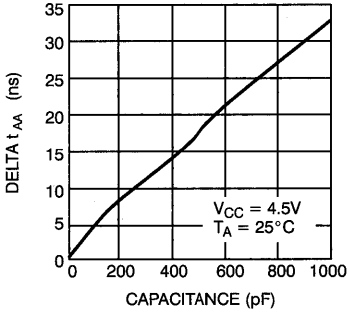
NORMALIZED ACCESS TIME vs. TEMPERATURE



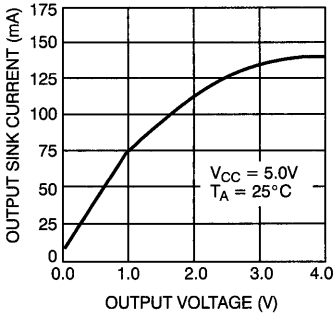
OUTPUT SOURCE CURRENT vs. VOLTAGE



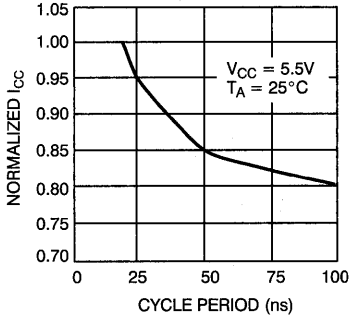
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C266–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–20WC	W16	28-Lead (600-Mil) Windowed CerDIP	
25	CY7C266–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–25WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266–25QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266–25WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
35	CY7C266–35PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
45	CY7C266–45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{AOE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Note:

8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Document #: 38–00086–D

8K x 8 Registered Diagnostic PROM

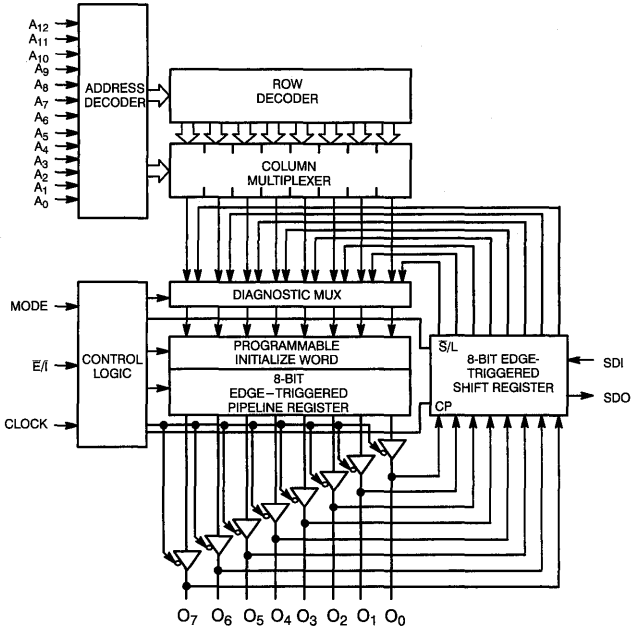
Features

- CMOS for optimum speed/power
- High speed (commercial and military)
  - 15-ns max set-up
  - 12-ns clock to output
- Low power
  - 660 mW (commercial)
  - 770 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register
  - For serial observability and controllability of the output register
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C269W)
- 5V ±10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 300-mil, 28-pin plastic or hermetic DIP

Functional Description

The CY7C269 is a 8K x 8 registered diagnostic PROM. It is organized as 8,192 words by 8 bits wide, and has both a pipeline output register and an onboard diagnostic shift register. The device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM, and may be programmed to any desired value.

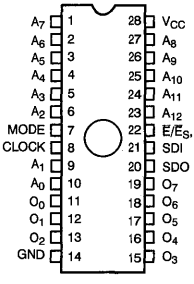
Logic Block Diagram



C269-1

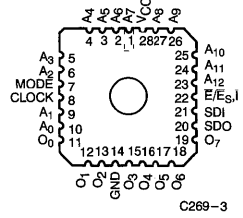
Pin Configurations

CerDIP/Flatpack
Top View



C269-2

LCC/PLCC (Opaque Only)
Top View



C269-3

Selection Guide

		7C269-15	7C269-25	7C269-40	7C269-50
Maximum Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	120	120	100	80
	Military	140	140		120

Functional Description (continued)

The CY7C269 is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, it has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/I$ (Enable or Initialize), and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SDI (shift in), and SDO (shift out). Normal pipelined operation and diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the $\overline{E}/I$ pin is used for a $\overline{INIT}$ (asynchronous initialize) function, the outputs are permanently enabled and the initialize word is loaded into the pipeline register on a HIGH to LOW transition of the $\overline{INIT}$ signal. The $\overline{INIT}$ LOW disables CLOCK and must return high to re-enable CLOCK. If the $\overline{E}/I$ pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The $\overline{E}/I$ signal becomes a secondary mode signal designating whether to shift the diagnostic shift register or to load either the diagnostic register or the pipeline register. If $\overline{E}/I$ is HIGH, it shifts SDI into the least-significant location of the diagnostic register and all bits one location toward the most-significant location on each rising edge. The contents of the most-significant location in the diagnostic register are available on the SDO pin.

If the $\overline{E}/I$ signal is LOW, SDI becomes a direction signal, transferring the contents of the diagnostic register into the pipeline register when SDI is LOW. When SDI is HIGH, the contents of the output pins are transferred into the diagnostic register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the outputs are enabled, the contents of the pipeline register are transferred into the diagnostic register. If the outputs are disabled, an external source of data may be loaded into the diagnostic register. In this condition, the SDO signal is internally driven to be the same as the SDI signal, thus propagating the "direction of transfer information" to the next device in the string.

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	− 40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C269–15, 25		7C269–40		7C269–50		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4						V
		V_{CC} = Min., I_{OH} = −4.0 mA				2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4					V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4					
		V_{CC} = Min., I_{OL} = 12.0 mA	Com'l				0.4		0.4	V
		V_{CC} = Min., I_{OL} = 8.0 mA	Mil				0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	μA
I_{OS}[5]	Output Short Circuit Current				90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100		80	mA
			Mil		140				120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Capacitance[4,6]

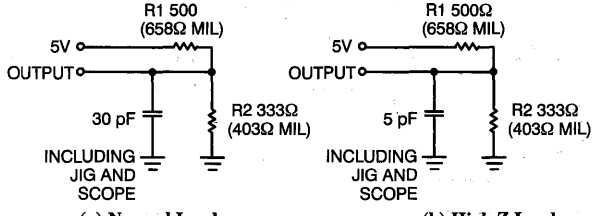
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

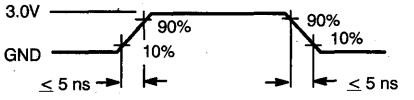
AC Test Loads and Waveforms

Test Load for −15 through −25 speeds



(a) Normal Load (b) High Z Load

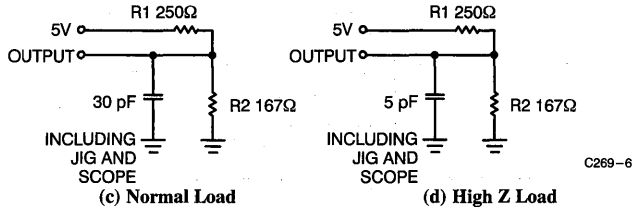
C269-4



C269-5

Equivalent to: THEVENIN EQUIVALENT

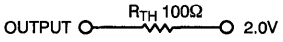
Test Load for −40 through −50 speeds



(c) Normal Load (d) High Z Load

C269-6

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3,4]

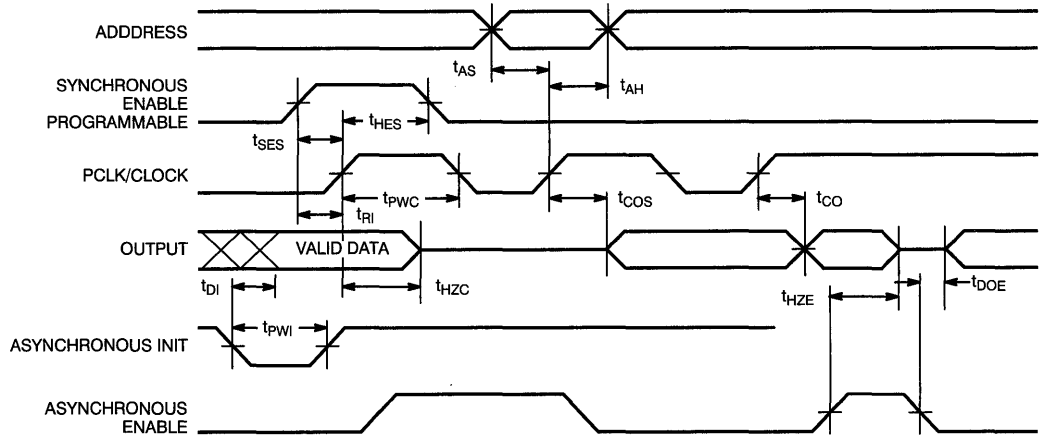
Parameter	Description	7C269−15		7C269−25		7C269−40		7C269−50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{AH}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PW}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Out Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Asynch. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Diagnostic Mode Switching Characteristics Over the Operating Range[3,4]

Parameter	Description		7C269–15		7C269–25		7C269–40,50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SSDI}	Set-Up SDI to Clock	Com'l	20		25		30		ns
		Mil	25		30		35		
t_{HSDI}	SDI Hold from Clock	Com'l	0		0		0		ns
		Mil	0		0		0		
t_{DSDO}	SDO Delay from Clock	Com'l		20		25		30	ns
		Mil		25		30		40	
t_{DCL}	Minimum Clock LOW	Com'l	20		25		25		ns
		Mil	25		25		25		
t_{DCH}	Minimum Clock HIGH	Com'l	20		25		25		ns
		Mil	25		25		25		
t_{SM}	Set-Up to Mode Change	Com'l	20		25		25		ns
		Mil	25		30		30		
t_{HM}	Hold from Mode Change	Com'l	0		0		0		ns
		Mil	0		0		0		
t_{MS}	Mode to SDO	Com'l		20		25		25	ns
		Mil		25		30		30	
t_{SS}	SDI to SDO	Com'l		30		40		40	ns
		Mil		35		40		45	
t_{SO}	Data Set-Up to DCLK	Com'l	20		25		25		ns
		Mil	25		30		30		
t_{HO}	Data Hold from DCLK	Com'l	10		10		10		ns
		Mil	13		13		15		

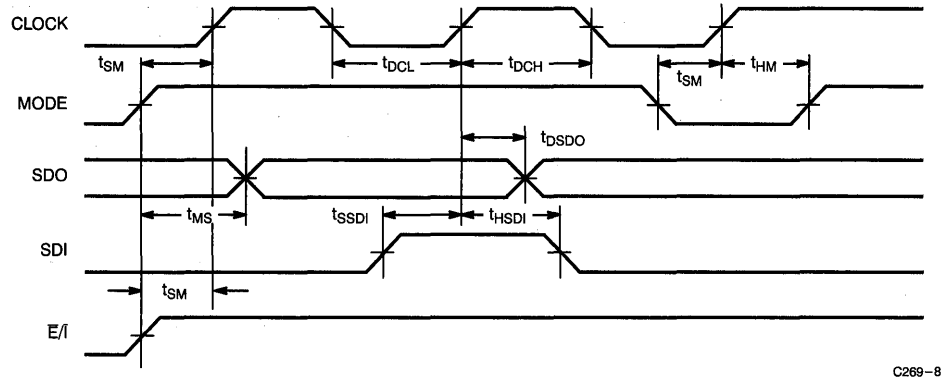
Switching Waveforms[3,4]

Pipeline Operation (Mode = 0)

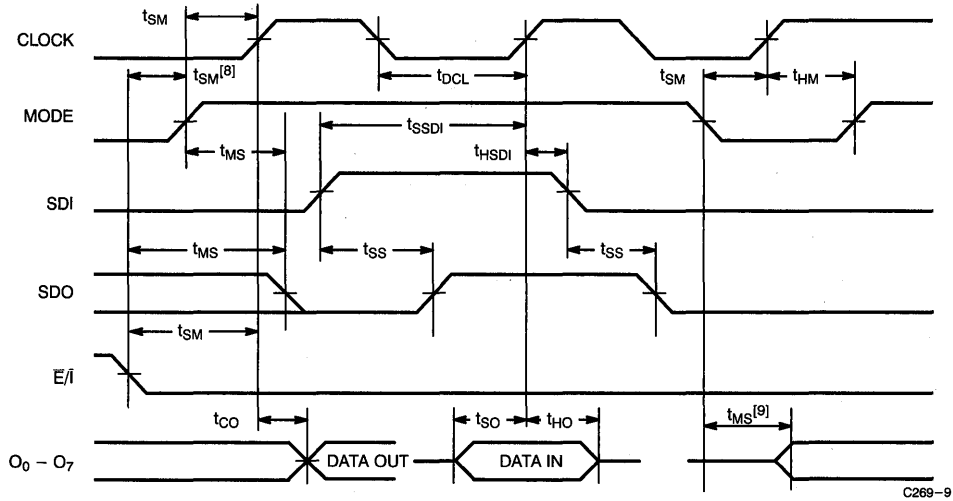


C269–7

Diagnostic Application (Shifting the Shadow Register[7])



Diagnostic Application (Parallel Data Transfer)



Notes:

7. Diagnostic register = shadow register = shift register.
8. Asynchronous enable mode only.
9. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H ⏵ L) then the output impedance change delay is t_{MS}.

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	Init Byte
8193	2001	Control Byte

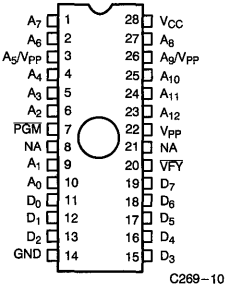
Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

CerDIP/Flatpack



LCC/PLCC (Opaque Only)

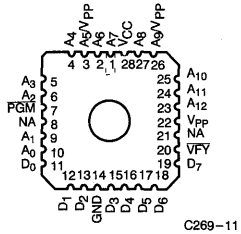


Figure 1. Programming Pinouts

Mode Selection

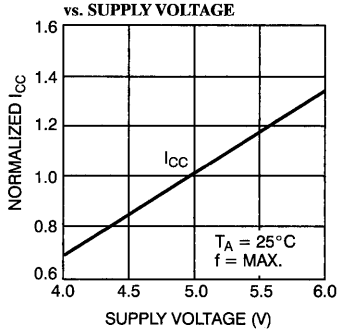
Mode	Read or Output Disable / Other	Pin Function[10]							
	Read or Output Disable	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**	**A_1**
	Other	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**	**A_1**
Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load SR to PR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load Output to SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Shift SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}	A_1
Program Initialize		V_{ILP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	A_1
Program Initial Byte		A_{12}	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	A_1

Mode	Read or Output Disable / Other	Pin Function[10]						
	Read or Output Disable	**A_0**	**MODE**	**CLK**	**SDI**	**SDO**	**$\overline{E}, \overline{I}$**	**$O_7 - O_0$**
	Other	**A_0**	**$\overline{PGM}$**	**CLK**	**NA**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Load SR to PR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IL}	SDI	V_{IL}	$O_7 - O_0$
Load Output to SR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IH}	SDI	V_{IL}	$O_7 - O_0$
Shift SR		A_0	V_{IH}	V_{IL}/V_{IH}	D_{IN}	SDO	V_{IH}	$O_7 - O_0$
Asynchronous Enable Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Program Memory		A_0	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_0	V_{IHP}	V_{ILP}	X	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_0	V_{IHP}	V_{ILP}	X	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{IHP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$

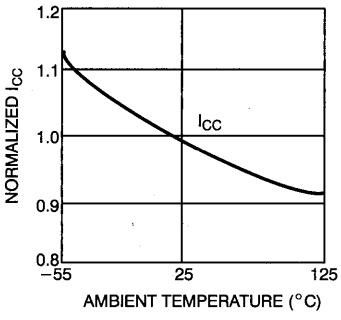
Note:
10. X = "don't care" but not to exceed V_{CC} + 5%.

Typical DC and AC Characteristics

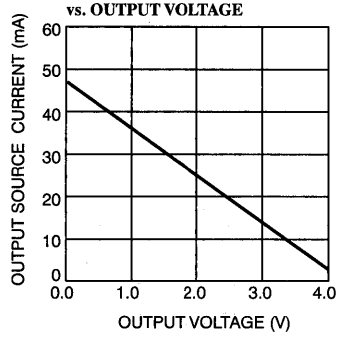
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



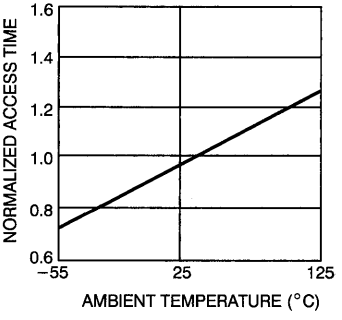
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



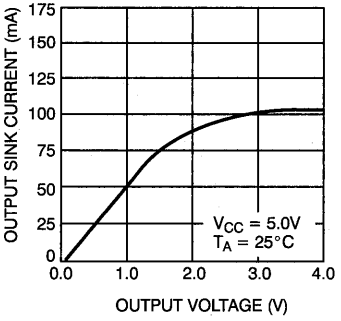
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



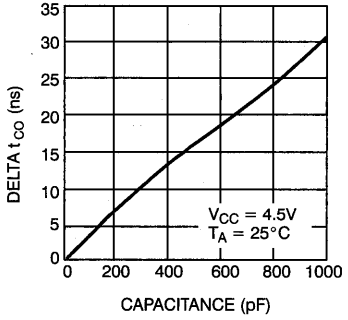
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



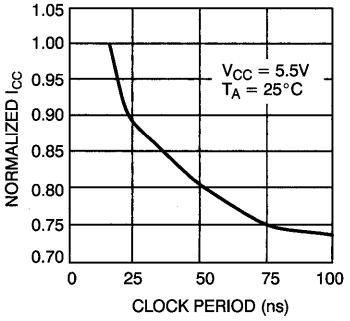
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



Ordering Information[11]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C269–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–15PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C269–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–15LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
25	140	CY7C269–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–25PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C269–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	100	CY7C269–40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C269–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C269–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Note:
11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t_{SSDI}	7, 8, 9, 10, 11
t_{HSDI}	7, 8, 9, 10, 11
t_{DSDO}	7, 8, 9, 10, 11
t_{DCL}	7, 8, 9, 10, 11
t_{DCH}	7, 8, 9, 10, 11
t_{HM}	7, 8, 9, 10, 11
t_{MS}	7, 8, 9, 10, 11
t_{SS}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

CY7C270

Reprogrammable 16K x 16 Processor-Intelligent PROM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed (for commercial and military)**
  - **— 25-ns single access time**
  - **— 11-ns burst access time**
- **16-bit-wide words**
- **Input address registered, latched, or transparent**
- **On-chip programmable burst logic**
- **Programmable compatibility with many common microprocessors**
- **Three programmable chip selects**
- **Programmable output enable**
- **44-pin PLCC and 44-pin LCC packages**
- **100% reprogrammable in windowed packages**
- **TTL-compatible I/O**
- **Capable of withstanding greater than 2001V static discharge**

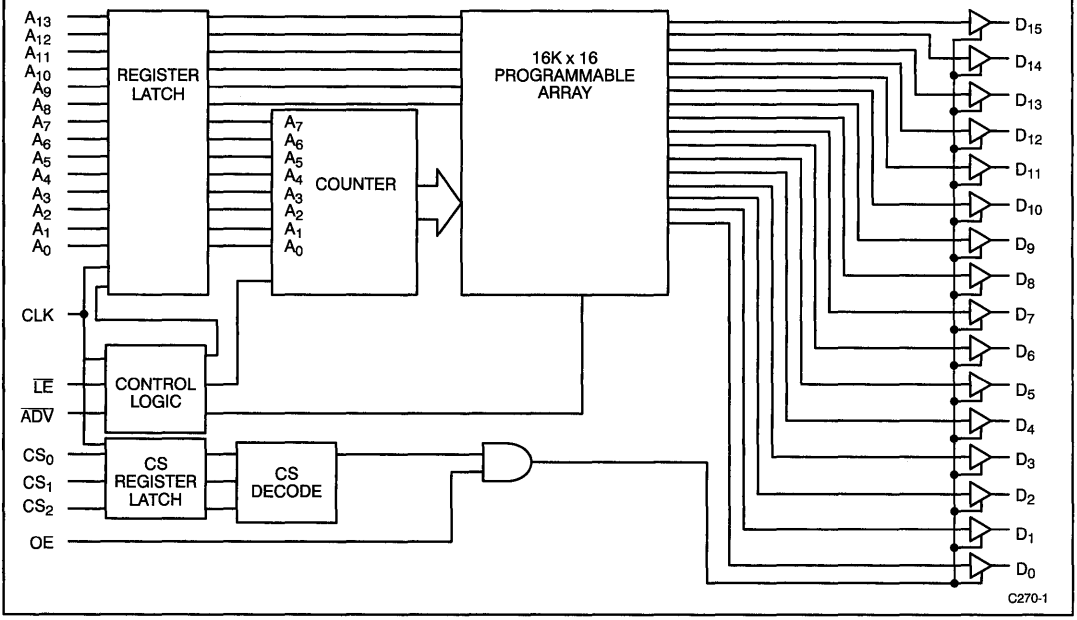
Functional Description

The CY7C270 is a 16K-word by 16-bit PROM designed to support a number of popular microprocessors with little or no "glue" logic. This PROM is packaged in a 44-pin PLCC package and a 44-pin LCC package. The CY7C270 is available in windowed packages for 100% reprogrammability. The memory cells utilize proven EPROM floating-gate technology.

The CY7C270 offers a number of programmable features that allow the user to configure the PROM for use with their chosen microprocessor. The programmable features include a choice between registered and latched modes of operation. The CY7C270 also has an on-board programmable counter for burst reads. The user may select a 2-bit, 4-bit, or 8-bit linear counter, or program the PROM to use the Intel 80486 burst pattern (*Table 2*). A separate control input ($\overline{ADV}$) is used to choose between single reads and bursts. In addition, the burst counter and latch may be bypassed for asynchronous operation to be used with DSP processors.

The CY7C270 allows the user to independently program the polarity of each chip select ($CS_2 - CS_0$). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin ($\overline{OE}$) is also programmable.

Logic Block Diagram

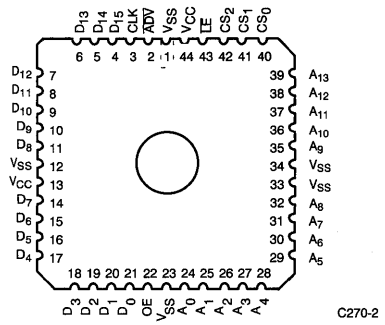


Selection Guide

		CY7C270–15	CY7C270–20	CY7C270–30
Minimum Clock Period (ns)		15	20	30
Maximum Operating Current (mA)	Commercial	175	175	175
	Military	200	200	200

Pin Configuration

LCC/PLCC (Opaque Only)
Top View



C270-2

Operating Modes

The CY7C270 can be specifically configured for use with many popular microprocessors. The PROM configuration for some of these processors is detailed in *Table 1*. Note that many of the processors can use either registered or latched mode depending on their speed.

Table 1. Processor-Intelligent PROM Configuration

Processor	Registered/Latched	Burst Counter
SPARC	Registered	—
Intel 486	Latched	Table Logic[1]
80386	Latched	—
Motorola 68040	Latched	2-Bit Counter
Motorola 68030	Latched	2-Bit Counter
Intel 80960KB	Registered	2-Bit Counter
Intel 80960CA	Latched	2-Bit Counter
AMD 29000	Latched	8-Bit Counter
MIPS R3000	Registered	—
MIPS R2000	Registered	—
Motorola 88000	Registered	—

Note:

1. The Intel 486 uses a non-sequential burst. The CY7C270 is equipped with a look-up table (described in *Table 2*) for use with this processor.

Single Read Access in Registered Mode

A read access is initiated in registered mode on the rising edge of CLK if all three chip selects are asserted and $\overline{LE}$ is sampled LOW. The address applied to the input is stored in a register and is delivered to both the PROM core and the counter. The contents of the memory location accessed by the original address are delivered to the outputs. When $\overline{LE}$ is asserted the system ignores the advance enable ($\overline{ADV}$) input.

Single Read Access in Latched Mode

In latched mode, the CY7C270 can take advantage of situations where the address is available well before the rising edge of CLK. A read is initiated when the latch is opened (on the falling edge of $\overline{LE}$). The address is sent directly to the PROM core and to the counter. The contents of the memory location addressed by the original address are delivered to the outputs. The latch is closed when $\overline{LE}$ is deasserted.

Burst Sequence

During a burst, the first read is initiated as a single access read. After the initial read, the $\overline{LE}$ input is held inactive. The advance enable input ($\overline{ADV}$) controls the address sequencing starting with the second read. $\overline{ADV}$ is sampled on the rising edge of the CLK input. If $\overline{ADV}$ is sampled LOW, the address is incremented to the next location. The number of address bits incremented by the counter is programmed by the user. The counter wraps around after reaching the maximum count without affecting other bits in the address.

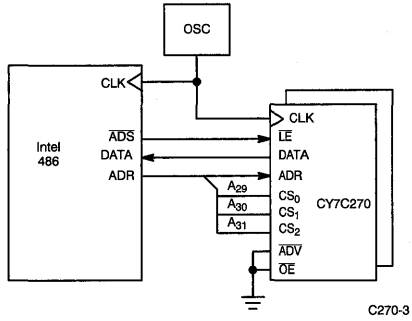
Special burst advancement logic is included in the CY7C270 to support the Intel 80486 burst operation. The 80486 bursts in the non-sequential pattern shown in *Table 2*.

Some processors have the capability to suspend a burst. In order to suspend a burst in the CY7C270 the processor must simply deassert the $\overline{ADV}$ input. When the $\overline{ADV}$ input is reasserted the burst will continue from where it left off. It is not necessary for the processor to send a new address to the PROM.

Table 2. Look-Up Table for Use with Intel 486

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

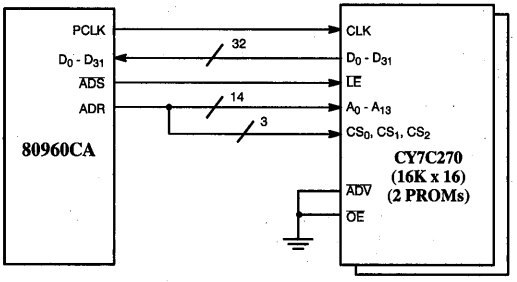
Application Example 1



C270-3

80486 Instruction Memory Using Two CY7C270s

Application Example 2



Intel 80960CA Using Two CY7C270s

Pin Definitions

Signal Name	I/O	Description
$A_{13} - A_0$	I	Address Inputs
CLK	I	Clock
$\overline{LE}$	I	Latch Enable
$\overline{ADV}$	I	Advance Enable
$CS_2 - CS_0$	I	Programmable Chip Selects
OE	I	Programmable Output Enable
$D_{15} - D_0$	O	Data Outputs
V_{CC}	–	Power Supply
V_{SS}	–	Ground

Pin Descriptions

Input Signals

$A_{13} - A_0$ (Address lines). The address inputs are stored in a register at the rising edge of CLK if the device is programmed in registered mode. If the device is programmed in latched mode, the address inputs flow into the PROM while $\overline{LE}$ is active and are captured at the rising edge of $\overline{LE}$. For asynchronous operation, the device should be programmed in the latch mode with $\overline{LE}$ tied LOW.

CLK (Clock line). The clock is used to sample the $\overline{ADV}$ input. In registered mode, the clock is also used to sample $\overline{LE}$, $CS_2 - CS_0$, and the address.

$\overline{LE}$ (Latch Enable). In registered mode, this input is sampled on the rising edge of CLK. If it is active, the address and chip selects are stored in a register. In latched mode, the address and chip selects are latched on the rising edge of this signal.

$\overline{ADV}$ (Advance Enable). This signal is used for burst reads. If $\overline{LE}$ is inactive, $\overline{ADV}$ is sampled on the rising edge of CLK. If $\overline{ADV}$ is LOW, the counter will be incremented and the next address will be delivered to the PROM core. $\overline{ADV}$ should be tied HIGH, and in the programming mode, the burst enable (BE) should be disabled for asynchronous operation.

$CS_2 - CS_0$ (Synchronous Chip Selects). The polarity of each chip select is programmed by the user. The inputs from these pins are stored in a register on the rising edge of CLK in registered mode. In latched mode, the inputs are latched on the rising edge of $\overline{LE}$. All three chip selects must be active in order to select the device.

OE (Asynchronous Output Enable). The polarity of this pin is programmable. The outputs are active when OE is asserted and tri-stated when OE is deasserted.

Output Signals

$D_{15} - D_0$ (Data Outputs). Data from the array location addressed on inputs $A_{13} - A_0$ will appear on these pins. The outputs will be tri-stated if OE is deasserted or if the chip is not selected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[2]	– 40°C to +85°C	5V ±10%
Military[3]	– 55°C to +125°C	5V ±10%

Notes:

2. Contact a Cypress representative for industrial temperature range specifications.
3. T_A is the "instant on" case temperature.

Electrical Characteristics[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 4				μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		− 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		− 20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		175	mA
			Military		200	mA

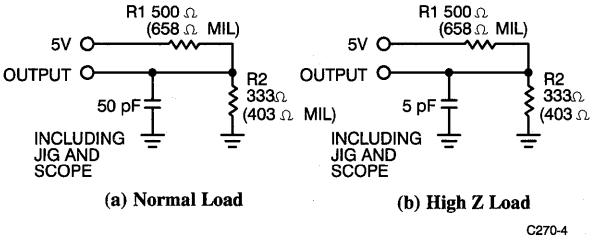
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. See the last page of this specification for Group A subgroup testing information.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms



(a) Normal Load (b) High Z Load

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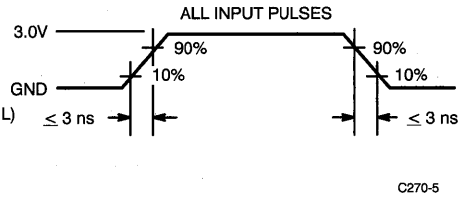
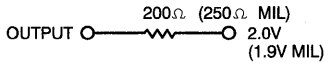


C270-5

Equivalent to: THÉVENIN EQUIVALENT



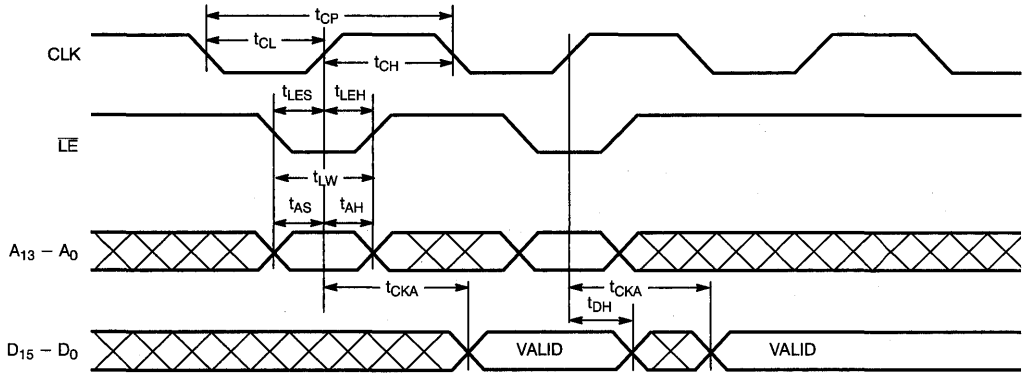
C270-6

Switching Characteristics Over the Operating Range[5]

Parameter	Description	Commercial and Military						Unit
		CY7C270–15		CY7C270–20		CY7C270–30		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	15		20		30		ns
t_{CH}	Clock HIGH Pulse Width	6		8		13		ns
t_{CL}	Clock LOW Pulse Width	6		8		13		ns
t_{AS}	Address Set-Up to CLK Rise	3		4		4		ns
t_{AH}	Address Hold from CLK Rise	2		3		4		ns
t_{LES}	$\overline{LE}$ Set-Up to CLK Rise	3		4		4		ns
t_{LEH}	$\overline{LE}$ Hold from CLK Rise	2		3		4		ns
t_{LW}	Latch Pulse Width	7		10		12		ns
t_{ADVS}	$\overline{ADV}$ Set-Up to CLK Rise	3		4		4		ns
t_{ADVH}	$\overline{ADV}$ Hold from CLK Rise	2		3		4		ns
t_{ASL}	Address Set-Up to Latch Close	3		4		4		ns
t_{AHL}	Address Hold from Latch Close	2		3		4		ns
t_{DH}	Data Hold	3		3		3		ns
t_{AA}	Address to Data for Single Read		25		28		35	ns
t_{LEA}	$\overline{LE}$ Low to Data Valid for Single Read		25		28		35	ns
t_{CKA}	Clock to Data for Single Read		25		28		35	ns
t_{CKB}	CLK Rise to Data for Burst Read		11		12		15	ns
t_{CSS}	CS Set-Up to CLK Rise	3		4		4		ns
t_{CSH}	CS Hold from CLK Rise	2		3		4		ns
t_{COV}	CLK Rise to Output Valid		11		12		15	ns
t_{COZ}	CLK Rise to High Z Output		11		12		15	ns
t_{CSOV}	CS Asserted to Output Valid		13		15		18	ns
t_{CSOZ}	CS Deasserted to High Z Output		13		15		18	ns
t_{CSSL}	CS Set-Up to Latch Close	3		4		4		ns
t_{CSHL}	CS Hold from Latch Close	2		3		4		ns
t_{LOV}	Latch Open to Output Valid		13		15		18	ns
t_{LOZ}	Latch Open to High Z Output		13		15		18	ns
t_{OEV}	OE Asserted to Output Valid		11		12		15	ns
t_{OEZ}	OE Deasserted to High Z Output		11		12		15	ns

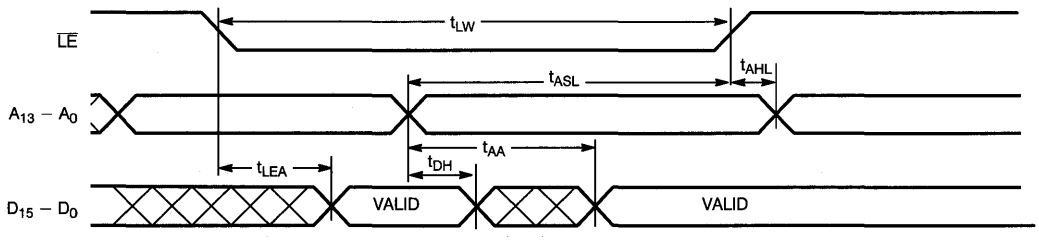
Switching Waveforms

Single Reads – Registered Mode[7, 8]



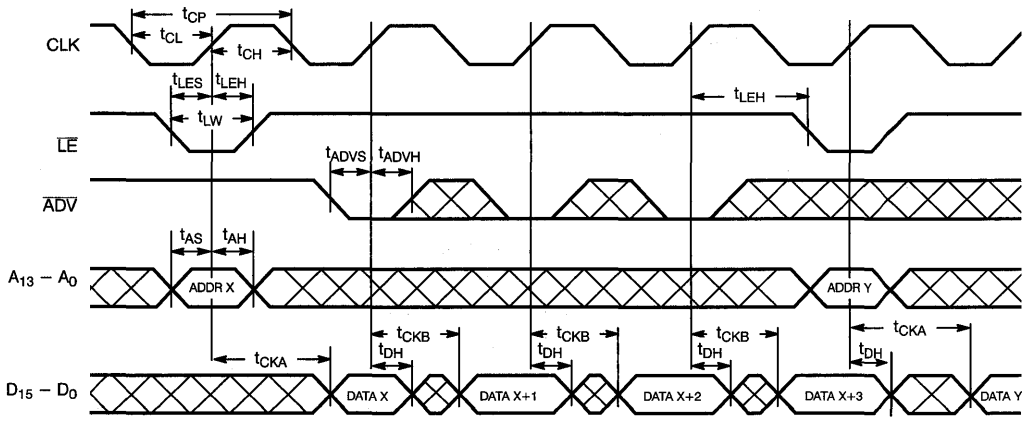
C270-7

Single Reads – Latched Mode[8]



C270-8

4-Word Burst Followed by Single Read – Registered Mode[8]



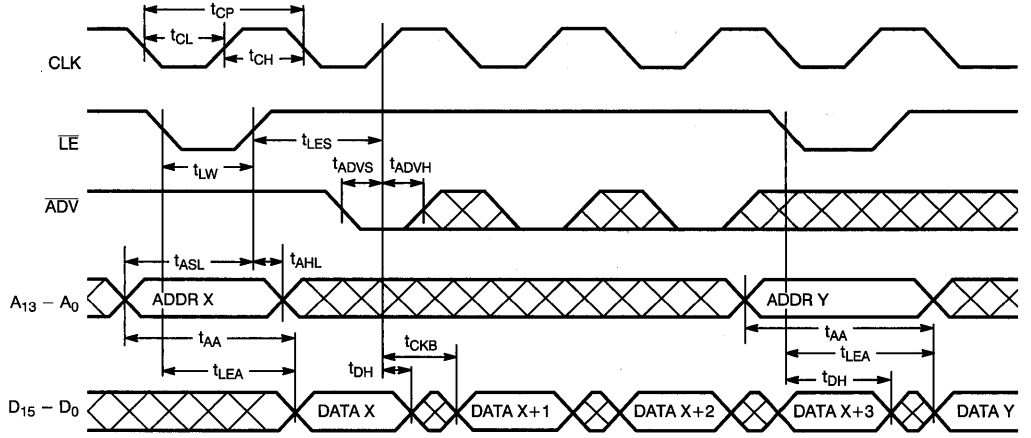
C270-9

Notes:

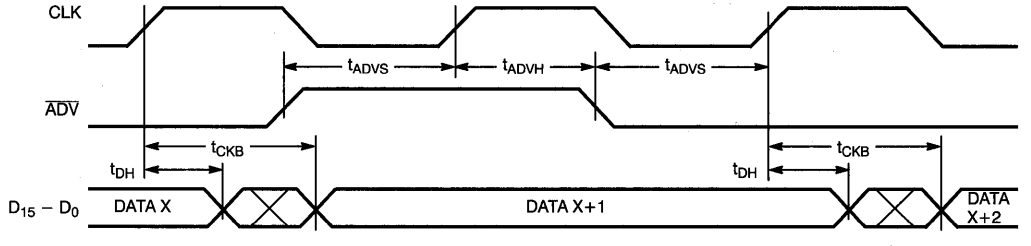
7. $\overline{ADV}$ is assumed HIGH.
8. $CS_2 - CS_0$, OE are assumed active.

Switching Waveforms (continued)

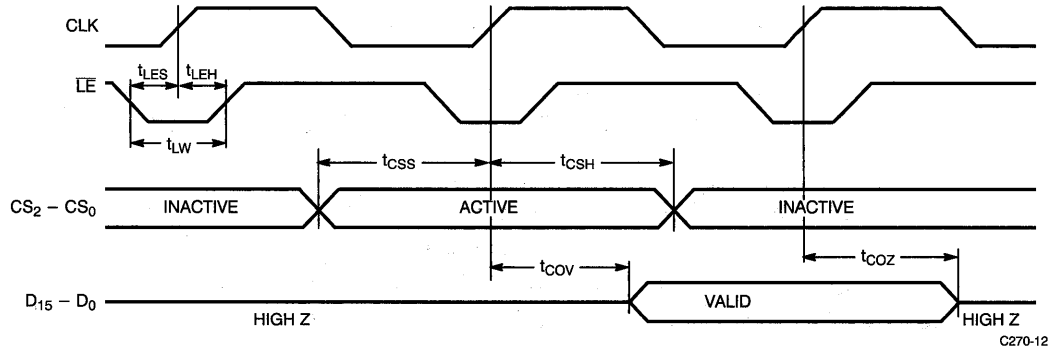
4-Word Burst Followed by Single Read – Latched Mode[8]



Suspended Burst[8, 9]



Output Controlled by CS and CLK – Registered Mode[10]

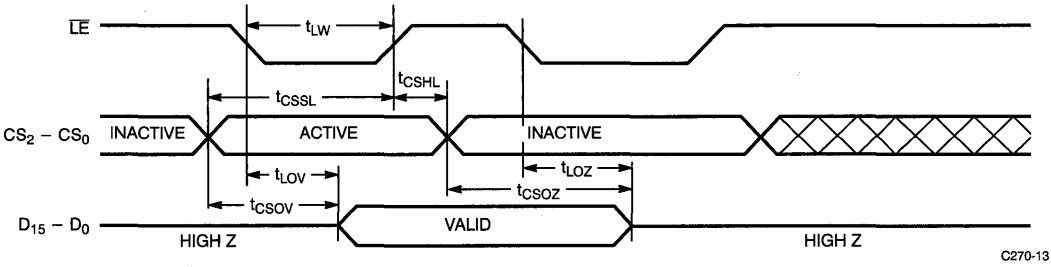


Notes:

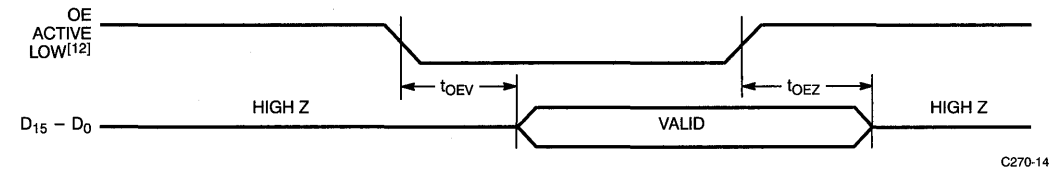
9. Burst in progress.
10. OE assumed active.

Switching Waveforms (continued)

Outputs Controlled by CS and $\overline{LE}$ – Latched Mode



Outputs Controlled by OE[11]



Notes:
11. $CS_2 - CS_0$ are assumed active.
12. OE active HIGH is a programmable option.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C270. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure of ultraviolet light is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C270 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Architecture Configuration Bits

The CY7C270 is configured by programming the Control Word located at the end of the programmable array (4000H). *Table 3* gives the specific information for configuring the architecture.

To use the CY7C270 as a purely asynchronous PROM, tie the $\overline{ADV}$ signal to V_{CC}, the CLK and $\overline{LE}$ signal to V_{SS}, and program the control word for No Burst and Latched mode of operation ($D_3 = 1$, $D_{15} = 0$).

Table 3. Control Word for Architecture Configuration

Control Option	Control Word		Function
	Bit	Programmed Level	
OE Output Enable	D_0	0 = Default 1 = Programmed	OE Active LOW OE Active HIGH
C_1 C_0 (Counter Configuration)	D_2 D_1	00 = Default 01 = Programmed 10 = Programmed 11 = Programmed	486 2-Bit Counter Linear 2-Bit Counter Linear 4-Bit Counter Linear 8-Bit Counter
R/L Registered/Latched	D_3	0 = Default 1 = Programmed	Registered Mode Latched Mode
CS_0 Chip Select 0	D_{12}	0 = Default 1 = Programmed	CS_0 Active LOW CS_0 Active HIGH
CS_1 Chip Select 1	D_{13}	0 = Default 1 = Programmed	CS_1 Active LOW CS_1 Active HIGH
CS_2 Chip Select 2	D_{14}	0 = Default 1 = Programmed	CS_2 Active LOW CS_2 Active HIGH
BE (Burst Enable)	D_{15}	0 = Default 1 = Programmed	No Burst Burst (follow C_1 C_0)

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word

Control Word (4000H – default state is 00H)

D_{15} D_0

BE CS_2 CS_1 CS_0 X X X X X X X X R/L C_1 C_0 OE

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 4. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 5. Configuration Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	Control Word

Table 6. Signature Mode Table

Signature Mode	A_0	A_9	$D_0 - D_{15}$
Cypress Code	V_{ILP}	V_{PP}	0034H
Device Code	V_{IHP}	V_{PP}	0013H

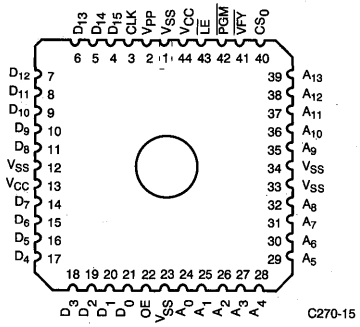
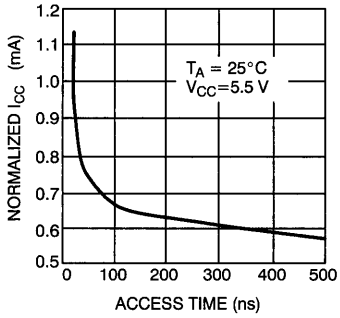


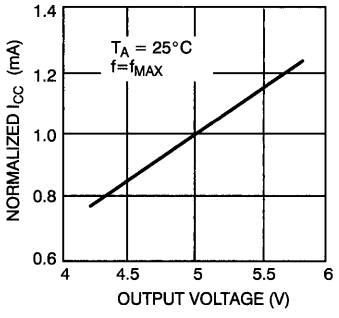
Figure 1. Programming Pinout

Typical DC and AC Characteristics

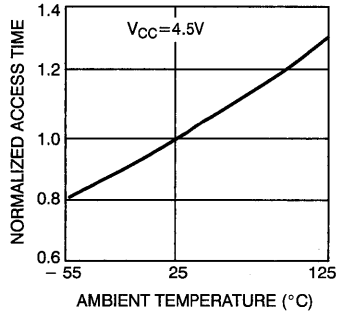
NORMALIZED I_{CC} vs. t_{CKA} CYCLE



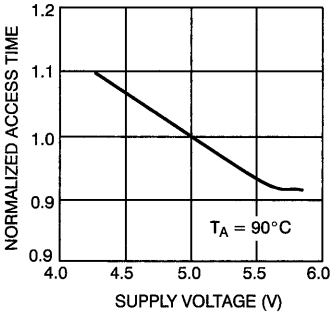
NORMALIZED I_{CC} vs. OUTPUT VOLTAGE



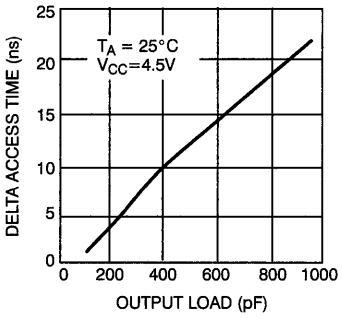
NORMALIZED t_{CKA} vs. TEMPERATURE



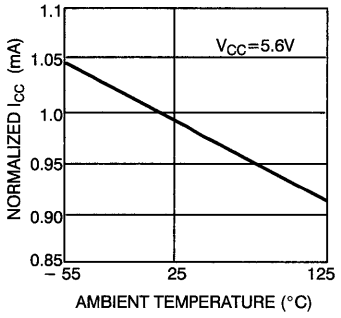
NORMALIZED t_{CKA} vs. SUPPLY VOLTAGE



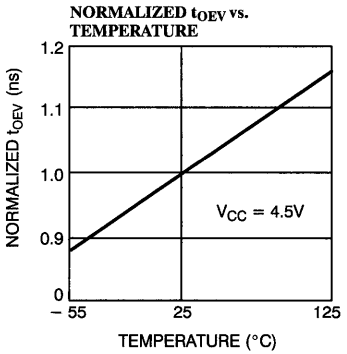
t_{CKA} CHANGE vs. OUTPUT LOADING



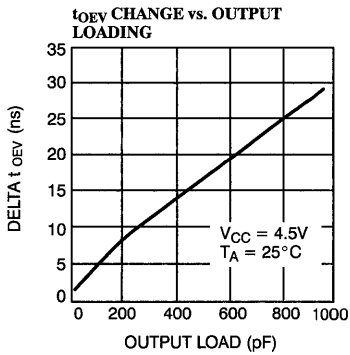
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



NORMALIZED t_{OEV} vs. TEMPERATURE



t_{OEV} CHANGE vs. OUTPUT LOADING



C270-16

Ordering Information[13]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C270–15HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–15JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–15QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
20	CY7C270–20HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–20JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–20HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–20QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C270–30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{LES}	7, 8, 9, 10, 11
t_{LEH}	7, 8, 9, 10, 11
t_{ADVS}	7, 8, 9, 10, 11
t_{ADVH}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{CKA}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{CKB}	7, 8, 9, 10, 11
t_{LEA}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{LW}	7, 8, 9, 10, 11
t_{ASL}	7, 8, 9, 10, 11
t_{CSSL}	7, 8, 9, 10, 11
t_{AHL}	7, 8, 9, 10, 11
t_{CSHL}	7, 8, 9, 10, 11
t_{CSOV}	7, 8, 9, 10, 11
t_{LOV}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11

Note:

13. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Document #: 38–00179–E

CYPRESS SEMICONDUCTOR

32K x 8 PROM Power-Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 715 mW (military)**
- **Super low standby power**
  - **— Less than 165 mW when deselected**
- **EPROM technology 100% programmable**
- **Slim 300-mil package (7C271)**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

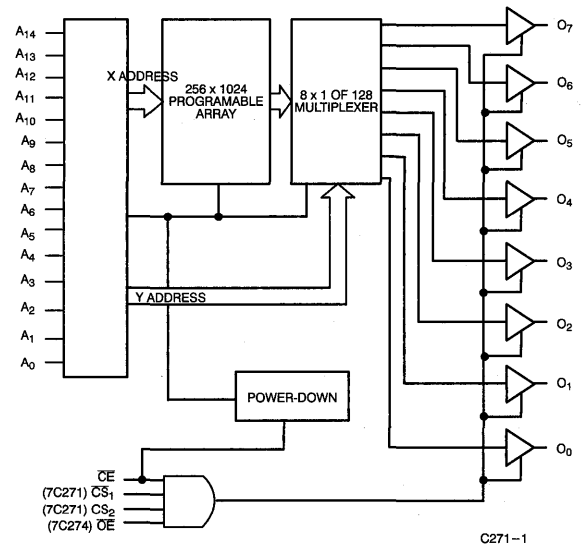
Functional Description

The CY7C271 and CY7C274 are high-performance 32,768-word by 8-bit CMOS PROMs. When disabled ($\overline{CE}$ HIGH), the 7C271/7C274 automatically powers down into a low-power stand-by mode. The CY7C271 is packaged in the 300-mil slim package. The CY7C274 is packaged in the industry standard 600-mil package. Both the 7C271 and 7C274 are available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 and CY7C274 offer the advantage of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

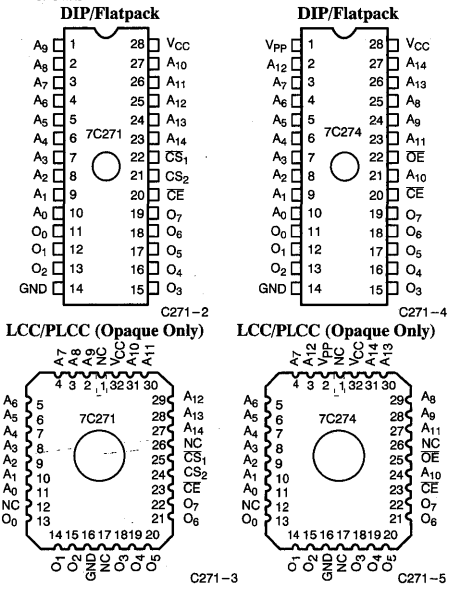
Reading the 7C271 is accomplished by placing active LOW signals on $\overline{CS_1}$ and $\overline{CE}$, and an active HIGH on CS_2. Reading the 7C274 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram



C271-1

Pin Configurations



Selection Guide

		7C271-30 7C274-30	7C271-35 7C274-35	7C271-45 7C274-45	7C271-55 7C274-55
Maximum Access Time (ns)		30	35	45	55
Maximum Operating Current (mA)	Com'l	120	120	120	120
	Military		130	130	130
Standby Current (mA)	Com'l	30	30	30	30
	Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C271−30, 35, 45, 55 7C274−30, 35, 45, 55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA[4]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA, $\overline{CE}$=V_{IL}	Commercial		120	mA
			Military		130	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Commercial		30	mA
			Military		40	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

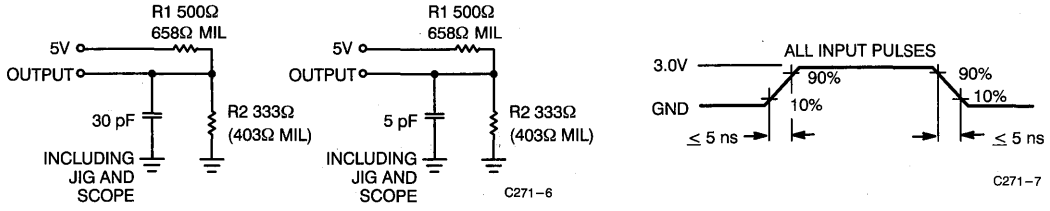
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for information on industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. 6.0 mA military
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms[6]

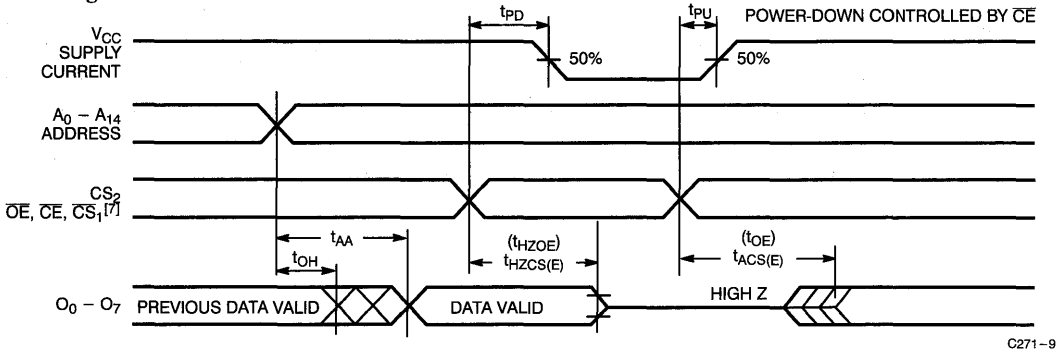


Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C271-30 7C274-30		7C271-35 7C274-35		7C271-45 7C274-45		7C271-55 7C274-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z ($\overline{CS_1}$ and CS_2, 7C271 Only)		20		25		30		30	ns
t_{ACS}	Chip Select Active to Output Valid ($\overline{CS_1}$ and CS_2, 7C271 Only)		20		25		30		30	ns
t_{HZOE}	Output Enable Inactive to High Z ($\overline{OE}$, 7C274 Only)		20		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid ($\overline{OE}$, 7C274 Only)		20		20		25		25	ns
t_{HZCE}	Chip Enable Inactive to High Z ($\overline{CE}$ Only)		35		40		50		60	ns
t_{ACE}	Chip Enable Active to Output Valid ($\overline{CE}$ Only)		35		40		50		60	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		35		40		50		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Switching Waveform



Note:
7. CS_2 and $\overline{CS_1}$ are used on the 7C271 only. $\overline{OE}$ is used on the 7C274 only.

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C271 and 7C274 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C271 or 7C274 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C271 Mode Selection

		Pin Function[8]				
	Read or Output Disable	$A_{14} - A_0$	$\overline{CE}$	CS_2	$\overline{CS}_1$	$O_7 - O_0$
Mode	**Other**	$A_{14} - A_0$	$\overline{VFY}$	$\overline{PGM}$	V_{PP}	$D_7 - D_0$
Read		$A_{14} - A_0$	V_{IL}	V_{IH}	V_{IL}	$O_7 - O_0$
Power Down		$A_{14} - A_0$	V_{IH}	X	X	High Z
Output Disable		$A_{14} - A_0$	X	V_{IL}	X	High Z
Output Disable		$A_{14} - A_0$	X	X	V_{IH}	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

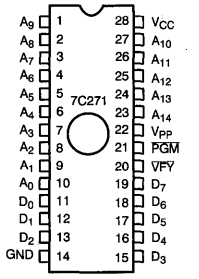
Table 2. CY7C274 Mode Selection

		Pin Function[8]				
	Read or Output Disable	$A_{14} - A_0$	$\overline{OE}$	$\overline{CE}$	V_{PP}	$O_7 - O_0$
Mode	**Other**	$A_{14} - A_0$	$\overline{VFY}$	$\overline{PGM}$	V_{PP}	$D_7 - D_0$
Read		$A_{14} - A_0$	V_{IL}	V_{IL}	Note 9	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Power Down		$A_{14} - A_0$	X	V_{IH}	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:

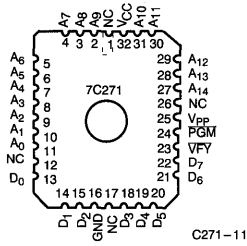
8. X can be V_{IL} (V_{ILP}) or V_{IH} (V_{IHP}).
9. V_{PP} should be tied to V_{CC} ±5% in read mode.

DIP
Top View



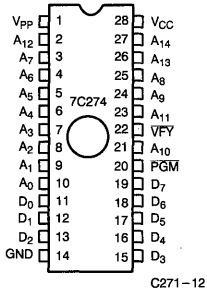
C271-10

LCC
Top View



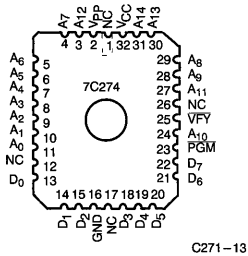
C271-11

DIP
Top View



C271-12

LCC
Top View

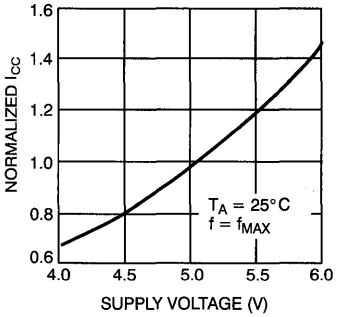


C271-13

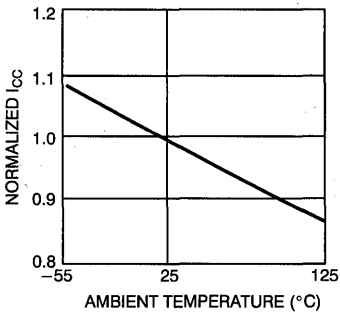
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

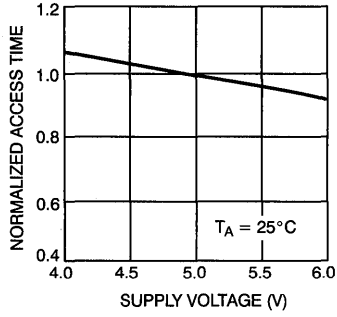
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



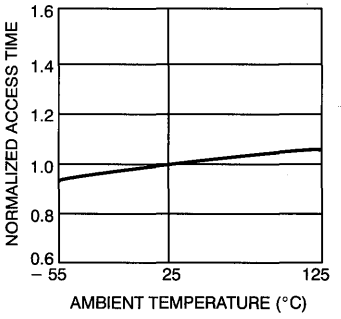
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



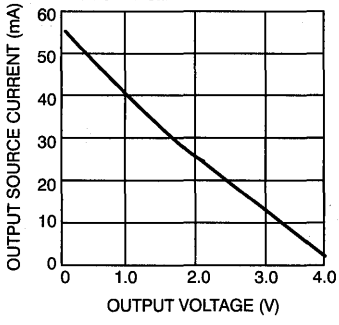
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



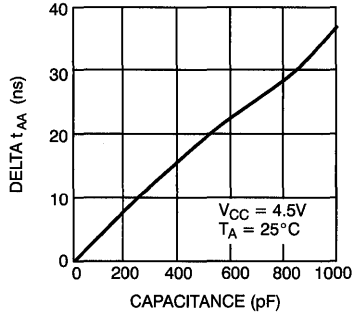
NORMALIZED ACCESS TIME vs. TEMPERATURE



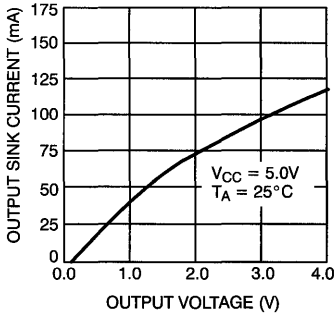
OUTPUT SOURCE CURRENT vs. VOLTAGE



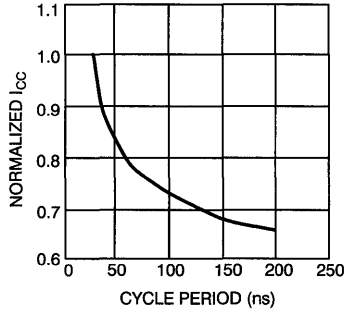
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



C271–14

Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C271–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271–30WC	W22	28-Lead (300-Mil) Windowed CerDIP	
35	CY7C271–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271–35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271–35WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271–35KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271–35WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
45	CY7C271–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271–45PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271–45KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271–45TMB	T74	28-Lead Windowed Cerpack	
	CY7C271–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C271–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271–55PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271–55KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271–55TMB	T74	28-Lead Windowed Cerpack	
	CY7C271–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[10] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C274–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C274–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C274–30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
35	CY7C274–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C274–35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C274–35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C274–35DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C274–35KMB	K74	28-Lead Rectangular Cerpack	
	CY7C274–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C274–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C274–35TMB	T74	28-Lead Windowed Cerpack	
	CY7C274–35WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
45	CY7C274–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C274–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C274–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C274–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C274–45KMB	K74	28-Lead Rectangular Cerpack	
	CY7C274–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C274–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C274–45TMB	T74	28-Lead Windowed Cerpack	
	CY7C274–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C274–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C274–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C274–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C274–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C274–55KMB	K74	28-Lead Rectangular Cerpack	
	CY7C274–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C274–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C274–55TMB	T74	28-Lead Windowed Cerpack	
	CY7C274–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[11]	7, 8, 9, 10, 11
t_{OE}[12]	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Notes:
11. 7C274 and 7C271 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).
12. 7C271 only.

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–89817	01XX	CY7C271–55WMB
5962–89817	01YX	CY7C271–55TMB
5962–89817	01ZX	CY7C271–55QMB
5962–89817	02XX	CY7C271–45WMB
5962–89817	02YX	CY7C271–45TMB
5962–89817	02ZX	CY7C271–45QMB

Document #: 38–00068–G

CYPRESS SEMICONDUCTOR

CY7C276

16K x 16 Reprogrammable PROM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed (for commercial and military)**
  - **—25-ns access time**
- **16-bit-wide words**
- **Three programmable chip selects**
- **Programmable output enable**
- **44-pin PLCC and 44-pin LCC packages**
- **100% reprogrammable in windowed packages**
- **TTL-compatible I/O**
- **Capable of withstanding greater than 2001V static discharge**

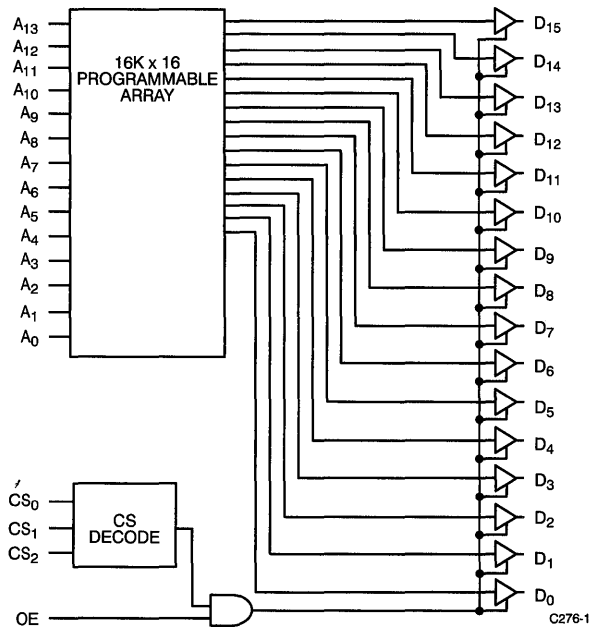
Functional Description

The CY7C276 is a high-performance 16K-word by 16-bit CMOS PROM. It is available in a 44-pin PLCC/CLCC and a 44-pin LCC packages, and is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms.

The CY7C276 allows the user to independently program the polarity of each chip select (CS_2–CS_0). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin (OE) is also programmable.

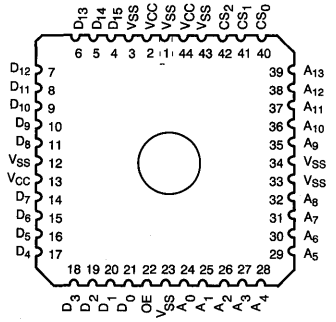
In order to read the CY7C276, all three chip selects must be active and OE must be asserted. The contents of the memory location addressed by the address lines (A_{13} – A_0) will become available on the output lines (D_{15} – D_0). The data will remain on the outputs until the address changes or the outputs are disabled.

Logic Block Diagram



Pin Configuration

LCC/PLCC/CLCC
Top View



Selection Guide

		CY7C276–25	CY7C276–30	CY7C276–35
Maximum Access Time (ns)		25	30	35
Maximum Operating Current (mA)	Commercial	175	175	175
	Military	200	200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	– 40°C to +85°C	5V ±10%
Military[2]	– 55°C to +125°C	5V ±10%

Electrical Characteristics[3, 4]

Parameter	Description	Test Conditions		CY7C276–25 CY7C276–30 CY7C276–35 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 3		µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		– 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[5]		– 20	– 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		175	mA
			Military		200	mA

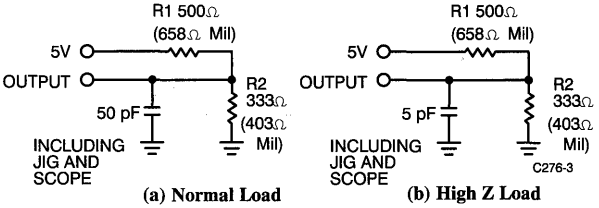
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

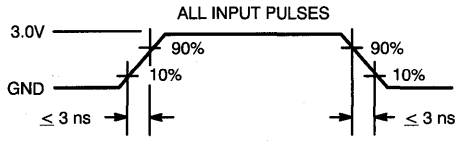
1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature
3. See Introduction to CMOS PROMs in this Data Book for general information on testing.
4. See the last page of this specification for Group A subgroup testing information.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

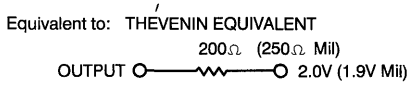
AC Test Loads and Waveforms



(a) Normal Load

(b) High Z Load





Switching Characteristics Over the Operating Range[3,4]

Parameter	Description	CY7C276–25		CY7C276–30		CY7C276–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Data Valid		25		30		35	ns
t_{CSOV}	CS Active to Output Valid		13		15		18	ns
t_{CSOZ}	CS Inactive to High Z Output		13		15		18	ns
t_{OEV}	OE Active to Output Valid		11		12		15	ns
t_{OEZ}	OE Inactive to High Z Output		11		12		15	ns

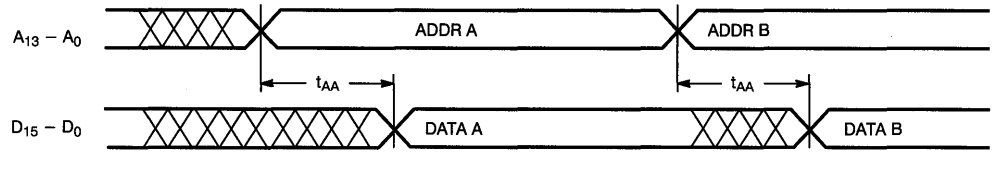
Erasure Characteristics

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C276 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Wavelengths of light less than 4000 Angstroms begin to erase the 7C276 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

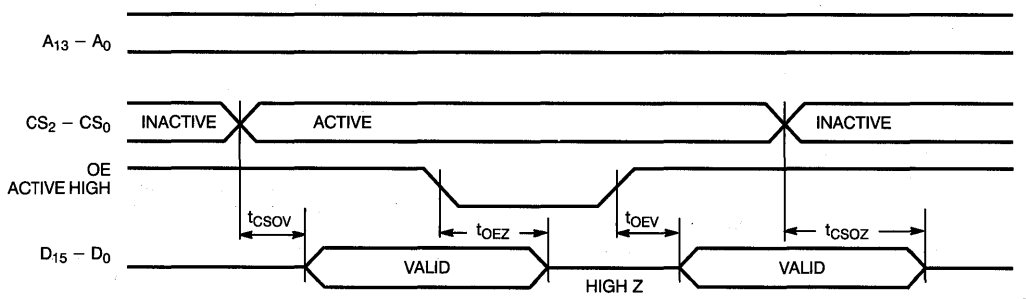
Switching Waveforms

Read Operation Timing Diagram[6]



C276-6

Chip Select and Output Enable Timing Diagrams



C276-7

Notes:
6. $CS_2 - CS_0$, OE assumed active.

Architecture Configuration Bits

The CY7C276 has four user-programmable options in addition to the reprogrammable data array. For detailed programming information contact your local Cypress representative.

The programmable options determine the active polarity for the three chip selects (CS_2 – CS_0) and OE. When these control bits are programmed with a 0 the inputs are active LOW. When these control bits are programmed with a 1 the inputs are active HIGH.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Control Word for Architecture Configuration

Control Option	Control Word		Function
	Bit	Programmed Level	
OE	D_0	0=Default 1=Programmed	OE Active LOW OE Active HIGH
CS_0	D_{12}	0=Default 1=Programmed	CS_0 Active LOW CS_0 Active HIGH
CS_1	D_{13}	0=Default 1=Programmed	CS_1 Active LOW CS_1 Active HIGH
CS_2	D_{14}	0=Default 1=Programmed	CS_2 Active LOW CS_2 Active HIGH

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word

Control Word (4000H)

D_{15} D_0

X CS_2 CS_1 CS_0 X X X X X X X X X 1 X X OE

Table 2. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 3. Configuration Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	Control Word

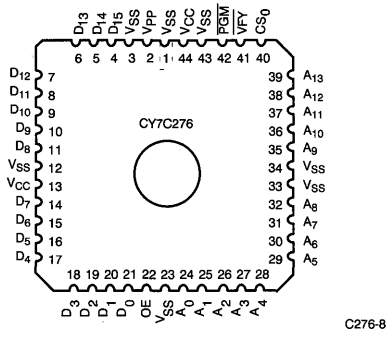
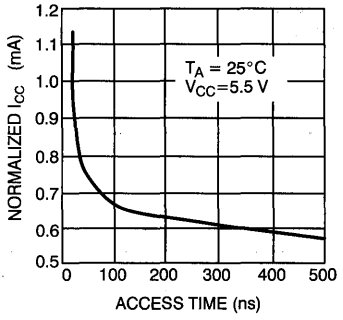


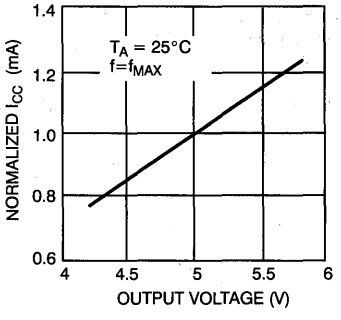
Figure 1. Programming Pinout

Typical DC and AC Characteristics

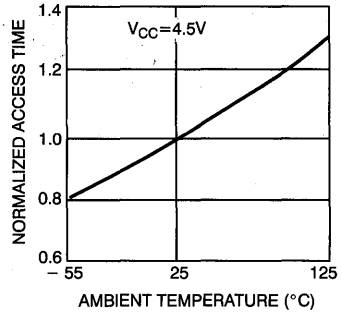
NORMALIZED I_{CC} vs. t_{CKA} CYCLE



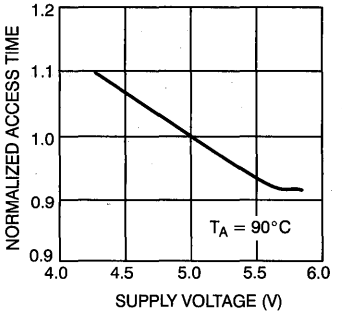
NORMALIZED I_{CC} vs. OUTPUT VOLTAGE



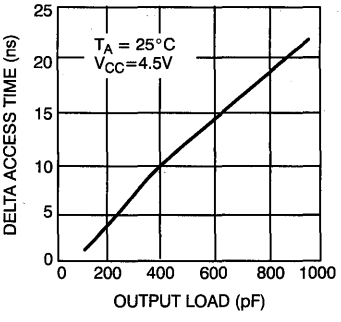
NORMALIZED t_{CKA} vs. TEMPERATURE



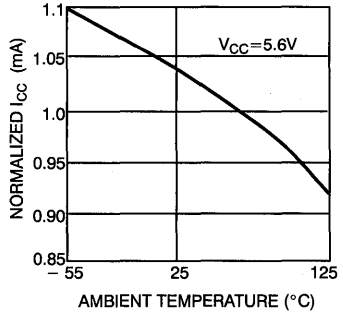
NORMALIZED t_{CKA} vs. SUPPLY VOLTAGE



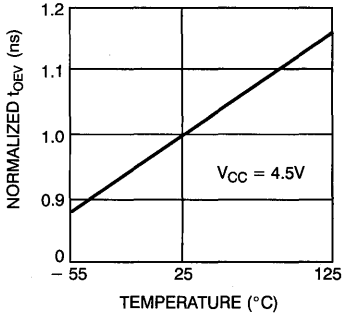
t_{CKA} CHANGE vs. OUTPUT LOADING



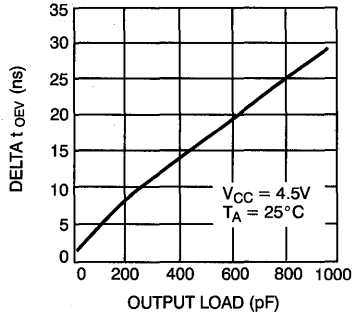
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



NORMALIZED t_{OEV} vs. TEMPERATURE



t_{OEV} CHANGE vs. OUTPUT LOADING



C276-9

Ordering Information[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C276–25HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–25JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–25QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C276–30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
35	CY7C276–35HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–35JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–35QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

Note:

7. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{CSOV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

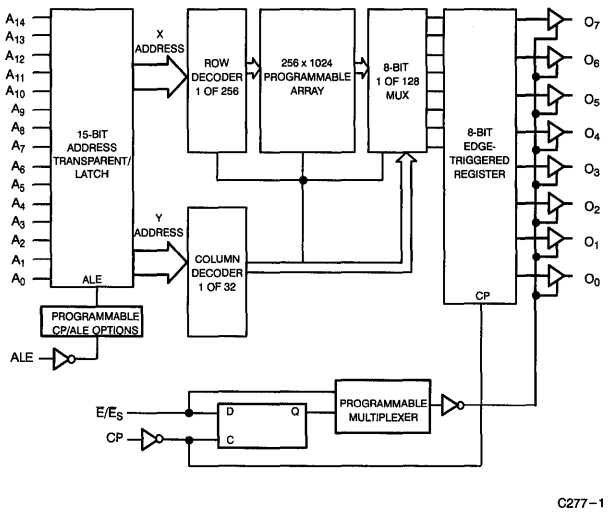
CY7C277

Reprogrammable 32K x 8 Registered PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 30-ns max. set-up
  - 15-ns clock to output
- Low power
  - 660 mW (commercial)
  - 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered output registers
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge

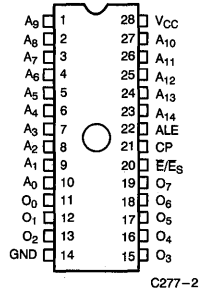
Logic Block Diagram



C277–1

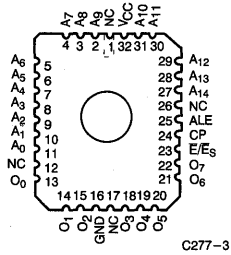
Pin Configurations

DIP/Flatpack
Top View



C277–2

LCC/PLCC (Opaque Only)
Top View



C277–3

Selection Guides

		7C277–30	7C277–40	7C277–50
Maximum Setup Time (ns)		30	40	50
Maximum Clock to Output (ns)		15	20	25
Maximum Operating Current (mA)	Com'l	120	120	120
	Mil		130	130

Functional Description

The CY7C277 is a high-performance 32K word by 8-bit CMOS PROMs. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C277 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge triggered output register. The $\overline{E}/\overline{E}_S$ input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin operates as an asynchronous output enable. If the synchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted. The user may define the polarity of the ALE signal, with the default being active HIGH.

3 PROMs

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	− 40°C to +85°C	5V ±10%
Military[2]	− 55°C to +125°C	5V ±10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

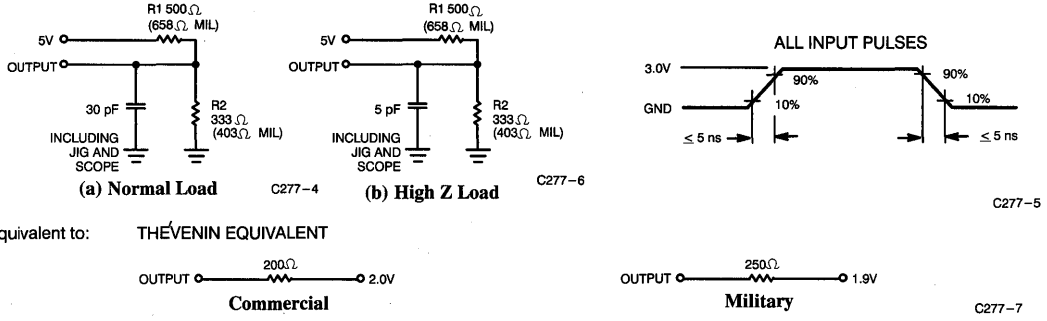
Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C277−30 Min.	7C277−30 Max.	7C277−40, 50 Min.	7C277−40, 50 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 4				
I_{OZ}	Output Leakage Current	0 ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, I_{OUT} = 0 mA	Commercial		120		120	mA
			Military				130	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[4]



Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

CY7C277 Switching Characteristics Over the Operating Range[3,4]

Parameter	Description	7C277-30		7C277-40		7C277-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AL}	Address Set-Up to ALE Inactive	5		10		10		ns
t_{LA}	Address Hold from ALE Inactive	10		10		15		ns
t_{LL}	ALE Pulse Width	10		10		15		ns
t_{SA}	Address Set-Up to Clock HIGH	30		40		50		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		10		10		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{LZC}[7]	Output Valid from Clock HIGH		15		20		30	ns
t_{HZC}	Output High Z from Clock HIGH		15		20		30	ns
t_{LZE}[8]	Output Valid from $\overline{E}$ LOW		15		20		30	ns
t_{HZE}[8]	Output High Z from $\overline{E}$ HIGH		15		20		30	ns

Notes:

7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

Architecture Configuration Bits

Architecture Bit	Architecture Verify $D_7 - D_0$		Function
ALE	D_1	0 = DEFAULT	Input Transparent
		1 = PGMED	Input Latched
ALEP	D_2	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW
$\overline{E}/\overline{E}_S$	D_0	0 = DEFAULT	Asynchronous Output Enable ($\overline{E}$)
		1 = PGMED	Synchronous Output Enable ($\overline{E}_S$)

Bit Map

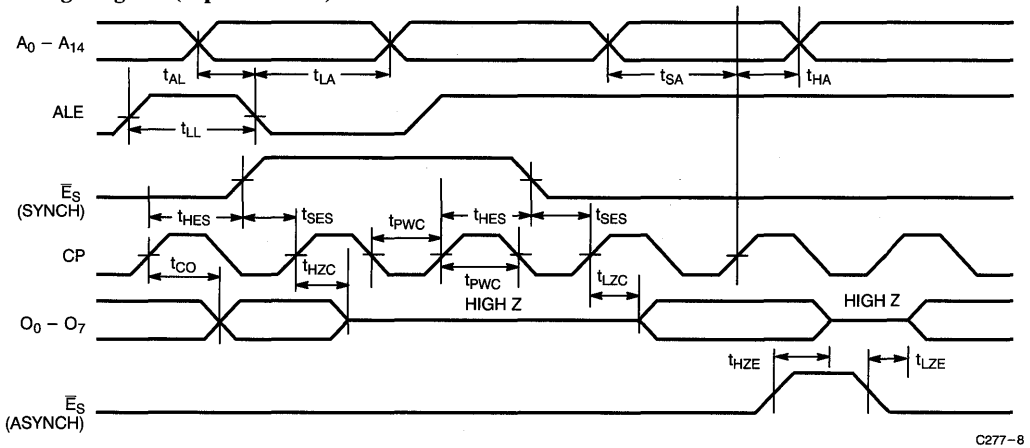
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
.	.
7FFF	Data
8000	Control Byte

Architecture Byte (8000)

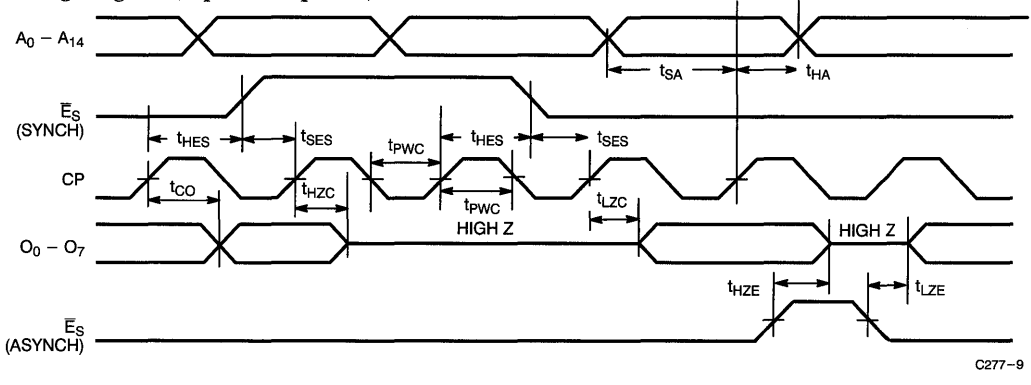
D_7 D_0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Timing Diagram (Input Latched)[9]



Timing Diagram (Input Transparent)



Note:
9. ALE is shown with positive polarity.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[10]				
	Read or Output Disable	$A_{14} - A_0$	$\overline{E}, \overline{E}_S$	CP	ALE	$O_7 - O_0$
	Other	$A_{14} - A_0$	$\overline{VFY}$	$\overline{PGM}$	V_{PP}	$D_7 - D_0$
Read		$A_{14} - A_0$	V_{IL}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

Note:
10. X = "don't care" but not to exceed V_{CC} ±5%.

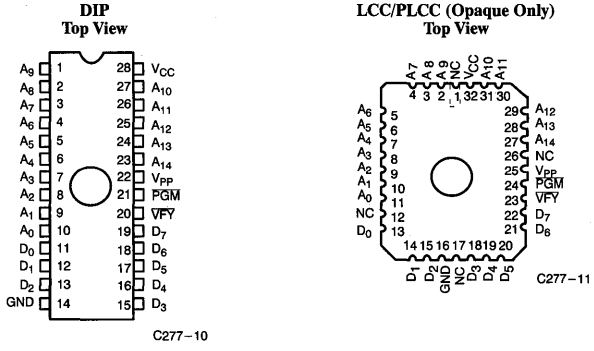
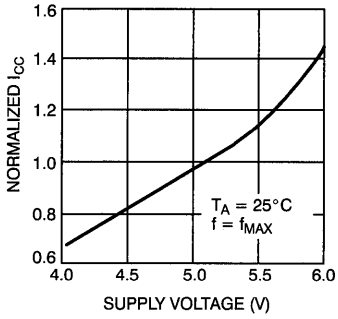


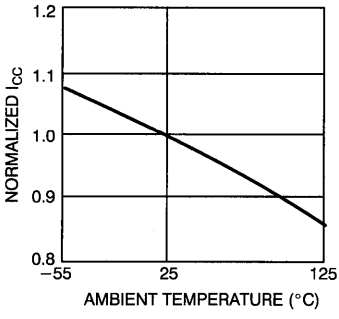
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

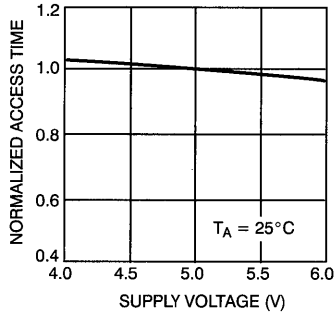
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



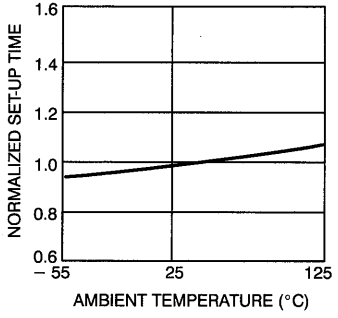
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



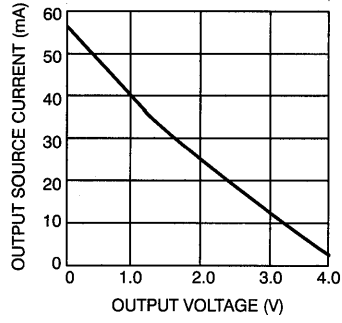
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



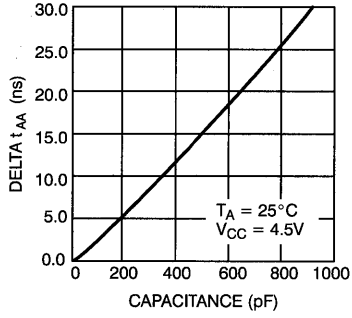
NORMALIZED SET-UP TIME vs. TEMPERATURE



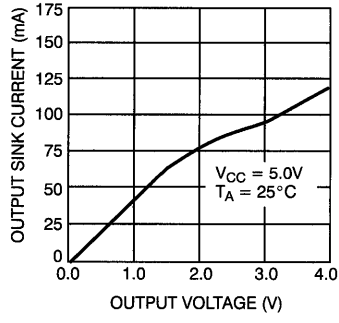
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C277–12

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C277–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–30WC	W22	28-Lead (300-Mil) Windowed CerDIP	
40	CY7C277–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C277–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C277–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C277–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C277–40QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C277–40TMB	T74	28-Lead Windowed Cerpack T74	
	CY7C277–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
50	CY7C277–50JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–50PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C277–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C277–50KMB	K74	28-Lead Rectangular Cerpack	
	CY7C277–50LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C277–50QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C277–50TMB	T74	28-Lead Windowed Cerpack T74	
	CY7C277–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

Document #: 38–00085–E

CY7C279

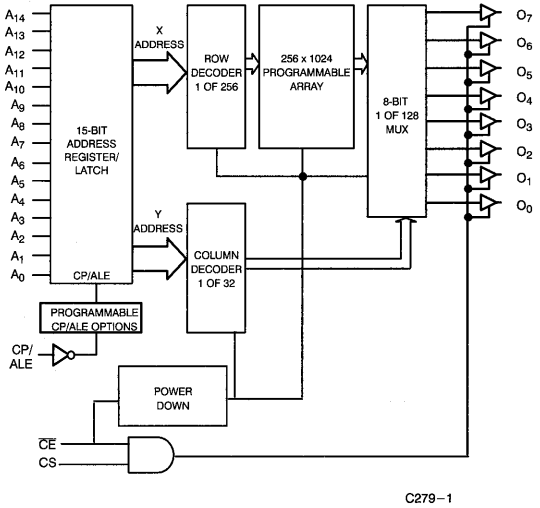
CYPRESS SEMICONDUCTOR

Reprogrammable 32K x 8 Registered PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - —3 ns max. set-up
  - —35 ns clock to output
- Low power
  - —660 mW (commercial)
  - —715 mW (military)
- Programmable address latch enable input
- Optional registered/latched address inputs
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge

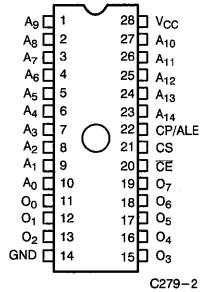
Logic Block Diagram



C279–1

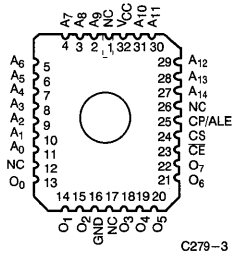
Pin Configurations

DIP
Top View



C279–2

LCC/PLCC (Opaque Only)
Top View



C279–3

Selection Guides

		7C279–35	7C279–45	7C279–55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		130	130
Maximum Standby Current (mA)	Commercial	30	30	30
	Military		40	40

Functional Description

The CY7C279 is a high-performance 32K word by 8-bit CMOS PROM. When deselected, the CY7C279 automatically powers dow into a low power standby mode. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C279 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C279, address registers are provided to easily interface with microprocessors that deliver addresses around a rising clock edge. A programmable bit is provided to select between latched and registered address inputs. The default is registered inputs, which will sample the address on the RISING EDGE of CP and load the address register. The latched address option will recognize any address changes while the ALE pin is active and load the address into the address latches on the deactiviating edge of ALE. If the latched address option is selected, another programmable bit is provided for the user to select the polarity that will define ALE active, with the default being active HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	− 40°C to +85°C	5V ±10%
Military[2]	− 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C279−35 Min.	7C279−35 Max.	7C279−45, 55 Min.	7C279−45, 55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage			Note 4				
I_{OZ}	Output Leakage Current	0 ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, I_{OUT} = 0 mA	Commercial		120		120	mA
			Military				130	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				40	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

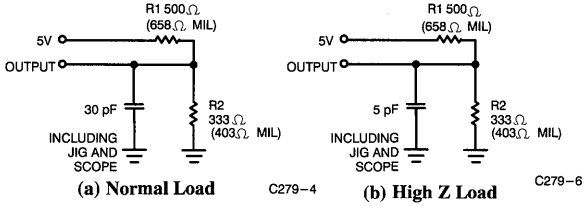
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Data Book for general information on testing.

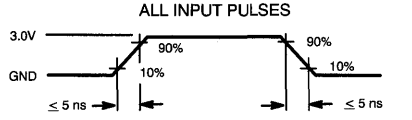
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[4]

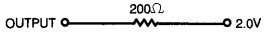


(a) Normal Load C279-4 (b) High Z Load C279-6

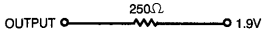


C279-5

Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

C279-7

Switching Characteristics Over the Operating Range[3,4]

Parameter	Description	7C279-35		7C279-45		7C279-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Data Valid (Latched Mode)		35		45		55	ns
t_{CO}	Clock to Output Valid (Registered Mode)		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		20	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		20	ns
t_{AR}	Address Set-up to Clock Rise (Registered Mode)	3		10		10		ns
t_{RA}	Address Hold from Clock Rise (Registered Mode)	6		10		10		ns
t_{ADH}	Data Hold from Clock Rise (Registered Mode)	5		5		5		ns
t_{SU}	Address Set-up to ALE Inactive (Latched Mode)	5		10		10		ns
t_{HD}	Address Hold from ALE Inactive (Latched Mode)	10		10		10		ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		40		50		60	ns
t_{OH}[7]	Output Hold from Address Change (Latched Mode)	0		0		0		ns
t_{PWA}	ALE Pulse Width	10		20		30		ns
t_{CESC}	Chip Enable Set-up to Clock Rise	10		10		10		ns
t_{CESL}	Chip Enable Set-up to Latch Close (Latch Mode)	10		10		10		ns
t_{LV}	Output Valid from ALE Active (Latched Mode)		40		50		60	ns

Notes:

5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. t_{AA} and t_{OH} apply only when the latched mode is selected.

Architecture Configuration Bits

Architecture Bit	Architecture Verify $D_7 - D_0$		Function
ALE	D_1	0 = DEFAULT	Input Registered
		1 = PGMED	Input Latched
ALEP	D_2	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW

Bit Map

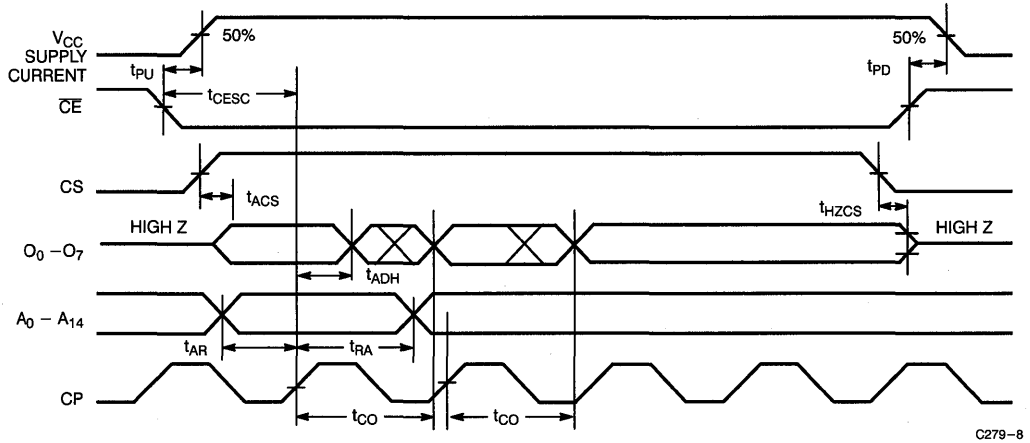
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
.	.
7FFF	Data
8000	Control Byte

Architecture Byte (8000)

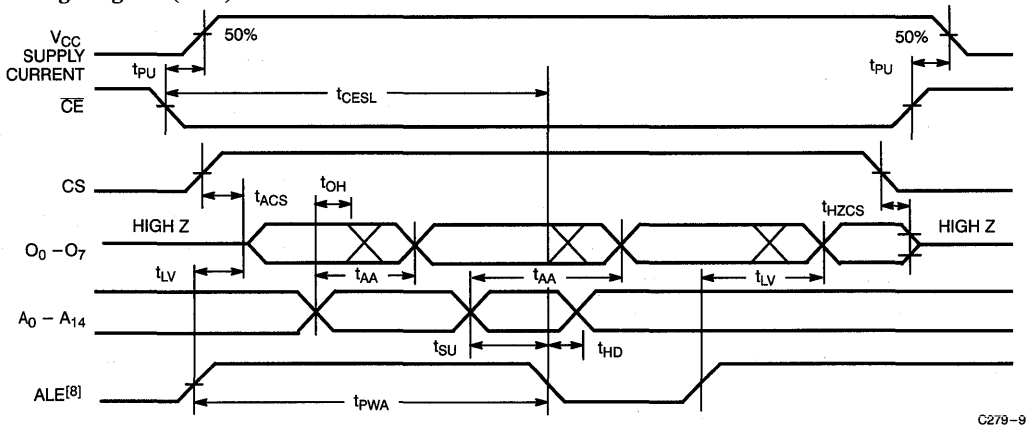
D_7 D_0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Timing Diagram (Registered)[8]



Timing Diagram (ALE)



Note:
8. ALE is shown with positive polarity.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[9]				
	Read or Output Disable	**$A_{14} - A_0$**	**$\overline{CE}$**	**CS**	**CP/ALE**	**$O_7 - O_0$**
	Other	**$A_{14} - A_0$**	**$\overline{VFY}$**	**$\overline{PGM}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{14} - A_0$	V_{IL}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

Note:
9. X = "don't care" but not to exceed V_{CC} ±5%.

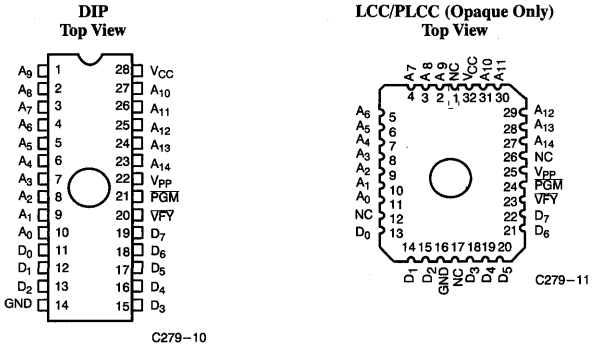
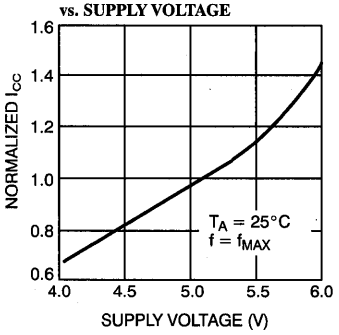


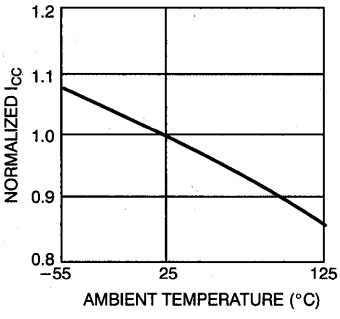
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

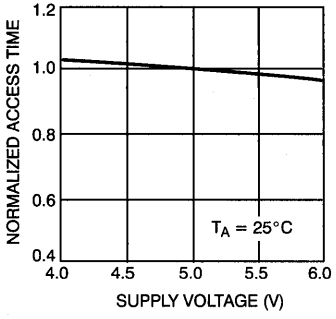
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



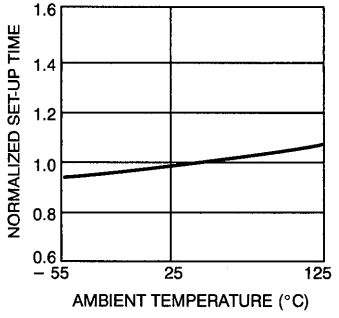
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



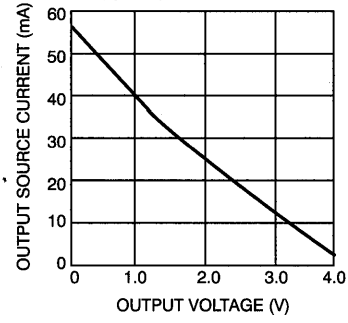
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



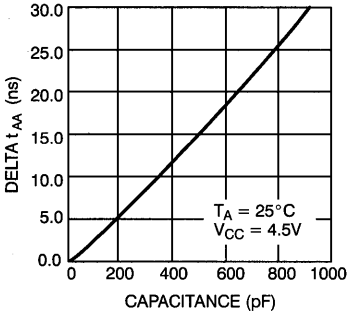
NORMALIZED SET-UP TIME vs. TEMPERATURE



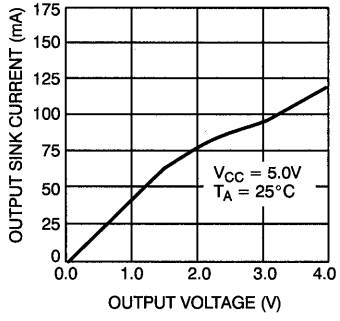
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C279–12

Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
35	CY7C279–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279–35WC	W22	28-Lead (300-Mil) Windowed CerDIP	
45	CY7C279–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C279–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
55	CY7C279–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C279–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military

Note:
10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AR}	7, 8, 9, 10, 11
t_{RA}	7, 8, 9, 10, 11
t_{DHA}	7, 8, 9, 10, 11

Document #: 38–00246

CY7C281
CY7C282

CYPRESS SEMICONDUCTOR

1K x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **—30 ns (commercial)**
  - **—45 ns (military)**
- **Low power**
  - **—495 mW (commercial)**
  - **—660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil DIP or 28-pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >1500V static discharge**

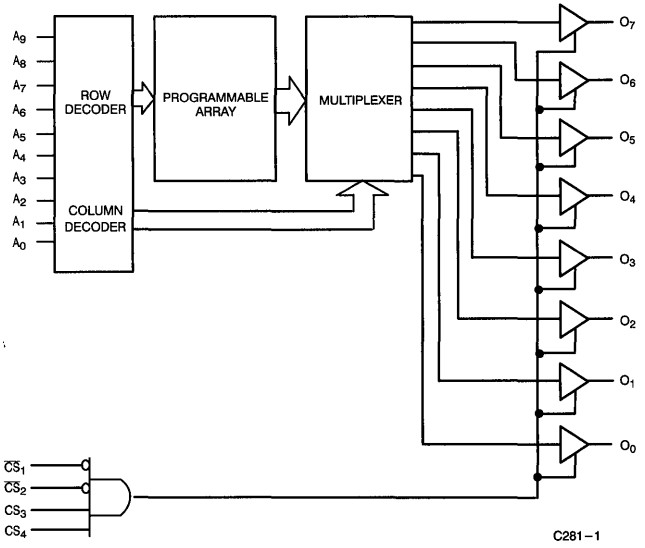
Functional Description

The CY7C281 and CY7C282 are high-performance 1024-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil-wide packages respectively. The CY7C281 is also available in a 28-pin leadless chip carrier. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C281 and CY7C282 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 13.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0 – A_9) will become available on the output lines (O_0 – O_7).

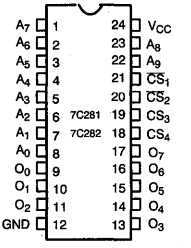
Logic Block Diagram



C281–1

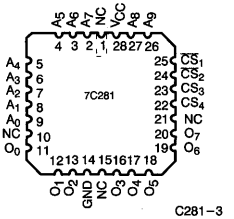
Pin Configurations

DIP
Top View



C281–2

LCC/PLCC
Top View



C281–3

Selection Guide

		7C281–30 7C282–30	7C281–45 7C282–45
Maximum Access Time (ns)		30	45
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C281−30 7C282−30 Min.	7C281−30 7C282−30 Max.	7C281−45 7C282−45 Min.	7C281−45 7C282−45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current[6]	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	
V_{PP}	Program Voltage			13	14	13	14	V
V_{IHP}	Program HIGH Voltage			3.0		3.0		V
V_{ILP}	Program LOW Voltage				0.4		0.4	V
I_{PP}	Program Supply Current				50		50	mA

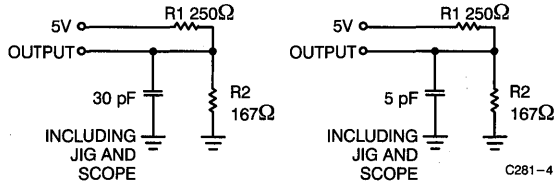
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

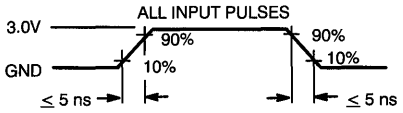
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Due to the design of the differential cell in this device, I_{cc} can only be accurately measured on a programmed array.

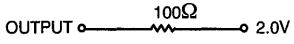
AC Test Loads and Waveforms[4]



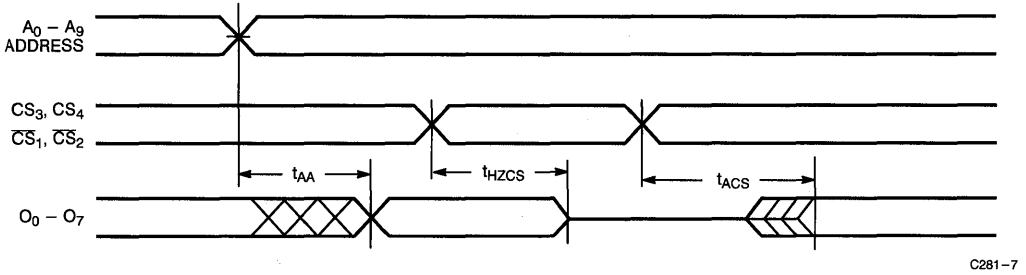
(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Waveforms



Switching Characteristics Over the Operating Range[2, 4]

Parameter	Description	7C281–30 7C282–30		7C281–45 7C282–45		Unit
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		20		25	ns

Programming Information

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[7]					
	Read or Output Disable	$A_9 - A_0$	CS_4	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	$O_7 - O_0$
	Other	$A_9 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS}_1$	$D_7 - D_0$
Read		$A_7 - A_0$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable		$A_7 - A_0$	X	X	V_{IH}	X	High Z
Output Disable		$A_7 - A_0$	X	V_{IL}	X	X	High Z
Output Disable		$A_7 - A_0$	V_{IL}	X	X	X	High Z
Output Disable		$A_7 - A_0$	X	X	X	V_{IH}	High Z
Program		$A_7 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Program Verify		$A_7 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	$O_7 - O_0$
Program Inhibit		$A_7 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		$A_7 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Blank Check Ones		$A_7 - A_0$	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		$A_7 - A_0$	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	Zeros

Note:
7. X = "don't care" but not to exceed V_{CC} ±5%.

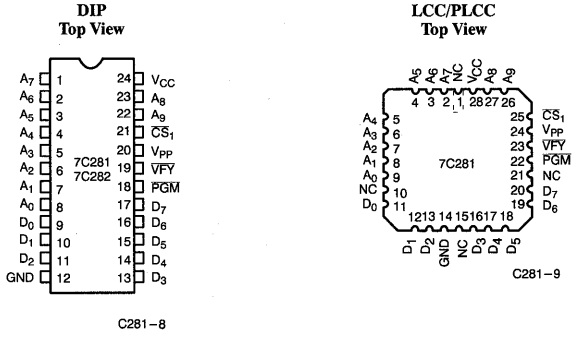
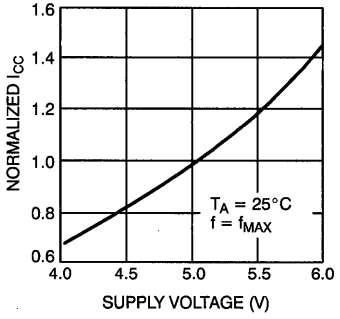


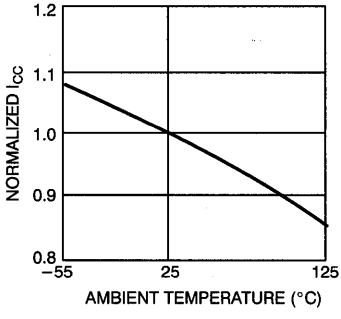
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

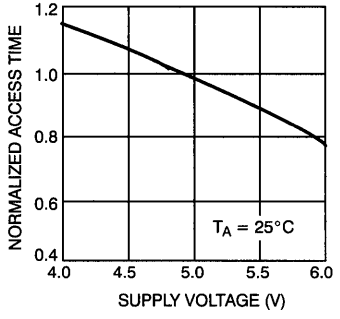
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



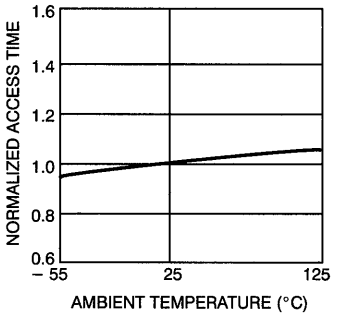
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



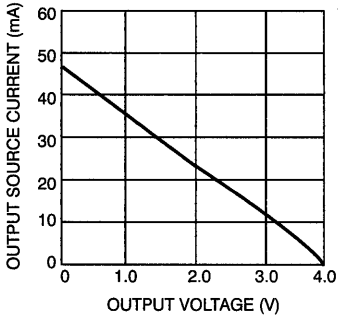
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



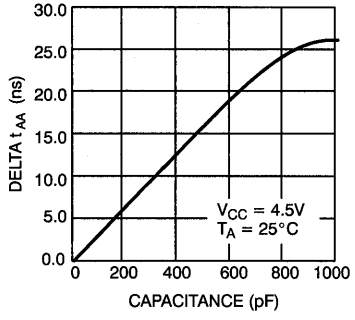
NORMALIZED ACCESS TIME vs. TEMPERATURE



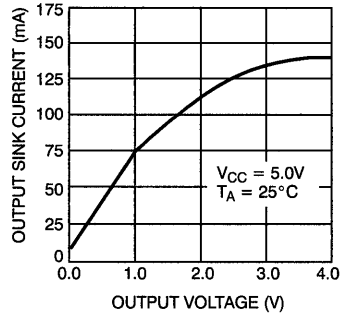
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C281–10

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C281–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281–30PC	P13	24-Lead (300-Mil) Molded DIP	
45	CY7C281–45DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281–45JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C281–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C281–45KMB	K73	24-Lead Rectangular Cerpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
	CY7C282–30PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C282–45PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C282–45DMB	D12	24-Lead (600-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38–00006–F

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–87651	01JX	CY7C282–45DMB
5962–87651	01KX	CY7C281–45KMB
5962–87651	01LX	CY7C281–45DMB
5962–87651	013X	CY7C281–45LMB

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C281A
CY7C282A

1K x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns (commercial)**
  - **— 30 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil DIP or 28-pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

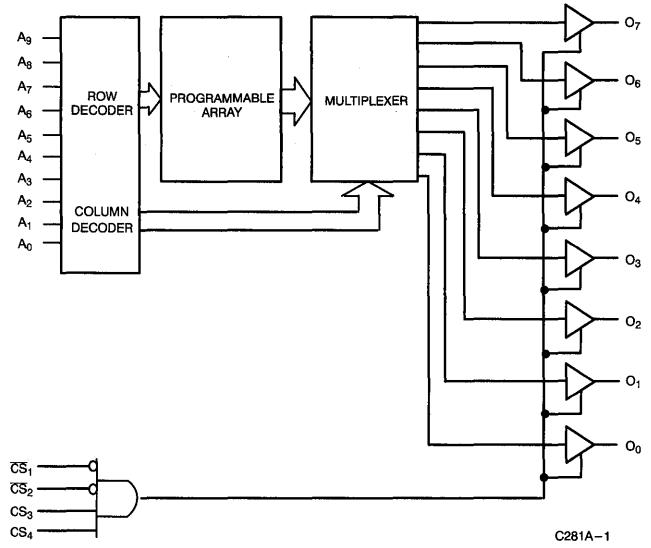
Functional Description

The CY7C281A and CY7C282A are high-performance 1024-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil-wide packages respectively. The CY7C281A is also available in a 28-pin leadless chip carrier. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C281A and CY7C282A are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0 – A_9) will become available on the output lines (O_0 – O_7).

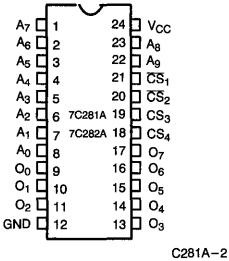
Logic Block Diagram



C281A–1

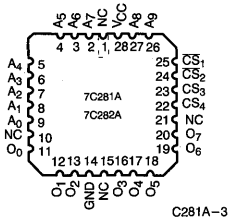
Pin Configurations

DIP
Top View



C281A–2

LCC/PLCC
Top View



C281A–3

Selection Guide

		7C281A–25 7C282A–25	7C281A–30 7C282A–30	7C281A–45 7C282A–45
Maximum Access Time (ns)		25	30	45
Maximum Operating Current (mA)	Commercial	100	100	90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	− 40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C281A−25 7C282A−25 Min.	7C281A−25 7C282A−25 Max.	7C281A−30 7C282A−30 Min.	7C281A−30 7C282A−30 Max.	7C281A−45 7C282A−45 Min.	7C281A−45 7C282A−45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	$V_0 \le V_{OUT} \le V_{CC}$, Output Disabled		− 10	+10	− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	− 20	− 90	− 20	− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		100		90	mA
			Military				120		120	
V_{PP}	Program Voltage			12	13	12	13	12	13	V
V_{IHP}	Program HIGH Voltage			3.0		3.0		3.0		V
V_{ILP}	Program LOW Voltage				0.4		0.4		0.4	V
I_{PP}	Program Supply Current				50		50		50	mA

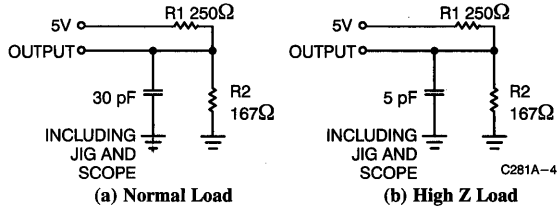
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

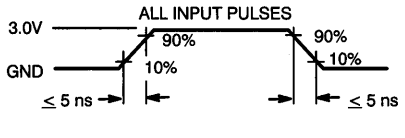
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

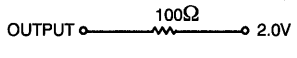
AC Test Loads and Waveforms[4]



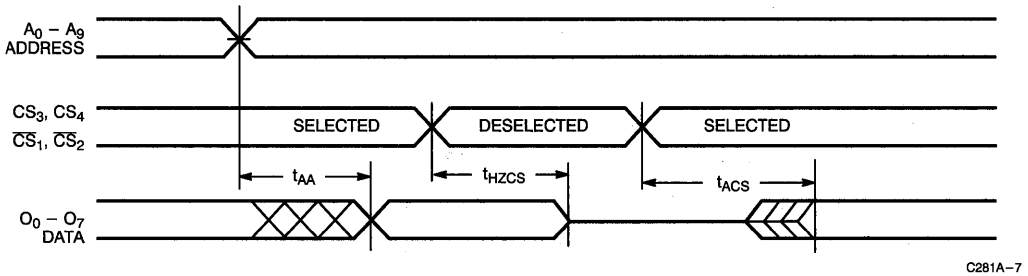
(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Waveforms



Switching Characteristics Over the Operating Range[2,4]

Parameter	Description	7C281A–25 7C282A–25		7C281A–30 7C282A–30		7C281A–45 7C282A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		25	ns

Programming Information

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Read or Output Disable / Other	Pin Function[6]					
	Read or Output Disable	$A_9 - A_0$	CS_4	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	$O_7 - O_0$
	Other	$A_9 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS}_1$	$D_7 - D_0$
Read		$A_9 - A_0$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable		$A_9 - A_0$	X	X	V_{IH}	X	High Z
Output Disable		$A_9 - A_0$	X	V_{IL}	X	X	High Z
Output Disable		$A_9 - A_0$	V_{IL}	X	X	X	High Z
Output Disable		$A_9 - A_0$	X	X	X	V_{IH}	High Z
Program		$A_9 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Program Verify		$A_9 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	$O_7 - O_0$
Program Inhibit		$A_9 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		$A_9 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Blank Check		$A_9 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Zeros

Note:
6. X = "don't care" but not to exceed V_{CC} ±5%.

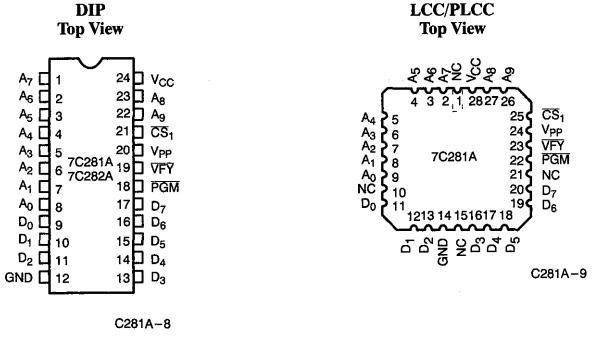
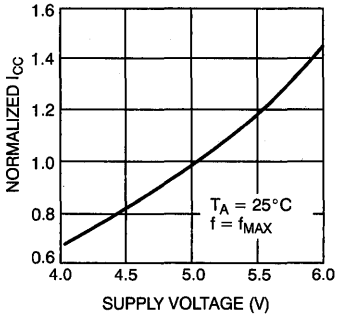


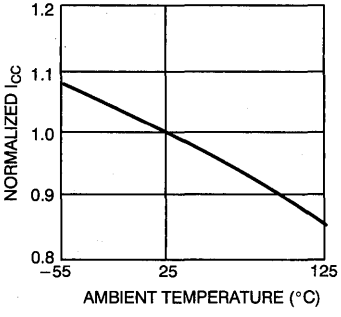
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

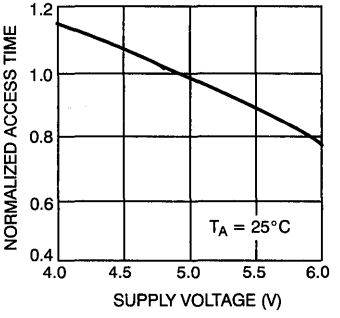
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



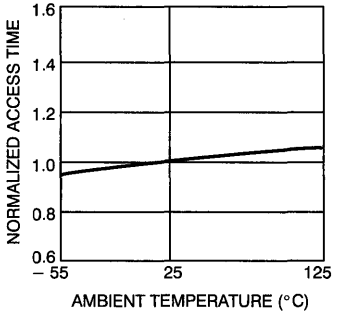
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



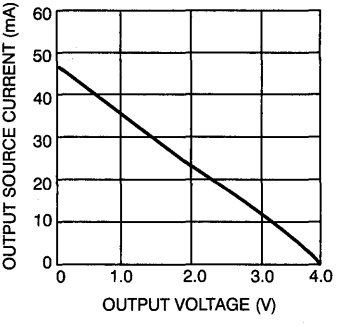
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



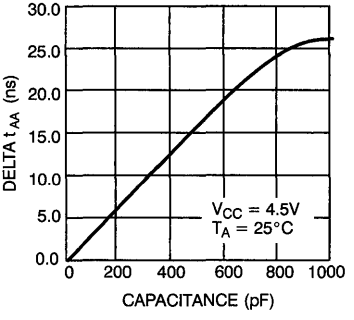
NORMALIZED ACCESS TIME vs. TEMPERATURE



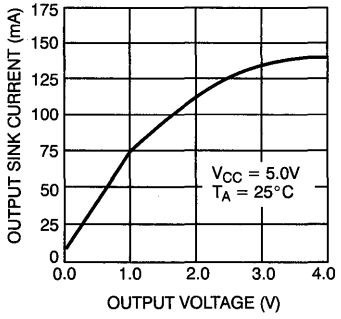
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C281A–10

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C281A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–25PC	P13	24-Lead (300-Mil) Molded DIP	
30	CY7C281A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–30PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C281A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C281A–45DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C281A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C281A–45KMB	K73	24-Lead Rectangular Cerpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C282A–25PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
30	CY7C282A–30PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C282A–30DMB	D12	24-Lead (600-Mil) CerDIP	Military
45	CY7C282A–45PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C282A–45DMB	D12	24-Lead (600-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38–00227–A

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–87651	01JX	CY7C282A–45DMB
5962–87651	01KX	CY7C281A–45KMB
5962–87651	01LX	CY7C281A–45DMB
5962–87651	013X	CY7C281A–45LMB

CYPRESS SEMICONDUCTOR

CY7C285

64K x 8 Reprogrammable Fast Column Access PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **Unique fast column access**
  - **— t_{AA} = 20 ns (commercial)**
  - **— t_{AA} = 25 ns (military)**
- **WAIT signal**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Slim 300-mil package**
- **Capable of withstanding >2001V static discharge**

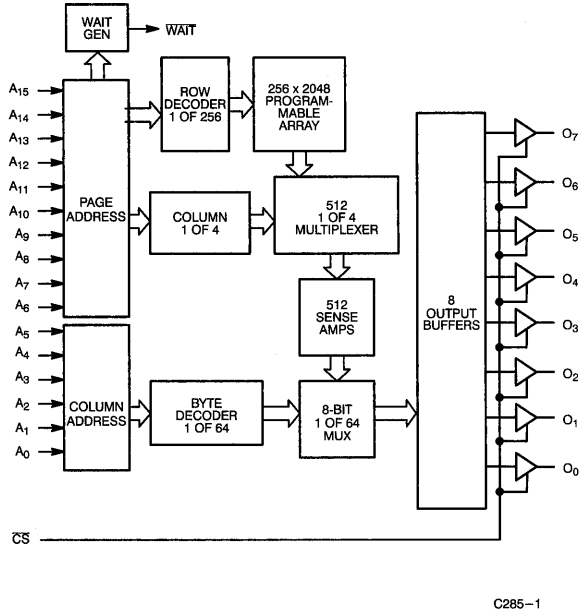
Functional Description

The CY7C285 is a high-performance 65,536 by 8-bit CMOS PROM. It is available in a 28-pin 300-mil package and features a unique fast column access feature that allow access times as fast as 20 ns for each byte in a 64-byte page. There are 1024 pages in the device. The access time when changing pages is 65 ns. In order to easily facilitate the use of the fast column access feature, a $\overline{WAIT}$ signal is generated to advise the processor of a page change.

The CY7C285 offers the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, allowing for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C285 is accomplished by placing an active LOW signal on the $\overline{CS}$ pin. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7).

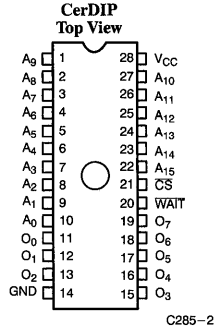
Logic Block Diagram



C285–1

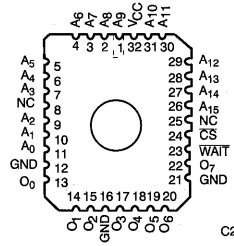
Pin Configurations

CerDIP
Top View



C285–2

LCC
Top View



C285–3

Selection Guide

Description		7C285–65	7C285–75	7C285–85
Maximum Access Time (ns)	Page Access Time	65	75	85
	Column Access Time	20	25	35
Maximum Operating Current (mA)	Commercial	180	180	180
	Military		200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pin 22) 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	− 40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C285 Min.	7C285 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA[5]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
V_{CD}	Input Diode Clamp Voltage			Note 4		V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180	mA
			Mil		200	mA

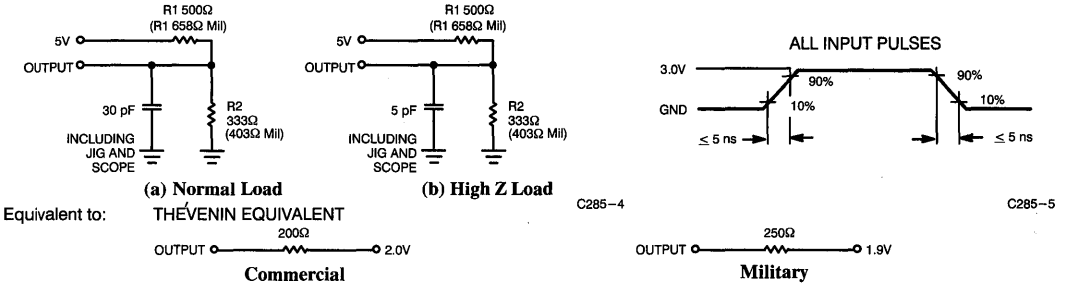
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. I_{OL} = 6.0 mA for military.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

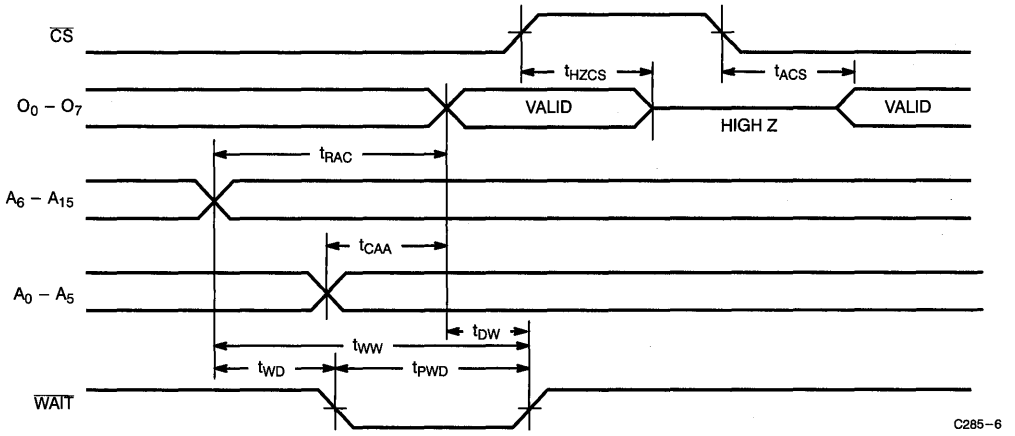
AC Test Loads and Waveform[4]



Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C285–65		7C285–75		7C285–85		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAC}	Slow Address Access Time ($A_6 - A_{15}$)		65		75		85	ns
t_{CAA}	Fast Address Access Time ($A_0 - A_5$)		20		25		35	ns
t_{HZCS}	Output High Z from $\overline{CS}$		15		20		25	ns
t_{ACS}	Output Valid from $\overline{CS}$		15		20		25	ns
t_{WD}	$\overline{WAIT}$ Delay from First Slow Address Change		20		25		35	ns
t_{DW}	$\overline{WAIT}$ Hold from Data Valid	0		0		0		ns
t_{WW}	$\overline{WAIT}$ Recovery from Last Address Change		90		110		120	ns
t_{PWD}	$\overline{WAIT}$ Pulse Width	10		12		15		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C285 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multipled by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C285 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Mode Selection

	Pin Number				
	22	23	21	20	19–15, 13–11
Mode: Read or Output Disable	**A_{15}**	**A_{14}**	**$\overline{CS}$**	**$\overline{WAIT}$**	**$O_7 - O_0$**
Read (within a page: $A_6 - A_{15}$ stable)	A_{15}	A_{14}	V_{IL}	V_{OH}	$O_7 - O_0$
Read (page break: $A_6 - A_{15}$ transition)	A_{15}	A_{14}	V_{IL}	Pulse LOW	$O_7 - O_0$
Output Disable	A_{15}	A_{14}	V_{IH}	Output	High Z
Mode: Other	**V_{PP}**	**LATCH**	**$\overline{PGM}$**	**$\overline{VFY}$**	**$D_7 - D_0$**
Program	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	$D_7 - D_0$
Program Inhibit	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	High Z
Program Verify	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	$O_7 - O_0$
Blank Check	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	Zeros

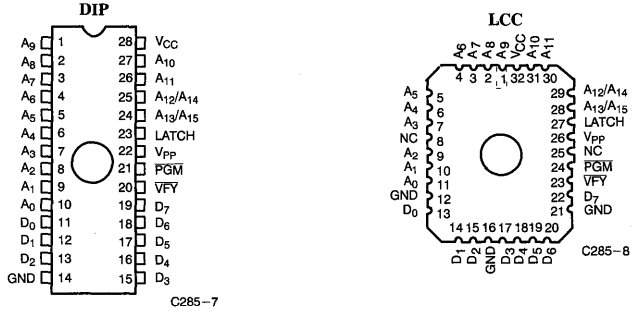


Figure 1. Programming Pinouts

Ordering Information[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
65	CY7C285–65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285–65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
75	CY7C285–75PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285–75WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C285–75DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C285–75LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C285–75QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C285–75WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
85	CY7C285–85PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285–85WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C285–85DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C285–85LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C285–85QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C285–85WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
7. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{CAA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38–00097–G

CY7C286
CY7C287

CYPRESS SEMICONDUCTOR

64K x 8 Reprogrammable Asynchronous/Registered PROMs

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - t_{SA} = 45 ns (7C287)
  - t_{CO} = 15 ns (7C287)
  - t_{ACC} = 50 ns (7C286)
- Low power
  - 120 mA active
  - 40 mA standby (7C286)
- On-chip, edge-triggered output registers (7C287)
- Programmable synchronous (7C287 only) or asynchronous output enable
- EPROM technology, 100% programmable
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Slim 300-mil package (7C287)
- Capable of withstanding >2001V static discharge

Functional Description

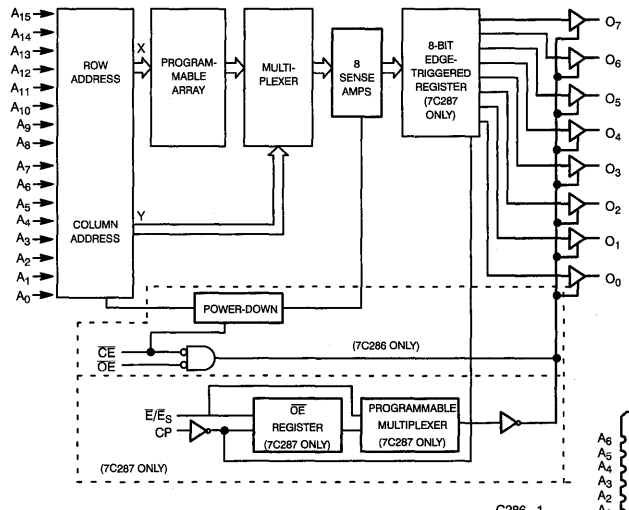
The CY7C286 and the CY7C287 are high-performance 65,536 by 8-bit CMOS PROMs. The CY7C286 is configured in the JEDEC-standard 512K EPROM pinout and is available in a 28-pin, 600-mil package. Power consumption is 120 mA in the active mode and 40 mA in the standby mode. Access time is 50 ns. The CY7C287 has registered outputs and operates in the synchronous mode. $\overline{E}$ can also be programmed into the synchronous mode, $\overline{E}_S$. It is available in a 28-pin, 300-mil package. The address set-up time is 45 ns and the time from clock HIGH to output valid is 15 ns.

Both the CY7C286 and the CY7C287 are available in a cerDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

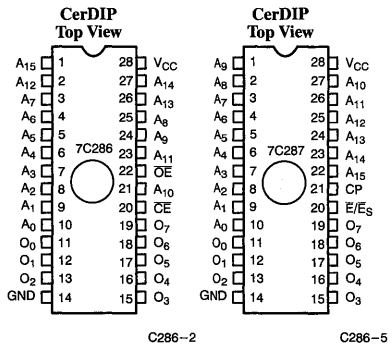
The CY7C286 and the CY7C287 offer the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

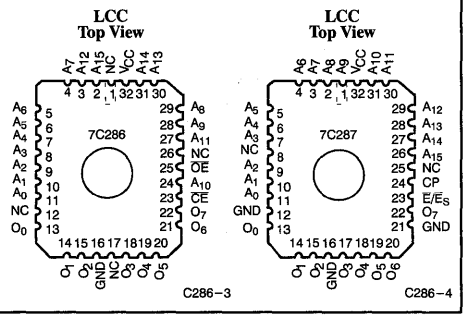
Reading the CY7C286 is accomplished by placing active LOW signals on the $\overline{OE}$ and $\overline{CE}$ pins. Reading the CY7C287 is accomplished by placing an active LOW signal on $\overline{E}/\overline{E}_S$. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7) on the next rising of CP.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C286–50	7C286–60	7C286–70	7C286–80
Maximum Access Time (ns)		50	60	70	80
Maximum Operating Current (mA)	Com'l	120	120	90	
	Mil		150	120	120
Maximum Standby Current (mA)	Com'l	40	40	30	
	Mil		50	40	40

		7C287–45	7C287–55	7C287–65
Maximum Set-Up Time (ns)		45	55	65
Maximum Clock to Output (ns)		15	20	25
Maximum Operating Current (mA)	Com'l	120	120	120
	Mil		150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V (Pin 28 to Pin 14)

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage (Pin 22) 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C286–50 7C287–45 Min.	Max.	7C286–60 7C287–55 Min.	Max.	7C286–70, 80 7C287–65 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil				0.4		0.4	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for Inputs			0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4						
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+40	– 40	+40	– 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[5]		– 20	– 90	– 20	– 90	– 20	– 90	mA
I_{CC} (7C286)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		90	mA
			Mil				150		120	
I_{CC} (7C287)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		120	mA
			Mil				150		150	
I_{SB}[6]	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = HIGH	Com'l		40		40		30	mA
			Mil				50		40	

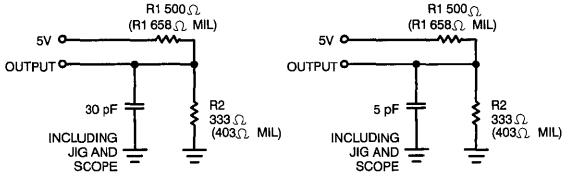
Notes:

1. Contact a Cypress representative for industrial termperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs for general information on testing.
5. Short circuit test should not exceed 30 seconds.
6. Only the CY7C286 has a standby mode.

Capacitance[4]

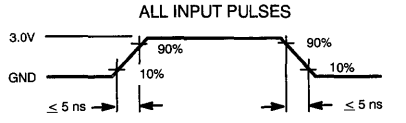
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveform[4]



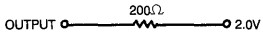
(a) Normal Load (b) High Z Load

C286-6

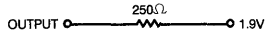


C286-7

Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

7C286 Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C286-50		7C286-60		7C286-70		7C286-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address Access Time		50		60		70		80	ns
t_{CE}	Output Valid from $\overline{CE}$		50		60		70		80	ns
t_{OE}	Output Valid from $\overline{OE}$		18		20		25		25	ns
t_{DF}	Output Tri-State from $\overline{CE}/\overline{OE}$		18		20		25		25	ns
t_{PU}	Chip Enable to Power-Up	0		0		0		0		ns
t_{PD}	Chip Disable to Power-Down		40		50		60		60	ns

7C287 Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C287-45		7C287-55		7C287-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	45		55		65		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{HZE}	Output High Z from $\overline{E}$		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		25		ns
t_{SEs}[7]	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		18		ns
t_{HEs}[7]	$\overline{E}_S$ Hold from Clock HIGH	5		8		10		ns
t_{HZC}[7]	Output High Z from CLK/$\overline{E}_S$		20		25		30	ns
t_{COs}[7]	Output Valid from CLK/$\overline{E}_S$		20		25		30	ns

Note:
7. Parameters with synchronous $\overline{E}_S$ option.

Architecture Configuration Bits

Architecture Bit	Device	Architecture Verify D_0		Function
$\overline{E}/\overline{E}_S$	7C287	D_0	0 = Erased	Asynchronous Output Enable (Pin 20 = $\overline{E}$)
			1 = PGMED	Synchronous Output Enable (Pin 20 = $\overline{E}_S$)

Bit Map

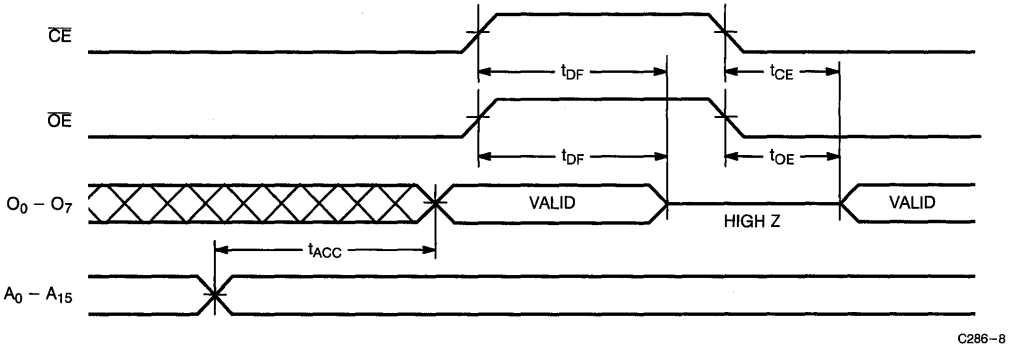
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
FFFF	Data
10000	Control Byte

Architecture Byte (10000H)

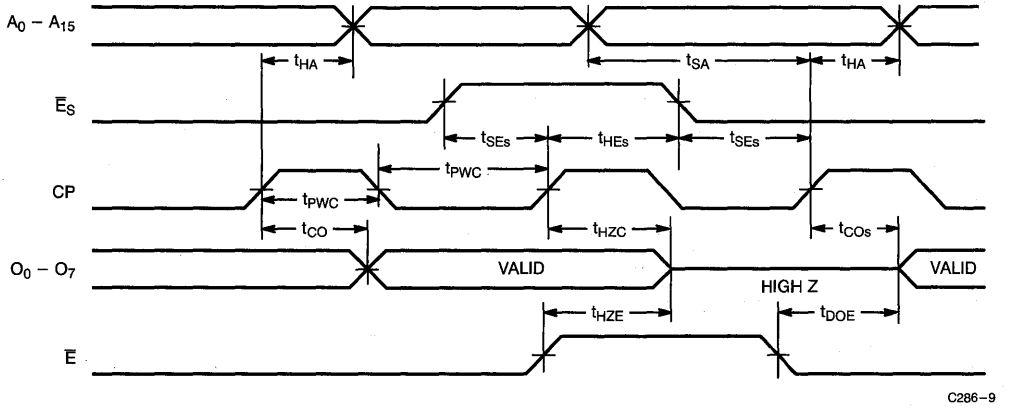
D_7 D_0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Switching Waveform for the 7C286



Switching Waveform for the 7C287



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C286 and 7C287 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C286 or 7C287 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C286 Mode Selection

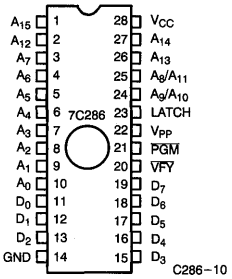
	Pin Number[8]				
	21	23	20	22	19–15, 13–11
Mode: Read or Output Disable	**A_{10}**	**A_{11}**	**$\overline{CE}$**	**$\overline{OE}$**	**$O_7 - O_0$**
Read	A_{10}	A_{11}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable	A_{10}	A_{11}	X	V_{IH}	High Z
Output Disable & Power Down	A_{10}	A_{11}	V_{IH}	X	High Z
Mode: Other	**$\overline{PGM}$**	**LATCH**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Program	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Blank Check	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Zeros

Table 2. CY7C287 Mode Selection

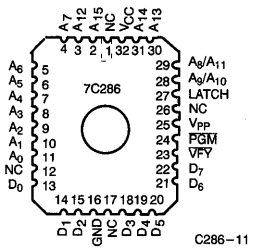
	Pin Function[8]				
	21	23	20	22	19–15, 13–11
Mode: Read or Output Disable	**CP**	**A_{14}**	**$\overline{E}$, $\overline{E}_S$**	**A_{15}**	**$O_7 - O_0$**
Synchronous Read	V_{IL}/V_{IH}	A_{14}	V_{IL}	A_{15}	$O_7 - O_0$
Output Disable – Asychronous	X	A_{14}	V_{IH}	A_{15}	High Z
Output Disable – Synchronous	V_{IL}/V_{IH}	A_{14}	V_{IH}	A_{15}	High Z
Mode: Other	**$\overline{PGM}$**	**LATCH**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Program	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Blank Check	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

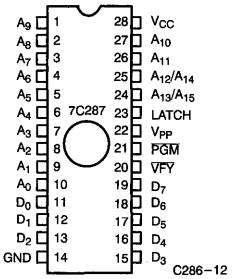
DIP



LCC



DIP



LCC

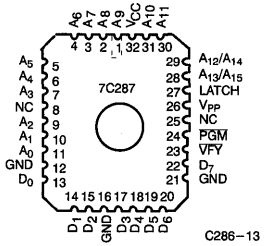


Figure 1. Programming Pinouts

Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
50	CY7C286–50PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C286–50WC	W16	28-Lead (600-Mil) Windowed CerDIP	
60	CY7C286–60PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C286–60WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C286–60DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C286–60LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C286–60QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C286–60WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
70	CY7C286–70PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C286–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C286–70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C286–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C286–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C286–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
80	CY7C286–80WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
	CY7C286–80QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C287–45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C287–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C287–55PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C287–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C287–65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C287–65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287–65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[10]	1, 2, 3

Switching Characteristics

Device	Parameter	Subgroups
7C286	t_{ACC}	7, 8, 9, 10, 11
	t_{CE}	7, 8, 9, 10, 11
	t_{OE}	7, 8, 9, 10, 11
7C287	t_{SA}	7, 8, 9, 10, 11
	t_{HA}	7, 8, 9, 10, 11
	t_{CO}	7, 8, 9, 10, 11
	t_{DOE}	7, 8, 9, 10, 11
	t_{PWC}	7, 8, 9, 10, 11

Note:
10. CY7C286 only.

Document #: 38−00103−G

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the CY7C291A/2A.

CY7C291
CY7C292

CYPRESS SEMICONDUCTOR

Reprogrammable 2K x 8 PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **—35 ns (commercial)**
  - **—35 ns (military)**
- **Low power**
  - **—330 mW (commercial)**
  - **—660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

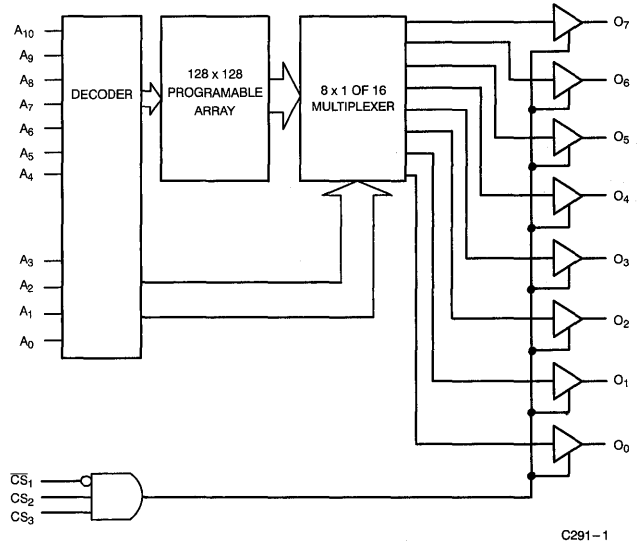
Functional Description

The CY7C291 and CY7C292 are high-performance 2048-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil wide plastic and hermetic DIP packages respectively. The 300-mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0 – A_{10}) will become available on the output lines (O_0 – O_7).

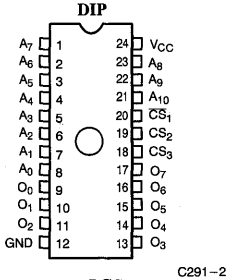
Logic Block Diagram



C291–1

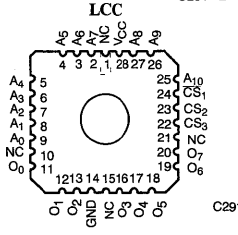
Pin Configurations

DIP



C291–2

LCC



C291–3

Window available on 300-mil cerdip only.

Selection Guide

			7C291–35 7C292–35	7C291–50 7C292–50
Maximum Access Time (ns)			35	50
Maximum Operating Current (mA)	STD	Commercial	90	90
		Military	120[1]	120
	L	Commercial	60	60

Note:
1. 7C291 only.

CY7C291A
CY7C292A/CY7C293A

CYPRESS SEMICONDUCTOR

Reprogrammable 2K x 8 PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial and military)**
- **Low standby power**
  - **— 220 mW (commercial and military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

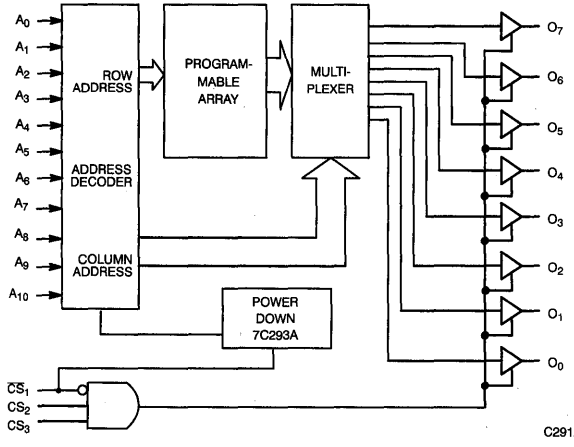
Functional Description

The CY7C291A, CY7C292A, and CY7C293A are high-performance 2K-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil (7C291A, 7C293A) and 600-mil wide plastic and hermetic DIP packages (7C292A). The CY7C293A has an automatic power down feature which reduces the power consumption by over 70% when deselected. The 300-mil ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C291A, CY7C292A, and CY7C293A are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

A read is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address line (A_0 – A_{10}) will become available on the output lines (O_0 – O_7).

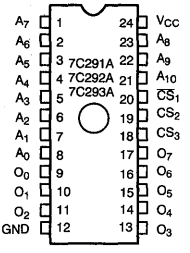
Logic Block Diagram



C291A–1

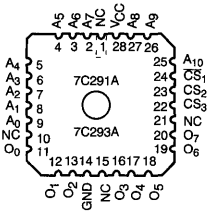
Pin Configurations

DIP
Top View



C291A–2

LCC/PLCC (Opaqe Only)
Top View



C291A–3

Window available on 7C291A and 7C293A only.

Selection Guide

			7C291A–20 7C292A–20 7C293A–20	7C291A–25 7C292A–25 7C293A–25 7C291AL–25 7C292AL–25 7C293AL–25	7C291A–35 7C292A–35 7C293A–35 7C291AL–35 7C292AL–35 7C293AL–35	7C291A–50 7C292A–50 7C293A–50 7C291AL–50 7C292AL–50 7C293AL–50
Maximum Access Time (ns)			20	25	35	50
Maximum Operating Current (mA)	Standard	Commercial	120	90	90	90
		Military		120	90	90
	L	Commercial		60	60	60
Standby Current (mA) 7C293A Only		Commercial	40	30	30	30
		Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±10%
Industrial[1]	− 40°C to + 85°C	5V ±10%
Military[2]	− 55°C to + 125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C291A−20 7C292A−20 7C293A−20 Min.	7C291A−20 7C292A−20 7C293A−20 Max.	7C291A−25 7C292A−25 7C293A−25 Min.	7C291A−25 7C292A−25 7C293A−25 Max.	7C291AL−25 7C292AL−25 7C293AL−25 Min.	7C291AL−25 7C292AL−25 7C293AL−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4						
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	− 20	− 90	− 20	− 90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		90		60	mA
			Mil				120			
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}	Com'l		40		30		30	mA
			Mil				40			
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

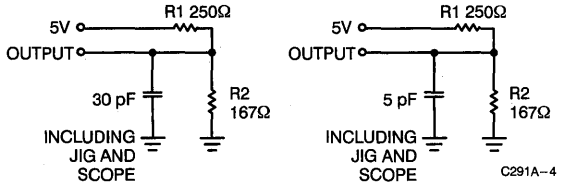
Electrical Characteristics Over the Operating Range[3, 4] (continued)

Parameter	Description	Test Conditions		7C291AL–35, 50 7C292AL–35, 50 7C293AL–35, 50		7C291A–35, 50 7C292A–35, 50 7C293A–35, 50		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	– 10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 10	+10	– 10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		– 20	– 90	– 20	– 90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT}=0 mA	Commercial		60		90	mA
			Military				90	
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}	Commercial		30		30	mA
			Military				40	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

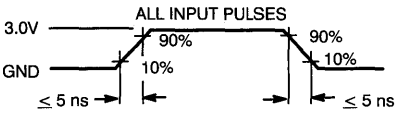
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

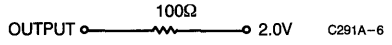
AC Test Loads and Waveforms[4]

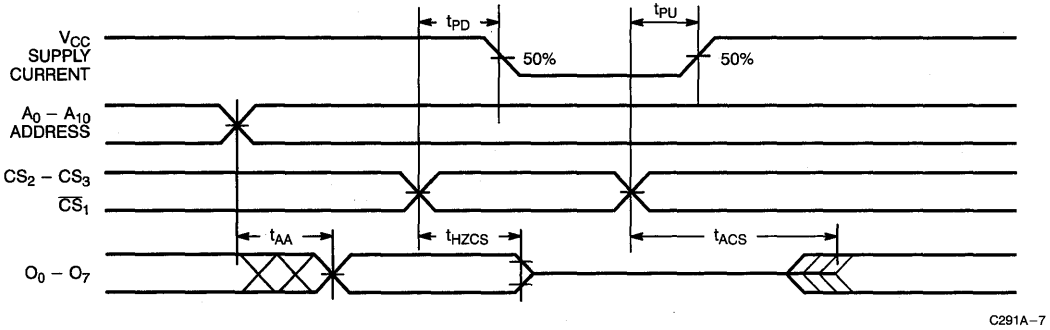


(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C291A-20 7C292A-20 7C293A-20		7C291A-25 7C292A-25 7C293A-25 7C291AL-25 7C292AL-25 7C293AL-25		7C291A-35 7C292A-35 7C293A-35 7C291AL-35 7C292AL-35 7C293AL-35		7C291A-50 7C292A-50 7C293A-50 7C291AL-50 7C292AL-50 7C293AL-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		50	ns
t_{HZCS1}	Chip Select Inactive to High Z		15		15		20		20	ns
t_{ACS1}	Chip Select Active to Output Valid		15		15		20		20	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C293A $\overline{CS_1}$ Only)[6]		22		27		35		45	ns
t_{ACS2}	Chip Select Active to Output Valid (7C293A $\overline{CS_1}$ Only)[6]		22		27		35		45	ns
t_{PU}	Chip Select Active to Power-Up (7C293A $\overline{CS_1}$ Only)	0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C293A $\overline{CS_1}$ Only)		22		27		35		45	ns

Notes:
6. t_{HZCS2} and t_{ACS2} refer to 7C293A $\overline{CS_1}$ only.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[7]				
	Read or Output Disable	$A_{10} - A_0$	CS_3	CS_2	$\overline{CS_1}$	$O_7 - O_0$
	Other	$A_{10} - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$D_7 - D_0$
Read		$A_{10} - A_0$	V_{IH}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable[8]		$A_{10} - A_0$	X	X	V_{IH}	High Z
Output Disable		$A_{10} - A_0$	X	V_{IL}	X	High Z
Output Disable		$A_{10} - A_0$	V_{IL}	X	X	High Z
Program		$A_{10} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{10} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{10} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_{10} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check Zeros		$A_{10} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Notes:

7. X = "don't care" but not to exceed V_{CC} +5%.
8. The power-down mode for the CY7C293A is activated by deselecting $\overline{CS_1}$.

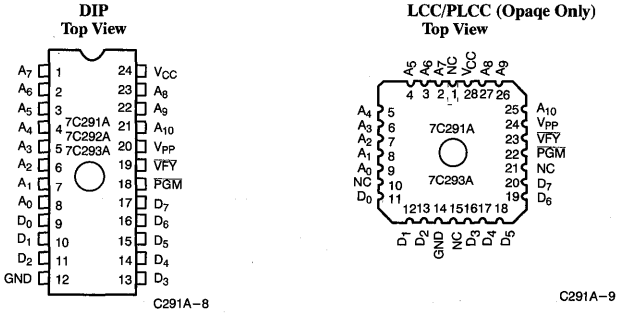
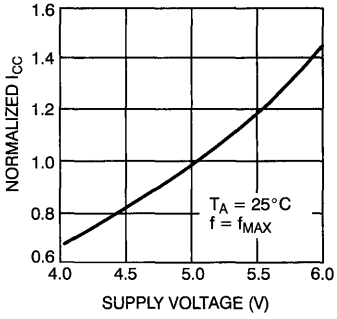


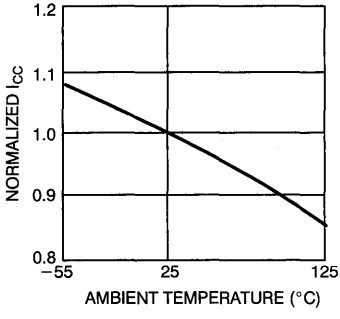
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

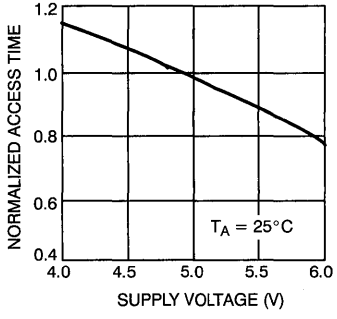
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

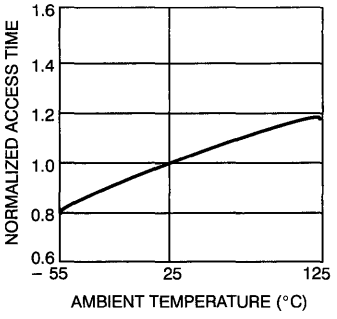


NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

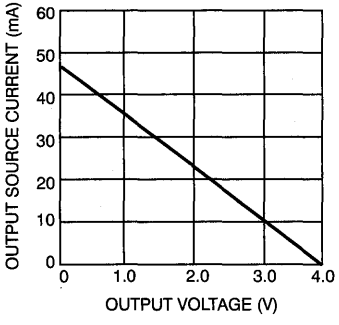


C291A–10

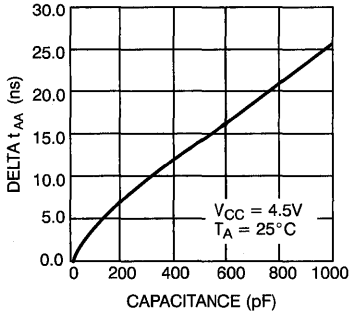
NORMALIZED ACCESS TIME vs. TEMPERATURE



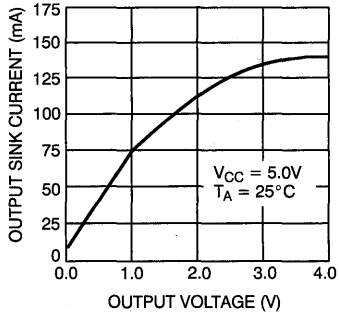
OUTPUT SOURCE CURRENT vs. VOLTAGE



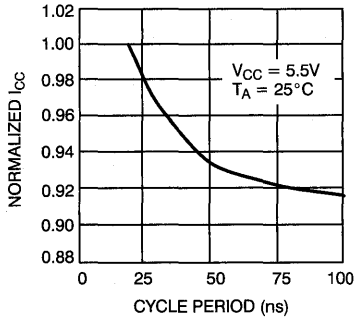
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



I_{CC} vs. CYCLE PERIOD



C291A–11

Ordering Information[9]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C291A–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291A–20PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–20SC	S13	24-Lead Molded SOIC	
		CY7C291A–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	60	CY7C291AL–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C291A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–25SC	S13	24-Lead Molded SOIC	
		CY7C291A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	CY7C291A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–25TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	120	CY7C291A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–30LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–30TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	60	CY7C291AL–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–35SC	S13	24-Lead Molded SOIC	Commercial
		CY7C291A–35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	CY7C291A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–35LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–35TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
50	60	CY7C291AL–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–50PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–50SC	S13	24-Lead Molded SOIC	Commercial
		CY7C291A–50PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–50DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–50TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:
9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[9] (continued)

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C292A–20DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–20PC	P11	24-Lead (600-Mil) Molded DIP	
25	120	CY7C292A–25DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–25PC	P11	24-Lead (600-Mil) Molded DIP	
		CY7C292A–25DMB	D12	24-Lead (600-Mil) CerDIP	Military
30	120	CY7C292A–30DMB	D12	24-Lead (600-Mil) CerDIP	Military
35	60	CY7C292AL–35PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	90	CY7C292A–35DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–35PC	P11	24-Lead (600-Mil) Molded DIP	
	120	CY7C292A–35DMB	D12	24-Lead (600-Mil) CerDIP	Military
50	60	CY7C292AL–50PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	90	CY7C292A–50DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–50PC	P11	24-Lead (600-Mil) Molded DIP	
	120	CY7C292A–50DMB	D12	24-Lead (600-Mil) CerDIP	Military

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C293A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C293A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		CY7C293A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	120	CY7C293A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–30LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	60	CY7C293AL–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–35LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
50	60	CY7C293AL–50PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293AL–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–50PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–50DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[10]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[11]	7, 8, 9, 10, 11
t_{ACS2}[10]	7, 8, 9, 10, 11

Notes:
10. 7C293A only.
11. 7C291A and 7C292A only.

Document #: 38-00075-G

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-87650	01KX	CY7C291-50TMB
5962-87650	01LX	CY7C291-50WMB
5962-87650	013X	CY7C291-50QMB
5962-87650	03KX	CY7C291-35TMB
5962-87650	03LX	CY7C291-35WMB
5962-87650	033X	CY7C291-35QMB
5962-88680	01LX	CY7C293A-50WMB
5962-88680	01KX	CY7C293A-50TMB
5962-88680	013X	CY7C293A-50QMB
5962-88680	02LX	CY7C293A-35WMB
5962-88680	02KX	CY7C293A-35TMB
5962-88680	023X	CY7C293A-35QMB
5962-88680	03LX	CY7C293A-30WMB
5962-88680	03KX	CY7C293A-30TMB
5962-88680	033X	CY7C293A-30QMB
5962-88680	04LX	CY7C293A-25WMB
5962-88680	04KX	CY7C293A-25TMB
5962-88680	043X	CY7C293A-25QMB
5962-88734	02JX	CY7C292A-45DMB
5962-88734	02KX	CY7C291A-45KMB
5962-88734	02LX	CY7C291A-45DMB
5962-88734	023X	CY7C291A-45LMB
5962-88734	03JX	CY7C292A-35DMB
5962-88734	03KX	CY7C291A-35KMB
5962-88734	03LX	CY7C291A-35DMB
5962-88734	033X	CY7C291A-35LMB
5962-88734	04JX	CY7C292A-25DMB
5962-88734	04KX	CY7C291A-25KMB
5962-88734	04LX	CY7C291A-25DMB
5962-88734	043X	CY7C291A-25LMB

PROM Programming Information

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970s and continue to provide the highest-speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are intact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a programming system. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. The result of this inability to completely test is less than 100% yield during programming by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the late 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than bipolar and, coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point of view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate, which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. When these cells are programmed, the performance of each cell in the memory can be tested, ensuring that we ship devices that program every time and will perform as specified when programmed. In addition, when these devices are supplied in a windowed package they can be programmed and erased indefinitely providing the designer a reprogrammable PROM for development.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Programming Algorithm

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis, unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data-out pins during the programming operation, and the data is read from these same pins for verification that the byte has been programmed.

Blank Check for Differential Cells

Since a differential cell contains neither a 1 not a 0 before it is programmed, the conventional blank check is not valid. For this reason, Cypress CMOS PROMs that use differential cells contain a special blank check mode of operation. Blank check is performed by separately examining the 0 and 1 sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes: one comparing the 0 side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier, and then repeating this operation for the 1 side of the cell. The modes are called blank check ones and blank check zeros. These modes are entered by applying a supervoltage to the device.

Blank Check for Single-Ended Cells

Single-ended cells blank check in a conventional manner. An erased device contains all 0s and a programmed cell will contain a 1. Cypress PROMs that use the single-ended approach provide a specific mode to perform the blank check, which also provides the verify function. This makes the need to switch high voltages unnecessary during the program verify operation. See specific datasheets for details.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a read and write pin in the programming mode. These are active-LOW signals and cause the data on the output pins to be written into the addressed memory location in the case of the write signal or read out of the device in the case of the read signal. When both the read and write signals are HIGH, the outputs are disabled and in a high-impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the write signal. Verification of data is accomplished by reading the information on the output pins while the read signal is active.

The timing for actual programming is supplied in the unique programming specifications for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable Initial Byte

and Programmable Synchronous/Asynchronous Enable available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

Programming Support

Programming support for Cypress CMOS PROMs is available on Cypress's QuickPro II. Support is also available from a number of programmer manufacturers, some of which are listed below.

AVAL Data Corp.
M. K. Bldg. 2F 4–8 Nakaitabashi,
Itabashi–ku
Tokyo, Japan 173
03 (5375)–7321

BP Microsystems
10681 Haddington, Ste. #190
Houston, TX 77043
(800) 225–2102

Cypress Semiconductor, Inc.
3901 North First St.
San Jose, CA 95134
(408) 943–2600

Data I/O
Customer Resource Center
10525 Willows Rd. NE
P.O. Box 97046
Redmond, WA 98073–9746
(800) 247–5700
(206) 881–6444

Logical Devices Inc.
692 South Military Trail
Deerfield, FL 33442
(305) 428–6868

Microprоss
Parc d'Activite des Pres
5, rue Denis-Papin
59650 Villenueve-d'Ascq. France
(20) 47.90.40

Minato Electronics
4105, Minami Yamada-cho
Kohoku-ku
Yokohama, Japan 223
(045) 591–5611

SMS Mikrocomputersystem GmbH
Im Grund 15
D–7988 Wangen im Allgeau
BRD
(49) 7522–5018

SMS Microcomputer
P.O. Box 1348
Lawrence, MA 01842
(508) 683–4659

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988–1118

System General
510 S. Park Victoria
Milpitas, CA 95035
(408) 263–6667

Document #: 38–00235

CYPRESS SEMICONDUCTOR

Section Contents

PLDs (Programmable Logic Devices)

Introduction to Cypress PLDs

Cypress PLD Family Features

Cypress Semiconductor's PLD family offers the user a wide range of programmable logic solutions that incorporate leading-edge circuit design techniques as well as diverse process technology capabilities. This allows Cypress PLD users to select PLDs that best suit the needs of their particular high-performance system, regardless of whether speed, power consumption, density, or device flexibility are the critical requirements imposed by the system.

Cypress offers enhanced-performance industry-standard 20- and 24-pin device architectures, proprietary 28-pin application-tailored architectures and highly flexible 28- to 84-pin universal device architectures. The range of technologies offered includes leading-edge 0.8-micron CMOS EPROM for high speed, low power, and high density, 0.8-micron bipolar for the highest-speed ECL devices, 0.8-micron BiCMOS for high-speed, power-sensitive applications, and 0.65-micron FLASH technology for high speed, low power and electrical alterability.

The reprogrammable memory cells used by Cypress serve the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or product terms are connected via the reprogrammable memory cell to both the true and complement inputs. When the reprogrammable memory cell is programmed, the inputs from a gate or product term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or product term. This is similar to "blowing" the fuses of BiCMOS or bipolar fusible devices, which disconnects the input gate from the product term. Selective programming of each of these reprogrammable memory cells enables the specific logic function to be implemented by the user.

The programmability of Cypress's PLDs allows the users to customize every device in a number of ways to implement their unique logic requirements. Using PLDs in place of SSI or MSI components results in more effective utilization of board space, reduced cost and increased reliability. The flexibility afforded by these PLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The PLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output, and product terms to the desired application.

PLD Notation

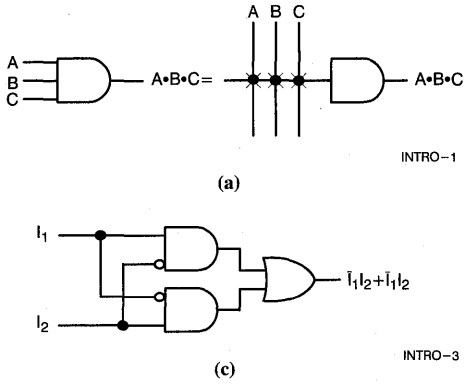
To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In part (a), an "×" represents an unprogrammed EPROM cell or intact fuse link that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in part (b), which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in part (c).

PLD Circuit Configurations

Cypress PLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows designers to select PLDs that best fit their applications. An example of some of the configurations that are available are listed below.

Programmable I/O

Figure 2 illustrates the programmable I/O offered in the Cypress PLD family that allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, when the three-state output is disabled, the I/O pin can be used as an input to the array.



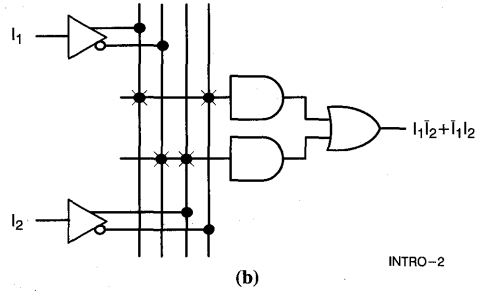


Figure 1. Logic Diagram Conventions

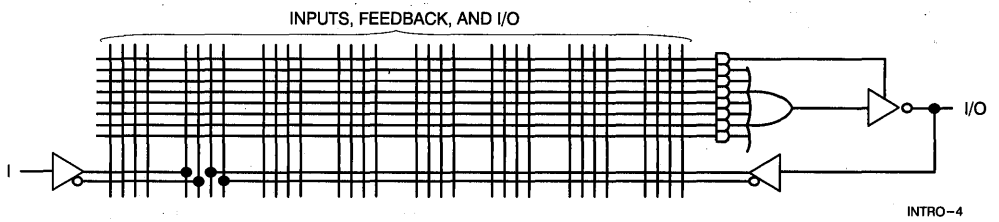


Figure 2. Programmable I/O

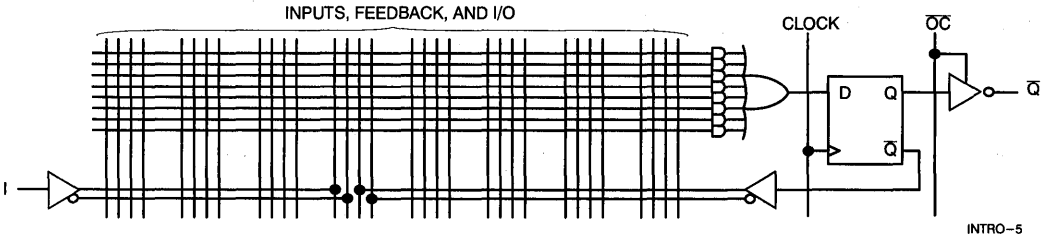


Figure 3. Registered Outputs with Feedback

Registered Outputs with Feedback

Figure 3 illustrates the registered outputs offered on a number of the Cypress PLDs which allow any of these circuits to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift, and branch.

Programmable Macrocell

The programmable macrocell, illustrated in *Figure 4*, provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "registered" or "combinatorial." Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a bidirectional I/O controlled by the programmable array (see *Figure 5*).

Buried Register Feedback

The CY7C330 and CY7C331 PLDs provide registers that may be "buried" or "hidden" by electing feedback of the register output. These buried registers, which are useful in state machines, may be implemented without sacrificing the use of the associated device pin as an input. In previous PLDs, when the feedback path was activated, the input pin-path to the logic array was blocked. The proprietary CY7C330 reprogrammable synchronous state machine macrocell illustrates the shared input multiplexer, which provides an alternative input path for the I/O pin associated with a buried macrocell register (*Figure 6*). Each pair of macrocells shares an input multiplexer, and as long as alternate macrocells are buried, up to six of the twelve output registers can be buried without the loss of any I/O pins as inputs. The CY7C330 also contains four dedicated hidden macrocells with no external output that are used as additional state registers for creating high-performance state machines (*Figure 7*).

Asynchronous Register Control

Cypress also offers PLDs that may be used in asynchronous systems in which register clock, set, and reset are controlled by the outputs of the product term array. The clock signal is created by the processing of external inputs and/or internal feedback by the logic of the product term array, which is then routed to the register clock. The register set and reset are similarly controlled by product term outputs and can be triggered at any time independent of the register clock in response to external and/or feedback inputs processed by the logic array. The proprietary CY7C331 Asynchronous Registered PLD, for which the I/O macrocell is illustrated in *Figure 8*, is an example of such a device. The register clock, set, and reset functions of the CY7C331 are all controlled by product terms and are dependent only on input signal timing and combinatorial delay through the device logic array to enable their respective functions.

Input Register Cell

Other Cypress PLDs provide input register cells to capture short duration inputs that would not otherwise be present at the inputs long enough to allow the device to respond. Both the proprietary CY7C330 Reprogrammable Synchronous State Machine and the proprietary CY7C332 Combinatorial PLD provide these input register cells (*Figure 9*). The clock for the input register may be provided from one of two external clock input pins selectable by a configuration bit, C4, dedicated for this purpose for each input register. This choice of input register clock allows signals to be captured and processed from two independent system sources, each controlled by its own independent clock. These input register cells are provided within I/O macrocells, as well as for dedicated input pins.

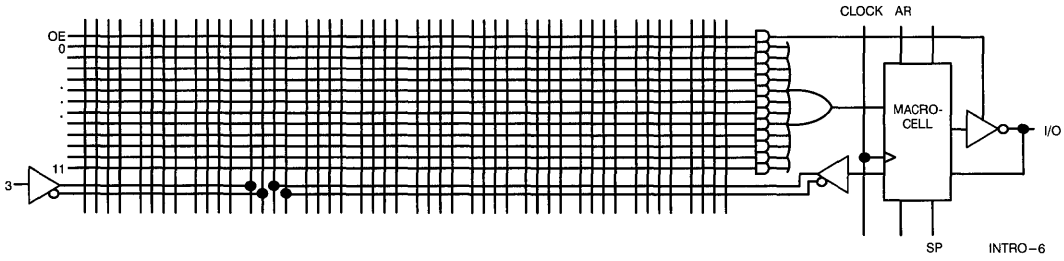


Figure 4. Programmable Macrocell

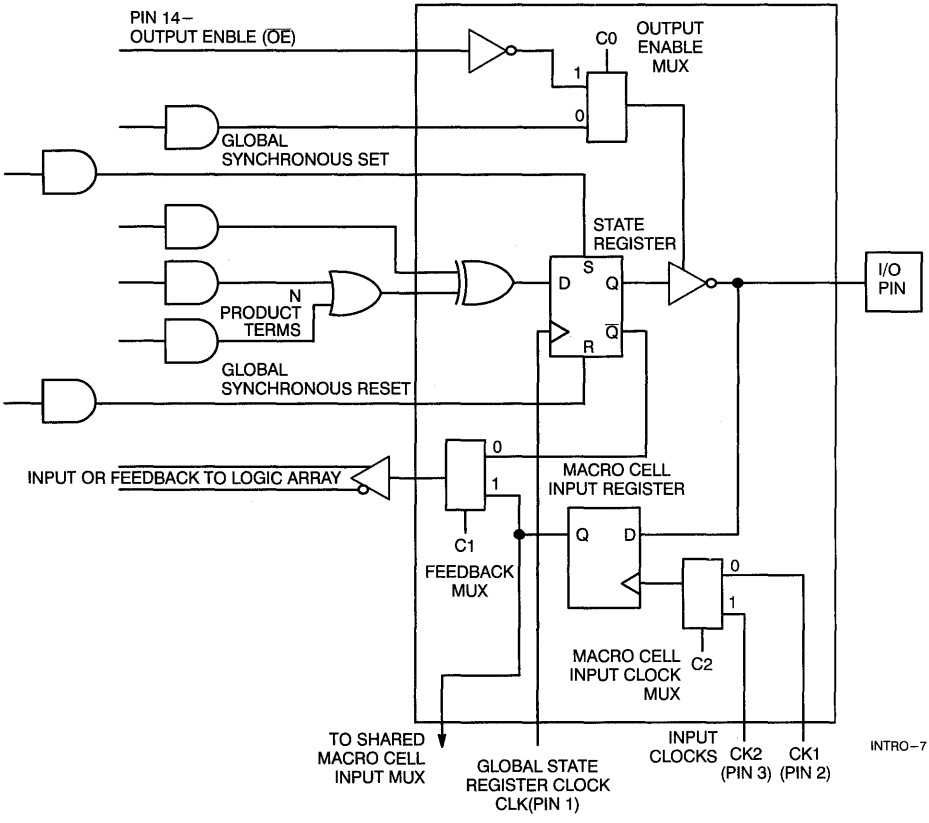


Figure 5. CY7C330 I/O Macrocell

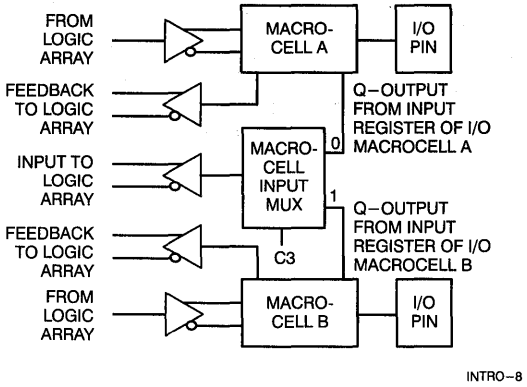


Figure 6. CY7C330 I/O Macrocell Pair Shared Input MUX

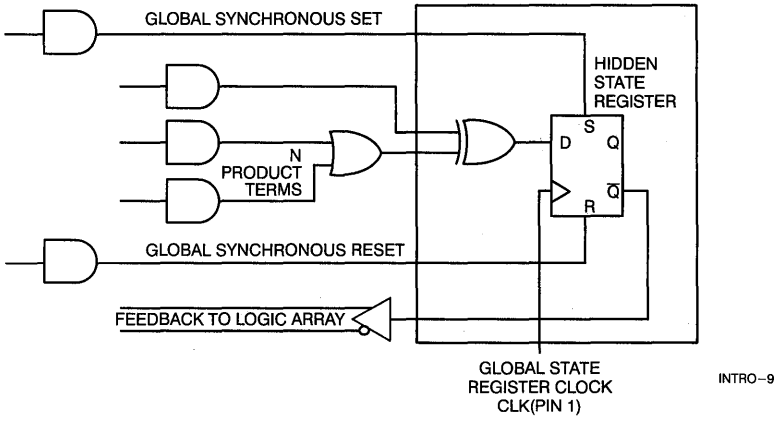


Figure 7. CY7C330 Hidden State Register Macrocell

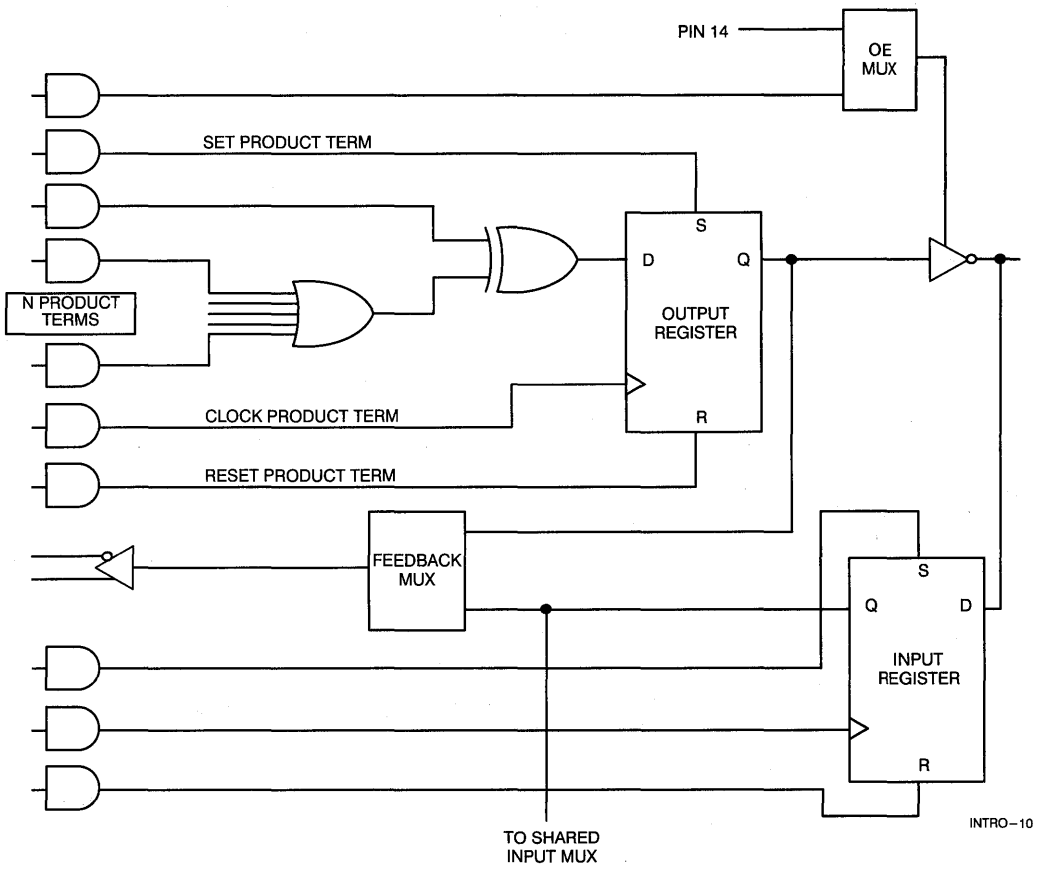


Figure 8. CY7C331 Registered Asynchronous Macrocell

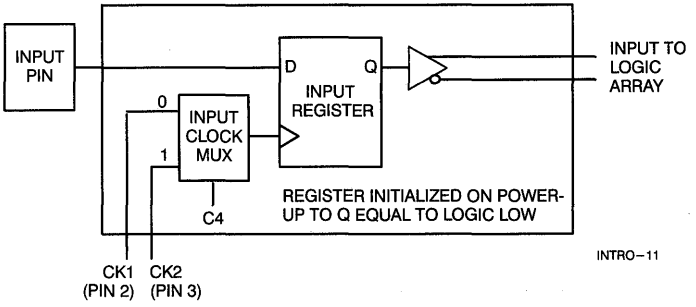


Figure 9. CY7C330 Dedicated Input Cell

Document #: 38–00165–A

This is an abbreviated datasheet. The complete CY7C258/9 datasheet is listed in the PROM section of this Data Book.

CY7C258
CY7C259

CYPRESS SEMICONDUCTOR

2K x 16 Reprogrammable State Machine PROM

Features

- **High speed: 100-MHz operation**
  - **— t_{CP} = 10 ns**
  - **— t_{CKO} = 8 ns**
  - **— t_{AS} = 2 ns**
- **16-bit-wide state word**
- **Can be programmed as asynchronous PROM t_{AA} = 18 ns**
- **Optimum speed/ power**
- **Individually bypassable input and output registers**
- **Individually programmable address/ feedback muxes**
- **Synchronous and asynchronous chip select**
- **Synchronous and asynchronous $\overline{INIT}$ and programmable initialize word**
- **16 outputs (CY7C259)**
- **Software support**
- **CY7C258 available in 28-pin, 300-mil plastic and ceramic DIP, LCC, PLCC**
- **CY7C259 available in 44-pin LCC and PLCC**
- **Reprogrammable in windowed packages**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C258 and CY7C259 are 2K x 16 CMOS PROMs specifically designed for use in state machine applications.

State machines are one of the most common applications for registered PROMs. The CY7C258 and CY7C259 feature internal state feedback and a variety of programmable features to support 100-MHz state machines with as many as 2,048 distinct states.

It is easy to use a PROM as a state machine. Each array location contains output data as well as information fed back to select the next state. Note that a PROM is only limited by the number of array inputs. If a given state machine can be implemented in the number of inputs/ feedbacks available (11 on the CY7C258/259), then it will always fit in the device. No software minimization is required.

Among the programmable features of the CY7C258/CY7C259 are individually bypassable input and output registers. The registers run off the same clock for pipeline capability. Each individual register can be programmed to capture data at the rising edge of the clock or to be transparent.

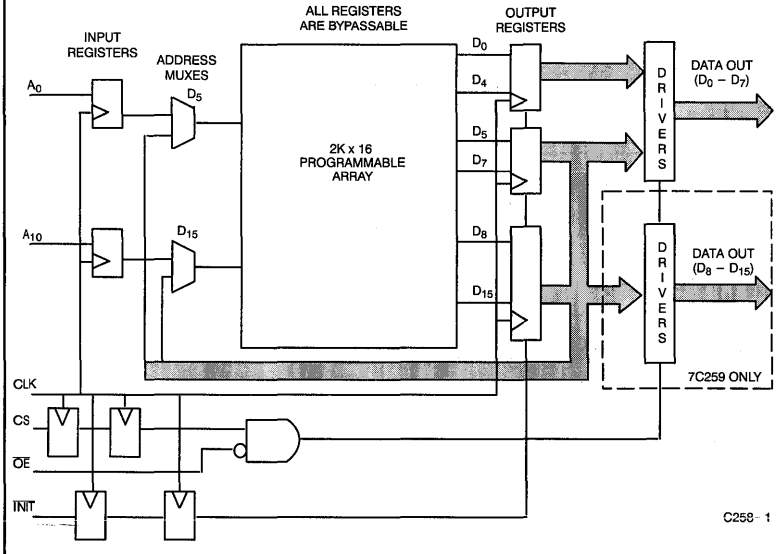
The registers at the inputs are useful for signals that require short set-up times (t_{AS} = 2 ns). The input register does introduce a cycle of latency, however. For signals that directly affect the next state of the machine, each input register can be bypassed. Note that the cycle time remains the same (10-ns min.), even if the inputs are bypassed.

Registers at the output are used to hold both state information and output data. These registers are also bypassable for maximum flexibility. Occasionally, an individual output cannot wait for the next clock edge. These outputs are sometimes called Mealy outputs, and can be created by bypassing the appropriate output register.

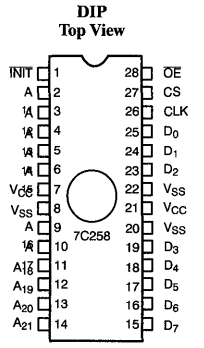
Since the CY7C258 and CY7C259 contain a 2K array, they each require 11 inputs. Each of these inputs can come from an input pin or from internal output register feedback. Eleven individually programmable address muxes allow the user to select the ratio of pin input and state feedback.

These devices have both an asynchronous output ($\overline{OE}$) and a synchronous chip select (CS).

Logic Block Diagram



Pin Configurations



CYPRESS SEMICONDUCTOR

CMOS Generic 20-Pin Programmable Logic Device

Features

- **Fast**
  - **— Commercial: t_{PD} = 12 ns, t_{CO} = 10 ns, t_S = 10 ns**
  - **— Military/Industrial: t_{PD} = 15 ns, t_{CO} = 12 ns, t_S = 12 ns**
- **Low power**
  - **— I_{CC} max. of 110 mA**
- **Commercial, industrial, and military temperature range**
- **User-programmable output cells**
  - **— Selectable for registered or combinatorial operation**
  - **— Output polarity control**
  - **— Output enable source selectable from pin 11 or product term**
- **Generic architecture to replace standard logic functions including: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - **— Uses proven EPROM technology**
  - **— Fully AC and DC tested**
  - **— Security feature prevents logic pattern duplication**
  - **— >2000V input protection for electrostatic discharge**

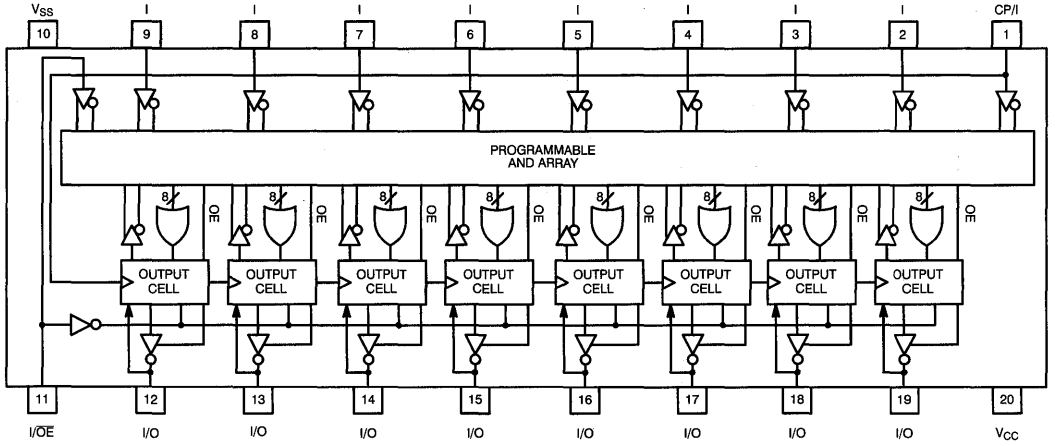
Functional Description

Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure, providing users with the ability to program custom logic functions for unique requirements.

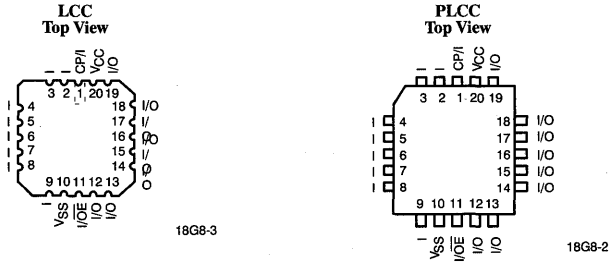
In an unprogrammed state, the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLD C18G8 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable

Logic Block Diagram, DIP and SOJ Pinout



Pin Configurations



Selection Guide

Generic Part Number	I_{CC} (mA)		t_{PD} (ns)		t_S		t_{CO}	
	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind
18G8–12	90		12		10		10	
18G8–15	90	110	15	15	12	12	12	12
18G8–15L	70		15		12		12	
18G8–20		110		20		15		15

Functional Description (continued)

element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit, reducing the customer's need to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

18G8 Functional Description

The PLDC18G8 is a generic 20-pin device that can be programmed to logic functions which include but are not limited to: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8. Thus, the PLDC18G8 provides significant design, inventory, and programming flexibility over dedicated 20-pin devices. It is executed in a 20-pin, 300-mil molded DIP and a 300-mil windowed cerDIP. It provides up to 18 inputs and 8 outputs. When the windowed cerDIP is exposed to UV light, the 18G8 is erased and can then be reprogrammed.

The programmable output cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with registered or combinatorial outputs, active HIGH or active LOW outputs, and product term or Pin 11 generated output enables. Four architecture bits determine the configurations as shown in the Configuration Table. A total of sixteen different configurations are possible. The default or unprogrammed state is registered/active LOW/Pin 11 OE. The entire programmable output cell is shown in *Figure 1.*

Architecture bit C1 controls the registered/combinatorial option. In either combinatorial or registered configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either registered or combinatorial configuration, the output of the register may be fed back to the array. This allows the creation of state machines by providing storage and feedback of the current system state. The register is clocked by the signal from Pin 1. The register is initialized upon power-up to Q output LOW and $\overline{Q}$ output HIGH.

In both the combinatorial and registered configurations, the source of the output enable signal can be individually chosen with architecture bit C2. The $\overline{OE}$ signal may be generated within the array or from the external $\overline{OE}$ (Pin 11). Pin 11 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for output polarity. The output can be either active HIGH or active LOW. This option is controlled by architecture bit C0.

Along with this increase in functional density, the Cypress PLDC18G8 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature.

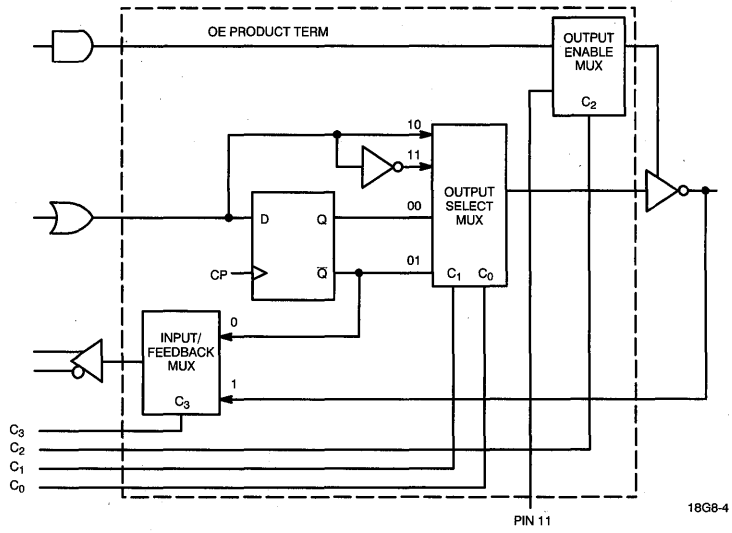


Figure 1. Programmable Output Cell

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 24 mA

DC Programming Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Industrial	− 40°C to +85°C	5V ±10%
Military[1]	− 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Commercial	2.4		V
			I_{OH} = − 2 mA	Military/Industrial			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.5	V
			I_{OL} = 12 mA	Military/Industrial			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			− 10	+10	µA
V_{PP}		Programming Voltage @ I_{PP} = 50 mA Max.			12.0	13.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]			− 30	− 90	mA
I_{CC}	Power Supply Current	V_{IN} = 0, V_{CC} = Max., I_{OUT} = 0 mA		Commercial −15L		70	mA
				Commercial −12, −15		90	mA
				Military/Industrial		110	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 40	+40	µA

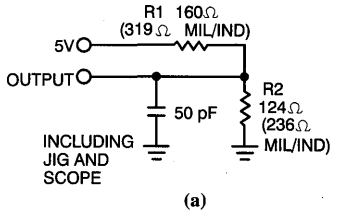
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V	10	pF

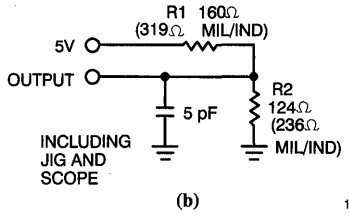
Notes:

1. T_A is the "instant on" case temperature.
2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



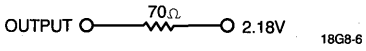
(a)



(b)

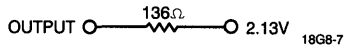
18G8-5

Equivalent to: THEVENIN EQUIVALENT (Commercial)



18G8-6

Equivalent to: THEVENIN EQUIVALENT (Military/Industrial)



18G8-7

Configuration Table[5]

C_3	C_2	C_1	C_0	Configuration
0	0	0	0	Active LOW, Registered Mode, Registered Feedback, Pin 11 OE
0	0	0	1	Active HIGH, Registered Mode, Registered Feedback, Pin 11 OE
0	0	1	0	Active LOW, Combinatorial Mode, Registered Feedback, Pin 11 OE
0	0	1	1	Active HIGH, Combinatorial Mode, Registered Feedback, Pin 11 OE
0	1	0	0	Active LOW, Registered Mode, Registered Feedback, Product Term OE
0	1	0	1	Active HIGH, Registered Mode, Registered Feedback, Product Term OE
0	1	1	0	Active LOW, Combinatorial Mode, Registered Feedback, Product Term OE
0	1	1	1	Active HIGH, Combinatorial Mode, Registered Feedback, Product Term OE
1	0	0	0	Active LOW, Registered Mode, Pin Feedback, Pin 11 OE
1	0	0	1	Active HIGH, Registered Mode, Pin Feedback, Pin 11 OE
1	0	1	0	Active LOW, Combinatorial Mode, Pin Feedback, Pin 11 OE
1	0	1	1	Active HIGH, Combinatorial Mode, Pin Feedback, Pin 11 OE
1	1	0	0	Active LOW, Registered Mode, Pin Feedback, Product Term OE
1	1	0	1	Active HIGH, Registered Mode, Pin Feedback, Product Term OE
1	1	1	0	Active LOW, Combinatorial Mode, Pin Feedback, Product Term OE
1	1	1	1	Active HIGH, Combinatorial Mode, Pin Feedback, Product Term OE

Notes:
5. In the virgin or unprogrammed state, a configuration bit is in the "0" state.

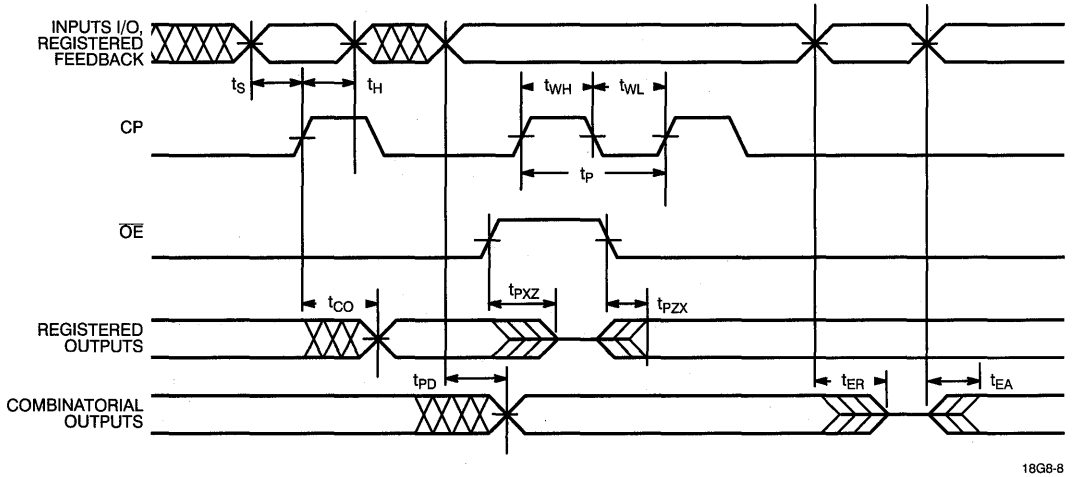
Switching Characteristics Over the Operating Range[1, 6, 7]

Parameters	Description	Commercial				Military/Industrial				Units
		−12		−15, −15L		−15		−20		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		12		15		15		20	ns
t_{EA}	Input to Output Enable		12		15		15		20	ns
t_{ER}	Input to Output Disable		12		15		15		20	ns
t_{PZX}	Pin 11 to Output Enable		10		12		12		15	ns
t_{PXZ}	Pin 11 to Output Disable		10		10		10		15	ns
t_{CO}	Clock to Output		10		12		12		15	ns
t_S	Input or Feedback Set-Up Time	10		12		12		15		ns
t_H	Hold Time	0		0		0		0		ns
t_P[8]	Clock Period	22		24		27		35		ns
t_{WH}	Clock High Time	7		8		9		10		ns
t_{WL}	Clock Low Time	8		9		10		11		ns
f_{MAX}[9]	Maximum Frequency	50.0		41.6		41.6		33.3		MHz

Notes:

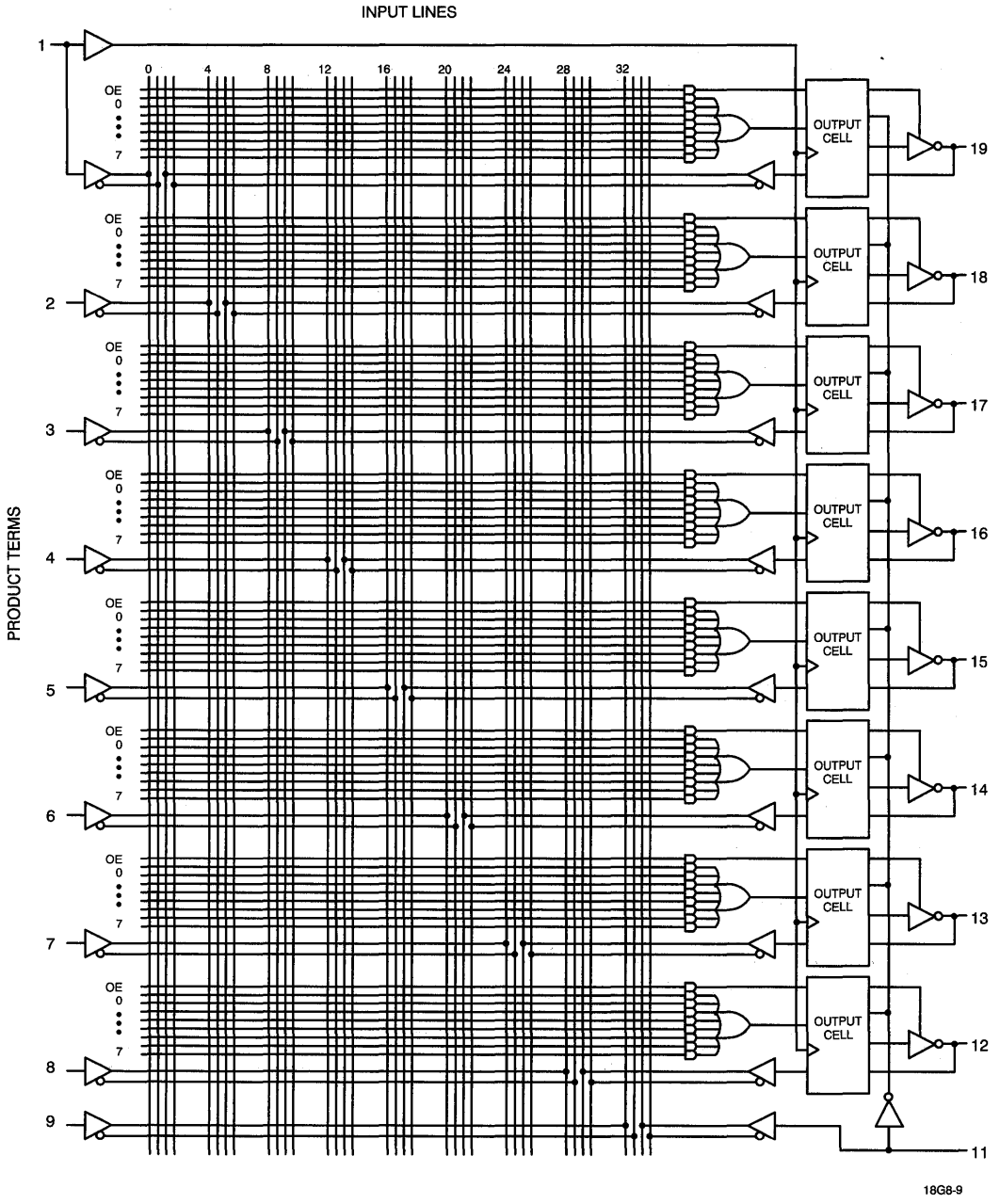
6. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms is used for t_{ER}, t_{PZX}, and t_{PXZ}.
7. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} − 0.5V for an enabled HIGH output or V_{OL} + 0.5V for an enabled LOW input.
8. t_P or minimum guaranteed clock period, is the clock period guaranteed for state machine operation and is calculated from $t_P = t_S + t_{CO}$. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of ($t_{WH} + t_{WL}$) or ($t_S + t_H$).
9. f_{MAX}, or minimum guaranteed operating frequency, is the operating frequency guaranteed for state machine operation and is calculated from $f_{MAX} = 1/(t_S + t_{CO})$. The minimum guaranteed f_{MAX} for registered data path operation (no feedback) can be calculated as the lower of $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$.

Switching Waveform



18G8-8

Functional Logic Diagram



Ordering Information

I_{CC} (mA)	Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	12	PLDC18G8–12JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
		PLDC18G8–12PC	P5	20-Lead (300-Mil) Molded DIP	
		PLDC18G8–12VC	V5	20-Lead (300-Mil) Molded SOJ	
		PLDC18G8–12WC	W6	20-Lead (300-Mil) Windowed CerDIP	
70	15	PLDC18G8L–15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
		PLDC18G8L–15PC	P5	20-Lead (300-Mil) Molded DIP	
		PLDC18G8L–15VC	V5	20-Lead (300-Mil) Molded SOJ	
		PLDC18G8L–15WC	W6	20-Lead (300-Mil) Windowed CerDIP	
90	15	PLDC18G8–15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
		PLDC18G8–15PC	P5	20-Lead (300-Mil) Molded DIP	
		PLDC18G8–15VC	V5	20-Lead (300-Mil) Molded SOJ	
		PLDC18G8–15WC	W6	20-Lead (300-Mil) Windowed CerDIP	
110	15	PLDC18G8–15JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
		PLDC18G8–15PI	P5	20-Lead (300-Mil) Molded DIP	
		PLDC18G8–15WI	W6	20-Lead (300-Mil) Windowed CerDIP	
110	15	PLDC18G8–15DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PLDC18G8–15LMB	L61	20-Pin Square Leadless Chip Carrier	
		PLDC18G8–15QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
		PLDC18G8–15WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
110	20	PLDC18G8–20JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
		PLDC18G8–20PI	P5	20-Lead (300-Mil) Molded DIP	
		PLDC18G8–20WI	W6	20-Lead (300-Mil) Windowed CerDIP	
110	20	PLDC18G8–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PLDC18G8–20LMB	L61	20-Pin Square Leadless Chip Carrier	
		PLDC18G8–20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
		PLDC18G8–20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

AC Characteristics

Parameters	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–00080–E

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYPRESS SEMICONDUCTOR

PAL®C20 Series

Reprogrammable CMOS PALC 16L8, 16R8, 16R6, 16R4

Features

- **CMOS EPROM technology for reprogrammability**
- **High performance at quarter power**
  - **—t_{PD} = 25 ns**
  - **—t_S = 20 ns**
  - **—t_{CO} = 15 ns**
  - **—I_{CC} = 45 mA**
- **High performance at military temperature**
  - **—t_{PD} = 20 ns**
  - **—t_S = 20 ns**
  - **—t_{CO} = 15 ns**
  - **—I_{CC} = 70 mA**
- **Commercial and military temperature range**
- **High reliability**
  - **—Proven EPROM technology**
  - **—>1500V input protection from electrostatic discharge**
  - **—100% AC and DC tested**
  - **—10% power supply tolerances**
  - **—High noise immunity**
  - **—Security feature prevents pattern duplication**
  - **—100% programming and functional testing**

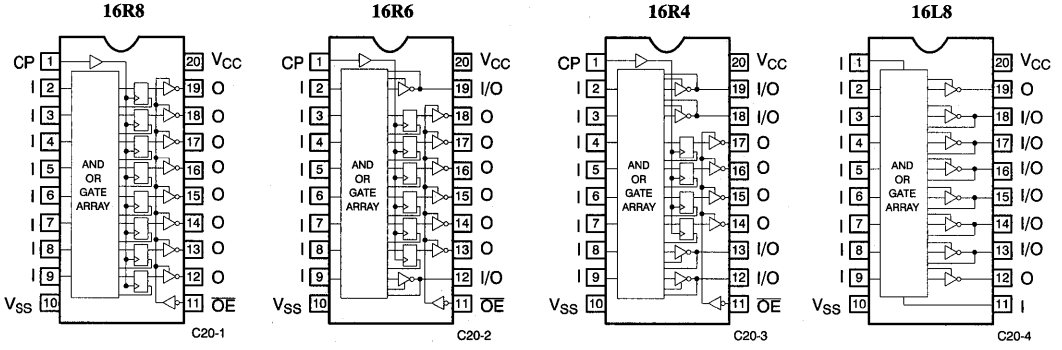
Functional Description

Cypress PALC20 Series devices are high-speed electrically programmable and UV-erasable logic devices produced in a proprietary N-well CMOS EPROM process. These devices utilize a sum-of-products (AND-OR) structure providing users with the ability to program custom logic functions serving unique requirements.

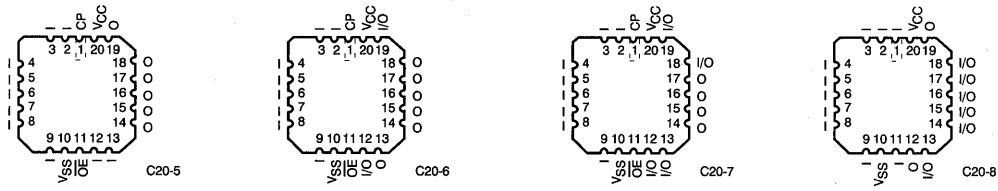
PALs are offered in 20-pin plastic and ceramic DIP, plastic SOJ, and ceramic LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

Before programming, AND gates or product terms are connected via EPROM cells to both true and complement inputs. Programming an EPROM cell disconnects an input term from a product term. Selective programming of these cells allows a specific logic function to be implemented in a PALC device. PALC devices are supplied in four functional configurations designated 16R8, 16R6, 16R4, and 16L8. These 8 devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the 4 functional variations of the product family.

Logic Symbols and DIP and SOJ Pinouts



LCC Pinouts



PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the $\overline{Q}$ bar side of the register fed back into the main array. The registers are automatically initialized upon power-up to Q output LOW and $\overline{Q}$ output HIGH. All unused inputs should be tied to ground.

All PALC devices feature a security function that provides the user with protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope.

Cypress PALC products are produced in an advanced 1.2-micron N-well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming, and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested, and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. Combining these inherent and designed-in features provides an extremely high degree of functionality, programmability and assured AC performance, and testing becomes an easy task.

The register preload allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

Commercial and Industrial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
				L	Com'l/Ind	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)	t_{PD} (ns)			t_S (ns)			t_{CO} (ns)		
					-20	-30	-40	-20	-30	-40	-20	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	30	40	—	—	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	—	—	20	25	35	15	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional										
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional										

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C
Ambient Temperature with Power Applied ..... − 55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... − 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V
DC Input Voltage ..... − 3.0V to +7.0V
Output Current into Outputs (LOW) ..... 24 mA
DC Programming Voltage 14.0V
UV Exposure ..... 7258 Wsec/cm^2
Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[1]	− 55°C to +125°C	5V ±10%
Industrial	− 40°C to +85°C	

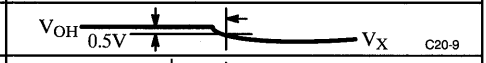
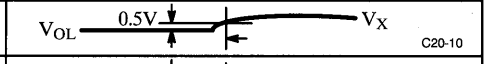
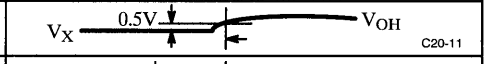
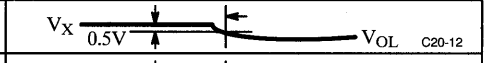
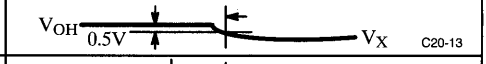
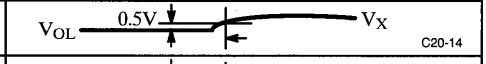
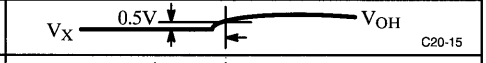
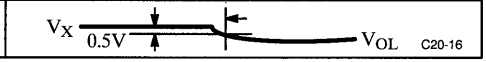
Electrical Characteristics Over the Operating Range (unless otherwise noted)[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = − 2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l/Ind		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[3] Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[3] Voltage for All Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			− 10	10	µA
V_{PP}	Programming Voltage	I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]				− 300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA[5]		"L"		45	mA
				Com'l/Ind		70	mA
				Military		70	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 100	100	µA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. $I_{CC(AC)}$ = (0.6 mA/MHz) × (Operating Frequency in MHz) + $I_{CC(DC)}$. $I_{CC(DC)}$ is measured with an unprogrammed device.

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2] (continued)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	 C20-9
t_{PXZ} (+)	2.6V	 C20-10
t_{PZX} (+)	V_{thc}	 C20-11
t_{PZX} (−)	V_{thc}	 C20-12
t_{ER} (−)	1.5V	 C20-13
t_{ER} (+)	2.6V	 C20-14
t_{EA} (+)	V_{thc}	 C20-15
t_{EA} (−)	V_{thc}	 C20-16

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	10	pF

Switching Characteristics Over Operating Range[2, 7, 8]

Parameter	Description	Commercial/Industrial				Military						Unit
		−25		−35		−20		−30		−40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{ER}	Input to Output Disable Delay 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		15		25		15		20		25	ns
t_S	Input or Feedback Set-Up Time 16R8, 16R6, 16R4	20		30		20		25		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		0		0		0		ns
t_P	Clock Period	35		55		35		45		60		ns
t_W	Clock Width	15		20		12		20		25		ns
f_{MAX}	Maximum Frequency		28.5		18		28.5		22		16.5	MHz

Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. Part (a) (part (c) for military) of AC Test Loads and Waveforms is used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. Part (b) (part (d) for military) of AC Test Loads and Waveforms is used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} − 0.5V for an enabled HIGH output or V_{OL} + 0.5V for an enabled LOW output. Please see Electrical Characteristics for waveforms and measurement reference levels.

PAL®20 Series
16L8/16R8
16R6/16R4

CYPRESS SEMICONDUCTOR

4.5-ns, Industry-Standard PLDs

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 4.5 ns**
  - **— t_S = 2.5 ns**
  - **— f_{MAX} = 142.9 MHz (external)**
- **Popular industry standard architectures**
- **Power-up RESET**
- **High reliability**
  - **— Proven Ti-W fuses**
  - **— AC and DC tested at the factory**
- **Security fuse**

Functional Description

Cypress PAL20 Series devices consist of the PAL16L8, PAL16R8, PAL16R6, and PAL16R4. Using BiCMOS process and Ti-W fuses, these devices implement the familiar sum-of-products (AND-OR) logic structure.

The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms while the OR array sums selected terms at the outputs.

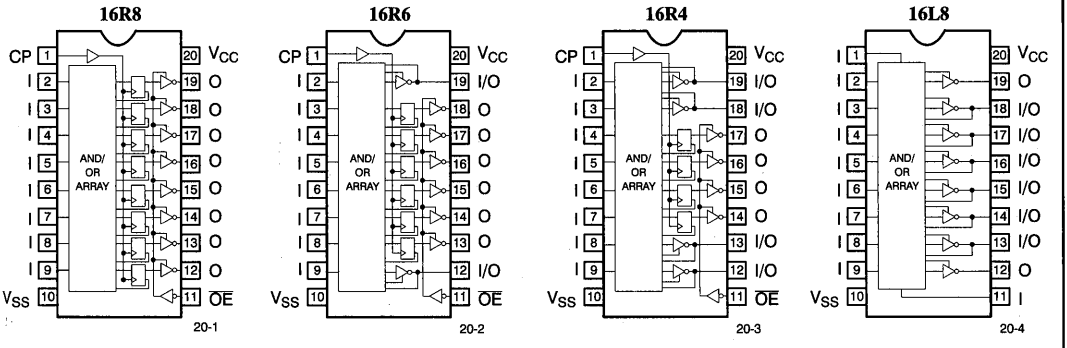
The product selector guide details all the different options available. All the registered devices feature power-up RESET. The register Q output is set to a logic LOW when power is applied to the devices.

A security fuse is provided on all the devices to prevent copying of the device fuse pattern.

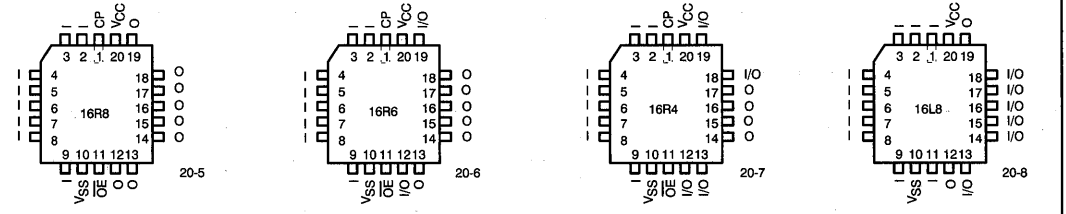
Programming

The PAL20 Series devices can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, BP Microsystems, Advin, B&C Microsystems, and other programmers. Please contact your local Cypress representative for further information.

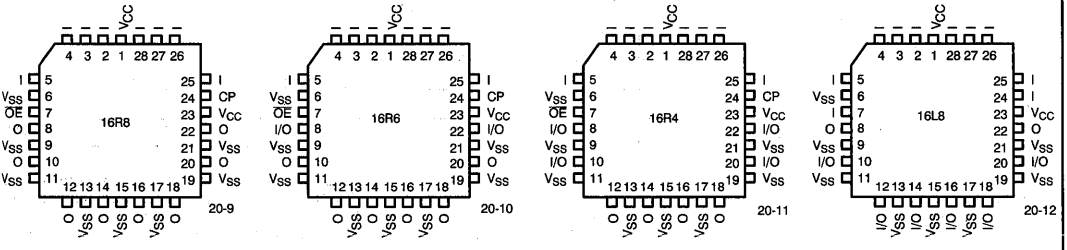
Logic Symbols and DIP Pinouts



20-Pin PLCC/LCC Pinouts



28-Pin PLCC (−4 Speed Bin Only) Pinouts



PAL is a registered trademark of Monolithic Memories Inc.

CYPRESS SEMICONDUCTOR

Function Selection Guide

Device	Dedicated Inputs	Outputs	Product Terms/Outputs	Feedback	Enable
PAL16L8	10	6 comb. 2 comb.	7 7	I/O —	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Speed Selection Guide (Commercial −4/−5/−7, Military −7/−10)

Speed Bin	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	f_{MAX} (MHz)	I_{CC} (mA)
−4	4.5	2.5	4.5	142.9	180
−5	5	2.5	5	133.3	180
−7	7	3.5	6	105.3	180
−10	10	4.5	7	87.0	180

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage ..... − 1.2V to V_{CC} + 0.5V

DC Input Current (except during programming) ..... − 30 mA to +5 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Military[1]	− 55°C to +125°C	5V ±10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Commercial	2.4		V
			I_{OH} = − 2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	0.4V ≤ V_{IN} ≤ 2.7V, V_{CC} = Max.[3]			−250	50	µA
I_I	Maximum Input Current	V_{IN} = 5.5V, V_{CC} = Max.				1	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} ≤ V_{OUT} ≤ V_{CC}[3]			−100	+100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−130	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open				180	mA

Notes:

1. T_A is the "instant on" case temperature.
2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. I/O pin leakage is the worse case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[5]

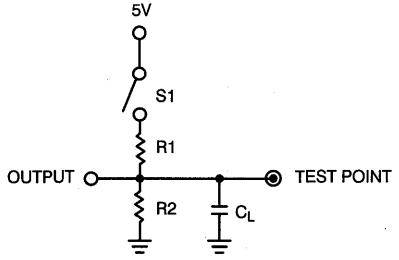
Parameter	Description		Test Conditions	Typical	Unit
C_{IN}	Input Capacitance	CP, $\overline{OE}$	T_A = 25°C, f = 1 MHz, V_{IN} = 0, V_{CC} = 5.0V	8	pF
		$I_1 - I_8$		5	pF
C_{OUT}	Output Capacitance			8	pF

Switching Characteristics Over the Operating Range[6]

Parameter	Description		-4		-5		-7		-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		1	4.5	1	5	2	7	2	10	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		2	6.5	2	6.5	2	7	2	10	ns
t_{ER}	Input to Output Disable Delay 16L8, 16R6, 16R4		2	5.5	2	5.5	2	7	2	10	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		1	6	1	6	2	7	2	10	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		1	5	1	5	2	7	2	10	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		1	4.5	1	5	2	6	2	7	ns
t_{SKEWR}	Skew Between Registered Outputs 16R8, 16R6, 16R4[5]			0.75		1		1		1	ns
t_S	Input or Feedback Set-Up Time 16R8, 16R6, 16R4		2.5		2.5		3.5		4.5		ns
t_H	Hold Time 16R8, 16R6, 16R4		0		0		0		0		ns
t_P	Clock Period (t_{CO} + t_S)		7		7.5		9.5		11.5		ns
t_W	Clock Width		3		3		3.5		5		ns
f_{MAX}	Maximum Frequency	External Feedback (1/tp)[7]		142.9		133.3		105.3		87	MHz
		Internal Feedback[5, 8]		175		175		150		133	

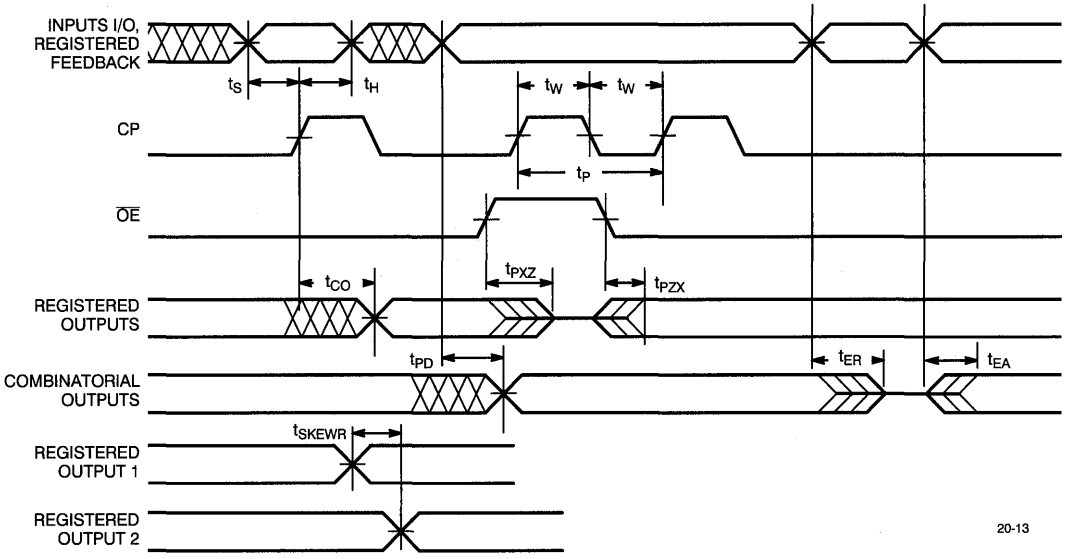
Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. See the last page of this specification for Group A subgroup testing information.
7. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
8. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate.

AC Test Loads and Waveforms



Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t_{PZX}, t_{EA}	Z ➧ H: Open Z ➧ L: Closed						1.5V
t_{PXZ}, t_{ER}	H ➧ Z: Open L ➧ Z: Closed	5 pF					H ➧ Z: V_{OH} − 0.5V L ➧ Z: V_{OL} + 0.5V

Switching Waveforms[9]



Note:
9. Input rise and fall time is 2-ns typical.

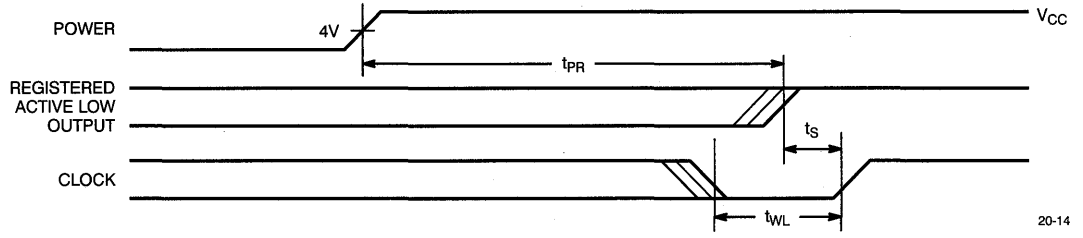
Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

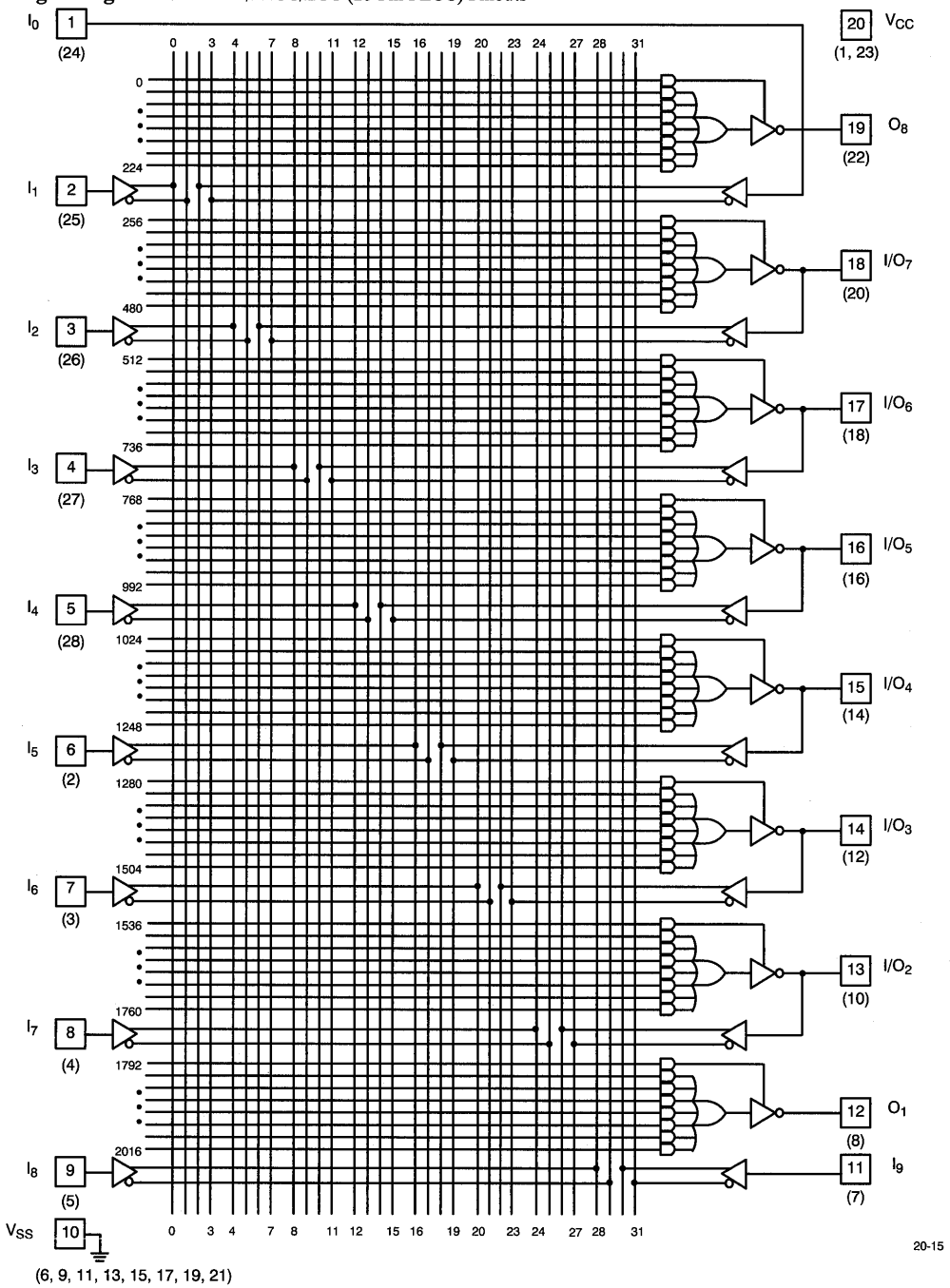
1. The V_{CC} must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback set-up times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Set-Up Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

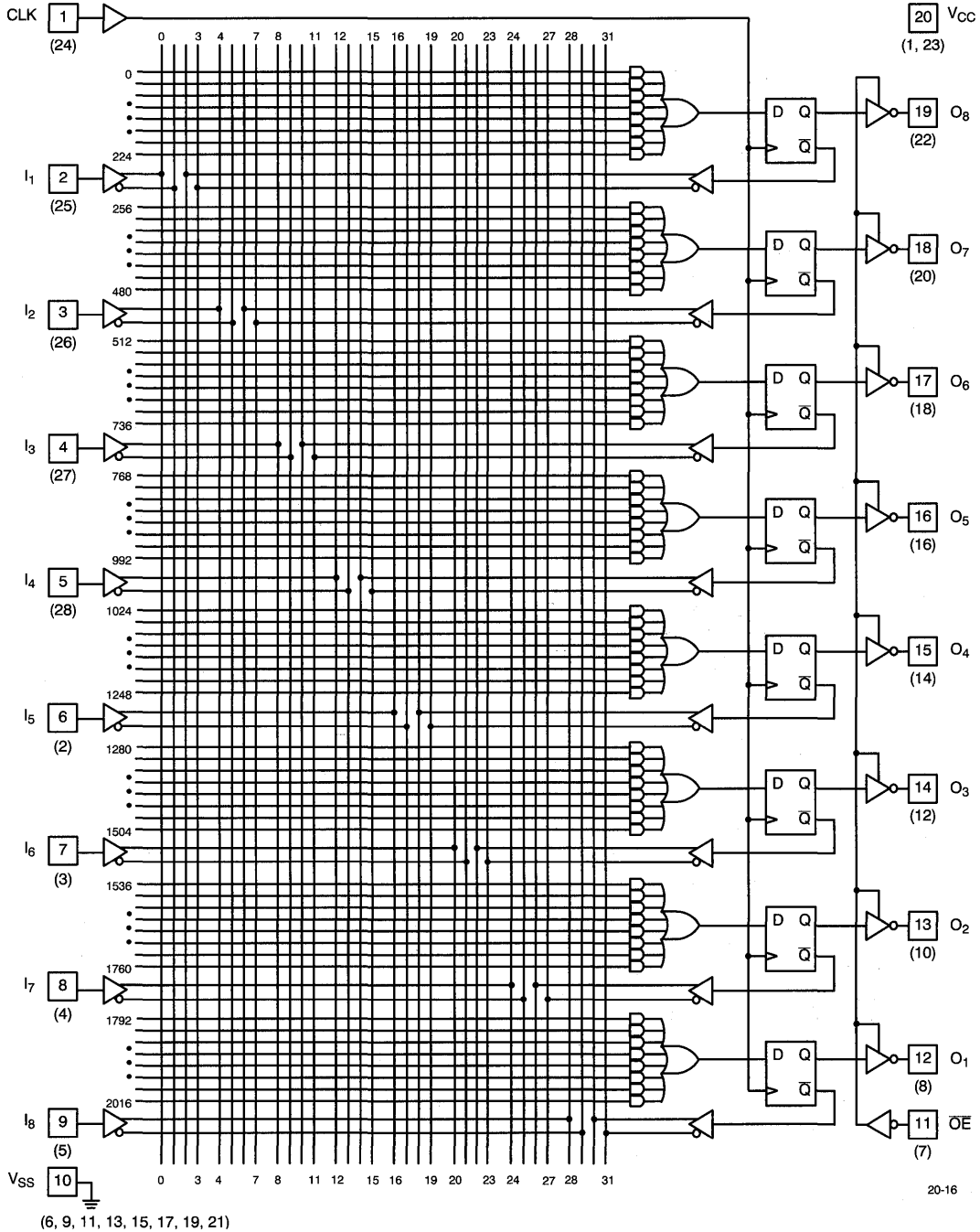
Power-Up Reset Waveform



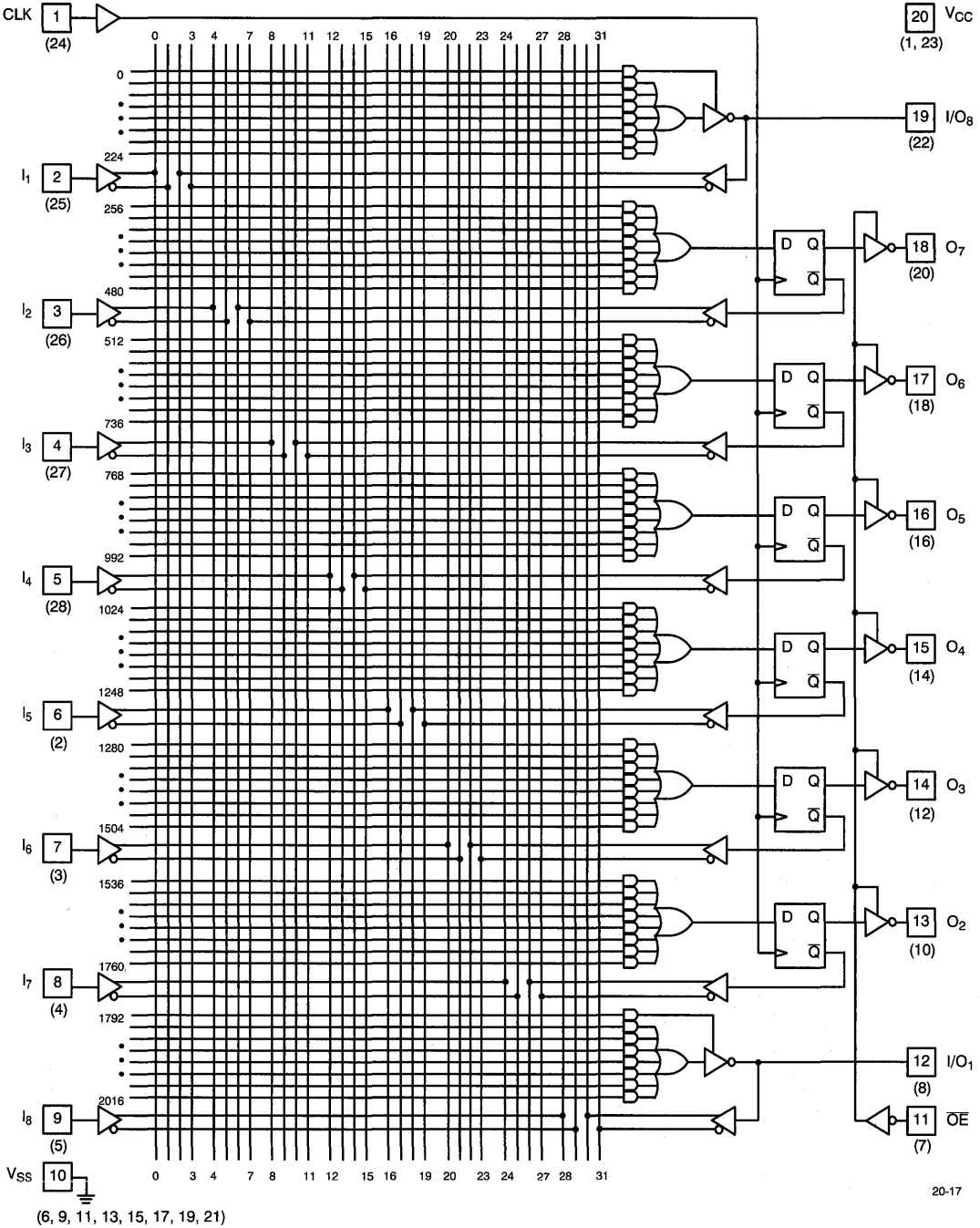
16L8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



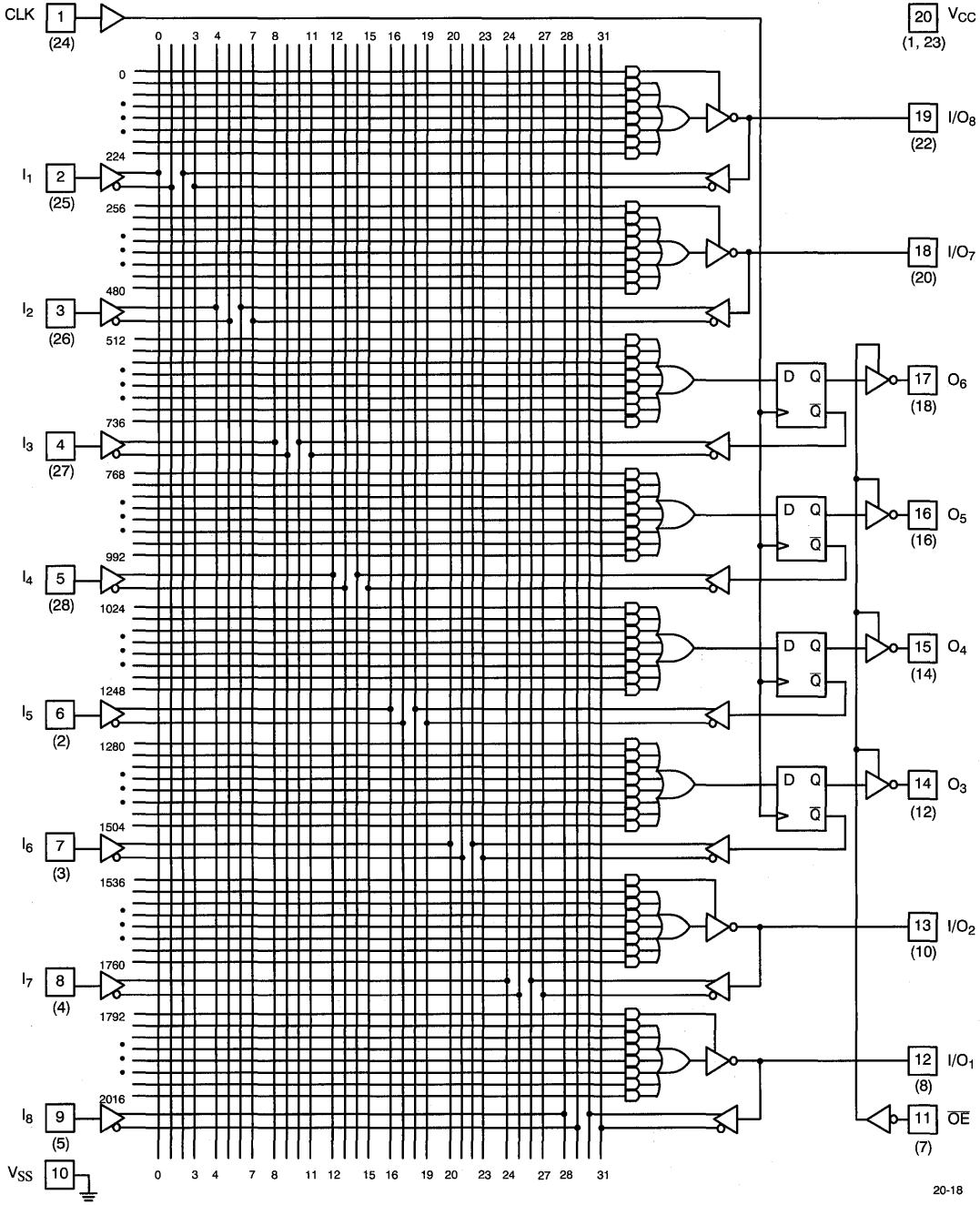
16R8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



16R6 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



16R4 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



CYPRESS SEMICONDUCTOR

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	PAL16L8–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	PAL16L8–5DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16L8–5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	PAL16L8–7DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16L8–7PC	P5	20-Lead (300-Mil) Molded DIP	
		PAL16L8–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PAL16L8–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	PAL16L8–10DMB	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–10LMB	L61	20-Pin Square Leadless Chip Carrier	

I_{CC} (mA)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	142.9	PAL16R8–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	133.3	PAL16R8–5DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16R8–5PC	P5	20-Lead (300-Mil) Molded DIP	
	105.3	PAL16R8–7DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16R8–7PC	P5	20-Lead (300-Mil) Molded DIP	
		PAL16R8–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PAL16R8–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	87	PAL16R8–10DMB	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–10LMB	L61	20-Pin Square Leadless Chip Carrier	

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	142.9	PAL16R6–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	133.3	PAL16R6–5DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R6–5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	105.3	PAL16R6–7DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R6–7PC	P5	20-Lead (300-Mil) Molded DIP	
			PAL16R6–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
			PAL16R6–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	87	PAL16R6–10DMB	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–10LMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information (continued)

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	142.9	PAL16R4–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	133.3	PAL16R4–5DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R4–5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	105.5	PAL16R4–7DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R4–7PC	P5	20-Lead (300-Mil) Molded DIP	
			PAL16R4–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
			PAL16R4–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	87	PAL16R4–10DMB	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4–10LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
V_{PP}	1, 2, 3
I_{CC}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–A–00025–C

PLDC20G10B/PLDC20G10

CMOS Generic 24-Pin Reprogrammable Logic Device

Features

- **Fast**
  - **Commercial: t_{PD} = 15 ns, t_{CO} = 10 ns, t_S = 12 ns**
  - **Military: t_{PD} = 20 ns, t_{CO} = 15 ns, t_S = 15 ns**
- **Low power**
  - **I_{CC} max.: 70 mA, commercial**
  - **I_{CC} max.: 100 mA, military**
- **Commercial and military temperature range**
- **User-programmable output cells**
  - **Selectable for registered or combinatorial operation**
  - **Output polarity control**
  - **Output enable source selectable from pin 13 or product term**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - **Uses proven EPROM technology**
  - **Fully AC and DC tested**
  - **Security feature prevents logic pattern duplication**
  - **±10% power supply voltage and higher noise immunity**

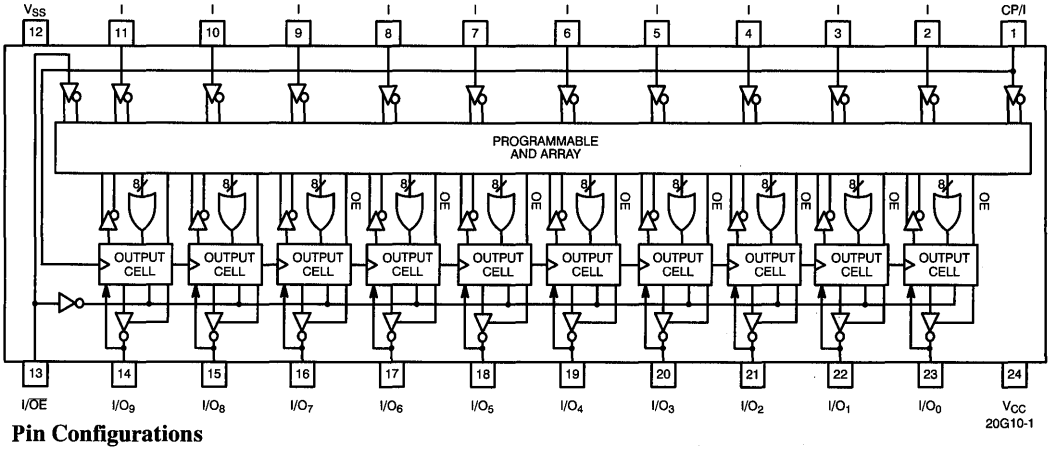
Functional Description

Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

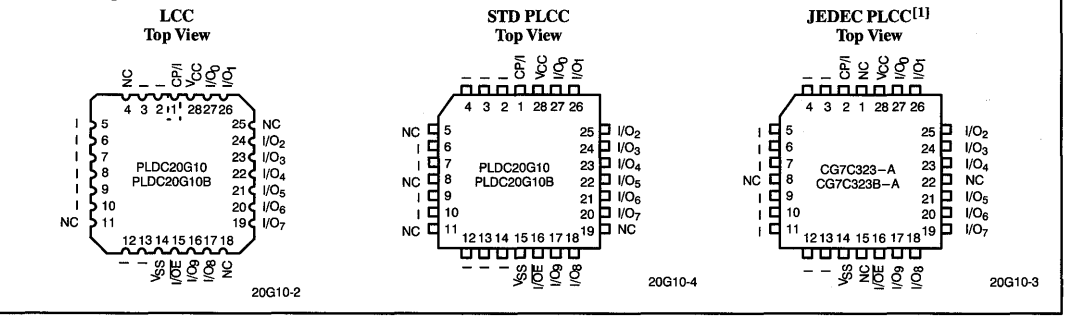
In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLDC20G10 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent

Logic Block Diagram



Pin Configurations



Note:

1. The CG7C323 is the PLDC20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The difference is in the location of the "no connect" or NC pins.

Selection Guide

Generic Part Number	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
20G10B–15	70		15		12		10	
20G10B–20	70	100	20	20	12	15	12	15
20G10B–25		100		25		18		15
20G10–25	55		25		15		15	
20G10–30		80		30		20		20
20G10–35	55		35		30		25	
20G10–40		80		40		35		25

Functional Description (continued)

advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

20G10 Functional Description

The PLDC20G10 is a generic 24-pin device that can be programmed to logic functions that include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8. Thus, the PLDC20G10 provides significant design, inventory and programming flexibility over dedicated 24-pin devices. It is executed in a 24-pin 300-mil molded DIP and a 300-mil windowed cerDIP. It provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The programmable output cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with registered or combinatorial outputs, active HIGH or active LOW outputs, and product term or Pin 13 generated output enables. Three architecture bits determine the configurations as shown in the Configuration Table and in *Figures 1* through *8*. A total of eight different configurations are possible, with the two most common shown in *Figure 3* and *Figure 5*. The default or unprogrammed state is registered/active/LOW/Pin 11 OE. The entire programmable output cell is shown in the next section.

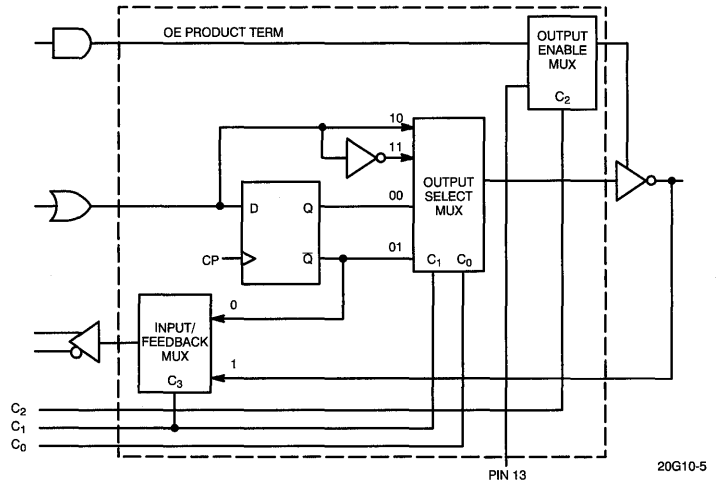
The architecture bit 'C1' controls the registered/combinatorial option. In either combinatorial or registered configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either registered or combinatorial configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and $\overline{Q}$ output HIGH.

In both the combinatorial and registered configurations, the source of the output enable signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external $\overline{OE}$ (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for output polarity. The output can be either active HIGH or active LOW. This option is controlled by architecture bit 'C0'.

Along with this increase in functional density, the Cypress PLDC20G10 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature.

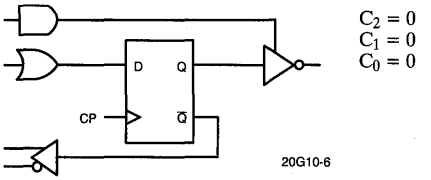
Programmable Output Cell



Configuration Table

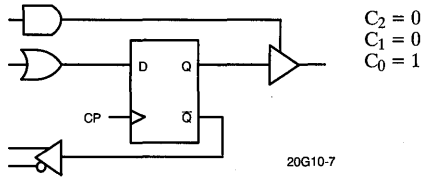
Figure	C_2	C_1	C_0	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin 13 OE/Registered/Active LOW
4	1	0	1	Pin 13 OE/Registered/Active HIGH
7	1	1	0	Pin 13 OE/Combinatorial/Active LOW
8	1	1	1	Pin 13 OE/Combinatorial/Active HIGH

Registered Output Configurations



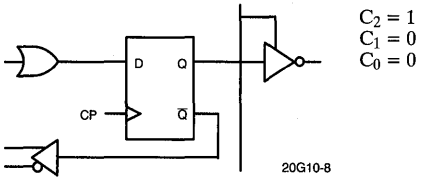
$C_2 = 0$
$C_1 = 0$
$C_0 = 0$

Figure 1. Product Term OE/Active LOW



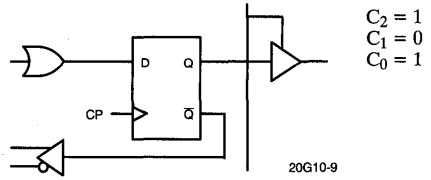
$C_2 = 0$
$C_1 = 0$
$C_0 = 1$

Figure 2. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 0$
$C_0 = 0$

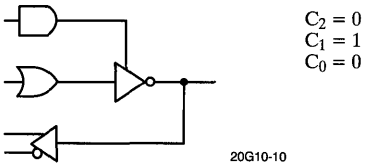
Figure 3. Pin 13 OE/Active LOW



$C_2 = 1$
$C_1 = 0$
$C_0 = 1$

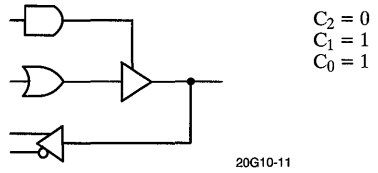
Figure 4. Pin 13 OE/Active HIGH

Combinatorial Output Configurations[2]



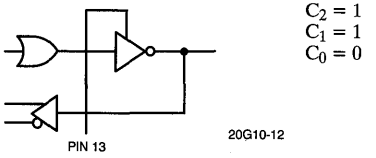
$C_2 = 0$
$C_1 = 1$
$C_0 = 0$

Figure 5. Product Term OE/Active LOW



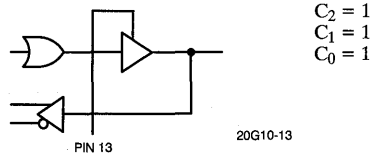
$C_2 = 0$
$C_1 = 1$
$C_0 = 1$

Figure 6. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 1$
$C_0 = 0$

Figure 7. Pin 13 OE/Active LOW



$C_2 = 1$
$C_1 = 1$
$C_0 = 1$

Figure 8. Pin 13 OE/Active HIGH

Note:
2. Bidirectional I/O configurations are possible only when the combinatorial output option is selected

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

DC Programming Voltage
PLDC20G10B and CG7C323B−A 13.0V
PLDC20G10 and CG7C323−A 14.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >500V (per MIL−STD−883, Method 8015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[3]	− 55°C to +125°C	5V ±10%
Industrial	− 40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[4]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = − 2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[5]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[5]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			− 10	+10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[6, 7]				− 90	mA
I_{CC}	Power Supply Current	$0 \le V_{IN} \le V_{CC}$ V_{CC} = Max., I_{OUT} = 0 mA Unprogrammed Device	Com'l/Ind−15, −20			70	mA
			Com'l/Ind−25, −35			55	mA
			Military−20, −25			100	mA
			Military−30, −40			80	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 100	100	µA

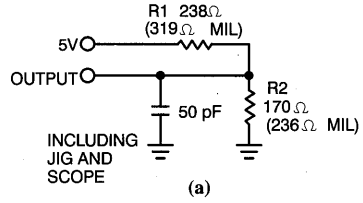
Capacitance[7]

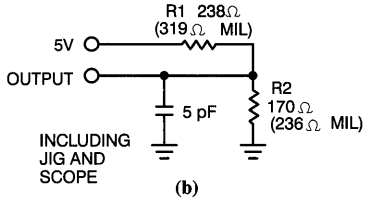
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V	10	pF

Notes:

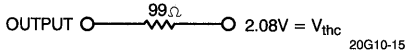
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms (Commercial)

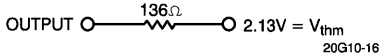




Equivalent to: THEVENIN EQUIVALENT (Commercial)



Equivalent to: THEVENIN EQUIVALENT (Military/Industrial)



Switching Characteristics Over Operating Range[3, 8, 9]

Parameter	Description	Commercial								Unit
		B–15		B–20		–25		–35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		15		20		25		35	ns
t_{EA}	Input to Output Enable		15		20		25		35	ns
t_{ER}	Input to Output Disable		15		20		25		35	ns
t_{PZX}	Pin 11 to Output Enable		12		15		20		25	ns
t_{PXZ}	Pin 11 to Output Disable		12		15		20		25	ns
t_{CO}	Clock to Output		10		12		15		25	ns
t_S	Input or Feedback Set-Up Time	12		12		15		30		ns
t_H	Hold Time	0		0		0		0		ns
t_P[10]	Clock Period	22		24		30		55		ns
t_{WH}	Clock High Time	8		10		12		17		ns
t_{WL}	Clock Low Time	8		10		12		17		ns
f_{MAX}[11]	Maximum Frequency	45.4		41.6		33.3		18.1		MHz

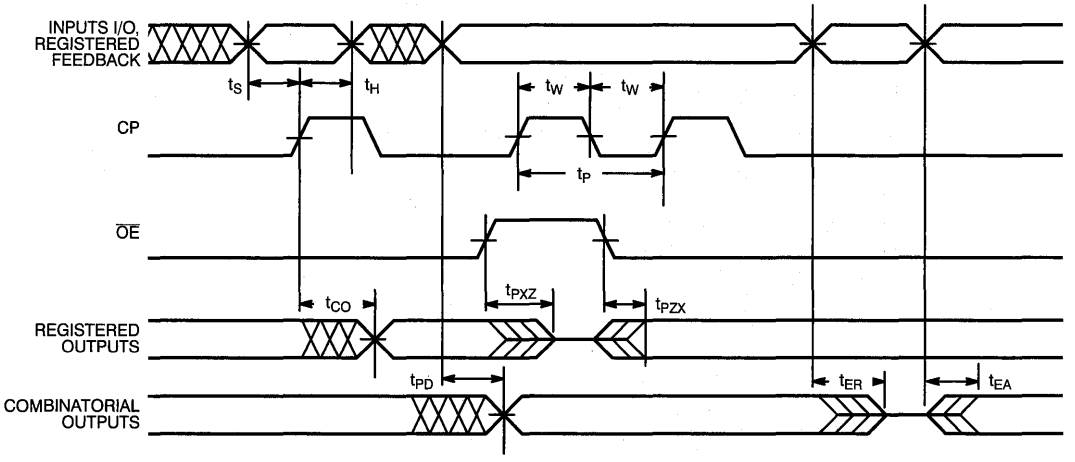
Notes:

8. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{ER}, t_{PZX}, and t_{PXZ}.
9. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW input.
10. t_P minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from $t_P = t_S + t_{CO}$. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of $(t_{WH} + t_{WL})$ or $(t_S + t_H)$.
11. f_{MAX}, minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from $f_{MAX} = 1/(t_S + t_{CO})$. The minimum guaranteed f_{MAX} for registered data path operation (no feedback) can be calculated as the lower of $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$.

Switching Characteristics Over Operating Range (continued)

Parameter	Description	Military/Industrial								Unit
		B–20		B–25		–30		–40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		20		25		30		40	ns
t_{EA}	Input to Output Enable		20		25		30		40	ns
t_{ER}	Input to Output Disable		20		25		30		40	ns
t_{PZX}	Pin 11 to Output Enable		17		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable		17		20		25		25	ns
t_{CO}	Clock to Output		15		15		20		25	ns
t_S	Input or Feedback Set-Up Time	15		18		20		35		ns
t_H	Hold Time	0		0		0		0		ns
t_P[10]	Clock Period	30		33		40		60		ns
t_{WH}	Clock High Time	12		14		16		22		ns
t_{WL}	Clock Low Time	12		14		16		22		ns
f_{MAX}[11]	Maximum Frequency	33.3		30.3		25.0		16.6		MHz

Switching Waveform



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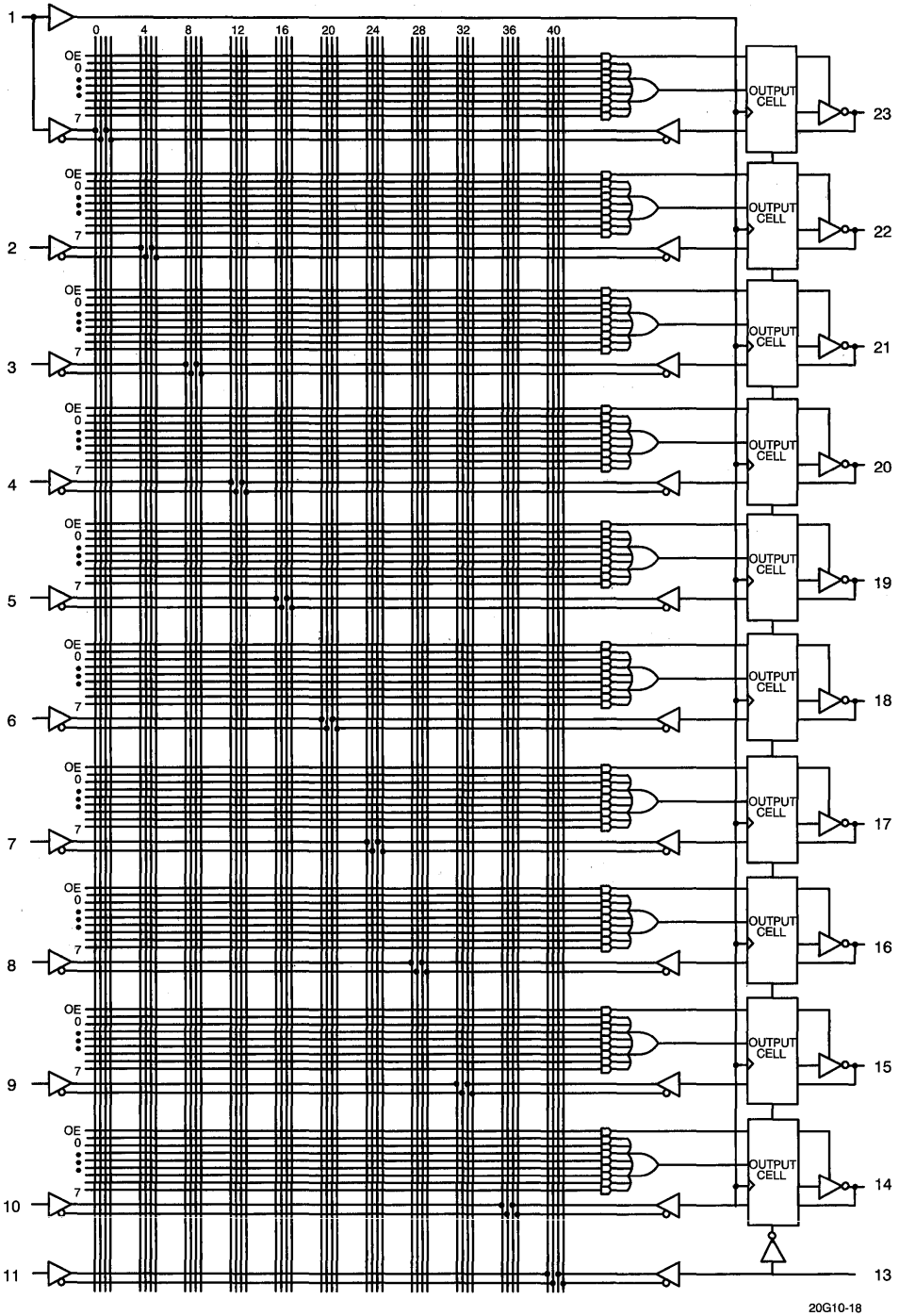
Functional Logic Diagram



20G10-18

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	12	10	70	PLDC20G10B–15PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PLDC20G10B–15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20G10B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				CG7C323B–A15JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
20	12	12	70	PLDC20G10B–20PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PLDC20G10B–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20G10B–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				CG7C323B–A20JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
20	15	15	100	PLDC20G10B–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B–20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20G10B–20LMB	L64	28-Square Leadless Chip Carrier	
25	15	15	55	PLDC20G10–25PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PLDC20G10–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20G10–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				CG7C323–A25JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
25	18	15	100	PLDC20G10B–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B–25LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10B–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	20	20	80	PLDC20G10–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10–30LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	30	25	55	PLDC20G10–35PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PLDC20G10–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20G10–35JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				CG7C323–A35JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
40	35	25	80	PLDC20G10–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10–40LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10–40WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

12. The CG7C323 is the PLD20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principle difference is in the location of the "no connect" (NC) pins.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–00019–G

PLD20G10C

Generic 24-Pin PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 7.5 ns**
  - **— t_{SU} = 3 ns**
  - **— f_{MAX} = 105 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Up to 22 inputs and 10 outputs for more logic power**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— Pin or product term output enable control**
- **Preload capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

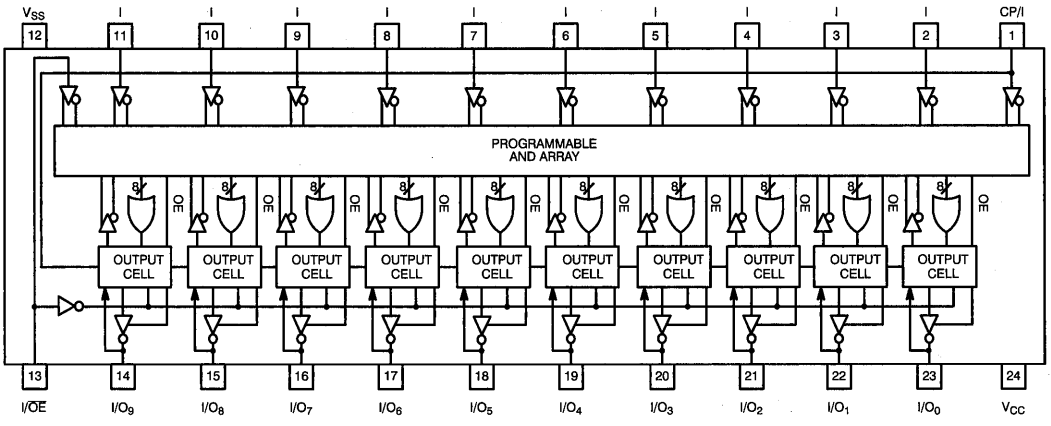
The PLD20G10C is a generic 24-pin device that can be used in place of 24 PAL devices. Thus, the PLD20G10C provides significant design, inventory, and programming flexibility over dedicated 24-pin devices.

Using BiCMOS process and Ti-W fuses, the PLD20G10C implements the familiar sum-of-products (AND-OR) logic structure. It provides 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O or a common pin controlled $\overline{OE}$ function allows this selection.

The PLD20G10C automatically resets on power-up. The Q output of all internal registers is set to a logic LOW and the $\overline{Q}$ output to a logic HIGH. In addition, the PRELOAD capability allows the registers to be set to any desired state during testing.

A security fuse is provided to prevent copying of the device fuse pattern.

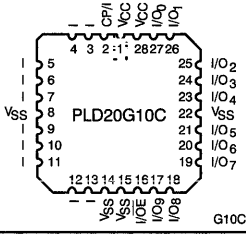
Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



G10C–1

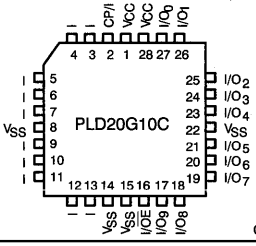
Pin Configurations

LCC (L) Top View



G10C–2

PLCC (J) Top View



G10C–3

PAL is a registered trademark of Monolithic Memories Inc.

Selection Guide

		20G10C–7	20G10C–10	20G10C–12	20G10C–15
I_{CC} (mA)	Commercial	190	190	190	
	Military		190	190	190
t_{PD} (ns)	Commercial	7.5	10	12	
	Military		10	12	15
t_S (ns)	Commercial	3.0	3.6	4.5	
	Military		3.6	4.5	7.5
t_{CO} (ns)	Commercial	6.5	7.5	9.5	
	Military		7.5	9.5	10
f_{MAX} (MHz)	Commercial	105	90	71	
	Military		90	71	57

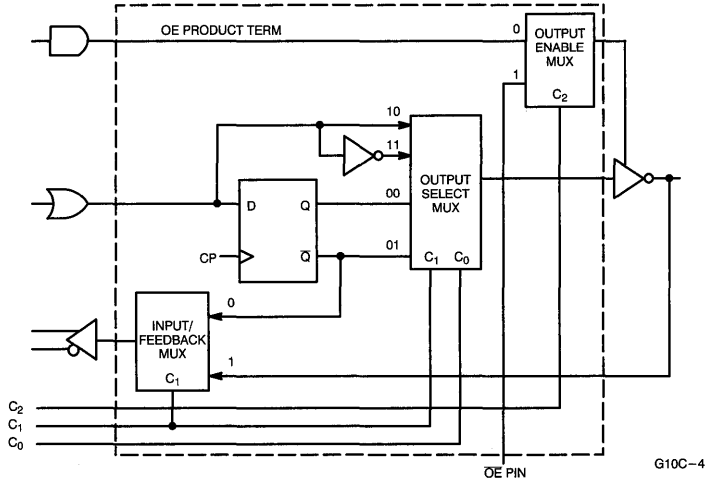
Programmable Macrocell

The PLD20G10C has 10 programmable I/O macrocells (see Macrocell). Two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output. An additional fuse (C_2) determines the source of the output enable signal. The signal can be generated either from the individual OE product term or from a common external $\overline{OE}$ pin.

Programming

The PLD20G10C can be programmed using the QuickPro II™ programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG, and other programmers. Please contact your local Cypress representative for further information.

Macrocell

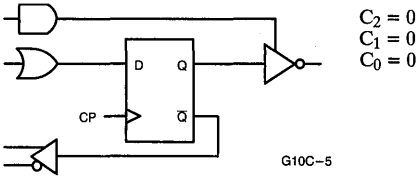


QuickPro II is a trademark of Cypress Semiconductor Corporation.

Configuration Table

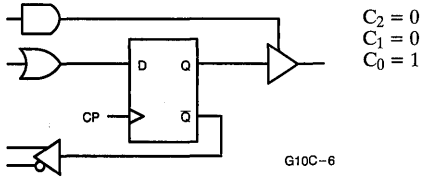
Figure	C_2	C_1	C_0	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin $\overline{OE}$/Registered/Active LOW
4	1	0	1	Pin $\overline{OE}$/Registered/Active HIGH
7	1	1	0	Pin $\overline{OE}$/Combinatorial/Active LOW
8	1	1	1	Pin $\overline{OE}$/Combinatorial/Active HIGH

Registered Output Configurations



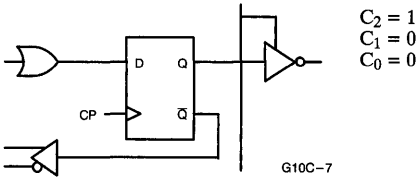
$C_2 = 0$
$C_1 = 0$
$C_0 = 0$

Figure 1. Product Term OE/Active LOW



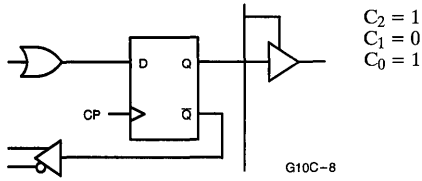
$C_2 = 0$
$C_1 = 0$
$C_0 = 1$

Figure 2. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 0$
$C_0 = 0$

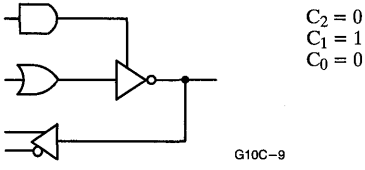
Figure 3. Pin $\overline{OE}$/Active LOW



$C_2 = 1$
$C_1 = 0$
$C_0 = 1$

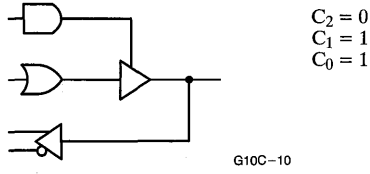
Figure 4. Pin $\overline{OE}$/Active HIGH

Combinatorial Output Configurations[1]



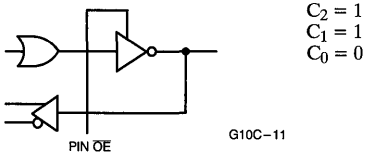
$C_2 = 0$
$C_1 = 1$
$C_0 = 0$

Figure 5. Product Term OE/Active LOW



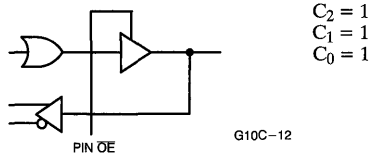
$C_2 = 0$
$C_1 = 1$
$C_0 = 1$

Figure 6. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 1$
$C_0 = 0$

Figure 7. Pin $\overline{OE}$/Active LOW



$C_2 = 1$
$C_1 = 1$
$C_0 = 1$

Figure 8. Pin $\overline{OE}$/Active HIGH

Note:
1. Bidirectional I/O configurations are possible only when the combinatorial output option is selected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC}

DC Input Voltage ..... − 0.5V to V_{CC}

DC Input Current ..... − 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	− 55°C to +125°C	4.75V to 5.5V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Com'l	2.4		V
			I_{OH} = − 2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			− 250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			− 30	− 120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

Notes:

2. T_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics PLD20G10C[5]

Parameter	Description	20G10C–7		20G10C–10		20G10C–12		20G10C–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[6]	2	7.5	2	10	2	12	2	15	ns
t_{EA}	Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t_{ER}	Input to Output Disable Delay[7]	2	7.5	2	10	2	12	2	15	ns
t_{PZX}	$\overline{OE}$ Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t_{PXZ}	$\overline{OE}$ Input to Output Disable Delay	2	7.5	2	10	2	12	2	15	ns
t_{CO}	Clock to Output Delay[6]	1	6.5	1	7.5	1	9.5	1	10	ns
t_S	Input or Feedback Set-Up Time	3		3.6		4.5		7.5		ns
t_H	Input Hold Time	0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	9		11.1		14		17.5		ns
t_{WH}	Clock Width HIGH[8]	3		3		3		6		ns
t_{WL}	Clock Width LOW[8]	3		3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]	105		90		71		57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[8, 10]	166		166		166		83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11]	133		100		83		66		MHz
t_{CF}	Register Clock to Feedback Input[12]		4.5		6.4		7.5		7.5	ns
t_{PR}	Power-Up Reset Time[13]	1		1		1		1		µs

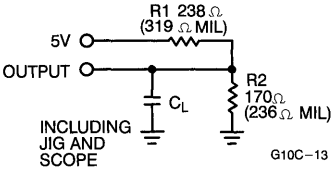
Capacitance[8]

Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

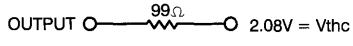
5. AC test load used for all parameters except where noted.
6. This specification is guaranteed for all device outputs changing state in a given access cycle.
7. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
8. Tested initially and after any design or process changes that may affect these parameters.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
13. The registers in the PLD20G10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

AC Test Loads and Waveforms



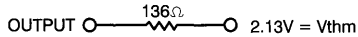
C_L[14]	Package
15 pF	P/D
50 pF	J/K/L

Equivalent to: THEVENIN EQUIVALENT

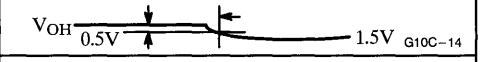
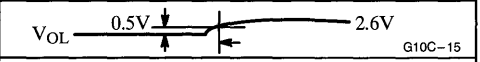
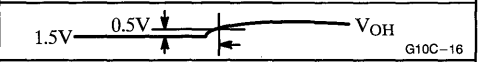
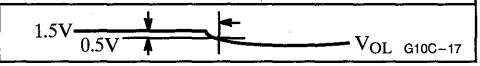


Commercial

Equivalent to: THEVENIN EQUIVALENT

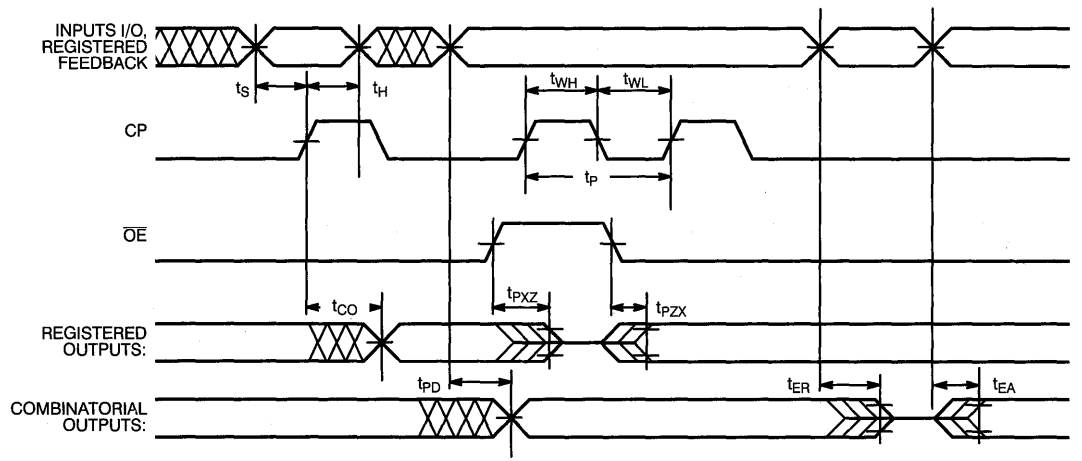


Military

Parameter	V_{th}	Output Waveform—Measurement Level
t_{ER} (–), t_{PHZ}	1.5V	
t_{ER} (+), t_{PLZ}	2.6V	
t_{EA} (+), t_{PZH}	1.5V	
t_{EA} (–), t_{PZL}	1.5V	

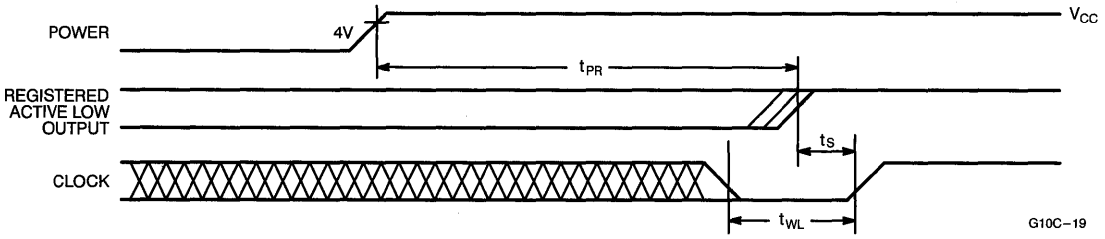
Note:
14. C_L = 5 pF for t_{ER} and t_{PXZ} measurements for all packages.

Switching Waveform

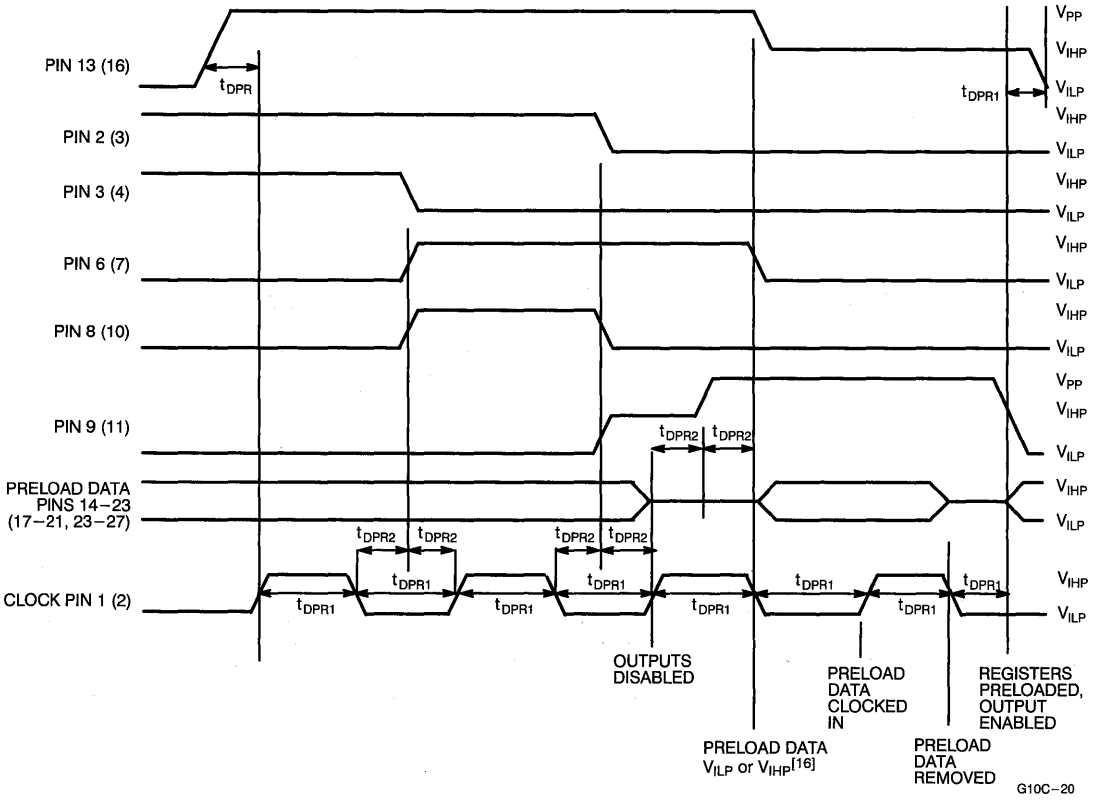


G10C–18

Power-Up Reset Waveform[13]



Preload Waveform[15]



Notes:

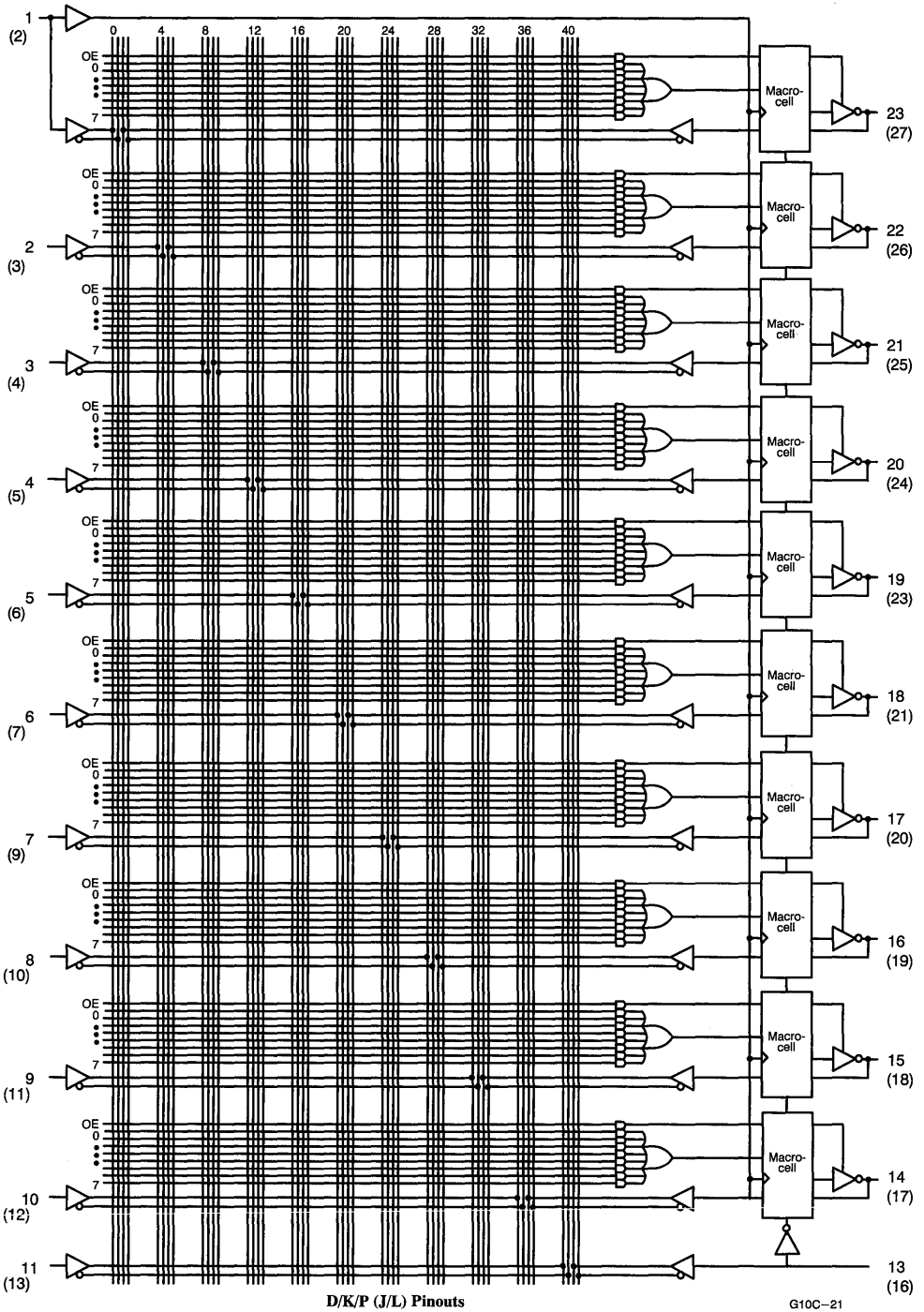
15. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
16. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/K/P (J/L) Pinouts

Forced level on register pin during preload	Register Q output state after preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PLD20G10C



D/K/P (J/L) Pinouts

G10C–21

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	7.5	105	PLD20G10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
	10	90	PLD20G10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PLD20G10C–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–10KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–10LMB	L64	28-Square Leadless Chip Carrier	
	12	71	PLD20G10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PLD20G10C–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–12KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–12LMB	L64	28-Square Leadless Chip Carrier	
	15	57	PLD20G10C–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–15KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–15LMB	L64	28-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00027–A

CYPRESS SEMICONDUCTOR

PLDC20RA10

Reprogrammable Asynchronous CMOS Logic Device

Features

- **Advanced-user programmable macrocell**
- **CMOS EPROM technology for reprogrammability**
- **Up to 20 input terms**
- **10 programmable I/O macrocells**
- **Output macrocell programmable as combinatorial or asynchronous D-type registered output**
- **Product-term control of register clock, reset and set and output enable**
- **Register preload and power-up reset**
- **Four data product terms per output macrocell**
- **Fast**
  - **Commercial**
    t_{PD} = 15 ns
    t_{CO} = 15 ns
    t_{SU} = 7 ns
  - **Military/Industrial**
    t_{PD} = 20 ns
    t_{CO} = 20 ns
    t_{SU} = 10 ns
- **Low power**
  - **I_{CC} max – 80 mA (Commercial)**
  - **I_{CC} max = 85 mA (Military)**
- **High reliability**
  - **Proven EPROM technology**
  - **>2001V input protection**
  - **100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

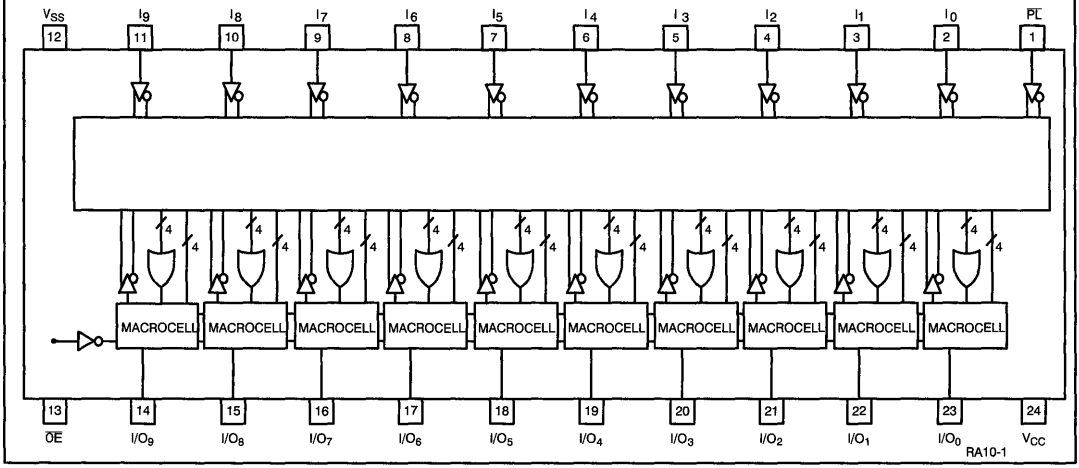
Functional Description

The Cypress PLDC20RA10 is a high-performance, second-generation programmable logic device employing a flexible macrocell structure that allows any individual output to be configured independently as a combinatorial output or as a fully asynchronous D-type registered output.

The Cypress PLDC20RA10 provides lower-power operation with superior speed performance than functionally equivalent bipolar devices through the use of high-performance 0.8-micron CMOS manufacturing technology.

The PLDC20RA10 is packaged in a 24 pin 300-mil molded DIP, a 300-mil windowed cerDIP, and a 28-lead square leadless chip carrier, providing up to 20 inputs and 10 outputs. When the windowed device is exposed to UV light, the 20RA10 is erased and can then be reprogrammed.

Logic Block Diagram

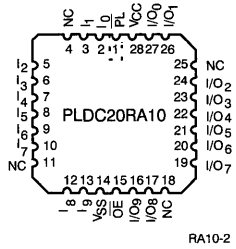


Selection Guide

Generic Part Number	t_{PD} ns		t_{SU} ns		t_{CO} ns		I_{CC} ns	
	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind
20RA10-15	15		7		15		80	
20RA10-20	20	20	10	10	20	20	80	85
20RA10-25		25		15		25		85
20RA10-35		35		20		35		85

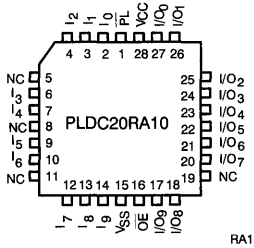
Pin Configurations

LCC
Top View



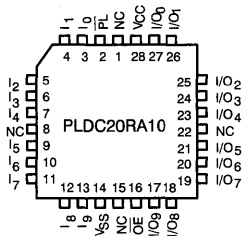
RA10-2

STD PLCC/HLCC
Top View



RA10-3

JEDEC PLCC/HLCC [1]
Top View



RA10-4

Macrocell Architecture

Figure 1 illustrates the architecture of the 20RA10 macrocell. The cell dedicates three product terms for fully asynchronous control of the register set, reset, and clock functions, as well as, one term for control of the output enable function.

The output enable product term output is ANDed with the input from pin 13 to allow either product term or hardwired external control of the output or a combination of control from both sources. If product-term-only control is selected, it is automatically chosen for all outputs since, for this case, the external output enable pin must be tied LOW. The active polarity of each output may be programmed independently for each output cell and is subsequently fixed. *Figure 2* illustrates the output enable options available.

When an I/O cell is configured as an output, combinatorial-only capability may be selected by forcing the set and reset product term outputs to be HIGH under all input conditions. This is achieved by programming all input term programming cells for these two product terms. *Figure 3* illustrates the available output configuration options.

An additional four uncommitted product terms are provided in each output macrocell as resources for creation of user-defined logic functions.

Programmable I/O

Because any of the ten I/O pins may be selected as an input, the device input configuration programmed by the user may vary from a total of nine programmable plus ten dedicated inputs (a total of nineteen inputs) and one output down to a ten-input, ten-output configuration with all ten programmable I/O cells configured as outputs. Each input pin available in a given configuration is available as an input to the four control product terms and four uncommitted product terms of each programmable I/O macrocell that has been configured as an output.

An I/O cell is programmed as an input by tying the output enable pin (pin 13) HIGH or by programming the output enable product term to provide a LOW, thereby disabling the output buffer, for all possible input combinations.

When utilizing the I/O macrocell as an output, the input path functions as a feedback path allowing the output signal to be fed back as an input to the product term array. When the output cell is configured as a registered output, this feedback path may be used to feed back the current output state to the device inputs to provide current state control of the next output state as required for state machine implementation.

Preload and Power-Up Reset

Functional testability of programmed devices is enhanced by inclusion of register preload capability, which allows the state of each register to be set by loading each register from an external source prior to exercising the device. Testing of complex state machine designs is simplified by the ability to load an arbitrary state without cycling through long test vector sequences to reach the desired state. Recovery from illegal states can be verified by loading illegal states and observing recovery. Preload of a particular register is accomplished by impressing the desired state on the register output pin and lowering the signal level on the preload control pin (pin1) to a logic LOW level. If the specified preload set-up, hold and pulse width minimums have been observed, the desired state is loaded into the register. To insure predictable system initialization, all registers are preset to a logic LOW state upon power-up, thereby setting the active LOW outputs to a logic HIGH.

Note:

1. The CG7C324 is the PLDC20RA10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin fuction and pin order is identical for both PLCC pinouts. The principle differencd is in the location of the "no connect" (NC) pins.

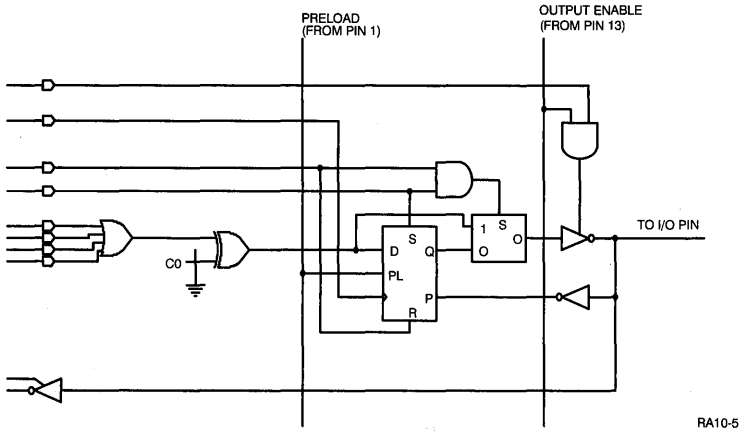


Figure 1. PLDC20RA10 Macrocell

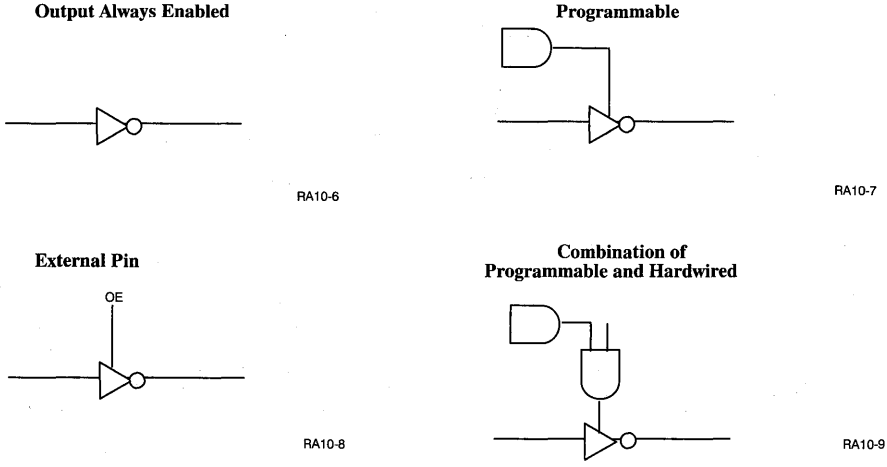
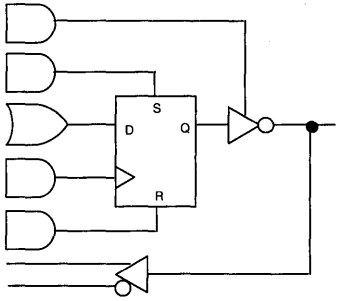


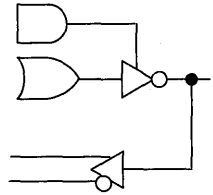
Figure 2. Four Possible Output Enable Alternatives for the PLDC20RA10

Registered/Active LOW



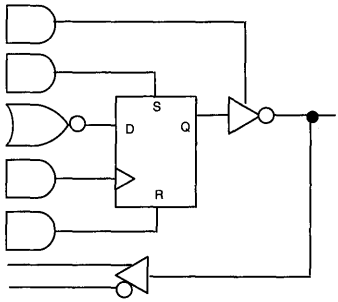
RA10-10

Combinatorial/Active LOW



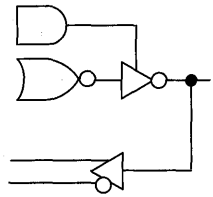
RA10-11

Registered/Active HIGH



RA10-12

Combinatorial/Active HIGH



RA10-13

Figure 3. Four Possible Macrocell Configurations for the PLDC20RA10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... −3.0 V to + 7.0 V

Output Current into Outputs (LOW) ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Program Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 8 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max			−10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−40	+40	µA
I_{SC}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = 0.5V[6]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC}= Max., V_{IN} = GND Outputs Open		Com'l		75	mA
				Mil/Ind		80	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (In High Z State) Device Operating af f_{MAX}		Com'l		80	mA
				Mil/Ind		85	mA

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz	10	pF

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

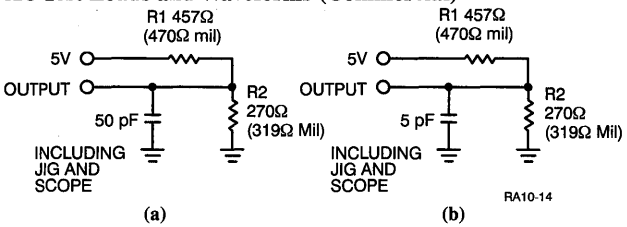
Switching Characteristics Over the Operating Range[3, 7, 8]

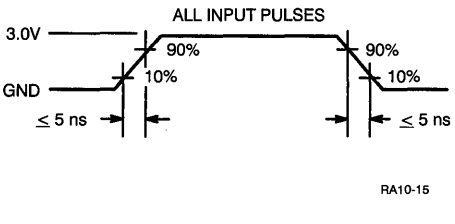
Parameter	Description	Commercial				Military/Industrial						Unit
		−15		−20		−20		−25		−35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		15		20		20		25		35	ns
t_{EA}	Input to Output Enable		15		20		20		30		35	ns
t_{ER}	Input to Output Disable		15		20		20		30		35	ns
t_{PZX}	Pin 13 to Output Enable		12		15		15		20		25	ns
t_{PXZ}	Pin 13 to Output Disable		12		15		15		20		25	ns
t_{CO}	Clock to Output		15		20		20		25		35	ns
t_{SU}	Input or Feedback Set-Up Time	7		10		10		15		20		ns
t_H	Hold Time	3		5		3		5		5		ns
t_P	Clock Period ($t_{SU} + t_{CO}$)	22		30		30		40		55		ns
t_{WH}	Clock Width HIGH[5]	10		13		12		18		25		ns
t_{WL}	Clock Width LOW[5]	10		13		12		18		25		ns
f_{MAX}	Maximum Frequency ($1/t_P$)[5]	45.5		33.3		33.3		25.0		18.1		MHz
t_S	Input of Asynchronous Set to Registered Output		15		20		20		25		40	ns
t_R	Input of Asynchronous Reset to Registered Output		15		20		20		25		40	ns
t_{ARW}	Asynchronous Reset Width[5]	15		20		20		25		25		ns
t_{ASW}	Asynchronous Set Width[5]	15		20		20		25		25		ns
t_{AR}	Asynchronous Set/ Reset Recovery Time	10		12		12		15		20		ns
t_{WP}	Preload Pulse Width	15		15		15		15		15		ns
t_{SUP}	Preload Set-Up Time	15		15		15		15		15		ns
t_{HP}	Preload Hold Time	15		15		15		15		15		ns

Notes:

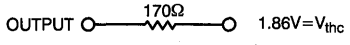
7. Part (a) of AC Test Loads was used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}, which use part (b).
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5$ V for an enabled HIGH output or $V_{OL} + 0.5$V for an enabled LOW output. Please see part (c) of AC Test Loads and Waveforms for waveforms and measurement reference levels.

AC Test Loads and Waveforms (Commercial)



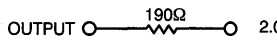


Equivalent to: THÉVENIN EQUIVALENT (Commercial)

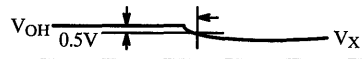
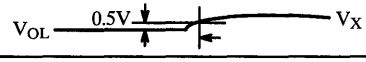
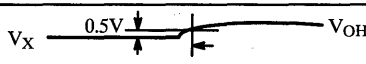
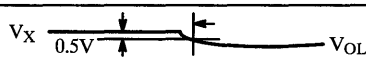
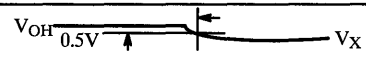
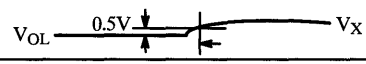
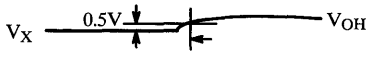
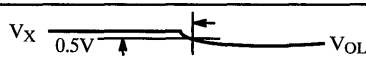


RA10-16

Equivalent to: THÉVENIN EQUIVALENT (Military/Industrial)

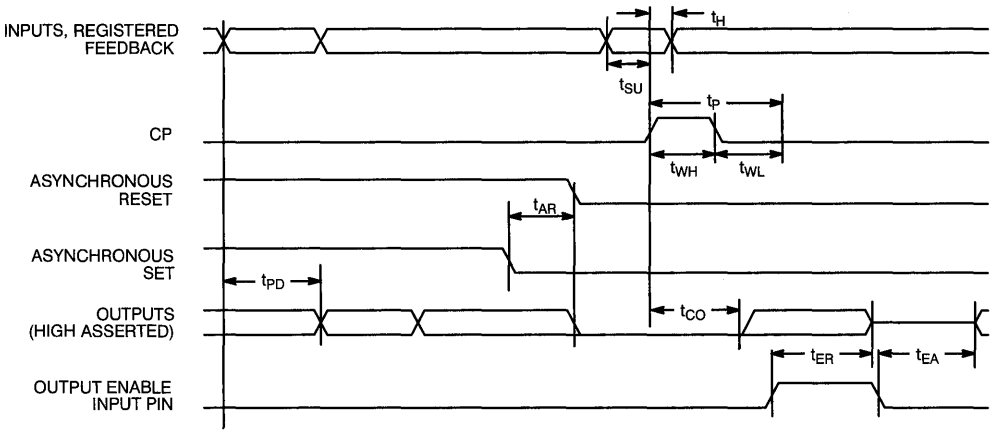


RA10-17

Parameter	V_{th}	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	 RA10-18
$t_{PXZ}(+)$	2.6V	 RA10-19
$t_{PZX}(+)$	V_{thc}	 RA10-20
$t_{PZX}(-)$	V_{thc}	 RA10-21
$t_{ER}(-)$	1.5V	 RA10-22
$t_{ER}(+)$	2.6V	 RA10-23
$t_{EA}(+)$	V_{thc}	 RA10-24
$t_{EA}(-)$	V_{thc}	 RA10-25

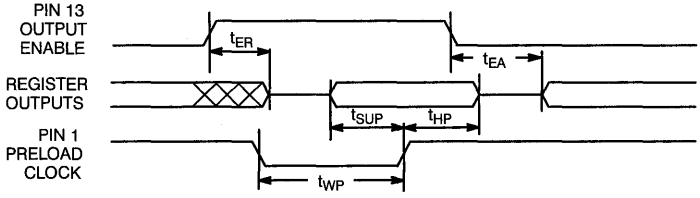
(c)

Switching Waveform



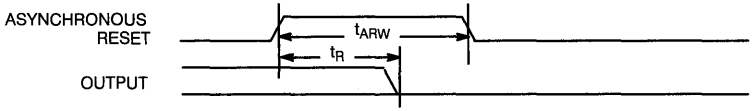
RA10-26

Preload Switching Waveform



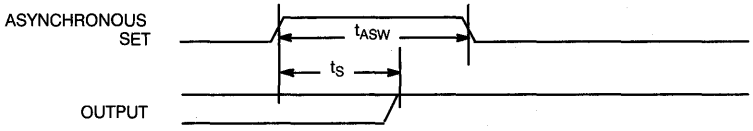
RA10-27

Asynchronous Reset



RA10-28

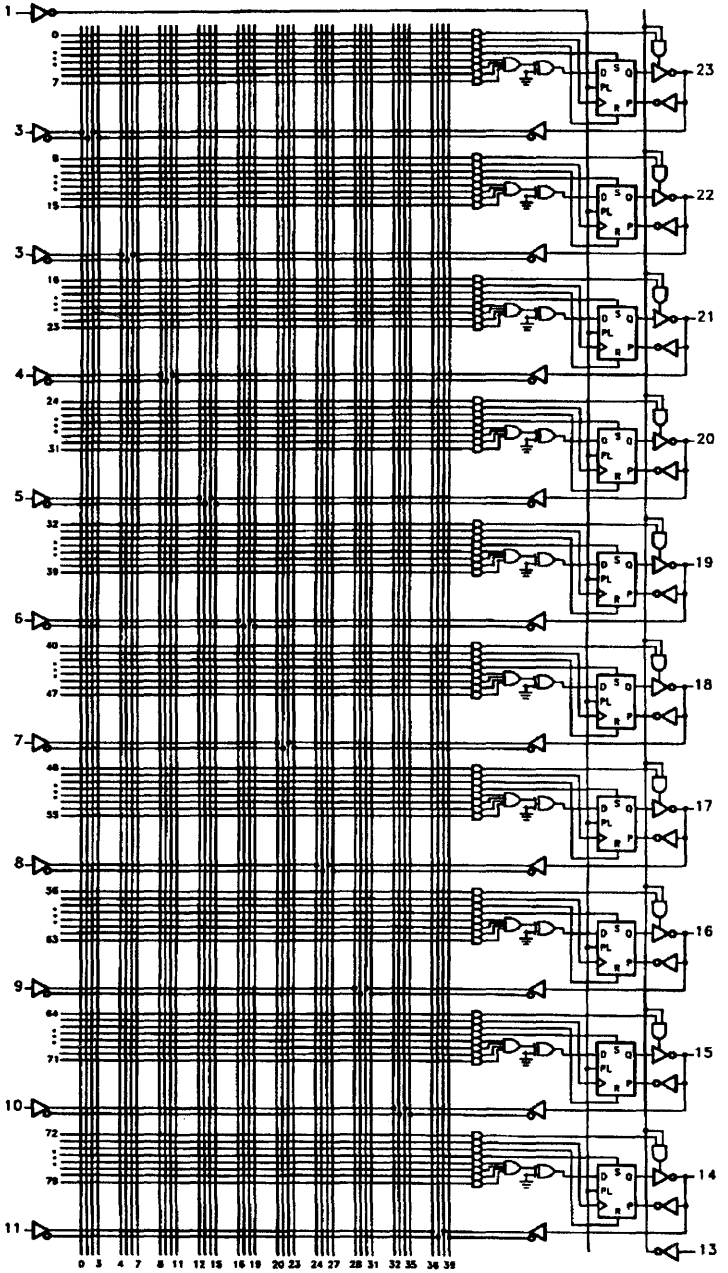
Asynchronous Set



RA10-29

4 PLDs

Functional Logic Diagram



Ordering Information

I_{CC2}	t_{PD} (ns)	t_{SU} (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
80	15	7	15	PLDC20RA10–15HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PLDC20RA10–15JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10–15PC	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10–15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C324–A15HC	H64	28-Pin Windowed Leaded Chip Carrier	
				CG7C324–A15JC	J64	28-Lead Plastic Leaded Chip Carrier	
80	20	10	20	PLDC20RA10–20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PLDC20RA10–20JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10–20PC	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C324–A20HC	H64	28-Pin Windowed Leaded Chip Carrier	
				CG7C324–A20JC	J64	28-Lead Plastic Leaded Chip Carrier	
85	20	10	20	PLDC20RA10–20DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10–20JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10–20PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10–20WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10–20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10–20LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10–2QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10–20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
85	25	15	25	PLDC20RA10–25DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10–25JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10–25PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10–25WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10–25HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10–25LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
85	35	20	35	PLDC20RA10–35DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10–3JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10–35PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10–35WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10–35HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10–35LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_{SU}	9, 10, 11
t_{H}	9, 10, 11

Document #: 38–00073–E

CYPRESS SEMICONDUCTOR

Reprogrammable CMOS PAL® Device

Features

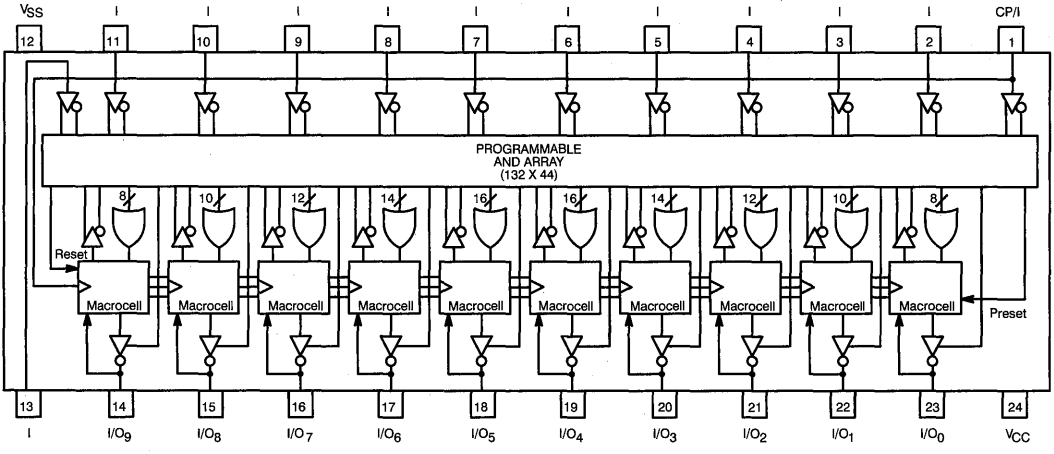
- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 55 mA max. "L"**
  - **— 90 mA max. standard**
  - **— 120 mA max. military**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **20, 25, 35 ns commercial and industrial**
- **25, 30, 40 ns military**
- **Up to 22 input terms and 10 outputs**
- **High reliability**
  - **— Proven EPROM technology**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, and PLCC available**

Functional Description

The Cypress PALC22V10 is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "programmable macrocell."

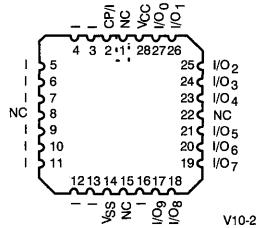
The PALC22V10 is available in 24-pin 300-mil molded DIPs, 300-mil windowed cerDIPs, 28-lead square ceramic leadless chip carriers, 28-lead square plastic leaded chip carriers, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10 is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as registered or combinatorial. Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through array-configurable output enable for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

Logic Block Diagram (PDIP/CDIP)



Pin Configuration

LCC/PLCC Top View



PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

PALC22V10 features a variable product term architecture. There are five pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10 include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization function. The device automatically resets on power-up.

For testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high-impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A 0 on the I/O pin preloads the register with a 0, and a 1 preloads the register with a 1. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed and pin 8 is returned to a normal TTL voltage. Again, care should be exercised to power sequence the device properly.

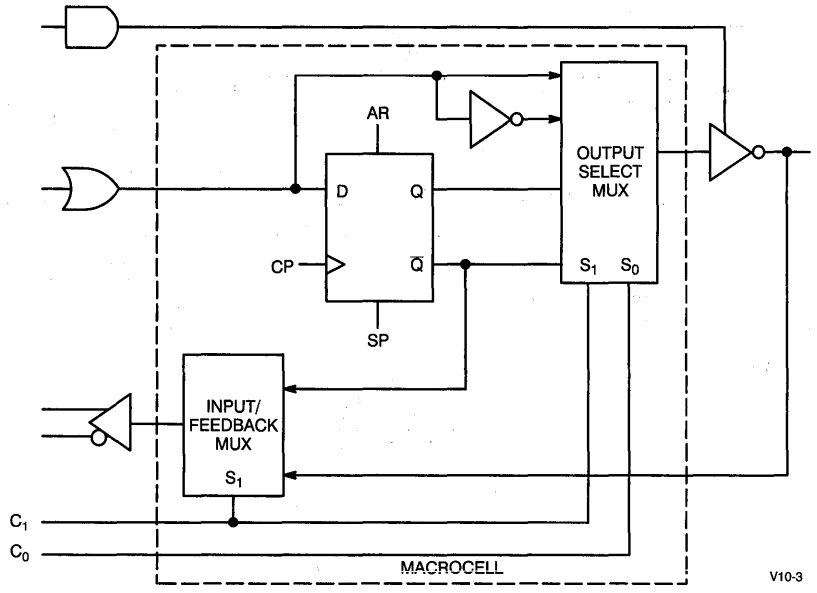
The PALC22V10 featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control state machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macrocell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of a programmable logic.

Along with this increase in functional density, the Cypress PALC22V10 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature. Preload facilitates testing programmed devices by loading initial values into the registers.

Configuration Table

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Selection Guide

Generic Part Number	I_{CC1} (mA)			t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	"L"	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10–20		90		20		12		12	
22V10–25	55	90	100	25	25	15	18	15	15
22V10–30			100		30		20		20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

UV Exposure ..... 7258 Wsec/cm^2

DC Programming Voltage 14.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >500V (per MIL–STD–883, Method 8015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Industrial	– 40°C to +85°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = – 2 mA	Mil			
V_{OH2}	HIGH Level CMOS Output Voltage[3]	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 100 µA		V_{CC}–1.0V		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			– 10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			– 40	+40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 5]			– 30	– 90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open for Unprogrammed Device		"L"		55	mA
				Com'l/Ind		90	mA
				Mil		100	mA
I_{CC2}	Operating Power Supply Current	f_{toggle} = F_{MAX}[3]		"L"		65	mA

Capacitance[3]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Commercial and Industrial Switching Characteristics PALC22V10[2, 6]

Parameter	Description	-20		-25		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		20		25	ns
t_{EA}	Input to Output Enable Delay		20		25	ns
t_{ER}	Input to Output Disable Delay[8]		20		25	ns
t_{CO}	Clock to Output Delay[9]		12		15	ns
t_S	Input or Feedback Set-Up Time	12		15		ns
t_H	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	24		30		ns
t_{WH}	Clock Width HIGH[3]	10		12		ns
t_{WL}	Clock Width LOW[3]	10		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	41.6		33.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	50.0		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	45.4		35.7		MHz
t_{CF}	Register Clock to Feedback Input[13]		10		13	ns
t_{AW}	Asynchronous Reset Width	20		25		ns
t_{AR}	Asynchronous Reset Recovery Time	20		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		25		25	ns
t_{SPR}	Synchronous Preset Recovery Time	20		25		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		μs

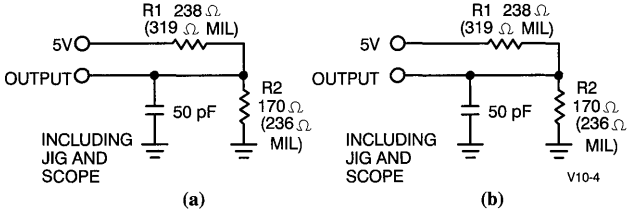
Notes:

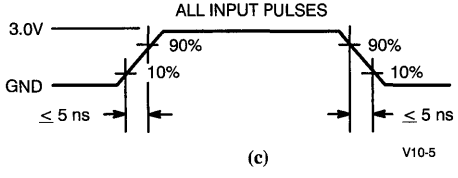
6. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}.
7. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{PD} for cases in which fewer outputs are changing state per access cycle.
8. This parameter is specified as the time after output disable input during which the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5V below V_{OH} min. or a previous LOW level has risen to 0.5V above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction that may be subtracted from t_{CO} for cases in which fewer outputs are changing state per access cycle.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 12 above) minus t_S.
14. The registers in the PALC22V10 have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

Military Switching Characteristics PALC22V10[2, 6]

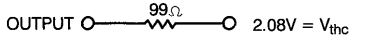
Parameter	Description	−25		−30		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		25		30	ns
t_{EA}	Input to Output Enable Delay		25		25	ns
t_{ER}	Input to Output Disable Delay[8]		25		25	ns
t_{CO}	Clock to Output Delay[9]		15		20	ns
t_S	Input or Feedback Set-Up Time	18		20		ns
t_H	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	33		40		ns
t_{WH}	Clock Width HIGH[3]	14		16		ns
t_{WL}	Clock Width LOW[3]	14		16		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	30.3		25.0		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	35.7		31.2		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	32.2		28.5		MHz
t_{CF}	Register Clock to Feedback Input[13]		13		15	ns
t_{AW}	Asynchronous Reset Width	25		30		ns
t_{AR}	Asynchronous Reset Recovery Time	25		30		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		25		30	ns
t_{SPR}	Synchronous Preset Recovery Time	25		30		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		μs

AC Test Loads and Waveforms

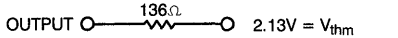




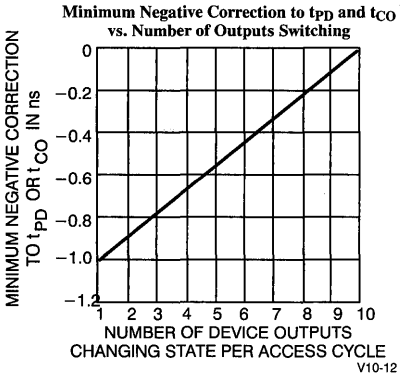
Equivalent to: THEVENIN EQUIVALENT (Commercial)



Equivalent to: THEVENIN EQUIVALENT (Military)



AC Test Loads and Waveforms (continued)

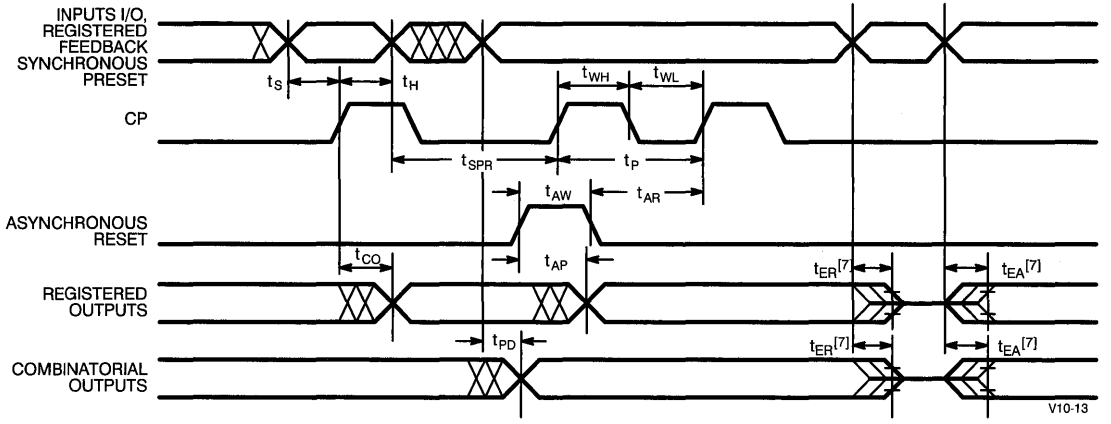


(d)

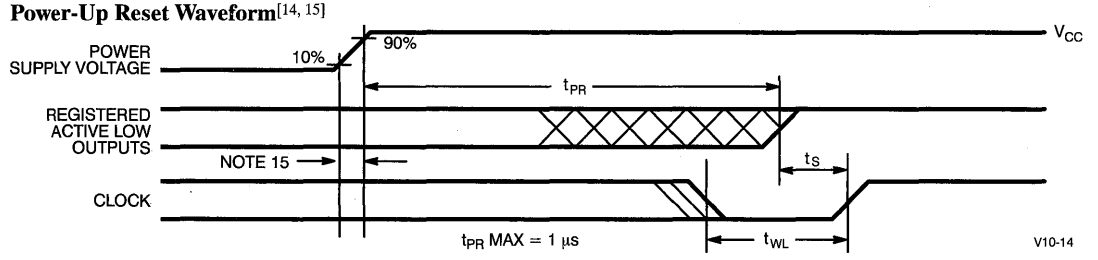
Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	V_{OH}, 0.5V, V_X — V10-8
t_{ER} (+)	2.6V	V_{OL}, 0.5V, V_X — V10-9
t_{EA} (+)	V_{thc}	V_X, 0.5V, V_{OH} — V10-10
t_{EA} (−)	V_{thc}	V_X, 0.5V, V_{OL} — V10-11

(e) Test Waveforms

Switching Waveform



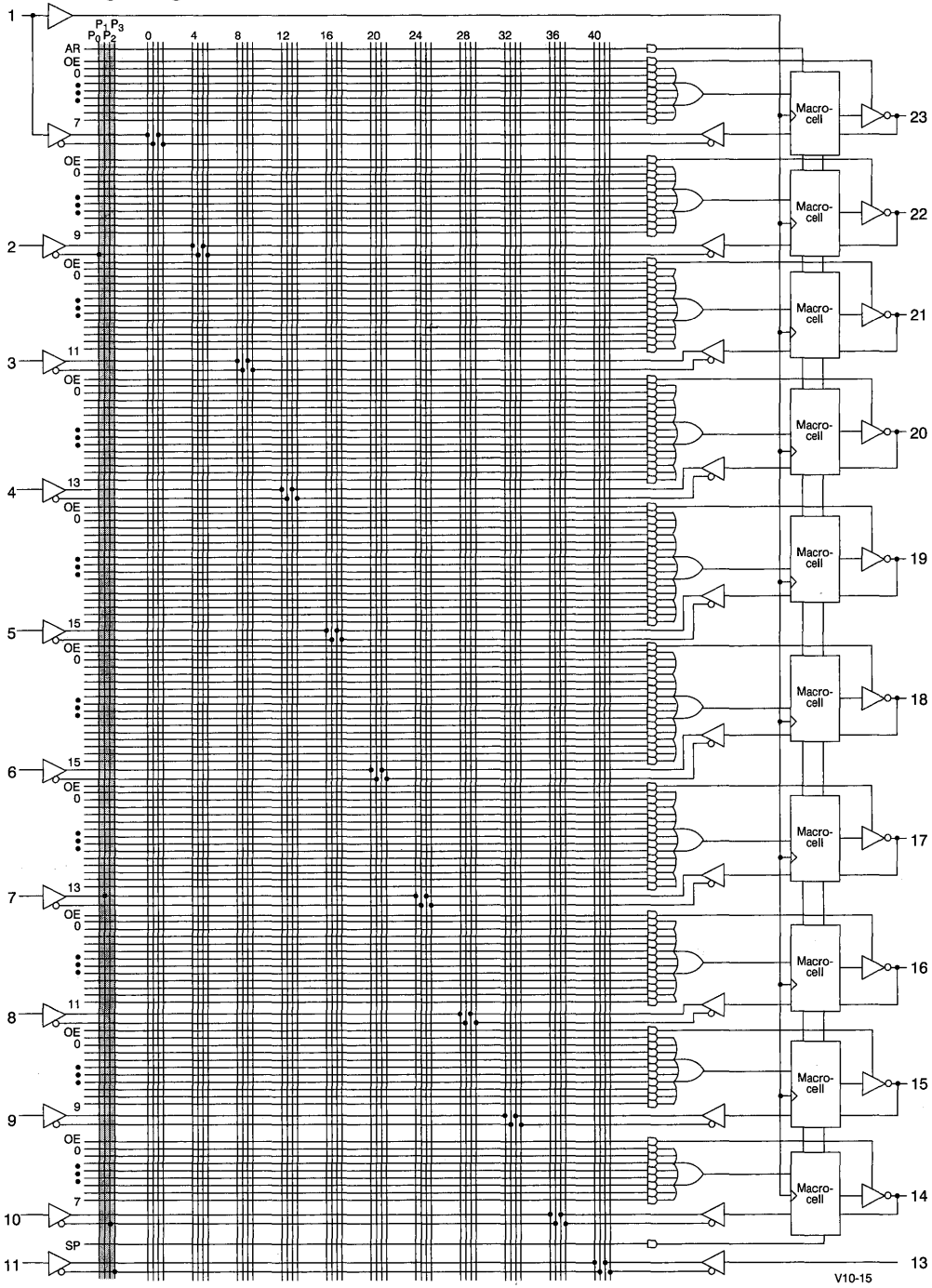
Power-Up Reset Waveform[14, 15]



Note:

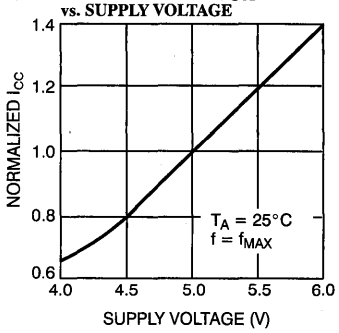
15. The clock signal input must be in a valid LOW state (V_{IN} less than 0.8V) or a valid HIGH state (V_{IN} greater than 2.4V) prior to occurrence of the 10% level on the monotonically rising power supply voltage as shown in Power-Up Reset Waveform. In addition, the clock input signal must remain stable in that valid state as indicated until the 90% level on the power supply voltage has been reached. The clock signal may transition LOW to HIGH to clock in new data or to execute a synchronous preset after the indicated delay ($t_{PR} + t_S$) has been observed.

Functional Logic Diagram for PALC22V10

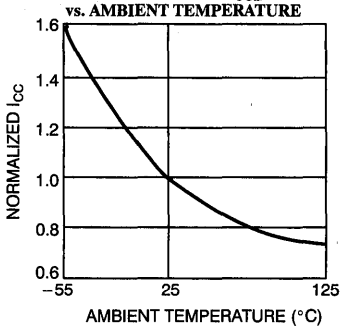


Typical DC and AC Characteristics

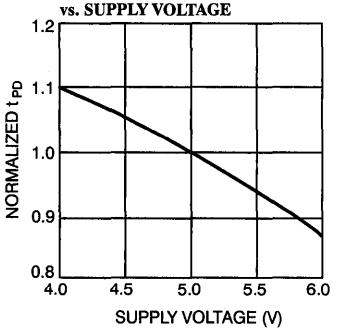
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. SUPPLY VOLTAGE



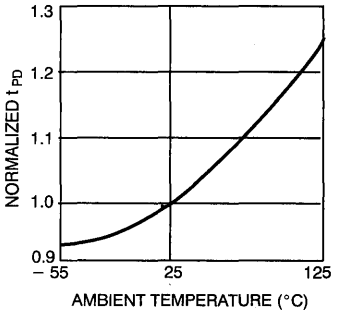
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. AMBIENT TEMPERATURE



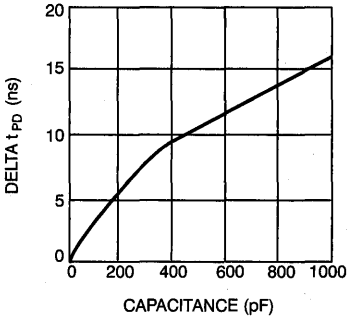
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



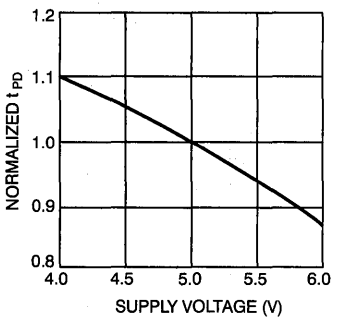
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



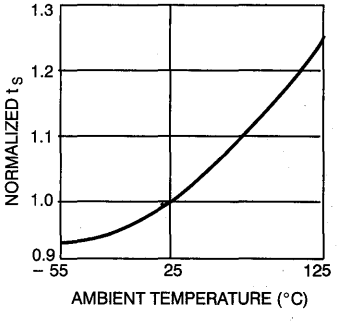
DELTA PROPAGATION TIME vs. OUTPUT LOADING



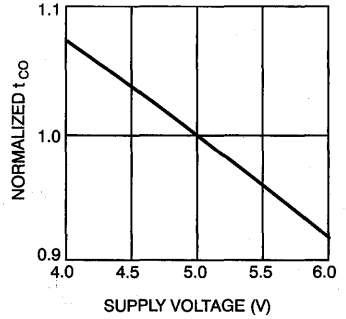
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



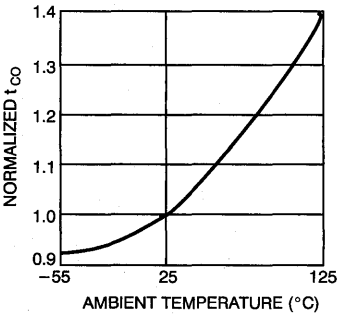
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. SUPPLY VOLTAGE

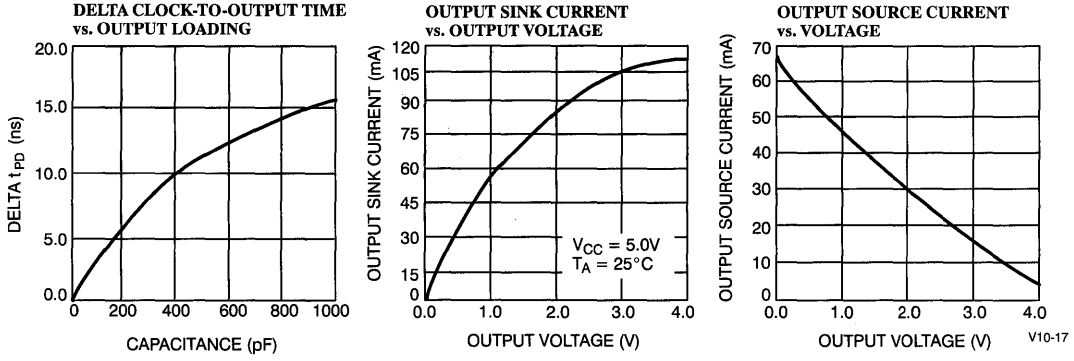


NORMALIZED CLOCK-TO-OUTPUT TIME vs. TEMPERATURE



V10-16

Typical DC and AC Characteristics (continued)



Erasure Characteristics

Wavelengths of light less than 4000Å begin to erase the PALC22V10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high-ambient light levels can create hole-electron pairs that may cause blank check failures or verify errors when programming windowed parts. This phenomenon can be avoided by placing an opaque label over the window during programming in high-ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec /cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC22V10 needs to be placed within one inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Ordering Information 22V10

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	20	12	12	PALC22V10–20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
				PALC22V10–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10–20PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10–20WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
55	25	15	15	PALC22V10L–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PALC22V10L–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10L–25PC	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10L–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
90	25	15	15	PALC22V10–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
				PALC22V10–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10–25PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10–25WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
100	25	18	15	PALC22V10–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10–25KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10–25LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10–25QMB	Q64	24-Pin Windowed Leadless Chip Carrier	
				PALC22V10–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Ordering Information 22V10 (continued)

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
100	30	20	20	PALC22V10–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10–30KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10–30LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10–30QMB	Q64	24-Pin Windowed Leadless Chip Carrier	
				PALC22V10–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–00020–G

PALC22V10B

Reprogrammable CMOS PAL® Device

Features

- **Advanced second generation PAL architecture**
- **Low power**
  - **— 90 mA max. standard**
  - **— 100 mA max. military**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
  - **— "15" commercial and industrial**
    10 ns t_{CO}
    10 ns t_S
    15 ns t_{PD}
    50 MHz
  - **— "15" and "20" military**
    10/15 ns t_{CO}
    10/17 ns t_S
    15/20 ns t_{PD}
    50/31 MHz
- **Up to 22 input terms and 10 outputs**
- **Enhanced test features**
  - **— Phantom array**
  - **— Top test**
  - **— Bottom test**
  - **— Preload**
- **High reliability**
  - **— Proven EPROM technology**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

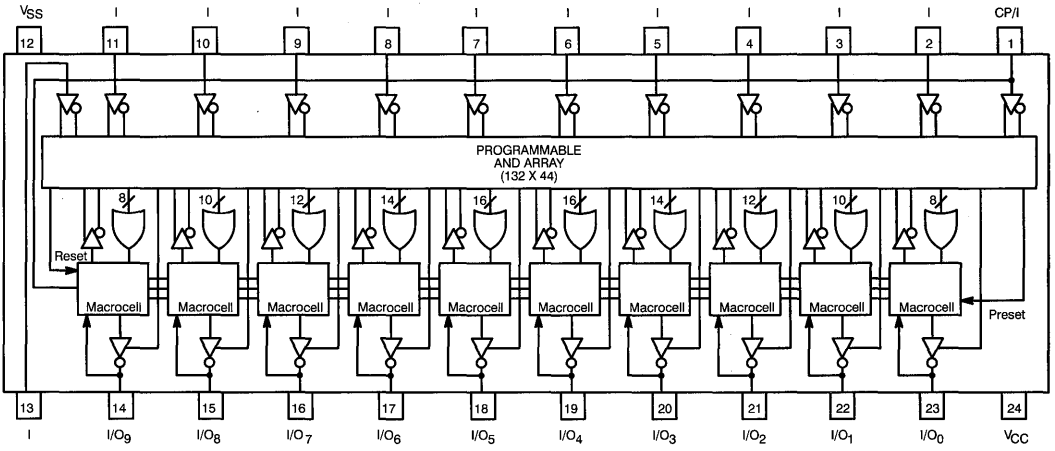
Functional Description

The Cypress PALC22V10B is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macrocell."

The PALC22V10B is executed in a 24-pin 300-mil molded DIP, a 300-mil windowed cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10B is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as "registered" or "combinatorial." Polarity of each output may also be

4 PLDs

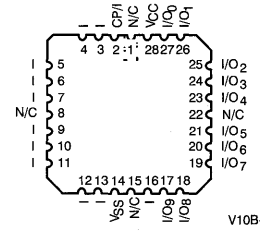
Logic Block Diagram (PDIP/CDIP)



V10B-1

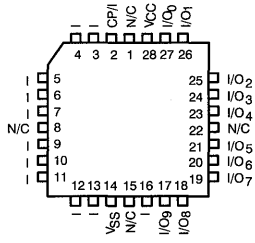
Pin Configurations

LCC
Top View



V10B-2

PLCC
Top View



V10B-3

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Functional Description (continued)

individually selected, allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10B features a "variable product term" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10B is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10B include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization function. The device automatically resets upon power-up.

For testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high-impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A 0 on the I/O pin preloads the register with a 0 and a 1 preloads the register with a 1. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Care should be exercised to power sequence the device properly.

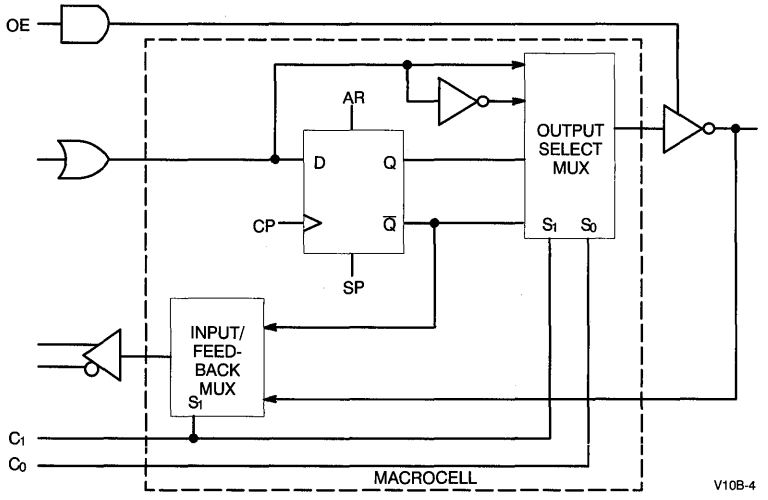
The PALC22V10B featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macrocell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of a programmable logic.

Along with this increase in functional density, the Cypress PALC22V10B provides lower-power operation through the use of CMOS technology, increased testability with a register preload feature, and guaranteed AC performance through the use of a phantom array. This phantom array ($P_0 - P_3$) and the "top test" and "bottom test" features allow the 22V10B to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PALC22V10B at incoming inspection before committing the device to a specific function through programming. Preload facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 2

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Selection Guide

Generic Part Number	I_{CC1} mA		t_{PD} ns		t_S ns		t_{CO} ns	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10B–15	90	100	15	15	10	10	10	10
22V10B–20	–	100	–	20	–	17	–	15

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (Low) ..... 16 mA

UV Exposure ..... 7258 Wsec/cm^2

DC Programming Voltage 13.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage (per MIL–STD 883 Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%
Industrial	–40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = –2 mA	Mil			
V_{OH2}	HIGH Level CMOS Output Voltage[3]	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA		V_{CC} – 1.0V		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			–10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			–40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 5]			–30	–90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open for Unprogrammed Device		Com'l/Ind		90	mA
				Mil		100	mA
I_{CC2}	Operating Power Supply Current	f_{toggle} = F_{MAX}[3]		Com'l/Ind		90	mA
		Device Programmed with Worst Case Pattern, Outputs Three-Stated		Mil		100	mA

Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[3]

Parameters	Description	Typical	Max.	Units
C_{IN}	Input Capacitance	11		pF
C_{OUT}	Output Capacitance	9		pF

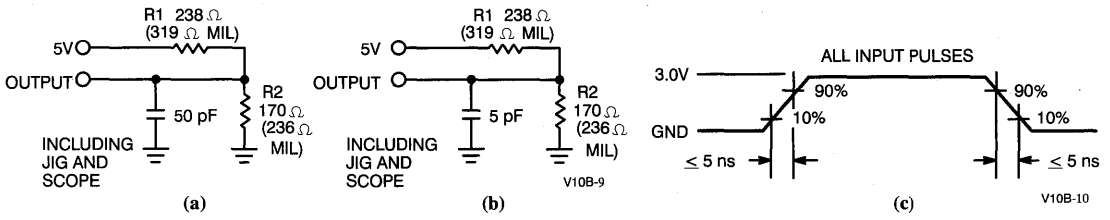
Switching Characteristics PALC22V10[2, 6]

Parameters	Description	Commercial & Industrial B–15		Military B–15		Military B–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		15		15		20	ns
t_{EA}	Input to Output Enable Delay		15		15		20	ns
t_{ER}	Input to Output Disable Delay[8]		15		15		20	ns
t_{CO}	Clock to Output Delay[9]		10		10		15	ns
t_S	Input or Feedback Set-Up Time	10		10		17		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	20		20		32		ns
t_{WH}	Clock Width HIGH[3]	6		6		12		ns
t_{WL}	Clock Width LOW[3]	6		6		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	50.0		50		31.2		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	83.3		83.3		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	80.0		80		33.3		MHz
t_{CF}	Register Clock to Feedback Input[13]		2.5		2.5		13	ns
t_{AW}	Asynchronous Reset Width	15		15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	10		12		20		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		20		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	10		20		20		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		1.0		μs

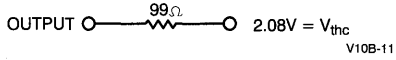
Notes:

6. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
7. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{PD} for cases in which fewer outputs are changing state per access cycle.
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{CO} for cases in which fewer outputs are changing state per access cycle.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 12 above) minus t_S.
14. The registers in the PALC22V10B has been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

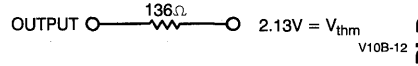
AC Test Loads and Waveforms (Commercial)

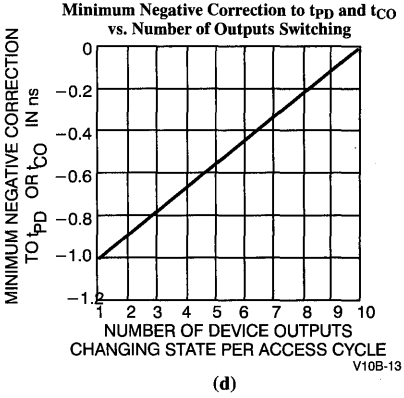


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



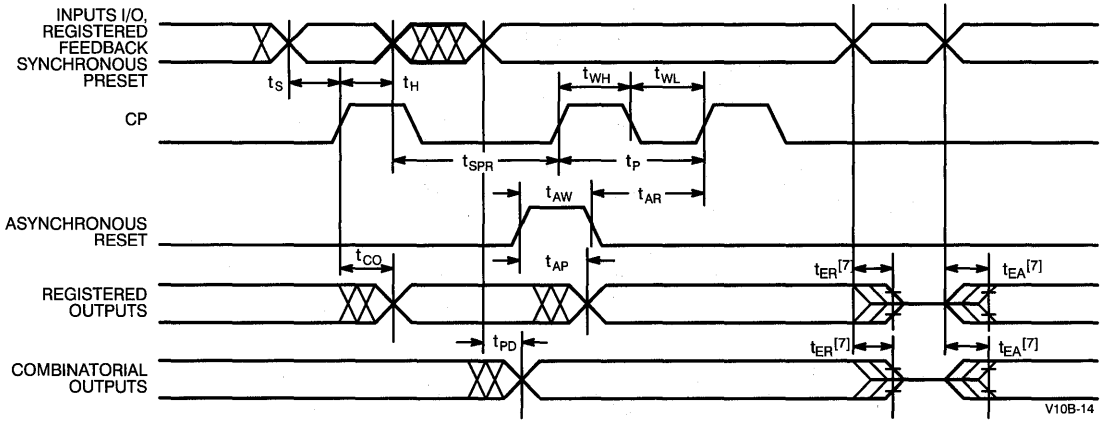


(d)

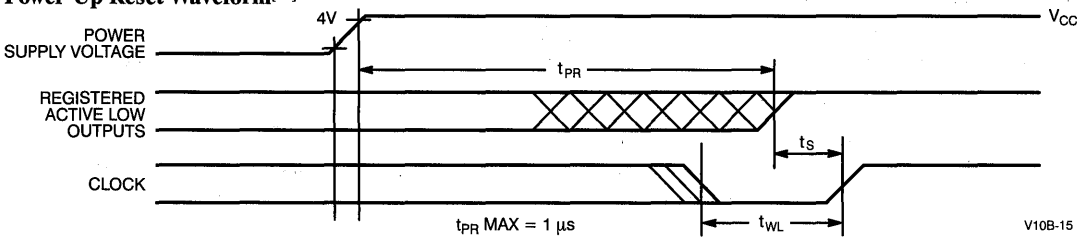
Parameter	V_X	Output Waveform—Measurement Level
$t_{ER}(-)$	1.5V	V_{OH} 0.5V V_X V10B-5
$t_{ER}(+)$	2.6V	V_{OL} 0.5V V_X V10B-6
$t_{EA}(+)$	V_{thc}	V_X 0.5V V_{OH} V10B-7
$t_{EA}(-)$	V_{thc}	V_X 0.5V V_{OL} V10B-8

(e) Test Waveforms

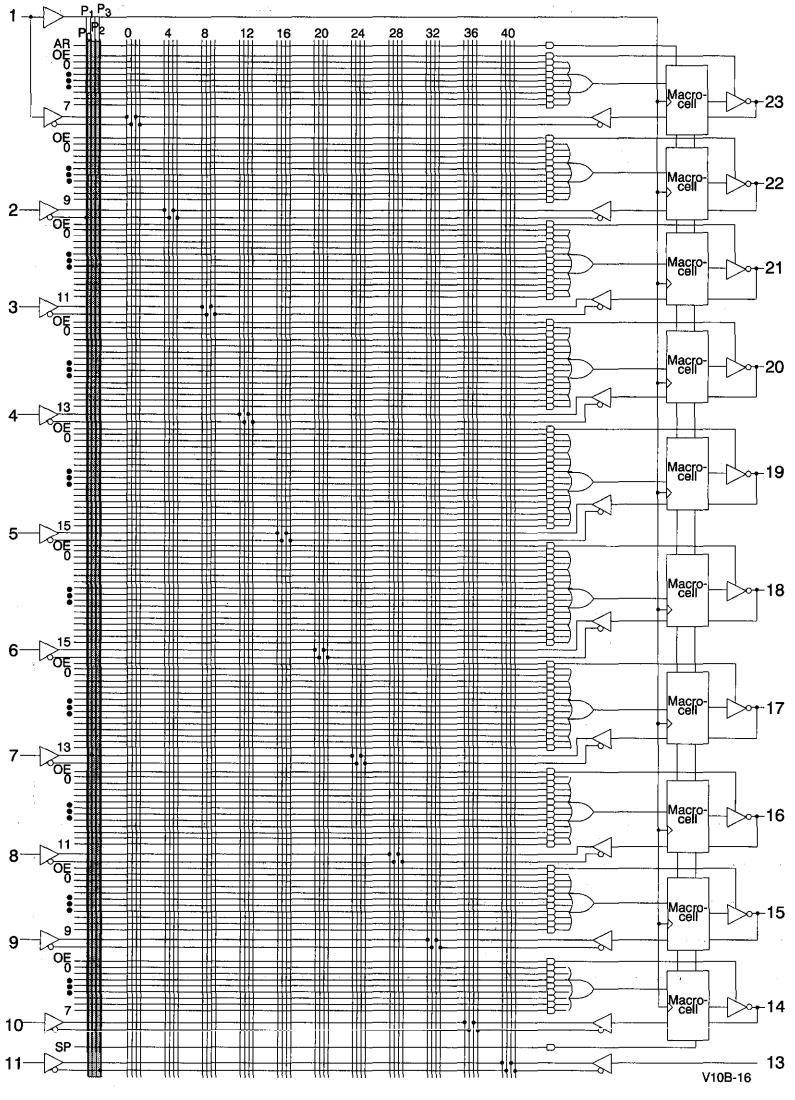
Switching Waveform



Power-Up Reset Waveform[14]

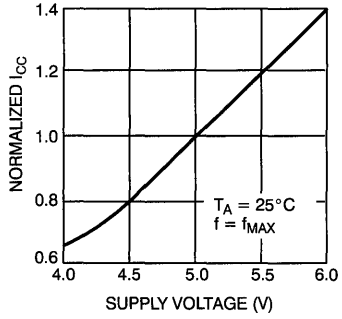


Functional Logic Diagram for PALC22V10B

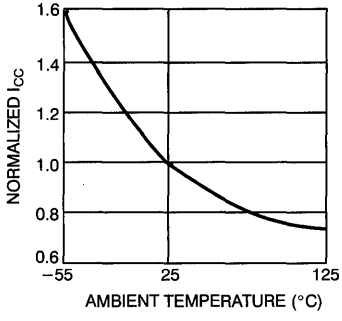


Typical DC and AC Characteristics

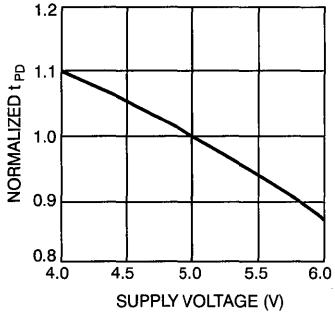
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. SUPPLY VOLTAGE



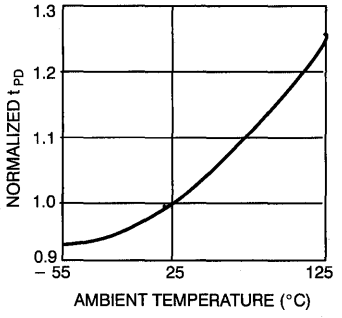
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. AMBIENT TEMPERATURE



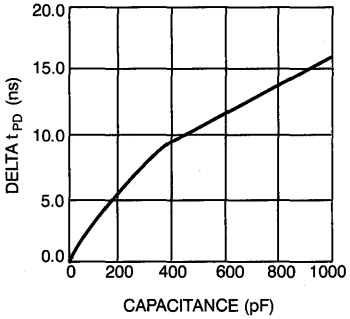
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



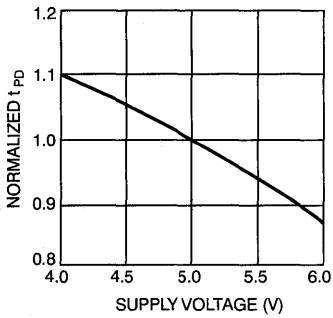
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



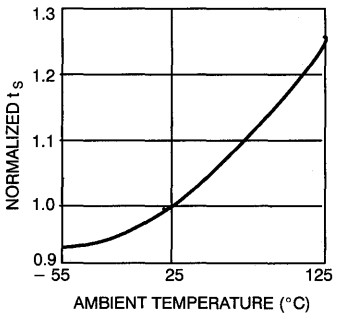
DELTA PROPAGATION TIME vs. OUTPUT LOADING



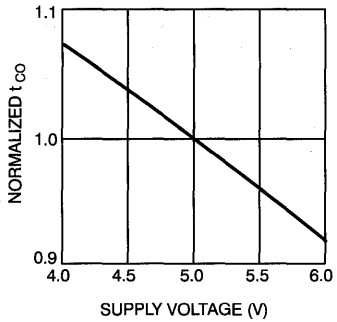
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



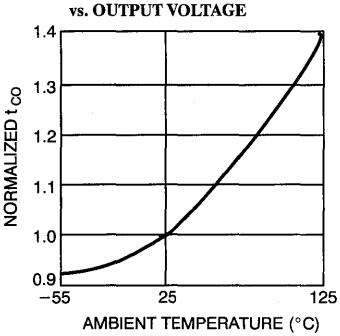
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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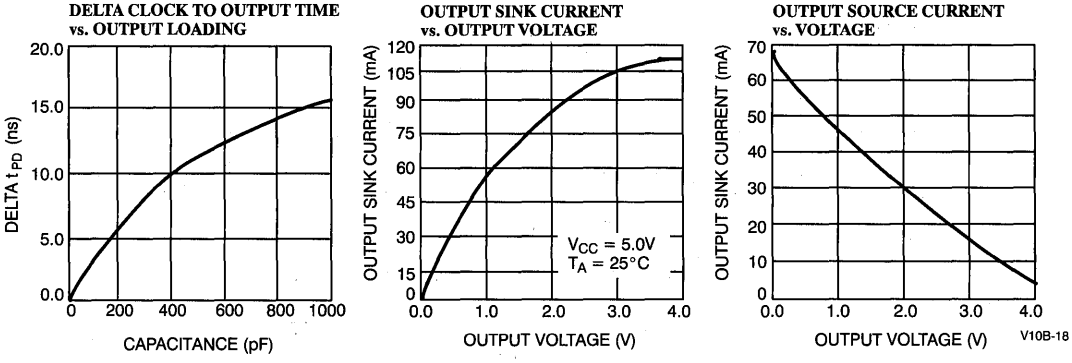
Typical DC and AC Characteristics (continued)



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PALC22V10B. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs that may cause "blank" check failures or "verify errors" when programming windowed parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC22V10B needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	15	10	10	PALC22V10B–15PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PALC22V10B–15WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10B–15HC	H64	28-Pin Windowed Leaded Chip Carrier	
100	15	10	10	PALC22V10B–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B–15WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–15HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B–15LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B–15KMB	K73	24-Lead Rectangular Cerpack	
100	20	17	15	PALC22V10B–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B–20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B–20LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B–20QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B–20KMB	K73	24-Lead Rectangular Cerpack	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38−00195

PAL22V10C
PAL22VP10C

CYPRESS SEMICONDUCTOR

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 6 ns**
  - **— t_{SU} = 3 ns**
  - **— f_{MAX} = 117 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10C)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

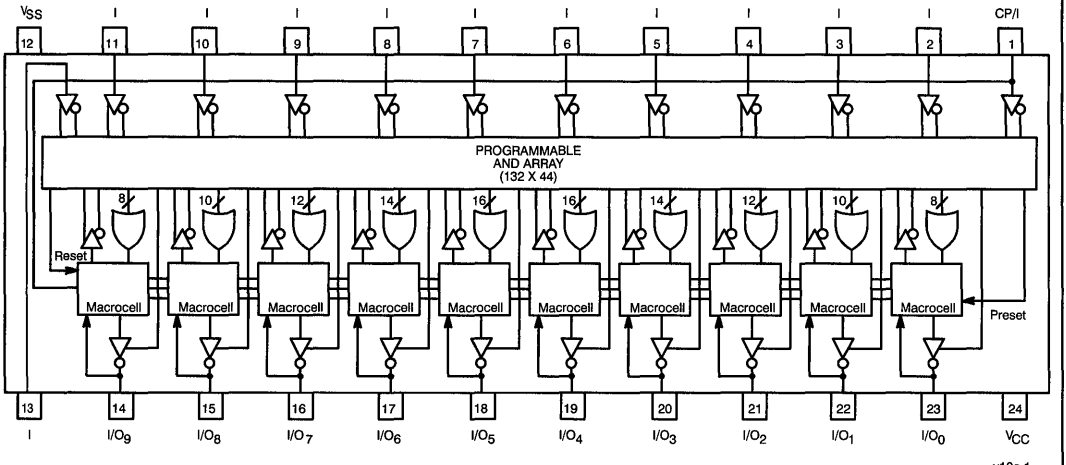
Functional Description

The Cypress PAL22V10C and PAL22VP10C are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10C and PAL22VP10C use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10C and PAL22VP10C provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10C and PAL22VP10C feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be

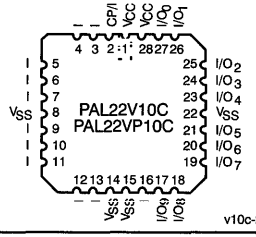
Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



v10c-1

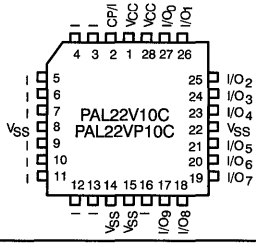
Pin Configurations

LCC (L) Top View



v10c-2

PLCC (J)/CLCC (Y) Top View



v10c-3

PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10C and PAL22VP10C automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10C and PAL22VP10C can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

Programmable Macrocell

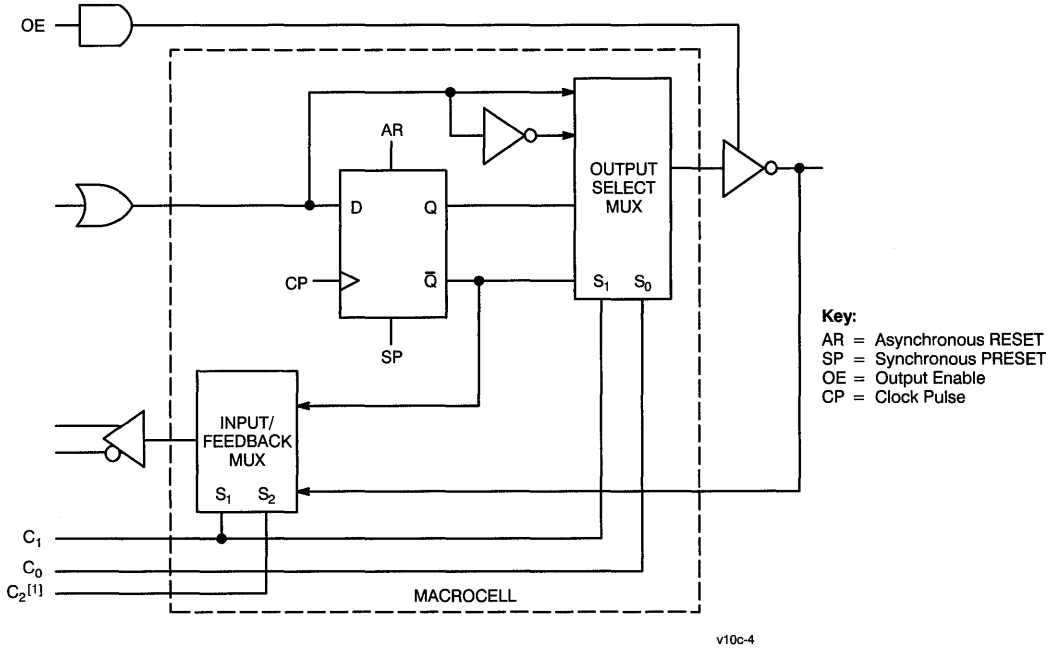
The PAL22V10C and PAL22VP10C each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10C two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10C provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10C and PAL22VP10C can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

4 PLDs

Macrocell

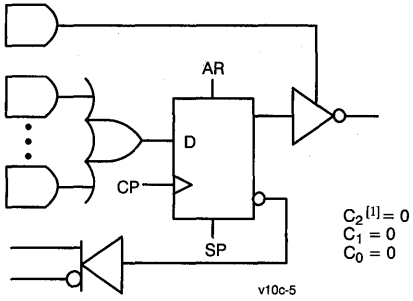


v10c-4

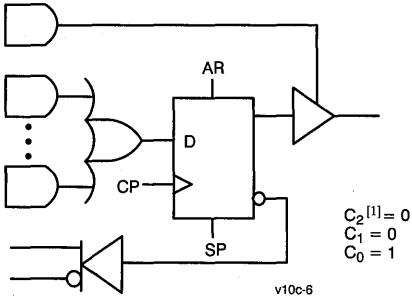
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

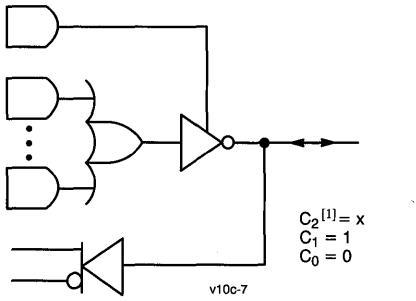
Notes:
1. PAL22VP10C only.



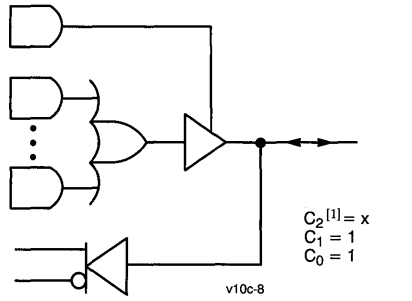
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

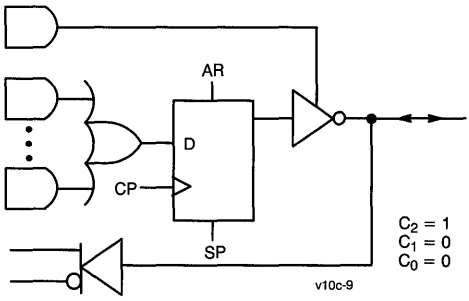


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

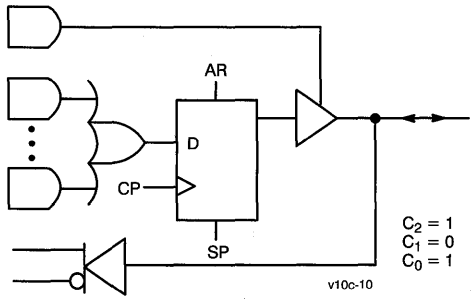


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10C and PAL22VP10C Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10C

Selection Guide

		22V10C–6 22VP10C–6	22V10C–7 22VP10C–7	22V10C–10 22VP10C–10	22V10C–12 22VP10C–12	22V10C–15 22VP10C–15
I_{CC} (mA)	Commercial	190	190	190	190	
	Military			190	190	190
t_{PD} (ns)	Commercial	6.0	7.5	10	12	
	Military			10	12	15
t_s (ns)	Commercial	3.0	3.0	3.6	4.5	
	Military			3.6	4.5	7.5
t_{CO} (ns)	Commercial	5.5	6.0	7.5	9.5	
	Military			7.5	9.5	10
f_{MAX} (MHz)	Commercial	117	111	90	71	
	Military			90	71	57

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC}

DC Input Voltage ..... – 0.5V to V_{CC}

DC Input Current ..... – 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	– 55°C to +125°C	5V ± 5%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	Com'l	2.4		V
			I_{OH} = – 2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			– 250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			– 100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			– 30	– 120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

Notes:

2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics[5]

Parameters	Description	22V10C–6 22VP10C–6		22V10C–7 22VP10C–7		22V10C–10 22VP10C–10		22V10C–12 22VP10C–12		22V10C–15 22VP10C–15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[6]	1	6	2	7.5	2	10	2	12	2	15	ns
t_{EA}	Input to Output Enable Delay	1	6	2	7.5	2	10	2	12	2	15	ns
t_{ER}	Input to Output Disable Delay[7]	1	6	2	7.5	2	10	2	12	2	15	ns
t_{CO}	Clock to Output Delay[6]	1	5.5	1	6.0	1	7.5	1	9.5	1	10	ns
t_S	Input or Feedback Set-Up Time	3		3		3.6		4.5		7.5		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	8.5		9		11.1		14		17.5		ns
t_{WH}	Clock Width HIGH[8]	3		3		3		3		6		ns
t_{WL}	Clock Width LOW[8]	3		3		3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]	117		111		90		71		57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[8, 10]	166		166		166		166		83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11]	142		133		100		83		66		MHz
t_{CF}	Register Clock to Feedback Input[12]		4		4.5		6.4		7.5		7.5	ns
t_{AW}	Asynchronous Reset Width	7.5		8.5		10		12		15		ns
t_{AR}	Asynchronous Reset Recovery Time	4		5		6		7		10		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	11	2	12	2	12	2	14	2	20	ns
t_{SPR}	Synchronous Preset Recovery Time	4		5		6		7		10		ns
t_{PR}	Power-Up Reset Time[13]	1		1		1		1		1		µs

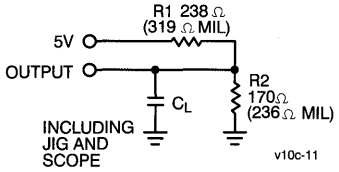
Capacitance[8]

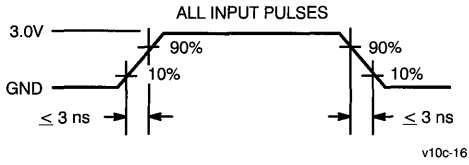
Parameters	Description	Max.	Units
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

5. AC test load used for all parameters except where noted.
6. This specification is guaranteed for all device outputs changing state in a given access cycle.
7. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
8. Tested initially and after any design or process changes that may affect these parameters.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
13. The registers in the PAL22V10C/PAL22VP10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

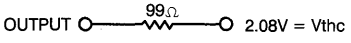
AC Test Loads and Waveforms





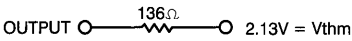
C_L[14]	Package
15 pF[15]	P/D
50 pF	J/K/L/Y

Equivalent to: THEVENIN EQUIVALENT

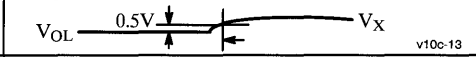
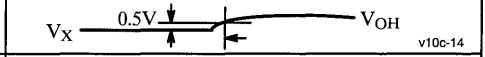
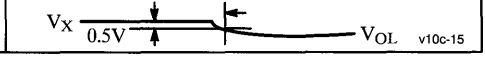


Commercial

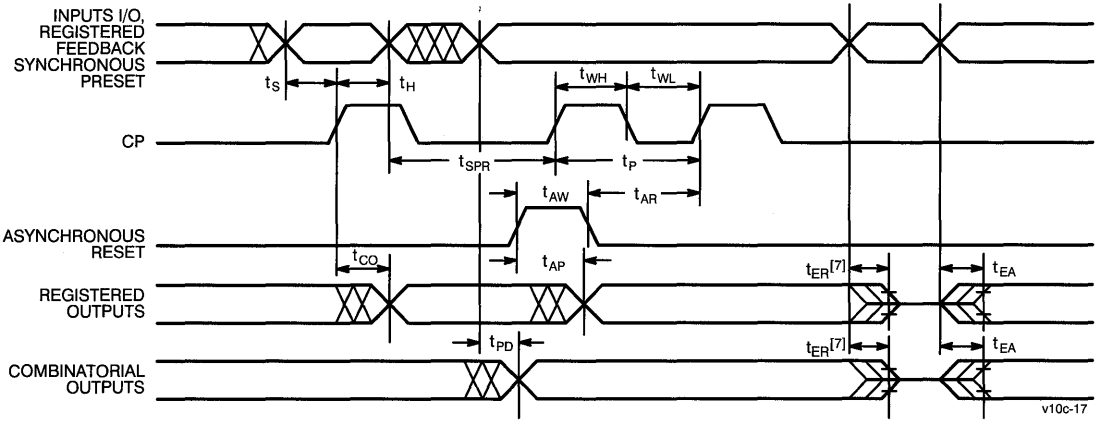
Equivalent to: THEVENIN EQUIVALENT



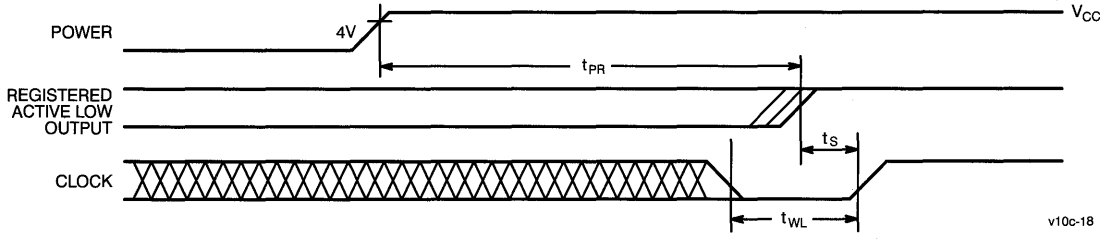
Military

Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	 v10c-12
t_{ER} (+)	2.6V	 v10c-13
t_{EA} (+)	1.5V	 v10c-14
t_{EA} (−)	1.5V	 v10c-15

Switching Waveform

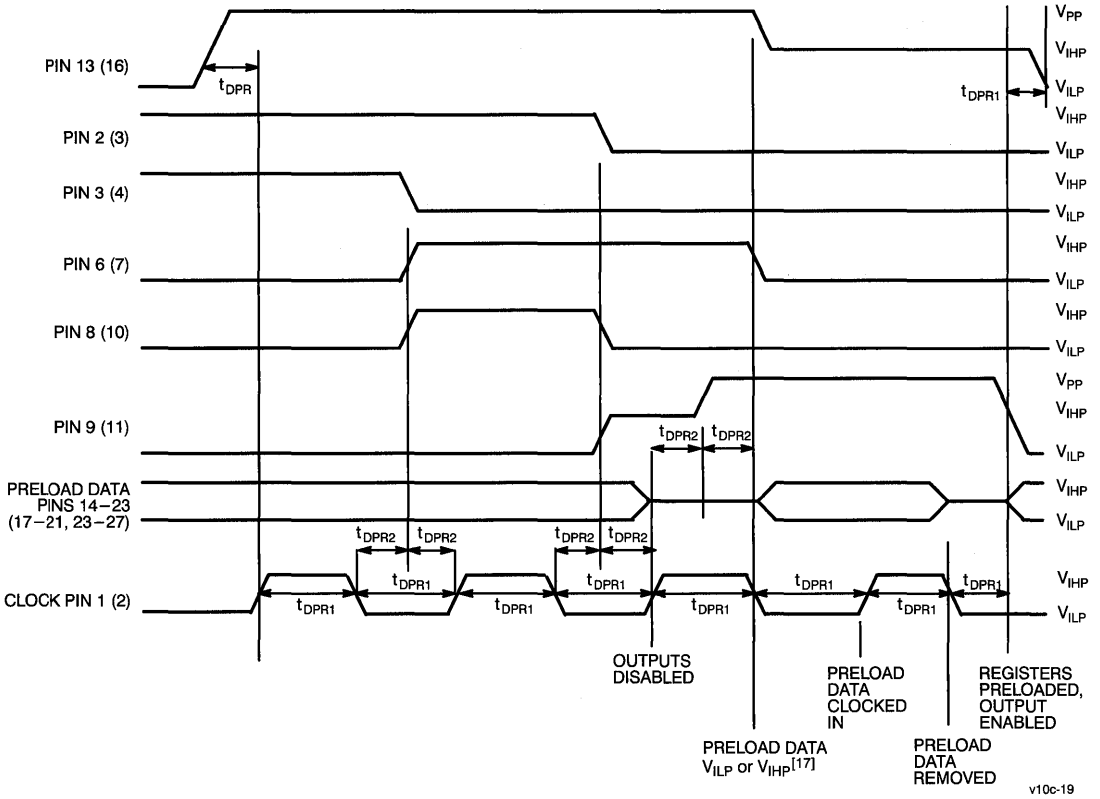


Power-Up Reset Waveform[13]



Notes:
14. C_L = 5 pF for t_{ER} measurement for all packages.
15. For high-capacitive load applications (C_L = 50 pF), use PAL22V10CF/PAL22VP10CF.

Preload Waveform[16]



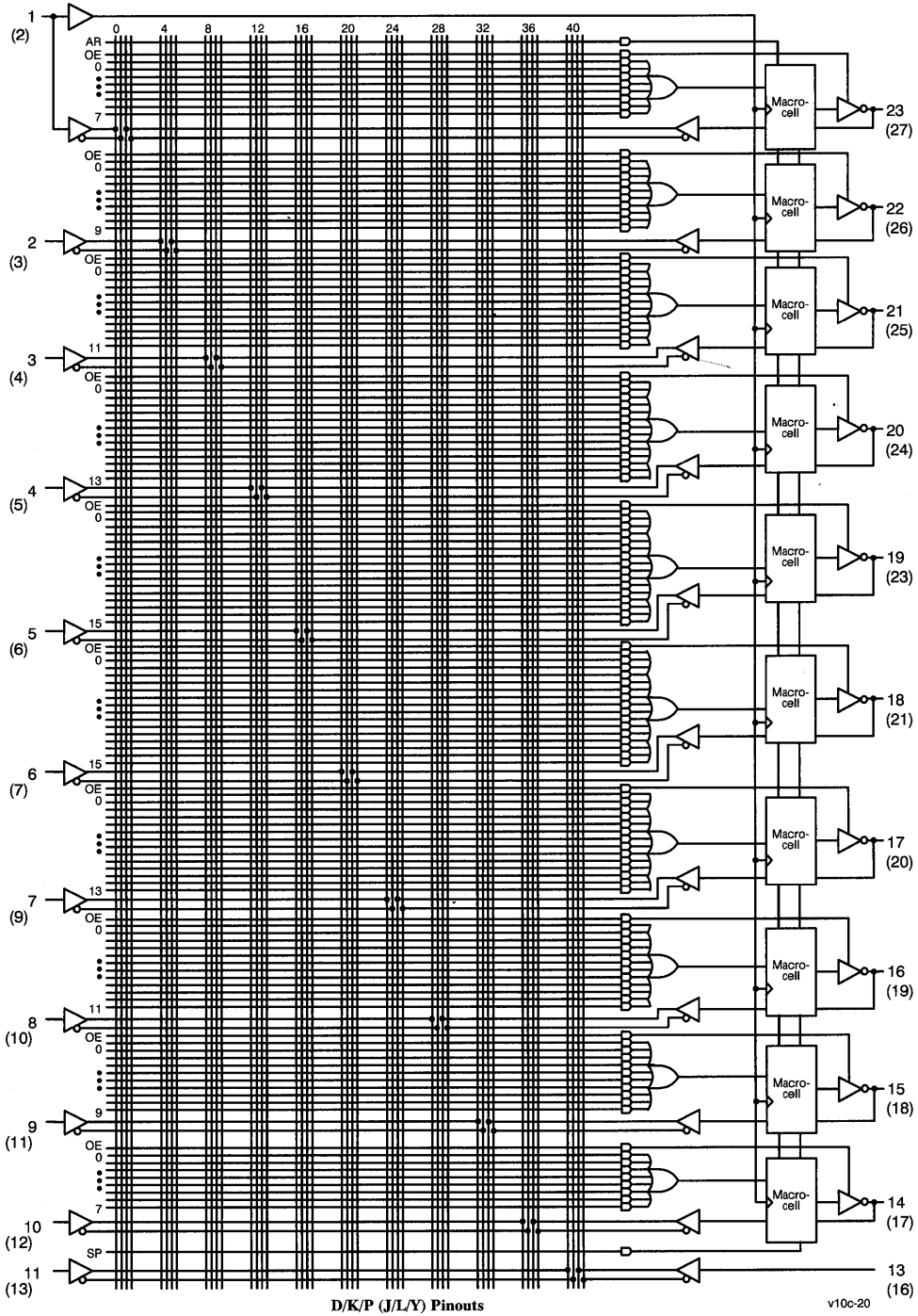
Notes:
16. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}
17. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/K/P (J/L/Y) Pinouts

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10C/PAL22VP10C



D/K/P (J/L/Y) Pinouts

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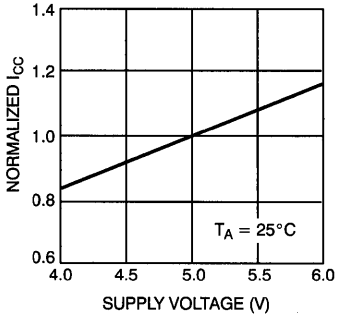
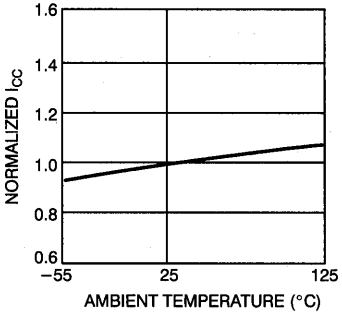
Typical DC and AC Characteristics

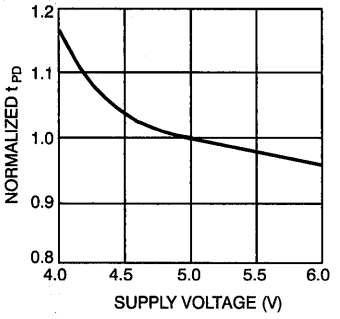
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



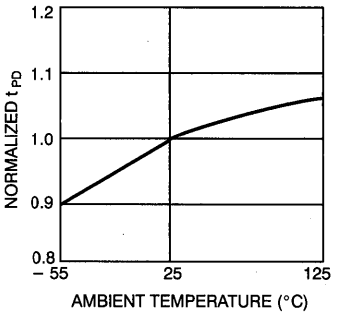
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



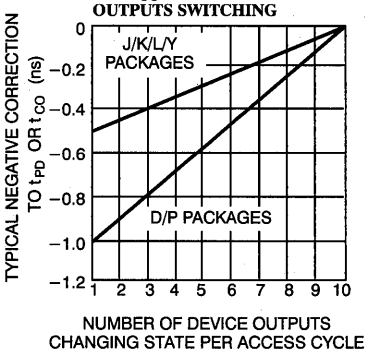
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



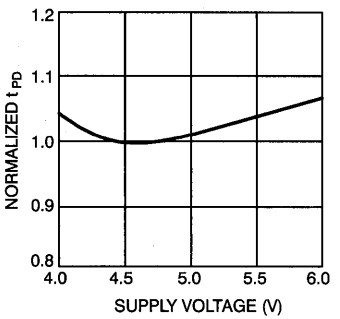
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



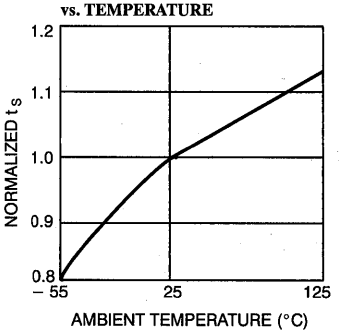
TYPICAL CORRECTION TO t_{PD} AND t_{CO} vs. NUMBER OF OUTPUTS SWITCHING



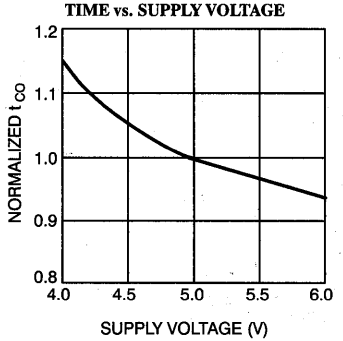
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



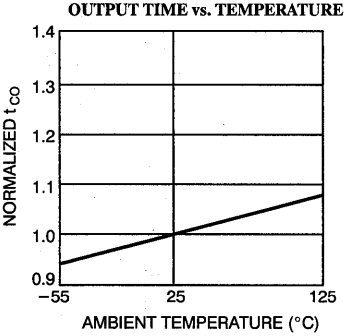
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



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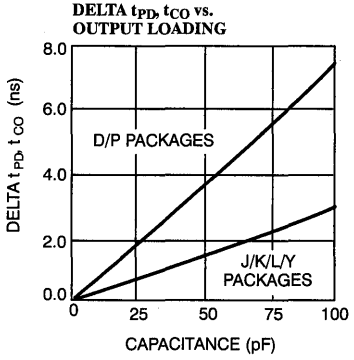
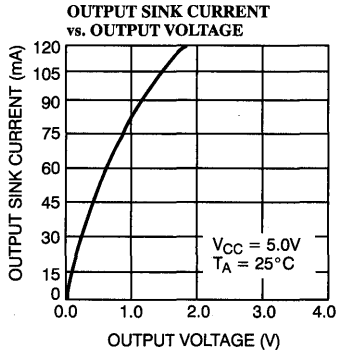
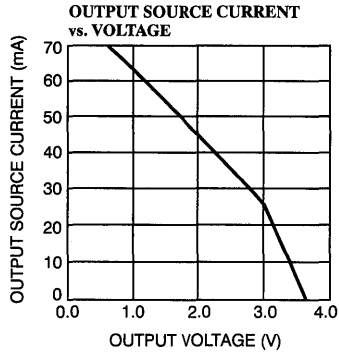
Typical DC and AC Characteristics (continued)







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Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	6	117	PAL22V10C–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22V10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–7YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
	10	90	PAL22V10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–10YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
			PAL22V10CM–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–10KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–10LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–10YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	
	12	71	PAL22V10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–12YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
			PAL22V10CM–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–12KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–12LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–12YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	
	15	57	PAL22V10CM–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–15KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–15LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–15YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	

Ordering Information (continued)

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	6	117	PAL22VP10C–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22VP10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–7YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
	10	90	PAL22VP10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–10YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
			PAL22VP10CM–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–10KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–10LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–10YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	
	12	71	PAL22VP10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–12YC	Y64	28-Pin Ceramic Leaded Chip Carrier	
			PAL22VP10CM–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–12KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–12LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–12YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	
	15	57	PAL22VP10CM–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–15KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–15LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–15YMB	Y64	28-Pin Ceramic Leaded Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00020–D

PAL22V10CF
PAL22VP10CF

CYPRESS SEMICONDUCTOR

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 7.5 ns**
  - **— t_{SU} = 3 ns**
  - **— f_{MAX} = 100 MHz**
  - **— Drives 50-pF load (C_L)**
- **"No Connect" PLCC pinout**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10CF)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

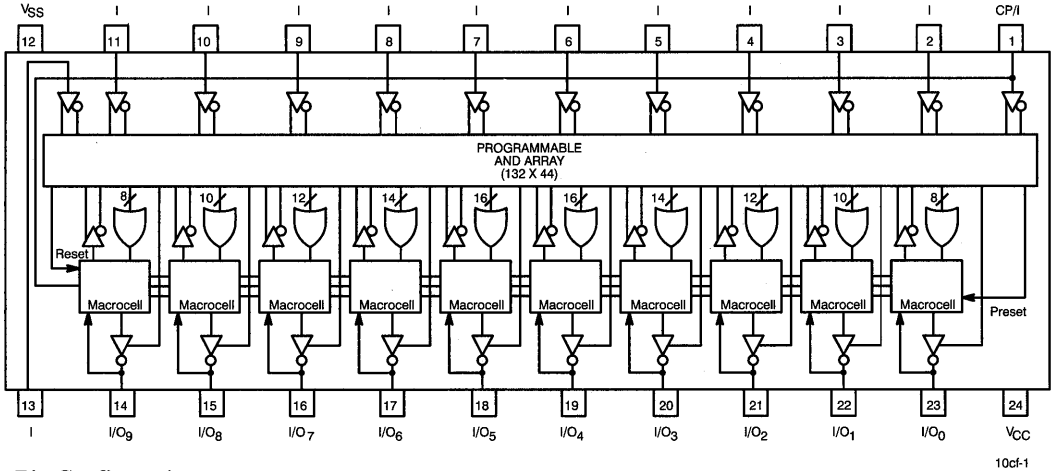
The Cypress PAL22V10CF and PAL22VP10CF are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10CF and PAL22VP10CF use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10CF and PAL22VP10CF provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10CF and PAL22VP10CF feature variable product-term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

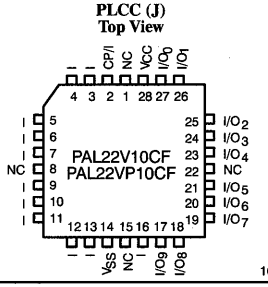
4 PLDs

Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



Pin Configuration

PLCC (J)
Top View



PAL is a registered trademark of Monolithic Memories Inc.
QuickProII is a trademark of Cypress Semiconductor Corporation.

Functional Description (continued)

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10CF and PAL22VP10CF automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10CF and PAL22VP10CF can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

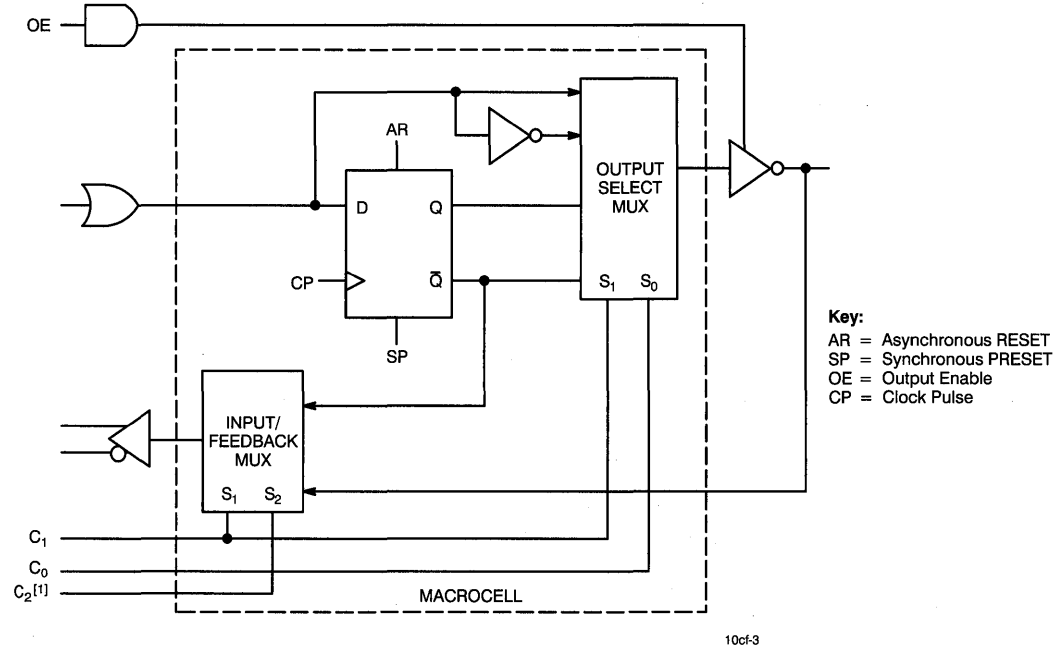
Programmable Macrocell

The PAL22V10CF and PAL22VP10CF each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10CF two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10CF provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10CF and PAL22VP10CF can be programmed using the QuickPro II™ programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

Macrocell

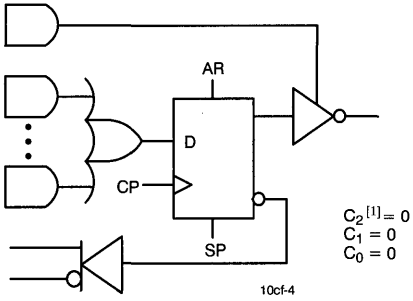


10cf-3

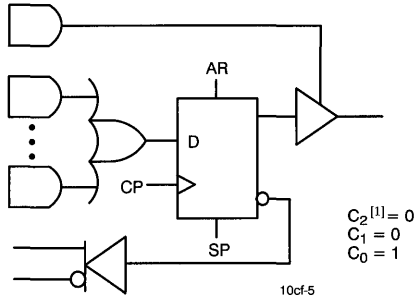
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

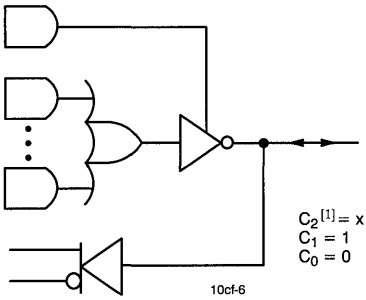
Notes:
1. PAL22VP10CF only.



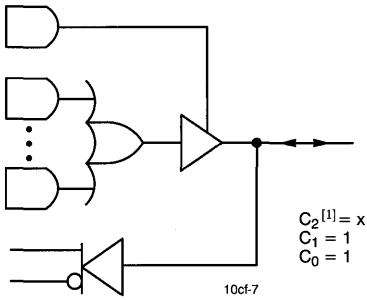
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

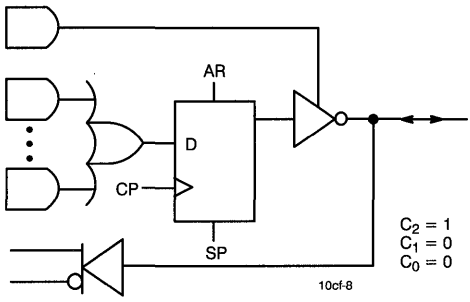


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

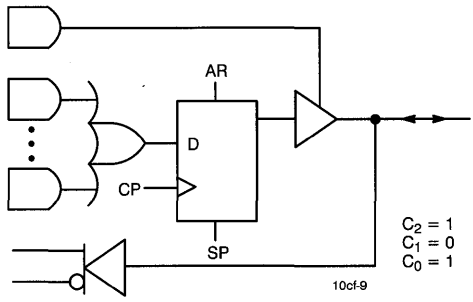


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10CF and PAL22VP10CF Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10CF

Selection Guide

	22V10CF–7 22VP10CF–7	22V10CF–10 22VP10CF–10
I_{CC} (mA)	190	190
t_{PD} (ns)	7.5	10
t_s (ns)	3.0	3.6
t_{CO} (ns)	7.0	7.5
f_{MAX} (MHz)	100	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC}

DC Input Voltage ..... – 0.5V to V_{CC}

DC Input Current ..... – 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.		– 250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.			100	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$		– 100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]		– 30	– 120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open			190	mA

Notes:

2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics[4]

Parameters	Description	22V10CF–7 22VP10CF–7		22V10CF–10 22VP10CF–10		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[5]	2	7.5	2	10	ns
t_{EA}	Input to Output Enable Delay	2	7.5	2	10	ns
t_{ER}	Input to Output Disable Delay[6]	2	7.5	2	10	ns
t_{CO}	Clock to Output Delay[5]	1	7.0	1	7.5	ns
t_S	Input or Feedback Set-Up Time	3		3.6		ns
t_H	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	10		11.1		ns
t_{WH}	Clock Width HIGH[7]	3		3		ns
t_{WL}	Clock Width LOW[7]	3		3		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[8]	100		90		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 9]	166		166		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[10]	133		100		MHz
t_{CF}	Register Clock to Feedback Input[11]		4.5		6.4	ns
t_{AW}	Asynchronous Reset Width	8.5		10		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	12	2	12	ns
t_{SPR}	Synchronous Preset Recovery Time	5		6		ns
t_{PR}	Power-Up Reset Time[12]	1		1		µs

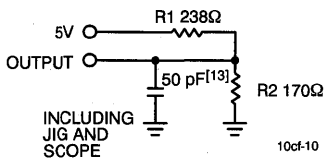
Capacitance[7]

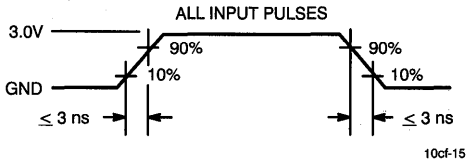
Parameters	Description	Max.	Units
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

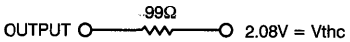
4. AC test load used for all parameters except where noted.
5. This specification is guaranteed for all device outputs changing state in a given access cycle.
6. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
7. Tested initially and after any design or process changes that may affect these parameters.
8. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
9. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
11. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 10) minus t_S.
12. The registers in the PAL22V10CF/PAL22VP10CF have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

AC Test Loads and Waveforms

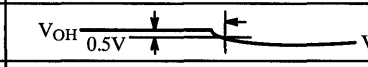
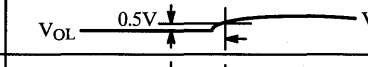
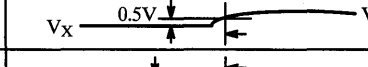
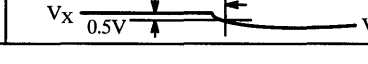




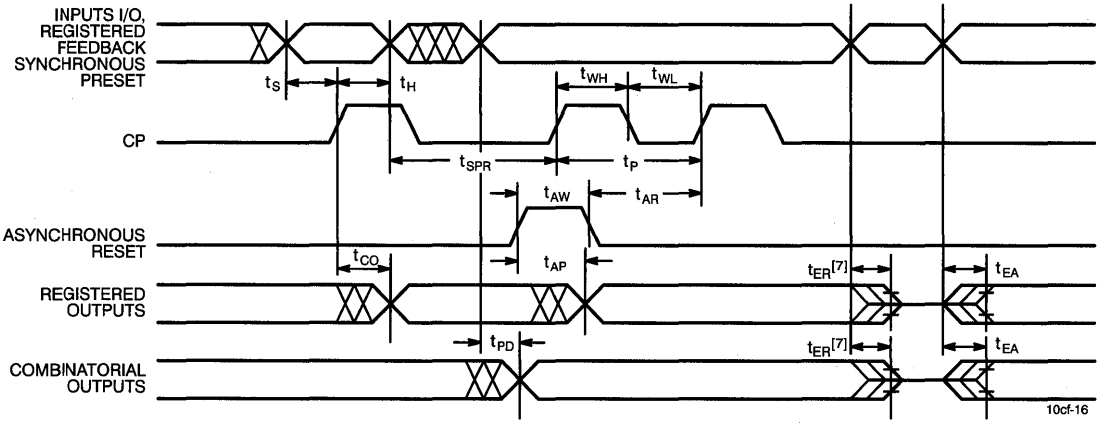
Equivalent to: THEVENIN EQUIVALENT



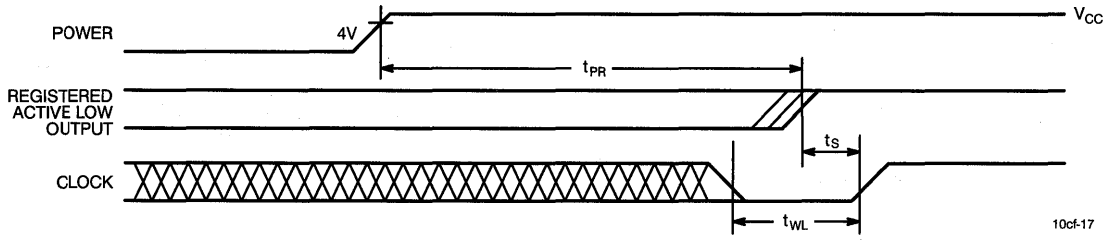
Commercial

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 10cf-11
$t_{ER(+)}$	2.6V	 10cf-12
$t_{EA(+)}$	1.5V	 10cf-13
$t_{EA(-)}$	1.5V	 10cf-14

Switching Waveform

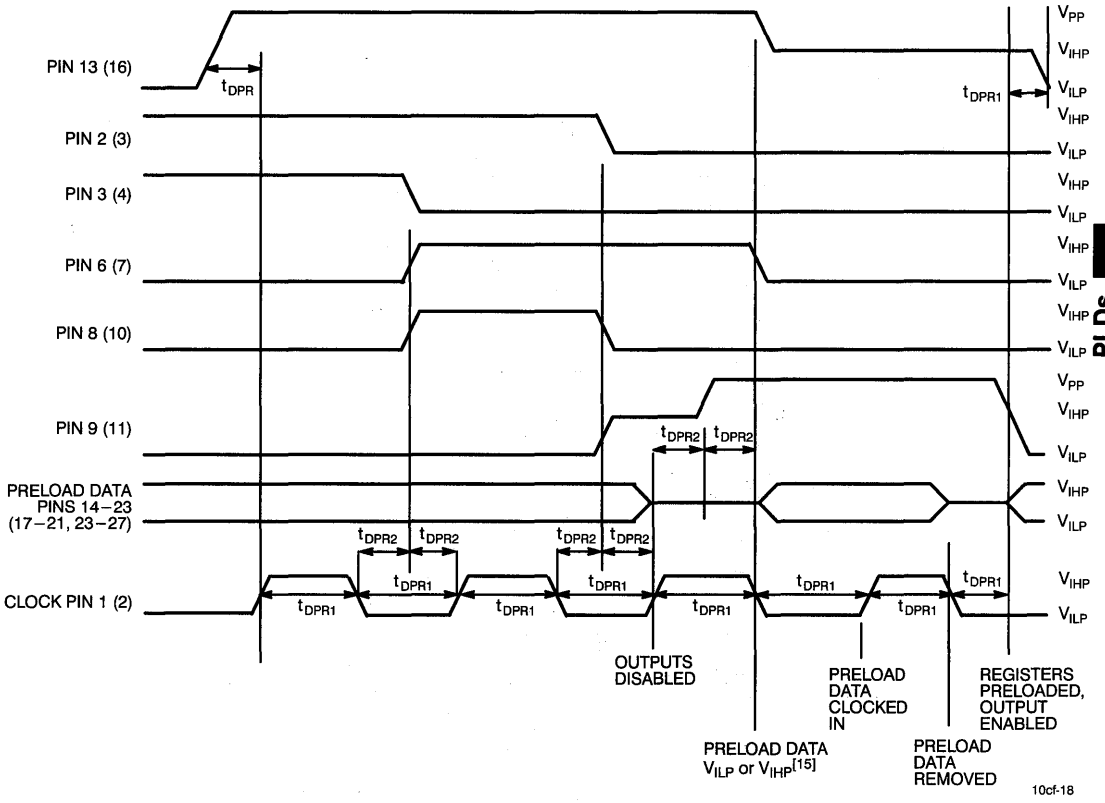


Power-Up Reset Waveform[13]



Notes:
13. C_L= 5 pF for t_{ER} measurement for all packages.

Preload Waveform[14]



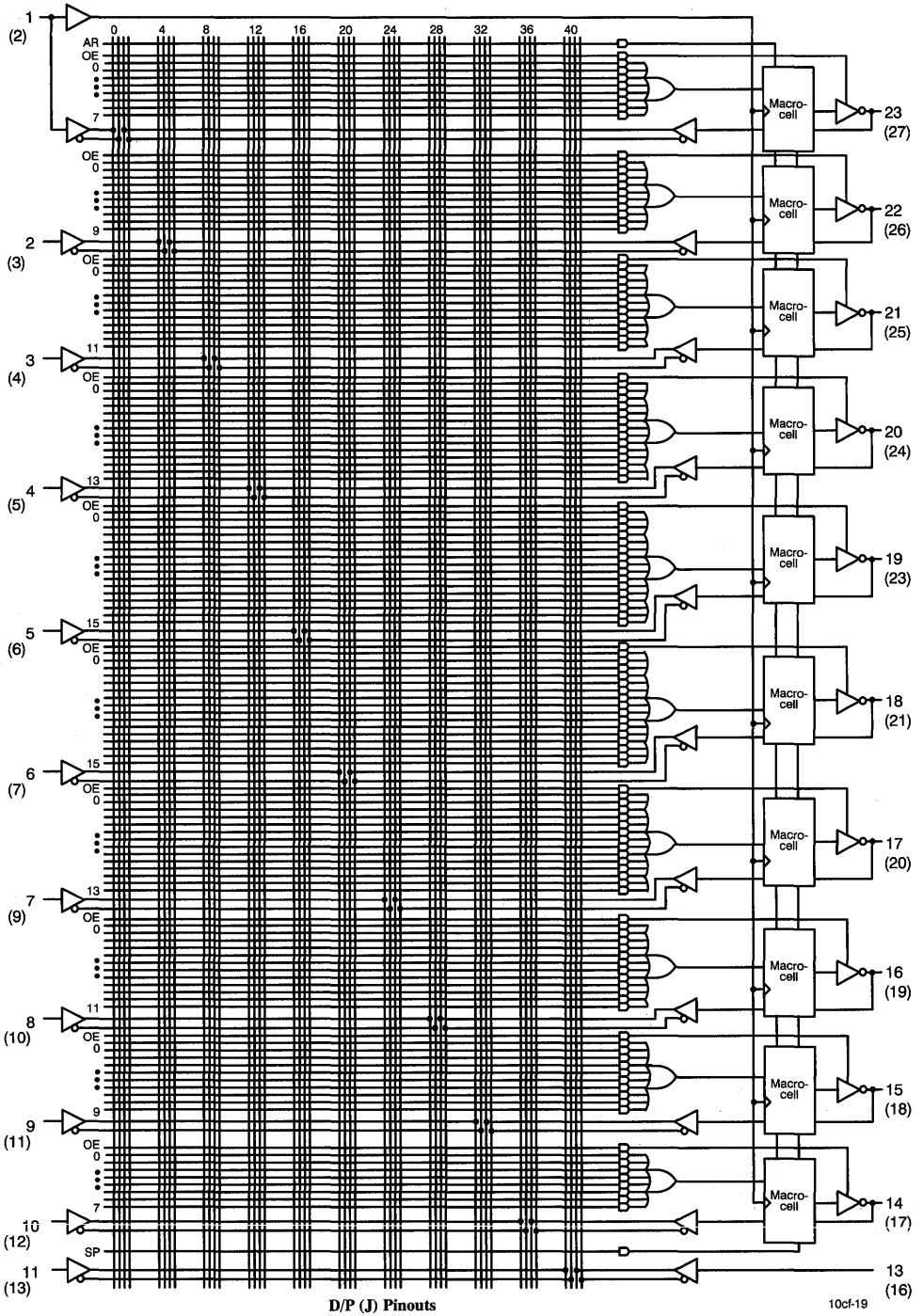
Notes:
14. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
15. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/P (J) Pinouts

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10CF/PAL22VP10CF

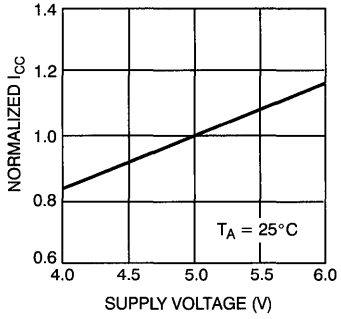


D/P (J) Pinouts

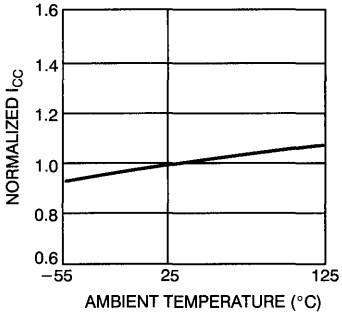
10cf-19

Typical DC and AC Characteristics

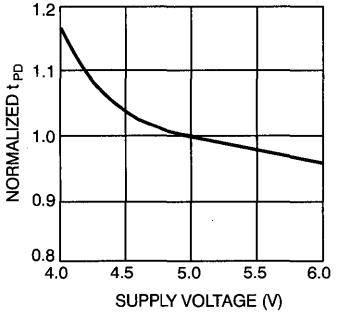
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



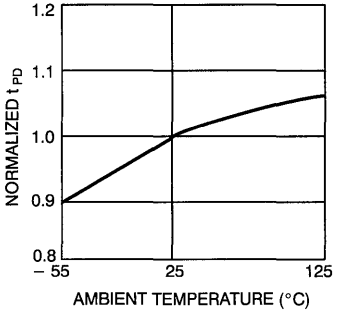
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



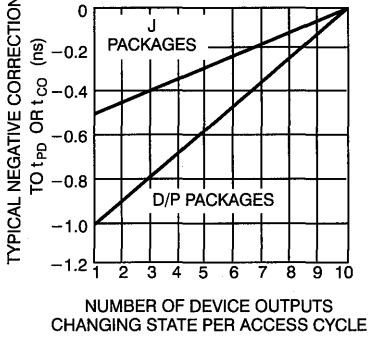
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



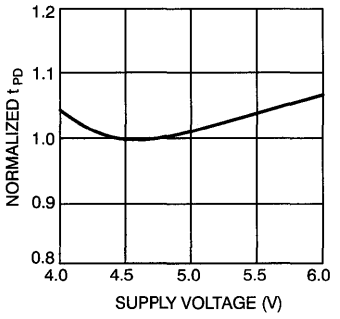
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



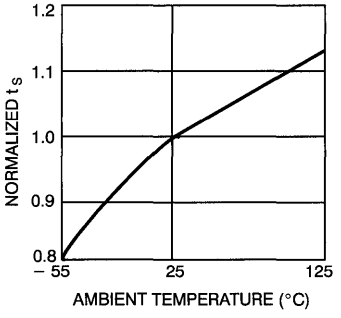
TYPICAL CORRECTION TO t_{PD} AND t_{CO} vs. NUMBER OF OUTPUTS SWITCHING



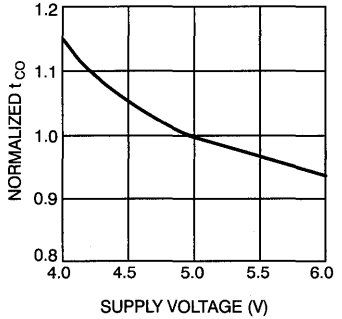
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



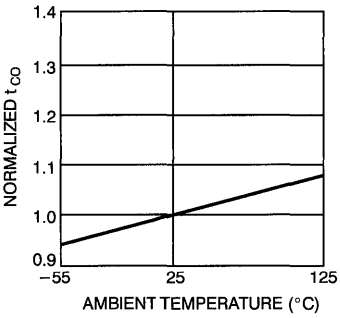
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE

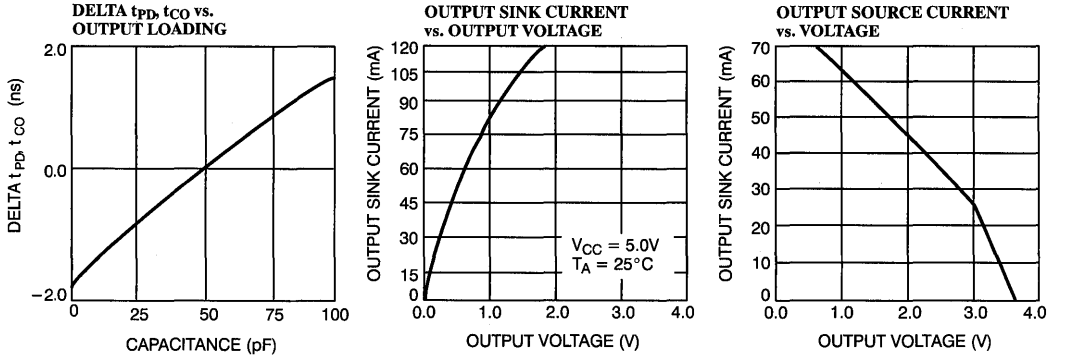


NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



10cf-20

Typical DC and AC Characteristics (continued)



10cf-21

Ordering Information

I_{CC} (mA)	t_{AA} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Package Type	Operating Range
190	7.5	100	PAL22V10CF−7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10CF−7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10CF−7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10CF−7DC	D14	24-Lead (300-Mil) CerDIP	
			PAL22VP10CF−7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10CF−7PC	P13	24-Lead (300-Mil) Molded DIP	
	10	90	PAL22V10CF−10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10CF−10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10CF−10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10CF−10DC	D14	24-Lead (300-Mil) CerDIP	
			PAL22VP10CF−10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10CF−10PC	P13	24-Lead (300-Mil) Molded DIP	

Document #: 38-A−00020

PALC22V10D

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 90 mA max. commercial (10 ns)**
  - **— 130 mA max. commercial (7.5 ns)**
- **CMOS Flash EPROM technology for electrical erasability and reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **Up to 22 input terms and 10 outputs**
- **DIP, LCC, and PLCC available**
  - **— 7.5 ns commercial version**
    - **5 ns t_{CO}**
    - **5 ns t_S**
    - **7.5 ns t_{PD}**
    - **133-MHz state machine**
  - **— 10 ns military and industrial versions**
    - **6 ns t_{CO}**
    - **6 ns t_S**
    - **10 ns t_{PD}**
    - **110-MHz state machine**
  - **— 15-ns commercial and military versions**
  - **— 25-ns commercial and military versions**
- **High reliability**
  - **— Proven Flash EPROM technology**
  - **— 100% programming and functional testing**

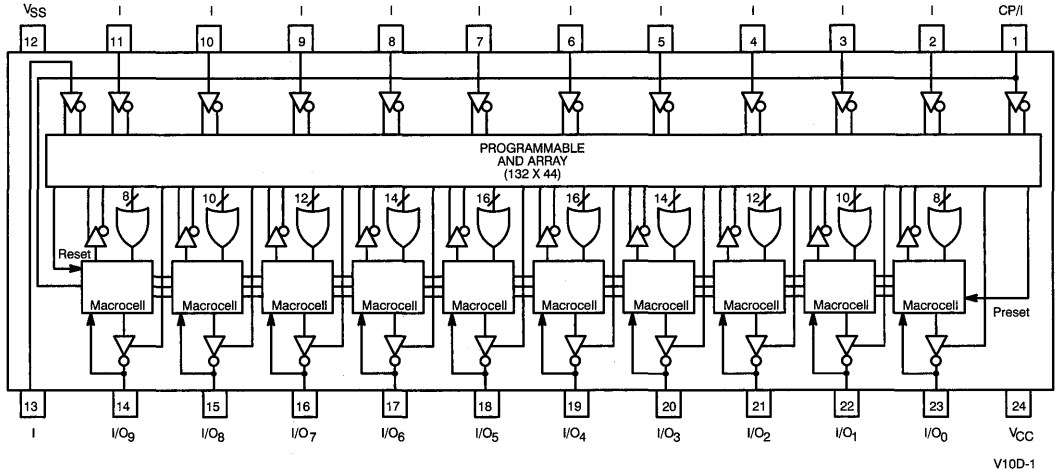
Functional Description

The Cypress PALC22V10D is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and the programmable macrocell.

The PALC22V10D is executed in a 24-pin 300-mil molded DIP, a 300-mil cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. The 22V10D can be electrically

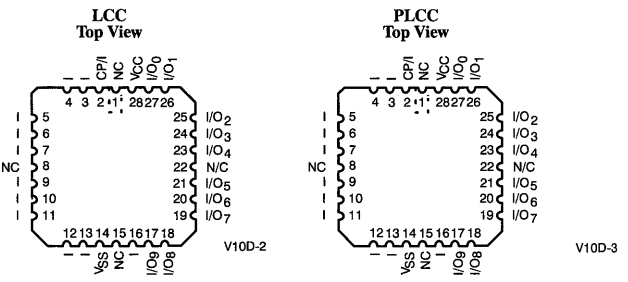
4 PLDs

Logic Block Diagram (PDIP/CDIP)



V10D-1

Pin Configuration



V10D-2 V10D-3

PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

erased and reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as "registered" or "combinatorial." Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10D features a variable product term architecture. There are 5 pairs of product term sums beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10D is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10D include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets upon power-up.

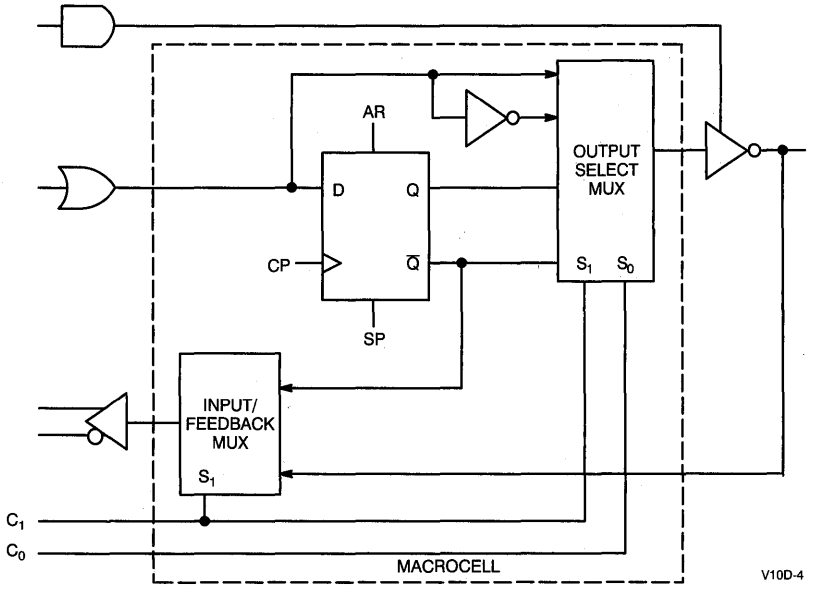
The PALC22V10D featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500- to 800-gate-array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control state machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PALC22V10D provides lower-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

Configuration Table 1

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

DC Programming Voltage 12.5V

Latch-Up Current ..... >200 mA

Static Discharge Voltage (per MIL−STD−883, Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[1]	− 55°C to +125°C	5V ±10%
Industrial	− 40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Com'l	2.4		V
			I_{OH} = − 2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}[4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			−0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			− 10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[5, 6]			− 30	− 90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open in Unprogrammed Device	10, 15, 25 ns	Com'l		90	mA
			7.5 ns			130	mA
			15, 25 ns	Mil/Ind		120	mA
			10 ns			120	mA
I_{CC2}[6]	Operating Power Supply Current	V_{CC} = Max., V_{IL} = 0V, V_{IH} = 3V, Output Open, Device Programmed as a 10-Bit Counter, f = 25 MHz	10, 15, 25 ns	Com'l		110	mA
			7.5 ns			140	mA
			15, 25 ns	Mil/Ind		130	mA
			10 ns			130	mA

Capacitance[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

Endurance Characteristics[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to −3.0V for pulse durations less than 20 ns.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested initially and after any design or process changes that may affect these parameters.

Commercial Switching Characteristics PALC22V10D[2, 7]

Parameter	Description	22V10D–7		22V10D–10		22V10D–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	7.5	3	10	3	15	ns
t_{EA}	Input to Output Enable Delay[10]		8		10		15	ns
t_{ER}	Input to Output Disable Delay[11]		8		10		15	ns
t_{CO}	Clock to Output Delay[8, 9]	2	5	2	7	2	8	ns
t_{S1}	Input or Feedback Set-Up Time	5		6		10		ns
t_{S2}	Synchronous Preset Set-Up Time	6		7		10		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	10		12		20		ns
t_{WH}	Clock Width HIGH[6]	3		3		6		ns
t_{WL}	Clock Width LOW[6]	3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	100		76.9		55.5		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	166		142		83.3		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6, 14]	133		111		68.9		MHz
t_{CF}	Register Clock to Feedback Input[6, 15]		2.5		3		4.5	ns
t_{AW}	Asynchronous Reset Width	8		10		15		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		10		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		13		20	ns
t_{SPR}	Synchronous Preset Recovery Time	6		8		10		ns
t_{PR}	Power-Up Reset Time[6, 16]	1		1		1		μs

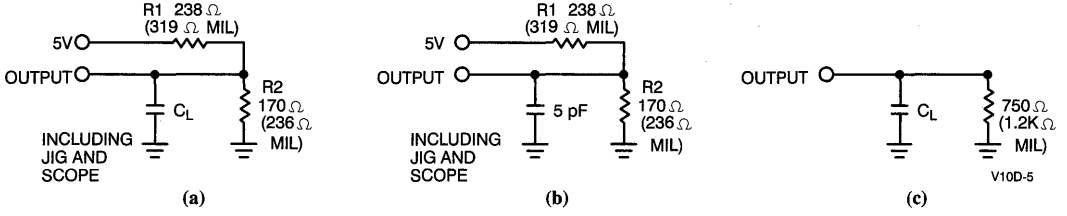
Notes:

7. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{ER} and $t_{EA}(+)$. Part (b) of AC Test Loads and Waveforms is used for t_{ER}. Part (c) of AC Test Loads and Waveforms is used for $t_{EA}(+)$.
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. The test load of part (a) of AC Test Loads and Waveforms is used for measuring $t_{EA}(-)$. The test load of part (c) of AC Test Loads and Waveforms is used for measuring $t_{EA}+$ only. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
11. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
15. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 11 above) minus t_S.
16. The registers in the PALC22V10D have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

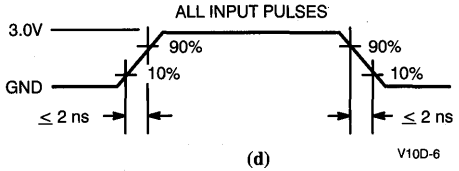
Military and Industrial Switching Characteristics PALC22V10D[2, 7]

Parameter	Description	22V10D–10		22V10D–15		22V10D–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[9]		10		15		25	ns
t_{EA}	Input to Output Enable Delay[11]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[11]		10		15		25	ns
t_{CO}	Clock to Output Delay[9]		7		8		15	ns
t_{S1}	Input or Feedback Set-Up Time	6		10		18		ns
t_{S2}	Synchronous Preset Set-Up Time	7		10		18		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	12		20		33		ns
t_{WH}	Clock Width HIGH[6]	3		6		14		ns
t_{WL}	Clock Width LOW[6]	3		6		14		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	76.9		50.0		30.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	142		83.3		35.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6, 14]	111		68.9		32.2		MHz
t_{CF}	Register Clock to Feedback Input[6, 14]		3		4.5		13	ns
t_{AW}	Asynchronous Reset Width	10		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	6		12		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	8		20		25		ns
t_{PR}	Power-Up Reset Time[6, 16]	1		1		1		µs

AC Test Loads and Waveforms

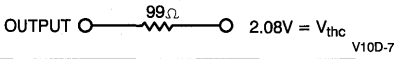


AC Test Loads and Waveforms (continued)

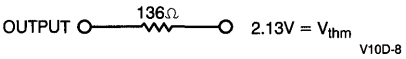


(d)

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)

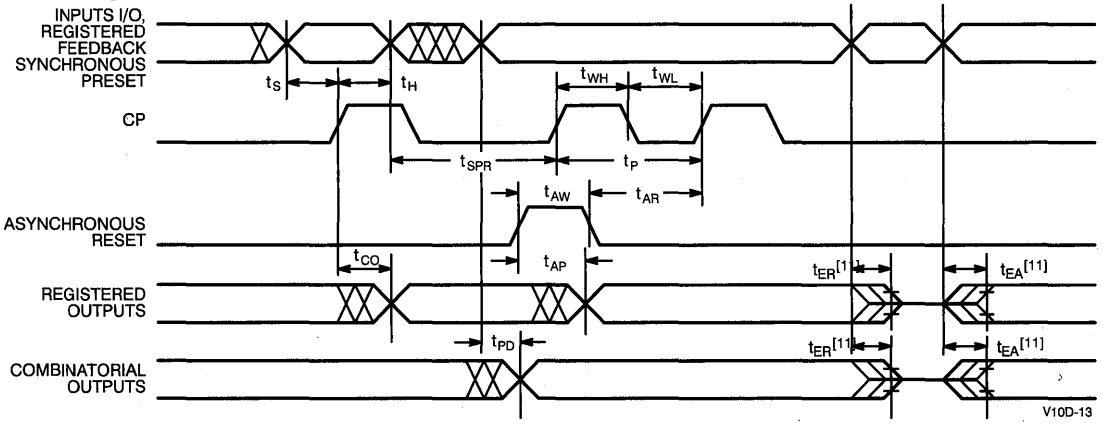


Load Speed	C_L	Package
7.5, 10, 15, 25 ns	50 pF	PDIP, CDIP, PLCC, LCC

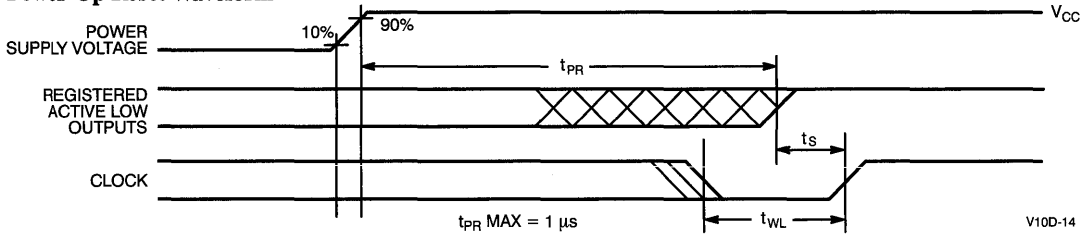
Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	V_{OH}, 0.5V, V_X — V10D-9
t_{ER} (+)	2.6V	V_{OL}, 0.5V, V_X — V10D-10
t_{EA} (+)	0V	V_X, 1.5V, V_{OH} — V10D-11
t_{EA} (−)	V_{thc}	V_X, 0.5V, V_{OL} — V10D-12

(e) Test Waveforms

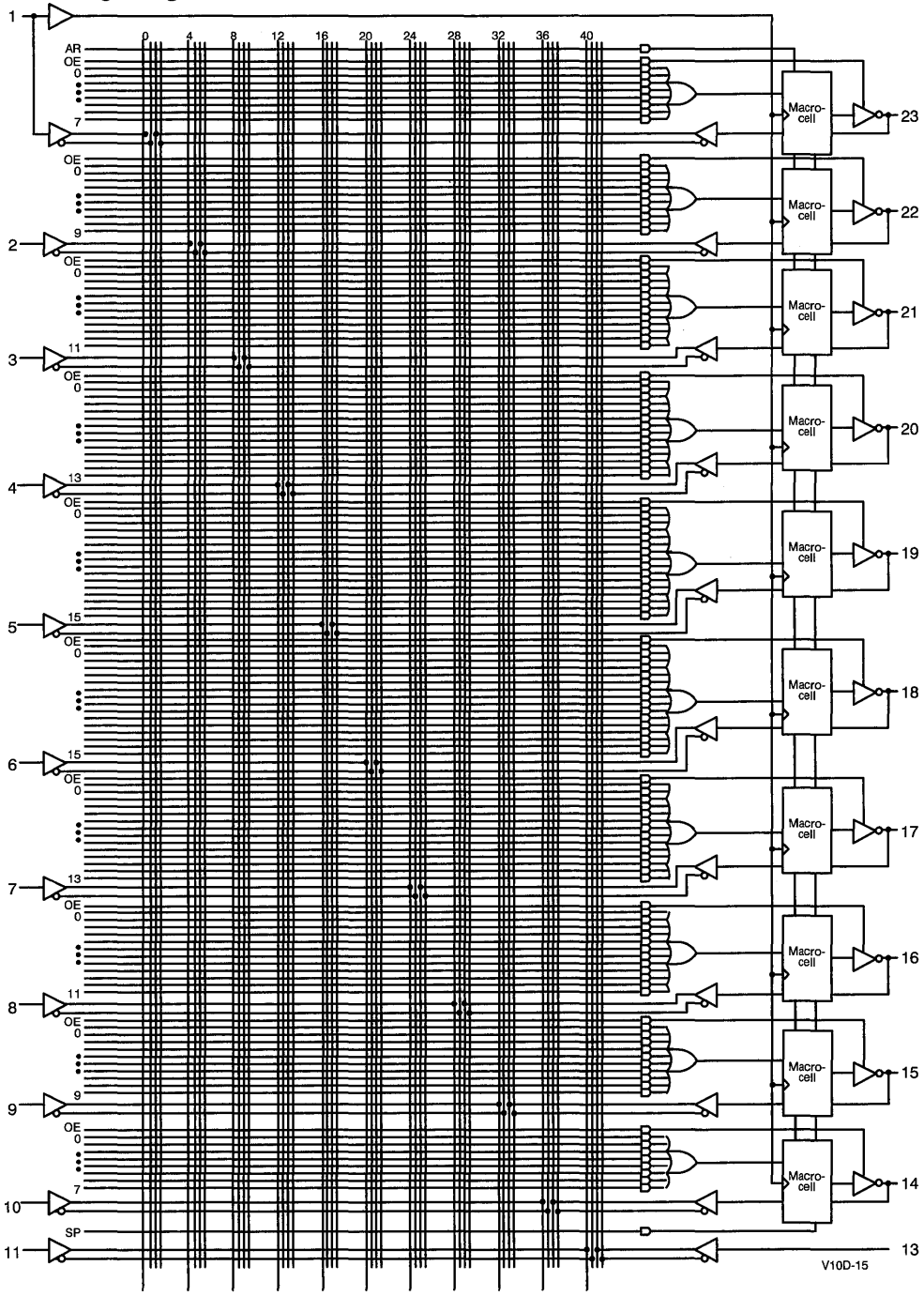
Switching Waveform



Power-Up Reset Waveform[16]



Functional Logic Diagram for PALC22V10D



Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
130	7.5	5	5	PALC22V10D–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–7PC	P13	24-Lead (300-Mil) Molded DIP	
90	10	6	7	PALC22V10D–10JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–10PC	P13	24-Lead (300-Mil) Molded DIP	
150	10	6	7	PALC22V10D–10DMB	D14	24-Lead (300-Mil) CerDIP	Military/ Industrial
				PALC22V10D–10JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–10KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–10LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–10PI	P13	24-Lead (300-Mil) Molded DIP	
90	15	7.5	10	PALC22V10D–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–15PC	P13	24-Lead (300-Mil) Molded DIP	
120	15	7.5	10	PALC22V10D–15DMB	D14	24-Lead (300-Mil) CerDIP	Military/ Industrial
				PALC22V10D–15JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–15KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–15LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–15PI	P13	24-Lead (300-Mil) Molded DIP	
	25	15	15	PALC22V10D–25DMB	D14	24-Lead (300-Mil) CerDIP	
				PALC22V10D–25JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–25KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–25LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–25PI	P13	24-Lead (300-Mil) Molded DIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

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Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 5 ns**
  - **— t_{SU} = 2.5 ns**
  - **— f_{MAX} = 153.8 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10G)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

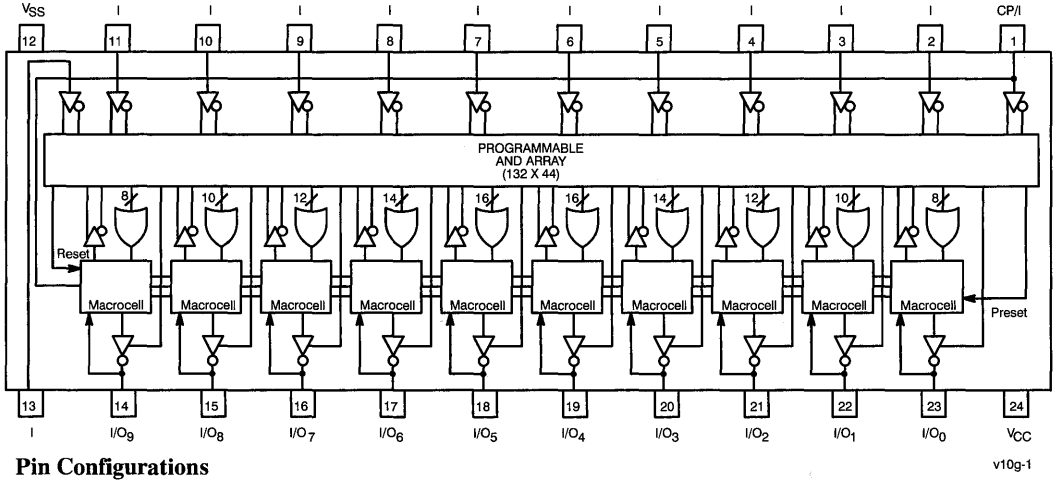
Functional Description

The Cypress PAL22V10G and PAL22VP10G are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10G and PAL22VP10G use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10G and PAL22VP10G provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10G and PAL22VP10G feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

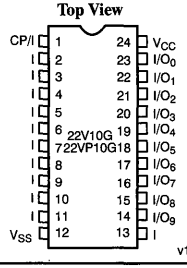
Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



v10g-1

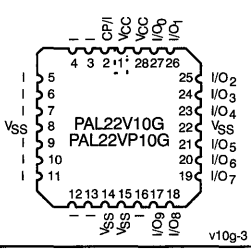
Pin Configurations

DIP (P, D) Top View



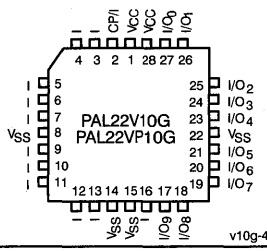
v10g-2

LCC (L) Top View



v10g-3

PLCC (J) Top View



v10g-4

PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10G and PAL22VP10G automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10G and PAL22VP10G can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

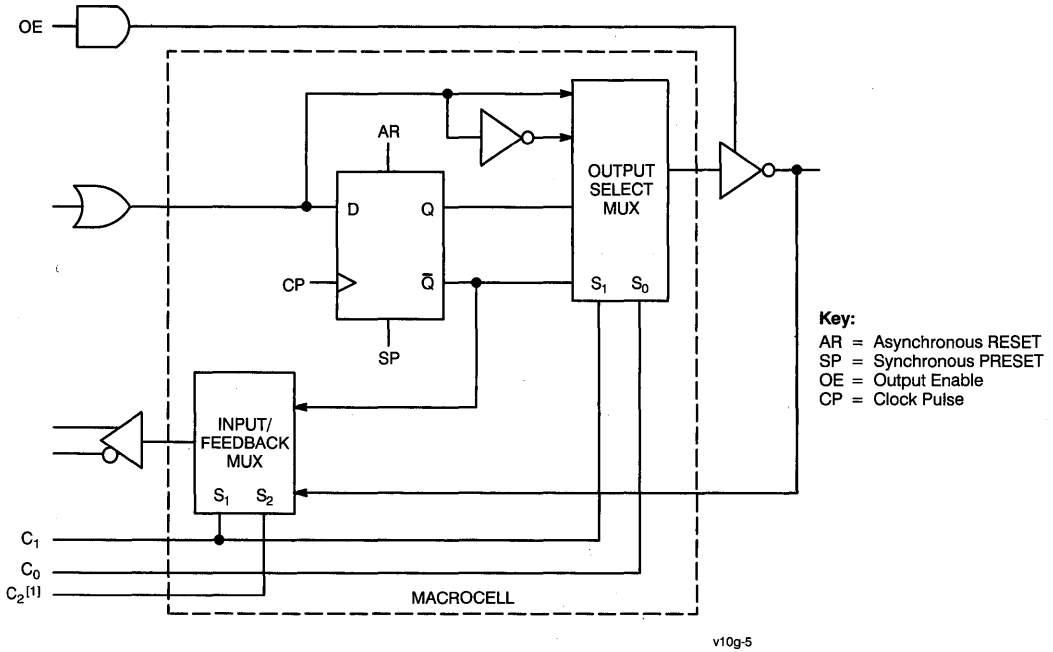
Programmable Macrocell

The PAL22V10G and PAL22VP10G each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10G two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10G provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10G and PAL22VP10G can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

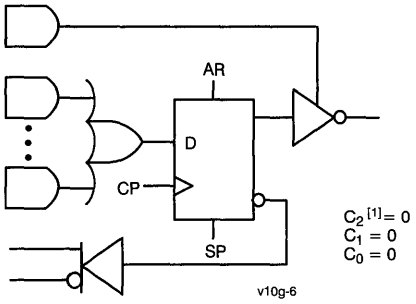
Macrocell



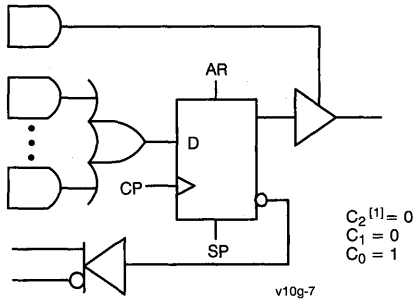
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

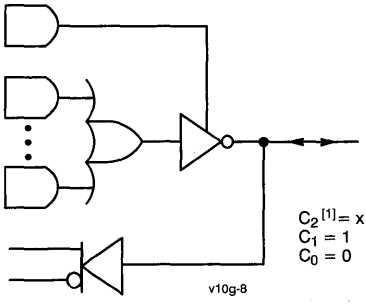
Notes:
1. PAL22V10G only.



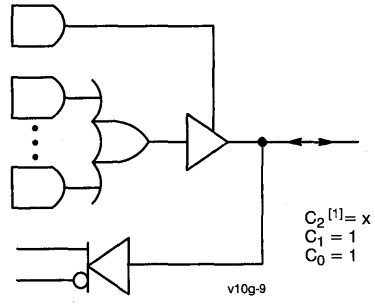
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

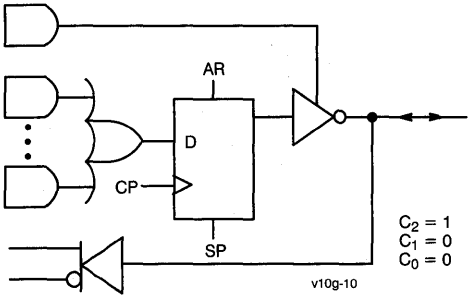


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

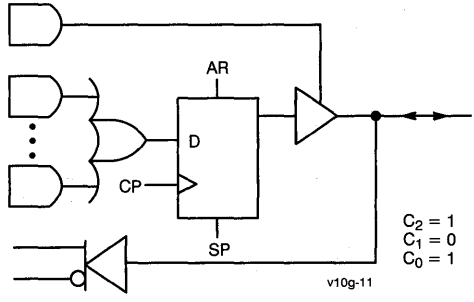


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10G and PAL22VP10G Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22V10G

Selection Guide

		22V10G–5 22VP10G–5	22V10G–6 22VP10G–6	22V10G–7 22VP10G–7	22V10G–10 22VP10G–10
I_{CC} (mA)	Commercial	190	190	190	190
	Military			190	190
t_{PD} (ns)	Commercial	5/5.5	6.0	7.5	10
	Military			7.5	10
t_S (ns)	Commercial	2.5	3.0	3.0	3.6
	Military			3.0	3.6
t_{CO} (ns)	Commercial	4/4.5	5.5	6.0	7.5
	Military			6.0	7.5/9.5
f_{MAX} (MHz)	Commercial	153/142	117	111	90
	Military			111	90/76

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC}

DC Input Voltage ..... – 0.5V to V_{CC}

DC Input Current ..... – 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	– 55°C to +125°C	5V ± 10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	Com'l	2.4		V
			I_{OH} = – 2 mA	Mil	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			– 250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			– 100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			– 30	– 120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

Notes:

2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics[5]

Parameter	Description	22V10G–5 22VP10G–5		22V10G–6 22VP10G–6		22V10G–7 22VP10G–7		22V10G–10[6] 22VP10G–10[6]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]	1	5 (PLCC) 5.5 (PDIP)	1	6	2	7.5	2	10	ns
t_{EA}	Input to Output Enable Delay	1	6	1	6	2	7.5	2	10	ns
t_{ER}	Input to Output Disable Delay[8]	1	5	1	6	2	7.5	2	10	ns
t_{CO}	Clock to Output Delay[7]	1	4 (PLCC) 4.5 (PDIP)	1	5.5	1	6.0	1	7.5/9.5	ns
t_S	Input or Feedback Set-Up Time	2.5		3		3		3.6		ns
t_H	Input Hold Time	0		0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	6.5 (PLCC) 7 (PDIP)		8.5		9		11.1/13.1		ns
t_{WH}	Clock Width HIGH[9]	3		3		3		3		ns
t_{WL}	Clock Width LOW[9]	3		3		3		3		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	153.8 (PLCC) 142.8 (PDIP)		117		111		90/76		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[9, 11]	166		166		166		166		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	181.8 (PLCC) 166 (PDIP)		142		133		100/90		MHz
t_{CF}	Register Clock to Feedback Input[13]		3 (PLCC) 3.5 (PDIP)		4		4.5		6.4/7.5	ns
t_{AW}	Asynchronous Reset Width	6		7.5		8.5		10		ns
t_{AR}	Asynchronous Reset Recovery Time	4		4		5		6		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	7	2	11	2	12	2	12	ns
t_{SPR}	Synchronous Preset Recovery Time	4		4		5		6		ns
t_{PR}	Power-Up Reset Time[14]	1		1		1		1		µs

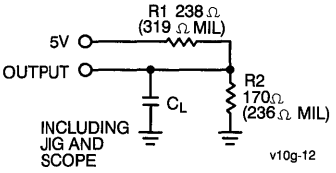
Capacitance[9]

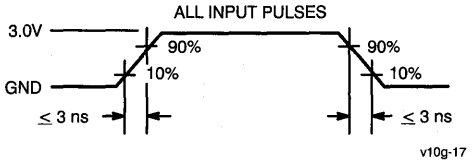
Parameter	Description	Typ.	Unit
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	8	pF

Notes:

5. AC test load used for all parameters except where noted.
6. If an entry in this column consists of two numbers, the second number is for the military version in CDIP packages.
7. This specification is guaranteed for all device outputs changing state in a given access cycle.
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
9. Tested initially and after any design or process changes that may affect these parameters.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
14. The registers in the PAL22V10G and PAL22VP10G have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

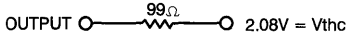
AC Test Loads and Waveforms





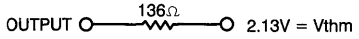
C_L[15] = 50 pF

Equivalent to: THEVENIN EQUIVALENT

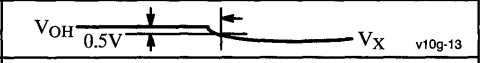
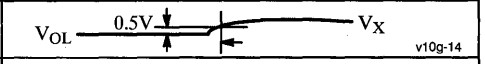
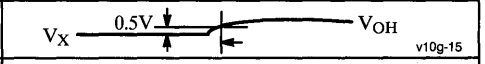
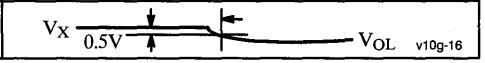


Commercial

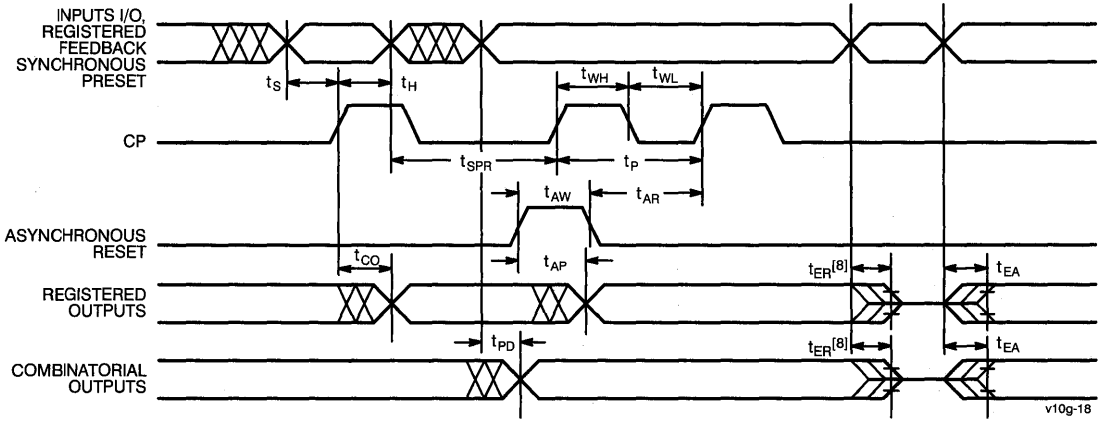
Equivalent to: THEVENIN EQUIVALENT



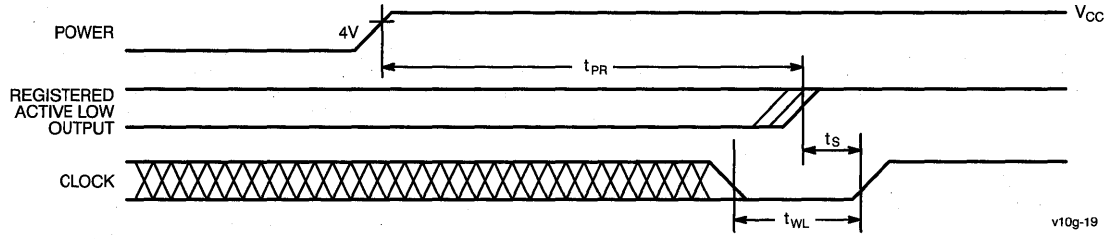
Military

Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	
t_{ER} (+)	2.6V	
t_{EA} (+)	1.5V	
t_{EA} (−)	1.5V	

Switching Waveform

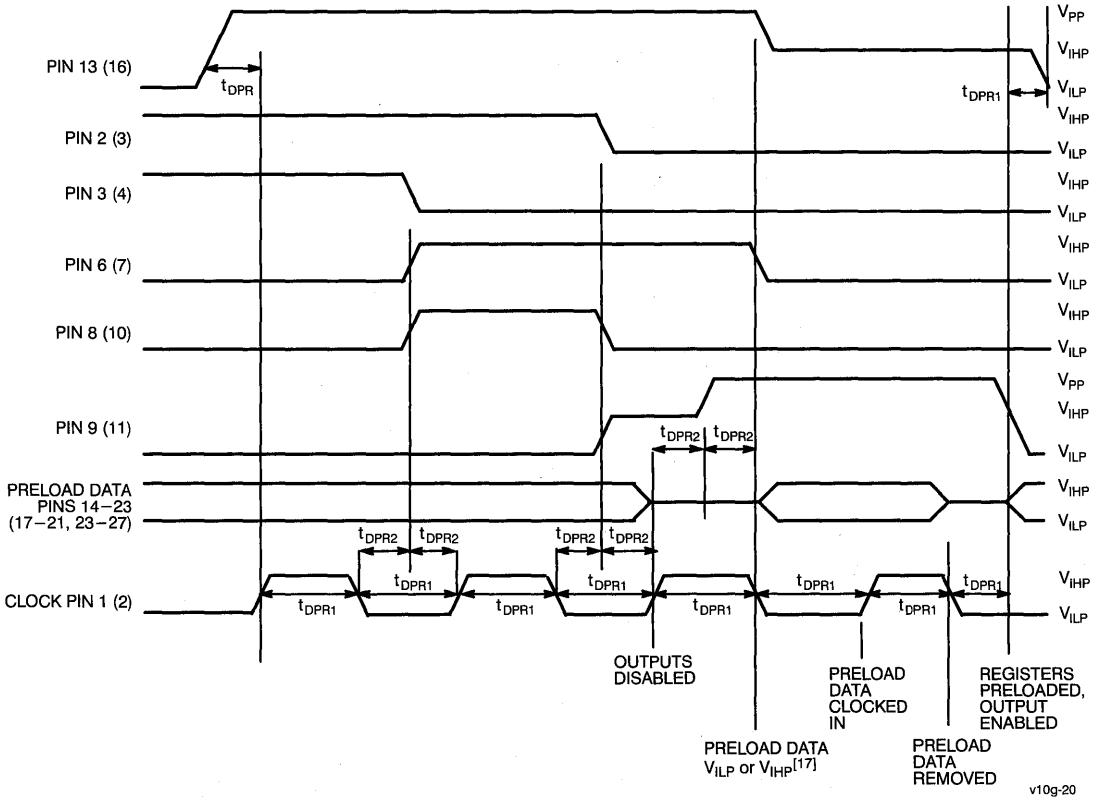


Power-Up Reset Waveform[14]



Notes:
15. C_L = 5 pF for t_{ER} measurement for all packages.

Preload Waveform[16]



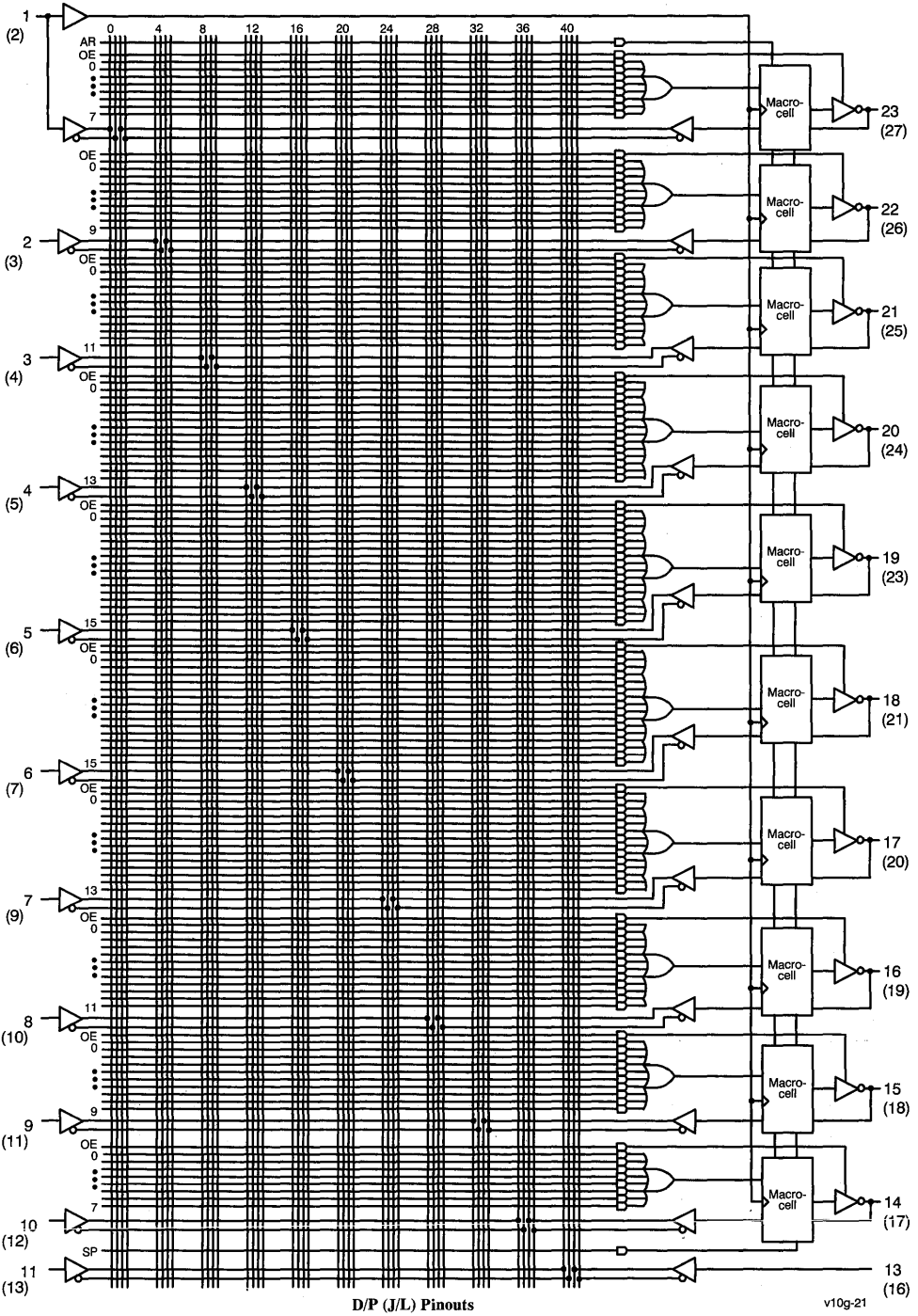
Notes:
16. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
17. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/P (J/L) Pinouts

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10G/PAL22VP10G



D/P (J/L) Pinouts

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	5	153.8	PAL22V10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5.5	142.8	PAL22V10G–5PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	6	117	PAL22V10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22V10G–6PC	P13	24-Lead (300-Mil) Molded DIP	
	7.5	111	PAL22V10G–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22V10G–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
		76	PAL22V10G–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
		90	PAL22V10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Package Type	Operating Range
190	5	153.8	PAL22VP10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5.5	142.8	PAL22VP10G–5PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	6	117	PAL22VP10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22VP10G–6PC	P13	24-Lead (300-Mil) Molded DIP	
	7.5	111	PAL22VP10G–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22VP10G–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
		76	PAL22VP10G–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
		90	PAL22VP10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00044

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the CY7C335.

CY7C330

CYPRESS SEMICONDUCTOR

CMOS Programmable Synchronous State Machine

Features

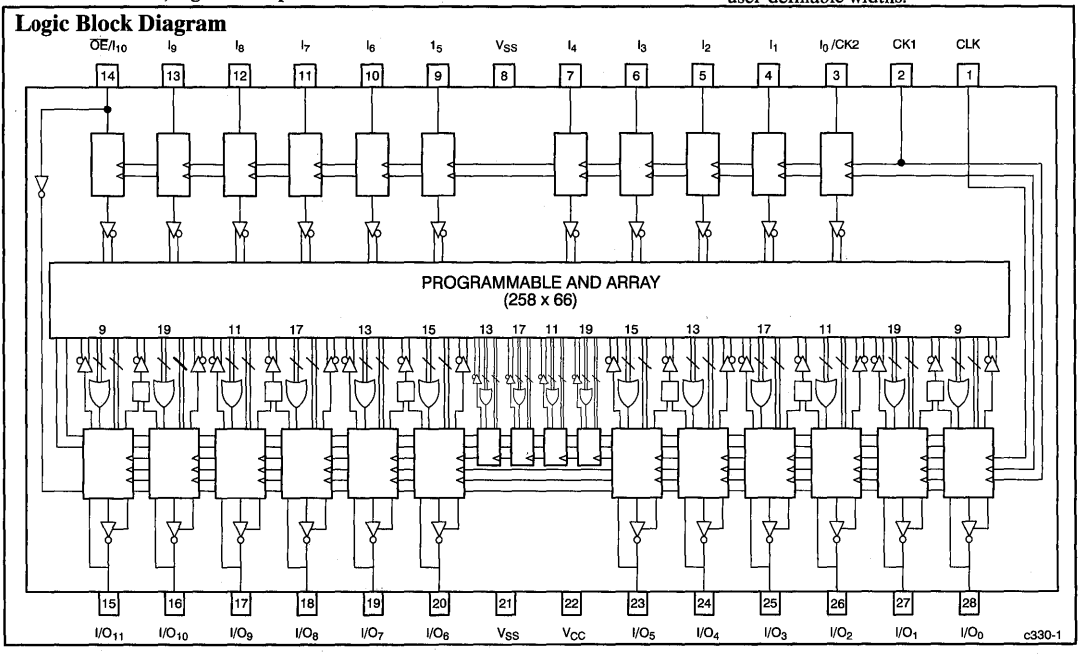
- Twelve I/O macrocells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macrocell state registers can be hidden
- User-configurable state registers—JK, RS, T, or D
- One input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input
- Four dedicated hidden registers
- Eleven dedicated, registered inputs
- Three separate clocks—two inputs, one output
- Common (pin 14–controlled) or product term–controlled output enable for each I/O pin
- 256 product terms—32 per pair of macrocells, variable distribution
- Global, synchronous, product term–controlled, state register set and reset—inputs to product term are clocked by input clock
- 66-MHz operation
  - 3-ns input set-up and 12-ns clock to output
  - 15-ns input register clock to state register clock
- Low power
  - 130 mA I_{CC}
- 28-pin, 300-mil DIP, LCC
- Erasable and reprogrammable

Functional Description

The CY7C330 is a high-performance, erasable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

Logic Block Diagram



Selection Guide

		7C330–66	7C330–50	7C330–40	7C330–33	7C330–28
Maximum Operating Frequency, f_{MAX} (MHz)	Commercial	66.6	50.0		33.3	
	Military		50.0	40.0		28.5
Power Supply Current I_{CC1} (mA)	Commercial	140	130		130	
	Military		160	150		150

Document #: 38–00064–E

CY7C331

Asynchronous Registered EPLD

Features

- **Twelve I/O macrocells each having:**
  - **— One state flip-flop with an XOR sum-of-products input**
  - **— One feedback flip-flop with input coming from the I/O pin**
  - **— Independent (product term) set, reset, and clock inputs on all registers**
  - **— Asynchronous bypass capability on all registers under product term control (r = s = 1)**
  - **— Global or local output enable on three-state I/O**
  - **— Feedback from either register to the array**
- **192 product terms with variable distribution to macrocells**
- **13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs**
- **High speed: 20 ns maximum t_{PD}**
- **Security bit**
- **Space-saving 28-pin slim-line DIP package; also available in 28-pin PLCC**
- **Low power**
  - **— 90 mA typical I_{CC} quiescent**
  - **— 180 mA I_{CC} maximum**
  - **— UV-erasable and reprogrammable**
  - **— Programming and operation 100% testable**

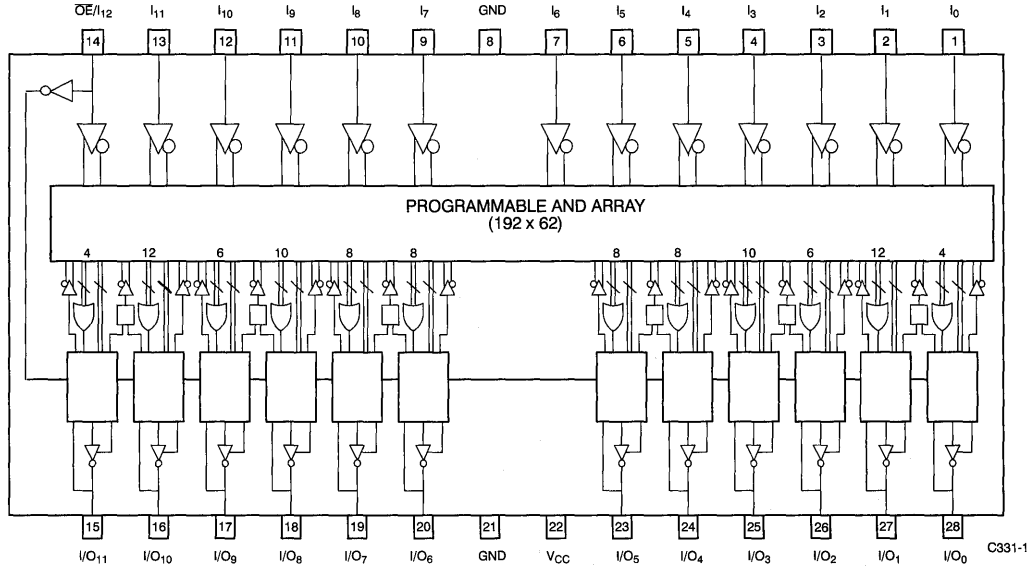
Functional Description

The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include twelve full D-type flip-flops with separate set, reset, and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per flip-flop is variably distributed.

I/O Resources

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell three-state outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

Logic Block Diagram

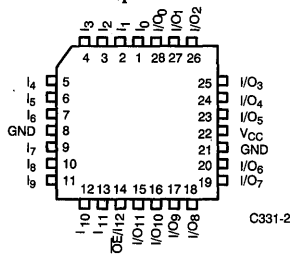


Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
CY7C331–20	130		20		12		20	
CY7C331–25	120	160	25	25	12	15	25	25
CY7C331–30		150		30		15		30
CY7C331–40		150		40		20		40

Pin Configuration

PLCC
Top View



I/O Resources (continued)

It should be noted that there are two ground connections (pins 8 and 21) which, together with V_{CC} (pin 22) are located centrally on the package. The reason for this placement and dual-ground structure is to minimize the ground-loop noise when the outputs are driving simultaneously into a heavy capacitive load.

The CY7C331 has twelve I/O macrocells (see *Figure 1*). Each macrocell has two D-type flip-flops. One is fed from the array, and one from the I/O pin. For each flip-flop there are three dedicated product terms driving the R, S, and clock inputs, respectively. Each macrocell has one input to the array and for each pair of macrocells there is one shared input to the array. The macrocell input to the array may be configured to come from the 'Q' output of either flip-flop.

The D-type flip-flop that is fed from the array (i.e., the state flip-flop) has a logical XOR function on its input that combines a single product term with a sum(OR) of a number of product terms. The single product term is used to set the polarity of the output or to implement toggling (by including the current output in the product term).

The R and S inputs to the flip-flops override the current setting of the 'Q' output. The S input sets 'Q' true and the R input resets 'Q' (sets it false). If both R and S are asserted (true) at once, then the output will follow the input ('Q' = 'D') (see *Table 1*).

Table 1. RS Truth Table

R	S	Q
1	0	0
0	1	1
1	1	D

Shared Input Multiplexer

The input associated with each pair of macrocells may be configured by the shared input multiplexer to come from either macrocell; the 'Q' output of the flip-flop coming from the I/O pin is used as the input signal source (see *Figure 2*).

Product Term Distribution

The product terms are distributed to the macrocells such that 32 product terms are distributed between two adjacent macrocells.

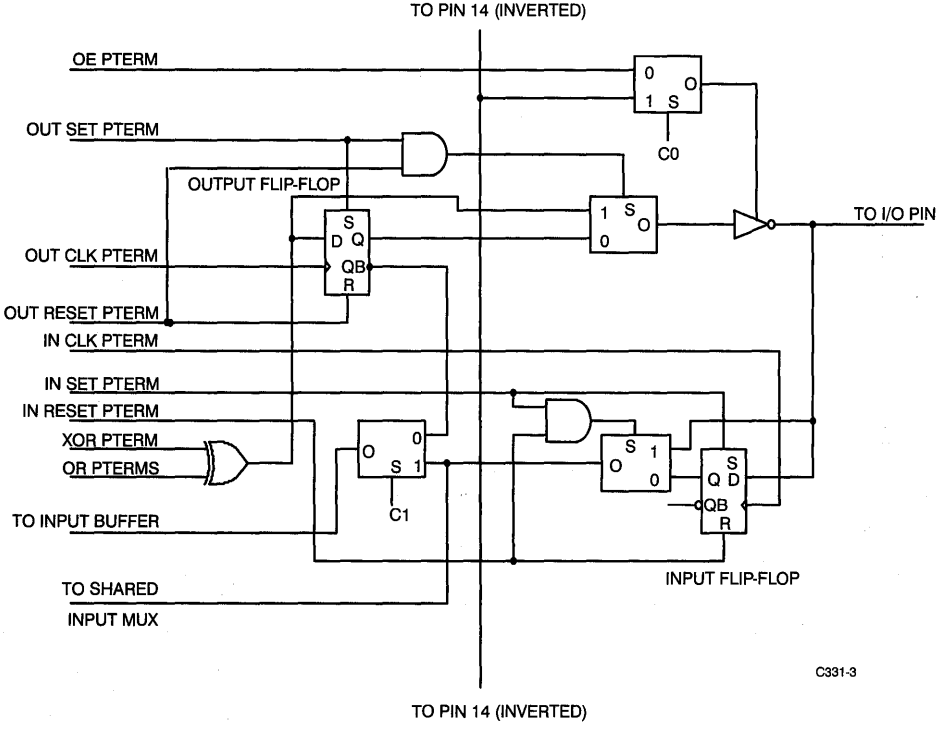


Figure 1. I/O Macrocell

Product Term Distribution (continued)

The pairing of macrocells is the same as it is for the shared inputs. Eight of the product terms are used in each macrocell for set, reset, clock, output enable, and the upper part of the XOR gate. This leaves 16 product terms per pair of macrocells to be divided between the sum-of-products inputs to the two state registers. The following table shows the I/O pin pairing for shared inputs, and the product term (PT) allocation to macrocells associated with the I/O pins (see *Table 2*).

The CY7C331 is configured by three arrays of configuration bits (C0, C1, C2). For each macrocell, there is one C0 bit and one C1 bit. For each pair of macrocells there is one C2 bit.

Table 2. Product Term Distribution

Macrocell	Pin Number	Product Terms
0	28	4
1	27	12
2	26	6
3	25	10
4	24	8
5	23	8
6	20	8
7	19	8
8	18	10
9	17	6
10	16	12
11	15	4

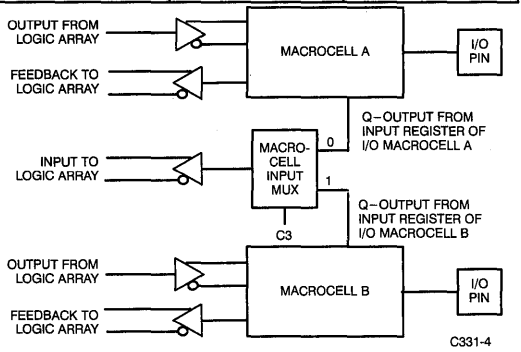


Figure 2. Shared Input Multiplexer

There are twelve C0 bits, one for each macrocell. If C0 is programmed for a macrocell, then the three-state enable (OE) will be controlled by pin 14 (the global OE). If C0 is not programmed, then the OE product term for that macrocell will be used.

Thereare twelve C1 bits, one for each macrocell. The C1 bit selects inputs for the product term (PT) array from either the state register (if the bit is unprogrammed) or the input register (if the bit is programmed).

There are six C2 bits, providing one C2 bit for each pair of macrocells. The C2 bit controls the shared input multiplexer; if the C2 bit is not programmed, then the input to the product term array comes from the upper macrocell (A). If the C2 bit is programmed, then the input comes from the lower macrocell (B).

The timing diagrams for the CY7C331 cover state register, input register, and various combinational delays. Since internal clocks are the outputs of product terms, all timing is from the transition of the inputs causing the clock transition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 8 or 21) ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage ..... 13.0 V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OH} = − 3.2 mA (Com'l), I_{OH} = − 2 mA (Mil)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OL} = 12 mA (Com'l), I_{OL} = 8 mA (Mil)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input, all Inputs[3]		2.2		V
V_{IL}	Input LOW Voltage	Guaranteed LOW Input, all Inputs[3]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	+10	μA
I_{OZ}	Output Leakage Current	V_{SS} < V_{OUT} < V_{CC}, V_{CC} = Max.		−40	+40	μA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0.5V[5]		−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open	Com'l −20		130	mA
			Com'l −25, −35		120	
			Mil −25		160	mA
			Mil −30, −40		150	
I_{CC2}	Power Supply Current at Frequency[4, 6]	V_{CC} = Max., Outputs Disabled (in High Z State) Device Operating at f_{MAX} External (f_{MAX1})	Com'l		180	mA
			Mil		200	

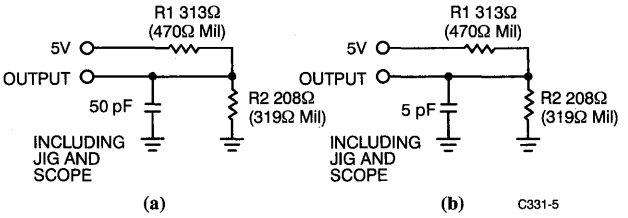
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	10	pF

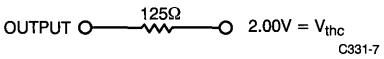
Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Because these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.

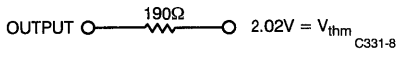
AC Test Loads and Waveforms

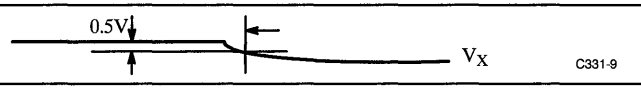
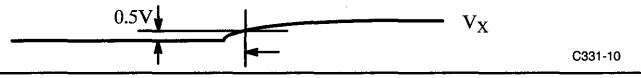
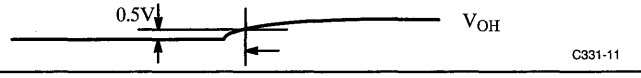
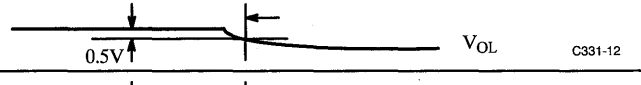
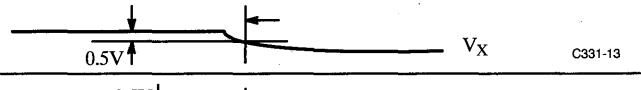
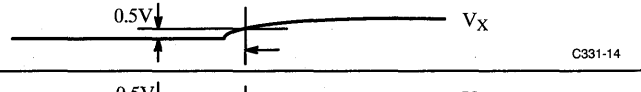
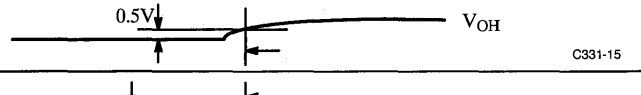
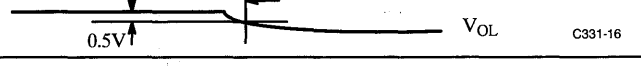


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	 C331-9
$t_{PXZ(+)}$	2.6V	 C331-10
$t_{PZX(+)}$	V_{thc}	 C331-11
$t_{PZX(-)}$	V_{thc}	 C331-12
$t_{ER(-)}$	1.5V	 C331-13
$t_{ER(+)}$	2.6V	 C331-14
$t_{EA(+)}$	V_{thc}	 C331-15
$t_{EA(-)}$	V_{thc}	 C331-16

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range[2]

Parameter	Description	Commercial				Unit
		−20		−25		
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		20		25	ns
t_{ICO}	Input Register Clock to Output Delay[8]		35		40	ns
t_{IOH}	Output Data Stable Time from Input Clock[8]	5		5		ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[8]	2		2		ns
t_{IH}	Input Register Hold Time from Input Clock[8]	11		13		ns

Switching Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Commercial				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
t_{IAR}	Input to Input Register Asynchronous Reset Delay[8]		35		40	ns
t_{IRW}	Input Register Reset Width[4, 8]	35		40		ns
t_{IRR}	Input Register Reset Recovery Time[4, 8]	35		40		ns
t_{IAS}	Input to Input Register Asynchronous Set Delay[8]		35		40	ns
t_{ISW}	Input Register Set Width[4, 8]	35		40		ns
t_{ISR}	Input Register Set Recovery Time[4, 8]	35		40		ns
t_{WH}	Input and Output Clock Width HIGH[8, 9, 10]	12		15		ns
t_{WL}	Input and Output Clock Width LOW[8, 9, 10]	12		15		ns
f_{MAX1}	Maximum Frequency with Feedback in Input Registered Mode ($1/(t_{ICO} + t_{IS})$)[11]	27.0		23.8		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_{IS} + t_{IH})$)[8]	28.5		25.0		MHz
$t_{IOH}-t_{IH}33X$	Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332[12, 13]	0		0		ns
t_{CO}	Output Register Clock to Output Delay[9]		20		25	ns
t_{OH}	Output Data Stable Time from Output Clock[9]	3		3		ns
t_S	Output Register Input Set-Up Time to Output Clock[9]	12		12		ns
t_H	Output Register Input Hold Time from Output Clock[9]	8		8		ns
t_{OAR}	Input to Output Register Asynchronous Reset Delay[9]		20		25	ns
t_{ORW}	Output Register Reset Width[9]	20		25		ns
t_{ORR}	Output Register Reset Recovery Time[9]	20		25		ns
t_{OAS}	Input to Output Register Asynchronous Set Delay[9]		20		25	ns
t_{OSW}	Output Register Set Width[9]	20		25		ns
t_{OSR}	Output Register Set Recovery Time[9]	20		25		ns
t_{EA}	Input to Output Enable Delay[14, 15]		25		25	ns
t_{ER}	Input to Output Disable Delay[14, 15]		25		25	ns
t_{PZX}	Pin 14 to Output Enable Delay[14, 15]		20		20	ns
t_{PXZ}	Pin 14 to Output Disable Delay[14, 15]		20		20	ns
f_{MAX3}	Maximum Frequency with Feedback in Output Registered Mode ($1/(t_{CO} + t_S)$)[16, 17]	31.2		27.0		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_S + t_H)$)[9]	41.6		33.3		MHz
$t_{OH}-t_{IH}33X$	Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332[13, 18]	0		0		ns
f_{MAX5}	Maximum Frequency Pipelined Mode[10, 17]	35.0		30.0		MHz

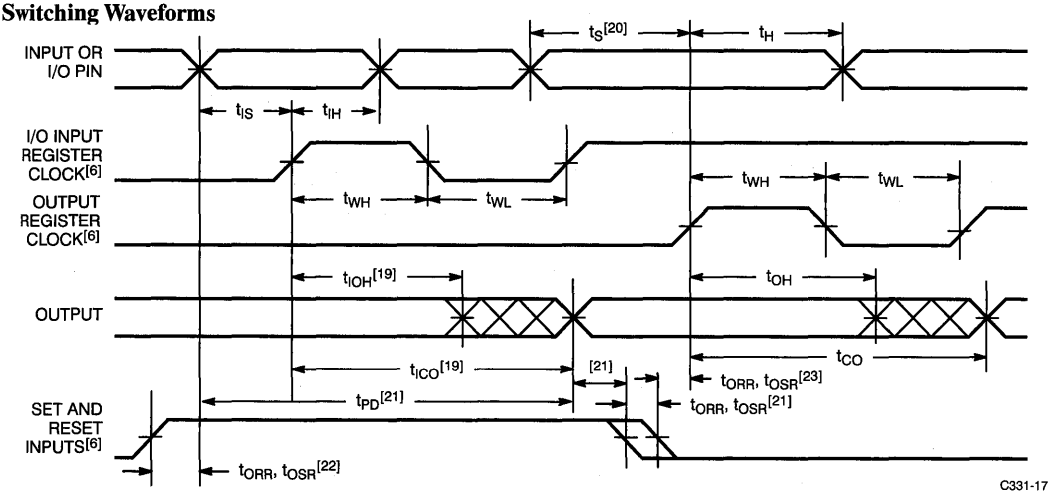
Notes:

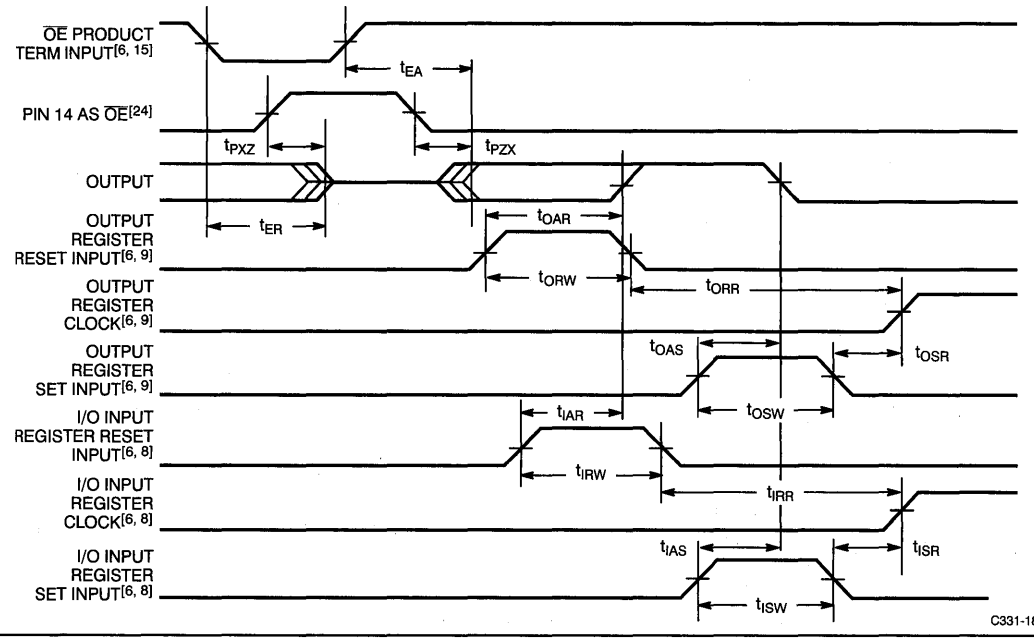
7. Refer to *Figure 3*, configuration 1.
8. Refer to *Figure 3*, configuration 2.
9. Refer to *Figure 3*, configuration 3.
10. Refer to *Figure 3*, configuration 6.
11. Refer to *Figure 3*, configuration 7.
12. Refer to *Figure 3*, configuration 9.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C331. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
14. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{PZXI}, t_{PXZI}, t_{PZX}, and t_{PXZ}, which use part (b). Part (c) shows the test waveforms and measurement levels.
15. Refer to *Figure 3*, configuration 4.
16. Refer to *Figure 3*, configuration 8.
17. This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
18. Refer to *Figure 3*, configuration 10.

Switching Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Military						Unit
		−25		−30		−40		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		25		30		40	ns
t_{ICO}	Input Register Clock to Output Delay[4, 8]		45		50		65	ns
t_{IOH}	Output Data Stable Time from Input Clock[4, 8]	5		5		5		ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[8]	5		5		5		ns
t_{IH}	Input Register Hold Time from Input Clock[4, 8]	13		15		20		ns
t_{IAR}	Input to Input Register Asynchronous Reset Delay[4, 8]		45		50		65	ns
t_{IRW}	Input Register Reset Width[8]	45		50		65		ns
t_{IRR}	Input Register Reset Recovery Time[8]	45		50		65		ns
t_{IAS}	Input to Input Register Asynchronous Set Delay[8]		45		50		65	ns
t_{ISW}	Input Register Set Width[8]	45		50		65		ns
t_{ISR}	Input Register Set Recovery Time[8]	45		50		65		ns
t_{WH}	Input and Output Clock Width High[8, 9, 10]	15		20		25		ns
t_{WL}	Input and Output Clock Width Low[8, 9, 10]	15		20		25		ns
f_{MAX1}	Maximum frequency with Feedback in Input Registered Mode $(1/(t_{ICO} + t_{IS}))$[11]	20.0		18.1		14.2		MHz
f_{MAX2}	Maximum frequency Data Path in Input Registered Mode (Lowest of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_{IS} + t_{IH})$[8]	22.2		20.0		15.3		MHz
$t_{IOH}-t_{IH}33X$	Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332[12, 13]	0		0		0		ns
t_{CO}	Output Register Clock to Output Delay[9]		25		30		40	ns
t_{OH}	Output Data Stable Time from Output Clock[9]	3		3		3		ns
t_S	Output Register Input Set−Up Time to Output Clock[9]	15		15		20		ns
t_H	Output Register Input Hold Time from Output Clock[9]	10		10		12		ns
t_{OAR}	Input to Output Register Asynchronous Reset Delay[9]		25		30		40	ns
t_{ORW}	Output Register Reset Width[9]	25		30		40		ns
t_{ORR}	Output Register Reset Recovery Time[9]	25		30		40		ns
t_{OAS}	Input to Output Register Asynchronous Set Delay[9]		25		30		40	ns
t_{OSW}	Output Register Set Width[9]	25		30		40		ns
t_{OSR}	Output Register Set Recovery Time[9]	25		30		40		ns
t_{EA}	Input to Output Enable Delay[14, 15]		25		30		40	ns
t_{ER}	Input to Output Disable Delay[14, 15]		25		30		40	ns
t_{PZX}	Pin 14 to Output Enable Delay[14, 15]		20		25		35	ns
t_{PXZ}	Pin 14 to Output Disable Delay[14, 15]		20		25		35	ns
f_{MAX3}	Maximum Frequency with Feedback in Output Registered Mode)$1/(t_{CO} + t_S)$[16, 17]	25.0		22.2		16.6		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_S + t_H)$[9]	33.3		25.0		20.0		MHz
$t_{OH}-t_{IH}33X$	Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332[13, 18]	0		0		0		ns
f_{MAX5}	Maximum Frequency Pipelined Mode[10, 17]	28.0		23.5		18.5		MHz

Switching Waveforms





Notes:

19. Output register is set in Transparent mode. Output register set and reset inputs are in a HIGH state.
20. Dedicated input or input register set in Transparent mode. Input register set and reset inputs are in a HIGH state.
21. Combinatorial Mode. Reset and set inputs of the input and output registers should remain in a HIGH state at least until the output responds at t_{PD}. When returning set and reset inputs to a LOW state, one of these signals should go LOW a minimum of t_{OSR} (set input) or t_{ORR} (reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial mode.
22. When entering the Combinatorial mode, input and output register set and reset inputs must be stable in a HIGH state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to application of logic input signals.
23. When returning to the input and/or output Registered mode, register set and reset inputs must be stable in a LOW state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to the application of the register clock input.
24. Refer to *Figure 3*, configuration 5.

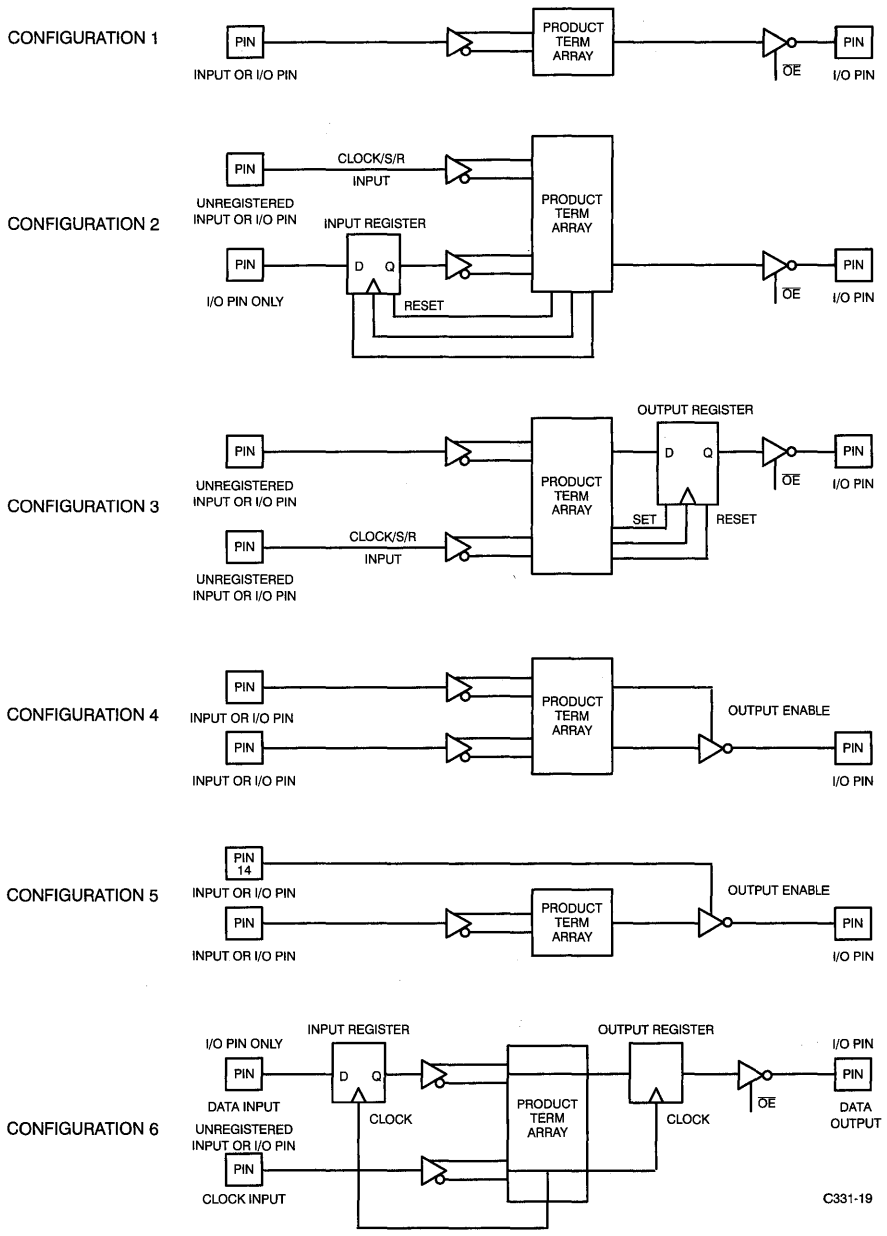
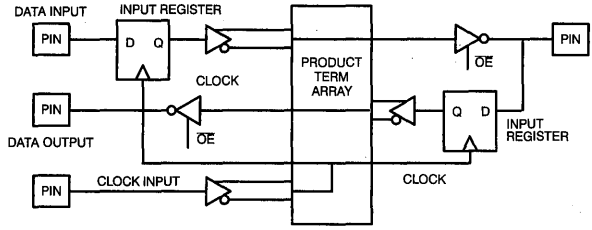
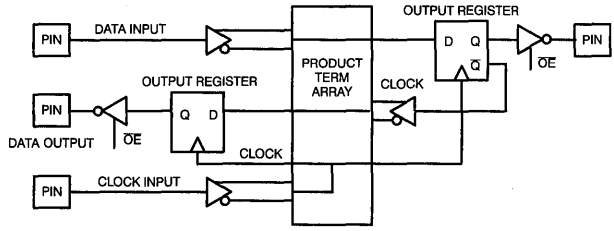


Figure 3. Timing Configurations

CONFIGURATION 7



CONFIGURATION 8



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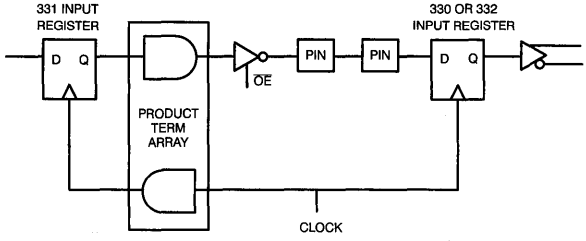
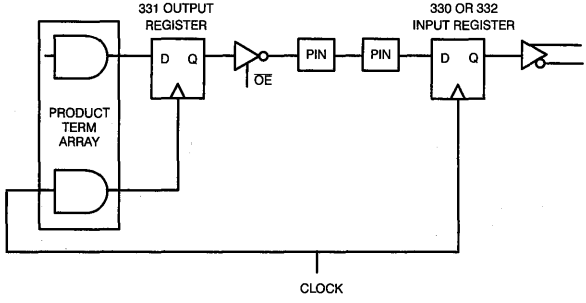
CONFIGURATION 9



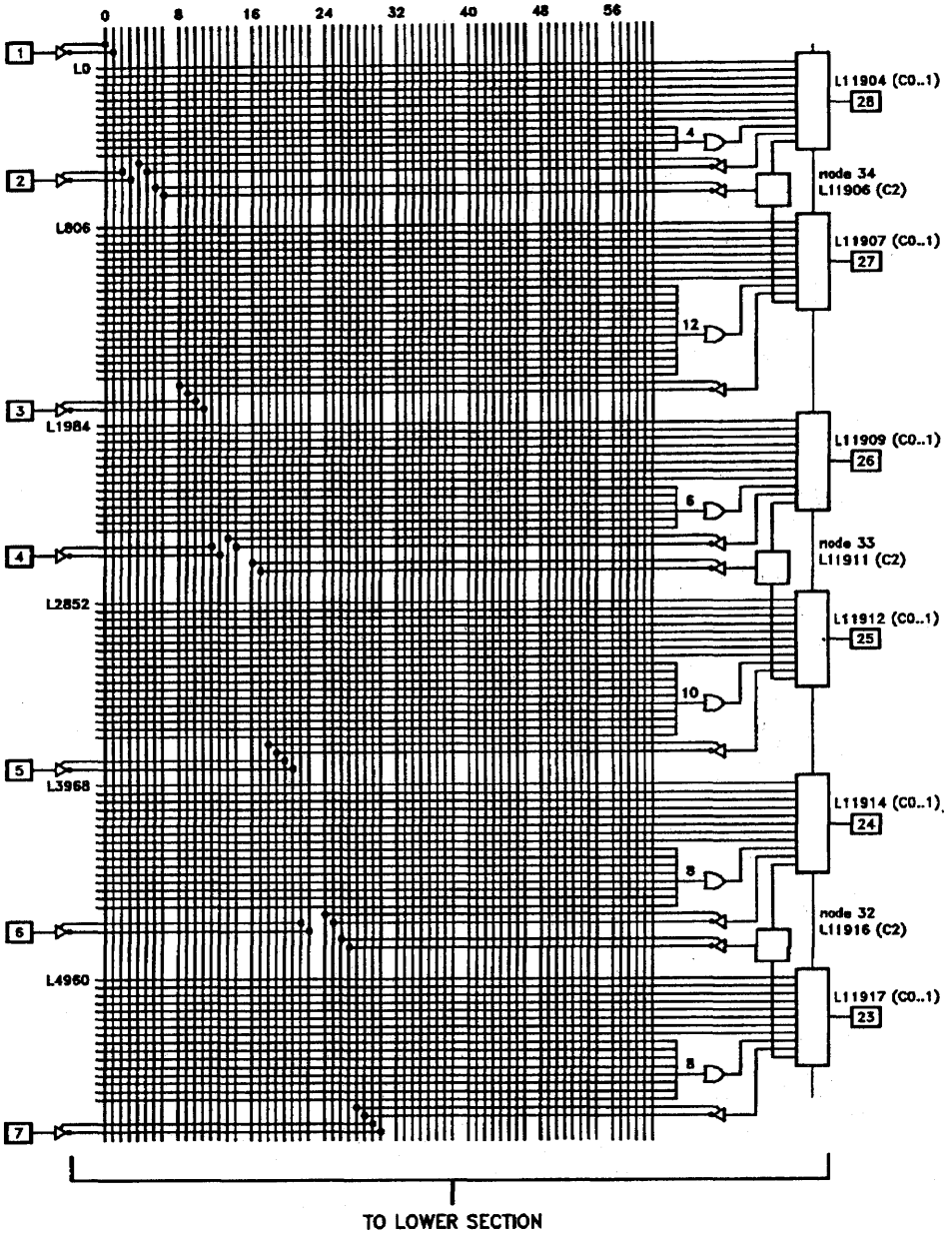
CONFIGURATION 10



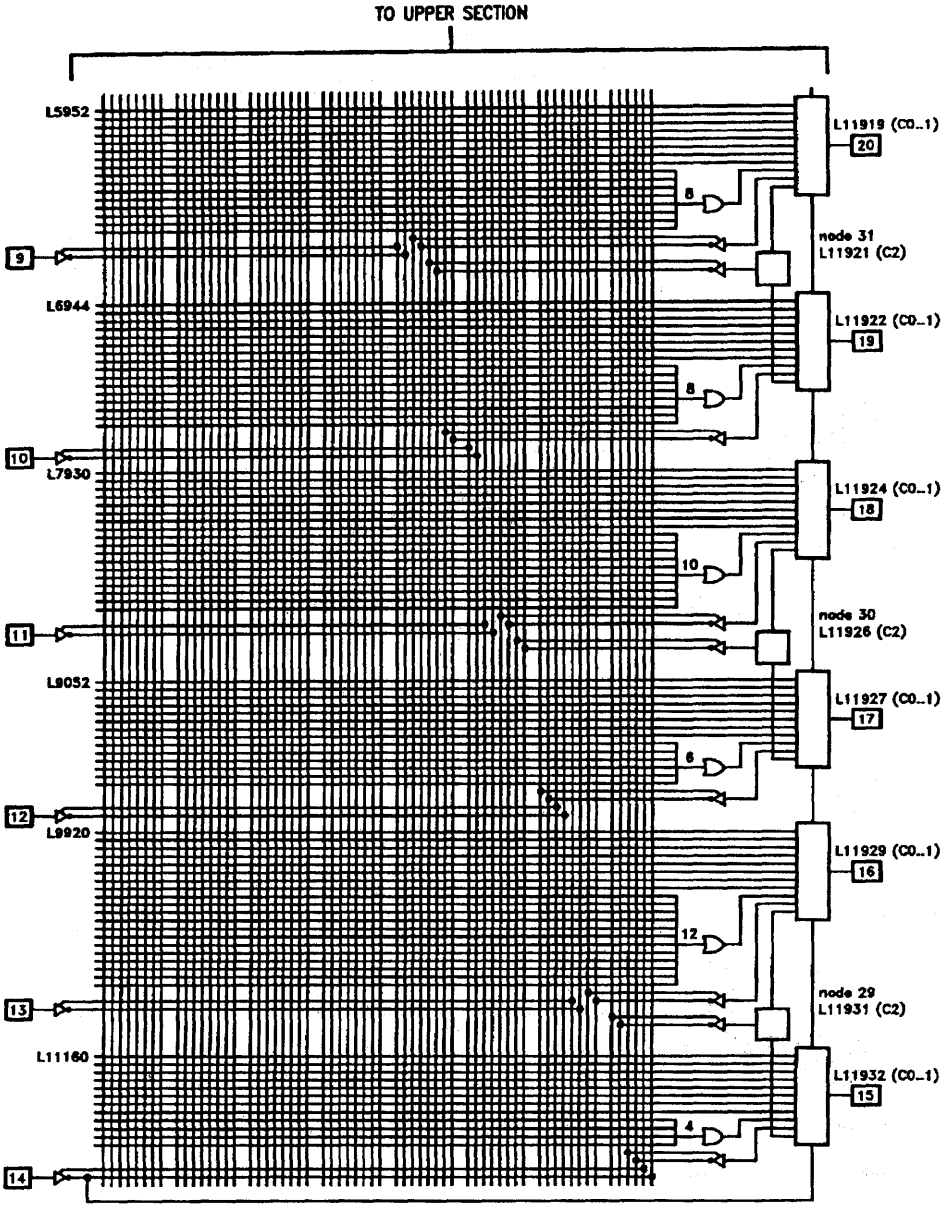
C331-21

Figure 3. Timing Configurations (continued)

CY7C331 Logic Diagram (Upper Half)



CY7C331 Logic Diagram (Lower Half)



Ordering Information

I_{CC1} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
130	20	12	20	CY7C331–20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C331–20JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C331–20PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C331–20WC	W22	28-Lead (300-Mil) Windowed CerDIP	
160	25	15	25	CY7C331–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–25HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–25LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–25TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
120	25	12	25	CY7C331–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C331–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C331–25PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C331–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
150	30	15	30	CY7C331–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–30HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–30LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–30TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–30WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
150	40	20	40	CY7C331–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–40LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–40TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{WH}	9, 10, 11
t_{WL}	9, 10, 11
t_{CO}	9, 10, 11
t_{PD}	9, 10, 11
t_{IAR}	9, 10, 11
t_{IAS}	9, 10, 11
t_{PXZ}	9, 10, 11
t_{PZX}	9, 10, 11
t_{ER}	9, 10, 11
t_{EA}	9, 10, 11
t_{S}	9, 10, 11
t_{H}	9, 10, 11

Document #: 38–00066–C

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the CY7C335.

CY7C332

CYPRESS SEMICONDUCTOR

Registered Combinatorial EPLD

Features

- **12 I/O macrocells each having:**
  - **— Registered, latched, or transparent array input**
  - **— A choice of two clock sources**
  - **— Global or local output enable (OE)**
  - **— Up to 19 product terms (PTs) per output**
  - **— Product term (PT) output polarity control**
- **192 product terms with variable distribution to macrocells**
  - **— An average of 14 PTs per macrocell sum node**
- **Two clock inputs with configurable polarity control**
- **13 input macrocells, each having:**
  - **— Complementary input**
  - **— Register, latch, or transparent access**
  - **— Two clock sources**
- **15 ns t_{PD} max.**
- **Low power**
  - **— 120 mA typical I_{CC} quiescent**
  - **— 180 mA max.**
  - **— Power-saving "Miser Bit" feature**
- **Security fuse**
- **28-pin slim-line package; also available in 28-pin PLCC**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Functional Description

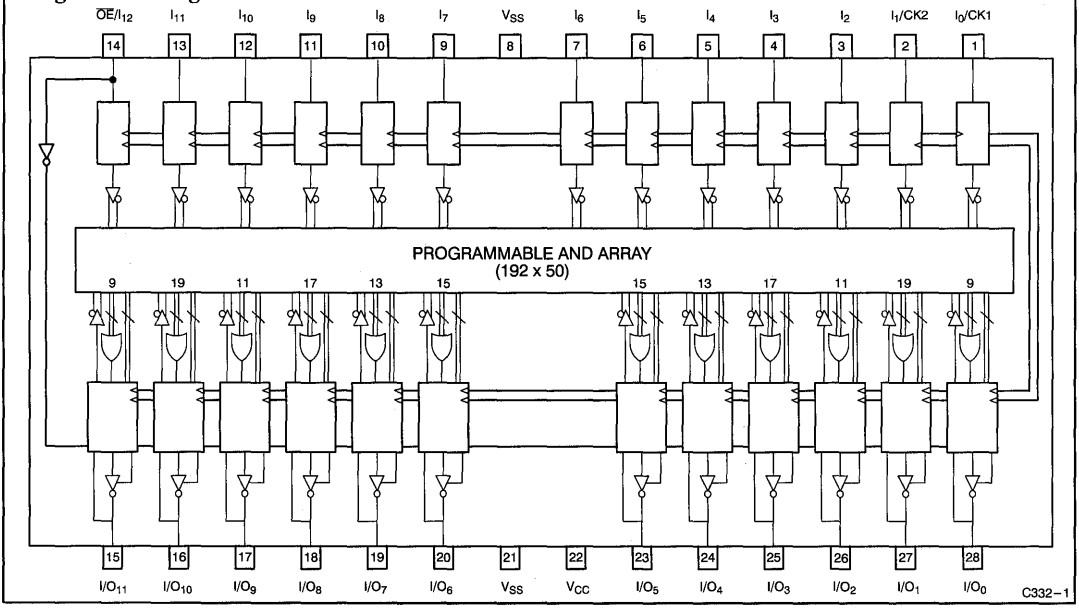
The CY7C332 is a versatile combinatorial PLD with I/O registers on-board. There are 25 array inputs; each has a macrocell that may be configured as a register, latch, or simple buffer. Outputs have polarity and three-state control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

I/O Resources

Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.

4 PLDs

Logic Block Diagram



Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{ICO}/t_{PD} (ns)		t_{IS} (ns)	
	Commercial	Military	Commercial	Military	Commercial	Military
7C332–15	130		18/15		3	
7C332–20	120	160	20	23/20	3	4
7C332–25	120	150	25	25	3	4
7C332–30		150		30		4

Document #: 38–00067–E

CYPRESS SEMICONDUCTOR

CY7C335

Universal Synchronous EPLD

Features

- **100-MHz output registered operation**
- **Twelve I/O macrocells, each having:**
  - **— Registered, three-state I/O pins**
  - **— Input and output register clock select multiplexer**
  - **— Feed back multiplexer**
  - **— Output enable ($\overline{OE}$) multiplexer**
- **Bypass on input and output registers**
- **All twelve macrocell state registers can be hidden**
- **User configurable I/O macrocells to implement JK or RS flip-flops and T or D registers**
- **Input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input**
- **Four dedicated hidden registers**
- **Twelve dedicated registered inputs with individually programmable bypass option**
- **Three separate clocks—two input clocks, two output clocks**
- **Common (pin 14—controlled) or product term—controlled output enable for each I/O pin**
- **256 product terms—32 per pair of macrocells, variable distribution**
- **Global, synchronous, product term—controlled, state register set and reset—inputs to product term are clocked by input clock**
  - **— 2-ns input set-up and 9-ns output register clock to output**
  - **— 10-ns input register clock to state register clock**
- **28-pin, 300-mil DIP, LCC, PLCC**
- **Erasable and reprogrammable**
- **Programmable security bit**

Functional Description

The CY7C335 is a high-performance, erasable, programmable logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance state machines.

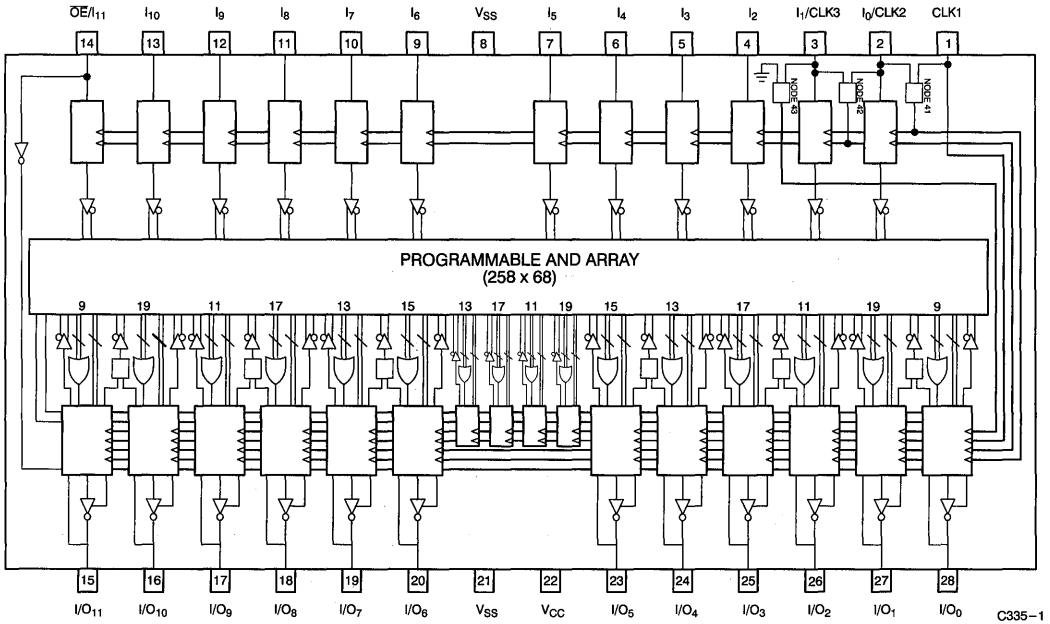
The architecture of the CY7C335, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

The four clocks permit independent, synchronous state machines to be synchronized to each other.

The user-configurable macrocells enable the designer to designate JK-, RS-, T-, or D-type devices so that the number of product terms required to implement the logic is minimized.

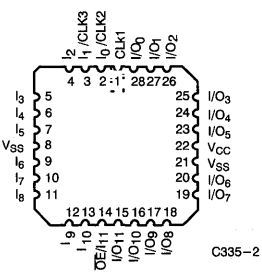
The CY7C335 is available in a wide variety of packages including 28-pin, 300-mil plastic and ceramic DIPs, PLCCs, and LCCs.

Logic Block Diagram



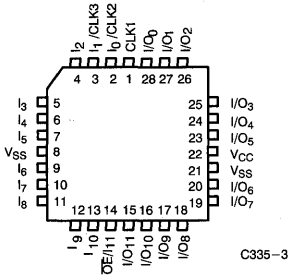
Pin Configurations

LCC
Top View



C335-2

PLCC
Top View



C335-3

Selection Guide

		CY7C335-100	CY7C335-83	CY7C335-66	CY7C335-50	CY7C335-40
Maximum Operating Frequency (MHz)	Commercial	100	83.3	66.6	50	
	Military		83.3	66.6	50	40.0
I_{CC1} (mA)	Commercial	140	140	140	140	
	Military		160	160	160	160

Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined in *Table 1.*

Table 1. Architecture Configuration Bits

Architecture Configuration Bit		Number of Bits	Value	Function
C0	Output Enable Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Output Enable Controlled by Product Term
			1—Programmed	Output Enable Controlled by Pin 14
C1	State Register Feed Back MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	State Register Output is Fed Back to Input Array
			1—Programmed	I/O Macrocell is Configured as an Input and Output of Input Path is Fed to Array
C2	I/O Macrocell Input Register Clock Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Input Register Clock Input
C3	Input Register Bypass MUX—I/O Macrocell	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Input to Feedback MUX from Input Register
			1—Programmed	Selects Input to Feedback MUX from I/O pin
C4	Output Register Bypass MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Output from the State Register
			1—Programmed	Selects Output from the Array, Bypassing the State Register
C5	State Clock MUX	16 Bits, 1 Per I/O Macrocell and 1 Per Hidden Macrocell	0—Virgin State	State Clock 1 Controls the State Register
			1—Programmed	State Clock 2 Controls the State Register
C6	Dedicated Input Register Clock Select MUX	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input

Table 1. Architecture Configuration Bits (continued)

Architecture Configuration Bit		Number of Bits	Value	Function
C7	Input Register Bypass MUX—Input Cell	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	Selects Input to Array from Input Register
			1—Programmed	Selects Input to Array from Input Pin
C8	ICLK2 Select MUX	1 Bit	0—Virgin State	Input Clock 2 Controlled by Pin 2
			1—Programmed	Input Clock 2 Controlled by Pin 3
C9	ICLK1 Select MUX	1 Bit	0—Virgin State	Input Clock 1 Controlled by Pin 2
			1—Programmed	Input Clock 1 Controlled by Pin 1
C10	SCLK2 Select MUX	1 Bit	0—Virgin State	State Clock 2 Grounded
			1—Programmed	State Clock 2 Controlled by Pin 3
CX (11–16)	I/O Macrocell Pair Input Select MUX	6 Bits, 1 Per I/O Macrocell Pair	0—Virgin State	Selects Data from I/O Macrocell Input Path of Macrocell A of Macrocell Pair
			1—Programmed	Selects Data from I/O Macrocell Input Path of Macrocell B of Macrocell Pair

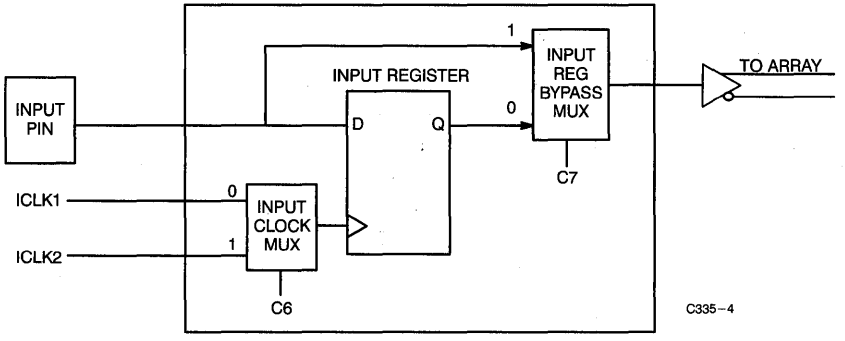


Figure 1. CY7C335 Input Macrocell

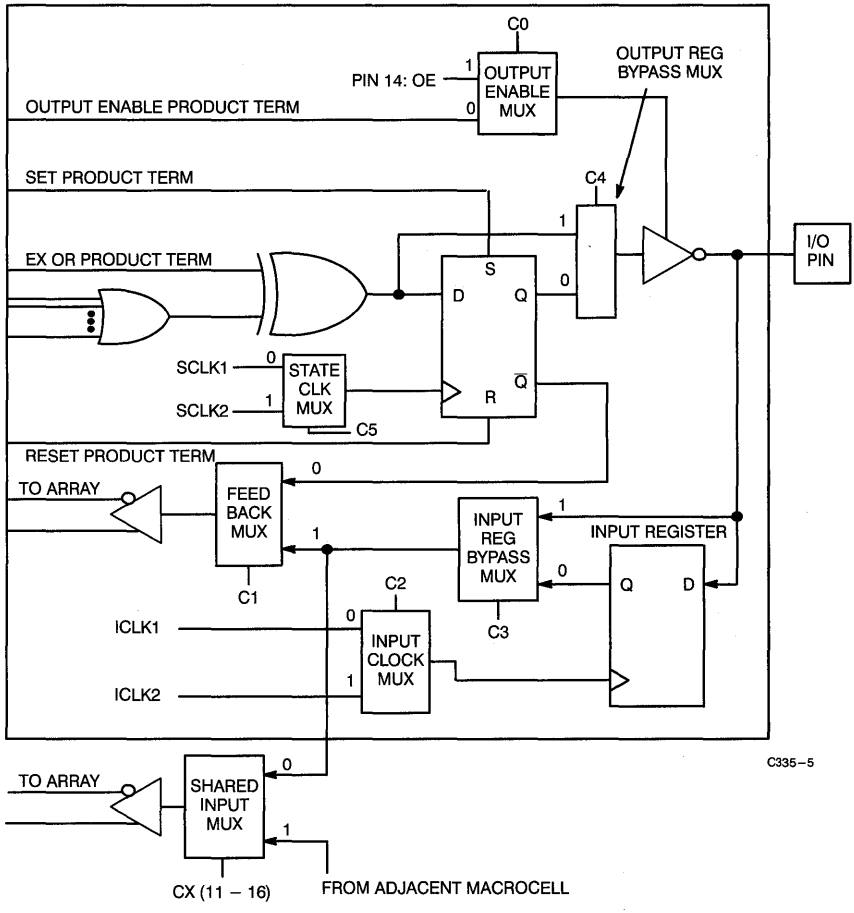


Figure 2. CY7C335 Input/Output Macrocell

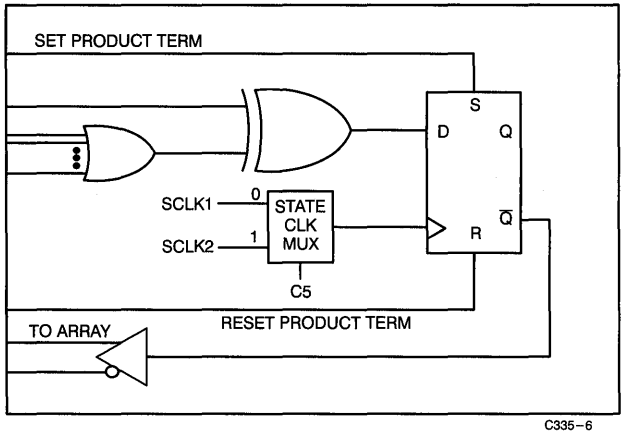


Figure 3. CY7C335 Hidden Macrocell

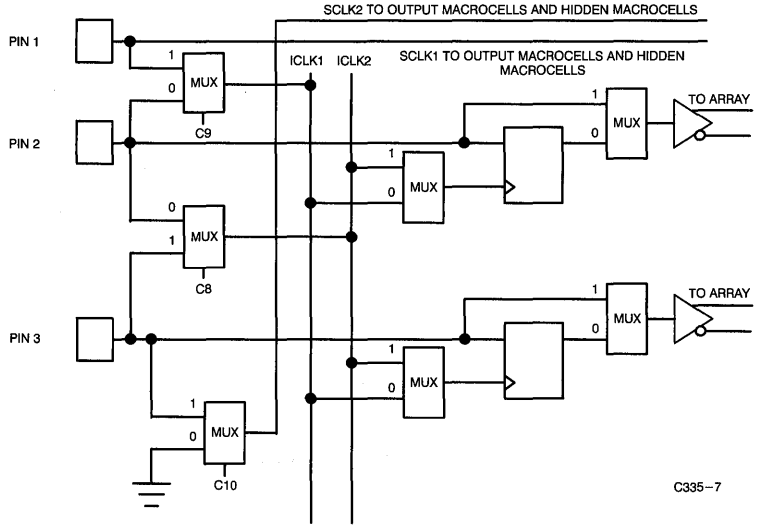


Figure 4. CY7C335 Input Clocking Scheme

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 12 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Com'l	2.4		V
			I_{OH} = − 2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Com'l		0.5	V
			I_{OL} = 8 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.2		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			− 10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			− 40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]			− 30	− 90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Com'l		140	mA
				Mil/Ind		160	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX} External (f_{MAX5})		Com'l		180	mA
				Mil/Ind		200	mA

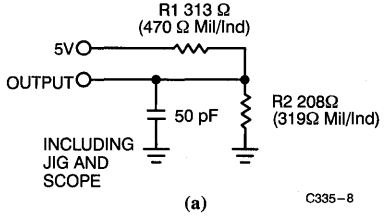
Capacitance[5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

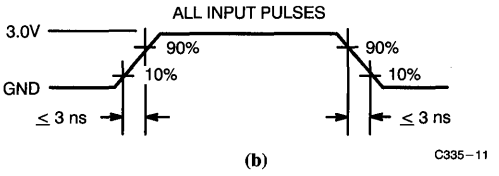
Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

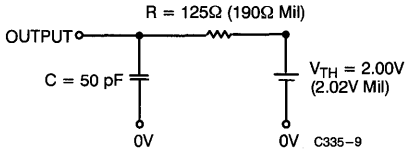
AC Test Loads and Waveforms (Commercial)



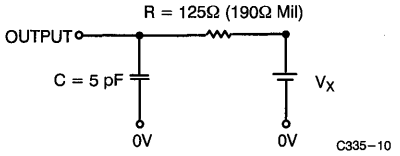
(a)



(b)



(c) Thévenin Equivalent (Load 1)



(d) Three-state Delay Load (Load 2)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	V_{OH} 0.5V V_X C335-12
t_{PXZ} (+)	2.6V	V_{OL} 0.5V V_X C335-13
t_{PZX} (+)	V_{th}	V_X 0.5V V_{OH} C335-14
t_{PZX} (−)	V_{th}	V_X 0.5V V_{OL} C335-15
t_{CER} (−)	1.5V	V_{OH} 0.5V V_X C335-16
t_{CER} (+)	2.6V	V_{OL} 0.5V V_X C335-17
t_{CEA} (+)	V_{th}	V_X 0.5V V_{OH} C335-18
t_{CEA} (−)	V_{th}	V_X 0.5V V_{OL} C335-19

Figure 5. Test Waveforms

Commercial AC Characteristics

Parameter	Description	7C335-100		7C335-83		7C335-66		7C335-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		15		15		20		25	ns
t_{EA}	Input to Output Enable		15		15		20		25	ns
t_{ER}	Input to Output Disable		15		15		20		25	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	4		5		6		8		ns
t_{WL}	Input and Output Clock Width LOW[5]	4		5		6		8		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	2		2		2		3		ns
t_{IH}	Input Register Hold Time from Input Clock	2		2		2		3		ns
t_{ICO}	Input Register Clock to Output Delay		18		18		20		25	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335 [6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		12		12		15		20	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		12		12		15		20	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO}+t_{IS})$ & $1/(t_{WL}+t_{WH})$)[5]	50		50		45.4		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH}+t_{WL})$, $1/(t_{IS}+t_{IH}))$[5]	55.5		55.5		50		40		MHz
t_{ICEA}	Input Clock to Output Enabled		17		17		20		25	ns
t_{ICER}	Input Clock to Output Disabled		15		15		20		25	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled[5]		17		17		20		25	ns
t_{CER}	Output Clock to Output Disabled[5]		15		15		20		25	ns
t_S	Output Register Input Set-Up Time from Output Clock	8		9		12		15		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		9		10		12		15	ns
t_{CO2}	Input Output Register Clock or Latcha Enable to Combinatorial Output Delay (Through Logic Array)[5]		17		18		23		30	ns
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array) [5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time [5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	100		83.3		66.6		50		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lowest of $1/(t_{CO}+t_S)$ & $1/(t_{WL}+t_{WH})$)[5]	58.8		50		41.6		33.3		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$)[5]	111		100		83.3		62.5		MHz
$t_{OH} - t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns

Commercial AC Characteristics (continued)

Parameter	Description	7C335-100		7C335-83		7C335-66		7C335-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipelined Mode Parameters										
t_{COS}	Input Clock to Output Clock	10		12		15		20		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{CO})$, $1/(t_{WL} + t_{WH})$), $1/(t_{IS} + t_{IH})$[5]	100		83.3		66.6		50		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO} + t_{IS})$ or $1/t_{COS}$)	90.9		83.3		66.6		50		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	µs

Military/Industrial AC Characteristics

Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		20		20		25		30	ns
t_{EA}	Input to Output Enable		20		20		25		30	ns
t_{ER}	Input to Output Disable		20		20		25		30	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	5		6		8		10		ns
t_{WL}	Input and Output Clock Width LOW[5]	5		6		8		10		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	3		3		3		4		ns
t_{IH}	Input Register Hold Time from Input Clock	3		3		3		4		ns
t_{ICO}	Input Register Clock to Output Delay		23		23		25		30	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		15		15		20		30	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		15		15		20		30	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO} + t_{IS})$ & $1/(t_{WL} + t_{WH})$)[5]	38.4		38.4		35.7		29.4		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH} + t_{WL})$, $1/(t_{IS} + t_{IH}))$[5]	43.4		43.4		40		33.3		MHz
t_{ICEA}	Input Clock to Output Enabled		20		20		25		30	ns
t_{ICER}	Input Clock to Output Disabled		20		20		25		30	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled [5]		20		20		25		30	ns
t_{CER}	Output Clock to Output Disabled [5]		20		20		25		30	ns
t_S	Output Register Input Set-Up Time to Output Clock	10		12		15		20		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		11		12		15		20	ns
t_{CO2}	Output Register Clock or Latch Enable to Combinatorial Output Delay (Through Logic Array)[5]		22		23		30		35	ns

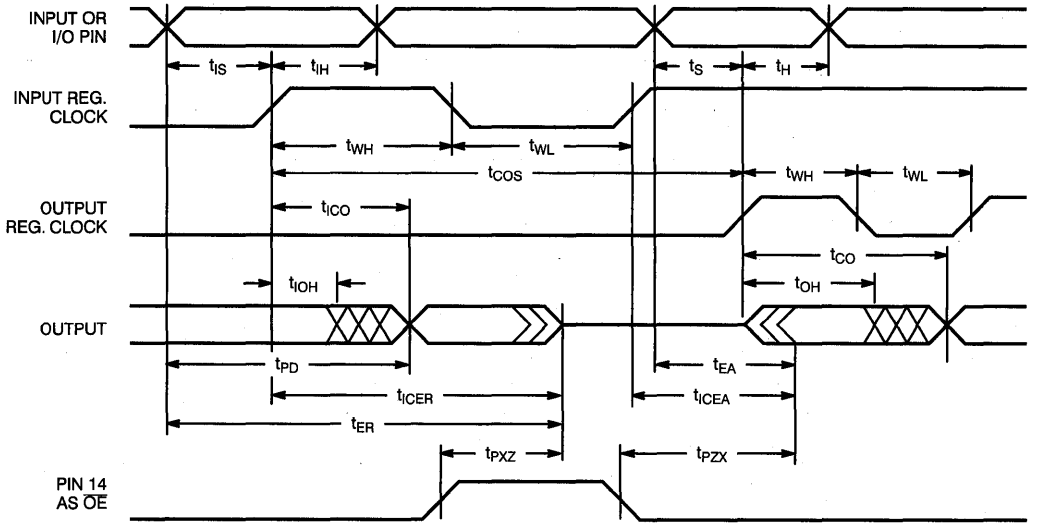
Notes:

6. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C335. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.
7. This part has been designed with the capability to reset during system power-up. Following power-up, the input and output registers will be reset to a logic LOW state. The output state will depend on how the array is programmed.

Military/Industrial AC Characteristics (continued)

Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array) [5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time [5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	83.3		66.6		50		40		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lower of $1/(t_{CO}+t_S)$ & $1/(t_{WL}+t_{WH})$)[5]	47.6		41.6		33.3		25		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$)[5]	90.9		83.3		62.5		50		MHz
$t_{OH}-t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{COS}	Input Clock to Output Clock	12		15		20		25		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{IS})$, or $1/(t_{CO})$), $1/(t_{IS}+t_{IH})$[5]	83.3		66.6		50		40		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO}+t_{IS})$ or $1/t_{COS}$)	71.4		66.6		50		40		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	µs

Switching Waveform



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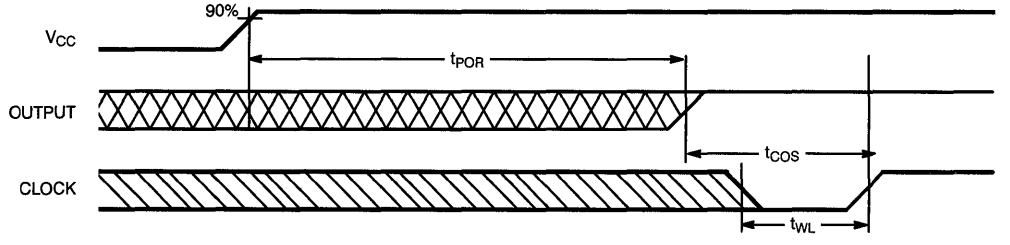
Power-Up Reset Waveform[7]



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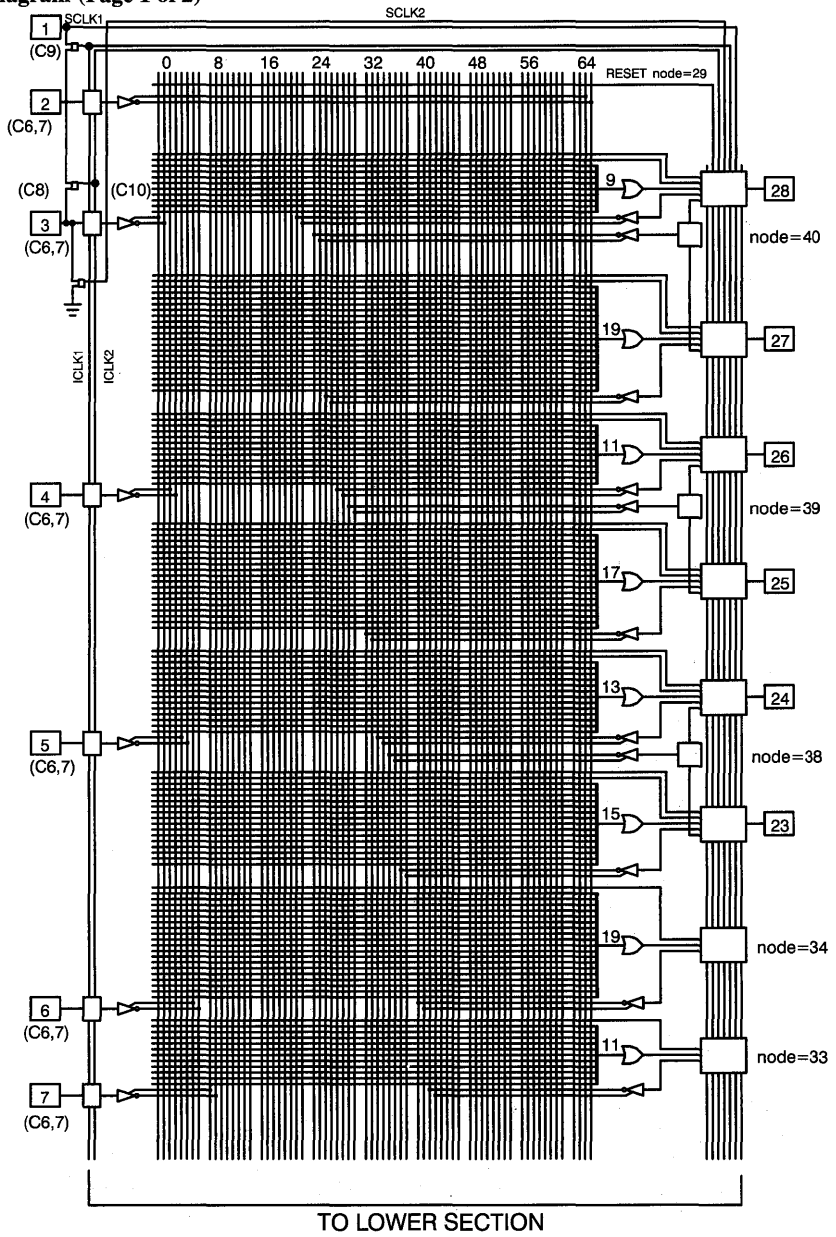
Block Diagram (Page 1 of 2)



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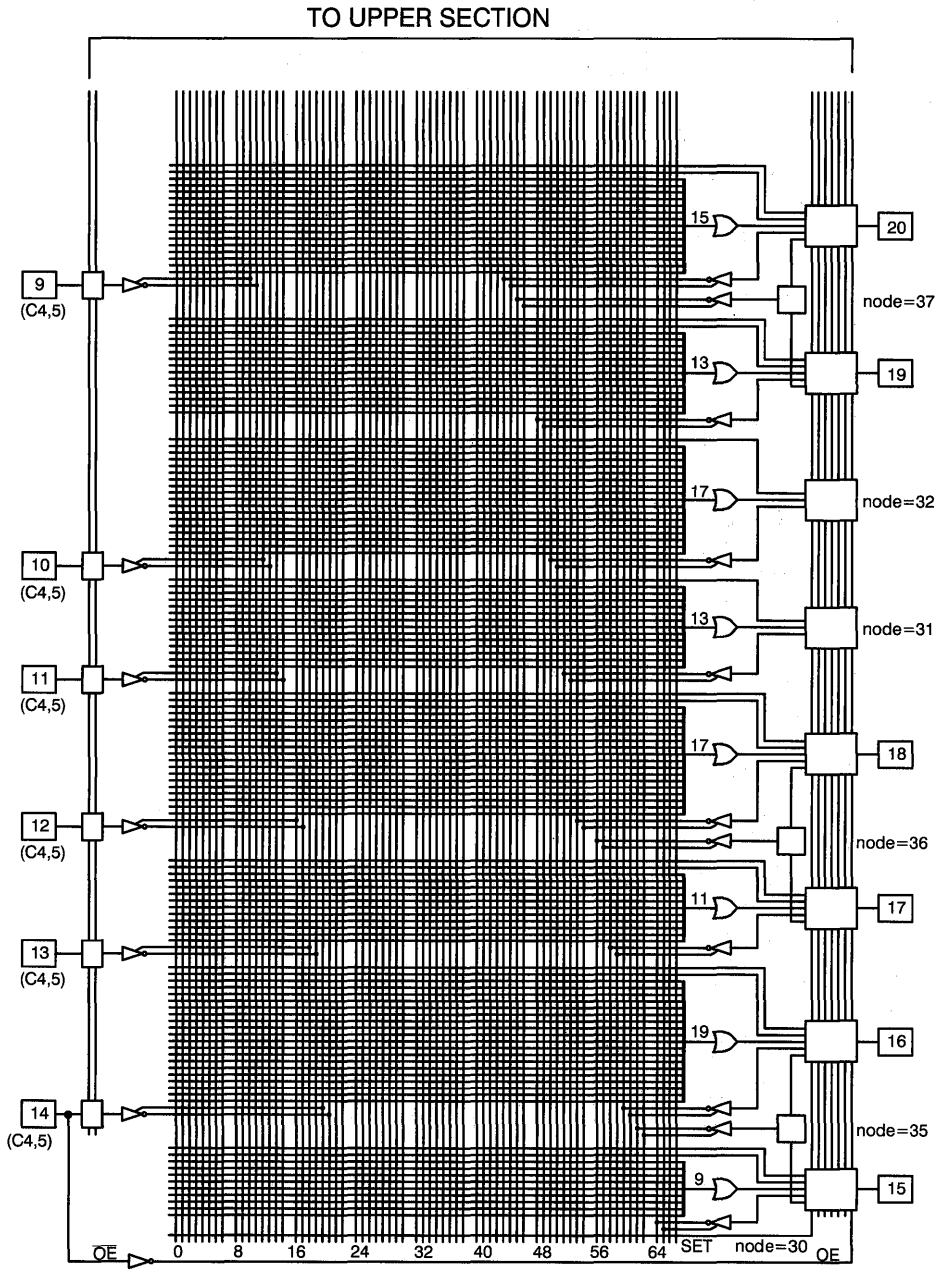
Block Diagram (Page 2 of 2)



C335-23

Ordering Information

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
100	140	CY7C335–100HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–100JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–100PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–100WC	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	160	CY7C335–83DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–83HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–83PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–83WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–83DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–83HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–83LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–83QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–83WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	140	CY7C335–83HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–83JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–83PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–83WC	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	160	CY7C335–66DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–66HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–66PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–66WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–66DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–66HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–66LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–66QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–66WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	140	CY7C335–66HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–66JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–66PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–66WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	140	CY7C335–50HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–50JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
50	160	CY7C335–50DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–50HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–50WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–50HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	160	CY7C335–40DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–40HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–40WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{ICO}	9, 10, 11
t_{IS}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{COS}	9, 10, 11

Document #: 38-00186-C

CY7C340 EPLD Family

Multiple Array Matrix High-Density EPLDs

Features

- **Erasable, user-configurable CMOS EPLDs capable of implementing high-density custom logic functions**
- **0.8-micron double-metal CMOS EPROM technology (CY7C34X)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C34XB)**
- **Multiple Array Matrix architecture optimized for speed, density, and straightforward design implementation**
  - **— Programmable Interconnect Array (PIA) simplifies routing**
  - **— Flexible macrocells increase utilization**
  - **— Programmable clock control**
  - **— Expander product terms implement complex logic functions**
- ***Warp2***
  - **— Low-cost VHDL compiler for PLDs**
  - **— IEEE 1076-compliant VHDL**
  - **— Available on PC and Sun platforms**
- ***Warp3***
  - **— VHDL synthesis**
  - **— ViewLogic graphical user interface**
  - **— Schematic capture (ViewDraw)**
  - **— VHDL simulation (ViewSim)**
  - **— Available on PC and Sun platforms**

General Description

The Cypress Multiple Array Matrix (MAX®) family of EPLDs provides a user-configurable, high-density solution to general-purpose logic integration requirements. With the combination of innovative architecture and state-of-the-art process, the MAX EPLDs offer LSI density without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 macrocells available in the CY7C342. Similarly, a 74151 8-to-1 multiplexer consumes less than 1% of the over 1,000 product terms in the CY7C342. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called expander product terms. These expanders are used and shared by the macrocells, allowing complex functions of up to 35 product terms to be easily implemented in a single macrocell. A Programmable Interconnect Array (PIA) globally routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress 0.8-micron, double-layer-metal CMOS EPROM process, yielding devices with significantly higher integration, density and system clock speed than the largest of previous generation EPLDs. The CY7C34XB devices are 0.65-micron shrinks of the original 0.8-micron family. The CY7C34XBs offer faster speed bins for each device in the Cypress MAX family.

The density and performance of the CY7C340 family is accessed using Cypress's *Warp2* and *Warp3* design software. *Warp2* provides state-of-the-art VHDL synthesis for MAX at a very low cost. *Warp3* is a sophisticated CAE tool that includes schematic capture (ViewDraw) and timing simulation (ViewSim) in addition to VHDL synthesis. Consult the *Warp2* and *Warp3* datasheets for more information about the development tools.

4 PLDs

Max Family Members

Feature	CY7C344(B)	CY7C343(B)	CY7C342(B)	CY7C341(B)
Macrocells	32	64	128	192
MAX Flip-Flops	32	64	128	192
MAX Latches[1]	64	128	256	384
MAX Inputs[2]	23	35	59	71
MAX Outputs	16	28	52	64
Packages	28H,J,W,D	44H,J	68H,J,R,G	84H,J,R,G

Key: D—DIP; G—Pin Grid Array; H—Windowed Ceramic Leaded Chip Carrier; J—J-Lead Chip Carrier; R—Windowed Pin Grid Array; W—Windowed Ceramic DIP

Notes:
1. When all expander product terms are used to implement latches.
2. With one output.

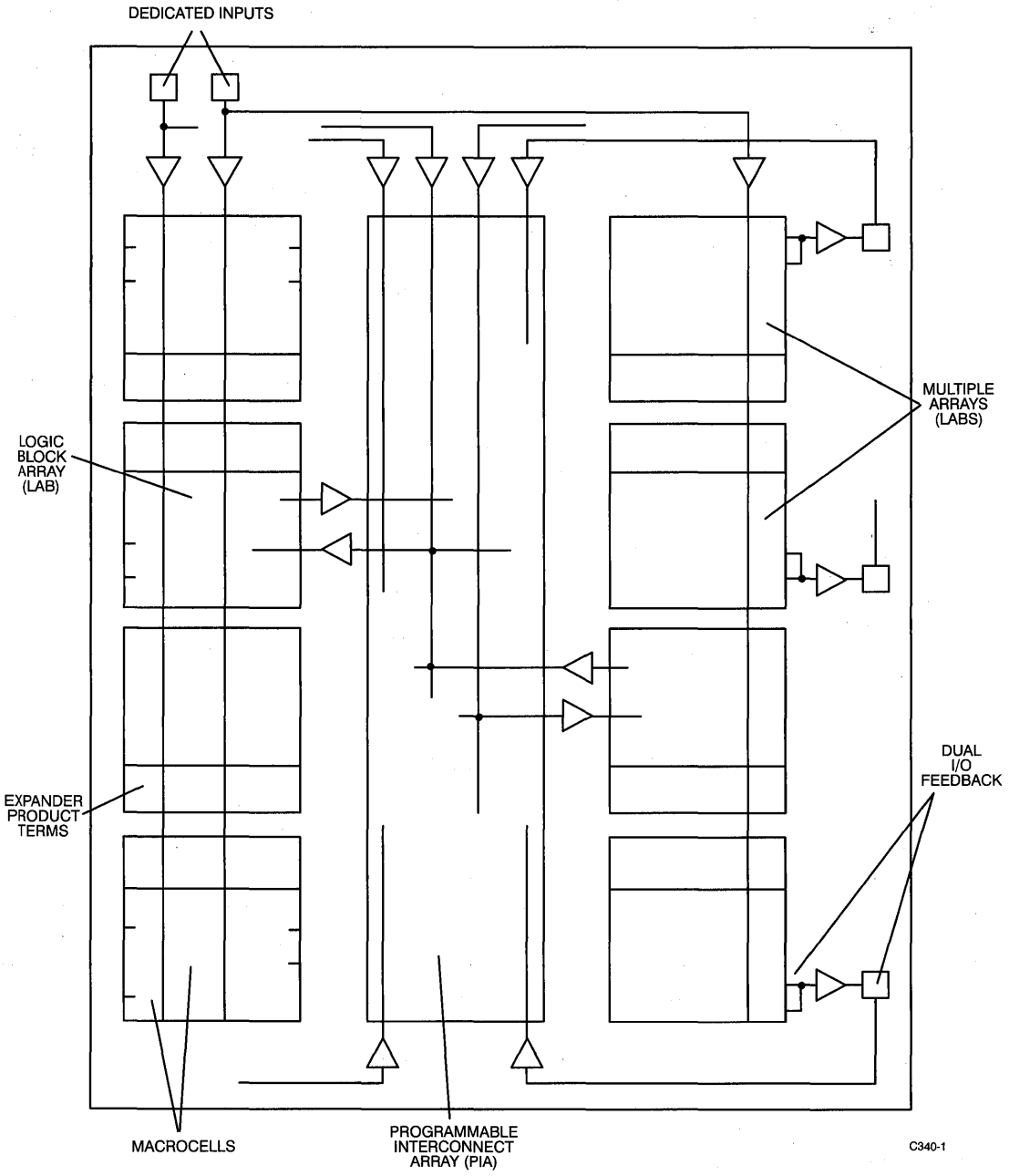


Figure 1. Key MAX Features

Functional Description

The Logic Array Block

The logic array block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a macrocell array, expander product term array, and an I/O block. The number of macrocells, expanders, and I/O vary, depending upon the device used. Global feedback of all signals is provided within a LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the programmable interconnect array and dedicated input bus. The feedbacks of the macrocells and I/O pins feed the PIA, providing access to them through other LABs in the device. The members of the CY7C340 family of EPLDs that have a single LAB use a global bus, so a PIA is not needed (see *Figure 3*).

The MAX Macrocell

Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL® (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per macrocell) require three product terms or less.

The macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 4*, each macrocell consists of a product term array and a configurable register. In the macrocell, combinatorial logic is implemented with three product terms ORed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active HIGH or active LOW logic and to implement T- and JK-type flip-flops.

If more product terms are required to implement a given function, they may be added to the macrocell from the expander product term array. These additional product terms may be added to any macrocell, allowing the designer to build gate-intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra macrocells.

The register within the macrocell may be programmed for either D, T, JK, or RS operation. It may alternately be configured as a flow-through latch for minimum input-to-output delays, or bypassed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters of shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

Expander Product Terms

The expander product terms, as shown in *Figure 5*, are fed by the dedicated input bus, the programmable interconnect array, the macrocell feedback, the expanders themselves, and the I/O pin feedbacks. The outputs of the expanders then go to each and every product term in the macrocell array. This allows expanders to be "shared" by the product terms in the logic array block. One expander may feed all macrocells in the LAB, or even multiple product terms in the same macrocell. Since these expanders feed the secondary product terms (preset, clear, clock, and output enable) of each macrocell, complex logic functions may be implemented without utilizing another macrocell. Likewise, expanders may feed and be shared by other expanders, to implement complex multilevel logic and input latches.

I/O Block

Separate from the macrocell array is the I/O control block of the LAB. *Figure 6* shows the I/O block diagram. The three-state buffer is controlled by a macrocell product term and the drives the I/O pad. The input of this buffer comes from a macrocell within the

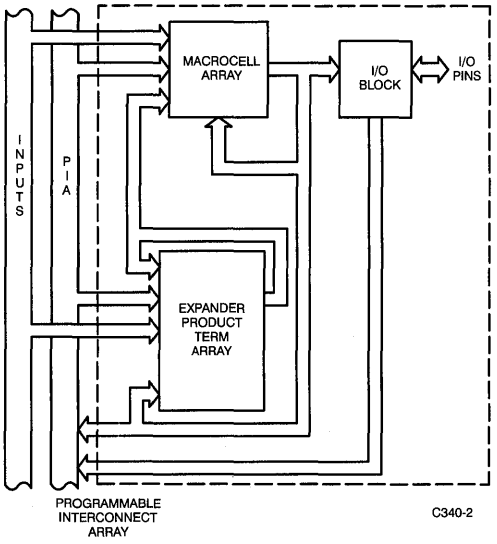


Figure 2. Typical LAB Block Diagram

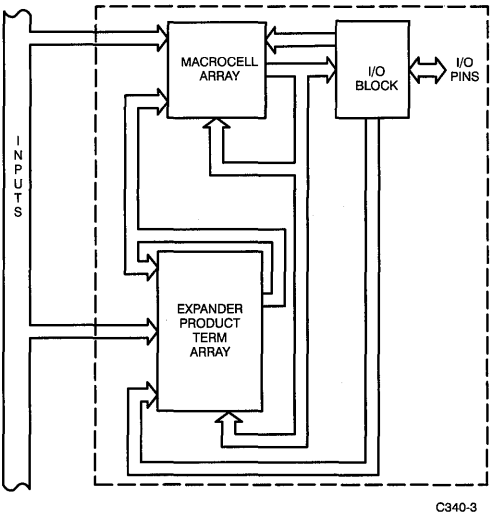


Figure 3. 7C344 LAB Block Diagram

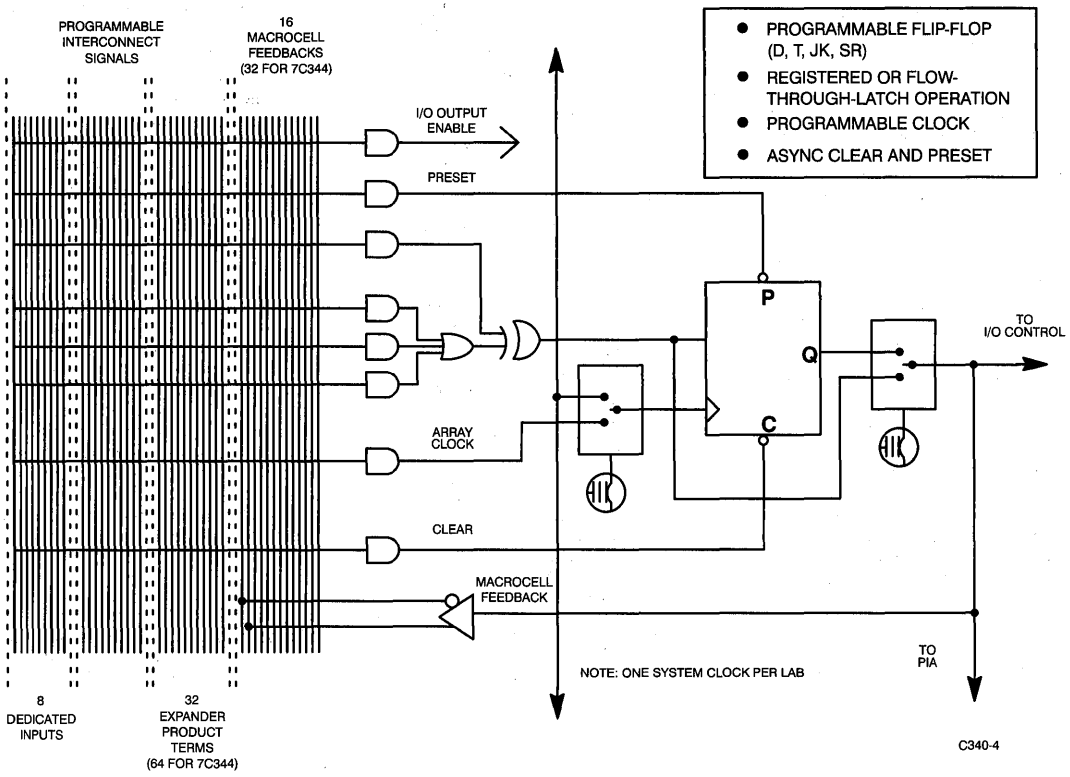


Figure 4. Macrocell Block Diagram

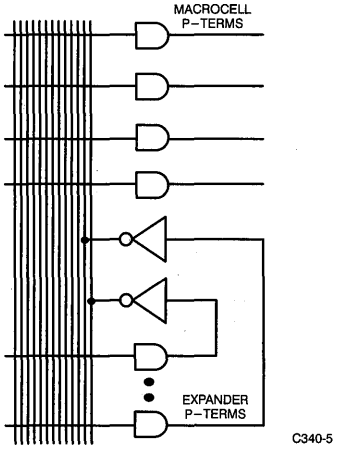


Figure 5. Expander Product Terms

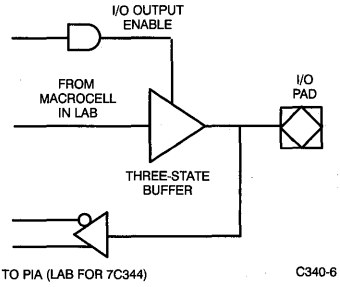


Figure 6. I/O Block Diagram

Functional Description (continued)

associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as the PIA. By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried," allowing the I/O pins to be used as dedicated outputs, bidirectional outputs, or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the macrocell register and the associated I/O pin, as in earlier devices.

The Programmable Interconnect Array

PLD density and speed has traditionally been limited by signal routing; i.e., getting signals from one macrocell to another. For smaller devices, a single array is used and all signals are available to all macrocells. But as the devices increase in density, the number of signals being routed becomes very large, increasing the amount of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible logic array blocks that, in the larger devices, are interconnected by a PIA.

The PIA solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed delay from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

Development Software Support

Warp2

Warp2 is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design entry process. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map for the desired device. For simulation, *Warp2* provides the graphical waveform simulator from the PLD ToolKit.

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense, and supported by every major vendor of CAE tools. VHDL allows designers to learn a single language that is useful for all facets of the design process.

Warp3

Warp3 is a sophisticated design tool that is based on the latest version of ViewLogic's CAE design environment. *Warp3* features schematic capture (ViewDraw®), VHDL waveform simulation (ViewSim®), a VHDL debugger, and VHDL synthesis, all integrated in a graphical design environment. *Warp3* is available on PCs using Windows 3.1 or subsequent versions, and on Sun workstations.

For further information on Warp software, see the *Warp2* and *Warp3* Datasheets contained in this data book.

Ordering Information

Device Adapters

CY3340	Adapter for CY7C341 in PLCC packages.
CY3340F	Adapter for CY7C341 in PGA packages.
CY3342	Adapter for CY7C342 in PLCC packages.
CY3342F	Adapter for CY7C342 in Flatpack packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY33435	Adapter for CY7C343 in PLCC packages.

Document #: 38–00087–C

CY7C341
CY7C341B

CYPRESS SEMICONDUCTOR

192-Macrocell MAX® EPLD

Features

- **192 macrocells in 12 LABs**
- **8 dedicated inputs, 64 bidirectional I/O pins**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin HLCC, PLCC, and PGA packages**

Functional Description

The CY7C341 and CY7C341B are Erasable Programmable Logic Devices (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341 and CY7C341B are divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341 and CY7C341B allows them to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341 and CY7C341B allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341 and CY7C341B reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J, and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Logic Array Blocks

There are 12 logic array blocks in the CY7C341 and CY7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341 and CY7C341B provide 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C341 and CY7C341B may be easily determined using *Warp* software or by the model shown in *Figure 1*. The CY7C341 and CY7C341B have fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp* software provides a timing simulator.

Design Recommendations

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C341 and CY7C341B contain a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

The CY7C341 and CY7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

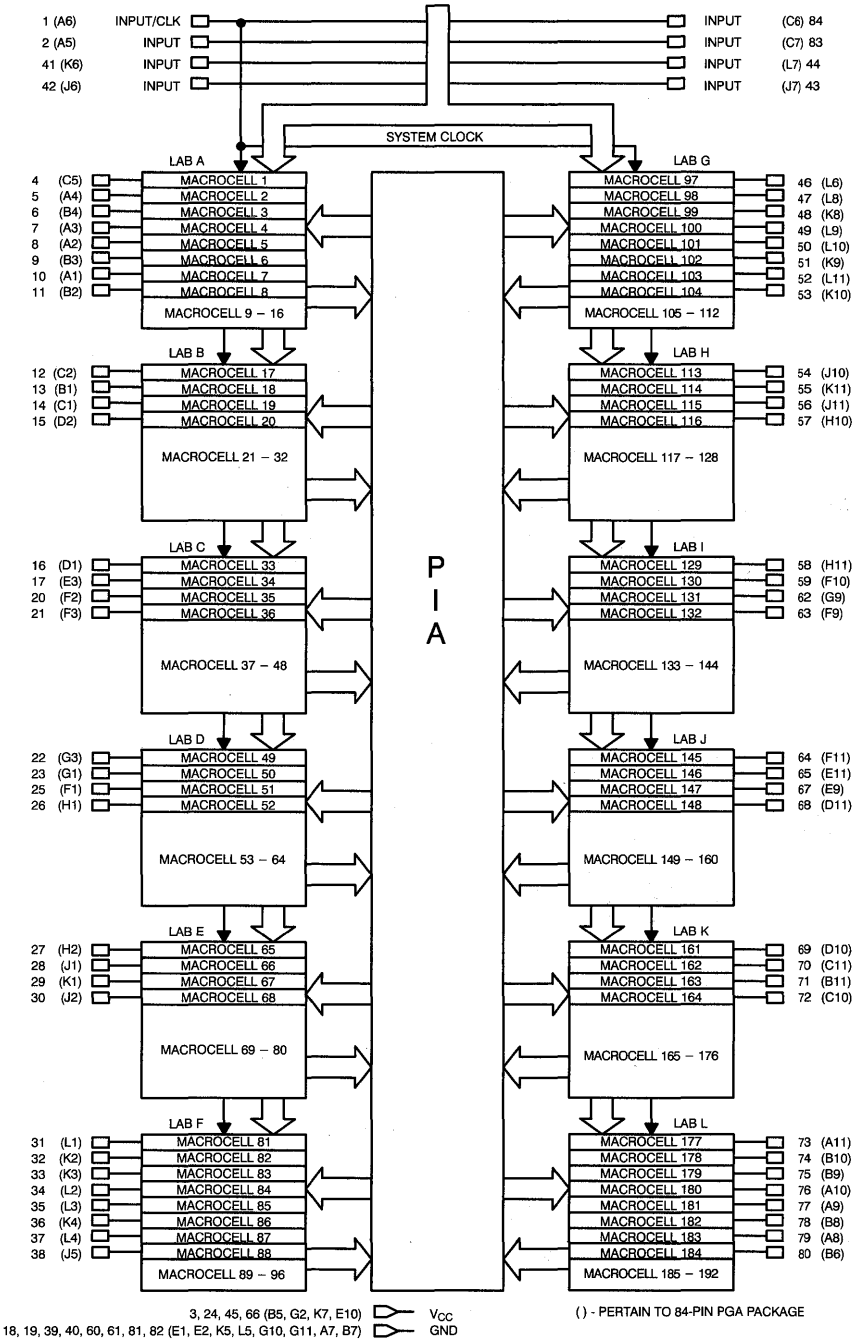
The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Selection Guide

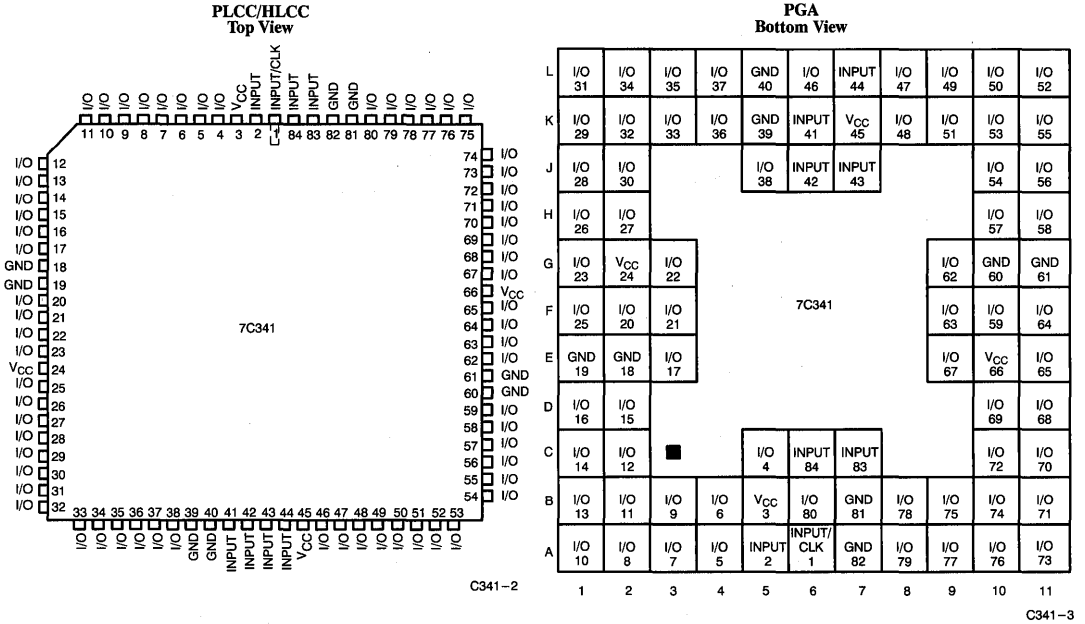
		7C341B–15	7C341B–20	7C341–25	7C341B–25	7C341–30	7C341–35	7C341–40
Maximum Access Time (ns)		15	20	25	25	30	35	40
Maximum Operating Current (mA)	Commercial	380	380	380		380	380	
	Industrial	480	480	480		480	480	
	Military		480		480	480	480	480
Maximum Standby Current (mA)	Commercial	360	360	360		360	360	
	Industrial	435	435	435		435	435	
	Military		435		435	435	435	435

Shaded areas contain preliminary information.

Logic Block Diagram



Pin Configurations



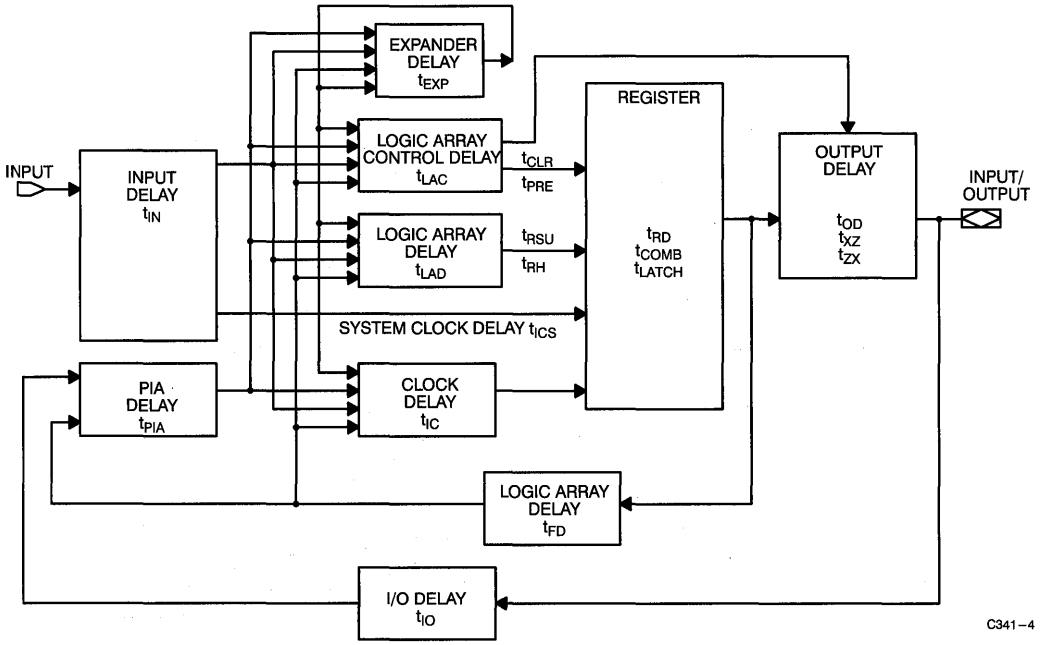


Figure 1. CY7C341 Internal Timing Model

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... 0°C to +70°C
Maximum Junction Temperature (Under Bias) ..... 150°C
Supply Voltage to Ground Potential ..... −2.0V to +7.0V
Maximum Power Dissipation ..... 2500 mW
DC V_{CC} or GND Current ..... 500 mA
DC Output Current, per Pin ..... −25 mA to +25 mA
DC Input Voltage[1] ..... −3.0V to +7.0V
DC Program Voltage 13.5V
Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	$GND \leq V_{IN} \leq V_{CC}$		−10	+10	μA
I_{OZ}	Output Leakage Current	$V_O = V_{CC}$ or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	$V_I = V_{CC}$ or GND (No Load)	Com'l		360	mA
			Mil/Ind		435	mA
I_{CC2}	Power Supply Current[5]	$V_I = V_{CC}$ or GND (No Load) f = 1.0 MHz[3, 5]	Com'l		380	mA
			Mil/Ind		480	mA
t_R (Recommended)	Input Rise Time				100	ns
t_F (Recommended)	Input Fall Time				100	ns

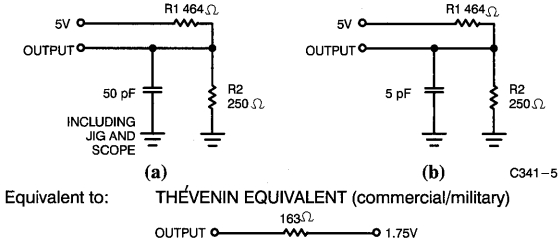
Capacitance[6]

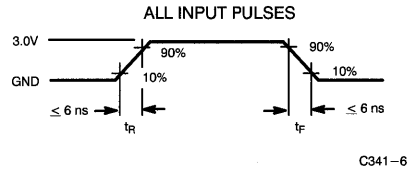
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Guaranteed but not 100% tested.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB and is tested periodically by sampling production material.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms





External Synchronous Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C341B–15		7C341B–20		7C341–25		7C341B–25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l		15		20		25			ns
		Mil				20				25	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l		25		33		40			ns
		Mil				33				40	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		23		30		37			ns
		Mil				30				37	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[3, 10]	Com'l		33		43		52			ns
		Mil				43				52	
t_{EA}	Input to Output Enable Delay[3, 7]	Com'l		15		20		25			ns
		Mil				20				25	
t_{ER}	Input to Output Disable Delay[6]	Com'l		15		20		25			ns
		Mil				20				25	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		7		8		14			ns
		Mil				8				14	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[3, 11]	Com'l		17		20		30			ns
		Mil				20				30	
t_{S1}	Dedicated Input or Feedback Set-upTime to Synchronous Clock Output[6,12]	Com'l	10		12		15				ns
		Mil			12				15		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[8]	Com'l	20		24		30				ns
		Mil			24				30		
t_H	Input Hold Time from Synchronous Clock Input[6]	Com'l	0		0		0				ns
		Mil			0				0		
t_{WH}	Synchronous Clock Input High Time	Com'l	5		7		8				ns
		Mil			7				8		
t_{WL}	Synchronous Clock Input Low Time	Com'l	5		7		8				ns
		Mil			7				8		
t_{RW}	Asynchronous Clear Width[3, 6]	Com'l	16		22		25				ns
		Mil			22				25		
t_{RR}	Asynchronous Clear Recovery[3, 7]	Com'l	16		22		25				ns
		Mil			22				25		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		15		20		25			ns
		Mil				20				25	
t_{PW}	Asynchronous Preset Width[3, 6]	Com'l	15		20		25				ns
		Mil			20				25		
t_{PR}	Asynchronous Preset Recovery Time[3, 6]	Com'l	15		20		25				ns
		Mil			20				25		

Shaded areas contain preliminary information.

External Synchronous Switching Characteristics Over the Operating Range[6](continued)

Parameter	Description		7C341B–15 Min.	7C341B–15 Max.	7C341B–20 Min.	7C341B–20 Max.	7C341–25 Min.	7C341–25 Max.	7C341B–25 Min.	7C341B–25 Max.	Unit
t_{PO}	Asynchronous Preset to Registered Output Delay[6]	Com'l		15		20		25			ns
		Mil				20				25	
t_{CF}	Synchronous Clock to Local Feedback Input[3, 13]	Com'l		3		3		3			ns
		Mil				3				3	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[3]	Com'l	12		14		16				ns
		Mil			14				16		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[3, 14]	Com'l	58.8		50		34.5				MHz
		Mil			50				34.5		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[3, 15]	Com'l	76.9		66.6		55.5				MHz
		Mil			66.6				55.5		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[3, 16]	Com'l	100		71.4		62.5				MHz
		Mil			71.4				62.5		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[3, 17]	Com'l	100		71.4		62.5				MHz
		Mil			71.4				62.5		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[3, 18]	Com'l	3		3		3				ns
		Mil			3				3		

Shaded areas contain preliminary information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic functions and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycle by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Synchronous Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description		7C341–30		7C341–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l		30		35			ns
		Mil		30		35		40	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l		45		55			ns
		Mil		45		55		65	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		44		55			ns
		Mil		44		55		65	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[3, 10]	Com'l		59		75			ns
		Mil		59		75		90	
t_{EA}	Input to Output Enable Delay[3, 7]	Com'l		30		35			ns
		Mil		30		35		40	
t_{ER}	Input to Output Disable Delay[6]	Com'l		30		35			ns
		Mil		30		35		40	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil		16		20		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[3, 11]	Com'l		35		42			ns
		Mil		35		42		48	
t_{S1}	Dedicated Input or Feedback Set-upTime to Synchronous Clock Output[6,12]	Com'l	20		25				ns
		Mil	20		25		28		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[8]	Com'l	39		45				ns
		Mil	39		45		52		
t_H	Input Hold Time from Synchronous Clock Input[6]	Com'l	0		0				ns
		Mil	0		0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{RW}	Asynchronous Clear Width[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		
t_{RR}	Asynchronous Clear Recovery[3, 7]	Com'l	30		35				ns
		Mil	30		35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		30		35			ns
		Mil		30		35		40	
t_{PW}	Asynchronous Preset Width[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		
t_{PR}	Asynchronous Preset Recovery Time[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		

External Synchronous Switching Characteristics Over the Operating Range[6](continued)

Parameter	Description		7C341–30		7C341–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PO}	Asynchronous Preset to Registered Output Delay[6]	Com'l		30		35			ns
		Mil		30		35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[3, 13]	Com'l		3		5			ns
		Mil		3		5		7	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[3]	Com'l	20		25				ns
		Mil	20		25		30		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[3, 14]	Com'l	27.7		22.2				MHz
		Mil	27.7		22.2		19.6		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[3, 15]	Com'l	43		33				MHz
		Mil	43		33		28.5		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[3, 16]	Com'l	50		40.0				MHz
		Mil	50		40.0		33.3		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[3, 17]	Com'l	50		40.0				MHz
		Mil	50		40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[3, 18]	Com'l	3		3				ns
		Mil	3		3		3		

External Asynchronous Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description		7C341B–15 Min.	7C341B–15 Max.	7C341B–20 Min.	7C341B–20 Max.	7C341–25 Min.	7C341–25 Max.	7C341B–25 Min.	7C341B–25 Max.	Unit
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[6]	Com'l		15		20		25			ns
		Mil				20				25	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [19]	Com'l		25		32		40			ns
		Mil				32				40	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[6]	Com'l	5		6		5				ns
		Mil			6				5		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[6]	Com'l	14		18		20				ns
		Mil			18				20		
t_{AH}	Input Hold Time from Asynchronous Clock Input[6]	Com'l	5		6		6				ns
		Mil			6				6		
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Com'l	5		7		11				ns
		Mil			7				11		
t_{AWL}	Asynchronous Clock Input LOW Time[6, 20]	Com'l	5		7		9				ns
		Mil			7				9		
t_{ACF}	Asynchronous Clock to Local Feedback Input[21]	Com'l		10		13		15			ns
		Mil				13				15	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)	Com'l	12		14		20				ns
		Mil			14				20		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[22]	Com'l	55.5		40		33.3				MHz
		Mil			40				33.3		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[23]	Com'l	76.9		58		50				MHz
		Mil			58				50		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[24]	Com'l	66.6		50		40				MHz
		Mil			50				40		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[25]	Com'l	77		58		50				MHz
		Mil			58				50		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[26]	Com'l	15		15		15				ns
		Mil			15				15		

Shaded areas contain preliminary information.

Notes:

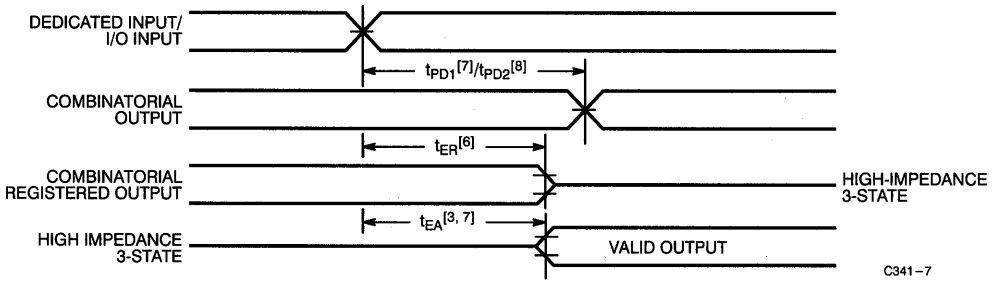
19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, and assumes there is no expander logic in the clock path and the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS1})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

External Asynchronous Switching Characteristics Over the Operating Range[6] (continued)

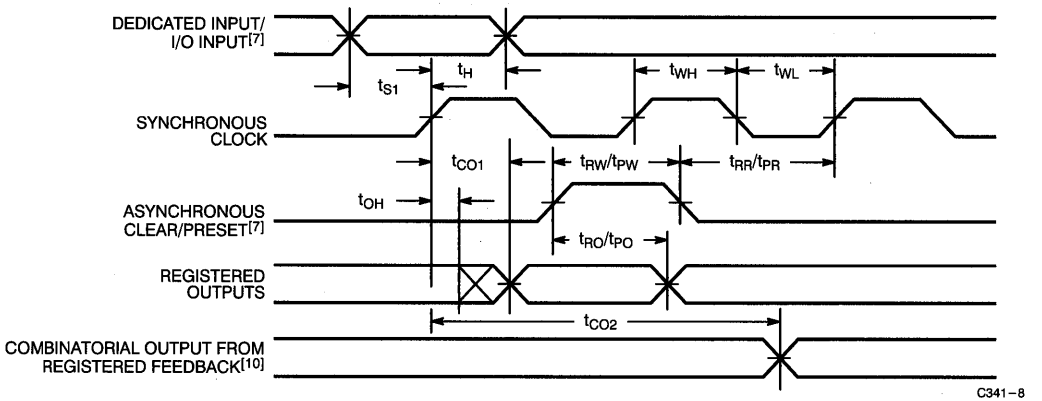
Parameter	Description		7C341–30		7C341–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[6]	Com'l		30		35			ns
		Mil		30		35		45	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [19]	Com'l		46		55			ns
		Mil		46		55		64	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[6]	Com'l	6		8				ns
		Mil	6		8		10		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[6]	Com'l	27		30				ns
		Mil	27		30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[6]	Com'l	8		10				ns
		Mil	8		10		12		
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Com'l	14		16				ns
		Mil	14		16		20		
t_{AWL}	Asynchronous Clock Input LOW Time[6, 20]	Com'l	11		14				ns
		Mil	11		14		20		
t_{ACF}	Asynchronous Clock to Local Feedback Input[21]	Com'l		18		22			ns
		Mil		18		22		26	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)	Com'l	25		30				ns
		Mil	25		30		40		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[22]	Com'l	27		23				MHz
		Mil	27		23		18		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[23]	Com'l	40		33.3				MHz
		Mil	40		33.3		25		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[24]	Com'l	33.3		28.5				MHz
		Mil	33.3		28.5		22.2		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[25]	Com'l	40		33.3				MHz
		Mil	40		33.3		25		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[26]	Com'l	15		15				ns
		Mil	15		15		15		

Switching Waveforms

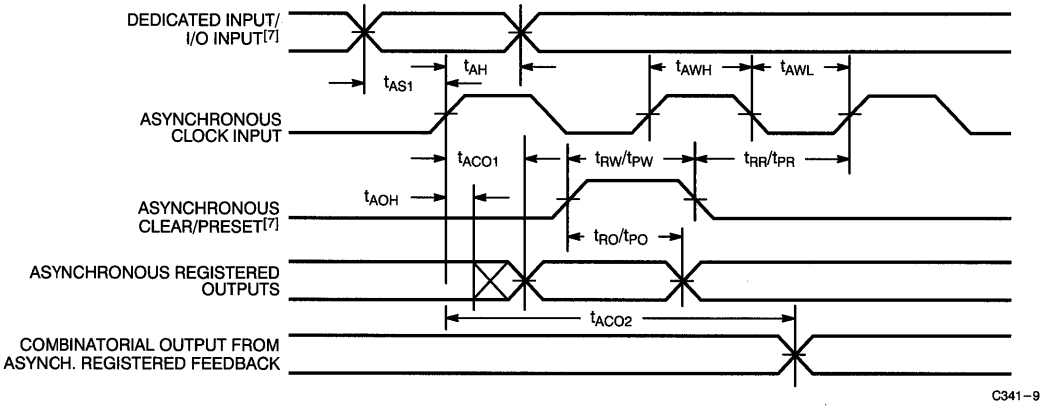
External Combinatorial



External Synchronous



External Asynchronous



Internal Switching Characteristics Over the Operating Range[1]

Parameter	Description		7C341B–15 Min.	7C341B–15 Max.	7C341B–20 Min.	7C341B–20 Max.	7C341–25 Min.	7C341–25 Max.	7C341B–25 Min.	7C341B–25 Max.	Unit
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		3		4		5			ns
		Mil				4				5	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		3		4		6			ns
		Mil				4				6	
t_{EXP}	Expander Array Delay	Com'l		8		10		12			ns
		Mil				10				12	
t_{LAD}	Logic Array Data Delay	Com'l		8		10		12			ns
		Mil				10				12	
t_{LAC}	Logic Array Control Delay	Com'l		5		5		10			ns
		Mil				5				10	
t_{OD}	Output Buffer and Pad Delay	Com'l		3		3		5			ns
		Mil				3				5	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l		5		5		10			ns
		Mil				5				10	
t_{XZ}	Output Buffer Disable Delay	Com'l		5		5		10			ns
		Mil				5				10	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	4		5		6				ns
		Mil			5				6		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	4		5		6				ns
		Mil			5				6		
t_{LATCH}	Flow-Through Latch Delay	Com'l		1		1		3			ns
		Mil				1				3	
t_{RD}	Register Delay	Com'l		1		1		1			ns
		Mil				1				1	
t_{COMB}	Transparent Mode Delay[28]	Com'l		1		1		3			ns
		Mil				1				3	
t_{CH}	Clock High Time	Com'l	4		6		8				ns
		Mil			6				8		
t_{CL}	Clock Low Time	Com'l	4		6		8				ns
		Mil			6				8		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		6		8		14			ns
		Mil				8				14	
t_{ICS}	Synchronous Clock Delay	Com'l		0		0		2			ns
		Mil				0				2	
t_{FD}	Feedback Delay	Com'l		1		1		1			ns
		Mil				1				1	
t_{PRE}	Asynchronous Register Preset Time	Com'l		3		3		5			ns
		Mil				3				5	
t_{CLR}	Asynchronous Register Clear Time	Com'l		3		3		5			ns
		Mil				3				5	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	3		4		5				ns
		Mil			4				5		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	3		4		5				ns
		Mil			4				5		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		10		13		14			ns
		Mil				13				14	

Shaded areas contain preliminary information

Notes:

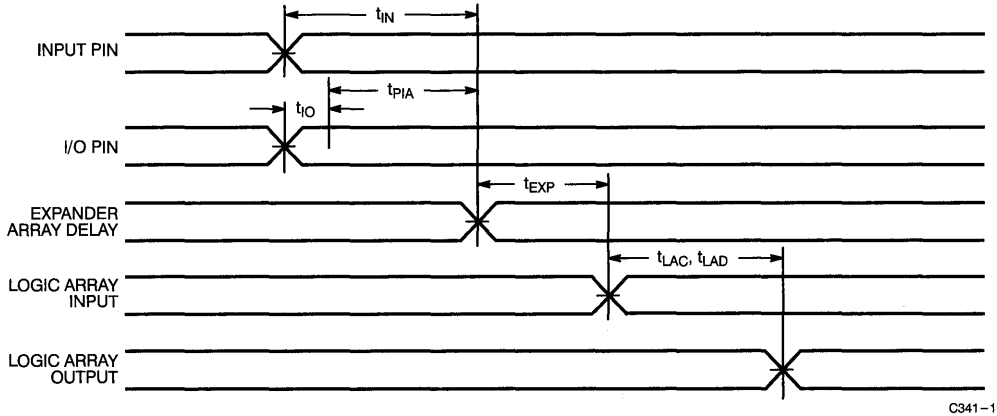
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Internal Switching Characteristics Over the Operating Range[1]

Parameter	Description		7C341–30		7C341–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil		7		9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		6		9			ns
		Mil		6		9		12	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil		14		20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil		14		16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil		12		13		14	
t_{OD}	Output Buffer and Pad Delay	Com'l		5		6			ns
		Mil		5		6		7	
t_{ZX}	Output Buffer Enable Delay[29]	Com'l		11		13			ns
		Mil		11		13		15	
t_{XZ}	Output Buffer Disable Delay	Com'l		11		13			ns
		Mil		11		13		15	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil	8		10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil	8		10		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l		4		4			ns
		Mil		4		4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil		2		2		2	
t_{COMB}	Transparent Mode Delay[30]	Com'l		4		4			ns
		Mil		4		4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil		16		18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil		2		3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil		1		2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil		6		7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil		6		7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil	6		7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil	6		7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil		16		20		24	

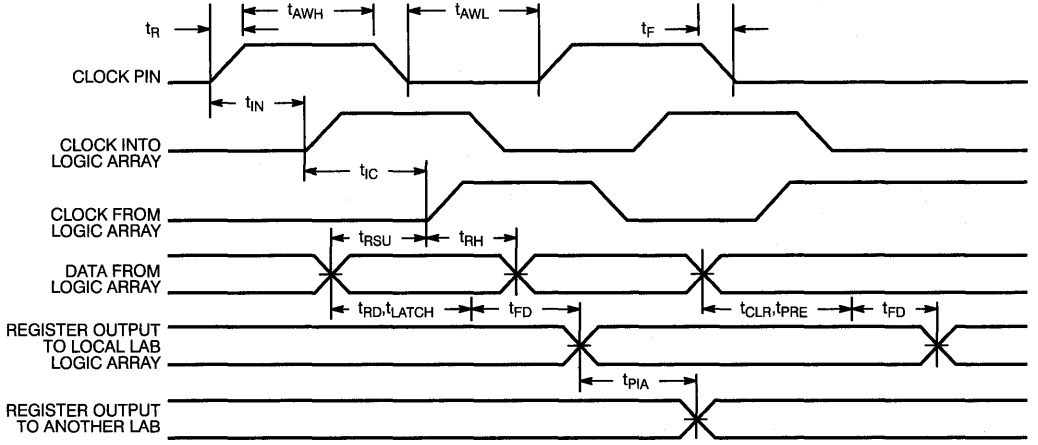
Switching Waveforms (continued)

Internal Combinatorial



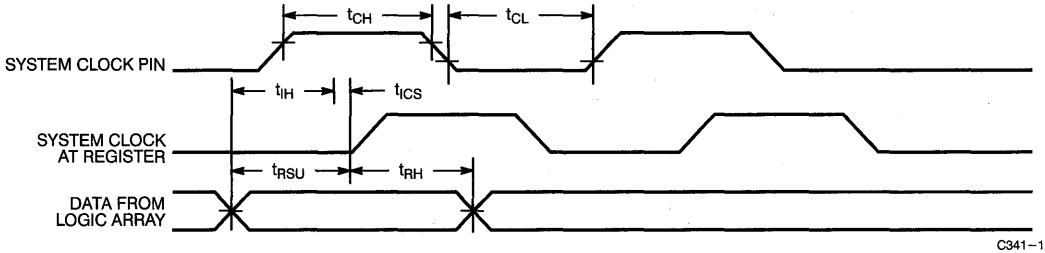
C341-10

Internal Asynchronous



C341-11

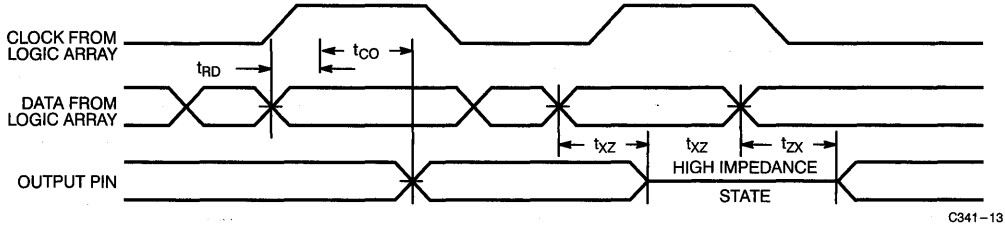
Internal Synchronous



C341-12

Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C341B-15HC	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C341B-15JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B-15RC/RI	R84	84-Lead Windowed Pin Grid Array	
20	CY7C341B-20HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C341B-20JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B-20RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B-20HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B-20RMB	R84	84-Lead Windowed Pin Grid Array	
25	CY7C341-25GC	G84	84-Pin Pin Grid Array (Cavity Up)	Commercial
	CY7C341-25HC	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341-25JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341-25RC	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B-25HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B-25RMB	R84	84-Lead Windowed Pin Grid Array	
30	CY7C341-30GC	G84	84-Pin Pin Grid Array (Cavity Up)	Commercial
	CY7C341-30HC	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341-30JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341-30RC	R84	84-Lead Windowed Pin Grid Array	
	CY7C341-30HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341-30RMB	R84	84-Lead Windowed Pin Grid Array	
35	CY7C341-35GC	G84	84-Pin Pin Grid Array (Cavity Up)	Commercial
	CY7C341-35HC	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341-35JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341-35RC	R84	84-Lead Windowed Pin Grid Array	
	CY7C341-35HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341-35RMB	R84	84-Lead Windowed Pin Grid Array	
40	CY7C341-40HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341-40RMB	R84	84-Lead Windowed Pin Grid Array	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38−00137−E

CY7C342
CY7C342B

CYPRESS SEMICONDUCTOR

128-Macrocell MAX® EPLDs

Features

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **Available in 68-pin HLCC, PLCC, PGA, and Flatpack**

Functional Description

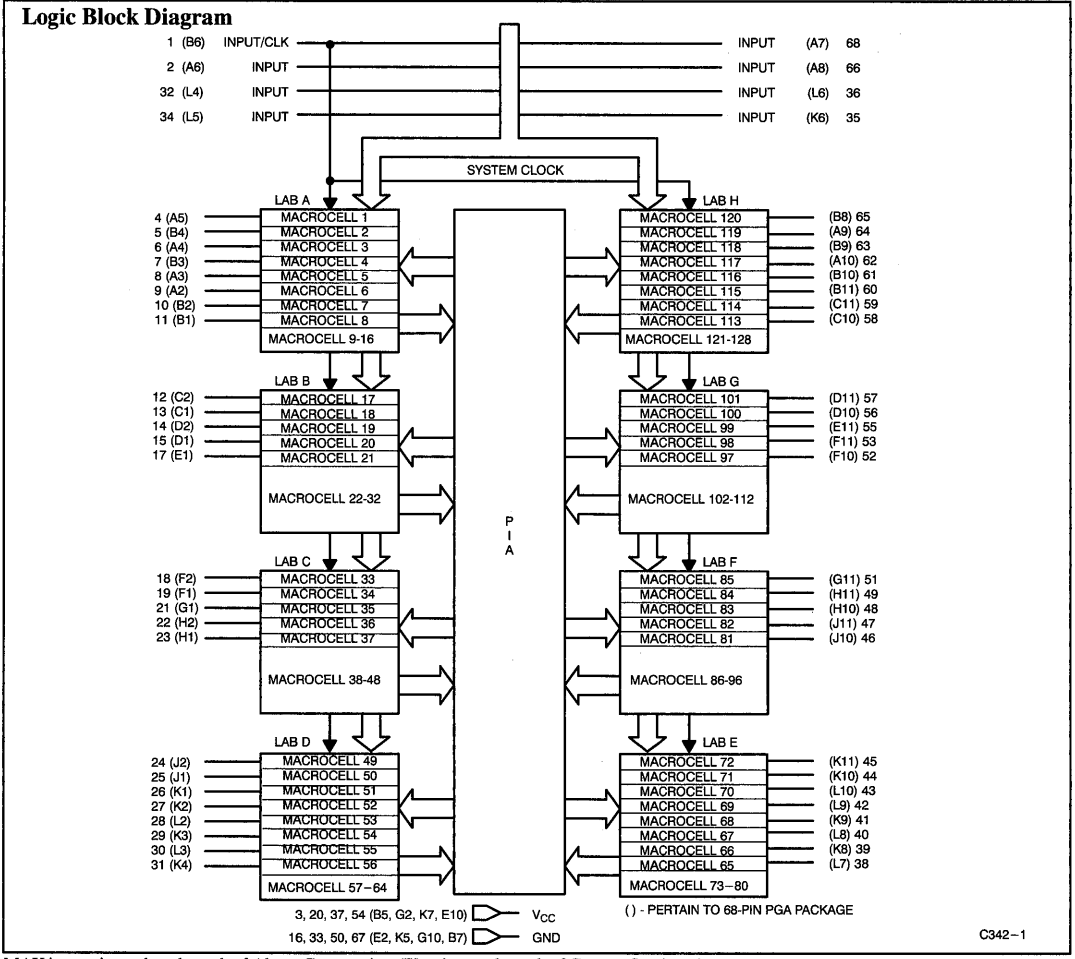
The CY7C342/CY7C342B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342/CY7C342B are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342/CY7C342B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342/CY7C342B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342/CY7C342B reduces board space, part count, and increases system reliability.

Logic Block Diagram



MAX is a registered trademark of Altera Corporation. *Warp* is a trademark of Cypress Semiconductor.

Selection Guide

		7C342B–15	7C342B–20	7C342–25	7C342–30	7C342–35
Maximum Access Time (ns)		15	20	25	30	35
Maximum Operating Current (mA)	Commercial	250	250	250	250	250
	Military		320	320	320	320
	Industrial	320	320	320	320	320
Maximum Static Current (mA)	Commercial	225	225	225	225	225
	Military		275	275	275	275
	Industrial	275	275	275	275	275

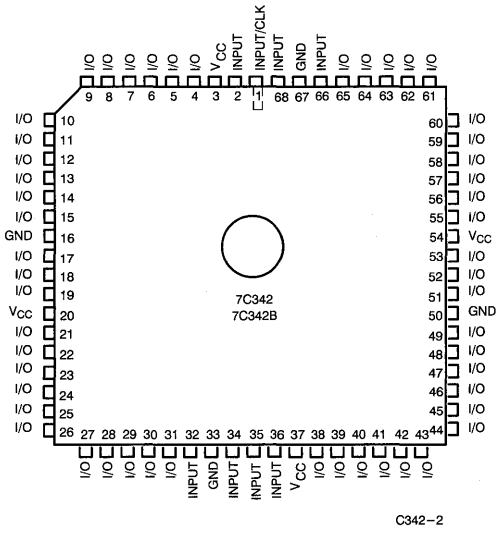
Shaded area contains preliminary information.

4

PLDs

Pin Configurations

PLCC/Flatpack
Top View



C342–2

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L		I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	I/O	I/O	
K	I/O	I/O	I/O	I/O	GND	INPUT	VCC	I/O	I/O	I/O	I/O
J	I/O	I/O								I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	VCC								GND	I/O
F	I/O	I/O				7C342 7C342B				I/O	I/O
E	I/O	GND								VCC	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O								I/O	I/O
B	I/O	I/O	I/O	I/O	VCC	INPUT/ CLK	GND	I/O	I/O	I/O	I/O
A	■	I/O	I/O	I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	

C342–3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (under bias) ..... 150°C

Supply Voltage to Ground Potential ..... − 3.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current per Pin ..... − 25 mA to +25 mA

DC Input Voltage[1] ..... − 3.0V to + 7.0V

DC Program Voltage 13.5V

Static Discharge Voltage ..... > 1100V (per MIL−STD−883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	− 40°C to +85°C	5V ± 10%
Military	− 55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			− 0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		− 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3,4]		− 30	− 90	mA
I_{CC1}	Power Supply Current (Static)	V_I = GND (No Load)	Com'l		225	mA
			Mil/Ind		275	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Com'l		250	mA
			Mil/Ind		320	
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

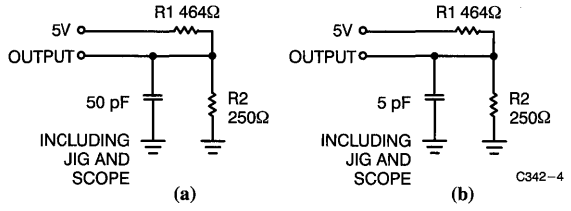
Capacitance[6]

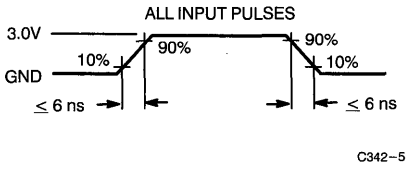
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2V, f = 1.0 MHz	10	pF

Notes:

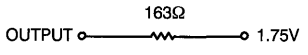
1. Minimum DC input is − 0.3V. During transitions, the inputs may undershoot to − 3.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[4]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Logic Array Blocks

There are 8 logic array blocks in the CY7C342/CY7C342B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342/CY7C342B provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals that may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a signal pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342/CY7C342B may be easily determined using *Warp*™ software or by the model shown in *Figure 1*. The CY7C342/CY7C342B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the *Warp*™ software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342/CY7C342B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

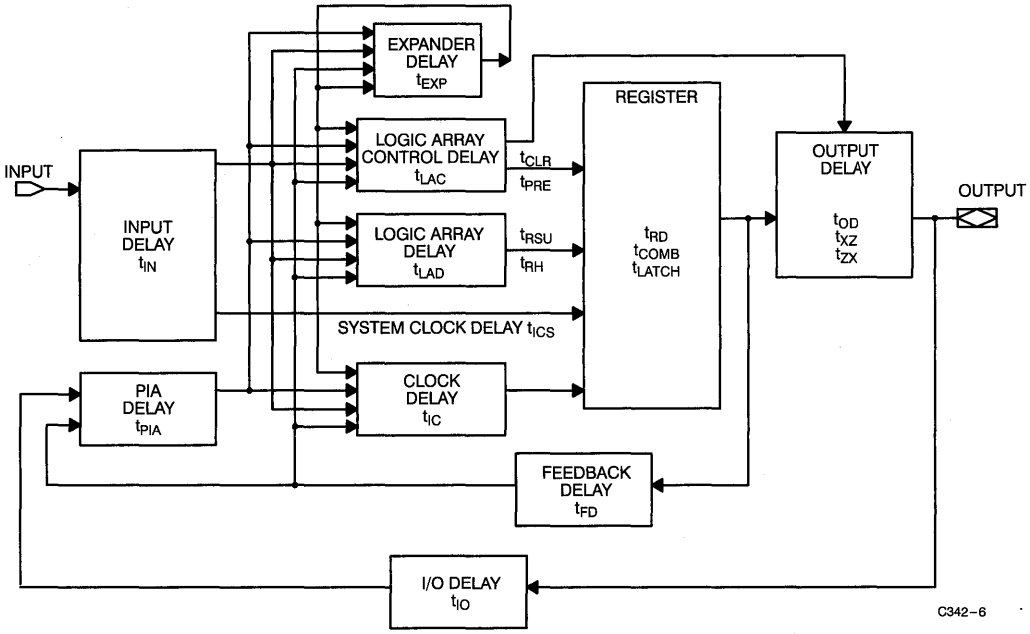


Figure 1. CY7C342/CY7C342B Internal Timing Model

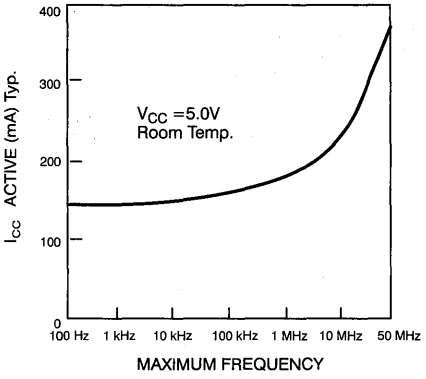
Design Security

The CY7C342/CY7C342B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

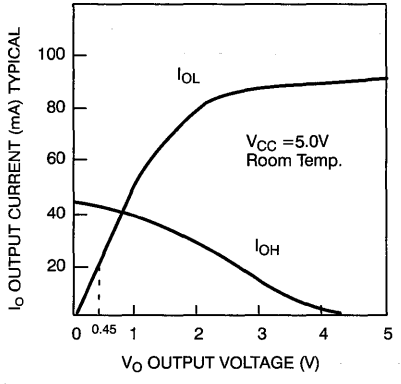
The CY7C342/CY7C342B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on dedicated input pins. The parameter t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same asynchronous clock as the CY7C342.CY7C342B

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		15		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		25		32		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		23		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		33		42		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		15		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		15		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		7		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		17		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	10		12		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	20		24		29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	5		7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	5		7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	16		22		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4,7]	16		22		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		15		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	15		20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	15		20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		15		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	12		14		16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	58.8		50.0		34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	100		71.4		55.5		43.4		32.2		MHz

Shaded area contains preliminary information.

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342B–15		7C342B–20		7C342–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	100		71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	100		71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		3		ns

Shaded area contains preliminary information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		15		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		25		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	4.5		5		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	14		18		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	4		4		6		8		10		ns
t_{AWH}	Asynchronous Clock Input High Time[7]	5		7		11		12.5		15		ns
t_{AWL}	Asynchronous Clock Input Low Time[7, 20]	5		7		11		12.5		15		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		10		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	12		14		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	51.3		40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	71.4		55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	66.6		50		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	100		71.4		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	15		15		15		15		15		ns

Shaded area contains preliminary information.

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.

    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the lesser of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		3		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		3		4		6		6		9	ns
t_{EXP}	Expander Array Delay		8		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		8		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		5		5		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		5		10		11		13	ns
t_{RSU}	Register Set-Up TimeRelative to Clock Signal at Register	4		5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		1		1		3		4		4	ns
t_{RD}	Register Delay		1		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		1		1		3		4		4	ns
t_{CH}	Clock HIGH Time	4		6		8		10		12.5		ns
t_{CL}	Clock LOW Time	4		6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		6		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0		0		2		2		3	ns
t_{FD}	Feedback Delay		1		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	3		4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	3		4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		10		13		14		16		20	ns

Shaded area contains preliminary information.

Notes:

27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Military External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B-20		7C342B-25		7C342-30		7C342-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		32		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		42		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	12		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	24		29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4,7]	22		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4,7]	22		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	14		16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	50.0		34.5		27.7		22.2		MHz

Shaded area contains preliminary information.

Military External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342B–20		7C342B–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	66.6		55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		ns

Shaded area contains preliminary information.

Military External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–20		7C342B–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	18		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	4		6		8		10		ns
t_{AWH}	Asynchronous Clock Input High Time[7]	7		11		12.5		15		ns
t_{AWL}	Asynchronous Clock Input Low Time[7, 20]	7		11		12.5		15		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period $(1/(f_{MAXA4}))$[4]	14		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $(1/(t_{ACO1} + t_{AS1}))$[4, 22]	40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	71.4		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	71.4		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	15		15		15		15		ns

Shaded area contains preliminary information.

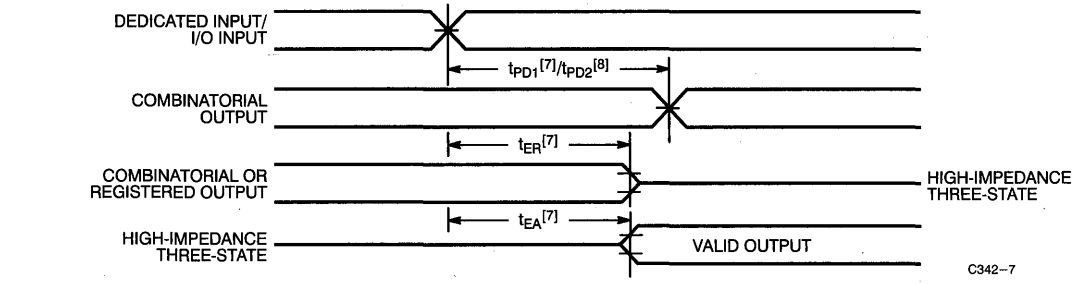
Military Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–20		7C342B–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		4		6		6		9	ns
t_{EXP}	Expander Array Delay		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		5		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		1		3		4		4	ns
t_{RD}	Register Delay		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		1		3		4		4	ns
t_{CH}	Clock HIGH Time	6		8		10		12.5		ns
t_{CL}	Clock LOW Time	6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0		2		2		3	ns
t_{FD}	Feedback Delay		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		13		14		16		20	ns

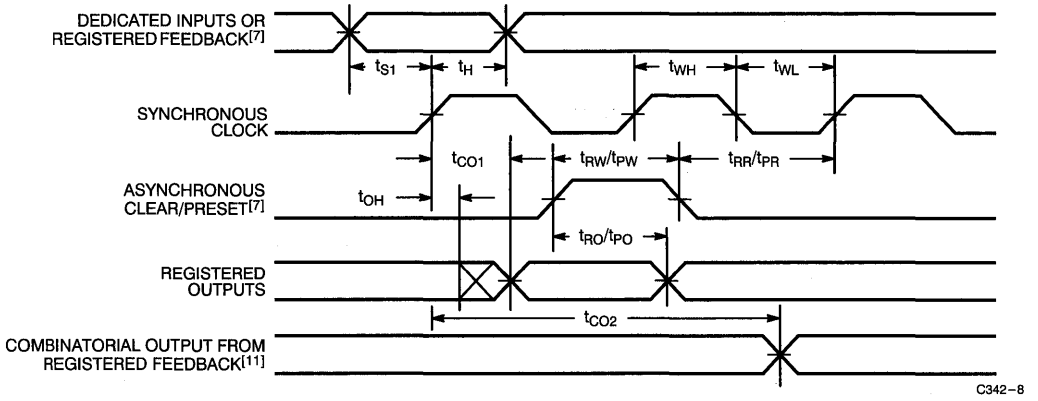
Shaded area contains preliminary information.

Switching Waveforms

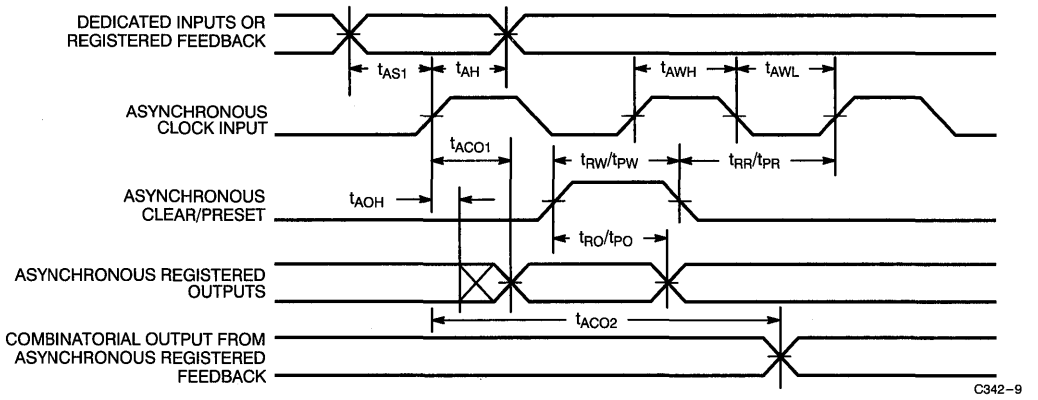
External Combinatorial



External Synchronous

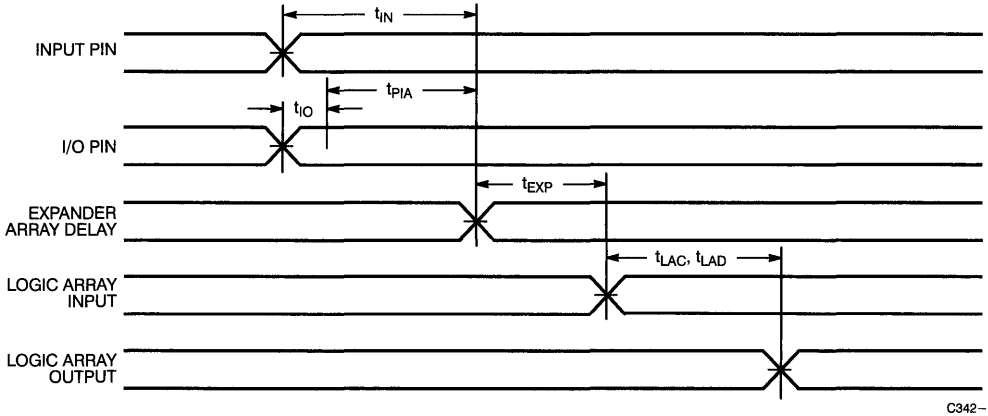


External Asynchronous



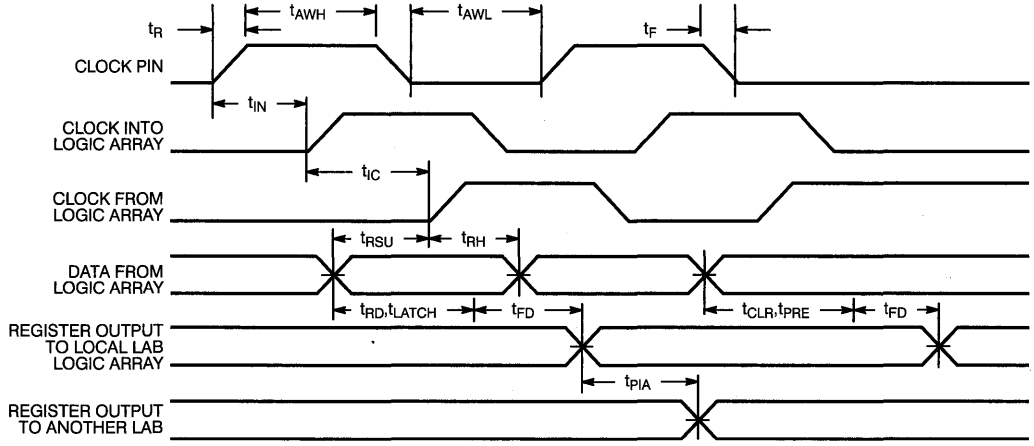
Switching Waveforms (continued)

Internal Combinatorial



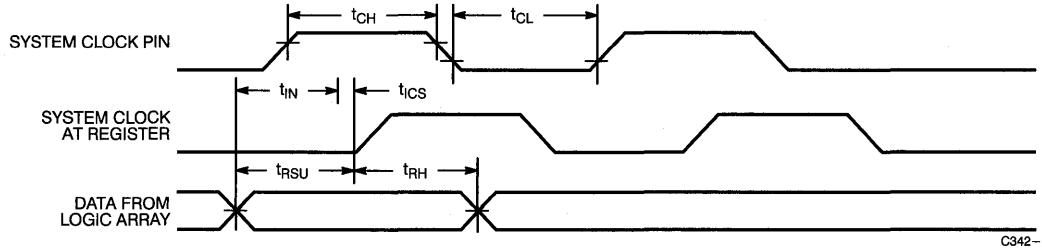
C342–10

Internal Asynchronous



C342–11

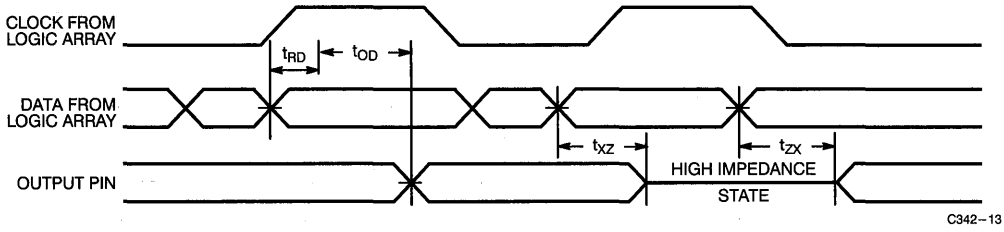
Internal Synchronous



C342–12

Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C342–25HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–25JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–25RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
30	CY7C342–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–30JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–30RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–30HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–30RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–30TMB	T91	68-Lead Windowed Cerquad Flatpack	
35	CY7C342–35HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–35JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–35RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–35HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–35RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–35TMB	T91	68-Lead Windowed Cerquad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C342B–15HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–15JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–15RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
20	CY7C342B–20HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–20JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–20RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–20HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–20RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–20TMB	T91	68-Lead Windowed Cerquad Flatpack	
25	CY7C342B–25HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–25RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–25TMB	T91	68-Lead Windowed Cerquad Flatpack	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{S2}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{WL}	7, 8, 9, 10, 11
t_{RO}	7, 8, 9, 10, 11
t_{PO}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{AWH}	7, 8, 9, 10, 11
t_{AWL}	7, 8, 9, 10, 11

Document #: 38–00119–E

CYPRESS SEMICONDUCTOR

CY7C343

64-Macrocell MAX® EPLD

Features

- **64 MAX macrocells in 4 LABs**
- **8 dedicated inputs, 24 bidirectional I/O pins**
- **Programmable interconnect array**
- **Available in 44-pin HLCC, PLCC**
- **Lowest power MAX device**

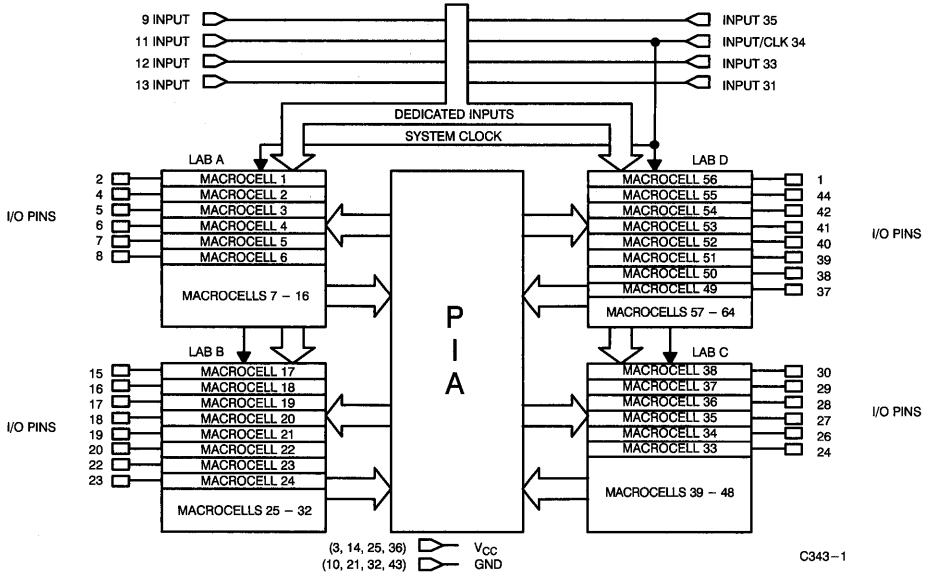
Functional Description

The CY7C343 is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343 contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Interconnect Array (PIA). There are 8 input pins, one of which doubles as a clock pin if needed. The CY7C343 also has 28 I/O pins, each connected to a macrocell (6 for LABs A and C, and 8 for LABs B and D). The remaining 36 macrocells are used for embedded logic.

The CY7C343 is excellent for a wide range of both synchronous and asynchronous applications.

Logic Block Diagram



Selection Guide

		7C343–20	7C343–25	7C343–30	7C343–35
Maximum Access Time (ns)		20	25	30	35
Maximum Operating Current (mA)	Commercial	135	135	135	135
	Military		225	225	225
	Industrial	225	225	225	225
Maximum Standby Current (mA)	Commercial	125	125	125	125
	Military		200	200	200
	Industrial	200	200	200	200

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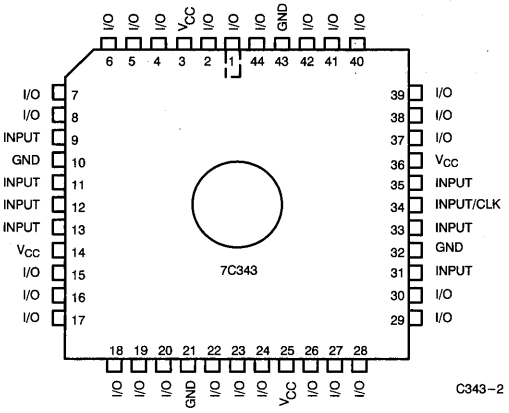
Pin Configuration

HLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... − 2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to +7.0V

DC Program Voltage 13.5V

Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	− 40°C to +85°C	5V ±10%
Military	− 55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		− 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		− 30	− 90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		125	mA
			Military/Industrial		200	mA
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 5]	Commercial		135	mA
			Military/Industrial		225	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. Measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.

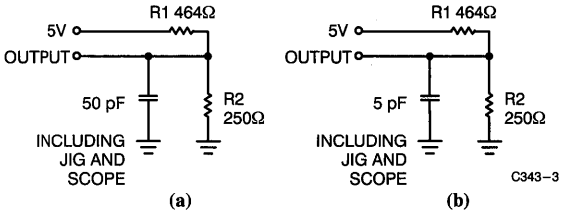
Capacitance[6]

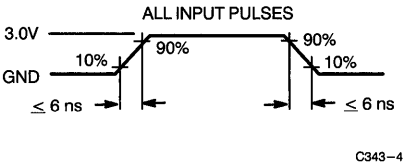
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

Notes:

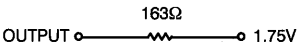
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by ensuring that internal signal skews or races are avoided. The result is simpler design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C343 may be easily determined using MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C343 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C343 contains circuitry to protect device pins from high static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AH})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest fre-

quency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C343.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

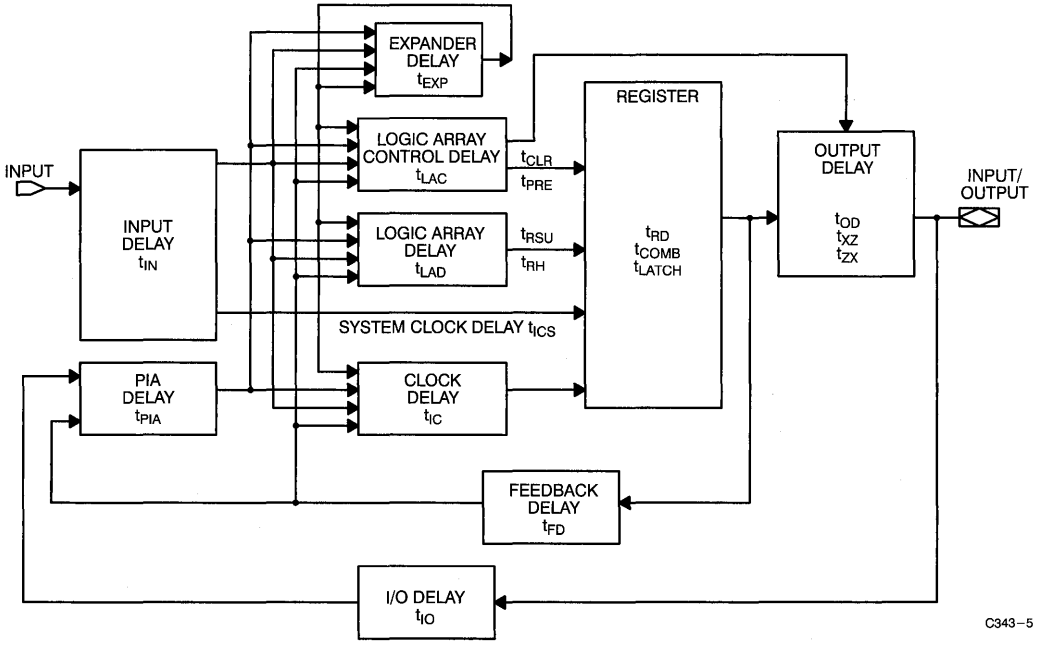


Figure 1. CY7C343 Internal Timing Model

External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description		CY7C343-20		CY7C343-25		CY7C343-30		CY7C343-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l & Ind		32		39		44		53	ns
		Mil				39		44		53	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l & Ind		30		37		44		55	ns
		Mil				37		44		55	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l & Ind		42		51		58		73	ns
		Mil				51		58		73	
t_{EA}	Input to Output Enable Delay[4,7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l & Ind		12		14		16		20	ns
		Mil				14		16		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l & Ind		25		30		35		42	ns
		Mil				30		35		42	
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7]	Com'l & Ind	12		15		20		25		ns
		Mil			15		20		25		
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7,12]	Com'l & Ind	24		30		35		42		ns
		Mil			30		35		42		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l & Ind	0		0		0		0		ns
		Mil			0		0		0		
t_{WH}	Synchronous Clock Input HIGH Time	Com'l & Ind	6		8		10		12.5		ns
		Mil			8		10		12.5		
t_{WL}	Synchronous Clock Input LOW Time	Com'l & Ind	6		8		10		12.5		ns
		Mil			8		10		12.5		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l & Ind	20		25		30		35		ns
		Mil			25		30		35		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l & Ind	20		25		30		35		ns
		Mil			25		30		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l & Ind	20		25		30		35		ns
		Mil			25		30		35		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		CY7C343-20 Min.	CY7C343-20 Max.	CY7C343-25 Min.	CY7C343-25 Max.	CY7C343-30 Min.	CY7C343-30 Max.	CY7C343-35 Min.	CY7C343-35 Max.	Unit
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l & Ind		3		3		3		5	ns
		Mil				3		3		5	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l & Ind	12		16		20		25		ns
		Mil			16		20		25		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l & Ind	41.6		34		27		22.2		MHz
		Mil			34		27		22.2		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	Com'l & Ind	66.7		55		43		33		MHz
		Mil			55		43		33		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[4, 16]	Com'l & Ind	83.3		62.5		50		40		MHz
		Mil			62.5		50		40		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[4, 17]	Com'l & Ind	83.3		62.5		50		40		MHz
		Mil			62.5		50		40		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l & Ind	3		3		3		3		ns
		Mil			3		3		3		
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l & Ind	20		25		30		35		ns
		Mil			25		30		35		

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input.
   If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local, originating within the same LAB.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics Over Operating Range[6]

Parameter	Description		CY7C343-20 Min.	CY7C343-20 Max.	CY7C343-25 Min.	CY7C343-25 Max.	CY7C343-30 Min.	CY7C343-30 Max.	CY7C343-35 Min.	CY7C343-35 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l & Ind		20		25		30		35	ns
		Mil				25		30		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l & Ind		32		40		46		55	ns
		Mil				40		46		55	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	Com'l & Ind	4		5		6		8		ns
		Mil			5		6		8		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	Com'l & Ind	15		20		25		30		ns
		Mil			20		25		30		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l & Ind	5		6		8		10		ns
		Mil			6		8		10		
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l & Ind	9		11		14		16		ns
		Mil			11		14		16		
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	Com'l & Ind	7		9		11		14		ns
		Mil			9		11		14		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l & Ind		13		15		18		22	ns
		Mil				15		18		22	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAXA4}$)[4]	Com'l & Ind	16		20		25		30		ns
		Mil			20		25		30		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[4, 22]	Com'l & Ind	41.6		33		27		23		MHz
		Mil			33		27		23		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	Com'l & Ind	62.5		50		40		33		MHz
		Mil			50		40		33		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l & Ind	50		40		33		28		MHz
		Mil			40		33		28		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l & Ind	62.5		50		40		33		MHz
		Mil			50		40		33		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l & Ind	15		15		15		15		ns
		Mil			15		15		15		

Notes:

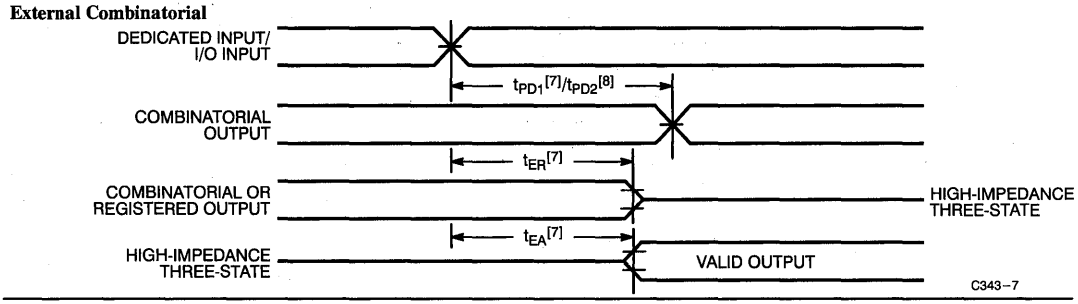
19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.

Internal Switching Characteristics Over Operating Range[1]

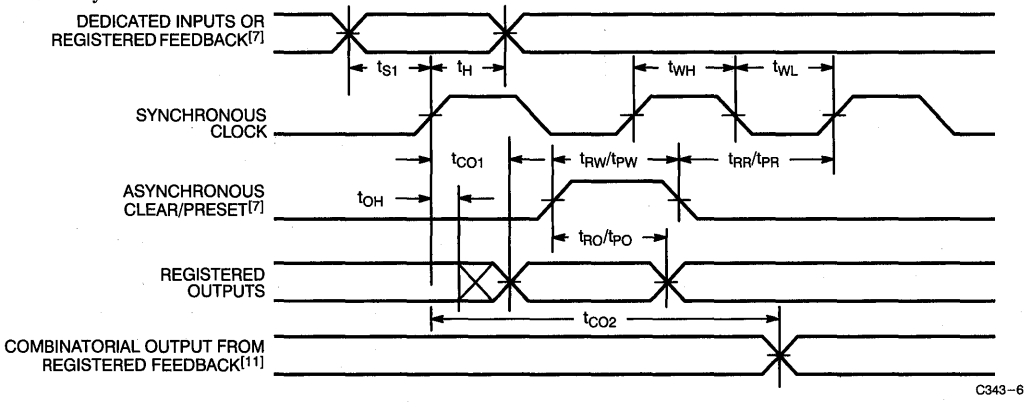
Parameter	Description		CY7C343-20 Min.	CY7C343-20 Max.	CY7C343-25 Min.	CY7C343-25 Max.	CY7C343-30 Min.	CY7C343-30 Max.	CY7C343-35 Min.	CY7C343-35 Max.	Unit
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l & Ind		4		5		7		9	ns
		Mil				5		7		9	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l & Ind		4		5		5		7	ns
		Mil				5		5		7	
t_{EXP}	Expander Array Delay	Com'l & Ind		10		12		14		20	ns
		Mil				12		14		20	
t_{LAD}	Logic Array Data Delay	Com'l & Ind		10		12		14		16	ns
		Mil				12		14		16	
t_{LAC}	Logic Array Control Delay	Com'l & Ind		8		10		12		13	ns
		Mil				10		12		13	
t_{OD}	Output Buffer and Pad Delay	Com'l & Ind		4		5		5		6	ns
		Mil				5		5		6	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l & Ind		8		10		11		13	ns
		Mil				10		11		13	
t_{XZ}	Output Buffer Disable Delay	Com'l & Ind		8		10		11		13	ns
		Mil				10		11		13	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l & Ind	4		6		8		10		ns
		Mil			6		8		10		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l & Ind	4		6		8		12		ns
		Mil			6		8		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l & Ind		2		3		4		4	ns
		Mil				3		4		4	
t_{RD}	Register Delay	Com'l & Ind		1		1		2		2	ns
		Mil				1		2		2	
t_{COMB}	Transparent Mode Delay[28]	Com'l & Ind		2		3		4		4	ns
		Mil				3		4		4	
t_{CH}	Clock HIGH Time	Com'l & Ind	6		8		10		12.5		ns
		Mil			8		10		12.5		
t_{CL}	Clock LOW Time	Com'l & Ind	6		8		10		12.5		ns
		Mil			8		10		12.5		
t_{IC}	Asynchronous Clock Logic Delay	Com'l & Ind		12		14		16		18	ns
		Mil				14		16		18	
t_{ICS}	Synchronous Clock Delay	Com'l & Ind		2		2		2		3	ns
		Mil				2		2		3	
t_{FD}	Feedback Delay	Com'l & Ind		1		1		1		2	ns
		Mil				1		1		2	
t_{PRE}	Asynchronous Register Preset Time	Com'l & Ind		4		5		6		7	ns
		Mil				5		6		7	
t_{CLR}	Asynchronous Register Clear Time	Com'l & Ind		4		5		6		7	ns
		Mil				5		6		7	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l & Ind	4		5		6		7		ns
		Mil			5		6		7		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l & Ind	4		5		6		7		ns
		Mil			5		6		7		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l & Ind		12		14		16		20	ns
		Mil				14		16		20	

Switching Waveforms

External Combinatorial



External Synchronous

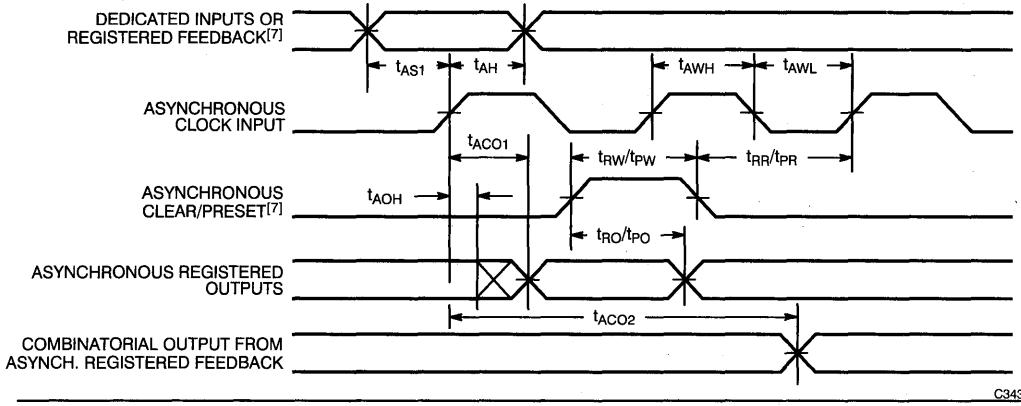


Notes:

23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS1})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

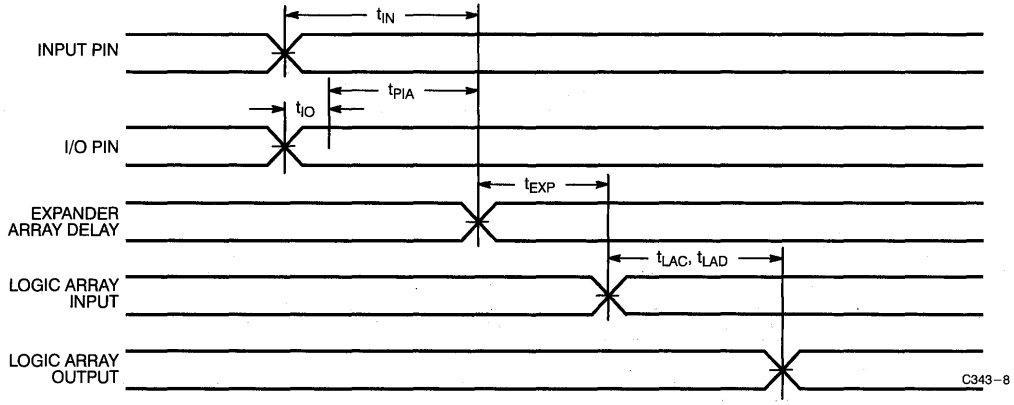
Switching Waveforms (continued)

External Asynchronous



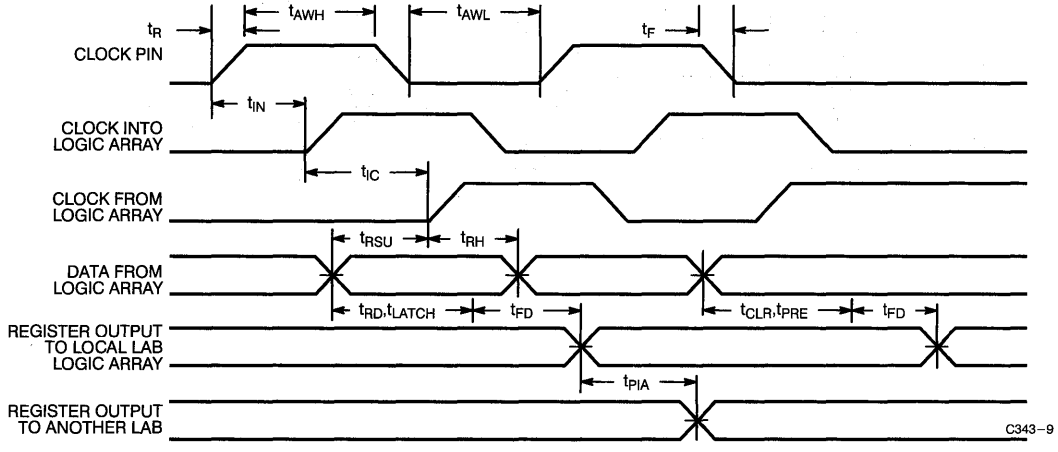
C343-10

Internal Combinatorial



C343-8

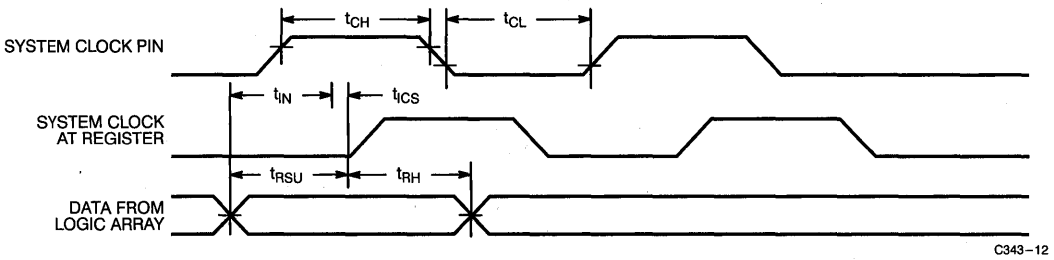
Internal Asynchronous



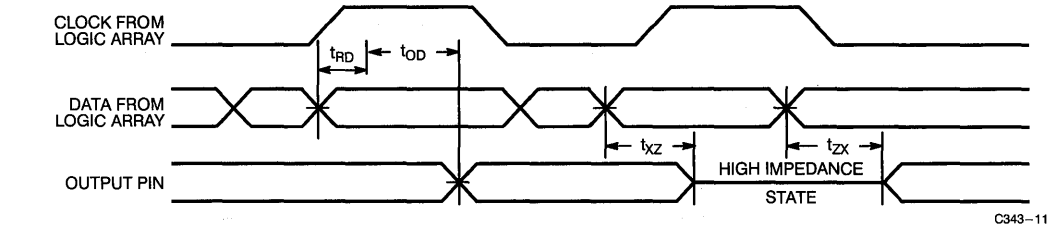
C343-9

Switching Waveforms (continued)

Internal Synchronous



Output Mode



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C343-20HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343-20JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
25	CY7C343-25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343-25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343-25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
30	CY7C343-30HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343-30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343-30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
35	CY7C343-35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343-35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343-35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38–00128–E

CYPRESS SEMICONDUCTOR

CY7C344

32-Macrocell MAX® EPLD

Features

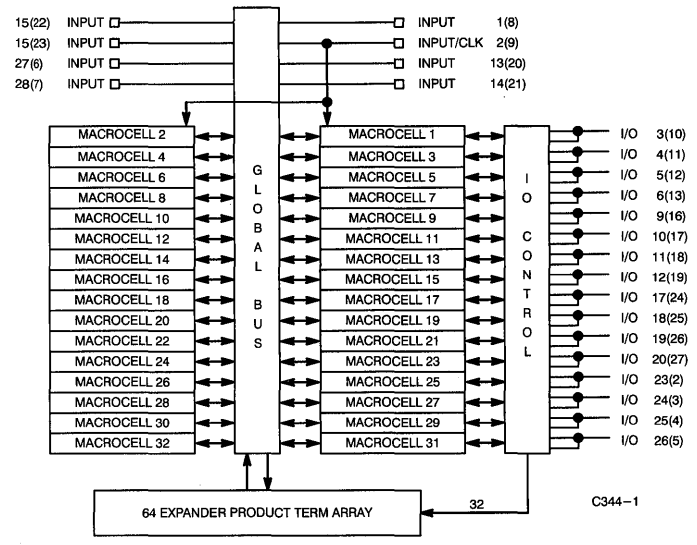
- **High-performance, high-density replacement for TTL, 74HC, and custom logic**
- **32 macrocells, 64 expander product terms in one LAB**
- **8 dedicated inputs, 16 I/O pins**
- **28-pin 300-mil DIP, cerDIP or 28-pin HLCC, PLCC package**

Functional Description

Available in a 28-pin 300-mil DIP or windowed J-leaded ceramic chip carrier (HLCC), the CY7C344 represents the densest EPLD of this size. Eight dedicated inputs and 16 bidirectional I/O pins communicate to one logic array block. In the CY7C344 LAB there are 32 macrocells and 64 expander product terms. When an I/O macrocell is used as an input, two expanders are used to create an input path. Even if all of the I/O pins are driven by macrocell registers, there are still 16 "buried" registers available. All inputs, macrocells, and I/O pins are interconnected within the LAB.

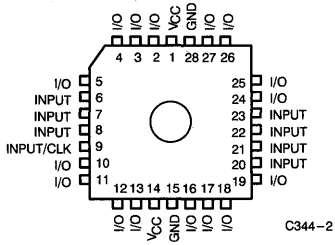
The speed and density of the CY7C344 makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344 to replace multichip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

Logic Block Diagram[1]

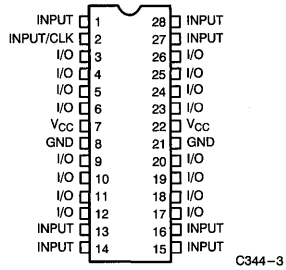


Pin Configurations

HLCC
Top View



CerDIP
Top View



Selection Guide

		7C344-20	7C344-25	7C344-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	200	200	200
	Military		220	220
	Industrial	220	220	
Maximum Standby Current (mA)	Commercial	150	150	150
	Military		170	170
	Industrial	170	170	

Note:
1. Figures in () are for J-leaded packages.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... − 2.0V to +7.0V

Maximum Power Dissipation ..... 1500 mW

DC V_{CC} or GND Current ..... 500 mA

Static Discharge Voltage (per MIL−STD−883, Method 3015) ..... >2001V

DC Output Current, per Pin ..... − 25 mA to +25 mA

DC Input Voltage[2] ..... − 3.0V to +7.0V

DC Program Voltage ..... −13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	− 40°C to +85°C	5V ±10%
Military	− 55°C to +125°C (Case)	5V ±10%

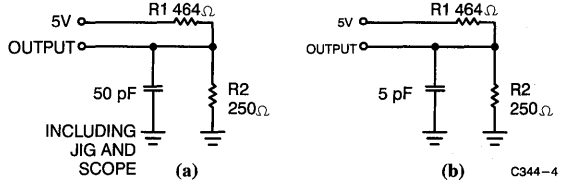
Electrical Characteristics Over the Operating Range[3]

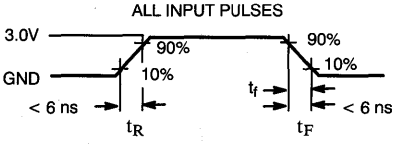
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		− 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]		− 30	− 90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 6]	Commercial		150	mA
			Military/Industrial		170	mA
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 6]	Commercial		200	mA
			Military/Industrial		220	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Capacitance

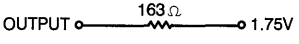
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

AC Test Loads and Waveforms[7]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Notes:

2. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Typical values are for T_A = 25°C and V_{CC} = 5V.
4. Guaranteed but not 100% tested.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Measured with device programmed as a 16-bit counter.
7. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

Timing Delays

Timing delays within the CY7C344 may be easily determined using MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C344 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344 contains circuitry to protect device pins from high-static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data-path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If ($t_{AS2} + t_{AH}$) is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data-path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C344.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

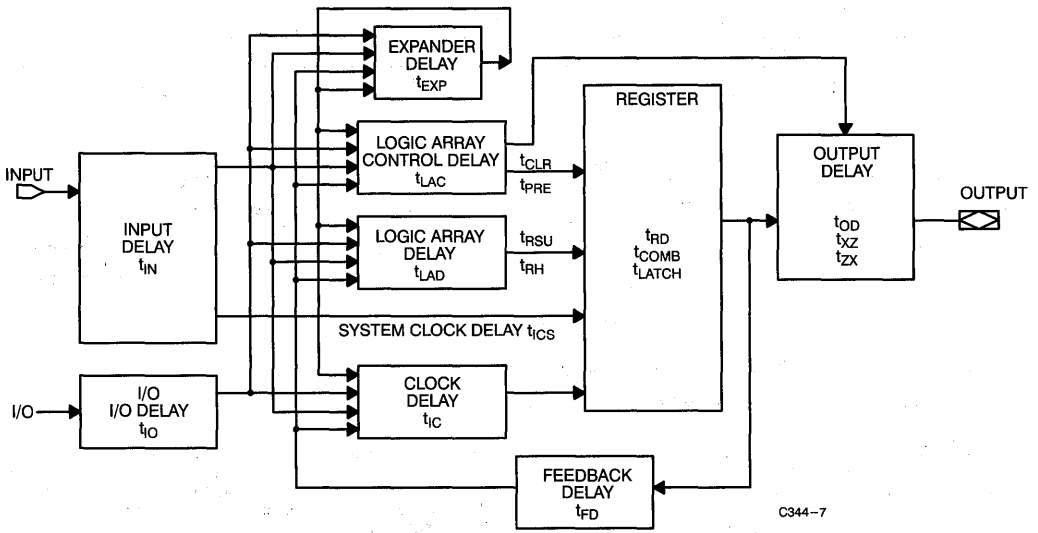


Figure 1. CY7C344 Timing Model

External Synchronous Switching Characteristics[7] Over Operating Range

Parameter	Description		CY7C344–20		CY7C344–25		CY7C344–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[9]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l & Ind		30		40			ns
		Mil				40		55	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l & Ind		30		40			ns
		Mil				40		55	
t_{EA}	Input to Output Enable Delay[4]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{ER}	Input to Output Disable Delay[4]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l & Ind		12		15			ns
		Mil				15		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l & Ind		22		29			ns
		Mil				29		37	
t_S	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input	Com'l & Ind	12		15				ns
		Mil			15		21		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l & Ind	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input HIGH Time[4]	Com'l & Ind	7		8				ns
		Mil			8		10		
t_{WL}	Synchronous Clock Input LOW Time[4]	Com'l & Ind	7		8				ns
		Mil			8		10		
t_{RW}	Asynchronous Clear Width[4]	Com'l & Ind	20		25				ns
		Mil			25		35		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l & Ind	20		25				ns
		Mil			25		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{PW}	Asynchronous Preset Width[4]	Com'l & Ind	20		25				ns
		Mil			25		35		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l & Ind		20		25			ns
		Mil				25		35	

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		CY7C344-20 Min.	CY7C344-20 Max.	CY7C344-25 Min.	CY7C344-25 Max.	CY7C344-35 Min.	CY7C344-35 Max.	Unit
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l & Ind		4		7			ns
		Mil				7		13	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l & Ind	14		16				ns
		Mil			16		20		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l & Ind	41.6		33.3				MHz
		Mil			33.3		24.3		
f_{MAX2}	Maximum Frequency with Internal Only Feedback ($1/(t_{CF} + t_S)$)[4, 15]	Com'l & Ind	62.5		45.4				MHz
		Mil			45.4		29.4		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l & Ind	71.4		62.5				MHz
		Mil			62.5		47.6		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL} + t_{WH})$[4, 17]	Com'l & Ind	71.4		62.5				MHz
		Mil			62.5		50.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l & Ind	3		3				ns
		Mil			3		3		

Notes:

8. This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
9. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
10. This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
12. This specification is a measure of the delay from synchronous register clock input to internal feedback of the register output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. This parameter is tested periodically by sampling production material.
13. This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register set-up time, t_S, is the minimum internal period for an internal state machine configuration. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO1}$. This specification assumes no expander logic is used. This parameter is tested periodically by sampling production material.
16. This frequency indicates the maximum frequency at which the device may operate in data-path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
17. This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics Over Operating Range[7]

Parameter	Description		CY7C344–20 Min.	CY7C344–20 Max.	CY7C344–25 Min.	CY7C344–25 Max.	CY7C344–35 Min.	CY7C344–35 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay	Com'l & Ind		20		25			ns
		Mil				25		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l & Ind		30		37			ns
		Mil				37		49	
t_{AS}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l & Ind	9		12				ns
		Mil			12		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l & Ind	9		12				ns
		Mil			12		17.5		
t_{AWH}	Asynchronous Clock Input HIGH Time[4, 20]	Com'l & Ind	7		9				ns
		Mil			9		15		
t_{AWL}	Asynchronous Clock Input LOW Time[4]	Com'l & Ind	9		11				ns
		Mil			11		15		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l & Ind		18		21			ns
		Mil				21		27	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)[4]	Com'l & Ind	16		20				ns
		Mil			20		30		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS})$[4, 22]	Com'l & Ind	34.4		27				MHz
		Mil			27		20		
f_{MAXA2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$ or $1/(t_{AWH} + t_{AWL})$[4, 23]	Com'l & Ind	37		30.3				MHz
		Mil			30.3		23.8		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l & Ind	50		40				MHz
		Mil			40		28.5		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l & Ind	62.5		50				MHz
		Mil			50		33.3		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l & Ind	15		15				ns
		Mil			15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register set-up time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. This parameter is tested periodically by sampling production material.
22. This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$. This specification assumes no expander logic is utilized. This parameter is tested periodically by sampling production material.
24. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. This frequency is least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS} + t_{AH})$, or $1/t_{ACO1}$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data-path mode. Assumes no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input or an I/O pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

Typical Internal Switching Characteristics Over Operating Range[7]

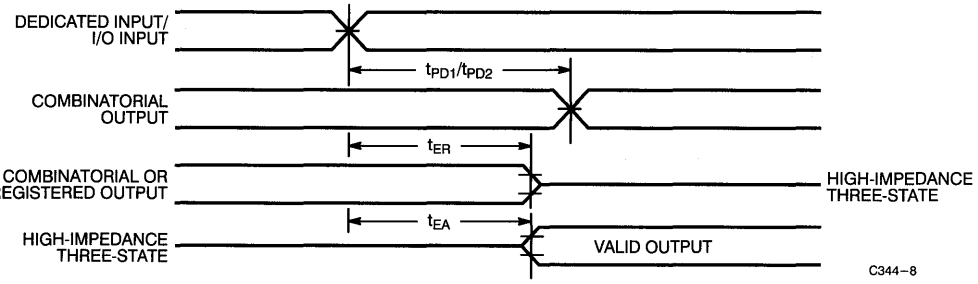
Parameter	Description		CY7C344–20 Min.	CY7C344–20 Max.	CY7C344–25 Min.	CY7C344–25 Max.	CY7C344–35 Min.	CY7C344–35 Max.	Unit
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l & Ind		5		7			ns
		Mil				7		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l & Ind		5		7			ns
		Mil				7		11	
t_{EXP}	Expander Array Delay	Com'l & Ind		10		15			ns
		Mil				15		20	
t_{LAD}	Logic Array Data Delay	Com'l & Ind		9		10			ns
		Mil				10		11	
t_{LAC}	Logic Array Control Delay	Com'l & Ind		7		7			ns
		Mil				7		7	
t_{OD}	Output Buffer and Pad Delay	Com'l & Ind		5		5			ns
		Mil				5		8	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l & Ind		8		11			ns
		Mil				11		12	
t_{XZ}	Output Buffer Disable Delay	Com'l & Ind		8		11			ns
		Mil				11		12	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l & Ind	5		8				ns
		Mil			8		11		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l & Ind	9		12				ns
		Mil			12		15		
t_{LATCH}	Flow-Through Latch Delay	Com'l & Ind		1		3			ns
		Mil				3		5	
t_{RD}	Register Delay	Com'l & Ind		1		1			ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l & Ind		1		3			ns
		Mil				3		5	
t_{CH}	Clock HIGH Time	Com'l & Ind	7		8				ns
		Mil			8		9		
t_{CL}	Clock LOW Time	Com'l & Ind	7		8				ns
		Mil			8		9		
t_{IC}	Asynchronous Clock Logic Delay	Com'l & Ind		8		10			ns
		Mil				10		12	
t_{ICS}	Synchronous Clock Delay	Com'l & Ind		2		3			ns
		Mil				3		5	
t_{FD}	Feedback Delay	Com'l & Ind		1		1			ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l & Ind		6		9			ns
		Mil				9		12	
t_{CLR}	Asynchronous Register Clear Time	Com'l & Ind		6		9			ns
		Mil				9		12	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l & Ind	5		7				ns
		Mil			7		9		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l & Ind	5		7				ns
		Mil			7		9		

Notes:

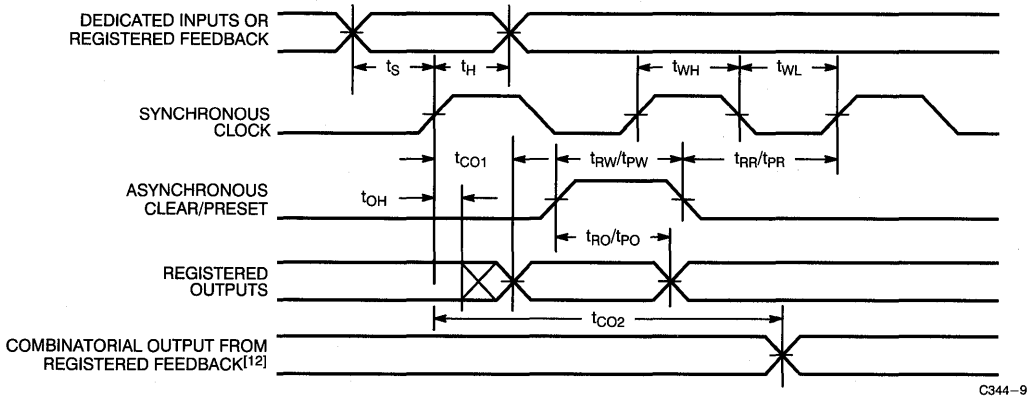
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Switching Waveforms

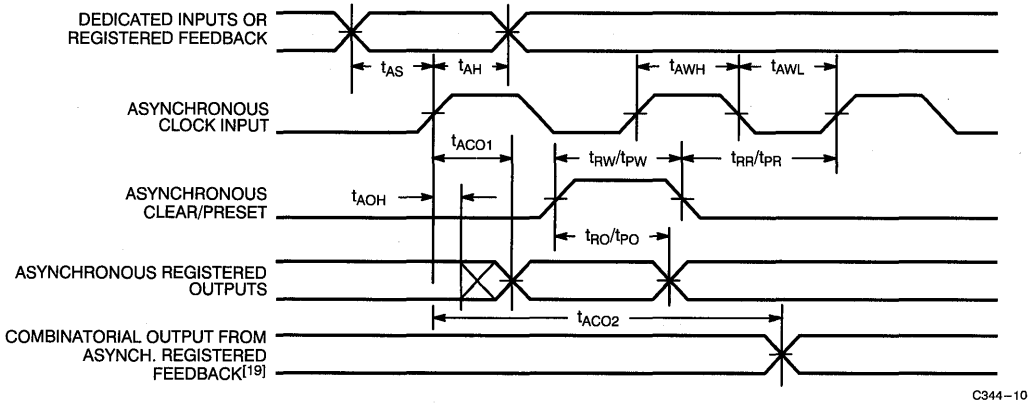
External Combinatorial



External Synchronous

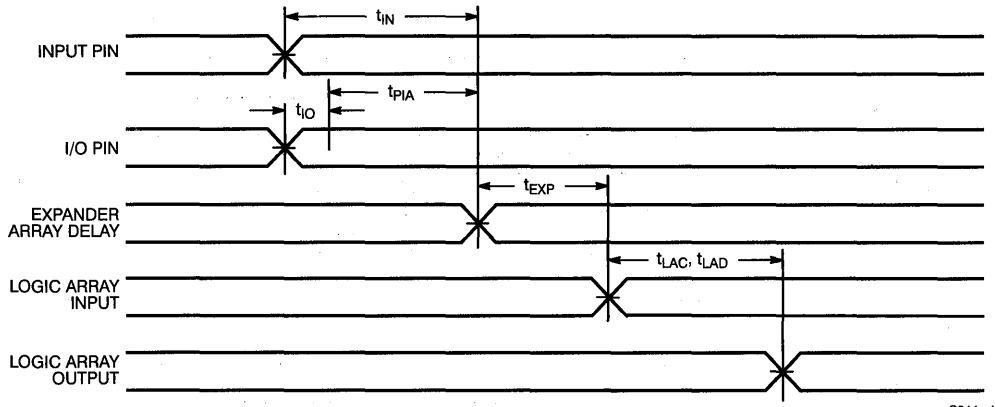


External Asynchronous



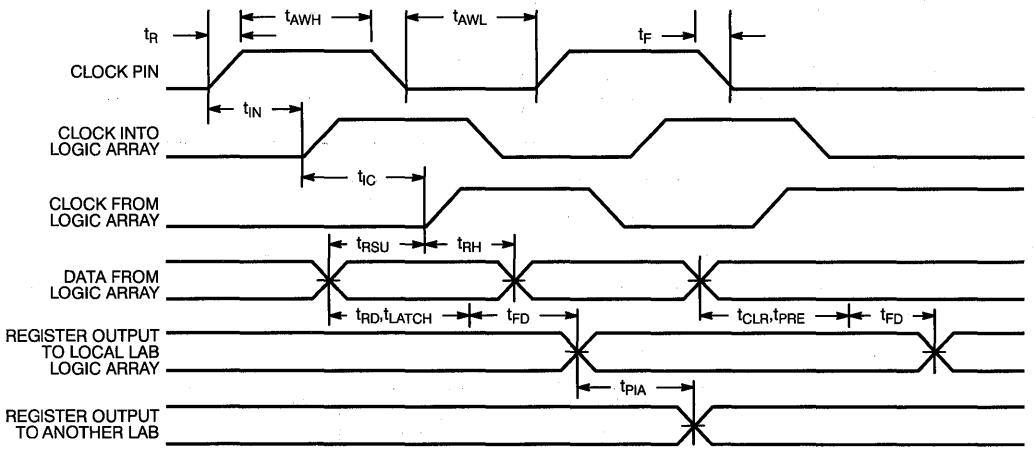
Switching Waveforms (continued)

Internal Combinatorial



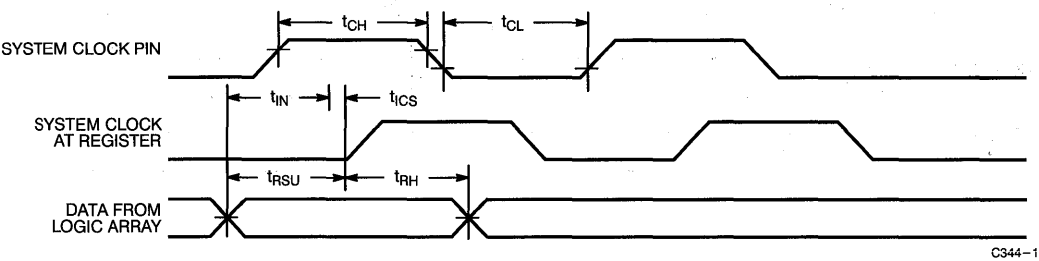
C344-11

Internal Asynchronous



C344-12

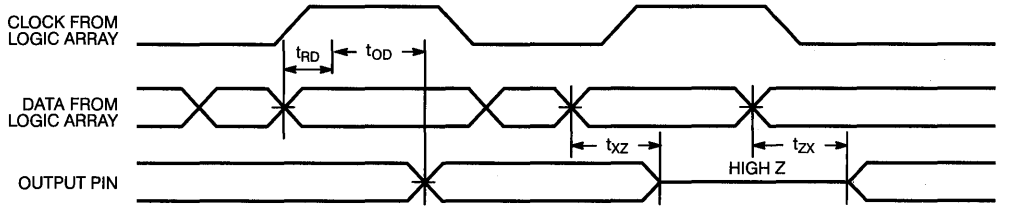
Internal Synchronous (Input Path)



C344-13

Switching Waveforms (continued)

Internal Synchronous (Output Path)



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C344-20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344-20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344-20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344-20WC/WI	W22	28-Lead Windowed CerDIP	
25	CY7C344-25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344-25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344-25PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344-25WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344-25HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344-25WMB	W22	28-Lead Windowed CerDIP	
35	CY7C344-35HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344-35WMB	W22	28-Lead Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38-00127-C

CYPRESS SEMICONDUCTOR

CY7C361

Ultra High Speed State Machine EPLD

Features

- **High speed: 125-MHz state machine output generation**
  - **Token passing**
  - **Multiple, concurrent processes**
  - **Multiway branch or join**
- **One clock with programmable clock doubler**
- **Programmable miser bits for power savings**
- **8 to 12 inputs with input macrocells**
  - **Metastability hardened: 10-year MBTF**
  - **0, 1, or 2 input registers**
  - **3 programmable clock enables**
- **32 synchronous state macrocells**
- **10 to 14 outputs**
  - **Skew-controlled OR output array**
  - **Outputs are sum of states like PLA**
- **Security fuse**
- **Available in 28-pin slimline DIP and 28-pin HLCC**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Product Characteristics

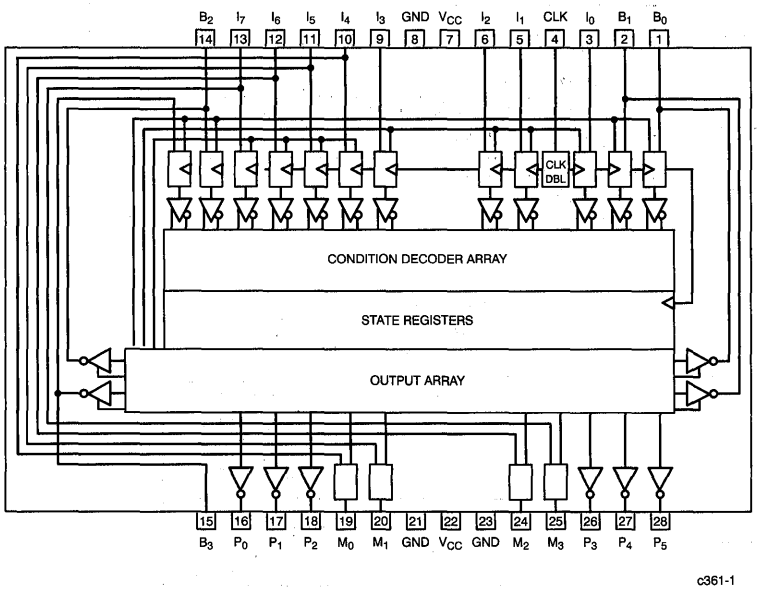
The CY7C361 is a CMOS erasable, programmable logic device (EPLD) with very high speed sequencing capabilities.

Applications include high-speed cache and I/O subsystems control, control of high-speed numeric processors, and high-speed arbitration between synchronous or asynchronous systems.

A programmable on-board clock doubler allows the device to operate at 125 MHz internally based on a 62.5-MHz input clock reference. The clock doubler is not a phase-locked loop. It produces an internal pulse on each edge of the external clock. The length of each internal pulse is determined by the intrinsic delays within the CY7C361. When the doubler is enabled, all macrocells in the CY7C361 are referenced to the doubled clock. If the clock doubler is disabled, a 125-MHz input clock can be connected to pin 4, and it will be used as a clock to all macrocells.

The CY7C361 has two arrays, similar to those in a PLA except that the registers are placed between the two arrays so that the long feedback path of the PLA is eliminated.

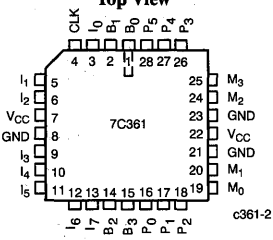
Logic Block Diagram



c361-1

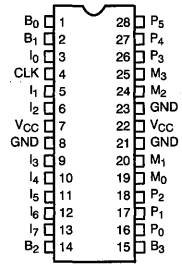
Pin Configurations

HLCC
Top View



c361-2

DIP
Top View



c361-3

Selection Guide

Generic Part Number	I_{CC} mA at f_{MAX}		f_{MAX} MHz		t_{IS} ns		t_{CO} ns	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
CY7C361–125	200		125.0		2		15	
CY7C361–100	200	200	100.0	100.0	3	3	19	19
CY7C361–83			83.3	83.3	5	5	23	23

Product Characteristics (continued)

In the CY7C361, the state information is contained in 32 state macrocells sandwiched between the input and output arrays. The current state information is fed back fast enough to achieve the 125-MHz operating frequency. These state macrocells also have serial connections that allow state machines to be built using a token-passing methodology similar to one hot encoding, but with the ability to support multiple active states at any given time.

The output array performs an OR function over the state macrocell outputs, allowing the control signals of the state machine to be produced directly. The signals from the output array are connected to the 14 device outputs (4 of which are bidirectional). In addition there are 3 sum terms that act as clock enables to the 3 groups of input macrocells. There are also 4 sum term output enables for the 4 bidirectional pins.

Input Macrocells

The CY7C361 has 12 input macrocells, shown in *Figure 1*. Each macrocell can be configured to have 0, 1, or 2 registers in the path of the input data. In the configuration where there is no input register, the set-up time required is the longest, because it includes the propagation delay through the input array plus the state register set-up time. In the single-registered configuration the set-up time is less than half of the unregistered case. The double-registered configuration is used to synchronize asynchronous inputs without causing metastable events.

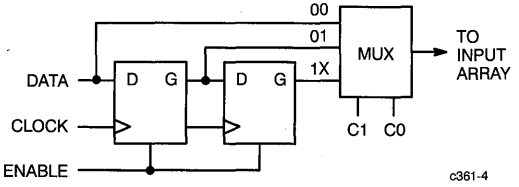


Figure 1. Input Macrocell

Input Register Enables

The input macrocells are divided into 3 groups of 4 macrocells each. Each of these groups has a register clock enable coming from the output array. The assignment of enable signal node numbers to input macrocells is as follows:

Input Nodes	Enable Node
3, 5, 6, 9	29
10, 11, 12, 13	30
1, 2, 14, 15	31

When the enable node is true, data is clocked into the registers of the input macrocells on the rising edge of the internal global clock.

Metastability Immunity

A high level of metastable immunity is afforded in the double-registered configuration. The CY7C361 registers are done in fast CMOS and they resolve inputs in a minimal amount of time. With all inputs switching at maximum frequency, one metastable event capable of violating the set-up time of a subsequent register occurs every 10 years. The probability of failure in a configured state machine is much lower than this calculation suggests, because there are more registers in the device and thus more decision time is allowed. No state machine failures due to metastable phenomena will be observed if the maximum frequency and double-registered operation frequency are used. This makes the CY7C361 ideally suited for constructing state machines requiring arbitration. For more information on metastability, refer to the "Are Your PLDs Metastable?" application note in the *Cypress Applications Handbook*.

Input Array

The input array is based on the condition decoder, shown in *Figure 2*. In a conventional PLA or PLD device, only PRODUCT1 would be present in the first array and the output and the feedback would be encoded by a second programmable or fixed or array. The speed of state machines is limited mainly by the feedback path.

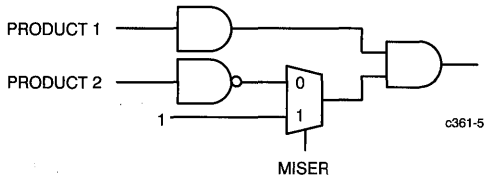


Figure 2. Condition Decoder

The condition decoder of the CY7C361 forms a product of a product and a sum over the input field. (The sum term is obtained by inverting the inputs to PRODUCT2.) Since there is immediate feedback information in the input field, multiway fork and join operations can be performed using this type of condition decoder. In other words, the condition decoder is used to control or gate the token being passed from macrocell to macrocell. In contrast, a traditional PLD or PLA requires more logic because the array is used to encode the states. In the CY7C361, state transitions can be made in half the time because there is no "state encoding" delay.

Each condition decoder has a miser bit in its sum term path. If the term is not used, the miser bit is automatically programmed. The miser bit completely disconnects the product term and replaces it with a logic HIGH. This results in a power savings.

The input array has 41 condition decoders: one global reset decoder, 8 local reset decoders, and 32 macrocell decoders. The array has 44 true/complement input pairs, 88 inputs total.

For speed reasons, the feedback signals are segmented. This means that for each group of 8 macrocells, 2 have global feedback, 2 have intermediate feedback to 16 of the 32 macrocells, and 4 have local feedback within their group of 8 macrocells only. Segmenting the feedback reduces the number of inputs per decoder to 56. Because the CY7C361 utilizes token passing, a large state machine will be effectively broken down into several smaller machines using 4 or less macrocells. The global and intermediate feedback is used to communicate between these smaller machines, and the local feedback is used within the smaller machines. For more information on the hot state encoding or token-passing design methodology, refer to the application notes titled "State Machine Design Considerations and Methodologies" and "Understanding the CY7C361" in the *Cypress Applications Handbook*.

State Machine Macrocells

The CY7C361 has 32 state macrocells. The state macrocells each have a single condition decode and share a common clock and global reset condition. The global reset is synchronous, and it lasts for two internal clock cycles. For each group of four state macrocells, there is a synchronous local reset condition.

All 32 of the macrocells are "daisy-chained." Each has a C_IN input that is connected to the C_OUT output of the previous macro-

cell, as shown in *Figure 3*. Configuration bit C2 is used in all state macrocells to select C_IN to be active (C2=0) or inactive (C2=1).

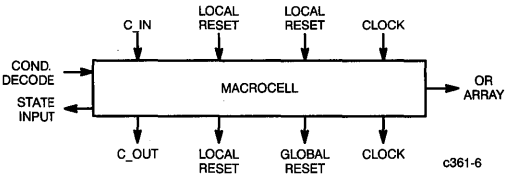
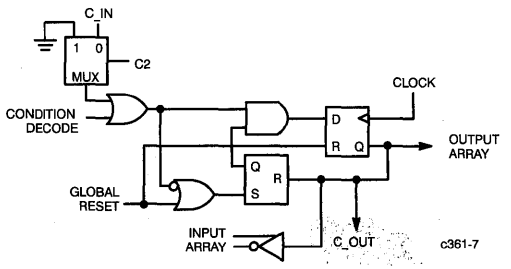


Figure 3. CY7C361 Macrocell

For the topmost macrocell (node 32), the C2 bit is used to specify a reset option. If the bit is 0, then the C_IN for this macrocell will be true (1). If the C2 bit is 1, then the C_IN for the macrocell will be false (0).

There are three state macrocell configurations: START, TOGGLE, and TERMINATE. The purpose of the START configuration is to create a "token" based on the condition decode. The TOGGLE configuration is used for building counters. The TERMINATE configuration is used to insert wait states in a process. It captures a token and holds it until a condition tells it to terminate the token.

Figure 4 shows a state macrocell in the START configuration. This configuration synchronously creates a token if C_IN or the condition decode is a logic HIGH. The token is represented by a true output on the macrocell register going to the output array and back as feedback to the input array. A machine implemented in the CY7C361 will consist of multiple machines or processes running concurrently, each with zero, one or more tokens active at any given time. Put another way, each state macrocell in the CY7C361 can be thought of as a line of microcode that can execute concurrently.



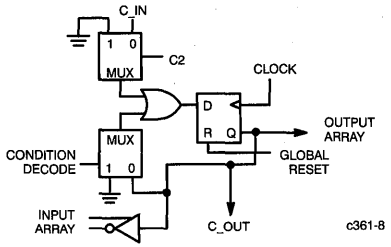
C1,C0 = 0,0: START

Figure 4. Start Configuration

In addition to the main register going to the array, there is an R-S latch in the feedback path that is used to convert the input condition to a pulse.

In operation, the START macrocell starts from a reset condition (output array input = FALSE). When a condition decode "fires" or a token is carried in (C_IN), the register output (Q going to the array) goes true for exactly one cycle. The OR of the condition decode and the C_IN must go FALSE before the START configuration can fire again. Local resets have no effect on this configuration.

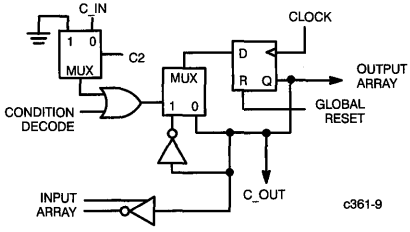
The TERMINATE macrocell (see *Figure 5*) captures a token via the C_IN path. The token is then held in the state register until the condition decoder fires, which causes the token to be terminated. Another way of saying this is that the TERMINATE macrocell is like a synchronous SR flip-flop. It is set by C_IN and reset by the condition decoder. Local resets have no effect on this configuration.



C1,C0 = 0,1: TERMINATE

Figure 5. Terminate Configuration

The TOGGLE macrocell (see *Figure 6*) operates like a T-type flip-flop. If C_IN or the condition decode is asserted, the state register will toggle on every rising edge of the internal clock. If neither the C_IN nor the condition decoder are asserted, the state register will retain its current state. The TOGGLE configuration is used to build counters. A local reset condition will synchronously reset the state register in this configuration.



C1,C0 = 1,0: TOGGLE

Figure 6. Toggle Configuration

The Output Array

The output array is an OR-based array. The array inputs are the LOW-asserted outputs of the 32 state macrocells. There are five types of array outputs. The first type is the three clock enables for the input macrocells. Each enable is a programmable OR of asserted state macrocells; when one of the connected macrocells is asserted, the clock is enabled. Next are the four output enables of the bidirectional I/O pins. Again, the output enables are a programmable OR of the connected asserted state macrocells; when one of the connected macrocells is asserted, the output is enabled. The third type of array output is the "pure" device output. These six outputs are a functional OR of the Low-asserted outputs of the state registers. Next is the output path of the four bidirectional I/O pins, which is identical to that of the "pure" outputs. The last type of array output is the Mealy output macrocell. The CY7C361 has four of these outputs; they can be used as a fast combinatorial out-

put. The three device outputs are pictured in *Figure 7*. Note that the Mealy output is the only one that is configurable.

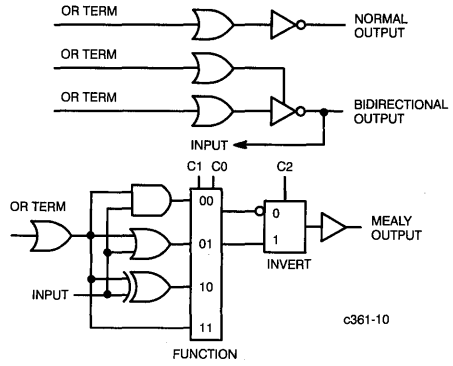


Figure 7. Output Configurations

In order to reduce output skew, the CY7C361 output array contains a set of self-timed latches in the output array path. These latches are controlled by an internal clock that has a delay equal to the worst-case path through the output array. While this delayed internal clock is LOW, the output array data is latched. When the delayed internal clock is HIGH, the latches become transparent, and the outputs change. These latches are the reason why the t_{CO} max is 15 ns with respect to the state registers, but the part can change its outputs every 7.5 ns. Since these latches cannot be accessed by the user, they have been left off of the block diagram.

The normal output signal from the device is a boolean sum of a subset of the state macrocell outputs. The subset selection is programmed into the output array. The number of state machines in the device, and the output mappings of each are determined by the user. The architecture is thus "horizontally divisible" and offers advantages in coding efficiency and event response time over the non-divisible architectures found in most PLA and sequencer implementations.

An output pin is normally LOW-asserted. The output gate performs an OR function over the flip-flop outputs of the state macrocells. The OR function includes only the outputs that are programmed to be connected to the OR line in the output array. When none of the connected state macrocell flip-flops are in the true or set condition, the output is HIGH, or deasserted. If any connected macrocell flip-flop is asserted (true) then the OR gate function is true and the output pin is LOW.

Forcing a false condition is easily accomplished by disconnecting all of the state macrocells from the OR line. To force a true condition, the OR line is connected only to node 73, which is labeled as V_{CC} in the block diagram. Any OR line connected to this node will be forced permanently true, which will cause any normal output to always be LOW.

The bidirectional outputs are I/O pins that may be used as either inputs or outputs. Under state machine control, these pins may be three-stated and used as inputs or outputs depending on how the OE term is programmed. If the OE is connected to node 73, the pin will always function as an output.

The Mealy outputs are designed to implement the fastest possible path between a device input and an output. Functions are available that combine the OR term and a specific input signal. These functions, XOR, AND, and OR, coupled with output polarity control are useful for data strobes and semaphore operations where signaling occurs based on the current state, but independent of a signal transition.

The AND and OR functions can be used to gate data strobe signals by the state. The XOR function can be used to implement two-cycle signaling, which is used in self-timed systems to minimize signaling delays. If these functions are not needed, then the Mealy outputs can be configured as normal outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (DIP Pins 7 or 22 to Pins 8, 21, or 23) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs During Programming ..... 0.0V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Programming Voltage 13.0V

Output Current into Outputs (LOW) ..... 8 mA

UV Exposure ..... 7258 Wsec/cm^2

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >1500V (per MIL−STD−883, Method 3015)

Operating Range

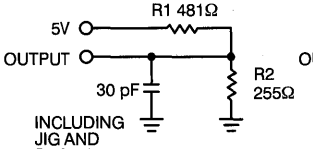
Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

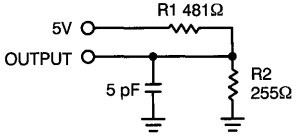
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed HIGH Input, All Inputs[1]		2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, All Inputs[1]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC}		−40	+40	μA
I_{SC}[2]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]		−30	−110	mA
I_{CC}[2, 4]	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open, Operating at f = f_{MAX}	Commercial		200	mA
			Military			

Notes:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Tested initially and after any design or process changes that may affect this parameter.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested with device programmed as an 8-bit counter.

AC Test Loads and Waveforms

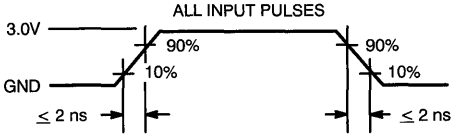


(a)



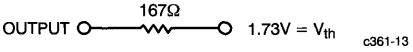
(b)

c361-11



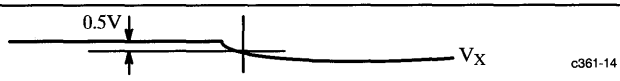
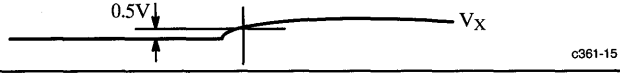
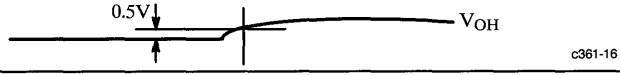
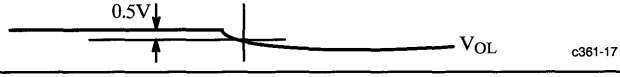
c361-12

Equivalent to: THÉVENIN EQUIVALENT



c361-13

Test Waveforms

Parameter	V_X	Output Waveform—Measurement Level
$t_{CER(-)}$	0.0V	 c361-14
$t_{CER(+)}$	2.6V	 c361-15
$t_{CEA(+)}$	V_{th}	 c361-16
$t_{CEA(-)}$	V_{th}	 c361-17

Commercial Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	-125		-100		-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Mealy Output Delay	2	9	2	11	2	12	ns
t_{CO}[7]	Clock to Output Delay		15		19		23	ns
t_{CM}[7]	Clock to Mealy Output Delay		17		20		25	ns
t_{OH}	Output Stable Time	5		5		5		ns
t_{IS}	Input Register Input Set-Up Time	2		3		5		ns
t_{IH}	Input Register Input Hold Time	3		4		5		ns
t_S[8]	State Register Input Set-Up Time	7		9		12		ns
t_H[8]	State Register Input Hold Time	0		0		0		ns
t_{DWH}[2, 9, 10]	Input Clock Pulse Width HIGH (Doubler Enabled)	6		7		9		ns
t_{DWL}[2, 9, 10]	Input Clock Pulse Width LOW (Doubler Enabled)	6		7		9		ns
t_{DP}[2, 10]	Input Clock Period (Doubler Enabled)	15		20		24		ns
t_{WH}[2, 9, 11]	Input Clock Pulse Width HIGH	2		3		4		ns
t_{WL}[2, 9, 11]	Input Clock Pulse Width LOW	2		3		4		ns
t_P[2, 11]	Input Clock Period	7.5		10		12		ns
t_{SO}[12]	Output Skew		2		2		2	ns
t_{SM}[13]	Mealy Output Skew		3		3		3	ns
f_{MAXI}[2, 11]	Input Maximum Frequency (Doubler Enabled)	62.5		50.0		41.7		MHz
f_{MAX}[2, 4]	Output Maximum Frequency	125.0		100.0		83.3		MHz
t_{CER}[2, 6]	Clock to Output Disable Delay		16		20		22	ns
t_{CEA}[2, 14, 15]	Clock to Output Enable Delay		16		20		22	ns

Notes:

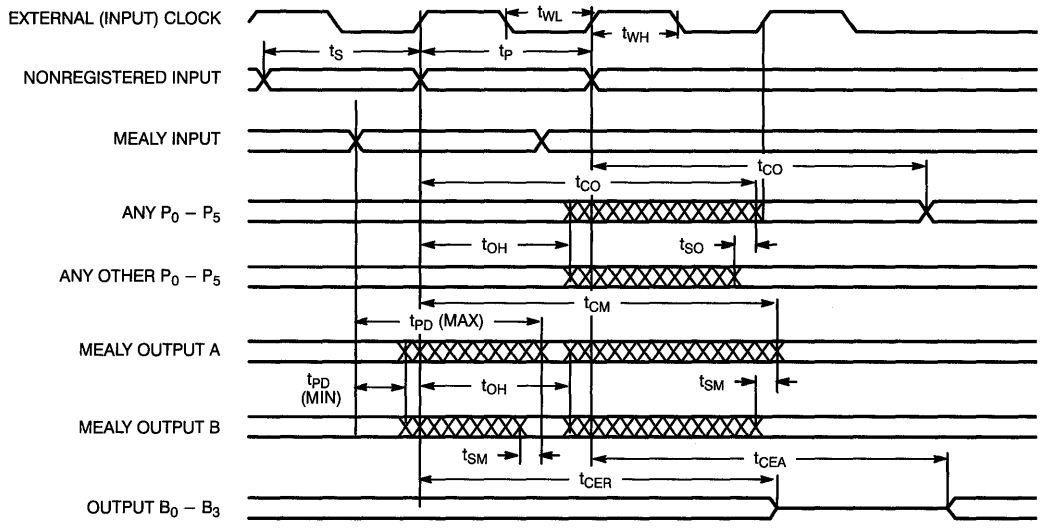
5. Output reference point on AC measurements is 1.5V, except as noted in Test Waveforms:
   $t_{CER(-)}$ negative going is measured at $V_{OH} - 0.5V$.
   $t_{CER(+)}$ positive going is measured at $V_{OL} + 0.5V$
6. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{CEA} and t_{CER}. Part (b) of AC Test Loads and Waveforms is used for t_{CEA} and t_{CER}.
7. This specification is guaranteed for the worst-case programmed pattern for which all device outputs are changing state on a given access or clock cycle.
8. Input register bypassed.
9. The clock input is tested to accommodate a 60/40 duty cycle waveform at the maximum frequency.
10. This applies to the input clock when the doubler is enabled.
11. This applies to the input clock when the doubler is disabled.
12. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs on the same device triggered by the same clock edge with all other device outputs changing state within the same clock cycle.
13. This parameter specifies the maximum allowable t_{PD} difference between any two Mealy outputs on the same device triggered by the same or simultaneous input signals with all other device outputs changing state within the same access or clock cycle.
14. R1 is disconnected for $t_{CEA(+)}$ positive going (open circuited). See part (b) of AC Test Loads and Waveforms.
15. R2 is disconnected for $t_{CEA(-)}$ negative going (open circuited). See part (b) of AC Test Loads and Waveforms.

Military Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	Military				Unit
		−100		−83		
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Mealy Output Delay	1.5	11	1.5	13	ns
t_{CO}[7]	Clock to Output Delay		19		23	ns
t_{CM}[7]	Clock to Mealy Output Delay		21		25	ns
t_{OH}	Output Stable Time	5		5		ns
t_{IS}	Input Register Input Set-Up Time	3		5		ns
t_{IH}	Input Register Input Hold Time	4		5		ns
t_S[8]	State Register Input Set-Up Time	9		12		ns
t_H[8]	State Register Input Hold Time	0		0		ns
t_{DWH}[2, 9, 10]	Input Clock Pulse Width HIGH (Doubler Enabled)	7		9		ns
t_{DWL}[2, 9, 10]	Input Clock Pulse Width LOW (Doubler Enabled)	7		9		ns
t_{DP}[2, 10]	Input Clock Period (Doubler Enabled)	20		24		ns
t_{WH}[2, 9, 11]	Input Clock Pulse Width HIGH	3		4		ns
t_{WL}[2, 9, 11]	Input Clock Pulse Width LOW	3		4		ns
t_P[2, 11]	Input Clock Period	10		12		ns
t_{SO}[12]	Output Skew		3		3	ns
t_{SM}[13]	Mealy Output Skew		4		4	ns
f_{MAXI}[2, 11]	Input Maximum Frequency (Doubler Enabled)	50		41.7		MHz
f_{MAX}[2, 4]	Output Maximum Frequency	100.0		83.3		MHz
t_{CER}[6]	Clock to Output Disable Delay		20		22	ns
t_{CEA}[2, 14, 15]	Clock to Output Enable Delay		20		22	ns

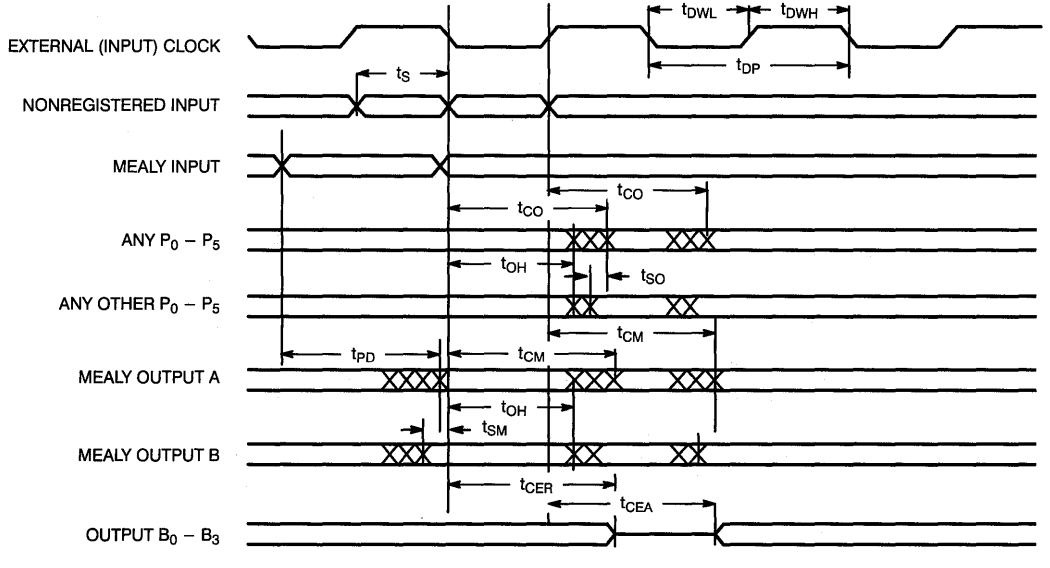
Switching Waveforms

Clock Doubler Inactive (Virgin State).
Nonregistered Input (Virgin State – C1,C0 = 0,0).



c361-18

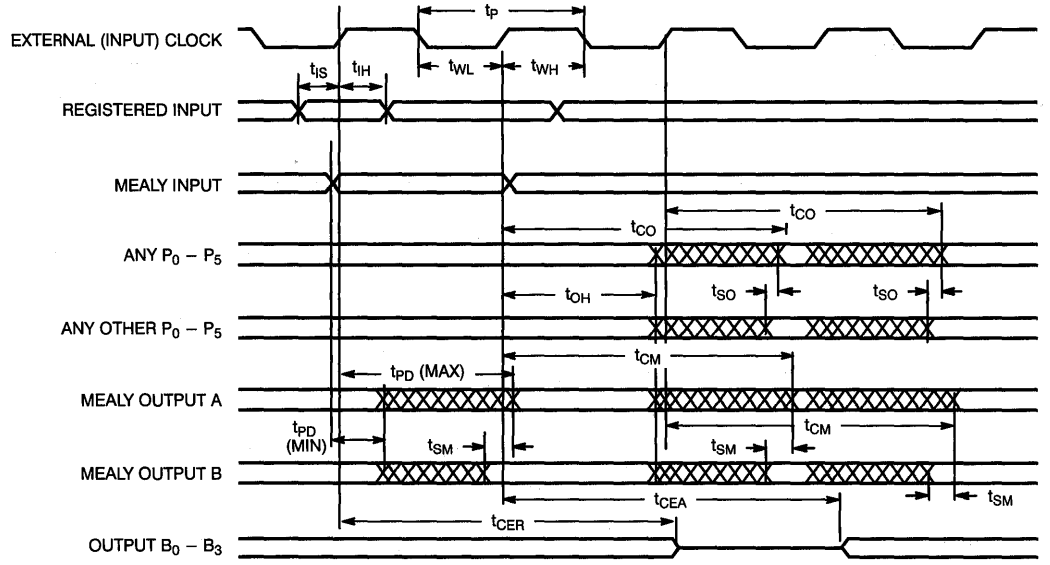
Clock Doubler Enabled (C0 = 1)
Nonregistered Input (Virgin State – C1,C0 = 0,0)



c361-19

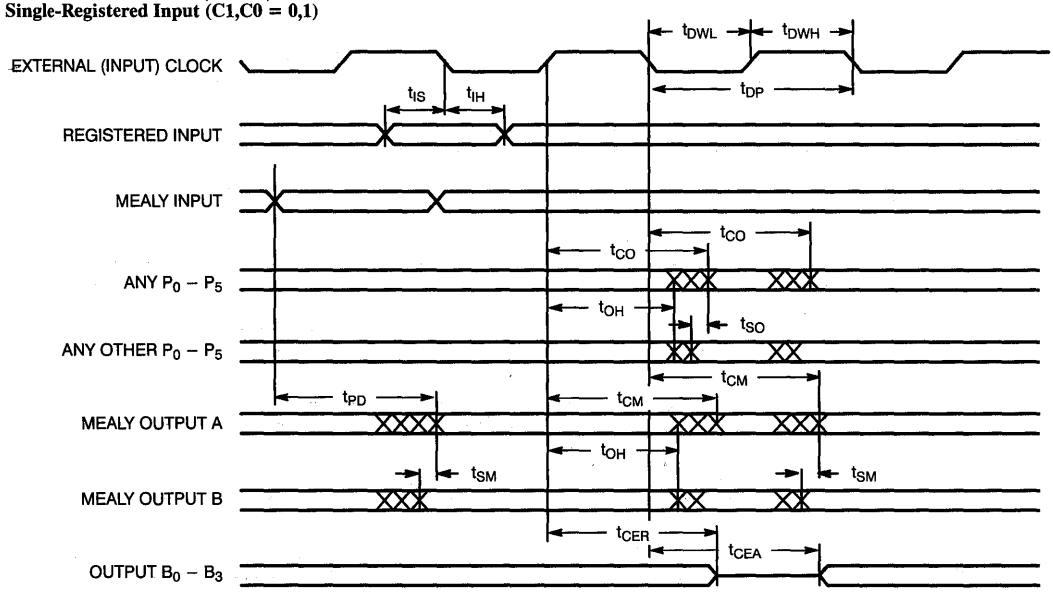
Switching Waveforms (continued)

Clock Doubler Inactive (Virgin State).
Single-Registered Input (C1,C0 = 0,1).



c361-20

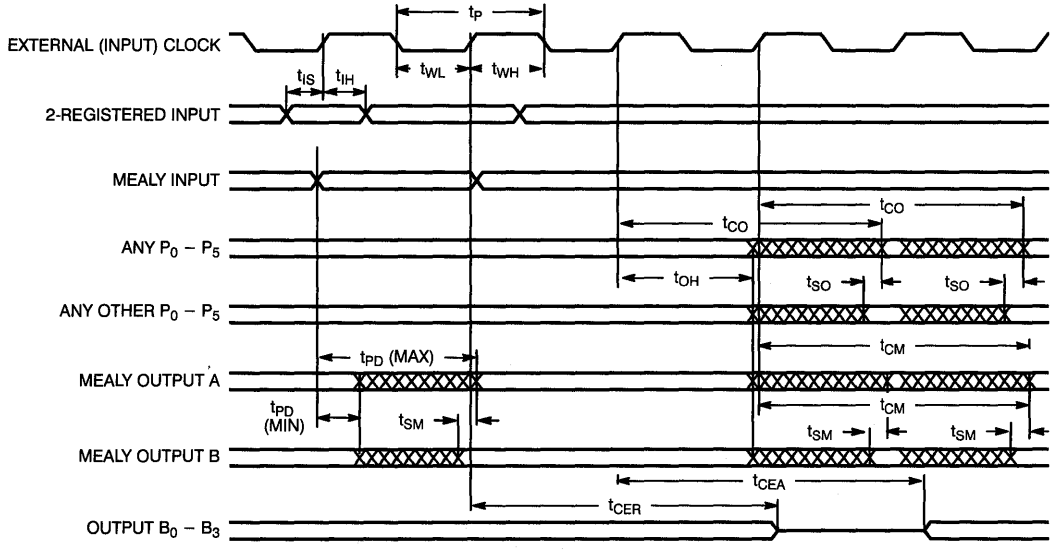
Clock Doubler Enabled (C0 = 1)
Single-Registered Input (C1,C0 = 0,1)



c361-21

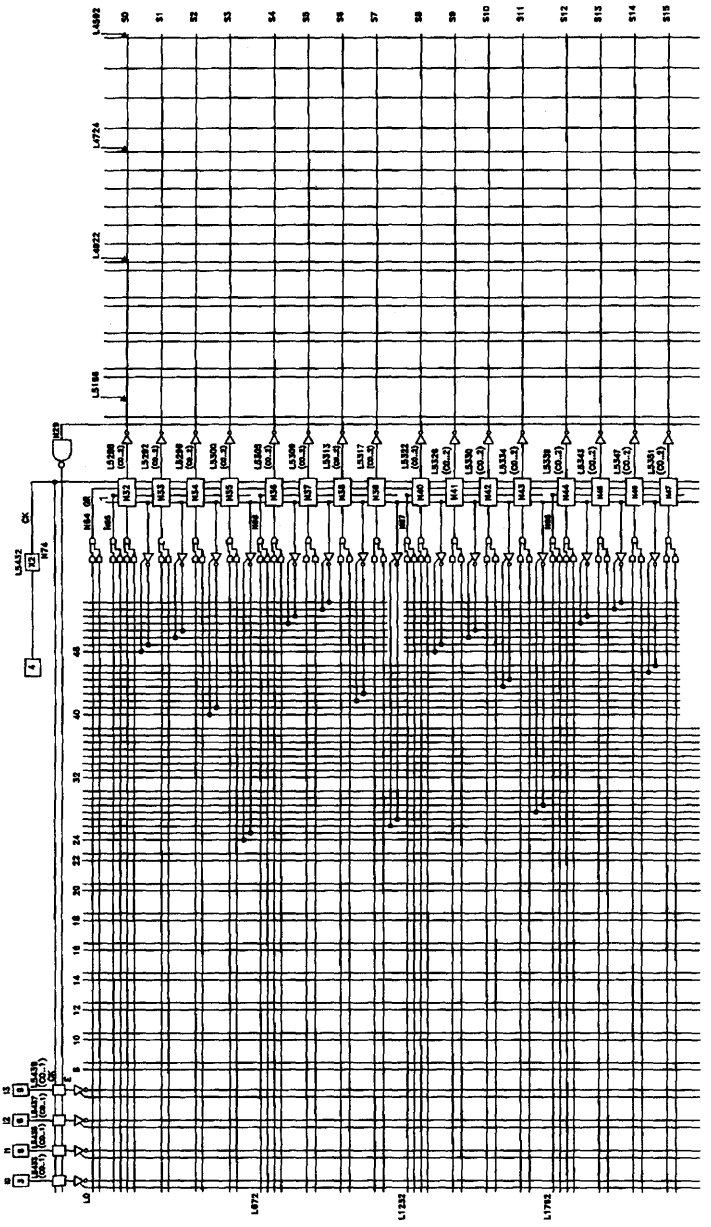
Switching Waveforms (continued)

Clock Doubler Inactive (Virgin State)
Double-Registered Input (C_1, C_0 = 1,X)

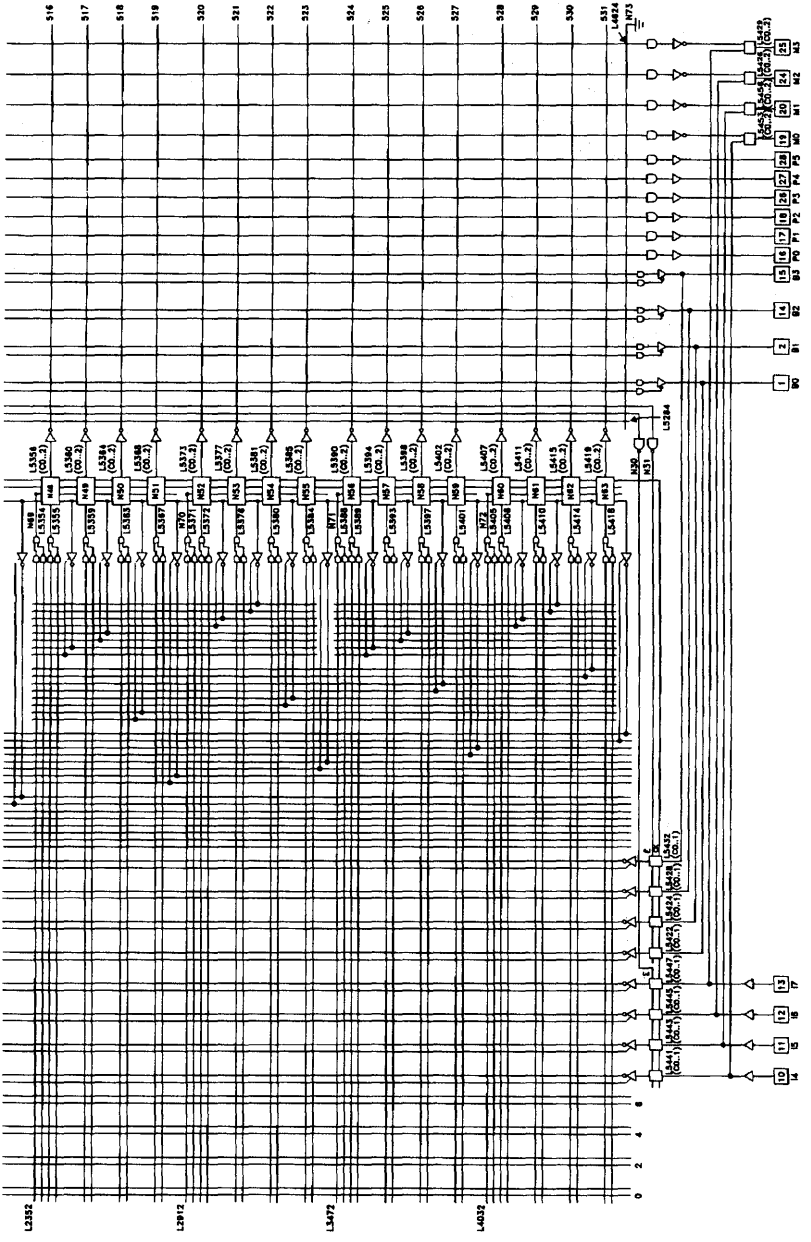


c361-22

CY7C361 Block Diagram (Upper Half)



CY7C361 Block Diagram (Lower Half)



Ordering Information

I_{CC} mA	f_{MAX} MHz	Ordering Code	Package Name	Package Type	Operating Range
200	125.0	CY7C361–125HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–125WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	100.0	CY7C361–100HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–100WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C361–100HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
		CY7C361–100QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C361–100WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
	83.3	CY7C361–83HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–83WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C361–83HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
		CY7C361–83QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C361–83WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{CM}	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–00106–C

Features

- **Flash erasable CMOS PLDs**
- **High density**
  - **—32–256 macrocells**
  - **—32–256 I/O pins**
  - **—Multiple clock pins**
- **High speed**
  - **—t_{PD} = 10–15 ns**
  - **—t_S = 7.5–12 ns**
  - **—t_{CO} = 7.5 ns–12 ns**
- **Fast Programmable Interconnect Matrix (PIM)**
  - **—Uniform predictable delay, independent of routing**
  - **—No penalty for traversing PIM**
- **Intelligent product term allocator**
  - **—0–16 product terms to any macrocell**
  - **—Provides product term steering on an individual basis**
  - **—Provides product term sharing among local macrocells**
  - **—Prevents wasting and stealing of neighboring product terms**
- **Simple timing model**
  - **—No fanout delays**
  - **—No expander delays**
  - **—No dedicated vs. I/O pin delays**
  - **—No additional delay through PIM**
  - **—No penalty for using full 16 product terms**
  - **—No delay for steering or sharing product terms**
- **Flexible clocking**
  - **—2–4 clock pins per device**
  - **—Clock polarity control**
- **Packages**
  - **—44–288 pins**
  - **—PLCC, LCC, PGA, and QFP packages**
- ***Warp2*™**
  - **—Low-cost, text-based design tool, PLD compiler**
  - **—IEEE 1076-compliant VHDL**
  - **—Available on PC and Sun platforms**
- ***Warp3*™ CAE development system**
  - **—VHDL input**
  - **—ViewLogic graphical user interface**
  - **—Schematic capture (ViewDraw)**
  - **—VHDL simulation (ViewSim)**
  - **—Available on PC and Sun platforms**

General Description

The FLASH370 family of CMOS PLDs provides a range of high-density programmable logic solutions with unparalleled performance. Each member of the family is designed with Cypress's state-of-the-art 0.65-micron Flash technology. All of the devices are electrically erasable and reprogrammable, simplifying product inventory and reducing costs.

The FLASH370 family is designed to bring the flexibility, ease of use and performance of the 22V10 to high-density PLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator array, and 16 macrocells. The PIM distributes signals from one logic block to another as well as all inputs from pins.

The family features a wide variety of densities and pin counts to choose from. At each density there are two packaging options to choose from—one that is I/O intensive and another that is register intensive. For example, the CY7C374 and CY7C375 both feature 128 macrocells. On the CY7C374 half of the macrocells are buried and the device is available in 84-pin packages. On the CY7C375 all of the macrocells are fed to I/O pins and the device is available in 164-pin packages. *Figure 1* shows a block diagram of the CY7C374/5.

Functional Description

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM is an extremely robust interconnect that avoids fitting and density limitations which plague competing high-density solutions. Routing is automatically accomplished by software and the propagation delay through the PIM is transparent to the user. Signals from any pin or any logic block can be routed to any or all logic blocks.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pincount and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic block(s). Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide PIM-to-logic block interface also improves the routing capacity of the FLASH370 family.

An important feature of the PIM involves timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact all inputs travel through the PIM. Likewise, there are no route-dependent timing parameters on the FLASH370 devices. The worst-case PIM delays are incorporated in all appropriate FLASH370 specifications.

FLASH370 Selection Guide

Device	Pins	Macrocells	Dedicated Inputs	I/O Pins	Flip-Flops	Speed (t_{PD})
371	44	32	6	32	44	10
372	44	64	6	32	76	12
373	84	64	6	64	76	12
374	84	128	6	64	140	12
375	160	128	6	128	140	12
376	160	256	6	128	268	15
377	288	256	6	256	268	15

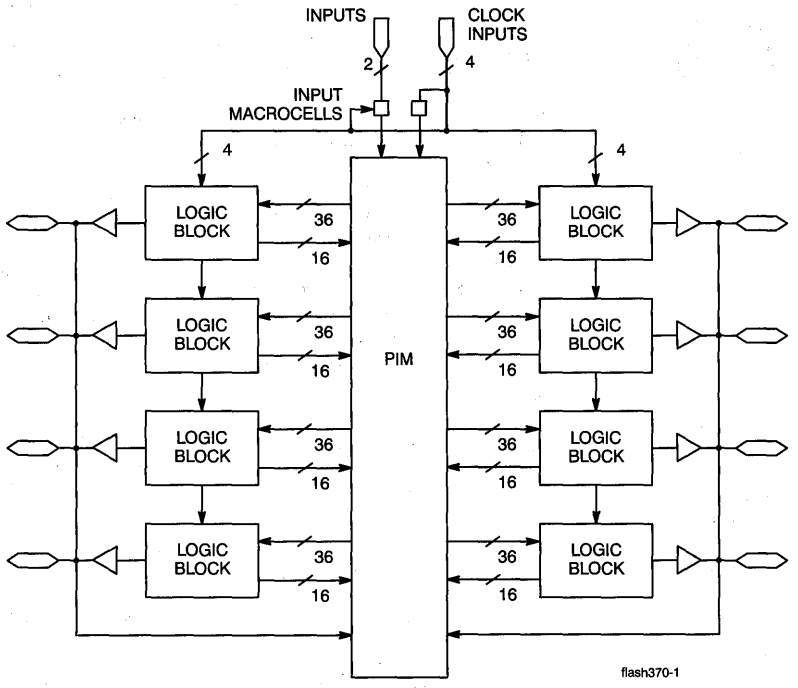


Figure 1. CY7C374/5 Block Diagram

Functional Description (continued)

Finally, routing signals through the PIM is completely invisible to the user. All routing is accomplished 100% by software—no hand routing is necessary. *Warp2* and third-party development packages automatically route designs for the FLASH370 family in a matter of minutes.

Logic Block

The logic block is the basic building block of the FLASH370 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used.

There are two types of logic blocks in the FLASH370 family. The first type features an equal number (16) of I/O cells and macrocells and is shown in *Figure 2*. This architecture is best for I/O-intensive applications. The second type of logic block features a buried macrocell along with each I/O macrocell. In other words, in each logic block, there are eight macrocells that are connected to I/O cells and eight macrocells that are internally fed back to the PIM only. This organization is designed for register-intensive applications and is displayed in *Figure 3*. Note that at each FLASH370 density (except the smallest), an I/O intensive and a register-intensive device is available.

Product Term Array

Each logic block features a 72 x 86 programmable product term array. This array is fed with 36 inputs from the PIM, which originate from macrocell feedbacks and input pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 86 product terms in the array can be created from any of the 72 inputs.

Of the 86 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining six product terms in the logic block are output enable (OE) product terms. The OE product terms control 8 of the 16 macrocells and are selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The final two product terms in each logic block are dedicated set and reset product terms.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of steering product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will "steer" ten product terms to one macrocell and three to the other. On FLASH370 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in

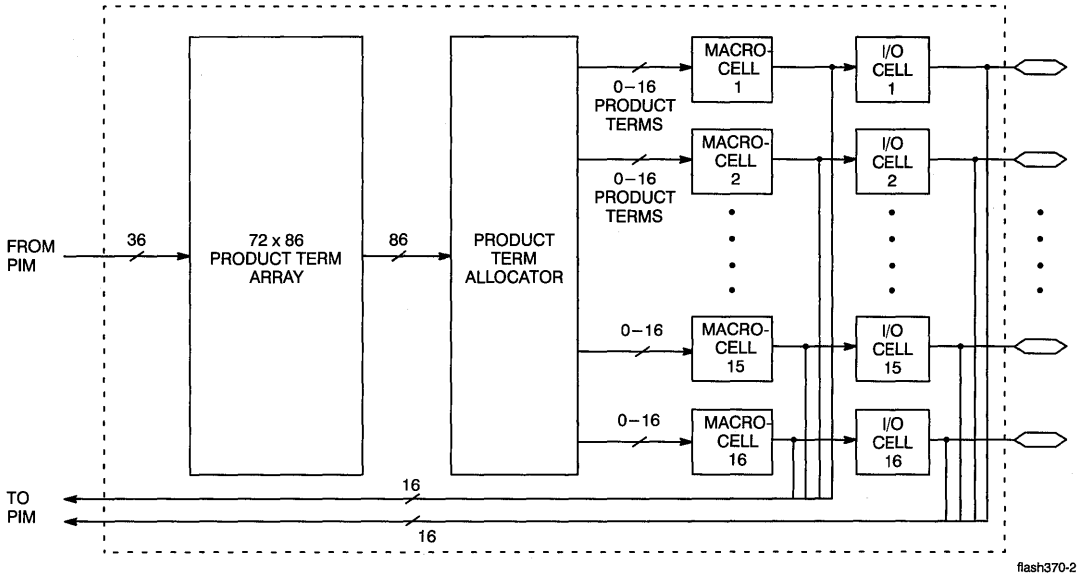


Figure 2. Logic Block for CY7C371, CY7C373, CY7C375, and CY7C377 (I/O Intensive)

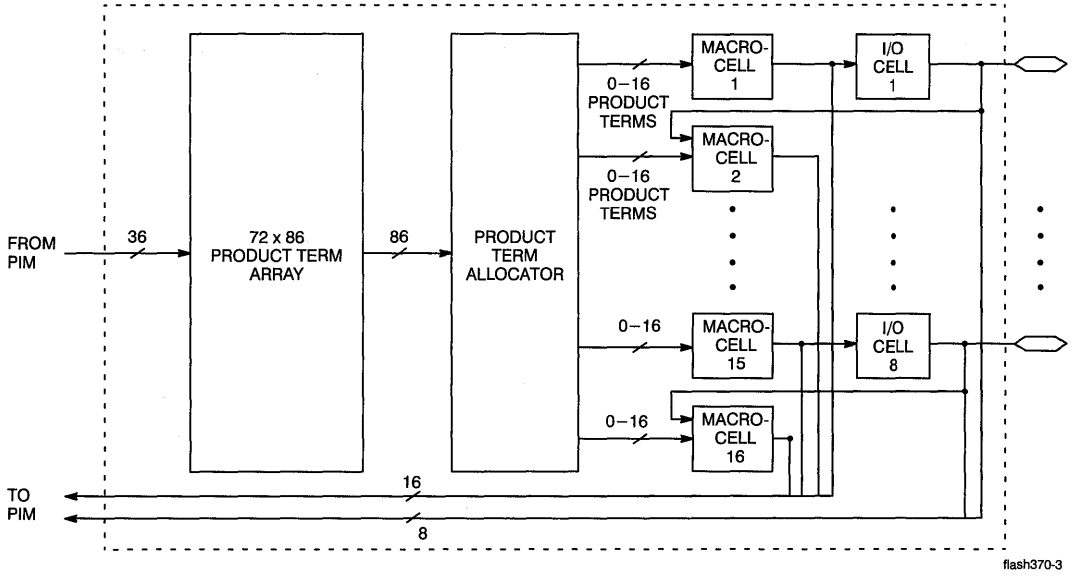


Figure 3. Logic Block for CY7C372, CY7C374, and CY7C376 (Register Intensive)

cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The FLASH370 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene. Note that greater usable density can often be achieved if the user "floats" the pin assignment. This allows the compiler to group macrocells that have common product terms adjacently.

One last thing to reiterate is that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the FLASH370 devices.

FLASH370Macrocell

I/O Macrocell

Within each logic block there are 8 or 16 I/O macrocells depending on the device used. *Figure 4* illustrates the architecture of the I/O macrocell. The macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or reset on a logic block basis with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on a single product term or sum term.

Clocking of the register is very flexible. Depending on the device, either two or four global synchronous clocks are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered off falling as well as rising edges (see the Dedicated/Clock Inputs section).

At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

One last thing to note about the I/O macrocell on the FLASH370 family concerns feedback. The macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Buried Macrocell

Some of the devices in the FLASH370 family feature additional macrocells that do not feed individual I/O pins. *Figure 5* displays the architecture of the I/O and buried macrocells for these devices. The I/O macrocell is identical to the one on devices without buried macrocells.

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. The primary difference between the I/O macrocell and the buried macrocell is that the buried macrocell does not have the ability to output data directly to an I/O pin.

One additional difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

FLASH370 I/O Cell

The I/O cell on the FLASH370 devices is illustrated along with the I/O macrocell in *Figures 4* and *5*. The user can program the I/O cell to change the way the three-state output buffer is enabled and/or disabled. Each output can be set permanently on (output only), permanently off (input only), or dynamically controlled by one of two OE product terms.

Dedicated/Clock Inputs

A number of pins on each member of the FLASH370 family are designated as input-only. There are two types of dedicated inputs on FLASH370 devices: input pins and input/clock pins. *Figure 6* il-

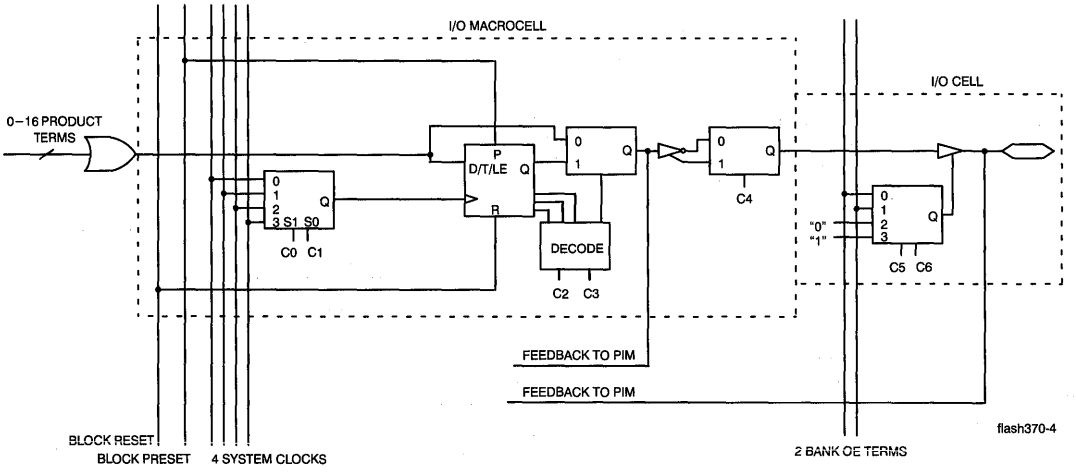


Figure 4. I/O Macrocell

lustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control. On double-registered inputs, a 10-year MTBF is guaranteed when sampling asynchronous signals.

Figure 7 illustrates the architecture of input/clock pins. There are either two or four input/clock pins available, depending on the device selected. Like the input pins, input/clock pins can be combinatorial, registered, double registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input is user-configurable in polarity. The polarity of the clock signal can also be controlled by the user. Note that this

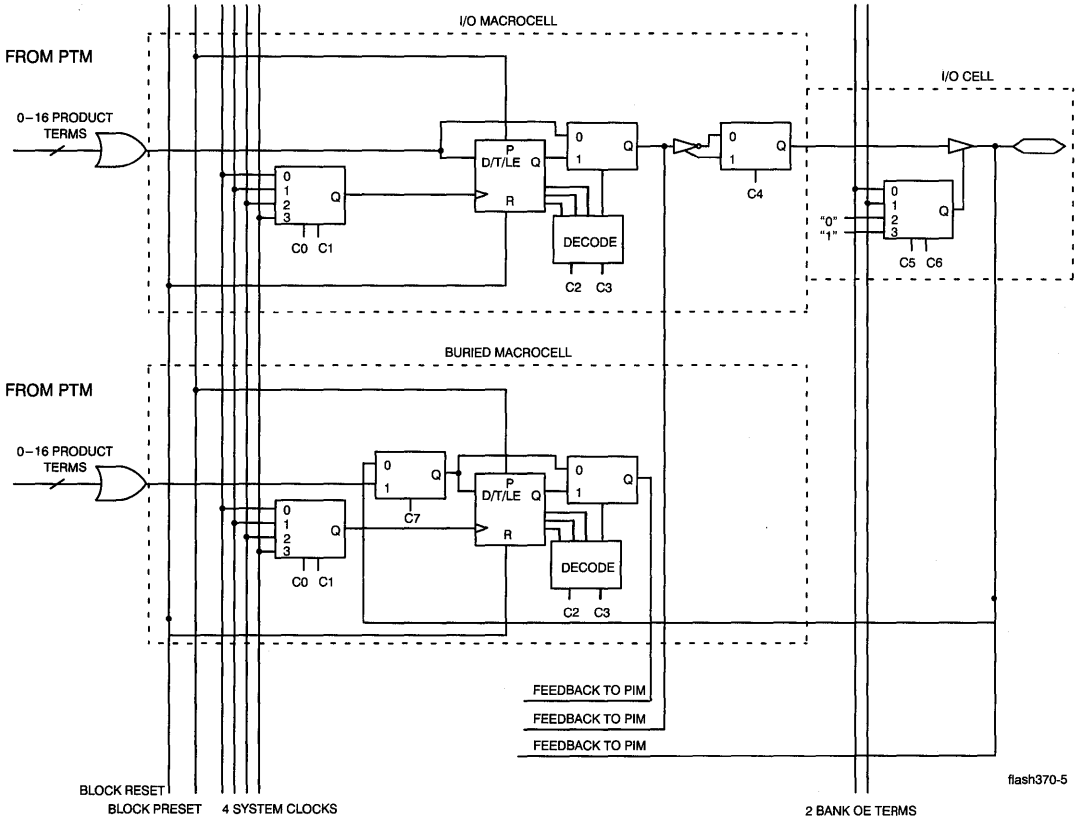


Figure 5. I/O and Buried Macrocells

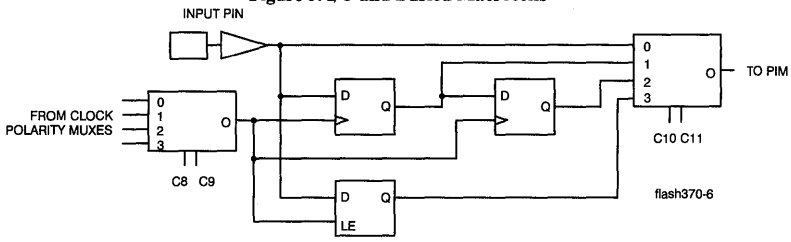


Figure 6. Input Pins

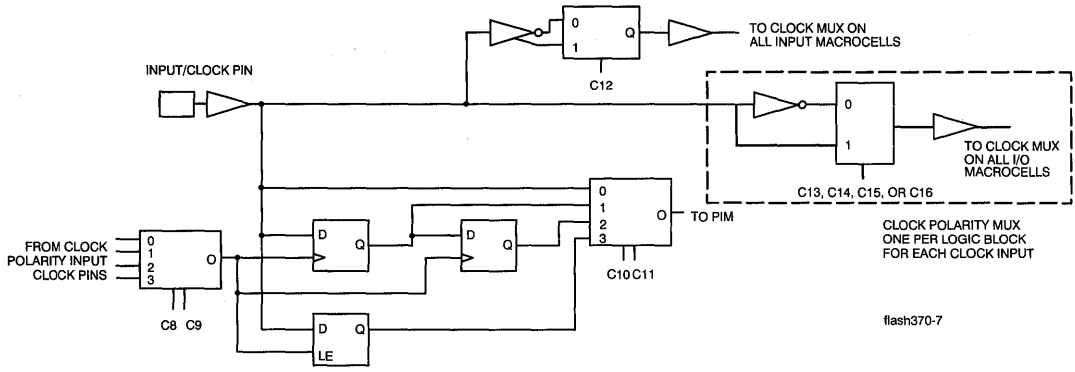


Figure 7. Input/Clock Pins

polarity is separately controlled for input registers and output registers.

Timing Model

One of the most important features of the FLASH370 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used or not used on the parts. *Figure 8* illustrates the true timing model for the 10-ns devices. For combinatorial paths, any input to any output incurs a 10-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 7.5 ns and the clock to output time is also 7.5 ns. Again, these measurements are for any output and clock, regardless of the logic used.

Stated another way, the FLASH370 features:

- no fanout delays
- no expander delays
- no dedicated vs. I/O pin delays
- no additional delay through PIM
- no penalty for using 0–16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no routing delays
- no output bypass delays

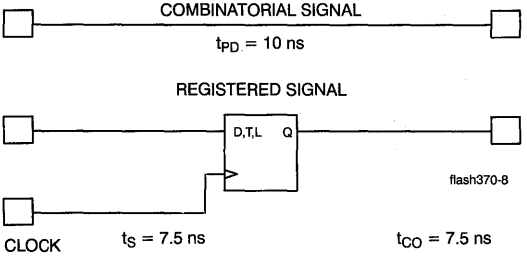


Figure 8. Timing Model for CY7C371

The simple timing model of the FLASH370 family eliminates unexpected performance penalties common in other high-density PLDs.

Development Software Support

Warp2

Warp2 is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design entry. VHDL provides a number of significant benefits for the design engineer. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map for the desired device. For simulation, *Warp2* provides the graphical waveform simulator from the PLD ToolKit.

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense and supported by every major vendor of CAE tools. VHDL allows designers to learn a signle language that is useful for all facets of the design process.

Warp3

Warp3 is a sophisticated design tool that is based on the latest version of ViewLogic's CAE design environment. *Warp3* features schematic capture (ViewDraw™), VHDL waveform simulation (ViewSim™), a VHDL debugger, and VHDL synthesis, all integrated in a graphical design environment. *Warp3* is available on PCs using Windows 3.1 or subsequent versions and on Sun workstations.

Third-Party Software

Cypress maintains a very strong commitment to third-party design software vendors. All major third-party software vendors (including ABEL™, LOG/iC™, CUPL™, and Minc) will provide support for the FLASH370 family of devices. To expedite this support, Cypress supplies vendors with all pertinent architectural information as well as design fitters for our products.

Programming

QuickPro II

The *Warp2* package includes the QuickPro II device programmer from Cypress. QuickPro II will program all Cypress PROMs and

PLDs. QuickPro II is a standalone programmer that connects to any IBM-compatible PC via the printer port.

Third-Party Programmers

As with development software, Cypress strongly supports third-party programmers. All major third-party programmers (including Data I/O, Logical Devices, Minato, SMS, and Stag) will support the FLASH370 family.

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C371**

32-Macrocell Flash PLD

Features

- **32 macrocells in two logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **No hidden delays**
- **High speed**
  - —f_{MAX} = 100 MHz
  - —t_{PD}= 10 ns
  - —t_S = 7.5 ns
  - —t_{CO} = 7.5 ns
- **Electrically alterable Flash technology**
- **Available in 44-pin PLCC, CLCC, and LCC packages**
- **Pin compatible with the CY7C372**

Functional Description

The CY7C371 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C371 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

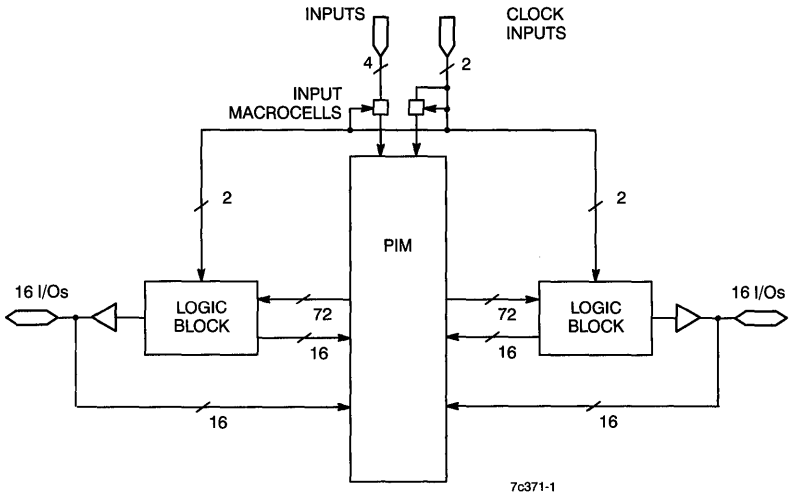
The 32 macrocells in the CY7C371 are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C371 is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C371 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371 remain the same.

Logic Block Diagram

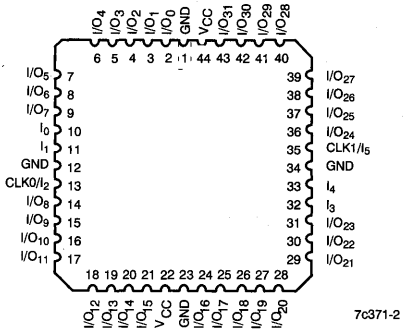


Selection Guide

		7C371–100	7C371–83	7C371–66	7C371–50
Maximum Propagation Delay, t_{PD} (ns)		10	12	15	20
Maximum Operating Current, I_{CC2} (mA)	Commercial	240	240	240	
	Military		260	260	260
Maximum Standby Current, I_{CC1} (mA)	Commercial	200	200	200	
	Military		220	220	220

Shaded area contains advanced information.

Pin Configuration



Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C371 includes two logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C371 has a separate associated I/O pin. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the two logic blocks on the CY7C371 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Design Tools

Development software for the CY7C371 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of thse products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools such as ABEL™, CUPL™, MINC, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs (LOW) ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)	2.4		V
			I_{OL} = −2.0 mA (Mil)			V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)		0.5	V
			I_{OL} = 12 mA (Mil)			V
V_{IH}	Input HIGH Voltage			2.0	7.0	V
V_{IL}	Input LOW Voltage			– 0.5	0.8	V

Electrical Characteristics Over the Operating Range[2] (continued)

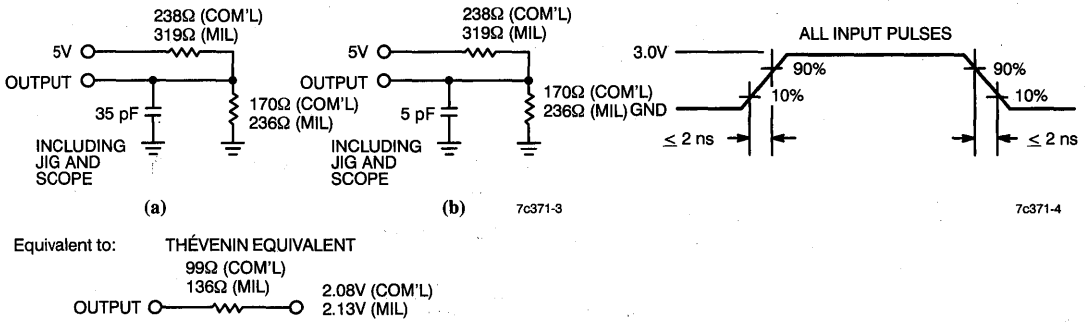
Parameter	Description	Test Conditions		Min.	Max.	Unit
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−10	+10	μA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V		−30	−90	mA
I_{CC2}	Power Supply Current	$V_I = V_{CC}$ or GND, f = 40 MHz	Com'l		240	mA
			Mil		260	
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}	Com'l		200	mA
			Mil		220	

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C371–100		7C371–83		7C371–66		7C371–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		12		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		14		16		19		24	ns
t_{EA}	Input to Output Enable		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time	4		5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	4		5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		16		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C371s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	62.5		55.5		45.4		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	71.4		62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		7.5		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	7.5		9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		20		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C371s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	66.6		55.5		41.6		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	125		100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	100		83.3		66.6		50		MHz
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	10		12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	100		83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:
5. All AC parameters are measured with 16 outputs switching.

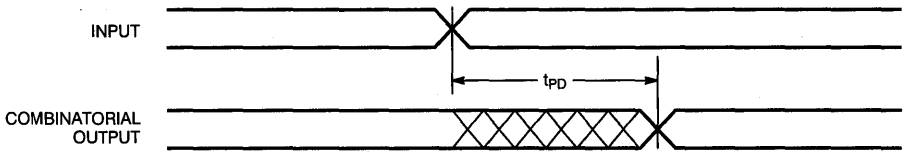
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C371–100		7C371–83		7C371–66		7C371–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output		16		18		21		26	ns

Shaded area contains advanced information.

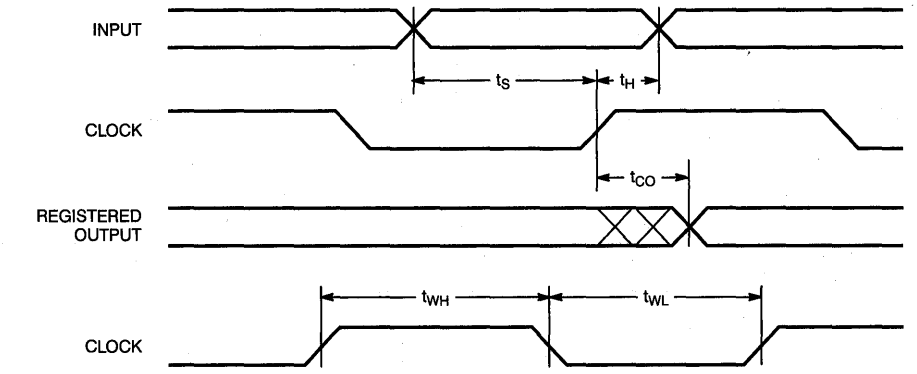
Switching Waveforms

Combinatorial Output



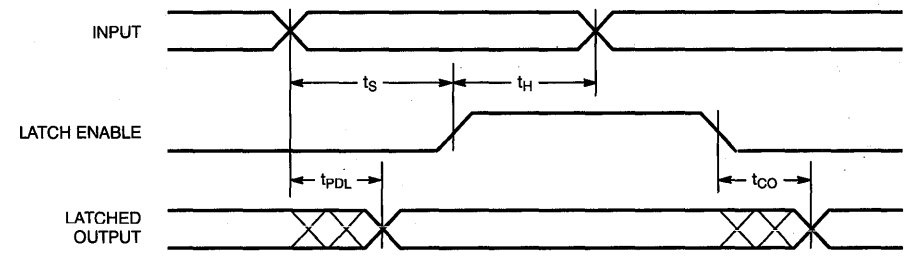
7c371-5

Registered Output



7c371-6

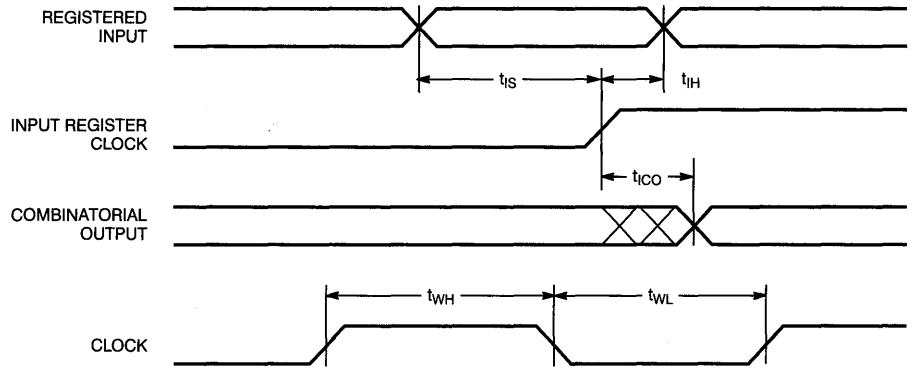
Latched Output



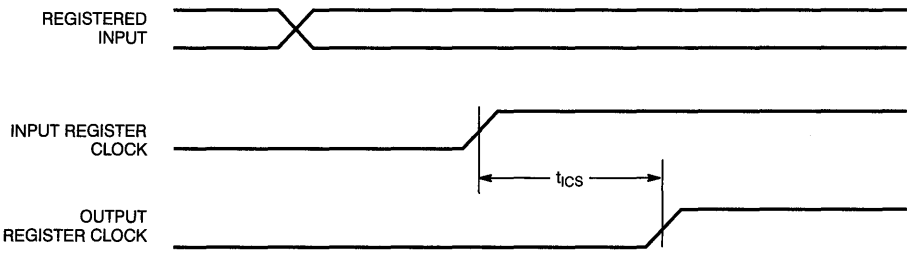
7c371-7

Switching Waveforms (continued)

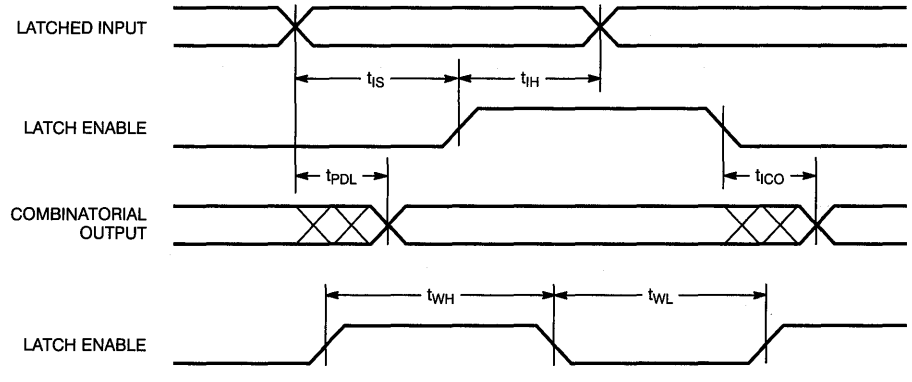
Registered Input



Input Clock to Output Clock

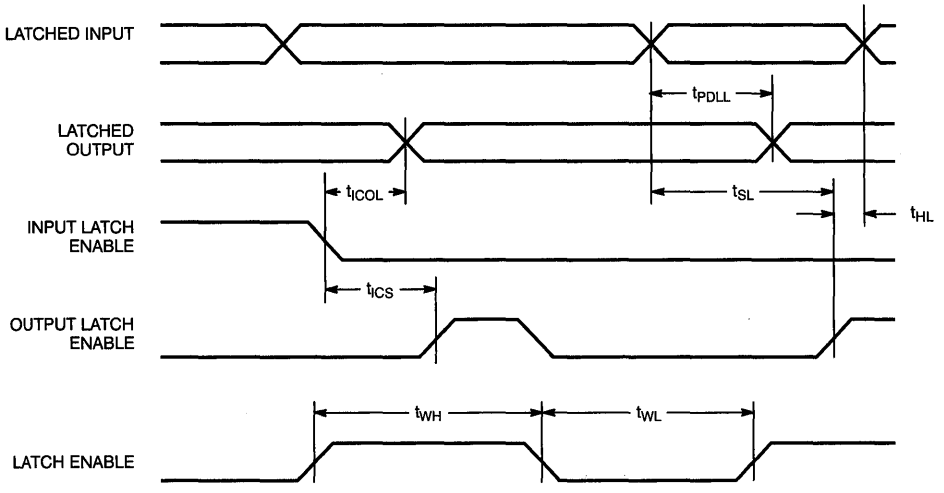


Latched Input

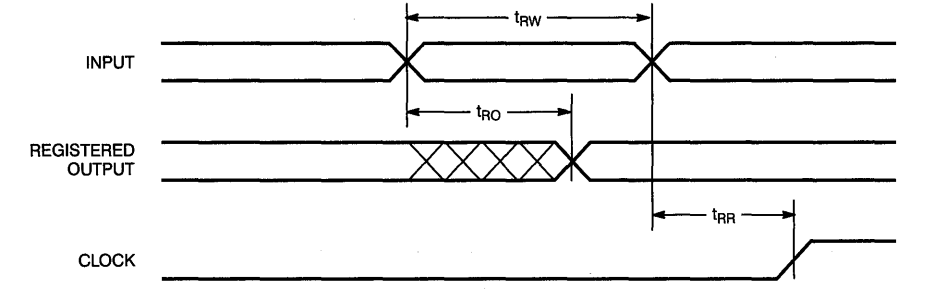


Switching Waveforms (continued)

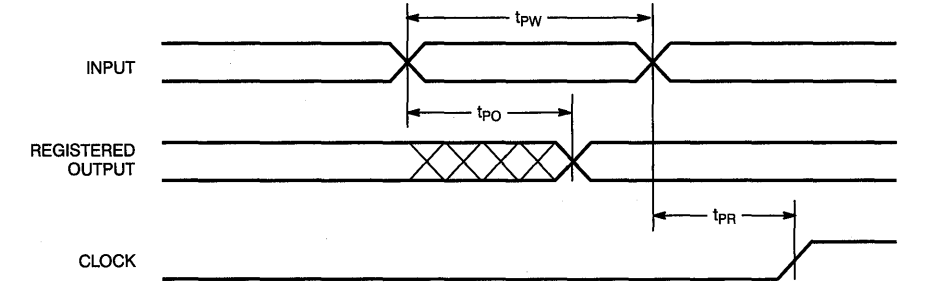
Latched Input and Output



Asynchronous Reset

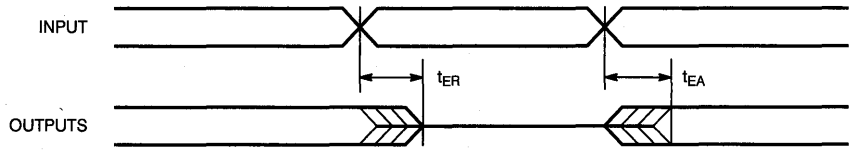


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



7c371-14

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C371-100JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
83	CY7C371-83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C371-83LMB	L67	44-Square Leadless Chip Carrier	Military
66	CY7C371-66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C371-66LMB	L67	44-Square Leadless Chip Carrier	Military
50	CY7C371-50LMB	L67	44-Square Leadless Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

Document #: 38-00212-A

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C372**

64-Macrocell Flash PLD

Features

- **64 macrocells in four logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **No hidden delays**
- **High speed**
  - **— f_{MAX} = 100 MHz**
  - **— t_{PD} = 12 ns**
  - **— t_S = 9 ns**
  - **— t_{CO} = 9 ns**
- **Electrically alterable Flash technology**
- **Available in 44-pin PLCC, CLCC, and LCC packages**
- **Pin compatible with the CY7C371**

Functional Description

The CY7C372 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C372 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

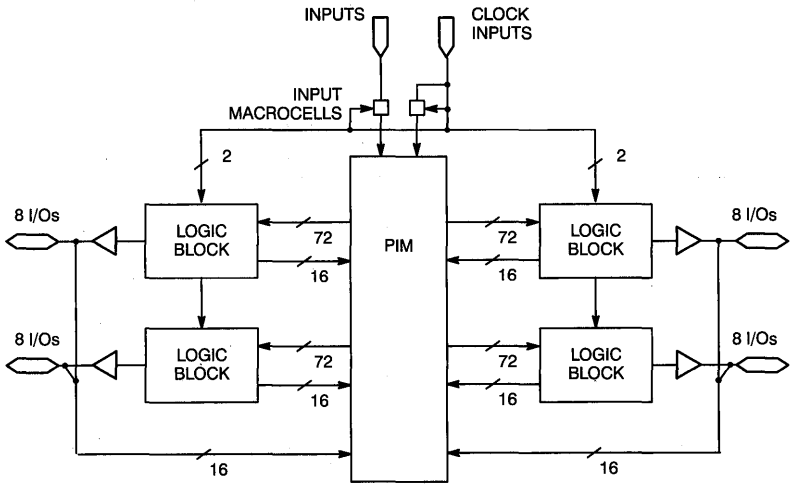
The 64 macrocells in the CY7C372 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C372 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 32 I/O pins on the CY7C372. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C372 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C372 remain the same.

Logic Block Diagram

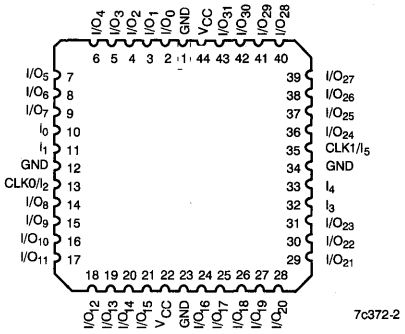


Selection Guide

		7C372–100	7C372–83	7C372–66
Maximum Propagation Delay t_{PD} (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	250	250	250
	Military		300	300
Maximum Operating Current, I_{CC2} (mA)	Commercial	280	280	280
	Military		330	330

Shaded area contains advanced information.

Pin Configuration



Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C372 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C372 have separate I/O pins associated with them. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The I/O macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C372 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C372 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	– 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C372 Min.	7C372 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OL} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage				2.0	7.0	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		250	mA
				Mil		300	
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND, f = 40 MHz		Com'l		280	mA
				Mil		330	

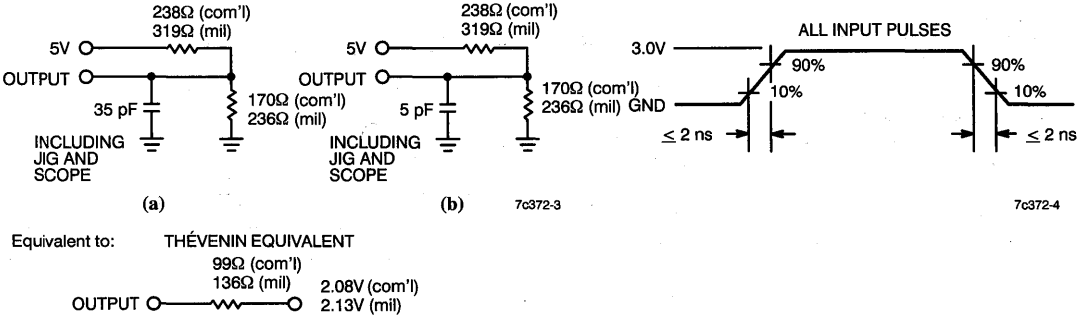
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C372–100 Min.	7C372–100 Max.	7C372–83 Min.	7C372–83 Max.	7C372–66 Min.	7C372–66 Max.	Unit
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C372s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	55.5		45.5		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C372s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	55.5		41.7		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	100		83		66		MHz
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:
5. All AC parameters are measured with 16 outputs switching.

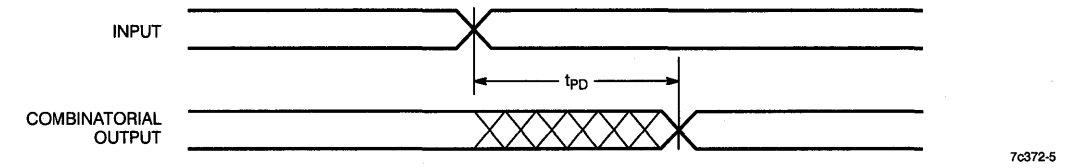
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C372–100		7C372–83		7C372–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

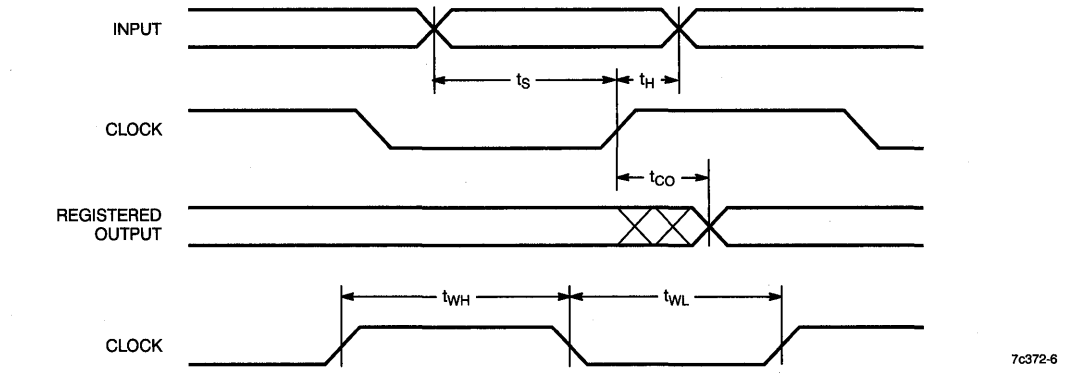
Shaded area contains advanced information.

Switching Waveforms

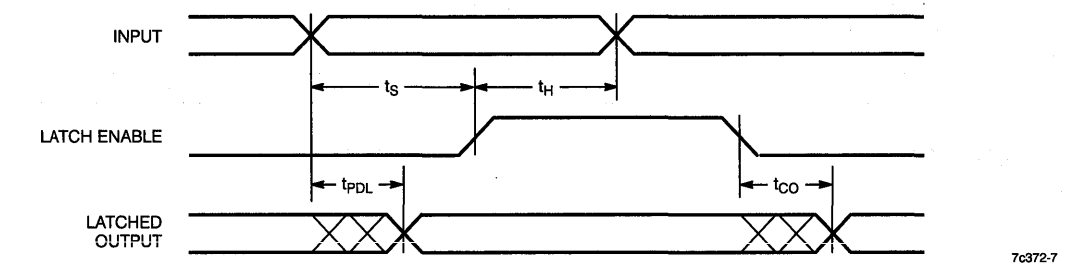
Combinatorial Output



Registered Output

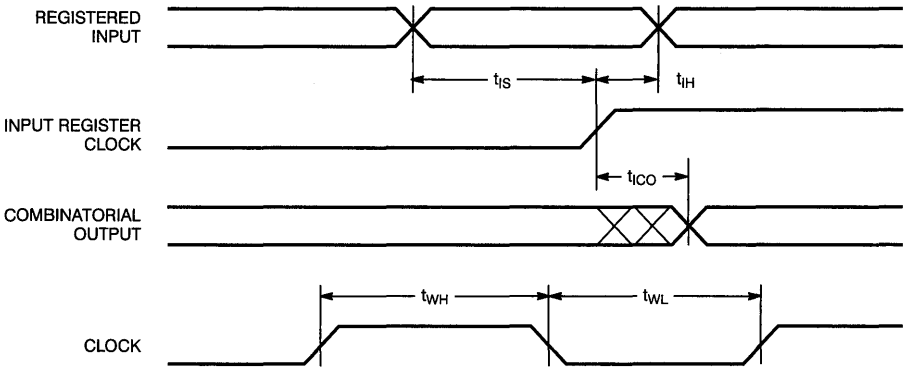


Latched Output

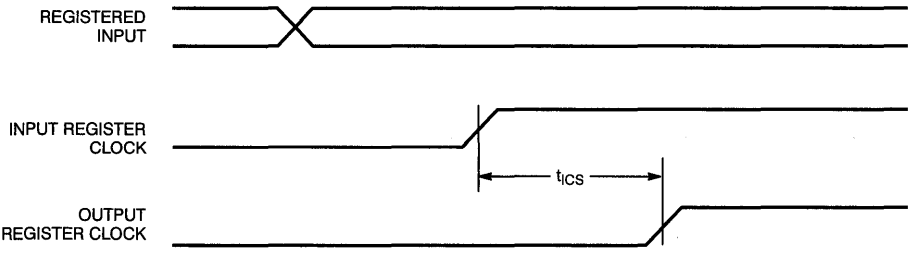


Switching Waveforms (continued)

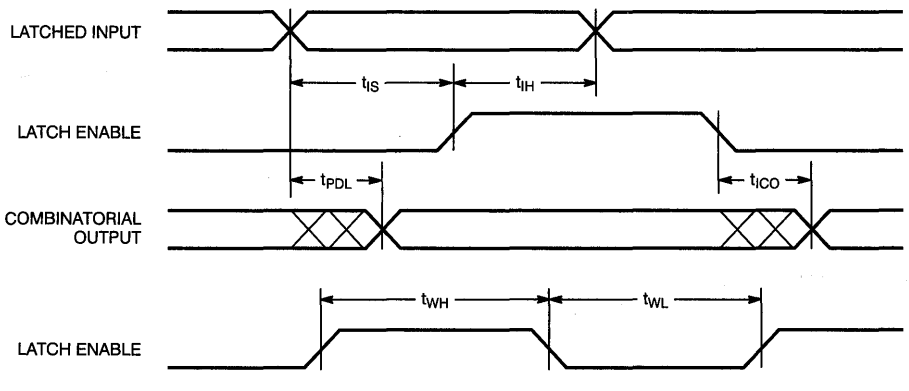
Registered Input



Input Clock to Output Clock

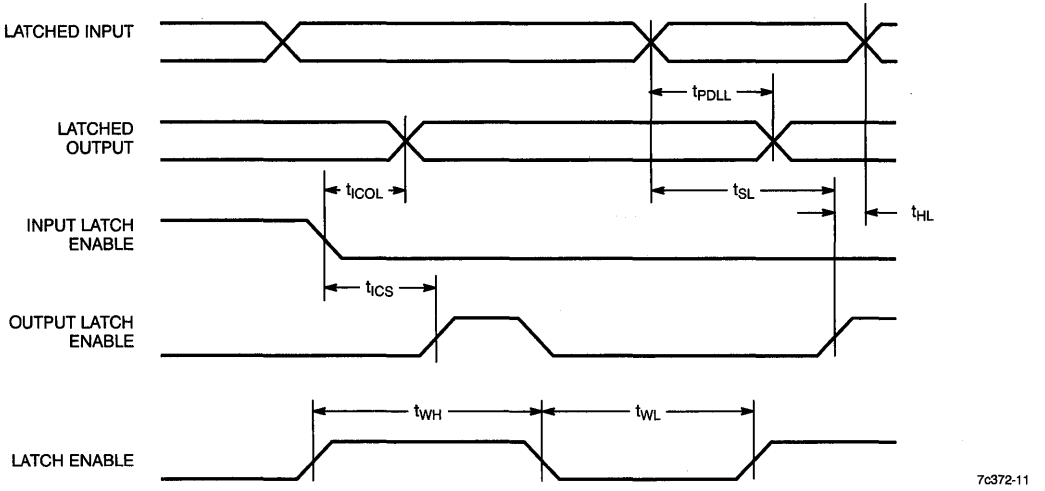


Latched Input

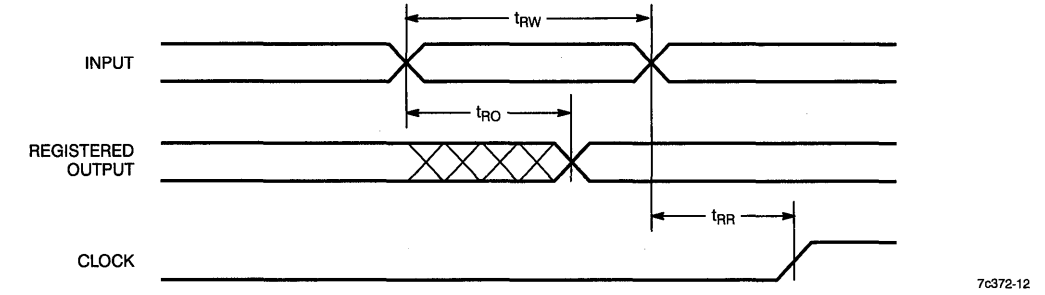


Switching Waveforms (continued)

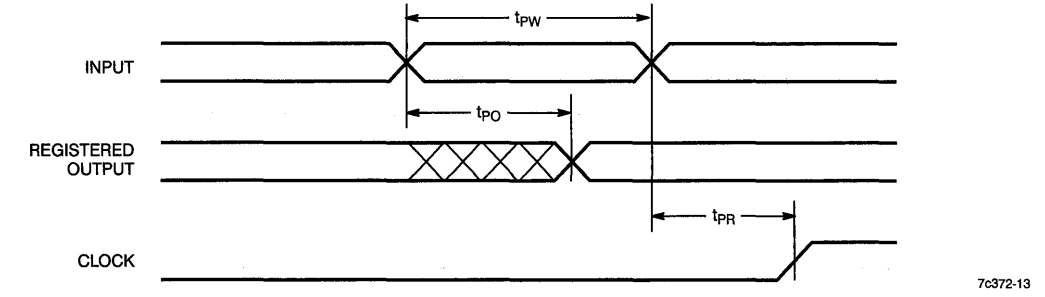
Latched Input and Output



Asynchronous Reset

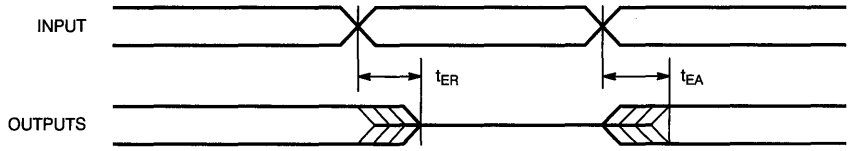


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



7c372-14

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C372–100JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
83	CY7C372–83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372–83LM	L67	44-Square Leadless Chip Carrier	Military
66	CY7C372–66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372–66LM	L67	44-Square Leadless Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

64-Macrocell Flash PLD

Features

- **64 macrocells in four logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **—f_{MAX} = 100 MHz**
  - **—t_{PD} = 12 ns**
  - **—t_S = 9 ns**
  - **—t_{CO} = 9 ns**
- **Electrically alterable Flash technology**
- **Available in 84-pin PLCC, CLCC, and CPGA packages**
- **Pin compatible with the CY7C374**

Functional Description

The CY7C373 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C373 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 64 macrocells in the CY7C373 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C373 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 64 I/O pins on the CY7C373. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C373 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C373 remain the same.

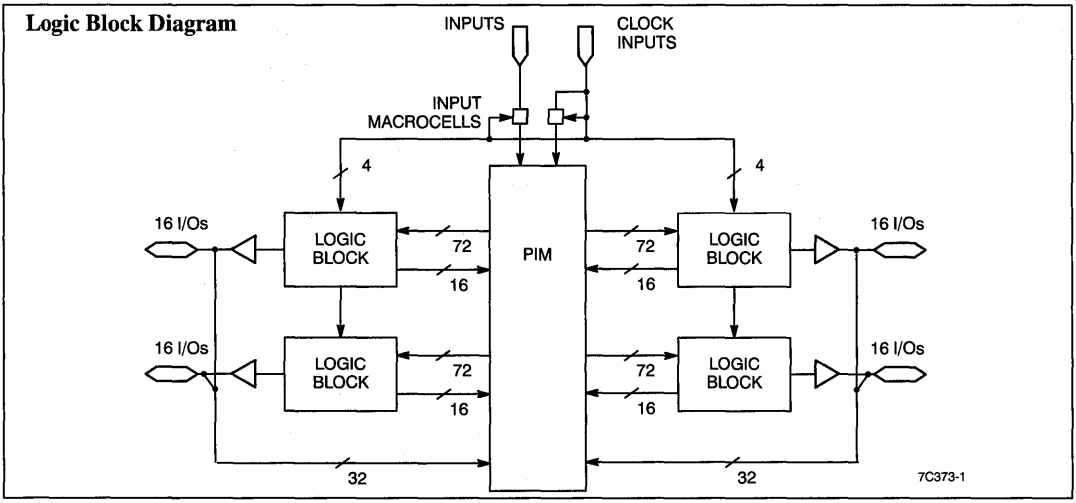
Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C373 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Logic Block Diagram



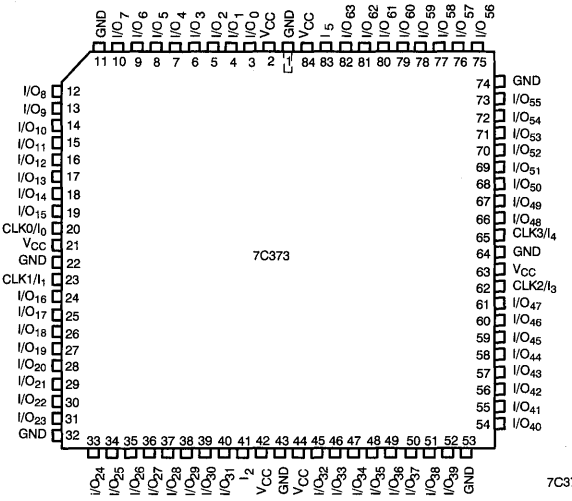
Selection Guide

		7C373-100	7C373-83	7C373-66
Maximum Propagation Delay t_{PD} (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	250	250	250
	Military		300	300
Maximum Operating Current, I_{CC2} (mA)	Commercial	280	280	280
	Military		330	330

Shaded area contains advanced information.

Pin Configuration

PLCC/CLCC/CQFP
Top View



7C373-2

Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product term resources to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that the product term allocator is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C373 has a separate I/O pin associated with it. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C373 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C373 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	– 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C373 Min.	7C373 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OL} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage				2.0	7.0	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		250	mA
				Mil		300	
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND, f = 40 MHz		Com'l		280	mA
				Mil		330	

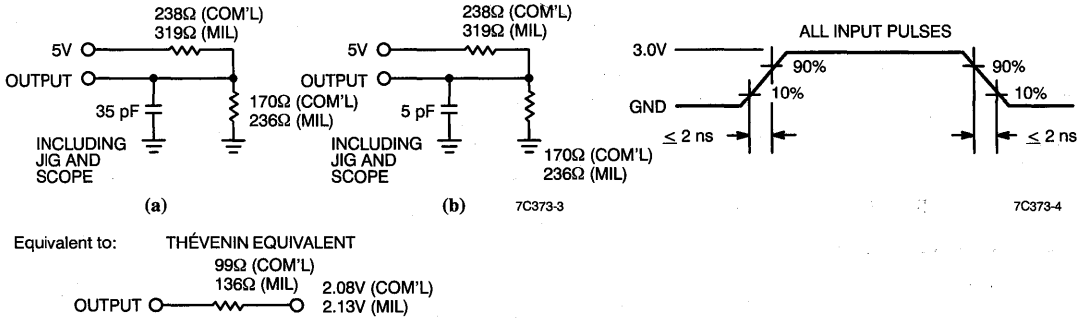
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C373–100		7C373–83		7C373–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C373s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	55.5		45.5		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C373s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	55.5		41.7		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	100		83		66		MHz
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:
5. All AC parameters are measured with 16 outputs switching.

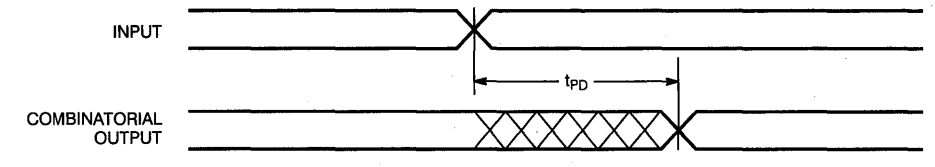
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C373–100		7C373–83		7C373–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

Shaded area contains advanced information.

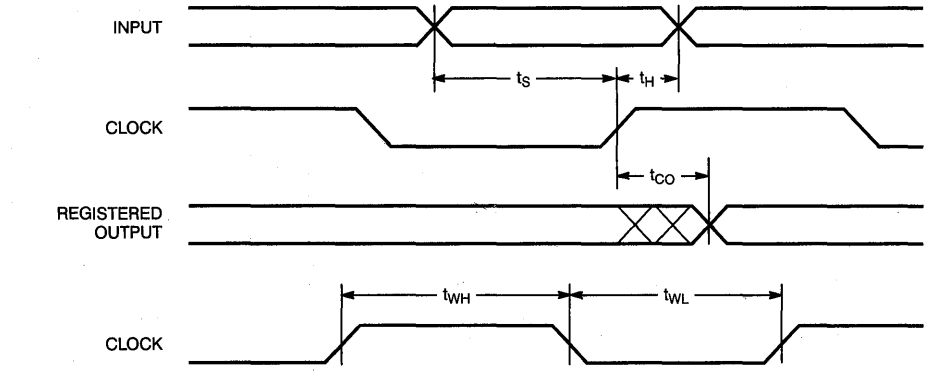
Switching Waveforms

Combinatorial Output



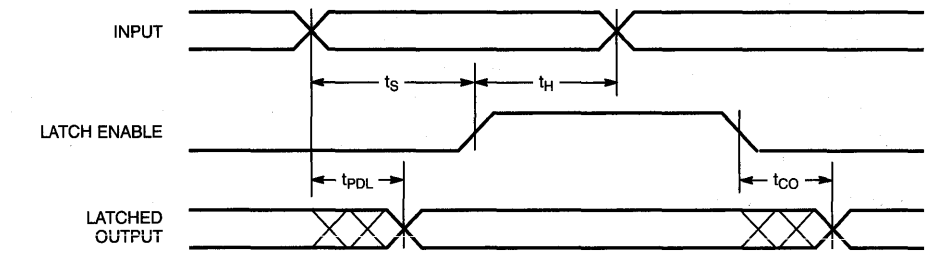
7C373-5

Registered Output



7C373-6

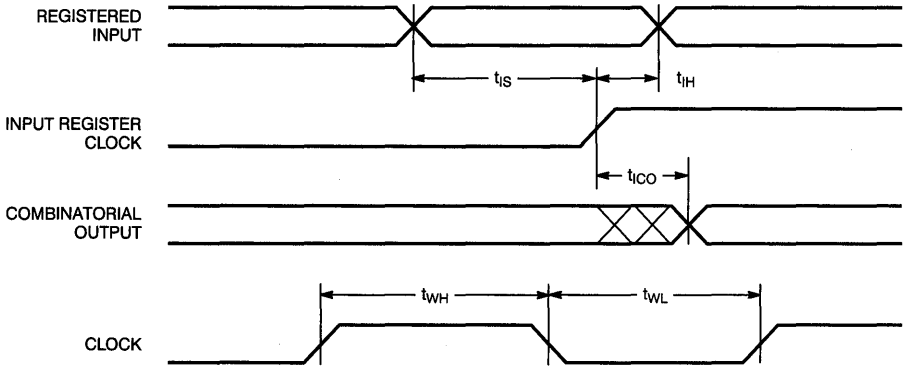
Latched Output



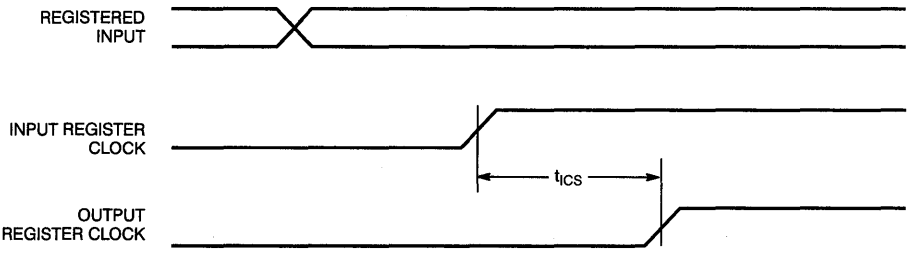
7C373-7

Switching Waveforms (continued)

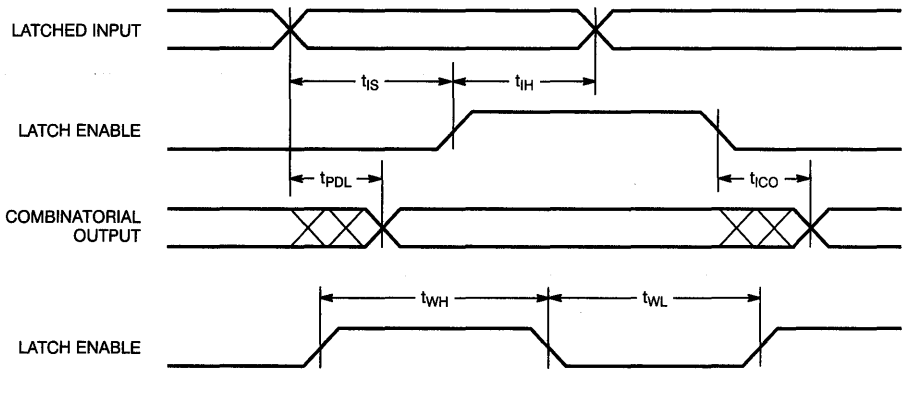
Registered Input



Input Clock to Output Clock



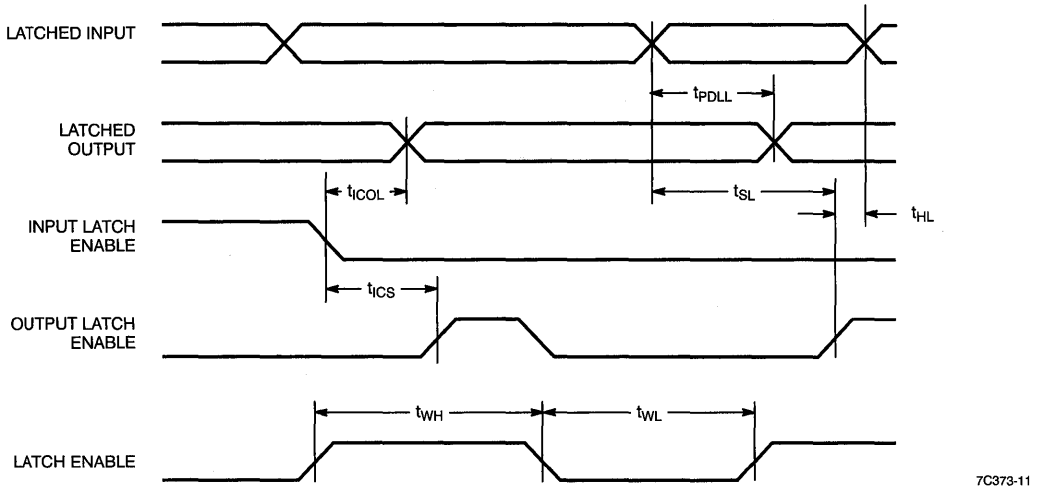
Latched Input



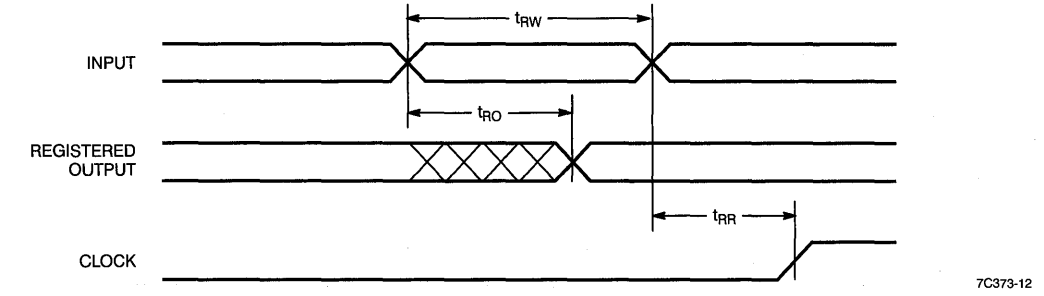
4 PLDs

Switching Waveforms (continued)

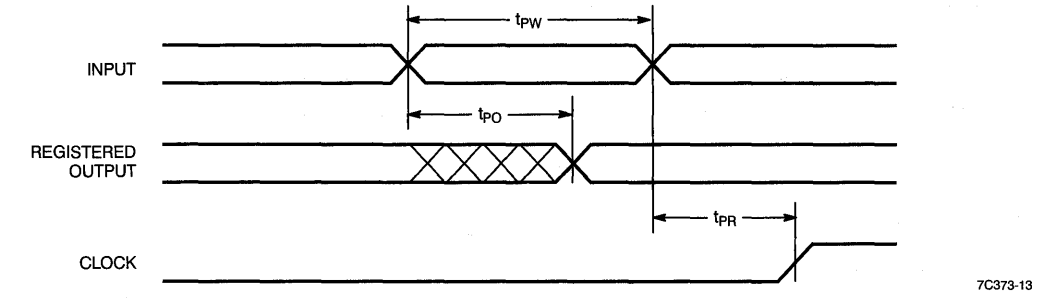
Latched Input and Output



Asynchronous Reset

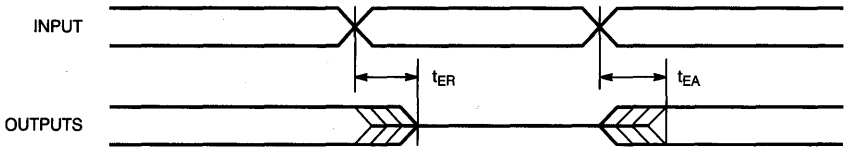


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



7C373-14

Ordering Information

Speed (MHz)	Ordering Code	Package Type	Package Type	Operating Range
100	CY7C373–100GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C373–100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C373–83GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C373–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373–83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military
66	CY7C373–66GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C373–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

Document #: 38–00216–A

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C374**

128-Macrocell Flash PLD

Features

- **128 macrocells in eight logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **—f_{MAX} = 100 MHz**
  - **—t_{PD} = 12 ns**
  - **—t_S = 9 ns**
  - **—t_{CO} = 9 ns**
- **Electrically Alterable Flash technology**
- **Available in 84-pin PLCC, CLCC, and CPGA packages**
- **Pin compatible with the CY7C373**

Functional Description

The CY7C374 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C374 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C374 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374 remain the same.

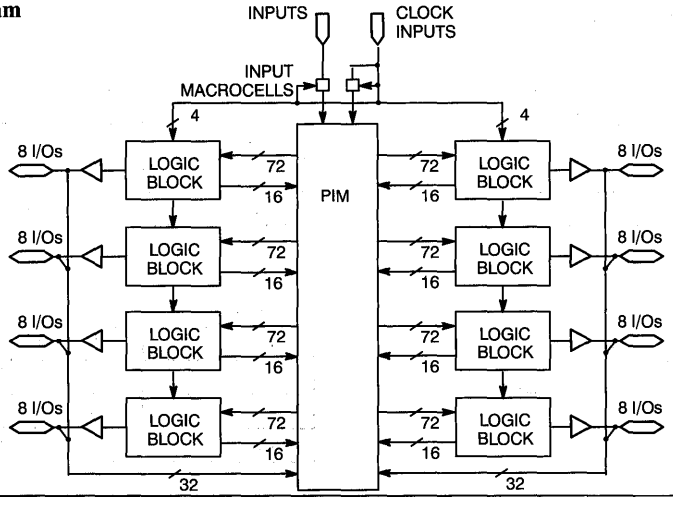
Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C374 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Logic Block Diagram



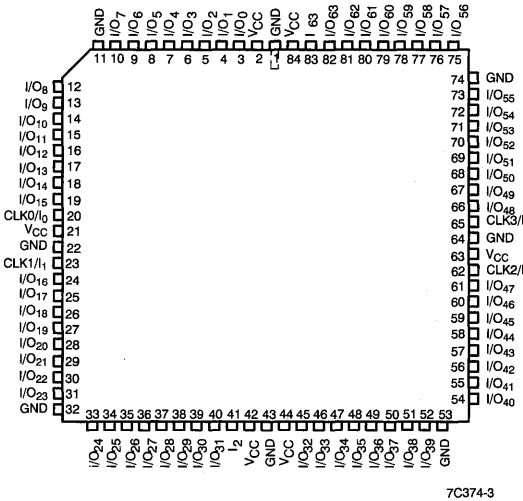
Selection Guide

		7C374–100	7C374–83	7C374–66
Maximum Propagation Delay t_{PD} (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	300	300	300
	Military		370	370
Maximum Operating Current, I_{CC2} (mA)	Commercial	330	330	330
	Military		400	400

Shaded area contains advanced information.

Pin Configurations

PLCC/CLCC
Top View



7C374-3

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O 23	I/O 25	I/O 26	I/O 28	I/O 31	I/O 33	V_{CC}	I/O 34	I/O 36	I/O 37	I/O 39
K	I/O 21	GND	I/O 24	I/O 27	I/O 30	I2	I/O 32	I/O 35	I/O 38	GND	I/O 41
J	I/O 20	I/O 22			I/O 29	V_{CC}	GND			I/O 40	I/O 42
H	I/O 18	I/O 19								I/O 43	I/O 44
G	CLK1 /I1	I/O 16	GND						CLK2 /I3	I/O 46	I/O 47
F	I/O 17	CLK0 /I0	V_{CC}						V_{CC}	I/O 45	GND
E	I/O 14	I/O 15	I/O 13						I/O 49	V_{CC} 48	CLK3 /I4
D	I/O 12	I/O 11								I/O 51	I/O 50
C	I/O 10	I/O 8	■		I/O 1	V_{CC}	I5			I/O 54	I/O 52
B	I/O 9	GND	I/O 6	I/O 3	I/O 0	I/O 61	I/O 63	I/O 59	I/O 56	GND	I/O 53
A	I/O 7	I/O 5	I/O 4	I/O 2	V_{CC}	GND	I/O 62	I/O 60	I/O 58	I/O 57	I/O 55

7C374-2

Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374 have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register whose input comes from the I/O pin associated with the neighboring macrocell. The ouptut of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C374 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C
Ambient Temperature with
Power Applied ..... – 55°C to +125°C
Supply Voltage to Ground Potential ..... – 0.5V to +7.0V
DC Voltage Applied to Outputs
in High Z State ..... – 0.5V to +7.0V
DC Input Voltage ..... – 0.5V to +7.0V
DC Program Voltage 12.5V
Output Current into Outputs ..... 16 mA
Static Discharge Voltage ..... >2001V
(per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

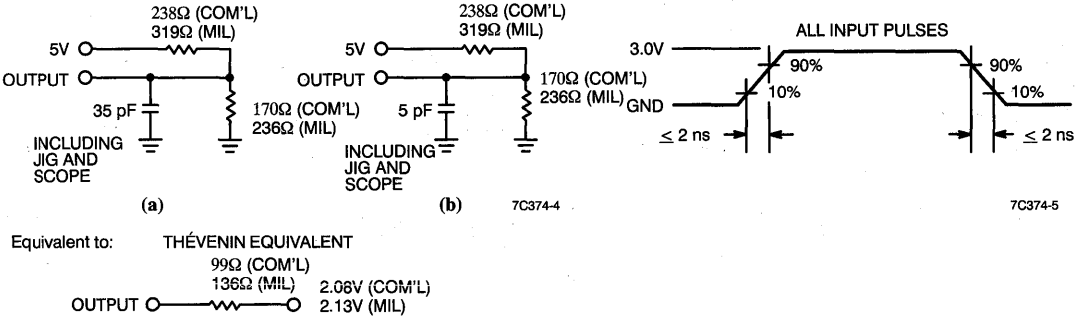
Parameter	Description	Test Conditions			7C374 Min.	7C374 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OL} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage				2.0	7.0	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		300	mA
				Mil		370	
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND, f = 40 MHz		Com'l		330	mA
				Mil		400	

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C374–100		7C374–83		7C374–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C374s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	55.5		45.5		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C374s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	55.5		41.7		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	100		83		66		MHz
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:

5. All AC parameters are measured with 16 outputs switching.

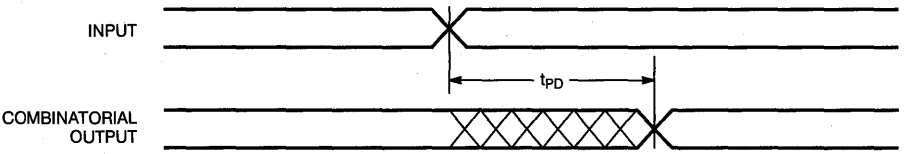
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C374–100		7C374–83		7C374–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

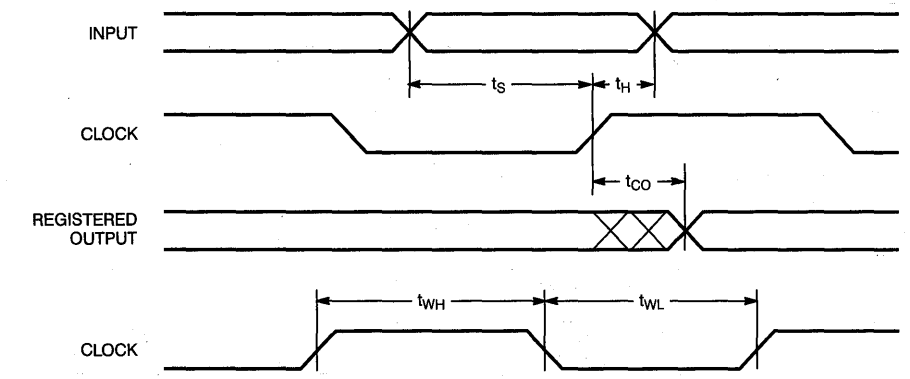
Shaded area contains advanced information.

Switching Waveforms

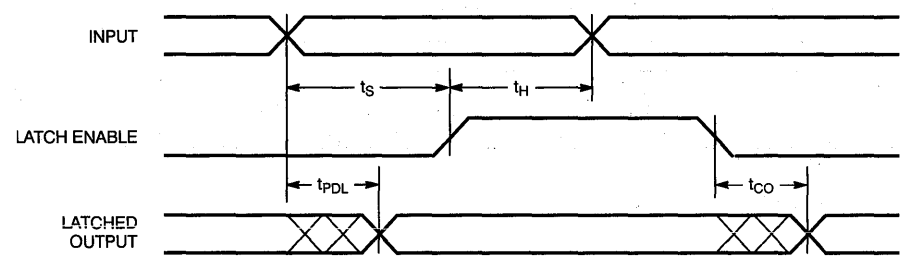
Combinatorial Output



Registered Output

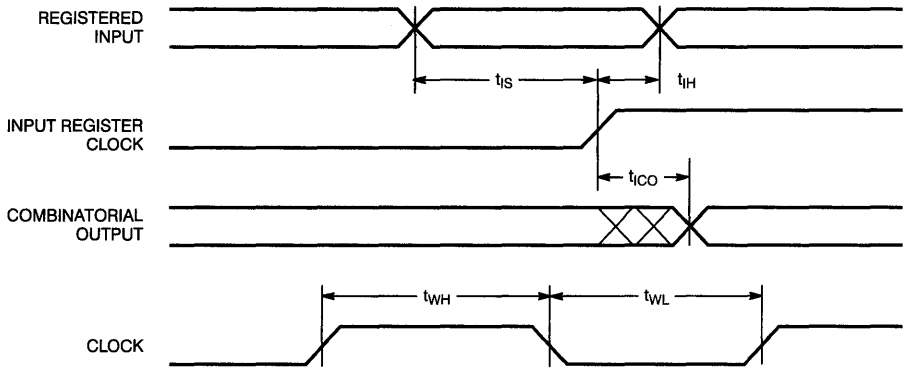


Latched Output

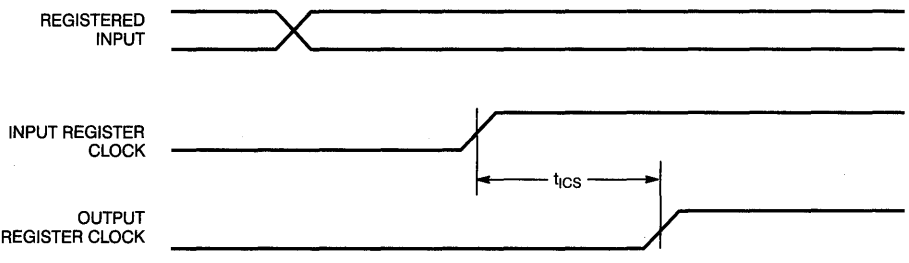


Switching Waveforms (continued)

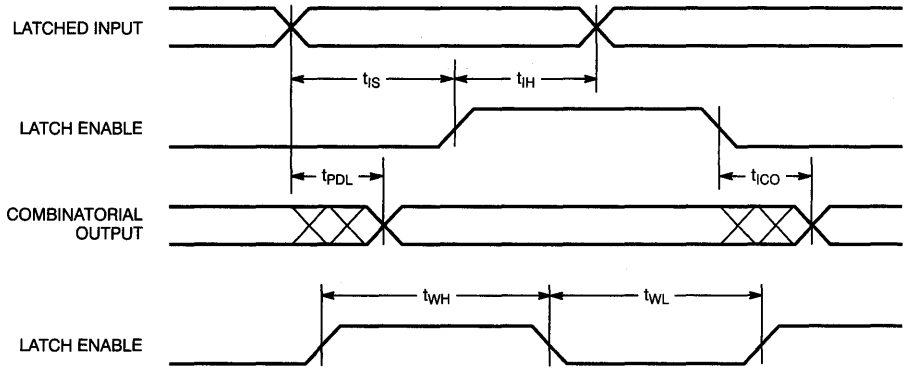
Registered Input



Input Clock to Output Clock

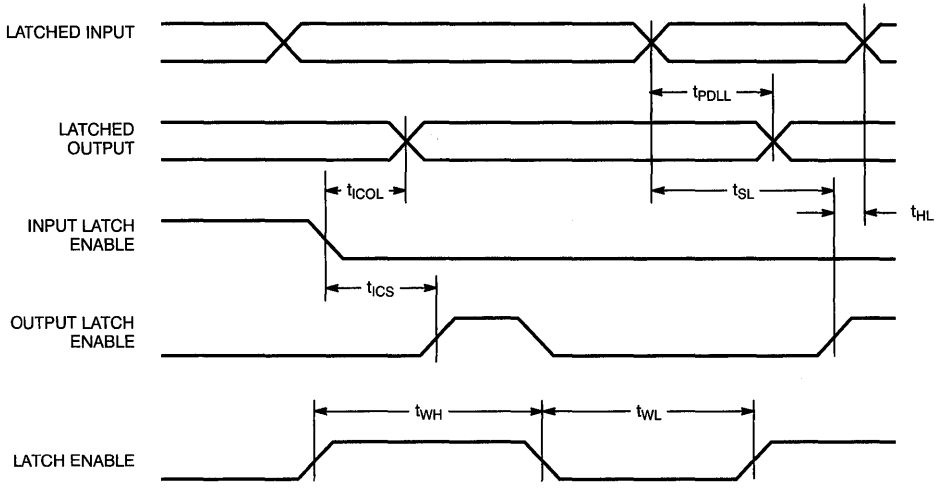


Latched Input

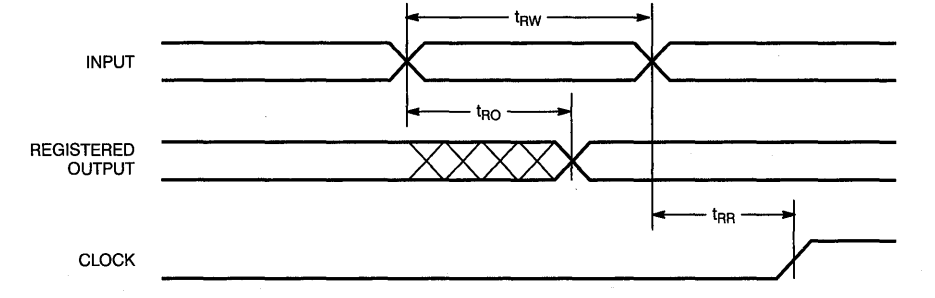


Switching Waveforms (continued)

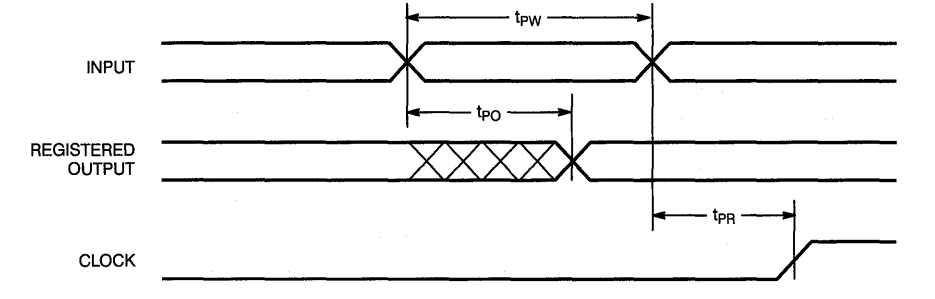
Latched Input and Output



Asynchronous Reset

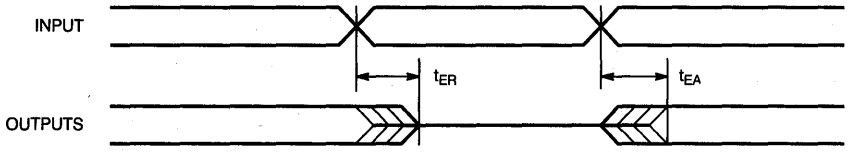


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



7C374-15

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C374–100GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C374–100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374–83GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C374–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374–83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military
66	CY7C374–66GC	G84	84-PGA (Cavity Up)	Commercial
	CY7C374–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

Document #: 38–00214–A

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C375**

128-Macrocell Flash PLD

Features

- **128 macrocells in eight logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - $-f_{MAX}$ = 100 MHz
  - $-t_{PD}$ = 12 ns
  - $-t_S$ = 9 ns
  - $-t_{CO}$ = 9 ns
- **Electrically alterable FLASH technology**
- **Available in 160-pin PQFP and CPGA packages**

Functional Description

The CY7C375 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C375 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

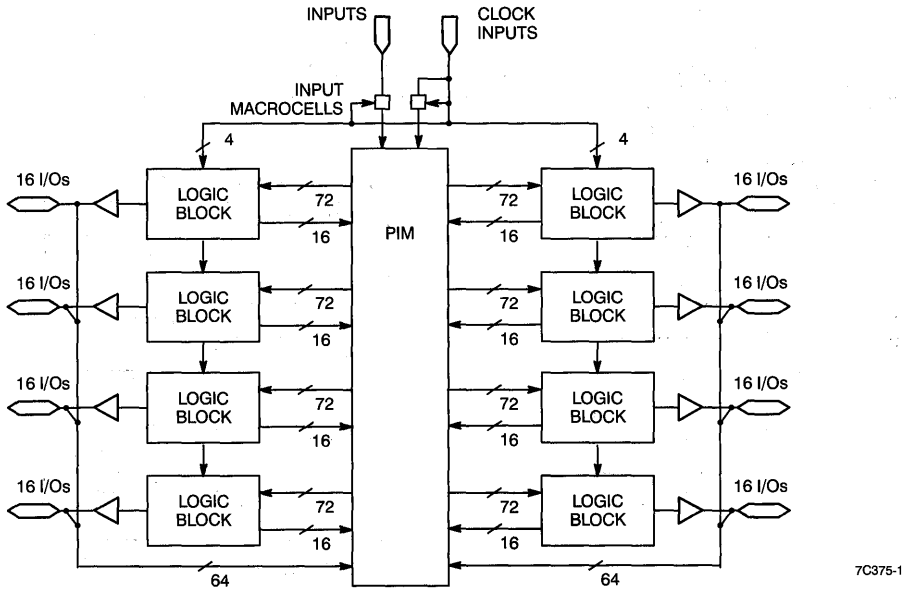
The 128 macrocells in the CY7C375 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C375 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 128 I/O pins on the CY7C375. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C375 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C375 remain the same.

Logic Block Diagram



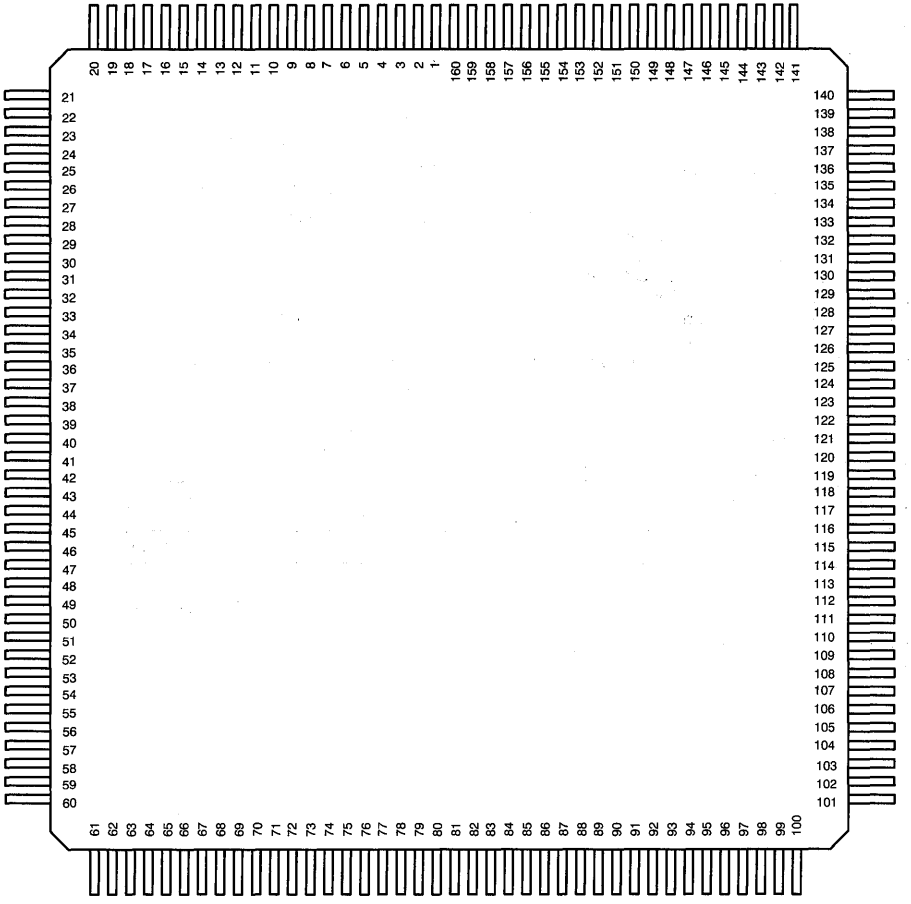
Selection Guide

		7C375–100	7C375–83	7C375–66
Maximum Propagation Delay (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	300	300	300
	Military		370	370
Maximum Operating Current, I_{CC2} (mA)	Commercial	330	330	330
	Military		400	400

Shaded area contains advanced information.

Pin Configuration

Ceramic Quad Flatpack (CQFP)
Top View



7C375-2

Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C375 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72x86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C375 has a separate I/O pin associated with it. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and four global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C375 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C375 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	− 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

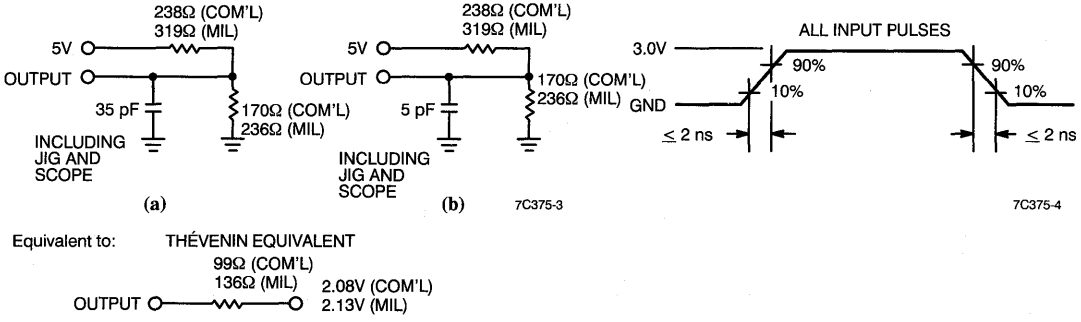
Parameter	Description	Test Conditions		7C375 Min.	7C375 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)	2.4		V
			I_{OL} = −2.0 mA (Mil)			V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)		0.5	V
			I_{OL} = 12 mA (Mil)			V
V_{IH}	Input HIGH Voltage			2.0	7.0	V
V_{IL}	Input LOW Voltage			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}	Com'l		300	mA
			Mil		370	
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND, f = 40 MHz	Com'l		330	mA
			Mil		400	

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C375–100		7C375–83		7C375–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C375s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	55.5		45.5		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C375s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	55.5		41.7		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	100		83		66		MHz
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:
5. All AC parameters are measured with 16 outputs switching.

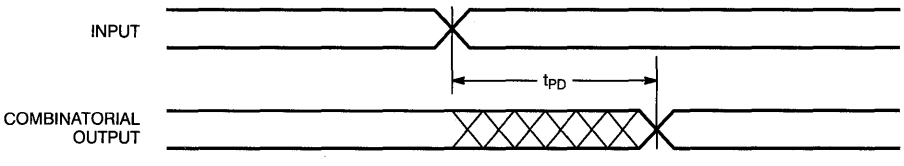
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C375–100		7C375–83		7C375–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

Shaded area contains advanced information.

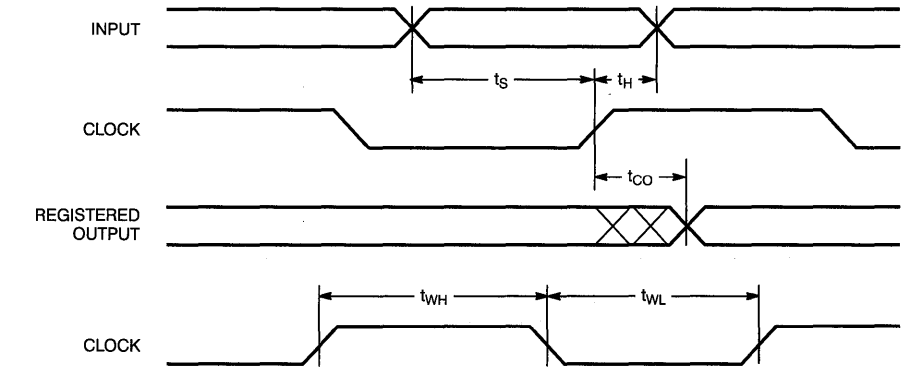
Switching Waveforms

Combinatorial Output



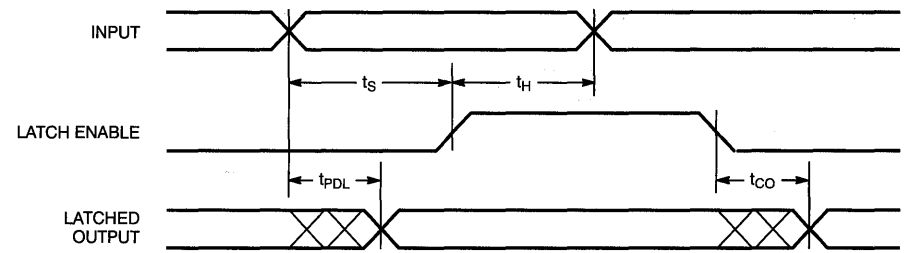
7C375-5

Registered Output



7C375-6

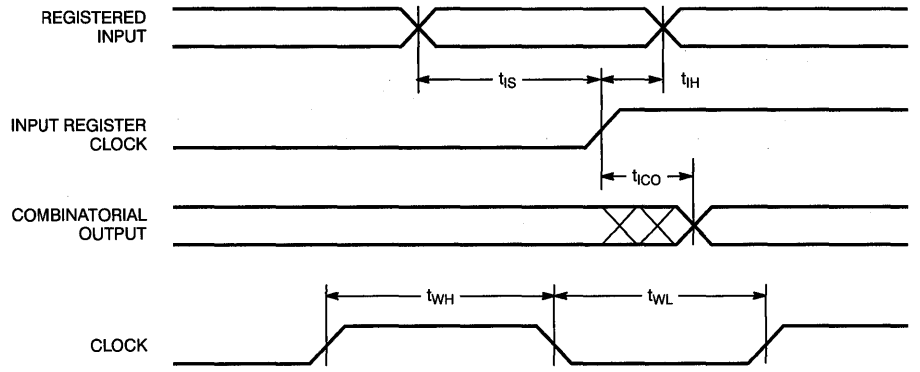
Latched Output



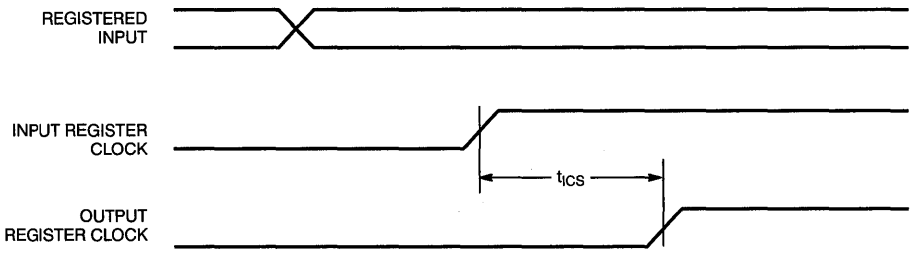
7C375-7

Switching Waveforms (continued)

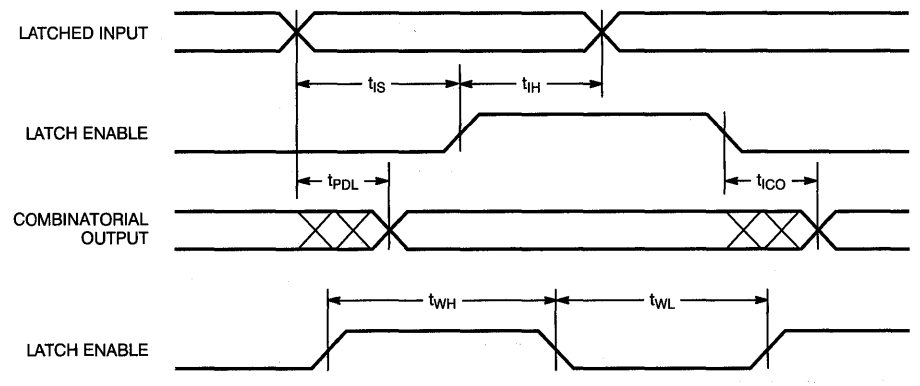
Registered Input



Input Clock to Output Clock

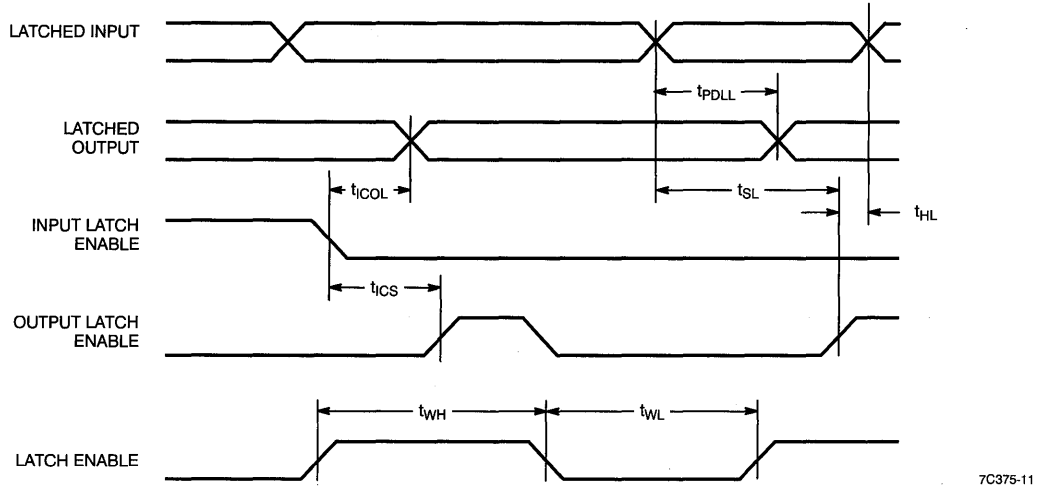


Latched Input

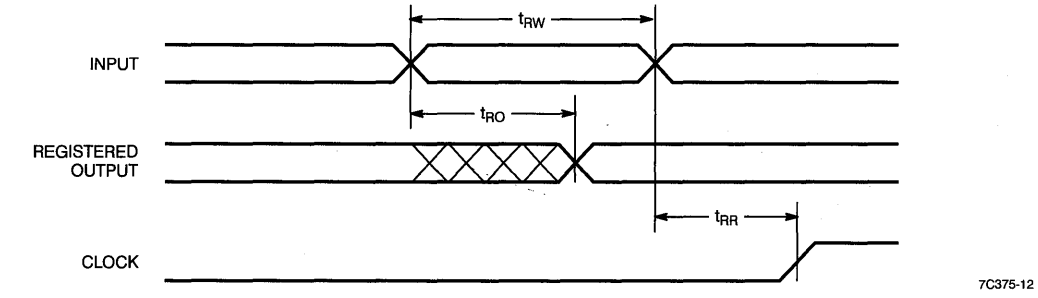


Switching Waveforms (continued)

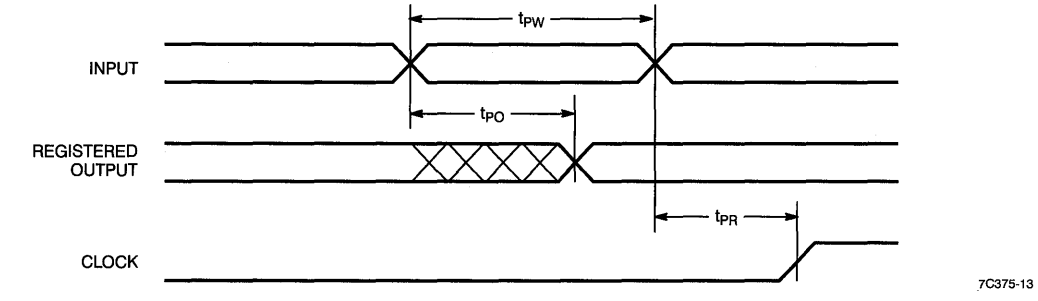
Latched Input and Output



Asynchronous Reset

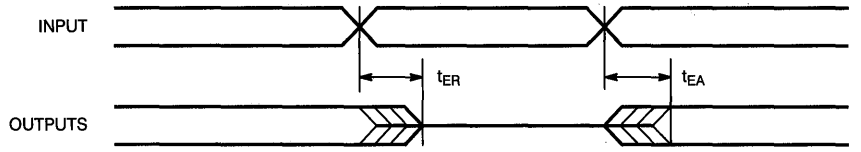


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



7C375-14

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C375–100NC	N160	160-Lead PQFP	Commercial
83	CY7C375–83NC	N160	160-Lead PQFP	Commercial
	CY7C375–83GMB	G160	160-Pin PGA	Military
66	CY7C375–66NC	N160	160-Lead PQFP	Commercial
	CY7C375–66GMB	G160	160-Pin PGA	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

Document #: 38–00217–A

CYPRESS SEMICONDUCTOR

256-Macrocell Flash PLD

Features

- **256 macrocells in 16 logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **— t_{PD} = 15 ns**
  - **— t_S = 12 ns**
  - **— t_{CO} = 12 ns**
- **Electrically alterable Flash technology**
- **Available in 160-pin PGA and PQFP packages**
- **Pin compatible with the CY7C375**

Functional Description

The CY7C376 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C376 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 256 macrocells in the CY7C376 are divided between sixteen logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

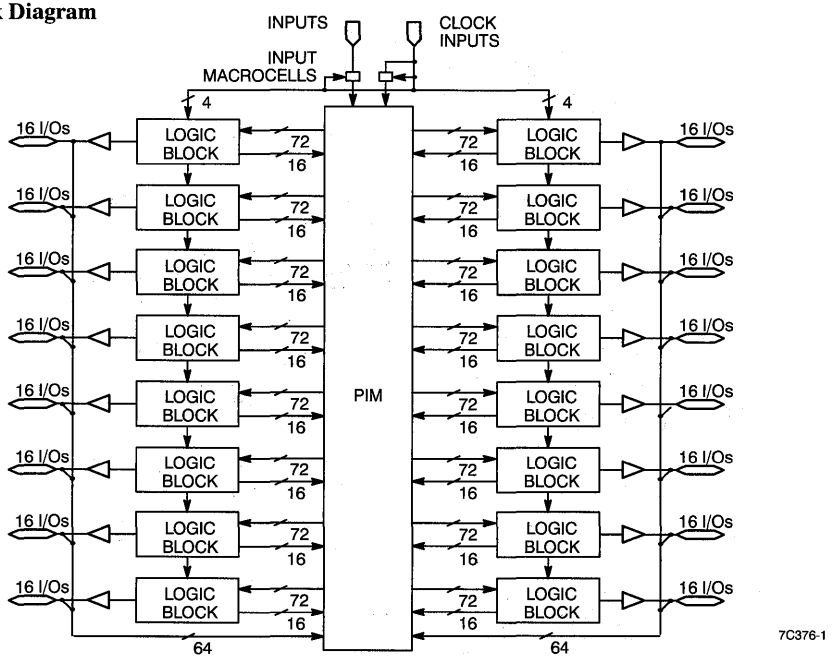
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C376 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 128 I/O pins on the CY7C376. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C376 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C376 remain the same.

4 PLDs

Logic Block Diagram



Document #: 38–00225

CYPRESS SEMICONDUCTOR

256-Macrocell Flash PLD

Features

- **256 macrocells in 16 logic blocks**
- **256 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **— t_{PD} = 15 ns**
  - **— t_S = 12 ns**
  - **— t_{CO} = 12 ns**
- **Electrically alterable Flash technology**
- **Available in 288-pin PGA and PQFP packages**

Functional Description

The CY7C377 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C377 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

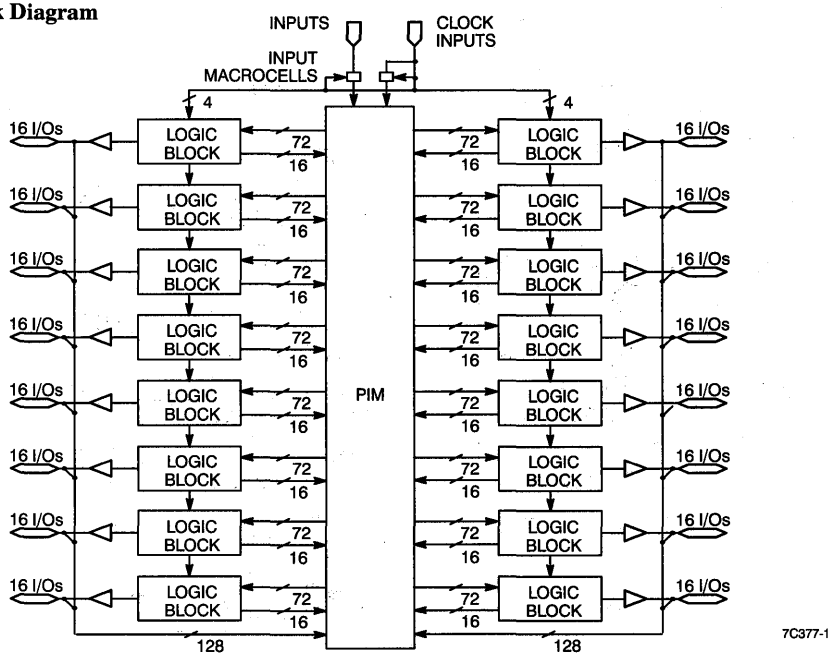
The 256 macrocells in the CY7C377 are divided between sixteen logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C377 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 256 I/O pins on the CY7C377. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C377 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C377 remain the same.

Logic Block Diagram



Document #: 38–00226

CYPRESS SEMICONDUCTOR

Very High Speed CMOS FPGAs

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 9 ns**
- **High usable density**
  - **Up to 4,000 "gate array" gates, equivalent to 12,000 EPLD or LCA gates**
  - **Technology migration path to 20,000 gates and above**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible FPGA architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (3.4 ns)**
- **Low-cost, easy-to-use design tools**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**

Functional Description

The pASIC380 family of very high speed CMOS user-programmable ASIC devices is based on the first FPGA technology to combine high speed, high density, and low power in a single architecture.

All pASIC380 family devices are based on an array of highly flexible logic cells that have been optimized for efficient implementation of high-speed arithmetic, counter, data path, state machine, and glue logic functions. Logic cells are configured and interconnected by rows and columns of routing metal lines and ViaLink metal-to-metal programmable-via interconnect elements.

ViaLink technology provides a non-volatile, permanently programmed custom logic function capable of operating at speeds of over 100 MHz. Internal logic cell delays are under 4 ns and total input to output combinatorial logic delays are under 10 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PALs™, GALs™, and discrete logic elements.

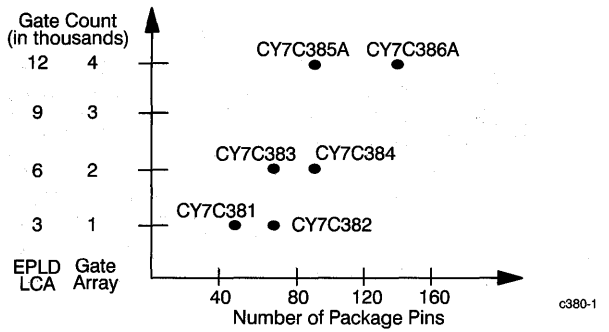
pASIC380 Family devices range in density from 1000 "gate array" gates (3,000 EPLD/LCA gates) in 44- and 68-pin packages to 4,000 (12,000) gates in 84- and 144-pin packages.

All devices share a common architecture and CAE design software to allow easy transfer of designs from one product to another. The small size of the ViaLink programming element insures a technology migration path to devices of 20,000 gates or more.

Designs are entered into the pASIC380 Family devices on PC or workstation platforms using third-party, general-purpose design-entry and simulation CAE packages, together with Cypress device-specific place and route and programming tools. Sufficient on-chip routing channels are provided to allow fully automatic place and route of desings using up to 100 percent of the available logic cells.

All the necessary hardware, software, documentation and accessories required to complete a design, from entering a schematic to programming a device are included in *Warp3*™, available from Cypress. *Warp3* includes a schematic capture system together with a waveform-based timing simulator. In addition to schematic entry, users can describe designs using VHDL. All applications run under Microsoft Windows™ graphical user interface to insure a highly productive and easy-to-use design environment. Sun workstation and other UNIX platforms will also be available.

pASIC380 Family Members



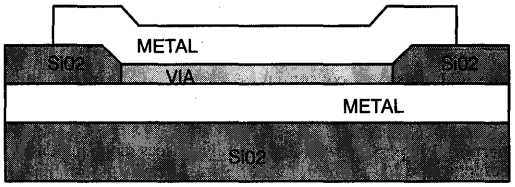


Figure 1. Unprogrammed ViaLink Element

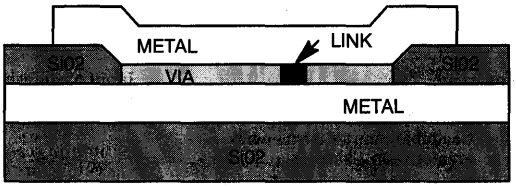


Figure 2. Programmed ViaLink Element

ViaLink Programming Element

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC380 devices, the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values as a low as 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

Figure 1 shows an unprogrammed ViaLink site. In a custom metal masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through the via. In a ViaLink programmable ASIC device, the two layers of metal are intially separated by an insulating semiconductor layer with resistence in excess of 1 gigaohm.

A programming pulse of 10 to 11 volts applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers, as shown in *Figure 2*. The tight distribution of link resistance is shown in *Figure 3*.

Standard CMOS Process

pASIC380 devices are the first FPGA devices to be fabricated on a conventional high-volume CMOS process. Initially, the base technology is a 1-micron, n-well CMOS technology with a single polysilicon layer and two layers of metal interconnect. The only deviation from the standard process flow occurs when the ViaLink module is inserted between the metal deposition steps.

As the size of a ViaLink is identical to that of a standard metal interconnect via, programmable elements can be packed very densely. The microphotograph in *Figure 4* shows an array of ViaLink elements. The density is limited only by the minimum dimensions of the metal-line pitch. Migration of the current process from 1-micron to Cypress's 0.65-micron process will allow the development of pASIC380 devices with tens of thousands of usable gates.

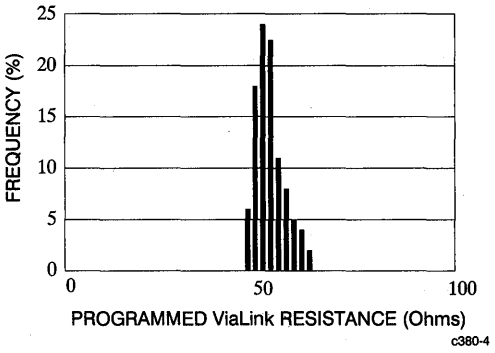


Figure 3. Distribution of Programmed Link Resistance

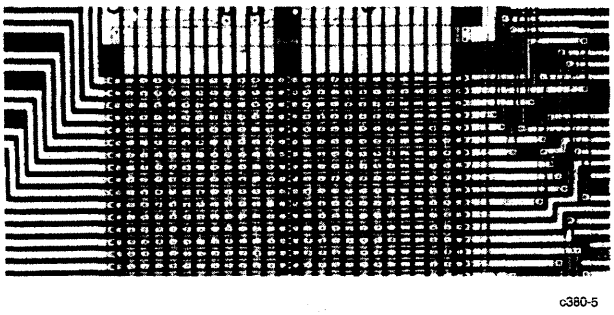


Figure 4. An Array of ViaLink Elements

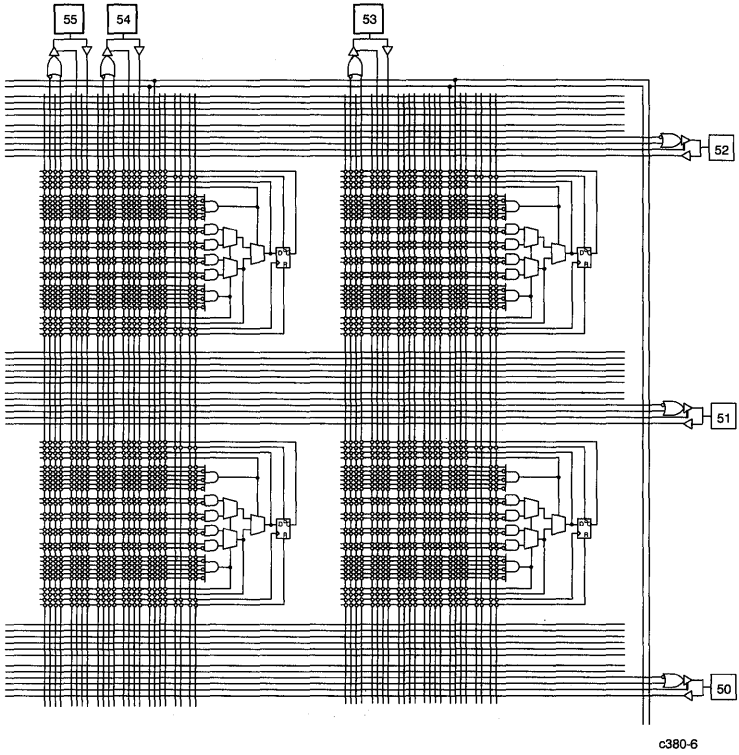


Figure 5. A Matrix of Logic Cells and Wiring Channels

The pASIC380 device architecture consists of an array of user-configurable logic building blocks, called logic cells. *Figure 5* shows a section of a pASIC380 device containing internal logic cells, input/output cells, and dual-layer vertical and horizontal metal routing channels. Through ViaLink elements located at the wire intersections, the output of any cell may be programmed to connect to the input of any other cell.

The regularity and orthogonality of this interconnect, together with the capability to achieve 100 percent routability of logic cells makes the pASIC380 architecture closer in structure and performance to a metal-masked gate array than any other FPGA family. It also makes system operating speed far less sensitive to partitioning and placement decisions, thus minor revisions to a logic design usually result in only small changes in performance.

Organization

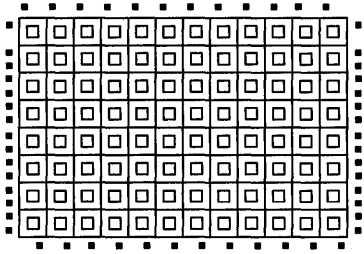
The pASIC380 Family of very high speed FPGAs contains devices covering a wide spectrum of I/O and density requirements. Four members, ranging from 1000 gates in 44- and 68-lead packages to 4,000 gates in 84- and 144-lead packages, are shown in *Figure 6*. The single lines between logic cells represent channels containing up to twenty-two wires.

The key features of all five pASIC380 devices are listed in *Table 1*. See the individual product datasheets for more specific information on each device.

Individual part numbers indicate unique logic cell and I/O cell combinations. For example, the CY7C383 contains 192 logic cells and 56 I/O cells in a 68-pin package. The CY7C384 also contains 192 logic cells, but it has 68 I/O cells and is packaged in 84- and 100-pin packages. Note that at each pASIC380 density there is a density upgrade available in the same package. In other words, the CY7C383 features 2,000 gates in the same pinout as the 1,000-gate CY7C382. The same applies to the CY7C385A and CY7C384.

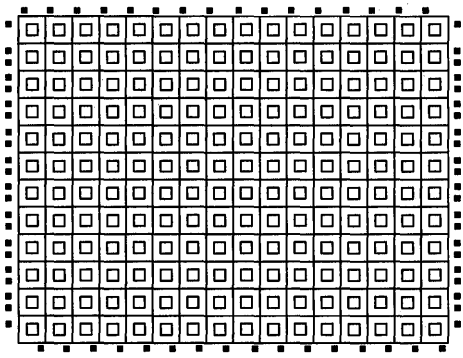
Gate counts for pASIC380 devices are based on the number of usable or "gate array" gates. Each of the internal logic cells has a total logic capacity of up to 30 gates. As a typical application will use 10 to 12 of these gates, the usable gate count is significantly lower than the total number of available gates. On the pASIC380 product family, Cypress uses the more conservative usable (gate array) gate method of specifying density. Total available gate densities may also be specified as EPLD/LCA gates.

CY7C381, 382

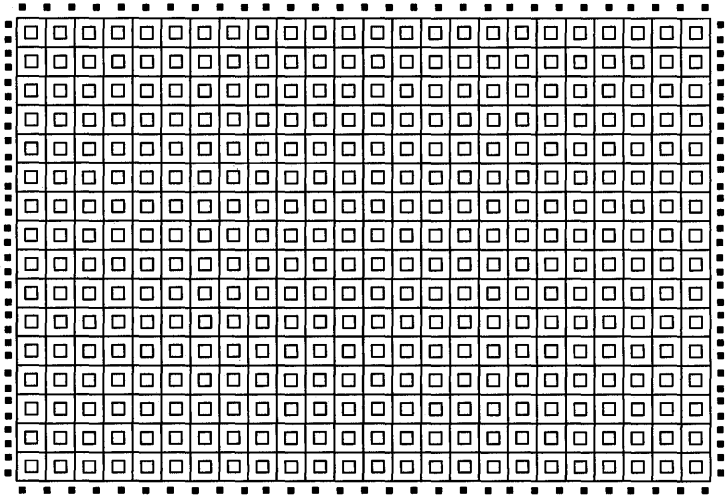


■ I/O/HIGH-DRIVE INPUT/ CLOCK CELLS

CY7C383, 384



CY7C385A, 386A



c380-7

Figure 6. pASIC380 Family Members

Table 1. Key Features of pASIC380 Devices

Device	Logic Cells	I/O Cells	Dedicated Inputs	Usable Gates	EPLD/LCA Gates	Packages
7C381	96	32	8	1000	3000	44-Pin PLCC
7C382	96	56	8	1000	3000	68-Pin PLCC, PGA 100-Pin TQFP
7C383	192	56	8	2000	6000	68-Pin PLCC, PGA
7C384	192	68	8	2000	6000	84-Pin PLCC, PGA 100-Pin TQFP
7C385A	384	68	8	4000	12000	84-Pin PLCC, PGA 100-Pin TQFP
7C386A	384	114	8	4000	12000	144-Pin TQFP 145-Pin PGA

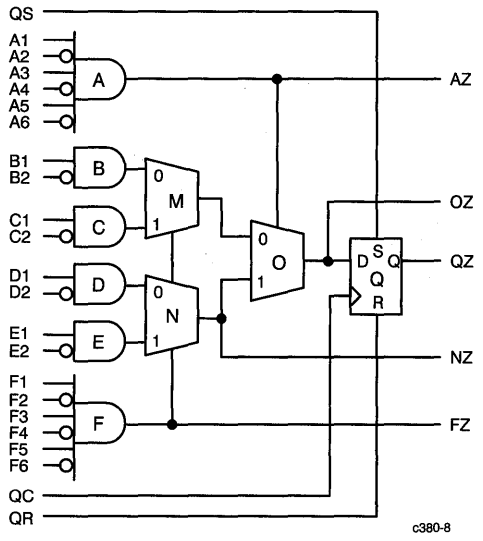


Figure 7. pASIC380 Internal Logic Cell

pASIC380 Internal Logic Cell

The pASIC380 internal logic cell, shown in *Figure 7*, is a general-purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while insuring maximum logic flexibility.

The logic cell consists of two 6-input AND gates, four 2-input AND gates, three 2-to-1 multiplexers and a D flip-flop. As noted above, each cell represents approximately 30 gate-equivalents of logic capability. The pASIC380 logic cell is unique among FPGA architectures in that it offers up to 14-input-wide gating functions. It can implement all possible Boolean transfer functions of up to three variables as well as many functions of up to 14 variables.

Glitch-free switching of the multiplexer is insured because the internal capacitance of the circuit maintains enough charge to hold the output in a steady state during input transitions. The multiplexer output feeds the D-type flip-flop, which can also be configured to provide JK-, SR-, or T-type functions as well as count with carry-in. Two independent SET and RESET inputs can be used to asynchronously control the output condition. The combination of wide gating capability and a built-in register makes the pASIC380 logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

Each pASIC380 logic cell features five separate outputs. The existance of multiple outputs makes it easier to pack independant functions into a single logic cell. For example, if one function requires a single register, both 6-input AND gates (A and F) are available for other uses. Logic packing is accomplished automatically by *Warp3* software.

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

The pASIC380 macro library contains more than 200 of the most frequently used logic funcitons already optimized to fit the logic cell architecture. A detailed understanding of the logic cell is therefore not necessary to successfully design with pASIC380 devices. CAE tools will automatically translate a conventional logic schematic and/or VHDL source code into a device and provide excellent performance and utilization.

Three types of input and output structures are provided on pASIC380 devices to configure buffering functions at the external pads. They are called the Bidirectional Input/Output (I/O) cell, the Dedicated Input (I) cell, and the Clock/Dedicated Input (CLK/I) cell.

The bidirectional I/O cell, shown in *Figure 8*, consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

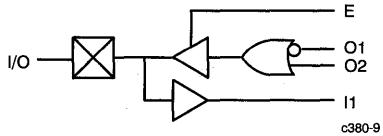


Figure 8. Bidirectional I/O Cell

The Dedicated Input cell, shown in *Figure 9*, conveys true and complement signals from the input pads into the array of logic cells. As these pads have nearly twice the current drive capability of the I/O

pads, they are useful for distributing high fanout signals across the device.

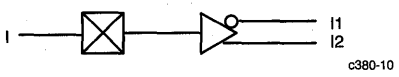


Figure 9. Dedicated Input High-Drive Cell

The Clock/Dedicated Input cell (*Figure 10*) drives a low-skew, fan-out-independent clock tree that can connect to the clock, set, or reset inputs of the logic cell flip-flops. The CY7C384, for example, has 68 I/O cells, 6 I cells, and 2 I/CLK cells.

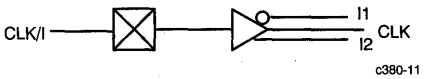


Figure 10. Clock/Dedicated Input Cell

pASIC380 Interconnect Structure

Multiple logic cells are joined together to form a complex logic function by interconnection through the routing channels. To describe the organization of these routing channels, a hypothetical 14-pin device consisting of two logic cells is shown in *Figure 11*. This device contains the same architectural features as the members of the pASIC380 family.

Active logic functions are performed by the internal logic cells, the I/O cells (pins 2, 3, 7, 9, 10, and 14) and the I cells (pins 4, 6, 11, and 13). These cells are connected with vertical and horizontal wiring channels.

Three types of signal wires are employed: segmented wires, express wires, and clock wires. Segmented wires are predominantly used for local connections and have ViaLink elements known as a Cross Link (denoted by the open box symbol), at every crossover point. They may also be connected to the segmented wires of cells above and below through ViaLink elements, called Pass Links (denoted by the X symbol). Express lines are similar to segmented wires except that they are not divided by Pass Links. Dedicated clock wires are lightly loaded with only three links per cell to distribute high-speed clock edges to the flip-flop CLK, SET, and RESET inputs. Express wires may also be used to deliver clock signals into the multiplexer region of the cell for combinatorial gating. The automatic place and route software allocates signals to the appropriate wires to insure the optimum speed/density combination.

Vertical V_{CC} and GND wires are located close to the logic cell gate inputs to allow any input that is not driven by the output of another cell to be automatically tied to either V_{CC} or GND. All of the vertical wires (segmented, express, clock, and power) considered as a group are called vertical channels. These channels span the full height of the device and run to the left of each column of logic cells.

Horizontal wiring channels, called rows, provide connections, via cross links, to other columns of logic cells and to the periphery of the chip. Appropriate programming of ViaLink elements allows electrical connection to be made from any logic cell output to the input of any other logic or I/O cell. Ample wires are provided in the channels to permit automatic place and route of many designs using up to 100 percent of the device logic cells. Designs can be com-

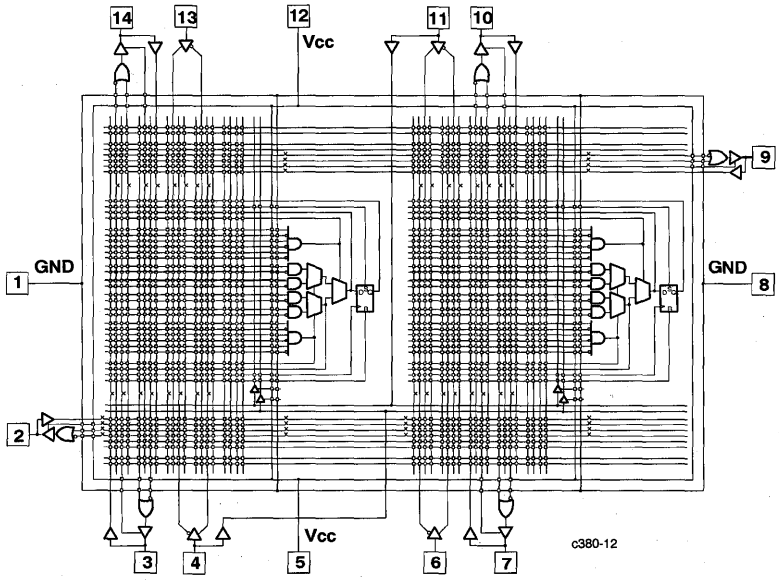


Figure 11. pASIC380 Device Features

pleted automatically even with a high percentage of fixed user placement of internal cells and pin locations.

This information is presented to provide the user with inisght into how a logic function is implemented in pASIC380 devices. However, it is not necessary to develop a detailed understanding of the architecture in order to achieve efficient designs. All routine tasks are fully automatic. No manual wire routing is necessary, nor is it permitted by the software. Fully automatic placement of logic functions is also offered. But if it is necessary to achieve a specific pin configuration or register alignment, for example, manual placement is supported.

Power Consumption

Typical standby power supply current consumption, I_{CC1}, of a pASIC380 device is 2 mA. The worst-case limit for standby current (I_{CC1}) over the full operating range of the pASIC380 devices is 10 mA. Formulas for calculating I_{CC} under AC conditions (I_{CC2}) are provided in the "pASIC380 Power vs. Operating Frequency" application note. As an example of the low-power consumption of pASIC380 devices, the 16-bit counter example detailed in the application note consumes just 50 mA at 100 MHz.

Programming and Testing

pASIC380 devices may be programmed and functionally tested on the Cypress Programmer supplied with the *Warp3* software. The unit is completely self contained. No add-in boards are required. Programming signals are donwloaded from the PC over an RS232 link. Third-party programmers are being qualified.

All pASIC380 device have a built-in serial scan path linking the logic cell register functions (*Figure 12*). This is provided to improve factory test coverage and to permit testing by the user with automatically generated test vectors following programming. Automatic Test Vector Generation software is included in *Warp3*. The Programmer permits a high degree of test coverage to be achieved conveniently and rapidly using test vectors optimized for the pASIC380 architecture.

Reliability

The pASIC380 Family is based on a 1-micron high-volume CMOS fabrication process with the VIALink programmable-via antifuse technology inserted between the metal deposition steps. The base CMOS process has been qualified to meet the requirements of MIL-STD-883B, Revision C.

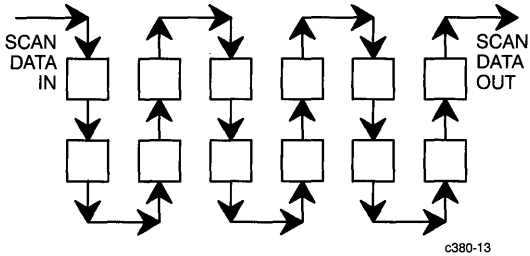


Figure 12. Internal Serial Scan Path

The ViaLink element exists in one of two states: a highly resistive unprogrammed state, OFF, and the low-impedance, conductive state, ON. It is connected between the output of one logic cell and the inputs of other logic cells directly or through other links. No DC current flows through either a programmed or an unprogrammed link during operation as a logic device. An unprogrammed link sees a worst-case voltage equal to V_{CC} biased across its terminals. A programmed link carries AC current caused by charging and discharging of device and interconnect capacitances during switching.

Study of test structures and complete pASIC380 devices has shown that an unprogrammed link under V_{CC} bias remains in the unprogrammed state over time. Similary tests on programmed links under current bias exhibit the same stability. The long-term reliability of the combined CMOS and ViaLink structure is similar to that of the base gate array process. For further details, see the pASIC380 Family Reliability Report.

Document #: 38–00210–A

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C381
CY7C382

Very High Speed 1K (3K) Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 9 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **8 x 12 array of 96 logic cells provides 3,000 total available gates**
  - **1,000 typically usable "gate array" gates in 44- and 68-pin PLCC/CPGA packages**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (3.4 ns)**
- **Low-cost, powerful design tools**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **32 (CY7C381) to 56 (CY7C382) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <1 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **68-pin PLCC is compatible with EPLD 1800 and LCA 2064 industry-standard pinouts**

Functional Description

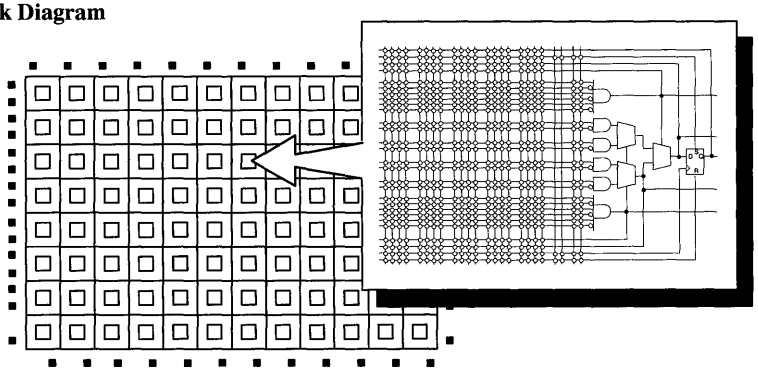
The CY7C381 and CY7C382 are members of the pASIC380 family of very high speed CMOS user-programmable ASIC (pASIC) devices. The 96 logic cell field-programmable gate array (FPGA) offers 1,000 typically usable "gate array" gates. This is equivalent to 3,000 EPLD or LCA gates. The CY7C381 is available in a 44-pin PLCC. The CY7C382 is available in a 68-pin PLCC and CPGA.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input and output delays under 4 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C381 and CY7C382 using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C381 and CY7C382 feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



■ I/O/HIGH-DRIVE INPUT CLOCK CELLS

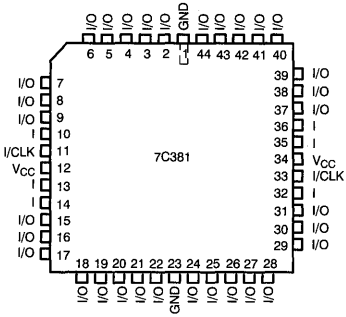
44 or 68 PINS, INCLUDING 56 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS

c381-1

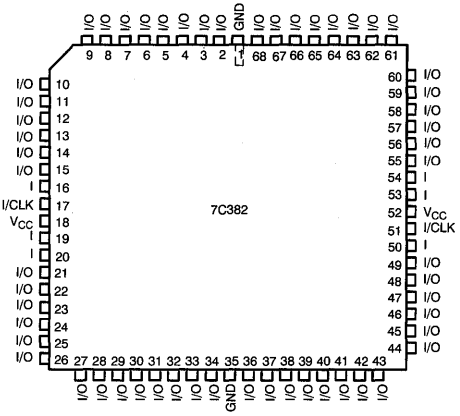
ViaLink is a trademark of QuickLogic Corporation.

Pin Configurations

PLCC
Top View



PLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... − 65°C to +150°C
Plastic ..... −40°C to +125°C

Lead Temperature ..... 300°C

Supply Voltage ..... − 0.5V to +7.0V

Input Voltage ..... − 0.5V to V_{CC} +0.5V

ESD Pad Protection ..... ±2000 V

DC Input Voltage ..... ±20 mA

Latch-Up Current ..... ±100 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40° to +85°C	5V ± 10%

Delay Factor (K)

Speed Grade	Industrial		Commercial	
	Min.	Max.	Min.	Max.
−0	0.4	1.67	0.46	1.55
−1	0.4	1.43	0.46	1.33
−2			0.46	1.25

Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0 mA	3.7		V
		I_{OH} = − 8.0 mA	2.4		V
		I_{OH} = − 10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = GND	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or GND		10	mA
I_{CC2}	Supply Current[1, 2]	f = 1.0 MHz, V_I = V_{CC} or GND		20	mA

Capacitance

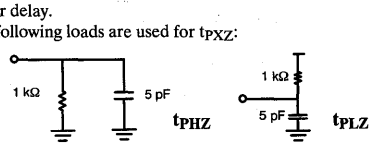
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Switching Characteristics Over the Operating Range

Parameter	Description	Propagation Delays[4] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[5]	3.4	3.8	4.2	4.8	8.1	ns
t_{SU}	Set-Up Time[5]	3.7	3.7	3.7	3.7	3.7	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9	ns
t_{SET}	Set Delay	2.7	3.1	3.5	4.1	7.4	ns
t_{RESET}	Reset Delay	2.9	3.2	3.6	4.2	7.5	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	3.6	3.6	3.6	3.6	3.6	ns
t_{SW}	Set Width	2.1	2.1	2.1	2.1	2.1	ns
t_{RW}	Reset Width	1.9	1.9	1.9	1.9	1.9	ns
INPUT CELLS							
t_{IN}	Input Delay (HIGH Drive)	3.7	3.8	4.2	4.6	6.4	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.5	3.6	4.0	4.4	6.2	ns
t_{IO}	Input Delay (Bidirectional Pad)	2.3	2.6	3.2	4.1	5.5	ns
t_{GCK}	Clock Buffer Delay [6]	4.4	4.5	4.6	4.6	5.0	ns
		Propagation Delays[4] with Output Load Capacitance (pF) of					
OUTPUT CELLS		**30**	**50**	**75**	**100**	**150**	
t_{OUTLH}	Output Delay LOW to HIGH	3.1	3.8	4.6	5.5	7.2	ns
t_{OUTHL}	Output Delay HIGH to LOW	3.1	3.9	5.0	6.1	8.3	ns
t_{PZH}	Output Delay Three-State to HIGH	4.4	5.3	6.5	7.7	10.1	ns
t_{PZL}	Output Delay Three-State to LOW	4.0	4.6	5.4	6.2	7.7	ns
t_{PHZ}	Output Delay HIGH to Three-State[7]	3.3	3.3	3.3	3.3	3.3	ns
t_{PLZ}	Output Delay LOW to Three-State[7]	3.7	3.7	3.7	3.7	3.7	ns

Notes:

1. Measured with six 16-bit counters configured internally and all outputs driving. To calculate power for your application, see the "pASIC380 Power vs. Operating Frequency" application note.
2. Guaranteed but not 100% tested.
3. C_I = 20 pF max. on pin 32 (7C381) or pin 50 (7C382).
4. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Mulitply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
5. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
6. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
7. The following loads are used for t_{PXZ}:

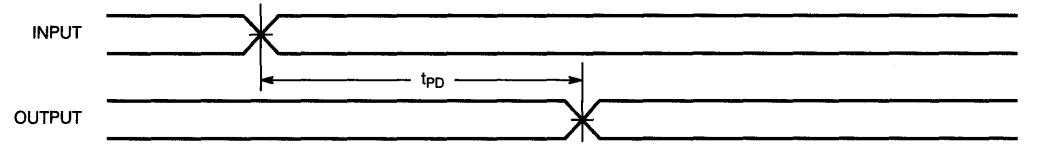


High Drive Buffer

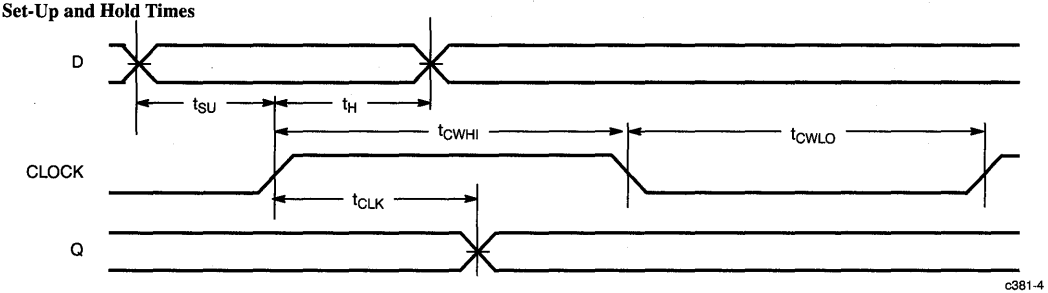
Parameter	Description	# High Drives Wired Together	Propagation Delays[4] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	7.9	11.2				ns
		2		8.0	9.7			ns
		3			8.6	10.4	11.8	ns
		4				9.4	10.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	7.5	10.8				ns
		2		7.5	9.3			ns
		3			8.2	10.0	11.8	ns
		4				9.0	10.8	ns

Switching Waveforms

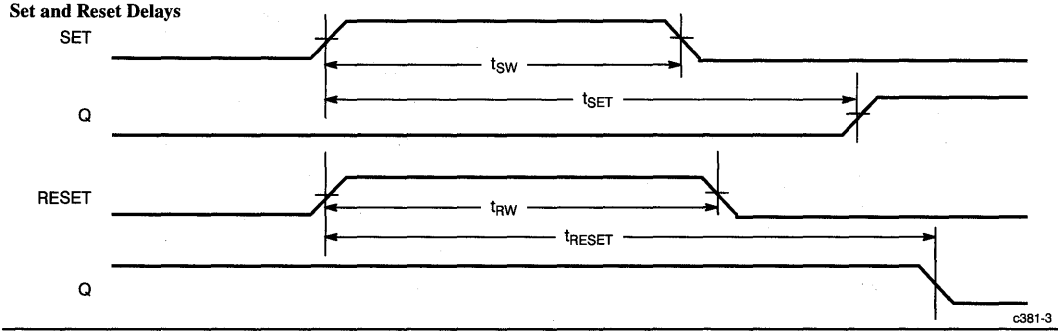
Combinatorial Delay



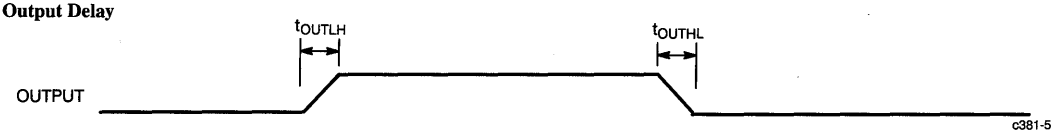
Set-Up and Hold Times



Set and Reset Delays

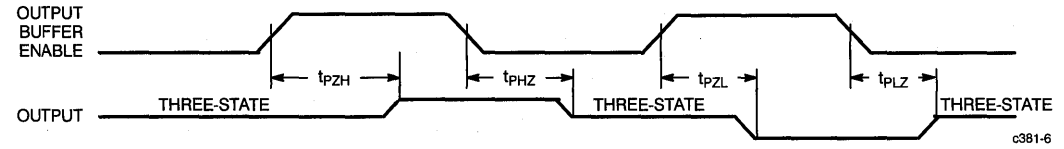


Output Delay



Switching Waveforms (continued)

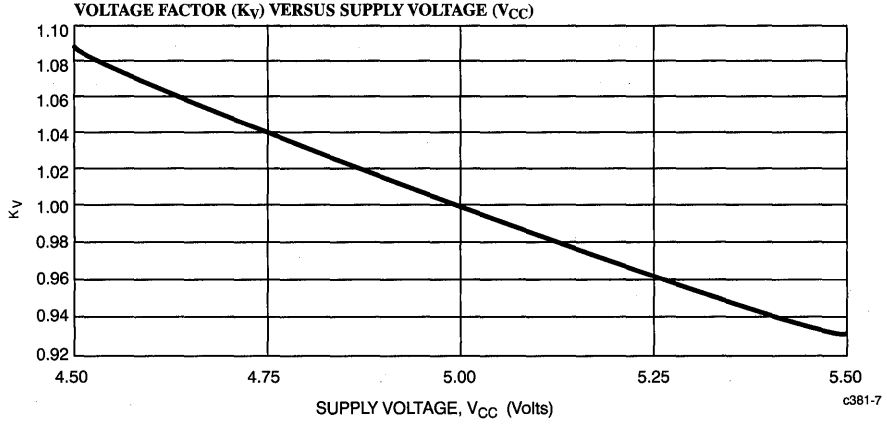
Three-State Delay



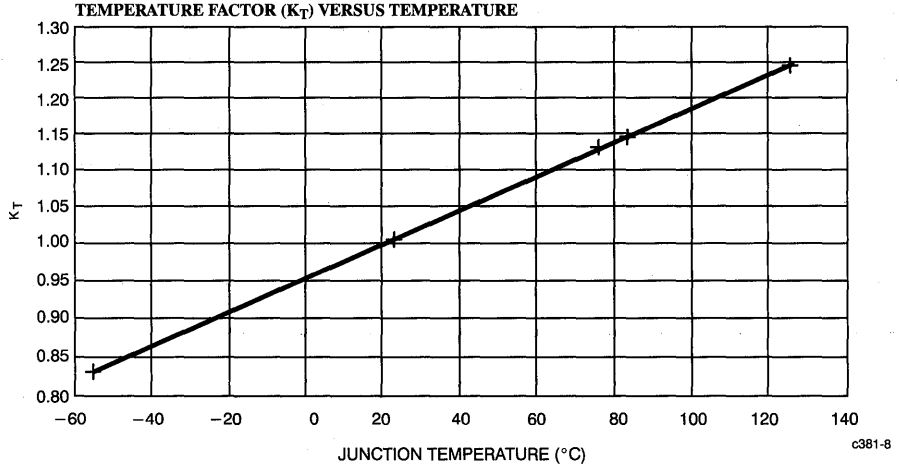
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})

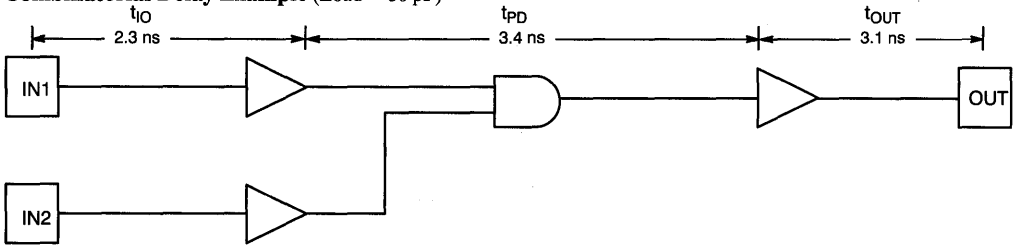


TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



*THETA JA = 45 °C/WATT FOR PLCC

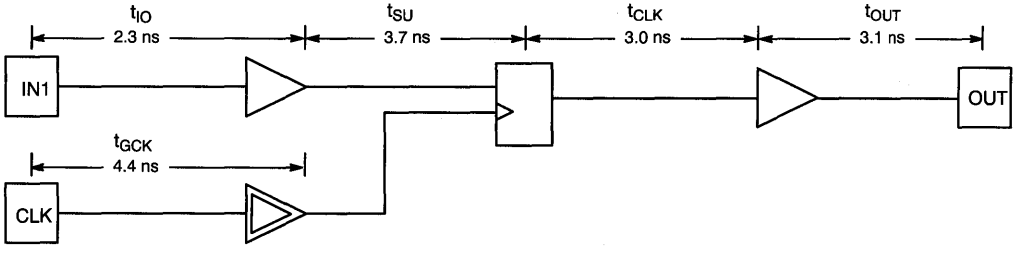
Combinatorial Delay Example (Load = 30 pF)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 8.8 ns

c381-9

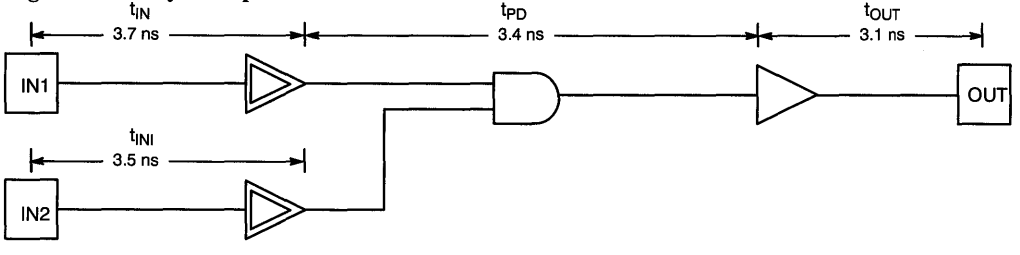
Sequential Delay Example (Load = 30 pF)



INPUT DELAY + REG SET-UP + CLOCK TO OUTPUT + OUTPUT DELAY = 12.1 ns

c381-10

High-Drive Delay Example



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 10.2 ns

c381-11

4

PLDs

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C381–2JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
1	CY7C381–1JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381–1JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C381–0JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381–0JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C382–2GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382–2JC	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C382–1GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382–1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382–1GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C382–1JI	J81	68-Lead Plastic Leaded Chip Carrier	
0	CY7C382–0GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382–0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382–0GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C382–0JI	J81	68-Lead Plastic Leaded Chip Carrier	

Shaded areas contain advanced information.

Document #: 38–00207

CY7C383
CY7C384

CYPRESS SEMICONDUCTOR

Very High Speed 2K (6K) Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 9 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **12 x 16 array of 192 logic cells provides 6,000 total available gates**
  - **2,000 typically usable "gate array" gates in 68- and 84-pin PLCC/CPGA packages**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (3.4 ns)**
- **Low-cost, powerful design tools**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **56 (CY7C383) to 68 (CY7C384) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <1 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **68-pin PLCC is compatible with CY7C382 footprint for easy upgrade**
- **84-pin PLCC is compatible with ACT1020 power supply and ground pinouts**

Functional Description

The CY7C383 and CY7C384 are members of the pASIC380 family of very high speed CMOS user-programmable ASIC (pASIC) devices. The 192 logic cell field-programmable gate array (FPGA) offers 2,000 typically usable "gate array" gates. This is equivalent to 6,000 EPLD or LCA gates. The CY7C383 is available in a 68-pin PLCC. The CY7C384 is available in an 84-pin PLCC and CPGA.

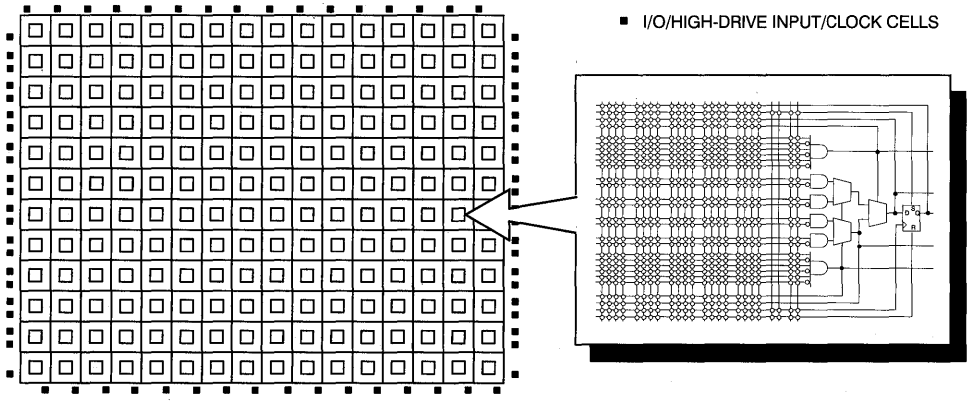
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input and output delays under 4 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C383 and CY7C384 using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C383 and CY7C384 feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

4 PLDs

Logic Block Diagram

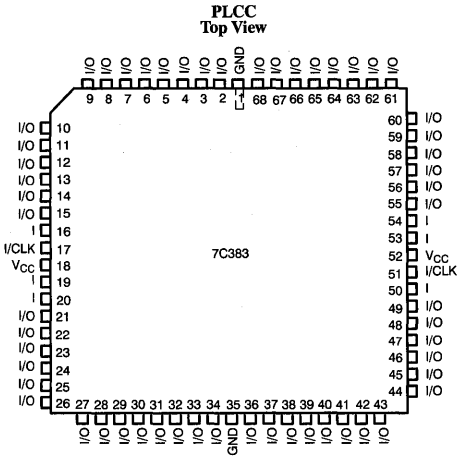


68 or 84 PINS, INCLUDING 68 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS c383-1

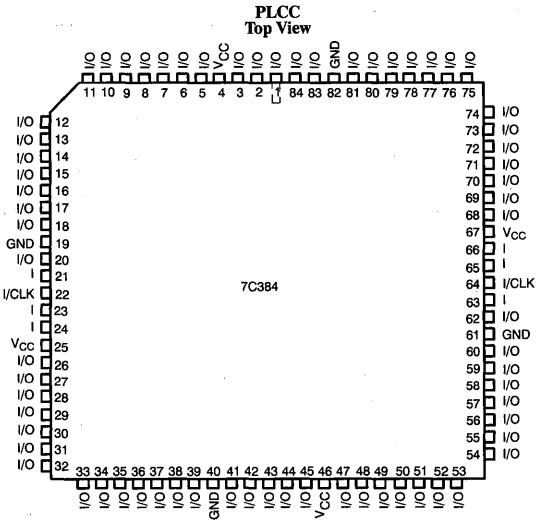
ViaLink is a trademark of QuickLogic Corporation.

Pin Configurations

PLCC
Top View



PLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... − 65°C to +150°C
Plastic ..... −40°C to +125°C
Lead Temperature ..... 300°C
Supply Voltage ..... − 0.5V to +7.0V
Input Voltage ..... − 0.5V to V_{CC} +0.5V
ESD Pad Protection ..... ±2000 V
DC Input Voltage ..... ±20 mA
Latch-Up Current ..... ±100 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40° to +85°C	5V ± 10%

Delay Factor (K)

Speed Grade	Industrial		Commercial	
	Min.	Max.	Min.	Max.
−0	0.4	1.67	0.46	1.55
−1	0.4	1.43	0.46	1.33
−2			0.46	1.25

Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0 mA	3.7		V
		I_{OH} = − 8.0 mA	2.4		V
		I_{OH} = − 10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = GND	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or GND		10	mA
I_{CC2}	Supply Current[1, 2]	f = 1.0 MHz, V_I = V_{CC} or GND		25	mA

Capacitance

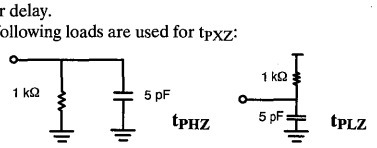
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Switching Characteristics Over the Operating Range

Parameter	Description	Propagation Delays[4] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[5]	3.4	3.8	4.2	4.8	8.1	ns
t_{SU}	Set-Up Time[5]	3.7	3.7	3.7	3.7	3.7	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9	ns
t_{SET}	Set Delay	2.7	3.1	3.5	4.1	7.4	ns
t_{RESET}	Reset Delay	2.9	3.2	3.6	4.2	7.5	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	3.6	3.6	3.6	3.6	3.6	ns
t_{SW}	Set Width	2.1	2.1	2.1	2.1	2.1	ns
t_{RW}	Reset Width	1.9	1.9	1.9	1.9	1.9	ns
INPUT CELLS							
t_{IN}	Input Delay (HIGH Drive)	3.7	3.8	4.2	4.6	6.4	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.5	3.6	4.0	4.4	6.2	ns
t_{IO}	Input Delay (Bidirectional Pad)	2.3	2.6	3.2	4.1	5.5	ns
t_{GCK}	Clock Buffer Delay [6]	4.4	4.5	4.6	4.6	5.0	ns
		Propagation Delays[4] with Output Load Capacitance (pF) of					
OUTPUT CELLS		**30**	**50**	**75**	**100**	**150**	
t_{OUTLH}	Output Delay LOW to HIGH	3.1	3.8	4.6	5.5	7.2	ns
t_{OUTHL}	Output Delay HIGH to LOW	3.1	3.9	5.0	6.1	8.3	ns
t_{PZH}	Output Delay Three-State to HIGH	4.4	5.3	6.5	7.7	10.1	ns
t_{PZL}	Output Delay Three-State to LOW	4.0	4.6	5.4	6.2	7.7	ns
t_{PHZ}	Output Delay HIGH to Three-State[7]	3.3	3.3	3.3	3.3	3.3	ns
t_{PLZ}	Output Delay LOW to Three-State[7]	3.7	3.7	3.7	3.7	3.7	ns

Notes:

1. Measured with twelve 16-bit counters configured internally and all outputs driving. To calculate power for your application, see the "pASIC380 Power vs. Operating Frequency" application note.
2. Guaranteed but not 100% tested.
3. C_I = 20 pF max. on pin 50 (7C383) or pin 63 (7C384.).
4. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Mulitply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
5. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
6. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
7. The following loads are used for t_{PXZ}:

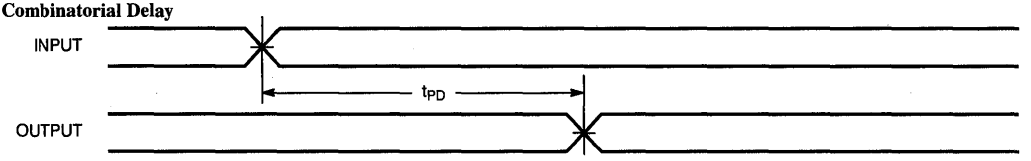


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[4] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	7.9	11.2				ns
		2		8.0	9.7			ns
		3			8.6	10.4	11.8	ns
		4				9.4	10.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	7.5	10.8				ns
		2		7.5	9.3			ns
		3			8.2	10.0	11.8	ns
		4				9.0	10.8	ns

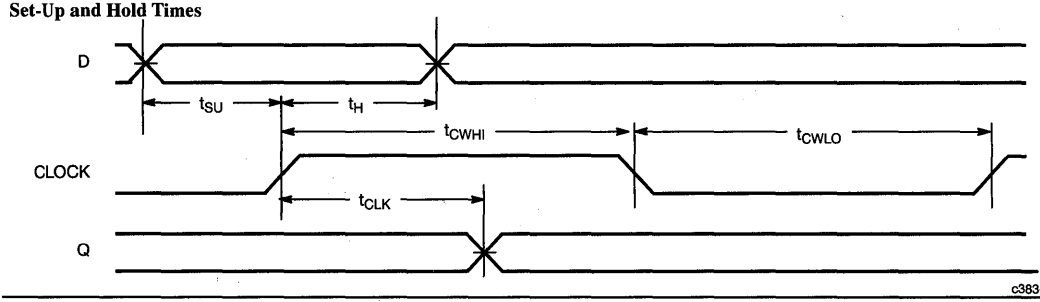
Switching Waveforms

Combinatorial Delay



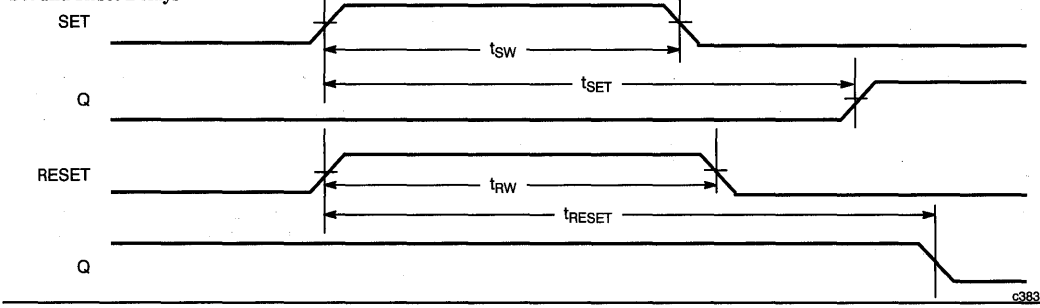
c383-2

Set-Up and Hold Times



c383-3

Set and Reset Delays



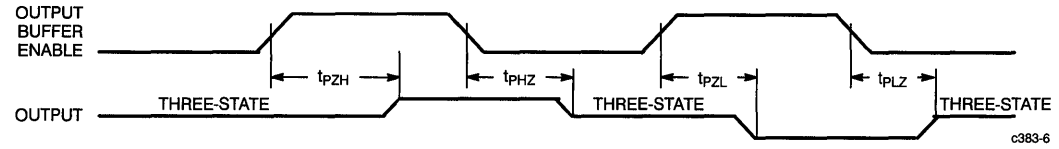
c383-4

Output Delay

c383-5

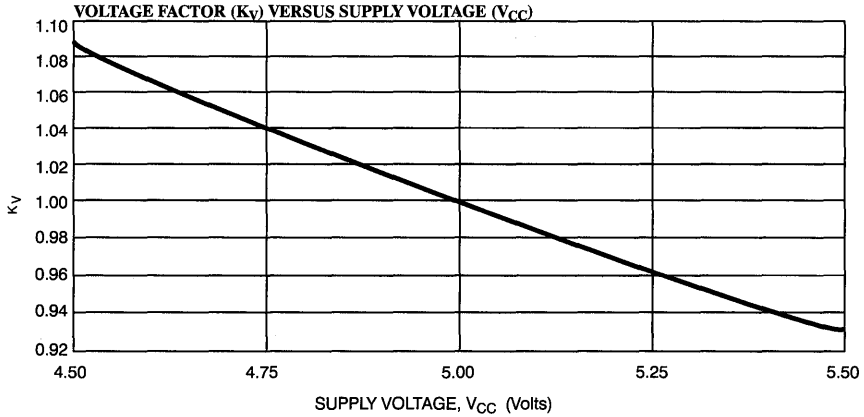
Switching Waveforms (continued)

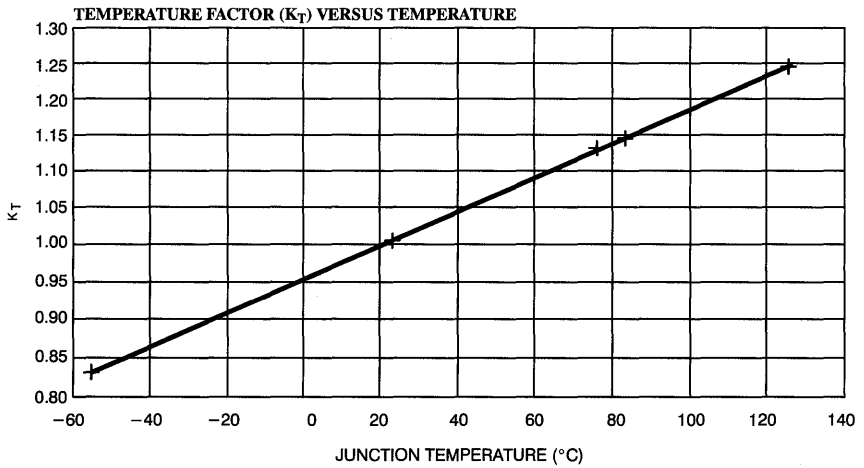
Three-State Delay



Typical AC Characteristics

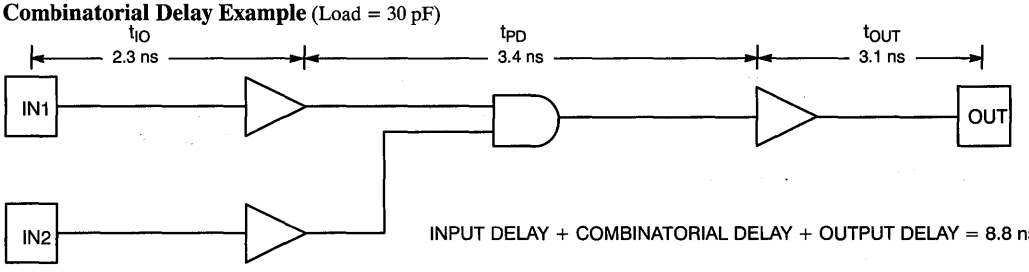
Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre–place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.





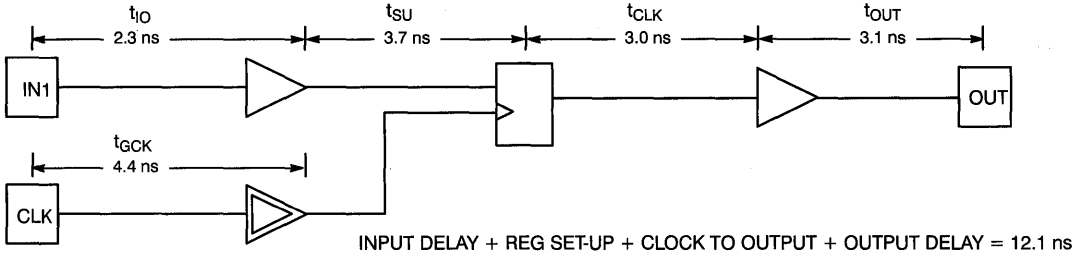
*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF)



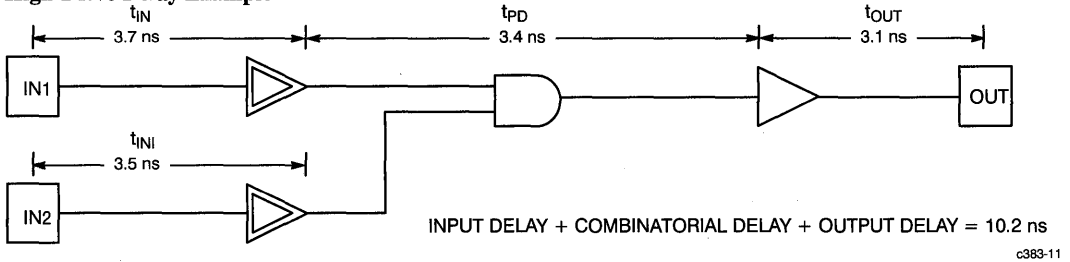
c383-9

Sequential Delay Example (Load = 30 pF)



c383-10

High-Drive Delay Example



c383-11

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C383–2GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–2JC	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C383–1GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C383–1GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C383–1JI	J81	68-Lead Plastic Leaded Chip Carrier	
0	CY7C383–0GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C383–0GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C383–0JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C384–2GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–2JC	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C384–1GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384–1GI	G84	84-Pin Grid Array (Cavity Up)	Industrial
	CY7C384–1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C384–0GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384–0GI	G84	84-Pin Grid Array (Cavity Up)	Industrial
	CY7C384–0JI	J83	84-Lead Plastic Leaded Chip Carrier	

Shaded area contains advanced information.

Document #: 38–00208–A

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7C385A
CY7C386A

Very High Speed 4K (12K) Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 9 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **16 x 24 array of 384 logic cells provides 12,000 total available gates**
  - **4,000 typically usable "gate array" gates in 84-pin PLCC/CLCC and 144-pin PQFP packages**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (3.4 ns)**
- **Low-cost, powerful design tools**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **68 (7C385A) to 114 (7C386A) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <1 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **0.65µ CMOS process with ViaLink℠ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **84-pin PLCC is compatible with the CY7C384 footprint for easy upgrade**

Functional Description

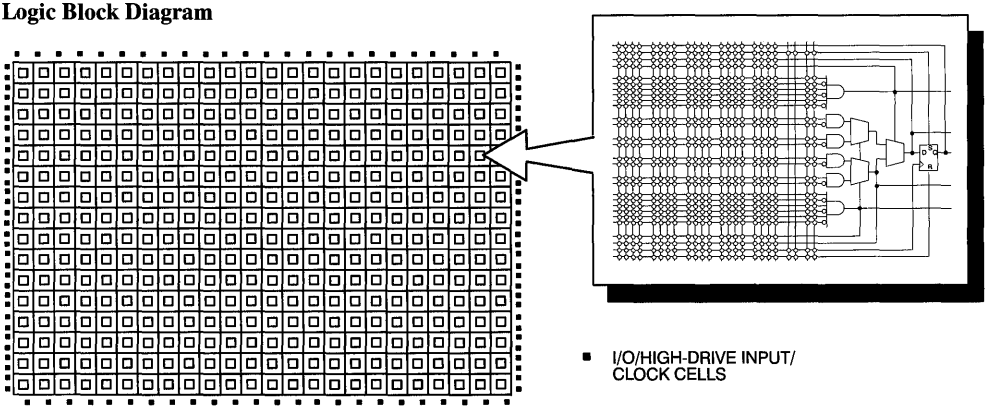
The CY7C385A and CY7C386A are members of the pASIC380 family of very high speed CMOS user-programmable ASIC (pASIC) devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 typically usable "gate array" gates. This is equivalent to 12,000 EPLD or LCA gates. The CY7C385A is available in a 84-pin PLCC and CLCC. The CY7C386A is available in 144-pin PQFP and PGA packages.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input and output delays under 4 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C385A and CY7C386A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C385A and CY7C386A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



144 PINS, 114 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

c386-1

Vialink is a trademark of QuickLogic Corporation.

Document #: 38–00209–A

PLD Programming Information

Introduction

PLDs, or programmable logic devices, provide an attractive alternative to logic implemented with discrete devices. Cypress Semiconductor is in the enviable position of being able to offer PLDs in several different process technologies, thus assuring our customers of a wide range of options for leading-edge speed as well as very low power consumption. Cypress optimizes the mix of technology and device architecture to insure that the programmable logic requirements of today's highest-performance electronics systems can be fully supported by a single PLD vendor.

Cypress offers a wide variety of PLDs based on our leading-edge CMOS EPROM process technology. This technology facilitates the lowest power consumption and the highest logic density of any nonvolatile PLD technology on the market today, at speeds that are nearly as fast as state-of-the-art bipolar technology would provide. Futhermore, these devices offer the user the option of device erasure and reprogrammability in windowed packages. Cypress also offers a number of PLDs based on our state-of-the-art BiCMOS and bipolar technologies. These PLDs are targeted at applications where power consumption and density are not as critical as leading-edge speed. And in, 1992 Cypress introduced PLDs based on CMOS Flash technology. Thus Cypress offers solutions for state-of-the-art systems regardless of what the optimal balance is between speed, power, and density for any particular system.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation, permanently turning off the transistor. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

Two Transistor Cells

Cypress uses a two-transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

BiCMOS and Bipolar Process Technology

In addition to CMOS, Cypress offers BiCMOS TTL and bipolar ECL I/O-compatible PLDs. The BiCMOS devices offer the advantages of CMOS (high density and low power) and bipolar (high speed). Both the BiCMOS and bipolar devices are one-time fuse programmable. The fuses are Ti-W and are connected directly to first metal. First metal is a reliable composite of Ti-TiW-AlSi-Ti to ensure excellent electromigration resistance, eliminate contact spiking, and minimize hillocking.

Flash Process Technology

In addition to offering PLDs based on EPROM, BiCMOS and high-performance bipolar technologies, Cypress introduced our first PLDs based on CMOS Flash technology in 1992. The Flash cell is programmed in the same manner as the EPROM cell, and is electrically erased via Fowler-Nordheim tunneling. This next-generation PLD technology will combine a number of key advantages for future Cypress PLDs. The principal advantages will be leading-edge speed, low CMOS power consumption, and electrical alterability for simplified inventory management. In addition, Flash technology offers two inherent advantages for PLDs over the commonly used full-features EE CMOS technology. One is its superior migratability to higher logic densities, due to the smaller Flash cell size. The second is superior reliability, due to the Flash cell's higher immunity to voltage transients and the accompanying risk of data corruption.

Programming Algorithm

Byte Addressing and Programming

Most Cypress programmable logic devices are addressed and programmed on a byte or extended byte basis where an extended byte is a filed that is as wide as the output path of the device. Each device or family of devices has a unique address map that is available in the product datasheet. Each byte or extended byte is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a 1 or HIGH is placed on the input pin and a 0 or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A 1 or HIGH during program verify operation indicates an unprogrammed cell, while a 0 or LOW indicates that the cell accessed has been programmed.

Blank Check

Before programming, all programmable logic devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a 1 or HIGH output indicates that the addressed cell is unprogrammed, while a 0 or LOW indicates a programmed cell.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation (except for the CY7C361), the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a read/write pin in the programming mode. This signal causes a write operation when switched to a supervoltage and a read operation when switched to a logic 0 or LOW. In the logic HIGH or 1 state, the device is in a program inhibit condition and the output pins are in a high-impedance state. During a write operation, the data on the output pins is written into the addressed array location. In a read operation, the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins and writing it into the addressed location. Verification of data is accomplished by examining the information on the output pins during a read operation.

The timing for actual programming is supplied in the unique programming specification for each device.

Phantom Operating Modes

All Cypress programmable logic devices except for the Flash PLDs contain a Phantom array for post assembly testing. This array is accessed, programmed, and operated in a special Phantom mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the Phantom array is connected. In normal operation the Phantom array is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging and, if desired, by the user before programming and use. The Phantom modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific datasheets for details.

Special Features

Cypress programmable logic devices, depending on the device, have several special features. For example, the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PALC22V10, PLDC20G10, and CY7C330, the macrocells are programmable through the use of the architecture bits. This allows users to more effectively tailor the device architecture to their unique system requirements. Specific programming is detailed in the device datasheet.

Programming Support

Programming support for Cypress programmable logic devices is available from a number of programmer manufacturers, some of which are listed here. They can be contacted directly for information regarding programming support of Cypress devices. Alternatively, all Cypress sales representatives and distributors have access to this information.

Cypress Semiconductor Inc.
3901 North First Street
San Jose, CA 95134
(408) 943–2600

Data I/O Corporation
10525 Willows Rd., N.E.
P.O. Box 97046
Redmond, WA 98073–9746
(206) 881–6444

Digelec Corporation
1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
(201) 493–2420

Kontron Electronics
1230 Charleston Road
Mountain View, CA 94039–7230
(415) 965–7020

Logical Devices Inc.
1201 N.W. 65th Place
Ft. Lauderdale, FL 33309
(305) 974–0975

SMS Mikrocomputersysteme GmbH
Im Morgental 13, D–8994 Hergatz
Germany 5018
(49) 7522–5018 (phone)
(49) 7522–8929 (fax)

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988–1118
STAG ZL32 Rev. 30A03

Third-Party Development Software

ABEL™
Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073–9764
(206) 881–6444

CUPL™
Logical Devices Inc.
1201 N.W. 65th Place
Ft. Lauderdale, FL 33309
(305) 974–0975

LOG/iC™
ISDATA GmbH
Haid-und-Neu-Strasse 7
D–7500 Karlsruhe 1
Germany
(0721) 69 30 92

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Section Contents

FIFOs

CY7C401/CY7C403
CY7C402/CY7C404

CYPRESS SEMICONDUCTOR

Cascadable 64 x 4 FIFO and 64 x 5 FIFO

Features

- **64 x 4 (CY7C401 and CY7C403) 64 x 5 (CY7C402 and CY7C404) High-speed first-in first-out memory (FIFO)**
- **Processed with high-speed CMOS for optimum speed/power**
- **25-MHz data rates**
- **50-ns bubble-through time—25 MHz**
- **Expandable in word width and/or length**
- **5-volt power supply ±10% tolerance, both commercial and military**
- **Independent asynchronous inputs and outputs**
- **TTL-compatible interface**
- **Output enable function available on CY7C403 and CY7C404**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Pin compatible with MMI 67401A/67402A**

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four-bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five-bit words. Both the CY7C403 and CY7C404 have an output enable (OE) function.

The devices accept 4- or 5-bit words at the data input ($DI_0 - DI_n$) under the control of the shift in (SI) input. The stored words stack up at the output ($DO_0 - DO_n$) in the order they were entered. A read command on the shift out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The input ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The output ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

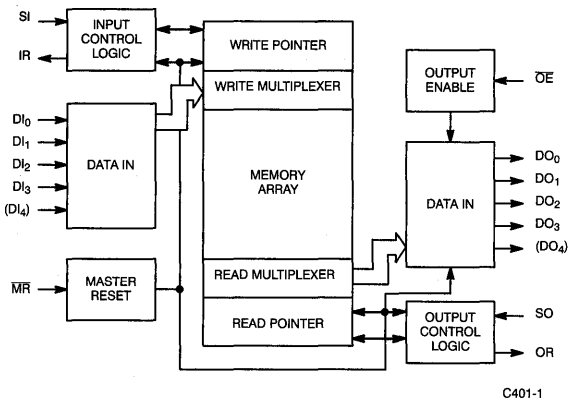
Parallel expansion for wider words is accomplished by logically ANDing the IR and OR signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The IR pin of the receiving device is connected to the SO pin of the sending device, and the OR pin of the sending device is connected to the SI pin of the receiving device.

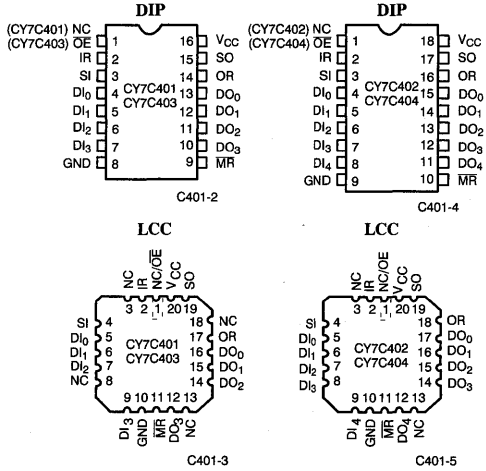
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25-MHz operation makes these FIFOs ideal for high-speed communication and controller applications.

5 FIFOs

Logic Block Diagram



Pin Configurations



Selection Guide

		7C401/2–5	7C40X–10	7C40X–15	7C40X–25
Maximum Access Time (ns)		5	10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75	75
	Military		90	90	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2]

Parameters	Description	Test Conditions		7C40X–10, 15, 25 Min.	7C40X–10, 15, 25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	µA
V_{CD}[3]	Input Diode Clamp Voltage[3]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		– 50	+50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

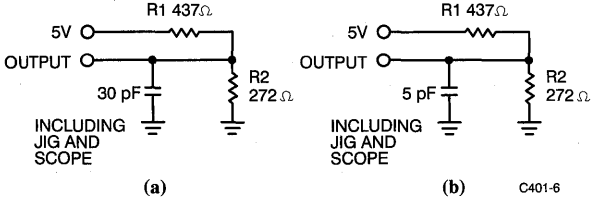
Capacitance[5]

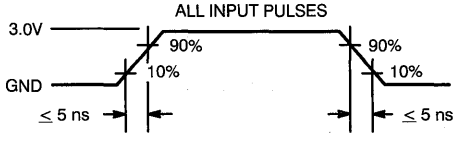
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

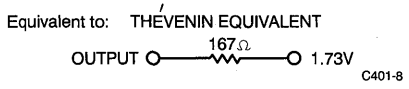
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to –3V dc input levels and –5V undershoot pulses of less than 10 ns (measured at 50% output).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms







Switching Characteristics Over the Operating Range[2, 6]

Parameters	Description	Test Conditions	7C401–5 7C402–5		7C40X–10		7C40X–15		7C40X–25[7]		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 8		5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		20		20		20		11		ns
t_{PLSI}	SO LOW Time		45		30		25		20		ns
t_{SSI}	Data Set-Up to SI	Note 9	0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 9	60		40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			75		40		35		21/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			75		45		40		28/30	ns
t_{PHSO}	SO HIGH Time		20		20		20		11		ns
t_{PLSO}	SO LOW Time		45		25		25		20		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			75		40		35		19/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			80		55		40		34/37	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		ns
t_{BT}	Bubble-Through Time			200	10	95	10	65	10	50/60	ns
t_{SIR}	Data Set-Up to IR	Note 10	5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 10	30		30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		20		20		20		15		ns
t_{POR}	Output Ready Pulse HIGH		20		20		20		15		ns
t_{PMR}	MR Pulse Width		40		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		40		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			85		40		35		35	ns
t_{DIR}	MR LOW to IR HIGH			85		40		35		35	ns
t_{LZMR}	MR LOW to Output LOW	Note 11		50		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			—		35		30		20	ns
t_{HZOE}	Output High Z from OE HIGH	Note 12		—		30		25		15	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads and Waveforms.
7. Commercial/Military
8. $I/f_O > t_{PHSI} + t_{DHIR}$, $I/f_O > t_{PHSO} + t_{DHOR}$
9. t_{SSI} and t_{HSI} apply when memory is not full.
10. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
11. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
12. HIGH-Z transitions are referenced to the steady-state V_{OH} −500 mV and V_{OL} +500 mV levels on the output. t_{HZOE} is tested with 5-pF load capacitance as in part (b) of AC Test Loads and Waveforms.

Operational Description

Concept

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the SO and SI respectively. The availability of an empty space to shift in data is indicated by the IR signal, while the presence of data at the output is indicated by the OR signal. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an OR signal. The output enable ($\overline{OE}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

Resetting the FIFO

Upon powe-up, the FIFO must be reset with a master reset (MR) signal. This causes the FIFO to enter an empty condition signified by the OR signal being LOW at the same time the IR signal is HIGH. In this condition, the data outputs ($DO_0 - DO_n$) will be in a LOW state.

Shifting Data In

Data is shifted in on the rising edge of the SI signal. This loads input data into the first word location of the FIFO. On the falling edge of the SI signal, the write pointer is moved to the next word position and the IR signal goes HIGH, indicating the readiness to accept new data. If the FIFO is full, the IR will remain LOW until a word of data is shifted out.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of the SO signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the OR signal will go HIGH. If data is not present, the OR signal will stay LOW indicating the FIFO is empty. Upon the rising edge of SO, the OR signal goes LOW. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

Bubble-Through

Two bubble-through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the OR flag goes HIGH, indicating valid data at the output.

The second bubble-through condition occurs when the device is full. Shifting data out creates an empty location that propagates to the input. After a delay, the IR flag goes HIGH. If the SI signal is HIGH at this time, data on the input will be shifted in.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

When this violation occurs, the operation of the FIFO is unpredictable. It must then be reset, and all data is lost.

Application of the 7C403–25/7C404–25 at 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFOs requires knowledge of characteristics that are not easily specified in a datasheet, but which are necessary for reliable operation under all conditions, so we will specify them here.

When an empty FIFO is filled with initial information at maximum "shift in" SI frequency, followed by immediate shifting out of the data also at maximum "shift out" SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the OR signal, during which time the SO signal is not recognized. This condition exists only at high-speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full-frequency operation, but rather delays the full 25-MHz operation until after the window has passed.

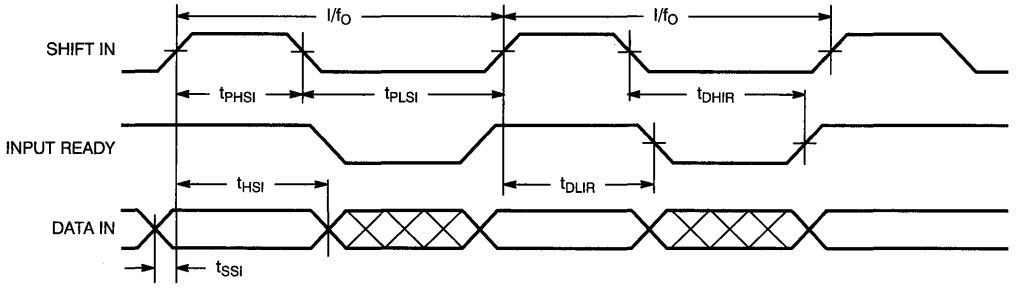
There are several implementation techniques for managing the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. However, this requires that the SO operation be at least temporarily synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is more than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of IR and SI conditions as well as SO.
4. Handshaking with the OR signal is a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This ensures that the SO pulse that is initiated in the window will be automatically extended long enough to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will ensure the correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and is dependent on the specific application needs.

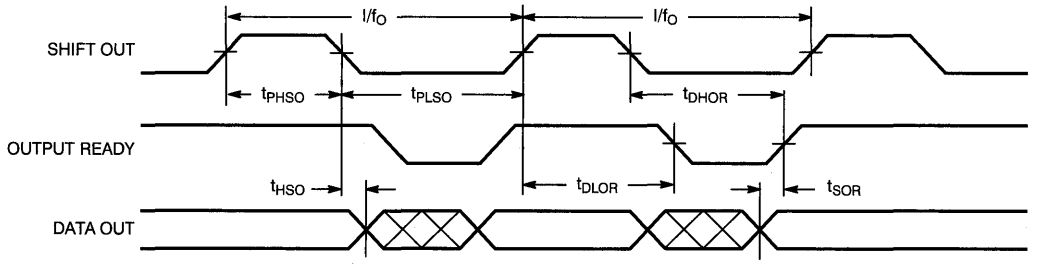
Switching Waveforms

Data In Timing Diagram



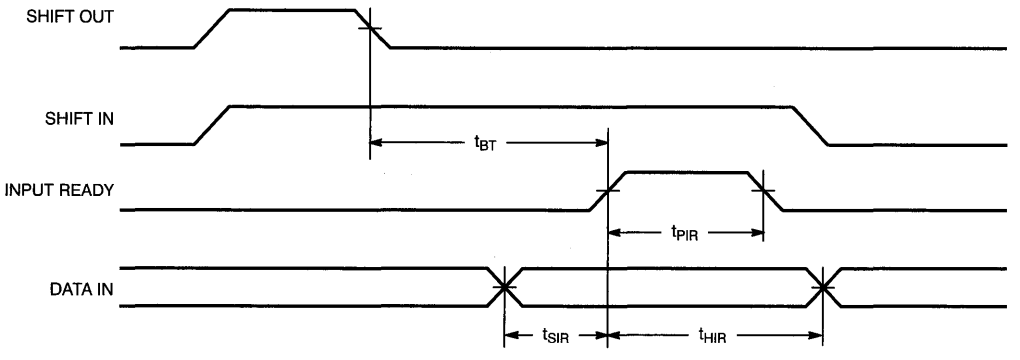
C401-9

Data Out Timing Diagram



C401-10

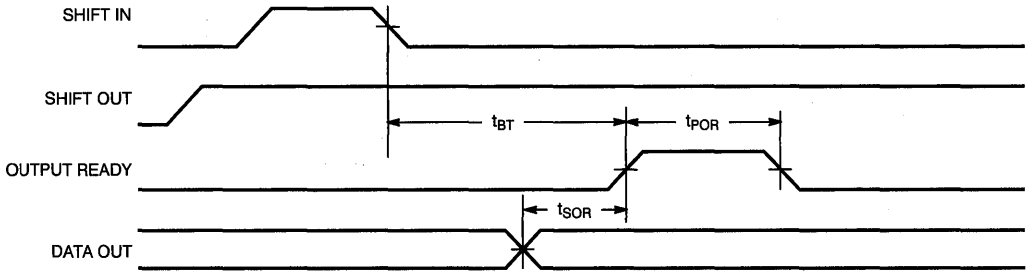
Bubble Through, Data Out To Data In Diagram



C401-11

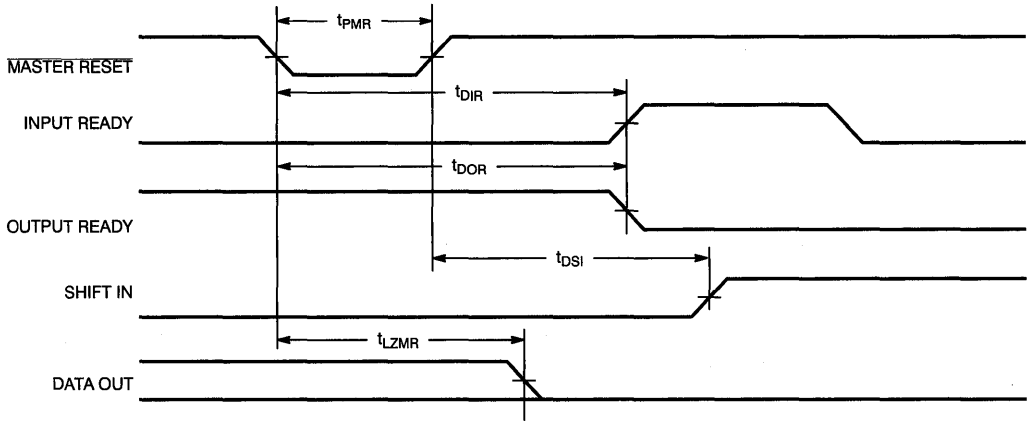
Switching Waveforms (continued)

Bubble Through, Data In To Data Out Diagram



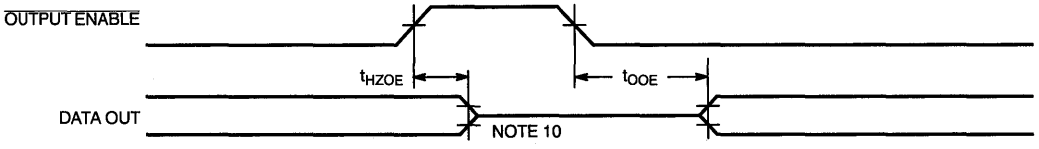
C401-12

Master Reset Timing Diagram



C401-13

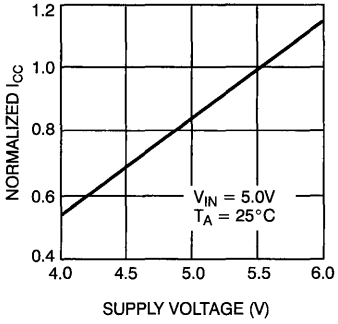
Output Enable Timing Diagram



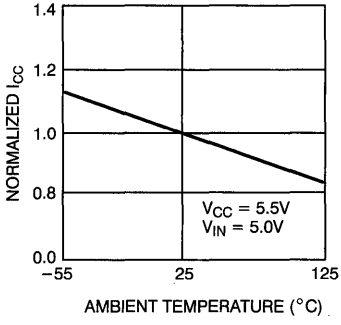
C401-14

Typical DC and AC Characteristics

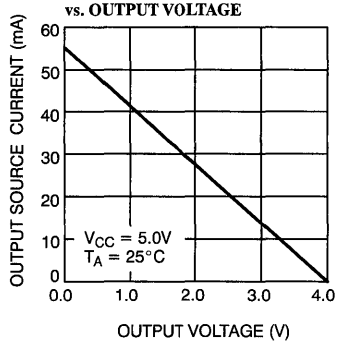
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



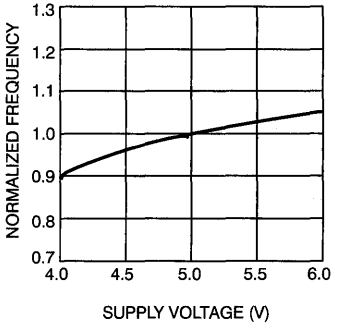
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



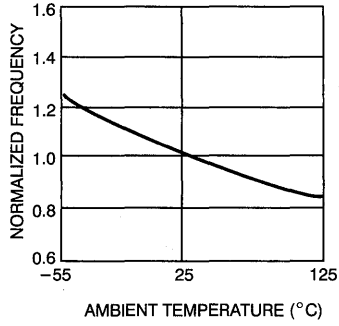
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



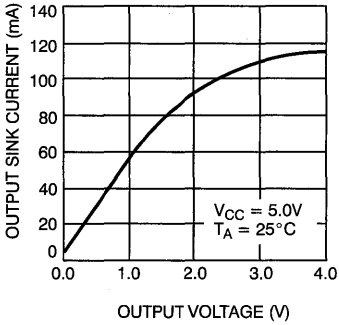
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



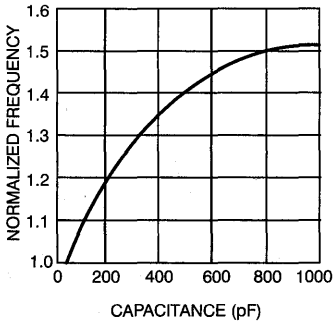
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



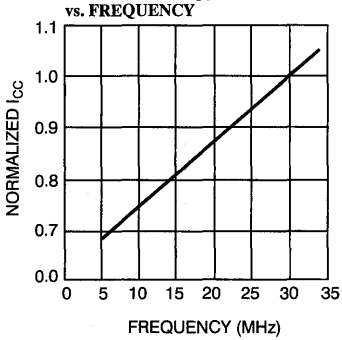
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



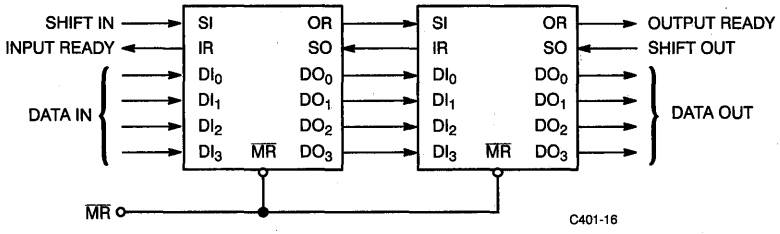
NORMALIZED I_{CC} vs. FREQUENCY



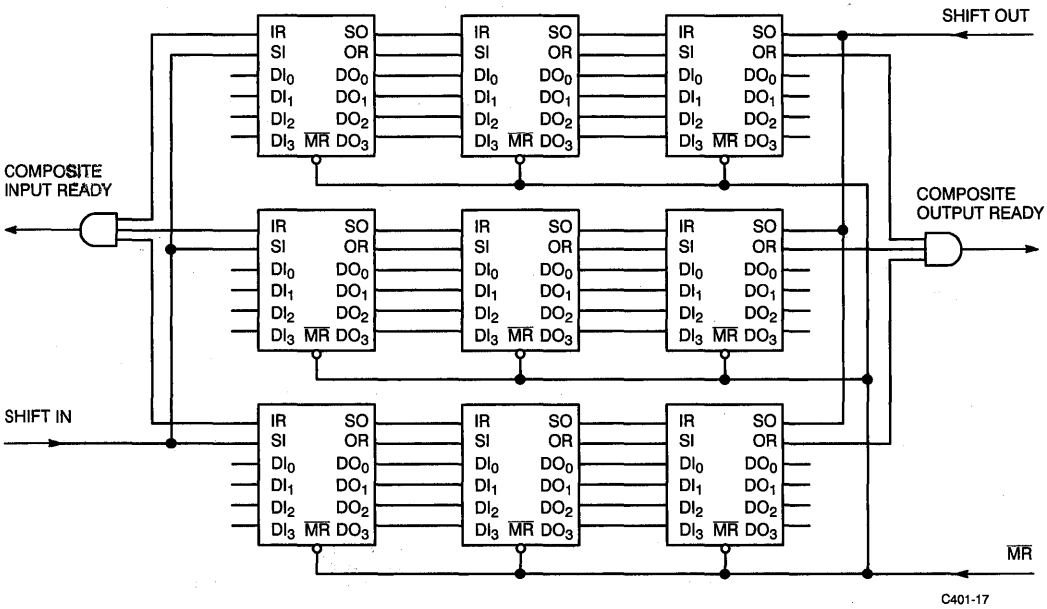
C401-15

FIFO Expansion[13, 14, 15, 16, 17]

128 x 4 Application[18]



192 x 12 Application[19]



Notes:

13. When the memory is empty, the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
14. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data, and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid, stable data on the outputs.
15. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
16. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH, then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
17. All Cypress FIFOs will cascade with other Cypress FIFOs. However, hey may not cascade with pin-compatible FIFOs from other manufacturers.
18. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
19. FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite input and output ready flags. This need is due to the variation of delays of the FIFOs.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C401–5PC	P1	16-Lead (300-Mil) Molded DIP	Commercial
10	CY7C401–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C401–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C401–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C402–5PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
10	CY7C402–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–10PC	P3	20-Pin Square Leadless Chip Carrier	
	CY7C402–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C402–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C402–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C403–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C403–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C403–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C404–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–10PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C404–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C404–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–25LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{OOE}	7, 8, 9, 10, 11
t_{HZOE}	7, 8, 9, 10, 11

Document #: 38–00040–G

CY7C408A
CY7C409A

CYPRESS SEMICONDUCTOR

Cascadable 64 x 8 FIFO
Cascadable 64 x 9 FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35-MHz shift in and shift out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual-port RAM architecture**
- **Fast (50-ns) bubble-through**
- **Independent asynchronous inputs and outputs**
- **Output enable (CY7C408A)**
- **Expandable in word width and FIFO depth**
- **5V ±10% supply**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge voltage**
- **300-mil, 28-pin DIP**

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry-standard handshaking signals, almost full/almost empty (AFE) and half full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an output enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI_0 – DI_8) under the control of the shift in (SI) input when the input ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO_0 – DO_8 output pins under the control of the shift out (SO) input when the output ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

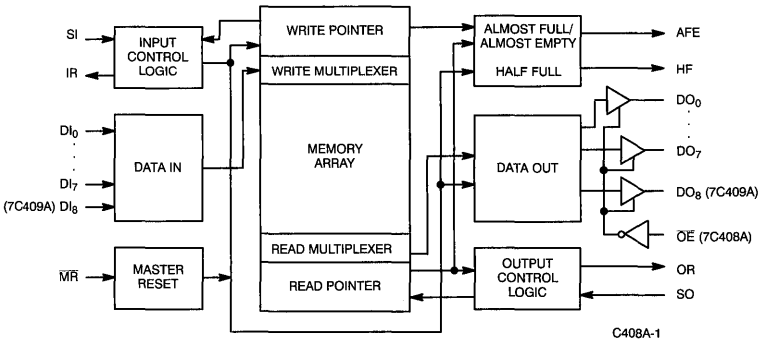
The IR and OR signals are also used to connect the FIFOs in parallel to make a wider word or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together (*Figure 5*). The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

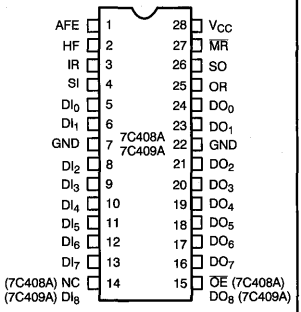
Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO (*Figure 4*). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

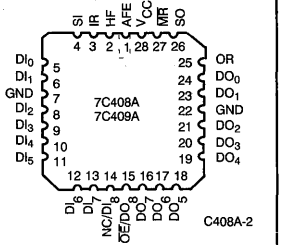
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift in and shift out rates of these FIFOs, and their high throughput rate due to the fast bubble-through time, which is due to their dual-port RAM architecture, make them ideal for high-speed communications and controllers.

Logic Block Diagram



Pin Configurations





Flag Definitions

HF	AFE	Words Stored
L	H	0 – 8
L	L	9 – 31
H	L	32 – 55
H	H	56 – 64

Selection Guide

		7C408A–15 7C409A–15	7C408A–25 7C409A–25	7C408A–35 7C409A–35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)[1]	Commercial	115	125	135
	Military	140	150	N/A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C
Ambient Temperature with Power Applied ..... – 55°C to +125°C
Supply Voltage to Ground Potential ..... – 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State (7C408A) ..... – 0.5V to +7.0V
DC Input Voltage ..... – 3.0V to +7.0V
Power Dissipation 1.0W
Output Current, into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[3]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		– 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	mA
I_{CC}	Power Supply Current	$I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$				

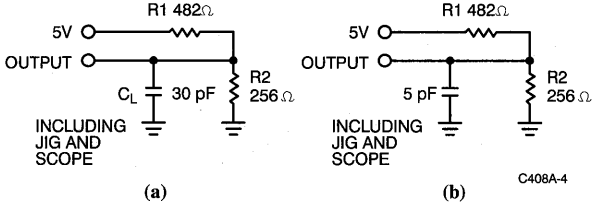
Capacitance[5]

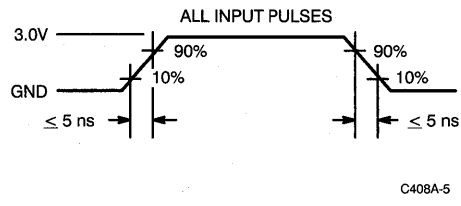
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

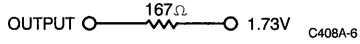
1. $I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 6]

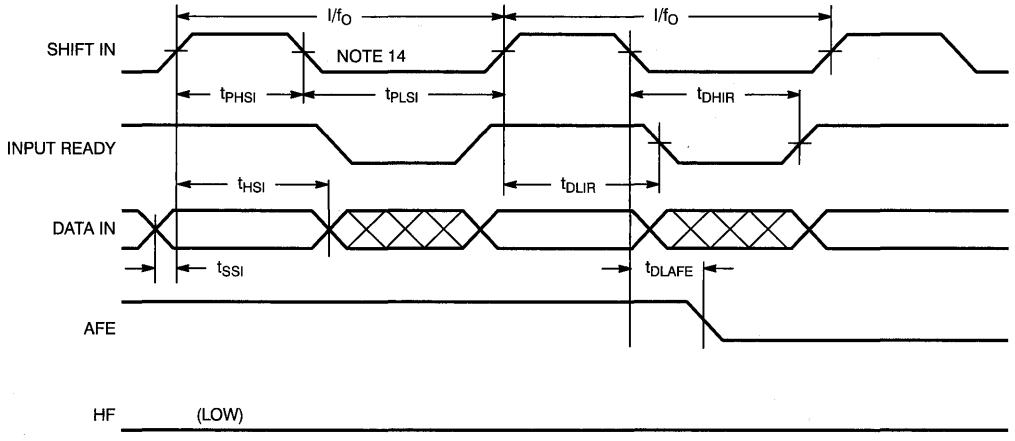
Parameters	Description	Test Conditions	7C408A–15 7C409A–15		7C408A–25 7C409A–25		7C408A–35 7C409A–35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		15		25		35	MHz
t_{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t_{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t_{SSI}	Data Set-Up to SI	Note 8	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t_{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Fall-through, Bubble-back Time		10	65	10	60	10	50	ns
t_{SIR}	Data Set-Up to IR	Note 9	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t_{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t_{DLZOE}	OE LOW to LOW Z (7C408A)	Note 12		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408A)	Note 12		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 13		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns
t_{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in parts (a) and (b) of AC Test Loads and Waveforms.
7. $1/f_O \geq (t_{PHSI} + t_{PLSI})$, $1/f_O \geq (t_{PHSO} + t_{PLSO})$.
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
10. At any given operating condition $t_{PIR} \geq (t_{PHSO}$ required).
11. At any given operating condition $t_{POR} \geq (t_{PHSI}$ required).
12. t_{DHZOE} and t_{DLZOE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. t_{DHZOE} transition is measured ±500 mV from steady-state voltage. t_{DLZOE} transition is measured ±100 mV from steady-state voltage. These parameters are guaranteed and not 100% tested.
13. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

Switching Waveforms

Data In Timing Diagram



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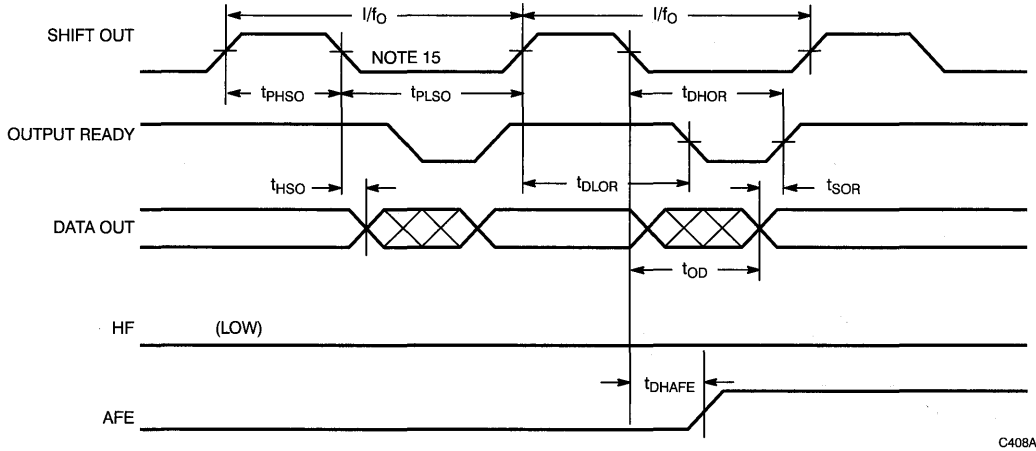
Data Out Timing Diagram

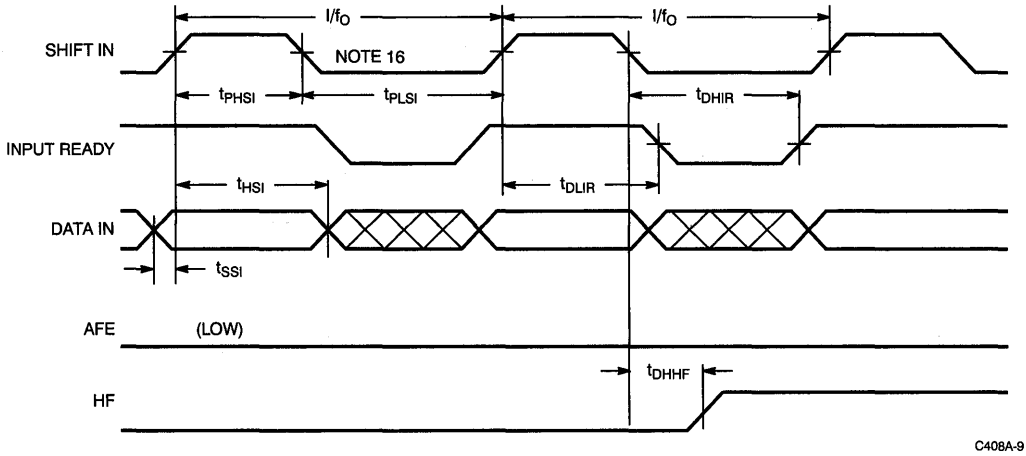


C408A-8

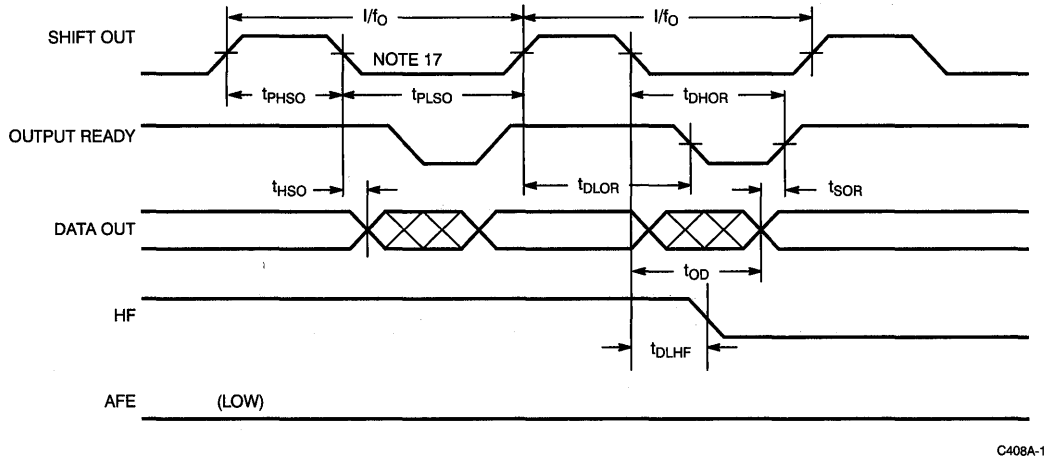
Notes:
14. FIFO contains 8 words.
15. FIFO contains 9 words.

Switching Waveforms (continued)

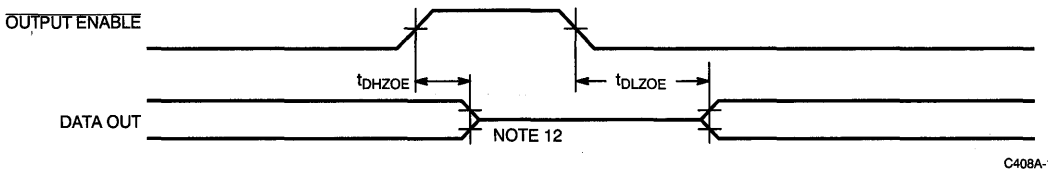
Data In Timing Diagram



Data Out Timing Diagram



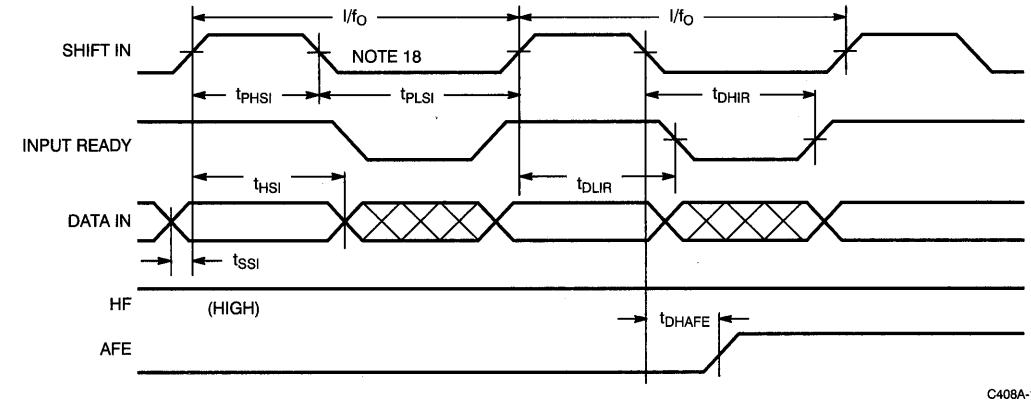
Output Enable (CY7C408A only)



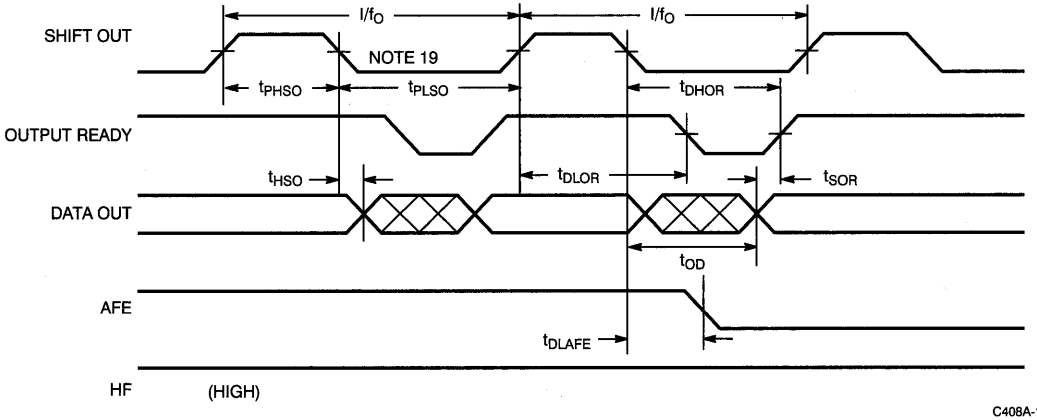
Notes:
16. FIFO contains 31 words.
17. FIFO contains 32 words.

Switching Waveforms (continued)

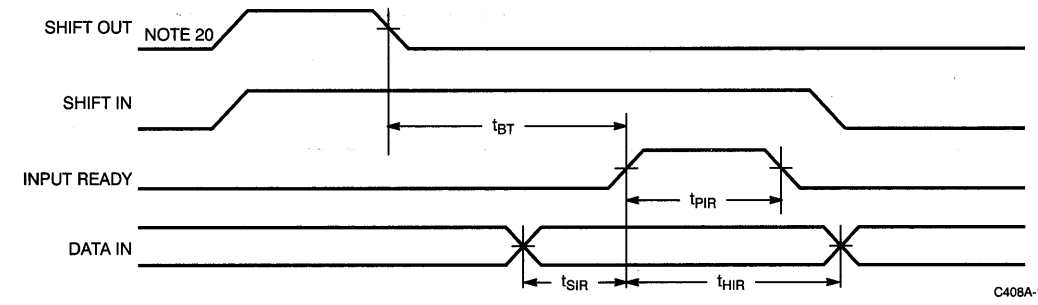
Data In Timing Diagram



Data Out Timing Diagram



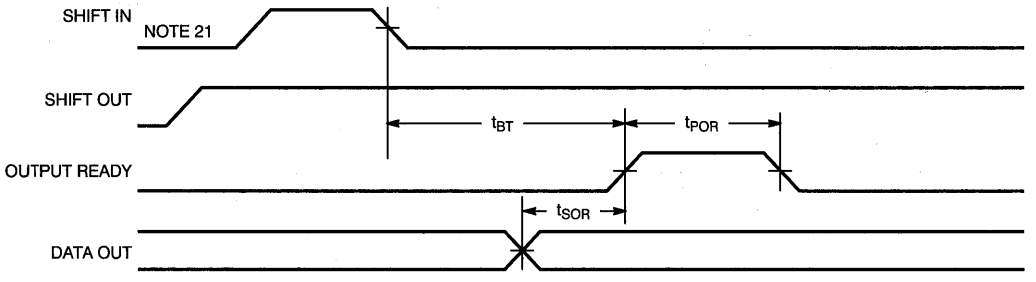
Bubble-Back, Data Out To Data In Diagram



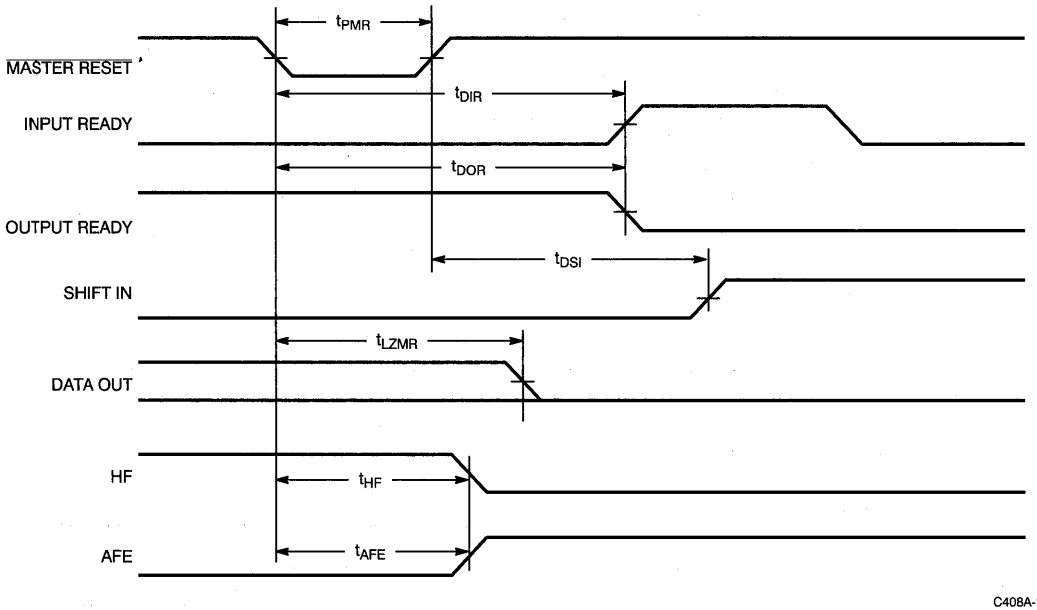
Notes:
18. FIFO contains 55 words.
19. FIFO contains 56 words.
20. FIFO contains 64 words.

Switching Waveforms (continued)

Fall-Through, Data In to Data Out Diagram



Master Reset Timing Diagram



Note:
21. FIFO is empty.

Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8 or 9 bits each (which are implemented using a dual-port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the almost full/almost empty (AFE) and half full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which it would have to do if the memory were implemented using the conventional register array architecture.

Fall-Through and Bubble-Back

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the fall-through time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the bubble-back time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or near empty) and by the bubble-back time when it is full (or near full).

The conventional definitions of fall-through and bubble-back do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst-case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 – DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the input ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the shift in (SI) pin will clock the data on the DI_0 – DI_8 inputs into the FIFO. Data propagates through the device at the falling edge of SI.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.

Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the output ready (OR) signal. After the FIFO is reset all data outputs (DO_0 – DO_8) will be in the LOW state. As long as the FIFO remains empty, the OR signal will be LOW and all SO pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

AFE and HF Flags

Two flags, almost full/almost empty (AFE) and half full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are 8 or fewer or 56 or more words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (*Figures 1* and *2*).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay (t_{DHAFE}, t_{DLAFE}, t_{DHHF} or t_{DLHF}). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

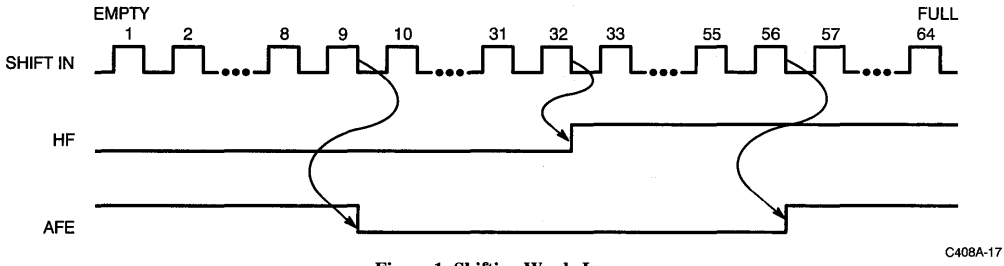


Figure 1. Shifting Words In

Cascading the 7C408/9A–35 Above 25 MHz

First, the capacity of N cascaded FIFOs is decreased from N × 64 to (N × 63) + 1.

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin (*Figure 3*). Two things should be noted when this configuration is implemented.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data shifted in faster than it is shifted out, and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.[28]

When data packets[29] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 (=2 × 63 + 1) words may be shifted in at up to 35 MHz and then the entire packet may be shifted out at up to 35 MHz.

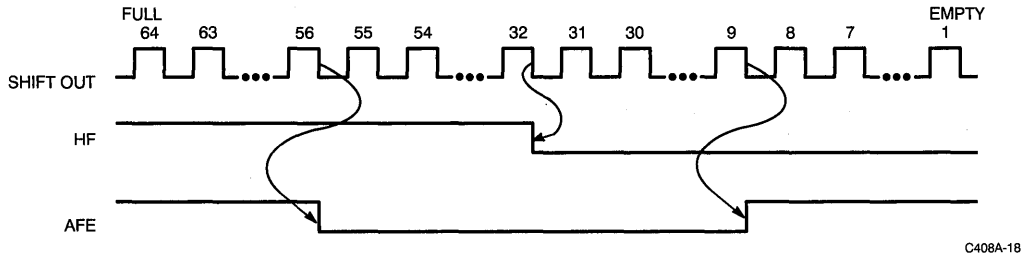


Figure 2. Shifting Words Out

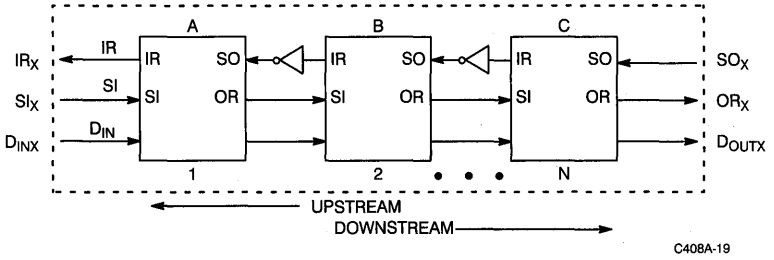


Figure 3. Cascaded Configuration Above 25 MHz

128 x 9 Configuration

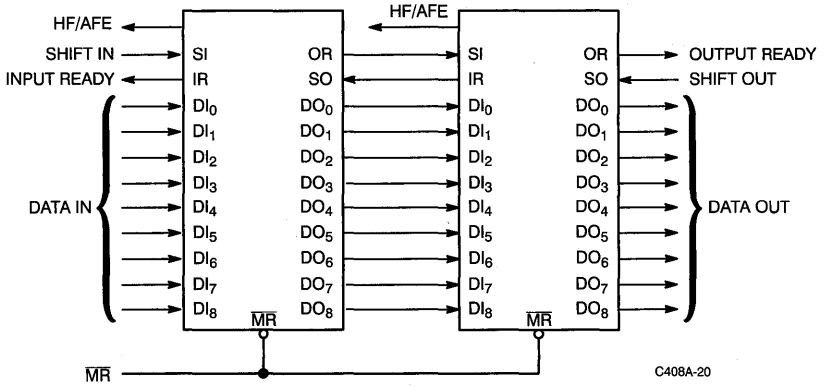


Figure 4. Cascaded Configuration at or below 25 MHz[22, 23, 24, 25, 26]

192 x 27 Configuration

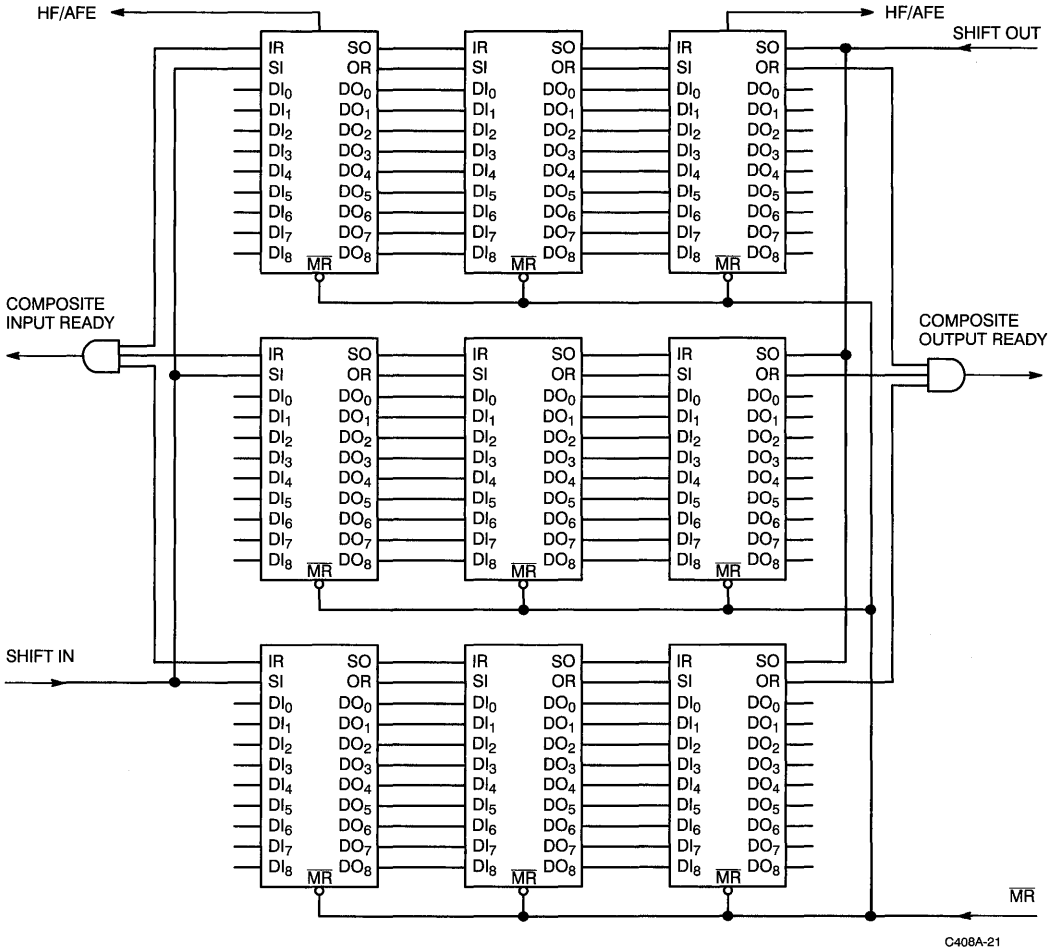


Figure 5. Depth and Width Expansion[23, 24, 25, 26, 27]

Notes:

22. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
23. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
24. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
25. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
26. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH, and OR goes LOW.
27. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite input ready and output ready flags. This need is due to the variation of delays of the FIFOs.

If data is to be shifted out simultaneously with the data being shifted in, the concept of "virtual capacity" is introduced. Virtual capacity is simply how large a packet of data can be shifted in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted out at any given frequency. *Figure 6* is a graph of packet size[30] vs. shift out frequency (f_{SOx}) for two different values of shift in frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high shift out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep.[31] If data is shifted in simultaneously, *Figure 6* applies with f_{SIx} and f_{SOx} interchanged.

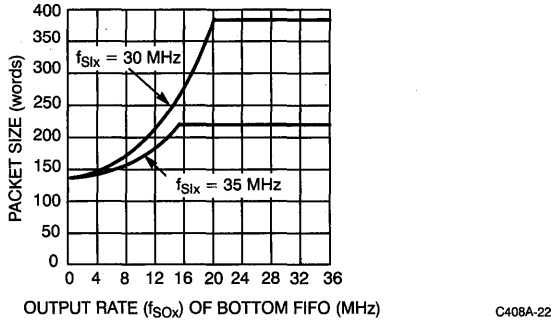


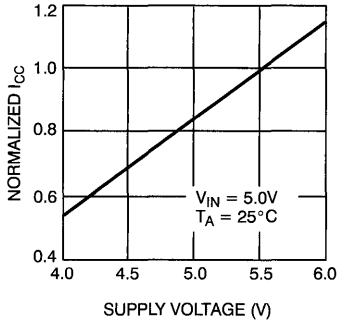
Figure 6. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter

Notes:

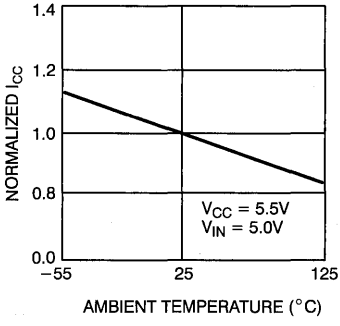
28. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
29. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is shifted in without simultaneous shift out clock occurring. The complement of this holds when data is shifted out as a packet.
30. These are typical packet sizes using an inverter whose delay is 4 ns.
31. Only devices with the same speed grade are specified to cascade together.

Typical DC and AC Characteristics

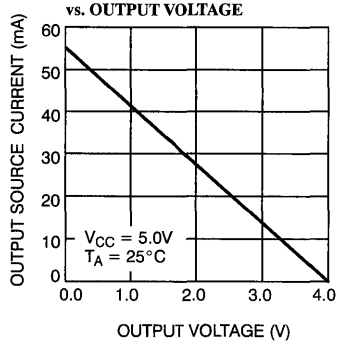
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



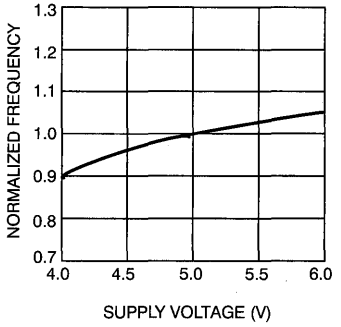
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



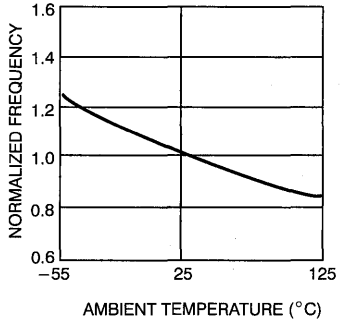
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



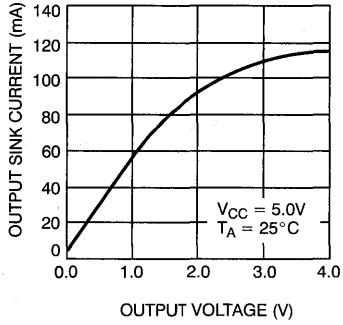
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



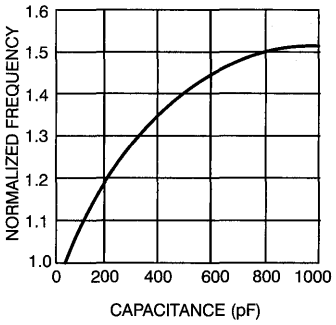
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



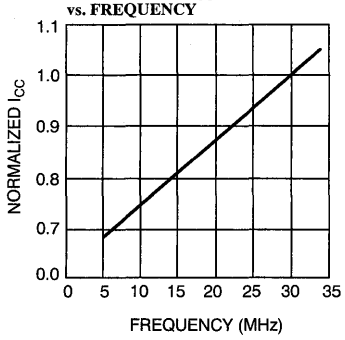
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



C408A-23

5 FIFOs

Ordering Information

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C408A–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C408A–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C408A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–15KMB	K74	28-Lead Rectangular CerPack	
	CY7C408A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C408A–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C408A–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C408A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–25KMB	K74	28-Lead Rectangular CerPack	
	CY7C408A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C408A–35DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C408A–35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C408A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C409A–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C409A–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C409A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–15KMB	K74	28-Lead Rectangular CerPack	
	CY7C409A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C409A–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C409A–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C409A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–25KMB	K74	28-Lead Rectangular CerPack	
	CY7C409A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C409A–35DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C409A–35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C409A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CCQ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{SIIR}	7, 8, 9, 10, 11
t_{SOOR}	7, 8, 9, 10, 11
t_{DLZOE}	7, 8, 9, 10, 11
t_{DHZOE}	7, 8, 9, 10, 11
t_{DHHF}	7, 8, 9, 10, 11
t_{DLHF}	7, 8, 9, 10, 11
t_{DLAFE}	7, 8, 9, 10, 11
t_{DHAFE}	7, 8, 9, 10, 11
t_B	7, 8, 9, 10, 11
t_{OD}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{AFE}	7, 8, 9, 10, 11
t_{HF}	7, 8, 9, 10, 11

Document #: 38–00059–F

CY7C420, CY7C421
CY7C424, CY7C425
CY7C428, CY7C429

CYPRESS SEMICONDUCTOR

Cascadable 512 x 9 FIFO
Cascadable 1K x 9 FIFO
Cascadable 2K x 9 FIFO

Features

- **512 x 9, 1,024 x 9, 2,048 x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  - **I_{CC} (max.) = 142 mA (commercial)**
  - **I_{CC} (max.) = 147 mA (military)**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil DIP packaging**
- **300-mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7201, IDT7202, and IDT7203**

Functional Description

The CY7C420/CY7C421, CY7C424/CY7C425, and CY7C428/CY7C429 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 512, 1,024, and 2,048 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

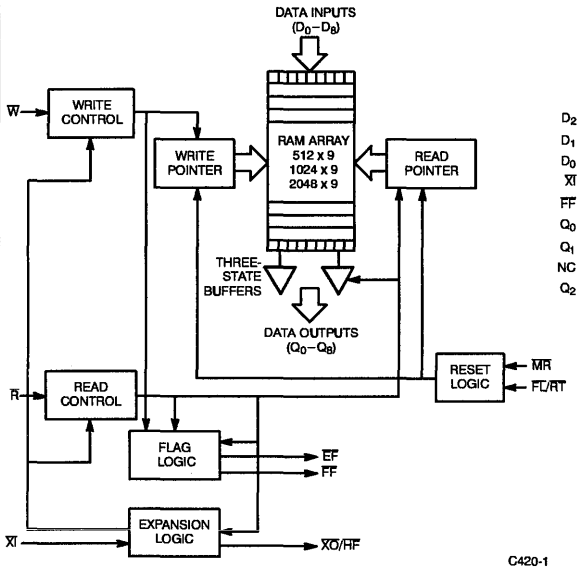
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

The CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, and CY7C429 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

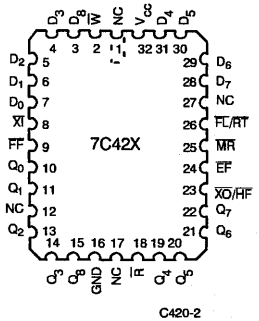
Logic Block Diagram



C420-1

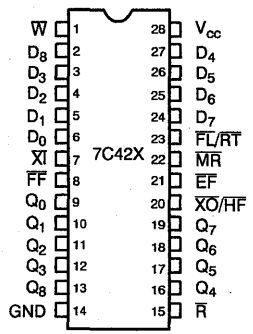
Pin Configurations

PLCC/LCC
Top View



C420-2

DIP
Top View



C420-3

CYPRESS SEMICONDUCTOR

Selection Guide

		7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20	7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25	7C420-30 7C421-30 7C424-30 7C425-30 7C428-30 7C429-30	7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40	7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65
Frequency (MHz)		33.3	28.5	25	20	12.5
Maximum Access Time (ns)		20	25	30	40	65
Maximum Operating Current (mA)	Commercial	142	132	125	115	100
	Military/Industrial		147	140	130	115

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20		7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25		7C420-30 7C421-30 7C424-30 7C425-30 7C428-30 7C429-30		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2..4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind			2.2	V_{CC}	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		142		132		125	mA
			Mil/Ind[4]				147		140	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		30		25		25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		25		20		20	mA
			Mil/Ind				25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90		− 90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 100 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 115 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

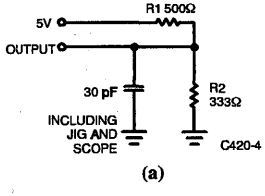
Parameter	Description	Test Conditions		7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40 Min.	7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40 Max.	7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65 Min.	7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2..4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		− 10	+10	− 10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		115		100	mA
			Mil/Ind[4]		130		115	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil		30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		20		20	mA
			Mil		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90	mA

Capacitance[6]

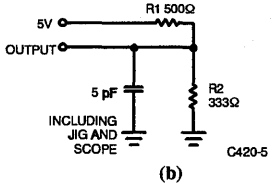
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

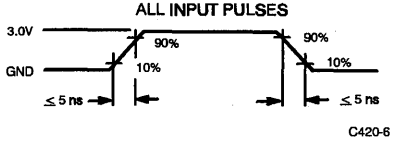
AC Test Loads and Waveforms



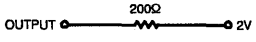
(a)



(b)



Equivalent to: THÉVENIN EQUIVALENT

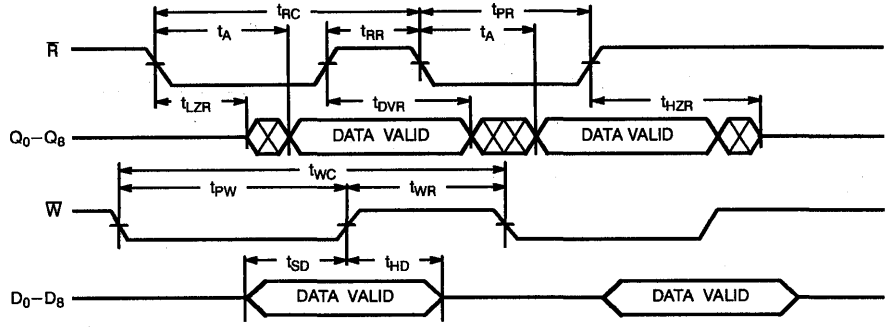


Switching Characteristics Over the Operating Range[7, 8]

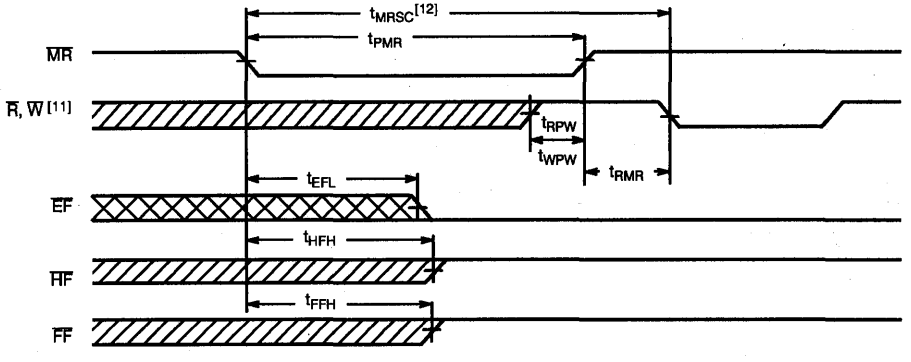
Parameter	Description	7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20		7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25		7C420–30 7C421–30 7C424–30 7C425–30 7C428–30 7C429–30		7C420–40 7C421–40 7C424–40 7C425–40 7C428–40 7C429–40		7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		35		40		50		80		ns
t_A	Access Time		20		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		10		15		ns
t_{PR}	Read Pulse Width	20		25		30		40		65		ns
t_{LZR}[9]	Read LOW to Low Z	3		3		3		3		3		ns
t_{DVR}[9,10]	Data Valid After Read HIGH	3		3		3		3		3		ns
t_{HZR}[9,10]	Read HIGH to High Z		15		18		20		25		30	ns
t_{WC}	Write Cycle Time	30		35		40		50		80		ns
t_{PW}	Write Pulse Width	20		25		30		40		65		ns
t_{HWZ}[9]	Write HIGH to Low Z	10		10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		10		15		ns
t_{SD}	Data Set-Up Time	12		15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	20		25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	30		35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	20		25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		30		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		30		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		25		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		30		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		20		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	20		25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		20		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	20		25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		20		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		20		25		30		40		65	ns

Switching Waveforms

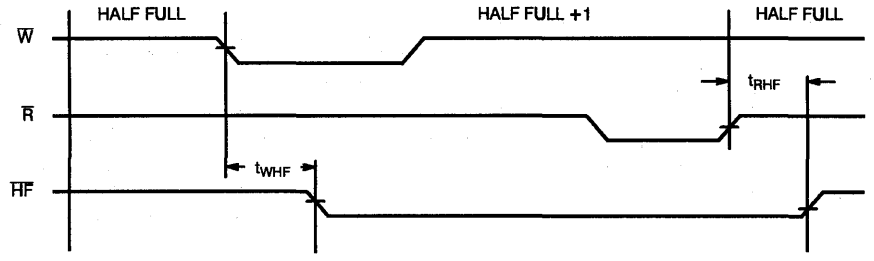
Asynchronous Read and Write



Master Reset



Half-Full Flag

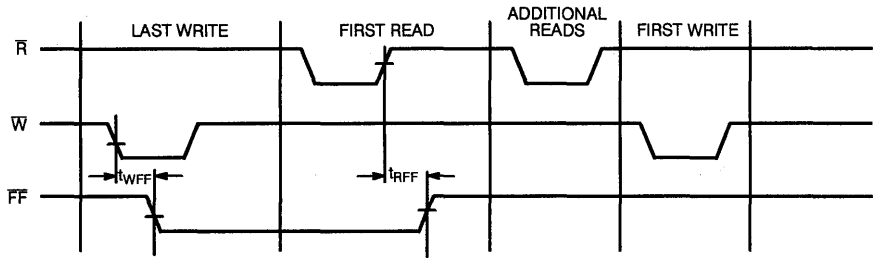


Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
10. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveforms.
11. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
12. $t_{MRSC} = t_{PMR} + t_{RMR}$.

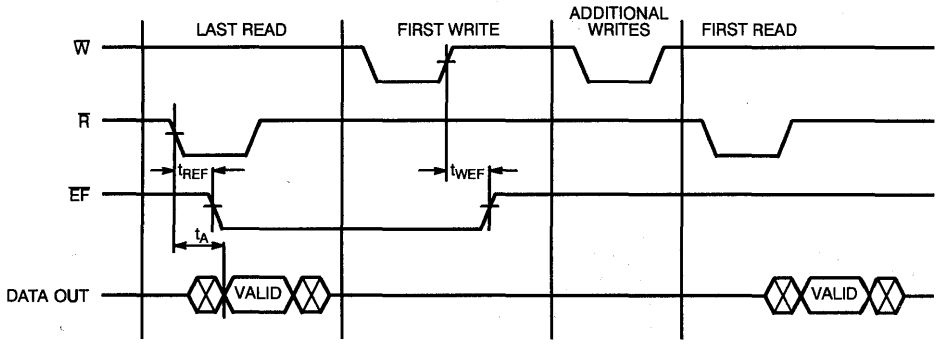
Switching Waveforms (continued)

Last Write to First Read Full Flag



C420-10

Last Read to First Write Empty Flag



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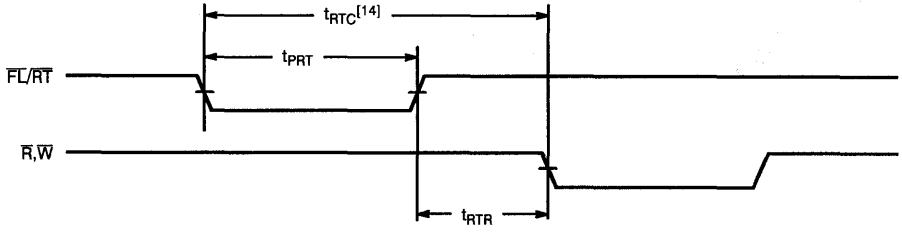
Retransmit[13]

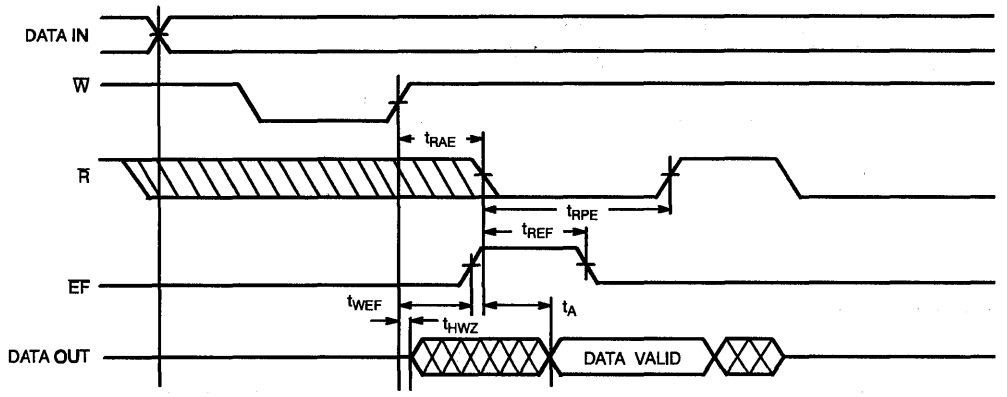


C420-12

Notes:
13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
14. $t_{RTC} = t_{PRT} + t_{RTR}$.

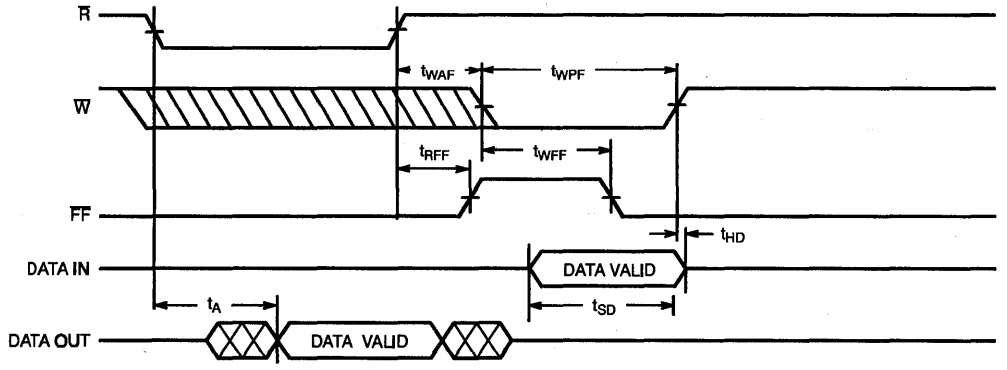
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



C420-13

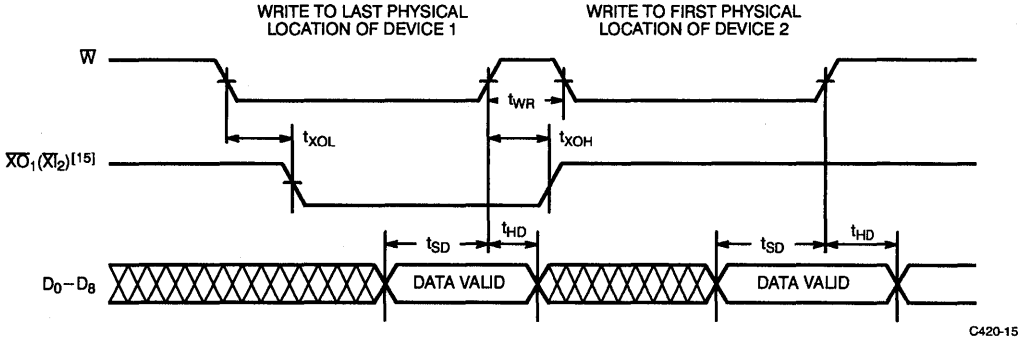
Full Flag and Write Data Flow-Through Mode

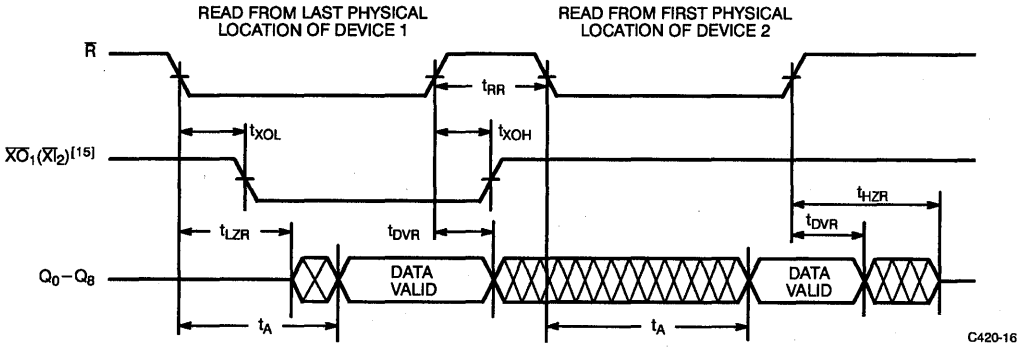


C420-14

Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
15. Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

Architecture

The CY7C420/421/424/425/428/429 FIFOs consist of an array of 512/1024/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{REF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH) when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly transmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

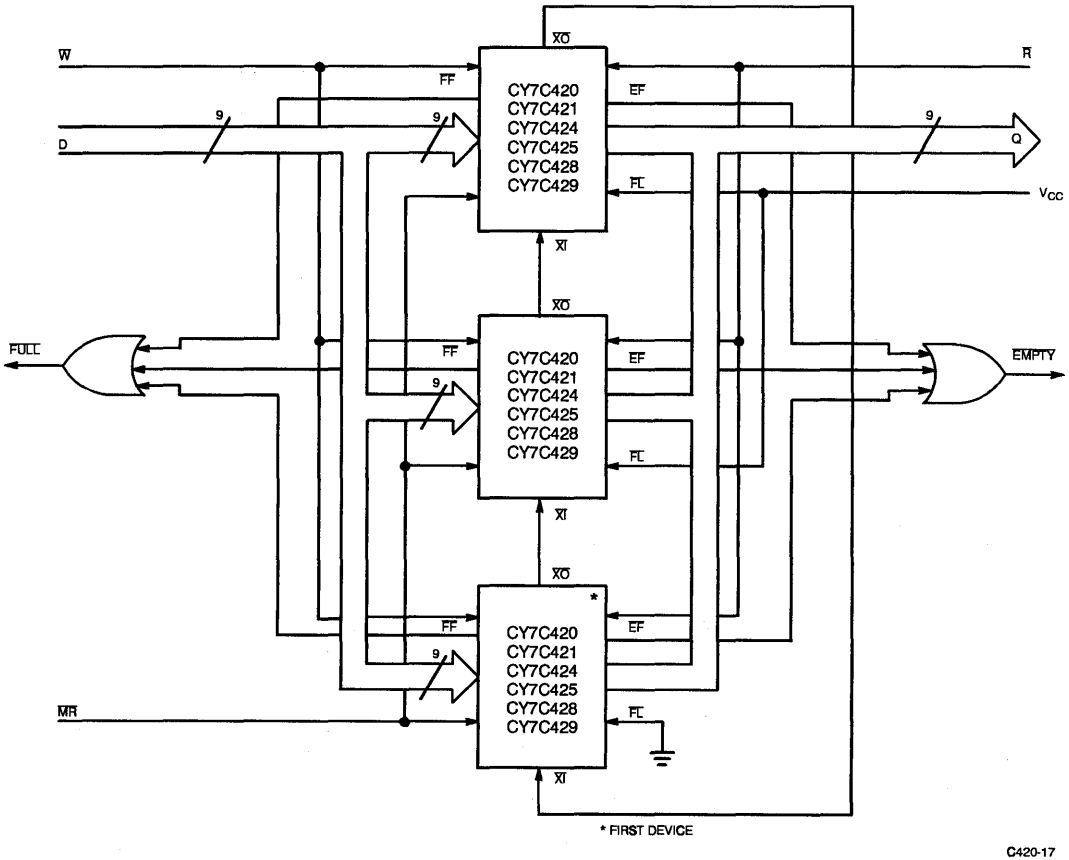
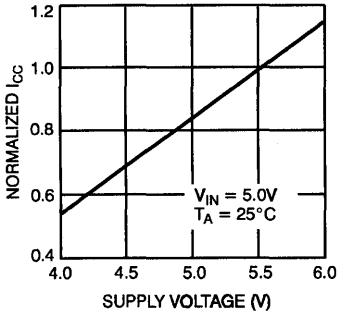


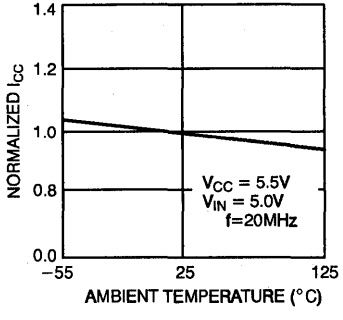
Figure 1. Depth Expansion

Typical DC and AC Characteristics

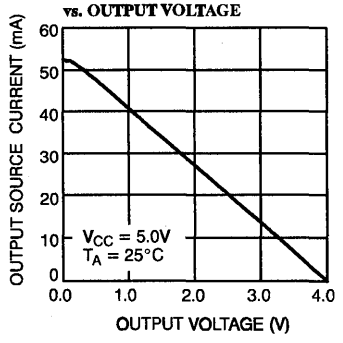
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



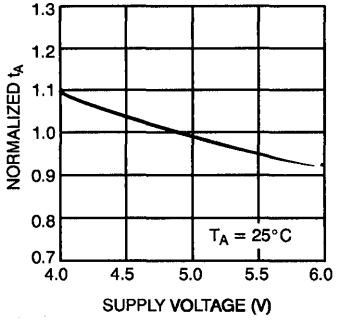
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



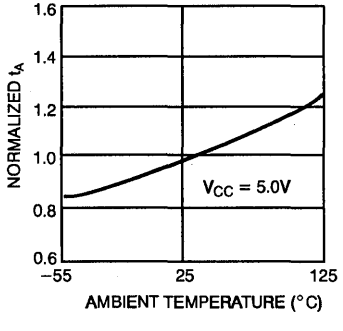
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



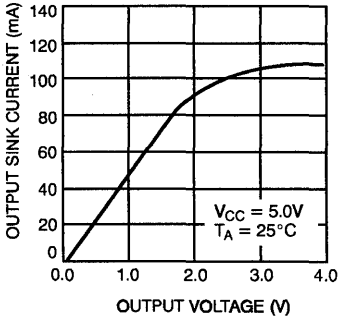
NORMALIZED t_A vs. SUPPLY VOLTAGE



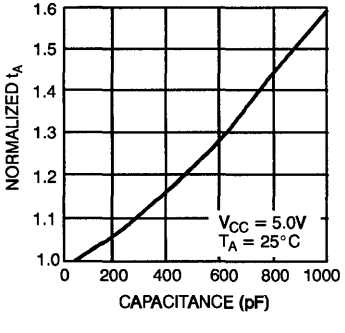
NORMALIZED t_A vs. AMBIENT TEMPERATURE



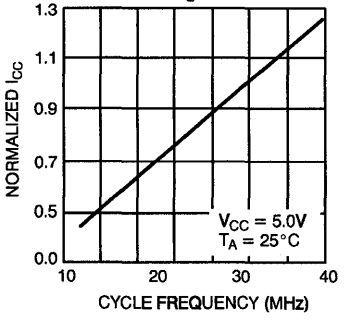
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED t_A CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE FREQUENCY



Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C420–20DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C420–20PC	P15	28-Lead (600-Mil) Molded DIP	
25	CY7C420–25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C420–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C420–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C420–30DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C420–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C420–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C420–40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C420–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C420–40PI	P15	28-Lead (600-Mil) Molded DIP	Industry
	CY7C420–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C420–65DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C420–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C420–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C421-20DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C421-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-20VC	V21	28-Lead (300-Mil) Molded SOJ	
25	CY7C421-25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C421-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-25KMB	K74	28-Lead Rectangular Cerpack	
	CY7C421-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C421-30DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C421-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-30KMB	K74	28-Lead Rectangular Cerpack	
	CY7C421-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C421-40DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C421-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C421-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C421-65DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C421-65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-65KMB	K74	28-Lead Rectangular Cerpack	
	CY7C421-65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C424–20DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C424–20PC	P15	28-Lead (600-Mil) Molded DIP	
25	CY7C424–25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C424–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C424–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C424–30DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C424–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C424–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C424–40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C424–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C424–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C424–65DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C424–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C424–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C425–20DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C425–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–20VC	V21	28-Lead (300-Mil) Molded SOJ	
25	CY7C425–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C425–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–25KMB	K74	28-Lead Rectangular Cerpack	
	CY7C425–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C425–30DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C425–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–30KMB	K74	28-Lead Rectangular Cerpack	
	CY7C425–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C425–40DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C425–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C425–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C425–65DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C425–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–65KMB	K74	28-Lead Rectangular Cerpack	
	CY7C425–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C428–20DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C428–20PC	P15	28-Lead (600-Mil) Molded DIP	
25	CY7C428–25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C428–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C428–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C428–30DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C428–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C428–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C428–40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C428–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C428–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C428–65DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C428–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C428–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C429–20DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C429–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–20VC	V21	28-Lead (300-Mil) Molded SOJ	
25	CY7C429–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C429–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–25KMB	K74	28-Lead Rectangular Cerpack	
	CY7C429–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C429–30DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C429–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–30KMB	K74	28-Lead Rectangular Cerpack	
	CY7C429–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C429–40DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C429–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C429–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C429–65DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C429–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–65KMB	K74	28-Lead Rectangular Cerpack	
	CY7C429–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38-00079-I

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C421A
CY7C425A

High-Speed Cascadable 512 x 9 FIFO 1K x 9 FIFO

Features

- **512 x 9 and 1K x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 66.6-MHz read/write independent of depth/width**
- **10-ns access time**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone mode**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil 28-pin DIP and 32-pin PLCC packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7201 and IDT7202**

Functional Description

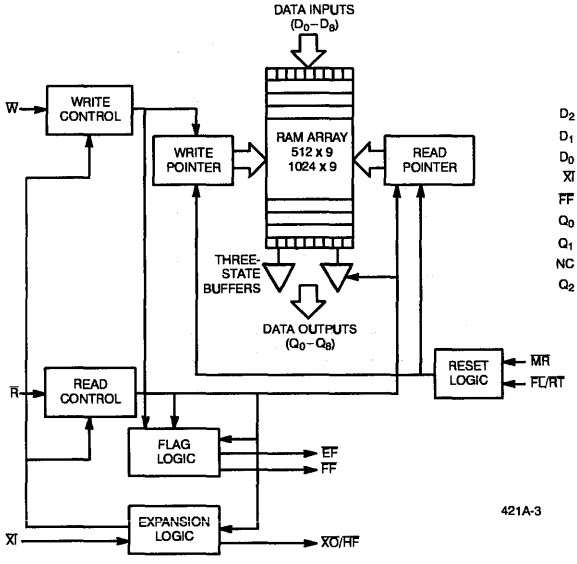
The CY7C421A and CY7C425A are first-in first-out (FIFO) memories. They are, respectively, 512 and 1,024 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 66.6 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

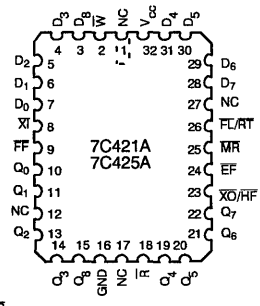
Logic Block Diagram



421A-3

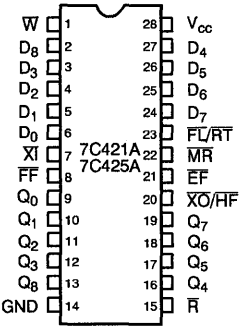
Pin Configurations

PLCC
Top View



421A-1

DIP
Top View



421A-2

Selection Guide

		7C421A–10 7C425A–10	7C421A–15 7C425A–15
Frequency (MHz)		66.6	40
Maximum Access Time (ns)		10	15
Maximum Operating Current (mA)	Commercial	10	15

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C421A–10 7C425A–10 Min.	7C421A–10 7C425A–10 Max.	7C421A–15 7C425A–15 Min.	7C421A–15 7C425A–15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		– 1	+1	– 1	+1	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}, V_{CC} = Max.		– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180		120	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		15		15	mA
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} – 0.2V	Com'l		5		5	mA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			– 90		– 90	mA

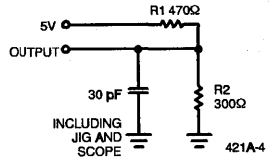
Capacitance[4]

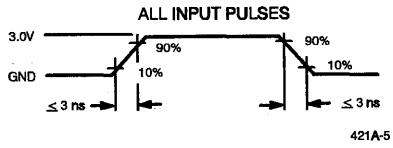
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		7	pF

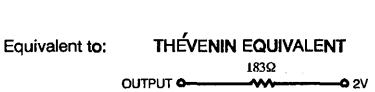
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





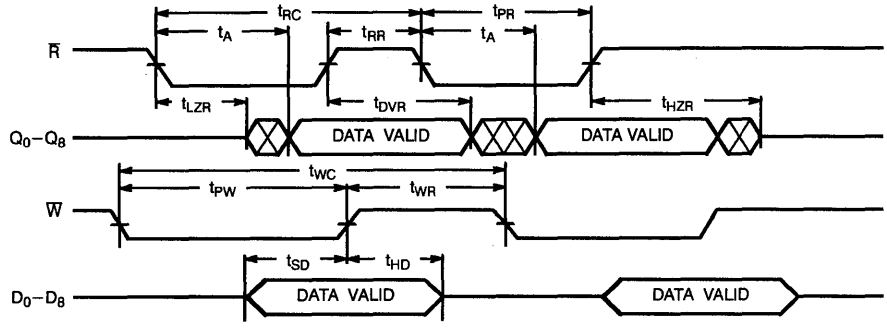


Switching Characteristics Over the Operating Range[5,6]

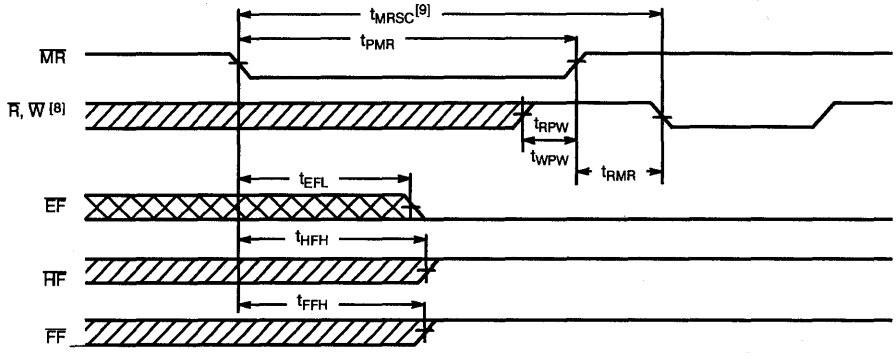
Parameter	Description	7C421A–10 7C425A–10		7C421A–15 7C425A–15		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	15		25		ns
t_A	Access Time		10		15	ns
t_{RR}	Read Recovery Time	5		10		ns
t_{PR}	Read Pulse Width	10		15		ns
t_{DVR}[7]	Data Valid After Read HIGH	5		5		ns
t_{HZR}[7]	Read HIGH to High Z		15		15	ns
t_{WC}	Write Cycle Time	15		25		ns
t_{PW}	Write Pulse Width	10		15		ns
t_{WR}	Write Recovery Time	5		10		ns
t_{SD}	Data Set-Up Time	8		10		ns
t_{HD}	Data Hold Time	0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	15		25		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		ns
t_{RMR}	$\overline{MR}$ Recovery Time	5		10		ns
t_{RTC}	Retransmit Cycle Time	15		25		ns
t_{PRT}	Retransmit Pulse Width	10		15		ns
t_{RTR}	Retransmit Recovery Time	5		10		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		10		15	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		10		15	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		10		15	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15	ns
t_{XOL}	Expansion Out LOW Delay from Clock		12		15	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		12		15	ns
t_{LZR}	Read LOW to Low Z	1		1		ns
t_{HWZ}	Write HIGH to Low Z	5		5		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{RAE}	Effective Read from Write HIGH		10		15	ns
t_{RPE}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns
t_{WAF}	Effective Write from Read HIGH		10		15	ns
t_{WPF}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns

Switching Waveforms

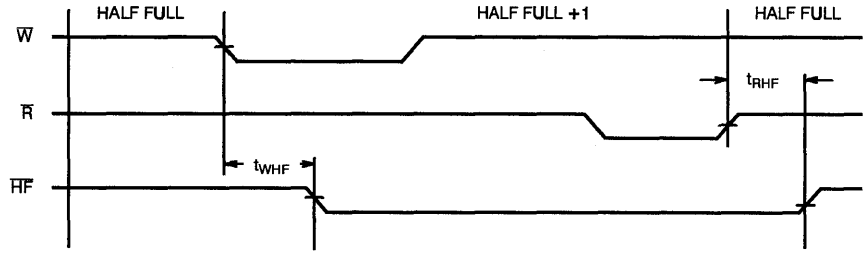
Asynchronous Read and Write



Master Reset



Half-Full Flag

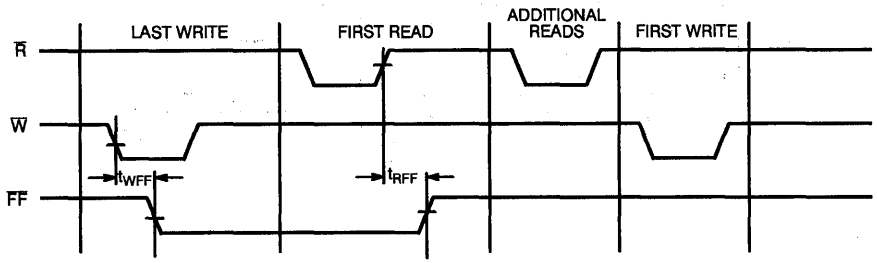


Notes:

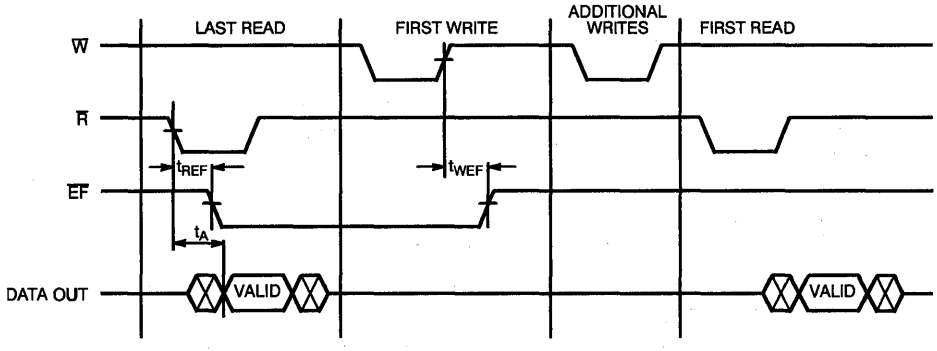
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
8. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)

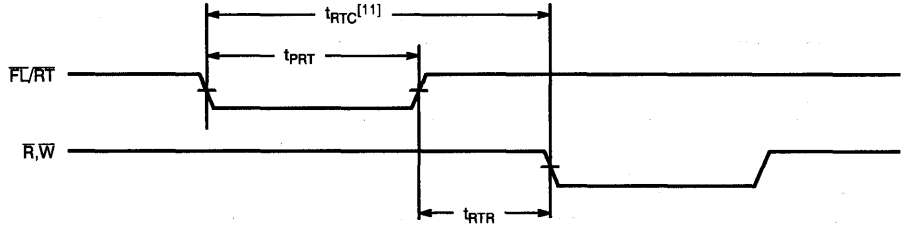
Last Write to First Read Full Flag



Last Read to First Write Empty Flag



Retransmit[10]

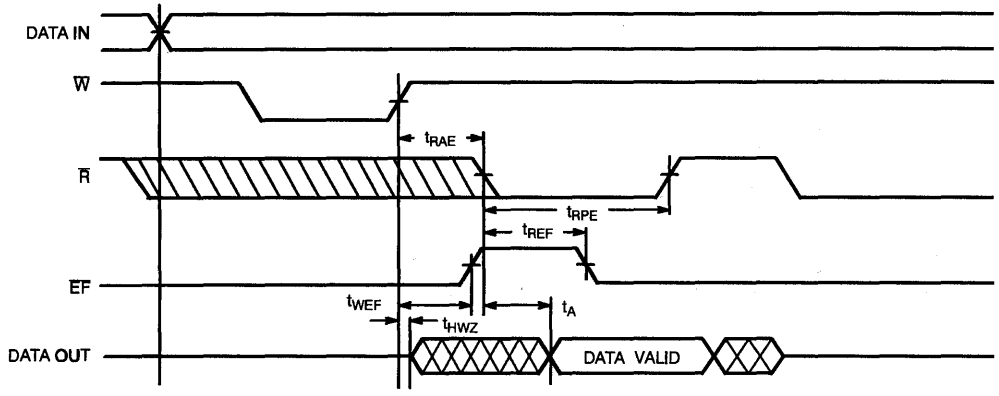


Notes:

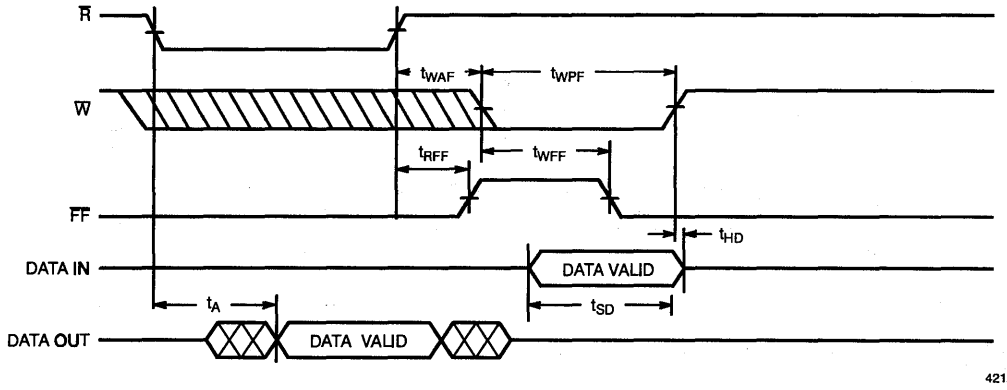
10. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
11. $t_{RTC} = t_{PRT} + t_{RTR}$.

Switching Waveforms (continued)

Empty Flag and Empty Boundary Timing Diagram

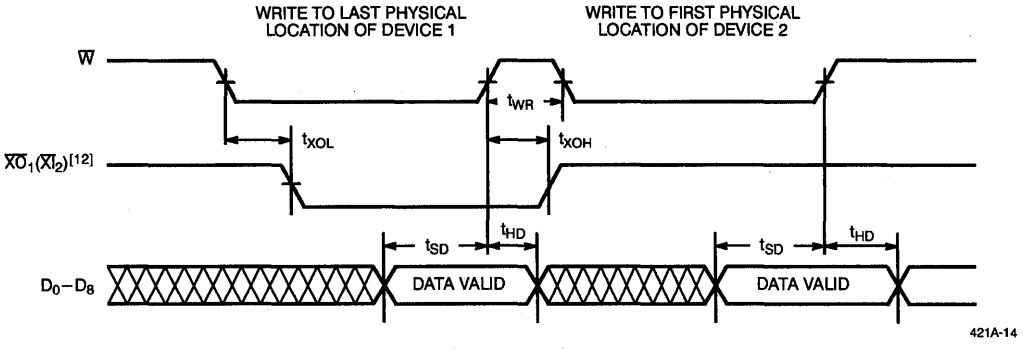


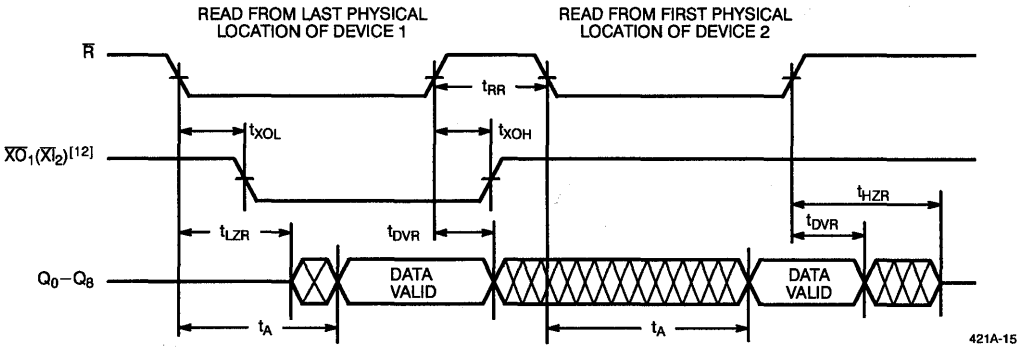
Full Flag and Full Boundary Timing Diagram



Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
12. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

Architecture

The CY7C421A/425A FIFOs consist of an array of 512/1024 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{REF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH) when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly transmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

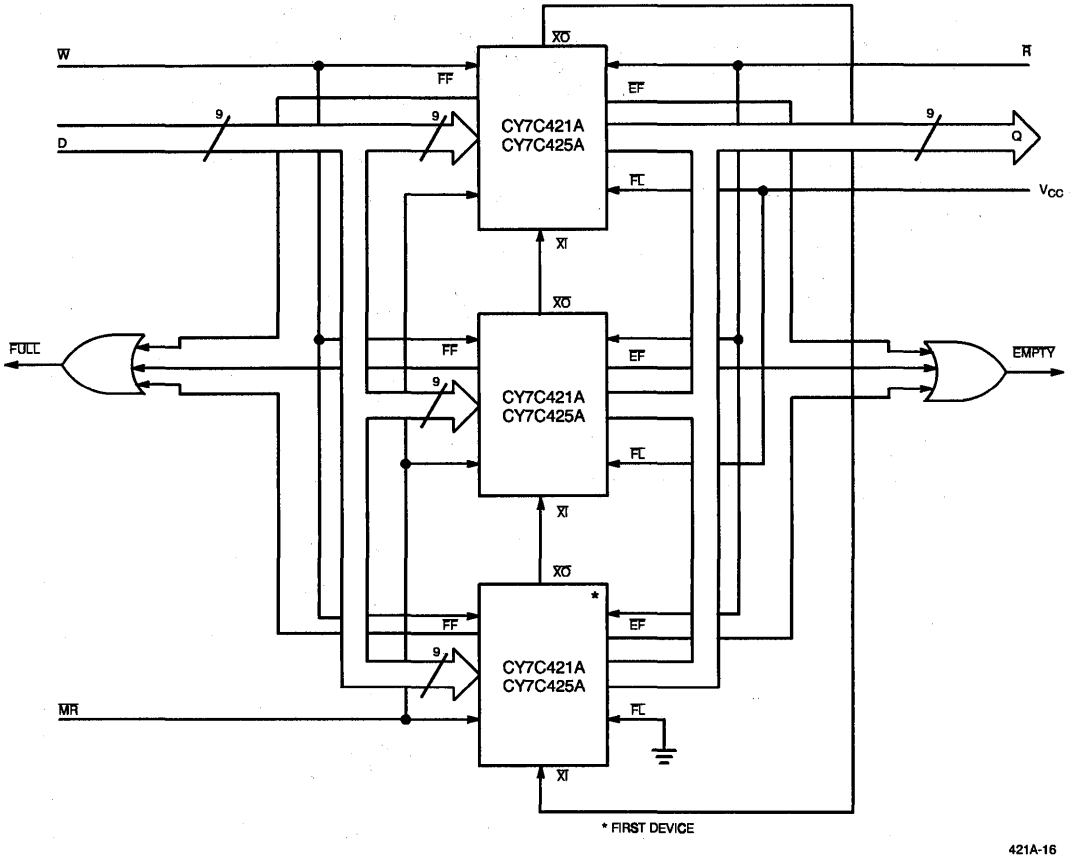


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C421A–10JC	J65	Commercial
	CY7C421A–10PC	P21	
15	CY7C421A–15JC	J65	Commercial
	CY7C421A–15PC	P21	

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C425A–10JC	J65	Commercial
	CY7C425A–10PC	P21	
15	CY7C425A–15JC	J65	Commercial
	CY7C425A–15PC	P21	

Document #: 38–00248

CY7C429A
CY7C433A

High-Speed Cascadable 2K x 9 FIFO 4K x 9 FIFO

Features

- **2,048 x 9 and 4,096 x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 66.6-MHz read/write independent of depth/width**
- **10-ns access time**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone mode**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil 28-pin DIP and 32-pin PLCC packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7203 and IDT7204**

Functional Description

The CY7C429A and CY7C433A are first-in first-out (FIFO) memories. They are, respectively, 2,048 and 4,096 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

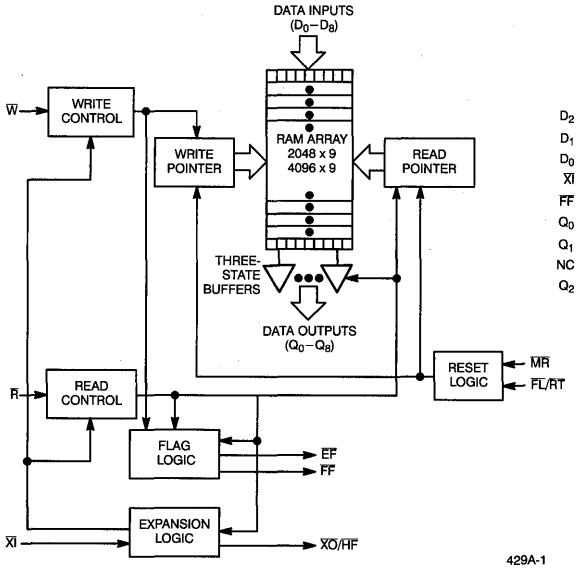
The read and write operations may be asynchronous; each can occur at a rate of 66.6 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

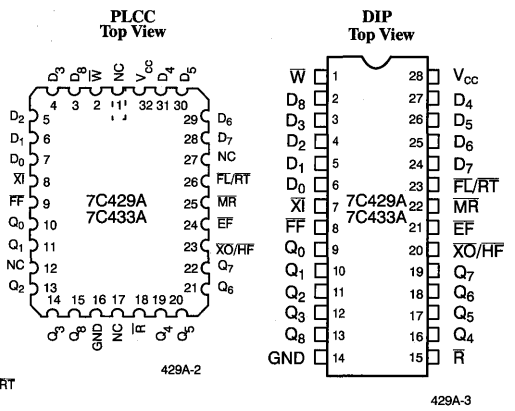
5 FIFOs

Logic Block Diagram



429A-1

Pin Configurations



Selection Guide

		7C429A–10 7C433A–10	7C429A–15 7C433A–15
Frequency (MHz)		66	40
Maximum Access Time (ns)		10	15
Maximum Operating Current (mA)	Commercial	180	120

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C429A–10 7C433A–10 Min.	 Max.	7C429A–15 7C433A–15 Min.	 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		– 1	+1	– 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}, V_{CC} = Max.		– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180		120	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		15		15	mA
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} – 0.2V	Com'l		5		5	mA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			– 50		– 50	mA

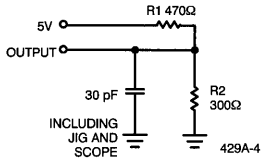
Capacitance[4]

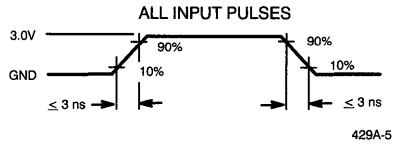
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz	7	pF

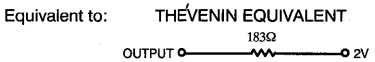
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





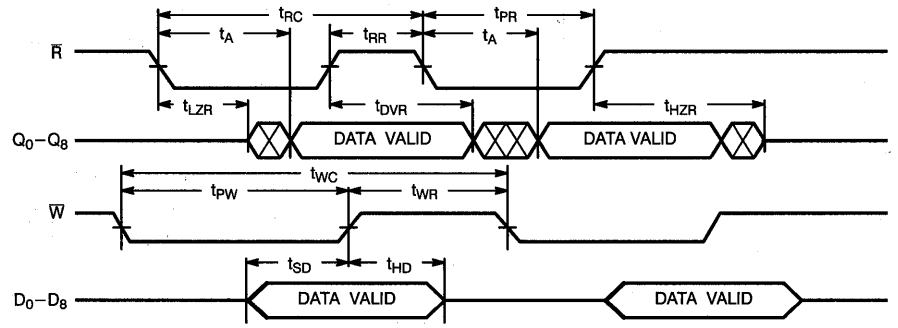


Switching Characteristics Over the Operating Range[5,6]

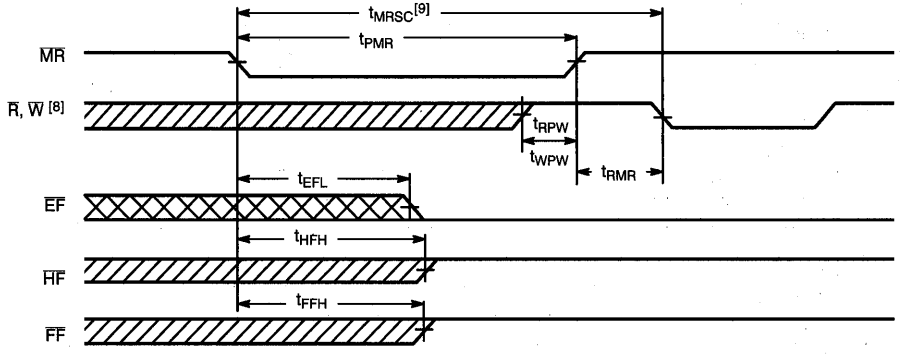
Parameter	Description	7C429A–10 7C433A–10		7C429A–15 7C433A–15		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	15		25		ns
t_A	Access Time		10		15	ns
t_{RR}	Read Recovery Time	5		10		ns
t_{PR}	Read Pulse Width	10		15		ns
t_{DVR}[7]	Data Valid After Read HIGH	5		5		ns
t_{HZR}[7]	Read HIGH to High Z		15		15	ns
t_{WC}	Write Cycle Time	15		25		ns
t_{PW}	Write Pulse Width	10		15		ns
t_{WR}	Write Recovery Time	5		10		ns
t_{SD}	Data Set-Up Time	8		10		ns
t_{HD}	Data Hold Time	0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	15		25		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		ns
t_{RMR}	$\overline{MR}$ Recovery Time	5		10		ns
t_{RTC}	Retransmit Cycle Time	15		25		ns
t_{PRT}	Retransmit Pulse Width	10		15		ns
t_{RTR}	Retransmit Recovery Time	5		10		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		10		15	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		10		15	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		10		15	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15	ns
t_{XOL}	Expansion Out LOW Delay from Clock		12		15	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		12		15	ns
t_{LZR}	Read LOW to Low Z	1		1		ns
t_{HWZ}	Write HIGH to Low Z	5		5		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{RAE}	Effective Read from Write HIGH		10		15	ns
t_{RPE}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns
t_{WAF}	Effective Write from Read HIGH		10		15	ns
t_{WPF}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns

Switching Waveforms

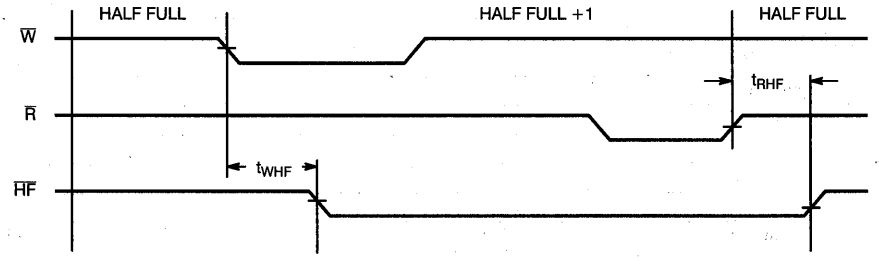
Asynchronous Read and Write



Master Reset



Half-Full Flag

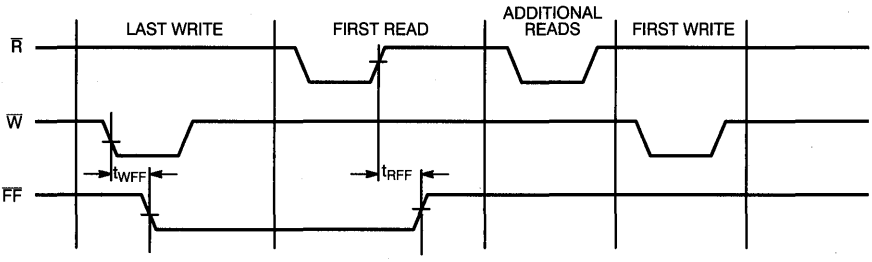


Notes:

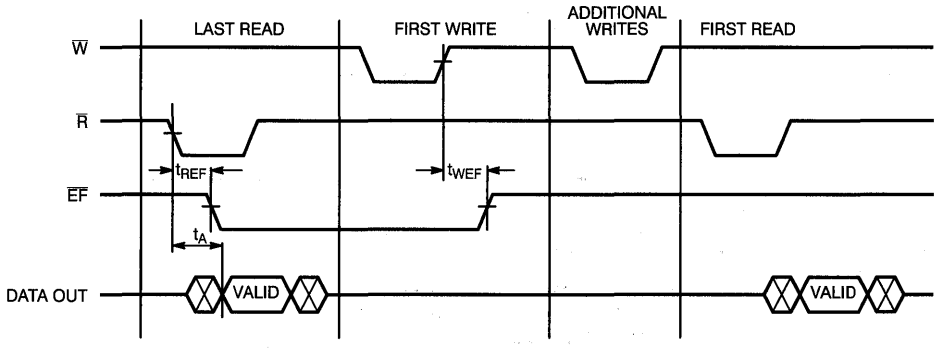
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
8. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)

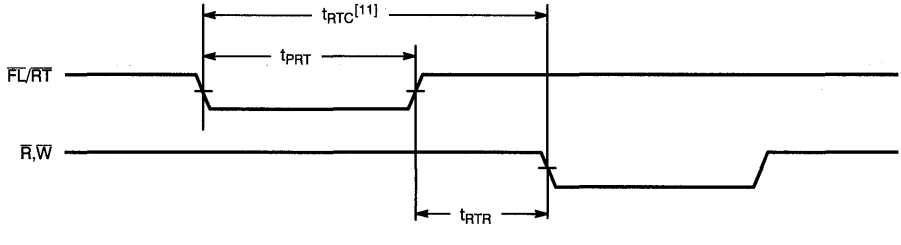
Last Write to First Read Full Flag



Last Read to First Write Empty Flag



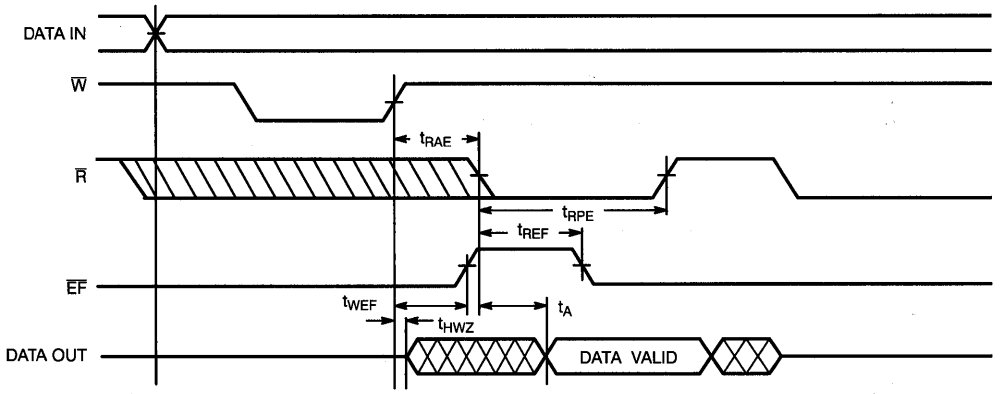
Retransmit[10]



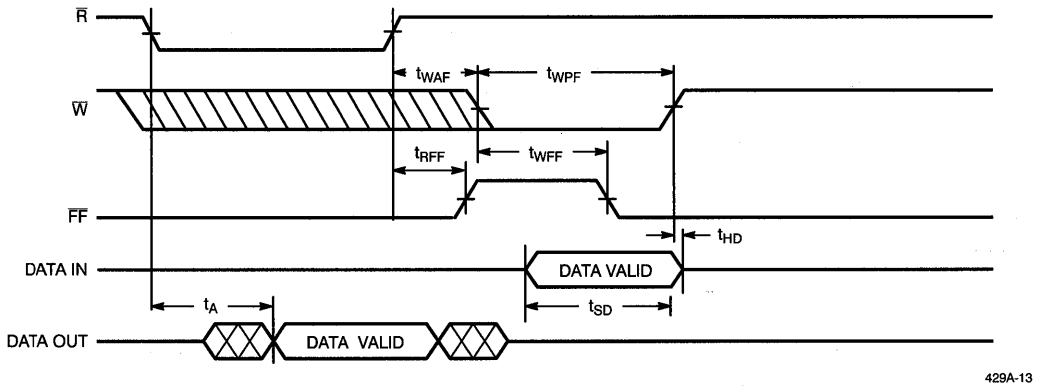
Notes:
10. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
11. $t_{RTC} = t_{PRT} + t_{RTR}$.

Switching Waveforms (continued)

Empty Flag and Empty Boundary Timing Diagram

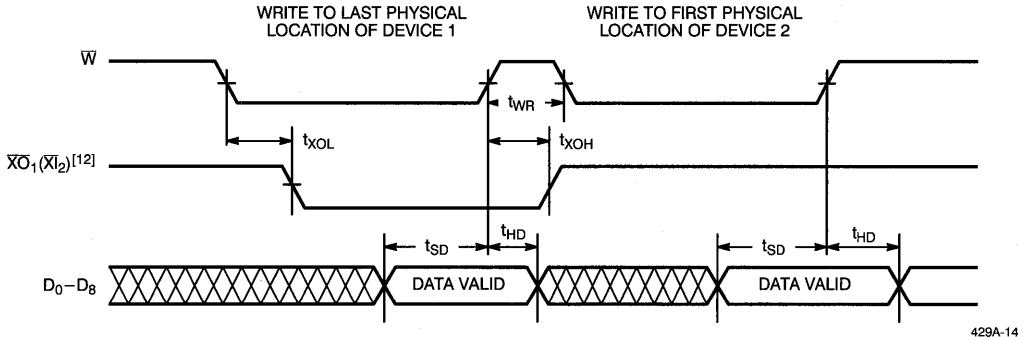


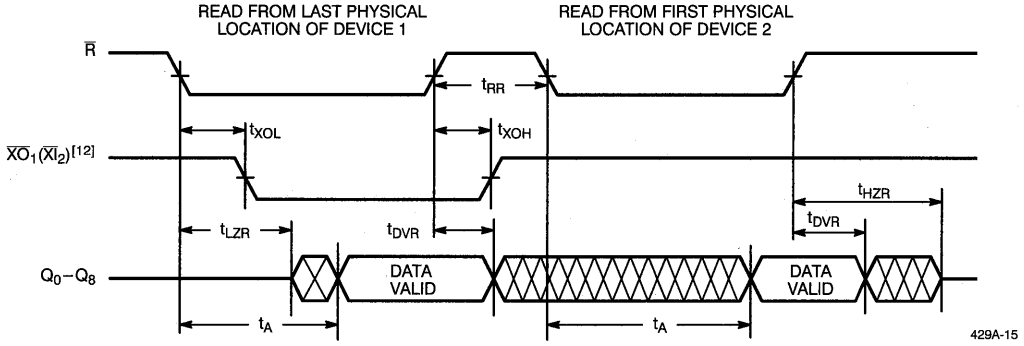
Full Flag and Full Boundary Timing Diagram



Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
12 Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

Architecture

The CY7C429A/433A FIFOs consist of an array of 1024/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{REF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH) when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly transmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

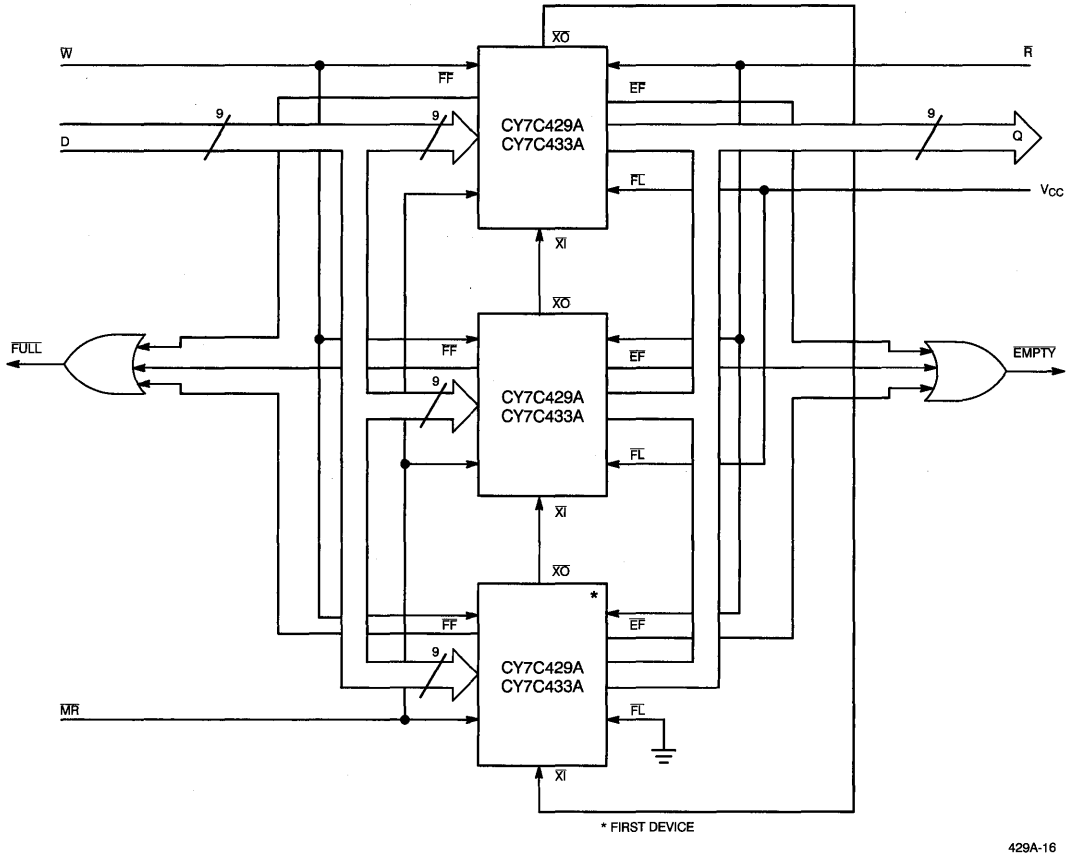


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C429A–10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C429A–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433A–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433A–10PC	P21	28-Lead (300-Mil) Molded DIP	
15	CY7C429A–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C429A–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433A–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433A–15PC	P21	28-Lead (300-Mil) Molded DIP	

Document #: 38–00249

CY7C432
CY7C433

CYPRESS SEMICONDUCTOR

Cascadable 4K x 9 FIFO

Features

- **4096 x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 28.5-MHz read/write independent of depth/width**
- **25-ns access time**
- **Low operating power**
  - **I_{CC} (max.) = 142 mA commercial**
  - **I_{CC} (max.) = 155 mA military**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Expandable in width and depth**
- **Retransmit in standalone**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil DIP packaging**
- **300-mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functionally equivalent to IDT7204**

Functional Description

The CY7C432 and CY7C433 are first-in first-out (FIFO) memories offered in 600-mil-wide and 300-mil-wide packages, respectively. They are 4096 words by 9 bits wide. Each FIFO memory is organized so that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

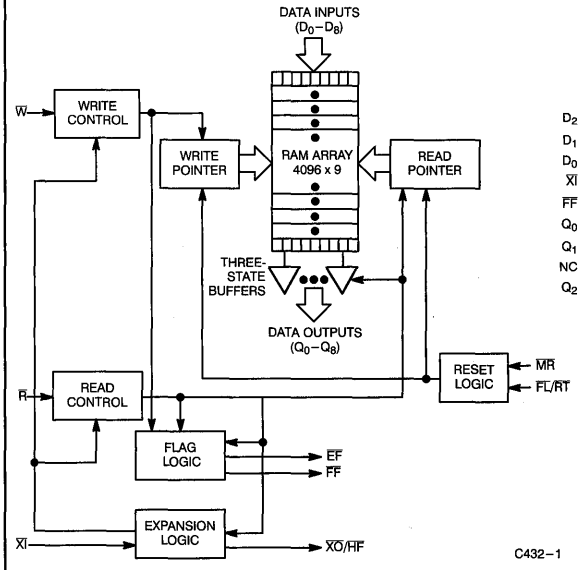
The read and write operations may be asynchronous; each can occur at a rate of 28.5 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

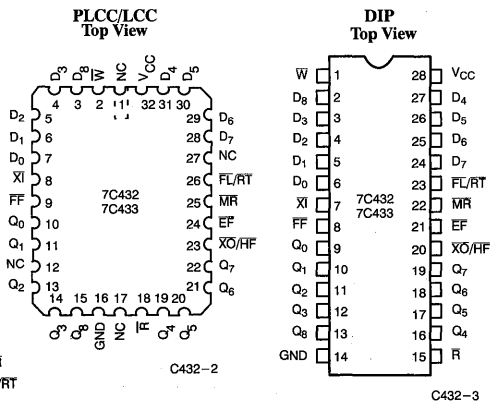
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C432 and CY7C433 are fabricated using advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C432–25 7C433–25	7C432–30 7C433–30	7C432–40 7C433–40	7C432–65 7C433–65
Frequency (MHz)		28.5	25	20	12.5
Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	142	135	125	110
	Military/Industrial		155	145	130

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Power Dissipation 0.88W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C432–25 7C433–25 Min.	7C432–25 7C433–25 Max.	7C432–30 7C433–30 Min.	7C432–30 7C433–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind			2.2	V_{CC}	
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		140		135	mA
			Mil/Ind[4]				155	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind				30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} – 0.2V	Com'l		20		20	mA
			Mil/Ind				25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			–90		–90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 110 mA + [($\bar{f}$ – 12.5) • 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 130 mA + [($\bar{f}$ – 12.5) • 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

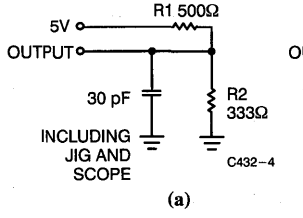
Parameter	Description	Test Conditions		77C432-40 77C433-40 Min.	77C432-40 77C433-40 Max.	77C432-65 77C433-65 Min.	77C432-65 77C433-65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		125		110	mA
			Mil/Ind[4]		145		130	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind		30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		20		20	mA
			Mil/Ind		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA

Capacitance[6]

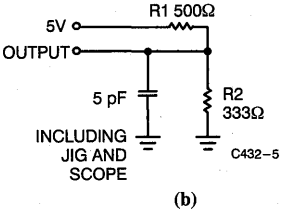
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

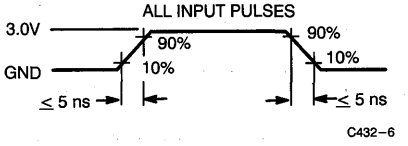
AC Test Loads and Waveforms



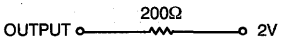
(a)



(b)



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7,8]

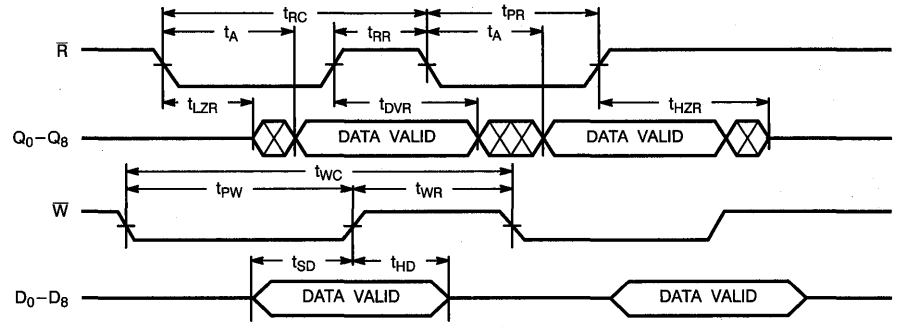
Parameter	Description	7C432–25 7C433–25		7C432–30 7C433–30		7C432–40 7C433–40		7C432–65 7C433–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_A	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[9,10]	Read HIGH to Data Valid	3		3		3		3		ns
t_{HZR}[9,10]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[9]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{FF}$ HIGH	25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		25		30		40		65	ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
10. t_{HZR} and t_{DVR} use capacitance loading as in part (a) of AC Test Loads.

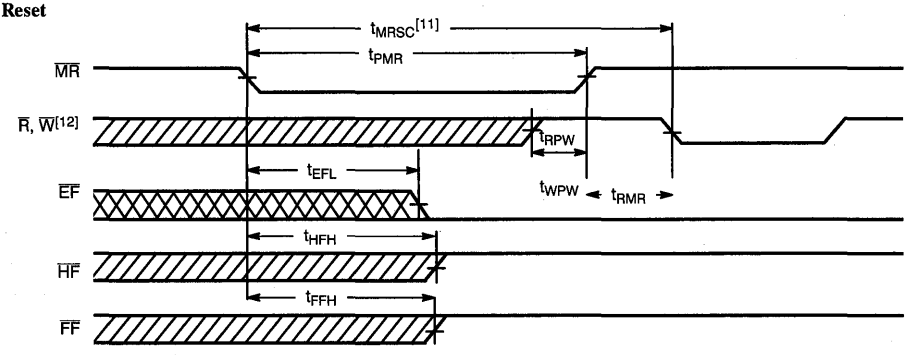
Switching Waveforms

Asynchronous Read and Write



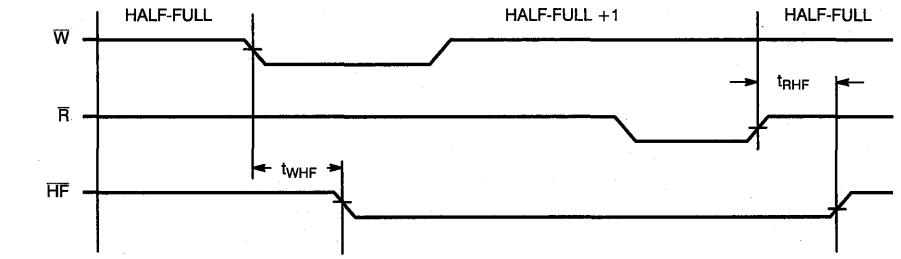
C432-7

Master Reset



C432-8

Half-Full Flag

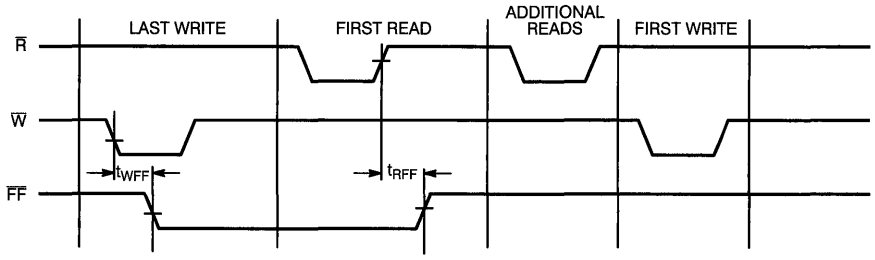


C432-9

Notes:
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.
12. $\overline{W}$ and $\overline{R} \geq V_{IH}$ for at least t_{WPW} or t_{RPR} before the rising edge of $\overline{MR}$.

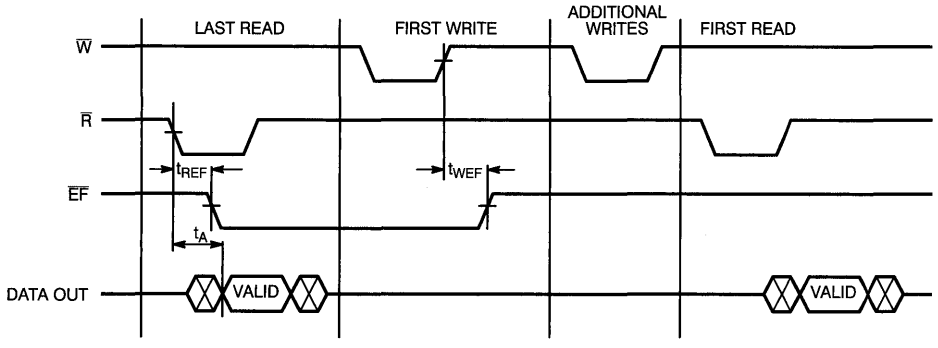
Switching Waveforms (continued)

Last Write to First Read Full Flag



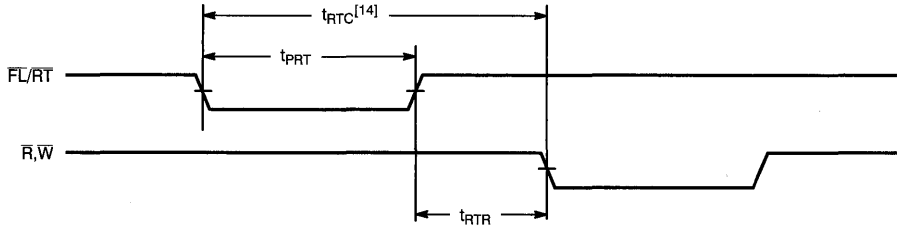
C432–10

Last Read to First Write Empty Flag



C432–11

Retransmit[13]



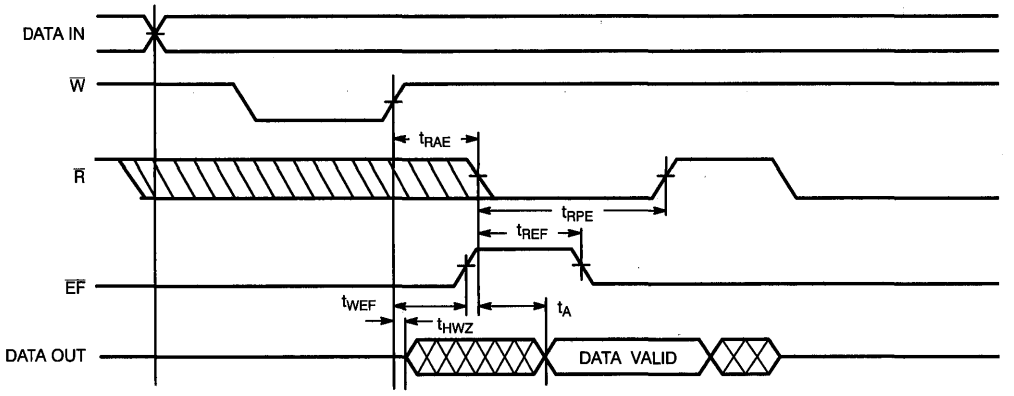
C432–12

Notes:

13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
14. $t_{RTC} = t_{PRT} + t_{RTR}$.

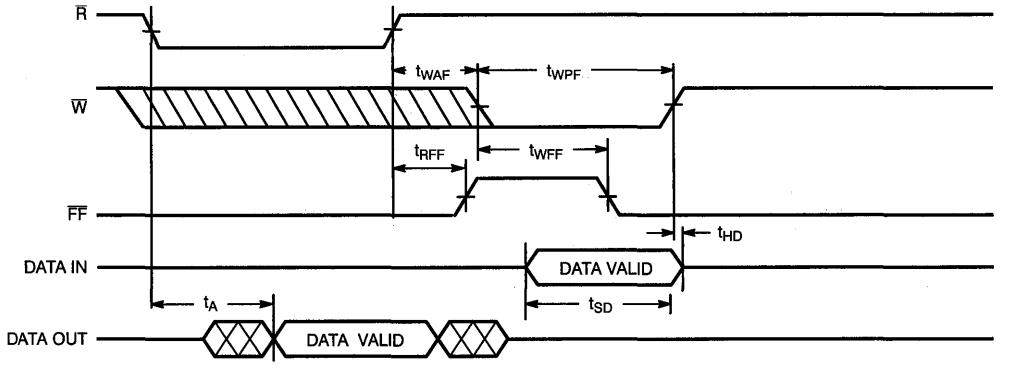
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



C432–13

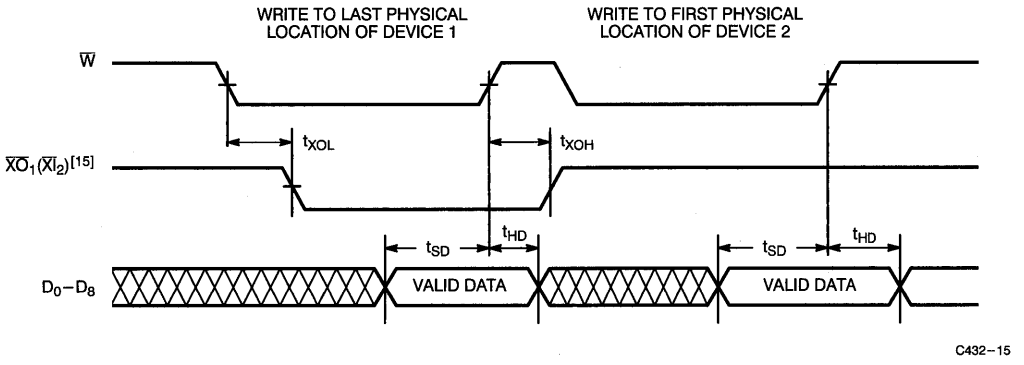
Full Flag and Write Data Flow-Through Mode

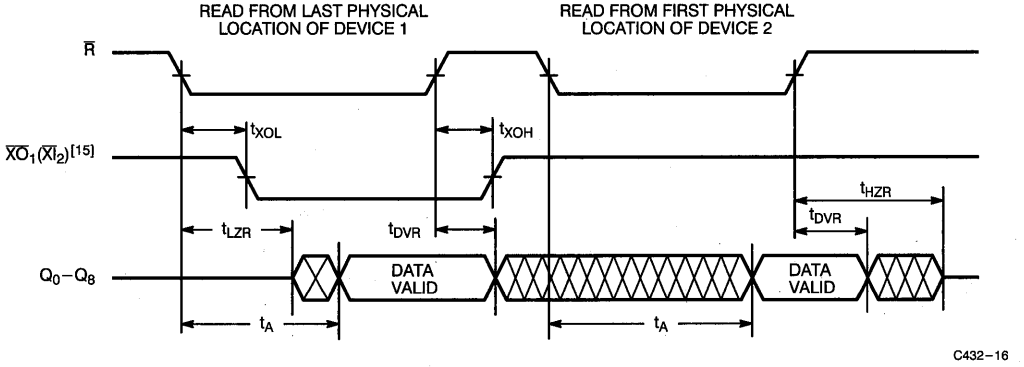


C432–14

Switching Waveforms (continued)

Expansion





Note:
15. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

Architecture

The CY77C432/33 FIFOs consist of an array of 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operations of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} nanoseconds before and t_{RMR} nanoseconds after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ($\overline{FF}$). A falling edge of write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW-to-HIGH transition occurs t_{WEF} nanoseconds after the first LOW-to-HIGH transition on the write clock of an empty FIFO. The Half Full flag ($\overline{HF}$) will go LOW on the falling edge of the write clock following the occurrence of half full. $\overline{HF}$ will remain LOW while less than one half of the total memory of this device is available for writing. The LOW-to-HIGH transition of the $\overline{HF}$ flag occurs on the rising edge of read ($\overline{R}$). $\overline{HF}$ is available in single device mode only. The Full flag ($\overline{FF}$) goes LOW on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs (Q_0-Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the depth expansion mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH-to-LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be interrogated by the receiver and retransmitted if necessary.

The retransmit ($\overline{RT}$) input is active in the single device mode only. The retransmit feature is intended for use when 4096 or less writes have occurred since the previous $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and will be updated by a retransmit operation.

After a retransmit cycle, previously read data may be reaccessed using $\overline{R}$ to initiate standard read cycles beginning with the first physical location.

Single Device/Width Expansion Modes

Single device and width expansion modes are entered by connecting $\overline{XI}$ to ground prior to an $\overline{MR}$ cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During width expansion mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion Out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the first load ($\overline{FL}$) input, when grounded, indicates that this part is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

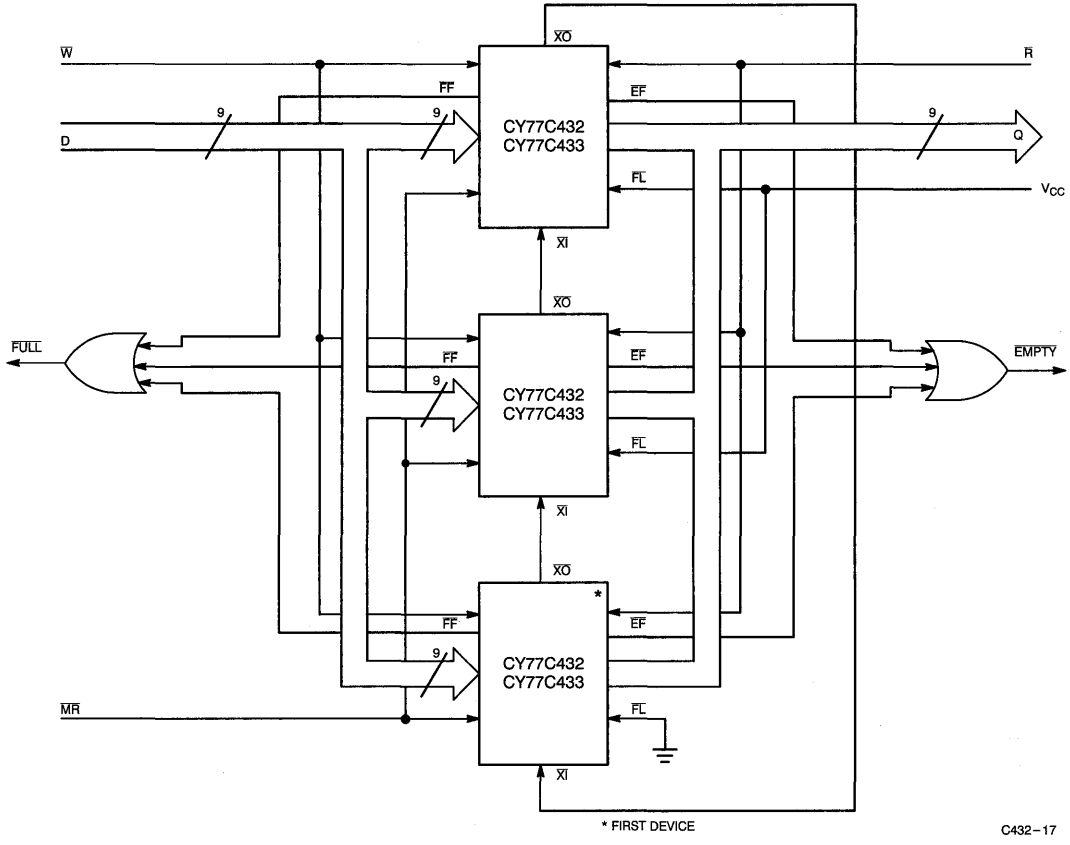
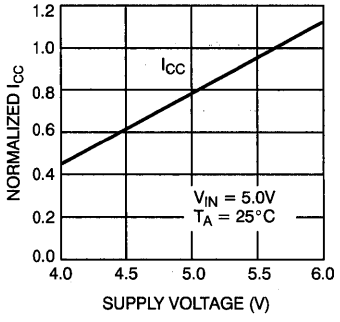


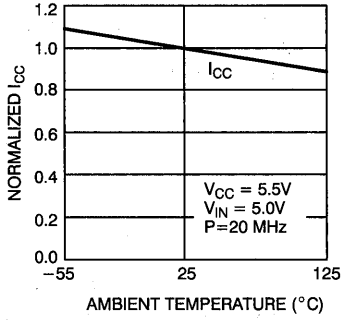
Figure 1. Depth Expansion

Typical DC and AC Characteristics

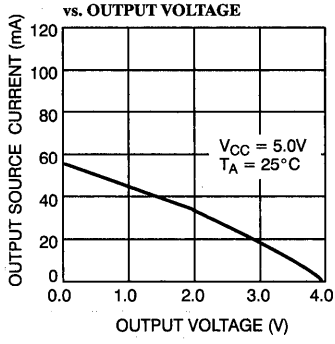
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



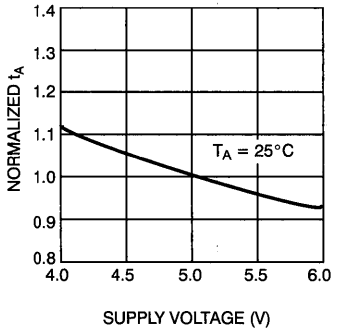
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



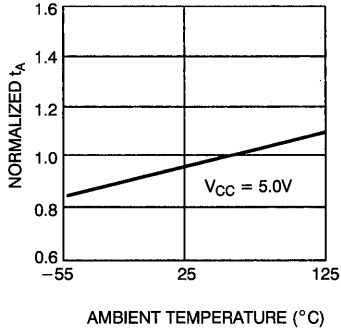
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



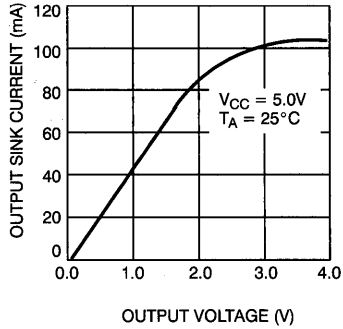
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



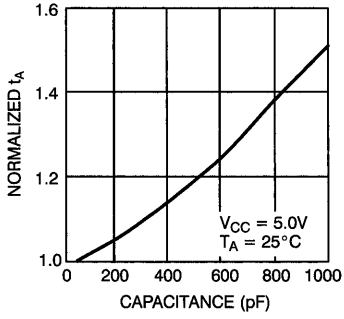
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



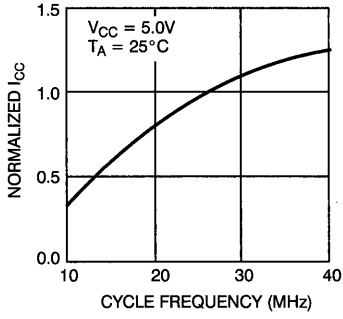
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



C432–18

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C432–25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–25PC	P15	28-Lead (600-Mil) Molded DIP	
30	CY7C432–30DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C432–40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C432–65DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C433–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VC	V21	28-Lead (300-Mil) Molded SOJ	
30	CY7C433–30DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–30KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C433–40DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C433–65DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–65KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38-00109-C

CYPRESS SEMICONDUCTOR

CY7C439

Bidirectional 2K x 9 FIFO

Features

- **2048 x 9 FIFO buffer memory**
- **Bidirectional operation**
- **High-speed 28.5-MHz asynchronous reads and writes**
- **Simple control interface**
- **Registered and transparent bypass modes**
- **Flags indicate Empty, Full, and Half Full conditions**
- **5V ± 10% supply**
- **Available in 300-mil DIP, PLCC, LCC, and SOJ packages**
- **TTL compatible**

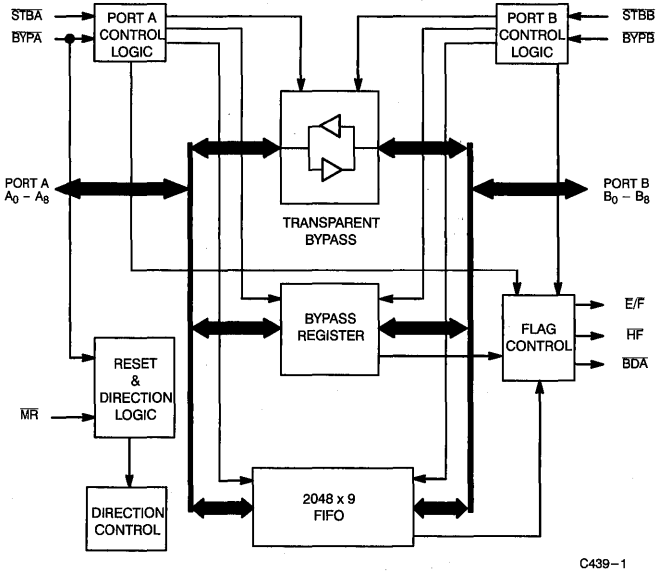
Functional Description

The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block—$\overline{E}/\overline{F}$ (Empty/Full) and $\overline{HF}$ (Half Full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin ($\overline{MR}$) and the bypass/direction pin ($\overline{BYPA}$). There are no control or status registers on the CY7C439, making the part simple to use while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 28.5 MHz. The port designated as the write port drives its strobe pin ($\overline{STBX}$, X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin ($\overline{BYPX}$, X = A or B) to remain HIGH.

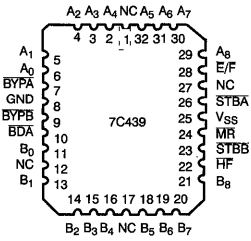
In addtion to the FIFO, two other data paths are provided; registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The

Logic Block Diagram



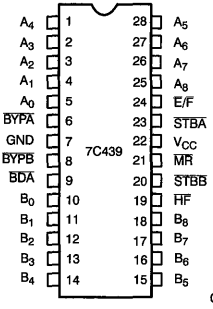
Pin Configurations

PLCC/LCC
Top View



C439-2

DIP
Top View



C439-3

Selection Guide

		7C439-25	7C439-30	7C439-40	7C439-65
Frequency (MHz)		28.5	25	20	12.5
Maximum Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	147	140	130	115
	Military		170	160	145

Functional Description (continued)

bypass register provides a means of sending a 9-bit status or control word to the FIFO-write port. The bypass data available pin ($\overline{BDA}$) indicates whether the bypass register is full or empty. The direction of the bypass register is always opposite to that of the main FIFO.

The port designated to write to the bypass register drives its bypass control pin ($\overline{BYPX}$) LOW. The other port detects the presence of data by monitoring $\overline{BDA}$ and reads the data by driving its bypass control pin ($\overline{BYPX}$) LOW. Registered bypass operations require that the associated FIFO strobe pin ($\overline{STBX}$) remains HIGH. Registered bypass operations do not affect data residing in the FIFO, or FIFO operations at the other port.

Transparent bypass provides a means of transferring a single word (9 bits) of data immediately in either direction. This feature allows the device to act as a simple 9-bit bidirectional buffer. This is useful for allowing the controlling circuitry to access a dumb peripheral for control/programming information.

For transparent bypass, the port wishing to send immediate data to the other side drives both its bypass and its strobe pins LOW simultaneously. This causes the buffered data to be driven out of the other port. On-chip circuitry detects conflicting use of the control pins and causes both data ports to enter a high-impedance state until the conflict is resolved.

Additionally, a Test mode is offered on the CY7C439. This mode allows the user to load data into the FIFO and then read it back out of the same port. Built-In Self Test (BIST) and diagnostic functions can take advantage of these features.

The CY7C439 is fabricated using an advanced 0.8µ N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Power Dissipation 1.0W

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPA}$ and $\overline{STBA}$
$B_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPB}$ and $\overline{STBB}$
$\overline{BYPA}$	I	Registered Bypass Mode Select for A Side
$\overline{BYPB}$	I	Registered Bypass Mode Selectr for B Side
$\overline{BDA}$	O	Bypass Data Available Flag
$\overline{STBA}$	I	Data Strobe for A Side
$\overline{STBB}$	I	Data Strobe for B Side
$\overline{E/F}$	O	Encoded Empty/Full Flag
$\overline{HF}$	O	Half Full Flag
$\overline{MR}$	I	Master Reset

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C439–25 Min.	7C439–25 Max.	7C439–30 Min.	7C439–30 Max.	7C439–40 Min.	7C439–40 Max.	7C439–65 Min.	7C439–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
			Mil			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{STBX}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		147		140		130		115	mA
			Mil[4]				170		160		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		40		40		40		40	mA
			Mil				45		45		45	
I_{SB2}	Power-Down Current	All Inputs V_{CC} – 0.2V	Com'l		20		20		20		20	mA
			Mil				25		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			– 90		– 90		– 90		– 90	mA

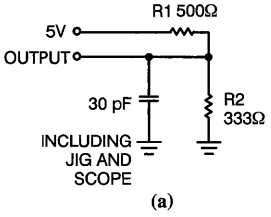
Capacitance[6]

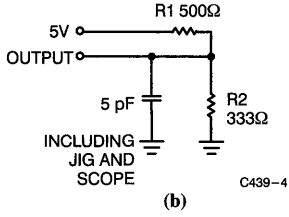
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

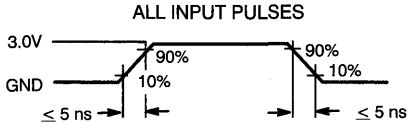
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 115 mA + [($\bar{f}$ – 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 145 mA + [($\bar{f}$ – 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveform



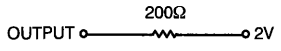


C439–4



C439–5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7,8]

Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_A	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[9,10]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[9,10]	Data Valid from Read HIGH	3		3		3		3		ns
t_{HZR}[9,10]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[9,10]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPS}	$\overline{STBX}$ HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RPBS}	$\overline{BYPA}$ to $\overline{MR}$ HIGH	10		10		15		20		ns
t_{RPBH}	$\overline{BYPA}$ Hold after $\overline{MR}$ HIGH	0		0		0		0		ns
t_{BDH}	$\overline{MR}$ LOW to $\overline{BDA}$ HIGH		35		40		50		80	ns
t_{BSR}	$\overline{STBX}$ HIGH to $\overline{BYPA}$ LOW	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{BRS}	$\overline{BYPX}$ HIGH to $\overline{STBX}$ LOW	10		10		10		15		ns
t_{REF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Read)		25		30		35		60	ns
t_{RFF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Read)		25		30		35		60	ns
t_{WEF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Write)		25		30		35		60	ns
t_{WFF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Write)		25		30		35		60	ns
t_{BDA}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ LOW (Write)		25		30		35		60	ns
t_{BDB}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ HIGH (Read)		25		30		35		60	ns
t_{BA}	$\overline{BYPX}$ LOW to Data Valid (Read)		30		30		40		60	ns
t_{BHZ}[9,10]	$\overline{BYPX}$ HIGH to High Z (Read)		18		20		25		30	ns
t_{TSB}	$\overline{STBX}$ HIGH to $\overline{BYPX}$ LOW Set-Up	10		10		10		15		ns
t_{TBS}	$\overline{STBX}$ LOW after $\overline{BYPX}$ LOW	0	10	0	10	0	10	0	10	ns
t_{TSN}	$\overline{STBX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TSD}[9,10]	$\overline{STBX}$ HIGH to Data High Z		18		20		25		30	ns
t_{TBN}	$\overline{BYPX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TBD}	$\overline{BYPX}$ HIGH to Data High Z		18		20		25		30	ns

Switching Characteristics Over the Operating Range[7,8] (continued)

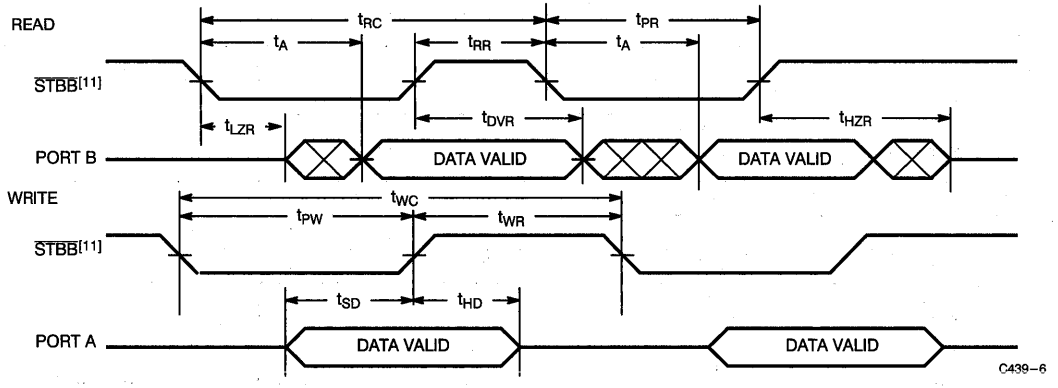
Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{TPD}[9,10]	$\overline{STBX}$ LOW to Data Valid		20		20		30		55	ns
t_{DL}	Transparent Propagation Delay		20		20		25		30	ns
t_{ESD}[9,10]	$\overline{STBX}$ LOW to High Z		18		20		25		30	ns
t_{EBD}[9,10]	$\overline{BYPX}$ LOW to High Z		18		20		25		30	ns
t_{EDS}	$\overline{STBX}$ HIGH to Low Z		18		20		25		30	ns
t_{EDB}	$\overline{BYPX}$ HIGH to Low Z		18		20		25		30	ns
t_{BPW}	$\overline{BYPX}$ Pulse Width (Trans.)	25		30		40		65		ns
t_{TSP}	$\overline{STBX}$ Pulse Width (Trans.)	20		20		30		55		ns
t_{BLZ}[9,10]	$\overline{BYPX}$ LOW to Low Z (Read)	10		10		10		10		ns
t_{BDV}	$\overline{BYPX}$ HIGH to Data Invalid (Read)	3		3		3		3		ns
t_{WHF}	$\overline{STBX}$ LOW to $\overline{HF}$ LOW (Write)		35		40		50		80	ns
t_{RHF}	$\overline{STBX}$ HIGH to $\overline{HF}$ HIGH (Read)		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{E/F}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{E/F}$ HIGH	25		30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	15		18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		0		10		ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance as in part (a) of AC Test Loads, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{DVR}, t_{BDV}, t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, t_{TSD}, t_{LZR}, t_{HWZ}, and t_{BLZ} use capacitance loading as in part (b) of AC Test Loads.
10. t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, and t_{TSD} transition is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}. t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR}, t_{HWZ}, and t_{BLZ} transition is measured at ±100 mV from the steady state.

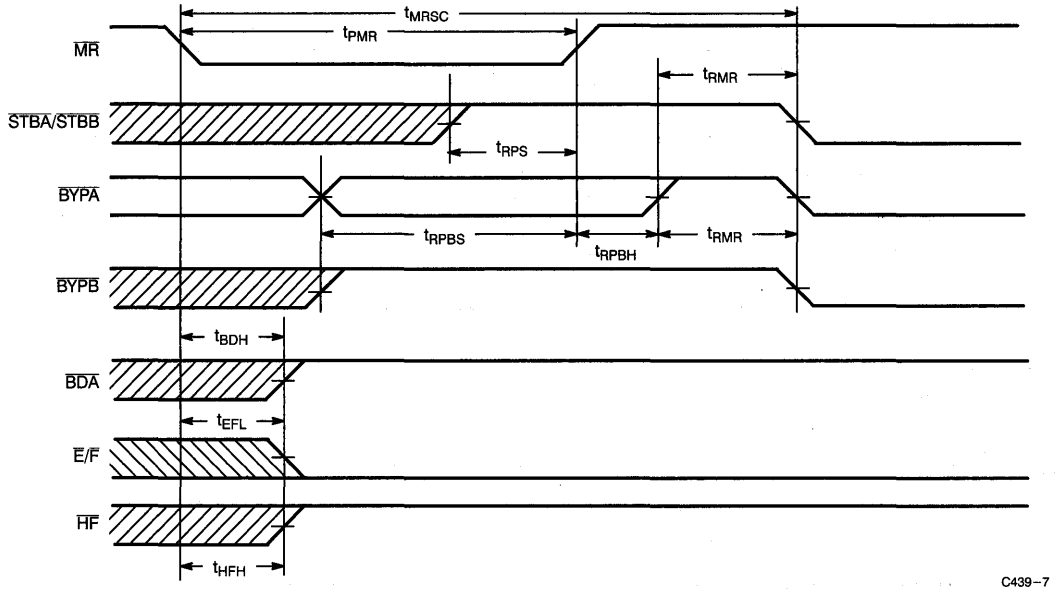
Switching Waveforms

Asynchronous Read and Write Timing Diagram

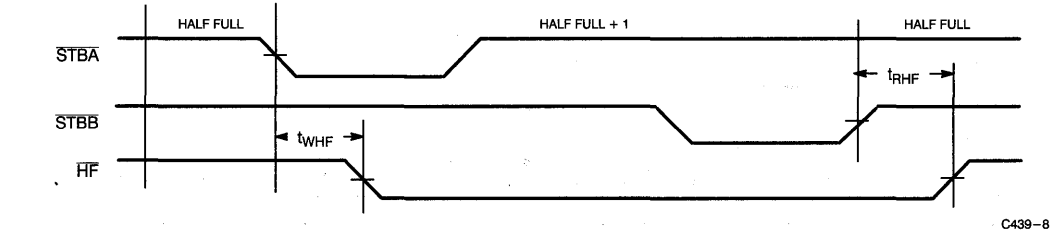


Switching Waveforms (continued)

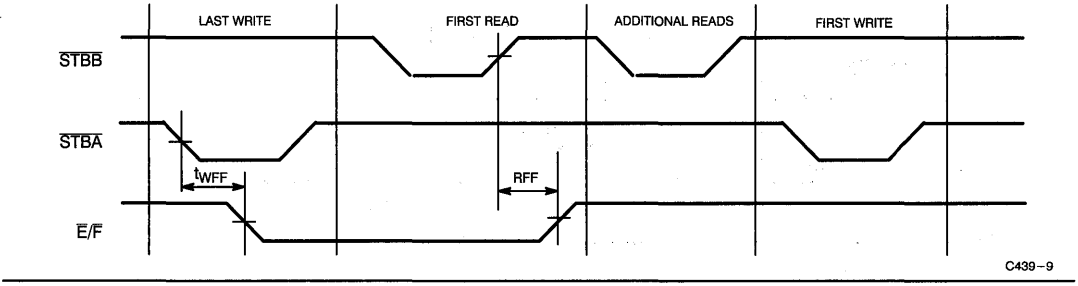
Master Reset Timing Diagram



Half-Full Flag Timing Diagram[12]



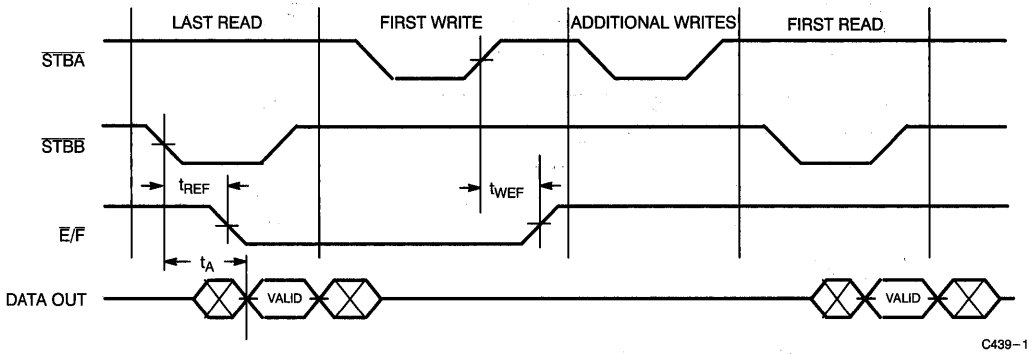
Last Write to First Read Empty/Full Flag Timing Diagram[12]



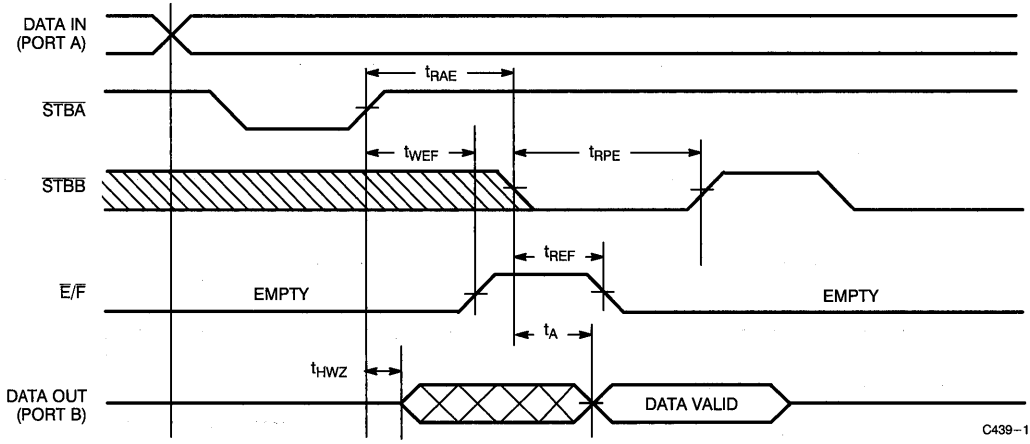
Notes:
11. Direction selected Port A to Port B.
12. Direction selected as A to B.

Switching Waveforms (continued)

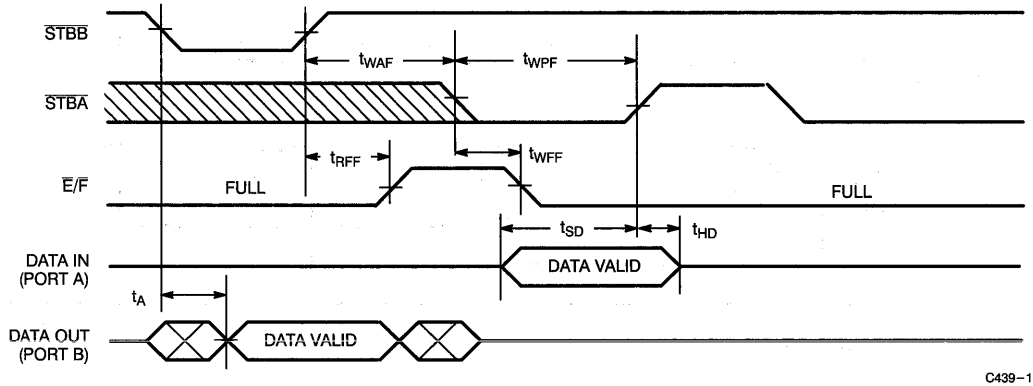
Last Read to First Write Empty/Full Flag Timing Diagram[12]



Empty/Full Flag and Read Bubble-Through Mode Timing Diagram[12]

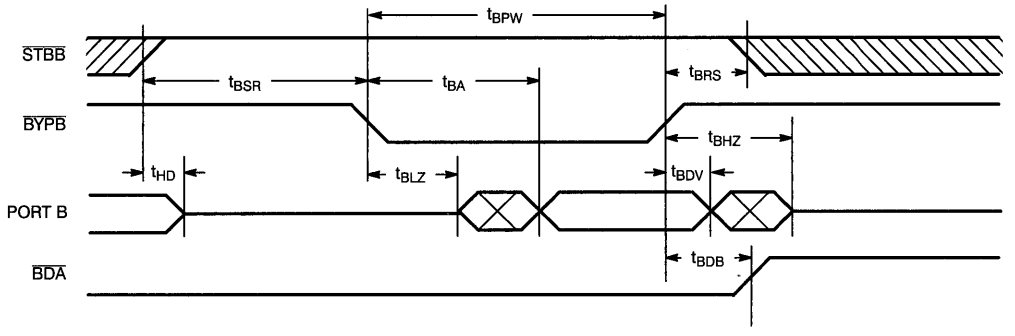


Empty/Full Flag and Write Bubble-Through Mode Timing Diagram[12]

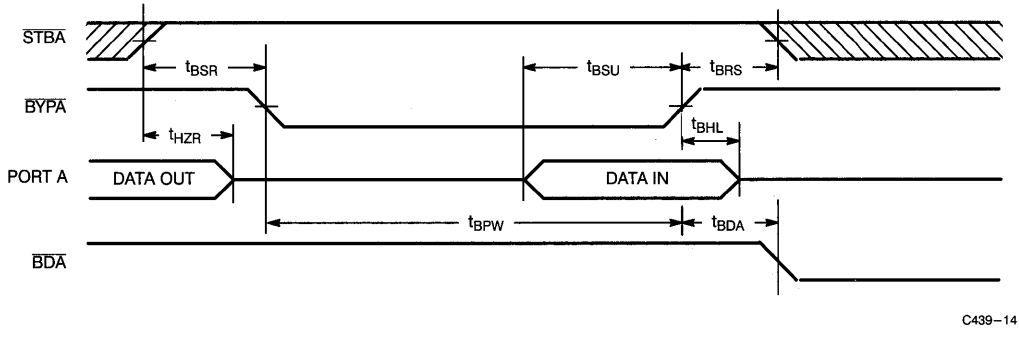


Switching Waveforms (continued)

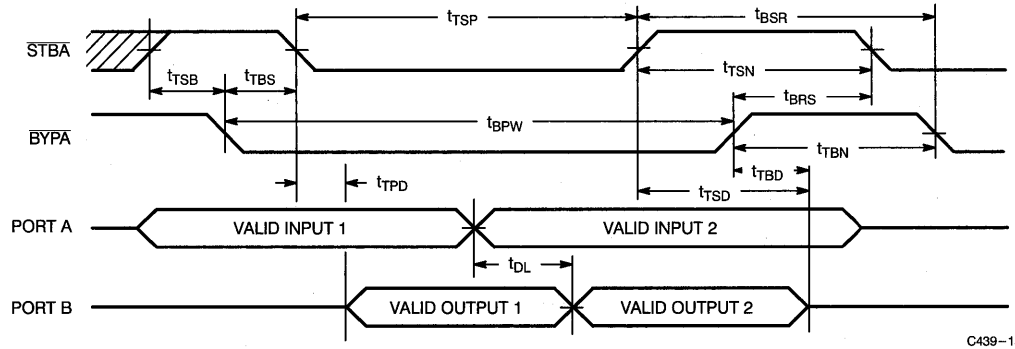
Registered Bypass Read Timing Diagram[13]



Registered Bypass Write Timing Diagram[14]



Transparent Bypass Read Timing Diagram[15]

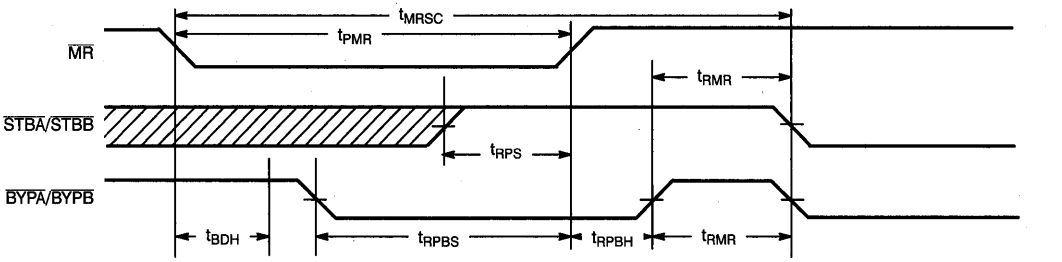


Notes:

13. Port B selected to read bypass register (FIFO direction Port B to Port A).
14. Port A selected to write bypass register (FIFO direction Port B to Port A.
15. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

Switching Waveforms (continued)

Test Mode Timing Diagram



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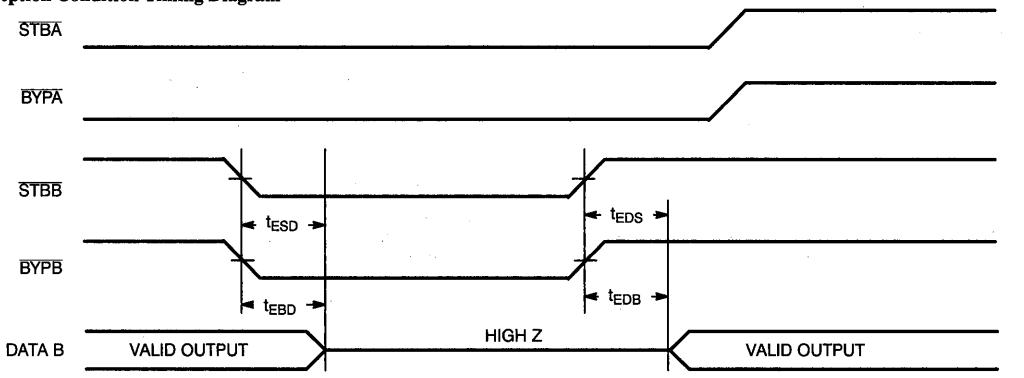
Exception Condition Timing Diagram[15]



C439–17

Architecture

The CY7C439 consists of a 2048 by 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals ($\overline{STBA}$, $\overline{STBB}$, $\overline{BYPA}$, $\overline{BYPB}$, $\overline{MR}$), and flags ($\overline{E}/\overline{F}$, $\overline{HF}$, $\overline{BDA}$).

Operation at Power-On

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. During an $\overline{MR}$ cycle, the user can initialize the device by choosing the direction of FIFO operation (see *Table 1*). There is a minimum LOW period for $\overline{MR}$, but no maximum time. The state of $\overline{BYPA}$ is latched internally by the rising edge of $\overline{MR}$ and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the reset condition (see *Table 1*), the FIFO three-states the data ports, sets $\overline{BDA}$ and $\overline{HF}$ HIGH, $\overline{E}/\overline{F}$ LOW, and ignores the state of $\overline{BYPA}/B$ and $\overline{STBA}/B$. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving $\overline{BYPA}$ HIGH or LOW, and $\overline{BYPB}$, $\overline{STBA}$, and $\overline{STBB}$ HIGH. If $\overline{BYPA}$ is LOW (selecting direction B>A), the FIFO will then remain in a reset condition until the user terminates the reset operstion by driving $\overline{BYPA}$ HIGH. If $\overline{BYPA}$ is HIGH (selecting direction A>B), the reset condition terminates after the rising edge of $\overline{MR}$. The entire reset phase can be accomplished in one cycle time of t_{RC}.

FIFO Operation

The operation of the FIFO requires only one control pin per port ($\overline{STBX}$). The user determines the direction of the FIFO data flow by initiating an $\overline{MR}$ cycle (see *Table 1*), which clears the FIFO and bypass register and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another $\overline{MR}$ cycle. Data is written into the FIFO on the rising edge of the input, $\overline{STBX}$, and read from the FIFO by a low level at the output, $\overline{STBX}$. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a bubble-through read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter if the read strobe ($\overline{STBX}$) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at which time the bubble-through write is performed if the write strobe ($\overline{STBX}$) is still LOW.

Registered Bypass Operation

The registered bypass feature provides a means of transferring one 9-bit word of data in the opposite direction to normal data flow without affecting either the FIFO contents or the FIFO write operations at the other port. The bypass register is configured during reset to provide a data path in the opposite direction to that of the FIFO (see *Table 1*). For example, if port A is writing data to the FIFO (hence port B is reading data from the FIFO) then $\overline{BYPB}$ is used to write to the bypass register at port B, and $\overline{BYPA}$ is used to read a single word from the bypass register at port A. The bypass data available flag ($\overline{BDA}$) is generated to notify port A that bypass data is available. $\overline{BDA}$ goes true on the trailing edge of the $\overline{BYPX}$ write operation and false upon the trailing edge of the $\overline{BYPX}$ read operation.

Data is written on the rising edge of $\overline{BYPX}$ into the bypass register for later retrieval by the other port, regardless of the state of $\overline{BDA}$. The bypass register is read by a low level at $\overline{BYPX}$, regardless of the state of $\overline{BDA}$.

Transparent Bypass Operation

The transparent bypass feature provides a means of sending immediate data "around" the FIFO in either direction. The FIFO contents are not affected by the use of transparent bypass, but the control signals for transparent bypass are shared with those of the normal FIFO operation. Hence there are limitations on the use of transparent bypass to ensure that data integrity and ease of use are preserved. The port wishing to send immediate data must ensure that the other port will not attempt a FIFO read or write during the transparent bypass cycle. If this is not possible, registered bypass or external circuitry should be used.

Transparent bypass mode is initiated by bringing both $\overline{BYPA}$ and $\overline{STBA}$ LOW together. Care should be taken to observe the following constraints on the timing relationships. Since $\overline{STBA}$ is used for normal FIFO operations, it must follow $\overline{BYPA}$ falling edge by t_{TBS} to prevent erroneous FIFO read or write operations. Since $\overline{BYPA}$ is used alone to initiate registered bypass read and write, it is internally delayed before initiating registered bypass. If $\overline{STBA}$ falls during this time, delay registered bypass is averted, and transparent bypass is initiated. Identical arguments apply to $\overline{BYPB}$ and $\overline{STBB}$.

If a transparent bypass sequence is successfully accomplished, data presented to the initiating port (port A in the above discussion) will be buffered to the other (port B) after t_{DL}. Either port can initiate a transparent bypass operation at any time, but if the control signals ($\overline{STBA}$/B, $\overline{BYPA}$/B) are in conflict (exception condition), internal circuitry will switch both ports to high-impedance until the conflict is resolved.

Test Mode Operation

The Test mode feature provides a means of reading the FIFO contents from the same port that the data was written to the FIFO. This feature is useful for Built-In Self Test (BIST) and diagnostic functions. To utilize this capability, initialize FIFO direction A to B and load data into the FIFO using normal write timing. In order to read data back out of the same port (port A), initiate a $\overline{MR}$ cycle with both $\overline{BYPA}$ and $\overline{BYPB}$ LOW (see Test Mode Timing diagram). After completing the cycle, the data can be read out of port A in FIFO order. Data will be inverted when read out of the device. Also, flags are not valid when reading data.

Flag Operation

There are two flags, Empty/Full ($\overline{E}/\overline{F}$) and Half Full ($\overline{HF}$), which are used to decode four FIFO states (see *Table 4*). The states are empty, 1–1024 locations full, 1025–2047 locations full, and full. Note that two conditions cause the $\overline{E}/\overline{F}$ pin to go LOW, Empty and Full, hence both flag pins must be used to resolve the two conditions.

Table 1. FIFO Direction Select Truth Table

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal Operation
⌐¬	1	1	1	1	FIFO Direction A to B, Registered Bypass Direction B to A
⌐¬	0	1	1	1	FIFO Direction B to A, Registered Bypass Direction A to B
0	X	X	X	X	Reset Condition

Table 2. Bypass Operation Truth Table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A⇸B	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at A, Read at B
A⇸B	1	⌐¬	⌐¬	1	Normal FIFO Read at B, Bypass Register Read at A
A⇸B	⌐¬	1	1	⌐¬	Normal FIFO Write at A, Bypass Register Write at B
B⇸A	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at B, Read at A
B⇸A	1	⌐¬	⌐¬	1	Normal FIFO Write at B, Bypass Register Write at A
B⇸A	⌐¬	1	1	⌐¬	Normal FIFO Read at A, Bypass Register Read at B
X	0	0	1	1	No FIFO Operations, Transparent Data A to B
X	1	1	0	0	No FIFO Operations, Transparent Data B to A

Table 3. Exception Conditions: Operation Not Defined

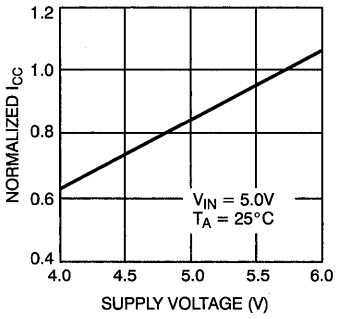
Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYBP}$	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

Table 4. Flag Truth Table

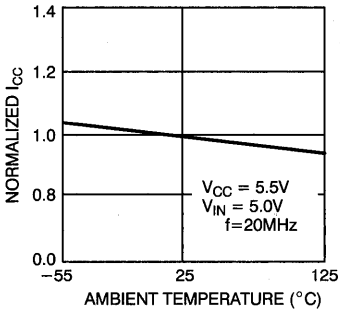
$\overline{E}/\overline{F}$	$\overline{HF}$	State
0	1	Empty
1	1	1–1024 Locations Full
1	0	1025–2047 Locations Full
0	0	Full

Typical DC and AC Characteristics

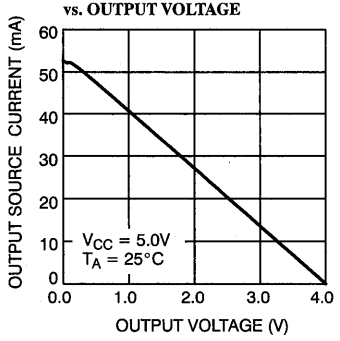
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



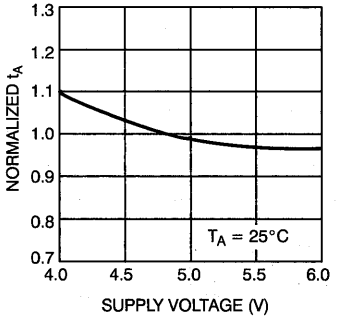
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



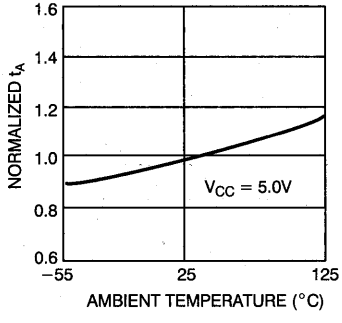
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



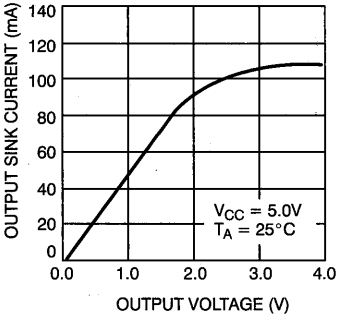
NORMALIZED t_A vs. SUPPLY VOLTAGE



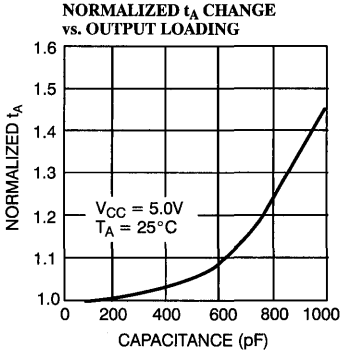
NORMALIZED t_A vs. AMBIENT TEMPERATURE

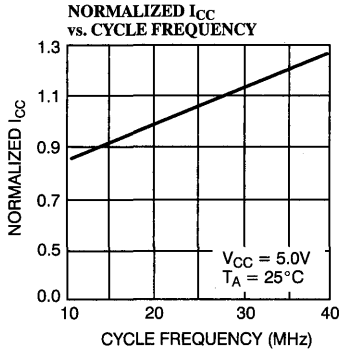


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)





Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C439–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C439–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C439–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C439–25DC	D22	28-Lead (300-Mil) CerDIP	
30	CY7C439–30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C439–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C439–30VC	V21	28-Lead (300-Mil) Molded SO	
	CY7C439–30DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C439–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C439–40PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C439–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C439–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C439–40DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C439–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C439–65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C439–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C439–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C439–65DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C439–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPS}	9, 10, 11
t_{RPBS}	9, 10, 11
t_{RPBH}	9, 10, 11
t_{BDH}	9, 10, 11
t_{BSR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{BRS}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{BSU}	9, 10, 11
t_{BHL}	9, 10, 11
t_{BDA}	9, 10, 11
t_{BDB}	9, 10, 11
t_{BA}	9, 10, 11
t_{BHZ}	9, 10, 11
t_{TSB}	9, 10, 11
t_{TBS}	9, 10, 11
t_{TSN}	9, 10, 11
t_{TSD}	9, 10, 11
t_{TBN}	9, 10, 11
t_{TBD}	9, 10, 11
t_{TPD}	9, 10, 11
t_{DL}	9, 10, 11
t_{ESD}	9, 10, 11
t_{EBD}	9, 10, 11
t_{EDS}	9, 10, 11
t_{EDB}	9, 10, 11
t_{BPW}	9, 10, 11
t_{TSP}	9, 10, 11
t_{BLZ}	9, 10, 11
t_{BDV}	9, 10, 11

Document #: 38−00126−C

CY7C441
CY7C443

CYPRESS SEMICONDUCTOR

Clocked 512 x 9, 2K x 9 FIFOs

Features

- **512 x 9 (CY7C441) and 2,048 x 9 (CY7C443) FIFO buffer memory**
- **High-speed 70-MHz operation**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, and Almost Full status flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Width expandable**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 28-pin DIP, PLCC, LCC, and SOJ packages**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**
- **Low power – I_{CC}=70 mA**

Functional Description

The CY7C441 and CY7C443 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C441 has a 512 word by 9 bit memory array, while the CY7C443 has a 2048 word by 9 bit memory array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

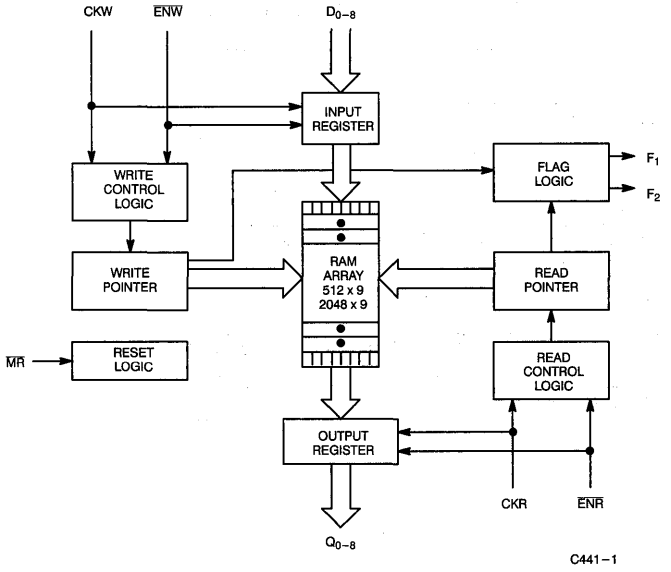
Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable.

The CY7C441 and CY7C443 clocked FIFOs provide two status flag pins (F1 and F2). These flags are decoded to determine one of four states: Empty, Almost Empty, Intermediate, and Almost Full (*Table 1*). The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). The Empty and Almost Empty states are updated exclusively by the CKR while Almost Full is updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C441 and the CY7C443 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

5 FIFOs

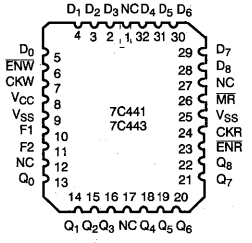
Logic Block Diagram



C441–1

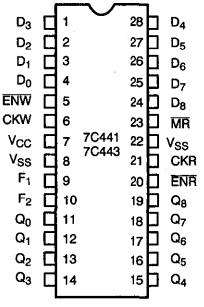
Pin Configurations

PLCC/LCC
Top View



C441–2

DIP/SOJ
Top View



C441–34

Selection Guide

		7C441–14 7C443–14	7C441–20 7C443–20	7C441–30 7C443–30
Maximum Frequency (MHz)		71.4	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: when the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_0 – D_8) into the FIFO's memory
Q_{0-8}	O	Data Outputs: when the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_0 – Q_8) out of the FIFO's memory
$\overline{ENW}$	I	Enable Write: enables the CKW input
$\overline{ENR}$	I	Enable Read: enables the CKR input
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW and updates the Almost Full flag state
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW and updates the Almost Empty and Empty flag states
F1	O	Flag 1: is used in conjunction with Flag 2 to decode which state the FIFO is in (see *Table 1*)
F2	O	Flag 2: is used in conjunction with Flag 1 to decode which state the FIFO is in (see *Table 1*)
$\overline{MR}$	I	Master Reset: resets the device to an empty condition

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

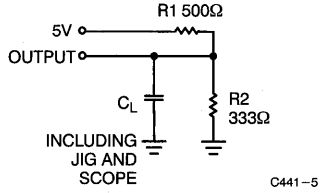
Parameter	Description	Test Conditions		7C441–14 7C443–14 Min.	7C441–14 7C443–14 Max.	7C441–20 7C443–20 Min.	7C441–20 7C443–20 Max.	7C441–30 7C443–30 Min.	7C441–30 7C443–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	µA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		– 90		– 90		– 90		mA
I_{CC1}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[6]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

Capacitance[7]

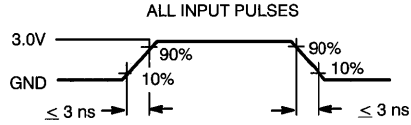
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time and do not test any output for more than one second.
4. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
5. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
6. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveform[8,9]

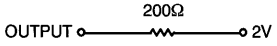


C441–5



C441–6

Equivalent to: THÉVENIN EQUIVALENT



5 FIFOs

Switching Characteristics Over the Operating Range[2,10]

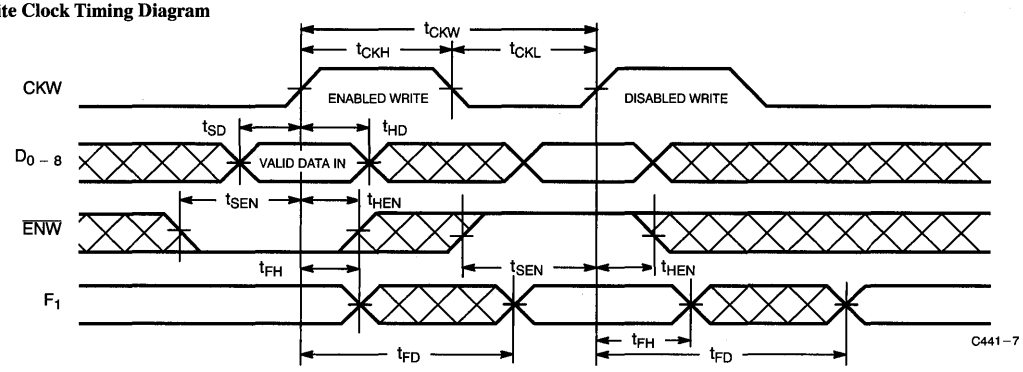
Parameter	Description	7C441–14 7C443–14		7C441–20 7C443–20		7C441–30 7C443–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[11]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[12]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[13]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns

Notes:

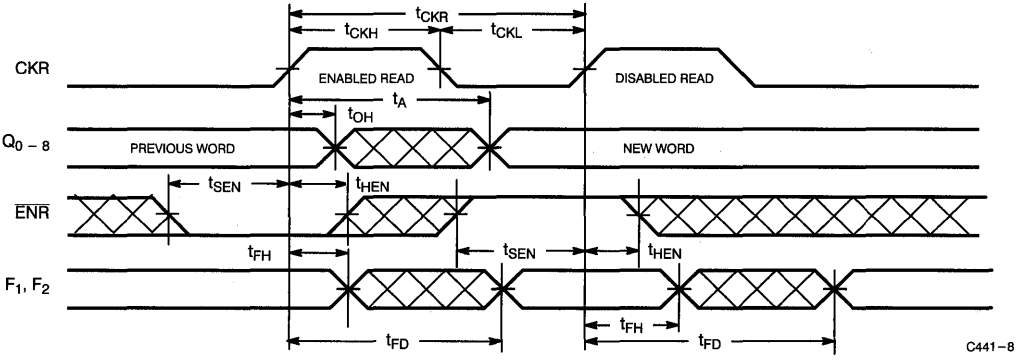
8. C_L = 30 pF for all AC parameters.
9. All AC measurements are referenced to 1.5V.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in the AC Test Loads and Waveforms and capacitance as in note 6, unless otherwise specified.
11. Access time includes all data outputs switching simultaneously.
12. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.
13. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is abritrary. See Note 12 for definition of clock and opposite clock.

Switching Waveforms

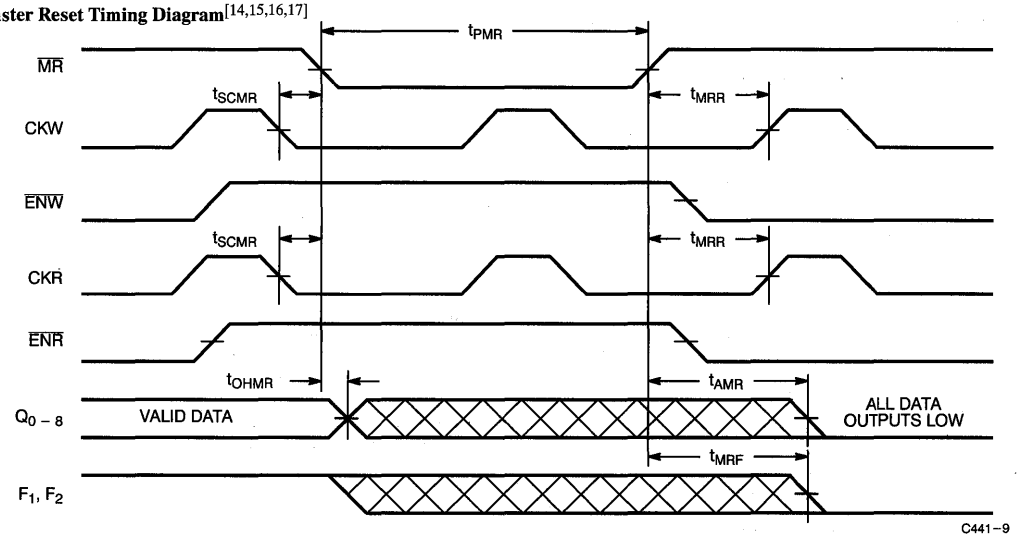
Write Clock Timing Diagram



Read Clock Timing Diagram



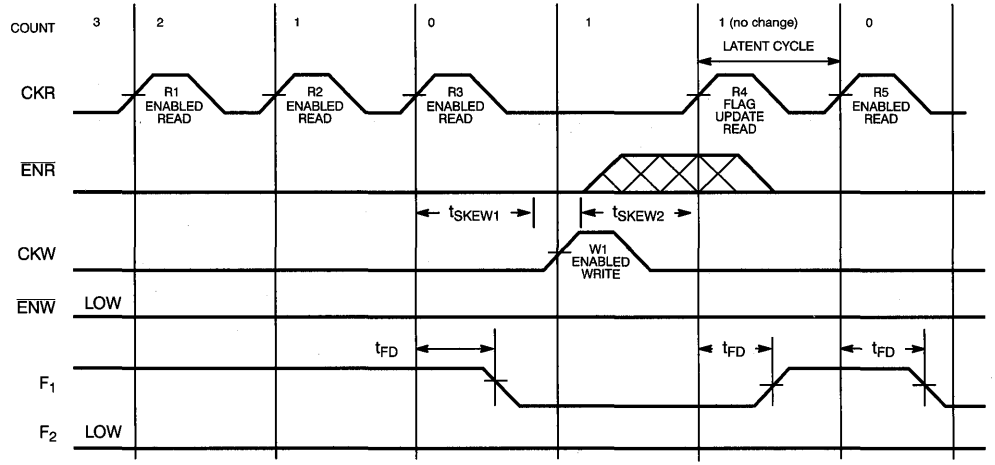
Master Reset Timing Diagram[14,15,16,17]



5 FIFOs

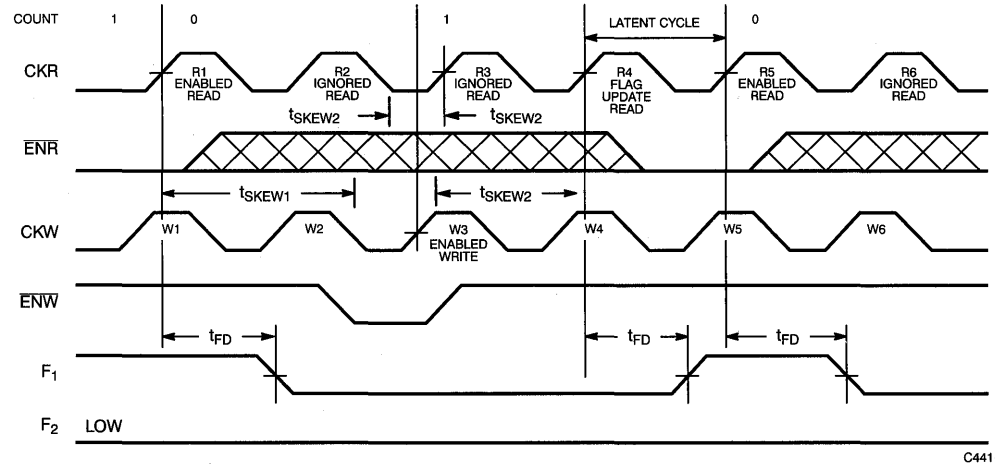
Switching Waveforms (continued)

Read to Empty Timing Diagram[18,20,21]



C441-11

Read to Empty Timing Diagram with Free-Running Clocks[18,19,20]



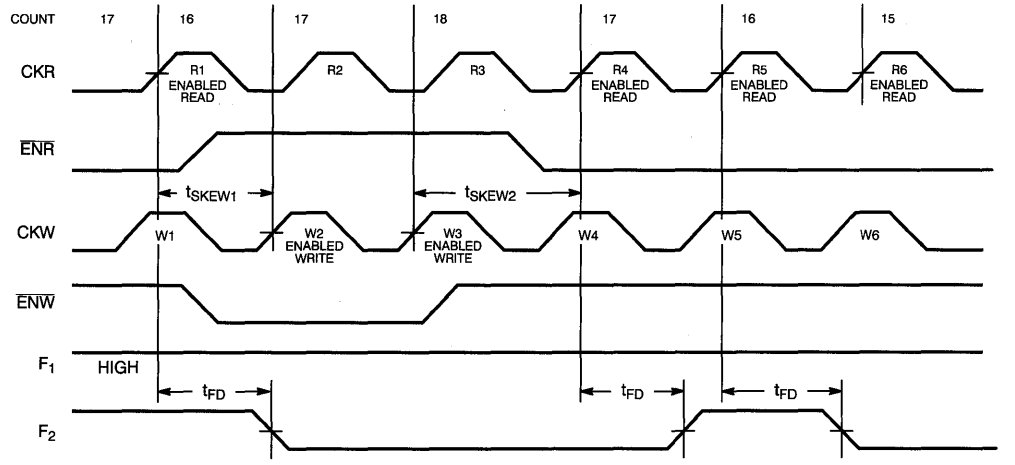
C441-10

Notes:

14. $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
15. $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
16. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$.
17. In this example, Q_{0-8} will remain valid until t_{OHMR} if the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
18. "Count" is the number of words in the FIFO.
19. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
20. CKR is clock and CKW is opposite clock.
21. R3 updates the flags to the Empty state by bringing F1 LOW. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and therefore updates the FIFO to the Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status, regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

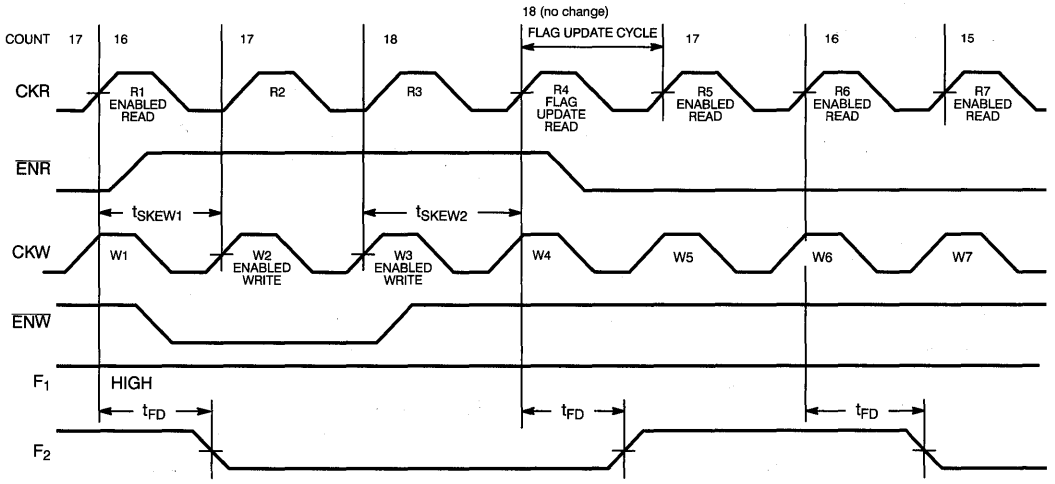
Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[18,20]



C441–12

Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[18,20,22,23]



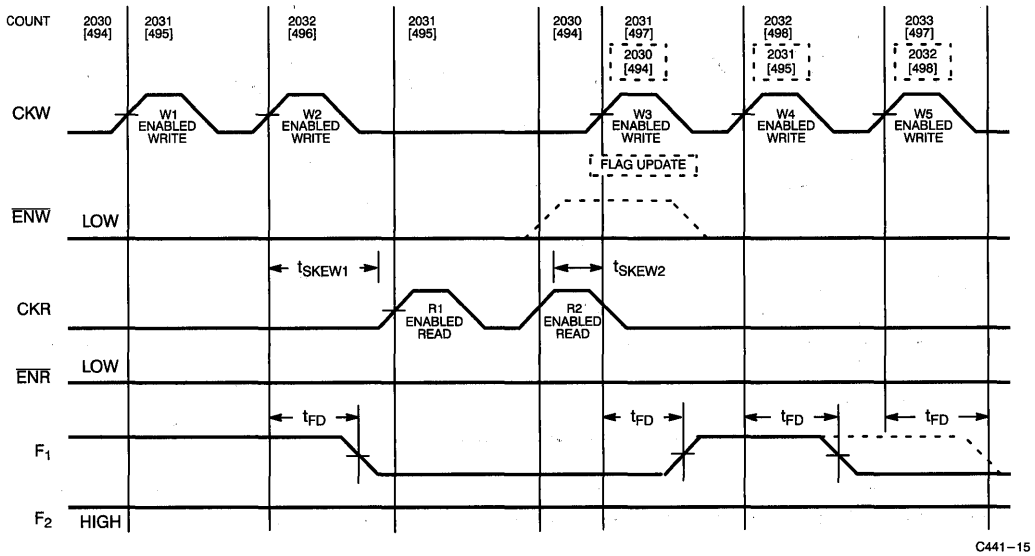
C441–13

Notes:

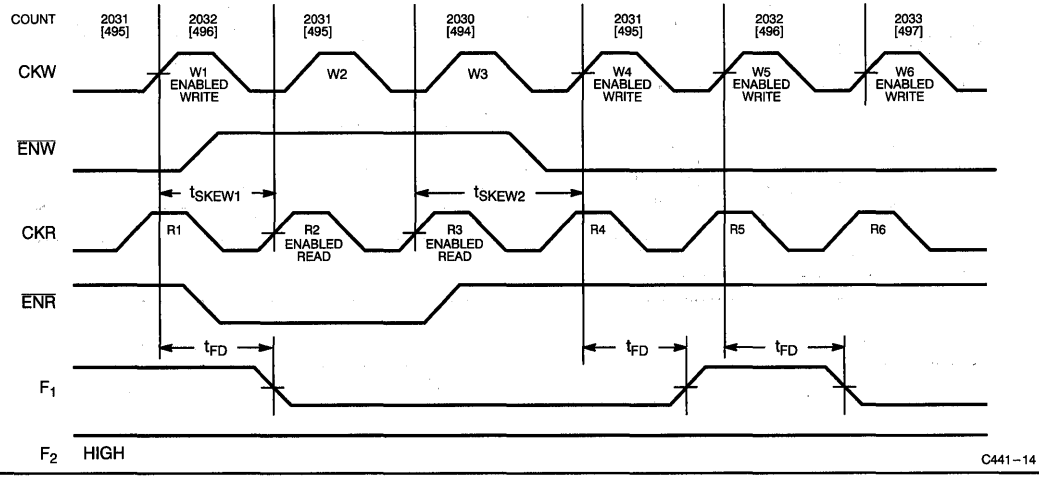
22. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
23. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ▸ 18; two enabled writes: W2, W3) before a read (R4) can update flags to the Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram[18,24,25,26,27]



Write to Almost Full Timing Diagram with Free-Running Clocks[18,24,25]

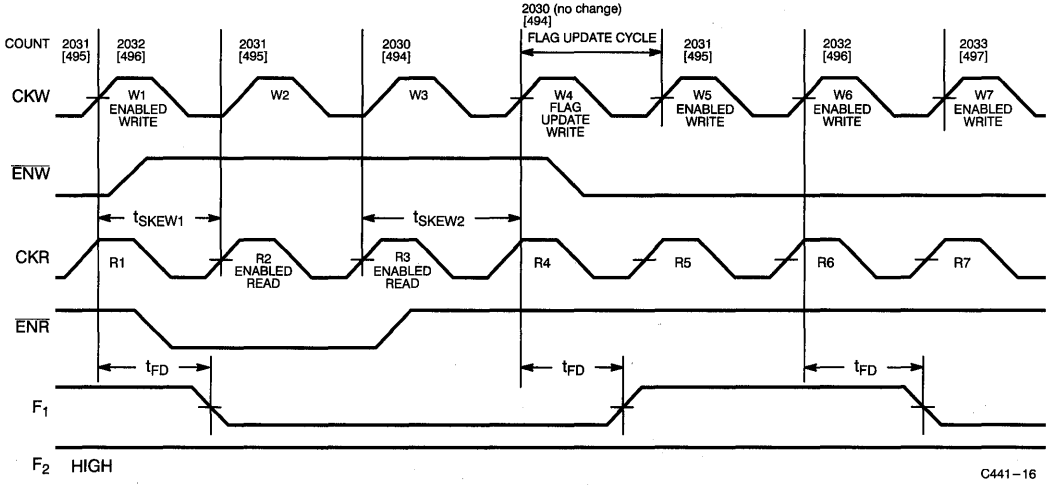


Notes:

24. CKW is clock and CKR is opposite clock.
25. Count = 2032 indicates Almost Full for CY7C443 and count = 496 indicates Almost Full for CY7C441. Values for the CY7C441 count are shown in brackets.
26. The dashed lines show W3 as flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.
27. W2 updates the flags to the Almost Full state by bringing F1 LOW. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
28. When making the transition from Almost Full to Intermediate, the count must decrease by two (2032 ◗ 2030; two enabled reads: R2, R3) before a write (W4) can update flags to Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clock[18,24,25,28]



Architecture

The CY7C441/443 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$), and flags (F1, F2).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by both flags F1 and F2 being LOW. All data outputs (Q_{0-8}) go LOW at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. F_1 and F_2 are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read duration. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Flag Operation

The CY7C441/3 provide two flags, F1 and F2, which are used to decode four FIFO states (see *Table 1*). All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate; see *Figure 1*). The synchronous architecture guarantees some minimum valid time for the flags.

The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the F1 and F2 pins to output a state signifying the Empty condition. The Almost Full flag is updated exclusively by the write clock (CKW). For example, if the CY7C443 FIFO contains 2031 words (2032 words or greater indicates Almost Full in the CY7C443), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the F1 and F2 pins to output the Almost Full state.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the Almost Full flag is only updated by the CKW, careful attention must be given to the flag operation. The user must be aware that if a flag boundary (Empty, Almost Empty, and Almost Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKR does not effect Almost Full), a flag update is necessary to represent the FIFO's new state. This signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for the Almost Full flag).

Table 1. Flag Truth Table

F1	F2	State	CY7C441 Number of Words in FIFO	CY7C443 Number of Words in FIFO
0	0	Empty	0	0
1	0	Almost Empty	1 – 16	1 – 16
1	1	Intermediate Range	17 – 495	17 – 2031
0	1	Almost Full or Full	496 – 512	2032 – 2048

5 FIFOs

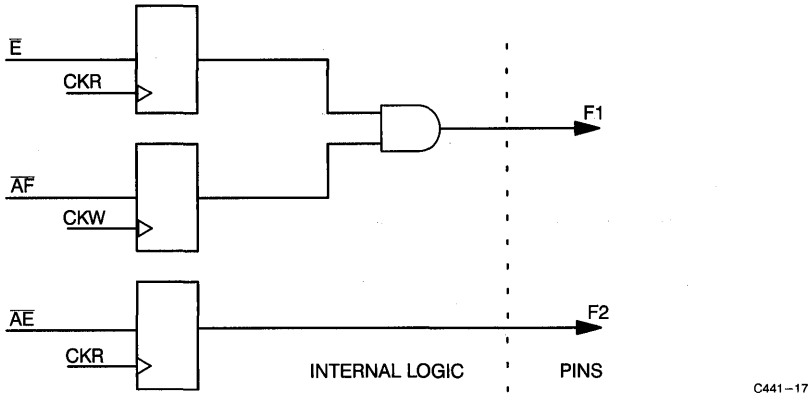


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Until the flag update cycle is executed, the synchronous flags do not show the true state of the FIFO. For example, if 2,040 writes are performed to an empty CY7C443 without a single read, F1 and F2 will still exhibit an Empty flag. This is because F2 is exclusively updated by the CKR, therefore, a single read (flag update cycle) is necessary to update flags to Almost Full state. It should be noted that this flag update read does not require $\overline{ENR}$ = LOW, so a free-running read clock will initiate the flag update cycle.

When updating the flags, the CY7C441/443 decide whether or not the opposite clock was recognized when a clock updates the flag. For example, if a write occurs at least t_{SKEW1} after a read when updating the Empty flag, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates the flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Almost Full) is different from that used to update the boundary flag (Empty). Both operations are described below.

Boundary Flag (Empty)

The Empty flag is synchronized to the CKR signal. The Empty flag can only be updated by a clock pulse on the CKR pin. An empty FIFO that is written to will be described with an Empty flag state until a clock pulse is presented on the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Intermediate or Empty to Almost Full), a clock cycle on the CKR is necessary to update the flags to the current state. Such a state (flags displaying empty even though data has been written to the FIFO) would require two read cycles to read data out of FIFO. The first read serves only to update the flags to the Almost Empty, Intermediate, or Almost Full state, and the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flags are updated regardless of the $\overline{ENR}$ state. Therefore the update occurs even when $\overline{ENR}$ is deasserted (HIGH) so that a valid read is not necessary to update the flags to correctly describe the FIFO. With a free-running clock connected to CKR, the flag updates with each cycle. *Table 2* shows sample operations that update the Empty flag.

Although a Full flag is not supplied externally on the CY7C441/CY7C443, a Full flag exists internally. The operation of the FIFO at the Full boundary is analogous to its operation at the Empty boundary. See the text section "Boundary Flags (Full)" in the CY7C451/CY7C453 datasheet.

Non-Boundary Flags (Almost Empty, Almost Full)

The flag status pins, F_1 and F_2, exhibit the Almost Empty status when both the CY7C441 and the CY7C443 contain 16 words or less. The Almost Full Flag becomes active when the FIFO contains 16 or less empty locations. The CY7C441 becomes Almost Full when it contains 496 words. The CY7C443 becomes Almost Full when it contains 2032 words. The Almost Empty flag (like the Empty flag) is synchronous to the CKR signal, whereas the Almost Full flag is synchronous to the CKW signal. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO state. For example, if the FIFO just reaches the Almost Empty state (16 words) and then two words are written, a read clock (CKR) will be required to update the flags to the Intermediate state. However, unlike the boundary (Empty) flag's update cycle, the state of the enable pin ($\overline{ENR}$ in this case) affects the operation. Therefore, ENR set-up (t_{SEN}) and hold (t_{HEN}) times must be met. If $\overline{ENR}$ is asserted ($\overline{ENR}$=LOW) during the latent cycle, the count and data update in addition to F1 and F2. If $\overline{ENR}$ is not active ($\overline{ENR}$=1) during the flag update cycle, only the flag is updated.

The same principles apply for updating the flags when a transition from the Almost Full to the Intermediate state occurs. If the CY7C443 just reaches the Almost Full state (2032 words) and then two words are read, a write clock (CKW) will be required to update the flag to the Intermediate state. If $\overline{ENW}$ is LOW during the flag update cycle, the count and data update in addition to the flags. If $\overline{ENW}$ is HIGH, only the flag is updated. Therefore, $\overline{ENW}$ set-up (t_{SEN}) and hold (t_{HEN}) times must be met. *Tables 3* and *4* show examples for a sequence of operations that affect the Almost Empty and Almost Full flags, respectively.

Width Expansion

The CY7C441/3 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode, all control inputs are common. When the FIFO is being read near

the Empty boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty condition on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width expanded devices (A and B), device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). The first write occurs because a read within t_{SKEW2} of the first write is only guaranteed to be either recognized or ignored, but which of the two is not guaranteed. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to outpout "staggered" data assuming more data has been written to the FIFOs.

In the width expansion configuration, any of the devices' flags may be monitored for the composite Almost Full status.

Table 2. Empty Flag Operation Example [29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Write ($\overline{ENW}$ = LOW)	Empty	0	0	2	Write
Empty	0	0	2	Read ($\overline{ENR}$ = HIGH)	AE	1	0	2	Flag Update
AE	1	0	2	Read ($\overline{ENR}$ = LOW)	AE	1	0	1	Read
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition for Almost Empty to Empty)
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	Flag Update
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition from Almost Empty to Empty)

Table 3. Almost Empty Flag Operation Example[29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
AE	1	0	16	Write ($\overline{ENW}$ = LOW)	AE	1	0	17	Write
AE	1	0	17	Write ($\overline{ENW}$ = LOW)	AE	1	0	18	Write
AE	1	0	18	Read ($\overline{ENR}$ = LOW)	Intermediate	1	1	17	Flag Update and Read
Intermediate	1	1	17	Read ($\overline{ENR}$ = LOW)	AE	1	0	16	Read (Transition from Intermediate to Almost Empty)
AE	1	0	16	Read ($\overline{ENR}$ = HIGH)	AE	1	0	16	Ignored Read

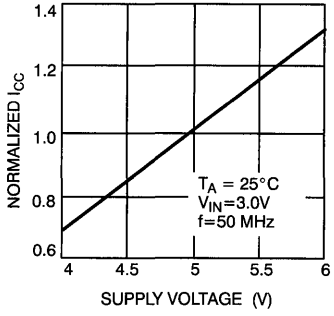
Table 4. Almost Full Flag Operation Example[30,31]

Status Before Operation							Status After Operation				
Current State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Comments
AF	0	1	496	2032	Read ($\overline{ENR}$=LOW)	AF	0	1	495	2031	Read
AF	0	1	495	2031	Read ($\overline{ENR}$=LOW)	AF	0	1	494	2030	Read
AF	0	1	494	2030	Write ($\overline{ENW}$=HIGH)	Intermediate	1	1	494	2030	Flag Update
Intermediate	1	1	494	2030	Write ($\overline{ENW}$=LOW)	Intermediate	1	1	495	2031	Write
Intermediate	1	1	495	2031	Write ($\overline{ENW}$=LOW)	AF	0	1	496	2032	Write (Transition from Intermediate to Almost Full)

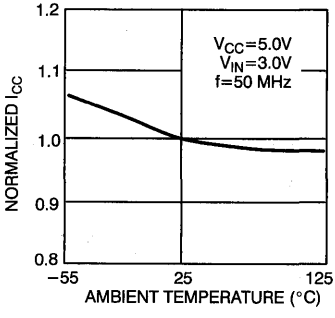
Notes:
29. Applies to both the CY7C441 and CY7C443 operations.
30. The CY7C441 Almost Full state is represented by 496 or more words.
31. The CY7C443 Almost Full state is represented by 2032 or more words.

Typical DC and AC Characteristics

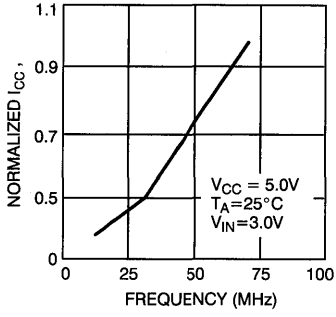
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



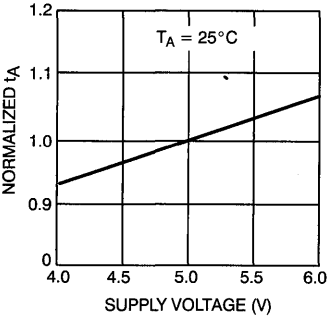
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



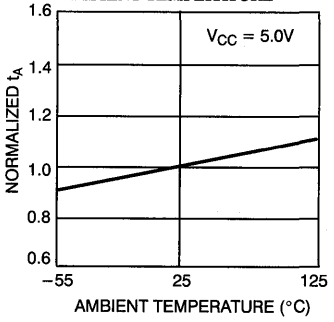
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



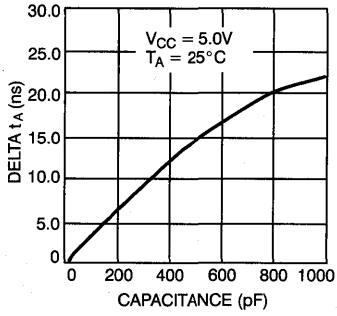
NORMALIZED t_A vs. SUPPLY VOLTAGE



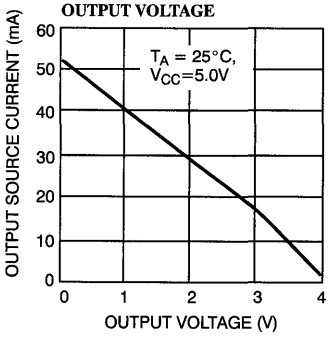
NORMALIZED t_A vs. AMBIENT TEMPERATURE



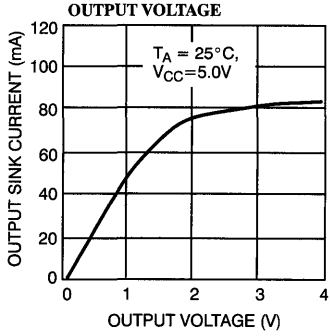
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



5 FIFOs

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C441-14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-14DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C441-14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C441-14KMB	K74	28-Lead Rectangular Cerpack	
20	CY7C441-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-20DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C441-20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C441-20KMB	K74	28-Lead Rectangular Cerpack	
30	CY7C441-30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441-30DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C441-30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441-30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C441-30KMB	K74	28-Lead Rectangular Cerpack	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C443-14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443-14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443-14DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C443-14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443-14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443-14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C443-14KMB	K74	28-Lead Rectangular Cerpack	
20	CY7C443-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443-20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443-20DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C443-20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443-20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C443-20KMB	K74	28-Lead Rectangular Cerpack	
30	CY7C443-30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443-30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443-30DC	D22	28-Lead (300-Mil) CerDIP	
	CY7C443-30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443-30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C443-30KMB	K74	28-Lead Rectangular Cerpack	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKR}	9, 10, 11
t_{CKW}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{HENR}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11

Document #: 38–00124–E

PRELIMINARY

CYPRESS SEMICONDUCTOR

Cascadable Clocked 512 x 18, 1K x 18, and 2K x 18 FIFOs with Programmable Flags

Features

- **512 x 18 (CY 7C445and CY7C455), 1,024 x 18 (CY7C446 and CY7C456), 2,048 x 18 (CY7C447 and CY7C457) FIFO buffer memory**
- **Expandable in width**
- **CY7C455, CY7C456, and CY7C457 expandable in depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$) pin on CY7C455, CY7C456, and CY7C457**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **52-pin PLCC (CY7C45X) or 48-pin 600-mil DIP (CY7C44X)**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**

Functional Description

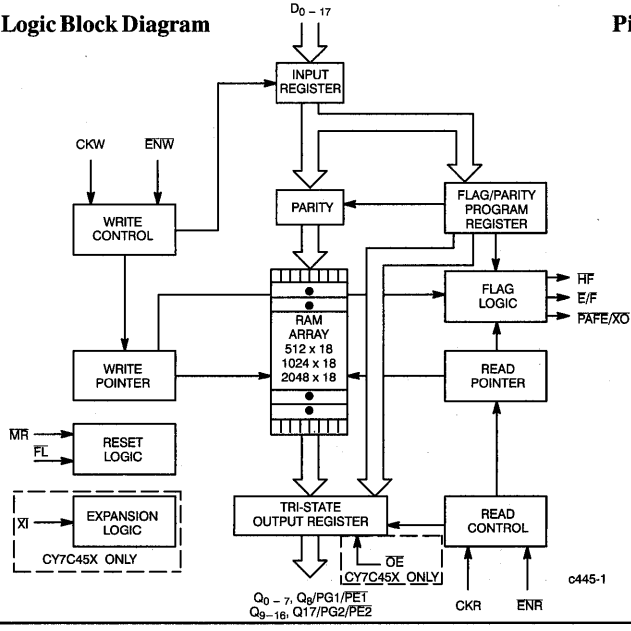
The CY7C445, CY7C446, CY7C447, CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C445 and CY7C455 have a 512-word memory array, the CY7C446 and CY7C456 have a 1,024-word memory array, and the CY7C447 and CY7C457 have a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$).

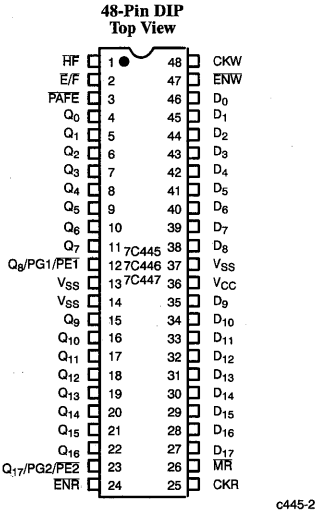
When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin ($\overline{OE}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are achievable in the standalone configuration, and up to 50 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$), cascade output ($\overline{XO}$), and First Load ($\overline{FL}$) pins. The $\overline{XO}$ pin is connected to the $\overline{XI}$ pin of the next device, and the $\overline{XO}$ pin of the last device should be connected to the $\overline{XI}$ pin of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS}.

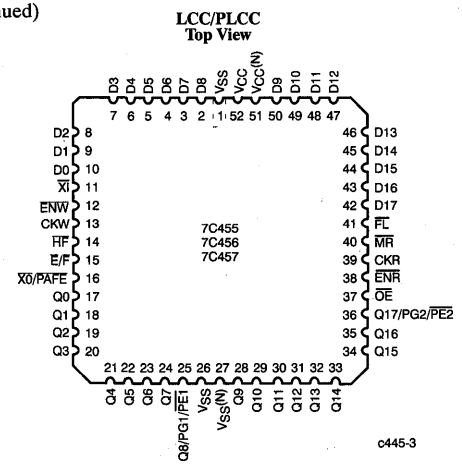
Logic Block Diagram



Pin Configurations



Pin Configurations (continued)



Functional Description (continued)

The CY7C445, CY7C446, CY7C447, CY7C455, CY7C456, and CY7C457 provide three status pins. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) shares the $\overline{XO}$ pin on the CY7C455, CY7C456, and CY7C457. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time. This time is typically equal to approximately one cycle time.

The CY7C44X and CY7C45X use center power and ground for reduced noise. All configurations are fabricated using an advanced 0.8µ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings and a substrate bias generator.

Selection Guide

		7C4XX–14	7C4XX–20	7C4XX–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadeable Frequency		N/A	50 (7C45X only)	33.3 (7C45X only)
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		5	7	9
Minimum Data or Enable Hold (ns)		1	1	1
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	160	140	120
	Military/Industrial	180	160	140

	CY7C445	CY7C446	CY7C447	CY7C455	CY7C456	CY7C457
Density	512 x 18	1,024 x 18	2,048 x 18	512 x 18	1,024 x 18	2,048 x 18
$\overline{OE}$, Depth Cascadable	No	No	No	Yes	Yes	Yes
Package	48-Pin DIP	48-Pin DIP	48-Pin DIP	52-Pin PLCC	52-Pin PLCC	52-Pin PLCC

Note:
1. 71.4-MHz operation is available only in the standalone configuration.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-17}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-17}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW, data is written into the FIFO's programming register. $D_{8,17}$ are ignored if the device is configured for parity generation.
Q_{0-7} Q_{9-16}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}, Q_{9-16}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR, data is read from the programming register.
Q_8/PG1/$\overline{PE1}$ Q_{17}/PG2/$\overline{PE2}$	O	Function varies according to mode: Parity disabled – same function as Q_{0-7} and Q_{9-16} Parity enabled, generation – parity generation bit (PG_x) Parity enabled, check – Parity Error Flag ($\overline{PE_x}$)
$\overline{ENW}$	I	Enable Write: Enables the CKW input (for both non-program and program modes).
$\overline{ENR}$	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag: Synchronized to CKW.
$\overline{E}/\overline{F}$	O	Empty or Full Flag: $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW.
$\overline{PAFE}/\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded – expansion out signal, connected to $\overline{XI}$ of next device.
$\overline{XI}$	I	Expansion-In Pin: Not Cascaded – $\overline{XI}$ is tied to V_{SS}. Cascaded – expansion Input, connected to $\overline{XO}$ of previous device.
$\overline{FL}$	I	First Load Pin: Cascaded – the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure 1*). Not Cascaded – tied to V_{CC}.
$\overline{MR}$	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of $\overline{CKW}$. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7}, Q_{9-16}, Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$ pins.

Note:
2. T_A is the "instant on" case temperature.

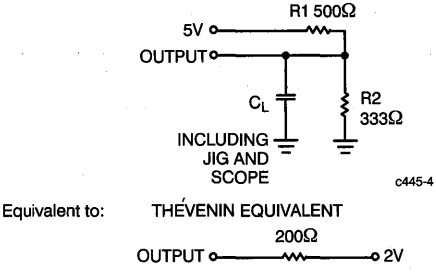
Electrical Characteristics Over the Operating Range[3]

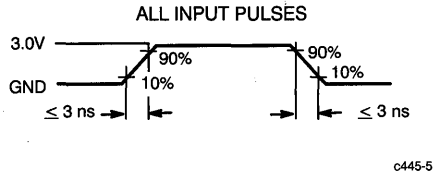
Parameter	Description	Test Conditions		7C44X–14 7C45X–14 Min.	7C44X–14 7C45X–14 Max.	7C44X–20 7C45X–20 Min.	7C44X–20 7C45X–20 Max.	7C44X–30 7C45X–30 Min.	7C44X–30 7C45X–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[4]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[4]	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		– 10	+10	– 10	+10	– 10	+10	μA
I_{OS}[5]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		– 90		– 90		– 90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		– 10	+ 10	– 10	+ 10	– 10	+ 10	μA
I_{CC}[6]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		160		140		120	mA
			Mil/Ind		180		160		140	mA

Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms[8, 9, 10, 11, 12]





Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
5. Test no more than one output at a time for not more than one second.
6. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
7. Tested initially and after any design or process changes that may affect these parameters.
8. C_L = 30 pF for all AC parameters except for t_{OHZ}.
9. C_L = 5 pF for t_{OHZ}.
10. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
11. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
12. t_{OHZ} is measured at +500 mV from V_{OL} and – 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[3, 13]

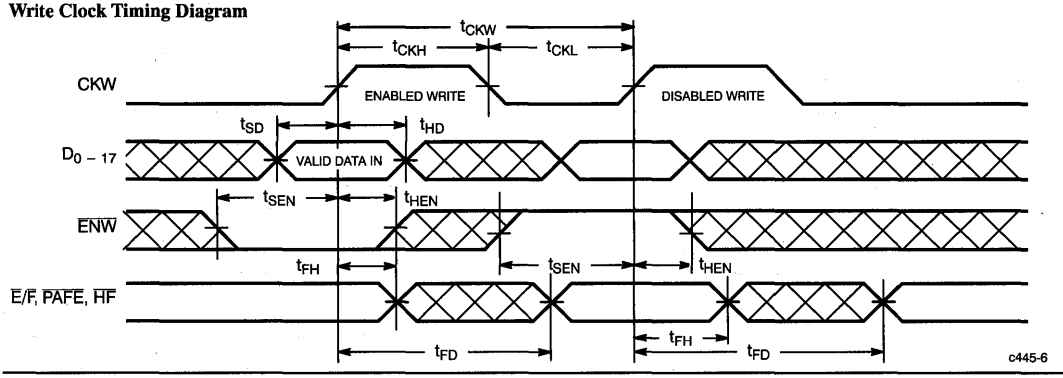
Parameter	Description	7C44X–14 7C45X–14		7C44X–20 7C45X–20		7C44X–30 7C45X–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	5		7		9		ns
t_{HD}	Data Hold	1		1		1		ns
t_{SEN}	Enable Set-Up	5		7		9		ns
t_{HEN}	Enable Hold	1		1		1		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[7, 14]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[7, 14]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[15]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[16]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		20		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

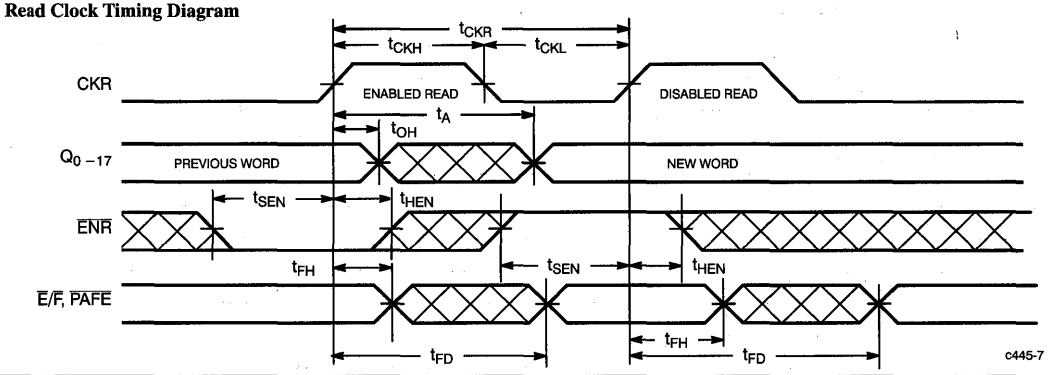
13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 5 and 9, unless otherwise specified.
14. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
15. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, and CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, and CKR is the clock for Empty and Almost Empty flags.
16. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 15 for definition of clock and opposite clock.

Switching Waveforms

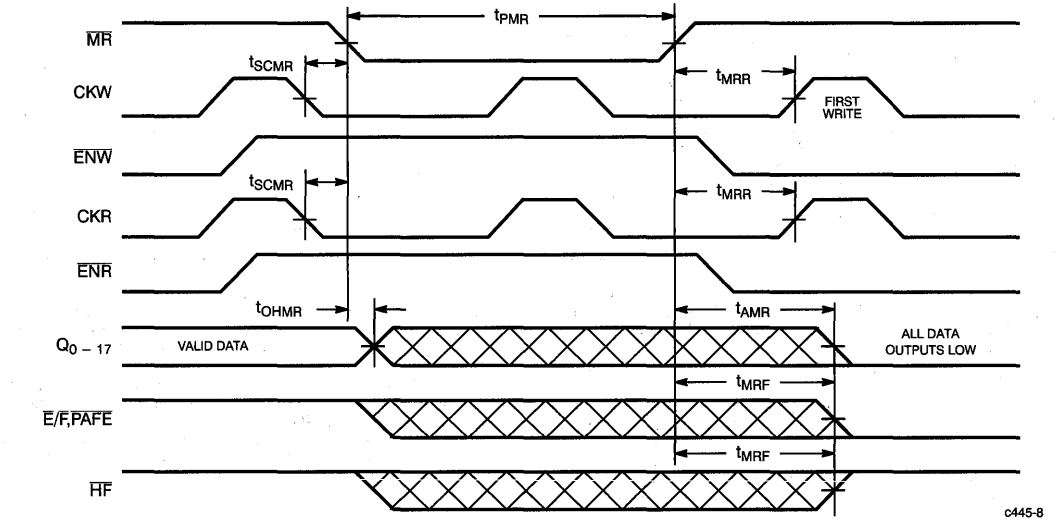
Write Clock Timing Diagram



Read Clock Timing Diagram

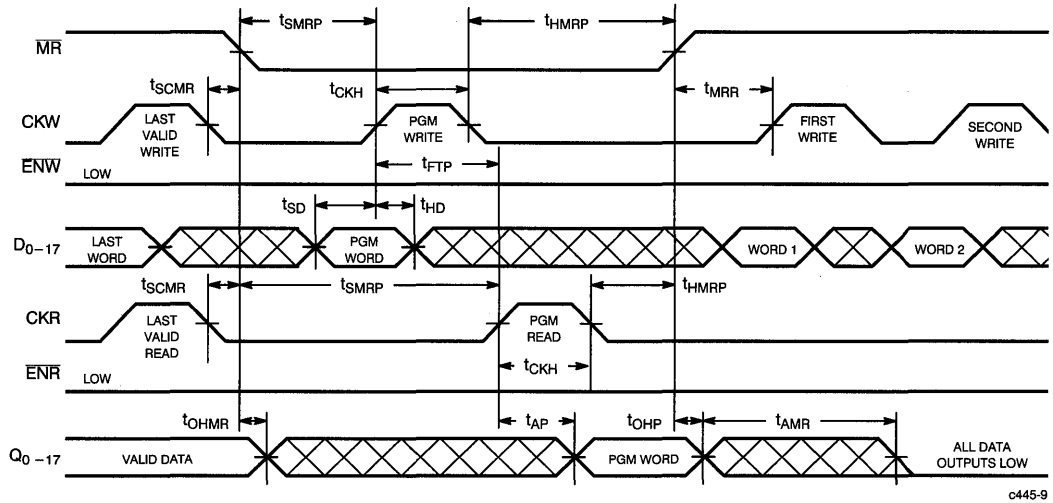


Master Reset (Default with Free-Running Clocks) Timing Diagram[17, 18, 19, 20]

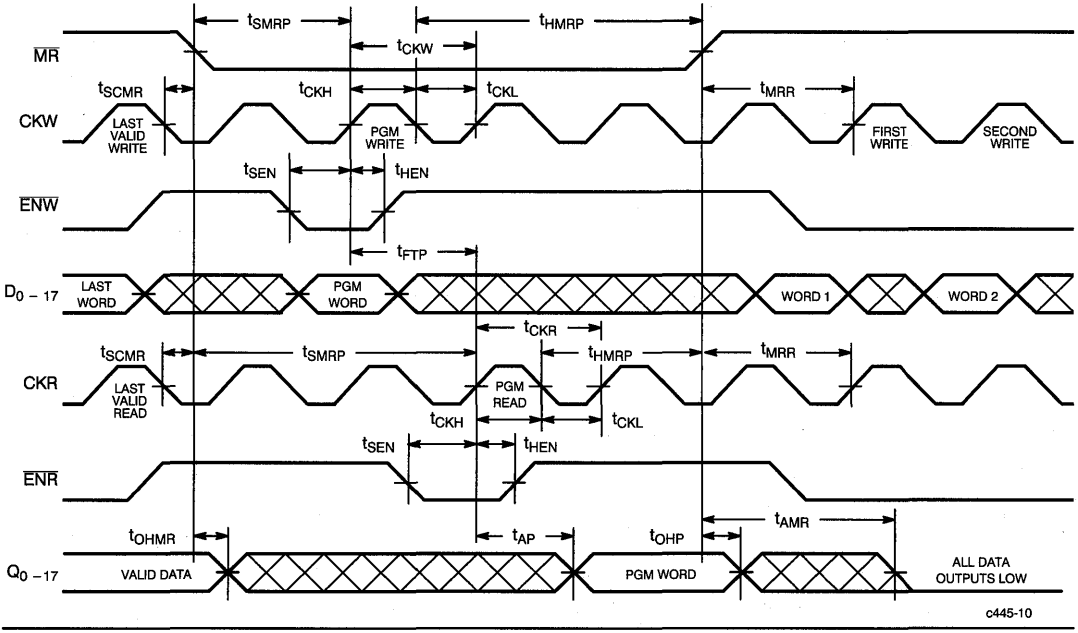


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[19, 20]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[19, 20]

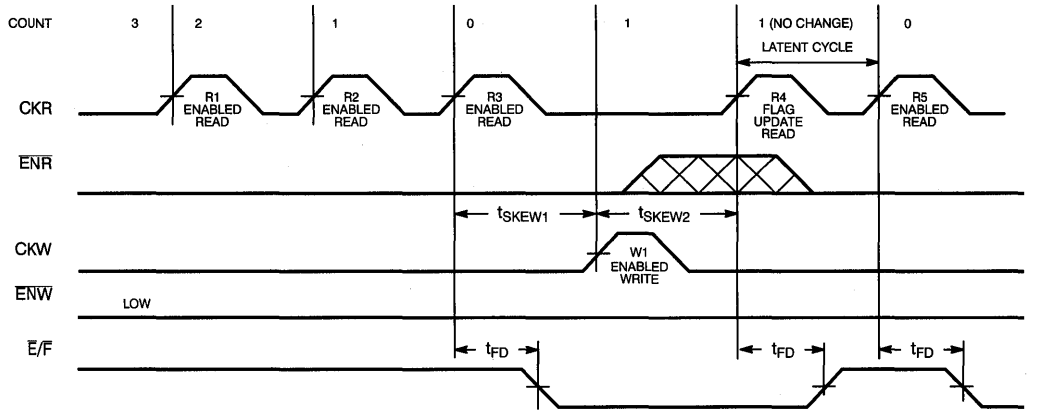


Notes:

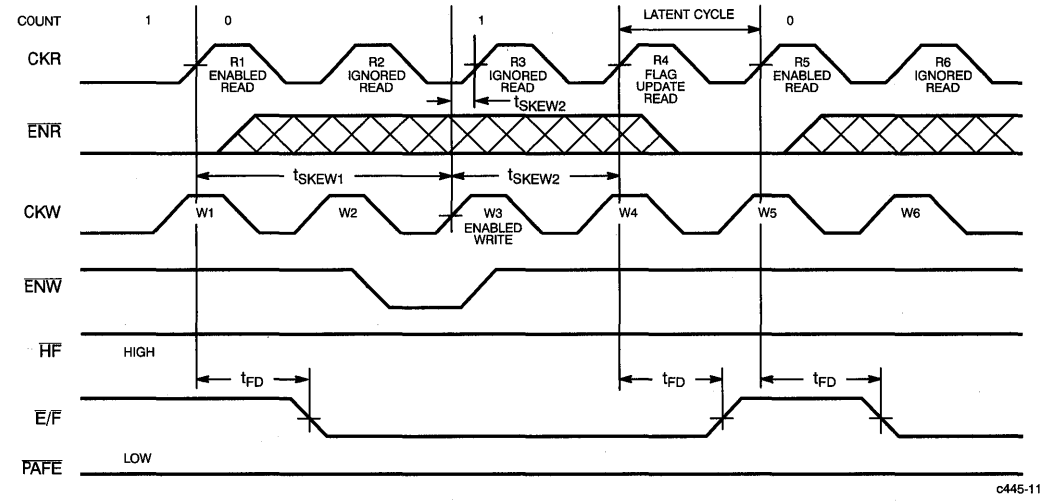
17. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
18. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
19. All data outputs (Q_{0-17}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
20. In this example, Q_{0-17} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Read to Empty Timing Diagram[21, 24, 25]



Read to Empty Timing Diagram with Free-Running Clocks[21, 22, 23, 24]

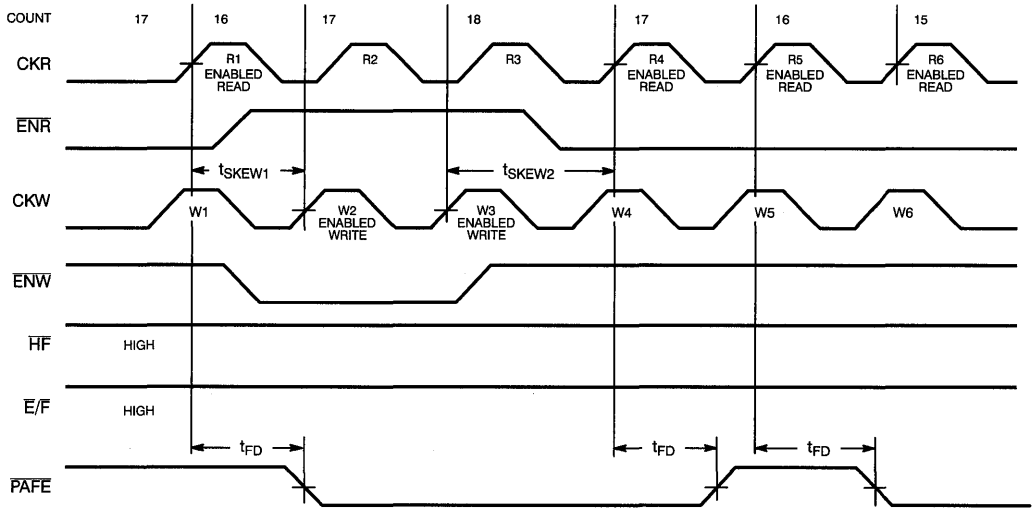


Notes:

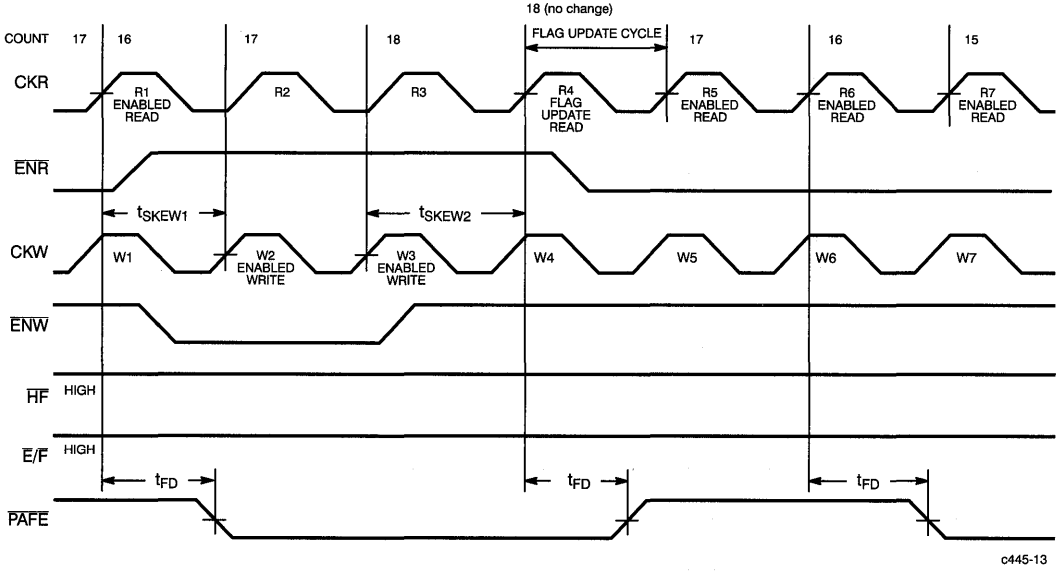
21. "Count" is the number of words in the FIFO.
22. The FIFO is assumed to be programmed with P > 0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
23. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
24. CKR is clock and CKW is opposite clock.
25. R3 updates the flag to the Empty state by asserting $\overline{E}/\overline{F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[21, 24, 26]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks[21, 24, 26, 27, 28]

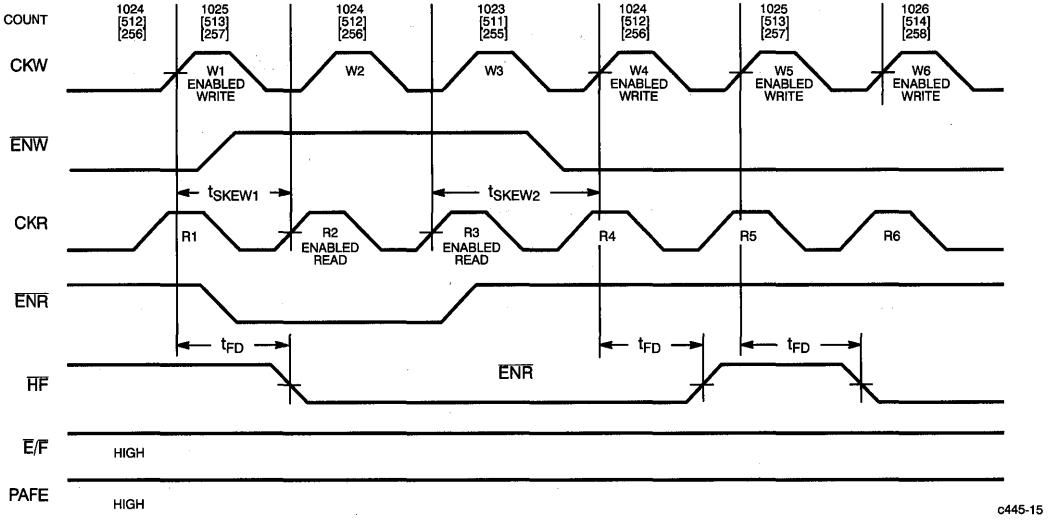


Notes:

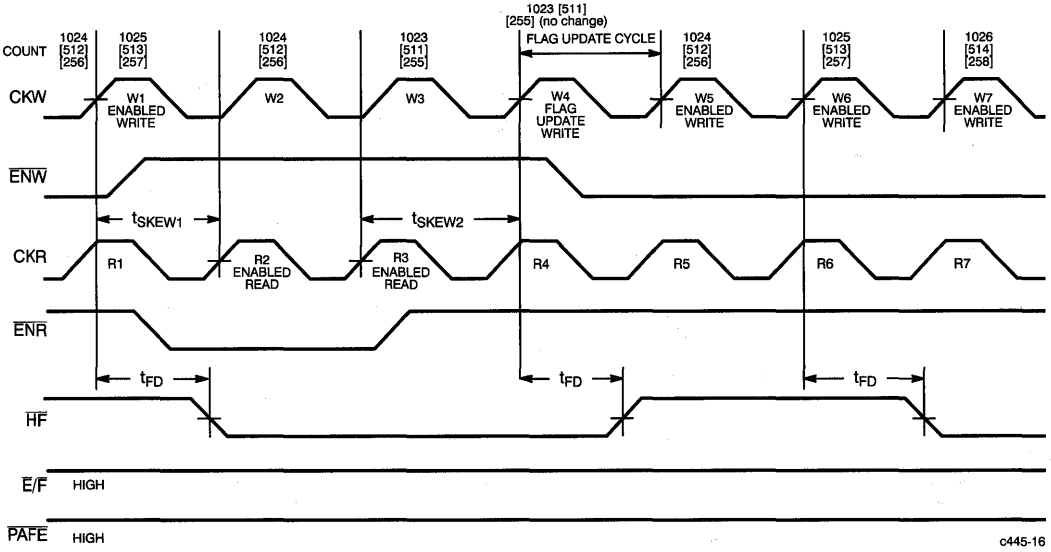
26. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
27. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
28. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ⇒ 18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[21, 29, 30, 31]



Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[21, 29, 30, 31, 32, 33]

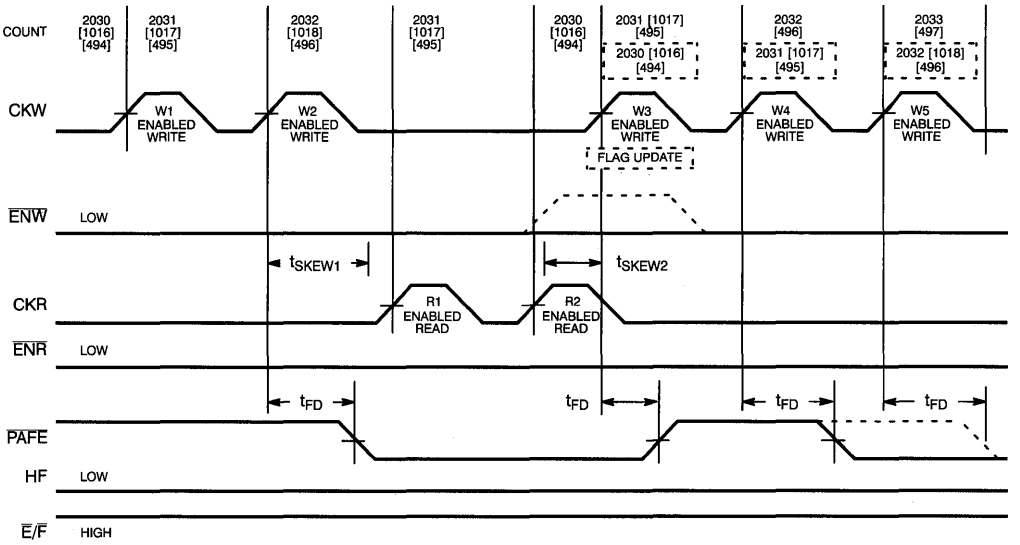


Notes:

29. CKW is clock and CKR is opposite clock.
30. Count = 1,025 indicates Half Full for the CY7C446 and CY7C456. Count = 513 indicates Half Full for the CY7C447 and CY7C457. Count = 257 indicates Half Full for the CY7C448 and CY7C458.
31. When the FIFO contains 1,024 [512] [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
32. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
33. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (i.e., 1,025 ➧ 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

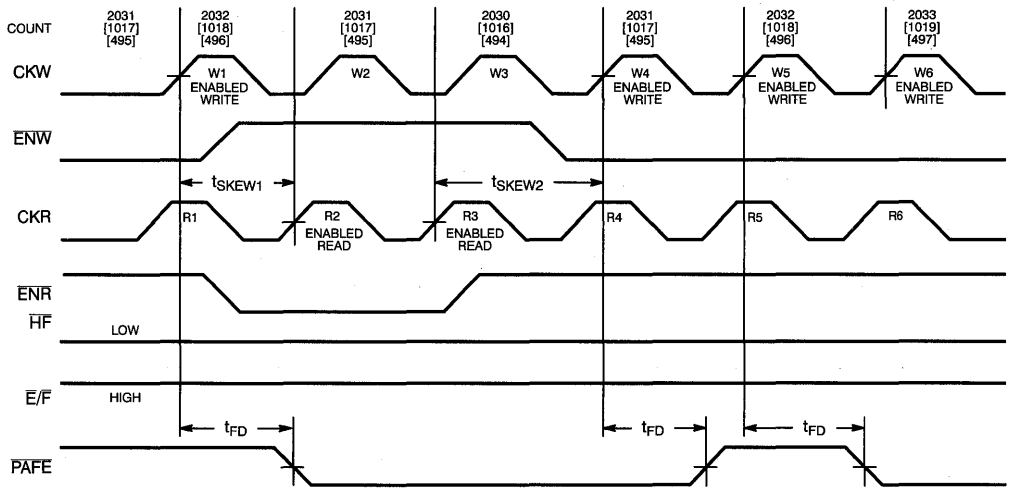
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[21, 26, 29, 34, 35]



c445-18

Write to Almost Full Timing Diagram with Free-Running Clocks[21, 26, 29]



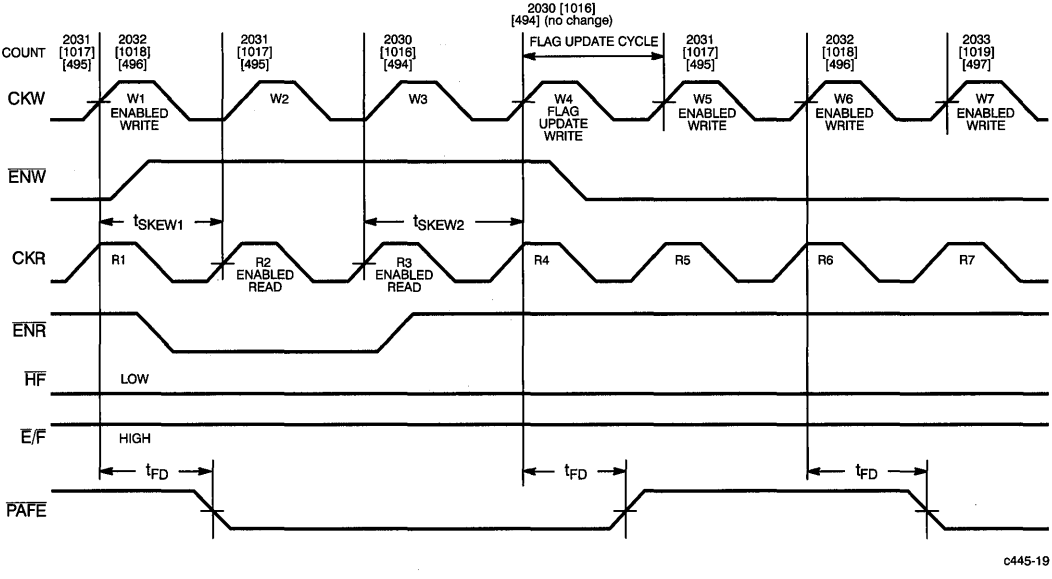
c445-17

Notes:

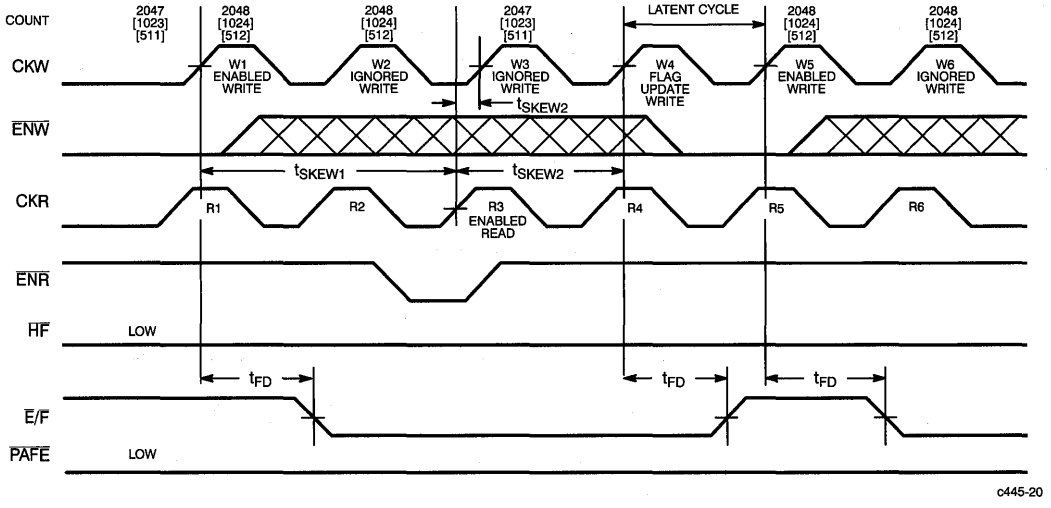
34. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
35. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is HIGH.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[21, 26, 29]



Write to Full Flag Timing Diagram with Free-Running Clocks[21, 29, 36]

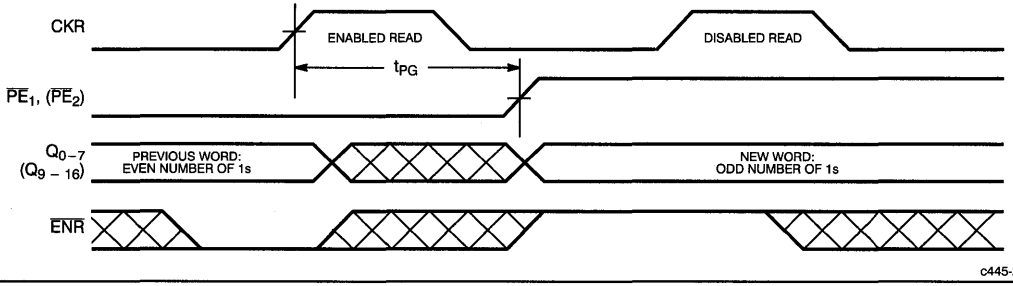


Note:

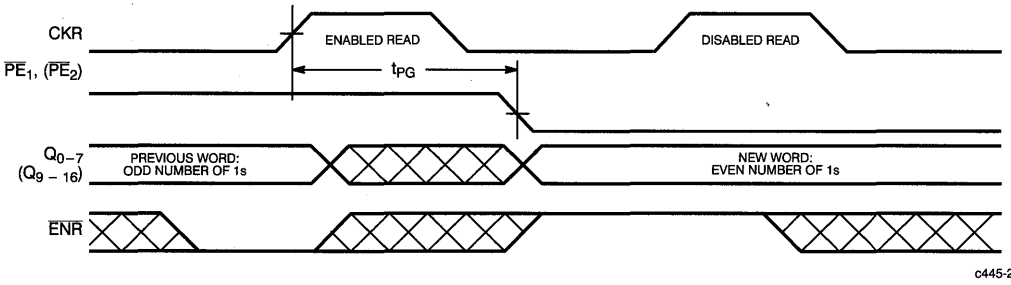
36. W2 is ignored because the FIFO is full (count = 2,048 [1,024] [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram[37, 38]



Even Parity Generation Timing Diagram[37, 39]

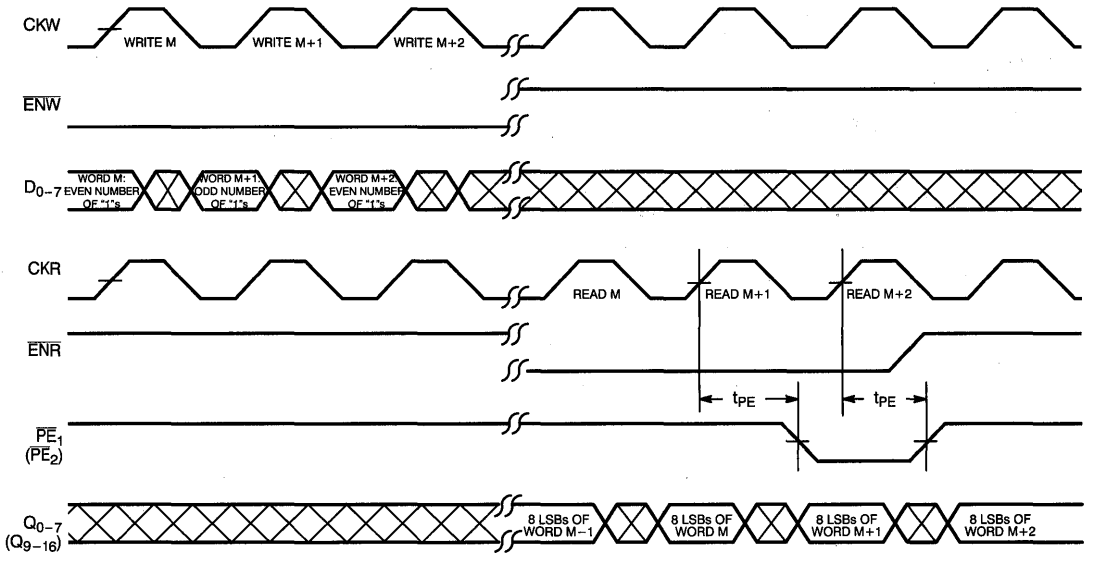


Notes:

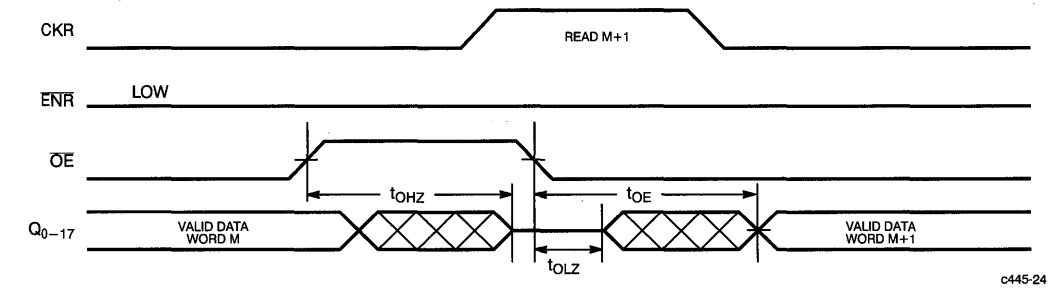
37. In this example, the FIFO is assumed to be programmed to generate even parity. The Q_{0-7} word is shown. The example is similar for the Q_{9-16} word.
38. If Q_{0-7} "new word" also has an even number of 1s, then PG1 stays LOW.
39. If Q_{0-7} "new word" also has odd number of 1s, then PG1 stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[40]



Output Enable Timing[41, 42]



Notes:

40. In this example, the FIFO is assumed to be programmed to check for even parity. The Q_{0-7} word is shown.
41. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$. The Q_{0-7} word is shown.
42. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C44X and CY7C45X consist of an array of 512, 1024, or 2,048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, and $\overline{MR}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$). The CY7C45X also includes the control signals $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, and $\overline{XO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-17}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided on the CY7C45X to three-state the Q_{0-17} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (low), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C44X and CY7C45X are programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write the $D_{0-9,10\text{ or }11}$ inputs into the programming register[43]. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on $D_{0-9,10\text{ or }11}$ during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in *Table 1* refers to the decimal equivalent of the binary number represented by $D_{0-9,10\text{ or }11}$. Programming options for the CY7C44X and CY7C45X are listed in *Table 5*.

The programmable $\overline{PAFE}$ function on the CY7C45X is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the D_{15-17} bits. See *Table 5* for a summary of the various parity programming options. Data present on D_{15-17} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-7} and D_{9-16} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C44X and CY7C45X provide three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when the CY7C45X is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).[44] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock

Table 1. Flag Truth Table[45]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	7C445, 7C455 Words in FIFO	7C446, 7C456 Words in FIFO	7C447, 7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 ➧ P	1 ➧ P	1 ➧ P
1	1	1	Less than or Equal to Half Full	P + 1 ➧ 256	P + 1 ➧ 512	P + 1 ➧ 1024
1	1	0	Greater than Half Full	257 ➧ 511 − P	513 ➧ 1023 − P	1025 ➧ 2047 − P
1	0	0	Almost Full	512 − P ➧ 511	1024 − P ➧ 1023	2048 − P ➧ 2047
0	0	0	Full	512	1024	2048

Notes:

43. For the CY7C445 and CY7C455 the CKW will write to D_{0-9}, for the CY7C446 and CY7C456 it will write to D_{0-10}, and for the CY7C447 and CY7C457 it will write to D_{0-11}.
44. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.
45. P is the decimal value of the binary number represented by D_{0-9} for the CY7C445 and CY7C455, D_{0-10} for the CY7C446 and CY7C456, and D_{0-11} for the CY7C447 and CY7C457. P = 0 signifies that the Almost Empty state = Empty state.

Flag Operation (continued)

(CKW). For example, if the CY7C457 contains 2,047 words (2,048 words indicate Full for the CY7C457), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the FIFO must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1} after or t_{SKEW2} before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read clock cycles are required to read data out of the FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is deasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C44X and CY7C45X feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at any distance from the Empty/Full boundary. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

The default distance from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Tables 3* and *4* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

The CY7C44X and CY7C45X also feature even or odd parity checking and generation. D_{15-17} are used during a program write to describe the parity option desired. *Table 5* summarizes programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on two multimode output pins (Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$). The three possible modes are described in the following paragraphs.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation					Operation	Status After Operation					Comments
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO		Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Programmable Parity

Parity Disabled (Q_8/Q_{17} mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on D_{0-17} inputs internally and will output all 18 bits on Q_{0-17}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7} and D_{9-16}. D_8 and D_{17} inputs are ignored. The parity bits are stored internally as D_8 and D_{17}, and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated (Q_{0-7} and Q_{9-16}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the FIFO is programmed for parity checking, it will compare the parity of D_{0-8} and D_{9-17} with the program register. For example, D_8 and D_{17} will be set according to the result of the parity check on each word. When these words are later read, $\overline{PE}_1$ and $\overline{PE}_2$ will reflect the result of the parity check. If a parity error occurs in D_{0-8}, D_8 will be set LOW internally. When this word is later read, $\overline{PE1}$ will be LOW.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C45X can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-17}, Q_{0-17}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-17} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-17} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-17} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C45X is cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-17} during a program read. Q_{0-17} of all other devices will remain in a high-impedance state to avoid bus contention.

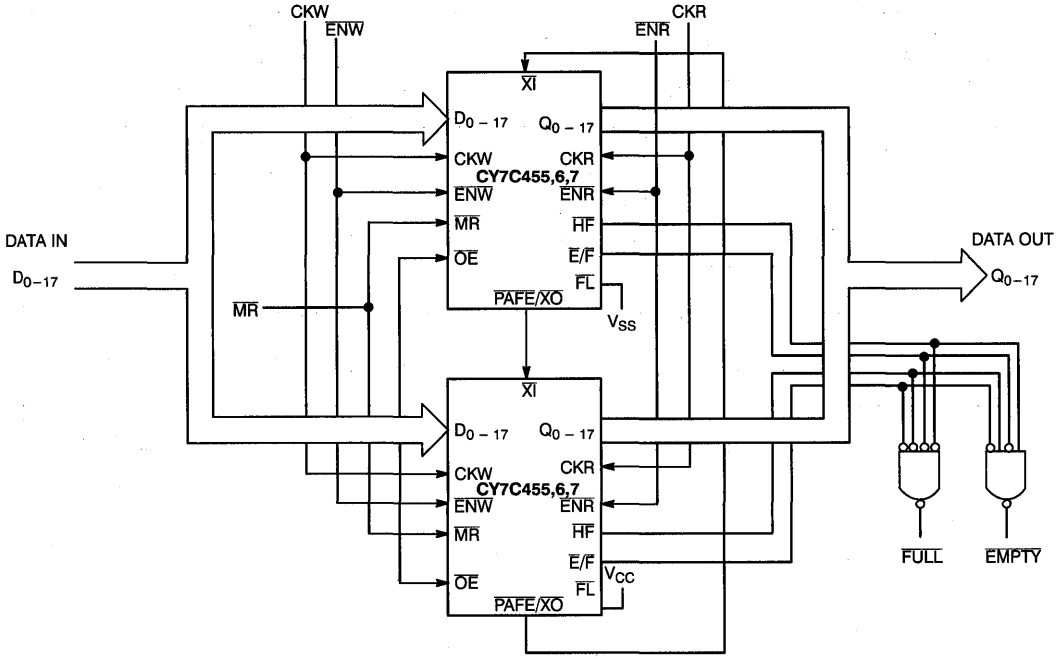


Figure 1. Depth Expansion with CY7C45X

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[46]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (transition from <HF to AE)

Note:
46. Applies to both CY7C44X and CY7C45X operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.

Table 4. Almost Full Flag Operation Example[47]

Status Before Operation							
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO 7C445	Number of Words in FIFO 7C446	Number of Words in FIFO 7C447	Operation
AF	1	0	0	496	1008	2032	Read ($\overline{ENR}$ = 0)
AF	1	0	0	495	1007	2031	Read ($\overline{ENR}$ = 0)
AF	1	0	0	494	1006	2030	Write ($\overline{ENW}$ = 1)
>HF	1	1	0	494	1006	2030	Write ($\overline{ENW}$ = 0)
>HF	1	1	0	495	1007	2031	Write ($\overline{ENW}$ = 0)

Status After Operation							
Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of Words in FIFO 7C445	Number of Words in FIFO 7C446	Number of Words in FIFO 7C447	Comments
AF	1	0	0	495	1007	2031	Read
AF	1	0	0	494	1006	2030	Read
>HF	1	1	0	494	1006	2030	Flag Update
>HF	1	1	0	495	1007	2031	Write
AF	1	0	0	496	1008	2032	Write (transition from >HF to AF)

Table 5. Programmable Parity Options

D17	D16	D15	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

Note:
47. Default condition or programmed so that Almost Full becomes active when the FIFO contains 16 or less empty locations.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C445–14DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C445–14PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C445–14PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C445–14DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
20	CY7C445–20DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C445–20PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C445–20PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C445–20DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
30	CY7C445–30DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C445–30PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C445–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C445–30DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C446–14DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C446–14PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C446–14PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C446–14DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
20	CY7C446–20DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C446–20PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C446–20PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C446–20DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
30	CY7C446–30DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C446–30PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C446–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C446–30DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C447–14DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C447–14PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C447–14PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C447–14DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
20	CY7C447–20DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C447–20PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C447–20PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C447–20DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
30	CY7C447–30DC	D26	48-Lead (600-Mil) Sidebraze DIP	Commercial
	CY7C447–30PC	P25	48-Lead (600-Mil) Molded DIP	
	CY7C447–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C447–30DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C455–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455–14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C455–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455–20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C455–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455–30LMB	L69	52-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C456–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456–14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C456–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456–20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C456–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456–30LMB	L69	52-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C457–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–14LC	L69	52-Square Leadless Chip Carrier	
	CY7C457–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457–14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C457–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457–20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C457–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457–30LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{CKW}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{OE}	9, 10, 11
t_{PG}	9, 10, 11
t_{PE}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11
t_{SMRP}	9, 10, 11
t_{HMRP}	9, 10, 11
t_{FTP}	9, 10, 11
t_{AP}	9, 10, 11
t_{OHP}	9, 10, 11

Document #: 38−00211−A

CY7C451
CY7C453

CYPRESS SEMICONDUCTOR

Cascadable Clocked 512 x 9 and Cascadable Clocked 2K x 9 FIFOs with Programmable Flags

Features

- **512 x 9 (CY7C451) and 2,048 x 9 (CY7C453) FIFO buffer memory**
- **Expandable in width and depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable Almost Full/Empty flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$)**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 32-pin DIP, PLCC, and LCC packages**
- **Proprietary 0.8μ CMOS technology**
- **Low power**
  - **$-I_{CC}$=70 mA**

Functional Description

The CY7C451 and CY7C453 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C451 has a 512-word by 9-bit memory array, while the CY7C453 has a 2,048-word by 9-bit memory array. Devices can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

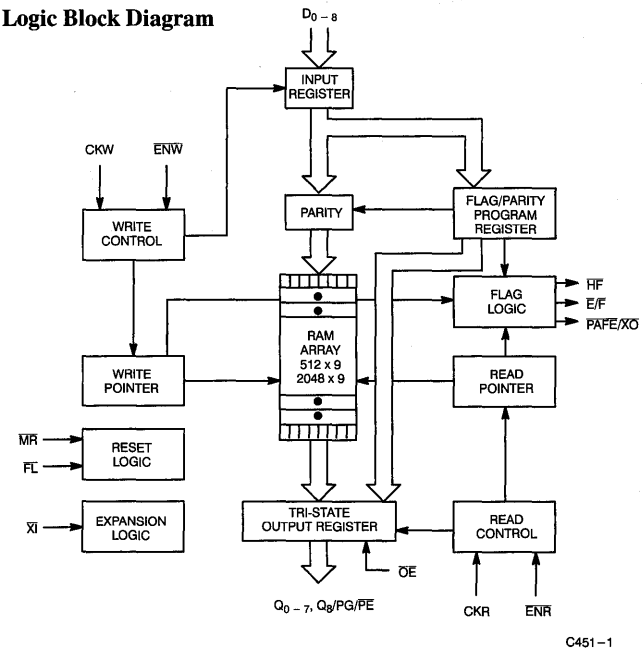
Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable in the standalone configuration, and up to 50 MHz is acceptable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$) and cascade output ($\overline{XO}$). The $\overline{XO}$ signal is connected to the $\overline{XI}$ of the next device, and the $\overline{XO}$ of the last device should be connected to the $\overline{XI}$ of the first device. In standalone mode, the input ($\overline{XI}$) pin is simply tied to V_{SS}.

The CY7C451 and CY7C453 provide three status pins to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) and $\overline{XO}$ functions share the same pin. The Almost Empty/Full flag is valid in the standalone and width

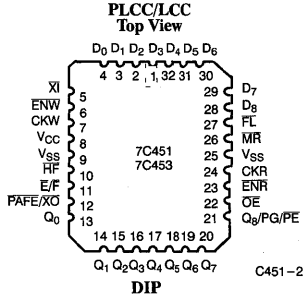
5 FIFOs

Logic Block Diagram

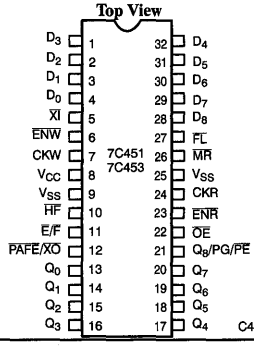


Pin Configurations

PLCC/LCC
Top View



DIP
Top View



Functional Description (continued)

expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C451 and the CY7C453 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

Selection Guide

		7C451–14 7C453–14	7C451–20 7C453–20	7C451–30 7C453–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadable Frequency		N/A[2]	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[3]	– 55°C to +125°C	5V ± 10%

Notes:

1. 71.4-MHz operation is available only in the standalone configuration.
2. The –14 device cannot be cascaded.
3. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-8}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW then data is written into the FIFO's programming register. D_8 is ignored if the device is configured for parity generation.
Q_{0-7}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR then data is read from the programming register.
$Q_8/PG/\overline{PE}$	O	Function varies according to mode: Parity disabled – same function as Q_{0-7} Parity enabled, generation – parity generation bit (PG) Parity enabled, check – Parity Error Flag ($\overline{PE}$)
$\overline{ENW}$	I	Enable Write: enables the CKW input (for both non-program and program modes)
$\overline{ENR}$	I	Enable Read: enables the CKR input (for both non-program and program modes)
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag – synchronized to CKW.
$\overline{E}/\overline{F}$	O	Empty or Full Flag – $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW
$\overline{PAFE}/\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – Programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR Cascaded – Expansion Out signal, connected to $\overline{XI}$ of next device
$\overline{XI}$	I	Not Cascaded – $\overline{XI}$ is tied to V_{SS} Cascaded – Expansion Input, connected to $\overline{XO}$ of previous device
$\overline{FL}$	I	First Load Pin: Cascaded – the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure2*) Not Cascaded – tied to V_{CC}
$\overline{MR}$	I	Master Reset: resets device to empty condition. Non-Programming Mode: program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of CKW. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7} and $Q_8/PG/\overline{PE}$ pins

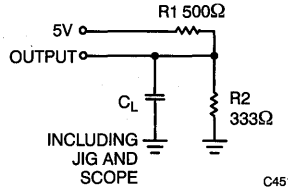
Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C451–14 7C453–14 Min.	7C451–14 7C453–14 Max.	7C451–20 7C453–20 Min.	7C451–20 7C453–20 Max.	7C451–30 7C453–30 Min.	7C451–30 7C453–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[5]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[5]	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		– 10	+10	– 10	+10	– 10	+10	µA
I_{OS}[6]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		– 90		– 90		– 90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{CC1}[7]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[8]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[9]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

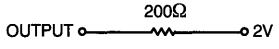
Capacitance[10]

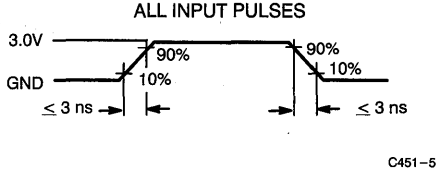
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms[11, 12, 13, 14, 15]



Equivalent to: THÉVENIN EQUIVALENT





Notes:

4. See the last page of this specification for Group A subgroup testing information.
5. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
6. Test no more than one output at a time for not more than one second.
7. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
8. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
9. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
10. Tested initially and after any design or process changes that may affect these parameters.
11. C_L = 30 pF for all AC parameters except for t_{OHZ}.
12. C_L = 5 pF for t_{OHZ}.
13. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
14. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
15. t_{OHZ} is measured at +500 mV from V_{OL} and – 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[2, 16]

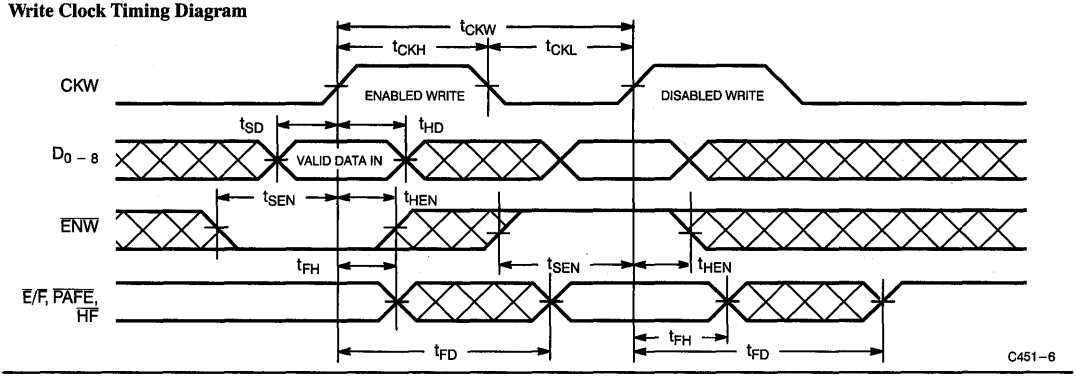
Parameter	Description	7C451–14 7C453–14		7C451–20 7C453–20		7C451–30 7C453–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[17]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[6]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[6]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[18]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[19]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		25		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

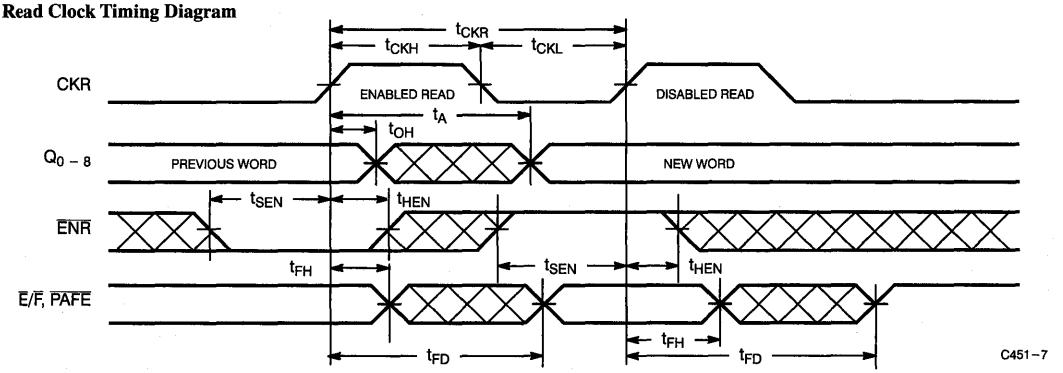
16. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 6 and 12, unless otherwise specified.
17. Access time includes all data outputs switching simultaneously.
18. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.
19. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 18 for definition of clock and opposite clock.

Switching Waveforms

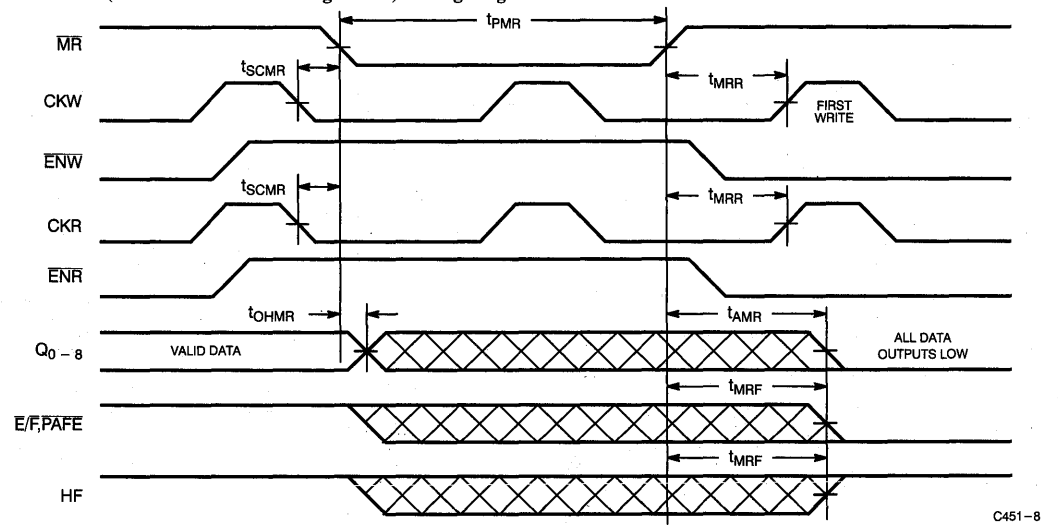
Write Clock Timing Diagram



Read Clock Timing Diagram

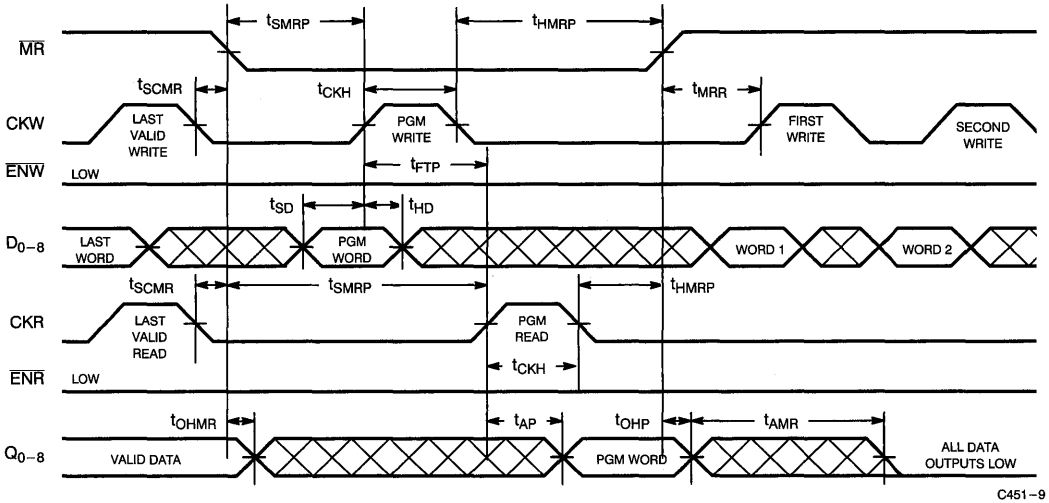


Master Reset (Default with Free-Running Clocks) Timing Diagram[20, 21, 22, 23]

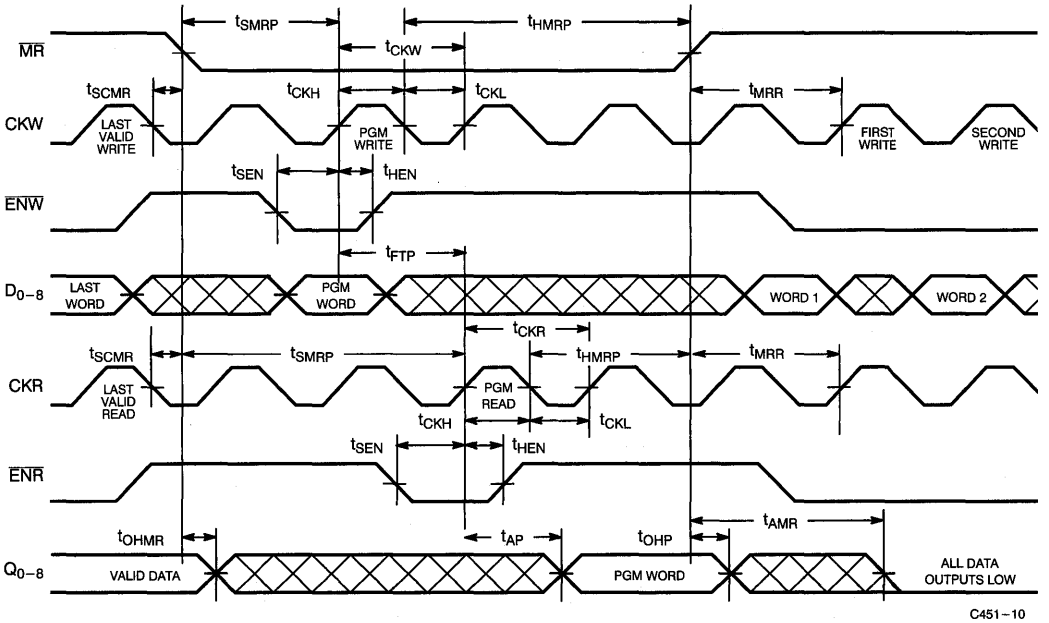


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[22, 23]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[22, 23]

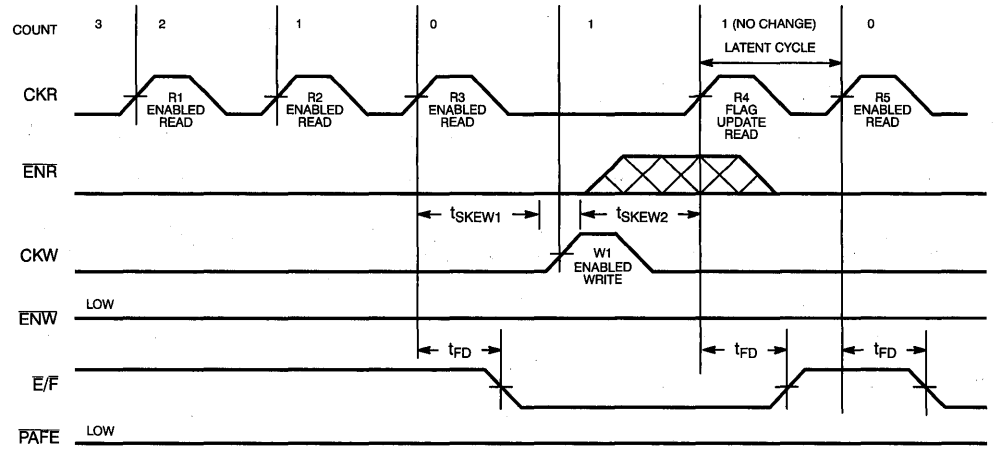


Notes:

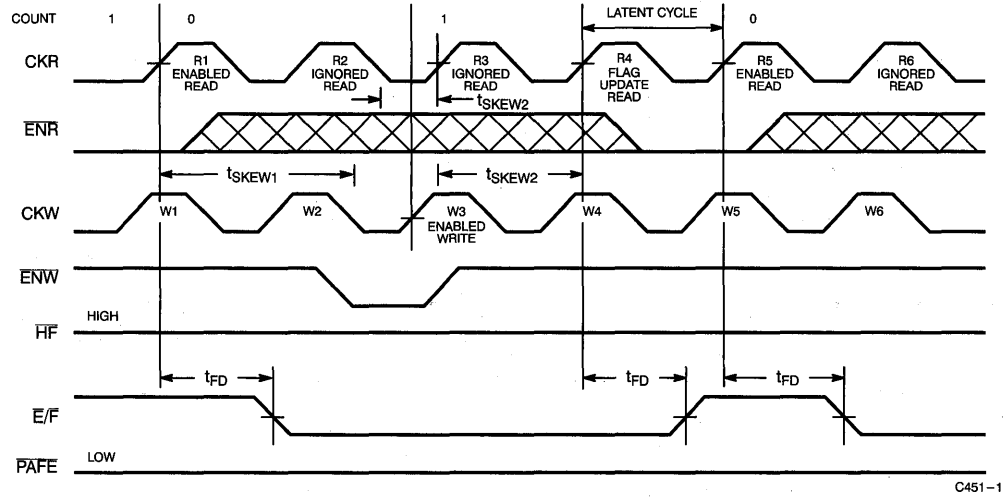
20. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
21. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
22. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
23. In this example, Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Read to Empty Timing Diagram[24, 27, 28]



Read to Empty Timing Diagram with Free-Running Clocks[24, 25, 26, 27]

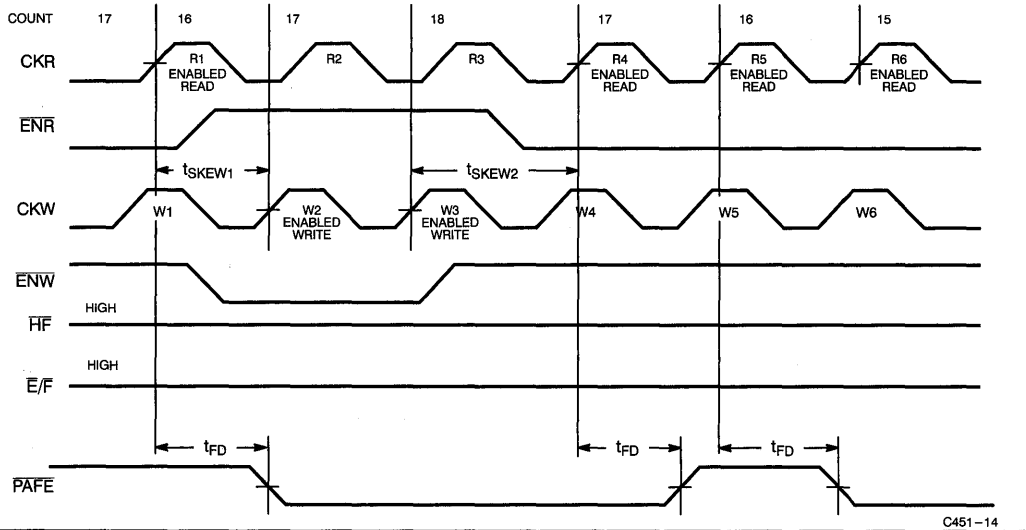


Notes:

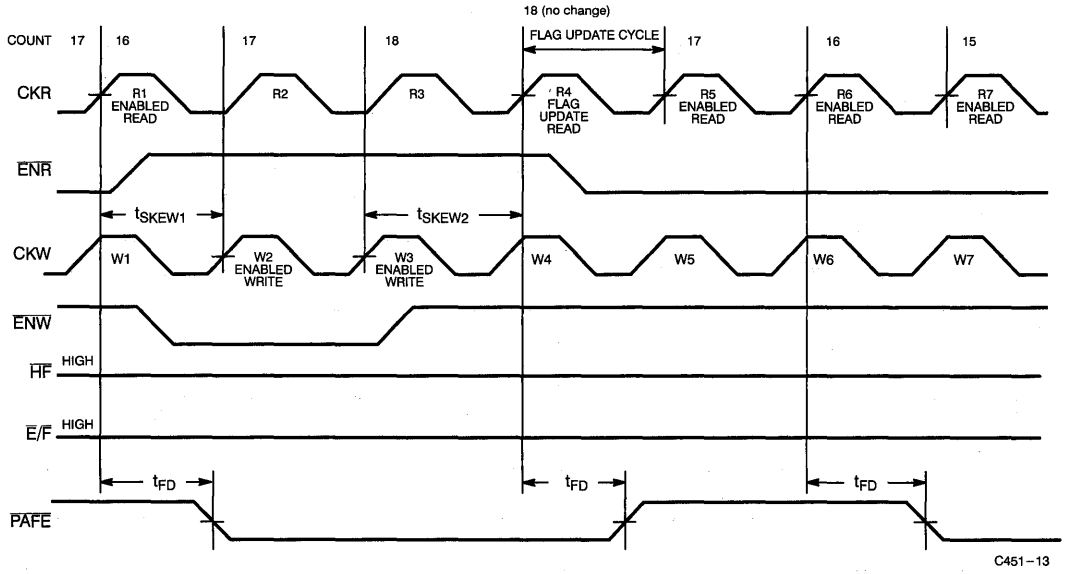
24. "Count" is the number of words in the FIFO.
25. The FIFO is assumed to be programmed with P>0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
26. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
27. CKR is clock; CKW is opposite clock.
28. R3 updates the flag to the Empty state by asserting $\overline{E/F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[24, 27, 29]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[24, 27, 29, 30, 31]

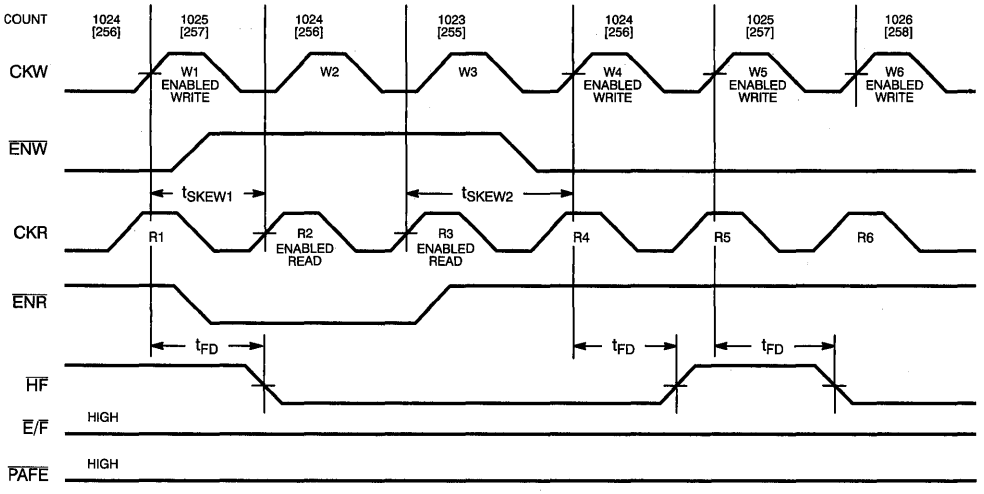


Notes:

29. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
30. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
31. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

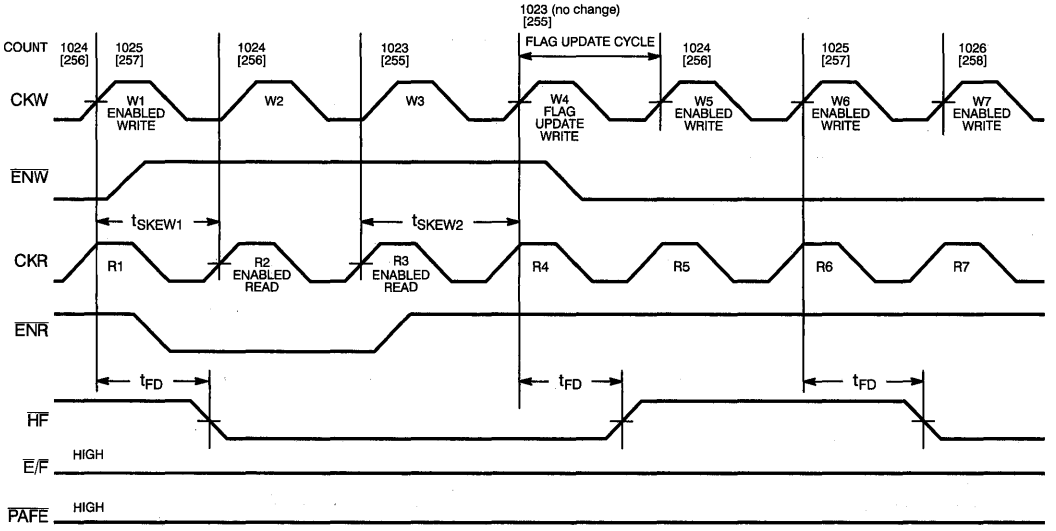
Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[24, 32, 33, 34]



C451–15

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[24, 32, 33, 34, 35, 36]



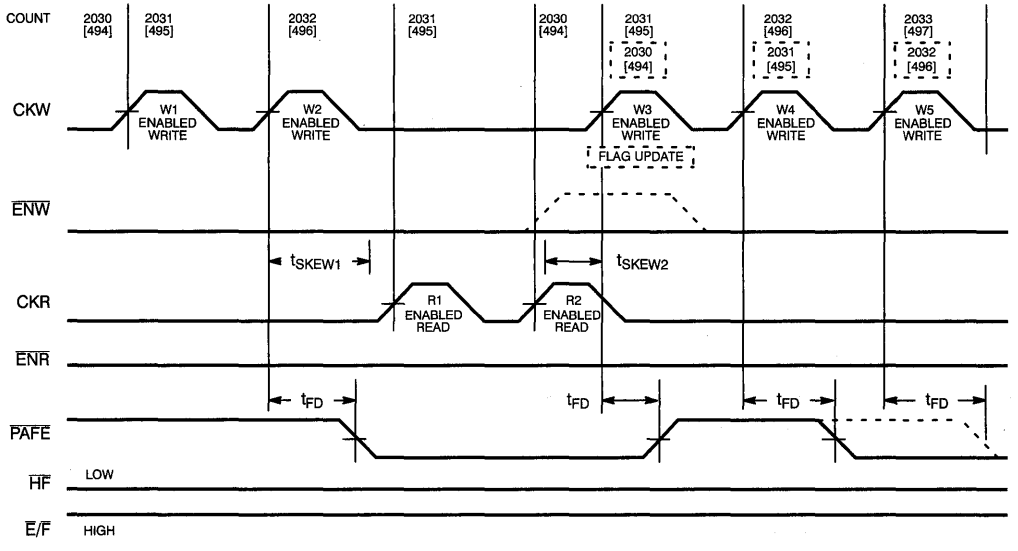
C451–16

Notes:

32. CKW is clock and CKR is opposite clock.
33. Count = 1,025 indicates Half Full for the CY7C453 and count = 257 indicates Half Full for the CY7C451. Values for CY7C451 count are shown in brackets.
34. When the FIFO contains 1,024 [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
35. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
36. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (1,025 ➧ 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

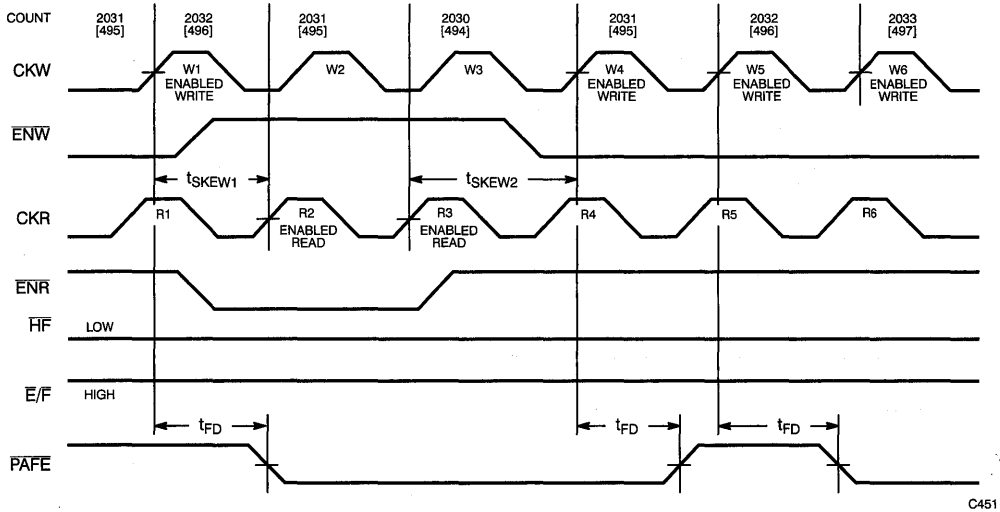
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[24, 29, 32, 37, 38]



C451–18

Write to Almost Full Timing Diagram with Free-Running Clocks[24, 29, 32]



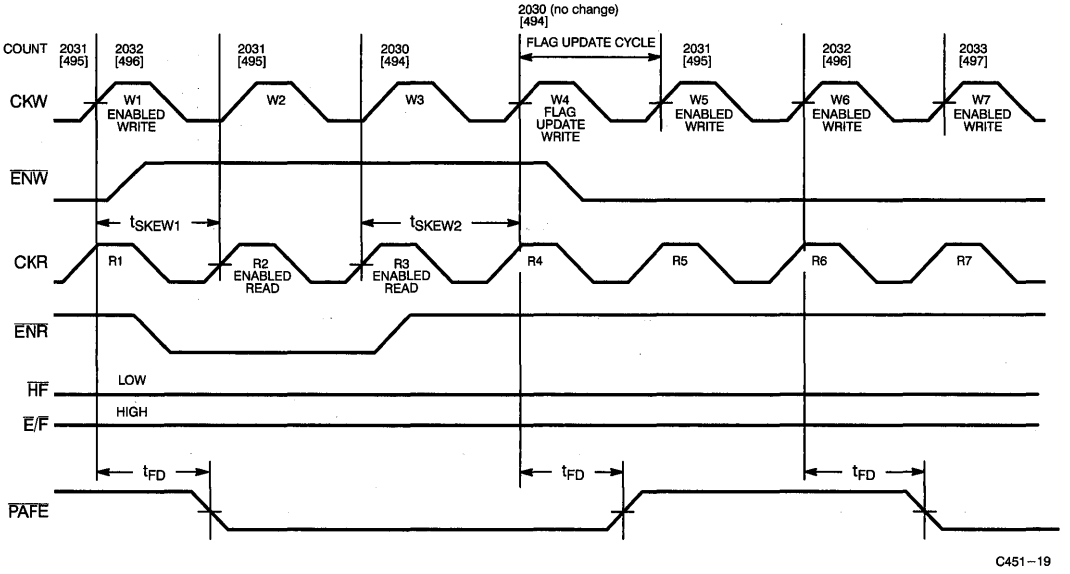
C451–17

Notes:

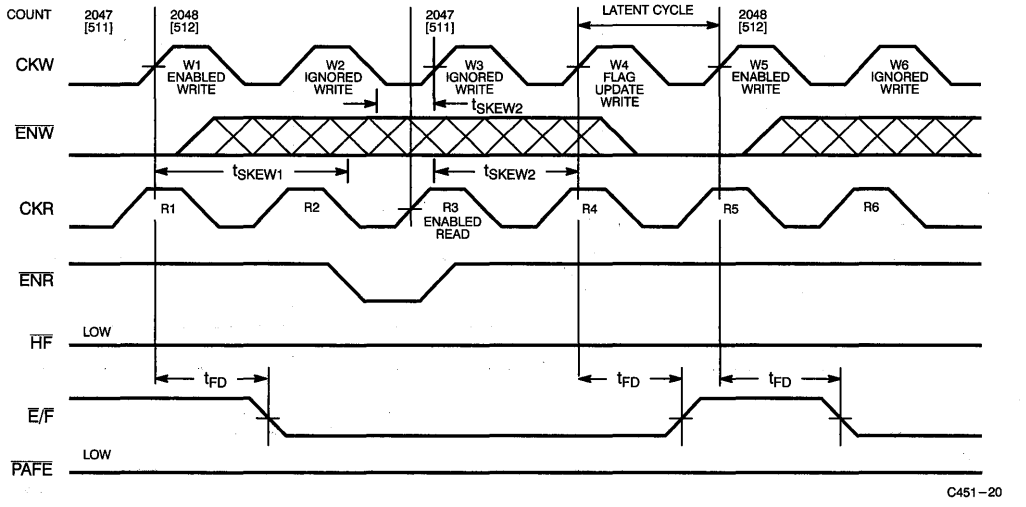
37. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
38. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[24, 29, 32]



Write to Full Flag Timing Diagram with Free-Running Clocks[24, 25, 32, 39]

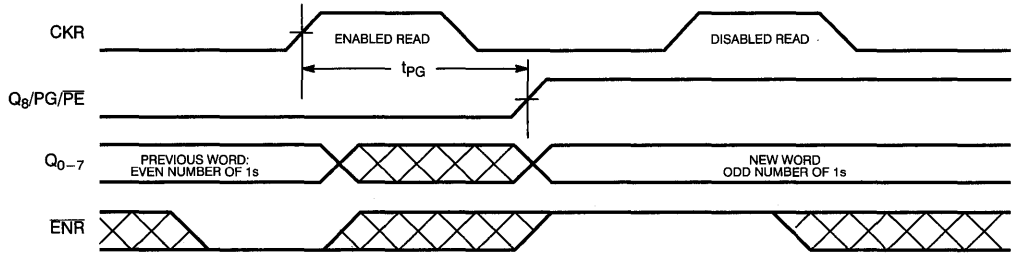


Notes:

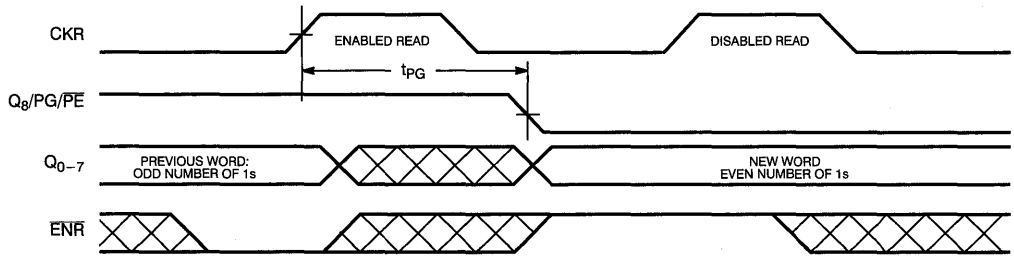
39. W2 is ignored because the FIFO is full (count = 2,048 [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram[40, 41]



Even Parity Generation Timing Diagram[40, 42]

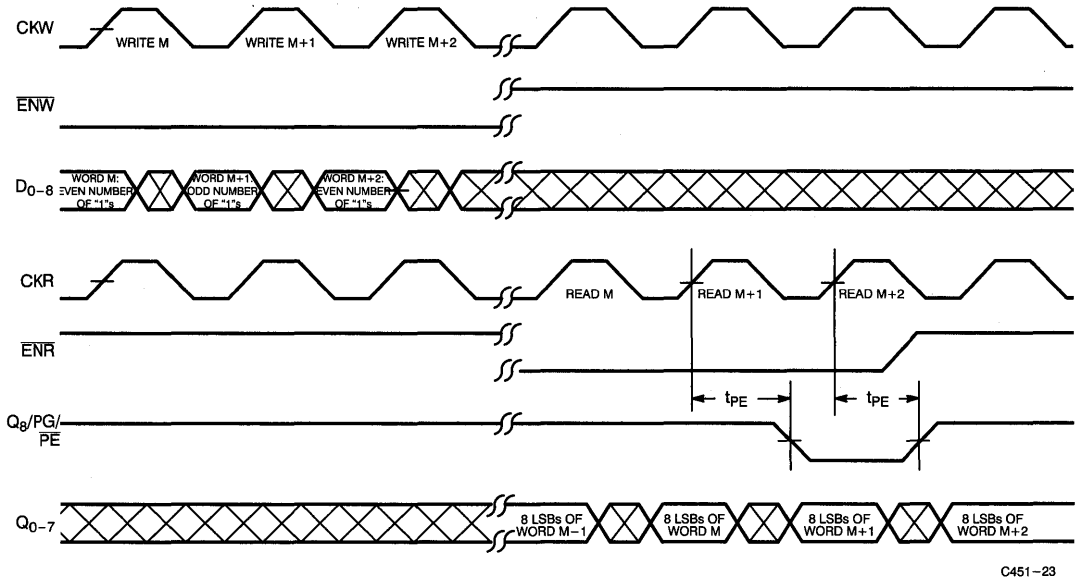


Notes:

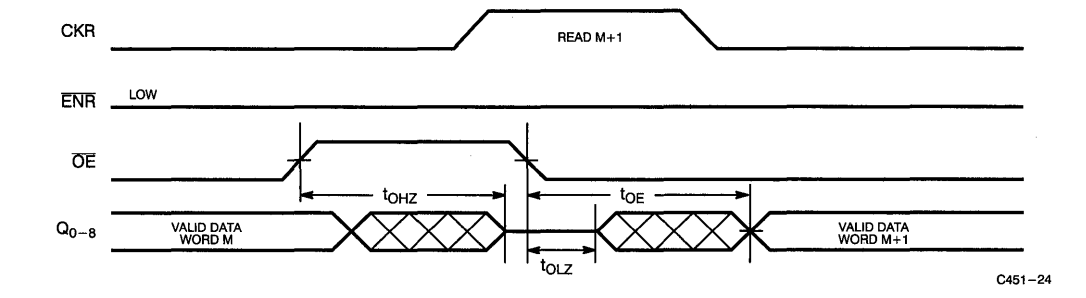
40. In this example, the FIFO is assumed to be programmed to generate even parity.
41. If Q_{0-7} "new word" also has an even number of 1s, then PG stays LOW.
42. If Q_{0-7} "new word" also has an odd number of 1s, then PG stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[43]



Output Enable Timing[44, 45]



Notes:

43. In this example, the FIFO is assumed to be programmed to check for even parity.
44. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$.
45. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C451 and CY7C453 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{CKR}$, $\overline{CKW}$, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$, $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, $\overline{XO}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-8}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to tri-state the Q_{0-8} outputs when $\overline{OE}$ is not asserted. When $\overline{OE}$ is enabled, data in the output register will be available to Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Programming

The CY7C451 and CY7C453 are programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write D_{0-8} inputs into the programming register. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-5} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in *Table 1* refers to the decimal equivalent of the binary number represented by D_{0-5}. Programming options for the CY7C451 and CY7C453 are listed in *Table 5*. Programming resolution is 16 words for either device.

The programmable $\overline{PAFE}$ function is only valid when the CY7C451/453 are not cascaded. If the user elects not to program the FIFO's flags, the default (P=1) is as follows: Almost Empty condition (Almost Full condition) is activated when the CY7C451/453 contain 16 or less words (empty locations).

Parity is programmed with the D_{6-8} bits. See *Table 1* for a summary of the various parity programming options. Data present on D_{6-8} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-8} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C451/453 provide three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when FIFOs are cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate. See *Figure 1.*). The synchronous architecture guarantees some minimum valid time for the flags. The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock (CKW). For example, if the CY7C453 FIFO contains 2047 words (2048 words indicate Full for the CY7C453), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Table 1. Flag Truth Table[46]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	CY7C451 512 x 9 Number of Words in FIFO	CY7C453 2K x 9 Number of Words in FIFO
0	0	1	Empty	0	0
1	0	1	Almost Empty	1 ⧫ (16 • P)	1 ⧫ (16 • P)
1	1	1	Less than or Equal to Half Full	(16 • P)+1 ⧫ 256	(16 • P)+1 ⧫ 1024
1	1	0	Greater than Half Full	257 ⧫ 511 − (16 • P)	1025 ⧫ 2047 − 16 • P
1	0	0	Almost Full	512 − (16 • P) ⧫ 511	2048 − (16 • P) ⧫ 2047
0	0	0	Full	512	2048

Note:

46. P is the decimal value of the binary number represented by D_{0-5}. When programming the CY7C451/53, P can have values from 0 to 15 for the CY7C451 and values from 0 to 63 for the CY7C453. See *Table 5* for D_{0-5} representation. P = 0 signifies Almost Empty state = Empty state.

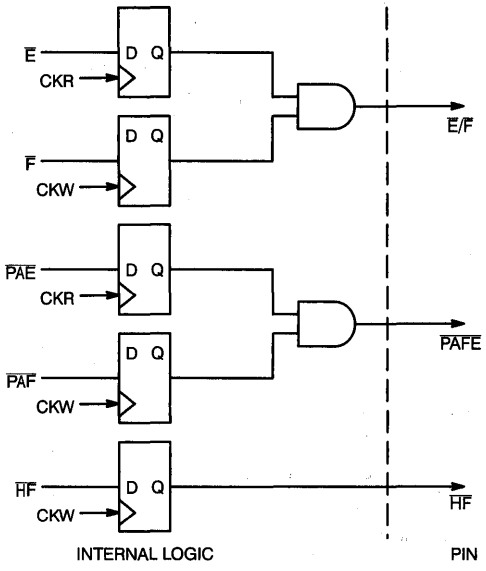


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the CY7C451/453 must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on the CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read cycles are required to read data out of FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is unasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on the CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C451/453 feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at a distance of up to 1008 words/locations for the CY7C453 (240 words/locations for the CY7C451) from the Empty/Full boundary. The programming resolution is 16 words/locations. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

The default distance (CY7C451/453 not programmed) from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Tables 3* and *4* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

Programmable Parity

The CY7C451/453 also features even or odd parity checking and generation. D_{6-8} are used during a program write to describe the parity option desired. *Table 6* gives a summary of programmable parity options. If user elects not to program the device, then parity is disabled. Parity information is provided on one multi-mode output pin (Q8/PG/$\overline{PE}$). The three possible modes are described in the following paragraphs. Regardless of the mode selected, the $\overline{OE}$ pin retains tri-state control of all 9 Q_{0-8} bits.

Parity Disabled (Q8 mode)

When parity is disabled (or user does not program parity option) the CY7C451/453 stores all 9 bits present on D_{0-8} inputs internally and will output all 9 bits on Q_{0-8}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7}. D_8 input is ignored. The parity bit is stored internally as D_8 and during a subsequent read will be available on the PG pin along with the data word from which the parity was generated (Q_{0-7}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the CY7C451/453 is programmed for parity checking, the FIFO will compare the parity of D_{0-8} with the program register. If the expected parity is present, D_8 will be set HIGH internally. When this word is later read, $\overline{PE}$ will be HIGH. If a parity error occurs, D_8 will be set LOW internally. When this word is later read, $\overline{PE}$ will be LOW. For example, if parity check is set to odd and D_{0-8} have an even number of 1s, a parity error occurs. When that word is later read, $\overline{PE}$ will be asserted (LOW).

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. The CY7C451/453 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C451/453 can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with

$\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-8}, Q_{0-8}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-8} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-8} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-8} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C451/453 are cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-8} during a program read. Q_{0-8} of all other devices will remain in a high-impedance state to avoid bus contention.

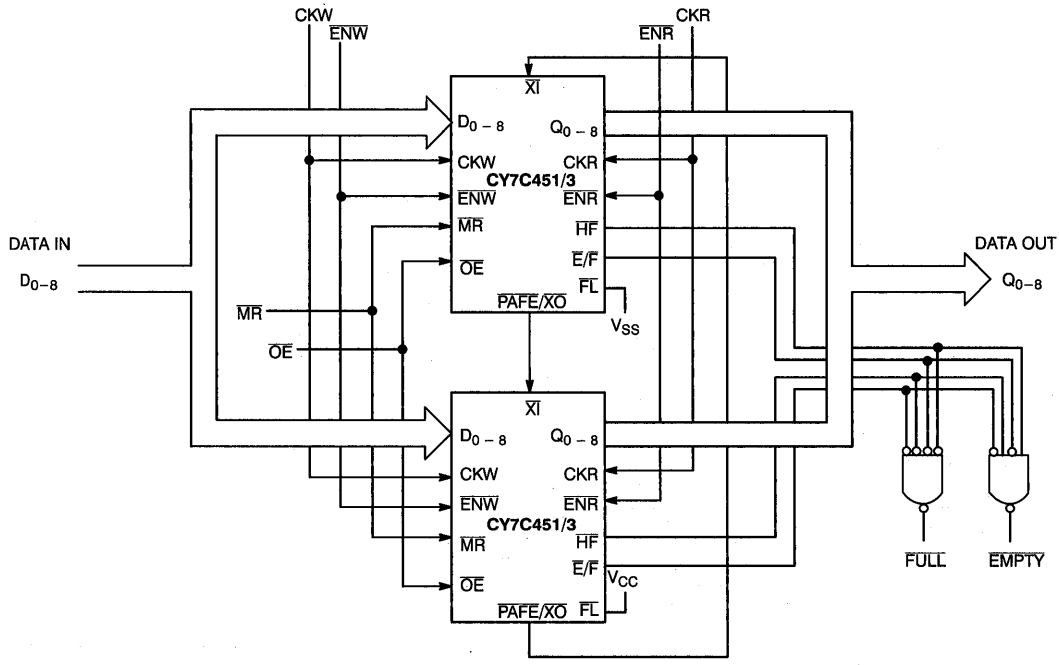


Figure 2. Depth Expansion with CY7C451/3

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[47]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (Transition from <HF to AE)

Table 4. Almost Full Flag Operation Example[48]

Status Before Operation							Status After Operation						
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	Operation	Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	Comments
AF	1	0	0	496	2032	Read ($\overline{ENR}$ = 0)	AF	1	0	0	495	2031	Read
AF	1	0	0	495	2031	Read ($\overline{ENR}$ = 0)	AF	1	0	0	494	2030	Read
AF	1	0	0	494	2030	Write ($\overline{ENW}$ = 1)	>HF	1	1	0	494	2030	Flag Update
>HF	1	1	0	494	2030	Write ($\overline{ENW}$ = 0)	>HF	1	1	0	495	2031	Write
>HF	1	1	0	495	2031	Write ($\overline{ENW}$ = 0)	AF	1	0	0	496	2032	Write (Transition from >HF to AF)

Table 5. Programmable Almost Full/Almost Empty Options – CY7C451/CY7C453[49]

D5	D4	D3	D2	D1	D0	PAFE Active when CY7C451/453 is:	P[50]
0	0	0	0	0	0	Completely Full and Empty.	0
0	0	0	0	0	1	16 or less locations from Empty/Full (default)	1
0	0	0	0	1	0	32 or less locations from Empty/Full	2
0	0	0	0	1	1	48 or less locations from Empty/Full	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	1	1	0	224 or less locations from Empty/Full	14
0	0	1	1	1	1	240 or less locations from Empty/Full	15
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	992 or less locations from Empty/Full	62
1	1	1	1	1	1	1008 or less locations from Empty/Full	63

Table 6. Programmable Parity Options

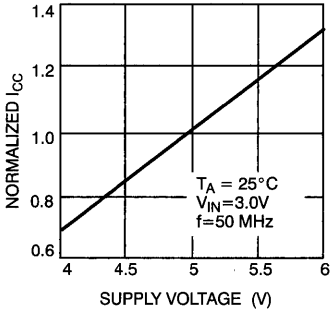
D8	D7	D6	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

Notes:

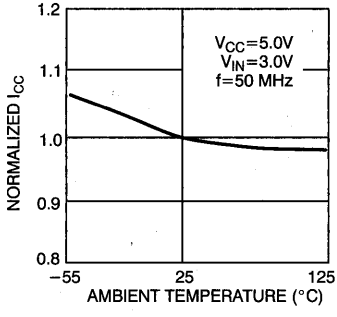
47. Applies to both CY7C451 and CY7C453 operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.
48. Programmed so that Almost Full becomes active when the FIFO contains 16 or less empty locations.
49. D4 and D5 are don't care for CY7C451.
50. Referenced in *Table 1*.

Typical DC and AC Characteristics

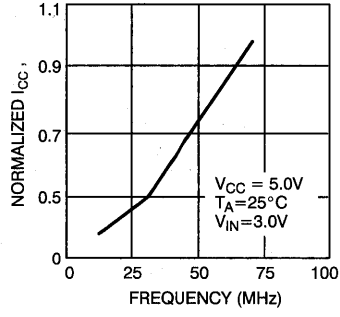
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



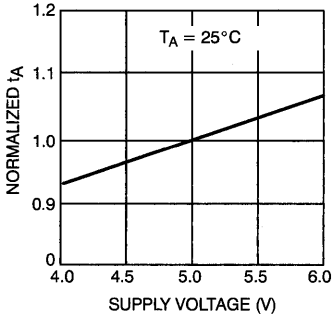
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



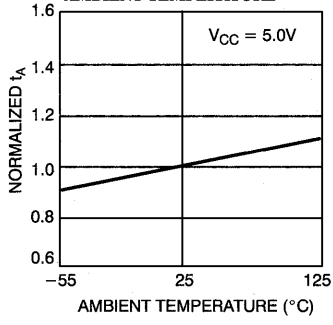
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



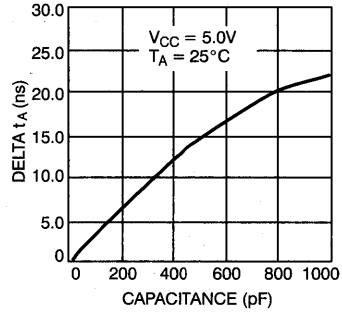
NORMALIZED t_A vs. SUPPLY VOLTAGE



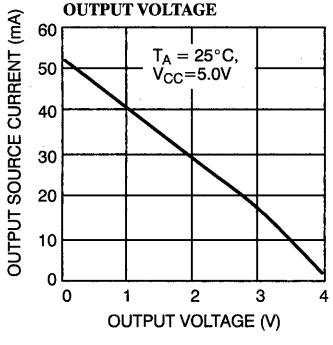
NORMALIZED t_A vs. AMBIENT TEMPERATURE



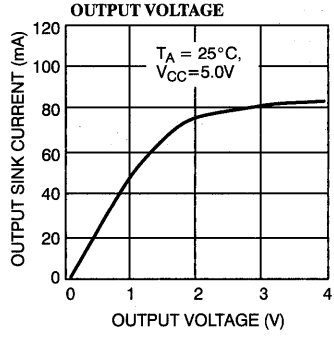
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



5 FIFOs

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C451–14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C451–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C451–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–30JI	D32	32-Lead (300-Mil) CerDIP	Industrial
	CY7C451–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C453–14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C453–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C453–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKW}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{OE}	9, 10, 11
t_{PG}	9, 10, 11
t_{PE}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11
t_{SMRP}	9, 10, 11
t_{HMRP}	9, 10, 11
t_{FTP}	9, 10, 11
t_{AP}	9, 10, 11
t_{OHP}	9, 10, 11

Document #: 38–00125–E

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C460
CY7C462
CY7C464

Cascadable 8K x 9 FIFO
Cascadable 16K x 9 FIFO
Cascadable 32K x 9 FIFO

Features

- **8K x 9, 16K x 9, 32K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  - **I_{CC} (max.) = 160 mA (commercial)**
  - **I_{CC} (max.) = 165 mA (military)**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **5V ± 10% supply**
- **PLCC, LCC, and 600-mil DIP packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible to IDT7205 and IDT7206**

Functional Description

The CY7C460, CY7C462, and CY7C464 are respectively, 8K, 16K, and 32K words by 9-bit wide first-in-first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

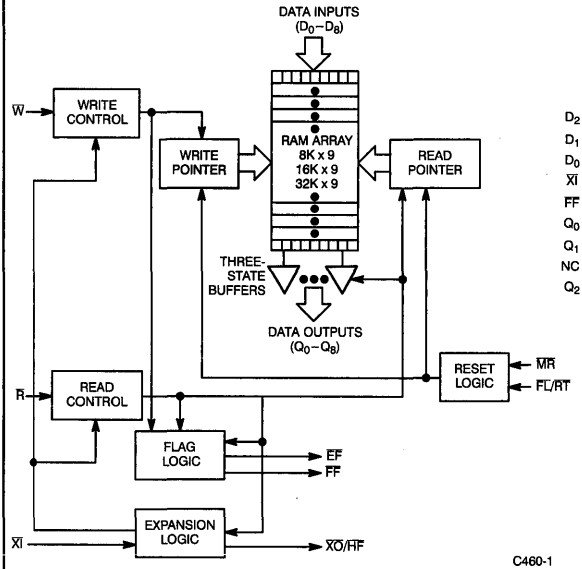
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

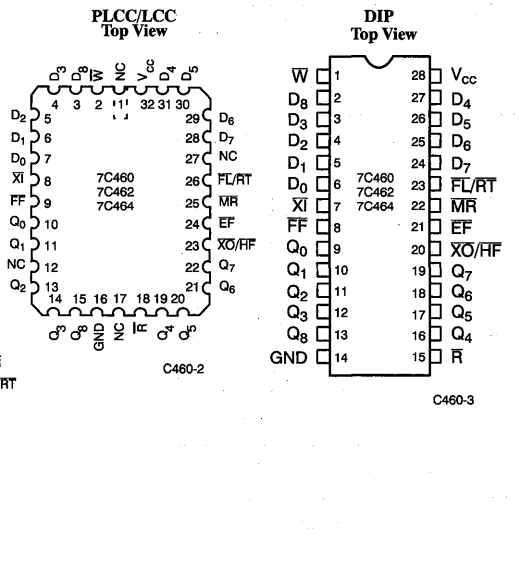
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C460, CY7C462, and CY7C464 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C460–15 7C462–15 7C464–15	7C460–20 7C462–20 7C464–20	7C460–25 7C462–25 7C464–25	7C460–40 7C462–40 7C464–40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	160		145	125
	Military		165	165	145

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C460-15 7C462-15 7C464-15 Min.	Max.	7C460-20 7C462-20 7C464-20 Min.	Max.	7C460-25 7C462-25 7C464-25 Min.	Max.	7C460-40 7C462-40 7C464-40 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0				2.0		2.0		V
			Mil/Ind			2.2		2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		160				145		125	mA
			Mil/Ind[4]				165		165		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25		25	mA
			Mil/Ind				30		30		30	
I_{SB2}	Power-Down Current	All Inputs V_{CC} – 0.2V	Com'l		20				20		20	mA
			Mil/Ind				25		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			–90		–90		–90		–90	mA

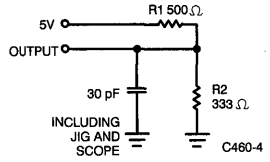
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 125 mA + [(f – 20) * 2.5 mA/MHz] for f ≥ 20 MHz
   where f = the larger of the write or read operating frequency.
4. I_{CC} (military) = 130 mA + [(f – 20) * 2.5 mA/MHz] for f ≥ 20 MHz
   where $\overline{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.
6. Tested initially and after any design or process changes that may affect these parameters.

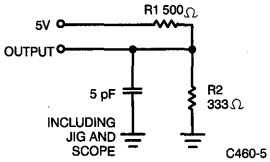
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

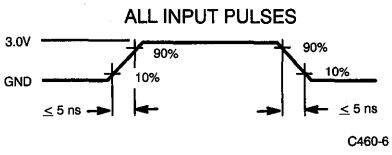
AC Test Loads and Waveforms



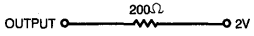
(a)



(b)



Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 7]

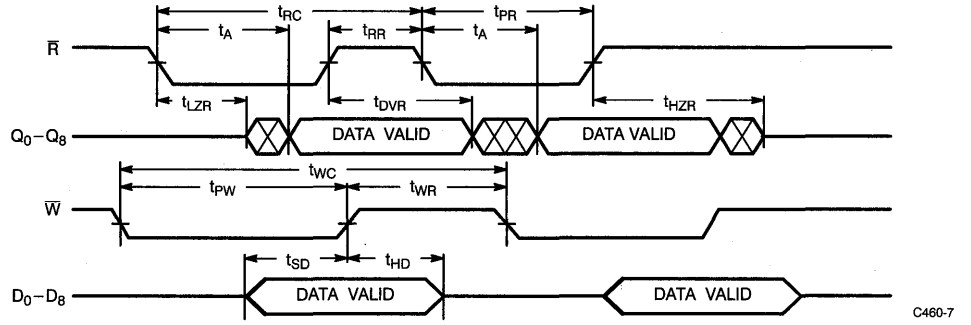
Parameter	Description	7C460–15 7C462–15 7C464–15		7C460–20 7C462–20 7C464–20		7C460–25 7C462–25 7C464–25		7C460–40 7C462–40 7C464–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		30		35		50		ns
t_A	Access Time		15		20		25		40	ns
t_{RR}	Read Recovery Time	10		10		10		10		ns
t_{PR}	Read Pulse Width	15		20		25		40		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8]	Data Valid After Read HIGH	3		3		3		3		ns
t_{HZR}[8]	Read HIGH to High Z		15		15		18		25	ns
t_{WC}	Write Cycle Time	30		30		35		50		ns
t_{PW}	Write Pulse Width	15		20		25		40		ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-Up Time	11		12		15		20		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		30		35		50		ns
t_{PMR}	$\overline{MR}$ Pulse Width	15		20		25		40		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	15		20		25		40		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	15		20		25		40		ns
t_{RTC}	Retansmit Cycle Time	30		30		35		50		ns
t_{PRT}	Retransmit Pulse Width	15		20		25		40		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		25		30		35		50	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		25		30		35		50	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		25		30		35		50	ns

Switching Characteristics Over the Operating Range[2,7] (continued)

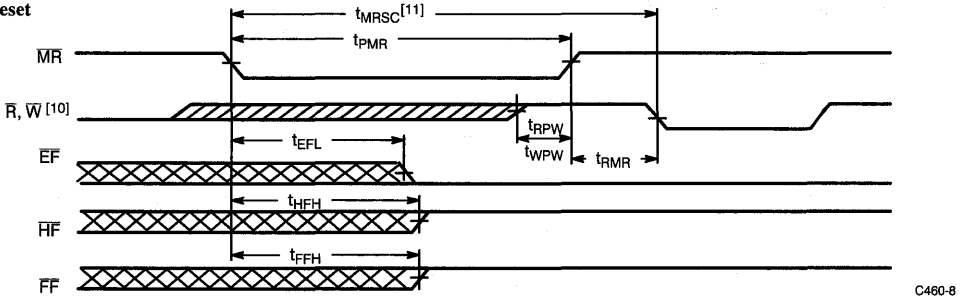
Parameter	Description	7C460–15 7C462–15 7C464–15		7C460–20 7C462–20 7C464–20		7C460–25 7C462–25 7C464–25		7C460–40 7C462–40 7C464–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Read LOW to $\overline{EF}$ LOW		15		20		25		40	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		15		20		25		40	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		15		20		25		40	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		15		20		25		40	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		25		30		35		50	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		25		30		35		50	ns
t_{RAE}	Effective Read from Write HIGH		15		20		25		40	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	15		20		25		40		ns
t_{WAF}	Effective Write from Read HIGH		15		20		25		40	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	15		20		25		40		ns
t_{XOL}	Expansion Out LOW Delay from Clock		15		20		25		40	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		35		35		50	ns

Switching Waveforms[9]

Asynchronous Read and Write



Master Reset

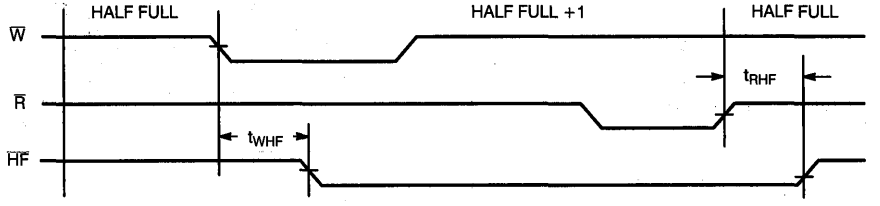


Notes:

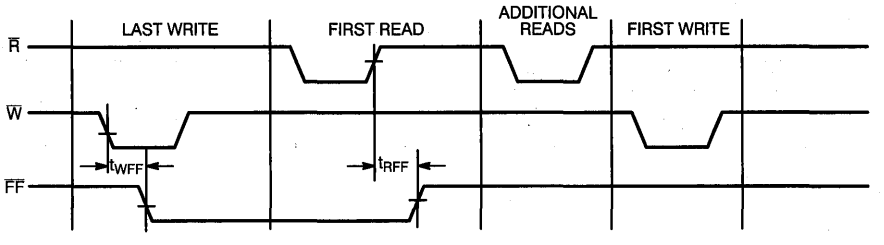
7. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load, unless otherwise specified.
8. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load.
9. A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a low-to-high strobe transition causes a LOW-to-HIGH flag transition.
10. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms

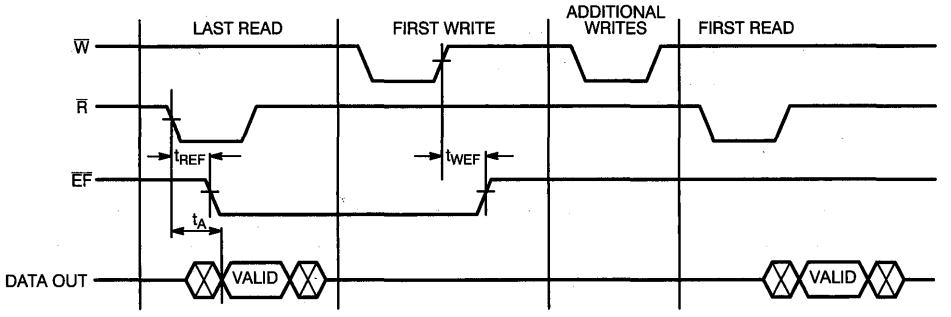
Half Full Flag



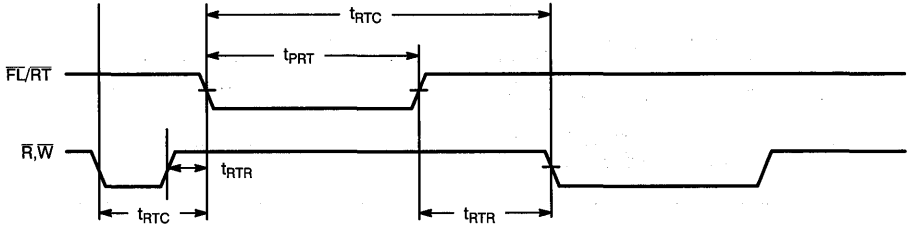
Last Write to First Read Full Flag



Last READ to First WRITE Empty Flag



Retransmit[12, 13]

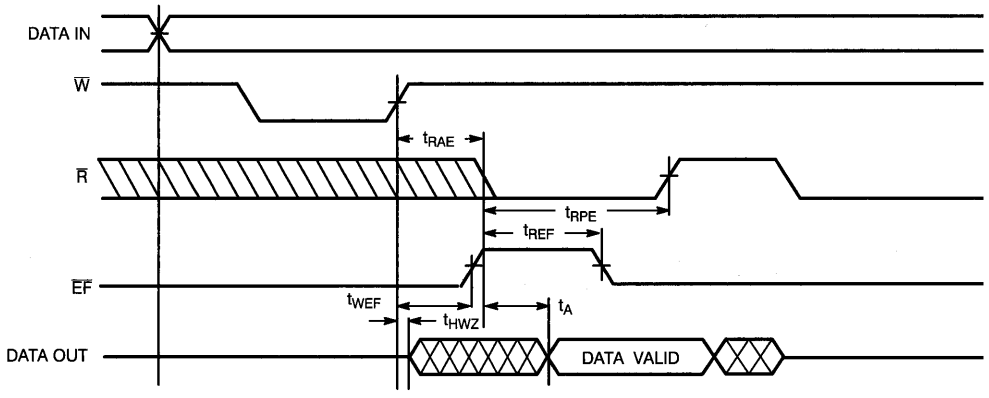


Notes:

12. $t_{RTC} = t_{PRT} + t_{RTR}$.
13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

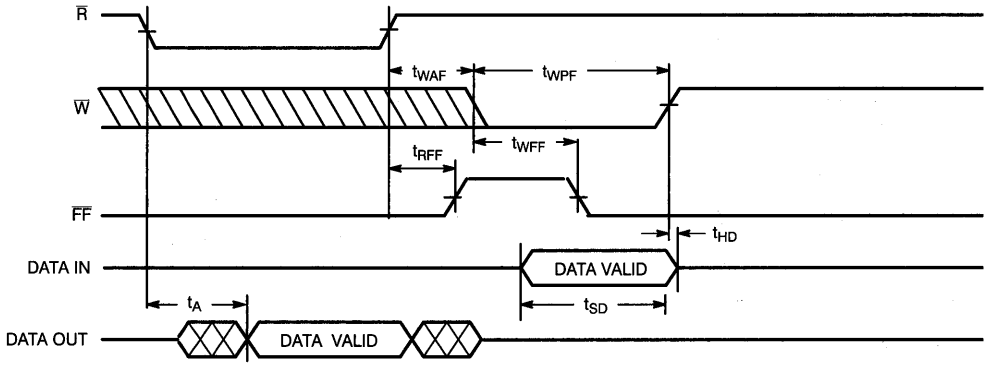
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



C460-13

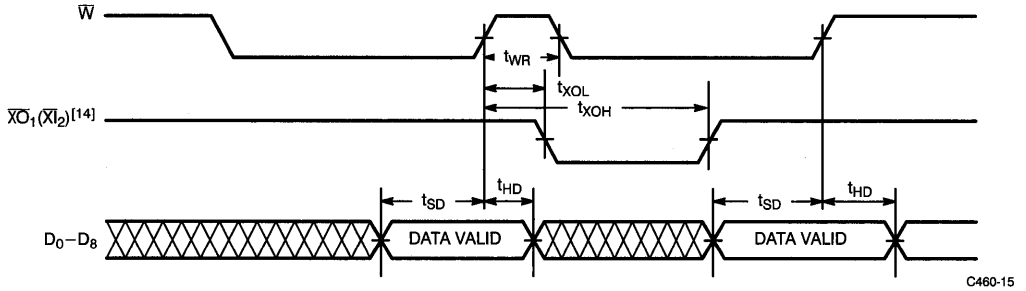
Full Flag and Write Data Flow-Through Mode

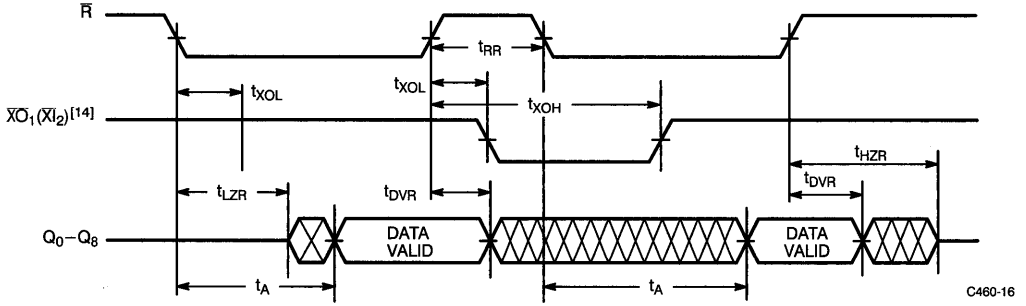


C460-14

Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
14. Expansion out of device 1 ($\overline{XO}_1$) is connected to expansion in of device 2 ($\overline{XI}_2$).

Architecture

Resetting the FIFO

Upon power up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$), and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs ($D_0 - D_8$) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being half full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs ($Q_0 - Q_8$) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal-to-or-less-than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer incremented until equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding expansion in ($\overline{XI}$) and tying first load ($\overline{FL}$) to V_{CC} prior to a $\overline{MR}$ cycle. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (*see Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode, the first load ($\overline{FL}$) input, when grounded, indicates that this is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created with word widths in increments of nine. When expanding in depth, a composite $\overline{FF}$ is created by ORing the $\overline{FF}$s together. Likewise, a compostie $\overline{EF}$ is created by ORing $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

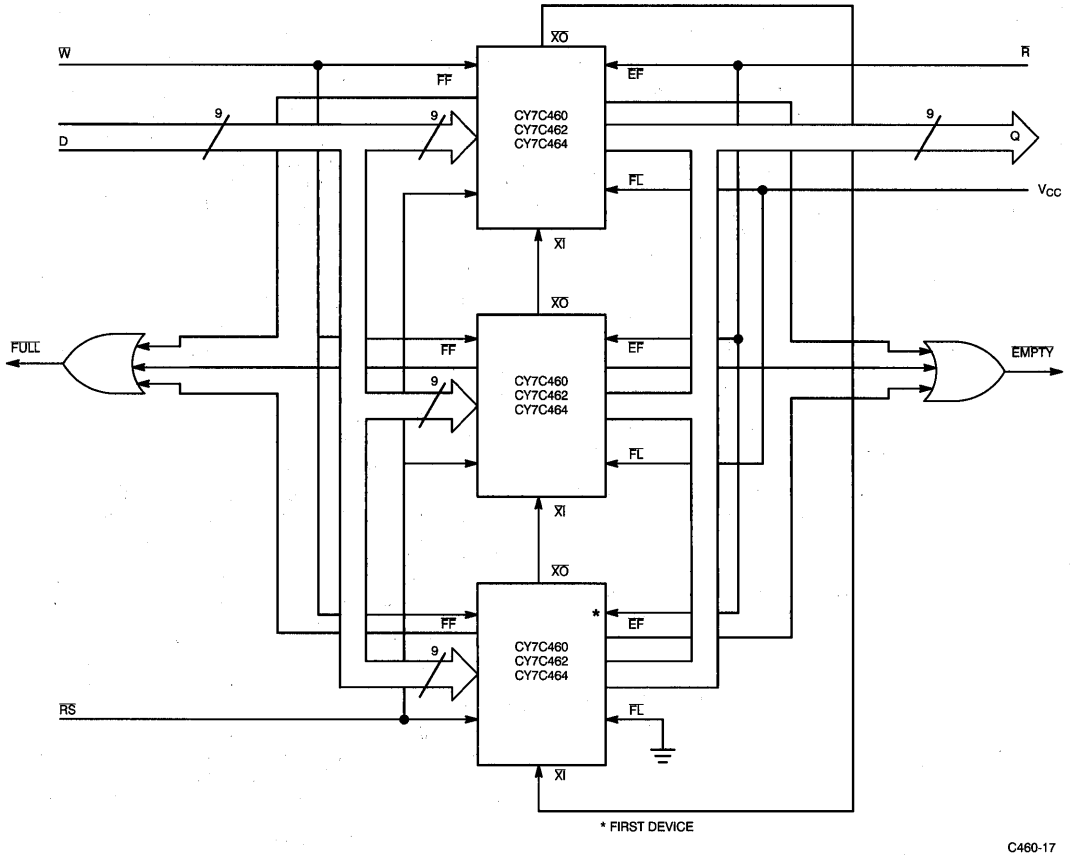


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C460-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C460-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C460-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C460-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C460-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C460-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C460-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C460-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C460–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C460-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C460-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C460-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C460-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C462-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C462-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C462-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C462-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C462-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C462-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C462-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C462-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C462-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C462-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C462-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C462-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C462-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C464-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C464-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C464-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C464-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C464-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C464-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C464-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C464-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464−25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C464−25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C464-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C464-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C464-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C464-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38–00141–D

CYPRESS SEMICONDUCTOR

PRELIMINARY

8K x 9 FIFO, 16K x 9 FIFO, 32K x 9 FIFO with Programmable Flags

Features

- **8K x 9, 16K x 9, and 32K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  - **I_{CC} (max.) = 160 mA (commercial)**
  - **I_{CC} (max.) = 165 mA (military)**
- **Programmable Almost Full/Empty flag**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable retransmit**
- **Expandable in width**
- **5V ± 10% supply**
- **TTL compatible**
- **Three-state outputs**
- **Proprietary 0.8-micron CMOS technology**

Functional Description

The CYC47X FIFO series consists of high-speed, low-power, first-in first-out (FIFO) memories with programmable flags and retransmit mark. The CY7C470, CY7C472, and CY7C474 are 8K, 16K, and 32K words by 9 bits wide, respectively. They are offered in 600-mil DIP, PLCC, and LCC packages. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Three status pins—Empty/Full ($\overline{E}/\overline{F}$), Programmable Almost Full/Empty ($\overline{PAFE}$), and Half Full ($\overline{HF}$)—are provided to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than Half Full, Greater than Half Full, Almost Full, and Full.

The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal goes LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go into a high-impedance state when $\overline{R}$ is HIGH.

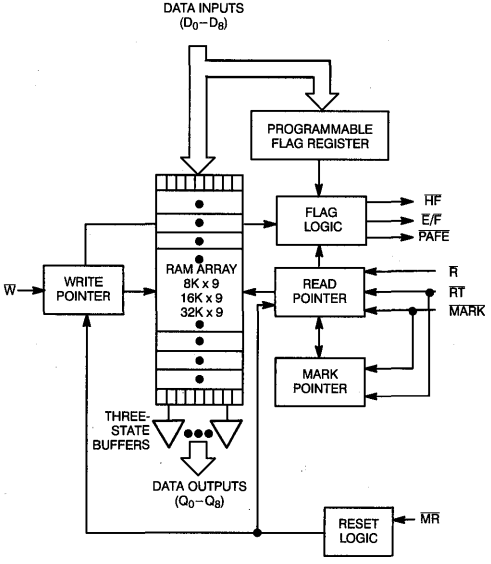
The user can store the value of the read pointer for retransmit by using the $\overline{MARK}$ pin. A LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend data by resetting the read pointer to the value stored in the mark pointer.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend the data. With the mark feature, retransmit can start from any word in the FIFO.

The CYC47X series is fabricated using a proprietary 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2001V and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

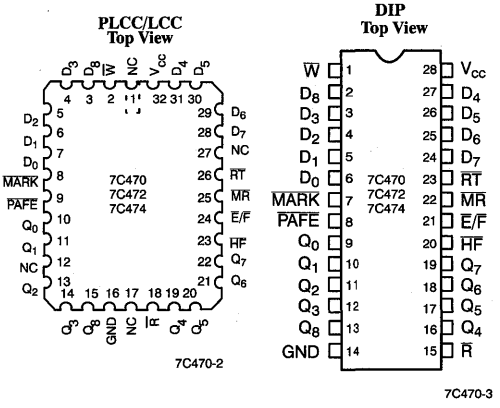
5 FIFOs

Logic Block Diagram



7C470-1

Pin Configurations



Selection Guide

		7C470–15 7C472–15 7C474–15	7C470–20 7C472–20 7C474–20	7C470–25 7C472–25 7C474–25	7C470–40 7C472–40 7C474–40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	160		145	125
	Military/Industrial		165	165	145

Maximum Ratings

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C470–15 7C472–15 7C474–15		7C470–20 7C472–20 7C474–20		7C470–25 7C472–25 7C474–25		7C470–40 7C472–40 7C474–40		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0				2.0		2.0		V
			Mil/Ind			2.2		2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		160				145		125	mA
			Mil[4]/Ind				165		165		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25		25	mA
			Mil/Ind				30		30		30	
I_{SB2}	Power-Down Current	All Inputs = V_{CC} – 0.2V	Com'l		20				20		20	mA
			Mil/Ind				25		25		25	
I_{OS}[5]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			–90		–90		–90		–90	mA

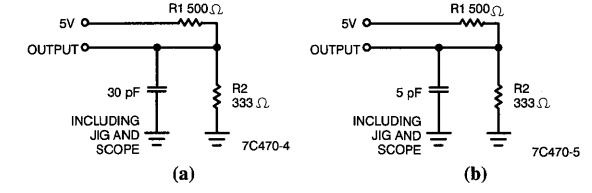
Notes:

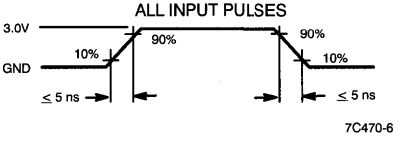
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 125 mA + (f – 20) • 2.5 mA/MHz for f ≥ 20 MHz
   where $\overline{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 130 mA + (f – 20) • 2.5 mA/MHz for f ≥ 20 MHz
   where $\overline{f}$ = the larger of the write or read operating frequency.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.

Capacitance[6]

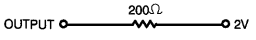
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7,8]

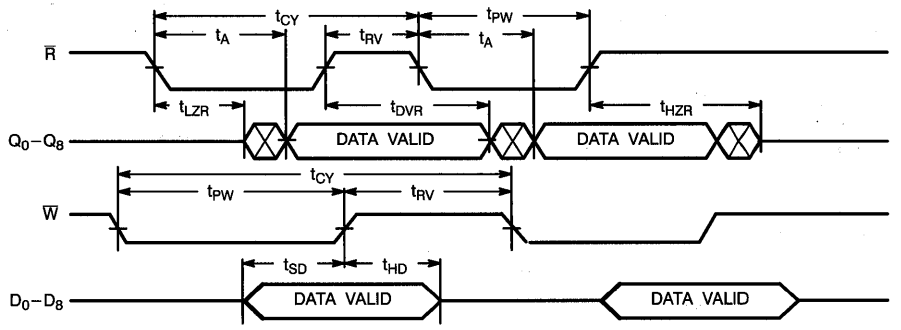
Parameter	Description	7C470–15 7C472–15 7C474–15		7C470–20 7C472–20 7C474–20		7C470–25 7C472–25 7C474–25		7C470–40 7C472–40 7C474–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	30		30		35		50		ns
t_A	Access Time		15		20		25		40	ns
t_{RV}	Recovery Time	10		10		10		10		ns
t_{PW}	Pulse Width	15		20		25		40		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[9]	Valid Data from Read HIGH	3		3		3		3		ns
t_{HZR}[9]	Read HIGH to High Z		15		15		18		25	ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		ns
t_{SD}	Data Set-Up Time	11		12		15		20		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{EFD}	$\overline{E}/\overline{F}$ Delay		15		20		25		40	ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		25		30		35		50	ns
t_{HFD}	$\overline{HF}$ Delay		25		30		35		50	ns
t_{AFED}	$\overline{PAFE}$ Delay		25		30		35		50	ns
t_{RAE}	Effective Read from Write HIGH	15		20		25		40		ns
t_{WAF}	Effective Write from Read HIGH	15		20		25		40		ns

Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads. t_{HZR} transition is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.

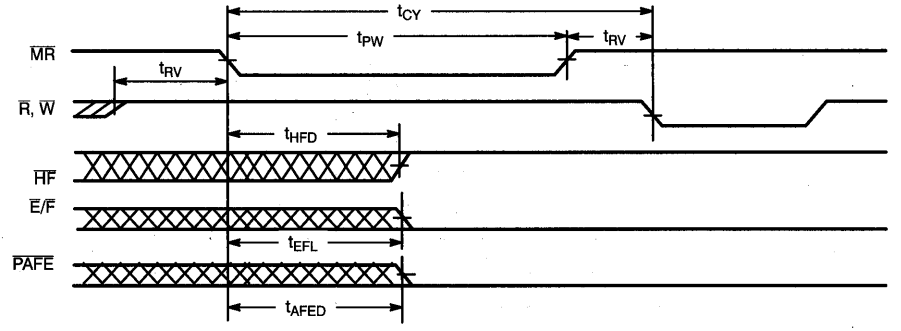
Switching Waveforms

Asynchronous Read and Write



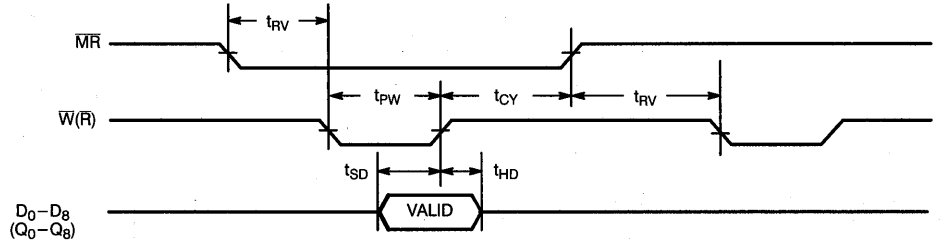
7C470-7

Master Reset (No Write to Programmable Flag Register)



7C470-8

Master Reset (Write to Programmable Flag Register)[10]

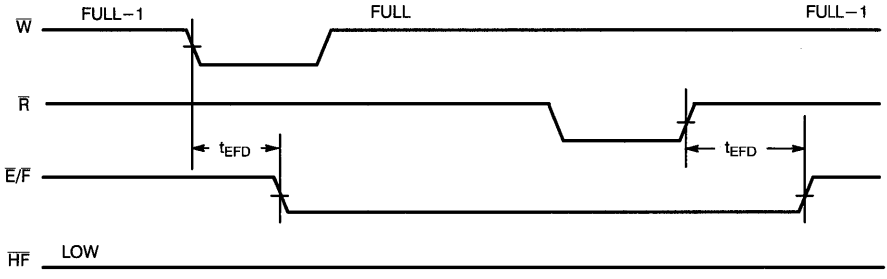


7C470-9

Note:
10. Waveform labels in parentheses pertain to writing the programmable flag register from the output port ($Q_0 - Q_8$).

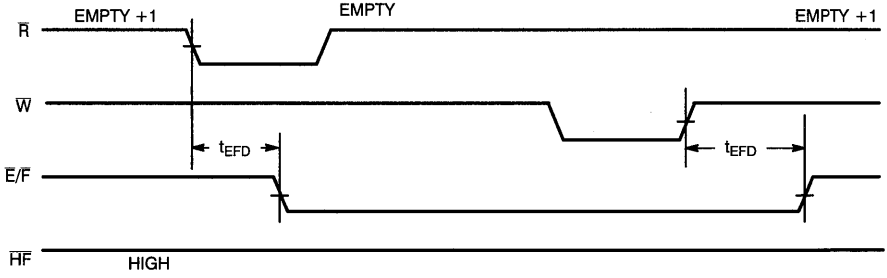
Switching Waveforms (continued)

$\overline{E}/\overline{F}$ Flag (Last Write to First Read Full Flag)



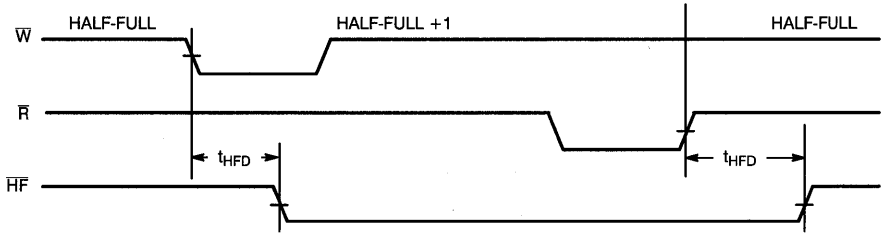
7C470-10

$\overline{E}/\overline{F}$ Flag (Last Read to First Write Empty Flag)



7C470-11

Half Full Flag

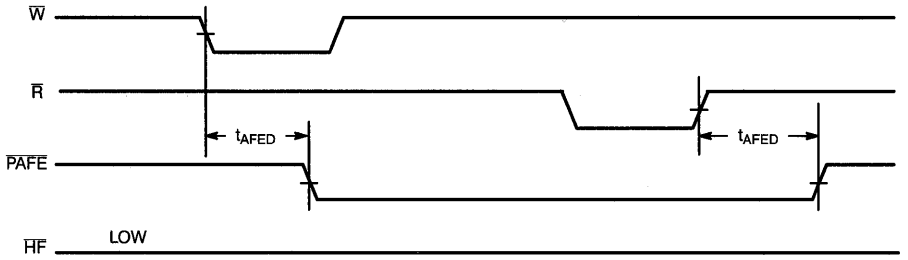


7C470-12

5 FIFOs

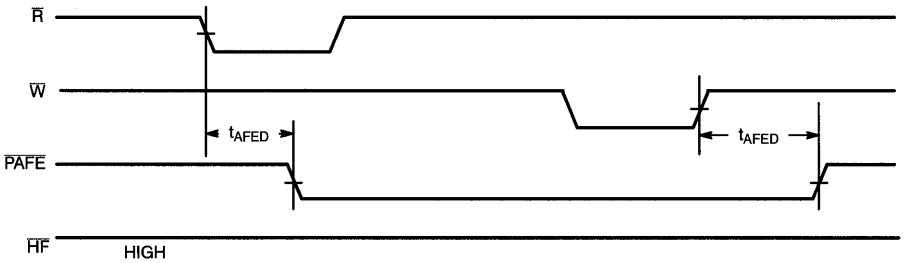
Switching Waveforms (continued)

$\overline{\text{PAFE}}$ Flag (Almost Full)



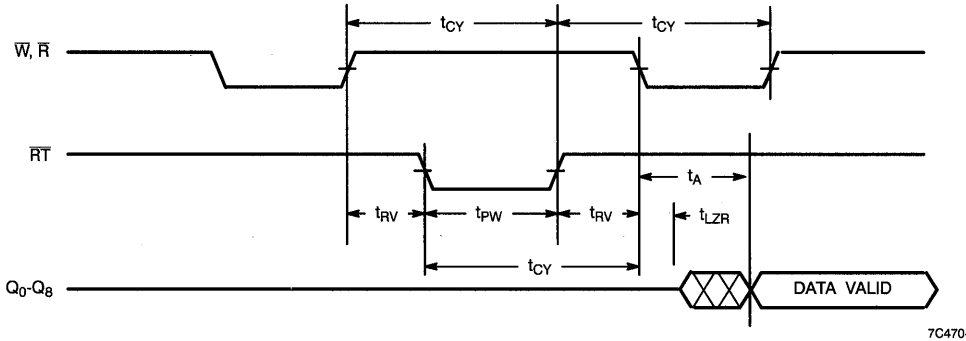
7C470-13

$\overline{\text{PAFE}}$ Flag (Almost Empty)



7C470-14

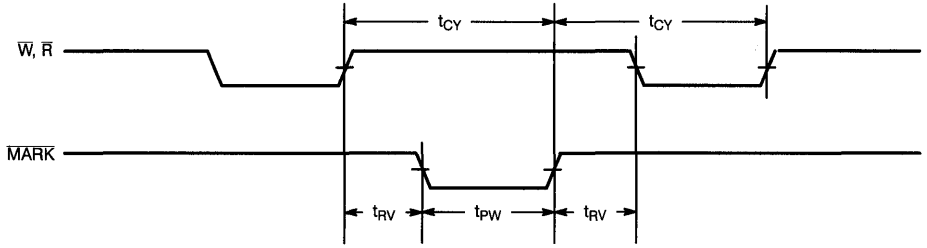
Retransmit



7C470-15

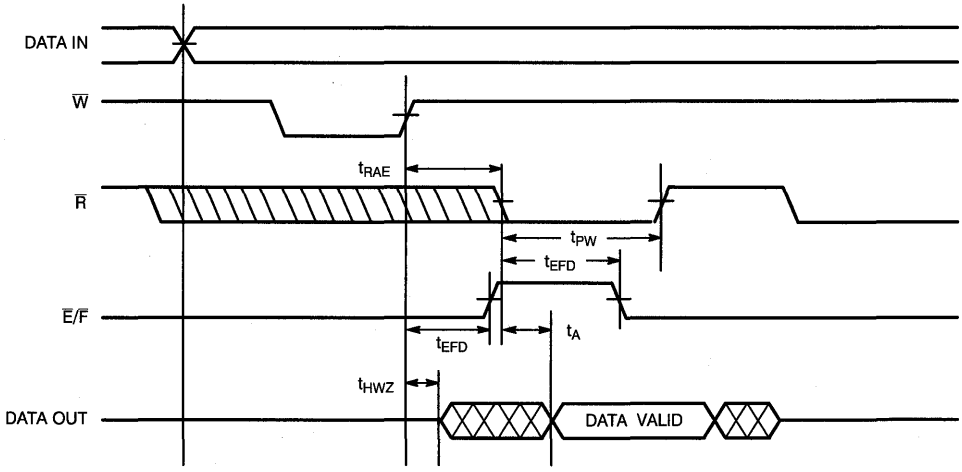
Switching Waveforms (continued)

Mark



7C470-16

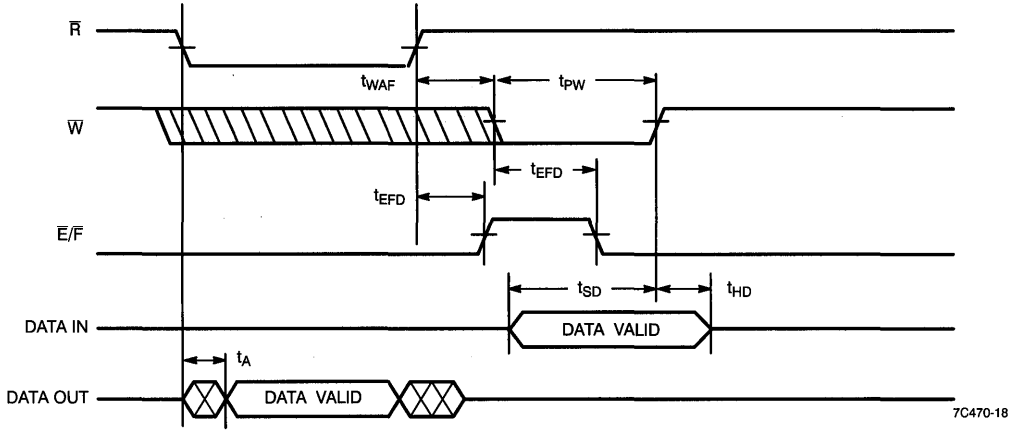
Empty Flag and Read Data Flow-Through Mode



7C470-17

Switching Waveforms (continued)

Full Flag and Write Data Flow-Through Mode



Architecture

The CY7C470, CY7C472, and CY7C474 FIFOs consist of an array of 8,192, 16,384, and 32,768 words of 9 bits each, respectively. The control consists of a read pointer, a write pointer, a retransmit pointer, control signals (i.e., write, read, mark, retransmit, and master reset), and flags (i.e., Empty/Full, Half Full, and Programmable Almost Full/Empty).

Resetting the FIFO

Upon power up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{E}/\overline{F}$) and Almost Full/Empty flag ($\overline{PAFE}$) being LOW, and Half Full flag ($\overline{HF}$) being HIGH. The read pointer, write pointer, and retransmit pointer are reset to zero. For a valid reset, read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before the falling edge and t_{RMR} after the rising edge of $\overline{MR}$.

Writing Data to the FIFO

Data can be written to the FIFO when it is not FULL[11]. A falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

Reading Data from the FIFO

Data can be read from the FIFO when it is not empty[12]. A falling edge of $\overline{R}$ initiates a read cycle. Data outputs (Q_0-Q_8) are in a high-impedance condition when the FIFO is empty and between read operations ($\overline{R}$ HIGH). The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a high-to-low transition of $\overline{E}/\overline{F}$, prohibiting any further read operations until t_{RFF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and resent if necessary. Retransmission can start from anywhere in the FIFO and be repeated without limitation.

The retransmit methodology is as follows: mark the current value of the read pointer, after an error in subsequent read operations return to that location and resume reading. This effectively resends all of the data from the mark point. When $\overline{MARK}$ is LOW, the current value of the read pointer is stored. This operation marks the beginning of the packet to be resent. When $\overline{RT}$ is LOW, the read pointer is updated with the mark location. During each subsequent read cycle, data is read and the read pointer incremented.

Care must be taken when using the retransmit feature. Use the mark function such that the write pointer does not pass the mark pointer, because further write operations will overwrite data.

Programmable Almost Full/Empty Flag

The CY7C470/2/4 offer a variable offset for the Almost Empty and the Almost Full condition. The offset is loaded into the programmable flag register (PFR) during a master reset cycle. While $\overline{MR}$ is LOW, the PFR can be loaded from Q_8-Q_0 by pulsing $\overline{R}$ LOW or from D_8-D_0 by pulsing $\overline{W}$ LOW. The offset options are listed in *Table 2*. See *Table 1* for a description of the six FIFO states. If the PFR is not loaded during master reset ($\overline{R}$ and $\overline{W}$ HIGH) the default offset will be 256 words from Full and Empty.

Notes:

11. When the FIFO is less than half full, the flags make a LOW-to-HIGH transition on the rising edge of $\overline{W}$ and make the HIGH-to-LOW transition on the falling edge of $\overline{R}$. If the FIFO is more than half full, the flags make the LOW-to-HIGH transition on the rising edge of $\overline{R}$ and HIGH-to-LOW transition on the falling edge of $\overline{W}$.
12. Full and empty states can be decoded from the Half-Full ($\overline{HF}$) and Empty/Full ($\overline{E}/\overline{F}$) flags.

Table 1. Flag Truth Table[13]

$\overline{HF}$	$\overline{E/F}$	$\overline{PAFE}$	State	CY77C470 (8K x 9) Number of Words in FIFO	CY77C472 (16K x 9) Number of Words in FIFO	CY77C474 (32K x 9) Number of Words in FIFO
1	0	0	Empty	0	0	0
1	1	0	Almost Empty	1 → (P − 1)	1 → (P − 1)	1 → (P − 1)
1	1	1	Less than Half Full	P → 4096	P → 8192	P → 16384
0	1	1	Greater than Half Full	4097 → (8192 − P)	8193 → (16384 − P)	16385 → (32768 − P)
0	1	0	Almost Full	(8192 − P+1) → 8191	(16384 − P+1) → 16383	(32768 − P+1) → 32767
0	0	0	Full	8192	16384	32768

Table 2. Programmable Almost Full/Empty Empty Options[14]

D3	D2	D1	D0	PAFE Active when:	P
0	0	0	0	256 or less locations from Empty/Full (default)	256
0	0	0	1	16 or less locations from Empty/Full	16
0	0	1	0	32 or less locations from Empty/Full	32
0	0	1	1	64 or less locations from Empty/Full	64
0	1	0	0	128 or less locations from Empty/Full	128
0	1	0	1	256 or less locations from Empty/Full (default)	256
0	1	1	0	512 or less locations from Empty/Full	512
0	1	1	1	1024 or less locations from Empty/Full	1024
1	0	0	0	2048 or less locations from Empty/Full	2048
1	0	0	1	4098 or less locations from Empty/Full[15]	4098
1	0	1	0	8192 or less locations from Empty/Full[16]	8192

Notes:
13. See *Table 2* for P values.
14. Almost flags default to 256 locations from Empty/Full.
15. Only for CY7C472 and CY7C474.
16. Only for CY7C470.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C470-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C470-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-15DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C470-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C470-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C470-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C470-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C470-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-25DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C470-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C470-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C470-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C470-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-40DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C470-40JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C470-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C470-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C472-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C472-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-15DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C472-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C472-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C472-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C472-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C472-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-25DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C472-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C472-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C472-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C472-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-40DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C472-40JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C472-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C472-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C474-15DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C474-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-15DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C474-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-15PI	P15	28-Lead (600-Mil) Molded DIP	
20	CY7C474-20DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C474-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C474-25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C474-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-25DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C474-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-25PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C474-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C474-40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C474-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-40DI	D16	28-Lead (600-Mil) CerDIP	Industrial
	CY7C474-40JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C474-40PI	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C474-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CY}	9, 10, 11
t_{A}	9, 10, 11
t_{RV}	9, 10, 11
t_{PW}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{EFD}	9, 10, 11
t_{HFD}	9, 10, 11
t_{AFED}	9, 10, 11
t_{RAE}	9, 10, 11
t_{WAF}	9, 10, 11

Document #: 38−00142−E

Section Contents

Logic

CY7C611A

CYPRESS SEMICONDUCTOR

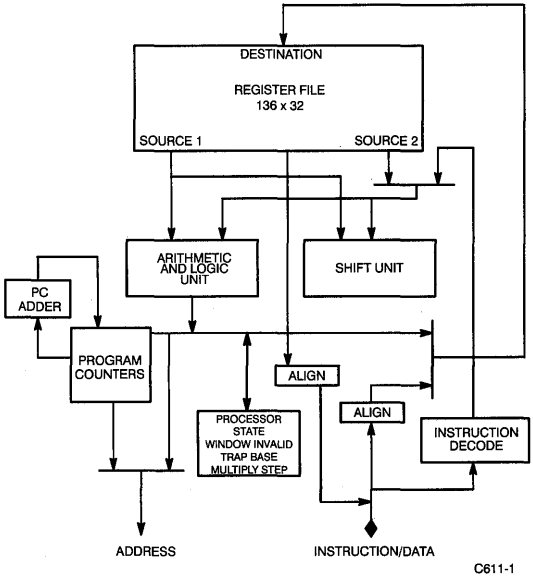
32-Bit RISC Controller

Features

- SPARC® processor optimized for embedded control applications
- Reduced Instruction Set Computer (RISC) architecture
  - Simple format instructions
  - Most instructions execute in a single cycle
- Very high performance
  - 40-ns instruction cycle with 4-stage pipeline
  - 18 sustained MIPS at 25 MHz
  - 240-ns worst-case interrupt response
- 136 32-bit registers
  - Eight overlapping windows of 24 registers each
  - Dividing registers into seperate register banks allows fast context switching
  - 8 global registers
- Hardware pipeline interlocks
- 16 prioritized interrupts levels
- Large address space
  - 24-bit address space
  - 3-bit address space indentifier
- Multitasking support
  - User/supervisor modes
  - Privileged instructions
- Artificial intelligence support
- Multiprocessing support
- High-performance floating-point processor interface
  - Concurrent execution of floating-point instructions
- 0.8-micron 2-layer metal CMOS technology
- 160-pin quad flat package
- Power
  - 3 watts maximum

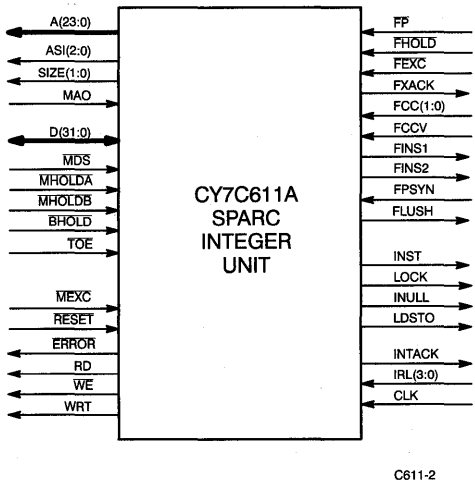
6 LOGIC

Logic Block Diagram



C611-1

Pin Configuration



C611-2

Selection Guide

		CY7C611A-25
Maximum Operating Current (mA)	Commercial	600

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Overview

The CY7C611A controller is a high-speed CMOS implementation of the SPARC 32-bit RISC architecture processor optimized for embedded control applications. RISC architecture makes possible the creation of a processor which can execute instructions at a rate of one instruction per processor clock. The CY7C611A supports a tightly-coupled floating-point coprocessor capable of executing at a rate of 4 to 5 MFLOPS. The CY7C611A SPARC controller provides the following features:

Simple instruction format. All instructions are 32 bits wide and aligned on 32-bit boundaries in memory. Three basic instruction formats feature uniform placement of opcode and address fields.

Register intensive architecture. Most instructions operate on either two registers or one register and a constant, and place the result in a third register. Only load and store instructions access off-chip memory.

Large windowed register file. The processor has 136 on-chip 32-bit general purpose registers. Eight of these are global registers. The remaining 128 registers can be configured as four separate non-overlapping register banks or as eight overlapping sets of 24 registers each. The first configuration allows for extremely fast context switch times and the second provides for very low overhead procedure calls. The actual configuration and use of the registers is determined by the user's application.

Delayed control transfer. The processor always fetches the next instruction after a control transfer, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after a delayed control transfer and thereby take better advantage of the processor pipeline.

Concurrent floating point. Floating-point instructions can execute concurrently with each other and with non-floating-point instructions.

Fast interrupt response. Interrupt inputs are sampled on every clock cycle and can be acknowledged in one to three cycles. The first instruction of an interrupt service routine can be executed within six to eight cycles of receiving the interrupt request.

The 7C600 Family

The SPARC processor family consists of the CY7C601A and CY7C611A integer units and the CY7C602A floating-point unit. The CY7C601A and CY7C611A integer units are a high-speed implementation of the SPARC architecture, and are binary compatible with all SPARC processors. The CY7C602A is a high-performance floating-point unit that allows floating-point instructions to execute concurrently with the CY7C601A or the CY7C611A.

The CY7C611A is designed for embedded control and application specific systems. The CY7C611A communicates with external memory via a 24-bit address bus and a 32-bit data/instruction bus. In many dedicated controller applications, the CY7C611A can function by itself with high-speed local memory. The CY7C611A retains the signals supplied on the CY7C601A for discrete implementations of cache systems. The CY7C157A cache storage unit can be used with the CY7C611A to provide a zero wait-state memory system with no glue logic. The CY7C289 registered PROM provides a zero wait-state PROM memory for most accesses and requires no glue logic for interfacing to the CY7C611A.

Floating-Point Coprocessor Interface

The CY7C611A is the basic processing engine which executes all of the instruction set except for floating-point operations. The CY7C602A and CY7C611A operate concurrently. The CY7C602A recognizes floating-point instructions and places them in a queue while the CY7C611A continues to execute non-floating point instructions. If the CY7C602A encounters an instruction which will not fit in its queue, the CY7C602A holds the CY7C611A until the instruction can be stored. The CY7C602A contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the CY7C611A via floating-point load/store instructions. Processor interlock hardware hides floating-point concurrency from the compiler or assembly language programmer. A program containing floating-point computations generates the same results as if instructions were executed sequentially.

Multitasking Support

The CY7C611A supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

Interrupts and Traps

The CY7C611A supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). The occurrence of a trap causes the CY7C611A to fetch the beginning address of the trap routine from a trap table. The base address of the trap table is specified by a trap base register and the offset is a function of the trap type. After fetching the trap routine address, program control jumps to the trap routine. Traps are taken before the current instruction is executed and can therefore be considered to occur between instructions.

Registers

The following sections provide an overview of the CY7C611A registers. The CY7C611A has two types of registers; working registers (r registers), and control registers. The r registers provide storage for processes, and the control registers keep track of and control the state of the CY7C611A.

Special r Registers. The utilization of four r registers is partially fixed by the instruction set. Global register r[0] is dummy register; it returns the value "0" when it is used as a source register, and it is not modified when used as a destination register. This feature makes the most common value easily available and eliminates the need for a clear register instruction. Another r register fixed by the instruction set is r[15]. Upon executing a CALL instruction, the address of the CALL instruction is written into r[15]. Upon entering a trap routine, registers r[17] and r[18] contain the PC and nPC.

r Register Addressing. r registers r8 through r31 are addressed internally using the register number and current window pointer (CWP) field of the processor status register (PSR; see next section). The CWP is essentially an index field for r register addressing, and acts as a pointer to a group of 24 registers. *Figure 1*

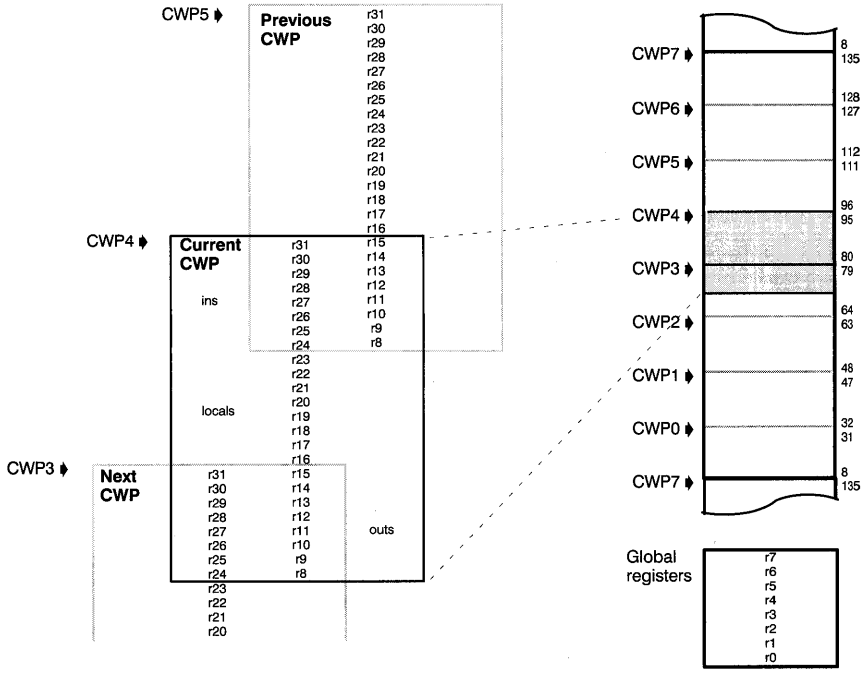


Figure 1. CWP Register Addressing

Registers (continued)

illustrates r register addressing using the CWP. Incrementing or decrementing the CWP changes the register offset by 16, thereby causing the register addressing to overlap by eight registers. Thisallows r24 through r31 of the current window to act as r8 through r15 of the previous window. Registers r0 through r7 do not use the CWP to address them, therefore they are global in nature.

The window invalid mask register (WIM) is used to disallow selected CWP values. Each bit of the least significant byte of the WIM register corresponds to a register window or CWP value. Incrementing or decrementing the CWP to a window invalidated by the WIM register causes the CY7C611A to cause a window underflow or window overflow trap. This is used in a register window environment to set the boundaries for software. The WIM register can also be used to set boundaries for register banks in a bank switching environment.

CY7C611A Control Registers. The CY7C611A's control registers contain various addresses and pointers used by the system to control its internal state. They include the program counters (PC and nPC), the processor state register (PSR), the window invalid mask register (WIM), the trap base register (TBR), and the Y register. The following paragraphs briefly describe each:

Processor Status Register (PSR). The processor status register contains fields that describe and control the state of the CY7C611A. *Figure 2* illustrates the bit assignments for the PSR.

IU Implementation and IU Version Numbers. These are read-only fields in the PSR. The version number is set to "0001" and the implementation number is set to binary "0011".

Integer Condition Codes. The integer condition codes consist of four flags: negative, zero, overflow, and carry. These flags are set by the conditions occurring during integer logic and arithmetic operations.

Enable Floating-Point Unit (EF bit). This bit is used to enable the floating-point unit. If a floating-point operation (FPop) is encountered and the EF bit is cleared (i.e., FPU disabled), a floating-point disabled trap is generated.

Processor Interrupt Level (PIL). This four bit field sets the CY7C611A interrupt level. The CY7C611A will only acknowledge interrupts greater than the level indicated by the PIL field. Bit 11 is the MSB; bit 8 is the LSB.

Supervisor Mode (S). S = 1 indicates that the CY7C611A is in supervisor mode. Supervisor mode can only be entered by a software or hardware trap.

Previous Supervisor Mode (PS). This bit indicates the state of the supervisor bit before the most recent trap.

Trap Enable (ET). This bit enables or disables the CY7C611A traps. This bit is automatically set to 0 (traps disabled) upon entering a trap. When ET = 0, all asynchronous traps are ignored.

If a synchronous trap occurs when ET = 0, the CY7C611A enters error mode.

Current Window Pointer (CWP). The r registers are addressed by the Current Window Pointer (CWP), a field of the Processor Status Register (PSR) that points to the 24 active local registers. It is incremented by a RESTORE instruction and decremented by a SAVE instruction. Note that the globals are always accessible regardless of the CWP. In the overlapping configuration each window shares its ins and outs with adjacent windows. The outs from a previous window (CWP +1) are the ins of the current window, and the outs from the current window are the ins for the next window (CWP −1). In both the windowed and register bank configurations globals are equally available and the locals are unique to each window.

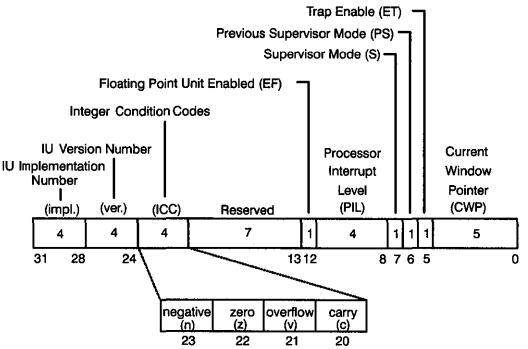


Figure 2. Processor State Register

Program Counters (PC and nPC). The program counter (PC) holds the address of the instruction being executed, and the next program counter (nPC) holds the address of the next instruction to be executed.

Trap Base Register (TBR). The trap base register contains the base address of the trap table and a field that provides a pointer into the trap table.

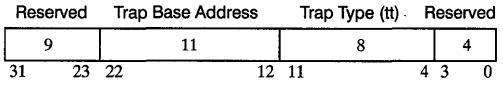


Figure 3. Trap Base Register

Window Invalid Mask Register (WIM). The window invalid mask register determines which windows are valid and which window accesses cause window_overflow and window_underflow traps.

Y register. The Y register is used to hold the partial product during execution of the multiply-step instruction (MULSCC).

Pin Description

The integer unit's external signals fall into three categories:

1. memory subsystem interface signals,
2. floating-point unit interface signals, and
3. miscellaneous I/O signals.

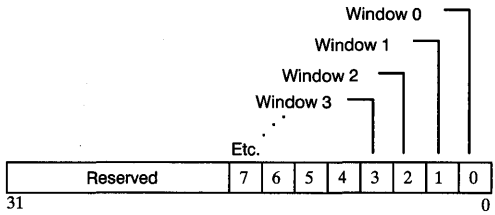


Figure 4. Window Invalid Mask

These are described in the following sections. Paragraphs after the tables describe each signal. Signals that are active LOW are marked with an overbar; all others are active HIGH. For example, $\overline{WE}$ is active LOW, while RD is active HIGH.

Memory Subsystem Interface Signals

The memory interface signals consist of 27 bits of address (24 bits of address and a three-bit address space identifier), 32 bits of bidirectional data lines, and two bits to identify the size (byte, halfword, word, or double word) of data bus transactions.

A[23:0]—These 24 bits are the addresses of instructions or data and they are sent out "unlatched" by the CY7C611A. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous (missed) address on the address bus. A[23:0] pins are three-stated if the $\overline{TOE}$ signal is deasserted.

ASI[2:0]—These three bits are the address space identifier for an instruction or data access to the memory. ASI[2:0] are sent out "unlatched" by the integer unit. The value on these pins during any given cycle is the address space identifier corresponding to the memory address on the A[23:0] pins at that cycle. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous address space identifier on the ASI[2:0] pins. ASI[2:0] pins are three-stated if the $\overline{TOE}$ signal is deasserted. Normally, the encoding of the ASI bits is as shown in *Table 1*. The remaining codes are software generated.

Table 1. ASI Bit Assignment

Address Space Identifier (ASI)	Address Space
000	User Instruction
010	User Data
001	Supervisor Instruction
011	Supervisor Data

D[31:0]—D[31:0] is the bidirectional data bus to and from the integer unit. The data bus is driven by the integer unit during the execution of integer store instructions and the store cycle of atomic load/store instructions. Similarly, the data bus is driven by the floating-point unit only during the execution of floating-point store instructions. The store data is sent out unlatched and must be latched externally before it is used. Once latched, store data is valid during the second data cycle of a store single access, the second and third data cycle of a store double access, and the third data cycle of an atomic load store access. The alignment for load and store instructions is done inside the processor. A double word is aligned on an eight-byte boundary, a word is aligned on a four-byte boundary, and a half word is aligned on a two-byte boundary. D(31) corresponds to the most significant bit of the least

significant byte of the 32-bit word. If a double-word, word, or half-word load or store instruction generates an improperly aligned address, a memory address not aligned trap will occur.

Memory Subsystem Interface Signals (continued)

Instructions and operands are always expected to be fetched from a 32-bit wide memory.

SIZE[1:0]. These two bits specify the data size associated with a data or instruction fetch. Size bits are sent out "unlatched" by the CY7C611A. The value on these pins at any given cycle is the data size corresponding to the memory address on the A[23:0] pins in that cycle. SIZE[1:0] remains valid on the bus during all data cycles of loads, stores, load_doubles, store_doubles and atomic load stores. Since all instructions are 32-bits long, SIZE[1:0] is set to "10" during all instruction fetch cycles. Encoding of the SIZE[1:0] bits is shown in *Table 2*.

Table 2. Size Bit Assignment

SIZE1	SIZE0	Data Transfer Type
0	0	Byte
0	1	Halfword
1	0	Word
1	1	Word (Load/Store Double)

$\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$. The processor pipeline will be frozen while $\overline{\text{MHOLDA}}$ is asserted and the CY7C611A outputs will revert to and maintain the value they had at the rising edge of the clock in the cycle before $\overline{\text{MHOLDA}}$ was asserted. $\overline{\text{MHOLDA}}$ is used to freeze the clock to both the integer and floating-point units during a cache miss (for systems with cache) or when a slow memory is accessed. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock. Either $\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$ can be used for stopping the processor during a cache miss or memory exception. $\overline{\text{MHOLDB}}$ has the same definition as $\overline{\text{MHOLDA}}$. The processor hardware uses the logical "OR" of all hold signals (i.e., $\overline{\text{MHOLDA}}$, $\overline{\text{MHOLDB}}$, and $\overline{\text{BHOLD}}$) to generate a final hold signal for freezing the processor pipeline. All HOLD signals are latched (transparent latch) in the CY7C611A before they are used.

$\overline{\text{BHOLD}}$. $\overline{\text{BHOLD}}$ is asserted by the I/O controller when an external bus master requests the data bus. Assertion of this signal will freeze the processor pipeline. External logic should guarantee that after deassertion of $\overline{\text{BHOLD}}$, the data at all inputs to the chip is the same as what it was before $\overline{\text{BHOLD}}$ was asserted. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock since the CY7C611A processes the $\overline{\text{BHOLD}}$ input through a transparent latch before it is used. $\overline{\text{BHOLD}}$ should be used only for bus access requests by an external device since the $\overline{\text{MDS}}$ and $\overline{\text{MEXC}}$ signals are not recognized while this input is active. $\overline{\text{BHOLD}}$ should not be deasserted while LOCK is asserted.

$\overline{\text{MDS}}$. Assertion of this signal will enable the clock input to the on-chip instruction register (during an instruction fetch) or to the load result register (during a data fetch). In a system with cache, $\overline{\text{MDS}}$ is used to signal the processor when the missed data (cache miss) is ready on the bus. In a system with slow memories, $\overline{\text{MDS}}$ is used to signal the processor when the read data is available on the bus. $\overline{\text{MDS}}$ must be asserted only while the processor is frozen by either the $\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$ input signals. The CY7C611A samples the $\overline{\text{MDS}}$ signal via an on-chip transparent latch before it is used. The $\overline{\text{MDS}}$ signal is also used for strobing memory exceptions. In other words, $\overline{\text{MDS}}$ should be asserted whenever $\overline{\text{MEXC}}$ is asserted (see $\overline{\text{MEXC}}$ definition).

$\overline{\text{MEXC}}$. This signal is asserted by the memory (or cache) controller to initiate an instruction (or data) exception trap. $\overline{\text{MEXC}}$ is latched in the processor at the rising edge of CLK and is used in the following cycle. If $\overline{\text{MEXC}}$ is asserted during an instruction fetch cycle, an instruction access exception is generated, and if $\overline{\text{MEXC}}$ is asserted during a data fetch cycle, a data access exception trap is generated. The $\overline{\text{MEXC}}$ signal is used during ($\overline{\text{MHOLD}}$) in conjunction with the $\overline{\text{MDS}}$ signal to indicate to the CY7C611A that the memory system was unable to supply valid instruction or data. If $\overline{\text{MDS}}$ is applied without $\overline{\text{MEXC}}$, the CY7C611A accepts the contents of the data bus as valid information, but when $\overline{\text{MDS}}$ is applied with $\overline{\text{MEXC}}$ an exception trap is generated and the contents of the data bus is ignored by the CY7C611A. (In other words, $\overline{\text{MHOLD}}$ and $\overline{\text{MDS}}$ must be LOW when $\overline{\text{MEXC}}$ is asserted.) $\overline{\text{MEXC}}$ must be deasserted in the same clock cycle in which $\overline{\text{MHOLD}}$ is released.

RD. This signal specifies whether the current memory access is a read or write operation. It is sent out "unlatched" by the integer unit and must be latched externally before it is used. RD is set to "0" only during address cycles of store instructions including the store cycles of atomic load store instructions. This signal, when used in conjunction with SIZE[1:0] and LDSTO, can be used to check access rights of bus transactions. In addition, the RD signal may be used to turn off the output drivers of data RAMs during a store operation. For atomic load store instructions the RD signal is "1" during the first address cycle (read cycle), and "0" during the second and third address cycles (write cycle).

$\overline{\text{WE}}$. This signal is asserted by the integer unit during the second address cycle of store single instructions, the second and third address cycles of store double instructions, and the the third data cycle of atomic load/store instructions. The $\overline{\text{WE}}$ signal is sent out "unlatched" and must be latched externally before it is used. The $\overline{\text{WE}}$ signal may be externally qualified by HOLD signals (i.e., $\overline{\text{MHOLDA}}$ and $\overline{\text{MHOLDB}}$) to avoid writing into the memory during memory exceptions.

WRT. This signal is asserted (set to "1") by the processor during the first address cycle of single or double integer store instructions, the first data cycle of single or double floating-point store instructions, and the second data cycle of atomic load/store instructions. WRT is sent out "unlatched" and must be latched externally before it is used.

LDSTO. This signal is asserted by the integer unit during the data cycles of atomic load store operations. LDSTO is sent out "unlatched" by the integer unit and must be latched externally before it is used.

LOCK. This signal is set to "1" when the processor needs the bus for multiple cycle transactions such as atomic load/store, double loads and double stores. The LOCK signal is sent "unlatched" and should be latched externally before it is used. The bus may not be granted to another bus master as long as the LOCK signal is asserted (i.e., $\overline{\text{BHOLD}}$ should not be asserted in the following processor clock cycle when LOCK=1).

INULL. Assertion of INULL indicates that the current memory

Memory Subsystem Interface Signals (continued)

access (whose address is held in an external latch) is to be nullifiedby the processor. INULL is intended to be used to disable cachemisses (in systems with cache) and to disable memory exception generation for the current memory access (i.e., $\overline{MDS}$ and $\overline{MEXC}$ should not be asserted for a memory access when INULL=1). INULL is a latched output and is active during the same cycle as the address which it nullifies. INULL is asserted under the following conditions: During the second cycle of a store instruction, or whenever the CY7C611A address is invalid due to an external or internal exception. If a floating-point unit or coprocessor unit is present in the system INULL should be ORed with the FNULL and CNULL signals from these units.

Floating-Point Interface Signals

The floating-point/coprocessor unit interface is a dedicated group of connections between the CY7C611A and the CY7C602A. Note that no external circuits are required between the CY7C611A and the CY7C602A; all traces should connect directly. The interface consists of the following signals:

$\overline{FP}$. This signal indicates whether or not a floating-point unit exists in the system. The $\overline{FP}$ signal is normally pulled up to VDD by a resistor. It is grounded when the CY7C602A chip is present. The integer unit generates a floating-point disable trap if $\overline{FP}$ = 1 during the execution of a floating-point instruction, FBfcc instruction or floating-point load and store instructions.

FCC[1:0]. These bits are taken as the current condition code bits of the CY7C602A. They are considered valid if FCCV=1. During the execution of the FBfcc instruction, the processor uses these bits to determine whether the branch should be taken or not. FCC[1:0] are latched by the processor before they are used.

FCCV. This signal should be asserted only when the FCC[1:0] bits are valid. The floating-point unit deasserts FCCV if pending floating-point compare instructions exist in the floating-point queue. FCCV is reasserted when the compare instruction is completed and the floating-point condition codes FCC[1:0] are valid. The integer unit will enter a wait state if FCCV is deasserted (i.e., FCCV = "0"). The FCCV signal is latched (transparent latch) in the CY7C611A before it is used.

$\overline{FHOLD}$. This signal is asserted by the floating-point unit if a situation arises in which the CY7C602A cannot continue execution. The floating-point unit checks all dependencies in the Decode stage of the instruction and asserts $\overline{FHOLD}$ (if necessary) in the next cycle. This signal is used by the integer unit to freeze the instruction pipeline in the same cycle. The CY7C602A must eventually deassert $\overline{FHOLD}$ in order to unfreeze the integer unit's pipeline. The $\overline{FHOLD}$ signal is latched (transparent latch) in the CY7C611A before it is used.

$\overline{FEXC}$. Assertion of this signal indicates that a floating-point exception has occurred. $\overline{FEXC}$ must remain asserted until the integer unit takes the trap and acknowledges the CY7C602A via FXACK signal. Floating-point exceptions are taken only during the execution of floating-point instructions, FBfcc instruction and floating-point load and store instructions. $\overline{FEXC}$ is latched in the integer unit before it is used. The CY7C602A should deassert $\overline{FHOLD}$ if it detects an exception while $\overline{FHOLD}$ is asserted. In this case $\overline{FEXC}$ should be asserted a cycle before $\overline{FHOLD}$ is deasserted.

INST. This signal is asserted by the integer unit whenever a new instruction is being fetched. It is used by the CY7C602A to latch the instruction on the D[31:0] bus into the CY7C602A instruction buffer. The CY7C602A needs two instruction buffers (D1 and D2) to save the last two fetched instructions. When INST is asserted a new instruction enters into the D1 buffer and the old instruction in D1 enters into the D2 buffer.

FLUSH. This signal is asserted by the integer unit and is used by the CY7C602A to flush the instructions in its instruction registers. This may happen when a trap is taken by the integer unit. Instructions that have entered into the floating-point queue may continue their execution if FLUSH is raised as a result of a trap or exception other than floating-point exceptions.

FINS1. This signal is asserted by the integer init during the decode stage of a CY7C602A instruction if the instruction is in the D1 buffer of the CY7C602A chip. The CY7C602A uses this signal to latch the instruction in D1 buffer into its execute stage instruction register.

FINS2—This signal is asserted by the integer unit during the decode stage of a CY7C602A instruction if the instruction is in the D2 buffer of the CY7C602A chip. The CY7C602A uses this signal to latch the instruction in D2 buffer into its execute stage instruction register.

FXACK—This signal is asserted by the integer unit in order to acknowledge to the CY7C602A that the current $\overline{FEXC}$ trap is taken. The CY7C602A must deassert $\overline{FEXC}$ after it receives an asserted level of FXACK signal so that the next floating-point instruction does not cause a "repeated" floating-point exception trap.

Miscellaneous I/O Signals

These signals are used by the CY7C611A to control external events or to receive input from external events. This interface consists of the following signals:

IRL[3:0]. The data on these pins defines the external interrupt level. IRL[3:0]=0000 indicates that no external interrupts are pending. The integer unit uses two on-chip synchronizing latches to sample these signals on the rising edge of CLK. A given interrupt level must remain valid for at least two consecutive cycles to be recognized by the integer unit. IRL[3:0]=1111 signifies an non-maskable interrupt. All other interrupt levels are maskable by the PIL field of the Processor State Register (PSR). External interrupts should be latched and prioritized by the external logic before they are passed to the integer unit. The external interrupt latches should keep the interrupts pending until they are taken (and acknowledged) by the integer unit. External interrupts can be acknowledged by software or by the Interrupt Acknowledge (INTACK) output.

INTACK—This signal is asserted by the integer unit when an external interrupt is taken.

$\overline{RESET}$—Assertion of this pin will reset the integer unit. The $\overline{RESET}$ signal must be asserted for a minimum of eight processor clock cycles. After a reset, the integer unit will start fetching from address 0. The $\overline{RESET}$ signal is latched by the integer unit before it is used.

$\overline{ERROR}$—This signal is asserted by the integer unit when a trap is encountered while traps are disabled via the ET bit in the PSR.

Miscellaneous I/O Signals (continued)

In this situation the integer unit saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state, asserts the $\overline{\text{ERROR}}$ signal and then halts. The only way to restart the processor trapped in the error state, is to trigger a reset by asserting the $\overline{\text{RESET}}$ signal.

$\overline{\text{TOE}}$—This signal is used to force all output drivers of the processor chip into a high-impedance state. It is used to isolate the chip from the rest of the system for debugging purposes. *This pin should be tied LOW for normal operation.*

FPSYN—This pin is a mode pin which is used to allow execution of additional instructions in future designs. It should be normally kept deasserted (FPSYN=0) to disable the execution of these instructions.

Document #: 38-R-10003-A

CLK—CLK is a 50% duty-cycle clock used for clocking the CY7C611A's pipeline registers. It is HIGH during the first half of the processor cycle, and LOW during the second half. The rising edge of CLK defines the beginning of each pipeline stage in the CY7C611A chip.

Features

- **1024 x 42 fully associative processor**
- **1024 single-bit ALUs; one ALU per CAM entry**
- **User-friendly instruction set**
- **Binary and Quad compare modes**
- **Supports "don't care" and "never match" states**
- **Match length expandable in 42-bit entry increments**
- **32-bit data bus**
- **Full cascade support**
- **80-pin PQFP, 68-pin PLCC**
- **Advanced CMOS process**

Functional Overview

The CY7C915 SmartCAM is a high-performance associative processor. It consists of a 1024 x 42 CAM array and a Row Logic section containing 1024 single-bit ALUs. Under program control, data patterns supplied by external logic via the 32 data lines are compared against the contents of the CAM array. The match result is then processed by the ALUs in the Row Logic. Individual bit positions in the data pattern can be removed from the match process by setting the corresponding bits in the mask pattern. Mask patterns can be supplied externally or generated on-chip.

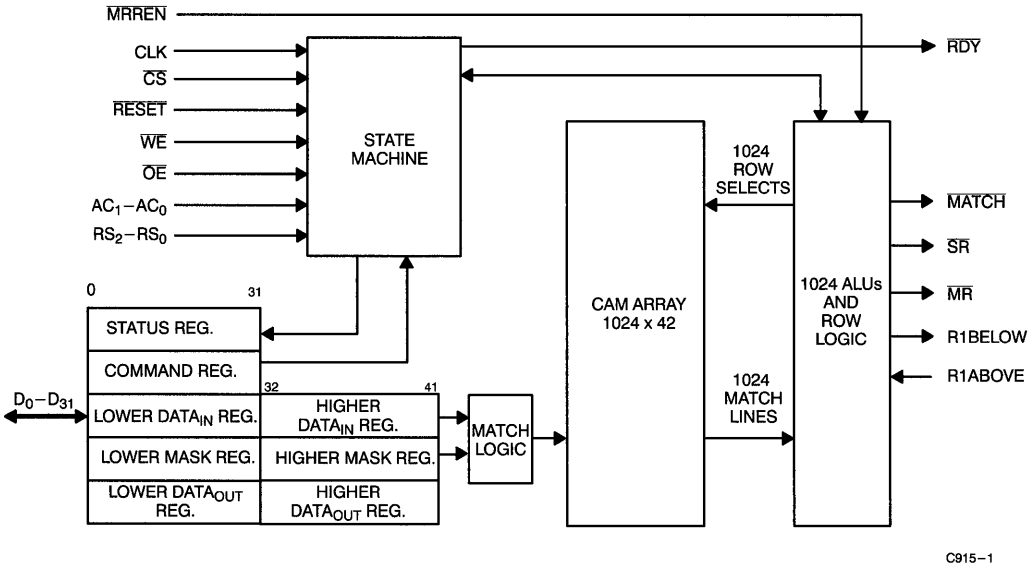
Two types of matches are supported by the CY7C915: binary match and quad match. In a binary match, the contents of the CAM array is compared against the external data pattern on a bit-by-bit basis. In a quad match, the 42 bits in each CAM entry are paired to form 21 quad values. The four states in a quad value are logic one, logic zero, don't care, and never match. These quad values are compared against quad-value patterns from external logic.

If the data pattern is longer than 42 bits, multiple adjacent CAM entries can be linked to form a multiword storage unit. On-chip logic supports multiword match and collation.

Twelve instructions are supported. They control operations such as match, read/write CAM entries, and data flow within a SmartCAM, as well as data flow between cascaded SmartCAMs.

The CY7C915 is designed for data-intensive applications such as pattern recognition, database systems, neural networks, text processing, and digital noise suppression.

Logic Block Diagram



SmartCAM is a trademark of Cypress Semiconductor Corporation.

Functional Description

Communications between the CY7C915 SmartCAM and external logic are conducted via the 32 data lines. Data patterns supplied externally are stored in the $Data_{IN}$ register before they are compared against the contents of the CAM array. If a match is detected, the $\overline{MATCH}$ output will be asserted. In case multiple matches are found, the Multiple Response ($\overline{MR}$) output will be asserted as well. An on-chip Multiple Response Resolver (MRR) prioritizes all matched CAM entries and points to the first matched location.

Individual bit positions of the externally supplied data pattern can be removed from the match process by setting the corresponding bit positions in the Mask register. Bits set HIGH in the Mask register force a match between corresponding bits in the $Data_{IN}$ register and the CAM array. During CAM update operations, the same Mask register can be used to specify which of the 42 columns in the CAM array are to be updated. Besides writing externally generated mask patterns into the Mask register, the user can select internally generated mask patterns via the "Msksrc" field of the instruction.

After a match operation, the 1024 match results (one from each CAM entry) can be stored in one of three 1024-bit-long Response registers in the row logic function block. These registers are labelled as R1, R2, and R3. R1 is a multipurpose register. Besides being a storage for match results, R1 also serves as the input register feeding the MRR, as well as the chip-wide bidirectional shift register. Cascading multiple SmartCAMs is accomplished by connecting the top-most and the bottom-most bits of R1 to the upper and lower devices in the cascade chain, respectively. Response registers R2 and R3 are used to store match results only.

The CY7C915 SmartCAM contains 1024 single-bit ALUs. The contents of the three Response registers are inputs to the ALUs. Each ALU is capable of performing 256 Boolean operations on the three sets of inputs and storing the processed data back into one of the Response registers. The Boolean operation to be performed is selected by the 8-bit "GPLBterms" field in the instruction.

Two types of matches are supported: binary match and quad match. In a binary match, the binary contents of the CAM array are compared against the contents of the $Data_{IN}$ register on a bit-by-bit basis. Bit positions masked out by the mask pattern are not compared. In a quad match, the 42 bits in each CAM entry are paired up to form 21 quad values. The four states in each quad value are zero (0), one (1), don't care (X), and never match (N). In a similar manner, the contents of the $Data_{IN}$ register and the Mask register are encoded into 21 quad values. *Table 1* illustrates how the quad values are matched against each other; a 1 indicates a match, a 0 indicates a miss. Note that a don't care (X) can match any value, while a never match (N) will match only don't cares.

Table 1. Truth Table

	0	1	X	N
0	1	0	1	0
1	0	1	1	0
X	1	1	1	1
N	0	0	1	0

Instructions

Twelve instructions are supported in the CY7C915.

Match: Starts a compare operation.

Move: Copies data from one location to another.

Read: Moves the contents of the selected CAM entry into the $Data_{OUT}$ register or to the 32 data lines.

Readshift: Moves the contents of the selected CAM entry into the $Data_{OUT}$ register or to the 32 data lines. After the data move, the contents of R1 are shifted one bit position in the direction specified in the instruction.

Readsnext: Moves the contents of the selected CAM entry into the $Data_{OUT}$ register or to the 32 data lines. After the data move, the top-most non-zero entry in R1 is reset to zero.

Shift: The contents of R1 are shifted one bit position in the direction specified in the instruction.

Snext: The top-most non-zero entry in R1 is reset to zero.

Write: The data in the specified source is written into the selected CAM entry.

Writeshift: The data in the specified source is written into the selected CAM entry. After the write, the contents of R1 are shifted one bit position in the direction specified in the instruction.

Writesnext: The data in the specified source is written into the selected CAM entry. After the write, the top-most non-zero entry in R1 is reset to zero.

Writecol: A column in the selected CAM entry is loaded with data from a source specified in the instruction.

NOP: No operation.

Instruction Format

The 32-bit instruction contains 11 fields (see *Figure 1*).

Opcode: Selects one of the twelve instructions.

Respreg: Selects one of the three response registers.

Selvect: Specifies the pointer into the CAM array for reads and writes.

Datasrc: Specifies the data source for writing and matching.

Msksrc: Specifies the mask source for writing and matching.

Dir: Specifies the direction of the shift operation.

GPLBterms: An 8-bit field selecting 1 of the 256 Boolean operations to be performed.

Mpat: Selects one of the two types of internally generated mask patterns.

Mpatbit: Location control bit for the internally generated mask patterns.

Bitpos: Pattern control bits for the internally generated mask patterns.

Resv: Reserved for future use.

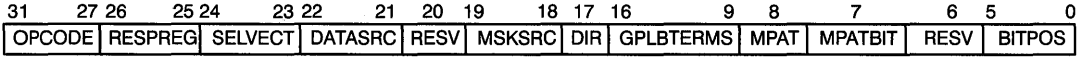


Figure 1. Instruction Format

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		CY7C915 Min.	CY7C915 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 3.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 6.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	Vcc +0.3	V
V_{IL}	Input LOW Voltage			– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			TBD	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		TBD	mA
			Mil			
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		TBD	mA
			Mil			

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	TBD	pF
C_{OUT}	Output Capacitance		TBD	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Document #: 38–00206

Programmable Skew Clock Buffer (PSCB)

Features

- **Output pair skew <100 ps typical (250 max.)**
- **All outputs skew <250 ps typical (500 max.)**
- **3.75- to 80-MHz output operation**
- **User-selectable output functions**
  - **— Selectable skew to 18 ns**
  - **— Inverted and non-inverted**
  - **— Operation at ½ and ¼ input frequency**
  - **— Operation at 2x and 4x input frequency (input as low as 3.75 MHz)**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **32-pin PLCC/LCC package**
- **Jitter < 0.5% peak to peak**
- **Compatible with the Pentium™ processor**

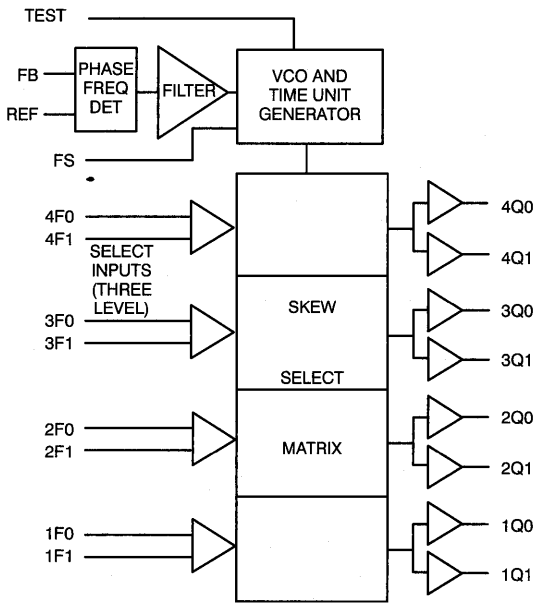
Functional Description

The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user-selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this "zero delay" capability of the PSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

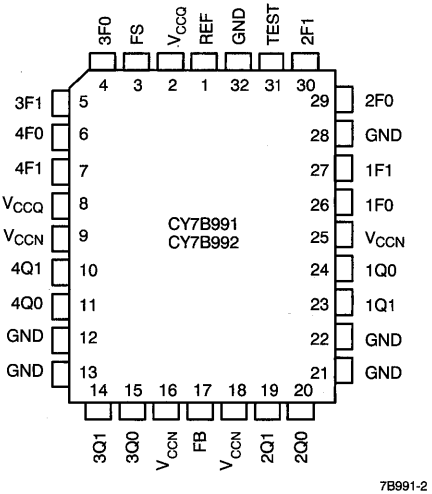
Logic Block Diagram



7B991-1

Pin Configuration

PLCC/LCC



7B991-2

Pentium is a trademark of Intel Corporation.

Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three-level frequency range select. See *Table 1.*
1F0, 1F1	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See *Table 2.*
2F0, 2F1	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See *Table 2.*
3F0, 3F1	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See *Table 2.*
4F0, 4F1	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See *Table 2.*
TEST	I	Three-level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	O	Output pair 1. See *Table 2.*
2Q0, 2Q1	O	Output pair 2. See *Table 2.*
3Q0, 3Q1	O	Output pair 3. See *Table 2.*
4Q0, 4Q1	O	Output pair 4. See *Table 2.*
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in *Table 1.*

Table 1. Frequency Range Select and t_U Calculation[1]

FS[2]	f_{NOM} (MHz) Min.	f_{NOM} (MHz) Max.	$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. *Table 2* below shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations[1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Note:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see *Table 2*). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.

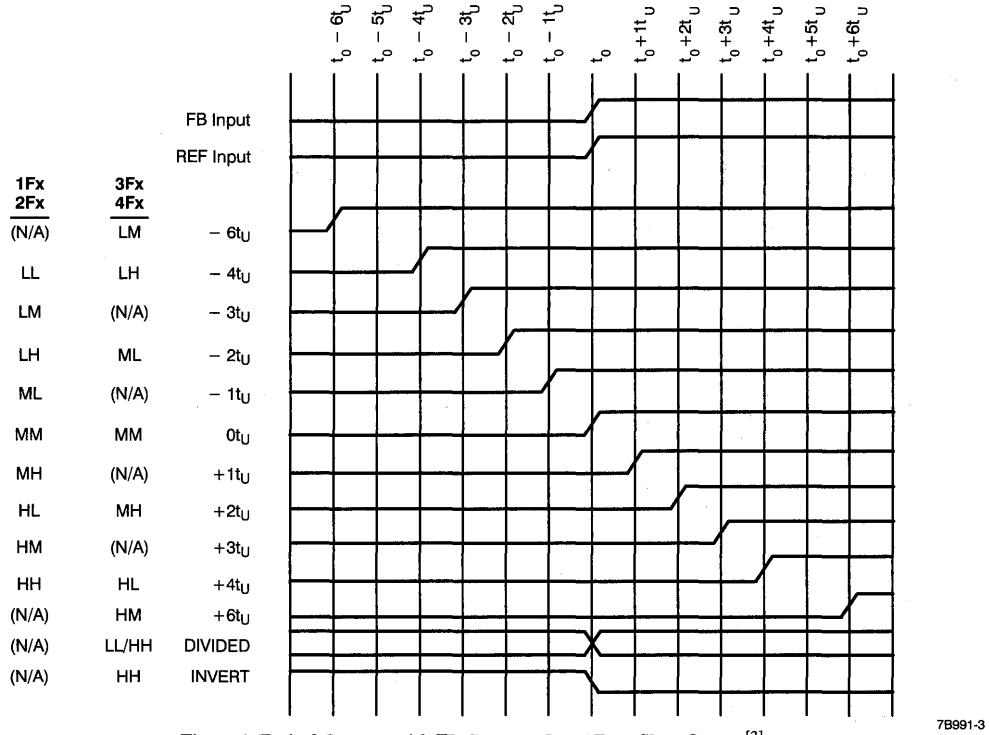


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[3]

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991/CY7B992 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military[4]	− 55°C to +125°C	5V ± 10%

Notes:

3 FB connected to an output selected for "zero" skew (i.e., xF1 = xF0 = MID).

4. Indicates case temperature.

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions	CY7B991 Min.	CY7B991 Max.	CY7B992 Min.	CY7B992 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 16 mA	2.4				V
		V_{CC} = Min., I_{OH} = − 40 mA			V_{CC} − 0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} = 46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		− 0.5	0.8	− 0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS, xFn)[6]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	− 500		− 500		µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = V_{CC}/2	− 50	50	− 50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		− 200		− 200	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND (25°C only)		− 250			mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open		80		80	mA
I_{CCN}	Output Buffer Current per Output Pair[8]	V_{CCN} = V_{CCQ} = Max., C = 50 pf, Z = 50Ω, Input Selects Open, f_{MAX}		45		57	mA
PD	Power Dissipation per Output Pair[9]	V_{CCN} = V_{CCQ} = Max., C = 50 pf, Z = 50Ω, Input Selects Open, f_{MAX}		171		148[10]	mW

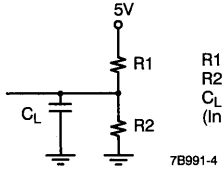
Capacitance[11]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

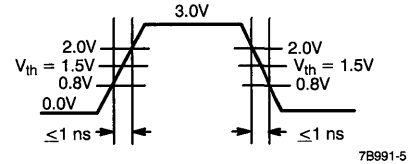
5. See the last page of this specification for Group A subgroup testing information.
6. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
7. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
8. I_{CCN} can be approximated by the following expressions:
   CY7B991:
   I_{CCN} = (2 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N
   CY7B992:
   I_{CCN} = (1.5 + 1.7F) + [((1160 − 2.8F)/Z) + (.0025FC)]N
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
9. Power dissipation can be approximated by the following expressions:
   CY7B991:
   PD = (11 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N
   CY7B992:
   PD = (8.25 + 0.94F) + [((700 + 6F)/Z) + (.017FC)]N
   See note 8 for variable definition.
10. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
11. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

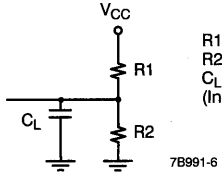


R1 = 130
R2 = 91
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B991)

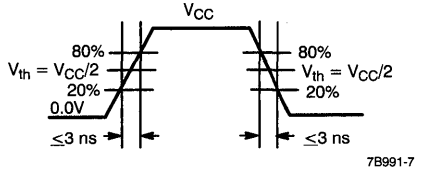


TTL Input Test Waveform (CY7B991)



R1 = 100
R2 = 100
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B992)



CMOS Input Test Waveform (CY7B992)

Switching Characteristics Over the Operating Range[2, 12]

Parameter	Description		CY7B991–5 Min.	CY7B991–5 Typ.	CY7B991–5 Max.	CY7B992–5 Min.	CY7B992–5 Typ.	CY7B992–5 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		80[13]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{UE}	Programmable Skew Unit Error[14]			0.0	±0.5		0.0	±0.5	ns
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.25	0.5		0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	0.7		0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			0.6	1.2		0.6	1.2	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.6	1.0		0.6	1.0	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			0.6	1.3		0.6	1.3	ns
t_{SKEW5}	Device-to-Device Skew[19]				0.2			0.2	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.5	0.0	+0.5	− 0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.0	0.0	+1.0	− 1.0	0.0	+1.0	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 24]				2.5			3.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 24]				3			3.5	ns
t_{ORISE}	Output Rise Time[21, 25]		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time[21, 25]		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time[22]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter, Peak to Peak[23]				0.5			0.5	%

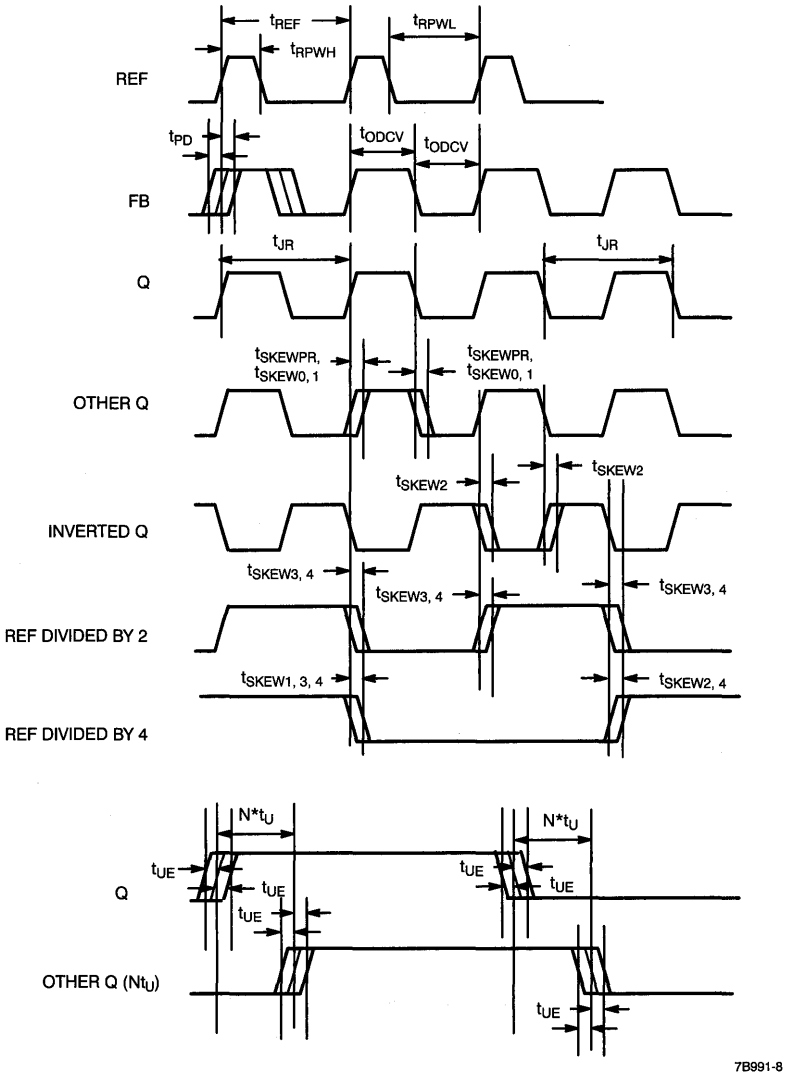
Switching Characteristics Over the Operating Range[2, 12] (continued)

Parameter	Description		CY7B991–7 Min.	CY7B991–7 Typ.	CY7B991–7 Max.	CY7B992–7 Min.	CY7B992–7 Typ.	CY7B992–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{UE}	Programmable Skew Unit Error[14]			0.0	±0.7		0.0	±0.7	ns
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.3	0.75		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	1.0		0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			1.0	1.5		1.0	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.7	1.2		0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			1.2	1.7		1.2	1.7	ns
t_{SKEW5}	Device-to-Device Skew[19]				0.2		0.2		ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.7	0.0	+0.7	− 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.2	0.0	+1.2	− 1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 24]				3			5.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 24]				3.5			5.5	ns
t_{ORISE}	Output Rise Time[21, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[21, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[22]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter, Peak to Peak[23]			0.5			0.5		%

Notes:

12. Test measurement levels for the CY7B991 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B992 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
13. Except as noted, all CY7B992−5 timing parameters are specified to 80-MHz with a 30-pF load.
14. t_{UE} is a measure of the timing error from t_U as calculated in *Table 1*. The major contributors to this error include output edge variations, cross talk, and load-induced variations between package pins and between signal lines external to the chip. t_{UE} is not cumulative across multiple t_U delays.
15. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
16. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
17. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
18. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
19. t_{SKEW5} is the output-to-output skew between the outputs used as the FB input of two or more devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.). The maximum variation between two pins on different parts is t_{SKEW5} plus the skews associated with each part.
20. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
21. Specified with outputs loaded with 30 pF for the CY7B99X−5 devices and 50 pF for the CY7B99X−7 devices. Devices are terminated through 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
22. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
23. Tested initially and after any design or process changes that may affect these parameters.
24. t_{PWH} is measured at 2.0V for the CY7B991 and 0.8 V_{CC} for the CY7B992. t_{PWL} is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
25. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or $0.8V_{CC}$ and $0.2V_{CC}$ for the CY7B992.

AC Timing Diagrams



Operational Mode Descriptions

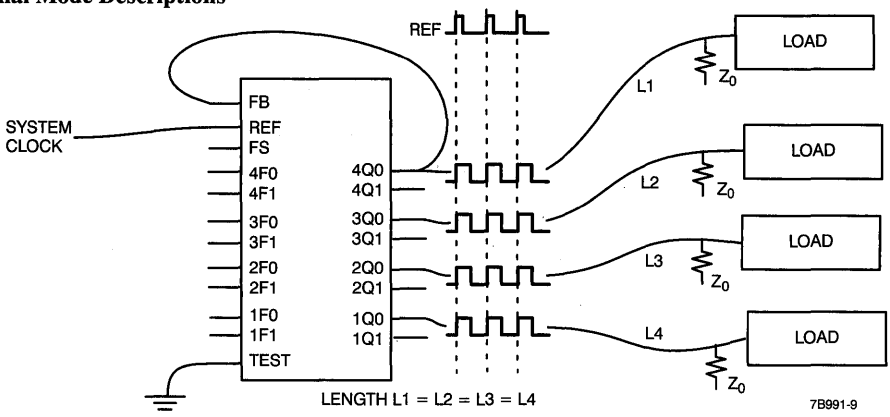


Figure 2. Zero-Skew and/or Zero-Delay Clock Driver

Figure 2 shows the PSCB configured as a zero-skew clock buffer. In this mode the 7B991/992 can be used as the basis for a low-skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

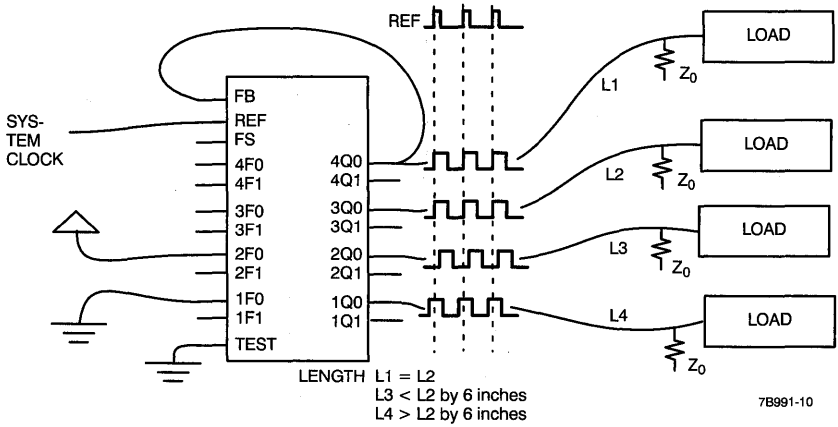


Figure 3. Programmable-Skew Clock Driver

Figure 3 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB can be programmed to stagger the timing of its outputs. The four groups of output pairs can each be programmed to different output timing. Skew timing can be adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0-ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to insure that all outputs have precise phase alignment.

Clock skews can be advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, it is possible to create wider output skews by proper selection of the xFn inputs. For example a $+10\ t_U$ between REF and 3Qx can be achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4\ t_U$ and 3Qx skews to $+6\ t_U$, a total of $+10\ t_U$ skew is realized.) Many other configurations can be realized by skewing both the output used as the FB input and skewing the other outputs.

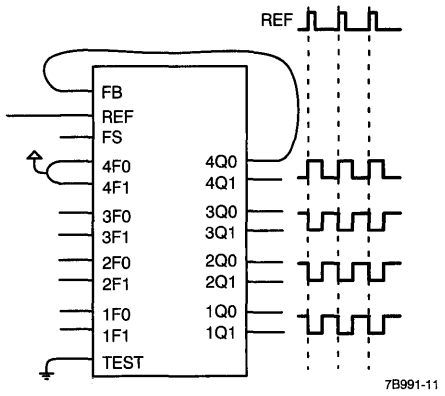


Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configuration would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 5 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40-MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This will allow the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80-MHz operation because that is the frequency of the fastest output.

Figure 6 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15- to 30-MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the "1X" clock. Without this feature, an external divider would need to be added, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the PSCB to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The PSCB can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

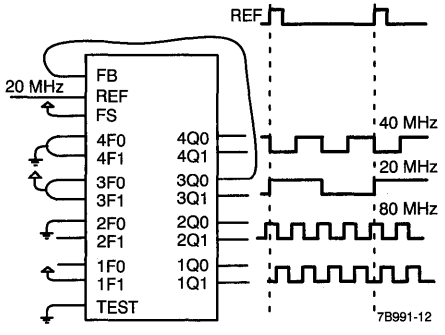


Figure 5. Frequency Multiplier with Skew Connections

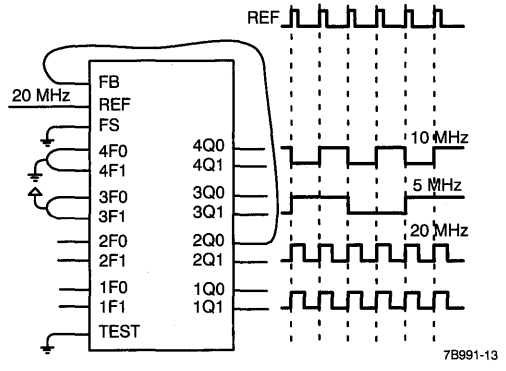


Figure 6. Frequency Divider Connections

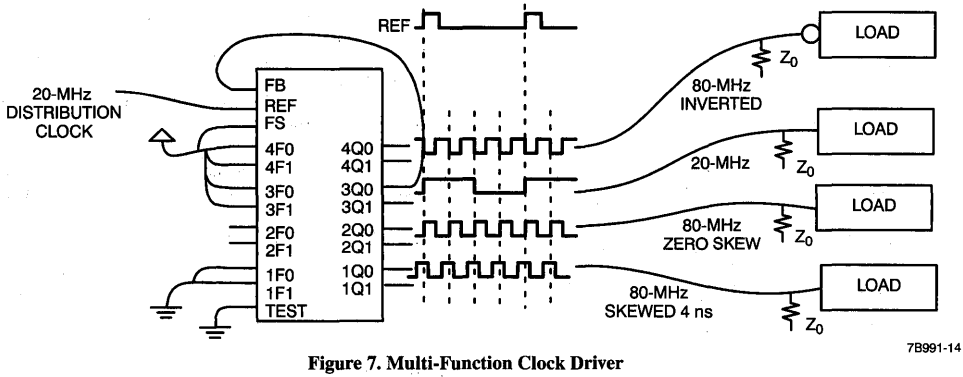


Figure 7. Multi-Function Clock Driver

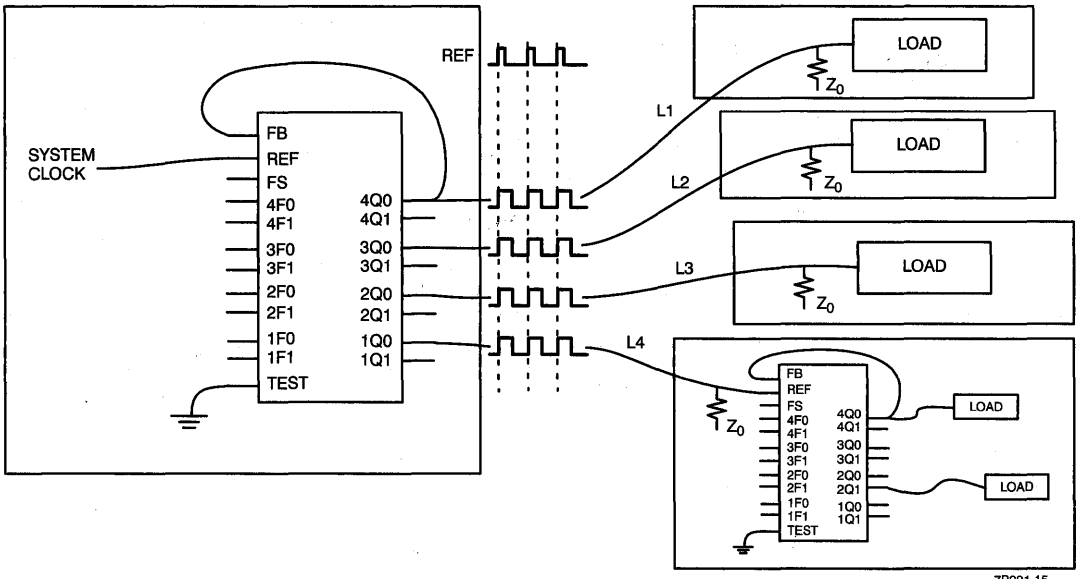


Figure 8. Board-to-Board Clock Distribution

Figure 8 shows the CY7B991/992 connected in series to construct a zero-skew clock distribution tree between boards. Delays of the downstream clock buffers can be programmed to compensate for the wire length (i.e., select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero-delay clock tree. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B991–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–5LC	L55	32-Pin Rectangular Leadless Chip Carrier	

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
750	CY7B991–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–7LC	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B991–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B991–7LI	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B991–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B992–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–5LC	L55	32-Pin Rectangular Leadless Chip Carrier	

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
750	CY7B992–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–7LC	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B992–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B992–7LI	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7B992–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{IHH}	1, 2, 3
V_{IMM}	1, 2, 3
V_{ILL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{IHH}	1, 2, 3
I_{IMM}	1, 2, 3
I_{ILL}	1, 2, 3
I_{OS}	1
I_{CCQ}	1, 2, 3
I_{CCN}	1, 2, 3
PD	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
t_{REF}	9, 10, 11
t_{RPWH}	9, 10, 11
t_{RPWL}	9, 10, 11
t_{U}	9, 10, 11
t_{UE}	9, 10, 11
t_{SKEWPR}	9, 10, 11
t_{SKEW0}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{SKEW3}	9, 10, 11
t_{SKEW4}	9, 10, 11
t_{SKEW5}	9, 10, 11
t_{PD}	9, 10, 11
t_{ODCV}	9, 10, 11
t_{PWH}	9, 10, 11
t_{PWL}	9, 10, 11
t_{QRISE}	9, 10, 11
t_{QFALL}	9, 10, 11
t_{LOCK}	9, 10, 11

CYPRESS SEMICONDUCTOR

CY7C9101

CMOS 16-Bit Slice

Features

- **Fast**
  - **—CY7C9101–30 has a 30-ns (max.) clock cycle (commercial)**
  - **—CY7C9101–35 has a 35-ns (max.) clock cycle (military)**
- **Low power**
  - **—I_{CC} (max. at 10 MHz) = 60 mA (commercial)**
  - **—I_{CC} (max. at 10 MHz) = 85 mA (military)**
- **V_{CC} margin of 5V ±10%**
- **All parameters guaranteed over commercial and military operating temperature range**
- **Replaces four 2901s with carry look-ahead logic**
- **Eight-function ALU performs three arithmetic and five logical operations on two 16-bit operands**
- **Infinitely expandable in 16-bit increments**
- **Four status flags: carry, overflow, negative, zero**
- **Capable of withstanding greater than 2001V static discharge voltage**
- **Pin compatible and functional equivalent to AM29C101**

Functional Description

The CY7C9101 is a high-speed, expandable, 16-bit-wide ALU slice that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C9101 is basic, yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C9101, as shown in the logic block diagram, consists of a 16-word by 16-bit dual-port RAM register file, a 16-bit ALU, and the necessary data manipulation and control logic.

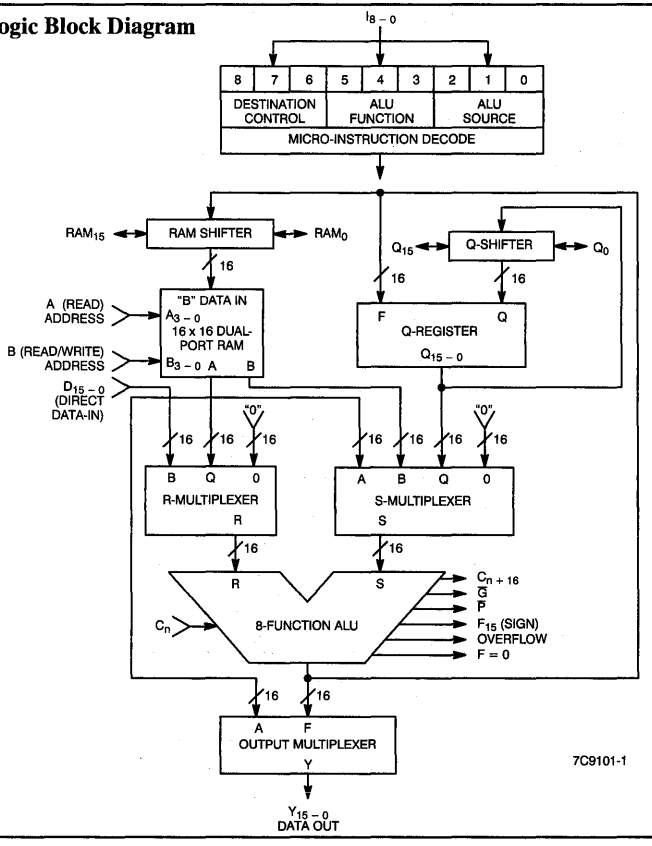
The function performed is determined by 9-bit instruction word (I_8 to I_0), which is usually input via a micro-instruction register.

The CY7C9101 is expandable in 16-bit increments, has three-state data outputs as well as flag outputs, and can implement either a full look-ahead carry or a ripple carry.

The CY7C9101 is a pin-compatible, functional equivalent for the Am29C101 with improved performance. The 7C9101 replaces four 2901s and includes on-chip carry look-ahead logic.

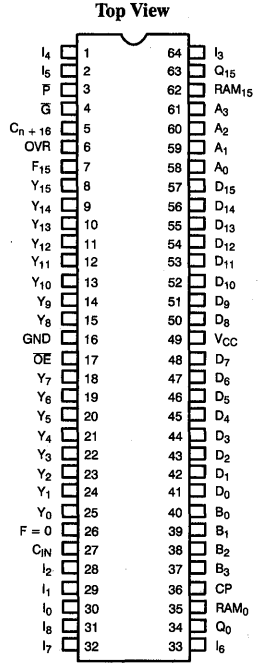
Fabricated in an advanced 1.2-micron CMOS process, the CY7C9101 eliminates latch-up, has ESD protection greater than 2000V, and achieves superior performance with low power dissipation.

Logic Block Diagram



Pin Configurations

Top View



7C9101-2

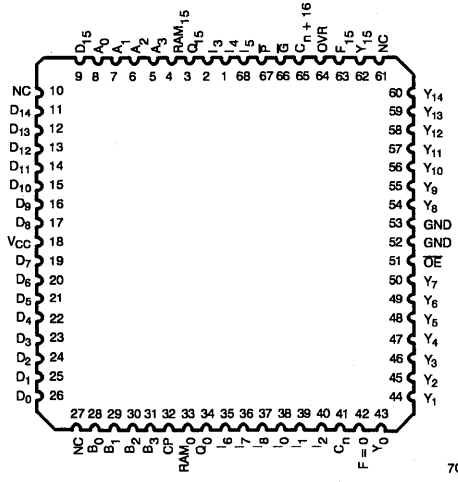
Pin Configurations (continued)

PGA
Top View

	51 Y_1	50 Y_2	48 Y_4	46 Y_6	44 $\overline{OE}$	42 NC	40 Y_8	38 Y_{10}	36 Y_{12}	
53 F=0	52 Y_0	49 Y_3	47 Y_5	45 Y_7	43 V_{SS}	41 V_{SS}	39 Y_9	37 Y_{11}	35 Y_{13}	34 Y_{14}
55 I_2	54 C_n								32 F_{15}	33 Y_{15}
57 I_0	56 I_1								30 C_{n+16}	31 OVR
59 I_7	58 I_8								28 $\overline{P}$	29 $\overline{G}$
61 Q_0	60 I_6								26 I_4	27 I_5
63 CP	62 RAM_0								24 Q_{15}	25 I_3
65 B_2	64 B_3								22 A_3	23 RAM_{15}
67 B_0	66 B_1								20 A_1	21 A_2
68 D_0	69 D_1	71 D_3	73 D_5	75 D_7	77 NC	79 D_8	81 D_{10}	83 D_{12}	18 D_{15}	19 A_0
■	70 D_2	72 D_4	74 D_6	76 V_{CC}	78 V_{CC}	80 D_9	82 D_{11}	84 D_{13}	17 D_{14}	

7C9101-3

LCC/PLCC
Top View



7C9101-4

Selection Guide

		CY7C9101–30 CY7C9101–35	CY7C9101–40 CY7C9101–45
Minimum Clock Cycle (ns)	Commercial	30	40
	Military	35	45
Maximum Operating Current at 10 MHz (mA)	Commercial	60	60
	Military	85	85

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_3 - A_0$	I	RAM Address A. This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) A port.
$B_3 - B_0$	I	RAM Address B. This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) B port. When data is written back to the register file, this is the destination address.
$I_8 - I_0$	I	Instruction Word. This 9-bit word is decoded to determine the ALU data sources ($I_{0,1,2}$), the ALU operation ($I_{3,4,5}$), and the data to be written to the Q register or register file ($I_{6,7,8}$).
$D_{15} - D_0$	I	Direct Data Input. This 16-bit data word may be selected by the $I_{0,1,2}$ lines as an input to the ALU.
$Y_{15} - Y_0$	O	Data Output. These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latch, as determined by the code on the $I_{6,7,8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the $Y_{15} - Y_0$ outputs. A HIGH level on this signal places the output drivers at the high-impedance state.
CP	I	Clock. The LOW level of CP is used to write data to the RAM register file. A HIGH level of CP writes data from the dual-port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the LOW level of CP and transferred from master to slave during CP = HIGH.
Q_{15} RAM_{15}	I/O	These two lines are bidirectional and are controlled by $I_{6,7,8}$. They are three-state output drivers connected to the TTL-compatible CMOS inputs.
Q_{15} RAM_{15} (cont.)	I/O	Output Mode: When the destination code on lines $I_{6,7,8}$ indicates a left shift (UP) operation, the three-state outputs are enabled and the MSB of the Q register is output on the Q_{15} pin and likewise, the MSB of the ALU output (F_{15}) is output on the RAM_{15} pin. Input Mode: When the destination code indicates a right shift (DOWN), the pins are the data inputs to the MSB of the Q register and the MSB of the RAM, respectively.
Q_0 RAM_0	I/O	These two lines are bidirectional and function similarly to the Q_{15} and RAM_{15} lines. The Q_0 and RAM_0 lines are the LSB of the Q register and the RAM.
C_n	I	Carry In. The carry in to the internal ALU.
C_{n+16}	O	Carry Out. The carry out from the internal ALU.
$\overline{G}, \overline{P}$	O	Carry Generate, Carry Propagate. Outputs from the ALU that may be used to perform a carry look-ahead operation over the 16 bits of the ALU.
OVR	O	Overflow. This signal is the logical exclusive-OR of the carry in and the carry out of the MSB of the ALU. This indicates when the result of the ALU operation has exceeded the capacity of the ALU's two's complement number range.
F = 0	O	Zero Detect. Open drain output that goes HIGH when the data on outputs ($F_{15} - F_0$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic assumed).
F_{15}	O	Sign. The MSB of the ALU output.

Description of Architecture

General Description

The CY7C9101 general block diagram is shown on the first page of this datasheet, in the Logic Block Diagram section. Detailed block diagrams (*Figures 1* through *3*) show the operation of specific sections as described below. The device is a 16-bit slice consisting of a register file (16-word by 16-bit dual-port RAM), the ALU, the Q register, and the necessary control logic. It is expandable in 16-bit increments.

Register File

The dual-port RAM is addressed by two 4-bit address fields ($A_3 - A_0$, $B_3 - B_0$) that cause the data to simultaneously appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

Data to be written to RAM is applied to the D inputs of the 7C9101 and is passed (unchanged) through the ALU to the RAM location specified by the B-address word. New data is written into the RAM by specifying a B address while RAM write enable (RAM EN) is active and the clock input is LOW. RAM EN is an internal signal decoded from the signals $I_{6,7,8}$. As shown in *Figure 1*, each of the 16 RAM inputs is driven by a three-input multiplexer that allows the ALU output ($F_{15} - F_0$) to be shifted one bit position to the left or right, or not shifted at all. The RAM_{15} and RAM_0 I/O pins are also inputs to the 16-bit, 3-input multiplexer.

During the left-shift (upshift) operation, the RAM_{15} output buffer and RAM_0 input multiplexer are enabled. For the right-shift (downshift) operation, the RAM_0 output buffer and the RAM_{15} input multiplexer are enabled.

The A and B outputs of the RAM drive separate 16-bit latches that are enabled when the clock is HIGH. The outputs of the A latch go to the three multiplexers that feed the two ALU inputs ($R_{15} - R_0$ and $S_{15} - S_0$) and the chip output ($Y_{15} - Y_0$). The B latch outputs are directed to the multiplexer that feeds the S input to the ALU.

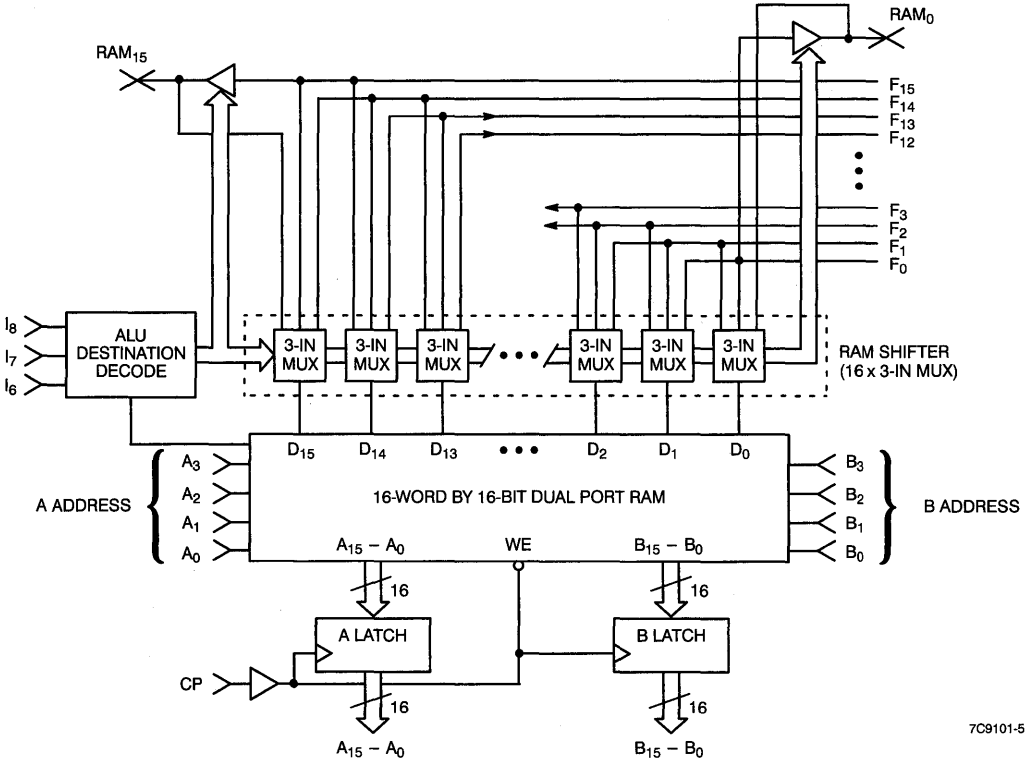


Figure 1. Register File

Description of Architecture (continued)

Q Register

The Q register is mainly intended for use as a separate working register for multiplication and division routines. It may also function as an accumulator or temporary storage register. Sixteen master-slave latches are used to implement the Q register. As shown in *Figure 2*, the Q-register inputs are driven by the outputs of the Q shifter (sixteen 3-input multiplexers, under the control of $I_{6,7,8}$). The function of the Q register input multiplexers is to allow the Q register to be shifted either left or right, or loaded with the ALU output ($F_{15} - F_0$). The Q_{15} and Q_0 pins (I/O) function similarly to the RAM_{15} and RAM_0 pins described earlier. Data is entered into the master latches when the clock is LOW and is transferred to the slave (output) at the clock LOW-to-HIGH transition.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on the two 16-bit input operands, R and S. The R input multiplexer selects between data from the RAM A port and data at the external data input, $D_{15} - D_0$. The S input multiplexer selects between data from the RAM A port, the RAM B port, and the Q register. The R and S multiplexers are controlled by the $I_{0,1,2}$ inputs as shown in *Table 1*. The R and S input multiplexers each have an "inhibit capability," offering a state where no data is passed. This is equivalent to a source operand consisting of all zeros. The R and S ALU source multiplexers are configured to allow eight pairs of combinations of A, B, D, Q, and "0" to be selected as ALU input operands.

The ALU input functions, which are controlled by $I_{3,4,5}$, are shown in *Table 2*. Carry look-ahead logic is resident on the 7C9101, using the ALU carry in (C_n) input and the ALU carry propagate ($\overline{P}$), carry generate ($\overline{G}$), carry out (C_{n+16}), and overflow outputs to implement carry look-ahead arithmetic and determine if arithmetic overflow has occurred. Note that the carry in (C_n) signal affects the arithmetic result and internal flags only; it has no effect on the logical operations.

Control signals $I_{6,7,8}$ route the ALU data output ($F_{15} - F_0$) to the RAM, the Q register inputs, and the Y outputs as shown in *Table 3*. The ALU result MSB (F_{15}) is output so the user may examine the sign bit without needing to enable the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open drain output that may be wire ORed across multiple 7C9101 processor slices. *Figure 3* shows a block diagram of the ALU.

The ALU source operands and ALU function matrix are summarized in *Table 4* and separated by logic operation or arithmetic operation in *Tables 5* and *6*, respectively. The $I_{0,1,2}$ lines select eight pairs of source operands and the $I_{3,4,5}$ lines select the operation to be performed.

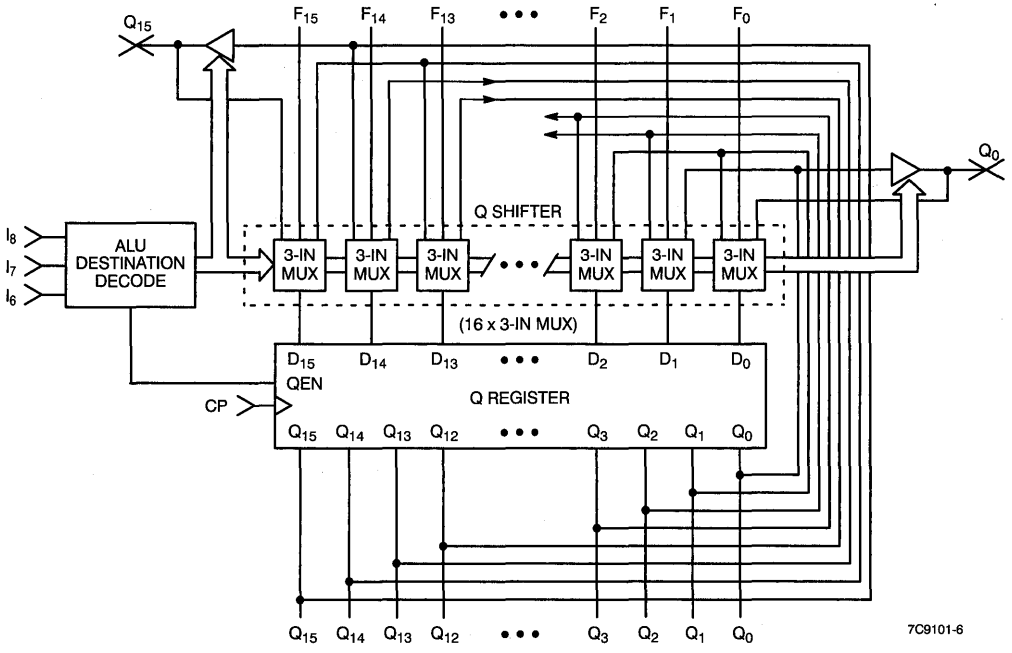


Figure 2. Q Register

Description of Architecture (continued)

Conventional Addition and Pass-Increment/Decrement

When the carry in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation. In logical operations, the carry in (C_n) will not affect the ALU output.

Subtraction

Recall that in two's complement integer coding − 1 is equal to all ones, and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Table 6* the symbol − Q represents the two's complement of Q, so the one's complement of Q is then − Q − 1.

Table 1. ALU Source Operand Control

	Micro Code				ALU Source Operands	
Mnemonic	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

	Micro Code					
Mnemonic	I_5	I_4	I_3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
XOR	H	H	L	6	R XOR S	$R \veebar S$
XNOR	H	H	H	7	R XNOR S	$\overline{R \veebar S}$

Table 3. ALU Destination Control

	Micro Code				RAM Function		Q-Reg. Function			RAM Shifter		Q Shifter	
Mnemonic	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load	Y Output	RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F ⇧ Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F ⇧ B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F ⇧ B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 ⇧ B	DOWN	Q/2 ⇧ Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 ⇧ B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F ⇧ B	UP	2Q ⇧ Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F ⇧ B	X	None	F	IN_0	F_{15}	X	Q_{15}

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output that is in the high-impedance state.
A = Register addressed by A inputs.
B = Register addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Description of Architecture (continued)

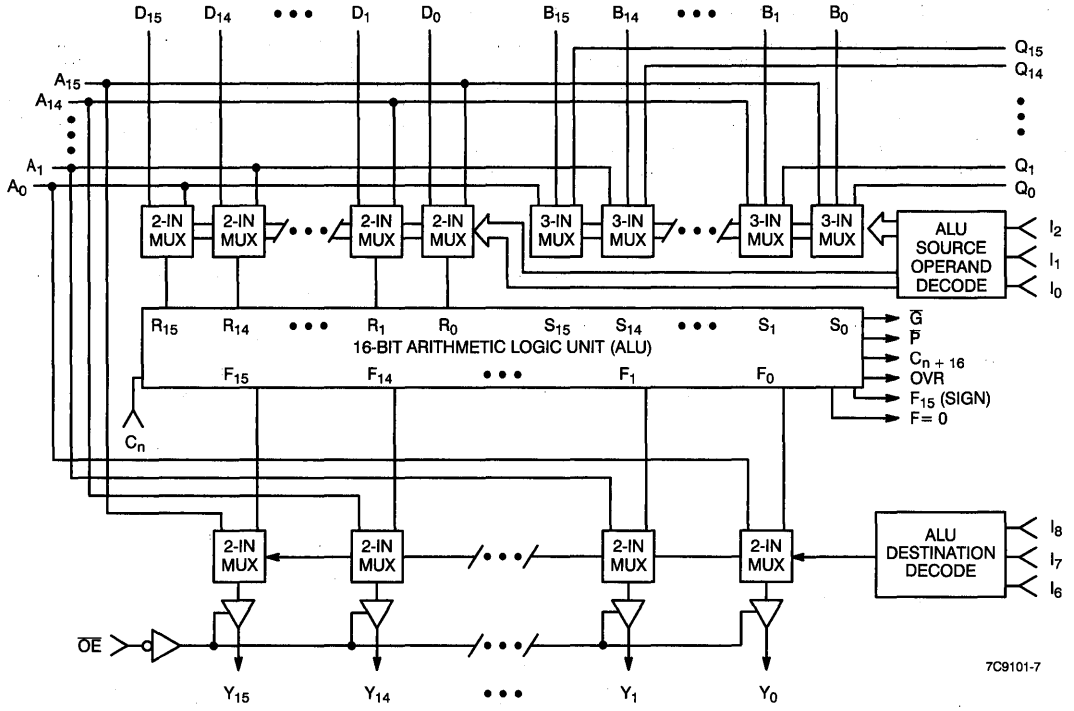


Figure 3. ALU

Table 4. Source Operand and ALU Function Matrix

Octal I_{543}	I_{210} Octal	0	1	2	3	4	5	6	7
	ALU Source	A	A	O	O	O	D	D	D
	ALU Function	Q	B	Q	B	A	A	Q	O
0	C_n = L R plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ⊻ Q	A ⊻ B	Q	B	A	D ⊻ A	D ⊻ Q	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Description of Architecture (continued)

Table 5. ALU Logic Mode Functions

Octal I_{543}, I_{210}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee Q$
60	XOR	$A \veebar Q$
61		$A \veebar B$
65		$D \veebar A$
66		$D \veebar Q$
70	XNOR	$\overline{A \veebar Q}$
71		$\overline{A \veebar B}$
75		$\overline{D \veebar A}$
76		$\overline{D \veebar Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{543}, I_{210}	C_n = 0 (LOW)		C_n = 1 (HIGH)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1's Comp.	− Q − 1	2's Comp. (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1's Comp.)	Q − A − 1	Subtract (2's Comp.)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

Electrical Characteristics Over Commercial and Military Operating Range[2]

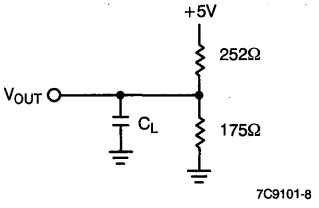
V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 3.4 mA All Outputs Except F = 0		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.		−10	10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V All Outputs Except F = 0		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V		16		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max.			+40	μA
		V_{OUT} = V_{SS} to V_{CC}		−40		μA
I_{SC}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0V All Outputs Except F = 0			−85	mA
$I_{CC}(Q_1)$[4]	Supply Current (Quiescent)	$V_{SS} \le V_{IN} \le V_{IL}$ or $V_{IH} \le V_{IN} \le V_{CC}$; $\overline{OE}$ = HIGH	Commercial		30	mA
			Military		35	mA
$I_{CC}(Q_2)$[4]	Supply Current (Quiescent)	$V_{SS} \le V_{IN} \le 0.4V$ or $3.85V \le V_{IN} \le V_{CC}$; $\overline{OE}$ = HIGH	Commercial		25	mA
			Military		30	mA
I_{CC}(Max.)[4]	Supply Current	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH	Commercial		60	mA
			Military		85	mA

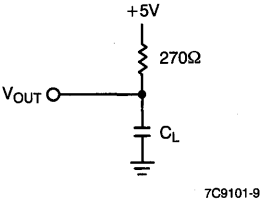
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Output Loads Used for AC Performance Characteristics[6, 7]



All Outputs Except Open Drain



Open Drain (F = 0)

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given frequency, use $I_{CC}(Q_1) + I_{CC}(AC)$ where $Icc(Q_1)$ is shown above and $I_{CC}(AC)$ = (3 mA/MHz) × Clock Frequency for the commercial temperature. $I_{CC}(AC)$ = (5 mA/MHz) × Clock Frequency for military temperature range.
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 50 pF includes scope probe, wiring, and stray capacitance.
7. C_L = 5 pF for output disable tests.

Table 7. Logic Functions for CARRY and OVERFLOW Conditions

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+16}	OVR
0	R + S	$\overline{P_0 - P_{15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_1 - P_{15}G_0}$	C_{16}	$C_{16} \veebar C_{15}$
1	S − R	⧫ Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions ⧫			
2	R − S	⧫ Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions ⧫			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$\overline{R} \wedge S$				
6	$\overline{R \veebar S}$				
7	$R \veebar S$				

Definitions (+ = OR)

$P_0 - P_{15} = P_{15}P_{14}P_{13}P_{12}P_{11}P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$

$P_0 = R_0 + S_0$

$P_1 = R_1 + S_1$

$P_2 = R_2 + S_2$

$P_3 = R_3 + S_3$, etc.

$G_0 - G_{15} = G_{15}G_{14}G_{13}G_{12}G_{11}G_{10}G_9G_8G_7G_6G_5G_4G_3G_2G_1G_0$

$G_0 = R_0S_0$

$G_1 = R_1S_1$

$G_2 = R_2S_2$

$G_3 = R_3S_3$, etc.

$C_{16} = G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_0 - P_{15}C_n$

$C_{15} = G_{14} + P_{14}G_{13} + P_{14}P_{13}G_{12} + \ldots + P_0 - P_{14}C_n$

6 LOGIC

CY7C9101−30 and CY7C9101−40 Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See the Electrical Characteristics section for loading circuit information.

This data applies to parts with the following numbers:
CY7C9101−30PC CY7C9101−30JC CY7C9101−30GC CY7C9101−40PC CY7C9101−40JC CY7C9101−40GC

Cycle Time and Clock Characteristics

CY7C9101	−30	−40
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	30 ns	40 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	33 MHz	25 MHz
Minimum Clock LOW Time	20 ns	25 ns
Minimum Clock HIGH Time	10 ns	15 ns
Minimum Clock Period	30 ns	40 ns

Combinatorial Propagation Delays (C_L = 50 pF)[8]

To Output	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_{15}		Q_{15}	
Speed (ns)	30	40	30	40	30	40	30	40	30	40	30	40	30	40	30	40
A, B Address	37	47	36	47	35	44	32	41	35	46	32	42	32	40	—	—
D	29	34	28	34	25	32	25	30	29	36	21	26	27	33	—	—
C_n	22	27	22	27	20	25	—	—	22	26	22	26	24	30	—	—
I_{012}	32	40	32	40	30	38	28	36	34	42	26	32	27	35	—	—
I_{345}	34	43	33	42	33	42	27	35	34	40	32	42	29	38	—	—
I_{678}	19	22	—	—	—	—	—	—	—	—	—	—	22	26	22	26
A Bypass ALU (I = 2XX)	25	30	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	31	40	30	39	30	38	27	34	28	37	34	34	27	35	20	23

Note:

8. A dash indicates a propagation delay path or set-up time constraint does not exist.

Set-Up and Hold Times Relative to Clock (CP) Input[8]

	CP: Set-Up Time Before H ⧫ L		Hold Time After H ⧫ L		Set-Up Time Before L ⧫ H		Hold Time After L ⧫ H	
Speed (ns)	30	40	30	40	30	40	30	40
A, B Source Address	10	15	3[9]	3[9]	30[10]	40[10]	0	0
B Destination Address	10	15	⧫ Do Not Change[11] ⧫				0	0
Data	—	—	—	—	22	28	0	0
C_n	—	—	—	—	16	22	0	0
$I_{0, 1, 2}$	—	—	—	—	26	35	0	0
$I_{3, 4, 5}$	—	—	—	—	29	37	0	0
$I_{6, 7, 8}$	10	12	⧫ Do Not Change[11] ⧫				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	11	14	0	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101–30	$\overline{OE}$	Y	18	16
CY7C9101–40	$\overline{OE}$	Y	22	19

Notes:

9. Source addresses must be stable prior to the clock HIGH-to-LOW transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
10. The set-up time prior to the clock LOW-to-HIGH transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock LOW-to-HIGH transition, regardless of when the clock HIGH-to-LOW transition occurs.
11. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

CY7C9101–35 and CY7C9101–45 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the military (– 55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See the Electrical Characteristics section for loading circuit information.

This data applies to parts with the following numbers:
CY7C9101–35DMB CY7C9101–35LMB CY7C9101–35GMB
CY7C9101–45DMB CY7C9101–45LMB CY7C9101–45GMB

Cycle Time and Clock Characteristics[2]

CY7C9101	–35	–45
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	35 ns	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	28 MHz	22 MHz
Minimum Clock LOW Time	23 ns	28 ns
Minimum Clock HIGH Time	12 ns	17 ns
Minimum Clock Period	35 ns	45 ns

Combinatorial Propagation Delays (C_L = 50 pF)[2, 8]

To Output	Y		F_{15}		$C_n + 16$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_{15}		$C_n + 16$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_{15}		Q_{15}	
Speed (ns)	35	45	35	45	35	45	35	45	35	45	35	45	35	45	35	45
A, B Address	41	52	40	51	38	48	37	45	40	48	36	46	36	43	—	—
D	31	37	31	36	29	36	28	32	33	40	23	32	30	35	—	—
C_n	25	30	24	29	23	27	—	—	24	29	23	27	26	31	—	—
I_{012}	36	44	35	43	33	41	31	38	38	46	29	38	30	38	—	—
I_{345}	38	48	37	47	37	46	31	38	38	45	36	45	33	41	—	—
I_{678}	21	24	—	—	—	—	—	—	—	—	—	—	24	28	24	28
A Bypass ALU (I = 2XX)	28	33	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	35	44	34	43	34	42	30	37	34	40	28	38	30	37	21	25

Set-Up and Hold Times Relative to Clock (CP) Input[2, 8]

	CP:							
	Set-Up Time Before H ⧫ L		Hold Time After H ⧫ L		Set-Up Time Before L ⧫ H		Hold Time After L ⧫ H	
Speed (ns)	35	45	35	45	35	45	35	45
A, B Source Address	12	17	3[9]	3[9]	35[10]	45[10]	0	0
B Destination Address	12	17	⧫ Do Not Change[11] ⧫				1	1
D	—	—	—	—	25	30	0	0
C_n	—	—	—	—	19	24	0	0
I_{012}	—	—	—	—	30	37	0	0
I_{345}	—	—	—	—	33	40	0	0
I_{678}	12	16	⧫ Do Not Change[11] ⧫				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	13	15	1	1

Output Enable/Disable Times[2]

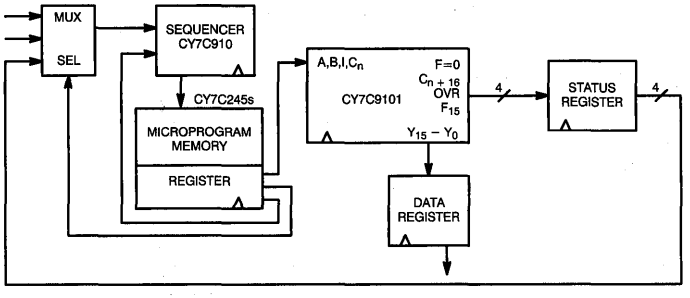
Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101–35	$\overline{OE}$	Y	20	17
CY7C9101–45	$\overline{OE}$	Y	23	20

Applications

Minimum Cycle Time Calculations for 16-Bit Systems

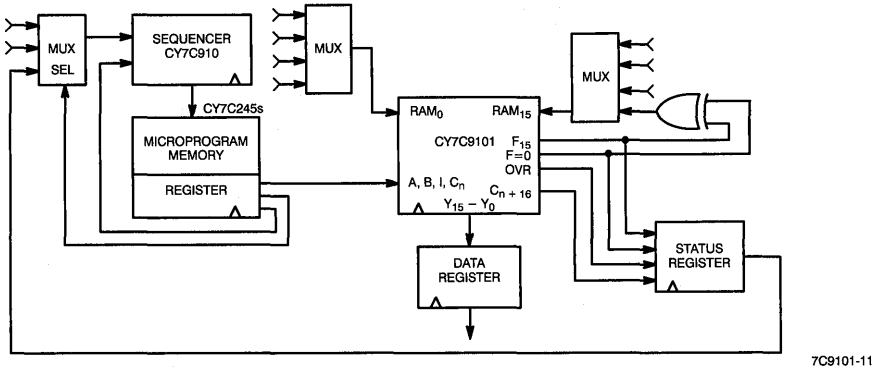
Speed used in calculations for parts other than CY7C9101 and CY7C910 are representative for available MSI parts.



Pipelined System, Add Without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
Register	Set-Up	4	CY7C910	CC to Output	22
		53 ns	CY7C245	Access Time	20
					66 ns

Minimum Clock Period = 66 ns



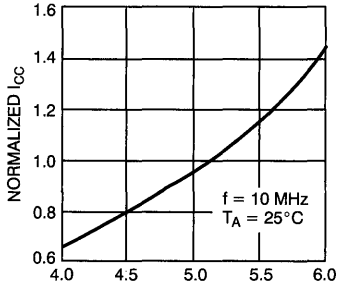
Pipelined System, Simultaneous Add and Shift Down (Right)

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C9101	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
XOR and MUX	Prop. Delay, Select to Output	20	CY7C910	CC to Output	22
			CY7C245	Access Time	20
CY7C9101	RAM_{15} Set-Up	11			66 ns
		80 ns			

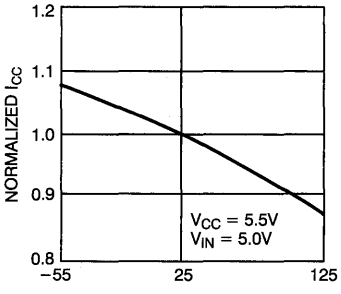
Minimum Clock Period = 80 ns

Typical DC and AC Characteristics

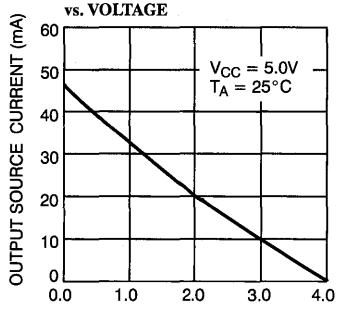
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



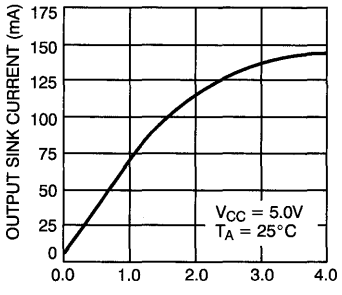
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



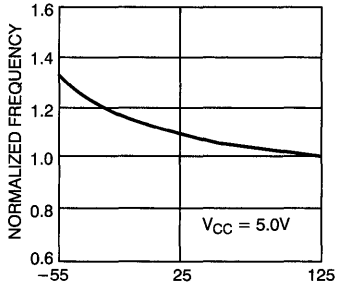
OUTPUT SOURCE CURRENT vs. VOLTAGE



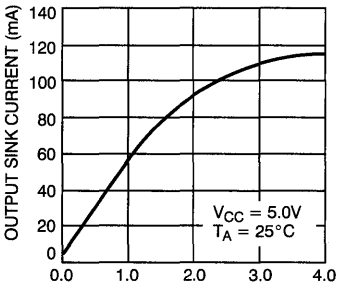
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



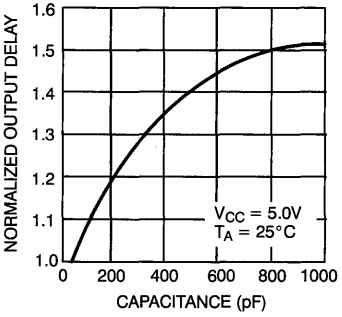
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



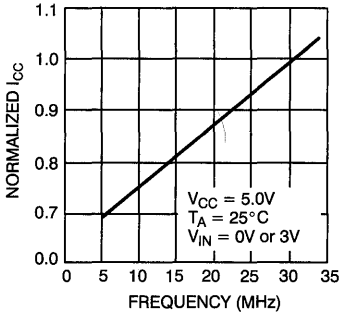
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL OUTPUT DELAY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C9101-12

6 LOGIC

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C9101–30GC	G68	68-Pin PGA (Cavity Down)	Commercial
	CY7C9101–30JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C9101–30PC	P29	64-Lead (900-Mil) Molded DIP	
35	CY7C9101–35DMB	D30	64-Lead (900-Mil) Bottombraze	Military
	CY7C9101–35GMB	G68	68-Pin PGA (Cavity Down)	
	CY7C9101–35LMB	L81	68-Square Leadless Chip Carrier	
40	CY7C9101–40GC	G68	68-Pin PGA (Cavity Down)	Commercial
	CY7C9101–40JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C9101–40PC	P29	64-Lead (900-Mil) Molded DIP	
45	CY7C9101–45DMB	D30	64-Lead (900-Mil) Bottombraze	Military
	CY7C9101–45GMB	G68	68-Pin PGA (Cavity Down)	
	CY7C9101–45LMB	L81	68-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
$I_{CC}(Q_1)$	1, 2, 3
$I_{CC}(Q_2)$	1, 2, 3
I_{CC}(Max.)	1, 2, 3

Combinational Propagation Delays

Parameter	Subgroups
From A, B Address to Y	7, 8, 9, 10, 11
From A, B Address to F_{15}	7, 8, 9, 10, 11
From A, B Address to C_{n+16}	7, 8, 9, 10, 11
From A, B Address to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From A, B Address to F = 0	7, 8, 9, 10, 11
From A, B Address to OVR	7, 8, 9, 10, 11
From A, B Address to $RAM_{0,15}$	7, 8, 9, 10, 11
From D to Y	7, 8, 9, 10, 11
From D to F_{15}	7, 8, 9, 10, 11
From D to C_{n+16}	7, 8, 9, 10, 11
From D to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From D to F = 0	7, 8, 9, 10, 11
From D to OVR	7, 8, 9, 10, 11
From D to $RAM_{0,15}$	7, 8, 9, 10, 11
From C_n to Y	7, 8, 9, 10, 11
From C_n to F_{15}	7, 8, 9, 10, 11
From C_n to C_{n+16}	7, 8, 9, 10, 11

Combinational Propagation Delays (continued)

Parameter	Subgroups
From C_n to F = 0	7, 8, 9, 10, 11
From C_n to OVR	7, 8, 9, 10, 11
From C_n to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{0,1,2}$ to Y	7, 8, 9, 10, 11
From $I_{0,1,2}$ to F_{15}	7, 8, 9, 10, 11
From $I_{0,1,2}$ to C_{n+16}	7, 8, 9, 10, 11
From $I_{0,1,2}$ to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From $I_{0,1,2}$ to F = 0	7, 8, 9, 10, 11
From $I_{0,1,2}$ to OVR	7, 8, 9, 10, 11
From $I_{0,1,2}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{3,4,5}$ to Y	7, 8, 9, 10, 11
From $I_{3,4,5}$ to F_{15}	7, 8, 9, 10, 11
From $I_{3,4,5}$ to C_{n+16}	7, 8, 9, 10, 11
From $I_{3,4,5}$ to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From $I_{3,4,5}$ to F = 0	7, 8, 9, 10, 11
From $I_{3,4,5}$ to OVR	7, 8, 9, 10, 11
From $I_{3,4,5}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{6,7,8}$ to Y	7, 8, 9, 10, 11
From $I_{6,7,8}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{6,7,8}$ to $Q_{0,15}$	7, 8, 9, 10, 11
From A Bypass ALU to Y (I = 2XX)	7, 8, 9, 10, 11
From Clock LOW to HIGH to Y	7, 8, 9, 10, 11
From Clock LOW to HIGH to F_{15}	7, 8, 9, 10, 11
From Clock LOW to HIGH to C_{n+16}	7, 8, 9, 10, 11
From Clock LOW to HIGH to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to F = 0	7, 8, 9, 10, 11
From Clock LOW to HIGH to OVR	7, 8, 9, 10, 11
From Clock LOW to HIGH to $RAM_{0,15}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to $Q_{0,15}$	7, 8, 9, 10, 11

Set-Up and Hold Times Relative to Clock (CP) Input

Parameter	Subgroups
A, B Source Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
A, B Source Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
B Destination Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
B Destination Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
D Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
D Hold Time After L ⧫ H	7, 8, 9, 10, 11
C_n Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
C_n Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{012} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{012} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{345} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{345} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{678} Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
I_{678} Hold Time After H ⧫ L	7, 8, 9, 10, 11
I_{678} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{678} Hold Time After L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_{15}, Q_0, Q_{15} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_{15}, Q_0, Q_{15} Hold Time After L ⧫ H	7, 8, 9, 10, 11

Document #: 38–00017–D

Section Contents

Data Communications Products

HOTLink™ Transmitter/Receiver

Features

- **Fibre Channel compliant**
- **IBM ESCON™ compliant**
- **ATM Compatible**
- **8B/10B-coded or 10-bit unencoded**
- **160- to 330-Mbps data rate**
- **TTL synchronous I/O**
- **No external PLL components**
- **Triple ECL 100K serial outputs**
- **Dual ECL 100K serial inputs**
- **Low power: 350 mW (Tx), 650 mW (Rx)**
- **Compatible with fiber optic modules, coaxial cable, and twisted pair media**
- **Built-In Self-Test**
- **Single +5V supply**
- **28-pin DIP/PLCC/LCC**
- **0.8μ BiCMOS**

Functional Description

The CY7B923 HOTLink Transmitter and CY7B933 HOTLink Receiver are point-to-point communications building blocks that transfer data over high-speed serial links (fiber, coax, and twisted pair) at 160 to 330 Mbits/second. *Figure 1* illustrates typical connections to host systems or controllers.

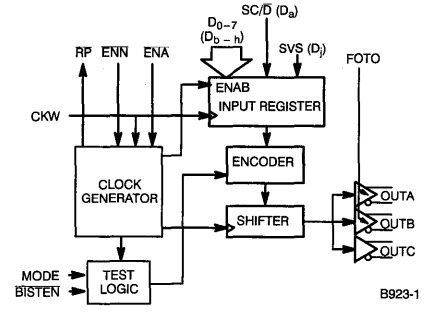
Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is shifted out of the three differential Pseudo ECL (PECL) serial ports at the bit rate (which is 10 times the byte rate).

The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs, and using a completely integrated PLL clock synchronizer recovers the timing information necessary for data reconstruction. The bit stream is deserialized, decoded, and checked for transmission errors. The recovered byte is presented in parallel to the receiving host along with a byte rate clock.

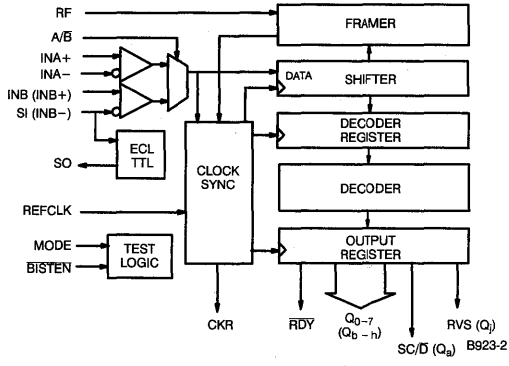
The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/Os are available to create a seamless interface with both asynchronous FIFOs (i.e., CY7C42X) and clocked FIFOs (i.e., CY7C44X). A Built-In Self-Test pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

HOTLink devices are ideal for a variety of applications where a parallel interface can be replaced with a high-speed point-to-point serial link. Applications include interconnecting workstations, servers, mass storage, and video transmission equipment.

CY7B923 Transmitter Logic Block Diagram



CY7B933 Receiver Logic Block Diagram



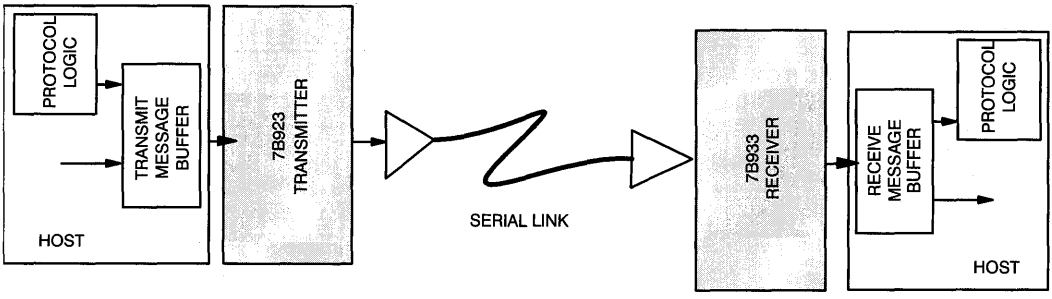
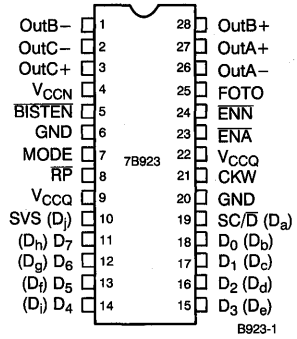


Figure 1. HOTLink System Connections

HOTLink is a trademark of Cypress Semiconductor Corporation.
ESCON is a registered trademark of IBM.

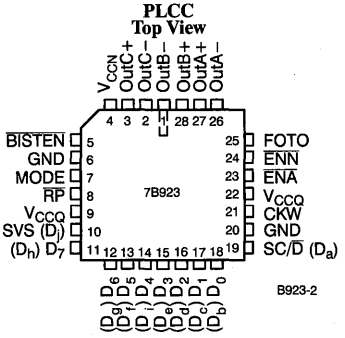
CY7B923 Transmitter Pin Configurations

DIP
Top View



B923-1

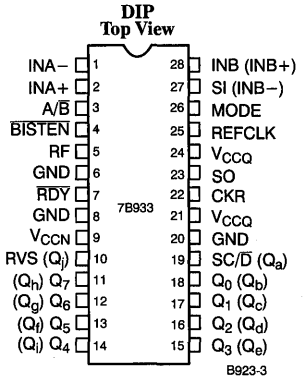
PLCC
Top View



B923-2

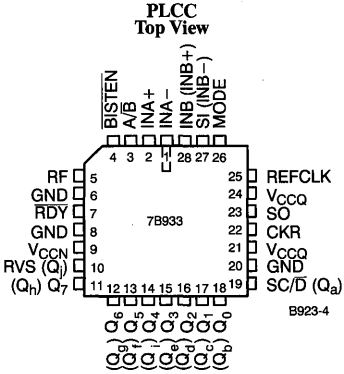
CY7B933 Receiver Pin Configurations

DIP
Top View



B923-3

PLCC
Top View



B923-4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65 C to +150 C

Ambient Temperature with Power Applied ..... −55 C to +125 C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military	− 55°C to +125°C Case Temperature	5V ± 10%

Pin Descriptions

CY7B923 HOTLink Transmitter

Name	I/O	Description
D_{0-7} (D_{b-h})	TTL In	Parallel Data Input. Data is clocked into the Transmitter on the rising edge of CKW if $\overline{ENA}$ is LOW (or on the next rising CKW with $\overline{ENN}$ LOW). If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, a Null character (K28.5) is sent. When MODE is HIGH, $D_{0,1,...7}$ become $D_{b,c,...h}$ respectively.
SC/$\overline{D}$ (D_a)	TTL In	Special Character/Data Select. A HIGH on SC/$\overline{D}$ when CKW rises causes the transmitter to encode the pattern on D_{0-7} as a control code (Special Character), while a LOW causes the data to be coded using the 8B/10B data alphabet. When MODE is HIGH, SC/$\overline{D}$ (D_a) acts as D_a input.
SVS (D_j)	TTL In	Send Violation Symbol. If SVS is HIGH when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. If SVS is LOW, the state of D_{0-7} and SC/$\overline{D}$ determines the code sent. In normal or test mode, this pin overrides the BIST generator and forces the transmission of a Violation code. When MODE is HIGH, SVS (D_j) acts as D_j input.
$\overline{ENA}$	TTL In	Enable Parallel Data. If $\overline{ENA}$ is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If $\overline{ENA}$ is HIGH, the data inputs are ignored and the Transmitter will insert a Null character (K28.5) to fill the space between user data. $\overline{ENA}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte to be sent. If $\overline{ENA}$ is being used for data control, $\overline{ENN}$ will normally be strapped HIGH, but can be used for BIST function control.
$\overline{ENN}$	TTL In	Enable Next Parallel Data. If $\overline{ENN}$ is LOW, the data appearing on D_{0-7} at the next rising edge of CKW is loaded, encoded, and sent. If $\overline{ENN}$ is HIGH, the data appearing on D_{0-7} at the next rising edge of CKW will be ignored and the Transmitter will insert a Null character to fill the space between user data. $\overline{ENN}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte sent. If $\overline{ENN}$ is being used for data control, $\overline{ENA}$ will normally be strapped HIGH, but can be used for BIST function control.
CKW	TTL In	Clock Write. CKW is both the clock frequency reference for the multiplying PLL that generates the high-speed transmit clock, and the byte rate write signal that synchronizes the parallel data input. CKW must be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber Optic Transmitter Off. FOTO determines the function of two of the three ECL transmitter output pairs. If FOTO is LOW, the data encoded by the Transmitter will appear at the outputs continuously. If FOTO is HIGH, OUTA± and OUTB± are forced to their "logic zero" state (OUT+ = LOW and OUT− = HIGH), causing a fiber optic transmit module to extinguish its light output. OUTC is unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUT A± OUT B± OUT C±	ECL Out	Differential Serial Data Outputs. These ECL 100K outputs (+5V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of outputs can be wired to V_{CC} to reduce power if the output is not required. OUTA± and OUTB± are controlled by the level on FOTO, and will remain at their "logical zero" states when FOTO is asserted. OUTC± is unaffected by the level on FOTO. (OUTA+ and OUTB+ are used as a differential test clock input while in Test mode, i.e., MODE=UNCONNECTED.)
MODE	3-Level In	Encoder Mode Select. The level on MODE determines the encoding method to be used. When wired to GND, MODE selects 8B/10B encoding. When wired to V_{CC}, data inputs bypass the encoder and the bit pattern on D_{a-j} goes directly to the shifter. When left floating (internal resistors hold the input at $V_{CC}/2$) the internal bit-clock generator is disabled and OUTA+/OUTB+ become the differential bit clock to be used for factory test. In typical applications MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW and $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the transmitter sends an alternating 1−0 pattern (D10.2 or D21.5). When either $\overline{ENA}$ or $\overline{ENN}$ is set LOW the transmitter begins a repeating test sequence that allows the Transmitter and Receiver to work together to test the function of the entire link. In normal use this input is held HIGH or wired to V_{CC}. The BIST generator is a free-running pattern generator that need not be initialized, but if required, the BIST sequence can be initialized by momentarily asserting SVS while $\overline{BISTEN}$ is LOW.
$\overline{RP}$	TTL Out	Read Pulse. $\overline{RP}$ is a 60% LOWduty-cycle byte-rate pulse train suitable for the read pulse in CY7C42X FIFOs. The frequency on $\overline{RP}$ is the same as CKW when enabled by $\overline{ENA}$, and duty cycle is independent of the CKW duty cycle. Pulse widths are set by logic internal to the transmitter. In BIST mode, $\overline{RP}$ will remain HIGH for all but the last byte of a test loop. $\overline{RP}$ will pulse LOW one byte time per BIST loop.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B933 HOTLink Receiver

Name	I/O	Description
Q_{0-7} (Q_{b-h})	TTL Out	Q_{0-7} Parallel Data Output. Q_{0-7} contain the most recently received data. These outputs change synchronously with CKR. When mode is HIGH, $Q_{0,1,...7}$ become $Q_{b,c,...h}$ respectively.
SC/$\overline{D}$ (Q_a)	TTL Out	Special Character/Data Select. SC/$\overline{D}$ indicates the context of received data. HIGH indicates a Control (Special Character) code, LOW indicates a Data character. When MODE is HIGH, SC/$\overline{D}$ acts as Q_a output.
RVS (Q_j)	TTL Out	Received Violation Symbol. A HIGH on RVS indicates that a code rule violation has been detected in the received data stream. A LOW shows that no error has been detected. In BIST mode, a LOW on RVS indicates correct operation of the Transmitter, Receiver, and link on a byte-by-byte basis. When MODE is HIGH, RVS acts as Q_j output.
$\overline{RDY}$	TTL Out	Data Output Ready. A LOW pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In BIST mode $\overline{RDY}$ will remain LOW for all but the last byte of a test loop and will pulse HIGH one byte time per BIST loop.
CKR	TTL Out	Clock Read. This byte rate clock output is phase and frequency aligned to the incoming serial data stream. $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	ECL in	Serial Data Input Select. This ECL 100K (+5V referenced) input selects INA or INB as the active data input. If A/$\overline{B}$ is HIGH, INA is connected to the shifter and signals connected to INA will be decoded. If A/$\overline{B}$ is LOW INB is selected.
INA±	Diff In	Serial Data Input A. The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of A/$\overline{B}$.
INB (INB+)	ECL in (Diff In)	Serial Data Input B. This pin is either a single-ended ECL data receiver (INB) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, INB becomes a single-ended ECL 100K (+5V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB−)	ECL in (Diff In)	Status Input. This pin is either a single-ended ECL status monitor input (SI) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, SI becomes a single-ended ECL 100K (+5V referenced) status monitor input.
SO	TTL Out	Status Out. SO is the TTL-translated output of SI. It is typically used to translate the Carrier Detect output from a fiber-optic receiver. When this pin is normally connected and loaded (without any external pull-up resistor), SO will assume the same logical level as SI and INB will become a single-ended ECL serial data input. If the status monitor translation is not desired, then SO may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
RF	TTL In	Reframe Enable. RF controls the Framer logic in the Receiver. When RF is held HIGH, each SYNC (K28.5) symbol detected in the shifter will frame the data that follows. When RF is held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.
REFCLK	TTL In	Reference Clock. REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK must be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency must be the same as the transmitter CKW frequency (within CKW ±0.1%).
MODE	3-Level In	Decoder Mode Select. The level on the MODE pin determines the decoding method to be used. When wired to GND, MODE selects 8B/10B decoding. When wired to V_{CC}, registered shifter contents bypass the decoder and are sent to Q_{a-j} directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW the Receiver awaits a D0.0 (sent once per BIST loop) character and begins a continuous test sequence that tests the functionality of the Transmitter, the Receiver, and the link connecting them. In BIST mode the status of the test can be monitored with $\overline{RDY}$ and RVS outputs. In normal use $\overline{BISTEN}$ is held HIGH or wired to V_{CC}.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground

CY7B923 HOTLink Transmitter Block Diagram Description

Input Register

The Input register holds the data to be processed by the HOTLink transmitter and allows the input timing to be made consistent with standard FIFOs. The Input register is clocked by CKW and loaded with information on the D_{0-7}, SC/$\overline{D}$, and SVS pins. Two enable inputs ($\overline{ENA}$ and $\overline{ENN}$) allow the user to choose when data is to be sent. Asserting $\overline{ENA}$ (Enable, active LOW) causes the inputs to be loaded on the rising edge of CKW. If $\overline{ENN}$ (Enable Next, active LOW) is asserted when CKW rises, the data present on the inputs on the next rising edge of CKW will be loaded into the input register. These two inputs allow proper timing and function for compatibility with either asynchronous FIFOs or clocked FIFOs without external logic, as shown in *Figure 2.*

In BIST mode, the Input register becomes the signature pattern generator by logically converting the parallel input register into a Linear Feedback Shift Register (LFSR). When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

Encoder

The Encoder transforms the input data held by the Input register into a form more suitable for transmission on a serial interface link. The code used is specified by ANSI X3T9.3 (Fibre Channel) and the IBM ESCON channel (code tables are at the end of this datasheet). The eight D_{0-7} data inputs are converted to either a Data symbol or a Special Character, depending upon the state of the SC/$\overline{D}$ input. If SC/$\overline{D}$ is HIGH, the data inputs represent a control code and are encoded using the Special Character code tables. If SC/$\overline{D}$ is LOW, the data inputs are converted using the Data code table. If a byte time passes with the inputs disabled, the Encoder will output a Special Character Comma K28.5 (or SYNC) that will maintain link synchronization. SVS input forces the transmission of a specified Violation symbol to allow the user to check error handling system logic in the controller.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller. This bypass is controlled by setting the MODE select pin HIGH. When in bypass mode, D_{a-j} (note that bit order is specified in Fibre Channel 8B/10B code) become the ten inputs to the Shifter, with D_a being the first bit to be shifted out.

Shifter

The Shifter accepts parallel data from the Encoder once each byte time and shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at ten (10) times the byte clock rate. Timing for the parallel transfer is controlled by the counter included in the Clock Generator and is not affected by signal levels or timing at the input pins.

OutA, OutB, OutC

The serial interface ECL output buffers (100K referenced to +5v) are the drivers for the serial media. They are all connected to the Shifter and contain the same serial data. Two of the output pairs (OUTA± and OUTB±) are controllable by the FOTO input and can be disabled by the system controller to force a logical zero (i.e., "light off") at the outputs. The third output pair (OUTC±) is not affected by FOTO and will supply a continuous data stream suitable for loop-back testing of the subsystem.

OUTA± and OUTB± will respond to FOTO input changes within a few bit times. However, since FOTO is not synchronized with the transmitter data stream, the outputs will be forced off or turned on at arbitrary points in a transmitted byte. This function is intended to augment an external laser safety controller and as an aid for Receiver PLL testing.

In wire-based systems, control of the outputs may not be required, and FOTO can be strapped LOW. The three outputs are intended to add system and architectural flexibility by offering identical serial bit streams with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to V_{CC} to disable and power down the unused output circuitry.

Clock Generator

The clock generator is an embedded phase-locked loop (PLL) that takes a byte-rate reference clock (CKW) and multiplies by ten (10) to create a bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the Input register. This clock must be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the HOTLink Transmitter/Receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the Input register and the Shifter.

The read pulse ($\overline{RP}$) is derived from the feedback counter used in the PLL multiplier. It is a byte-rate pulse stream with the proper phase and pulse widths to allow transfer of data from an asynchronous FIFO. Pulse width is independent of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The $\overline{RP}$ pulse stream will insure correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic to properly select the data encoding. Test logic is discussed in more detail in the CY7B923 HOTLink Transmitter Operating Mode Description.

CY7B933 HOTLink Receiver Block Diagram Description

Serial Data Inputs

This pair of differential line receivers are the inputs for the serial data stream. INA± or INB± can be selected with the A/$\overline{B}$ input. INA± is selected with A/$\overline{B}$ HIGH and INB± is selected with A/$\overline{B}$ LOW. The threshold of A/$\overline{B}$ is compatible with the ECL 100K signals from ECL fiber optic interface modules. TTL logic elements can be used to select the A or B inputs by adding a resistor pull-up to the TTL driver connected to A/$\overline{B}$. The differential threshold of INA± and INB± will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 20 db ($V_{DIF} \geq 50$mv) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K) with up to 1.2 volts of differential signal. The common mode tolerance will accommodate a wide range of signal termination voltages. The highest HIGH input that can be tolerated is $V_{IN} = V_{CC}$, and the lowest LOW input that can be interpreted correctly is V_{IN} = GND+2.0V.

ECL-TTL Translator

The function of the INB(INB+) input and the SI(INB−) input is defined by the connections on the SO output pin. If the ECL/TTL translator function is not required, the SO output is wired to V_{CC}. A sensor circuit will detect this connection and cause the inputs to become INB± (a differential line-receiver serial-data input). If the ECL/TTL translator function is required, the SO output is connected to its normal TTL load (typically one or more TTL inputs,

but no pull-up resistor) and the inputs become INB (single-ended ECL-100K serial-data input) and SI (single-ended ECL-100K status input).

This positive-referenced ECL-to-TTL translator is provided to eliminate external logic between an ECL fiber-optic interface module "carrier detect" output and the TTL input in the control logic. The input threshold is compatible with ECL 100K levels (+5V referenced). It can also be used as part of the link status indication logic for wire connected systems.

Clock Sync

The Clock Synchronizer function is performed by an embedded phase-locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the serial data transitions. This block contains the logic to transfer the data from the Shifter to the Decode register once every byte. The counter that controls this transfer is initialized by the Framer logic. CKR is a buffered output derived from the bit counter used to control Decode register and Output register transfers.

Clock output logic is designed so that when reframing causes the counter sequence to be interrupted, the period and pulse width of CKR will never be less than normal. Reframing may stretch the period of CKR by up to 90%, and either CKR Pulse Width HIGH or Pulse Width LOW may be stretched, depending on when reframe occurs.

The REFCLK input provides a byte-rate reference frequency to improve PLL acquisition time and limit unlocked frequency excursions of the CKR when no data is present at the serial inputs. The frequency of REFCLK is required to be within ±0.1% of the frequency of the clock that drives the transmitter CKW pin.

Framer

Framer logic checks the incoming bit stream for the pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3T9.3 symbol defined as a Special Character Comma (K28.5). When it is found, the free-running bit counter in the Clock Sync block is synchronously reset to its initial state, thus framing the data correctly on the correct byte boundaries.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. The RF input prevents this by inhibiting reframing during times when normal message data is present. When RF is held LOW, the HOTLink receiver will deserialize the incoming data without trying to reframe the data to incoming patterns. When RF rises, $\overline{\text{RDY}}$ will be inhibited until a K28.5 has been detected, after which $\overline{\text{RDY}}$ will resume its normal function. While RF is HIGH, it is possible that an error could cause misframing, after which all data will be corrupted. Likewise, a K28.7 followed by D11.x, D20.x, or an SVS (C0.7) followed by D11.x will cause erroneous framing. These sequences must be avoided while RF is HIGH.

If RF remains HIGH for greater than 2048 bytes, the framer converts to double-byte framing, requiring two K28.5 within 5 bytes.

Shifter

The Shifter accepts serial inputs from the Serial Data inputs one bit at a time, as clocked by the Clock Sync logic. Data is transferred to the Framer on each bit, and to the Decode register once per byte.

Decode Register

The Decode register accepts data from the Shifter once per byte as determined by the logic in the Clock Sync block. It is presented to the Decoder and held until it is transferred to the output latch.

Decoder

Parallel data is transformed from ANSI X3T9.3 8B/10B codes back to "raw data" in the Decoder. This block uses the standard decoder patterns shown in the Valid Data Characters and Valid Special Character Codes and Sequences sections of this datasheet. Data patterns are signaled by a LOW on the SC/$\overline{\text{D}}$ output and Special Character patterns are signaled by a HIGH on the SC/$\overline{\text{D}}$ output. Unused patterns or disparity errors are signaled as errors by a HIGH on the RVS output and by specific Special Character codes.

Output Register

The Output register holds the recovered data (Q_{0-7}, SC/$\overline{\text{D}}$, and RVS) and aligns it with the recovered byte clock (CKR). This synchronization insures proper timing to match a FIFO interface or other logic that requires glitch free and specified output behavior. Outputs are changed synchronously with the rising edge of CKR.

In BIST mode, this register becomes the signature pattern generator and checker by logically converting the parallel output register into a Linear Feedback Shift Register (LFSR) pattern generator. When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized, it checks each byte in the Decoder with each byte generated by the LFSR and shows errors at RVS. Patterns generated by the LFSR are compared after being buffered to the output pins and then fed back to the comparators, allowing test of the entire receive function.

In BIST mode, the LFSR is initialized by the first occurrence of the transmitter BIST loop start code D0.0 (D0.0 is sent only once per BIST loop). Once the BIST loop has been started, RVS will be HIGH for pattern mismatches between the received sequence and the internally generated sequence. Code rule violations or running disparity errors that occur as part of the BIST loop will not cause an error indication. $\overline{\text{RDY}}$ will pulse HIGH once per BIST loop and can be used to check test pattern progress. The receiver BIST generator can be reinitialized by leaving and re-entering BIST mode.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic for the decoder. Test logic is discussed in more detail in the CY7B933 HOTLink Receiver Operating Mode Description.

CY7B923/CY7B933 Electrical Characteristics Over the Operating Range[1]

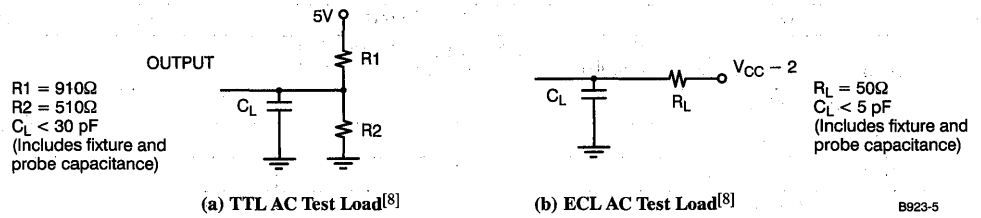
Parameter	Description	Test Conditions	Min.	Max.	Unit
Transmitter TTL-Compatible Pins: D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, CKW, FOTO, $\overline{BISTEN}$, $\overline{RP}$ Receiver TTL-Compatible Pins: Q_{0-7}, SC/$\overline{D}$, RVS, $\overline{RDY}$, CKR, REFCLK, $\overline{RF}$, $\overline{BISTEN}$, SO					
V_{OHT}	Output HIGH Voltage	I_{OH} = − 2 mA	2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA		0.45	V
I_{OST}	Output Short Circuit Current	V_{OUT} =0V[2]	−15	−90	mA
V_{IHT}	Input HIGH Voltage		2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage		− 0.5	0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{CC}	−10	+10	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0V		− 500	µA
Transmitter ECL-Compatible Output Pins: OUTA+, OUTA−, OUTB+, OUTB−, OUTC+, OUTC−					
V_{OHE}[3]	Output HIGH Voltage (V_{CC} referenced)	Load = 50 ohms to V_{CC} − 2V	V_{CC}−1.03	V_{CC}−0.83	V
V_{OLE}	Output LOW Voltage (V_{CC} referenced)	Load = 50 ohms to V_{CC} − 2V	V_{CC}−1.81	V_{CC}− 1.68	V
V_{ODIF}	Output Differential Voltage ($OUT+_{HIGH}$) to ($OUT-_{LOW}$) or ($OUT+_{LOW}$) to ($OUT-_{HIGH}$)	Load = 50 ohms to V_{CC} − 2V	0.6		V
Receiver ECL-Compatible Input Pins: A/$\overline{B}$, SI, INB					
V_{IHE}	Input HIGH Voltage		V_{CC}−1.17	V_{CC}	V
V_{ILE}	Input LOW Voltage		2.0	V_{CC}−1.48	V
I_{IHE}[4]	Input HIGH Current	V_{IN} = V_{IHE} Max.		+500	µA
I_{ILE}[4]	Input LOW Current	V_{IN} = V_{ILL} Min.	+0.5		µA
Differential Line Receiver Input Pins: INA+, INA−, INB+, INB−					
V_{DIFF}	Input Differential Voltage |(IN+) − (IN−)|		50	1200	mV
V_{IHH}	Highest Input HIGH Voltage			V_{CC}	V
V_{ILL}	Lowest Input LOW Voltage		2.0		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.		750	µA
I_{ILL}[5]	Input LOW Current	V_{IN} = V_{ILL} Min.	−200		µA
Miscellaneous					
I_{CCT}[6]	Transmitter Power Supply Current	V_{CC} = Max., T_A = Max., Freq. = Max. (One ECL output pair loaded with 50 ohms to V_{CC} − 2.0V, others tied to V_{CC})		85	mA
I_{CCR}	Receiver Power Supply Current	V_{CC} = Max., T_A = Max., Freq. = Max., RF = LOW		155	mA

Capacitance[7]

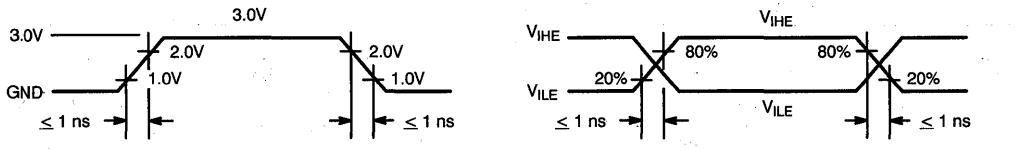
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:
1. See the last page of this specification for Group A subgroup testing information.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Specified only for temperatures above 0°C.
4. Applies to A/$\overline{B}$ only.
5. Input currents are always positive at all voltages above V_{CC}/2.
6. I_{CCT} includes current into V_{CCQ} (pin 9 and pin 22) only. Current into V_{CCN} is determined by ECL load currents, typically 30 mA with 50 ohms to V_{CC} −2V. Each additional enabled ECL pair adds 5 mA to I_{CCT} and additional load current to V_{CCN} as described.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) TTL AC Test Load[8] **(b) ECL AC Test Load**[8] B923-5



(c) TTL Input Test Waveform B923-6 **(d) ECL Input Test Waveform** B923-7

Transmitter Switching Characteristics Over the Operating Range[1]

Parameter	Description	7B923		Unit
		Min.	Max.	
t_{CKW}	Write Clock Cycle	30.3	62.5	ns
t_B	Bit Time[9]	3.03	6.25	ns
t_{CPWH}	CKW Pulse Width HIGH	5		ns
t_{CPWL}	CKW Pulse Width LOW	5		ns
t_{SD}	Data Set-Up Time[10]	5		ns
t_{HD}	Data Hold Time[10]	0		ns
t_{SENP}	Enable Set-Up Time (to insure correct $\overline{RP}$)[11]	$6t_B + 8$	$10t_B$	ns
t_{HENP}	Enable Hold Time (to insure correct $\overline{RP}$)[11]	0		ns
t_{PDR}	Read Pulse Rise Alignment[12]	−4	2	ns
t_{PPWH}	Read Pulse HIGH[12]	$4t_B-3$		ns
t_{PDF}	Read Pulse Fall Alignment[12]	$6t_B-3$		ns
t_{RISE}	ECL Output Rise Time 20–80% (ECL Test Load)		1.2	ns
t_{FALL}	ECL Output Fall Time 80–20% (ECL Test Load)		1.2	ns

Notes:

8. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
9. Transmitter t_B is calculated as $t_{CKW}/10$. The byte rate is one tenth of the bit rate.
10. Data includes D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, and $\overline{BISTEN}$. t_{SD} and t_{HD} minimum timing assures correct data load on rising edge of CKW, but not $\overline{RP}$ function or timing.
11. t_{SENP} and t_{HENP} timing insures correct $\overline{RP}$ function and correct data load on the rising edge of CKW.
12. Loading on $\overline{RP}$ pin is ≤2 mA and ≤15 pF.

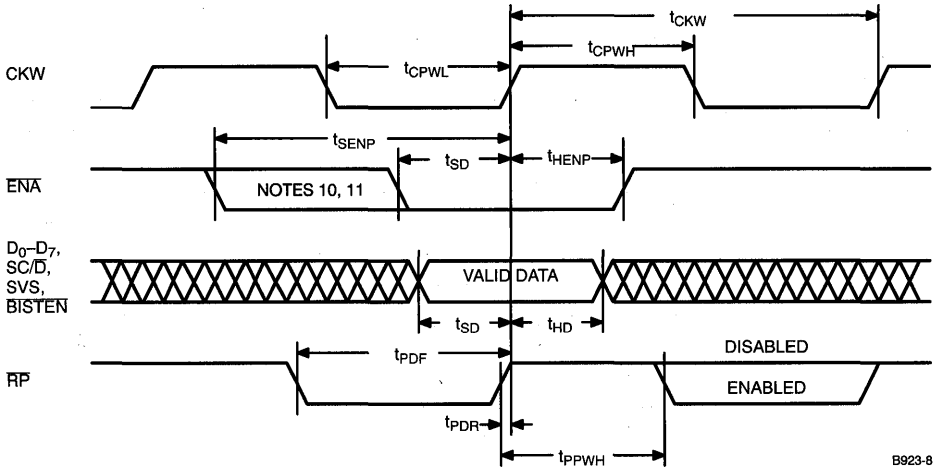
Receiver Switching Characteristics Over the Operating Range[1]

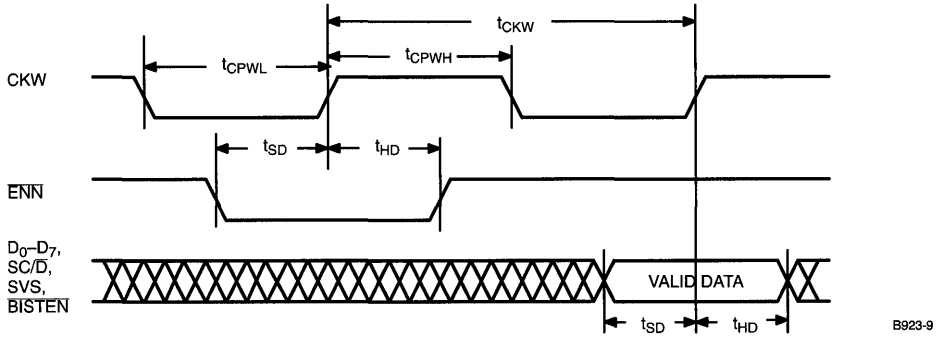
Parameter	Description	7B933		Unit
		Min.	Max.	
t_{CKR}	Read Clock Period (No Serial Data Input), REFCLK as Reference[13]	−1	+1	%
t_B	Bit Time[14]	3.03	6.25	ns
t_{CPRH}	Read Clock Pulse HIGH	$5t_B-3$		ns
t_{CPRL}	Read Clock Pulse LOW	$5t_B-3$		ns
t_{RH}	$\overline{RDY}$ Hold Time	t_B-3		ns
t_{PRF}	$\overline{RDY}$ Pulse Fall to CKR Rise	$5t_B-3$		ns
t_{PRH}	$\overline{RDY}$ Pulse Width HIGH	$4t_B-3$		ns
t_A	Data Access Time[15, 16]	$2t_B-3$	$2t_B+3$	ns
t_{ROH}	Data Hold Time[15, 16]	t_B-3		ns
t_{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter[17]	−0.1	+0.1	%
t_{CPXH}	REFCLK Clock Pulse HIGH	5		ns
t_{CPXL}	REFCLK Clock Pulse LOW	5		ns
t_{DS}	Propagation Delay SI to SO (note ECL and TTL thresholds)[18]		20	ns

Notes:

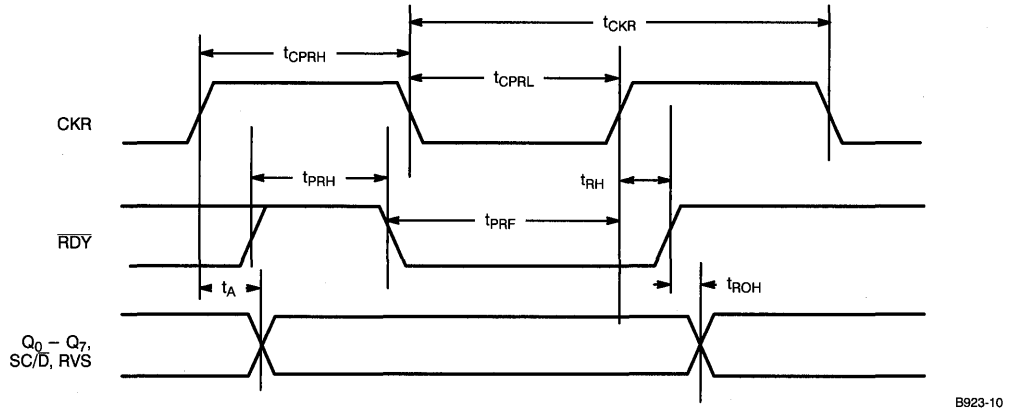
13. The period of t_{CKR} will match the period of the transmitter CKW when the receiver is receiving serial data. When data is interrupted, CKR may drift to one of the range limits above.
14. Receiver t_B is calculated as $t_{CKR}/10$ if no data is being received, or $t_{CKW}/10$ if data is being received. See note 9.
15. Data includes Q_{0-7}, SC/$\overline{D}$, and RVS.
16. t_A and t_{ROH} specifications are only valid if all outputs (CKR, $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS) are loaded with similar DC and AC loads.
17. REFCLK has no phase or frequency relationship with CKR and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within 0.1% of the transmitter CKW frequency, necessitating a ±500-PPM crystal.
18. The ECL switching threshold is the midpoint between the ECL–V_{OH}, and V_{OL} specification (approximately V_{CC} − 1.35V). The TTL switching threshold is 1.5V.

Switching Waveforms for the CY7B923 HOTlink Transmitter

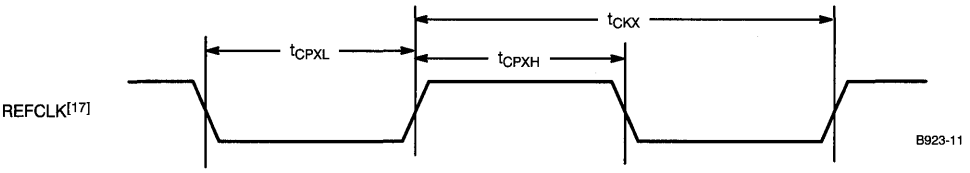




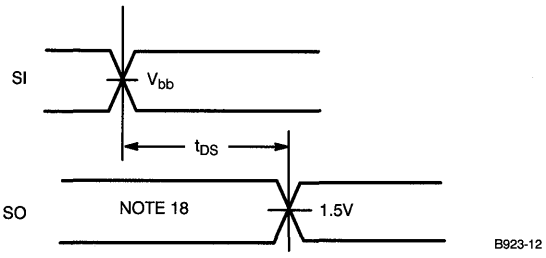
Switching Waveforms for the CY7B933 HOTlink Receiver



B923-10



B923-11



B923-12

CY7B923 HOTlink Transmitter Operating Mode Description

The CY7B923 Transmitter operating with the CY7B933 Receiver forms a general-purpose data communication subsystem capable of transporting user data at up to 33 Mbytes per second over several types of serial interface media. In normal operation, the Transmitter can operate in either of two modes. The Encoded mode allows a user to send and receive eight (8) bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed in an external protocol controller.

In either mode, data is loaded into the input register of the Transmitter on the rising edge of CKW. The input timing and functional response of the Transmitter input can be made to match timing and function of either an asynchronous FIFO or a clocked FIFO by an appropriate connection of input signals (See *Figure 2*). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

Encoded Mode Operation

In Encoded mode the input data is interpreted as eight bits of data ($D_0 - D_7$), a context control bit ($SC/\overline{D}$), and a system diagnostic input bit (SVS). If the context of the data is to be normal message data, the $SC/\overline{D}$ input will be LOW, and the data will be encoded using the valid data character set described in the Valid Data Characters section of this datasheet. If the context of the data is to be control or protocol information, the $SC/\overline{D}$ input will be HIGH, and the data will be encoded using the valid special character set described in the Valid Special Character Codes and Sequences section. Special characters include all protocol characters necessary to encode packets for Fibre Channel, ESCON, proprietary systems, and diagnostic purposes.

The diagnostic characters and sequences available as Special Characters include those for Fibre Channel link testing, as well as codes to be used for testing system response to link errors and timing. A Violation symbol can be explicitly sent as part of a user data packet (i.e., send C0.7; D_{7-0} = 111 00000 and $SC/\overline{D}$ = 1), or it can be sent in response to an external system using the SVS input. This will allow system diagnostic logic to evaluate the errors in an unambiguous manner, and will not require any modification to the transmission interface to force transmission errors for testing purposes.

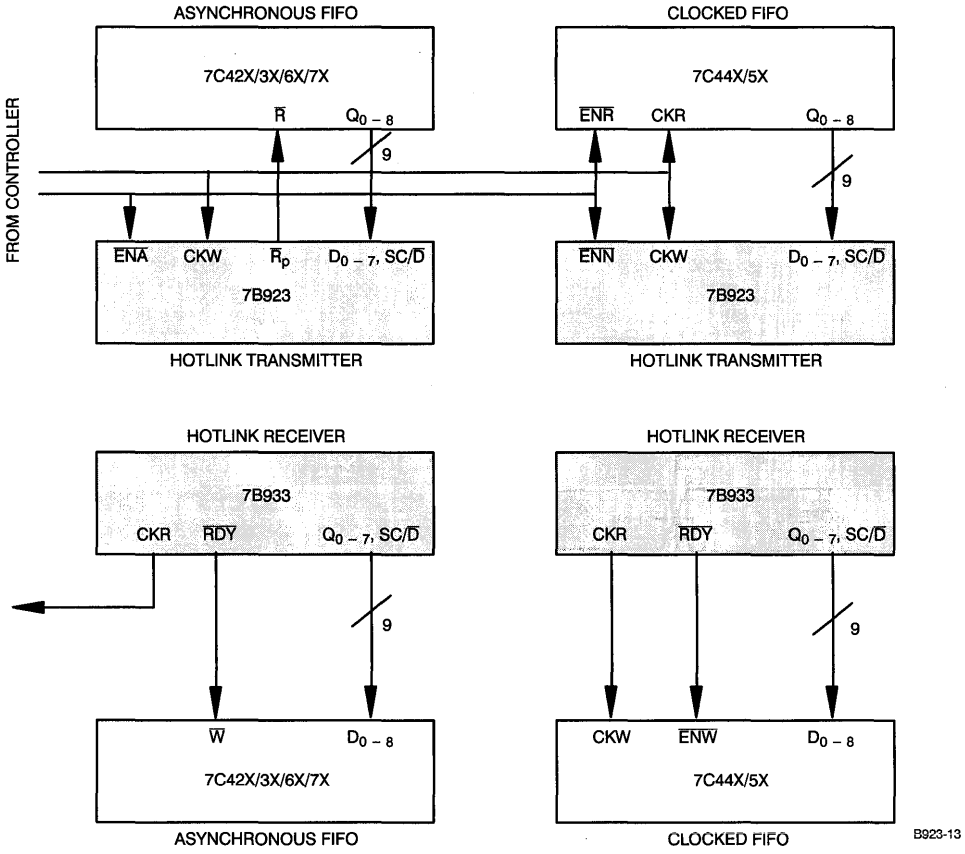


Figure 2. Seamless FIFO Interface

Bypass Mode Operation

In Bypass mode the input data is interpreted as ten (10) bits (D_{b-h}), SC/$\overline{D}$ (D_a), and SVS (D_j) of pre-encoded transmission data to be serialized and sent over the link. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per byte), and that it be compatible with the transmission media.

Data loaded into the Input register on the rising edge of CKW will be loaded into the Shifter on the subsequent rising edges of CKW. It will then be shifted to the outputs one bit at a time using the internal clock generated by the clock generator. The first bit of the transmission character (D_a) will appear at the output (OUTA±, OUTB±, and OUTC±) after the next CKW edge.

While in either the Encoded mode or Bypass mode, if a CKW edge arrives when the inputs are not enabled ($\overline{ENA}$ and $\overline{ENN}$ both HIGH), the Encoder will insert a pad character K28.5 (e.g., C5.0) to maintain proper link synchronization (in Bypass mode the proper sense of running disparity cannot be guaranteed for the first pad character, but is correct for all pad characters that follow). This automatic insertion of pad characters can be inhibited by insuring that the Transmitter is always enabled (i.e., $\overline{ENA}$/$\overline{ENN}$ is hardwired LOW).

ECL Output Functional and Connection Options

The three pairs of ECL outputs all contain the same information and are intended for use in systems with multiple connections. Each output pair may be connected to a different serial media, each of which may be a different length, link type, or interface technology. For systems that do not require all three output pairs, the unused pairs should be wired to V_{CC} to minimize the power dissipated by the output circuit, and to minimize unwanted noise generation.

In systems that require the outputs to be shut off during some periods when link transmission is prohibited (e.g., for laser safety functions), the FOTO input can be asserted. While it is possible to insure that the output state of the ECL drivers is LOW (i.e., light is off) by sending all 0's in Bypass mode, it is often inconvenient to insert this level of control into the data transmission channel, and it is impossible in Encoded mode. FOTO is provided to simplify and augment this control function (typically found in laser-based transmission systems). FOTO will force OUTA+ and OUTB+ to go LOW, OUTA− and OUTB− to go HIGH, while allowing OUTC± to continue to function normally (OUTC is typically used as a diagnostic feedback and cannot be disabled). This separation of function allows various system configurations without undue load on the control function or data channel logic.

Transmitter Serial Data Characteristics

The CY7B923 HOTLink Transmitter serial output conforms to the requirements of the Fibre Channel specification. The serial data output is controlled by an internal Phase-Locked Loop that multiplies the frequency of CKW by ten (10) to maintain the proper bit clock frequency. The jitter characteristics (including both PLL and logic components) are shown below:

Deterministic Jitter (D_j) < 8% of t_B. Typically measured while sending a continuous K28.5 (C5.0).

Random Jitter (R_j) < 8% of t_B. Typically measured while sending a continuous K28.7 (C7.0).

Transmitter Test Mode Description

The CY7B923 Transmitter offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver, and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 3*.

BIST Mode

BIST mode functions as follows:

1. Set $\overline{BISTEN}$ LOW to begin test pattern generation. Transmitter begins sending bit rate ...1010...
2. Set either $\overline{ENA}$ or $\overline{ENN}$ LOW to begin pattern sequence generation (use of the Enable pin not being used for normal FIFO or system interface can minimize logic delays between the controller and transmitter).
3. Allow the Transmitter to run through several BIST loops or until the Receiver test is complete. $\overline{RP}$ will pulse LOW once per BIST loop, and can be used by an external counter to monitor the number of test pattern loops.
4. When testing is completed, set $\overline{BISTEN}$ HIGH and $\overline{ENA}$ and $\overline{ENN}$ HIGH and resume normal function.

Note: It may be advisable to send violation characters to test the RVS output in the Receiver. This can be done by explicitly sending a violation with the SVS input, or allowing the transmitter BIST loop to run while the Receiver runs in normal mode. The BIST loop includes deliberate violation symbols and will adequately test the RVS function.

BIST mode is intended to check the entire function of the Transmitter (except the Transmitter input pins and the bypass function in the Encoder), the serial link, and the Receiver. It augments normal factory ATE testing and provides the designer with a rigorous test mechanism to check the link transmission system without requiring any significant system overhead.

While in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{BISTEN}$ = LOW causes the Transmitter to switch to Encoded mode and begin sending the BIST pattern, as if MODE = LOW. When $\overline{BISTEN}$ returns to HIGH, the Transmitter resumes normal BYPASS operation. In Test mode the BIST function works as in the Normal mode.

Test Mode

The MODE input pin selects between three transmitter functional modes. When wired to V_{CC}, the $D_{(a-j)}$ inputs bypass the Encoder and load directly from the Input register into the Shifter. When wired to GND, the inputs D_{0-7}, SVS, and SC/$\overline{D}$ are encoded using the Fibre Channel 8B/10B codes and sequences (shown at the end of this datasheet). Since the Transmitter is usually hard wired to Encoded or Bypass mode and not switched between them, a third function is provided for the MODE pin. Test mode is selected by floating the MODE pin (internal resistors hold the MODE pin at $V_{CC}/2$). Test mode is used for factory or incoming device test.

Test mode causes the Transmitter to function in its Encoded mode, but with OutA+/OutB+ (used as a differential test clock input) as the bit rate clock input instead of the internal PLL-generated bit clock. In this mode, inputs are clocked by CKW and transfers between the Input register and Shifter are timed by the internal counters. The phase and pulse width of $\overline{RP}$ are controlled by phases of the bit counter (PLL feedback counter) as in Normal mode. Input and output patterns can be synchronized with internal logic by observing the state of $\overline{RP}$ or the device can be initialized to match an ATE test pattern using the following technique:

1. Assert Test mode for several test clock cycles to initialize internal logic.
2. Assert $\overline{BISTEN}$ for one or more test clock cycles.

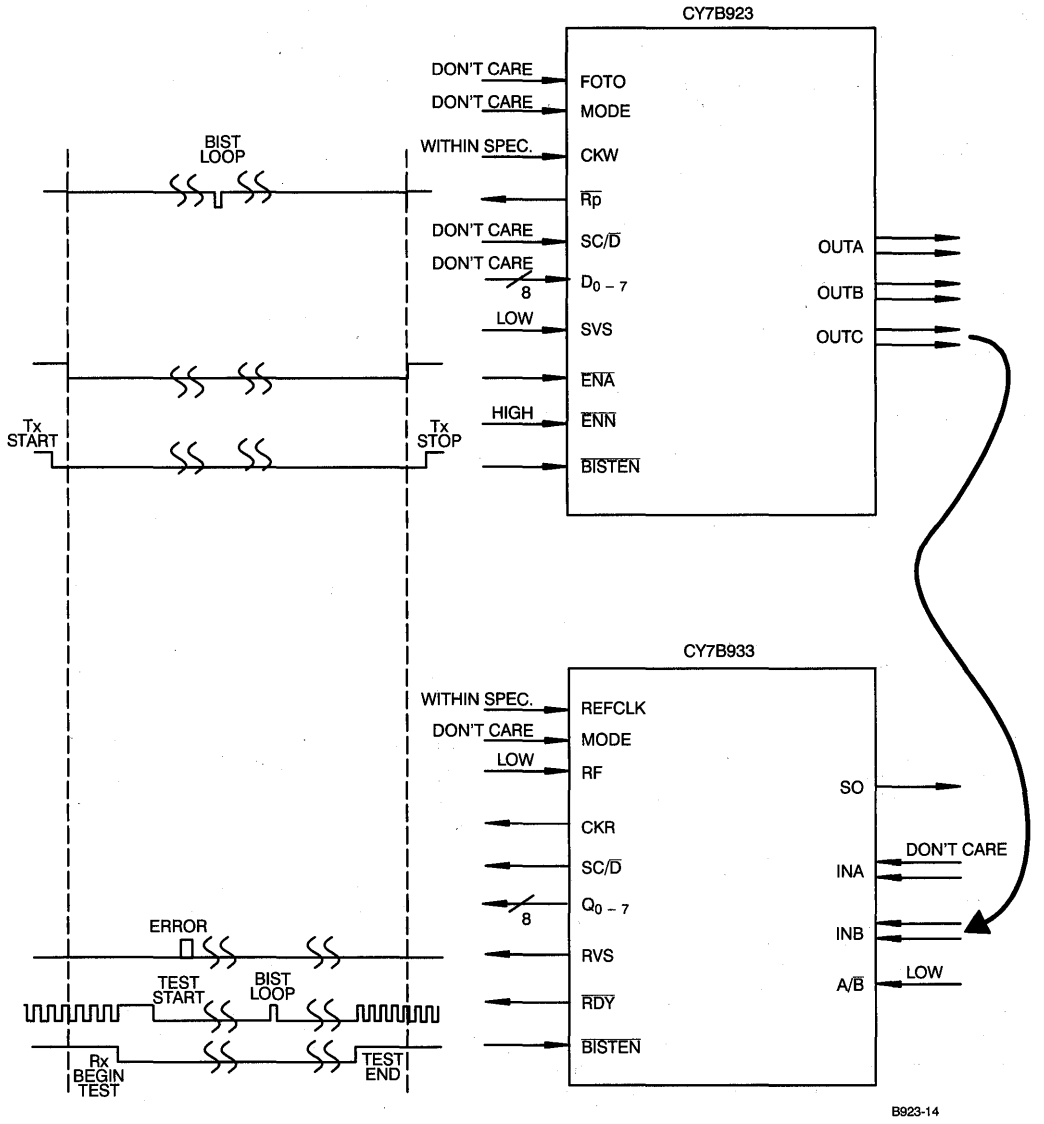


Figure 3. Built-In Self-Test Illustration

3. Deassert $\overline{\text{BISTEN}}$ and the next test clock cycle will reset the counter.
4. Proceed with pattern, voltage, and timing tests.

Test mode is intended to allow logical, DC, and AC testing of the Transmitter without requiring that the tester check output data patterns at the bit rate, or accommodate the PLL lock, tracking, and frequency range characteristics that are required when the HOTLink part operates in its normal mode. To use OutA+/OutB+ as the test clock input, the FOTO input is held HIGH while in Test mode. This forces the two outputs to go to an "ECL LOW," which can be ignored while the test system creates a differential input signal at some higher voltage.

CY7B933 HOTlink Receiver Operating Mode Description

The CY7B933 Receiver operating with the CY7B923 Transmitter forms a general-purpose data communication subsystem capable of transporting user data at up to 33 Mbytes per second over several types of serial interface media. In normal user operation, the Receiver can operate in either of two modes. The Encoded mode allows a user system to send and receive 8-bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed by an external protocol controller.

In either mode, serial data is received at one of the differential line receiver inputs and routed to the Shifter and the Clock Synchronizer. The PLL in the Clock Sync aligns the internally generated bit rate clock with the incoming data stream and clocks the data into the shifter. At the end of a byte time (ten bit times), the data accumulated in the shifter is transferred to the Decode register.

To properly align the incoming bit stream to the intended byte boundaries, the bit counter in Clock Sync must be initialized. The Framer logic block checks the incoming bit stream for the unique pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3T9.3 symbol defined as "Special Character Comma" (K28.5). Once K28.5 is found, the free running bit counter in the Clock Sync block is synchronously reset to its initial state, thus "framing" the data to the correct byte boundaries.

Since noise-induced errors can cause the incoming data to be corrupted, and since many combinations of error and legal data can create an alias K28.5, an option is included to disable resynchronization of the bit counter. The Framer will be inhibited when the RF input is held LOW. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, and $\overline{RDY}$ will resume its normal function. Data will continue to flow through the Receiver while $\overline{RDY}$ is inhibited.

Encoded Mode Operation

In Encoded mode the serial input data is decoded into eight bits of data ($Q_0 - Q_7$), a context control bit (SC/$\overline{D}$), and a system diagnostic output bit (RVS). If the pattern in the Decode register is found in the Valid Data Characters table, the context of the data is decoded as normal message data and the SC/$\overline{D}$ output will be LOW. If the incoming bit pattern is found in the Valid Special Character Codes and Sequences table, it is interpreted as "control" or "protocol information," and the SC/$\overline{D}$ output will be HIGH. Special characters include all protocol characters defined for use in packets for Fibre Channel, ESCON, and other proprietary and diagnostic purposes.

The Violation symbol that can be explicitly sent as part of a user data packet (i.e., Transmitter sending C0.7; D_{7-0} = 111 00000 and SC/$\overline{D}$ = 1; or SVS = 1) will be decoded and indicated in exactly the same way as a noise-induced error in the transmission link. This function will allow system diagnostics to evaluate the error in an unambiguous manner, and will not require any modification to the receiver data interface for error-testing purposes.

Bypass Mode Operation

In Bypass mode the serial input data is not decoded, and is transferred directly from the Decode register to the Output register's 10 bits ($Q_{(a-j)}$). It is assumed that the data has been pre-encoded prior to transmission, and will be decoded in subsequent logic external to HOTLink. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per byte) and that it be compatible with the transmission media.

The framer function in Bypass mode is identical to Encoded mode, so a K28.5 pattern can still be used to re-frame the serial bit stream.

Parallel Output Function

The 10 outputs (Q_{0-7}, SC/$\overline{D}$, and RVS) all transition simultaneously, and are aligned with $\overline{RDY}$ and CKR with timing allowances to interface directly with either an asynchronous FIFO or a clocked FIFO. Typical FIFO connections are shown in *Figure 2.*

Data outputs can be clocked into the system using either the rising or falling edge of CKR, or the rising or falling edge of $\overline{RDY}$. If CKR is used, $\overline{RDY}$ can be used as an enable for the receiving logic. A LOW pulse on $\overline{RDY}$ shows that new data has been received and is ready to be delivered. The signal on $\overline{RDY}$ is a 60%–LOW duty cycle byte-rate pulse train suitable for the write pulse in asynchronous FIFOs such as the CY7C42X, or the enable write input on Clocked FIFOs such as the CY7C44X. HIGH on $\overline{RDY}$ shows that the received data appearing at the outputs is the null character (normally inserted by the transmitter as a pad between data inputs) and should be ignored.

When the Transmitter is disabled it will continuously send pad characters (K28.5). To assure that the receive FIFO will not be overfilled with these dummy bytes, the $\overline{RDY}$ pulse output is inhibited during fill strings. Data at the Q_{0-7} outputs will reflect the correct received data, but will not appear to change, since a string of K28.5s all are decoded as Q_{7-0} = 000 00101 and SC/$\overline{D}$ = 1 (C5.0). When new data appears (not K28.5), the $\overline{RDY}$ output will resume normal function. The "last" K28.5 will be accompanied by a normal $\overline{RDY}$ pulse.

Fill characters are defined as any K28.5 followed by another K28.5. All fill characters will not cause $\overline{RDY}$ to pulse. Any K28.5 followed by any other character (including violation or illegal characters) will be interpreted as usable data and will cause $\overline{RDY}$ to pulse.

As noted above, $\overline{RDY}$ can also be used as an indication of correct framing of received data. While the Receiver is awaiting receipt of a K28.5 with RF HIGH, the $\overline{RDY}$ outputs will be inhibited. When $\overline{RDY}$ resumes, the received data will be properly framed and will be decoded correctly. In Bypass mode with RF HIGH, $\overline{RDY}$ will pulse once for each K28.5 received.

Code rule violations and reception errors will be indicated as follows:

	RVS	SC/$\overline{D}$	Qouts	Name
1. Good Data code received with good RD	0	0	00–FF	D0.0–31.7
2. Good Special Character code received with good RD	0	1	00–0B	C0.0–11.0
3. K28.7 immediately following K28.1 (ESCON Connect_SOF)	0	1	27	C7.1
4. K28.7 immediately following K28.5 (ESCON Passive_SOF)	0	1	47	C7.2
5. Unassigned code received	1	1	E0	C0.7
6. –K28.5+ received when RD was +	1	1	E1	C1.7
7. +K28.5– received when RD was –	1	1	E2	C2.7
8. Good code received with wrong RD	1	1	E4	C4.7

Receiver Serial Data Requirements

The CY7B933 HOTLink Receiver serial input capability conforms to the requirements of the Fibre Channel specification. The serial data input is tracked by an internal Phase-Locked Loop that is used to recover the clock phase and to extract the data from the serial bit

stream. Jitter tolerance characteristics (including both PLL and logic component requirements) are shown below:

Deterministic Jitter tolerance (D_j) >31% of t_B. Typically measured while receiving data carried by a bandwidth-limited channel (e.g., a coaxial transmission line) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Random Jitter tolerance (R_j) > 42% of t_B. Typically measured while receiving data carried by a random-noise-limited channel (e.g., a fiber-optic transmission system with low light levels) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Total Jitter tolerance >70% of t_B. Total of $D_j + R_j$.

PLL-Acquisition time <2500-bit times from worst-case phase or frequency change in the serial input data stream, to receiving data within BER objective of 10^{-12}. Stable power supplies within specifications, stable REFCLK input frequency and normal data framing protocols are assumed.

Receiver Test Mode Description

The CY7B933 Receiver offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 3*.

BIST Mode

BIST Mode function is as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to enable self-test generation and await $\overline{\text{RDY}}$ LOW indicating that the initialization code has been received.
2. Monitor RVS and check for any byte time with the pin HIGH to detect pattern mismatches. $\overline{\text{RDY}}$ will pulse HIGH once per BIST loop, and can be used by an external counter to monitor test pattern progress. Q_{0-7} and SC/$\overline{\text{D}}$ will show the expected pattern and may be useful for debug purposes.
3. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and resume normal function.

Note: A specific test of the RVS output may be required to assure an adequate test. To perform this test, it is only necessary to have the Transmitter send violation (SVS = HIGH) for a few bytes before beginning the BIST test sequence. Alternatively, the Receiver could enter BIST mode after the Transmitter has begun sending BIST loop data, or be removed before the Transmitter finishes sending BIST loops, each of which contain several deliberate violations and should cause RVS to pulse HIGH.

BIST mode is intended to check the entire function of the Transmitter, serial link, and Receiver. It augments normal factory ATE testing and provides the user system with a rigorous test mechanism to check the link transmission system, without requiring any significant system overhead.

When in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{\text{BISTEN}}$ = LOW causes the Receiver to switch to Encoded mode and begin checking the decoded received data of the BIST pattern, as if MODE = LOW. When $\overline{\text{BISTEN}}$ returns to HIGH, the Receiver resumes normal Bypass operation. In Test mode the BIST function works as in the normal mode.

Test Mode

The MODE input pin selects between three receiver functional modes. When wired to V_{CC}, the Shifter contents bypass the Decoder and go directly from the Decoder latch to the Q_{a-j} inputs of the Output latch. When wired to GND, the outputs are decoded using the 8B/10B codes shown at the end of this datasheet and become Q_{0-7}, RVS, and SC/$\overline{\text{D}}$. The third function is Test mode, used for factory or incoming device test. This mode can be selected by leaving the MODE pin open (internal circuitry forces the open pin to $V_{CC}/2$).

Test mode causes the Receiver to function in its Encoded mode, but with INB (INB+) as the bit rate Test clock instead of the Internal PLL generated bit clock. In this mode, transfers between the Shifter, Decoder register and Output register are controlled by their normal logic, but with an external bit rate clock instead of the PLL (the recovered bit clock). Internal logic and test pattern inputs can be synchronized by sending a SYNC pattern and allowing the Framer to align the logic to the bit stream. The flow is as follows:

1. Assert Test mode for several test clock cycles to establish normal counter sequence.
2. Assert RF to enable reframing.
3. Input a repeating sequence of bits representing K28.5 (Sync).
4. $\overline{\text{RDY}}$ falling shows the byte boundary established by the K28.5 input pattern.
5. Proceed with pattern, voltage and timing tests as is convenient for the test program and tester to be used.

(While in Test mode and in BIST mode with RF HIGH, the Q_{0-7}, RVS, and SC/$\overline{\text{D}}$ outputs reflect various internal logic states and not the received data.)

Test mode is intended to allow logical, DC, and AC testing of the Receiver without requiring that the tester generate input data at the bit rate or accommodate the PLL lock, tracking and frequency range characteristics that are required when the part operates in its normal mode.

X3T9.3 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and

h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation)

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name  D5.2
      Bits: ABCDE FGH
            10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
Bits: abcdei  fghj
      101001  0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and the SC/$\overline{D}$ pin is LOW) or a Special Character (c is set to K, and the SC/$\overline{D}$ pin is HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note: This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440–451 (September, 1983).

U.S. Patent 4,488,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical Level (FC_PH/92–001R3.0, X3T9.3/92–092). Working draft proposed for American National Standard for Information Systems, Rev 3.0 June 16, 1992.

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables shall be used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" shall be transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i shall be transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD–" or "Current RD+"). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter shall calculate a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3T9.3.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver shall decide whether the Transmission Character is valid or invalid according to the following rules and tables and shall calculate a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity shall be used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character shall be calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks shall be calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at

the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.

3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table shall be found for the Valid Data byte or the Special Character byte for which a Transmission Character is to be generated (encoded). The current value of the Transmitter's running disparity shall be used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity shall be calculated. This new value shall be used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 1* shows naming notations and examples of valid transmission characters.

Table 1. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	000101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity shall be searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character shall be used to calculate a new value of running disparity. The new value shall be used as the Receiver's current running disparity for the next received Transmission Character.

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 2* shows an example of this behavior.

Table 2. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Valid Data Characters (SC/$\overline{D}$ = LOW)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.2	010	11111	101011	0101	010100	0101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.4	100	00110	011001	1101	011001	0010
D7.4	100	00111	111000	1101	000111	0010
D8.4	100	01000	111001	0010	000110	1101
D9.4	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

Valid Special Character Codes and Sequences (SC/$\overline{D}$ = HIGH)[19, 20]

			Bits		Current RD−		Current RD+	
S.C. Byte Name	**S.C. Code Name**		**HGF**	**EDCBA**	**abcdei**	**fghj**	**abcdei**	**fghj**
K28.0	C0.0	(C00)	000	00000	001111	0100	110000	1011
K28.1	C1.0	(C01)	000	00001	001111	1001	110000	0110
K28.2	C2.0	(C02)	000	00010	001111	0101	110000	1010
K28.3	C3.0	(C03)	000	00011	001111	0011	110000	1100
K28.4	C4.0	(C04)	000	00100	001111	0010	110000	1101
K28.5	C5.0	(C05)	000	00101	001111	1010	110000	0101
K28.6	C6.0	(C06)	000	00110	001111	0110	110000	1001
K28.7	C7.0	(C07)	000	00111	001111	1000	110000	0111
K23.7	C8.0	(C08)	000	01000	111010	1000	000101	0111
K27.7	C9.0	(C09)	000	01001	110110	1000	001001	0111
K29.7	C10.0	(C0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111
Idle	C0.1	(C20)	001	00000	-K28.5+,D21.4,D21.5,D21.5,repeat[21]			
R_RDY	C1.1	(C21)	001	00001	-K28.5+,D21.4,D10.2,D10.2,repeat[22]			
EOFxx	C2.1	(C22)	001	00010	-K28.5,Dn.xxx0[23]		+K28.5,Dn.xxx1[23]	
	Follows K28.1 for ESCON Connect-SOF (Rx indication only)							
C-SOF	C7.1	(C27)	001	00111	001111	1000	110000	0111
	Follows K28.5 for ESCON Passive-SOF (Rx indication only)							
P-SOF	C7.2	(C47)	010	00111	001111	1000	110000	0111
					Code Rule Violation and SVS Tx Pattern			
Exception	C0.7	(CE0)	111	00000	100111	1000[24]	011000	0111[24]
-K28.5	C1.7	(CE1)	111	00001	001111	1010[25]	001111	1010[25]
+K28.5	C2.7	(CE2)	111	00010	110000	0101[26]	110000	0101[26]
					Running Disparity Violation Pattern			
Exception	C4.7	(CE4)	111	00100	110111	0101[27]	001000	1010[27]

Notes:

19. All codes not shown are reserved.
20. Notation for Special Character Byte Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn=the specified value between 00 and FF).
21. C0.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D21.5, D21.5, (repeat all four bytes)... defined in X3T9.3 as the primitive signal "Idle word." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

Notes (continued):

22. C1.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D10.2, D10.2,(repeat all four bytes)... defined in X3T9.3 as the primitive signal "Receiver_Ready (R_RDY)." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7 and the subsequent bytes are decoded as data.

23. C2.1 = Transmit either −K28.5+ or +K28.5− as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (−) the LSB becomes 1. This modification allows construction of X3T9.3 "EOF" frame delimiters wherein the second data byte is determined by the Current RD.

    For example, to send "EOFdt" the controller could issue the sequence C2.1−D21.4− D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D21.4−D21.4−D21.4 or K28.5−D21.5−D21.4−D21.4 based on Current RD. Likewise to send "EOFdti" the controller could issue the sequence C2.1−D10.4−D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D10.4−D21.4−D21.4 or K28.5−D10.5−D21.4− D21.4 based on Current RD.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

24. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. Transmission of this Special Character has the same effect as asserting SVS = HIGH.

    The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.

25. C1.7 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if −K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.

26. C2.7 = Transmit Positive K28.5 (+K28.5−) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD−, otherwise K28.5 is decoded as C5.0 or C1.7.

27. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation.

    The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B923−DC	D22	28-Lead (300-Mil) CerDIP	Commercial
CY7B923−JC	J64	28-Lead Plastic Leaded Chip Carrier	
CY7B923−LC	L64	28-Square Leadless Chip Carrier	
CY7B923−PC	P21	28-Lead (300-Mil) Molded DIP	
CY7B923−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B923−PI	P21	28-Lead (300-Mil) Molded DIP	
CY7B923−DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7B923−LMB	L64	28-Square Leadless Chip Carrier	

Ordering Code	Package Name	Package Type	Operating Range
CY7B933−DC	D22	28-Lead (300-Mil) CerDIP	Commercial
CY7B933−JC	J64	28-Lead Plastic Leaded Chip Carrier	
CY7B933−LC	L64	28-Square Leadless Chip Carrier	
CY7B933−PC	P21	28-Lead (300-Mil) Molded DIP	
CY7B933−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B933−PI	P21	28-Lead (300-Mil) Molded DIP	
CY7B933−DMB	D22	28-Lead (300-Mil) CerDIP	Military
CY7B933−LMB	L64	28-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroup
V_{OHT}	1, 2, 3
V_{OLT}	1, 2, 3
V_{OHE}	1, 2
V_{OLE}	1, 2, 3
V_{ODIF}	1, 2, 3
I_{OST}	1, 2, 3
V_{IHT}	1, 2, 3
V_{ILT}	1, 2, 3
V_{IHE}	1, 2, 3
V_{ILE}	1, 2, 3
I_{IHT}	1, 2, 3
I_{ILT}	1, 2, 3
I_{IHE}	1, 2, 3
I_{ILE}	1, 2, 3
I_{CC}	1, 2, 3
V_{DIFF}	1, 2, 3
V_{IHH}	1, 2, 3
V_{ILL}	1, 2, 3

Switching Characteristics

Parameter	Subgroup
t_{CKW}	9, 10, 11
t_{B}	9, 10, 11
t_{CPWH}	9, 10, 11
t_{CPWL}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SENP}	9, 10, 11
t_{HENP}	9, 10, 11
t_{PDR}	9, 10, 11
t_{PPWH}	9, 10, 11
t_{PDF}	9, 10, 11
t_{RISE}	9, 10, 11
t_{FALL}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CPRH}	9, 10, 11
t_{CPRL}	9, 10, 11
t_{RH}	9, 10, 11
t_{PRF}	9, 10, 11
t_{PRH}	9, 10, 11
t_{A}	9, 10, 11
t_{ROH}	9, 10, 11
t_{CKX}	9, 10, 11
t_{CPXH}	9, 10, 11
t_{CPXL}	9, 10, 11
t_{DS}	9, 10, 11

Document #: 38−00189−C

PRELIMINARY

CYPRESS SEMICONDUCTOR

HOTLink Evaluation Board

Features

- 160 to 330 Mbps point-to-point serial data link
- Parallel-to-serial and serial-to-parallel I/O
- 10-bit-wide 8B/10B encode, decode or unencoded
- Compliant with ESCON, Fiber Channel and ATM standards
- Compatible with Fiber Channel FC–0 specification (CY9266–C):
  - —25–TV–EL–S
  - —25–MI–EL–S
  - —25–TP–EL–S
- Compatible with Fiber Channel FC–0 specification (CY9266–F):
  - —25–M6–LE–I
- Development tool for proprietary networks
- Full system diagnostics with Built-In-Self-Test (BIST)
- Two-digit error display for BER analysis
- Multiple host interface:
  - — 48-pin connector (IBM OLC–266 compatible)
  - — 60-pin edge connector
  - — 60-pin two-row right-angle connector
- Socket for optional on-board crystal oscillator
- Multiple system configurations via DIP switch
- Multilayer board with surface-mount technology
- Easy to use for applications development

Applications

- Similar in function to IBM OLC–266 (single channel) and HP HOLC–0266
- HOTLink System Development
- Telecommunications
- Remote data acquisition
- Processor-to-disk/peripheral communications
- Backplane extender
- Point-to-point video/image communications
- Point-to-point CPU/server communications
- High-speed data switching (T1 multiplexer, etc.)

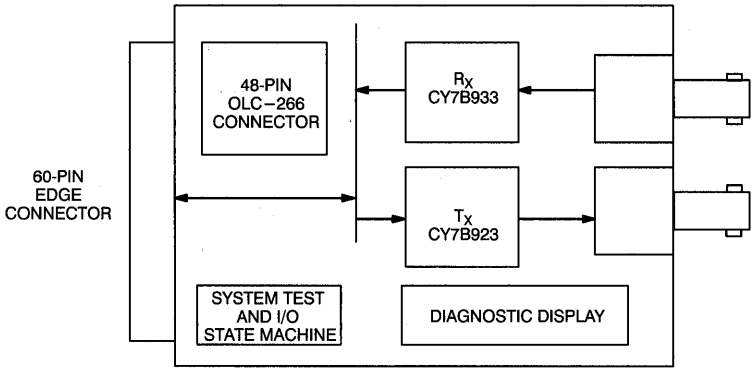


Figure 1. Copper Media Interface Evaluation Board CY9266–C 9266–1

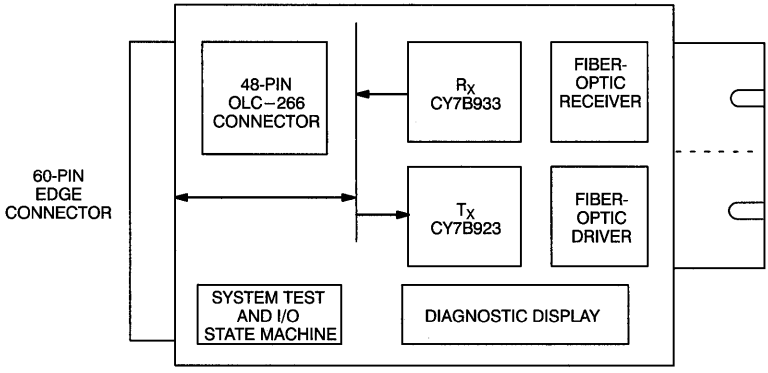


Figure 2. Fiber-Optic Interface Evaluation Board CY9266–F 9266–2

Specification

Board Dimensions	3.0″ x 4.0″ (approx., plus media connector)
Two media types:	
CY9266–C	Mini-coax or twisted-pair cables using two pin 0.25″ sq x 0.1″ header or right-angle BNC connectors
CY9266–F	LED based fiber optic using SC connector
Power Supply	+5V ± 5%
Maximum Clock Rate	33 MHz
Maximum Data Rate	330 Mbps
Parallel I/O	TTL
Serial I/O	Coax or twisted pair (CY9266–C) or Fiber optic with SC connector (CY9266–F)

General Description

The HOTLink Evaluation Board (CY9266) is a system development tool that facilitates the design and evaluation of the Cypress HOTLink transmitter (CY7B923) and receiver (CY7B933) devices. The CY9266 Evaluation Board is offered with two serial media interface options: CY9266–C (copper) and CY9266–F (fiber). The CY9266–C offers a low cost 1/4″ coaxial connection while the CY9266–F interfaces with a longwave (1300nm) LED optical transceiver and SC fiber optics connector.

The CY9266 accepts data and control commands from the host via the parallel interface ports (available in three connectors). The 48-pin header connector allows interoperability with the IBM OLC–266 interface. The two 60-pin connectors are functionally equivalent. The vertical pin connector is used for probing and monitoring the appropriate signals, while the edge connector can be connected to a flat ribbon cable as a direct host communication interface.

In a typical point-to-point link, the host downloads parallel data to the CY9266 Evaluation Board. Parallel data can be formatted as pre-encoded 10 bit patterns or 8-bit data/special characters to be encoded by the HOTLink transmitter. The data is then encoded (optionally) and serialized by CY7B923 HOTLink Transmitter. Serial data is then transmitted via coax or fiber.

In the receive operation, serial data is sent from a remote source (via copper/fiber) and transferred to the CY7B933 HOTLink receiver. The serialized data is converted to parallel and then optionally decoded. Parallel data is transferred to the host system along with various status and synchronizing signals. All I/O operations are performed between the host and the Evaluation Board using simple handshakes.

The CY9266 Evaluation Board can also operate in self-diagnostic mode and indicate errors in the serial transmission stream using a built-in two-digit, seven-segment LED display.

Document #: 38–00236

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HP HOLC–0266 is a trademark of Hewlett-Packard Corporation.

Section Contents

Modules **Page Number**

CYPRESS SEMICONDUCTOR

Custom Module Capabilities

Introduction

Cypress's Multichip Products group is a leading supplier of custom memory and/or logic modules. This turnkey capability provides designers with a fast, low-risk solution for when they require the ultimate in system performance and density. Detailed information on standard modules can be found in the Static RAM, FIFO, and Module sections of this book.

Packaging Guidelines

High-density memory modules are now available in a wide variety of package styles that satisfy a variety of needs for high-performance system design. Since board space is a primary concern, the choice of a package style is important in meeting layout constraints as well as thermal and mechanical design objectives.

Multichip Products currently supports several commonly used module technologies including plastic components on FR4 or polyimide substrate, and ceramic components mounted on ceramic substrates. Advanced technologies suitable for the demands of higher integration components are also available.

The plastic technology employs plastic encapsulated, surface-mount components and an epoxy laminate (FR4 or polyimide) substrate. The plastic components can be SOJ, SOIC, VSOP, TSOP, QFP, or other surface-mount packages. Die can also be mounted directly to the substrate and wire bonded to the substrate.

The ceramic technology employs hermetic, ceramic-packaged devices mounted on a ceramic substrate. The components are typically leadless chip carriers, but may include other package types. The ceramic substrate has a custom interconnect for the particular components it carries. The ceramic substrate and components offer improved thermal characteristics over the plastic modules. This makes these modules suitable for extended temperature range operation, such as in military applications.

Common Packaging Options

This section describes several common module packaging options available from Cypress. A summary table (*Table 1*) compares relative board areas of each option based on a module with eight 28-pin components.

SIP

The single in-line pin package, or SIP, is a vertically mounted module with a single row of pins along one edge for through-hole mounting. The SIP configuration is typically constructed with plastic-encapsulated components mounted on an FR4 or polyimide substrate, although ceramic SIPs are also used. The pins are on a 100-mil pitch. The vertical orientation and the mounting of components on both sides of the module can increase the component density by a factor of four or more.

Flat SIP

The flat single in-line pin package, or FSIP, is virtually identical to the SIP except that the substrate is mounted in the horizontal rather than the vertical direction. When mounted to a circuit board, the flat SIP lies close and parallel to the board. Flat SIP modules save board area since they, like other modules, employ fine lead pitch surface-mount components on a high-density substrate. The flat SIP density approximates double-sided surface-mounted boards with the advantage of a very low profile and improved mechanical stability over the vertical SIP.

ZIP

The zigzag in-line pin package, or ZIP, is vertically mounted and is usually built with plastic encapsulated components on an FR4 or polyimide substrate. The ZIP module has pins along both sides of the substrate and the pins on alternate sides are staggered by 50 mils. Adjacent pins on the same side of the substrate are separated by 100 mils. The dual row of staggered pins allows a higher connection density than that of the SIP while maintaining 100-mil minimum spacing between any adjacent pins. The ZIP is especially useful in large pin count devices where the host board is designed with through-hole design rules.

SIMM

The single in-line memory module, or SIMM, is similar to the ZIP except that there are no pins for through-hole mounting. Instead, the bottom edge of the module is equipped with edge connector contacts that are plated to the substrate. The SIMM is designed to plug into motherboard sockets. The contacts are on both sides of the substrate, and contacts directly opposite each other are connected together. SIMM edge connector contacts are on a 50-mil or 100-mil pitch. SIMMs allow greater system functionality and flexibility by allowing easy use of multiple densities and speed grades.

Some module devices are available in both ZIP and SIMM packages with the same form factor. The pin out is designed so that the pinout and footprint of the SIMM socket matches the footprint of the ZIP module allowing ZIPs or SIMMs to be used interchangeably with only one board layout. The SIMM may be used in prototyping to test different speed versions of a system and then replaced with a companion ZIP for production, or SIMMs may be used in production for flexibility in memory size or memory speed.

VDIP

The VDIP, or vertical dual in-line pin package, is a vertically mounted module with two rows of pins on 100-mil centers. Row to row spacing is 100 mils, with pins of the two rows aligned directly across from one another. The dual row of pins allows a higher connection density than that of the SIP while maintaining 100-mil minimum spacing between any adjacent pins. VDIP may be either plastic or ceramic. The VDIP is useful in large pin count devices where the host board is designed with through-hole design rules.

DIP

The DIP, or dual in-line pin module, is a low-profile package with excellent mechanical ruggedness. The ceramic DIP is ideally suited for military applications. Plastic DIPs are often used when a low vertical profile is required. In some cases, the DIP device is intended to have an identical footprint and similar form factor to standard integrated circuit components and can provide larger memory capacity in the same footprint.

PGA

The PGA, or pin grid array, has an array of pins that are perpendicular to the package plane. These pins are arranged in a matrix on a 100-mil grid. Most of the matrix is filled with pins except for a central square that is normally devoid of pins.

QUIP

The QUIP, or quad in-line pin package, is very similar to the DIP package except that there is a dual row of pins along the package edge. In-row and row-to-row pin spacing is 100 mils with pins in adjacent rows aligned directly across form one another. The QUIP is a low-profile package with excellent mechanical ruggedness, with the added advantage of higher pin density for the same package length.

QFP

The QFP, or quad flat pack, is a surface-mounted module. Gull wing pins extend out from the square package on all four sides and are formed to be coplanar with the package bottom. Lead pitches are typically 50 mils or smaller.

Package Summary

Table 1 summarizes the various characteristics of the packages discussed above.

Table 1. Package Types

Package Type	Typical Pin Count		Typical Height[1]		Mil[2]	Advantages	Disadvantages	Board Space (sq. in.)[3]	
	Min.	Max.	Min.	Max.				FR4	Cer
SIP	24	50	0.5	0.9	N	Vertical orientation. FR4 or ceramic technology.	Limited pin count.	1.2	0.9
FSIP	24	50	0.2	0.4	N	Very low profile. Mechanical stability. FR4 or ceramic technology.	Lower density due to horizontal orientation.	2.7	2.4
ZIP	24	100	0.5	0.9	N	Vertical orientation. JEDEC-standard pinouts. Pinout compatible with SIMM.		1.2	N/A
SIMM	24	100	0.5	0.9	N	Vertical orientation. Socket mounting. Pinout compatible with ZIP.		1.2	N/A
VDIP	36	104	0.5	0.95	Y	Vertical orientation.		1.2	0.9
DIP	24	60	0.17	0.37	Y	Low profile. Excellent mechanical ruggedness.	Horizontal orientation.	2.9	2.9
QUIP	48	200			Y	Low profile. Excellent mechanical ruggedness. Increased number of pins.	Horizontal orientation.	2.9	2.9
QFP	68	144			Y	Surface mount. Low profile. Excellent mechanical ruggedness. Large number of pins in small area.	Surface-mount technology required. Horizontal orientation. Components on one side only.	3.1	3.1
PGA	68	144			Y	Large number of pins in thru-hole technology. Low profile. Excellent mechanical ruggedness.	Multilayer boards. Horizontal orientation. Components on one side only.	2.9	2.9

Notes:
1. Minimum and maximum height are given in inches.
2. The Mil entry contains a Y(es) or N(o) indicating if the package type is suitable for military applications.
3. Board space roughly quantifies the main board area, in square inches, taken up by the module when the module contains eight, 28-pin components.

Component Selection

Cypress's Multichip Products group handles many types of components to build custom modules. Typically, any digital component that is available in surface-mount packaging can be used, but the module is not limited to this. Standard and custom modules include SRAM, FIFOs, dual ports, EPROM, Flash, and E^2PROM devices, combined or mixed. Logic may also be employed to provide decoding, pipelined storage, or extra drive capability. The CYM1461 and the CYM1540 are examples of such devices. In the CYM1461, sixteen 32K x 8 RAMs are arranged to form a 512K x 8 module and the individual SRAMs are selected by an on board decode. The CYM1540 provides address and control buffering for a 256K x 9 static RAM module so that only a single device load and capacitance is presented to the system. Other custom modules provide for unusual memory word widths. The CYM1720 is a memory module specifically designed for 24-bit-wide DSP processors.

ECL is also a logic family suitable for collecting into a module. Unless the system is largely ECL, it makes sense to place the ECL components onto a module that is optimized for performance. Delivered as a tested component, the ECL module can be assembled into the system with high confidence of proper functionality. Typical examples of custom ECL modules include wide ECL-to-TTL translators and deep and/or wide ECL PROM or RAM memory arrays.

More complex functions may also be integrated onto a custom module; e.g., processor subsystems, embedded within a system that are dedicated to specific functions. These functions may include several forms of memory, a microprocessor or DSP, communication ports, and bus interface circuitry with possibly shared memory control. A custom module may also include an ASIC designed especially to implement the desired function. One example of such a device is the CYM4241 deep FIFO. This device includes three high-speed SRAMs, a surface-mount 50-MHz crystal oscillator, and a wire-bonded ASIC die on substrate that integrates the RAM interface control and port access arbitration. This combination of components yields a 64K by 9 FIFO in a single 28-pin DIP. By simply changing the memory content, the device can be extended to 256K by 9.

Modules undergo complete characterization and qualification before being released to production. Characterization includes the following: AC and DC characterization over voltage and temperature, and complete custom specification review. Release to production requires a verified test program with test hardware and correlation samples, complete assembly drawings and approved parts list, production and test travelers, a formal design review, and customer approval. In production, custom (and standard) modules are built using fully tested components, and are rigorously tested before they are shipped. As an example of the rigorous production testing, memory modules are tested for all DC parametrics, all AC parametrics, and functionality. Functional testing includes a select set of memory pattern sensitivity tests. This complete testing allows the module to be treated by the user as a true component with a set of specifications that are guaranteed by the manufacturer. This saves time and effort during system manufacture and provides a degree of reliability not obtainable from operations focused on only assembly.

Future Technologies

The ultimate in multichip technology is multiple die on a substrate that offers highly efficient interconnect and the densest multichip assembly technology. The technology is available now for multichip configurations with silicon chips on ceramic, epoxy laminate, and silicon substrates.

Introduction to Modules for the New User

The use of modules is growing rapidly since it is a vehicle for obtaining high integration and high performance with minimal impact on cost. Almost every personal computer now has main memory as plug in SIMM packages constructed from surface-mount DRAM components. High-performance RISC and CISC CPU subsystems are available as modules where the supplier has optimized the component I/O design and the substrate layout for maximum performance amongst the tightly coupled components.

Size is one obvious advantage of modules; their small size allows a function to fit into a very small space. Consider the economics of having a large memory array together with the system CPU on a single card in contrast to the cost of multiple memory cards connected via a backplane bus and the resulting performance loss. In many cases, the module approach is a considerable savings in materials and manufacturing cost by reducing the total number of system cards.

Applying the tight design rules of modules has its limitations. A module has line widths and spacings that support close packing of VSOP and die components, and these spacing/width design rules are at the limit of what can be handled by capable volume production substrate producers. The use of fully tested modules gives the density gain of tight design rules at economically attractive system manufacturing yields. Therefore in the manufacturing process, the module exhibits the characteristics of a monolithic device: high integration, ease of application, and high system manufacturing yield. The module brings high-density surface-mount technology to the through-hole manufacturing environment.

Performance is another significant gain obtainable from module application. Unfortunately this is the most difficult gain to quantify. Consider a memory subsystem collected tightly around a CPU versus the same memory capacity spread over one or more boards. It seems intuitively plausible that the larger subsystem will be slower: the distance to travel is longer, and the memory address and data bus lines have larger capacitance due to their longer length and the larger number of stubs on the lines. This is indeed the case. Many of the custom modules include buffers for reduced loading, registers for data pipelining, and simple or specialized decoders to ease system bus interfacing. Taken as a component, these modules typically exhibit higher capacitance than a monolithic component and incur about 5 ns additional delay for on board decoders or buffers. However, the module is from four to sixteen times as dense as through-hole monolithic devices and consequently achieve a net performance advantage.

Custom Module Development Flow

Multichip's focus is on providing turnkey memory modules. *Figure 1* illustrates the tasks performed during the development of the module.

Module development commences with the generation of a detailed Objective Specification. The module is designed to this specification, and once in production it will be guaranteed to perform as indicated in the Objective Specification.

Components are selected while the specification is being generated. In many cases, the spec is designed such that multiple sources of components can be utilized. Once the spec is complete and the components are selected, a schematic for the module is generated. The netlist from the schematic is used to drive the circuit simulator.

Custom Module Development Flow (continued)

During simulation, several types of analyses are performed. A function simulation is used to ensure that the module's logic is designed properly. Timing simulation is run to verify that the module will function when subjected to the worst-case timing delays of the components. Finally, thermal analysis may be performed to determine the thermal characteristics of the module.

The layout of the module is also netlist driven. An autorouter may be used, depending on the complexity and density of the module. Design rule checks are run to ensure that the layout does not violate any electrical or mechanical design rules. Finally, the layout output is used to generate the module substrate.

The layout output is also used to drive the pick and place equipment. This ensures consistency between design and manufacturing. While the module prototypes are being assembled, the test program is generated and the test fixture is constructed. Test program generation is largely automated, using as inputs the simulation outputs and pre-defined test program subroutines for common configurations.

Once prototypes have been generated, the standard release procedure is initiated. This procedure includes steps such as bench testing, module characterization and qualification, and fine tuning of the test program. Following customer approval of the module, it is released to production.

Quoting Information

In order to prepare a quotation or proposal, we need as much as possible of the following information:

- Circuit schematic
- Functional description
- Mechanical dimensions required
- Speed and power requirements
- Prototype and production deadlines
- Production quantity estimates
- An engineering contact to answer questions

Once the above information is received, a budgetary quotation will typically be provided within one to two weeks.

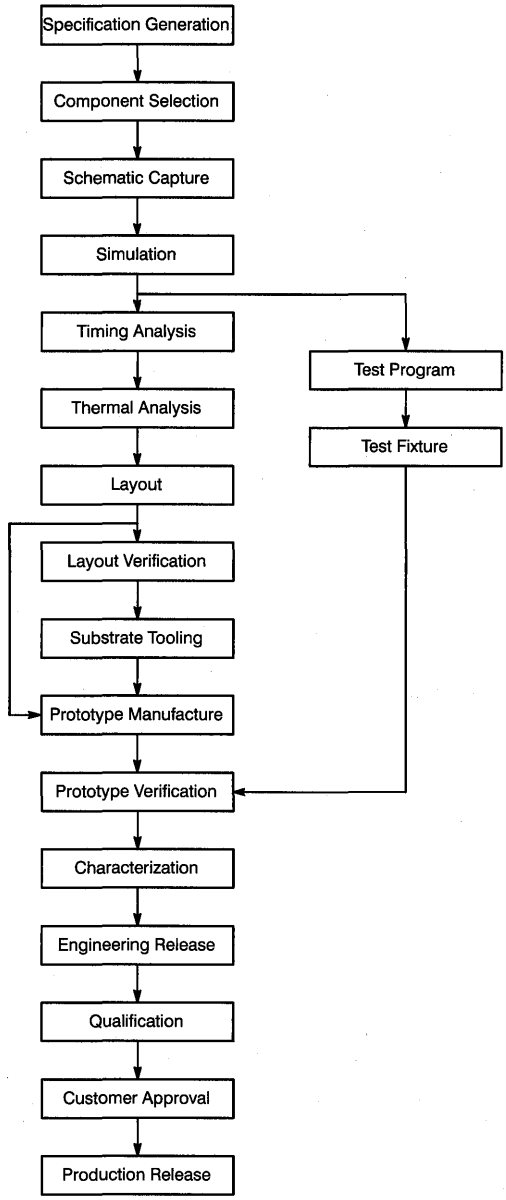


Figure 1. Custom Module Flow

CYM1420

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **Low active power**
  - **1.2W (max.)**
- **Hermetic or plastic SMD technology**
- **TTL-compatible inputs and outputs**
- **JEDEC-compatible pinout**
- **Commercial and military temperature ranges**

Functional Description

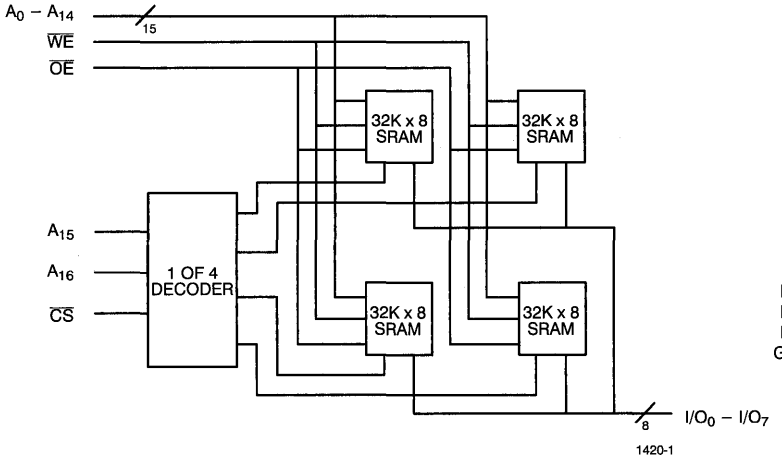
The CYM1420 is a very high performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 32K x 8 static RAMs mounted onto a substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and to select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight input/output pins.

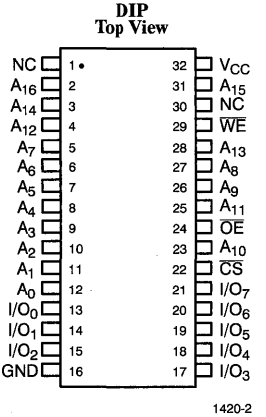
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1420-1

Pin Configuration



1420-2

Selection Guide

		1420–20	1420–25	1420–30	1420–35	1420–45	1420–55
Maximum Access Time (ns)		20	25	30	35	45	55
Maximum Operating Current (mA)	Commercial	210	210	210	210	210	210
	Military			210	210	210	210
Maximum Standby Current (mA)	Commercial	140	140	140	140	140	140
	Military			140	140	140	140

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C (Commercial) − 55°C to +125°C (Military)

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1420 Min.	CYM1420 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		80	mA

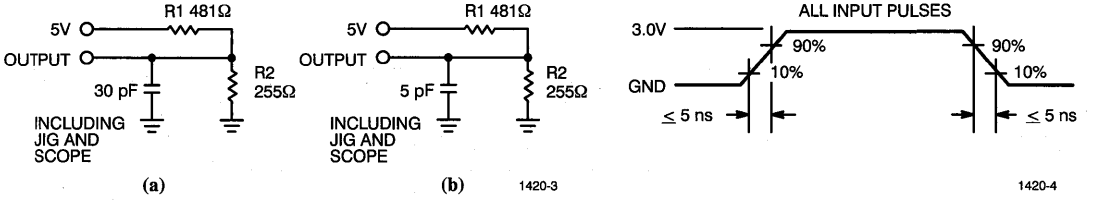
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

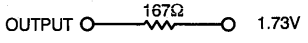
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameters	Description	1420–20		1420–25		1420–30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		10		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		20		25		ns
t_{AW}	Address Set-Up to Write End	15		20		25		ns
t_{HA}	Address Hold from Write End	2		2		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	10		12		18		ns
t_{HD}	Data Hold from Write End	2		2		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	8	0	10	0	15	ns

Notes:

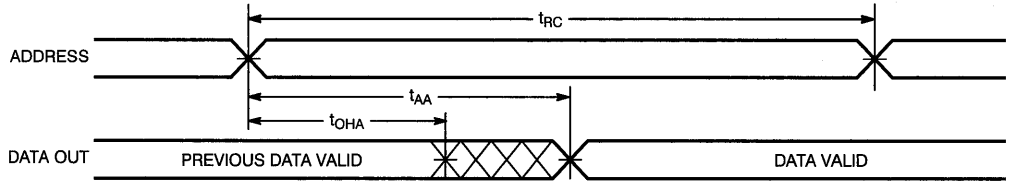
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

Parameters	Description	1420–35		1420–45		1420–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		18		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		25	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		45		ns
t_{AW}	Address Set-Up to Write End	30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		20		25		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	25	ns

Switching Waveforms

Read Cycle No. 1[8, 9]

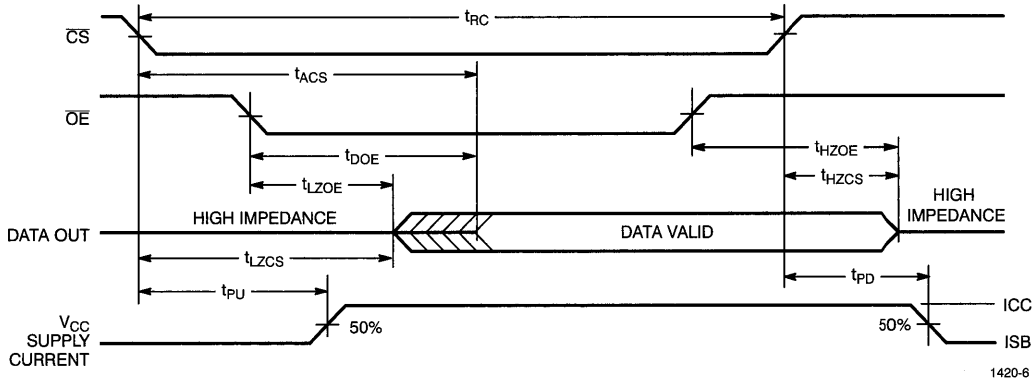


1420-5

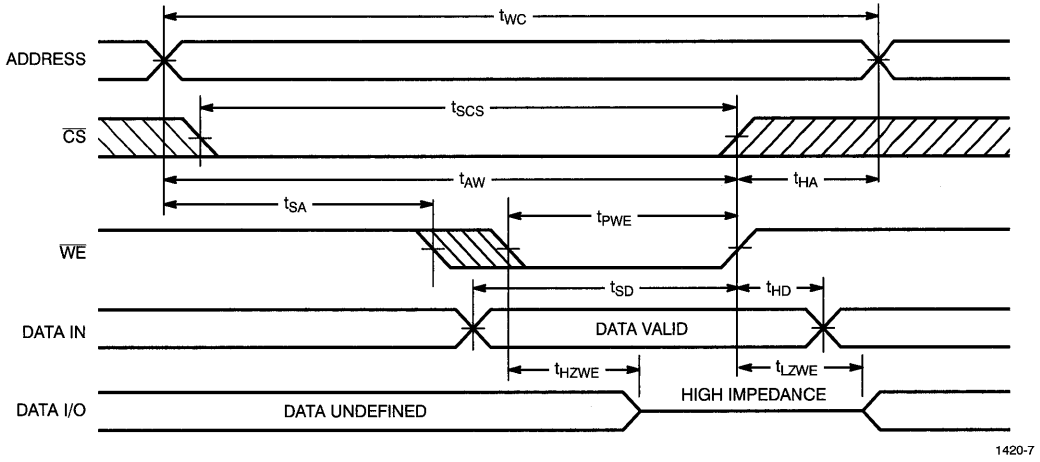
Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



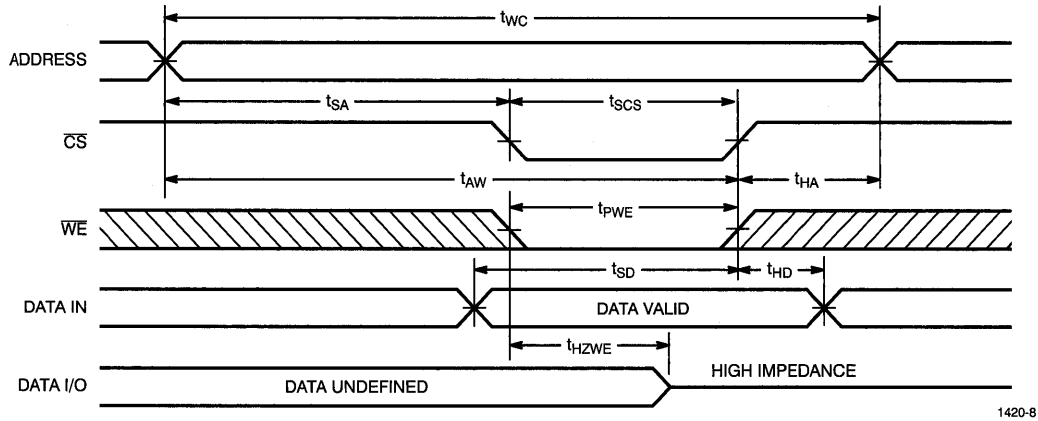
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



Notes:
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



Note:
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1420PD–20C	PD05	52-Pin DIP Module	Commercial
25	CYM1420HD–25C	HD04	32-Pin DIP Module	Commercial
	CYM1420PD–25C	PD05	52-Pin DIP Module	
30	CYM1420HD–30C	HD04	32-Pin DIP Module	Commercial
	CYM1420PD–30C	PD05	52-Pin DIP Module	
35	CYM1420HD–35C	HD04	32-Pin DIP Module	Commercial
	CYM1420PD–35C	PD05	52-Pin DIP Module	
	CYM1420HD–35MB	HD04	32-Pin DIP Module	Military
45	CYM1420HD–45C	HD04	32-Pin DIP Module	Commercial
	CYM1420PD–45C	PD05	52-Pin DIP Module	
	CYM1420HD–45MB	HD04	32-Pin DIP Module	Military
55	CYM1420HD–55C	HD04	32-Pin DIP Module	Commercial
	CYM1420PD–55C	PD05	52-Pin DIP Module	
	CYM1420HD–55MB	HD04	32-Pin DIP Module	Military

Document #: 38–M–00001–D

CYM1441

256K x 8 Static RAM Module

Features

- **High-density 2-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **5.3W (max.)**
- **SMD technology**
- **Separate data I/O**
- **60-pin ZIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.5 in.**
- **Small PCB footprint**
  - **1.14 sq. in.**

Functional Description

The CYM1441 is a very high performance 2-megabit static RAM module organized as 256K words by 8 bits. The module is constructed using eight 256K x 1 static RAMs in SOJ packages mounted onto an epoxy laminate substrate with pins. Two chip selects ($\overline{CS}_L$ and $\overline{CS}_U$) are used to independently enable the upper and lower 4 bits of the data word.

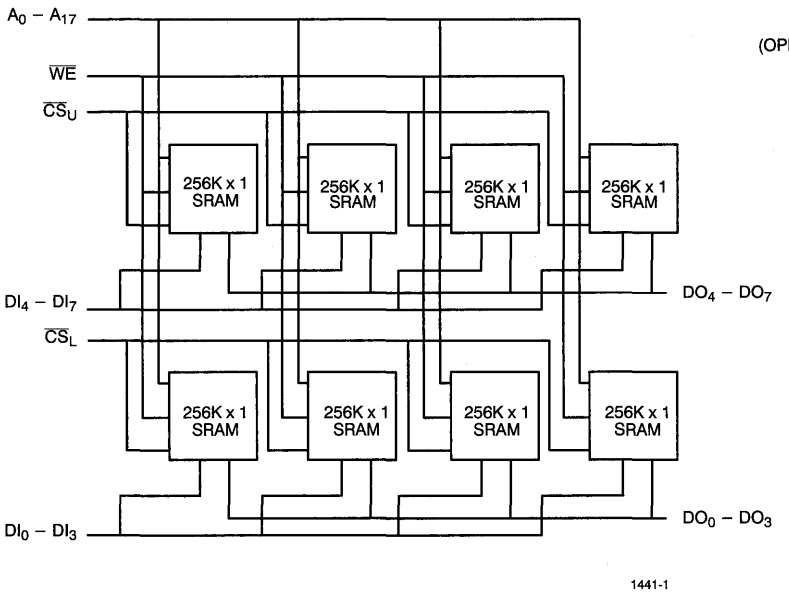
Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (DI_0 through DI_7) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data output pins (DO_0 through DO_7).

The data output pins remain in a high-impedance state unless the module is selected and write enable ($\overline{WE}$) is HIGH.

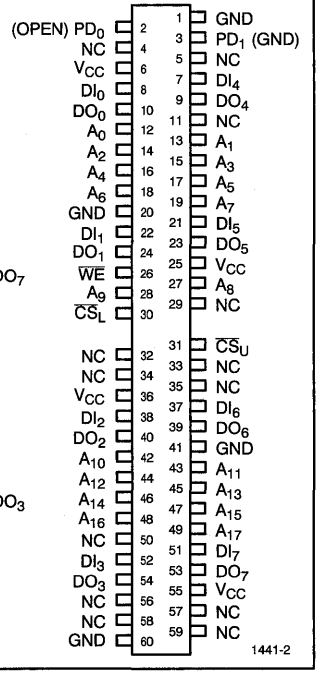
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1441–25	1441–35	1441–45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	960	960	960
Maximum Standby Current (mA)	320	320	320

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... – 55°C to +125°C

Ambient Temperature with Power Applied ..... – 10°C to +85°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1441 Min.	CYM1441 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	– 80	+80	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	– 50	+50	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V		160	mA

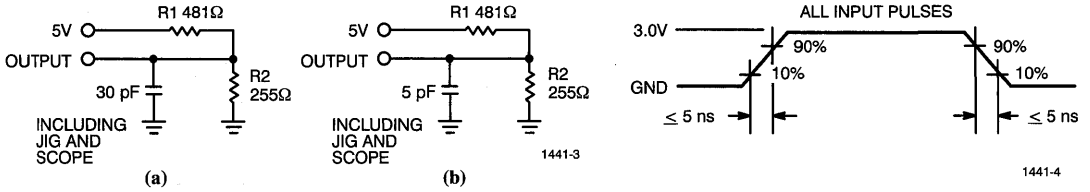
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{OUT}	Output Capacitance		15	pF

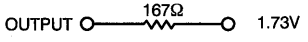
Notes:

1. $V_{IN(min.)}$ = – 3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

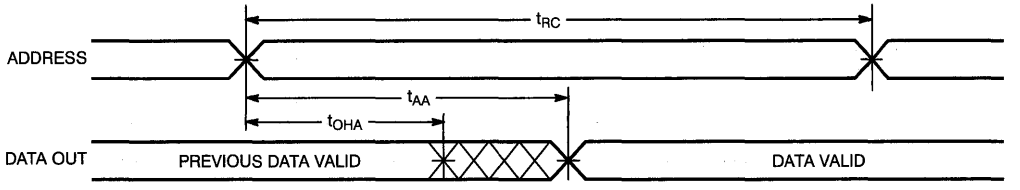
Parameter	Description	1441–25		1441–35		1441–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		25		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	15	0	20	0	25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.

Switching Waveforms

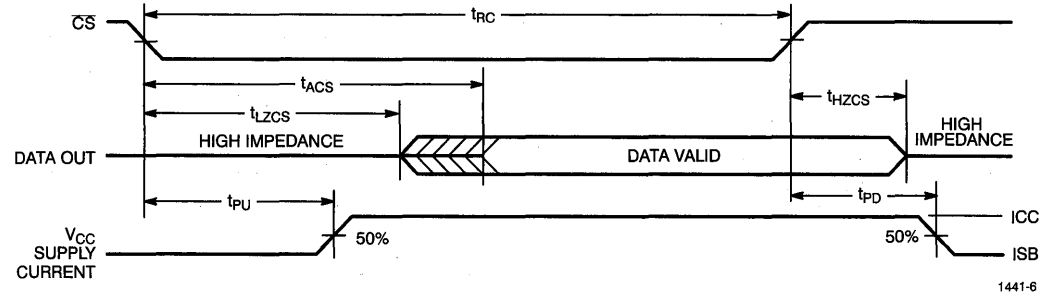
Read Cycle No. 1[6, 7]



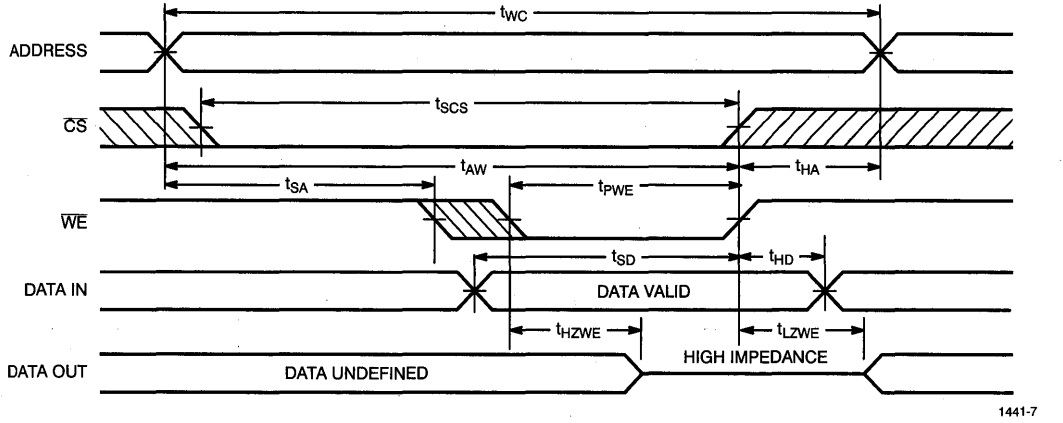
1441-5

Switching Waveforms (continued)

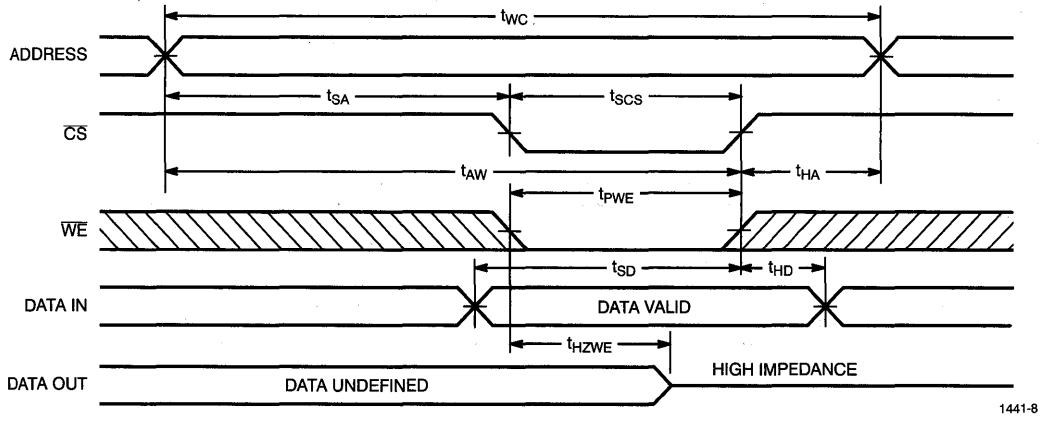
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:

8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write
L	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1441PZ–25C	PZ04	60-Pin ZIP Module	Commercial
35	CYM1441PZ–35C	PZ04	60-Pin ZIP Module	Commercial
45	CYM1441PZ–45C	PZ04	60-Pin ZIP Module	Commercial

Document #: 38–M–00020–A

CYPRESS SEMICONDUCTOR

CYM1464

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **1.93W (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.34 inches**

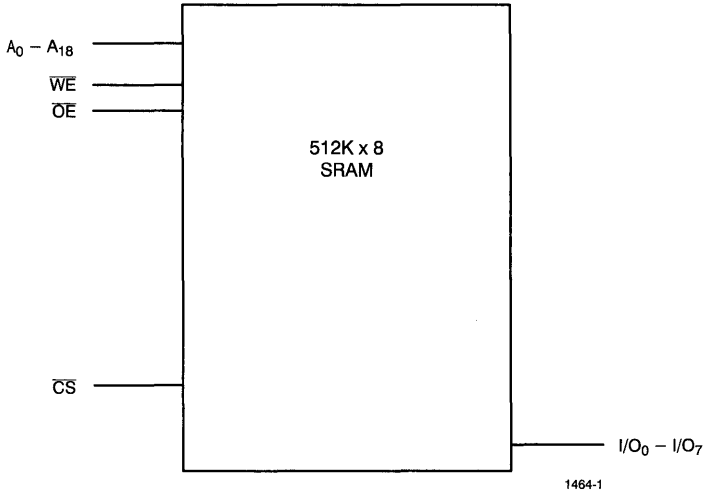
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

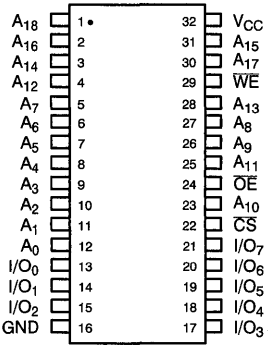
Logic Block Diagram



1464-1

Pin Configuration

DIP
Top View



1464-2

Selection Guide

	1464–20	1464–22	1464–25	1464–30	1464–35	1464–45	1464–55
Maximum Access Time (ns)	20	22	25	30	35	45	55
Maximum Operating Current (mA)	350	350	350	300	300	300	300
Maximum Standby Current (mA)	240	240	240	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1464−20, 22, 25		1464−30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		350		300	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		10		10	mA

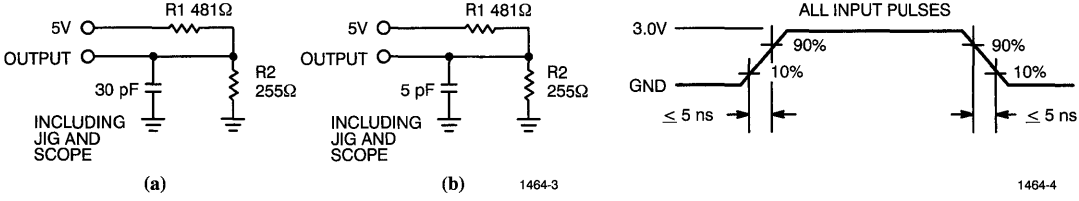
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		30	pF

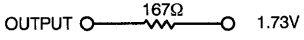
Notes:

1. $V_{IL\,(Min.)}$ = − 3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



8 MODULES

Switching Characteristics Over the Operating Range[3]

Parameter	Description	1464–20		1464–22		1464–25		1464–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	20		22		25		30		ns
t_{AA}	Address to Data Valid		20		22		25		30	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		22		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		13		15		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	10	0	10	0	10	0	10	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	15	0	15	0	15	0	20	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	20		22		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		17		20		25		ns
t_{AW}	Address Set-Up to Write End	15		15		20		25		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		15		20		ns
t_{SD}	Data Set-Up to Write End	12		12		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		15		15	ns

Notes:

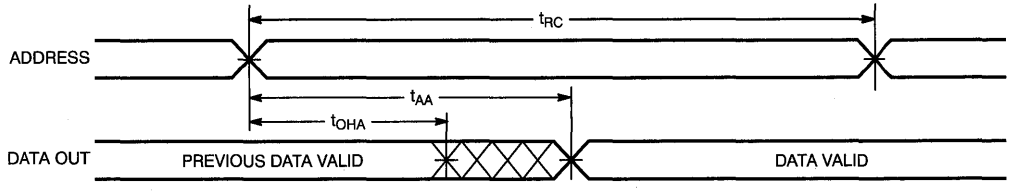
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

Parameter	Description	1464–35		1464–45		1464–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	15	0	15	0	15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	20	0	20	0	20	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	6		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		35		40		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		20	ns

Switching Waveforms

Read Cycle No. 1[6, 7]

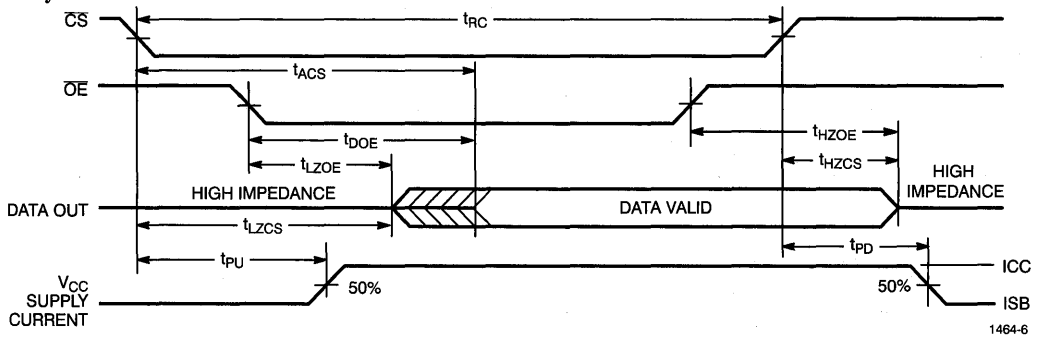


1464-5

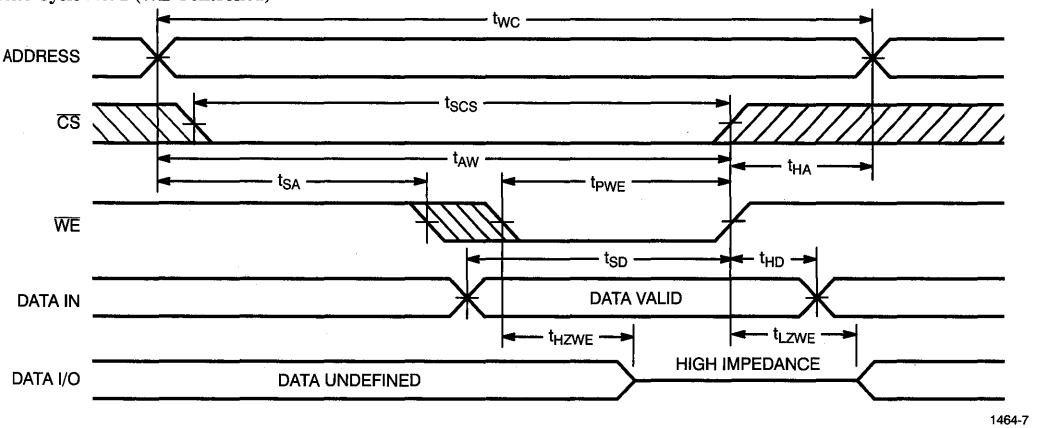
Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Switching Waveforms (continued)

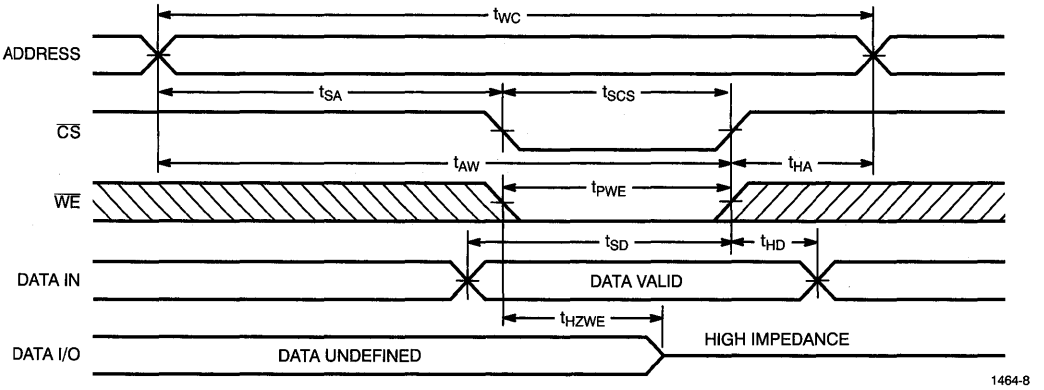
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:

8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CYM1464PD–20C	PD02	32-Pin DIP Module	Commercial
22	CYM1464PD–22C	PD02	32-Pin DIP Module	Commercial
25	CYM1464PD–25C	PD02	32-Pin DIP Module	Commercial
30	CYM1464PD–30C	PD02	32-Pin DIP Module	Commercial
35	CYM1464PD–35C	PD02	32-Pin DIP Module	Commercial
45	CYM1464PD–45C	PD02	32-Pin DIP Module	Commercial
55	CYM1464PD–55C	PD02	32-Pin DIP Module	Commercial

Document #: 38–M–00030–C

CYPRESS SEMICONDUCTOR

CYM1465

512K x 8 SRAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **605 mW (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.27 in.**
- **Small PCB footprint**
  - **0.98 sq. in.**

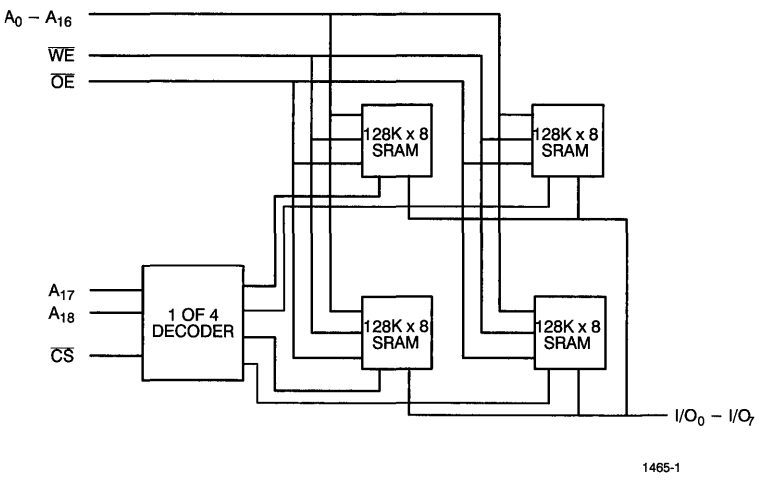
Functional Description

The CYM1465 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs mounted on a substrate with pins. A decoder is used to interpret the higher-order addresses (A_{17} and A_{18}) and to select one of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

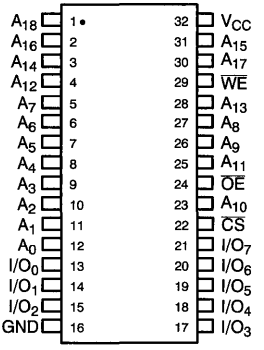
Logic Block Diagram



1465-1

Pin Configuration

DIP
Top View



1465-2

Selection Guide

	1465–70	1465–85	1465–100	1465–120	1465–150
Maximum Access Time (ns)	70	85	100	120	150
Maximum Operating Current (mA)	110	110	110	110	110
Maximum Standby Current (mA)	12	12	12	12	12

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 55°C to +150°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%

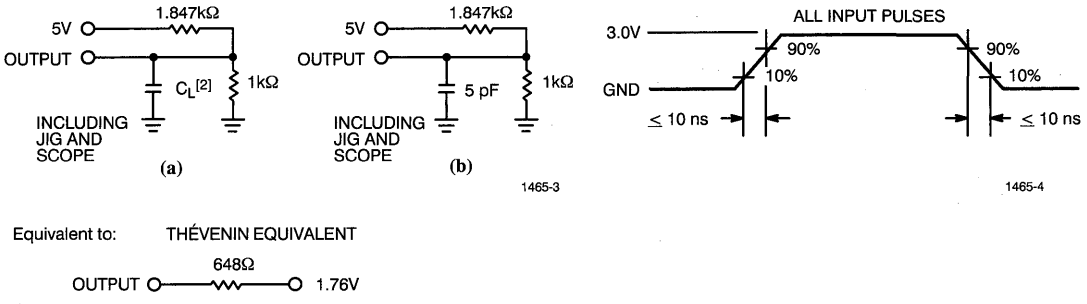
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		1465 Min.	1465 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		− 20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			110	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			12	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	Standard Version		8	mA
			L Version		420	µA

Capacitance[1]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	45	pF
C_{OUT}	Output Capacitance		45	pF

AC Test Loads and Waveforms



Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance for 85-, 100-, 120-, and 150-ns speeds. C_L = 30 pF for 70-ns speed.

Switching Characteristics Over the Operating Range[2]

Parameter	Description	1465–70		1465–85		1465–100		1465–120		1465–150		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	70		85		100		120		150		ns
t_{AA}	Address to Data Valid		70		85		100		120		150	ns
t_{OHA}	Data Hold from Address Change	10		10		10		10		10		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85		100		120		150	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		45		50		60		75	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		30		30		35		45		60	ns
WRITE CYCLE[4]												
t_{WC}	Write Cycle Time	70		85		100		120		150		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		90		100		115		ns
t_{AW}	Address Set-Up to Write End	65		75		90		100		110		ns
t_{HA}	Address Hold from Write End	0		5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	0		5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	55		65		75		85		95		ns
t_{SD}	Data Set-Up to Write End	30		35		40		45		50		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		25		30		35		40		45	ns

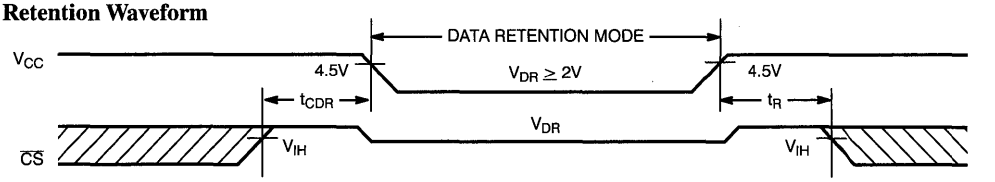
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		2		V
I_{CCDR3}	Data Retention Current	$V_{DR} = 3.0V$, $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		50		150	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		5		5		ms

Notes:

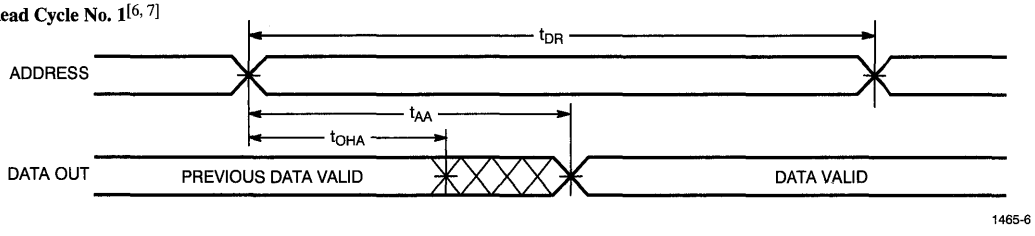
3. C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Guaranteed, not tested.

Data Retention Waveform

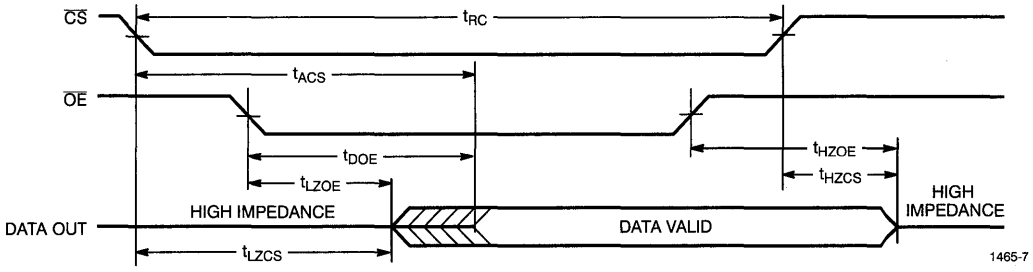


Switching Waveforms

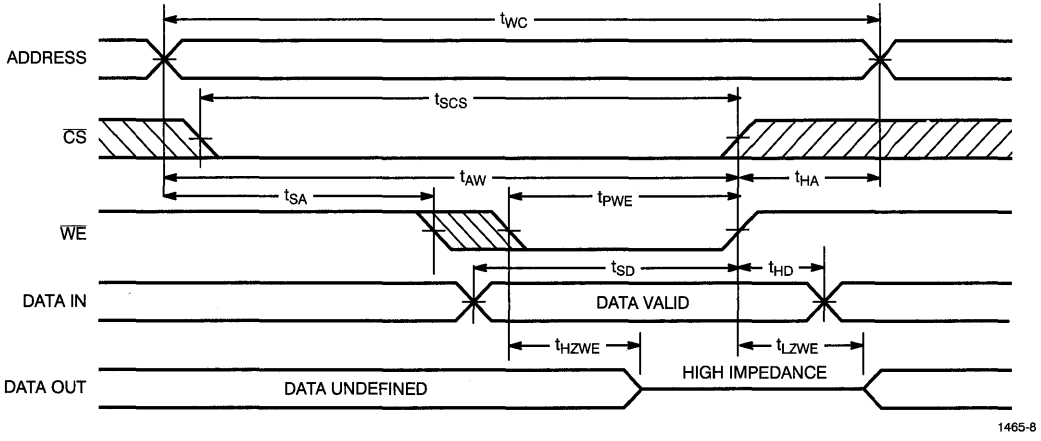
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[4]

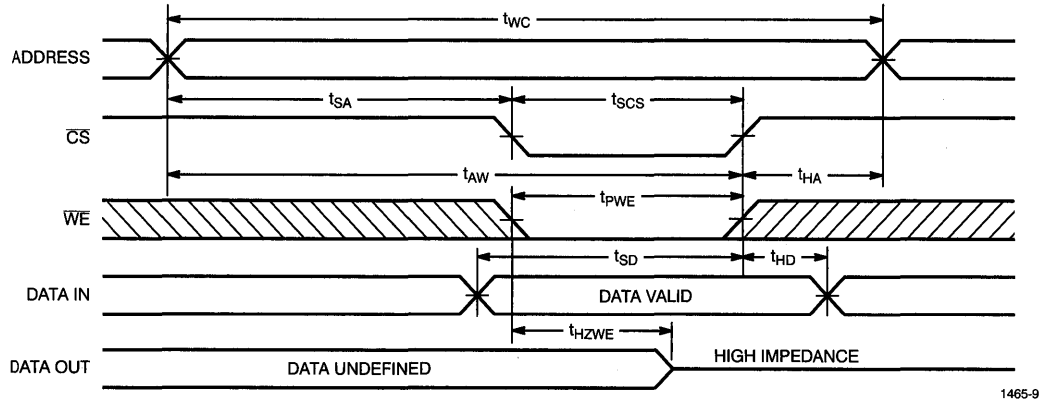


Notes:

6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[4, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

Inputs				
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM1465PD–70C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–70C			
85	CYM1465PD–85C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–85C			
	CYM1465PD–85I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–85I			
100	CYM1465PD–100C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–100C			
	CYM1465PD–100I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–100I			
120	CYM1465PD–120C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–120C			
	CYM1465PD–120I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–120I			
150	CYM1465PD–150C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–150C			
	CYM1465PD–150I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–150I			

Document #: 38–M–00036–C

CYM1471
CYM1481

CYPRESS SEMICONDUCTOR

1024K x 8 SRAM Module
2048K x 8 SRAM Module

Features

- **High-density 8-/16-megabit SRAM modules**
- **High-speed CMOS SRAMs**
  - **Access time of 85 ns**
- **Low active power**
  - **605 mW (max.), 2M x 8**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Very low profile version (PF)**
  - **Max. height of 0.205 in.**
- **Small footprint SIP version (PS)**
  - **PCB layout area of 0.72 sq. in.**
- **2V data retention (L version)**
- **Compatible with CYM1460/CYM1461**

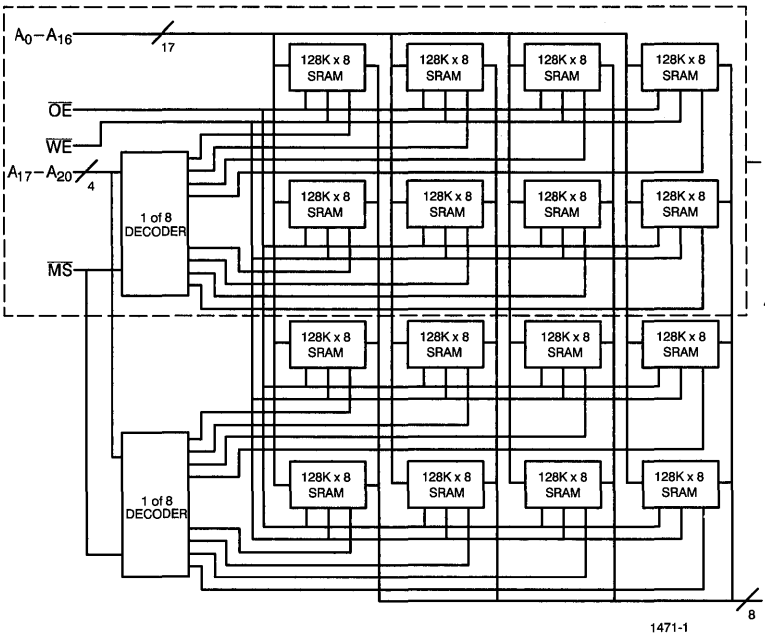
Functional Description

The CYM1471 and CYM1481 are high-performance 8-megabit and 16-megabit static RAM modules organized as 1024K words (1471) or 2048K words (1481) by 8 bits. These modules are constructed from eight (1471) or sixteen (1481) 128K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs $\overline{MS}$ and $\overline{OE}$ active LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

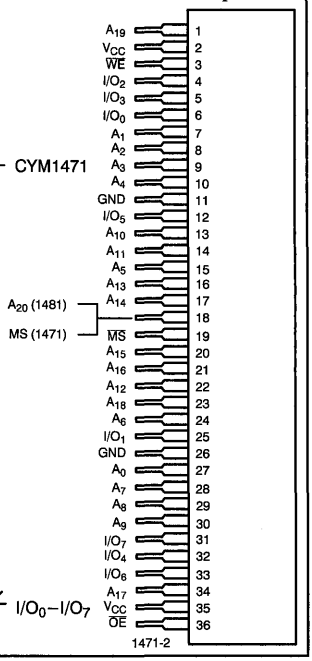
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration

SIP
Top View



Selection Guide

	CYM1471			CYM1481		
Maximum Access Time (ns)	85	100	120	85	100	120
Maximum Operating Current (mA)	95	95	95	110	110	110
Maximum Standby Current (mA)	16	16	16	32	32	32

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... − 0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.3V to +7.0V

DC Input Voltage ..... − 0.3V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

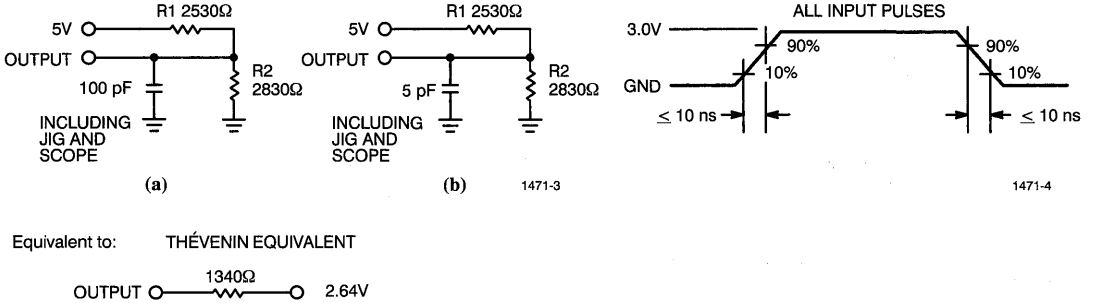
Parameter	Description	Test Conditions		1471 Min.	1471 Max.	1481 Min.	1481 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 20	+20	− 20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		− 20	+20	− 20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{MS}$ ≤ V_{IL}, I_{OUT} = 0 mA			95		110	mA
I_{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			16		32	mA
I_{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V	Standard		16		32	mA
			L Version		250		500	µA

Capacitance[1]

Parameter	Description	Test Conditions	CYM1471 Max.	CYM1481 Max.	Unit
C_{INA}	Input Capacitance (A_{0-16}, $\overline{OE}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	75	125	pF
C_{INB}	Input Capacitance (A_{17-20}, $\overline{MS}$)		25	25	pF
C_{OUT}	Output Capacitance		95	165	pF

Note:
1. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

8 MODULES

Switching Characteristics Over the Operating Range[2]

Parameter	Description	1471–85 1481–85		1471–100 1481–100		1471–120 1481–120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	85		100		120		ns
t_{AA}	Address to Data Valid		85		100		120	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{AMS}	$\overline{MS}$ LOW to Data Valid		85		100		120	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		45		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		30		35		45	ns
t_{LZMS}	$\overline{MS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZMS}	$\overline{MS}$ HIGH to High Z[3, 4]		30		35		45	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	85		100		120		ns
t_{SMS}	$\overline{MS}$ LOW to Write End	75		90		100		ns
t_{AW}	Address Set-Up to Write End	75		90		100		ns
t_{HA}	Address Hold from Write End	7		7		7		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	65		75		85		ns
t_{SD}	Data Set-Up to Write End	35		40		45		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		30		35		40	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

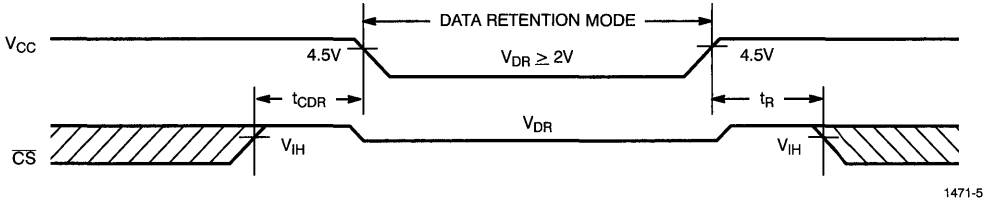
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1471–85		1471–100 1471–120		1481–85		1481–100 1481–120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 3.0V, $\overline{MS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2		2		2		2		V
I_{CCDR}	Data Retention Current			400		125		800		250	µA
t_{CDR}[6]	Chip Deselect to Data Retention Time		0		0		0		0		ns
t_R	Operation Recovery Time		5		5		5		5		ns

Notes:

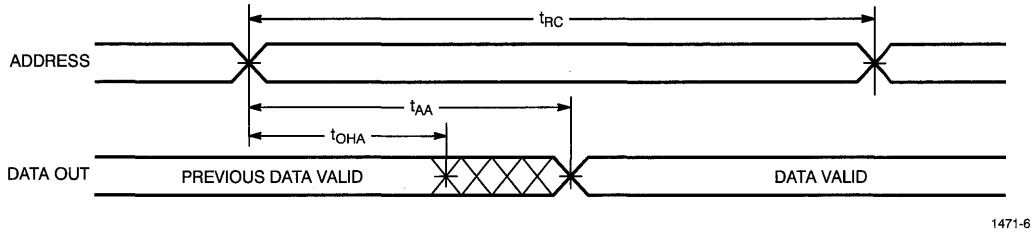
2. Test conditions assume signal transition time of 10 µs or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
3. t_{HZOE}, t_{HZMS}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. Guaranteed, not tested.

Data Retention Waveform

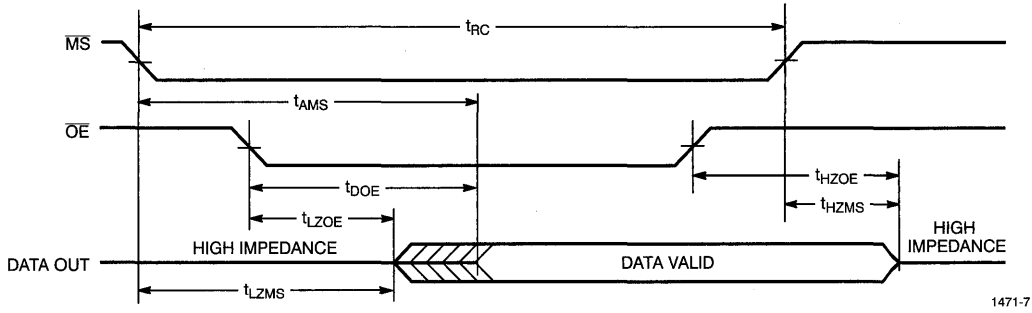


Switching Waveforms

Read Cycle No. 1[7, 8]



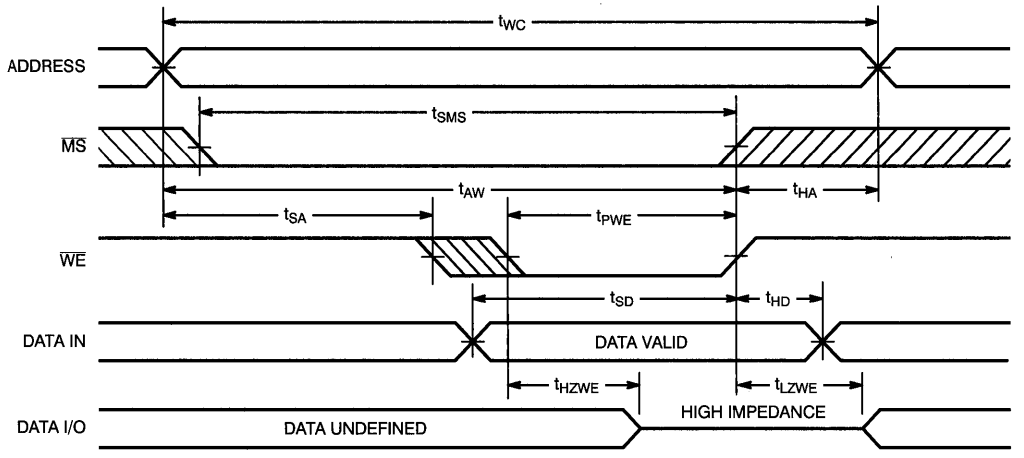
Read Cycle No. 2[8, 9]



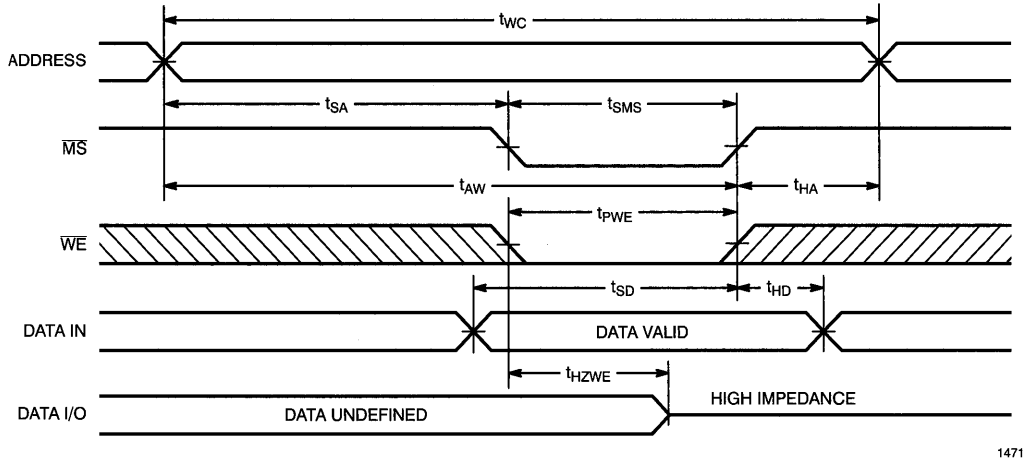
Notes:
7. Device is continuously selected. $\overline{OE}$, $\overline{MS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{MS}$ transition LOW
9. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 1[5, 10]



Write Cycle No. 2[5, 10, 11]



Notes:
10. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
11. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{MS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
85	CYM1471PF–85C	PF05	36-Pin Flat SIP Module	Commercial
	CYM1471LPF–85C			
	CYM1471PS–85C	PS08	36-Pin SIP Module	
	CYM1471LPS–85C			
100	CYM1471PF–100C	PF05	36-Pin Flat SIP Module	Commercial
	CYM1471LPF–100C			
	CYM1471PS–100C	PS08	36-Pin SIP Module	
	CYM1471LPS–100C			
120	CYM1471PF–120C	PF05	36-Pin Flat SIP Module	Commercial
	CYM1471LPF–120C			
	CYM1471PS–120C	PS08	36-Pin SIP Module	
	CYM1471LPS–120C			
85	CYM1481PF–85C	PF04	36-Pin Flat SIP Module	Commercial
	CYM1481LPF–85C			
	CYM1481PS–85C	PS06	36-Pin SIP Module	
	CYM1481LPS–85C			
100	CYM1481PF–100C	PF04	36-Pin Flat SIP Module	Commercial
	CYM1481LPF–100C			
	CYM1481PS–100C	PS06	36-Pin SIP Module	
	CYM1481LPS–100C			
120	CYM1481PF–120C	PF04	36-Pin Flat SIP Module	Commercial
	CYM1481LPF–120C			
	CYM1481PS–120C	PS06	36-Pin SIP Module	
	CYM1481LPS–120C			

Document #: 38–M–00041–A

PRELIMINARY **CYM1560**

1024K x 9 Buffered SRAM Module with Separate I/O

Features

- **High-density 8-megabit SRAM module plus parity**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Buffered address and control inputs**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.53 in.**
- **Small PCB footprint**
  - **1.5 sq. in.**

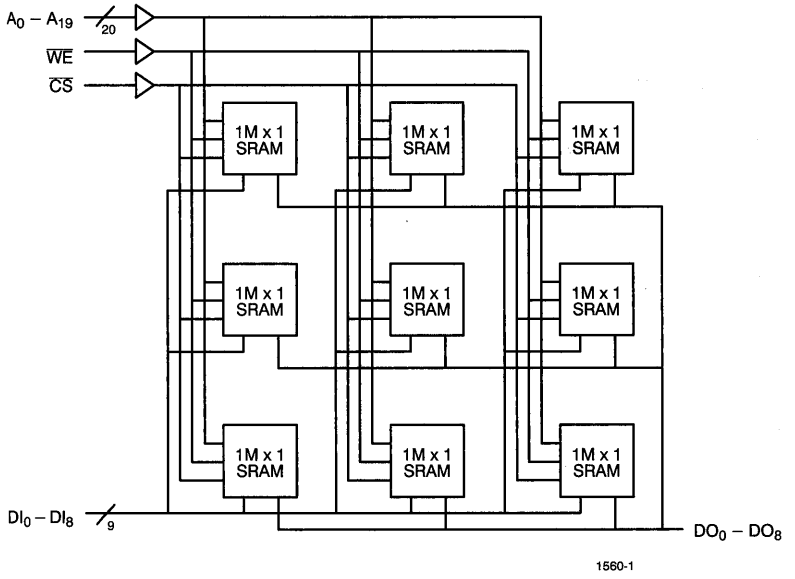
Functional Description

The CYM1560 is a very high performance 8-megabit static RAM module organized as 1024K words by 9 bits. This module is constructed using nine 1024K x 1 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. Input buffers are provided on the address and control lines to reduce input capacitance and loading.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data input pins (DI_0 through DI_8) of the device is written into the memory location specified on the address pins (A_0 through A_{19}). Reading the device is accomplished by taking chip select LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data output pins.

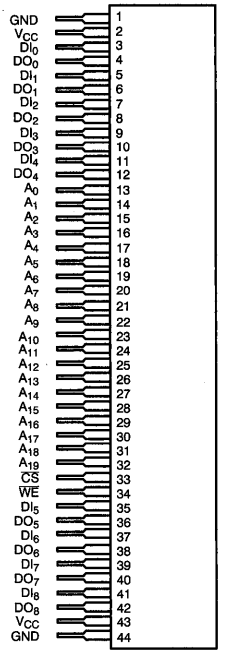
The data output pins remain in a high-impedance state when chip select is HIGH or when write enable is LOW.

Logic Block Diagram



Pin Configuration

SIP
Top View



Selection Guide

	CYM1560–30	CYM1560–35	CYM1560–45
Maximum Access Time (ns)	30	35	45
Maximum Operating Current (mA)	1125	1125	1125
Maximum Standby Current (mA)	350	350	350

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 45°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.3V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1560 Min.	CYM1560 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	V
V_{IL}	Input LOW Voltage		− 0.3	0.8	V
V_{IK}	Input Clamp Level, $A_0 - A_{19}$, $\overline{CS}$, $\overline{WE}$	V_{CC} = Min., I_{IN} = − 18 mA		− 1.2	V
I_{IL}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}, I_{OUT} = 0 mA		1125	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		350	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		230	mA

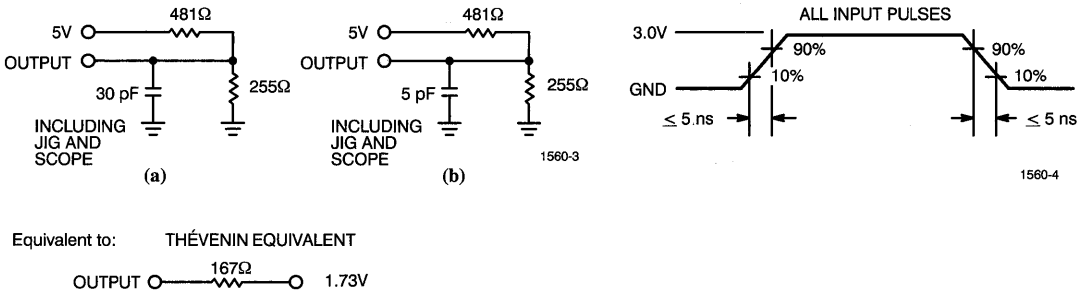
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3]

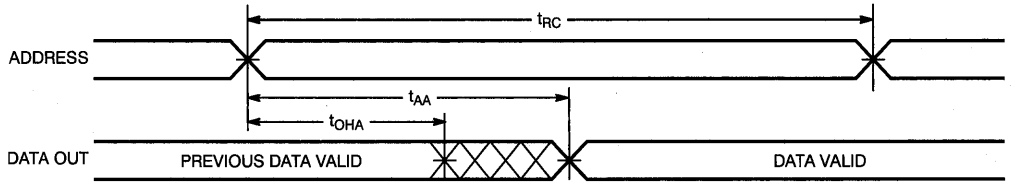
Parameters	Description	1560–30		1560–35		1560–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	30		35		45		ns
t_{AA}	Address to Data Valid		30		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	2	20	2	20	2	20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	3		3		3		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	2	20	2	20	2	20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.

Switching Waveforms

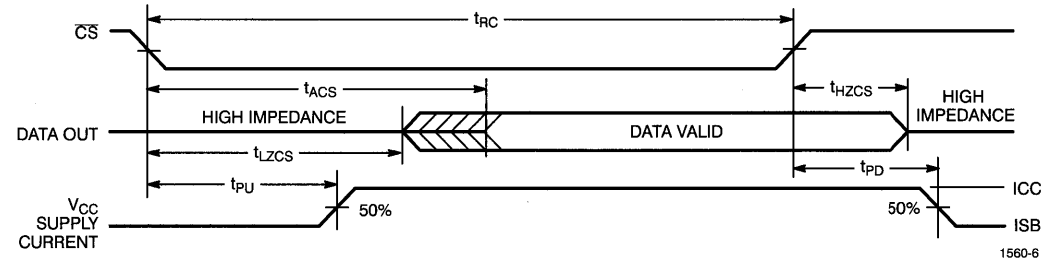
Read Cycle No. 1[6, 7]



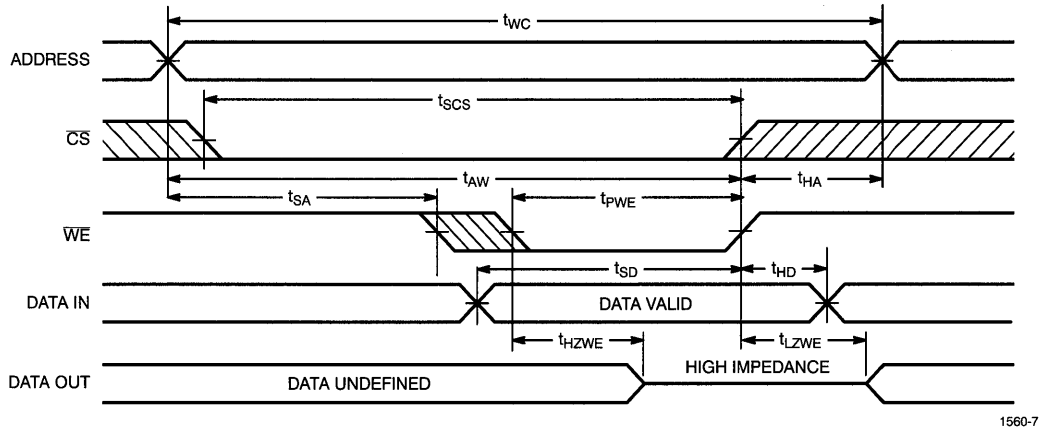
1560-5

Switching Waveforms (continued)

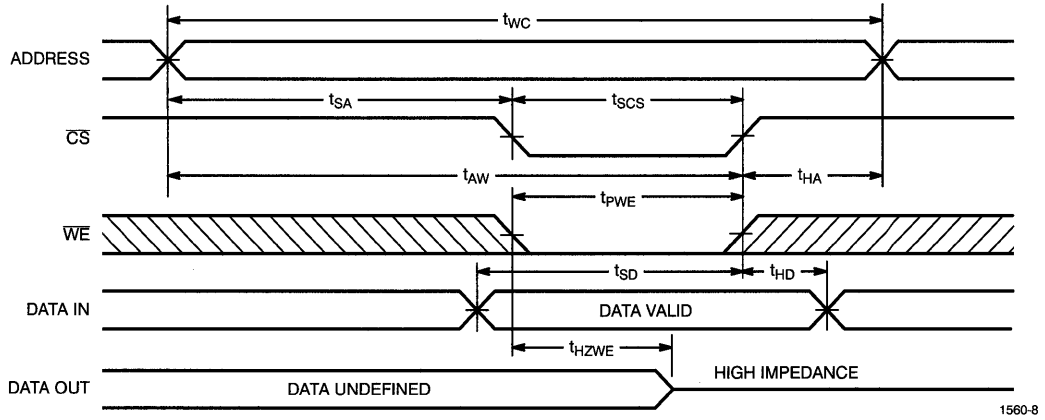
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Data In	Data Out	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	X	Data Out_{0-8}	Read
L	L	Data In_{0-8}	High Z	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
30	CYM1560PF–30C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–30C	PS07	44-Pin Plastic SIP Module	
35	CYM1560PF–35C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–35C	PS07	44-Pin Plastic SIP Module	
45	CYM1560PF–45C	PF06	44-Pin Flat SIP Module	Commercial
	CYM1560PS–45C	PS07	44-Pin Plastic SIP Module	

Document #: 38–M–00043–A

CYM1622

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **2.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pinout compatible with CYM1611**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **0.68 sq. in.**

Functional Description

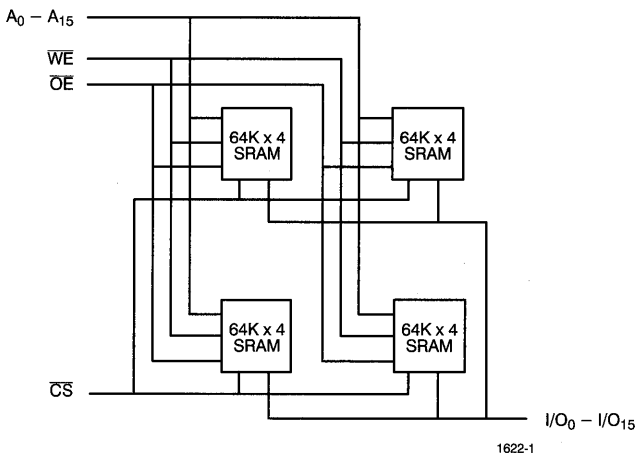
The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 64K x 4 static RAMs mounted onto a vertical substrate with pins. The pinout of this module is compatible with another Cypress module (CYM1611) to maximize system flexibility.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

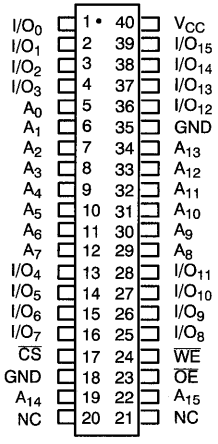
Logic Block Diagram



1622-1

Pin Configuration

VDIP
Top View



1622-2

Selection Guide

	1622–25	1622–30	1622–35	1622–45
Maximum Access Time (ns)	25	30	35	45
Maximum Operating Current (mA)	400	400	400	400
Maximum Standby Current (mA)	140	140	140	140

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +80°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1622 Min.	CYM1622 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		400	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		80	mA

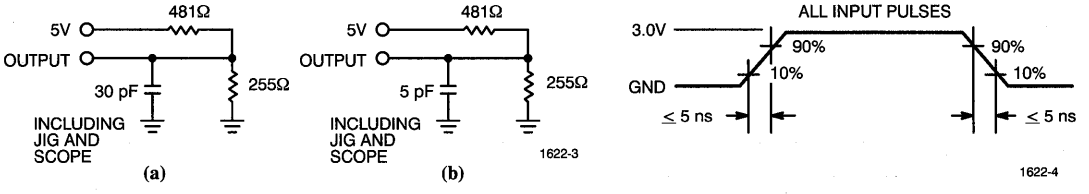
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

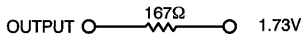
Notes:

1. $V_{IL(min.)}$ = − 3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

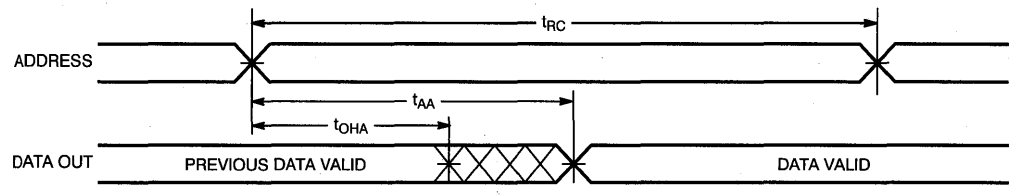
Parameter	Description	1622–25		1622–30		1622–35		1622–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid	25		30		35		45		ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid	25		30		35		45		ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0	25	0	30	0	35	0	45	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	15	0	15	0	15	0	20	ns

Notes:

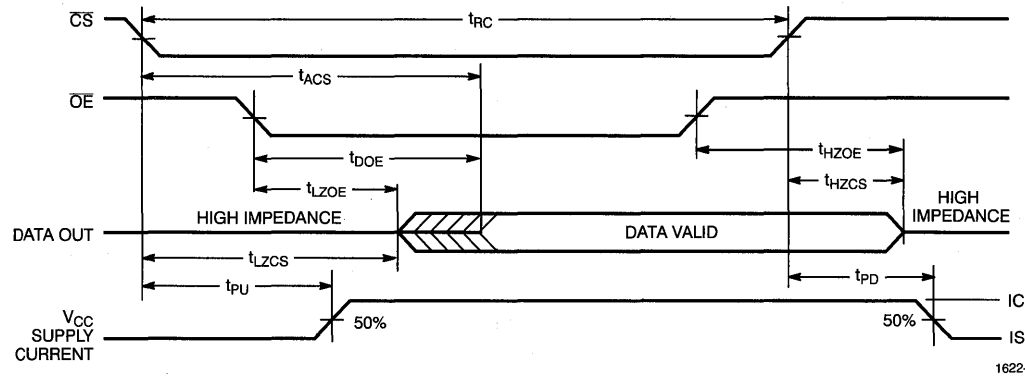
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

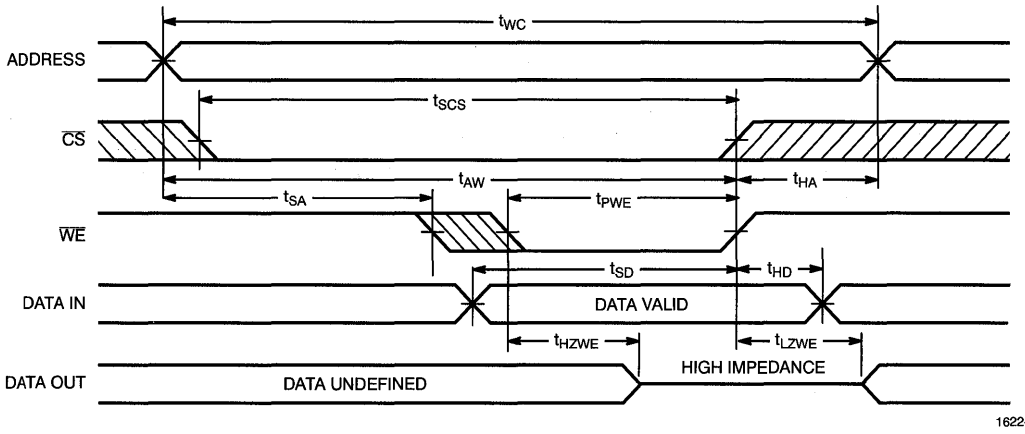
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



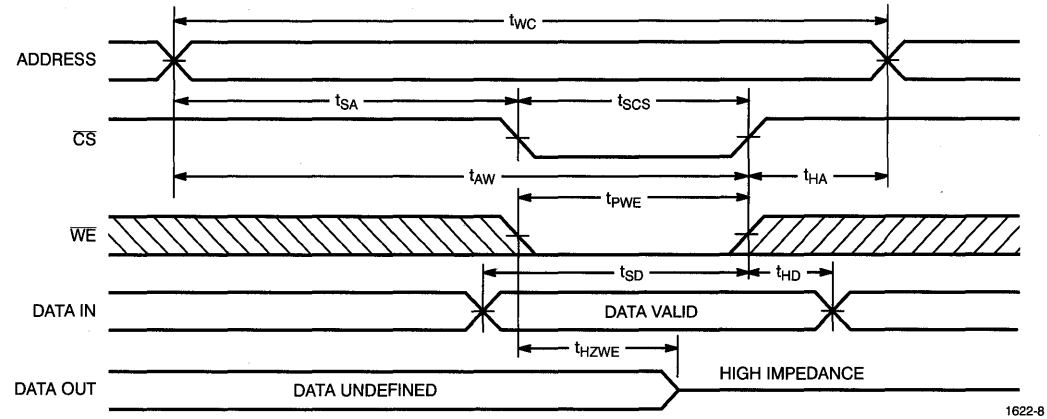
Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1622PV-25C	PV04	40-Pin Plastic VDIP Module	Commercial
30	CYM1622PV-30C	PV04	40-Pin Plastic VDIP Module	Commercial
35	CYM1622PV-35C	PV04	40-Pin Plastic VDIP Module	Commercial
45	CYM1622PV-45C	PV04	40-Pin Plastic VDIP Module	Commercial

Document #: 38-M-00001-C

CYM1720

CYPRESS SEMICONDUCTOR

32K x 24 Static RAM Module

Features

- **High-density 768-kilobit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  - **1.8W (max. for t_{AA} = 25 ns)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **0.66 sq. in.**

Functional Description

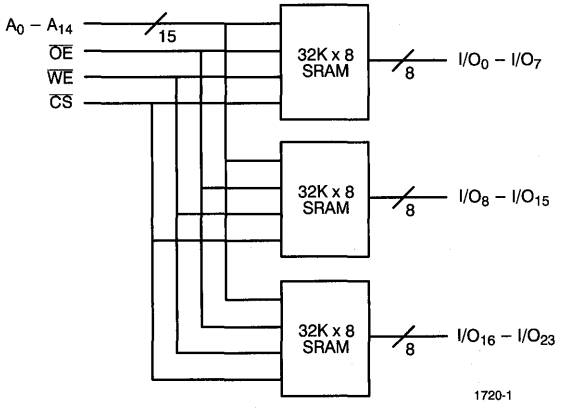
The CYM1720 is a high-performance 768-kilobit static RAM module organized as 32K words by 24 bits. This module is constructed using three 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

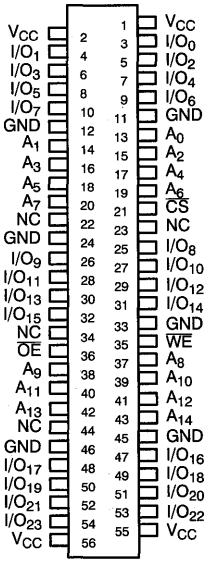
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration

ZIP
Top View



1720-2

Selection Guide

	1720–15	1720–20	1720–25	1720–30	1720–35
Maximum Access Time (ns)	15	20	25	30	35
Maximum Operating Current (mA)	450	450	330	330	330
Maximum Standby Current (mA)	120	120	60	60	60

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1720−15, 20		CYM1720−25, 30, 35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	− 20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		450		330	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		120		60	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		90		60	mA

Shaded area contains preliminary information.

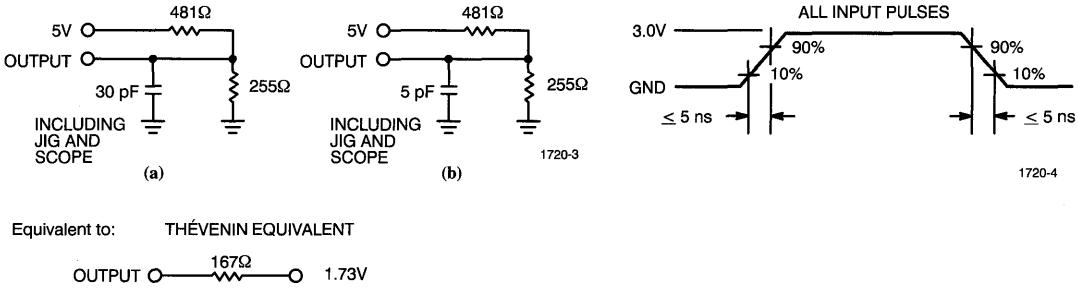
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

8 MODULES

Switching Characteristics Over the Operating Range[3]

Parameter	Description	1720–15		1720–20		1720–25		1720–30		1720–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		20		25		30		35		ns
t_{AA}	Address to Data Valid		25		20		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		20		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10		15		18	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		10		10		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		5		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		20		25		25		30	ns
WRITE CYCLE[6]												
t_{WC}	Write Cycle Time	25		20		25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		15		20		25		30		ns
t_{HA}	Address Hold from Write End	2		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		15		20		25		25		ns
t_{SD}	Data Set-Up to Write End	12		10		12		18		18		ns
t_{HD}	Data Hold from Write End	2		2		2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	10	0	8	0	10	0	15	0	15	ns

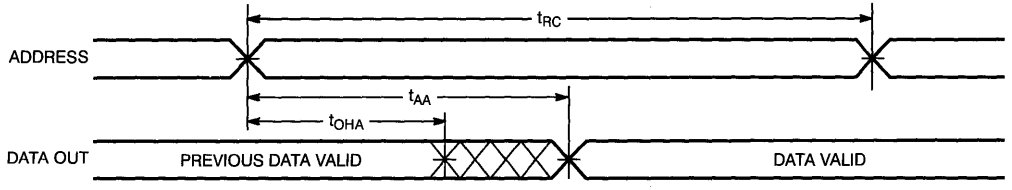
Shaded area contains preliminary information.

Notes:

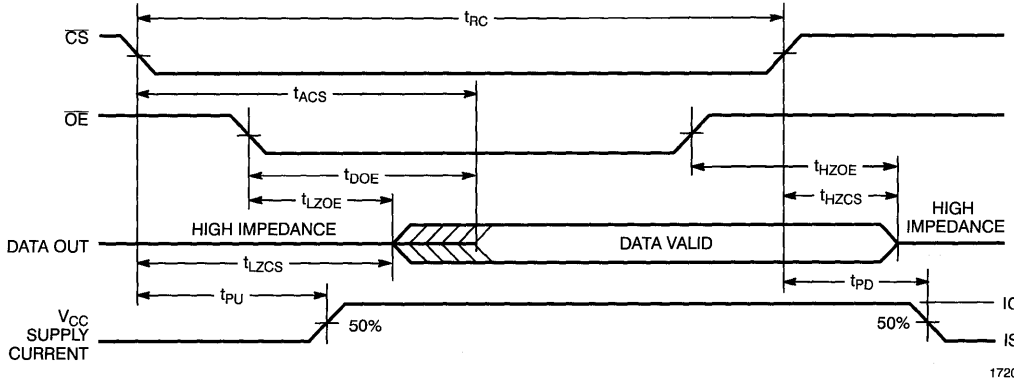
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

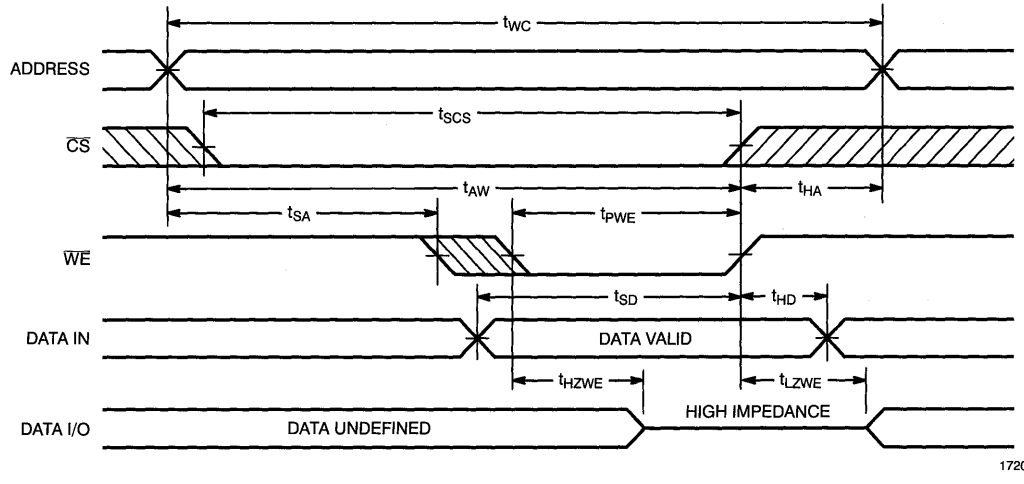
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



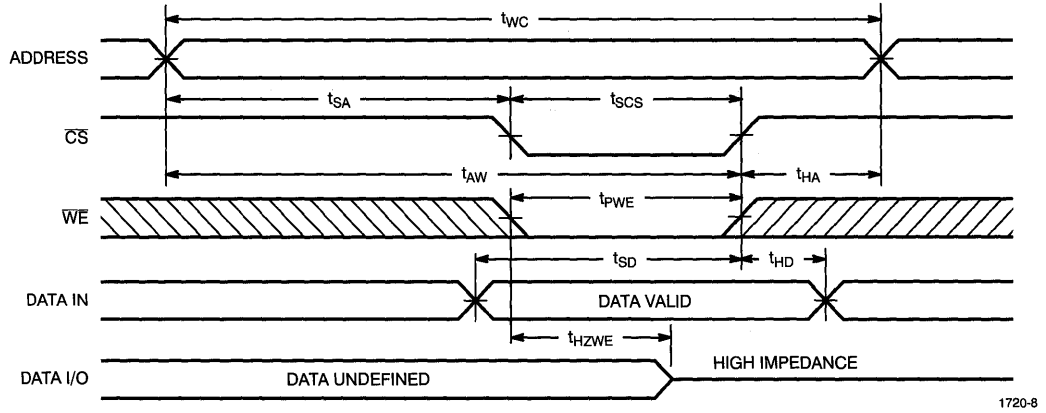
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1720PZ–15C	PZ05	56-Pin ZIP Module	Commercial
20	CYM1720PZ–20C	PZ05	56-Pin ZIP Module	Commercial
25	CYM1720PZ–25C	PZ05	56-Pin ZIP Module	Commercial
30	CYM1720PZ–30C	PZ05	56-Pin ZIP Module	Commercial
35	CYM1720PZ–35C	PZ05	56-Pin ZIP Module	Commercial

Document #: 38–M–00021–A

CYPRESS SEMICONDUCTOR

64K x 24 Static RAM Module

Features

- **High-density 1.5M SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  - **2.8W (max. for t_{AA} = 25 ns)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **1.05 sq. in.**

Functional Description

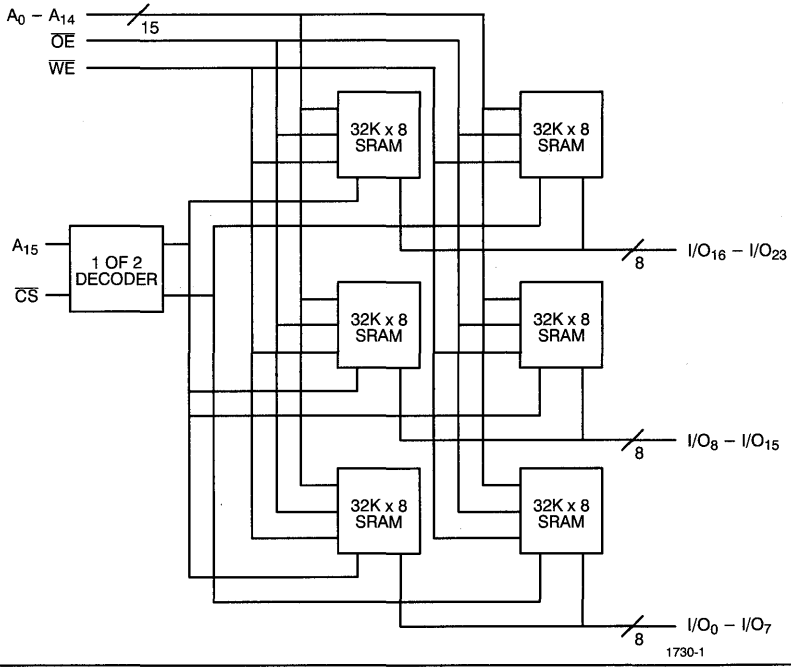
The CYM1730 is a high-performance 1.5M static RAM module organized as 64K words by 24 bits. This module is constructed using six 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

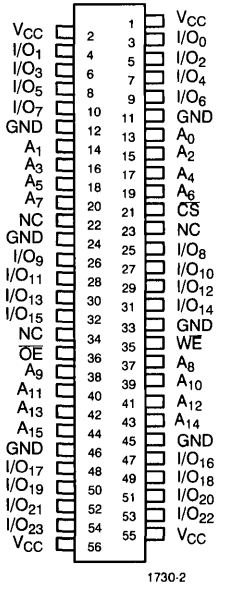
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1730–25	1730–30	1730–35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	510	510	510
Maximum Standby Current (mA)	180	180	180

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		510	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		180	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		180	mA

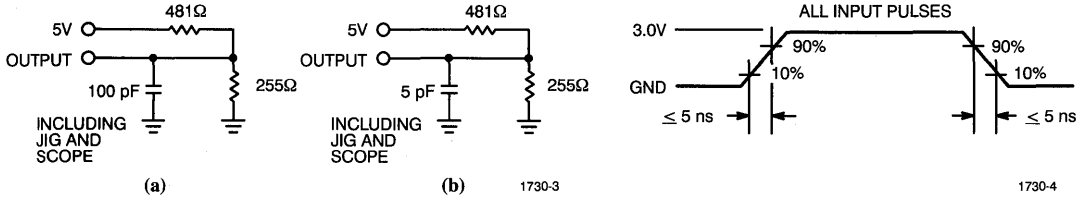
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		20	pF

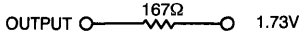
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

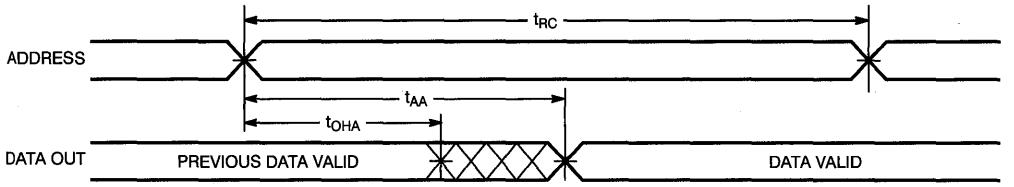
Parameter	Description	1730–25		1730–30		1730–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		15		15	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	22		25		30		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		23		25		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	10	0	10	0	15	ns

Notes:

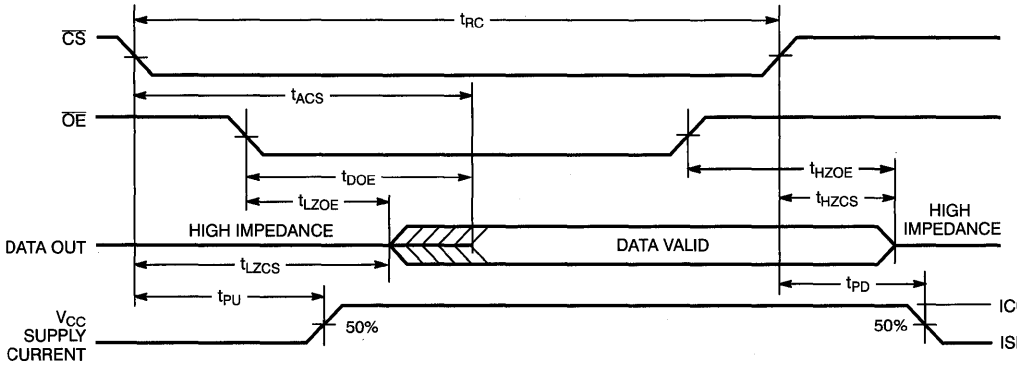
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

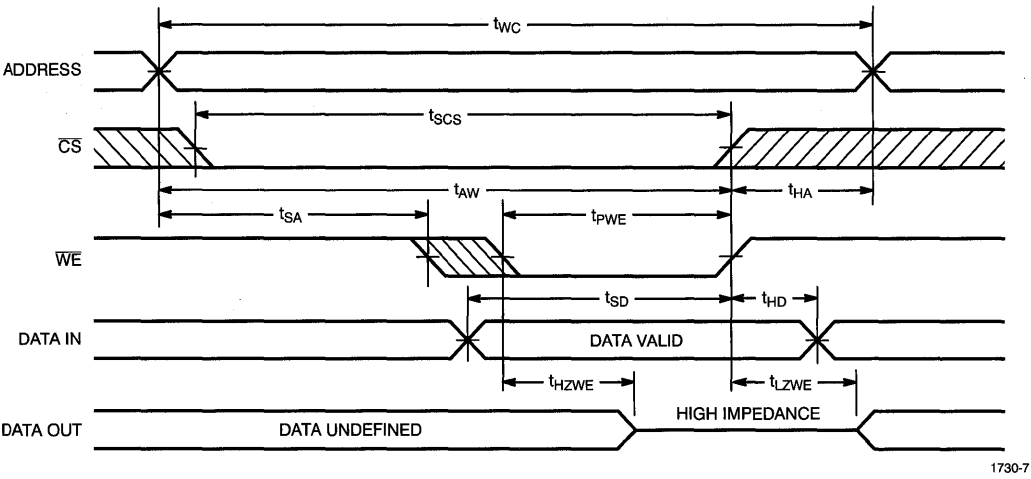
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



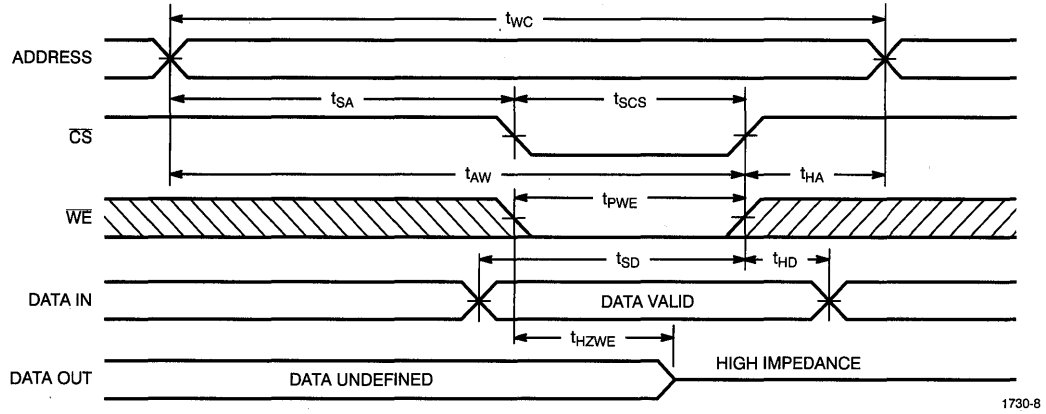
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if OE = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1730PZ–25C	PZ07	56-Pin ZIP Module	Commercial
30	CYM1730PZ–30C	PZ07	56-Pin ZIP Module	Commercial
35	CYM1730PZ–35C	PZ07	56-Pin ZIP Module	Commercial

Document #: 38–M–00049

CYM1821

16K x 32 Static RAM Module

Features

- **High-density 512-Kbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **1.0 sq. in.**
- **JEDEC-compatible pinout**
- **2V data retention (L version)**
- **SIMM version socket-compatible with CYM1831 and CYM1841**

Functional Description

The CYM1821 is a high-performance 512-Kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAM SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$, and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

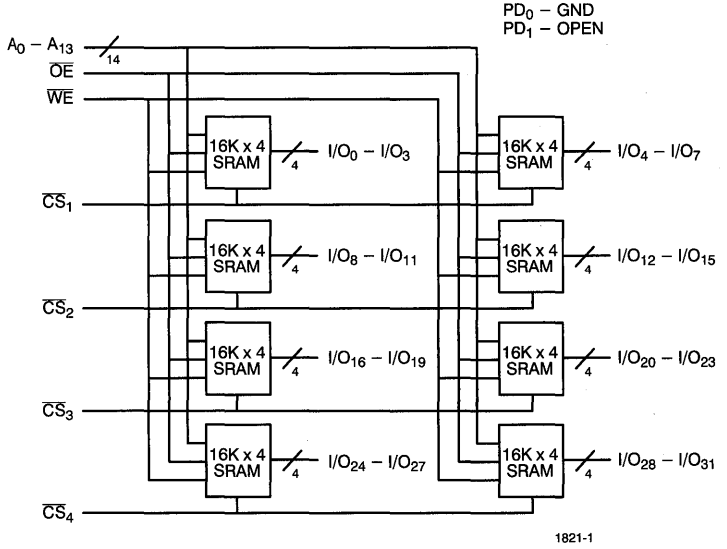
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

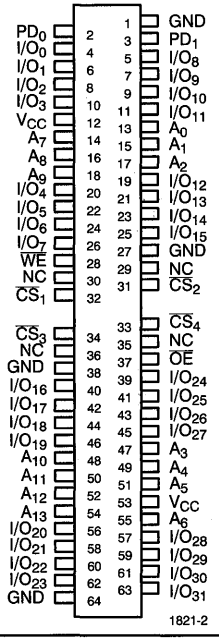
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1821–12	1821–15	1821–20	1821–25	1821–35	1821–45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	960	960	720	720	720	720
Maximum Standby Current (mA)	450	450	160	160	160	160

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1821−12 1821−15		1821−20 1821−25 1821−35 1821−45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 20	+20	− 20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 20	+20	− 20	+20	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		− 350		− 350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		450		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		160		160	mA

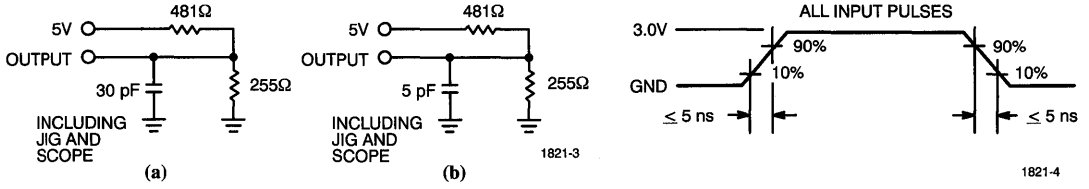
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (ADDR, $\overline{OE}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		35	pF
C_{OUT}	Output Capacitance		20	pF

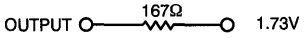
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameter	Description	1821–12		1821–15		1821–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	7	0	7	0	7	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

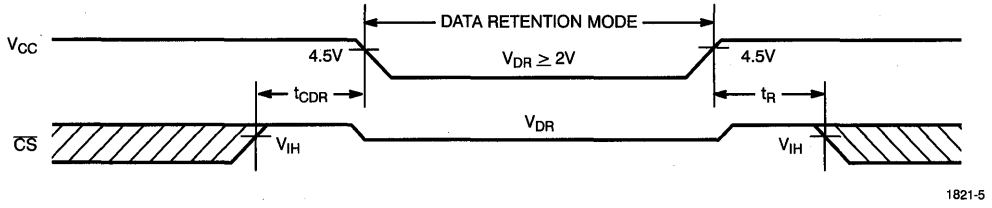
Parameter	Description	1821–25		1821–35		1821–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		10		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	7	0	10	0	15	ns

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1821		Unit
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2		V
I_{CCDR}	Data Retention Current			8	mA
t_{CDR}[8]	Chip Deselect to Data Retention Time		0		ns
t_R[8]	Operation Recovery Time		t_{RC}[9]		ns
I_{LI}[8]	Input Leakage Current			10	µA

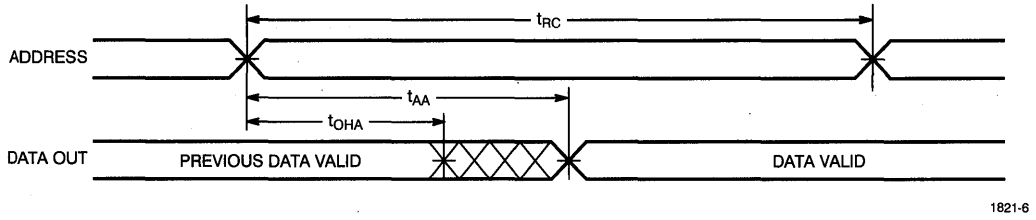
Notes:
8. Guaranteed, not tested.
9. t_{RC} = Read Cycle Time.

Data Retention Waveform

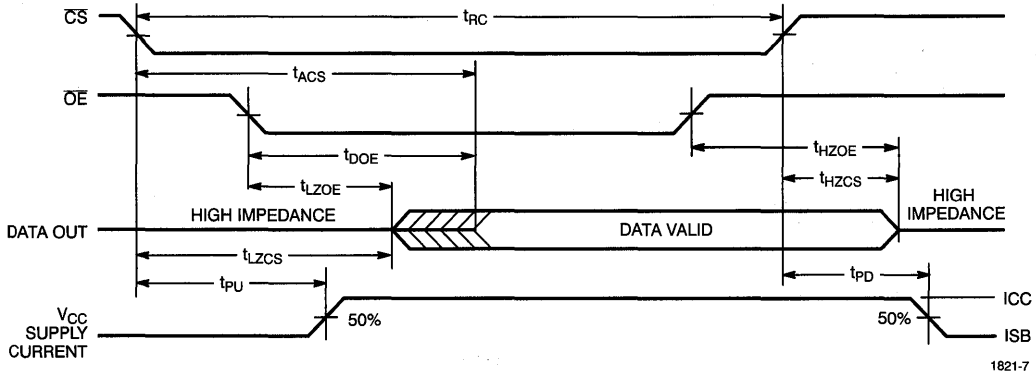


Switching Waveforms

Read Cycle No. 1[10, 11]



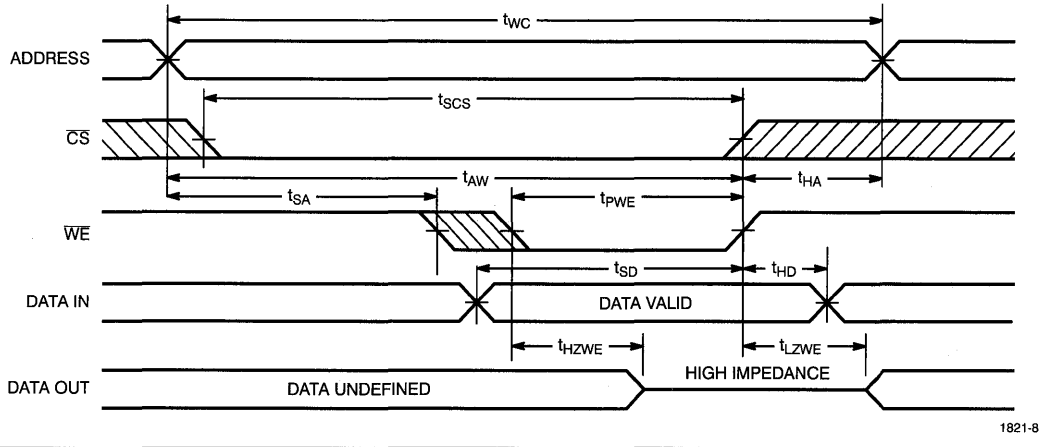
Read Cycle No. 2 ($\overline{WE}$ Controlled)[10, 12]



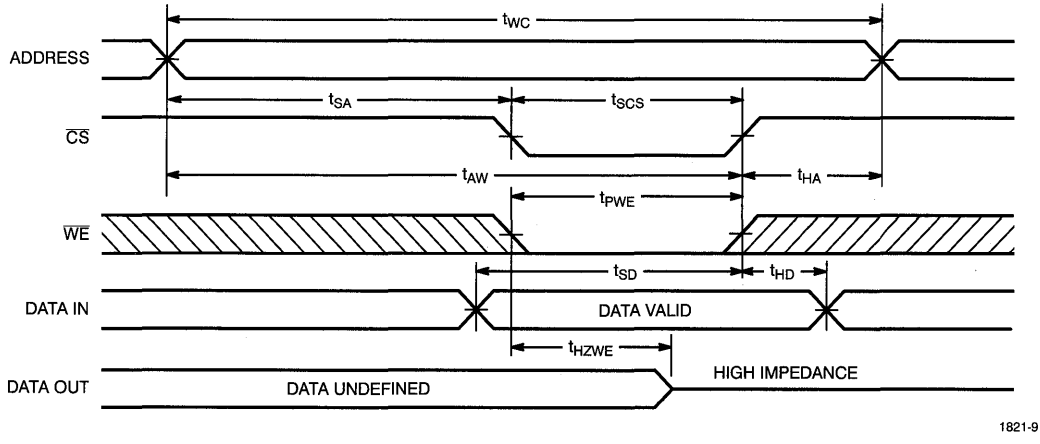
Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 13]



Note:
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS_N}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
12	CYM1821PM–12C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–12C	PZ01	64-Pin Plastic ZIP Module	
15	CYM1821PM–15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1821PM–20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM–20C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ–20C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ–20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1821PM–25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM–25C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ–25C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ–25C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1821PM–35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM–35C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ–35C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ–35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1821PM–45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM–45C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ–45C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ–45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38–M–00015–D

CYPRESS SEMICONDUCTOR

32K x 32 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **66-pin, 1.1-inch-square PGA package**
- **Low active power**
  - **3.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

The CYM1828 is a very high performance 1-megabit static RAM module organized as 32K words by 32 bits. The module is constructed using four 32K x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

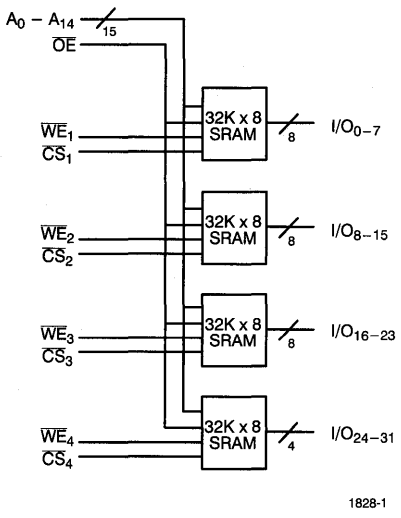
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW.

Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

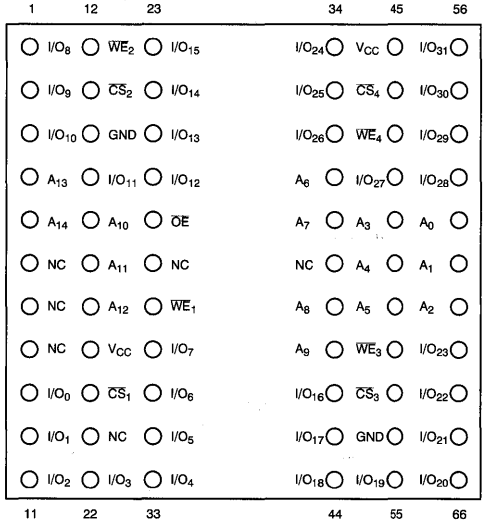
Logic Block Diagram



1828-1

Pin Configuration

Top View



1828-2

Selection Guide

		1828–25	1828–30	1828–35	1828–45	1828–55	1828–70
Maximum Access Time (ns)		25	30	35	45	55	70
Maximum Operating Current (mA)	Commercial	600	600	600	600	600	600
	Military			600	600	600	600
Maximum Standby Current (mA)	Commercial	200	200	200	200	200	200
	Military			200	200	200	200

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C
Supply Voltage to Ground Potential ..... − 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V
DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

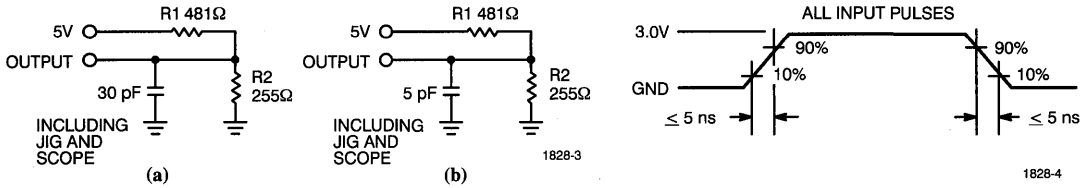
Parameter	Description	Test Conditions		1828 Min.	1828 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage			− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		− 20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		− 20	+20	μA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			600	mA
			L Version		400	
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			360	mA
			L Version		230	
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			240	mA
			L Version		145	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			200	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V			100	mA

Capacitance[2]

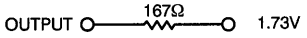
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1828–25		1828–30		1828–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		17		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		15		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-Up to Write End	15		20		17		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	20	0	30	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

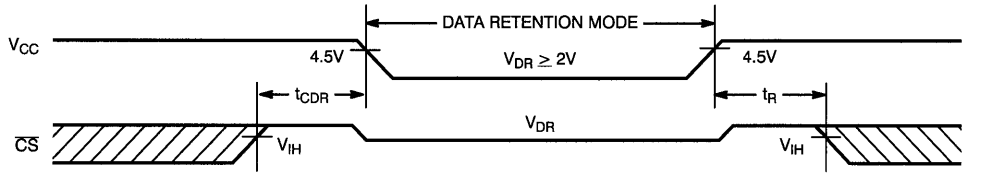
Parameter	Description	1828–45		1828–55		1828–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		25		30		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		30		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		45		55		ns
t_{AW}	Address Set-Up to Write End	40		45		55		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	25		30		40		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	30	0	30	0	30	ns

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1828		Unit
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		V
I_{CCDR3}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $V_{DR} = 3.0V$		320	µA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0		ns
t_R[7]	Operation Recovery Time		t_{RC}		ns

Note:
7. Guaranteed, not tested.

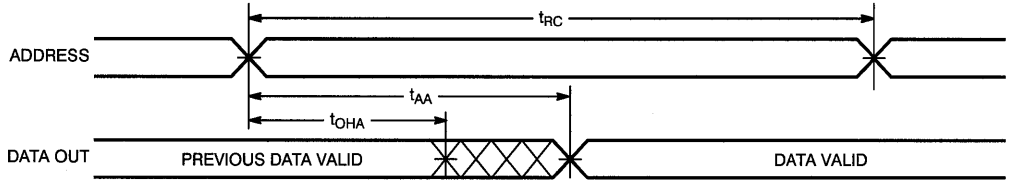
Data Retention Waveform



1828-5

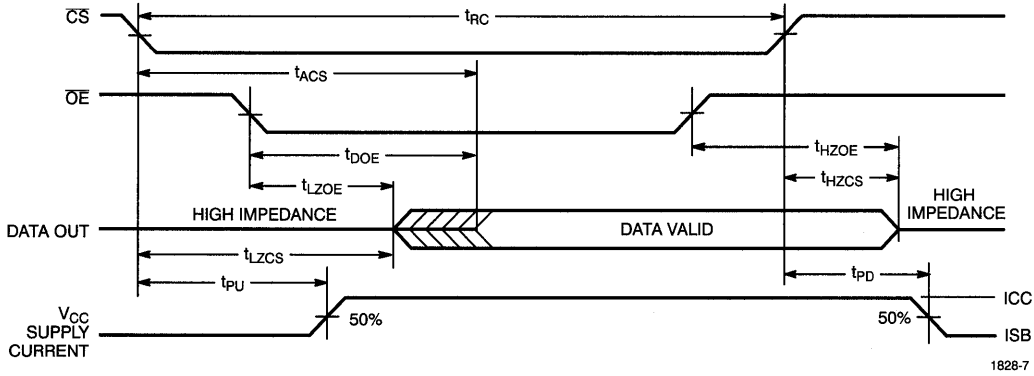
Switching Waveforms

Read Cycle No. 1[8, 9]



1828-6

Read Cycle No. 2[8, 10]

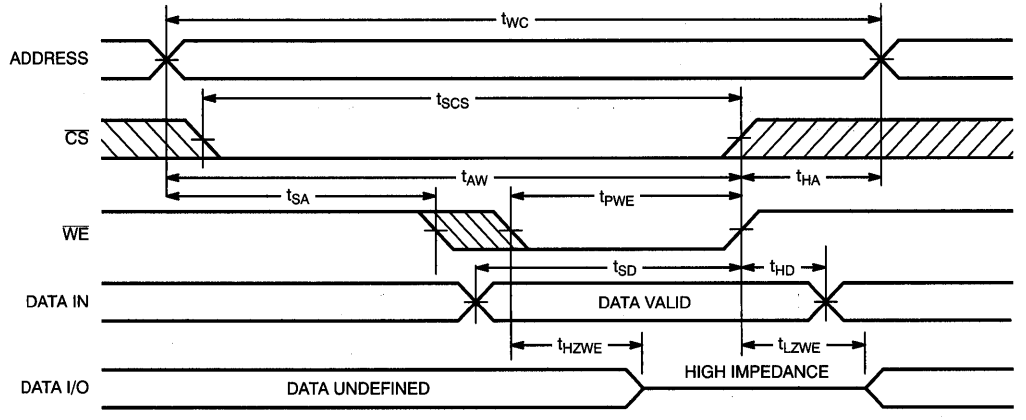


1828-7

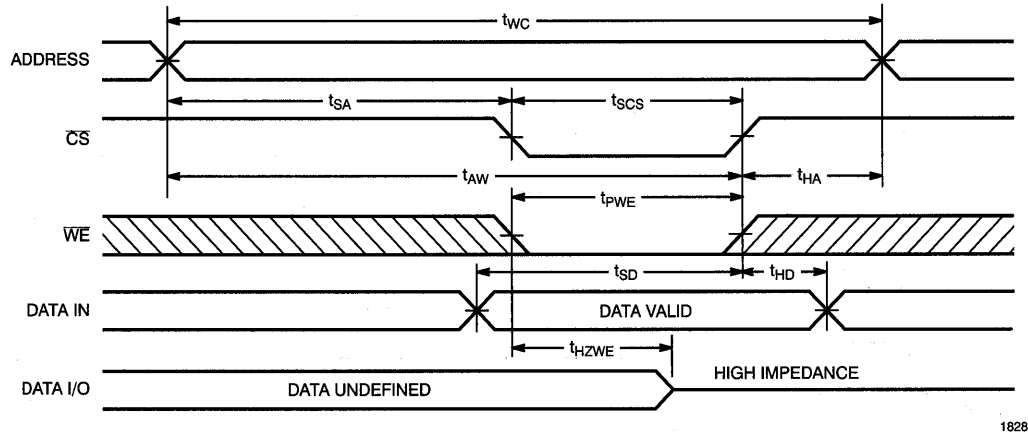
Notes:
8. $\overline{WE}_N$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 11]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 11, 12]



Notes:

11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}_N$ goes HIGH simultaneously with $\overline{WE}_N$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{OE}$	$\overline{WE}_N$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1828HG–25C	HG01	66-Pin PGA Module	Commercial
30	CYM1828HG–30C	HG01	66-Pin PGA Module	Commercial
35	CYM1828HG–35C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–35C	HG01	66-Pin PGA Module	
	CYM1828HG–35MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–35MB	HG01	66-Pin PGA Module	
45	CYM1828HG–45C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–45C	HG01	66-Pin PGA Module	
	CYM1828HG–45MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–45MB	HG01	66-Pin PGA Module	
55	CYM1828HG–55C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–55C	HG01	66-Pin PGA Module	
	CYM1828HG–55MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–55MB	HG01	66-Pin PGA Module	
70	CYM1828HG–70C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–70C	HG01	66-Pin PGA Module	
	CYM1828HG–70MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–70MB	HG01	66-Pin PGA Module	

Document #: 38–M–00042

CYPRESS SEMICONDUCTOR

CYM1831

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **Low active power**
  - **5.3W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **1.2 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1831 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

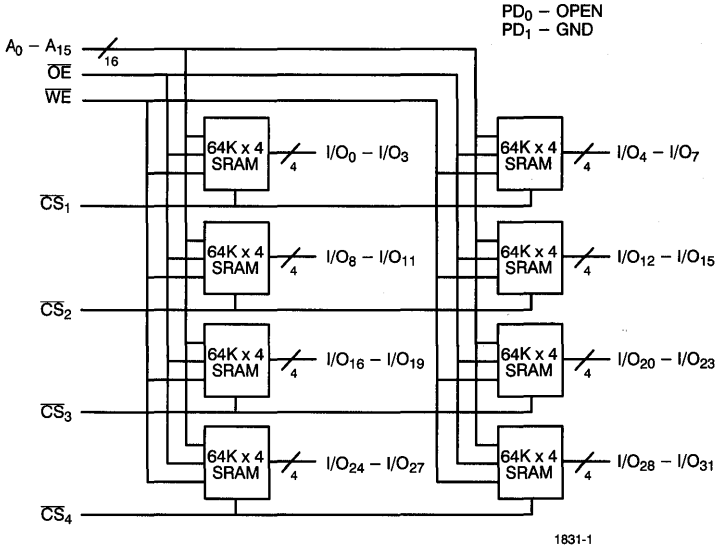
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW or the appropriate chip selects are HIGH.

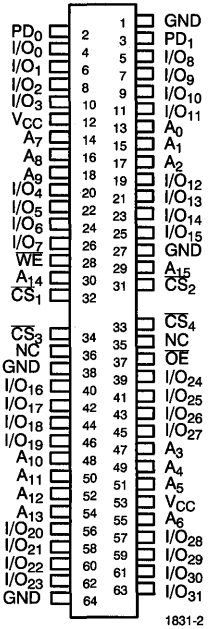
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP/SIMM
Top View



Selection Guide

	1831–15	1831–20	1831–25	1831–30	1831–35	1831–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	1120	960	720	720	720	720
Maximum Standby Current (mA)	160	160	160	160	160	160

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1831−15		1831−20		1831−25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	−20	+20	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}		1120		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}_N$ ≥ V_{IH}, Min. Duty Cycle = 100%		320		320		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}_N$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		160		160		160	mA

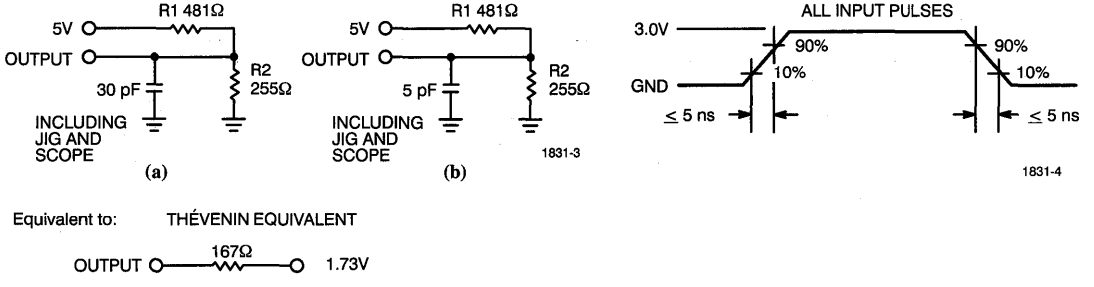
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (A_0 − A_{15}, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance (I/O_0 − I/O_{31})		15	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

8 MODULES

Switching Characteristics Over the Operating Range[3]

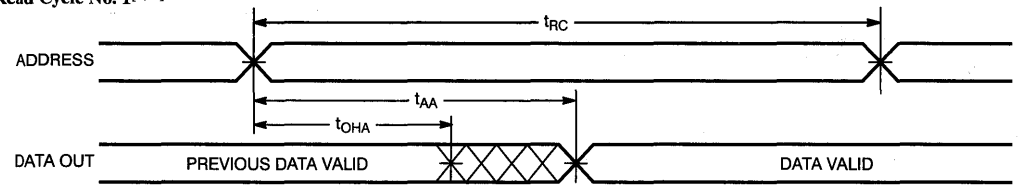
Parameter	Description	1831–15		1831–20		1831–25		1831–30		1831–35		1831–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		15		20		20		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		8		10		15		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	0		0		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		6		8		13		15		20		20	ns
WRITE CYCLE[6]														
t_{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		15		20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	8		12		15		15		20		20		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	7	0	10	0	13	0	15	0	20	0	20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.

Switching Waveforms

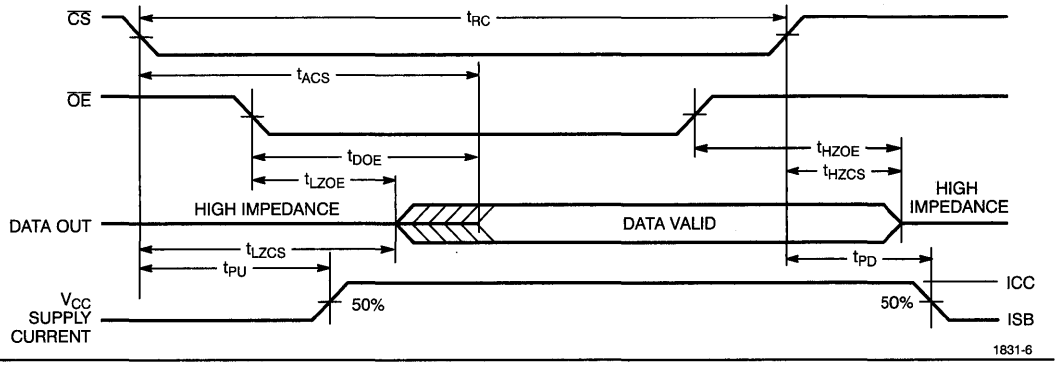
Read Cycle No. 1[7, 8]



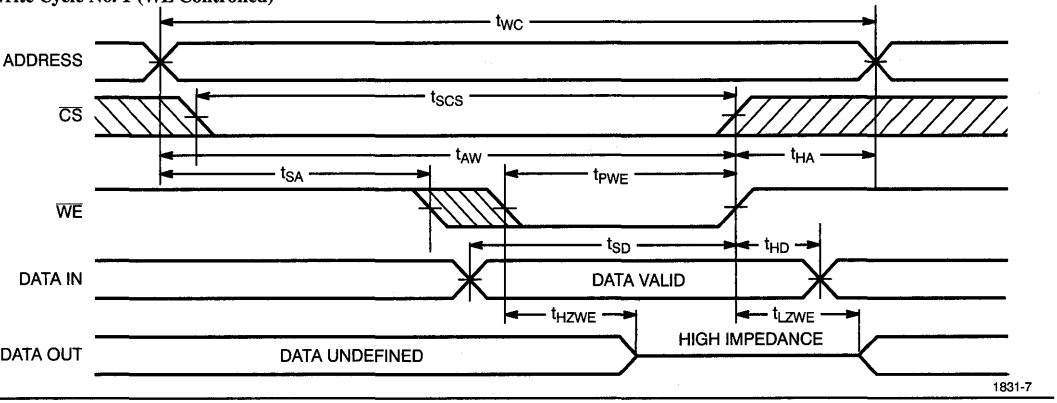
1831-5

Switching Waveforms

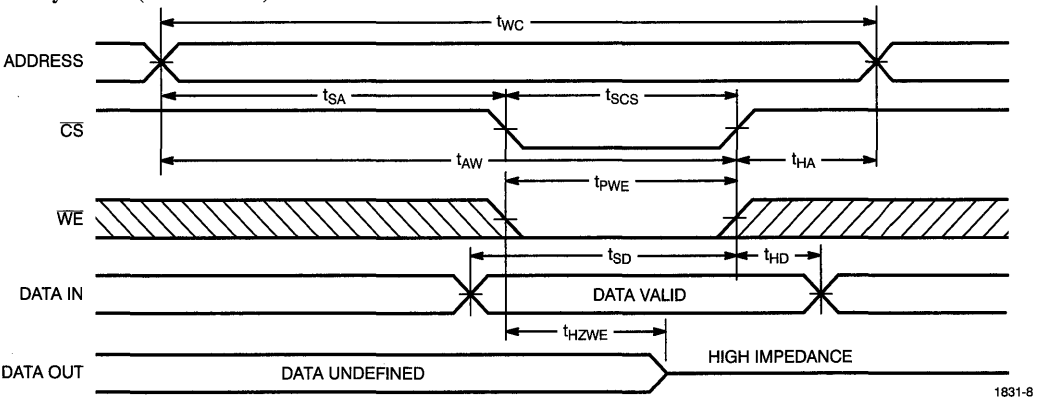
Read Cycle No. 2[7, 9]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Note:
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS_N}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1831PM–15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–15C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1831PM–20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–20C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1831PM–25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–25C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–25C	PZ01	64-Pin Plastic ZIP Module	
30	CYM1831PM–30C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–30C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–30C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1831PM–35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–35C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1831PM–45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–45C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38–M–00018–D

CYM1832

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **5.4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .5 in.**
- **Small PCB footprint**
  - **1.0 sq. in.**

Functional Description

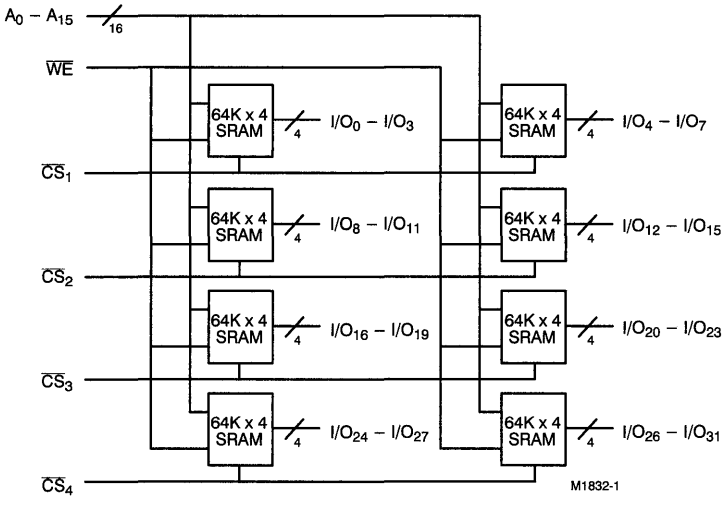
The CYM1832 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$, and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the chip select ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

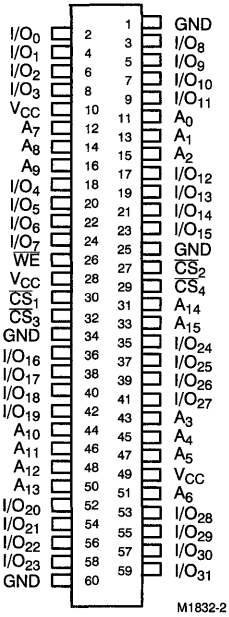
The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1832–25	1832–35	1832–45	1832–55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	980	980	980	980
Maximum Standby Current (mA)	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 45°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1832 Min.	CYM1832 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 100	+100	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N \le V_{IL}$		980	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N \ge V_{IH}$, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le$ 0.2V		120	mA

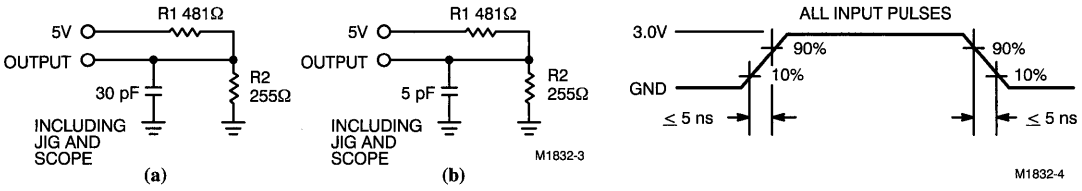
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (A_X, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		25	pF
C_{OUT}	Output Capacitance		15	pF

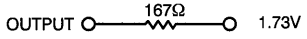
Notes:

1. $V_{IN(min.)}$ = − 3.0V for pulse widths less than 20 ns.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

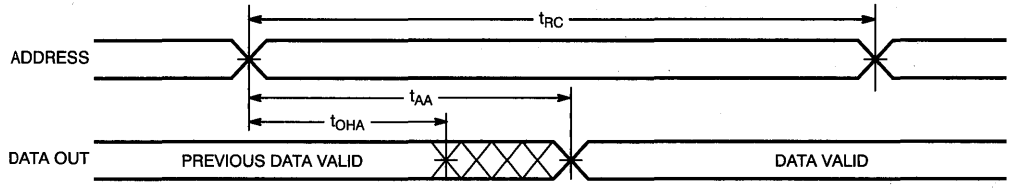
Parameter	Description	1832–25		1832–35		1832–45		1832–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	2		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]	0	15	0	25	0	30	0	30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45		55	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		40		45		ns
t_{AW}	Address Set-Up to Write End	20		30		35		45		ns
t_{HA}	Address Hold from Write End	2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		3		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		35		45		ns
t_{SD}	Data Set-Up to Write End	15		20		25		35		ns
t_{HD}	Data Hold from Write End	3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	20	0	30	ns

Notes:

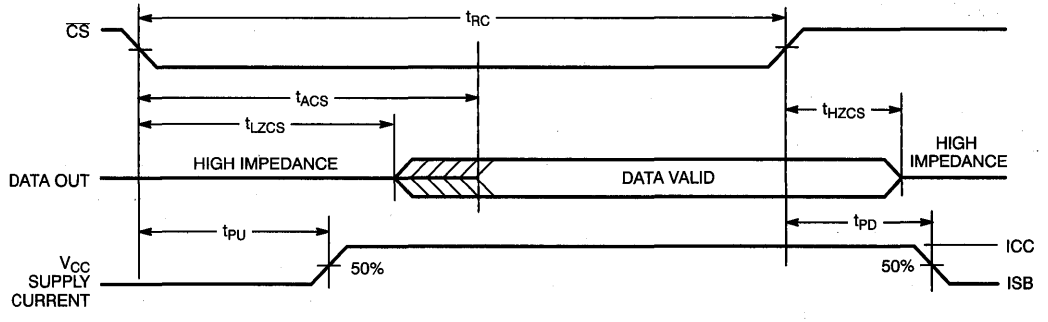
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

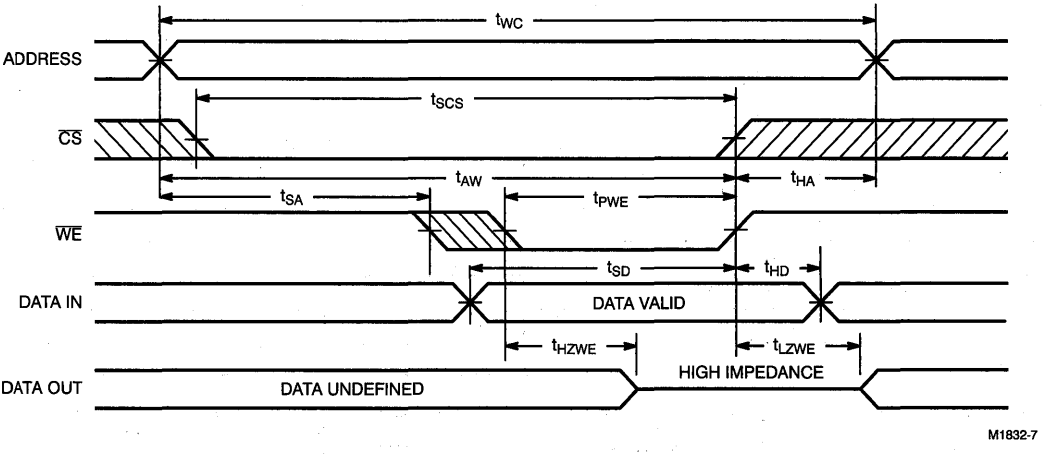
Read Cycle No. 1[8, 9]



Read Cycle No. 2[9, 10]



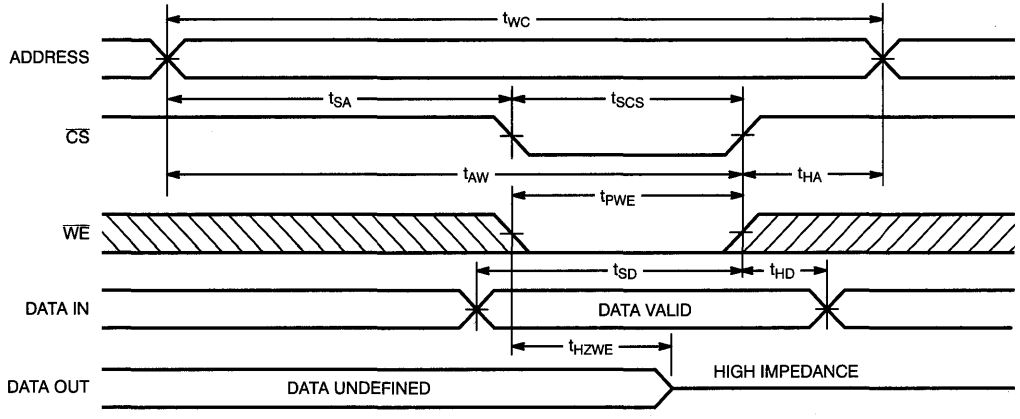
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Notes:
8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. $\overline{WE}$ is HIGH for read cycle.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1832PZ–25C	PZ02	60-Pin Plastic ZIP Module	Commercial
35	CYM1832PZ–35C	PZ02	60-Pin Plastic ZIP Module	Commercial
45	CYM1832PZ–45C	PZ02	60-Pin Plastic ZIP Module	Commercial
55	CYM1832PZ–55C	PZ02	60-Pin Plastic ZIP Module	Commercial

Document #: 38–M–00019–A

CYM1836

CYPRESS SEMICONDUCTOR

128K x 32 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **2.6W (max.) at 20 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.57 in.**
- **JEDEC-compatible pinout**
- **Small PCB footprint**
  - **0.78 sq. in.**
- **Available in SIMM, ZIP, or PLCC format**

Functional Description

The CYM1836 is a high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

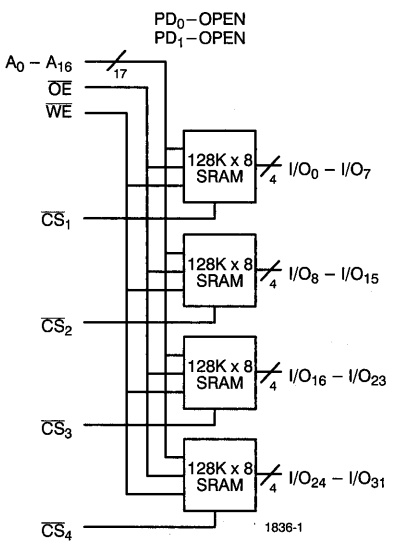
Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

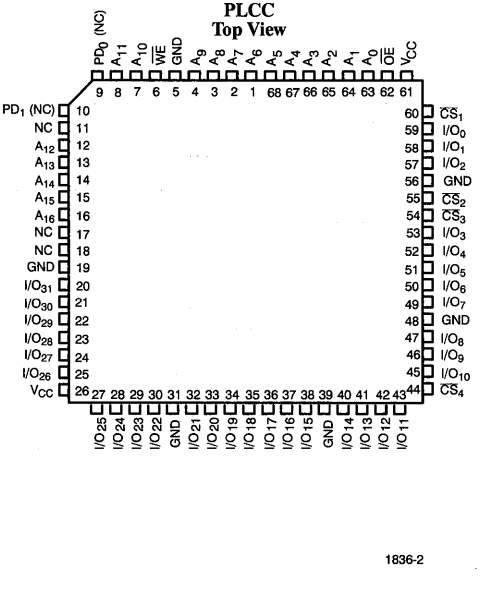
The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

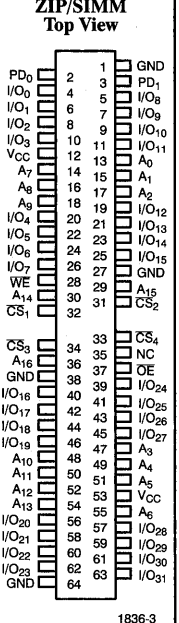
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configurations





Selection Guide

	1836–20	1836–25	1836–30	1836–35	1836–45
Maximum Access Time (ns)	20	25	30	35	45
Maximum Operating Current (mA)	480	480	480	480	480
Maximum Standby Current (mA)	100	100	100	100	100

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1836 Min.	1836 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		480	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max. , $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		100	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max. , $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		28	mA

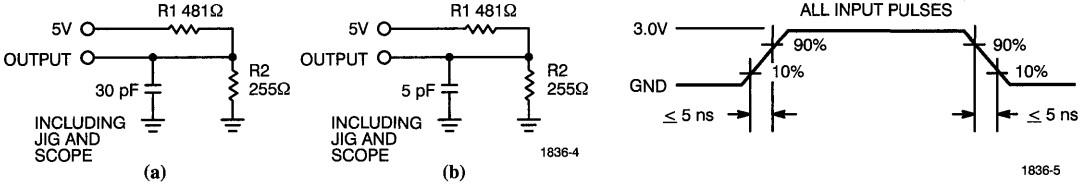
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		15	pF

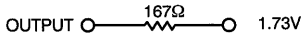
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1836–20		1836–25		1836–30		1836–35		1836–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		30		35		45		ns
t_{AA}	Address to Data Valid		20		25		30		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		8		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		10		11		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		10		13		15		18	ns
WRITE CYCLE[6]												
t_{WC}	Write Cycle Time	20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		15		18		20		25		ns
t_{AW}	Address Set-Up to Write End	15		15		18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		18		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		13		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	8	0	10	0	15	0	15	0	18	ns

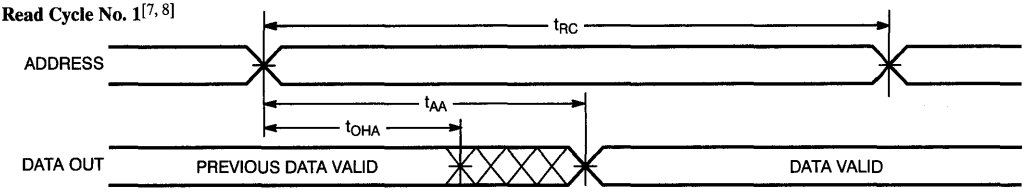
Shaded area contains preliminary information.

Notes:

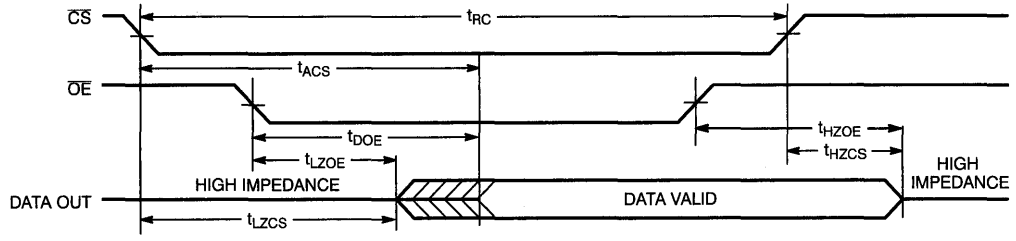
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

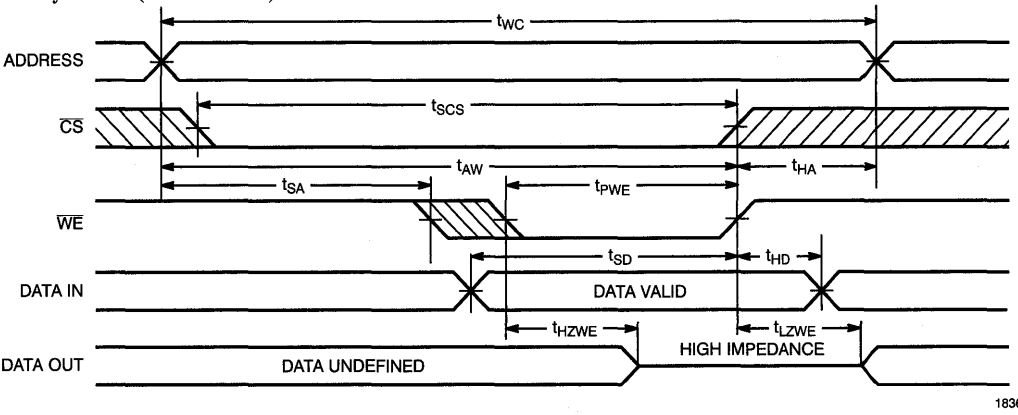
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



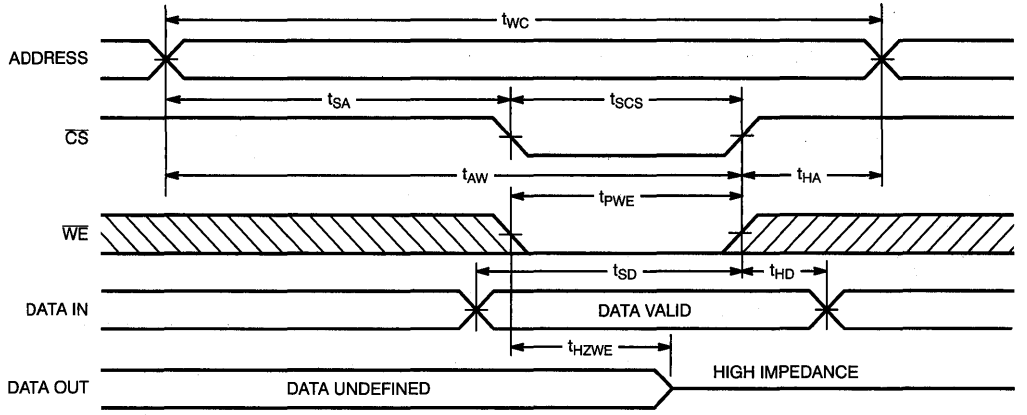
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1836PJ–20C	J81	68-Lead PLCC Module	Commercial
	CYM1836PM–20C	PM03	64-Pin SIMM Module	
	CYM1836PZ–20C	PZ08	64-Pin ZIP Module	
25	CYM1836PJ–25C	J81	68-Lead PLCC Module	Commercial
	CYM1836PM–25C	PM03	64-Pin SIMM Module	
	CYM1836PZ–25C	PZ08	64-Pin ZIP Module	
30	CYM1836PJ–30C	J81	68-Lead PLCC Module	Commercial
	CYM1836PM–30C	PM03	64-Pin SIMM Module	
	CYM1836PZ–30C	PZ08	64-Pin ZIP Module	
35	CYM1836PM–35C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ–35C	PZ08	64-Pin ZIP Module	
45	CYM1836PM–45C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ–45C	PZ08	64-Pin ZIP Module	

Shaded areas contain preliminary information

Document #: 38–M–00050–A

CYPRESS SEMICONDUCTOR

128K x 32 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **66-pin, 1.1-inch-square PGA package**
- **Low active power**
  - **4.0W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

The CYM1838 is a very high performance 4-megabit static RAM module organized as 128K words by 32 bits. The module is constructed using four 128K x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

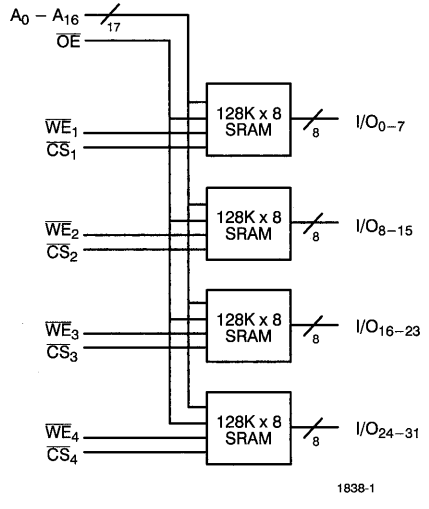
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW.

Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

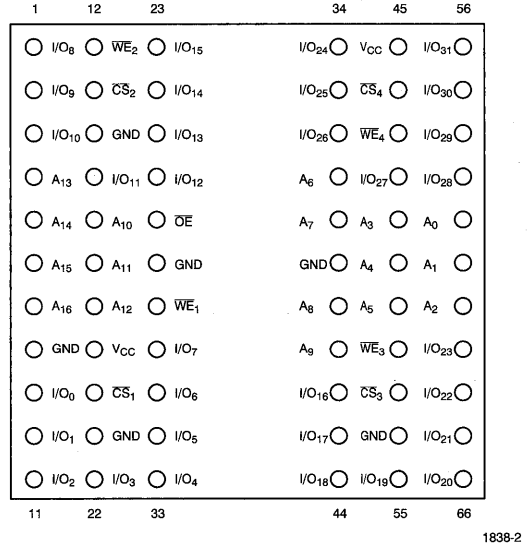
The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

PGA
Top View



Selection Guide

		1838–25	1838–30	1838–35
Maximum Access Time (ns)		25	30	35
Maximum Operating Current (mA)	Commercial	720	720	720
	Military	720	720	720
Maximum Standby Current (mA)	Commercial	240	240	240
	Military	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C
Supply Voltage to Ground Potential ..... − 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V
DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1838 Min.	1838 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	V
V_{IL}	Input LOW Voltage		− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		720	mA
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		480	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		360	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		40	mA

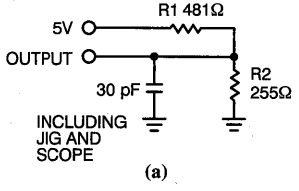
Capacitance[2]

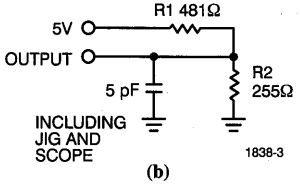
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		50	pF

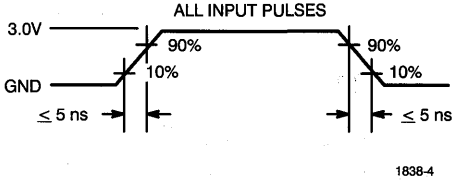
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

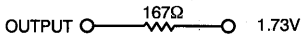
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

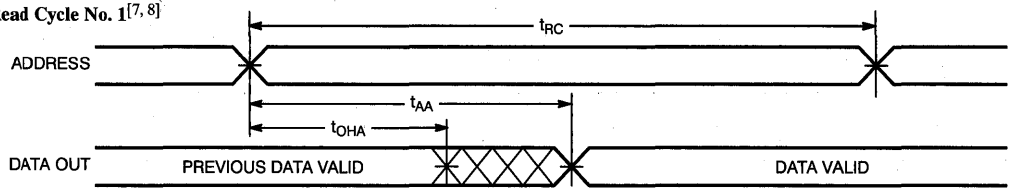
Parameter	Description	1838–25		1838–30		1838–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		13		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		18		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	17		21		25		ns
t_{SD}	Data Set-Up to Write End	12		13		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	10	0	12	0	15	ns

Notes:

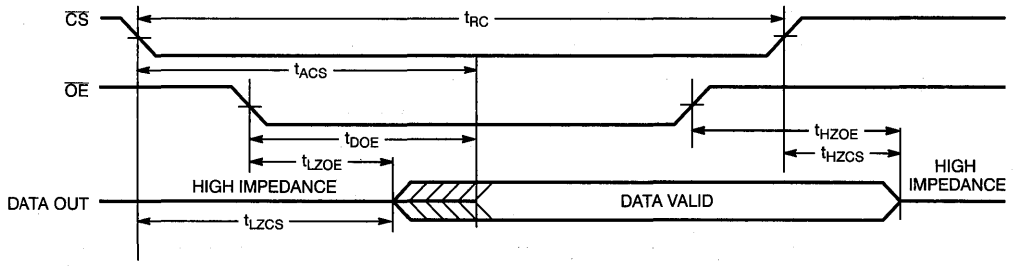
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

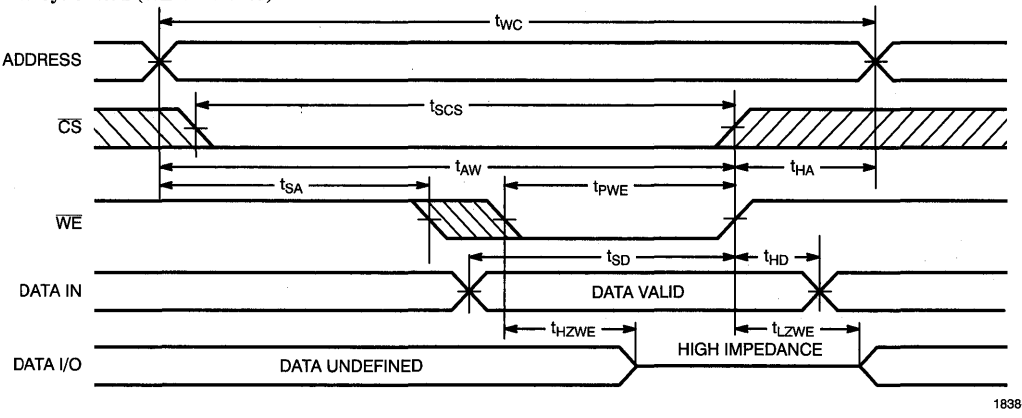
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



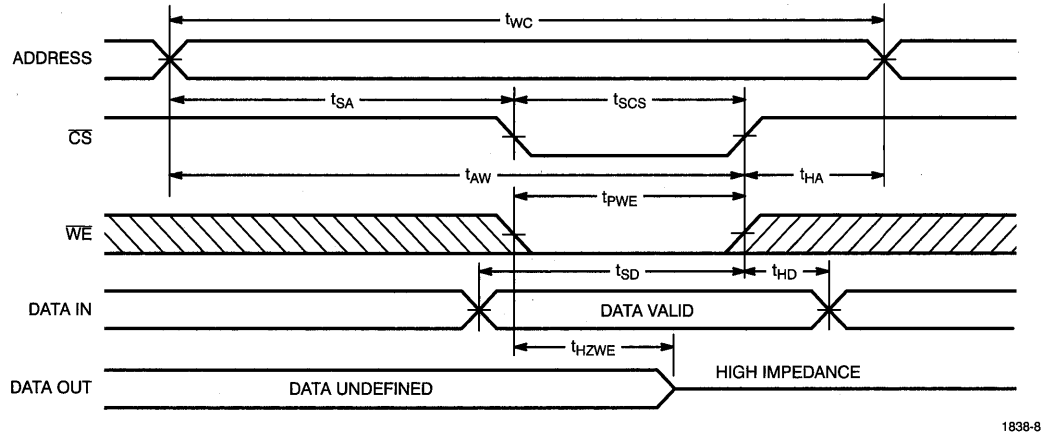
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}_N$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{OE}$	$\overline{WE}_N$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1838HG–25C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–25M	HG01	66-Pin PGA Module	Military
	CYM1838HG–25MB	HG01	66-Pin PGA Module	
30	CYM1838HG–30C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–30M	HG01	66-Pin PGA Module	Military
	CYM1838HG–30MB	HG01	66-Pin PGA Module	
35	CYM1838HG–35C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–35M	HG01	66-Pin PGA Module	Military
	CYM1838HG–35MB	HG01	66-Pin PGA Module	

Document #: 38–M–00046–B

CYPRESS SEMICONDUCTOR

CYM1840

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Independent byte and word controls**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .350 in.**
- **Small PCB footprint**
  - **1.8 sq. in.**

Functional Description

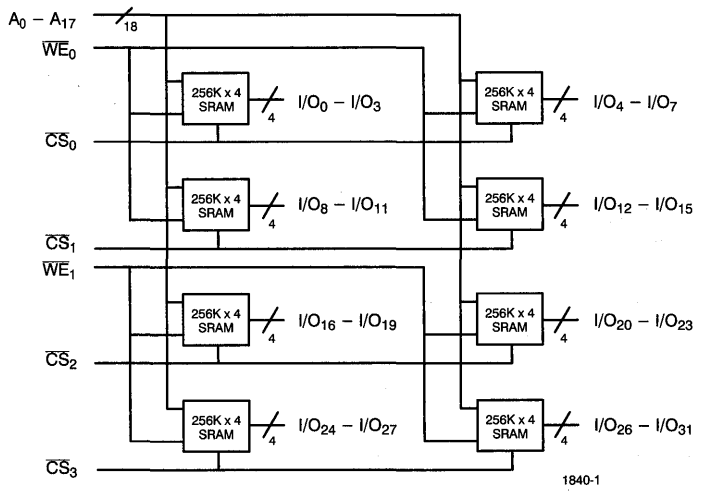
The CYM1840 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Four chip selects ($\overline{CS}_0$, $\overline{CS}_1$, $\overline{CS}_2$, and $\overline{CS}_3$) are used to independently enable the four bytes. Two write enables ($\overline{WE}_0$ and $\overline{WE}_1$) are used to independently write to either the upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through the proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins ($\overline{I/O}_X$) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}$) LOW, while write enables ($\overline{WE}$) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O}$).

The data input/output pins stay in the high-impedance state when write enables ($\overline{WE}$) are LOW or the appropriate chip selects are HIGH.

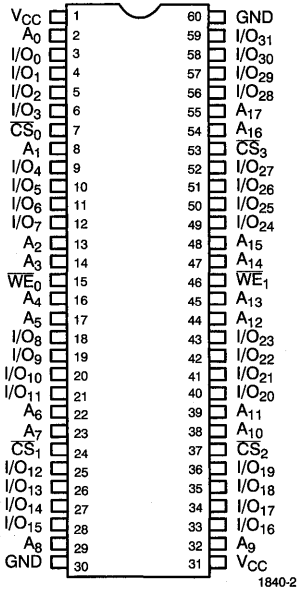
Logic Block Diagram



1840-1

Pin Configuration

DIP
Top View



1840-2

Selection Guide

	1840–20	1840–25	1840–30	1840–35	1840–45	1840–55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	1120	1120	1120	1120	1120
Maximum Standby Current (mA)	320	320	320	320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied (PD) ..... − 10°C to +85°C

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1840 Min.	CYM1840 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_X$ ≤ V_{IL}		1120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		160	mA

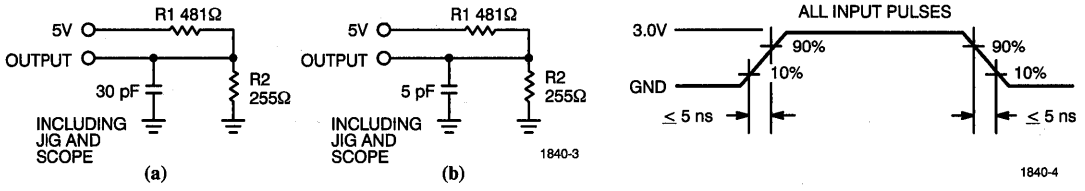
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	100	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

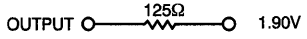
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1840–20		1840–25		1840–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Notes:

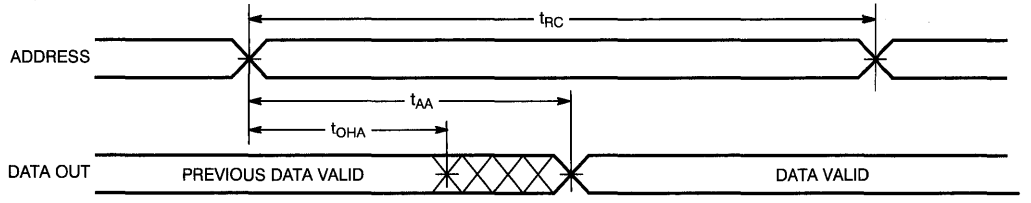
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3] (continued)

Parameter	Description	1840–35		1840–45		1840–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	6		6		6		ns
t_{SA}	Address Set-Up to Write Start	6		6		6		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		30		40		ns
t_{SD}	Data Set-Up to Write End	25		30		35		ns
t_{HD}	Data Hold from Write End	6		6		6		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	25	0	25	0	25	ns

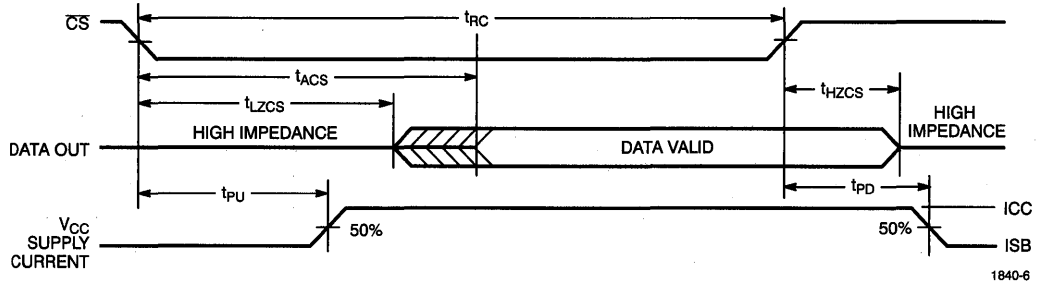
Switching Waveforms

Read Cycle No. 1[7, 8]

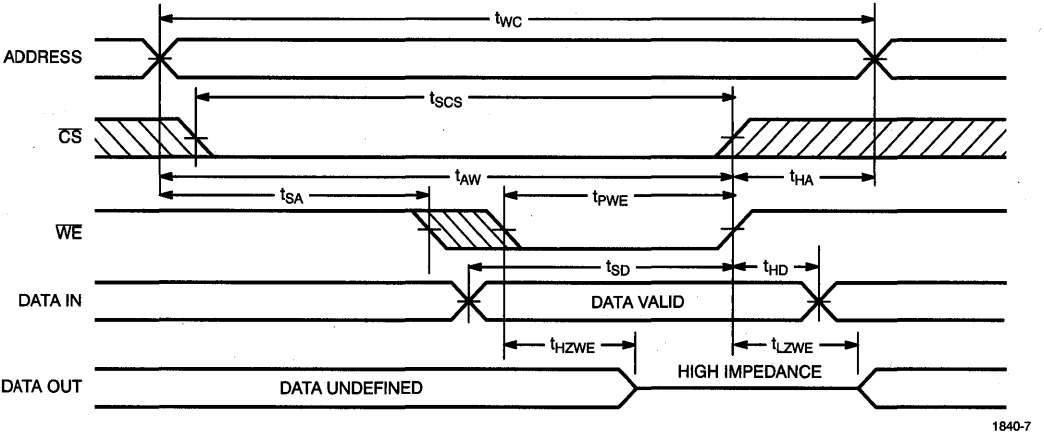


1840-5

Read Cycle No. 2[7, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]

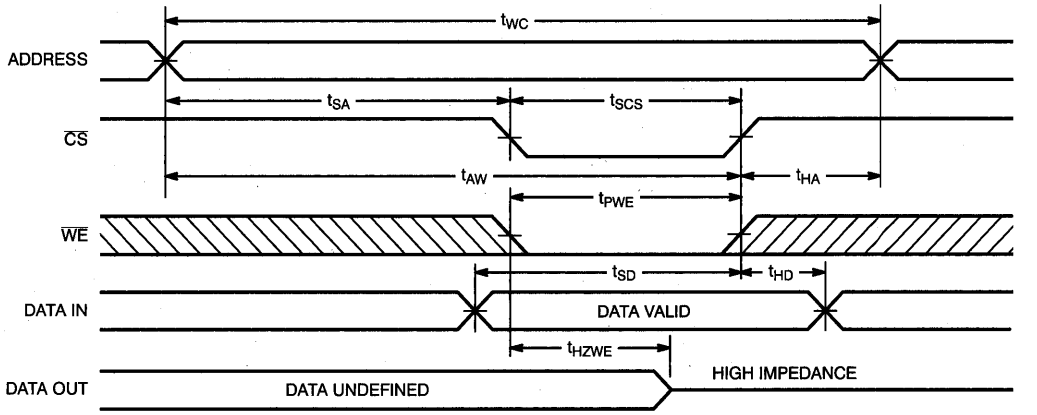


Notes:

7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1840PD–20C	PD06	60-Pin DIP Module	Commercial
25	CYM1840PD–25C	PD06	60-Pin DIP Module	Commercial
30	CYM1840PD–30C	PD06	60-Pin DIP Module	Commercial
35	CYM1840PD–35C	PD06	60-Pin DIP Module	Commercial
45	CYM1840PD–45C	PD06	60-Pin DIP Module	Commercial
55	CYM1840PD–55C	PD06	60-Pin DIP Module	Commercial

Document #: 38–M–00040–B

CYPRESS SEMICONDUCTOR

CYM1841

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.58 in.**
- **JEDEC-compatible pinout**
- **Available in ZIP, SIMM, and angled SIMM footprint**
- **72-pin SIMM version compatible with 1M x 32 (CYM1851)**

Functional Description

The CYM1841 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

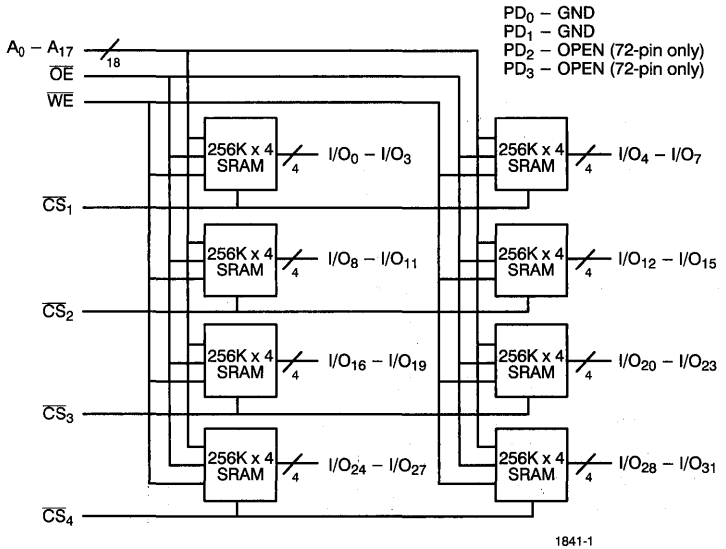
Reading the device is accomplished by taking the chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

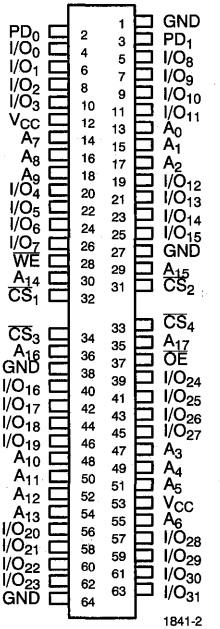
A 72-pin SIMM is offered for compatibility with future density generations. This version is socket upgradable to the CYM1851.

Logic Block Diagram



Pin Configurations

ZIP/SIMM
Top View

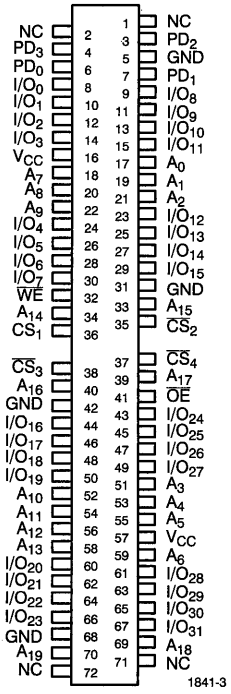


Selection Guide

	1841–20	1841–25	1841–30	1841–35	1841–45	1841–55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	960	960	960	960	960
Maximum Standby Current (mA)	480	480	480	480	480	480

Pin Configurations (continued)

SIMM
Top View



1841-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1841−20		1841−25, 30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 16	+16	− 16	+16	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		1120		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		480		480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		16		16	mA

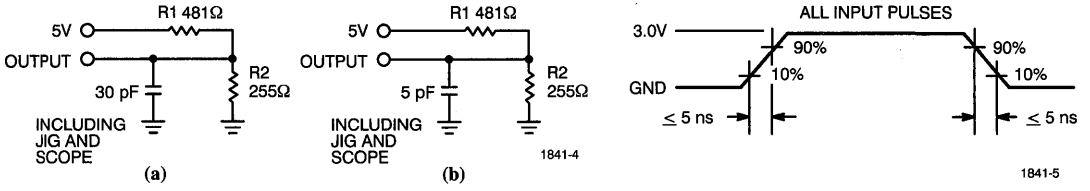
8 MODULES

Capacitance[2]

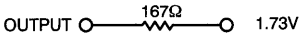
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1841–20		1841–25		1841–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Switching Characteristics Over the Operating Range (continued)[3]

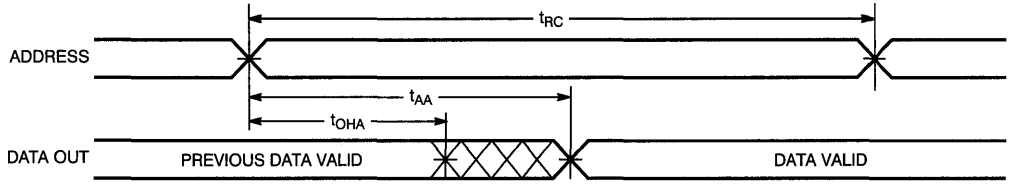
Parameter	Description	1841–35		1841–45		1841–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

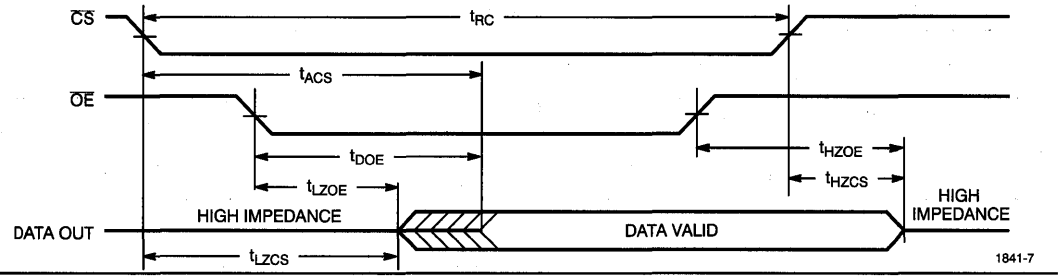
Read Cycle No. 1[7, 8]



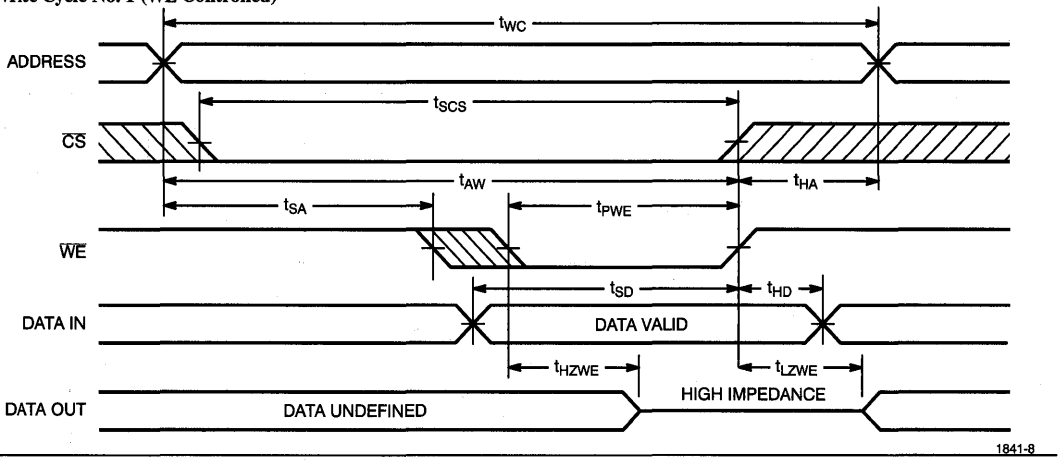
1841-6

Switching Waveforms (continued)

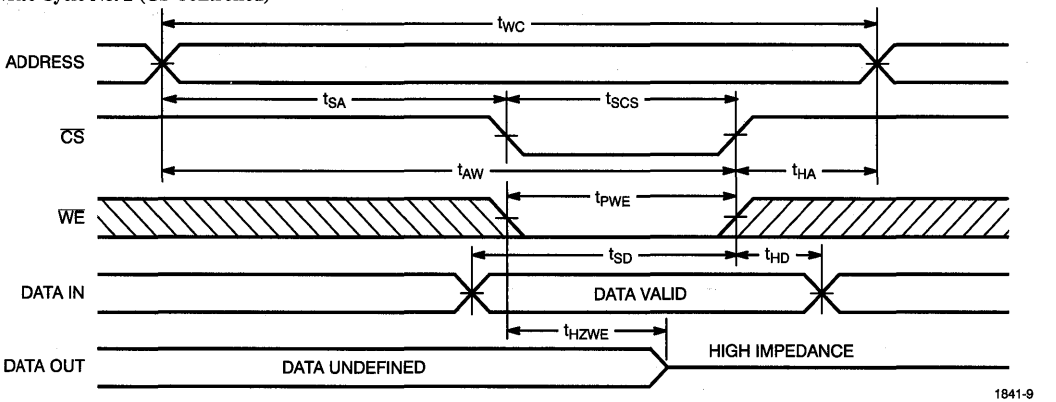
Read Cycle No. 2[7, 9]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Notes:

7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1841PM–20C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–20C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–20C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–20C	PZ03	64-Pin Plastic ZIP Module	
25	CYM1841PM–25C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–25C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–25C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–25C	PZ03	64-Pin Plastic ZIP Module	
30	CYM1841PM–30C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–30C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–30C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–30C	PZ03	64-Pin Plastic ZIP Module	
35	CYM1841PM–35C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–35C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–35C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–35C	PZ03	64-Pin Plastic ZIP Module	
45	CYM1841PM–45C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–45C	PZ03	64-Pin Plastic ZIP Module	
55	CYM1841PM–55C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–55C	PZ03	64-Pin Plastic ZIP Module	

Document #: 38–M–00031–C

PRELIMINARY **CYM1851**

CYPRESS SEMICONDUCTOR

1,024K x 32 Static RAM Module

Features

- **High-density 32-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **6.6W (max.) at 25 ns**
- **Downward compatible with CYM1821, CYM1831, CYM1836, and CYM1841 JEDEC modules**
- **72 pins**
- **Available in ZIP, SIMM, or angled SIMM format**

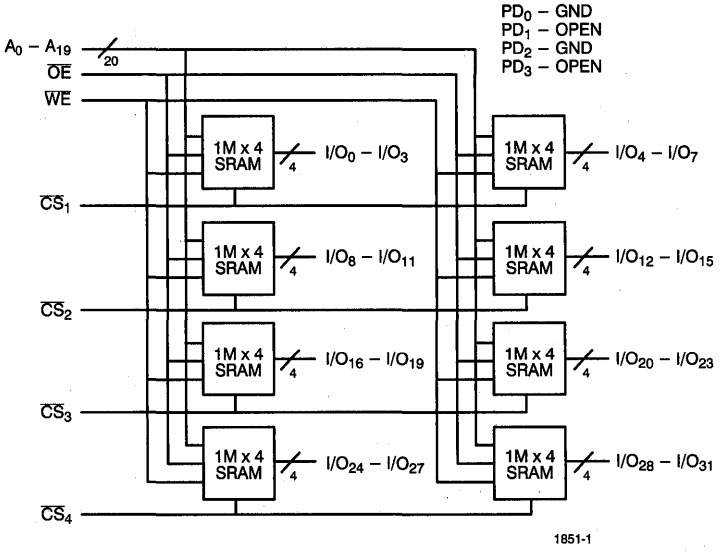
Functional Description

The CYM1851 is a high-performance 32-megabit static RAM module organized as 1,024K words by 32 bits. This module is constructed from eight 1,024K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1851 is designed for use with standard 72-pin SIMM sockets. The pinout is downward compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1,024K words (CYM1851).

Presence detect pins ($PD_0 - PD_3$) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

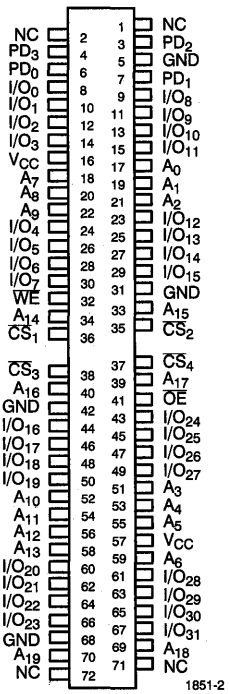
Logic Block Diagram



1851-1

Pin Configuration

ZIP/SIMM
Top View



1851-2

Selection Guide

	1851–25	1851–30	1851–35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	1200	1200	960
Maximum Standby Current (mA)	480	480	480

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +V_{CC}

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}		1200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		80	mA

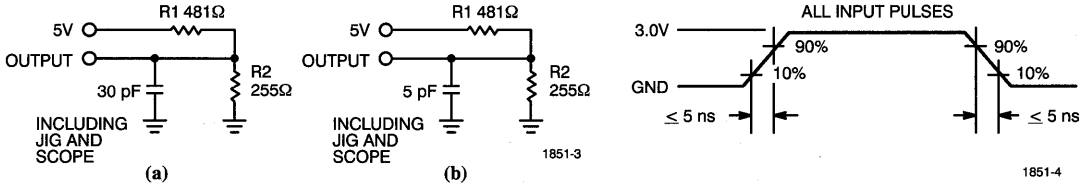
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance ($\overline{WE}$, $\overline{OE}$, A_{0-19})	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		20	pF
C_{OUT}	Output Capacitance		20	pF

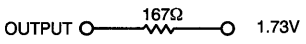
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



8 MODULES

Switching Characteristics Over the Operating Range[3]

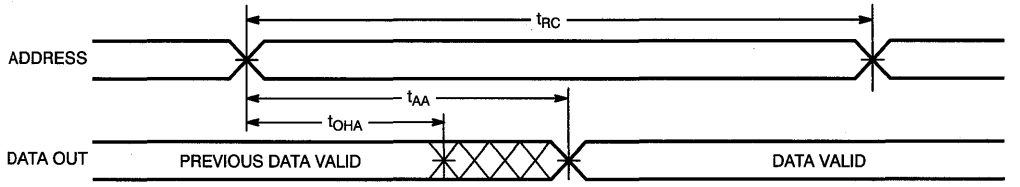
Parameter	Description	1851–25		1851–30		1851–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		12		12		12	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		12		12		12	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	12	0	12	0	12	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

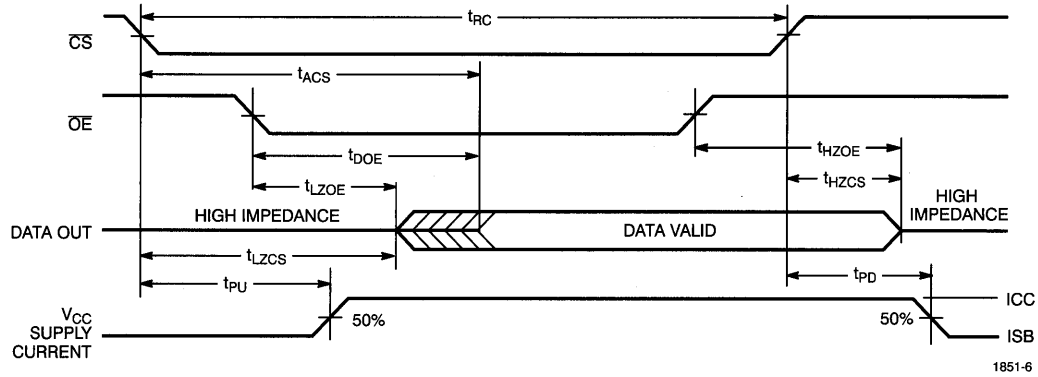
Read Cycle No. 1[7, 8]



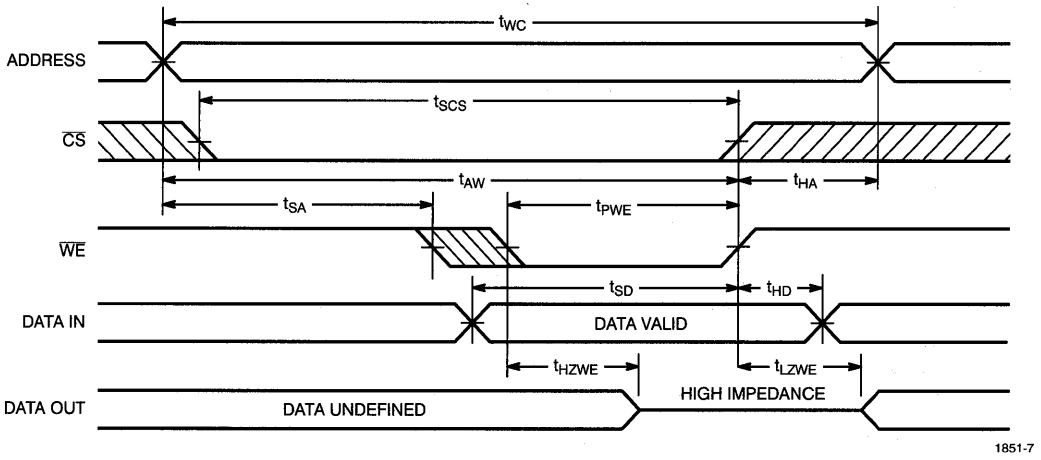
1851-5

Switching Waveforms (continued)

Read Cycle No. 2[7, 9]



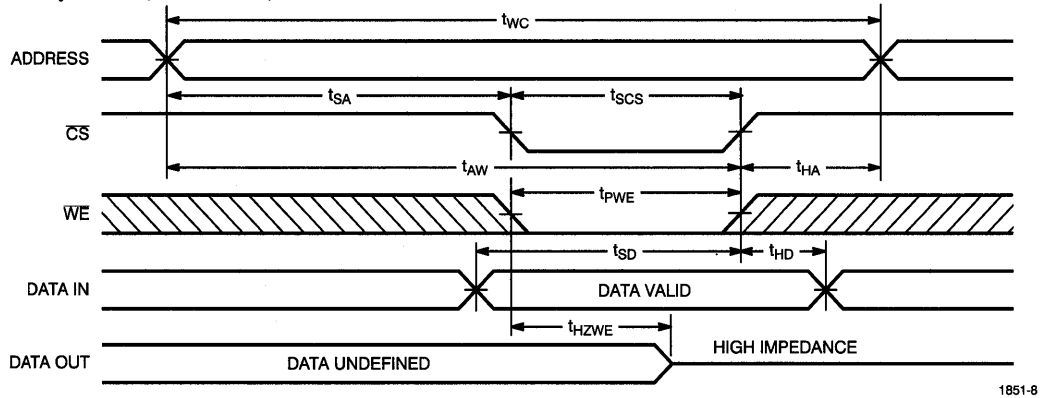
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}, and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
25	CYM1851PM–25C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–25C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–25C	PZ09	72-Pin Plastic ZIP Module	
30	CYM1851PM–30C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–30C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–30C	PZ09	72-Pin Plastic ZIP Module	
35	CYM1851PM–35C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–35C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–35C	PZ09	72-Pin Plastic ZIP Module	

Document #: 38–M–00052

CYM4208
CYM4209

CYPRESS SEMICONDUCTOR

Cascadable 64K x 9 FIFO
Cascadable 128K x 9 FIFO

Features

- **64K x 9 FIFO buffer memory (4208) or 128K x 9 FIFO buffer memory (4209)**
- **Asynchronous read/write**
- **High-speed, 28.5-MHz read/write**
- **Pin-compatible with standard, 28-pin monolithic FIFOs**
- **Low operating power**
  — **I_{CC} (max.) = 640 mA (commercial)**
- **600-mil DIP package**
- **Empty, Full flags**
- **Small PCB footprint**
  — **0.88 sq. in.**
- **Expandable in depth and width**

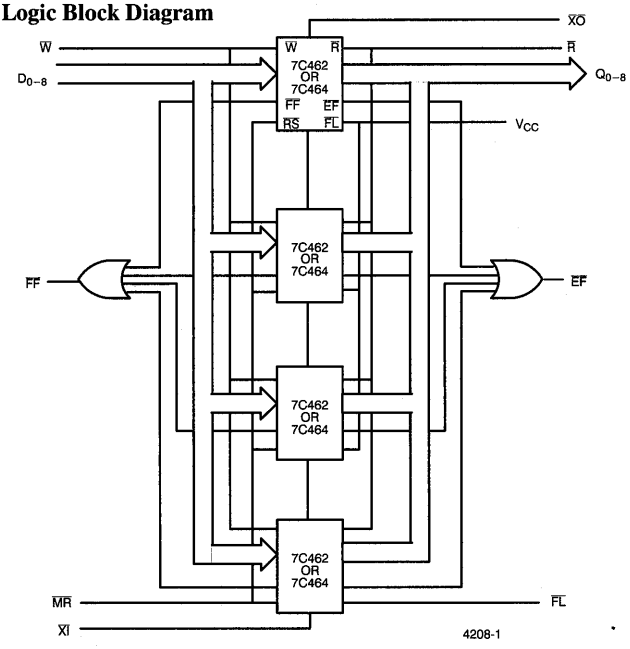
Functional Description

The CYM4208 is a first-in first-out (FIFO) memory module that is 64K words by 9 bits wide. The CYM4209 is 128K words by 9 bits wide. Each is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 28.5 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

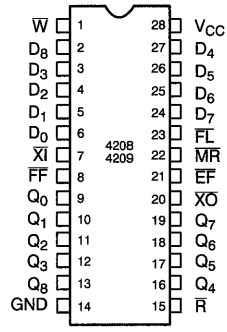
In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information that is used to tell the next FIFO that it will be activated.

Logic Block Diagram



Pin Configuration

DIP
Top View



4208-2

Selection Guide

		4208–25 4209–25	4208–30 4209–30	4208–40 4209–40
Frequency (MHz)		28.5	25	20
Access Time (ns)		25	30	40
Maximum Operating Current (mA)	Commercial	640	640	640
	Military		720	720

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		4208 4209 Min.	4208 4209 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}[2]	Input HIGH Voltage		Com'l	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 0.5	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, f_{MAX}, Outputs Open	Com'l		640	mA
			Mil/Ind		720	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min., V_{CC} = Max., f_{MAX}, I_{OUT} = 0 mA	Com'l		100	mA
			Mil/Ind		120	
I_{SB2}	Power-Down Current	All Inputs, V_{CC} – 0.2 ≤ V_{IN} ≤ 0.2, V_{CC} = Max., I_{OUT} = 0, f = 0	Com'l		80	mA
			Mil/Ind		100	

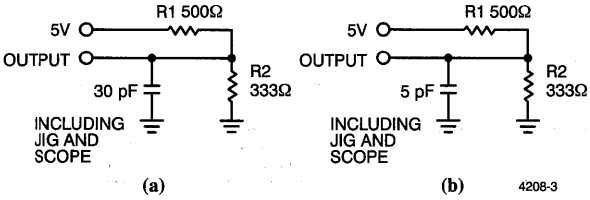
Capacitance

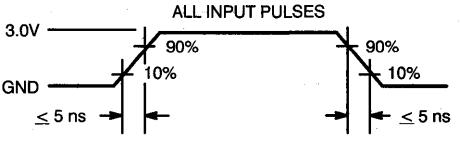
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	30	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

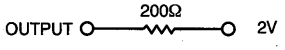
1. T_A is the "instant on" case temperature.
2. $\overline{XI}$ must use CMOS levels with V_{IH} ≥ 3.5V (CYM4209 only).

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 4, 5]

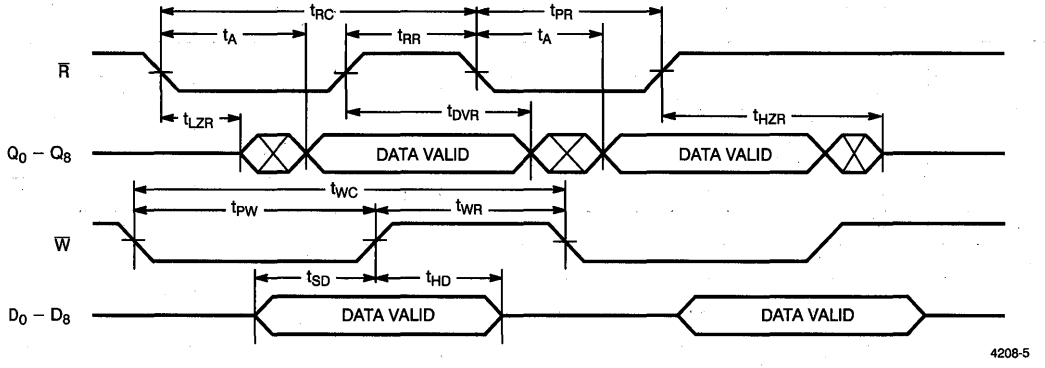
Parameters	Description	Spec.–25		Spec.–30		Spec.–40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		ns
t_A	Access Time		25		30		40	ns
t_{RR}	Read Recovery Time	10		10		10		ns
t_{PR}	Read Pulse Width	25		30		40		ns
t_{LZR}	Read LOW to Low Z	3		3		3		ns
t_{DVR}	Read HIGH to Data Valid	3		3		3		ns
t_{HZR}	Read HIGH to High Z		18		20		25	ns
t_{WC}	Write Cycle Time	35		40		50		ns
t_{PW}	Write Pulse Width	25		30		40		ns
t_{HWZ}	Write HIGH to Low Z	10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		ns
t_{SD}	Data Set-Up Time	18		18		20		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	25		30		40		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	25		30		40		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		35		40		50	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		35		40		50	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		30		40	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		30		40	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		30		40	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		30		40	ns
t_{RAE}	Effective Read from Write HIGH		25		30		40	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	25		30		40		ns
t_{WAF}	Effective Write from Read HIGH		25		30		40	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	25		30		40		ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		30		40	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		25		30		40	ns

Notes:

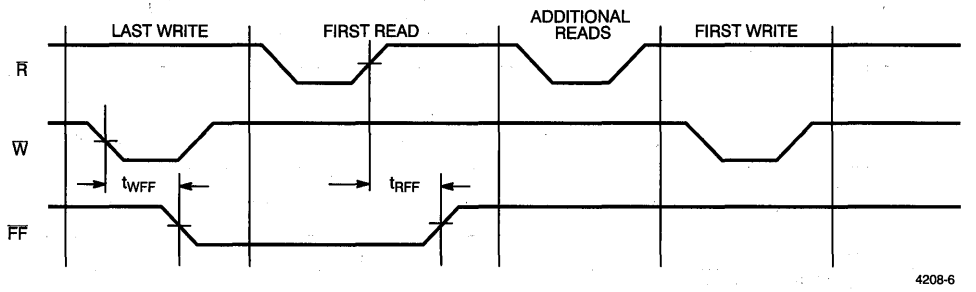
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads and Waveforms, unless otherwise specified.
4. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
5. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads and Waveforms.

Switching Waveforms

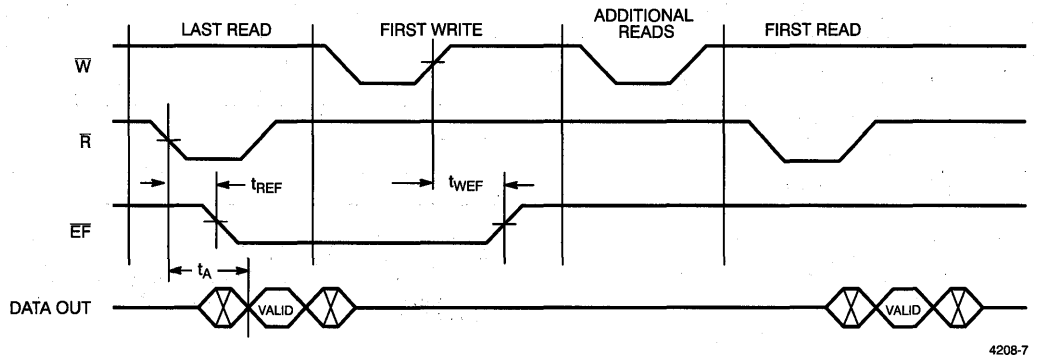
Asynchronous Read and Write Timing Diagram



Last Write to First Read Full Flag Timing Diagram

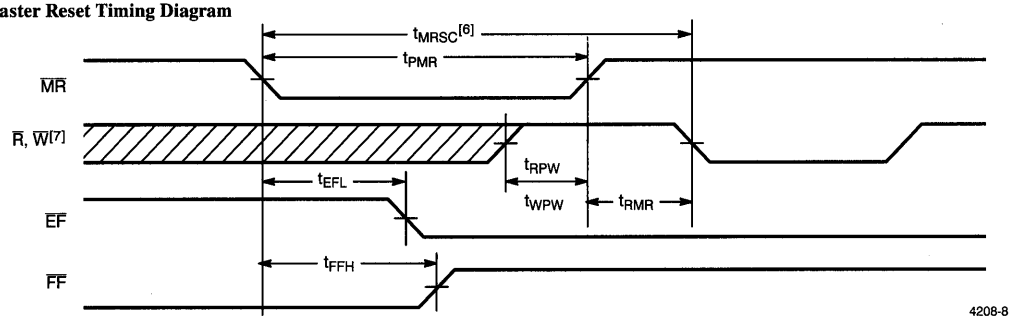


Last Read to First Write Empty Flag Timing Diagram

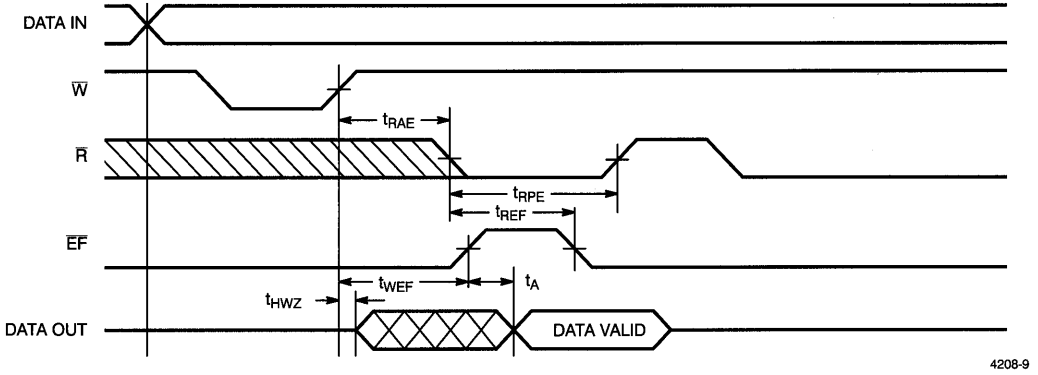


Switching Waveforms (continued)

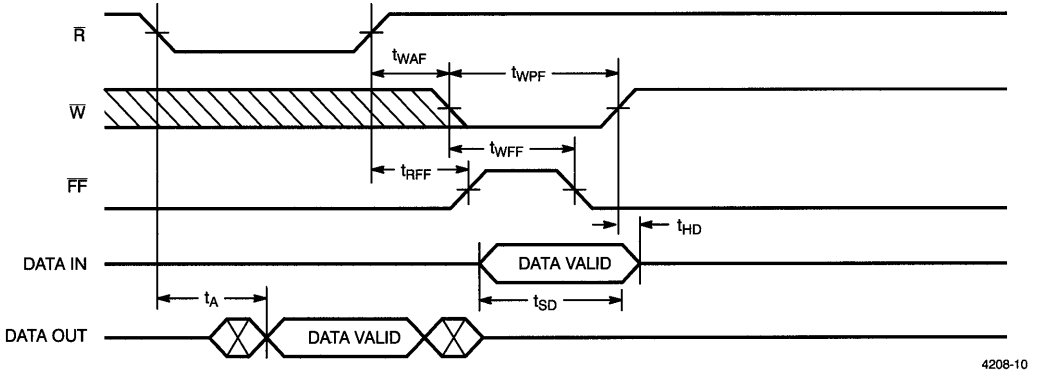
Master Reset Timing Diagram



Empty Flag and Read Bubble-Through Mode Timing Diagram



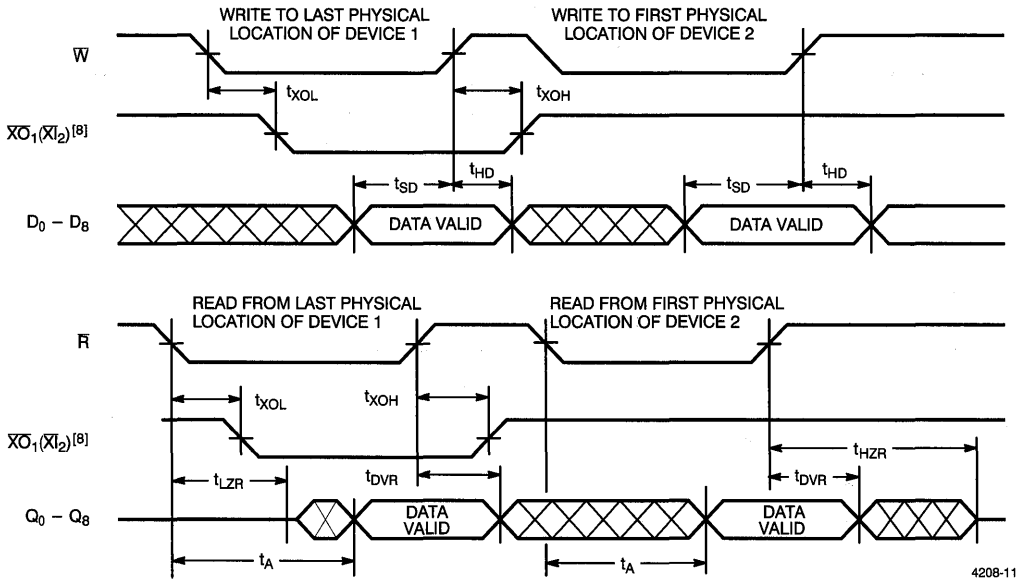
Full Flag and Write Bubble-Through Mode Timing Diagram



Notes:
6. $t_{MRSC} = t_{PMR} + t_{RMR}$.
7. $\overline{W}$ and $\overline{R} \geq V_{IH}$ for at least t_{WPW} or t_{RPR} before the rising edge of $\overline{MR}$.

Switching Waveforms (continued)

Expansion Timing Diagram



Note:
8. Expansion Out of Device 1 ($\overline{XO_1}$) is connected to Expansion In of Device 2 ($\overline{XI_2}$).

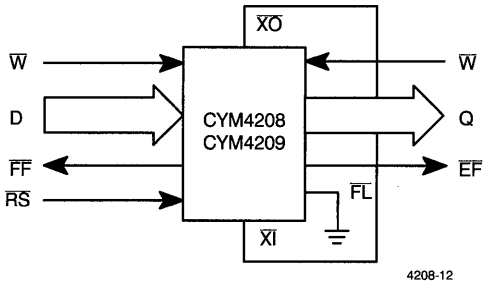


Figure 1. Single Device Mode

Architecture

The CYM4208 FIFO module is an array of 64K words of 9 bits each and is implemented using four 16K x 9 monolithic FIFOs. The CYM4209 is an array of 128K words of 9 bits each and is implemented using four 32K x 9 monolithic FIFOs. Each version has Full and Empty flags, but since the FIFOs are internally cascaded using the depth mode, the half full and retransmit features are not available.

Pinouts of the CYM4208 and CYM4209 are compatible with industry standard 28-pin DIP. The functionality is compatible with monolithic FIFO devices and with other FIFO modules.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW and the Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ($\overline{FF}$). A falling edge of write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs ($D_0 - D_8$) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition on the write clock of an empty FIFO. The Full flag ($\overline{FF}$) goes LOW on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs ($Q_0 - Q_8$) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the depth expansion mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH-to-LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Single Device Mode

Single device mode is entered by connecting $\overline{FL}$ to ground and connecting $\overline{XO}$ to $\overline{XI}$ (see *Figure 1*).

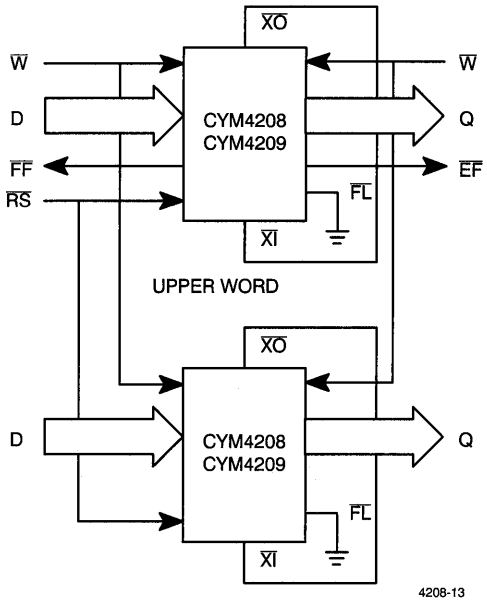


Figure 2. Width Expansion Mode

Width Expansion Mode

FIFOs can be expanded in width to provide word widths greater than 9 bits in increments of 9 bits. Devices are connected similar to the single device mode but with control line inputs in common to all devices. Flag outputs from any device can be monitored (see *Figure 2*).

Depth Expansion Mode

Depth expansion mode (see *Figure 3*) is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the first load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9 bits. When expanding in depth, a composite $\overline{FF}$ and $\overline{EF}$ must be created by ORing the $\overline{FF}$s together and the $\overline{EF}$s together.

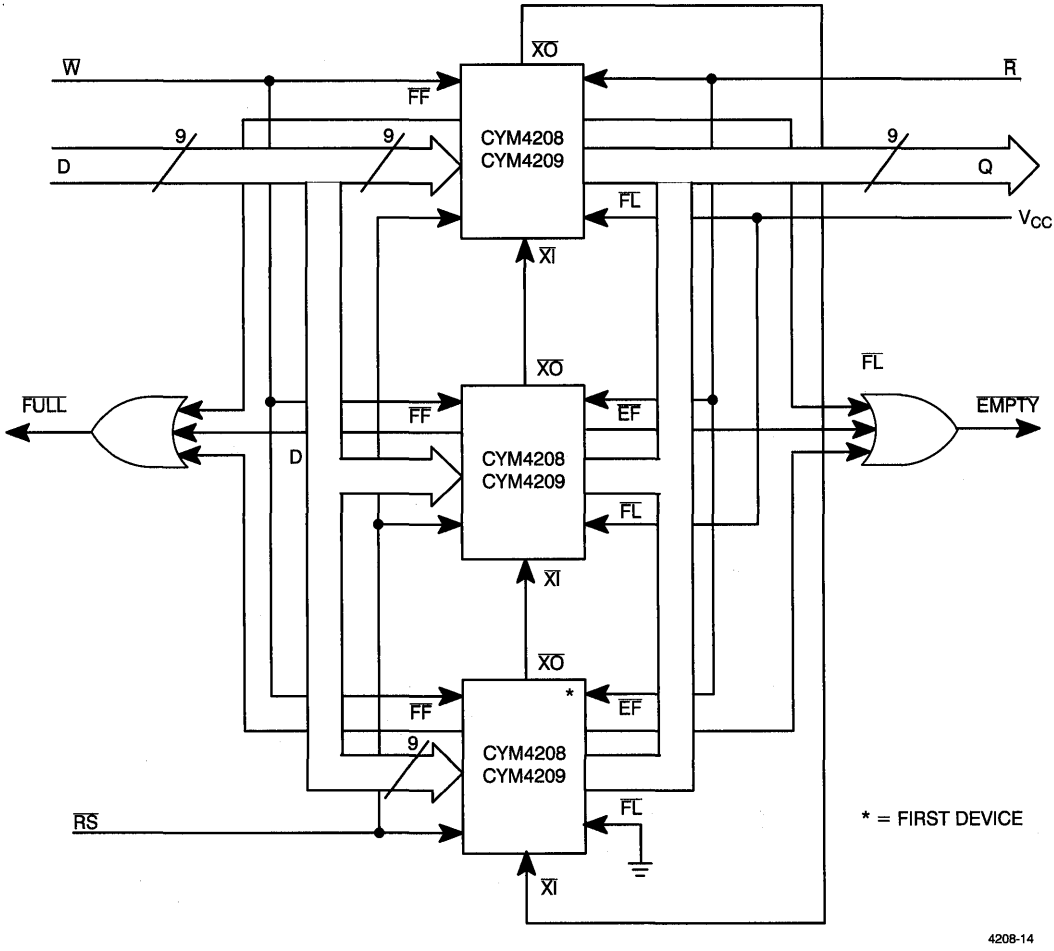


Figure 3. Depth Expansion Mode

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM4208HD–25C	HD10	28-Pin Ceramic DIP Module	Commercial
30	CYM4208HD–30C	HD10	28-Pin Ceramic DIP Module	Commercial
	CYM4208HD–30MB	HD10	28-Pin Ceramic DIP Module	Military
40	CYM4208HD–40C	HD10	28-Pin Ceramic DIP Module	Commercial
	CYM4208HD–40MB	HD10	28-Pin Ceramic DIP Module	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM4209HD–25C	HD10	28-Pin Ceramic DIP Module	Commercial
30	CYM4209HD–30C	HD10	28-Pin Ceramic DIP Module	Commercial
	CYM4209HD–30MB	HD10	28-Pin Ceramic DIP Module	Military
40	CYM4209HD–40C	HD10	28-Pin Ceramic DIP Module	Commercial
	CYM4209HD–40MB	HD10	28-Pin Ceramic DIP Module	Military

Document #: 38–M–00053

CYPRESS SEMICONDUCTOR

PRELIMINARY

CYM7232
CYM7264

DRAM Accelerator Module

Features

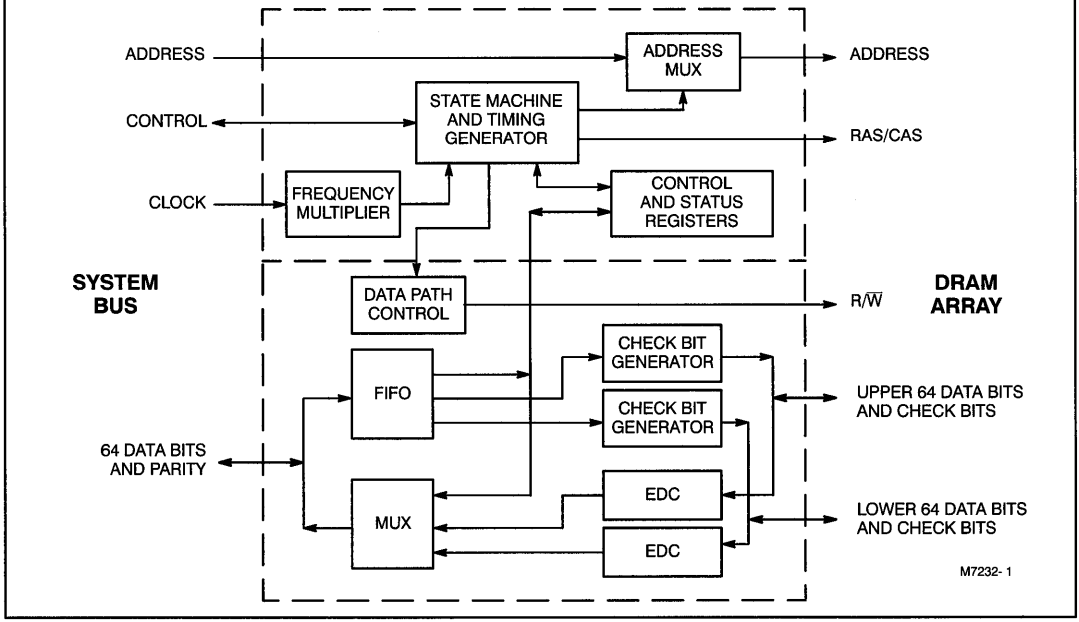
- **4-megabyte to 1-gigabyte control capability**
- **32- or 64-bit bus interface (M7232 only)**
- **32- or 64-bit EDC versions**
  - **— 1-bit correct; 2-bit detect**
- **Multiplexed or non-multiplexed bus**
- **i486, Pentium™, i860, 68040, 88110, Power PC, SPARC, and MIPS compatible**
- **Synchronous bus interface**
- **25-, 33-, and 40-MHz versions**
- **Error-logging facilities**
- **Cache line fill burst support; posted writes**
- **Cache line write-back support; write FIFO**
- **High performance**
  - **— 25-ns writes**
  - **— 175-, 25-, 50-, 25-ns burst read/80-ns DRAMs**
- **Automatic refresh with scrubbing**
- **Multiprocessor compatible**
  - **— Inhibited reads and writes**
  - **— Reflective reads**
  - **— Reads for ownership**
- **Bus parity generation and checking**
- **Very small size**

Functional Description

The CYM7232 and the CYM7264 consist of a full-function DRAM controller and a pipelined/FIFO data multiplexer/demultiplexer with error correction for cache-based, uniprocessor, and multiprocessor systems memory control. The CYM7232 performs 32-bit Error Detection and Correction (EDC) while CYM7264 performs 64-bit EDC. They both connect to the system bus through a 64-bit-wide data bus, and a 36-bit wide address bus. The CYM7232 also supports 32-bit system buses. The bus transfer control signals support i486, Pentium, i860, 68040, 88110, SPARC MBus, MIPS R4000, or other interfaces. The controller module interfaces to the DRAM array through a 16-byte-wide data bus plus check bits, a 12-bit row/column address bus, four $\overline{RAS}$ outputs, four $\overline{CAS}$ outputs, and four read/write control lines.

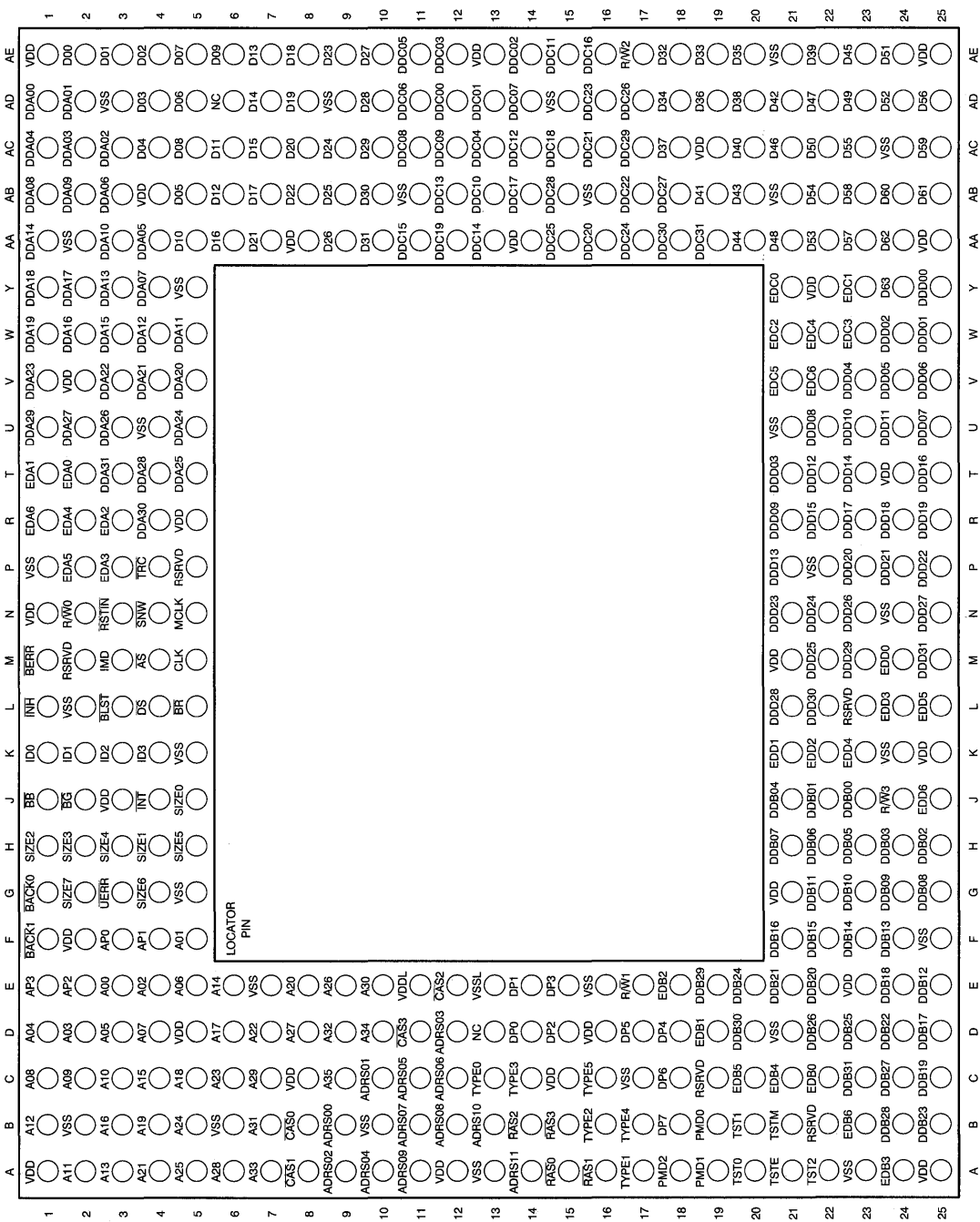
During write operations, data passes from the system bus through a FIFO array that acts as an incoming queue. Writes occur at the system bus speed until the FIFO is full (sixteen 64-bit words). The FIFO supports cache-line copy-back and fill operations, reducing system bus traffic to a minimum. The module supports posted writes, by suspending the actual write to DRAM until the cache-line read is completed during cache-line write-back. This speeds cache-line fill operations. The module pipelines a 16-byte-wide DRAM access into the data path for EDC, and multiplexes the data to the system bus during reads. This supports high-speed burst line fills with error corrected data. Reads and writes may be inhibited for multiprocessor support. Inhibited reads may be turned into reflective reads, and inhibited writes may be turned into reads-for-ownership.

Logic Block Diagram

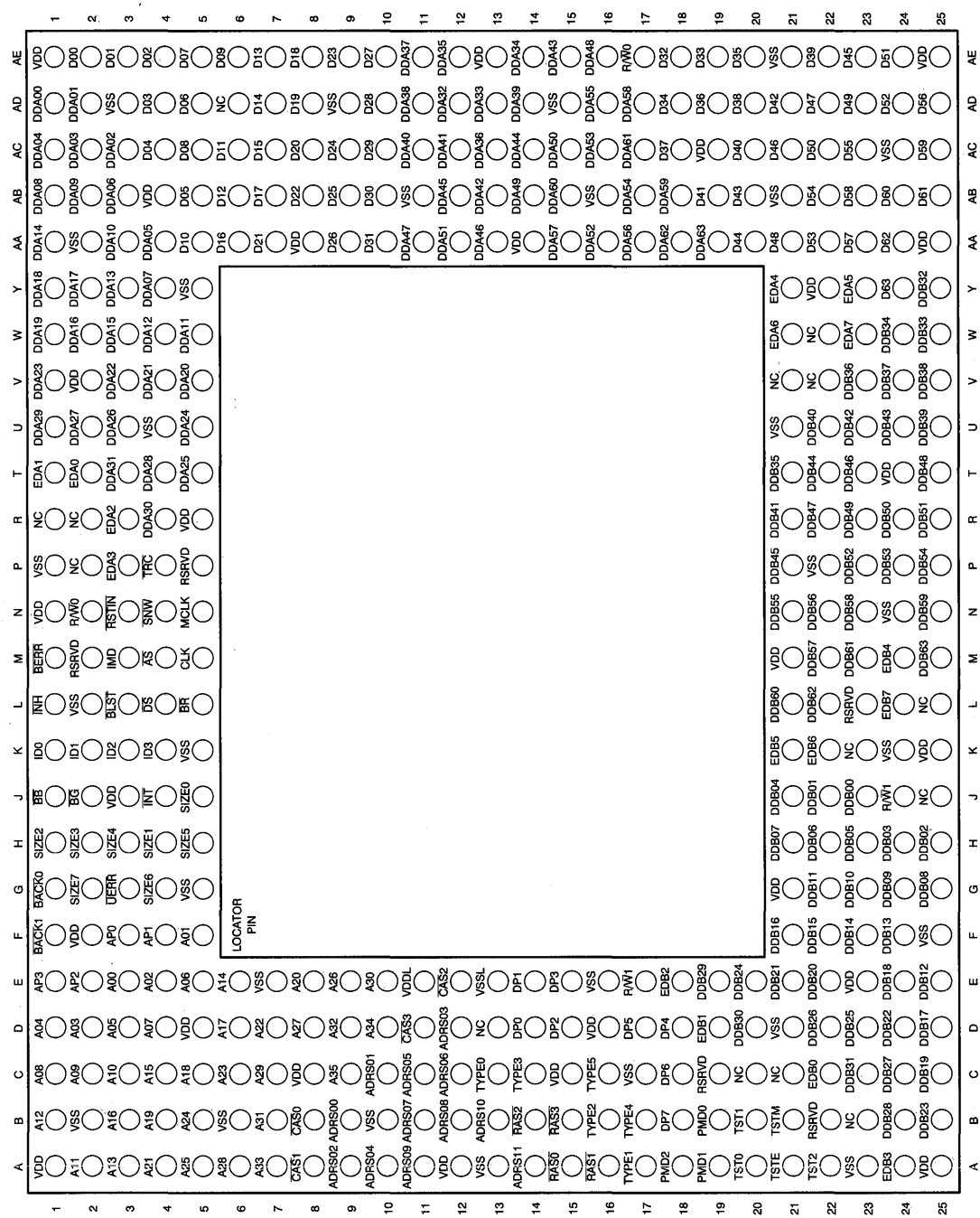


Pentium is a trademark of Intel Corporation.

Pin Configuration: CYM7232 Top View



Pin Configuration: CYM7264 Top View



Overview

Cypress Semiconductor offers two DRAM control subsystem module types: the CYM7232, which supports 32-bit EDC, and the CYM7264, which supports 64-bit EDC. The modules are very similar in functionality and architecture, with minor differences to support the EDC variation. Both modules support four blocks of DRAMs for a total capacity of 1 gigabyte of data storage. The CYM7232 divides the memory blocks into four 32-bit-wide data banks, each with 7 check bits, which provide a 156-bit-wide data path to the DRAM array. The CYM7264 divides the memory blocks into two banks of 64-bit-wide data, each with 8 check bits, for a total DRAM interface of 144 bits.

The CYM7232 can be programmed and wired for use with 32-bit system buses, and the operation is very similar to use in 64-bit systems.

The modules support multiplexed address/data buses as well as separate address and data buses for applications such as the SPARC MBus architecture. This datasheet includes a detailed MBus Operation section.

The modules are offered in high-speed and standard speed versions. The high-speed version may be programmed for 100 MHz DRAM timing resolution, while the standard speed version may be programmed for 80-MHz DRAM timing resolution.

System Bus Modes

The modules include selectable bus modes that support a variety of processors and cache controllers. Programmability includes the byte-ordering protocol (big endian/little endian); burst length is configurable for SPARC MBus, 88K or 68040 SIZE, or i86 and i860 byte enables. A data strobe initiates the bus handshake for systems where the bus master must indicate when it can supply or accept data; bus acknowledge signals are programmable to be early (active in the bus cycle preceding the data) or normal (active in the cycle in which the data transfer takes place). The early modes support the Motorola 88K family of microprocessors. Other programmable options allow optimization of the acknowledge timing to the system requirements.

General Description of Bus Transactions

The fully synchronous bus interface uses the rising edge of the system bus clock. Every system transaction has an address/control phase and one or more data phases.

Address Phase

During the address/control phase, which is specified by the assertion of the Address Strobe for one bus clock cycle, the address and nature (size and type) of the transaction is supplied over the system bus to the module.

Data Phase

During the data phase, which is specified by the assertion of the data strobe for one or more bus clock cycles, one or more data words is transferred over the system bus.

Data Write

The module supports four different write modes. Data strobe will be interpreted differently depending on the mode. Data strobe may be permanently asserted, asserted one clock early, or in real-time. Systems using Real-Time Data Strobe mode must monitor the Bus Request/FIFO Empty output and postpone data strobe assertion until the write FIFOs are empty. These systems do not require bus acknowledges since the FIFOs are empty when the data phase begins. The module will not respond with bus acknowledge (real-time data strobe case) or will assert bus acknowledge one cycle before, or during the same cycle, as the data transfer.

Write Data Flow

During system bus writes and reflective read operations, two identical sets of FIFOs buffer the incoming data. One set is used during normal write transactions, and the second set is used exclusively during reflective read transactions. In the CYM7232, each set contains four FIFOs that are 32 bits wide by 8 words deep. In the CYM7264, each set contains two FIFOs that are 64 bits wide by 8 words deep. During writes, the module demultiplexes the incoming data into the appropriate FIFO according to the address and burst order. As soon as the required data falls through the FIFOs, a write to DRAM commences. This process continues until completion of the burst. When the inhibit signal and transform cycle inputs are asserted during a read, the module demultiplexes the write data into the appropriate reflective FIFO. These FIFOs operate in an identical fashion to the normal write FIFOs.

During writes to DRAM, the module appends the demultiplexed data with associated error detection and correction check bits. For the 32-bit EDC version, the demultiplexed data word consists of four sets of 32 data bits plus their 7 associated error check bits for a total of 156 bits. For the 64-bit EDC version, the data word consists of two sets of 64 data bits plus their 8 associated error check bits for a total of 144 bits.

Data Phase Read

During read operations the module suspends data transfer until two clocks after the assertion of data strobe and the closing of the snoop window, whichever occurs last. The data transfer continues at the system bus speed. In systems where the master does not regulate the data flow, data strobe may be permanently asserted.

The module offers options for both early and real-time bus acknowledge for reads. At fast system bus clocks, wait states may be inserted to delay the bus acknowledge, allowing the data to propagate through the error-detection and correction logic.

Read Data Flow

The module reads 128 bits of data and the corresponding EDC check bits in parallel from the DRAM. The data then passes simultaneously through parallel error correction circuitry to a multiplexer that selects the corrected or uncorrected data. The module appends parity to the data and routes it to the system bus. The CYM7232 transfers the data in 32-bit packets, and the CYM7264 transfers 64-bit packets, which makes the CYM7264 incompatible with 32-bit system buses.

Burst Last

The module allows any read or write burst transaction to terminate prematurely with the assertion of Burst last.

Data Alignment

The data path portion of the module contains data buffers and demultiplexers on writes and multiplexers and error correctors on reads. The bus interface is 64 data bits wide and the DRAM interface is 128 data bits wide.

Bus Alignment

All data flowing between the DRAM controller and the system data bus is assumed to be aligned to the bus width. When a system bus transaction crosses aligned boundaries, the processor or cache controller must split the transaction into multiple operations and issue an address phase for each portion. The misaligned transactions cannot, therefore, be bursts.

DRAM Alignment

The DRAM controller stores data into memory on 128-bit aligned boundaries. Transactions over the system bus of 16 bytes or less are assumed to be aligned within a 128-bit DRAM page. This implies that a single DRAM transaction will be associated with bus transactions of 16 bytes or less. Burst transactions exceeding 16 bytes may be misaligned to the DRAM storage boundary. Such transactions will involve transfers of 4, 8, or 12 bytes between controller and DRAM during the first cycle of the burst (i.e., not all DRAM banks will be involved in the first data transfer). The DRAM address will wrap around within the burst boundary as more data is transferred. The final data transfer will include the bank(s) omitted during the first cycle of the DRAM transfer. The nature of the misalignment will depend on the defined burst order (i.e., sequential or Intel).

I/O Operations

The internal command and status registers are accessed through I/O transactions. The ID inputs select between Memory, I/O transactions, or the Indirect Address register. The Indirect Address register points to the desired command and status I/O registers. I/O read and write transactions follow the same bus acknowledge and data strobe protocols as memory operations.

I/O operations may be inhibited prior to the closure of the snoop window.

Multiprocessor Support

The modules provide complete multiprocessing support. Any operation may be inhibited or aborted, including I/O operations.

Reflective Read Operations

A reflective read transaction occurs when a main memory read operation is inhibited and transformed into a write. Such transactions can occur in a multiprocessor environment when a processor's cache controller requests a line from main memory. The particular main memory line may be stale with the only valid copy contained in another processor's snooping cache. The cache line owner will inhibit the main memory, and then fetch and supply the data to the requesting processor's cache. Simultaneously, the data is copied into FIFO buffers inside the controller module for later transfer to DRAM. The memory read operation is thereby transformed into a memory write operation.

Reads For Ownership

The address space of a copy-back cache-based system will typically be partitioned into distinct regions. Some of these regions will be cachable and others (typically peripheral I/O registers and some small portion of memory) will not be cachable. Whenever a processor begins a write operation to a particular address location, the cachability status of that location must be determined. Should the write operation result in a miss within a cachable region of main memory, a line would be fetched. The DRAM controller module permits a write to begin into DRAM before the cachability status is completely determined. When the status of the address in question is resolved the operation can be inhibited and transformed into a read of a cache line.

Write Operations

Address Phase

A write operation is initiated when Address Strobe ($\overline{AS}$) is asserted and an address and all appropriate control signals meet the set-up conditions to the rising edge of CLK. This is the address phase of the transaction. The control signals that accompany the address during the address phase include SIZE and TYPE inputs. The address and certain control information is strobed into the Address-Control register in the cycle in which $\overline{AS}$ is asserted. If address parity check is enabled, the lowest 32 bits of the system bus address is checked for byte parity. The control signals are not parity checked. If parity is error-free, the address and other control information is used to initiate the requested transaction. If address parity is enabled and an address bus parity error is detected, the Address Bus Parity Error (ABE) bit is set in the status register, the Bus Error ($\overline{BERR}$) output is asserted, and the write operation is aborted. This action takes place whether or not the address is decoded to address the DRAM controller.

Data Phase

Data placed on the bus is clocked into the Write Data FIFO on a rising CLK edge. The system will use $\overline{DS}$ (Data Strobe) to signal the onset of a write transaction. Once $\overline{DS}$ is asserted, it must remain asserted throughout the bus operation. The system must continue to assert the write data until it is acknowledged (except in the no acknowledge mode). If the SIZE[7:0] control indicated a non-burst transfer, the write transaction is terminated upon the acceptance of the data. When SIZE[7:0] control inputs indicate a burst transaction, the module will continue the write transaction by accepting data until the transaction is terminated. The transaction is terminated by one or more of the following events: the bus responds by asserting Burst Last ($\overline{BLST}$) or the burst length indicated by SIZE or the programmed default burst length is reached.

During the data phase, data is checked for valid parity (if data parity checking is enabled). Parity is checked over individual bytes. Should a data bus parity error occur, data is clocked into the Write Data FIFO (but is later discarded) and the Bus Error output ($\overline{BERR}$) is asserted. After parity check, data flows into the Write Data FIFO and is subsequently written into the DRAM memory. When a parity error occurs, the entire word that would have been written to DRAM with the byte(s) incurring the parity error is discarded. The discarded word consists of bits over which the EDC algorithm is applied. It is therefore 32 (CYM7232) or 64 (CYM7264) bits in length. Recovery schemes must consequently rewrite more than the byte(s) incurring the parity error. Subsequent data transferred to the FIFO is written to DRAM even though a previous data word may have incurred a parity error.

Burst operations are supported up to the full FIFO depth. The FIFO permits these operations to take place at the full bus speed. If the Write Data FIFO contains data from a previous write (FIFO not Empty), the address and control information is accepted into the controller's internal Write Address register, but the data phase cannot begin until the previous write is completed to DRAM. $\overline{BACK}$ remains three-state until the FIFO is available for the new write. The system must use the Bus Request/FIFO Empty ($\overline{BR/FE}$) output to determine if the controller is capable of accepting data when using the No Bus Acknowledge Mode.

Posted Writes

Posted writes support fast cache line fills. A posted write is accomplished by issuing the Posted Write encoding in the TYPE input during the address phase. The module accepts the write data as usual and holds the data in the Write Data FIFO. After the next read transaction is completed, the actual write of the data to DRAM is accomplished. The posted write operation allows a cache controller to purge a cache line and fetch the new cache line as rapidly as possible by postponing the DRAM access for the write. Posted writes must be followed by a read operation.

When the address of the posted write is in the same burst address region as that of the following read, a memory incoherency can result. To resolve the incoherency, the module compares the

Posted Writes (continued)

address of the posted write with that of the read for address bits A7 and higher. (A[6:0] span the longest possible burst). If the compare shows equal, the posted write is performed before the read. Posted writes may not be inhibited.

Byte Writes

Single byte and partial word transfers are supported by a read-modify-write DRAM memory cycle. The old word is accessed and combined with the new data under control of the address and SIZE inputs. A new set of EDC check bits is generated and the modified data and new check bits are written back to the memory to complete the read-modify-write cycle. In the 32-bit EDC version, a read-modify-write cycle occurs for all writes less than 32 bits. In the 64-bit EDC version, a read-modify-write cycle occurs for all writes less than 64 bits.

Inhibited Write Operations

A write operation may be inhibited at any time prior to the end of the snoop window by asserting Inhibit, $\overline{\text{INH}}$. When Inhibit is recognized, the module write operation is aborted and the module plays no further role in the bus transaction. Note that the system may perform data writes to the controller prior to the close of the snoop window and prior to the assertion of Inhibit. In these cases, the data will not be written to the DRAM and the write FIFO will be cleared upon recognition of the Inhibit. When data transfers occur prior to a write inhibit there must be at least two bus clock cycles between the close of the snoop window and the address strobe of the following transaction.

An inhibited write may also be converted into a read for ownership. This option is enabled by asserting the $\overline{\text{TRC}}$ input (Transform Cycle) along with the Inhibit. When Inhibit is recognized, the module write operation is transformed into a read operation. After Inhibit is recognized and before the read is completed, any data written to the Write FIFO is purged.

Write Snoop Window

The snoop window is determined by an internal counter that is programmable by the system or by an external input, $\overline{\text{SNW}}$. The snoop window source is selectable by driving $\overline{\text{UERR}}$ as an input when $\overline{\text{RSTIN}}$ is asserted. Refer to the signal descriptions for programming details. The write into the DRAM is postponed until the snoop window closes. This prevents data from an inhibited write operation from corrupting main memory data. Long snoop window intervals may cause performance degradation.

Read Operations

Address Phase

A read operation begins with the address phase similar to write operations.

Data Phase

The DRAM interface accesses 128 data bits from the memory simultaneously with their related check bits. The addressed 64-bit word (or the first word of the burst) is pipelined to the system bus and simultaneously to the error check logic. The data is accessed from DRAM but the transfer over the system bus is suspended until two clock cycles after the snoop window closes or two clock cycles after Data Strobe is asserted, whichever occurs last. The appropriate Bus Acknowledge is asserted as dictated by the selected modes. Byte-wide parity is appended to the data as it exits the module onto the system bus.

During bursts, data is pipelined consecutively over the bus until the transaction is terminated. Transactions may be terminated by Burst Last ($\overline{\text{BLST}}$) or when the burst length indicated by SIZE or the default burst length is reached.

The error detection logic generates check bits that are compared with the check bits from the memory. The exclusive NOR of the generated check bits and the check bits from the memory form the syndrome bits. When the two sets of check bits are identical, no errors have occurred in the data. Should the comparison show a difference, the Error Detector decodes the syndrome bits, identifying the type of error (single-bit correctable, double-bit detectable, or uncorrectable multi-bit error). The Error Position Decoder creates a 32-bit word that is used to correct the defective bit for single-bit errors.

Should the data contain an error, the appropriate status bits are set in the Interrupt Status register. An interrupt is generated when enabled. Whenever an error occurs, the syndrome bits are saved in the Syndrome FIFO allowing the syndrome to be read by the system. This output can be used to determine which bit was defective. The corrected data is not written back into the memory array but is corrected later as part of the refresh/scrubbing operations.

Inhibited Read Operations

Read operations may be inhibited. This action is required in multiprocessor systems when a main memory read must be terminated to allow a snooping cache to supply data to the requesting cache. A read operation may be inhibited prior to the close of the snoop window by asserting $\overline{\text{INH}}$. When an Inhibit is recognized, the module read operation is aborted and the module plays no further role in the bus transaction.

Reflective Reads

Inhibited reads may also be reflective. This option is enabled by asserting Transform Cycle ($\overline{\text{TRC}}$) simultaneously with $\overline{\text{INH}}$. When a transformed Inhibit is recognized, the module read operation is changed into a write operation. $\overline{\text{INH}}$ and $\overline{\text{TRC}}$ must be asserted within the snoop window. After Inhibit is recognized, $\overline{\text{BACK}}$ and the Data Bus become inputs. $\overline{\text{BACK}}$ are now used as a synchronous write enable to strobe the bus data into the Reflective Read FIFO. As the slave in the transaction, the snooping cache must supply $\overline{\text{BACK}}$. The timing of the $\overline{\text{BACK}}$ input to strobe data into the reflective FIFO is either early or real-time following the Bus Acknowledge mode selection for reads.

The Reflective FIFO is an image of the normal Write Data FIFO and is devoted exclusively to reflective read operations. Upon inhibit, the data bus is kept three-stated, allowing the snooping cache to drive the bus with the requested data. The module accepts the data into the Reflective Read FIFO at the full bus speed. A mechanism is required to prevent overrun of the reflective FIFO during consecutive transformed reads. As soon as the Inhibit is recognized, the module asserts Bus Request ($\overline{\text{BR}}$) in order to become the bus master in the next address phase. The system responds with Bus Grant ($\overline{\text{BG}}$). When the bus is acquired, the module asserts Bus Busy ($\overline{\text{BB}}$) until the reflective FIFO data is written to the DRAM and the module is capable of accepting another read. Since $\overline{\text{BR}}$ provides status of the availability of the reflective FIFO, the output may be used to delay the address phase of the next operation.

Read Snoop Window

As with writes, the snoop window may originate from either of two sources, one internal and the other external. On reads, the assertion of the bus acknowledge to transfer the data to the system is postponed until at least two clocks after the snoop window closes.

I/O Operations

Access to the internal Command and Status registers is controlled by the ID input. The details of the ID control are given in the Pin Description section. When the ID code for memory is input, all transactions access DRAM. The ID input can also point to the Indirect Address register. When the ID input specifies an I/O register, the Command and Status register accessed is the one pointed to by the Indirect Address register. The register address, position on the system bus, and the bit definition for each of the Command and Status registers is given in the Internal Registers section.

I/O register access follows the same Data Strobe and Bus Acknowledge modes as invoked for memory transactions with a few exceptions. In the Real-Time Data Strobe mode for writes, the $\overline{BR/FE}$ output plays no role and the transaction is acknowledged with the controller asserting $\overline{BACK}$. In all writes, system bus data must be valid at least one clock cycle before it is accepted. The controller delays $\overline{BACK}$ to meet this criterion. In all reads, data is always transferred in the second clock cycle after the snoop window closes or Data Strobe is asserted, whichever occurs last.

I/O operations may be inhibited. The duration of the I/O snoop window may be set externally or internally as in reads.

Write Bus Acknowledge and Data Strobe Modes

There are four modes of bus handshake: Early Data Strobe/Early Bus Acknowledge, Real-Time Data Strobe, Early Data Strobe/Real-Time Bus Acknowledge, and MBus. These modes are invoked by driving the $\overline{BACK}$ and $\overline{UERR}$ pins during Reset with a specific pattern. *Table 1* is a summary of the modes and their operation.

Early Data Strobe / Early Bus Acknowledge Mode

Data Strobe may be asserted at any time during or after the address phase. In *Table 1*, the cycle in which Data Strobe is asserted is designated cycle N. Data Strobe, once asserted, must remain asserted throughout the transaction. The FIFO may not be empty when the system asserts Data Strobe. If the FIFO goes empty in cycle N + k, the controller will assert Bus Acknowledge ($\overline{BACK}$) in the cycle following the one in which the FIFO goes empty (N + k + 1). The controller accepts the write data in the cycle following the one in which it asserted Bus Acknowledge (cycle N + k + 2). If the FIFO is empty when the Data Strobe is asserted, then k = 0. The controller would then assert Bus Acknowledge in the cycle following the one in which Data Strobe was asserted (cycle N + 1). Data is accepted in the following cycle (N + 2). If the transfer is a burst, Bus Acknowledge continues to be asserted until one cycle before the last data transfer.

Real-Time Data Strobe Mode

Writes are performed by programming the $\overline{BR/FE}$ output to include the status of the write data FIFO. The system may begin the write transaction with the address phase, but may not assert Data Strobe until the FIFO is known to be empty. In *Table 1*, the controller asserts $\overline{BR/FE}$ in cycle N. The system responds with Data Strobe in cycle N + k (k greater than or equal to 1) and the controller accepts the data in the same cycle. If the transaction is a burst, data is accepted each clock cycle thereafter until the burst is terminated. Data Strobe, once asserted, must remain asserted throughout the transaction.

Early Data Strobe/Real-Time Bus Acknowledge Mode

Data is accepted one clock cycle after Data Strobe is asserted in this mode. Bus Acknowledge is asserted in the same cycle in which the data is accepted (real-time Bus Acknowledge). Referring to *Table 1*, the system asserts Data Strobe in cycle N. The FIFO goes empty in cycle N + k. If the FIFO is already empty, k is 0. The controller asserts Bus Acknowledge and accepts the data in the next cycle (N + k + 1).

Table 1. Write Bus Acknowledge and Data Strobe Modes

Mode	Write Action	Write Cycle
Early $\overline{DS}$ Early $\overline{BACK}$	System asserts $\overline{DS}$	N
	Cntrlr FIFO goes empty	N+k, ($k \geq 0$)
	Cntrlr asserts $\overline{BACK}$	N+k+1
	Cntrlr accepts DATA	N+k+2
Real-Time $\overline{DS}$, No $\overline{BACK}$	Cntrlr asserts $\overline{BR/FE}$	N
	Systems asserts $\overline{DS}$, Cntrlr accepts DATA	N+k ($k \geq 1$)
Early $\overline{DS}$, Real-Time $\overline{BACK}$	System asserts $\overline{DS}$	N
	Cntrlr FIFO goes empty	N+k ($k \geq 0$)
	Cntrlr asserts $\overline{BACK}$, Cntrlr accepts DATA	N+k+1
MBus, $\overline{DS}$ Gnded	System asserts AS	N
	Cntrlr FIFO goes empty	N+k ($k \geq 0$)
	Cntrlr asserts $\overline{BACK}$ Cntrlr accepts DATA	N+k+1

MBus Mode

Data Strobe is permanently asserted in MBus mode. The controller operates as if it were in Early Data Strobe mode. The system asserts Address Strobe in cycle 0. The FIFO goes empty in cycle k. If the FIFO is already empty, k is 0. The controller asserts Bus Acknowledge and accepts the data in the next cycle (k + 1).

Read Operating Modes

The module offers several programmable options to control the data transfer during memory-read operations. Wait states may be inserted to allow additional propagation delay through the EDC path. Error correction can be disabled for diagnostic purposes. As in write operations, Data Strobe may be used to regulate transfers over the system interface. Finally, Bus Acknowledges may be programmed to occur one clock early or in real time with respect to the corresponding data transfer. The timing of the Bus Acknowledges is shown in *Figure 1*.

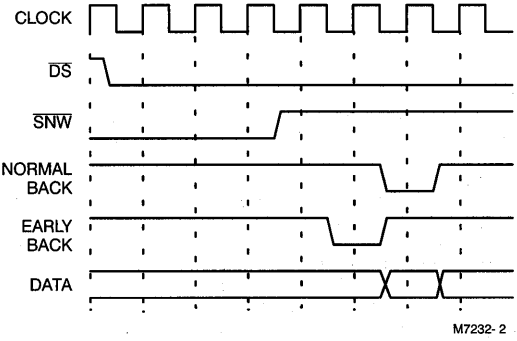


Figure 1. Early and Normal Bus Acknowledge Modes for Reads

Read Early BACK Mode

The Read Early BACK data transfer is triggered by the assertion of Data Strobe and closure of the snoop window (whichever occurs last) in cycle N. Data Strobe, once asserted, must remain asserted throughout the transaction. When read data is about to become available, $\overline{BACK}$[1] is asserted (cycle N + k). Read data is supplied to the bus in cycle N + k + 1.

Read Real-Time BACK Mode

The Read Real-Time BACK Mode begins when both Data Strobe is asserted and the snoop window is closed (cycle N). The controller responds with data and the corresponding Bus Acknowledge in cycle N + k + 2.

Wait States

The controller module may be programmed to insert wait states in the data path. This guarantees extra data set-up time when using error correction in system environments with fast bus clocks. The controller delays the Bus Acknowledges accordingly. Wait states may be inserted in either early or real-time Bus Acknowledge systems.

Acknowledge on Burst Reads

Read burst acknowledges will not generally be contiguous. The assertion of the acknowledge on long bursts (above 16 bytes) will be interrupted as more data is fetched from adjacent 128-bit DRAM pages. During a burst pause, the acknowledge is deasserted and then three-stated one-half clock later.

Bus Acknowledges in Transformed Transactions

When a read is transformed, the operation internal to the controller becomes a write. Bus Acknowledge becomes an input and is used as a strobe to clock the data into the reflective FIFO on each data transfer. The controller will treat the strobe derived from the incoming bus acknowledge as an early strobe when programmed in the early bus acknowledge mode. Otherwise the controller assumes that the data is aligned with the corresponding strobe derived from the incoming bus acknowledge.

When a write is transformed, the operation converts to a read. In this case, the controller behaves according to the invoked read mode. Transformed operations use a preprogrammed default burst length to specify their burst duration.

Bus Acknowledge Timing Characteristics

The Bus Acknowledge control signals are bidirectional and may be driven by the controller or another device on the system bus. Therefore there are times when no device will be driving this signal line. At high bus speeds, pull-ups may not be sufficient to guarantee that the Bus Acknowledge line will revert in a sufficiently short time to the deasserted state after the controller has ceased driving the line. To guarantee the state of the $\overline{BACK}$ signal lines at the end of a transaction, the controller first drives the outputs HIGH (deasserted) in the first half of the clock cycle in which Bus Acknowledge is to be deasserted and then three-states these outputs in the second half of this clock cycle. To insure that the Bus Acknowledge signal lines remain in the deasserted state when no device is driving them for long periods, pull-ups should be employed. At the beginning of a transaction cycle, Bus Acknowledge remains three-stated until it is to be asserted. Thus in the first acknowledge cycle of a transaction, $\overline{BACK}$ becomes driven and asserted at the same time. $\overline{BACK}$ continues to be driven until the end of the transaction cycle and terminates as described above.

Burst Last

Any read or write burst transaction may be terminated prematurely with the assertion of $\overline{BLST}$. $\overline{BLST}$ must be asserted during the clock cycle in which the last piece of data is transferred. Systems that require the data bus to go three-state in the next cycle must also deassert Data Strobe ($\overline{DS}$) when asserting $\overline{BLST}$. Burst last may not be used in Early Back mode or to prematurely terminate a transformed operation.

Inhibits and Snoop Window

Certain constraints apply to the system's assertion of inhibits and the closing of the snoop window.

The inhibit signal must not be asserted until at least two clocks after the address phase (i.e., if $\overline{AS}$ is asserted in bus clock N, inhibit may not be asserted until N + 2 or later).

Table 2. Read Bus Acknowledge Modes

Mode	Read Action	Read Cycle
Early BACK no wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK	N + k ($k \geq 2$)
	Cntrlr supplies data	N + k + 1
Early BACK with wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK	N + k + 1 ($k \geq 2$)
	Cntrlr supplies data	N + k + 2
Real Time BACK no wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK and supplies data	N + k ($k \geq 2$)
Real Time BACK with wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK and supplies data	N + k + 1 ($k \geq 2$)

Inhibits and Snoop Window (continued)

There must be a minimum of one bus clock cycle between the close of a transaction's snoop window and the address strobe of the next transaction (i.e., if the snoop window is deasserted on the system bus during bus clock N, the next transaction's address strobe must not be asserted until N + 2). This scenario would most likely occur when the first transaction is inhibited but not transformed.

DRAM Interface

The DRAM array is 128 data bits wide. This data is subdivided into banks: 4 banks of 32 bits each for the 32-bit EDC version and two banks of 64 bits each for the 64-bit EDC version. Each bank includes the associated error check bits: 7 bits for the 32-bit EDC version and 8 bits for the 64-bit EDC version. The DRAM array is divided in depth into blocks. Each block may be populated with different DRAM chip sizes, however, all DRAM chips in a given block must have the same depth. From one to four blocks may be populated with DRAM, however there are certain restrictions as given in other sections.

The DRAM interface consists of a bidirectional data bus for each DRAM bank, plus a bidirectional bus for the associated error detection and correction check bits. There is also a set of bank-associated write/read control outputs. The DRAM blocks are controlled by separate $\overline{RAS}$ and $\overline{CAS}$ control outputs. There is one $\overline{RAS}$ and one $\overline{CAS}$ for each block. The entire DRAM array is addressed through one set of 12 row/column multiplexed address lines. The row/column partition is dictated by the DRAM that populates a particular block.

Latch Requirements

Transparent latches are required between the R/W signals issued by the controller module and the DRAM. These latches guarantee that the R/W signals to the DRAM are stable while CAS is asserted. The latch is transparent when CAS is HIGH and closed when CAS is LOW. The latches can also be used to buffer R/W lines to the DRAM. A 74ABT373 or equivalent is recommended.

There are two alternatives for the latches:

1. One quad latch is devoted to each DRAM block. Each quad latch is enabled by the CAS for that block. R/W[3:0] is connected to the four inputs of the quad latch and the outputs of the quad latch are connected to the R/W inputs of the appropriate DRAM bank in that block. Refer to part (a) in *Figure 2*.
2. One quad latch is devoted to all of the DRAM blocks. the quad latch is enabled by the logical OR of CAS[3:0]. R/W[3:0] is connected to the four inputs of the quad latch and the outputs of the quad latch are connected to the R/W inputs of the appropriate DRAM bank for all of the blocks. Refer to part (b) in *Figure 2*.

DRAM Interface for the 32-Bit EDC

The controller supports an organization of DRAM that is 156 bits wide (four banks each consisting of 32 bits of data plus 7 error check bits) and up to four blocks deep. Each block is controlled by separate $\overline{RAS}$ and $\overline{CAS}$ signals ($\overline{RAS}$[3:0], $\overline{CAS}$[3:0]). Each Bank is controlled by separate read/write signals (R/$\overline{W}$[3:0]). The DRAM address outputs from the controller module consists of a 12-bit row/column multiplexed bus. This bus is intended to drive a symmetrical set of address driver devices, which in turn drive the DRAM array address lines. Timing for the $\overline{RAS}$ and $\overline{CAS}$ outputs as well as other DRAM related timing is programmable. A representation of the DRAM organization is shown in *Figure 3*.

Each square in *Figure 3* represents a bank of memory that is 32 data bits wide plus 7 check bits. A block is a column of four banks totalling 128 data bits wide plus 28 check bits. Each block is controlled by dedicated $\overline{RAS}$ and $\overline{CAS}$ signals. With 12 multiplexed row/column address lines, each bank can be up to 16 megabits deep. The row/column address multiplexing is programmable. The controller supports 256K-, 1M-, 4M-, and 16M-deep DRAMs.

DRAM Interface for the 64-Bit EDC

This controller supports an organization of DRAM that is 144 bits wide (two banks each consisting of 64 bits of data plus 8 error check bits) and up to four blocks deep. Each block is controlled by separate $\overline{RAS}$ and $\overline{CAS}$ signals ($\overline{RAS}$[3:0], $\overline{CAS}$[3:0]). Each bank is controlled by separate read/write signals (R/$\overline{W}$[1:0]). Address outputs, $\overline{RAS}$ and $\overline{CAS}$ outputs and DRAM timing is identical to that in the 32-bit EDC version. A representation of the DRAM organization is shown in *Figure 4*.

Each square in *Figure 4* represents a bank of memory that is 64 data bits wide plus 8 check bits. A block is a column of two banks totaling 128 data bits wide plus 16 check bits. Each block is controlled by dedicated $\overline{RAS}$ and $\overline{CAS}$ signals. With 12 multiplexed row/column address lines, each bank can be up to 16 megabits deep. As in the 32-bit EDC version, the row/column address multiplexing is programmable. The controller supports 256K-, 1M-, 4M-, and 16M-deep DRAMs.

DRAM Block Placement

There are four physical DRAM blocks. Each block may be populated with an array of DRAMs that are 128 bits wide by 256K, 1M, 4M, or 16M deep. Physical block population need not be contiguous.

An array of five registers are used to specify the DRAM configuration. At power-up, the controller module is programmed with the Base address (the starting address of the entire memory array) and the Logical Block Displacement and Population (the address gap between logical blocks and their respective DRAM sizes). Finally, the physical/logical mapping is assigned and each block's RAS/CAS address split point is specified.

During operation, an incoming memory address is evaluated. Once the controller determines that this address is valid, the appropriate RAS signal for the selected block is asserted. The controller will remain inactive if the comparison is invalid. Refer to the register description for programming details.

DRAM Interface Signals

CYM7232 – 32-bit EDC

The module interface to the DRAM array is made through the signals described below.

DDA[31:0] – Data Bus (Bank 0). DDA[31:0] forms a 32-bit data bus that is connected to bank 0 in every populated block.

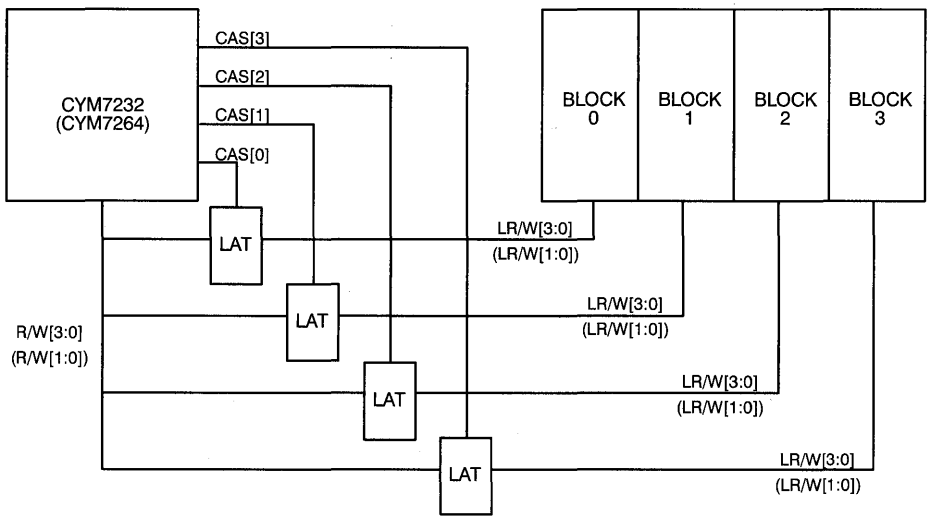
DDB[31:0] – Data Bus (Bank 1). DDB[31:0] forms a 32-bit data bus that is connected to bank 1 in every populated block.

DDC[31:0] – Data Bus (Bank 2). DDC[31:0] forms a 32-bit data bus that is connected to bank 2 in every populated block.

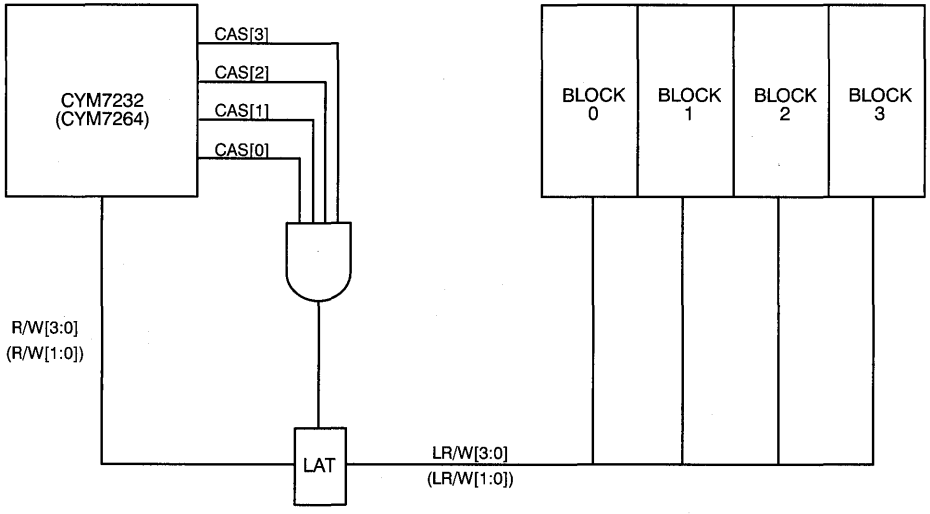
DDD[31:0] – Data Bus (Bank 3). DDD[31:0] forms a 32-bit data bus that is connected to bank 3 in every populated block.

EDA[6:0] – Check Bus (Bank 0). EDA[6:0] forms a 7-bit error check bit bus that is associated with the data on DDA[31:0].

EDB[6:0] – Check Bus (Bank 1). EDB[6:0] forms a 7-bit error check bit bus that is associated with the data on DDB[31:0].



(a)



(b)

Figure 2. R/W Latch Configurations

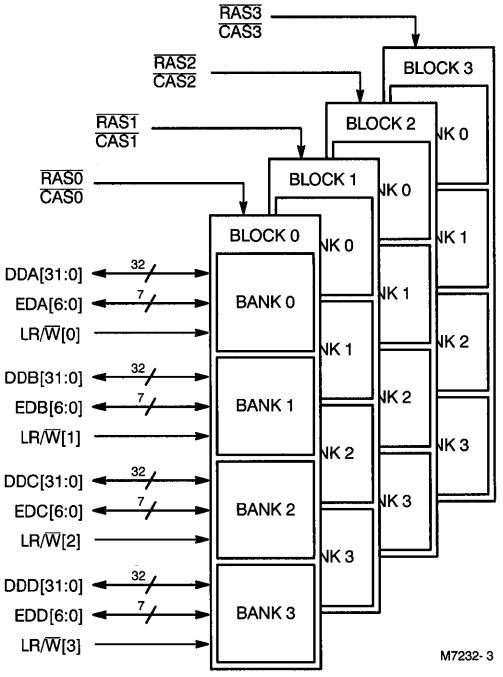


Figure 3. DRAM Configuration for the CYM7232

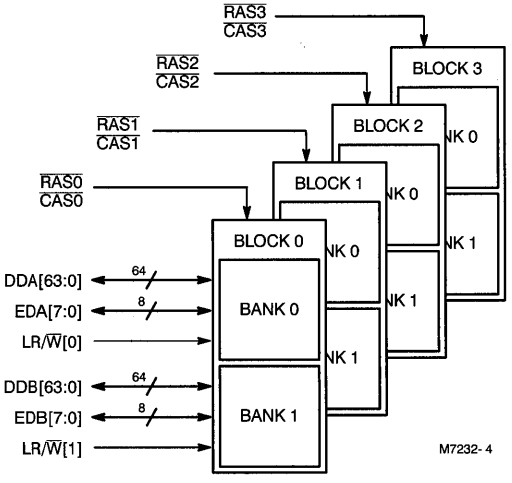


Figure 4. DRAM Configuration for the CYM7264

CYM7232 – 32-bit EDC (continued)

EDC[6:0] – Check Bus (Bank 2). EDC[6:0] forms a 7-bit error check bit bus that is associated with the data on DDC[31:0].

EDD[6:0] – Check Bus (Bank 3). EDD[6:0] forms a 7-bit error check bit bus that is associated with the data on DDD[31:0].

ADRS[11:0] – Address Bus. ADRS is a 12-bit row/column multiplexed address bus that supplies the address to the DRAM to access the proper 128-bit data word. The multiplexing is programmable for different depths of DRAM.

R/$\overline{W}$[3:0] – Read/Write Control. R/$\overline{W}$[3:0] are the read/write controls for the four banks of the DRAM array. R/$\overline{W}$0 controls read/write for all blocks of DDA[31:0], R/$\overline{W}$1 controls read/write for all blocks of DDB[31:0], R/$\overline{W}$2 controls read/write for all blocks of DDC[31:0], and R/$\overline{W}$3 controls read/write for all blocks of DDD[31:0].

$\overline{RAS}$[3:0] – These signals are the four $\overline{RAS}$ outputs to control each block of the DRAM.

$\overline{CAS}$[3:0] – These signals are the four $\overline{CAS}$ outputs to control each block of the DRAM.

The address bus, ADRS[11:0], RAS[3:0], CAS[3:0] should be connected through a set of drivers to the appropriate DRAM inputs. R/$\overline{W}$[3:0] should be connected through a set of latches, gated by the appropriate CAS to the DRAM R/W controls. The driver configuration is dependent upon the capacitance that must be driven.

The data bus, check bus, and read/write control signals are connected across the DRAM array. DDA[31:0] and EDA[6:0] are connected to the data I/O of all the Bank 0 DRAMs. The Bank 0 DRAMs are the top row of DRAMs in *Figure 3*. LR/$\overline{W}$0 is connected to the Write Control input of all the Bank 0 DRAMs. DDB[31:0] and EDB[6:0] are connected to the data I/O of all the Bank 1 DRAMs. The bank 1 DRAMs are the second row of DRAMs. LR/$\overline{W}$1 is connected to the Write Control input of all the Bank 1 DRAMs. This connection pattern continues with Banks 2 and 3.

$\overline{RAS}$0 and $\overline{CAS}$0 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of Block 0. Block 0 is the left column of DRAMs in the array in *Figure 3*. Note that each block consists of Banks 0 through 3. Similarly, $\overline{RAS}$1 and $\overline{CAS}$1 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of Block 1. This connection pattern continues through Block 3.

CYM7264 – 64-bit EDC

The module interface to the DRAM array is made through the signals described below.

DDA[63:0] – Data Bus (Bank 0). DDA[63:0] forms a 64-bit data bus that is connected to bank 0 in every populated block.

DDB[63:0] – Data Bus (Bank 1). DDB[63:0] forms a 64-bit data bus that is connected to bank 1 in every populated block.

EDA[7:0] – Check Bus (Bank 0). EDA[7:0] forms an 8-bit error check bit bus that is associated with the data on DDA[63:0].

EDB[7:0] – Check Bus (Bank 1). EDB[7:0] forms an 8-bit error check bit bus that is associated with the data on DDB[63:0].

ADRS[11:0] – Address Bus. ADRS is a 12-bit row/column multiplexed address bus that supplies the address to the DRAM to access the proper 128-bit data word. The multiplexing is programmable for different depths of DRAM.

CYM7264 – 64-bit EDC (continued)

R/$\overline{W}$[1:0] – Read/Write Control. R/$\overline{W}$[1:0] are the read/write controls for the two banks of the DRAM array. R/$\overline{W}$0 controls read/write for all blocks of DDA[63:0], R/$\overline{W}$1 controls read/write for all blocks of DDB[63:0].

$\overline{RAS}$[3:0] – These signals are the four $\overline{RAS}$ outputs to control each block of the DRAM.

$\overline{CAS}$[3:0] – These signals are the four $\overline{CAS}$ outputs to control each block of the DRAM.

The address bus, ADRS[11:0], RAS[3:0], CAS[3:0] should be connected through a set of drivers to the appropriate DRAM inputs. R/W[1:0] should be connected through a set of latches, gated by the appropriate CAS to the DRAM R/W controls. The driver configuration is dependent upon the capacitance that must be driven.

The data bus, check bus, and read/write control signals are connected across the DRAM array. DDA[64:0] and EDA[7:0] are connected to the data I/O of all the Bank 0 DRAMs. The Bank 0 DRAMs are the top row of DRAMs in *Figure 4*. LR/$\overline{W}$0 is connected to the Write Control input of all the Bank 0 DRAMs. DDB[63:0] and EDB[7:0] are connected to the data I/O of all the Bank 1 DRAMs. LR/$\overline{W}$[1] is connected to the read / write control inputs of all of the DRAMs of Bank 1.

$\overline{RAS}$0 and $\overline{CAS}$0 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of block 0. Block 0 is the left column of DRAMs in the array in *Figure 4*. Note that each block consists of Bank 0 and Bank 1. Similarly, $\overline{RAS}$1 and $\overline{CAS}$1 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of block 1.

DRAM Timing

The system bus clock rate determines the DRAM timing through an internal (X2, X4) phase locked loop, or an externally generated multiple clock (X1, X2, X3, X4 applied to MCLK input). Along with the multiplier selection, the appropriate VCO is selected to generate either a 66-MHz, 80-MHz, or 100-MHz internal clock. This selection is shown in *Table 3*. There are two versions, –H and –S. The –H version permits the use of the higher clock frequency multiples for maximum performance.

Table 3. Required PLL Frequency

Bus Clock (MHz)	Phase Lock Loop Frequency (MHz) – H	Phase Lock Loop Frequency (MHz) –S
40	80	80
33	66 (int), 99 (ext)	66
25	100	50 (ext)

The phase lock loops should be operated close to their center frequency to guarantee operation. For deviations from the bus clock frequencies listed in *Table 3*, consult Command Register 4 (programming of VCO[1:0]). Refer to the CLM[1:0] field in the Command register for programming details.

DRAM timing is fully programmable through internal registers. The resolution of the timing is equal to the period of the internal clock. (This is normally twice the bus clock frequency for 40-MHz bus speeds.) The parameters listed in *Table 4* are programmable.

Refer to the timing diagrams at the end of this data sheet for the timing definitions. Refer to the Register Descriptions for details.

Table 4. DRAM Programmable Timing Parameters

Parameter	Description
t_{AR}	Address to $\overline{RAS}$ assertion
t_{RAM}	$\overline{RAS}$ to multiplexed address
t_{MAC}	Multiplexed address to $\overline{CAS}$
t_{RAS}	$\overline{RAS}$ pulse width
t_{RPR}	$\overline{RAS}$ pre-charge width
t_{CP}	$\overline{CAS}$ pre-charge width
t_{DC}	FIFO data delay to $\overline{CAS}$
t_{RIN}	$\overline{RAS}$ completion during non-reflective inhibit
t_{ENR}	Enable delay on read
t_{ENW}	Enable delay on write

Refresh and Scrubbing

Refresh requirements vary depending on the density and organization of the DRAM chips in the system. However, rows must be refreshed at the same interval (approximately every 15 microseconds the next row is refreshed). The refresh requests are generated by two cascaded counters. A programmable 7-bit counter divides CLK down to create a 1-MHz clock signal. This clock is further divided by a 4-bit, modulo 15 counter, to generate a refresh request every 15 µsec. These refresh requests are synchronously arbitrated with memory requests.

The 26-bit Scrub Address counter is comprised of three smaller counters: the least significant 12 bits form a row scrub counter, the middle two bits form a block counter, and the most significant 12 bits form a column address counter.

All four banks of a given block are scrubbed simultaneously at a particular address. All error correction channels in the controller are used in parallel (4 channels in CYM7232, 2 channels in CYM7264). While one of the four DRAM blocks is scrubbed, the other three blocks undergo normal refresh. The 2-bit Scrub Block counter advances after all rows in a particular block are scrubbed. Finally, the column address is incremented so that all rows and blocks of the next column are refreshed and scrubbed. A fully populated memory using 16-Mbit devices to achieve 1-gigabyte capacity is scrubbed in little more than 15 minutes. When an error is detected during scrubbing operations, the correction address will be copied from the Refresh Address counter to the Error Location register. (Note that when an error occurs in a normal read operation, the corrected data is not written back into the memory array. Data is corrected inside the DRAMs during scrubbing cycles only.) When an error occurs during refresh/scrubbing operations the refresh cycle (i.e., a read to check for errors) is turned into a scrub cycle (i.e., read-modify-write to correct the errors).

Each block of memory may be populated with different sized DRAM components however, all banks within a given block must be populated with the same depth memory chip. For simplicity, the Refresh Address counter treats every block as if it were populated with DRAMs of maximum (16-Mbit) capacity. When refreshing smaller memories, the same address location will be scrubbed multiple times before the counter advances to the next location.

Refresh Modes

There are two modes of refresh/scrubbing. The four $\overline{RAS}$ signals are staggered differently in each mode. Staggering prevents noise problems when switching current simultaneously to multiple blocks of DRAM.

Staggered $\overline{RAS}$

The onset of each $\overline{RAS}$ signal is staggered by one bus clock (four bus clocks overall) in the first mode. Once all $\overline{RAS}$ lines are asserted a single $\overline{CAS}$ signal is selected for presentation to the scrubbed block of memory. The strobe signal used to enable clocking of the scrubbed data into the controller is also delayed by an amount equal to the staggered $\overline{RAS}$ delay.

Mutually Exclusive $\overline{RAS}$

Some SIMMs are constructed with multiple sections of $\overline{RAS}$ enabled DRAM (i.e., common $\overline{CAS}$ lines across sections) The controller offers a second non-overlapping $\overline{RAS}$ refresh mode that supports these SIMMs. This is essential so that the $\overline{CAS}$ that is asserted for the scrub operation will enable only the required SIMM section. Should this type of DRAM SIMM be used, pairs of blocks would be $\overline{RAS}$ enabled during refresh or normal DRAM accesses. Each block pair would share a common $\overline{CAS}$. The controller may be configured to internally OR the appropriate $\overline{CAS}$ pairs to produce a single $\overline{CAS}$ output for each pair of blocks. Refresh in the non-overlapping $\overline{RAS}$ mode is longer than that of the staggered $\overline{RAS}$ refresh mode. Refer to the Register Descriptions for details.

Initialization

The DRAM is initialized when the INIT command is given. The DRAMs are energized with 15 $\overline{RAS}$ only cycles. All of DRAM can then optionally be filled with zeros and the associated error check bits.

Diagnostic Features

For diagnostic purposes, the DRAM error check bits may be read or written by the system. The error check bits may be accessed by reading the EDC registers at any time. The error check bit fields will contain the error check bits from the previous DRAM read cycle. Error check bits may be directly written to DRAM by first writing the desired check bits to the Write Check Bit register and then setting the appropriate control bit in the Command register. All subsequent DRAM writes will write the check bits from this register. Clearing the control bit will return the check bit source to the data path's write error check bit generation circuitry.

Bus Interface Signal Description

D[63:0] – Data. During the data phase, D[63:0] contains the transactions data. The system data bus signals are equipped with holding buffers. These buffers use a weak feedback buffer combined with an input buffer to form a latch. The latch holds the last value driven on the bus.

DP[7:0] – Data Parity. During the data phase, DP[7:0] reflects the parity of the transaction's data. During the address phase, DP[7:0] is ignored and the outputs are three-stated. Data parity is checked only over those bytes that are enabled. During a data phase write, DP[7:0] are inputs, receiving the parity as transferred across the bus. During a data phase read, DP[7:0] are outputs, indicating the parity of the data that has been applied to the bus. The parity output is enabled only when the relevant data byte is enabled. The parity outputs remain three-stated when the parity is disabled. The parity's sense (i.e., odd/even and enable/disable) is specified by the Parity Mode bits, PM[2:0]. DP[7:0] are assigned as given in *Table 5*.

The system data bus parity signals are equipped with holding buffers similar to those used by the system data bus.

Table 5. Data Parity Assignments

Data Parity	Data Byte
DP[0]	D[7:0]
DP[1]	D[15:8]
DP[2]	D[23:16]
DP[3]	D[31:24]
DP[4]	D[39:32]
DP[5]	D[47:40]
DP[6]	D[55:48]
DP[7]	D[63:56]

PMD[2:0] – Parity Mode. The Parity Mode bits specify the parity computation algorithm and identify those signals that participate in the parity computation. They must be hardwired for the correct configuration. The parity mode selection is applied to both the address and data buses. These bits are defined below.

PM2
- 0 – Even Parity Computed (sum of bits in byte and parity bit is even.)
- 1 – Odd Parity Computed (sum of bits in byte and parity bit is odd.)

PM1
- 0 – Data Parity Disabled
- 1 – Data Parity Computed

PM0
- 0 – Address Parity Disabled
- 1 – Address Parity Computed

A[35:0] – Address. During the address phase, the system will supply the transaction's address on A[35:0] and assert $\overline{AS}$.

AP[3:0] – Address Parity. During the address phase, the lowest 32 bits of the transaction's address can be checked for parity. The system can generate a set of parity inputs AP[3:0] that correspond to A[31:0]. Parity is not supported for A[35:32]. The parity's sense (i.e., odd/even and enable/disable) is specified by the Parity Mode bits, PM[2:0]. Note that the parity mode bits also define the parity mode for the data bus. AP[3:0] are assigned as given in *Table 6*.

Table 6. Address Parity Assignments

Address Parity	Address Byte
AP[0]	A[7:0]
AP[1]	A[15:8]
AP[2]	A[23:16]
AP[3]	A[31:24]

TYPE[5:0] – Transaction Type. During the address phase, TYPE[5:0] specify the Transaction Type (see *Table 7*). These are synchronous inputs. Note that the TYPE input may be changed on a transaction by transaction basis, consequently, different processors may be mixed within the system.

TYPE0 – Read/Write. When 0, this bit indicates the transaction is a write. When 1, this bit indicates the transaction is a read.

Table 7. Type Interpretation

Type Bits						Data Size	Transaction Type
5	4	3	2	1	0		
0	0	X	X	X	0	Any	Write
0	X	X	X	X	1	Any	Read
1	0	X	X	X	0	Default Burst	Write
1	X	X	X	X	1	Default Burst	Read
X	X	X	X	0	X	≥ Bus Width	Sequential Burst Order
X	X	X	X	1	X	≥ Bus Width	Intel Burst Order
X	X	X	0	X	X	Any	Size [3:0] are Size Bits
0	X	X	1	X	X	≤ Bus Width	Size [7:0] are Byte Enables
X	X	0	X	X	X	Any	Little-Endian Bus
X	X	1	X	X	X	Any	Big-Endian Bus
0	1	X	X	X	0	Any	Posted Write
1	1	X	X	X	0	Default Burst	Posted Write

TYPE1 – Burst Order. Given a system bus of width N bytes (N = 4 or 8), any transaction as specified by the SIZE input which is greater than N constitutes a burst. Thus transactions of double words (8 bytes) and larger are bursts for a 32-bit bus and transactions of 16 bytes and larger are bursts for a 64-bit bus. The maximum burst length is 128 bytes. During bursts the lowest order bits of the address input are ignored. AD[1:0] are ignored for a 32 bit bus system and AD[2:0] are ignored for a 64 bit bus system. This is the alignment constraint.

The next higher set of address inputs are loaded into a counter, which generates the proper address as the burst proceeds. The counter length is given in *Table 8*. The generated burst address will wrap around at the cache line end and complete the burst access for the remainder of the cache line.

Table 8. Burst Counter Length

Burst Length (bytes)	Burst Counter Length for 32-Bit Bus (bits)	Burst Counter Length for 64-Bit Bus (bits)
8	1	Not Burst
16	2	1
32	3	2
64	4	3
128	5	4

A new address, in which the burst counter serves as the lowest portion, is formed. The counter extends the length of address bits as shown in *Table 8* and starts at AD2 for a 32-bit system bus and at AD3 for a 64-bit system bus. All higher address bits (above the counter) remain fixed throughout the burst transaction and are not affected by rollover of the burst counter. As an example, for a 64-bit system bus and a SIZE of 64 bytes, the system ignores AD[2:0], fixing these bits at 0. AD[5:3] form the internal burst counter starting from the address as transferred over the system bus, and AD[35:6] remain fixed as originally input. This address generation is shown for this example in *Table 9*.

Table 9. Burst Address Example

AD[35:6]	AD[5:3]	AD[2:0]
Fixed	Counter	000

When TYPE1 = 0 the burst order is sequential. Subsequent addresses are generated by sequentially incrementing the bits of the address within the range of the burst counter as determined above. After reaching the address in which all burst counter bits are ones, the counter wraps around to zero. Higher-order addresses remain fixed.

When TYPE1 = 1 the burst counter increments in the non-sequential fashion characteristic of Intel processors. In all other respects, the address for the burst is the same as that in the sequential case. The non-sequential burst counter algorithm extends the Intel scheme to any length burst. The nonsequential counting starts at the address specified by the address bus input. The counter bits are then incremented in the following fashion:

1. the lowest-order bit always toggles,
2. a bit toggles only if the next lowest order bit in the counter is toggling for the second time (independent of its value).

For example, if the burst counter is 3 bits in length (AD[5:3] as above) and begins at address 101, then the counting sequence is

101, 100, 111, 110, 001, 000, 011, 010

Notice that in this counting sequence, higher-order bits change the least often and therefore result in a minimum number of DRAM page mode accesses.

TYPE2 – SIZE Interpretation. The SIZE bits have two alternative interpretations. When TYPE2 = 0, the transaction length in bytes is given by the value of SIZE[3:0]. When TYPE2 = 1, the byte(s) that are enabled in the transaction are specified when their respective size bits are asserted LOW (e.g., SIZE[N] means BYTE[N] participates in the transaction). For elaboration see the SIZE[7:0] definition.

TYPE3 – Little Endian/Big Endian. Processors may define the position of BYTE 0 on the bus in either of two ways. Either BYTE 0 appears as the lowest byte on the bus (D[7:0] – little endian, TYPE3 = 0) or BYTE 0 appears as the highest byte on the bus (big endian – D[M:M−7], where M = Bw − 1. Bw is the bus width in bits, TYPE3 = 1). For elaboration see the definition of the SIZE[7:0] bits.

TYPE4 – Write Posting. When TYPE4 = 1, the write data is posted into the Write FIFO, where it remains until the next read is completed. This can be used to postpone the actual DRAM write until after the DRAM read is completed, thereby speeding cache line fills.

TYPE5 – Default Burst Mode. When TYPE5 = 0, the transaction's size is specified by SIZE[7:0] (which are interpreted according to TYPE2). When TYPE5 = 1, the transaction's size is specified by the default burst size programmed into the Command register. The burst size defaults to this value regardless of TYPE5 during reflective reads transformed into writes and writes transformed to reads for ownership.

SIZE[7:0] – Transaction Size. During the address phase, SIZE[3:0] specify the number of bytes to be transferred during a bus transaction. These are synchronous inputs. SIZE[7:4] are an extended size control used to support byte enabled transfers. The expanded definition is compatible with i486, i860, SPARC, MIPS, 88K and 68040 processors. The interpretation of SIZE is determined by TYPE2 as in *Table 10* through *Table 16*. Note that for size specifications that are larger than the system bus size, the Transaction Size specifies the internal burst address generation wraparound.

Two interpretations are offered in the above table to support SPARC MBus and Motorola 88K processors.

Table 10. Size Interpretation with TYPE2 = 0, SIZE[7:4] = XXXX

SIZE 3	SIZE 2	SIZE 1	SIZE 0	Transaction Size
0	0	0	0	Byte
0	0	0	1	Halfword (2 Bytes)
0	0	1	0	Word (4 Bytes)
0	0	1	1	Doubleword (8 Bytes)
0	1	0	0	16-Byte Burst
0	1	0	1	32-Byte Burst
0	1	1	0	64-Byte Burst
0	1	1	1	128-Byte Burst
1	0	0	0	32-Byte Burst
1	0	0	1	32-Byte Burst
1	0	1	0	64-Byte Burst
1	0	1	1	64-Byte Burst
1	1	0	0	Doubleword (8 Bytes)
1	1	0	1	Word (4 Bytes)
1	1	1	0	Halfword (2 Bytes)
1	1	1	1	Byte

Table 11. 64 Bit Bus Address Interpretation Size = 1 Byte

A2	A1	A0	Byte #	Big Endian	Little Endian
0	0	0	0	D[63:56]	D[7:0]
0	0	1	1	D[55:48]	D[15:8]
0	1	0	2	D[47:40]	D[23:16]
0	1	1	3	D[39:32]	D[31:24]
1	0	0	4	D[31:24]	D[39:32]
1	0	1	5	D[23:16]	D[47:40]
1	1	0	6	D[15:8]	D[55:48]
1	1	1	7	D[7:0]	D[63:56]

Table 12. 64 Bit Bus Address Interpretation Size = 2 Bytes

A2	A1	A0	Halfword #	Big Endian	Little Endian
0	0	X	0	D[63:48]	D[15:0]
0	1	X	1	D[47:32]	D[31:16]
1	0	X	2	D[31:16]	D[47:32]
1	1	X	3	D[15:0]	D[63:48]

Table 13. 64 Bit Bus Address Interpretation Size = 4 Bytes

A2	A1	A0	Word #	Big Endian	Little Endian
0	X	X	0	D[63:32]	D[31:0]
1	X	X	1	D[31:0]	D[63:32]

Table 14. 32 Bit Bus Address Interpretation Size = 1 Byte

A2	A1	A0	Byte #	Big Endian	Little Endian
X	0	0	0	D[31:24]	D[7:0]
X	0	1	1	D[23:16]	D[15:8]
X	1	0	2	D[15:8]	D[23:16]
X	1	1	3	D[7:0]	D[31:24]

Table 15. 32 Bit Bus Address Interpretation Size = 2 Bytes

A2	A1	A0	Half-Word #	Big Endian	Little Endian
X	0	X	0	D[31:16]	D[15:0]
X	1	X	1	D[15:0]	D[31:16]

Table 16. Size Interpretation with TYPE2 = 1

Size[x]								Byte
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	0	D[7:0]
X	X	X	X	X	X	0	X	D[15:8]
X	X	X	X	X	0	X	X	D[23:16]
X	X	X	X	0	X	X	X	D[31:24]
X	X	X	0	X	X	X	X	D[39:32]
X	X	0	X	X	X	X	X	D[47:40]
X	0	X	X	X	X	X	X	D[55:48]
0	X	X	X	X	X	X	X	D[63:56]

Processors generally require their byte enable signals to be contiguous. No checking is performed to distinguish invalid combinations from valid combinations.

$\overline{AS}$ – Address Strobe. This signal is asserted by the bus master during the address phase of the transaction. The address and transaction attributes are strobed into the Controller Module during the address phase. The address phase is one clock cycle long and is normally followed by one or more data phases.

$\overline{DS}$ – Data Strobe. This signal is asserted by the bus master to begin the data phase of the transaction. Data strobe is recognized in certain modes and can be used by the system to delay the onset of the transaction. If the transaction is a burst, data strobe can not be used to interrupt or delay individual data phases of the burst. Data Strobe may be permanently asserted in those applications that do not need this function. Refer to the section on Bus Acknowledge and Data Strobe Modes for details.

$\overline{BLST}$ – Burst Last. The burst length is specified by SIZE[3:0] or the programmed default burst length by way of the TYPE input during the address phase of every transaction. $\overline{BLST}$ may be used by the bus master to override the default or SIZE specified burst length by prematurely terminating the bus transaction. $\overline{BLST}$ must be asserted in the same cycle as the last data transfer.

$\overline{INH}$ – Inhibit. This signal may be asserted by a cache controller in multiprocessing environments to abort a bus transaction already in progress. When $\overline{INH}$ is received before the snoop window ends, the operation is terminated. If the transaction is a memory read, no data is transferred over the system bus while the snoop window is open. If the transaction is a memory write and data has already been transferred, the internal FIFOs are cleared. Inhibit may be used to prematurely terminate I/O opera-

tions before data is transferred. $\overline{INH}$ should not be asserted after the snoop window closes.

$\overline{TRC}$ – Transform Cycle. This signal, when asserted along with $\overline{INH}$, transforms an inhibited read cycle into a write cycle (reflective) or an inhibited write cycle into a read cycle (read-for-ownership). Transformed transactions use the programmed default burst length and ignore the SIZE specified in the original transaction. The burst begins at the address specified at the transaction start.

$\overline{SNW}$ – Snoop Window. This input may be used to define the duration of the snoop window. Operations may be inhibited and transformed in any cycles in which this signal is asserted. As an alternative, the duration of the snoop window may be defined by an internal counter.

$\overline{RSTIN}$ – Reset In. This signal is used to reset the controller. The signal must last for at least 16 clocks. This signal is internally synchronized to the bus clock.

$\overline{BACK}$[1:0] – Bus Acknowledge. These signals supply the transaction acknowledge to the bus master. They are defined in *Table 17*. These signals also receive acknowledges from the system during reflective reads thereby acting as data strobes. During system reset $\overline{BACK}$[1:0] act as inputs to program bus acknowledge modes and select the source of the snoop window signal.

$\overline{BACK}$[1:0] are used as inputs during Reset to select the Bus Acknowledge and Data Strobe modes. $\overline{BACK}$[1:0] must be driven according to *Table 18* when Reset is asserted to invoke the desired mode.

$\overline{UERR}$ – Uncorrectable Error Interrupt. This signal indicates the presence of an unrecoverable error condition on a read operation. The signal is asserted at the same time as the associated acknowledge is sent to the system bus. As with $\overline{BACK}$[1:0], $\overline{UERR}$ may serve as an input. The signal must be driven to select the source of the Snoop Window signal during system reset. $\overline{UERR}$ should be pulled up with a 1K-ohm resistor to V_{CC}.

Table 17. $\overline{BACK}$[1:0] Outputs

$\overline{BACK}$1	$\overline{BACK}$0	Definition
0	1	Valid Data Transfer
1	1	Wait States
Three-state	Three-state	Idle Cycles

Table 18. $\overline{BACK}$[1:0] Inputs When $\overline{RSTIN}$ is Asserted

$\overline{BACK}$1	$\overline{BACK}$0	$\overline{DS}$ Mode	$\overline{BACK}$ Mode
0	0	MBus ($\overline{DS}$ Gnd)	With Data
0	1	Early $\overline{DS}$ (1 Clk)	With Data
1	0	Real-Time $\overline{DS}$	None (Uses $\overline{BR/FE}$)
1	1	Early $\overline{DS}$ (2 Clks)	Early $\overline{BACK}$ (1 Clk)

Table 19. $\overline{UERR}$ Inputs When $\overline{RSTIN}$ is Asserted

$\overline{UERR}$ ($\overline{SNW}$)	Snoop Window Source
0	External
1	Internal

When a read is inhibited and transformed into a write, the $\overline{BACK}$[1:0] signals become inputs and are used to strobe the bus data into the Reflective FIFO. *Table 20* gives the interpretation of the $\overline{BACK}$[1:0] inputs when the reflective writes are in progress.

Table 20. $\overline{BACK}$[1:0] Inputs as Reflective Reads are Transformed Into Writes

$\overline{BACK}$1	$\overline{BACK}$0	Definition
0	1	Valid Data Transfer
1	1	Idle Cycle
Other	Modes	Invalid

$\overline{BERR}$ – Bus Error. This signal indicates that a parity error condition has occurred during the address or data phase of a transaction. This signal is asynchronous (i.e., it will occur one cycle after the corresponding address parity error or two cycles after the corresponding data parity error). $\overline{BERR}$ may be programmed to last for one clock cycle or until cleared. Due to the nature of $\overline{BERR}$ internal to the module, the controller will log a parity error in its status register if any other device pulls $\overline{BERR}$ LOW.

$\overline{BR/FE}$ – Bus Request/FIFO Empty. This signal will be issued by the controller during reflective read transactions. $\overline{BR}$ from the main memory system should be interpreted as the highest priority request for bus mastership to the system's arbiter. In this case $\overline{BR/FE}$ works in conjunction with $\overline{BG}$ and $\overline{BB}$ to effect this mastership. Additional system bus transactions will be prevented until the ongoing write (resulting from the reflective read) to main memory has completed. Systems having more elaborate protocols for acknowledging data transfers between a requesting cache and a cache data owner can use this signal to prevent the next transaction from overwriting the reflective data path inside the controller.

This output may also be programmed to include the empty status of the FIFOs. $\overline{BR/FE}$ will then be asserted if either the reflective FIFO or the normal write FIFO are not empty. This output may be used by systems that assess the availability of the controller before the data phase is initiated and pause until the controller becomes available.

$\overline{BG}$ – Bus Grant. This signal is asserted by the external arbiter in response to a $\overline{BR}$, to indicate that the controller has been granted ownership of the bus.

$\overline{BB}$ – Bus Busy. This signal is asserted by the controller for the duration of its bus ownership. The controller will acquire the bus as it completes the main memory write transaction during reflective read operations. When Bus Arbitration is disabled, this bidirectional pin may be used as an output to report read status. When the controller module begins a read operation, $\overline{BB}$ will be asserted indicating that the host can expect data in several clock cycles (actual number of clock cycles depends on programmed DRAM timings).

Table 21. ID[3:0] in Generic Mode

ID3	ID2	ID1	ID0	DRAM Mode Selection
0	0	X	X	Not Selected
0	1	0	0	Not Selected
0	1	0	1	I/O Registers
0	1	1	0	Indirect Address Register
0	1	1	1	Not Selected
1	X	X	X	Memory

ID[3:0] – Identification. The Identification bits are synchronous inputs recognized during the address phase. The ID bits are used in conjunction with address signals to define the nature of the bus

transaction and select I/O registers or DRAM memory. For MBus operation refer to *Table 39*. For the generic mode a match is required between ID[3:0] and the fixed values shown in *Table 21*.

CLK – Clock. CLK synchronizes all bus transactions. All transactions are strobed in at the rising edge of clock.

MCLK – Multiple Clock. MCLK may be used to supply a higher-frequency DRAM clock in lieu of using the internal PLLs. MCLK must be an integer multiple of CLK (either 1, 2, 3, or 4). When using the PLLs, MCLK must be tied to CLK.

$\overline{INT}$ – Interrupt. This signal indicates that the module has a pending interrupt that requires service. This output remains asserted until the interrupting condition is cleared.

$\overline{IMD}$ – Interface Mode. When tied LOW, the controller operates in the MBus mode. When tied HIGH, the controller operates in the generic mode.

Pin Description

Table 22 through *Table 25* summarize the functional pin connections of the controller module. Power and ground connections are not listed.

Table 22. Pin Descriptions

Signal Name	I/O	Description
D[63:0]	I/O	System Data Bus: These lines are used to transfer data to and from the DRAM Module. These lines are normally three-stated except when a valid read cycle is in progress.
DP[7:0]	I/O	Data Bus Parity: These signals follow the direction of the data bus. When the device is driving the data bus (read), data parity is generated and supplied to these pins. When data is entering the device, data parity is checked.
PMD[2:0]	I	Parity Mode: These inputs specify the parity mode for data and address.
A[35:0]	I	System Address Bus: These lines are used to transfer the address to the DRAM module.
AP[3:0]	I	Address Bus Parity: These inputs are examined for address integrity during accesses to the device.
$\overline{AS}$	I	Address Strobe: This input is used to indicate that the bus address and control signals are valid. It is used to enable clocking of the address and control information into the controller.
$\overline{DS}$	I	Data Strobe: This input is used to indicate that the data transaction is to take place.
$\overline{BLST}$	I	Burst Last: This input can be used to terminate a transaction.
$\overline{BACK}$[1:0]	I/O	Bus Acknowledge: These acknowledge signals output the transaction response back to the bus master. During reflective reads, these signals are inputs. During Reset, act as inputs and are used to invoke certain modes.
$\overline{UERR}$	I/O	Uncorrectable Error: This interrupt signal reports an unrecoverable error condition during a read. During reset it acts as an input to select Snoop Window source.
$\overline{RSTIN}$	I	Master Reset: Activating this input causes the module to set all control and status bits to their reset state.
CLK	I	System Bus Clock: This clock is used to synchronize the controller's operation to the system bus clock.
$\overline{BERR}$	O	Bus Error (Three-State): Indicates that a parity error has occurred on the bus. $\overline{BERR}$ is asynchronous.
$\overline{INH}$	I	Inhibit is used to abort read and write operations.
$\overline{SNW}$	I	Snoop Window: Defines the time in which Inhibit can be asserted.
$\overline{TRC}$	I	Transform Cycle: This input reverses the sense of inhibited operations.
TYPE[5:0]	I	Transaction Type: These inputs determine the transaction type.
SIZE[7:0]	I	Transaction Size: These inputs indicate the size of the transaction.
$\overline{INT}$	O	Interrupt (Three-State): This output indicates that an interrupt request is pending.
ID[3:0]	I	Identification: Selects memory or internal registers; positions the module in the address space.
$\overline{BR/FE}$	O	Bus Request/FIFO Empty: Reflects the status of the reflective or write FIFOs.
$\overline{BG}$	I	Bus Grant.
$\overline{BB}$	I/O	Bus Busy: Used to assert bus ownership or to indicate the beginning of a read operation.
ADRS[11:0]	O	DRAM row/column multiplexed address.
R/$\overline{W}$[3:0]	O	DRAM read/write control; one output per bank. (CYM7232 only)
R/$\overline{W}$[1:0]	O	DRAM read/write control; one output per bank. (CYM7264 only)
$\overline{RAS}$[3:0]	O	DRAM row address strobe; one per block.
$\overline{CAS}$[3:0]	O	DRAM column address strobe; one per block.

Table 23. Special Function Signals

Signal Name	I/O	Description
TSTE	I	Test Enable: This input must be set to 1 for proper operation.
TSTM	I	Test Mode.
TST[2:0]	O	Test Outputs.
MCLK	I	Multiple Frequency Clock: Optional input if internal PLLs are not used.
IMD	I	MBus/generic interface mode select.

Table 24. DRAM Data Signals (CYM7232)

Signal Name	I/O	Description
DDA[31:0]	I/O	DRAM data bus interface, Bank 0
EDA[6:0]	I/O	DRAM error check bit bus interface, Bank 0
DDB[31:0]	I/O	DRAM data bus interface, Bank 1
EDB[6:0]	I/O	DRAM error check bit bus interface, Bank 1
DDC[31:0]	I/O	DRAM data bus interface, Bank 2
EDC[6:0]	I/O	DRAM error check bit bus interface, Bank 2
DDD[31:0]	I/O	DRAM data bus interface, Bank 3
EDD[6:0]	I/O	DRAM error check bit bus interface, Bank 3

Table 25. DRAM Data Signals (CYM7264)

Signal Name	I/O	Description
DDA[63:0]	I/O	DRAM data bus interface, Bank 0
EDA[7:0]	I/O	DRAM error check bit bus interface, Bank 0
DDB[63:0]	I/O	DRAM data bus interface, Bank 1
EDB[7:0]	I/O	DRAM error check bit bus interface, Bank 1

Power and Ground Connections

There are two sets of power and ground connections. One set is for the logic and I/O circuitry and is indicated by V_{SS} and V_{DD} in the pin diagram. All V_{SS} pins should be connected to ground and all V_{DD} pins should be connected to the +5 volt supply. There are separate supply connections for the internal phase lock loops. V_{DDL} is the +5 volt supply connection and V_{SSL} is the ground connection for the phase lock loops. For superior noise immunity, V_{SSL} and V_{DDL} should be connected with independent pcb routing. These connections should run to the power supply where it connects to the circuit board on which the controller module resides.

The pinout lists several no connect (NC) pins. These connections should be left open. They may be used in future versions of the controller. IMD should be tied HIGH to invoke the generic bus interface mode or LOW for MBus mode. TSTE must be held HIGH.

32-Bit System Bus Connection

The 32-bit EDC version of the controller (CYM7232) may be connected to a 32-bit system data bus. This is accomplished by tying D0 to D32, D1 to D33 and so forth. The SBS field in the Command register must also be programmed with 0 to invoke the 32-bit system bus mode forcing the controller to multiplex read data onto the system bus and demultiplex write data from the system bus. The controller may be further connected for a multiplexed address/data bus by tying A[31:0] to D[31:0].

If the system bus employs bus parity, then DP0 should be tied to DP4, DP1 tied to DP5 and so forth forming a four-bit parity nibble for the 32-bit system bus.

64-Bit System Bus Connection

The 64-bit EDC version of the controller may only be connected to 64 bit bus systems. Address and data may be multiplexed, as in the 32 bit case, by connecting the module's address bus to a portion of its data bus. Address parity and data parity may also be shared, by connecting the module's address parity bus bits to a portion of its data parity bus.

Internal Registers

Several internal registers are available to set-up the controller and report status to the host. Each register is spaced 16 bytes apart in the address space so that its contents will be accessible on D[7:0] of the data bus regardless of system bus width or orientation (little/big endian). The EDC registers are accessed as 32-bit registers. An internal 8-bit indirect address register is provided to point to the individual I/O locations inside the controller. A register map is provided in *Table 26.*

Table 26. Register Map

Index	Name	R/W	7	6	5	4	3	2	1	0
00 H	Command Register 0	R/W	CIE	RFD						
01 H	Command Register 1	R/W	INIT	WC	AEM	SBS	ES	CLM		RFT
02 H	Command Register 2	R/W	BLP				BLK		DFB	
03 H	Command Register 3	R/W	RCM		BAM		SEN	CAM	RSM	BRM
04 H	Command Register 4	R/W	PLT		VCO		IOSWC			
05 H	Command Register 5	R/W	IE		EDP	EAP	EME	EUE	EDE	ESE
06 H	Command Register 6	R/W	SNWWRCNT				SNWRD CNT			
07 H	Reserved									
08 H	DRAM Timing 0	R/W	RAM				AR			
09 H	DRAM Timing 1	R/W	RAS				MAC			
0A H	DRAM Timing 2	R/W	CP				RPR			
0B H	DRAM Timing 3	R/W	RIN				DC			
0C H	DRAM Timing 4	R/W	ENW				ENR			
0D H	Reserved									
0E H	Reserved									
0FH	Reserved									
10 H	Base Address [7:0]	R/W	BA[27:20]							
11 H	Base Address [15:8]	R/W	BA[35:28]							
12 H	Logical Block Displacement [7:0]	R/W	Reserved		DS2		DS1			
13 H	Logical Block Displacement [15:8]	R/W	Reserved				DS3			
14 H	Reserved									
15 H	Reserved									
16 H	Reserved									
17 H	Reserved									

Table 26. Register Map (continued)

Index	Name	R/W	7	6	5	4	3	2	1	0
18 H	Logical Block Population Code [7:0]	R/W	LPC3		LPC2		LPC1		LPC0	
19 H	Logical Block Population Code [15:8]	R/W	Reserved				LBP3	LBP2	LBP1	LBP0
1A H	Physical/Logical Map [7:0]	R/W	PBL3		PBL2		PBL1		PBL0	
1B H	Reserved									
1C H	Logical Block Mux Position [7:0]	R/W	Reserved		LBMP1			LBMP0		
1D H	Logical Block Mux Position [15:8]	R/W	Reserved		LBMP3			LBMP2		
1E H	Reserved									
1F H	Reserved									
20 H	Error Location Address [7:0]	R	ELA[7:0]							
21 H	Error Location Address [15:8]	R	ELA[15:8]							
22 H	Error Location Address [23:16]	R	ELA[23:16]		ELA[23:16]					
23 H	Error Location Address [31:24]	R	ELA[31:24]							
24 H	EDC Register 0	R	See Section on Error Status Registers							
25 H	EDC Register 1	R								
26 H	Reserved									
27 H	Reserved									
28 H	Syndrome FIFO Flags 0	R								
29 H	Syndrome FIFO Flags 1	R								
2A H	Reserved									
2B H	Reserved									
2C H	Diagnostic Check Bit 0	W								
2D H	Diagnostic Check Bit 1	W								
2E H	Reserved									
2F H	Reserved									
30 H	Silicon Revision	R	Reserved				REV[3:0]			
31 H	Bus Error	W							BEM	BEC
32 H	Interrupt Status Register	R/W		IC	DBE	ABE	MEW	UEW	DEW	SBW

Index Register

IA[7:0] – Index Address. This register's contents points to all other registers inside the controller. During access to the controller's internal byte wide I/O path, little-endian processors should apply an address with A[3:0] = 0 to enable data onto D[7:0] on their system bus. Big-endian processors should apply an address with their A[3:0] = F to enable data onto D[7:0] on their system bus. Access to the internal registers is controlled through the ID bits. For ID3 equal to 1, all accesses occur to memory. For ID3 equal to 0, access is to the internal registers: with ID[2:0] equal to 110, transactions are directed to the Index register, with ID[2:0] equal to 101, transactions are directed to the register pointed to by the Index register. For all other combinations of the ID input, the controller is not selected. ID3 functions as the Memory/IO select and the remaining ID inputs function as selects or chip enables.

This register is not used in MBus mode. See MBus section for details on writing and reading I/O registers.

Command Registers – Write / Read

Command Register 0

Index	7	6	5	4	3	2	1	0
00 H	CIE	RFD						
Default	0	7F (h)						

CIE – Coherent Invalidate Acknowledge Enable. When this bit is set HIGH it enables acknowledges to MBus Coherent Invalidate cycles. BACK[1:0] are generated two clocks after the address phase in which the TYPE bits specify this cycle. Systems requiring different acknowledge delays should set CIE = 0 and use an external PLD to generate the acknowledge. This bit should be set to 0 when in the Generic Mode.

RFD – Refresh Counter Divisor. These bits divide CLK down to 1 MHz. The output of this counter is further divided by a fixed divide "by 15" counter, which produces the 15 microsecond refresh requests. The division factor is the load value plus 1. For example, the divisor load values in decimal for the various bus clock frequencies are:

24	25 MHz
32	33 MHz
39	40 MHz
49	50 MHz

Command Register 1

Index	7	6	5	4	3	2	1	0
01 H	INIT	WC	AEM	SBS	ES	CLM[1:0]		RFT
Default	0	0	0	0	0	0		0

INIT – Initialization. This bit, when set, triggers an initialization of the DRAM memory and its check bits. The contents of the memory are set to zero and the corresponding check bits are set.

WC – Write Check Bits. Enables writing of the EDC check bits from the registers inside the data path.

0	Write EDC check word computed from incoming data.
1	Write EDC check word from check bit register.

AEM – Address Error Mode. Controls assertion of $\overline{\text{BERR}}$ after an address parity error.

0	$\overline{\text{BERR}}$ asserted for one clock
1	$\overline{\text{BERR}}$ asserted until cleared by writing 1 to ABE in Interrupt Status register

SBS – System Bus Size. Specifies the number of data bits in the system bus.

0	32 Bits
1	64 Bits

ES – EDC Size. Specifies the number of data bits in each EDC packet.

0	32 Bits
1	64 Bits

CLM – Clock Multiplier. These bits program the multiplication factor from the incoming bus clock (CLK) to the internal DRAM timing clock. They are defined as follows:

CLM[1:0]	Clock Multiplier
00	X1
01	X2
10	X3
11	X4

RFT – Refresh Test Mode. This bit must be clear for proper operation.

Command Register 2

Index	7	6	5	4	3	2	1	0
02 H	BLP[3:0]				BLK		DFB	
Default	0				0		0	

BLP – Block Population. These bits define which physical blocks are populated. BLP[N] = 1 indicates that Block N is populated. Block population must be contiguous with one exception. BLP0 and BLP2 can be asserted simultaneously with BLP1 and BLP3 deasserted simultaneously when supporting 36- and 40-bit SIMMS populated with two sections of DRAM memory.

BLK – Number of Blocks. These bits specify the total number of populated blocks. 0 (H) = 1 block ... 3 (H) = 4 blocks.

DFB – Default Burst Length. This field defines the default burst length for cache line read/writes. The bus will execute burst transactions with this default length when the appropriate TYPE bit is asserted during the address phase of a transaction or when an operation is transformed. These bits are interpreted as follows:

DFB[1:0]	Default Burst Length
00	16 Bytes
01	32 Bytes
10	64 Bytes
11	128 Bytes

Command Register 3

Index	7	6	5	4	3	2	1	0
03 H	RCM[1:0]		BAM[1:0]		SEN	CAM	RSM	BRM
Default	0		0		0	0	0	0

RCM – Refresh Control Modes. These bits control refresh and the DRAM INIT process for test purposes. RCM must be set to 11 for proper operation. When asserted, RCM[0] enables refresh and RCM[1] enables the INIT process. (The INIT process occurs after DRAM energizing and fills all DRAM with 0.)

Index Register (continued)

BAM[1:0] – Bus Acknowledge Modes. These bits control the operating modes for read operations. BAM0 controls error correction. BAM1 controls the insertion of wait states.

BAM0 – Error Correction Enable

0 Error correction disabled

1 Error correction enabled

When error correction is disabled, reads as a result of Read Modify Write operations are not affected. Consequently, single-bit errors in the read portion of RMW cycles are corrected and merged with the write data. Uncorrectable errors cause the write back portion of RMW cycles to abort. Read Modify Write transactions are not possible in systems configured without DRAM check bits.

BAM1 – Wait State Insertion on Reads

0 No wait states inserted

1 Wait states inserted

The insertion of wait states allows corrected data to meet minimum set-up requirements in high-speed systems. Wait states should be inserted for systems requiring greater system bus set-up time on reads.

SEN – Scrub Enable. This bit enables scrubbing when asserted HIGH.

CAM – $\overline{CAS}$ Assertion Mode

0 $\overline{CAS}$[3:0] independently asserted.

1 $\overline{CAS}$[3:2] "ORed" to produce $\overline{CAS}$2, $\overline{CAS}$[1:0] "ORed" to produce $\overline{CAS}$0. This mode is provided to support some 36- or 40-bit-wide DRAM SIMMs that contain two rows of memory with independent $\overline{RAS}$ and common $\overline{CAS}$.

RSM – $\overline{RAS}$ Stagger Mode (during Refresh/Scrub operations).

0 $\overline{RAS}$[3:0] staggered by one bus clock.

1 $\overline{RAS}$[3:0] staggered to be non-overlapping (mutually exclusive in time). This mode is provided to support some 36- or 40-bit-wide DRAM SIMMs that contain two rows of memory with independent $\overline{RAS}$ and common $\overline{CAS}$. The $\overline{RAS}$ signals must be mutually exclusive when scrubbing these SIMMs.

BRM – Bus Request Mode

0 Bus arbiter ON. $\overline{BR/FE}$ assertion indicates reflective FIFO status only. With bus arbiter ON, $\overline{BR/FE}$ is deasserted with the recognition of Bus Grant ($\overline{BG}$) and Bus Busy ($\overline{BB}$) is asserted after the $\overline{BB}$ pin goes HIGH.

1 Bus arbiter OFF. $\overline{BR/FE}$ assertion combines write FIFO status and reflective FIFO status (logical OR). Both FIFOs must be empty for the $\overline{BR/FE}$ output to be deasserted. With the bus arbiter OFF, $\overline{BG}$ is ignored, the $\overline{BR/FE}$ output simply reflects the combined FIFO status, and $\overline{BB}$ acts as an output signaling the beginning of a read transaction.

Command Register 4

Index	7	6	5	4	3	2	1	0
04 H	PLT[1:0]		VCO[1:0]		IOSWC			
Default	O(h)		O(h)		F(h)			

PLT[1:0] – Phase-Locked Loop Test. This field is for test purposes only. PLT[1:0] should be programmed to 11 when enabling the internal VCOs, otherwise PLT[1:0] = 00.

VCO[1:0] – Voltage Controlled Oscillation Select. This field selects the appropriate VCO for generating the internal multiplied clock.

00 No VCO selected, use external MCLK
01 70-MHz VCO
10 80-MHz VCO
11 100-MHz VCO

The operating range of the VCOs is given in the following table. Each VCO requires a minimum of 20 ms to phase lock to the system bus clock after being enabled.

VCO (MHz)	Operating Range (MHz)
70	65 – 74.9
80	75 – 84.9
100	95 – 104.9

IOSWC – Snoop Window Count. This value programs the duration of the snoop window for I/O operations in bus clock cycles. The snoop window counter is enabled one clock after an address phase on the bus in which the controller is selected. When a 0 is programmed into the counter the snoop window closes immediately (i.e., the cycle after the address phase). The window can be extended up to 16 clocks after the address phase appears on the bus. After power-up the counter defaults to the maximum value. The internal snoop window is selected by driving $\overline{UERR}$ appropriately during reset.

Command Register 5

Index	7	6	5	4	3	2	1	0
05 H	IE	—	EDP	EAP	EME	EUE	EDE	ESE
Default	0	0	0	0	0	0	0	0

IE – Interrupt Enable. This bit must be set to enable interrupts to the system bus.

EDP – Enable Data Bus Parity Interrupt. Enables the interrupt indicating that one of the data bytes has a parity error.

EAP – Enable Address Bus Parity Interrupt. Enables the interrupt indicating that one of the address bytes has a parity error.

EME – Enable Read-Modify-Write Multiple Error Interrupt. Enables the interrupt indicating that a multiple error has occurred on a read-modify-write cycle.

EUE – Enable Uncorrectable Error in Word Interrupt. Enables the interrupt indicating that an uncorrectable error has occurred in a word.

EDE – Enable Double Bit Error in Word Interrupt. Enables the interrupt indicating that a double bit error has occurred in a 32- (64-) bit word.

ESE – Enable Single Bit Error Interrupt. Enables the interrupt indicating that a single bit correctable error has occurred in a 32- (64-) bit word.

Command Register 6

Index	7	6	5	4	3	2	1	0
06 H	SNWWRCNT[3:0]				SNWRDCNT[3:0]			
Default	F(h)				F(h)			

Index Register (continued)

SNWWRCNT specifies the snoop window duration for memory-write transactions and SNWRDCNT specifies the snoop window duration for memory-read transactions. The internal snoop window is used only if selected by driving $\overline{UERR}$ appropriately during reset. The snoop window counter is enabled one clock after an address phase on the bus in which the controller is selected. When a 0 is programmed into the counter, the snoop window closes immediately (e.g., the cycle after the address phase). the window can be extended up to 16 clocks after the address phase appears on the bus. After reset, the counter defaults to the maximum value.

DRAM Timing Program Registers – Write / Read

DRAM Timing Register 0

Index	7	6	5	4	3	2	1	0
08 H	RAM[3:0]				AR[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 1

Index	7	6	5	4	3	2	1	0
09 H	RAS[3:0]				MAC[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 2

Index	7	6	5	4	3	2	1	0
0A H	CP[3:0]				RPR[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 3

Index	7	6	5	4	3	2	1	0
0B H	RIN[3:0]				DC[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 4

Index	7	6	5	4	3	2	1	0
0C H	ENW[3:0]				ENR[3:0]			
Default	F(h)				F(h)			

The DRAM Timing Program registers should not be reprogrammed during operation. The user must reset the part and reprogram all DRAM timing before issuing an INIT.

For optimum performance, DC[3:0] should always be programmed to 0001(b). RIN[3:0] = RAS[3:0] – (RAM[3:0] + MAC[3:0]).

All timing values are set with 4-bit values. The time intervals are specified to 10-ns accuracy when the internal clock is running at 100 MHz, 12.5-ns accuracy when the internal clock is running at 80 MHz, 13.3-ns accuracy when the internal clock is running at 75 MHz, or 15.2-ns accuracy when the internal clock is running at 66 MHz. Refer to the timing diagrams for elaboration.

Table 27. DRAM Timing Values

Hex Value	Delay/Width (ns)			
	66 MHz	75 MHz	80 MHz	100 MHz
0	15.2	13.3	12.5	10
1	30.3	26.6	25	20
2	45.5	40	37.5	30
3	60.7	53.3	50	40
4	80	66.6	62.5	50
5	91	80	75	60
6	106	93.3	87.5	70
7	121	106.6	100	80
8	136	120	112.5	90
9	152	133.3	125	100
A	167	146.6	137.5	110
B	182	160	150	120
C	197	173.3	162.5	130
D	212	186.6	175	140
E	227	200	187.5	150
F	242	213.3	200	160

Table 28. DRAM Timing Program[1]

Parameter	Field Name	Description
t_{RAM}	RAM	$\overline{RAS}$ to multiplexed address
t_{AR}	AR	Address to $\overline{RAS}$ assertion
t_{RAS}	RAS	$\overline{RAS}$ pulse width
t_{MAC}	MAC	Multiplexed address to $\overline{CAS}$
t_{CP}	CP	$\overline{CAS}$ pre-charge width
t_{RPR}	RPR	$\overline{RAS}$ pre-charge width
t_{RIN}	RIN	$\overline{RAS}$ completion during non-reflective Inhibit
t_{DC}	DC	FIFO data delay to $\overline{CAS}$
t_{ENR}	ENR	Enable delay on read
t_{ENW}	ENW	Enable delay on write
t_{ACC}	—	DRAM access time (determine by DRAM chips)
t_{CLZ}	—	DRAM $\overline{CAS}$ to Output Low Z (determined by DRAM chips)
t_{CY}	—	Bus CLK period

Note:

1. All timings may be resolved to 1/n of t_{CY}, where n is the phase locked loop multiplier (e.g. 50-MHz systems having a PLL multiplier of 2 with t_{CY} = 20 ns can have DRAM timing resolutions defined to 10 ns). Therefore, unless the timing values are constrained, the DRAM read data could arrive at the data path input pipeline on a 10-ns boundary rather than a bus clock boundary. The controller will automatically extend certain values that are programmed to provide data on a bus clock boundary, whenever necessary.

DRAM Block Assignment Register Array

Five registers are used to map the incoming address to the four physical blocks of DRAM. These registers specify the Base address of the DRAM array, the gaps between blocks, the relationship between physical blocks and logical blocks, the size of memory each block is populated with, and the RAS/CAS address split point in the DRAMs in each block. The module should be re-initialized when any of these registers are changed during operation.

The Base Address register, Logical Block Displacement register, Logical Block Population Code register, and Logical Block MUX Position register are all 2-byte registers. The Physical/Logical Block Map register is a 1-byte register.

Base Address Register

Byte Address 10H, BA[27:20] (Bits 7:0)
Byte Address 11H, BA[35:28] (Bits 15:8)

15 8 7 0

	BA0[35:28]	BA0[27:20]
Default	00 H	00 H

BA[35:20] – Base Address of Memory. This entry specifies the base address of the memory. The base address must be evenly divisible by the depth of the largest DRAM device used multiplied by 16. For example, if the largest DRAM device used is 1M deep, then the smallest base address (other than 0) is BA = 0010 (h); BA[23:20] must be 0.

Logical Block Displacement Register

Byte Address 12H, LBD[7:0]
Byte Address 13H, LBD[15:8]

15 11 10 8 7 6 5 3 2 0

	Reserved	DS(3)[2:0]	Reserved	DS(2)[2:0]	DS(1)[2:0]
Default	0 H	0 H	0 H	0 H	0 H

DS(N)[2:0] – Address Displacement of logical block (N). This entry specifies the address displacement of logical block (N) from logical block (N – 1). The starting address of logical block (0) is the Base address of the memory. The starting address of logical block (1) is the sum of the Base address and the displacement selected by DS(1). The starting address of logical block (2) is the sum of the starting address of logical block (1) and the displacement selected by DS(2). The starting address of logical block (3) is the sum of the starting address of logical block (2) and the displacement selected by DS(3). The programmed displacement, DS(N), must be equal to or greater than the depth of the memory chips contained in logical block N–1. When the programmed displacement is equal to the memory chips depth, the memory is contiguous.

DS(N)[2:0]	Displacement
000	256K
001	1M
010	4M
011	16M
100	32M
101	64M
110	128M
111	256M

Logical Block Population Code Register
Byte Address 18H, LPCR[7:0]
Byte Address 19H, LPCR[15:8]

	7	6	5	4	3	2	1	0
	LPC3[1:0]			LPC2[1:0]		LPC1[1:0]		LPC0[1:0]
Default	00 H							

	15	12	11	10	9	8
	Reserved		LBP3	LBP2	LBP1	LBP0
Default	00 H					

LPC(N)[1:0] – Logical Block Population Code. LPC(N)[1:0] specifies the DRAM type in logical block (N).

LPC(N)[1:0]	DRAM Depth
11	16M
10	4M
01	1M
00	256K

The physical blocks may be configured in any order. To obtain a contiguous memory with no overlaps or gaps, the logical blocks must be populated in order with the largest DRAM type in logical block 0, followed by the next largest DRAM type in logical block 1, etc., and the logical block populations must be contiguous (no unpopulated logical blocks between populated blocks).

LBP(N) specifies whether or not the block is populated. LBP(N) = 0 block not populated. LBP(N) = 1 block populated.

Physical/Logical Block Map Register
Byte Address 1AH, PBLR[7:0]

	7	6	5	4	3	2	1	0
	PBL3[1:0]			PBL2[1:0]		PBL1[1:0]		PBL0[1:0]
Default	00 H							

PBL(N)[1:0] – Physical Block Association. PBL(N)[1:0] specifies the logical block to which physical block N is mapped.

PBL(N)[1:0]	Association
00	Logical Block 0
01	Logical Block 1
10	Logical Block 2
11	Logical Block 3

Logical Block MUX Position Register
Byte Address 1CH, MPR[7:0]
Byte Address 1DH, MPR[15:8]

	7	6	5	3	2	0
	Reserved		LBMP1[2:0]		LBMP0[2:0]	
Default	00 H					

	15	14	13	11	10	8
	Reserved		LBMP3[2:0]		LBMP2[2:0]	
Default	00 H					

LBMP(N)[2:0] specifies the DRAM column address/row address split for logical block (N). The split is specified in terms of the address applied to the DRAM. Note that bus address 4 is DRAM column address 0. All twelve DRAM address bits are valid for all split selections.

LBMP(N)[2:0]	Row/Column Address Split Location
000	8/7
001	9/8
010	10/9
011	11/10
100	12/11
101	unused
110	unused
111	unused

Error Location Register – Read Only

The Error Location register is a 32 bit register that contains the address of the most recent error. This register is read only and is byte addressable only. All bytes appear on D[7:0]. Byte addresses are as follows:

20H ELA[7:0]
21H ELA[15:8]
22H ELA[23:16]
23H ELA[31:24]

Error Location Address [31:0]

	31	0
	ELA[31:0]	
Default	00 H	

The Error Location Address register reports the address location of an error in the DRAM and how the error occurred. When the error ocurs during a read operation the ELA register reports the address as it appeared on the system bus and the physical block wherer the system bus address is mapped. When the error occurs during a refresh, or scrub, operation the ELA reports the physical block and address in row/column format.

Read Error Location Register Format

ELA[31:30] Physical Block in DRAM
ELA[29:28] 00 (Reports Read Error)
ELA[27:4] System Bus Address A[27:4]
ELA[3:0] 0

Refresh/Scrub Error Location Register Format

ELA[31:30] Physical Block in DRAM
ELA[29:28] 01 (Reports Ref. Error)
ELA[27:16] DRAM Row Address
ELA[15:4] DRAM Column Address
ELA[3:0] 0

After a system bus read error, diagnostic software will translate the system bus address to the row/column address inside the DRAM. This mapping will depend on the DRAM configuration.

When the error occurs during refresh, or scrub, diagnostic software will extract the meaningful portion of the row/column address (from the reported row/column address) based on the DRAM population of the particular physical block in error. The

Error Location Register – Read Only (continued)

DRAM array is always refreshed as if populated with 16-Megabit DRAMs in all blocks. Therefore higher order row and column address bits in the internal refresh counter will increment even when they are not required to span the address space within a block. These redundant bits must be ignored in calculating the location of an error which occurred during refresh.

The ELA register is constantly updated with the address of the current transaction. If an error is detected in the read from DRAM, further writing to this register is locked out until the interrupt bit is cleared. (If two successive transactions incur errors and the interrupt bit is not cleared before the address phase of the second transaction, the address of the second error is lost.)

Error Status Registers – CYM7232

The Error Status registers provide information on errors that have occurred during any read operation (including scrubbing and read modify write). The location of these registers on the data bus will depend on the system bus configuration (32 or 64 bits). *Table 29* shows the location of data path registers for the 64-bit system bus.*Table 30* shows the location of the same registers in the 32-bit system bus application.

Table 29. Error Status Register Map for CYM7232 with 64-Bit System Bus

Index	Name	R/W	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R					CB2	CB0	SYN2	SYN0
25 H	EDC Register 1	R	CB3	CB1	SYN3	SYN1				
26 H	Reserved									
27 H	Reserved									
28 H	Syndrome FIFO Flags 0	R								FL0
29 H	Syndrome FIFO Flags 1	R				FL1				
2A H	Reserved									
2B H	Reserved									
2C H	Diagnostic Check Bit 0	W								DCB0
2D H	Diagnostic Check Bit 1	W				DCB1				
2E H	Reserved									
2F H	Reserved									

Table 30. Error Status Register Map for CYM7232 with 32-Bit System Bus

Index	Name	R/W	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R	CB2	CB0	SYN2	SYN0
25 H	EDC Register 1	R	CB3	CB1	SYN3	SYN1
26 H	Reserved					
27 H	Reserved					
28 H	Syndrome FIFO Flags 0	R				FL0
29 H	Syndrome FIFO Flags 1	R				FL1
2A H	Reserved					
2B H	Reserved					
2C H	Diagnostic Check Bit 0	W				DCB0
2D H	Diagnostic Check Bit 1	W				DCB1
2E H	Reserved					
2F H	Reserved					

EDC Registers

The EDC Registers contain the Read Error Log FIFO and Check Bits fields. The registers are Read Only. The register at address 24 appears on D[31:0] and the register at address 25 appears on D[63:32] when the module is connected a 64 bit system bus. For 32 bit systems, both registers appear on D[31:0].

EDC Register 0

Index	31	30	24	23	22	16	15	14	8	7	6	0
24 H		CB2			CB0			SYN2			SYN0	
Default		00 H			00 H			Undefined			Undefined	

EDC Register 1

Index	31	30	24	23	22	16	15	14	8	7	6	0
25 H		CB3			CB1			SYN3			SYN1	
Default		00 H			00 H			Undefined			Undefined	

This register will appear on D[63:32] of the 64-bit system bus. When used in a 32-bit system bus application, this register will appear on D[31:0].

SYN0, SYN1, SYN2, SYN3 – Syndrome Bits. These bits originate from the outputs of the syndrome FIFO. They reflect the EDC syndrome bits on any memory read error condition (including reads, read bursts, scrubs, and read modify writes). The syndrome outputs contain valid information whenever the FIFO Flag register's corresponding status bits indicate that the FIFOs are not empty. SYN0 contains the syndrome values for errors in DRAM Bank 0. SYN1 contains the syndrome values for errors in DRAM Bank 1, and so forth.

CB0, CB1, CB2, CB3 – Check Bits. These bits reflect the EDC check bits that were present during the previous read operation. CB0 contains the check bits from DRAM Bank 0 for the most recent read. CB1 contains the check bits from DRAM Bank1 for the most recent read and so forth.

Syndrome FIFO Flag Registers

The Syndrome FIFO Flag registers contain the full/empty status of the syndrome FIFOs. The registers are read only (byte addressable only). When the module is used in a 64-bit bus system the register at address 28 appears on D[7:0] and the register at address 29 appears on D[39:32]. In 32-bit system bus operation the register at address 29 will appear on D[7:0].

Syndrome FIFO flag register 0 (32- & 64-bit system bus)

Index	7	6	5	4	3	2	1	0
28H	Reserved				FSF2	ESF2	FSF0	ESF0
Default	00 H				0	1	0	1

Syndrome FIFO flag register 1 (64-bit system bus)

Index	39	38	37	36	35	34	33	32
29H	Reserved				FSF3	ESF3	FSF1	ESF1
Default	00 H				0	1	0	1

Syndrome FIFO flag register 1 (32-bit system bus)

Index	7	6	5	4	3	2	1	0
29H	Reserved				FSF3	ESF3	FSF1	ESF1
Default	00 H				0	1	0	1

ESF0, ESF1, ESF2, ESF3 – Syndrome FIFO Empty Flags. These bits reflect the EDC syndrome FIFO empty status. When set to 1, these bits indicate that the associated FIFO is empty. ESF0 reflects the status of FIFO 0 which stores the syndrome values from DRAM Bank 0. ESF1 reflects the status of FIFO 1 which stores the syndrome values form DRAM Bank 1 and so forth.

FSF0, FSF1, FSF2, FSF3 – Syndrome FIFO Full Flags. These bits reflect the EDC syndrome FIFO full status. When set to 1, these bits indicate that the associated FIFO is full. FSF0 reflects the status of FIFO 0, which stores the syndrome values form DRAM Bank 0. FSF1 reflects the status of FIFO 1, which stores the syndrome values from DRAM Bank 1 and so forth.

Diagnostic Check Bit Registers

Diagnostic Check Bit Register 0 (32- & 64-bit system bus)

Index	7	6	5	4	3	2	1	0
2C H	–	DCB0						
Default	–	00 H						

Diagnostic Check Bit Register 1 (64-bit system bus)

Index	39	38	37	36	35	34	33	32
2D H	–	DCB1						
Default	–	00 H						

Diagnostic Check Bit Register 1 (32-bit system bus)

Index	7	6	5	4	3	2	1	0
2D H	–	DCB1						
Default	–	00 H						

DCB0, DCB1: Check Bit Register – Write only. These bits can be written to override the check bits generated by the write polynomial generator. In a 64-bit system bus configuration, the register at address 2C appears on D[7:0] and the register at address 2D appears on D[39:32]. When used in a 32-bit system bus, the register at address 2D will appear on D[7:0]. Data written into Diagnostic Check Bit register 0 will write into the check bits for DRAM Banks 0 and 2. Data written into Diagnostic Check Bit register 1 will write into the check bits for DRAM Banks 1 and 3. The selection to use EDC computed from the write data or use the EDC as contained in this register is determined by bit WC in the Command register 1.

Error Status Registers – CYM7264

Table 31. Data Path Register Map for CYM7264

Index	Name	R/W	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R		CB0		SYN0
25 H	EDC Register 1	R		CB1		SYN1
26 H	Reserved					
27 H	Reserved					
28 H	Syndrome FIFO Flags 0	R				FL0
29 H	Syndrome FIFO Flags 1	R				FL1
2A H	Reserved					
2B H	Reserved					
2C H	Diagnostic Check Bit 0	W				DCB0
2D H	Diagnostic Check Bit 1	W				DCB1
2E H	Reserved					
2F H	Reserved					

EDC Registers

The EDC Registers contain the Read Error Log FIFO and Check Bits fields. The registers are Read Only. These registers will appear in D[31:0] of the system data bus as shown in *Table 31*.

EDC Register 0

Index	31	24	23	16	15	8	7	0
24 H			CB0				SYN0	
Default	Undefined		00 H		Undefined		Undefined	

EDC Register 1

Index	31	24	23	16	15	8	7	0
25 H			CB1				SYN1	
Default	Undefined		00 H		Undefined		Undefined	

SYN0, SYN1 – Syndrome Bits. These bits reflect the EDC syndrome bits on an error condition. SYN0 contains the syndrome values for errors in DRAM Bank 0. SYN1 contains the syndrome values for errors in DRAM Bank 1.

CB0, CB1 – Check Bits. These bits reflect the EDC check bits that were present during the previous read operation. CB0 contains the check bits read from DRAM Bank 0. CB1 contains the check bits read from DRAM Bank 1.

Syndrome FIFO Flag Registers

Syndrome FIFO Flag Register 0

Index	7	6	5	4	3	2	1	0
28 H	Reserved						FSF0	ESF0
Default	01 H						0	1

Syndrome FIFO Flag Register 1

Index	7	6	5	4	3	2	1	0
29 H	Reserved						FSF1	ESF1
Default	01 H						0	1

ESF0, ESF1 – Syndrome FIFO Empty Flags. These bits reflect the EDC syndrome FIFO Empty status. When set to 1, these bits indicate that the associated FIFO is empty. ESF0 is the flag for Syndrome FIFO 0 and ESF1 is the flag for Syndrome FIFO 1.

FSF0, FSF1 – Syndrome FIFO Full Flags. These bits reflect the EDC syndrome FIFO full status. When set to 1, these bits indicate that the associated FIFO is full. FSF0 is the flag for Syndrome FIFO 0 and FSF1 is the flag for Syndrome FIFO 1.

Diagnostic Check Bit Registers

Diagnostic Check Bit Register 0

Index	7	6	5	4	3	2	1	0
2C H	DCB0							
Default	00 H							

Diagnostic Check Bit Register 1

Index	7	6	5	4	3	2	1	0
2D H	DCB1							
Default	00 H							

DCB0, DCB1 – Check Bit Register. These bits can be written to override the check bits generated by the write polynomial register. Data in DCB0 is written to DRAM Bank 0 and data in DCB1 is written to DRAM Bank 1. The selection to use EDC computed from the write data or use the EDC as contained in this register is determined by bit WC in the Command register Byte 1.

Silicon Revision Code – Read Only

Index	7	6	5	4	3	2	1	0
30 H					REV[3:0]			

REV[3:0] – Silicon Revision. This field gives the revision number of the module's address controller chip.

$\overline{\text{BERR}}$ Control Register – Write Only

Index	7	6	5	4	3	2	1	0
31 H							BEM	BEC

This register controls operation of the $\overline{\text{BERR}}$ output for data parity errors.

BEM – Data Bus Error Mode. When BEM is set, $\overline{\text{BERR}}$ remains asserted till explicitly cleared (when reporting data parity errors). Otherwise $\overline{\text{BERR}}$ is asserted for one clock only.

BEC – Clear Data Bus Error. This bit, when asserted, clears $\overline{\text{BERR}}$ when MBE (above) is set.

There are two BERR registers in the CYM7232 and two in the CYM7264. These locations on the data bus depend on the bus configuration as follows:

CYM7232
- 32-Bit Bus mode – Registers programmed simultaneously at D[7:0]
- 64-Bit Bus mode – Registers located at D[39:32], D[7:0]

CYM7264
- 64-Bit Bus mode – Registers programmed simultaneously at D[7:0]

All registers appear at the same address, 31H.

Interrupt Status Register

Index	7	6	5	4	3	2	1	0
32 H	–	IC	DBE	ABE	MEW	UEW	DEW	SBW
Default	0	0	0	0	0	0	0	0

IC – Initialization Complete. This bit indicates initialization of the DRAM is complete.

DBE – Data Parity Error. This bit indicates that a data bus parity error has occurred over the system bus.

ABE – Address Parity Error. This bit indicates that an address bus parity error has occurred over the system bus.

MEW – Multiple Errors in a Read-Modify-Write. This bit indicates that multiple errors have occurred during a read-modify-write operation.

UEW – Uncorrectable Error in a Word. This bit indicates that an uncorrectable error has occurred in a 32- (64-) bit word.

DEW – Double Error in a Word. This bit indicates that a double bit error has occurred in a 32- (64-)bit word.

SBW – Single Correctable Error. This bit indicates that a single correctable error has occurred in a 32- (64-) bit word.

Interrupt Status register bits ISR[6:0] are latched. Interrupts[5:0] can be cleared individually by writing the register with the desired bit high. Otherwise those status bits remain indefinitely, or until $\overline{\text{RSTIN}}$ is asserted LOW.

Special Characteristics of I/O Registers

The two EDC registers can be accessed with 32-bit reads over the system bus. All other I/O registers must be accessed by reading or writing a single byte at the address location shown. That byte will always be located at the lowest 8 bits of the system's data bus (D[7:0]). Programming registers are read/write for diagnostic purposes. These register's address locations are separated by 16 bytes to support wide system data paths.

Syndrome Decoding

The following tables give the decoding for the syndrome values for the 32- and 64-bit error detection and correction algorithms. *Table 32* gives the syndrome decoding for the 32-bit error-detection and correction algorithm. *Table 33* gives the syndrome decoding for the 64 bit error detection and correction algorithm. In these two tables, U indicates a multiple (greater than 2) bit uncorrectable error, D indicates a double bit error, nm indicates an error in data bit nm, Cn indicates an error in check bit n, and N indicates no error.

Table 32. Syndrome Decoding, 32-bit EDC

S6 S5 S4 S[3:0]	**0 0 0**	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
0000	U	D	D	0	D	U	U	D
0001	D	U	U	D	U	D	D	16
0010	D	29	7	D	U	D	D	U
0011	U	D	D	U	D	13	23	D
0100	D	28	6	D	U	D	D	17
0101	U	D	D	1	D	12	22	D
0110	U	D	D	U	D	11	21	D
0111	D	27	5	D	U	D	D	C3
1000	D	26	4	D	U	D	D	U
1001	U	D	D	U	D	10	20	D
1010	31	D	D	U	D	9	19	D
1011	D	25	3	D	15	D	D	C2
1100	U	D	D	U	D	8	18	D
1101	D	24	2	D	U	D	D	C1
1110	D	U	U	D	14	D	D	C0
1111	30	D	D	C6	D	C5	C4	N

Table 33. Syndrome Decoding, 64-bit EDC

S7 S6 S5 S4 S[3:0]	**0 0 0 0**	**0 0 0 1**	**0 0 1 0**	**0 0 1 1**	**0 1 0 0**	**0 1 0 1**	**0 1 1 0**	**0 1 1 1**	**1 0 0 0**	**1 0 0 1**	**1 0 1 0**	**1 0 1 1**	**1 1 0 0**	**1 1 0 1**	**1 1 1 0**	**1 1 1 1**
0000	N	C4	C5	D	C6	D	D	62	C7	D	D	46	D	U	U	D
0001	C0	D	D	14	D	U	U	D	D	U	U	D	U	D	D	30
0010	C1	D	D	U	D	34	56	D	D	50	40	D	U	D	D	U
0011	D	18	8	D	U	D	D	U	U	D	D	U	D	2	24	D
0100	C2	D	D	15	D	35	57	D	D	51	41	D	U	D	D	31
0101	D	19	9	D	U	D	D	63	U	D	D	47	D	3	25	D
0110	D	20	10	D	U	D	D	U	U	D	D	U	D	4	26	D
0111	U	D	D	U	D	36	58	D	D	52	42	D	U	D	D	U
1000	C3	D	D	U	D	37	59	D	D	53	43	D	U	D	D	U
1001	D	21	11	D	U	D	D	U	U	D	D	U	D	5	27	D
1010	D	22	12	D	33	D	D	U	49	D	D	U	D	6	28	D
1011	17	D	D	U	D	38	60	D	D	54	44	D	1	D	D	U
1100	D	23	13	D	U	D	D	U	U	D	D	U	D	7	29	D
1101	U	D	D	U	D	39	61	D	D	55	45	D	U	D	D	U
1110	16	D	D	U	D	U	U	D	D	U	U	D	0	D	D	U
1111	D	U	U	D	32	D	D	U	48	D	D	U	D	U	U	D

MBus Operation

Bus Transactions General Description

System transactions follow the MBus specification January 31st, 1991, Revision 1.2 (Review draft) including Level 2. Only those functions required of a main memory system are implemented. The generic interface is an extension of the MBus specification adapted to a variety of processors. The descriptions of the generic interface are therefore applicable to MBus applications. The intent of this section is not to repeat the MBus specification but to identify those operating characteristics and functions which are invoked with the MBus mode selection.

Module Connections

The SPARC MBus is an address/data multiplexed bus therefore, the address and data pins of the module must be wired together. The controller accommodates the multiplexed bus by storing the address and control information that is presented during the address phase allowing the data on the address pins to change after the deassertion of the address strobe. The module connections to MBus are given in the following tables. Note that some module pins are tied together to the MBus connection. Other connections must be permanently tied to a HIGH or LOW level.

Table 34. MBus Signal Translation

Controller	MBus
CLK	CLK
D[63:0]	MAD[63:0]
A[35:0]	MAD[35:0]
TYPE[3:0]	MAD[39:36]
SIZE[2:0]	MAD[42:40]
$\overline{AS}$	$\overline{MAS}$
$\overline{BACK}$[1]	$\overline{MRDY}$
$\overline{INH}$	$\overline{MIH}$
$\overline{BR}$	$\overline{MBR}$
$\overline{BG}$	$\overline{MBG}$
$\overline{BB}$	$\overline{MBB}$
ID[3:0]	ID[3:0]
$\overline{BERR}$ (Optional)	$\overline{AERR}$
$\overline{RSTIN}$	$\overline{RSTIN}$
$\overline{INT}$	$\overline{INTOUT}$
$\overline{UERR}$	$\overline{MERR}$

Table 35. Extra Signals in MBus

Controller	MBus
IMD	0 (MBus mode)
TYPE[5:4]	0 (Ignored)
SIZE[7:3]	0
$\overline{DS}$	0
$\overline{BLST}$	1
TSTE	1
PMD[2:0]	(Optional)
$\overline{TRC}$	Tied high for non-reflective memory Tied to $\overline{INH}$ for reflective memory

During reset, $\overline{BACK}$[1:0] and $\overline{UERR}$ must be driven to invoke the proper MBus modes. The snoop window source can originate internally. To make these selections, $\overline{UERR}$ and $\overline{BACK}$[1:0] must be driven to binary 100 during Reset. Refer to *Table 18* and *Table 19*.

Bus Interface Signal Description

The bus interface signal descriptions are identical to that given in the generic descriptions except for some minor variations and nomenclature. This section will present only those differences and highlight the nomenclature equivalences.

Transaction Specific Control

Transaction specific control information is contained in fields within the address as specified by MBus. These fields are given in *Table 36.*

Table 36. Multiplexed Bus Address Subfields

Signal Name	Physical Signal	Description
A[35:0]	MAD[35:0]	Physical Address
TYPE[3:0]	MAD[39:36]	Transaction Type
SIZE[2:0]	MAD[42:40]	Transaction Data Size
	MAD[63:43]	Reserved

Parity

Parity is not defined for MBus, however, the controller retains the capability to generate and check parity when configured for MBus.

TYPE[2:0]: Transaction Type

During the address phase, TYPE[2:0] specify the transaction type. TYPE[2:0] are multiplexed bus signals and are directly MBus compatible. The module fully responds to Write, Read, Coherent Read, Coherent Write and Invalidate, and Coherent Read and Invalidate. The response to Coherent Invalidate cycles is programmable. If the Coherent Invalidate Acknowledge Enable in the Command register is 0, the module makes no response to these cycles. This is the default condition after reset. If the Coherent Invalidate Acknowledge Enable in the Command register is 1, the module asserts $\overline{MRDY}$ for Coherent Invalidate cycles but, otherwise, plays no role in the transaction.

Table 37. Transaction Types

Type			Data Size	Transaction Site
2	**1**	**0**		
0	0	0	Any	Write
0	0	1	Any	Read
0	1	0	32 Bytes	Coherent Invalidate
0	1	1	32 Bytes	Coherent Read
1	0	0	Any	Coherent Write & Invalidate
1	0	1	32 Bytes	Coherent Read & Invalidate
All Other Combinations				Reserved

TYPE[2:0]: Transaction Size

During the address phase, SIZE[2:0] specify the number of bytes to be transferred during the data phase of the bus transaction. SIZE[2:0] are multiplexed bus signals and are directly MBus compatible.

Table 38. Size Transaction

Size2	Size1	Size0	Transaction Size
0	0	0	Byte
0	0	1	Halfword (2 Bytes)
0	1	0	Word (4 Bytes)
0	1	1	Doubleword (8 Bytes)
1	0	0	16-Byte Burst
1	0	1	32-Byte Burst
1	1	0	64-Byte Burst
1	1	1	128-Byte Burst

Table 39. Address Interpretation in Byte Mode (Size[2:0]=0)

A2	A1	A0	Byte#	Bits
0	0	0	0	D[63:56]
0	0	1	1	D[55:48]
0	1	0	2	D[47:40]
0	1	1	3	D[39:32]
1	0	0	4	D[31:24]
1	0	1	5	D[23:16]
1	1	0	6	D[15:8]
1	1	1	7	D[7:0]

Table 40. Address Interpretation in Halfword mode (Size[2:0]=1)

A2	A1	A0	Halfword#	Bits
0	0	X	0	D[63:48]
0	1	X	1	D[47:32]
1	0	X	2	D[31:16]
1	1	X	3	D[15:0]

Table 41. Address Interpretation in Word Mode (Size[2:0]=2)

A2	A1	A0	Word#	Bits
0	X	X	0	D[63:32]
1	X	X	1	D[31:0]

$\overline{BR}/\overline{FE}$ – Bus Request. This signal will be issued by the controller during reflective read transactions. $\overline{BR}$ from the main memory system should be interpreted as the highest priority request for bus mastership to the system's arbiter. Additional system bus transactions will be prevented until the ongoing write (resulting from the reflective read) to main memory has completed. (The original MBus specification has no explicit mechanism for reflective main memories to postpone the next bus transaction while the data being transferred between two caches is simultaneously written to DRAM.)

In the MBus mode, The BRM bit in Command register 3 should be programmed 0 to enable the bus request handshaking. When this is done, $\overline{BR}$ is deasserted upon the recognition of $\overline{BG}$ and is followed by the assertion of $\overline{BB}$. $\overline{BB}$ remains asserted until the Reflective FIFO is empty.

$\overline{BG}$ – Bus Grant. This signal is asserted by the external arbiter in response to a $\overline{BR}$, to indicate that the controller has been granted ownership of the bus.

$\overline{BB}$ – Bus Busy. This signal is asserted by the controller for the duration of its bus ownership. The controller will require the bus as it completes the main memory write transaction during reflective read operations.

ID[3:0] – Identification. The ID field selects various configuration spaces within the MBus address space for access to the Port register and other I/O registers.

Table 42. ID[3:0] Mapping

MBus CONFIGURATION SPACE	ID[3:0]
F/F000/000 H to F/F0FF/FFFF H	0 H reserved for boot PROM
F/F100/0000 H to F/F1FF/FFFF H	1 H
. .	.
F/Fn00/0000 H to F/Fn00/0000 H	n H
. .	.
F/FE00/0000 H to F/FEFF/FFFF H	E H
F/FF00/0000 H to F/FFFF/FFFF H	F H

Internal Registers

Several internal registers are available to set up the DRAM controller and report status to the host. The register's individual bits are defined in the sections describing the generic mode of operation. The registers appear on the MBus exactly as they would in the 64-bit bus generic mode, big-endian operation.

When the MBus mode is invoked, the MBus Port register becomes accessible. Its form, content, and address are defined below. In addition, the Command register 0 contains a control bit specific to MBus operation. This control bit affects the controllers response to MBus coherent invalidate cycles. Addressing of the internal registers is direct in the MBus mode and therefore the index register is not used. The address of each register has the form (in hexadecimal)

FFnxx0mpx

where n is a nibble that is compared to the input on the ID pins, x is a don't care condition, and mp are the two nibbles of the indexed address as given in the register descriptions. For example, if ID[3:0] is A H, then the MBus address for the $\overline{BERR}$ Register is FFAxx031x H.

MBus Port Register – 2 Bytes – Read Only

Address	7	6	5	4	3	2	1	0
FFF H	MR				MV			
Default	0 H				1 H			

Address	15	14	13	12	11	10	9	8
FFE H	MD							
Default	00 H or 01 H							

MV[3:0] – Vendor Code. This specifies the vendor code for MBus compatible devices – 1 H for Cypress Semiconductor.

Internal Registers (continued)

MR[3:0] – Revision Number. This specifies the revision level for MBus compatible devices – 0 H.

MD[7:0] – Device Number. This specifies a unique number that indicates the vendor specific MBus device present at this port.

00H CYM7232
01H CYM7264

MP[31:16] – Reserved for later use.

Specific Programming

For MBus, there will be specific register programming to configure the controller for MBus operation. For convenience, specific fields are listed below along with the load value appropriate to MBus. There are other programming selections that must be made which are dependent upon the specific application.

VCO[1:0] 10 80-MHz DRAM Clock

SBS 1 64-Bit System Bus

Timing

Bus timing diagrams reflect generic applications, however they are applicable to MBus. All of the diagrams must be interpreted for data strobe, $\overline{DS}$, permanently asserted.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 40°C to +125°C
Supply Voltage ..... – 0.3V to +7.0V
Input Voltage ..... – 3.0V to V_{CC} + 0.3V
Output Voltage ..... 0 to V_{CC} Volts

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7232 CYM7264 Min.	CYM7232 CYM7264 Max.	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
T_{AMB}	Ambient Temperature	Commercial	0	70	°C
V_{OH1}	Output HIGH Voltage Type 1	V_{CC} = Min., I_{OH1} = – 8.0 mA	2.4		V
V_{OH2}	Output HIGH Voltage Type 2	I_{OH2} = –12 mA	2.4		V
V_{OL1}	Output LOW Voltage Type 1	V_{CC} = Min., I_{O1L} = 8.0 mA		0.4	V
V_{OH2}	Output LOW Voltage Type 2	I_{OH2} = 12 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.4	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IN}	Input Leakage Current	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{SS}		+10	µA
I_{OUT}	Output Leakage Current	V_{CC} = Max., V_{SS} ≤ V_{OUT} ≤ V_{CC}		+10	µA
I_{CC}	Operating Current	Outputs Open, f = f_{MAX}		300	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C	Capacitance, In, Out, I/O	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	20	pF
CLK	Capacitance, Input		30	pF
$C_{\overline{BERR}}$, $C_{\overline{UERR}}$	Capacitance		30	pF

Output Signals by Type

Output	Description
$\overline{\text{BACK}}$[1]	Type 2
$\overline{\text{BERR}}$	Type 1
$\overline{\text{BR}}$/$\overline{\text{FE}}$	Type 2
$\overline{\text{BB}}$	Type 2
$\overline{\text{INT}}$, $\overline{\text{UERR}}$	Type 1
$\overline{\text{RAS}}$[3:0]	Type 2
$\overline{\text{CAS}}$[3:0]	Type 2
ADRS[11:0]	Type 2
DDA, DDB, DDC, DDD	Type 1
EDA, EDB, EDC, EDD	Type 1
R/$\overline{\text{W}}$[3:0]	Type 1
DP[7:0]	Type 1
D[63:0]	Type 1

Type 1 outputs are designed to drive 50-pF loads with a DC drive of 8 mA. Type 2 outputs are designed to drive 50-pF loads with a DC drive of 12 mA. MBus modules are tested with 100-pF loads to guarantee compatibility with the MBus specification.

Data and Data Parity Holding Buffers

The system bus data and data parity pins are equipped with holding buffers. These buffers use a weak feedback buffer combined with the input buffer to form a latch. The latch holds the last value driven on the bus.

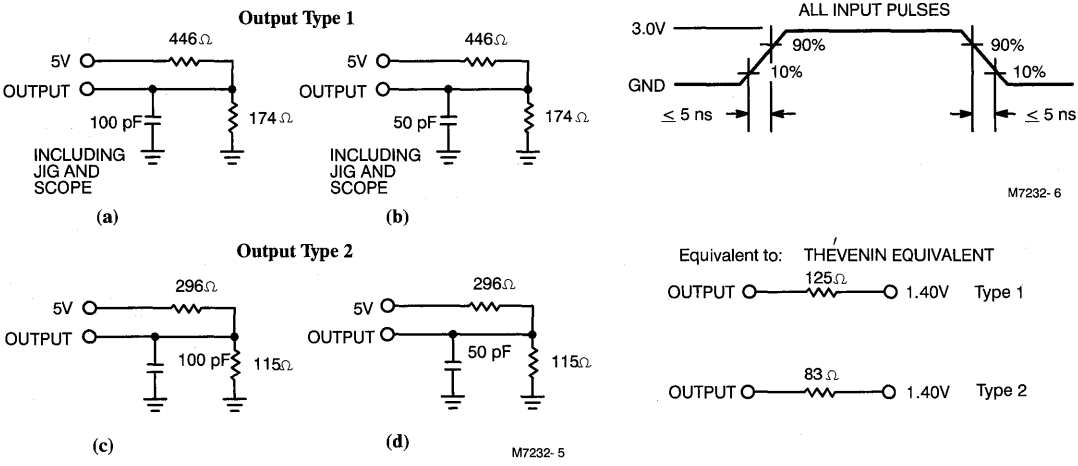
Holding Buffer DC Characteristics

Holding 0
V_{IN} = 0.4V — I_{IN} = 160 µA (Max.), 45 µA (Min.)
Holding 1
V_{IN} = 2.4V — I_{IN} = − 715 µA (Max.), − 175 µA (Min.)

Flipping Current

Holding 0
V_{IN} = 2.0V — I_{IN} = 565 µA (Max.)
V_{IN} = 2.4V — I_{IN} = 630 µA (Max.)
Holding 1
V_{IN} = 0.8V — I_{IN} = − 725 µA (Max.)
V_{IN} = 0.4V — I_{IN} = − 730 µA (Max.)

AC Test Loads and Waveforms



AC Timing Characteristics

Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
D[63:0], DP[7:0] Output Delay	7	18.5	9	21.5	11	23.5	ns
D[63:0], DP[7:0] Output Hold	3		3.5		3.5		ns
D[63:0], DP[7:0] Input Set-Up	4		5		7		ns
D[63:0], DP[7:0] Input Hold	2.5		2.5		2.5		ns
A[35:0], AP[3:0] Input Set-Up	4		5		7		ns
A[35:0], AP[3:0] Input Hold	2.5		2.5		2.5		ns
TYPE[5:0] Input Set-Up	4		5		7		ns
TYPE[5:0] Input Hold	2.5		2.5		2.5		ns
SIZE[7:0] Input Set-Up	4		5		7		ns
SIZE[7:0] Input Hold	2.5		2.5		2.5		ns
ID[3:0] Input Set-Up	4		5		7		ns
ID[3:0] Input Hold	2.5		2.5		2.5		ns
$\overline{AS}$ Set-Up	4		5		7		ns
$\overline{AS}$ Hold	2.5		2.5		2.5		ns
$\overline{DS}$ Set-Up	4		5		7		ns
$\overline{DS}$ Hold	2.5		2.5		2.5		ns
$\overline{INH}$ Set-Up	4		5		7		ns
$\overline{INH}$ Hold	2.5		2.5		2.5		ns
$\overline{SNW}$ Set-Up	4		5		7		ns
$\overline{SNW}$ Hold	2.5		2.5		2.5		ns
$\overline{TRC}$ Set-Up	4		5		7		ns
$\overline{TRC}$ Hold	2.5		2.5		2.5		ns
$\overline{BG}$ Set-Up	4		5		7		ns
$\overline{BG}$ Hold	2.5		2.5		2.5		ns
$\overline{BR}/\overline{FE}$ Output Delay	7	17.5	9	20.5	11	22.5	ns
$\overline{BR}/\overline{FE}$ Output Hold	3		3.5		3.5		ns
$\overline{BB}$ Output Delay	10	17.5	12	20.5	14	22.5	ns
$\overline{BB}$ Output Hold	3		3.5		3.5		ns
$\overline{BB}$ Input Set-Up	4		5		7		ns
$\overline{BB}$ Input Hold	2.5		2.5		2.5		ns
$\overline{IMD}$ Input Set-Up	10.5		13.5		16.5		ns
$\overline{IMD}$ Input Hold	2.5		2.5		2.5		ns
$\overline{RSTIN}$ Input Set-Up	10.5		13.5		16.5		ns
$\overline{RSTIN}$ Input Hold	5		5		5		ns
$\overline{INT}$ Output Delay	7	18.5	9	21.5	11	23.5	ns
$\overline{INT}$ Output Hold	3		3.5		3.5		ns
$\overline{BERR}$ Output Delay	7	18.5	9	21.5	11	23.5	ns

AC Timing Characteristics (continued)

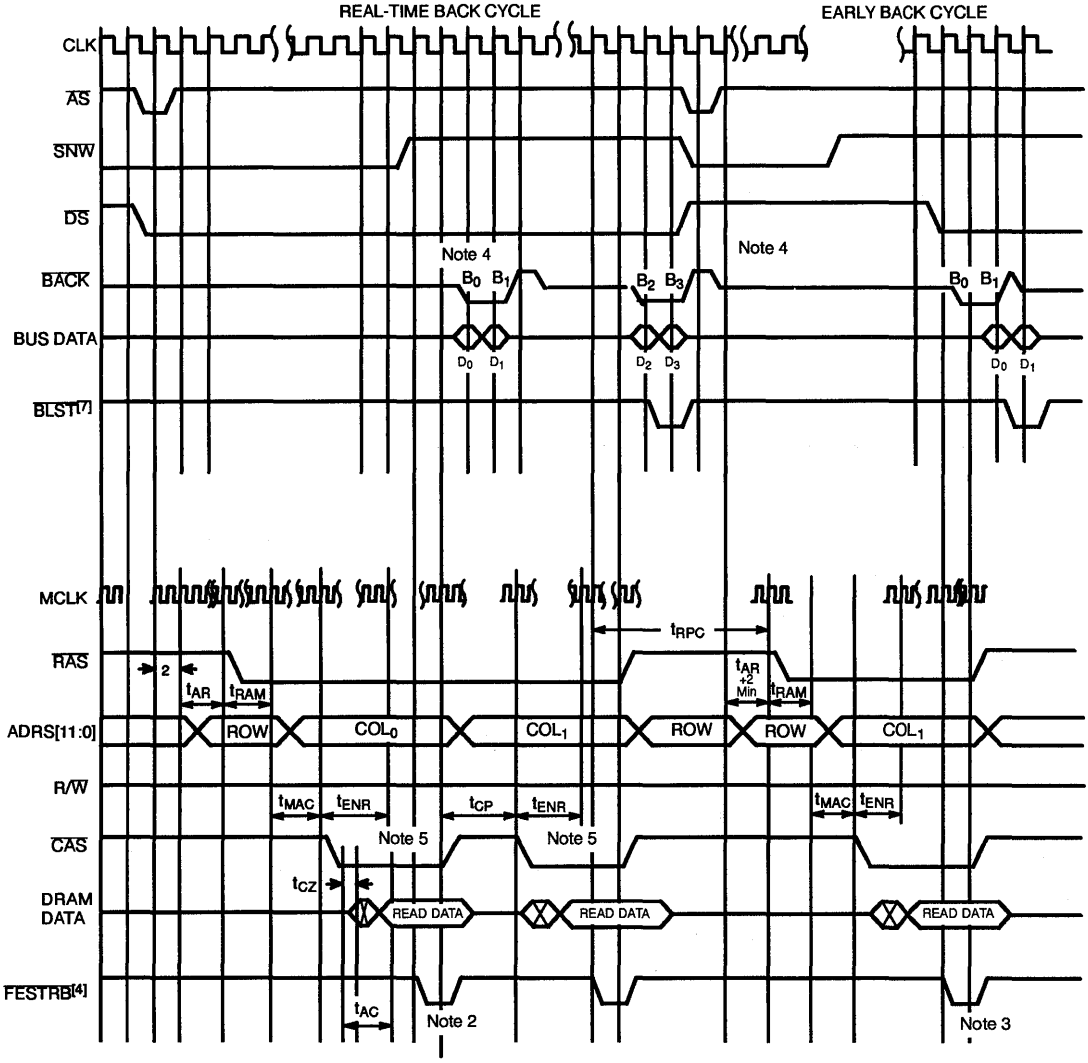
Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{\text{BERR}}$ Output Hold	3		3.5		3.5		ns
TSTE Input Set-Up	10.5		13.5		16.5		ns
TSTE Input Hold	3		3		3		ns
TSTM Input Set-Up	10.5		13.5		16.5		ns
TSTM Input Hold	3		3		3		ns
$\overline{\text{UERR}}$ Output Delay	7	17.5	9	20.5	11	22.5	ns
$\overline{\text{UERR}}$ Output Hold	3		3.5		3.5		ns
$\overline{\text{UERR}}$ Input Set-Up	7.5		10.5		13.5		ns
$\overline{\text{UERR}}$ Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$0 Input Set-Up	4		5		7		ns
$\overline{\text{BACK}}$0 Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$0 Output Delay (MBus)		17.5		20.5		22.5	ns
$\overline{\text{BACK}}$0 Output Hold (MBus)	3		3.5		3.5		ns
$\overline{\text{BACK}}$1 Output Delay (Real Time)	9	17.5	11	20.5	13	22.5	ns
$\overline{\text{BACK}}$1 Output Hold (Real Time)	3		3.5		3.5		ns
$\overline{\text{BACK}}$1 Input Set-Up	4		5		7		ns
$\overline{\text{BACK}}$1 Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$1 Output Delay (Early)	11	21	13	24	15	26	ns
$\overline{\text{BACK}}$1 Output Hold (Early)	3		3.5		3.5		ns
$\overline{\text{BLST}}$ Input Set-Up	4		5		7		ns
$\overline{\text{BLST}}$ Input Hold	2.5		2.5		2.5		ns
ADRS[11:0] Output Delay	7	16	9	18	11	21	ns
ADRS[11:0] Output Hold	3		3.5		3.5		ns
RAS[3:0] Output Delay	7	16	9	18	11	21	ns
RAS[3:0] Output Hold	3		3.5		3.5		ns
CAS[3:0] Output Delay	7	16	9	18	11	21	ns
CAS[3:0] Output Hold	3		3.5		3.5		ns
R/W[3:0]/[1:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
R/W[3:0]/[1:0] Output Hold	3						ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Output Hold	1		3		3		ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Input Set-Up	4		5		7		ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Intput Hold	2.5		2.5		2.5		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Output Hold	1		3		3		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Input Set-Up	4		5		7		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Intput Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$[1:0], $\overline{\text{UERR}}$ Input Set-Up During Reset	8		10		12		ns
$\overline{\text{BACK}}$[1:0], $\overline{\text{UERR}}$ Input Hold During Reset	5		5		5		ns

AC Timing Characteristics (continued)

Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency	20	40	20	33	20	25	MHz
Clock Cycle Time	50	25	50	30	50	40	ns
Clock Rise Time		1.6		1.6		1.6	ns
Clock Fall Time		1.6		1.6		1.6	ns
Clock Symmetry	45	55	45	55	45	55	%
Clock Pulse Width HIGH at 40, 33, and 25 MHz	11	14	13.5	16.5	18	22	ns
Clock Pulse Width LOW at 40, 33, and 25 MHz	11	14	13.5	16.5	18	22	ns
MCLK Frequency	20	80	20	66	20	75	MHz
MCLK Cycle Time	12.5	50	15	50	13.33	50	ns
MCLK Rise Time		1.6		1.6		1.6	ns
MCLK Fall Time		1.6		1.6		1.6	ns
MCLK Symmetry	45	55	45	55	45	55	%
MCLK Pulse Width HIGH at 80, 66, and 75 MHz)	5.5	7	6.5	8.5	6	7.5	ns
MCLK Pulse Width LOW at 80, 66, and 75 MHz)	5.5	7	6.5	8.5	6	7.5	ns
MCLK/CLK Skew	− 1.5	0	− 1.5	0	− 1.5	0	ns

Switching Waveforms

Read

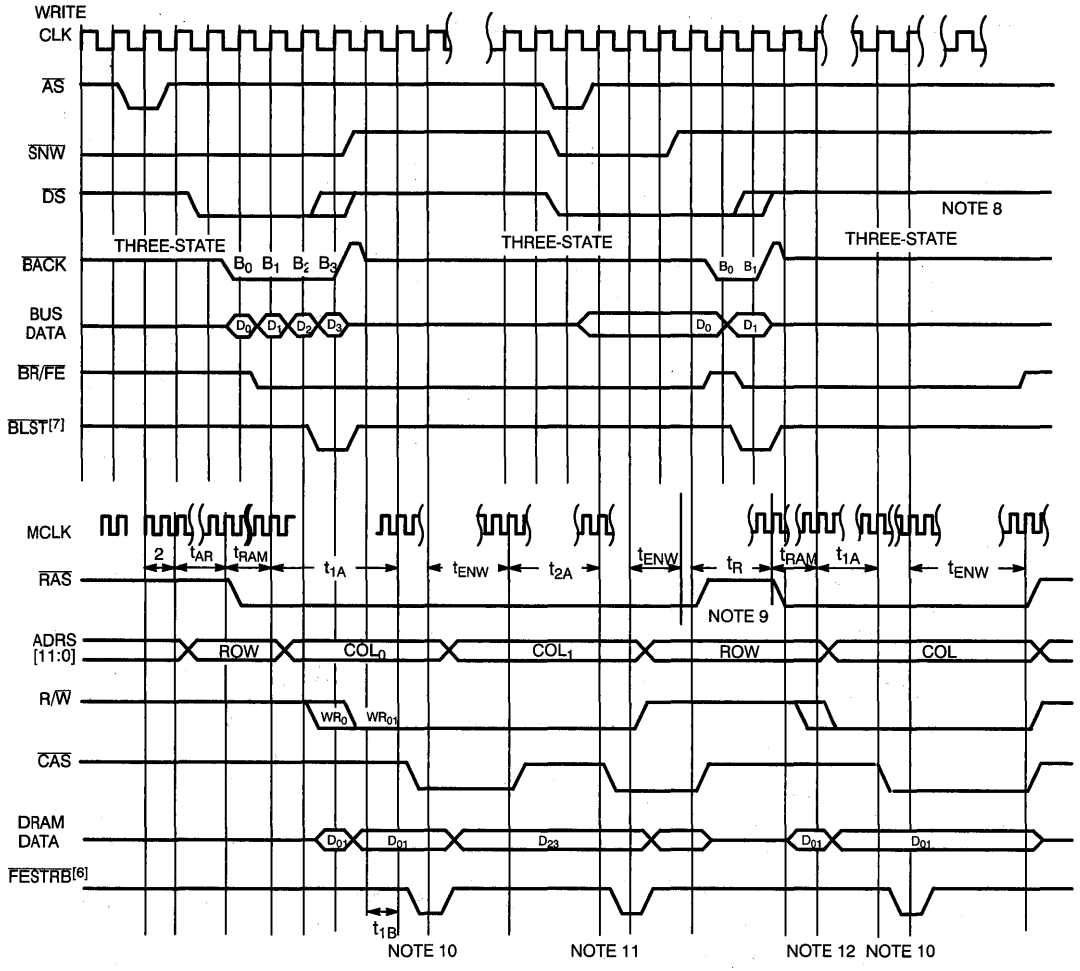


Notes:

2. FESTRB is asserted here following the closure of the snoop window in the previous clock cycle.
3. FESTRB would normally occur after t_{ENR} plus a delay if necessary to align FESTRB to a bus clock boundary. FESTRB is asserted here following the assertion of DS (data strobe) in the previous clock cycle.
4. BACK remains three-stated until it is first asserted. At the middle and end of the transaction, BACK is deasserted in the first half of the clock cycle and then three-stated.
5. FESTRB would normally occur here after t_{ENR}, however, it is automatically delayed by the controller to align to a bus clock boundary.

Switching Waveforms (continued)

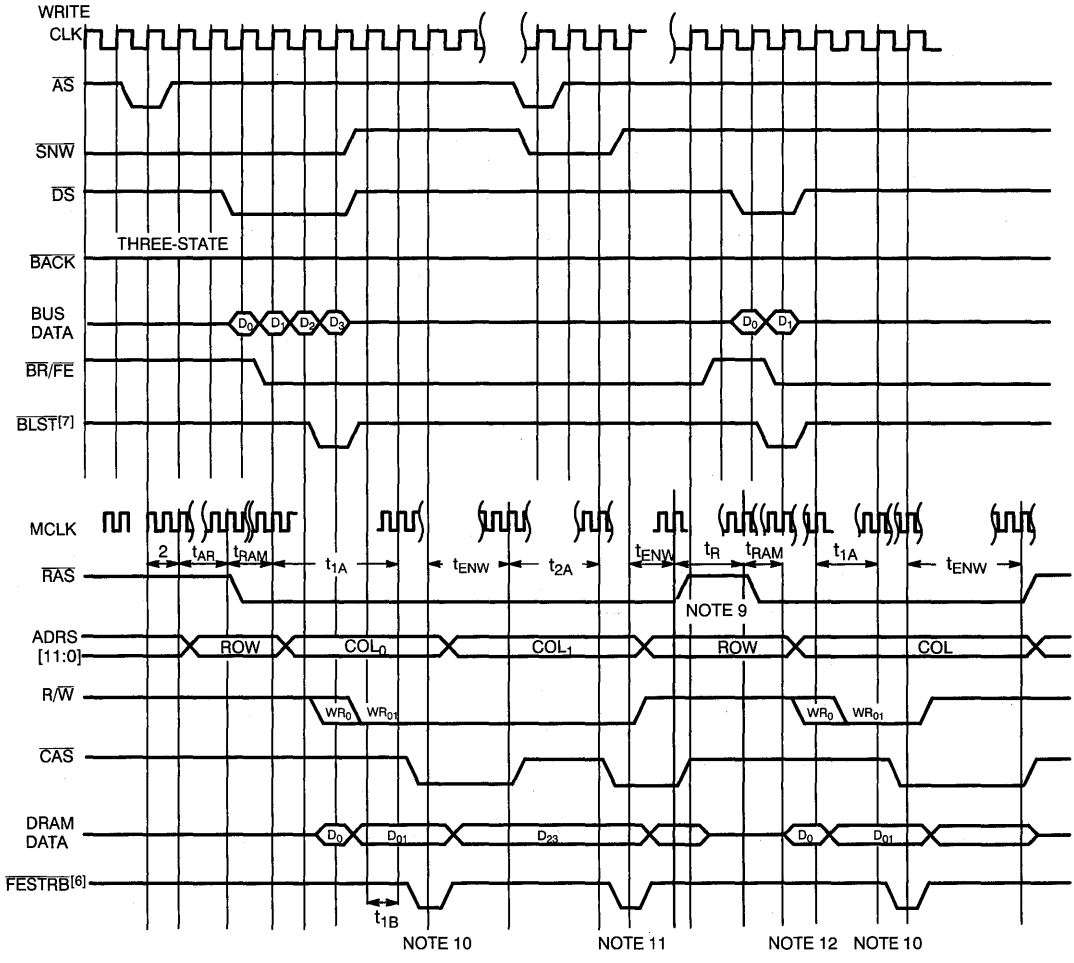
Write – Real-Time Bus Acknowledge/Early Data Strobe



Notes:

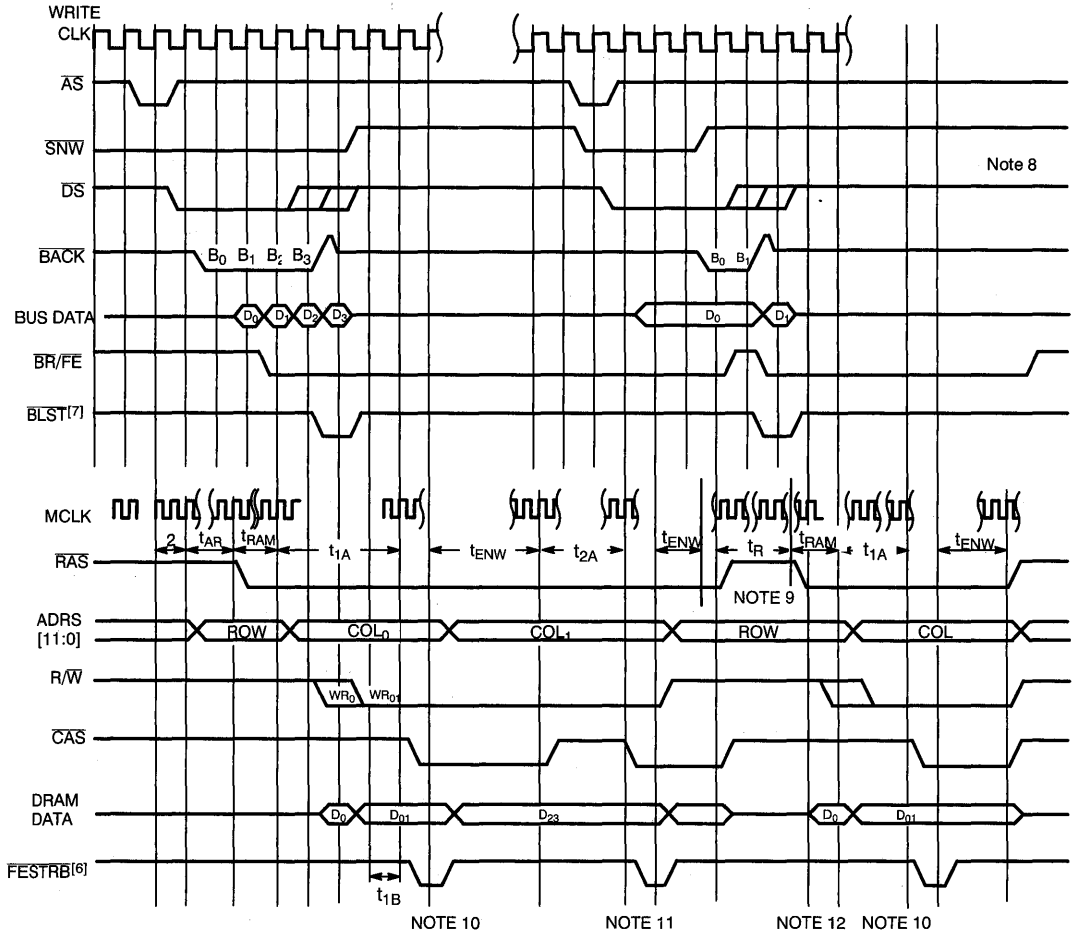
6. $\overline{\text{FESTRB}}$ is an internal signal that unclocks the FIFO. $\overline{\text{FESTRB}}$ is one bus clock cycle long.
7. $\overline{\text{BLST}}$ may be internal or external
8. $\overline{\text{DS}}$ may be deasserted in any of the cycles shown.
9. $t_R \geq t_{RPC} + 2$ MCLK
   $t_R \geq t_{AR} + 2$ MCLK
10. The assertion of $\overline{\text{CAS}}$ requires
    t_{CP} to have expired (from previous transaction)
    t_{MAC} have expired ($t_{1A} \geq t_{MAC}$)
    t_{DC} to have expired ($t_{1B} \geq t_{DC}$)
    $\overline{\text{SNW}}$ to have closed 2 bus clocks previous.
11. The assertion of $\overline{\text{CAS}}$ (and all subsequent $\overline{\text{CAS}}$ cycles of the burst) requires
    t_{DC} to have expired
    t_{CP} to have expired ($t_{2A} > t_{CP}$)
    After $\overline{\text{CAS}}$ asserted, $\overline{\text{FESTRB}}$ unclocks the write FIFO presenting the next data page to the DRAM.
12. t_{1A} is measured from the rising edge of the bus clock after t_{RAM} has expired.

Switching Waveforms (continued)
Write – Real-Time Data Strobe



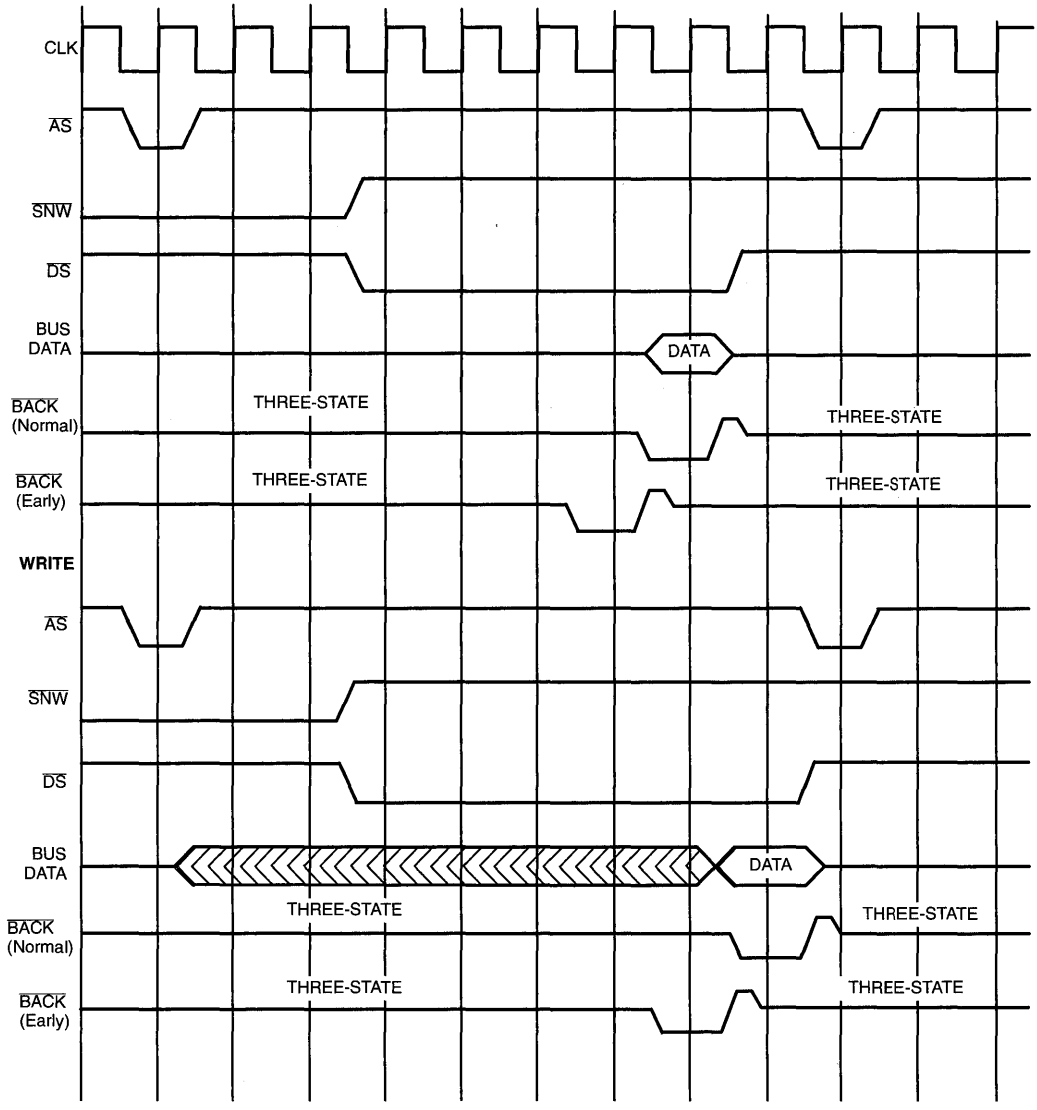
Switching Waveforms (continued)

Write – Early Bus Acknowledge



Switching Waveforms (continued)

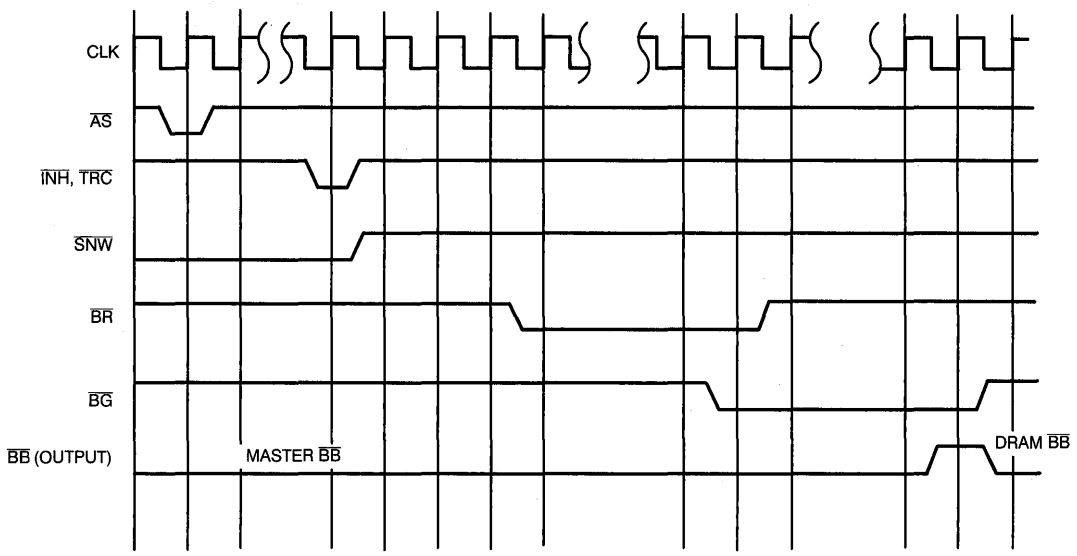
I/O Cycles – Read[13]



Note:
13. Data transfer occurs 5 clock cycles after $\overline{SNW}$ or $\overline{DS}$ whichever occurs last.

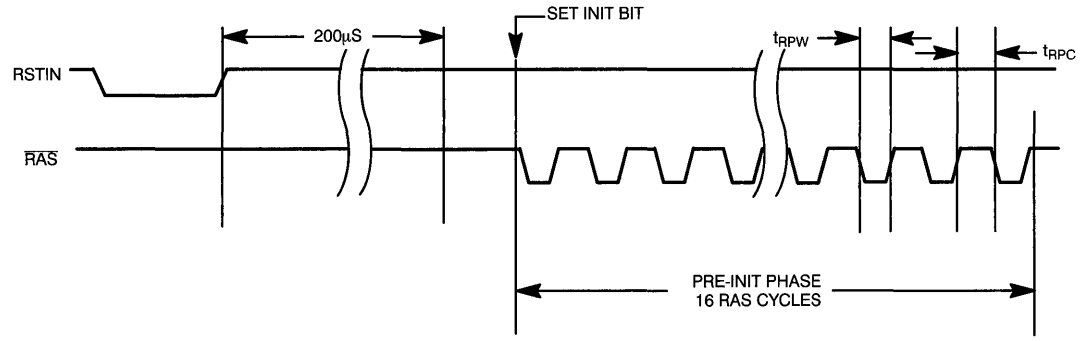
Switching Waveforms (continued)

Arbitration for Bus Mastership During Reflective Read

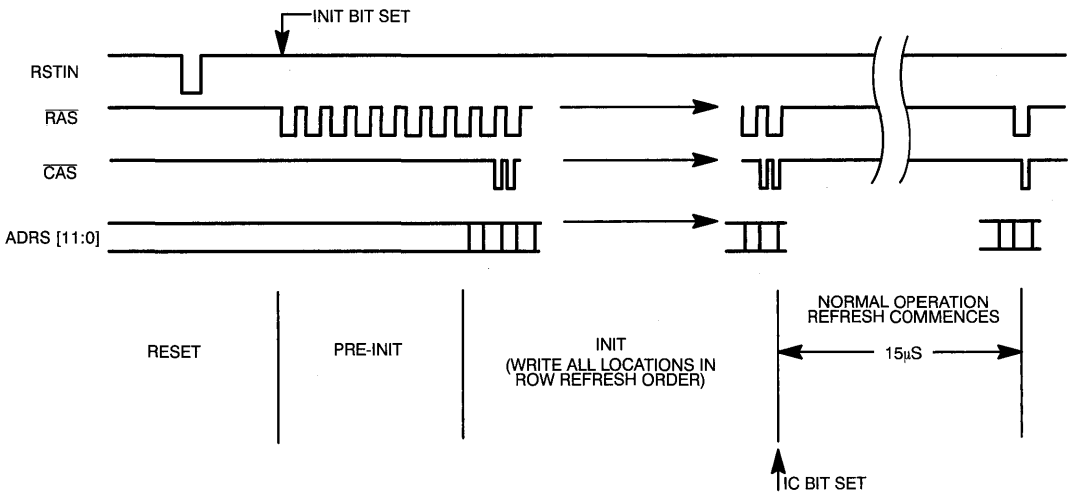


Switching Waveforms (continued)

Pre-initialization

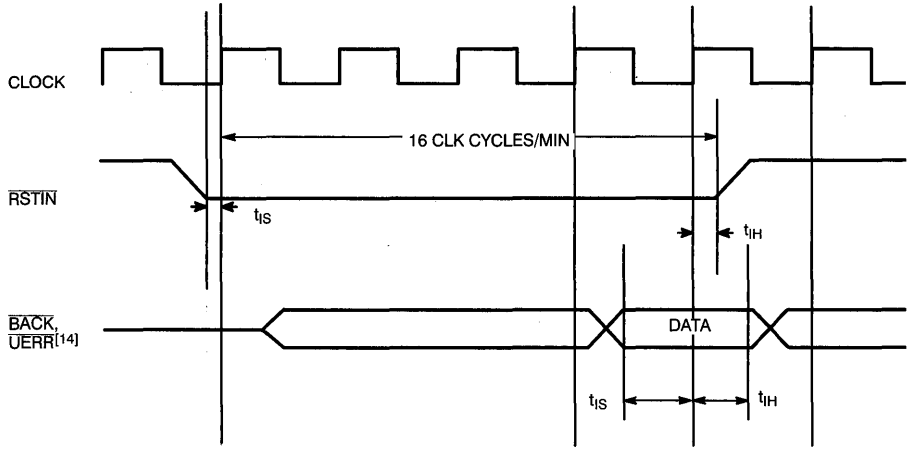


Initialization

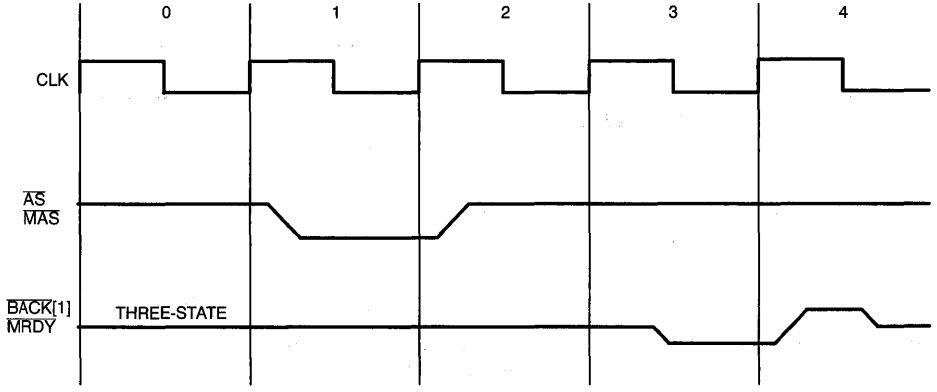


Switching Waveforms (continued)

Reset Cycle



MBus Coherent Invalidate Cycle (CIE set)

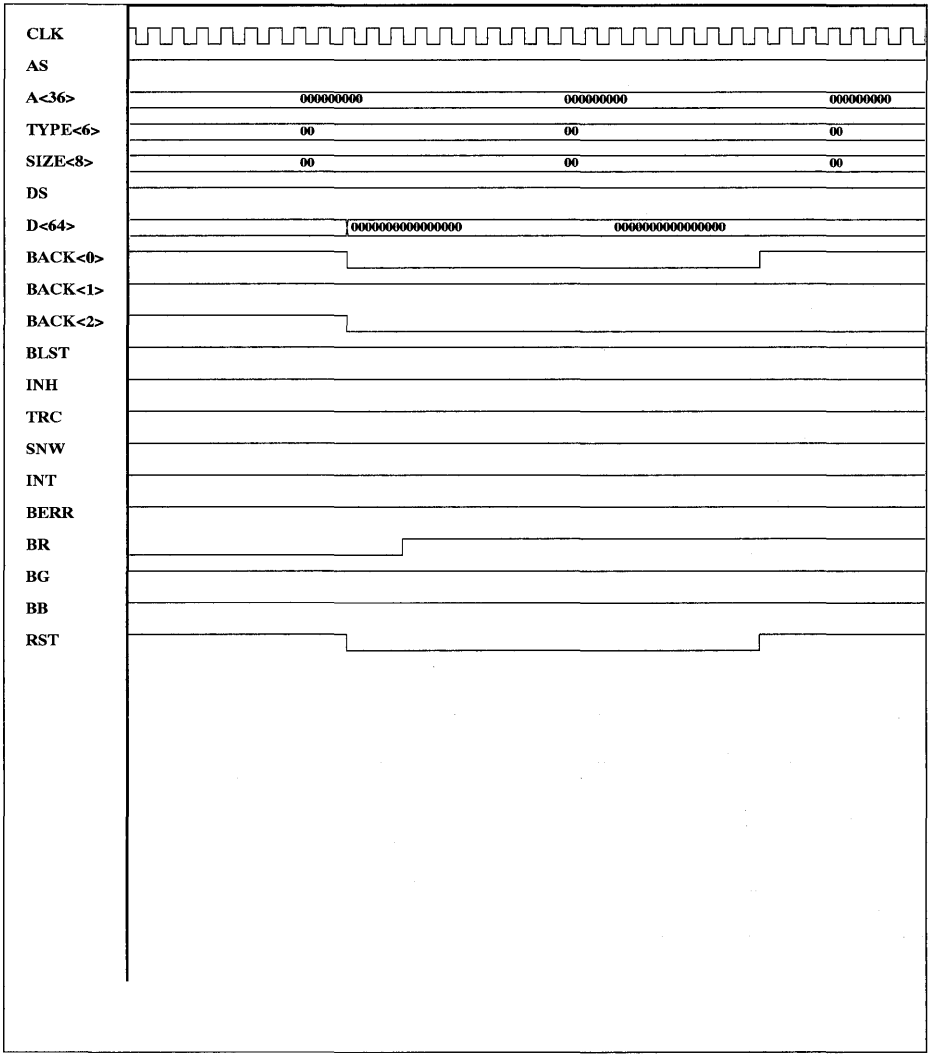


Note:

14. BACK and UERR used as input to select bus acknowledge modes and snoop window source during reset.

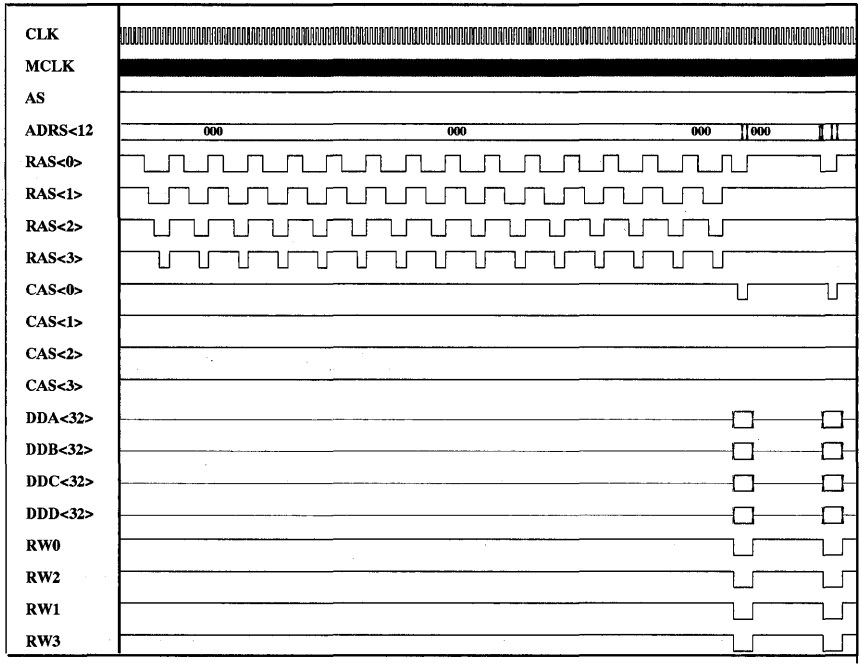
Timing Diagrams

RESET Invoking Mode 10, External Snoop Window

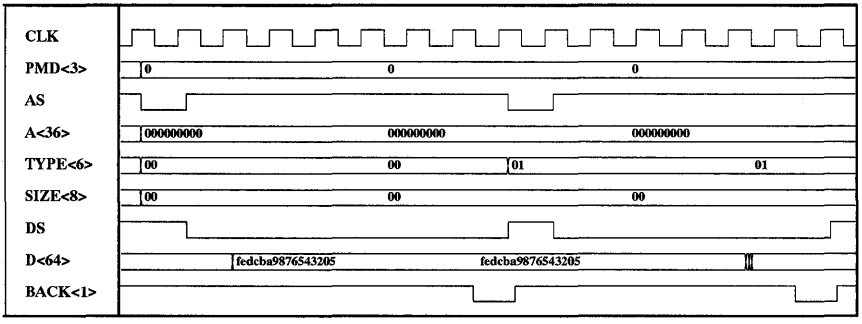


Timing Diagrams (continued)

Preinit Followed by Start of DRAM Init

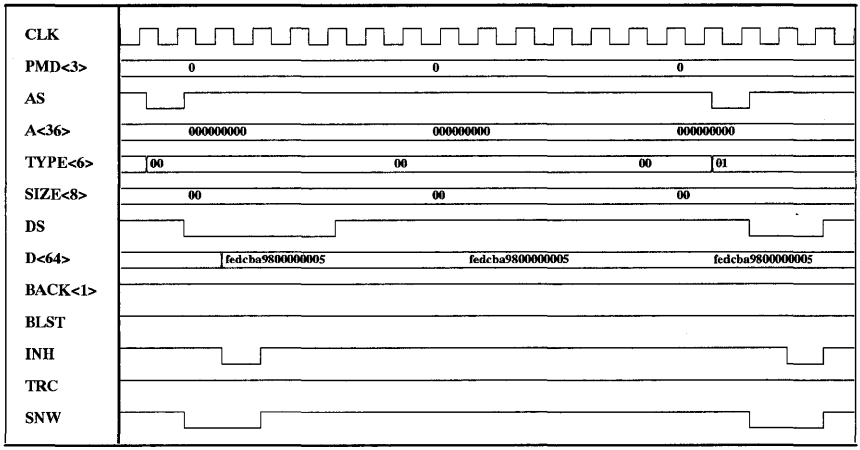


I/O Write Followed by Read, Mode 01

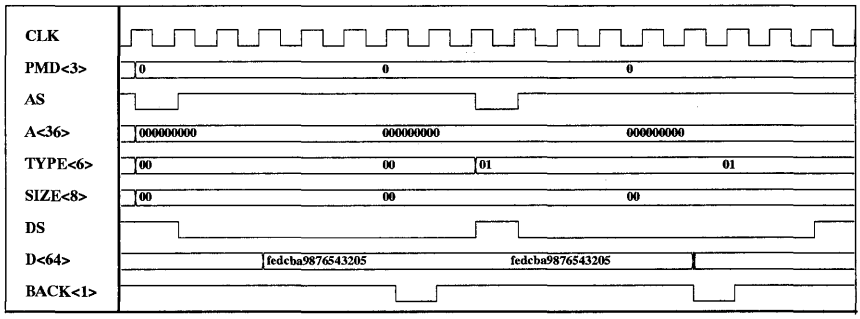


Timing Diagrams (continued)

I/O Write Inhibited Follwed by Read Inhibited

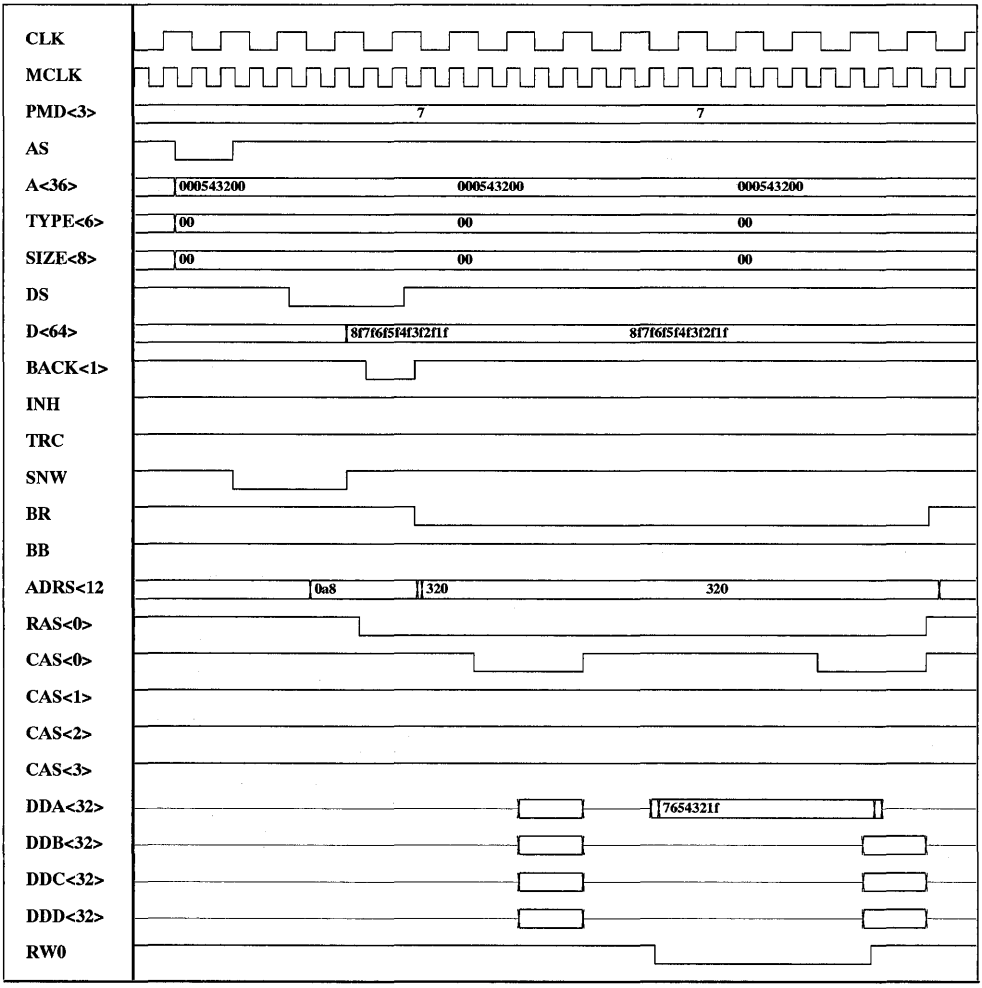


I/O Write Followed by Read, Mode 11



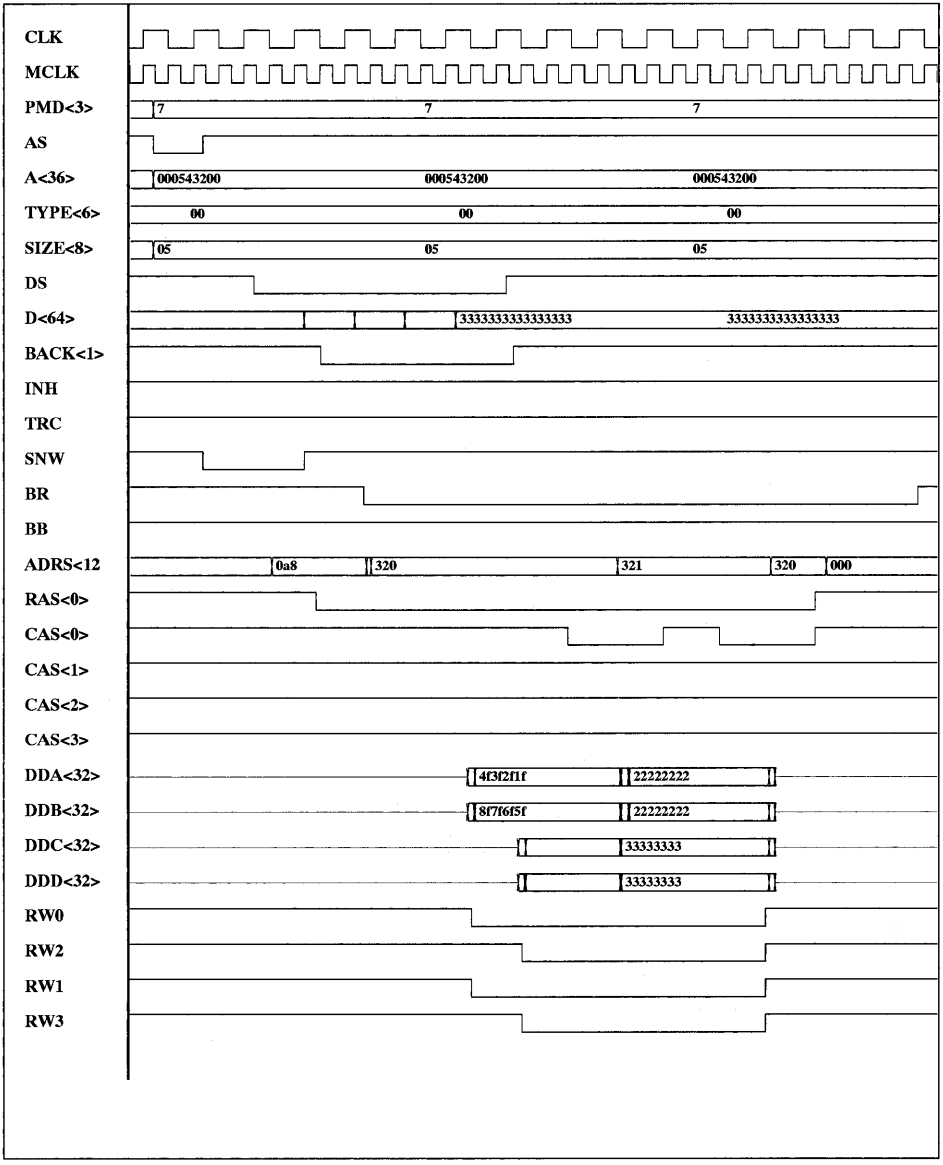
Timing Diagrams (continued)

Read-Modify-Write Mode 01



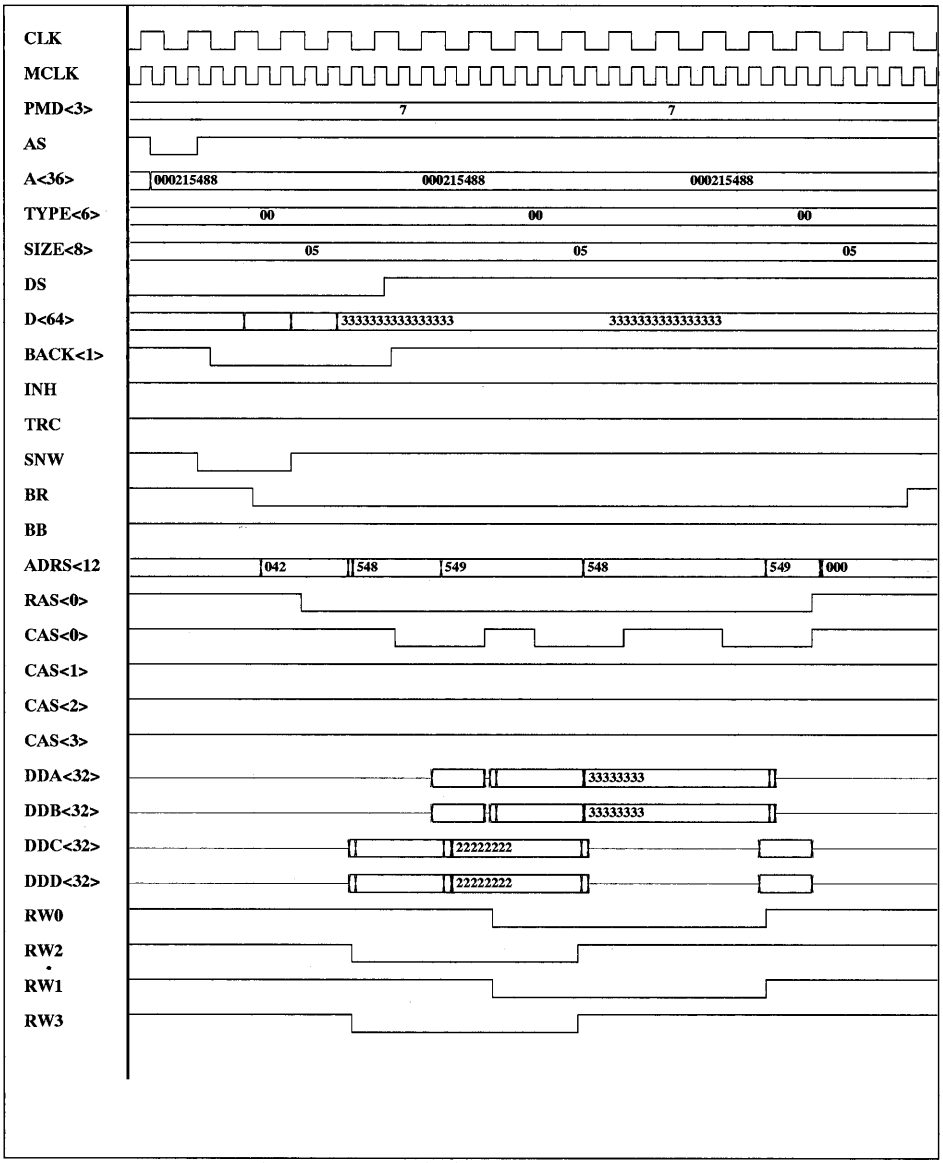
Timing Diagrams (continued)

Write Mode 01, Sequential, 32 Bytes



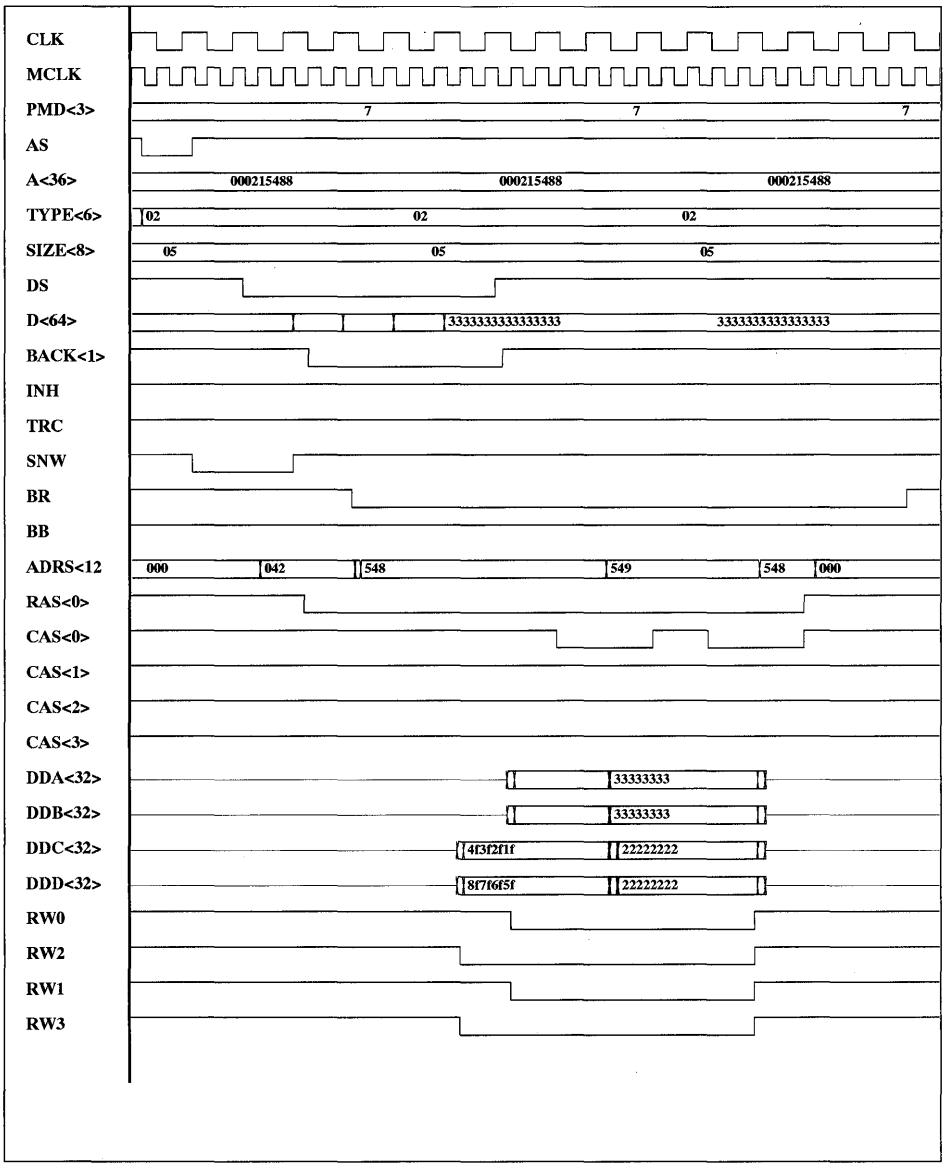
Timing Diagrams (continued)

Write Mode 01, Sequential, Misaligned, 32 Bytes



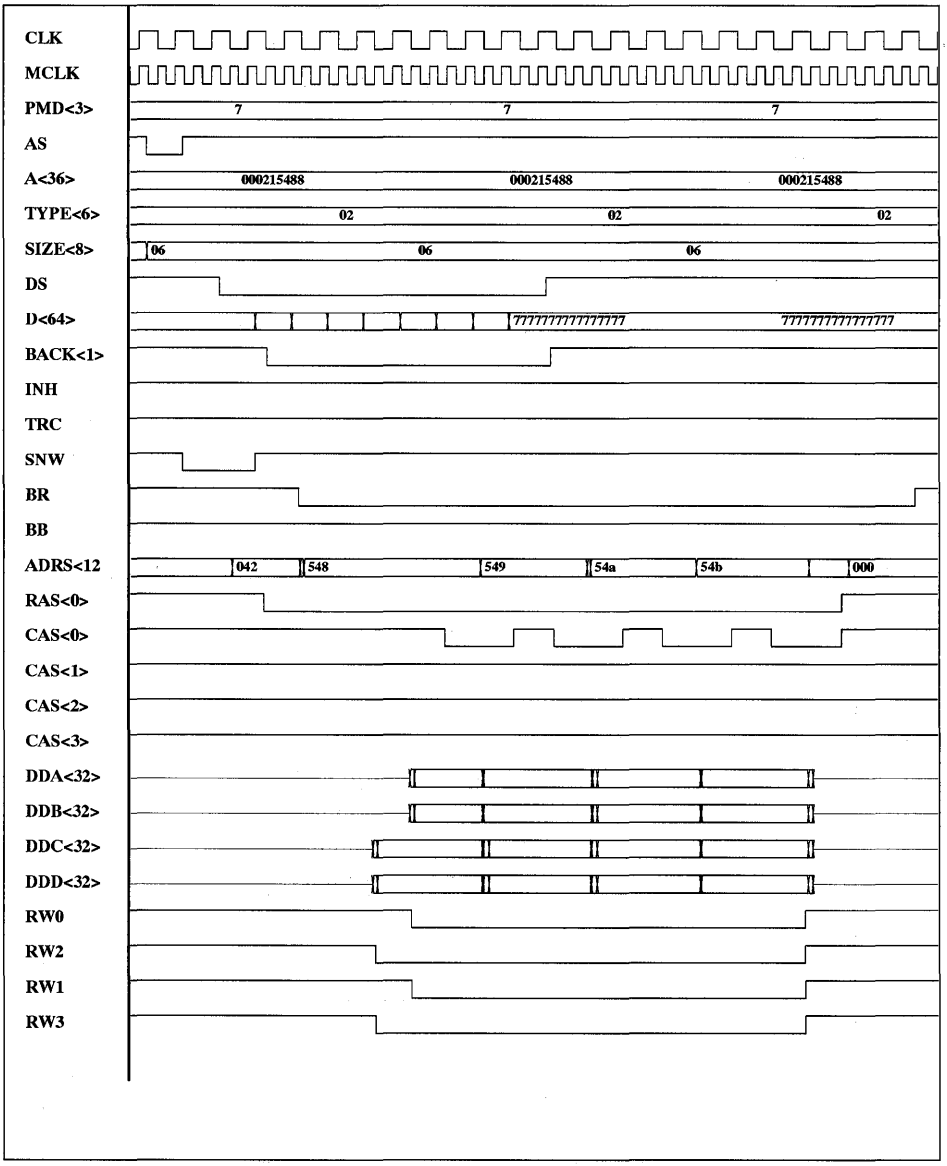
Timing Diagrams (continued)

Write Mode 01, Intel, Misaligned



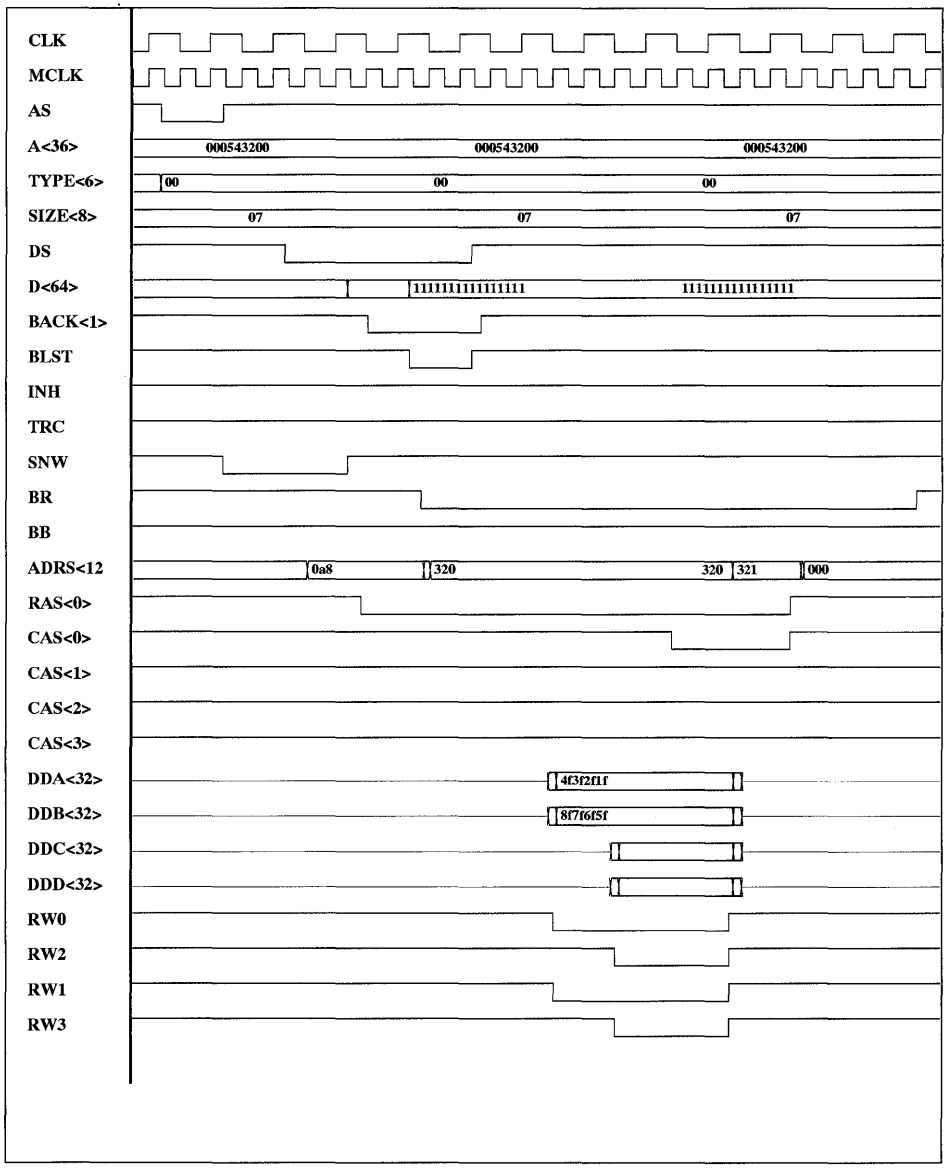
Timing Diagrams (continued)

Write Mode 01, Intel, Misaligned, 64 Bytes



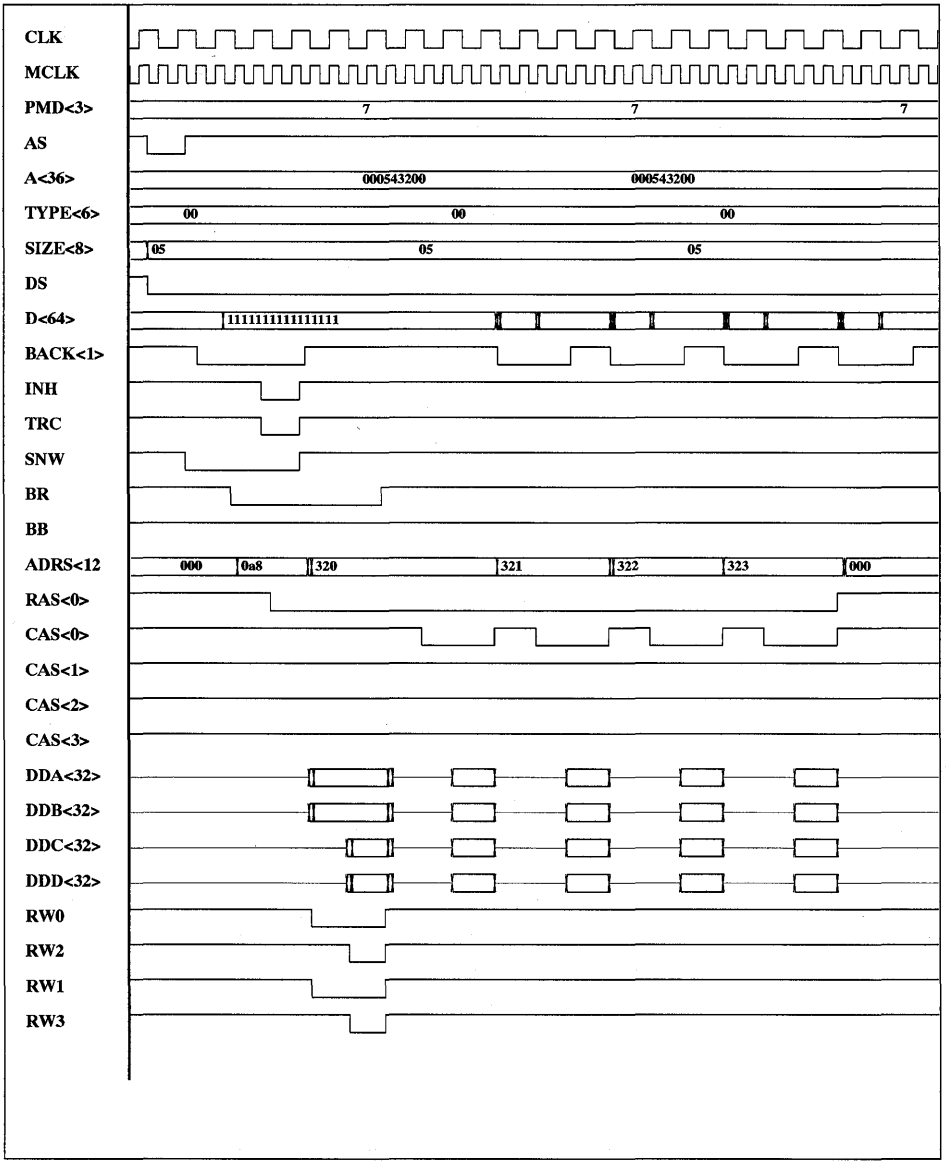
Timing Diagrams (continued)

Write Burst Truncated by BLST, Mode 01



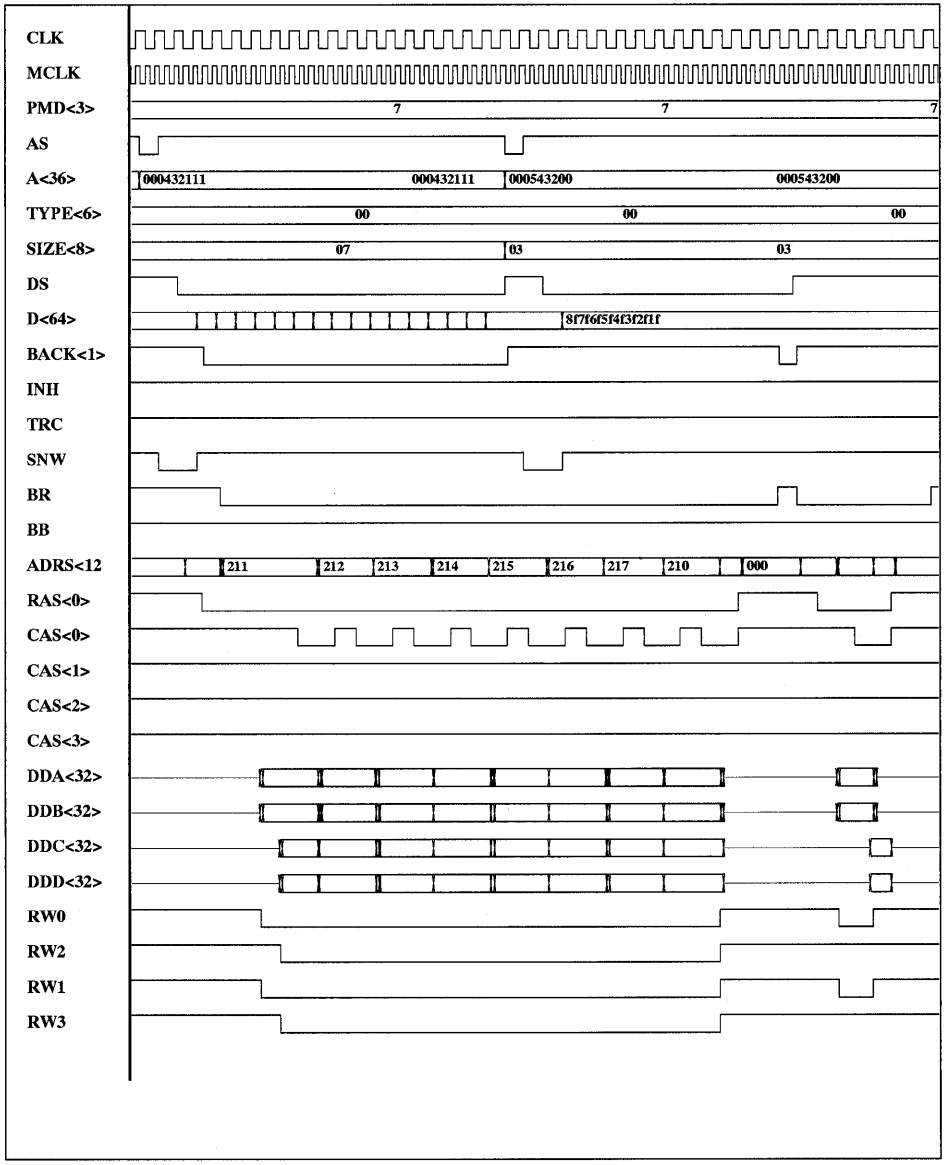
Timing Diagrams (continued)

Write Mode 01, Transformed



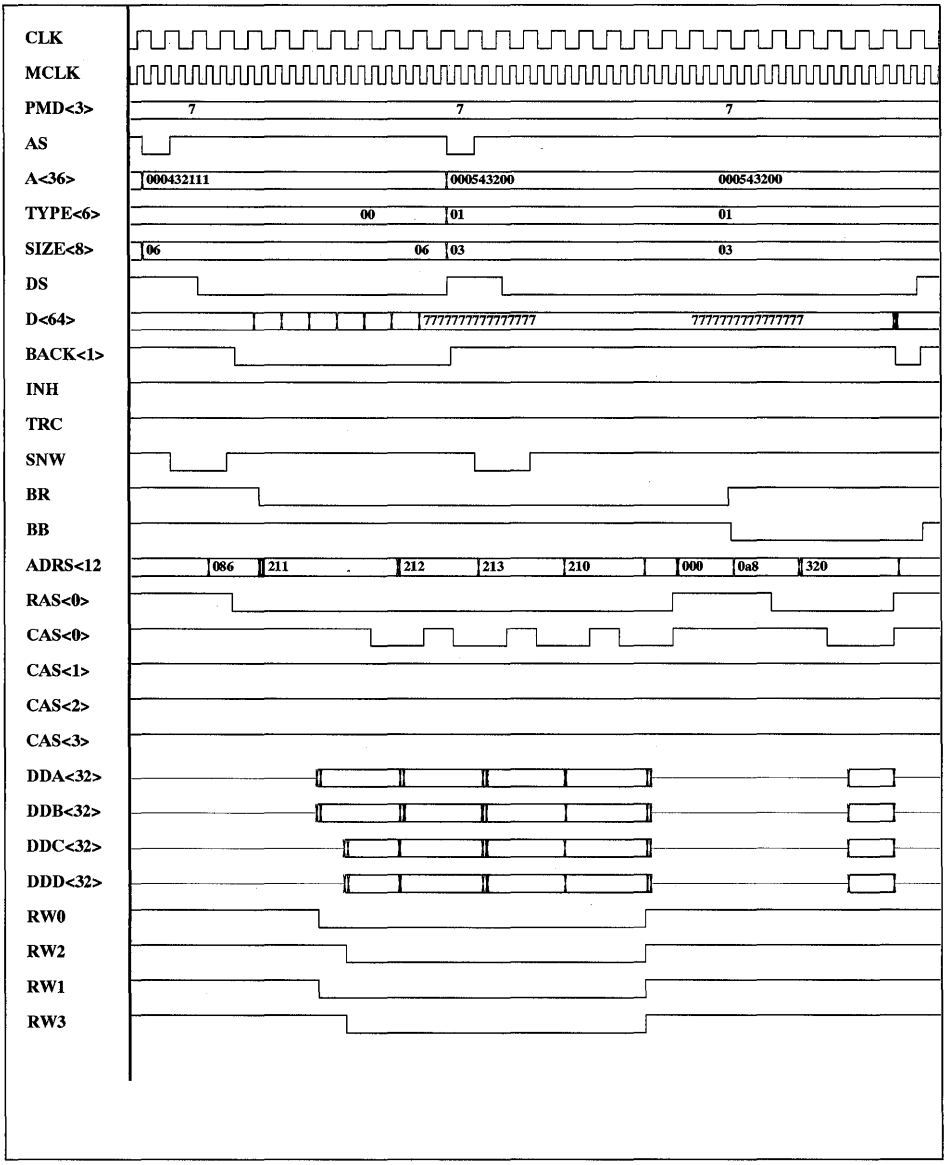
Timing Diagrams (continued)

Write Burst Followed by Write, Mode 01



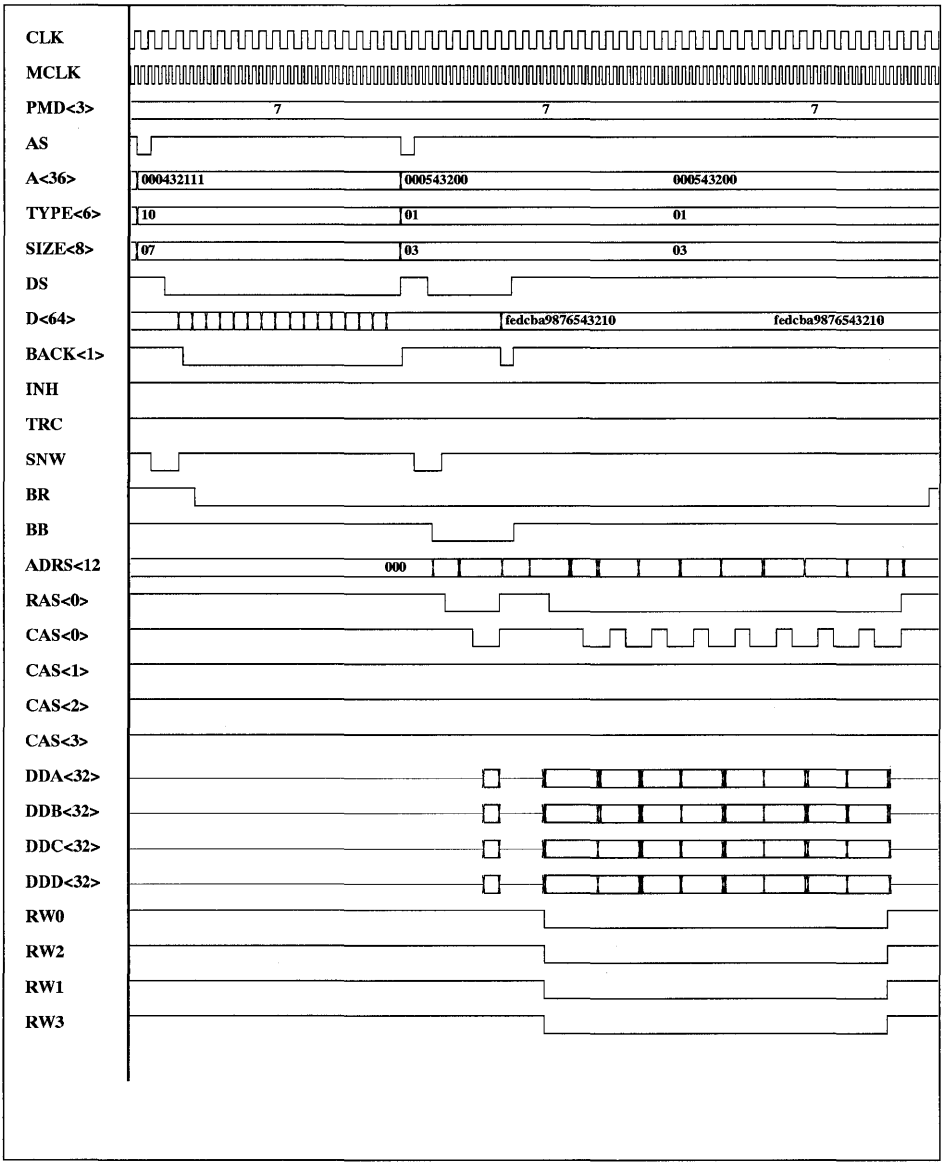
Timing Diagrams (continued)

Write Burst Followed by Read, Mode 01



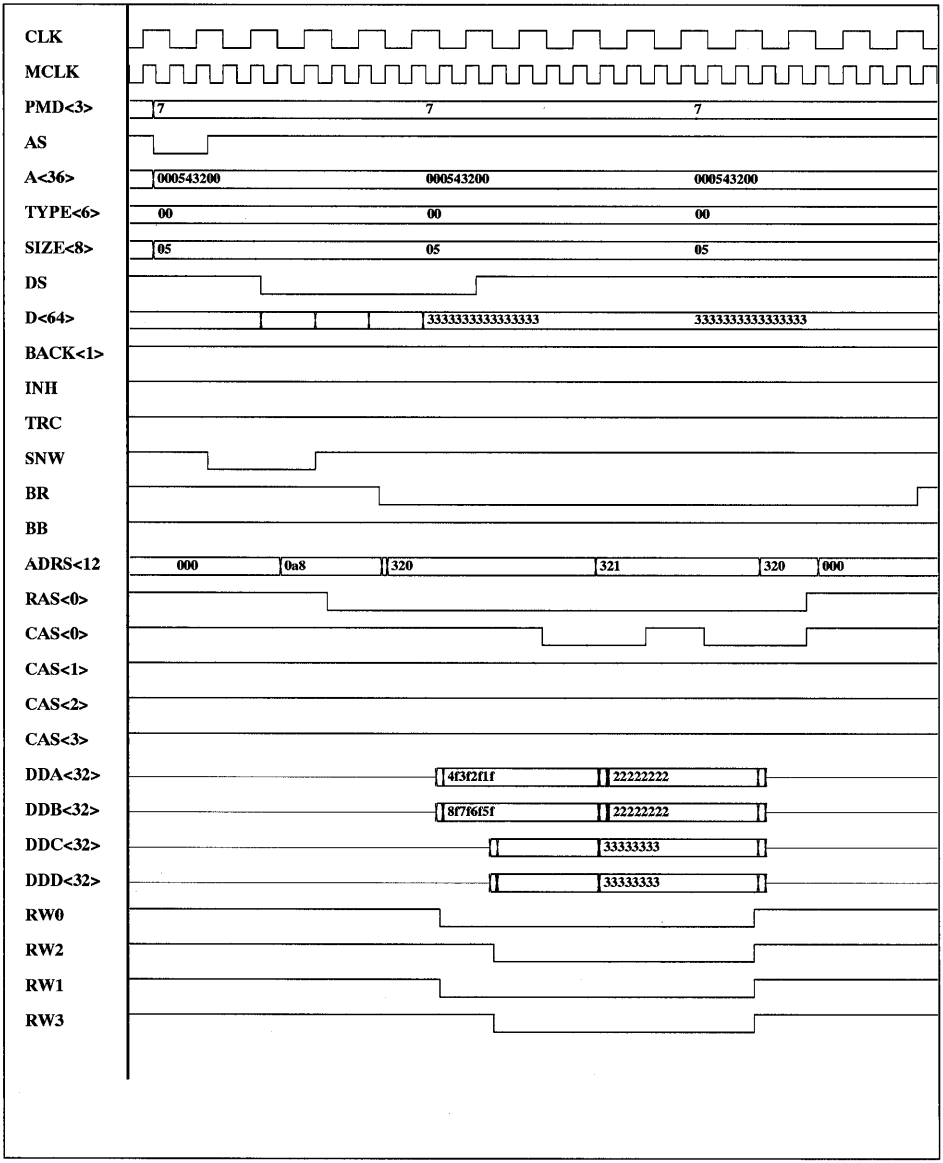
Timing Diagrams (continued)

Write Posted Followed by Read, Mode 01



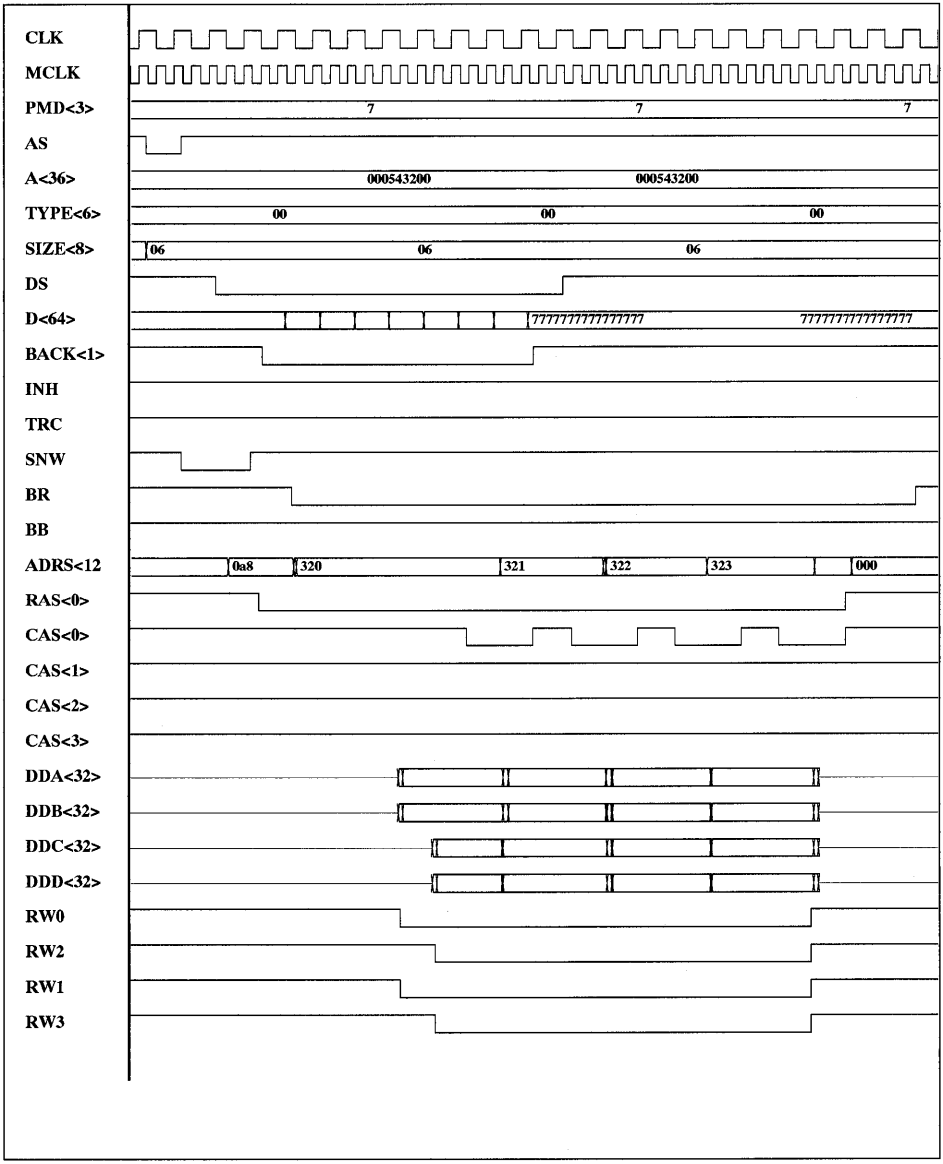
Timing Diagrams (continued)

Write Mode 10 Showing BR as FE



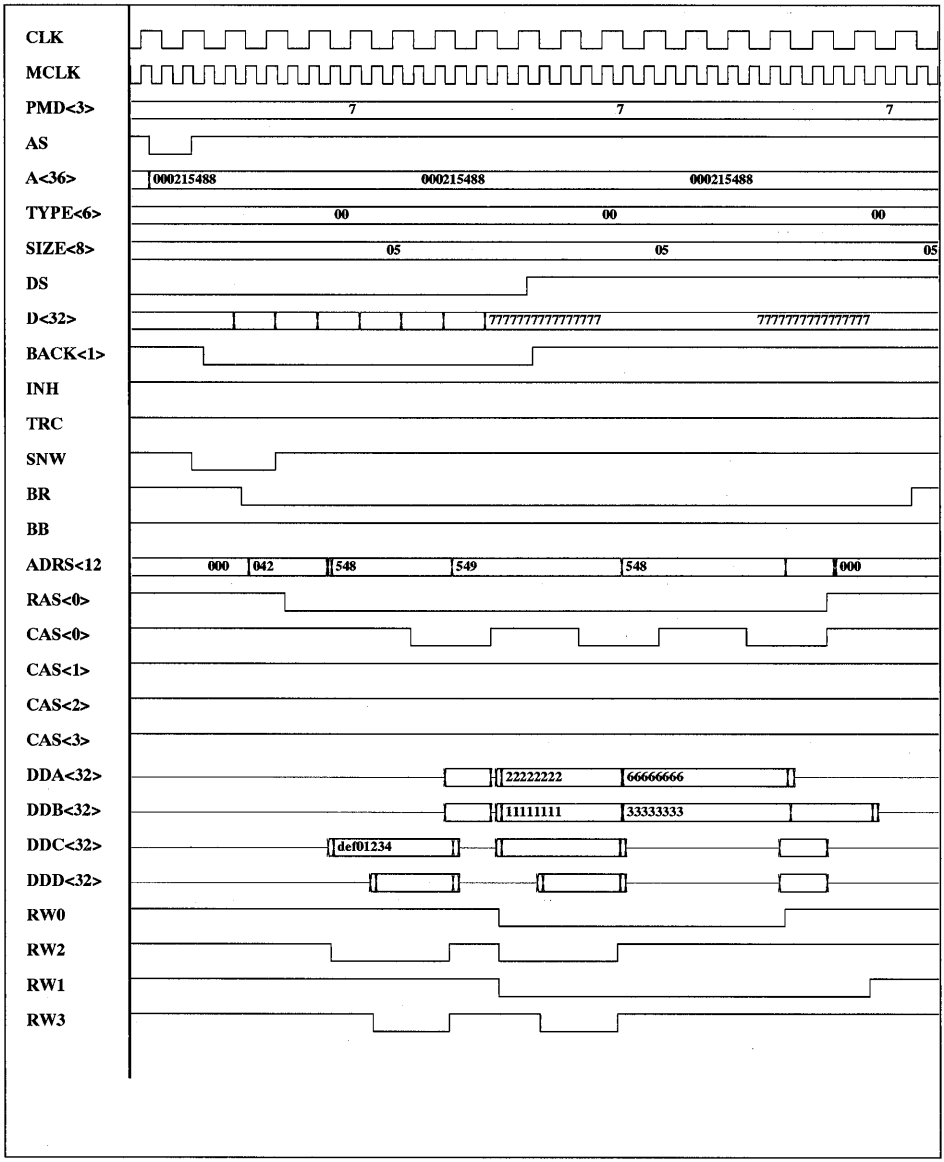
Timing Diagrams (continued)

Write Burst, Mode 11



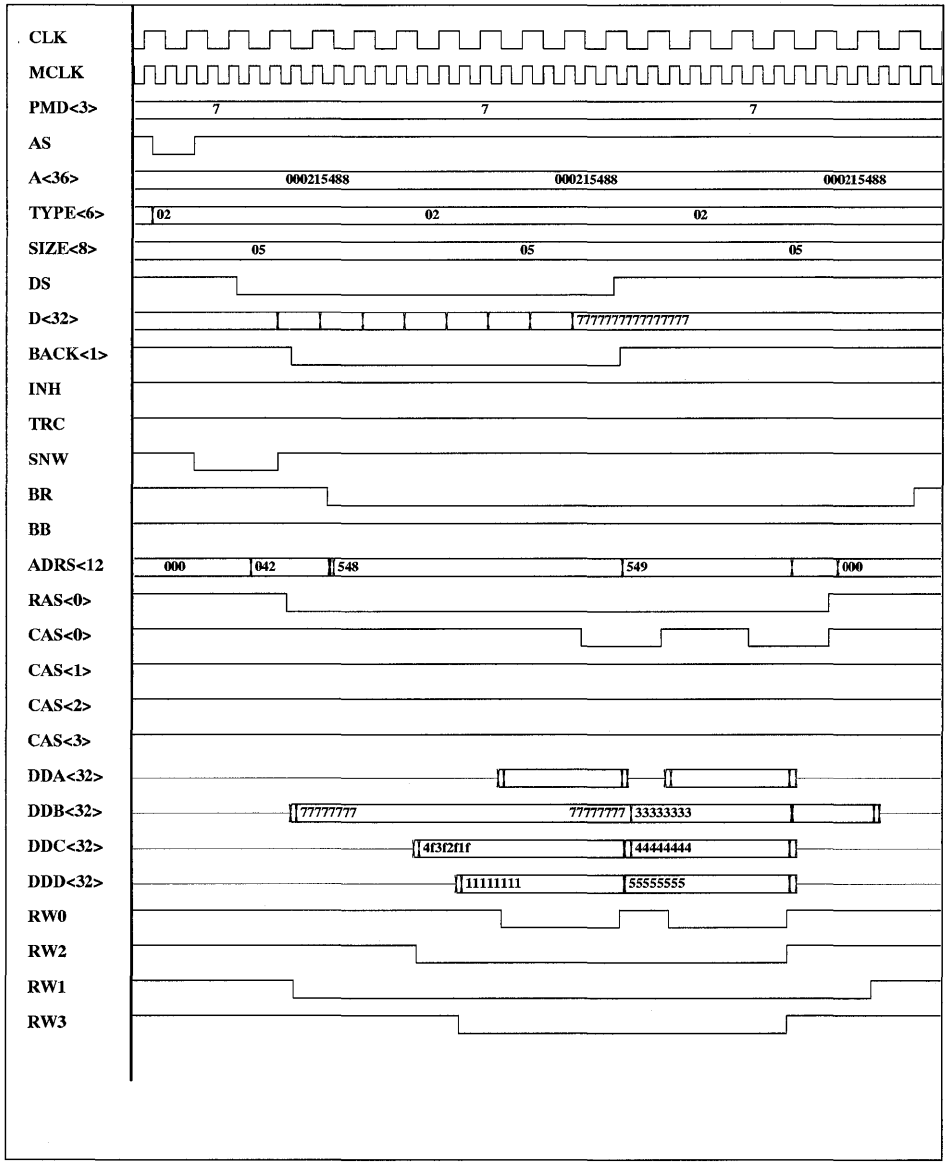
Timing Diagrams (continued)

Write 32 Bytes, Misaligned 32-Bit Bus



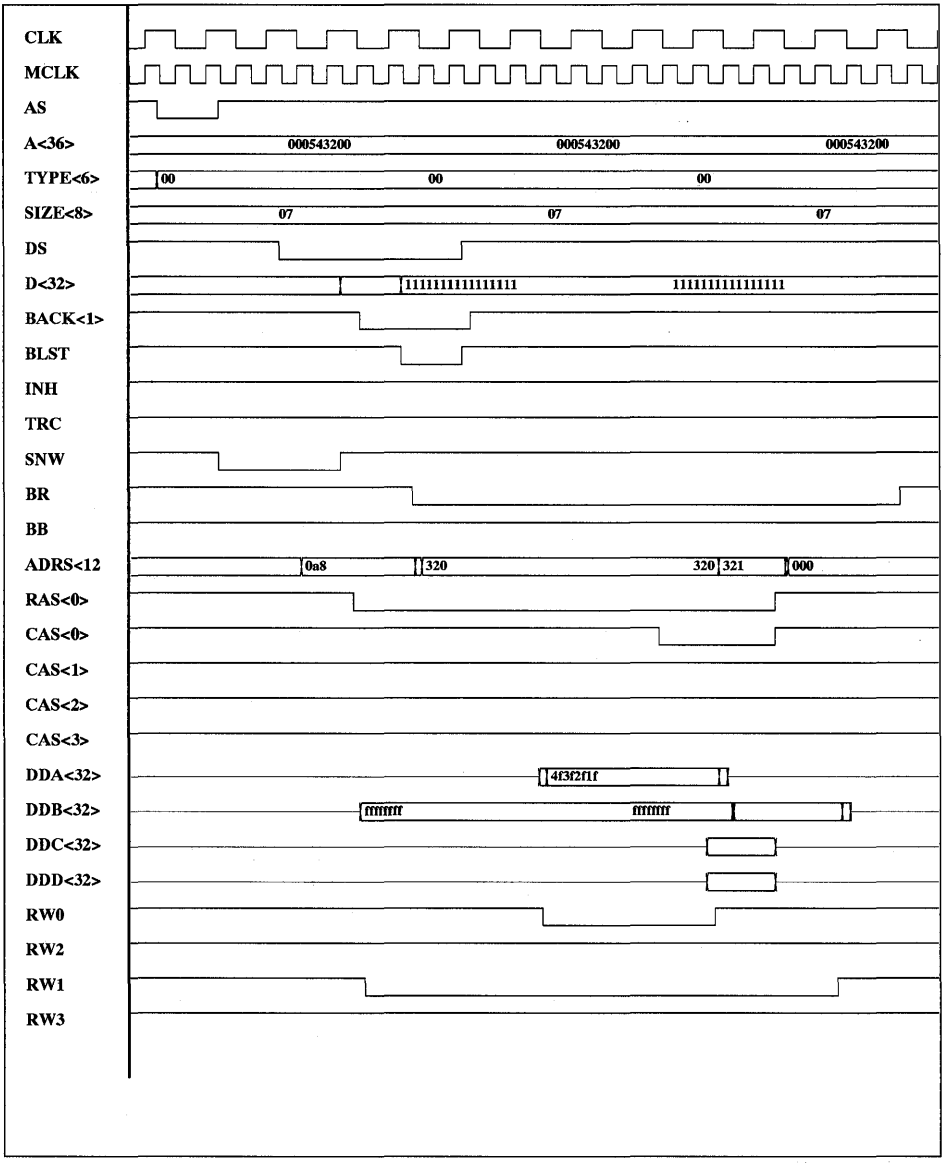
Timing Diagrams (continued)

Write 32 Bytes, Misaligned, Intel Order 32-Bit Bus



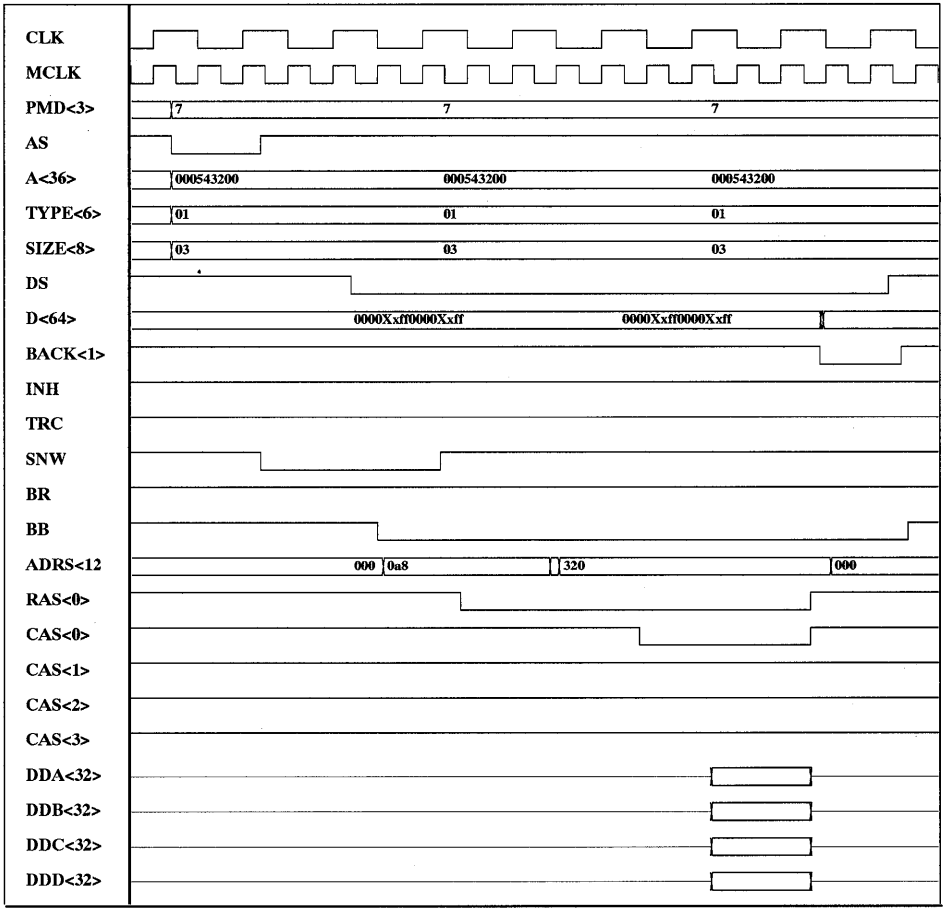
Timing Diagrams (continued)

Write with BLST, 32-Bit Bus



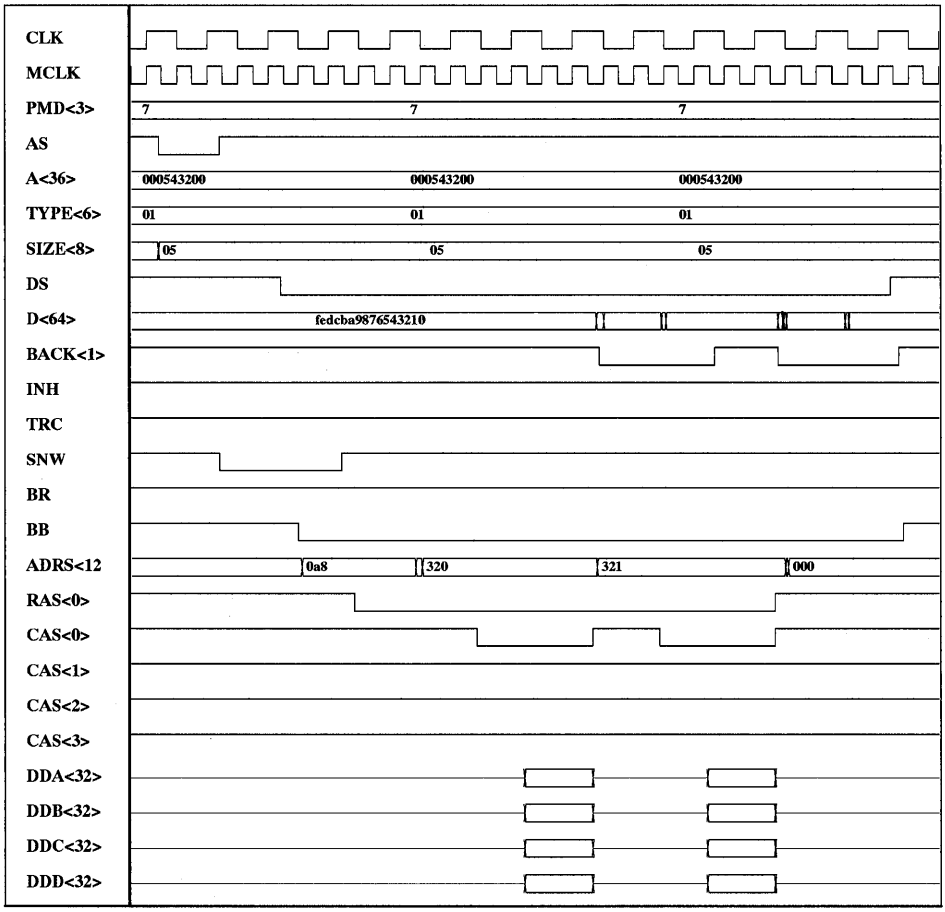
Timing Diagrams (continued)

Read Mode 01, 8 Bytes



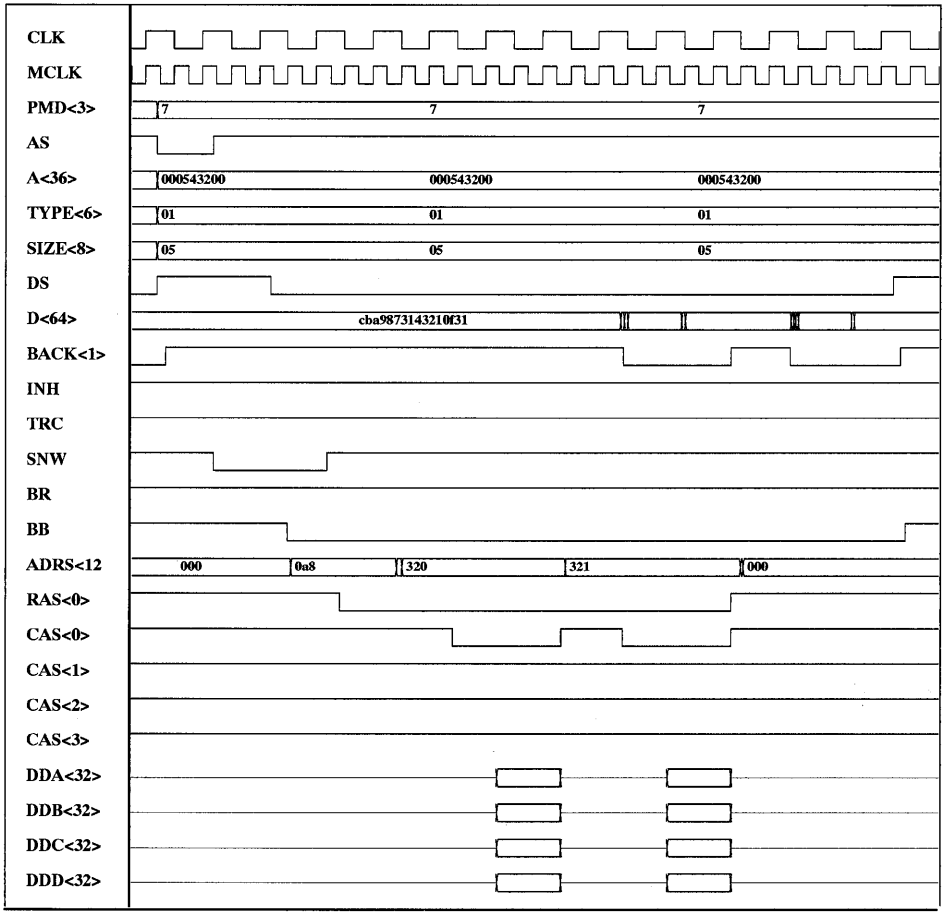
Timing Diagrams (continued)

Read Mode 01, 32 Bytes



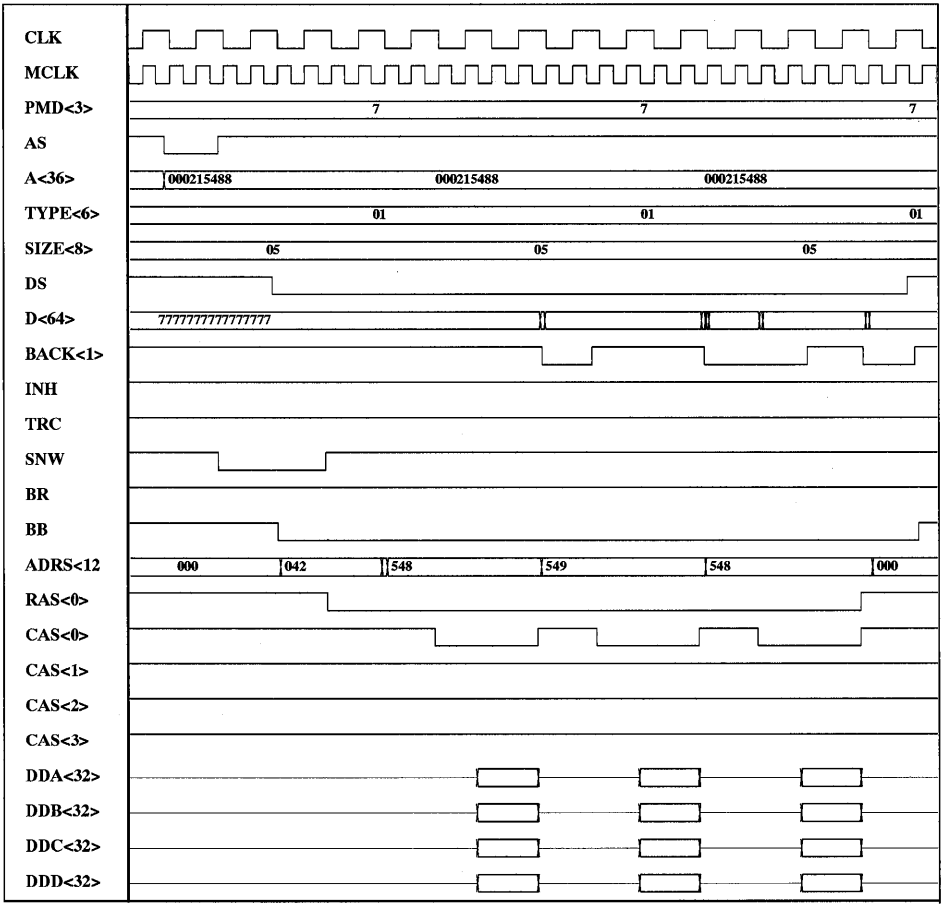
Timing Diagrams (continued)

Read Mode 01, Wait State, 32 Bytes



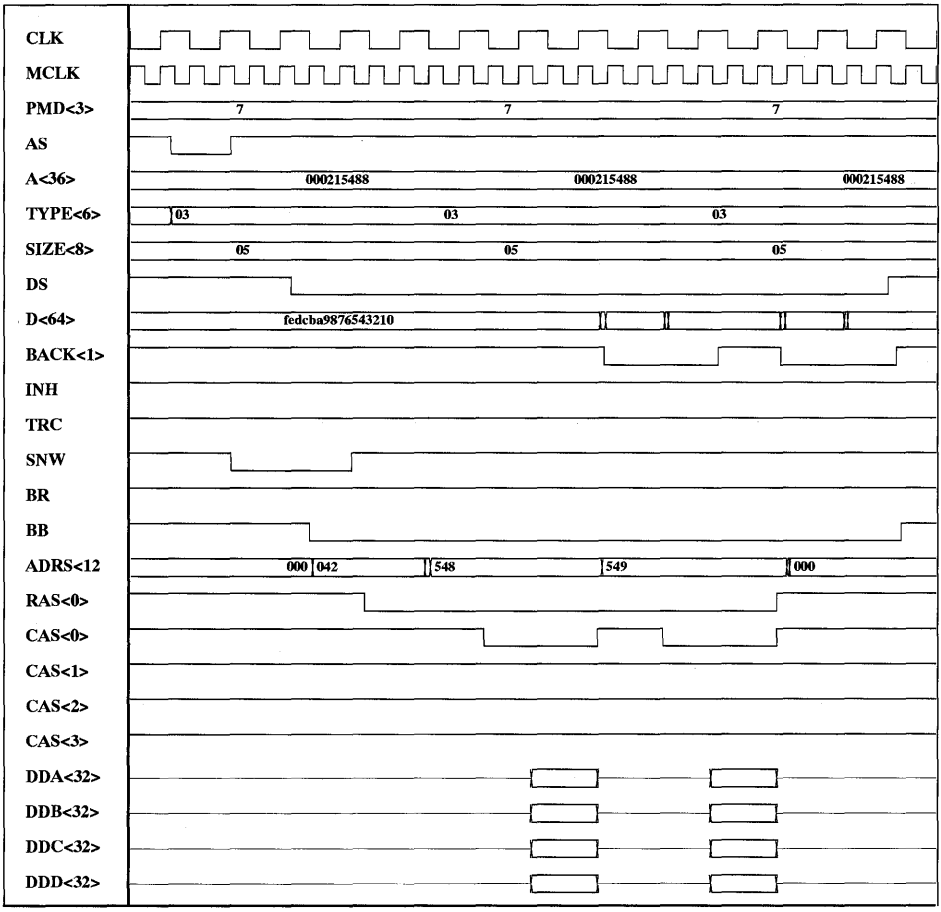
Timing Diagrams (continued)

Read Mode 01, Sequential, Misaligned



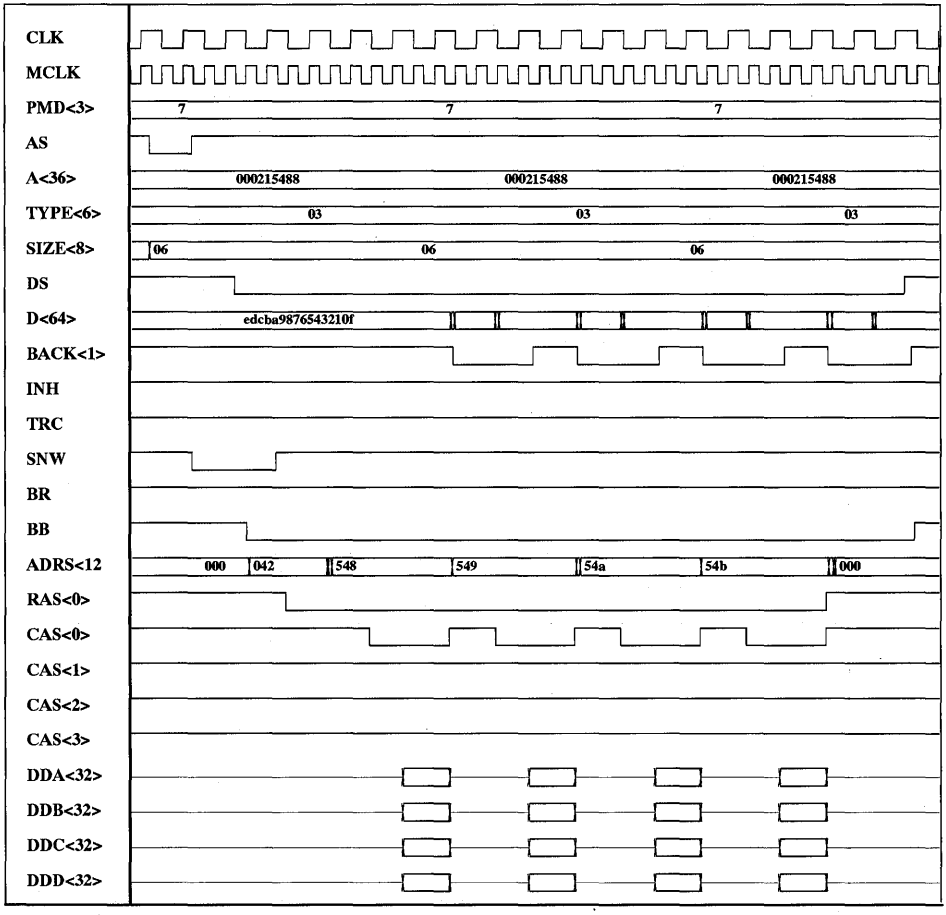
Timing Diagrams (continued)

Read Mode 01, Intel, Misaligned, 32 Bytes



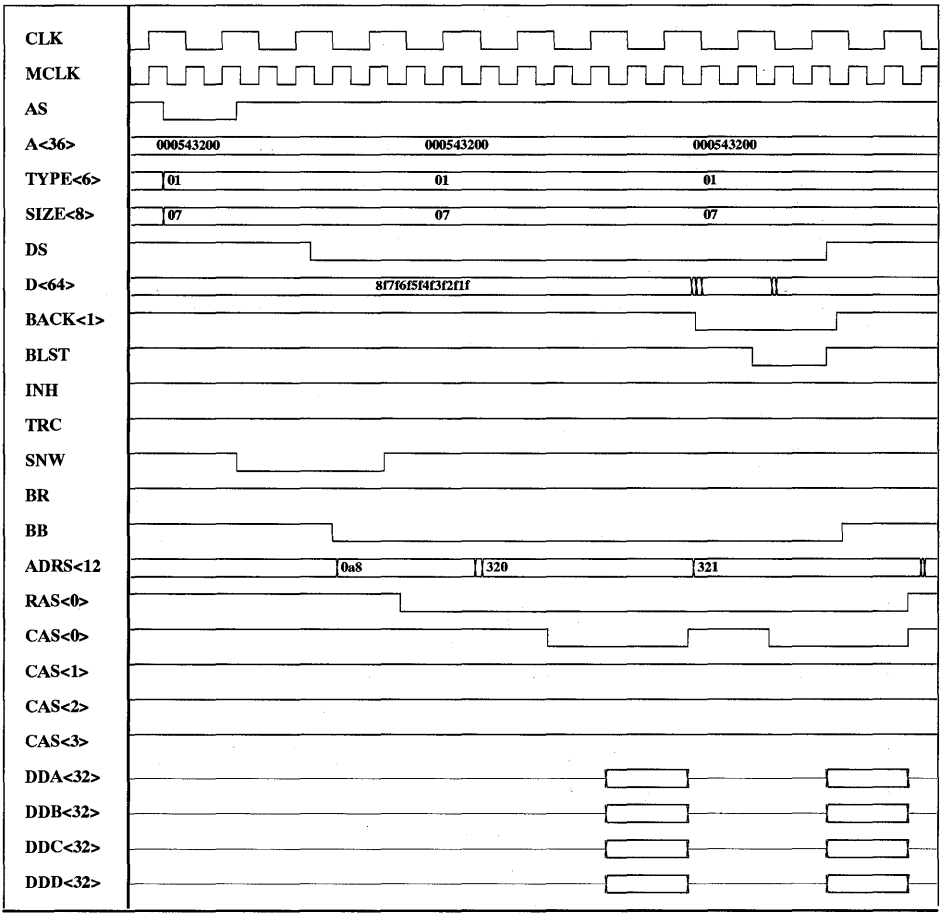
Timing Diagrams (continued)

Read Mode 01, Intel, Misaligned, 64 Bytes



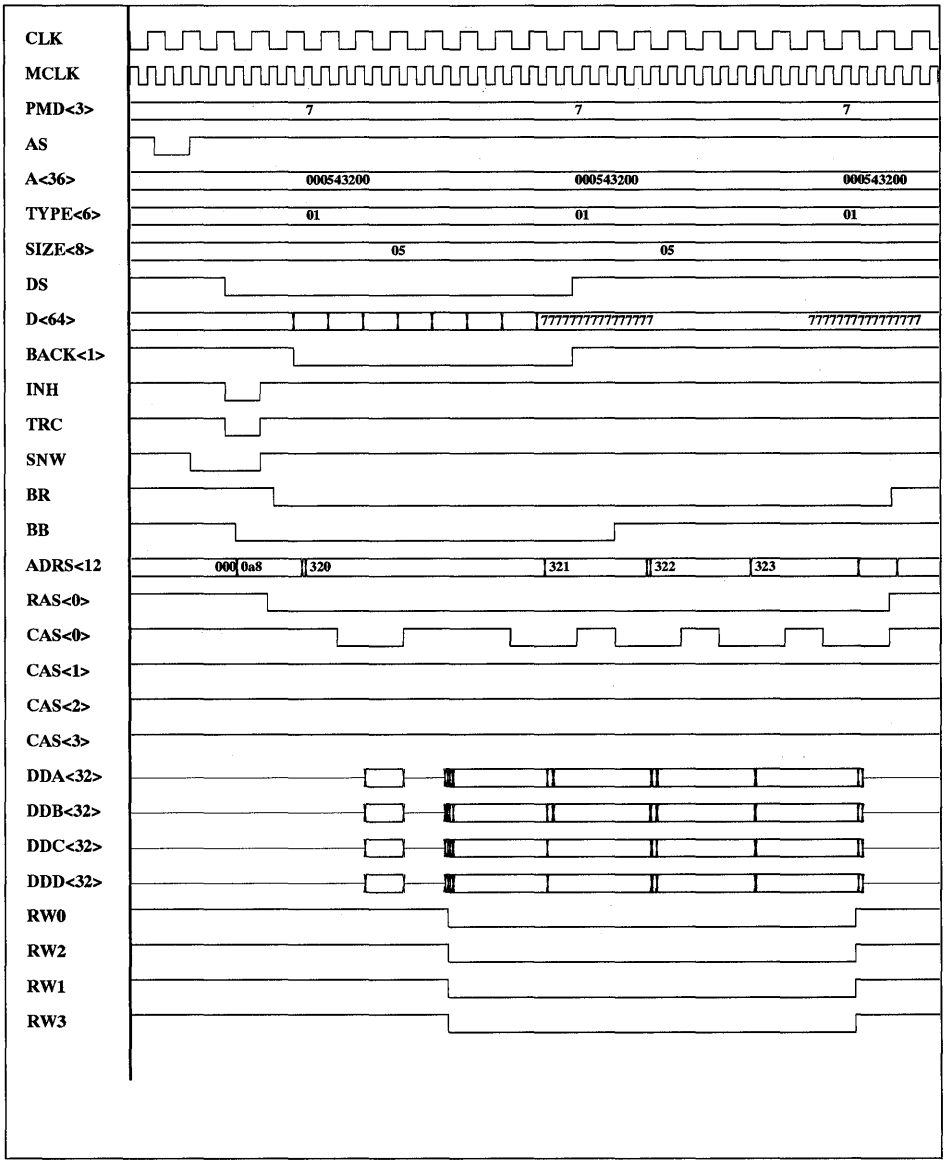
Timing Diagrams (continued)

Read with BLST Mode 01



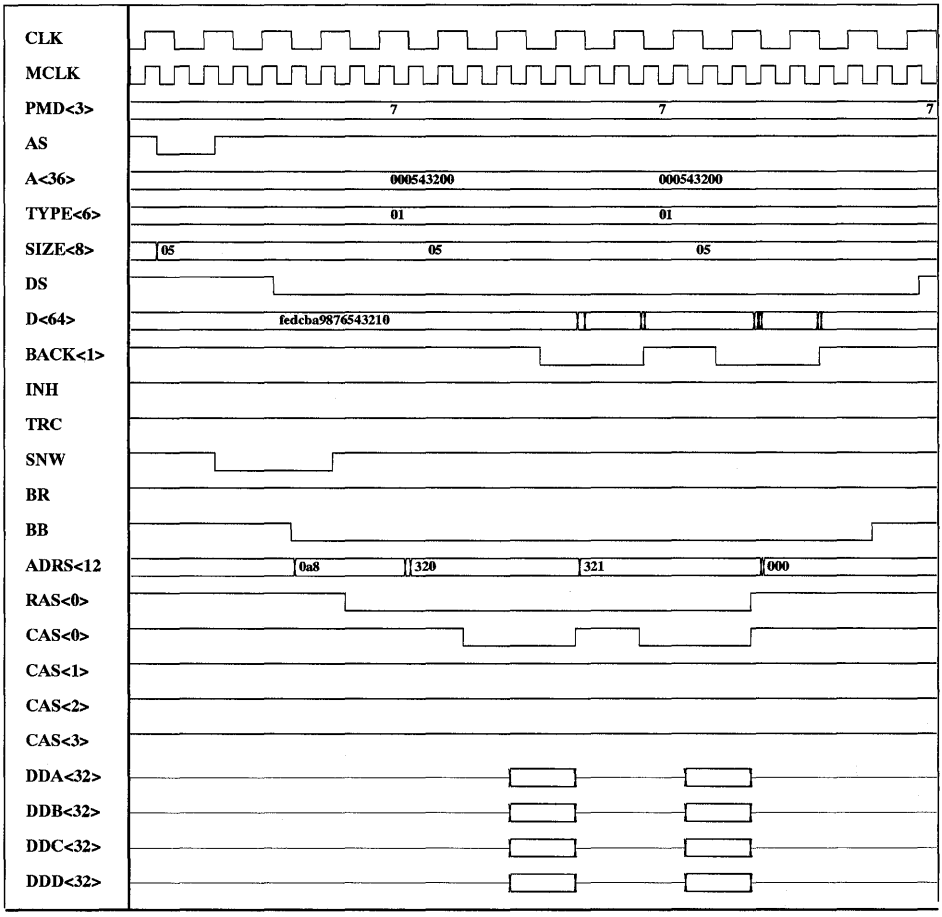
Timing Diagrams (continued)

Read Mode 01, Transformed



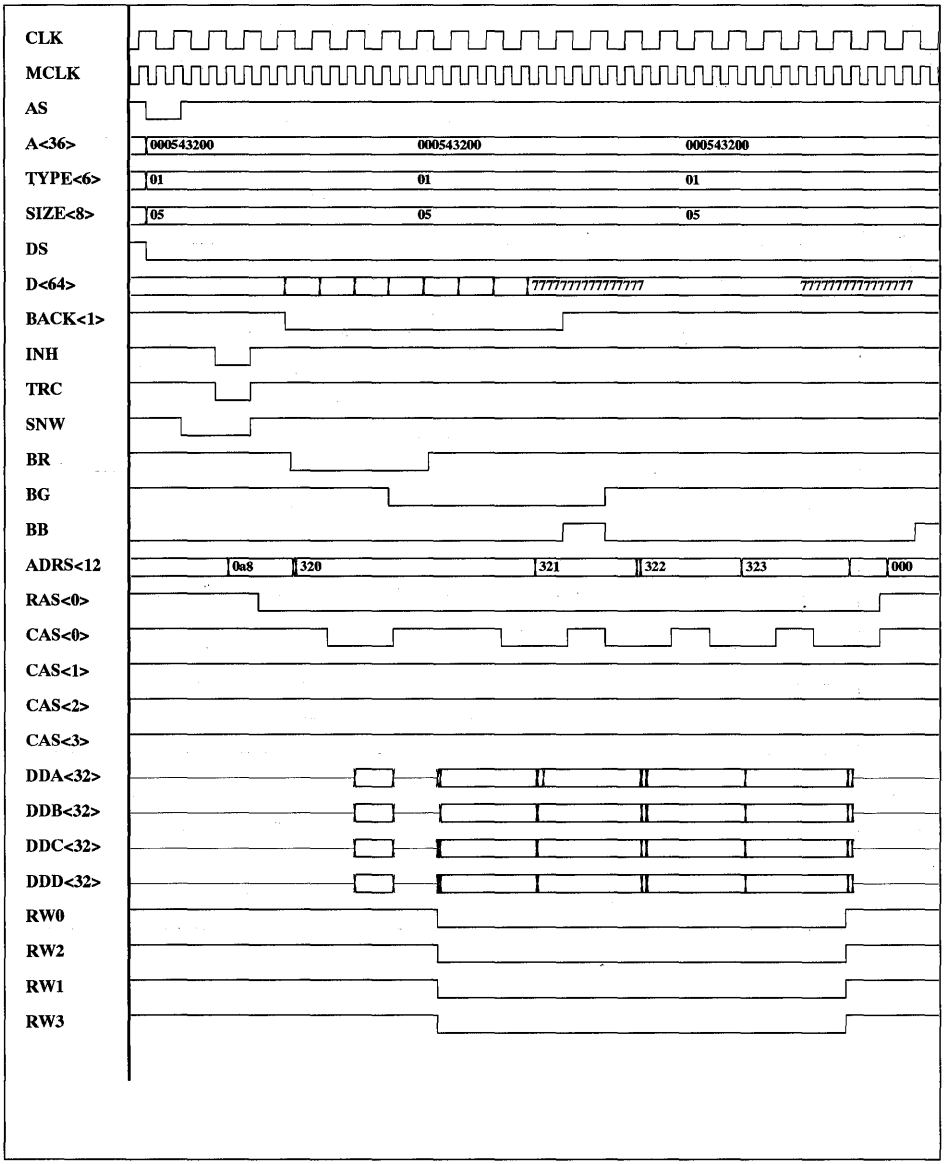
Timing Diagrams (continued)

Read Mode 11



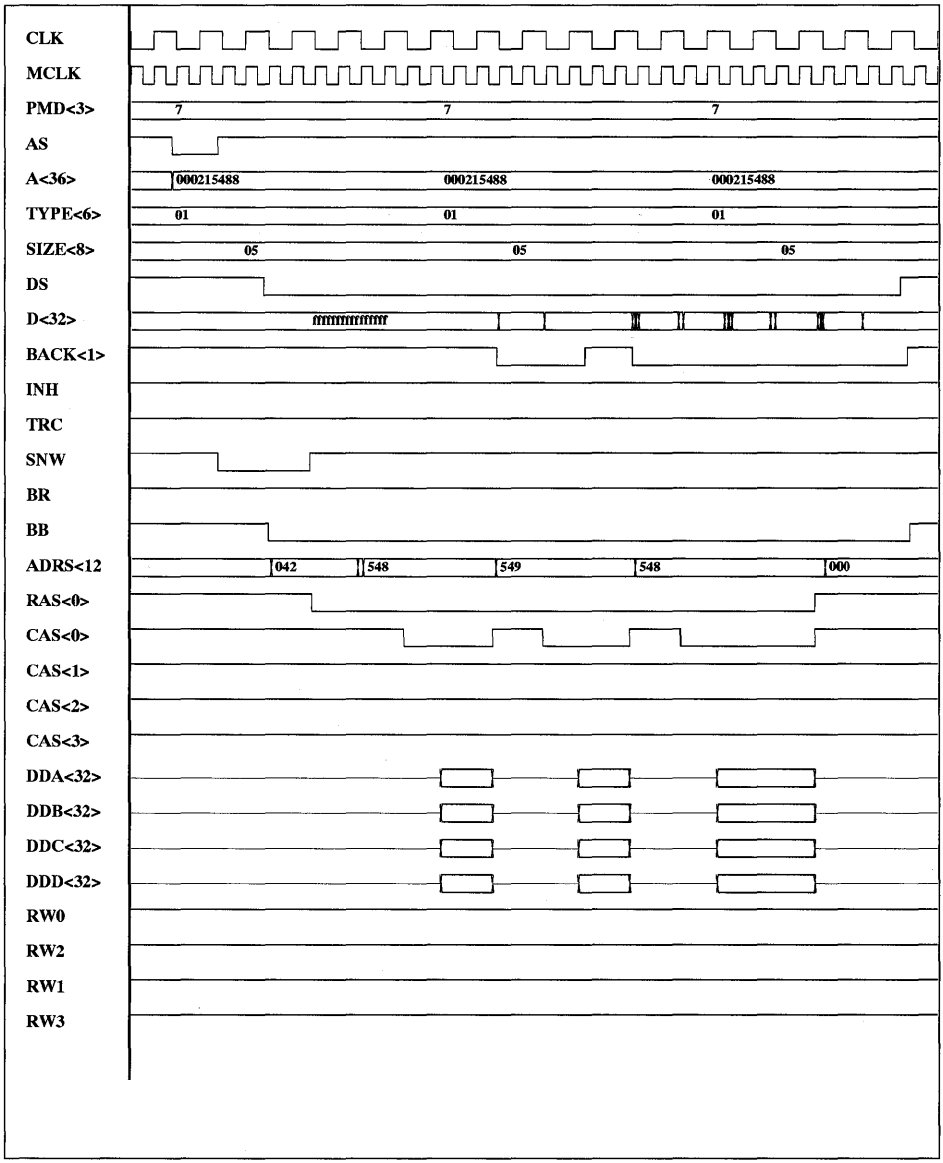
Timing Diagrams (continued)

Reflective Transaction Showing Bus Arbitration



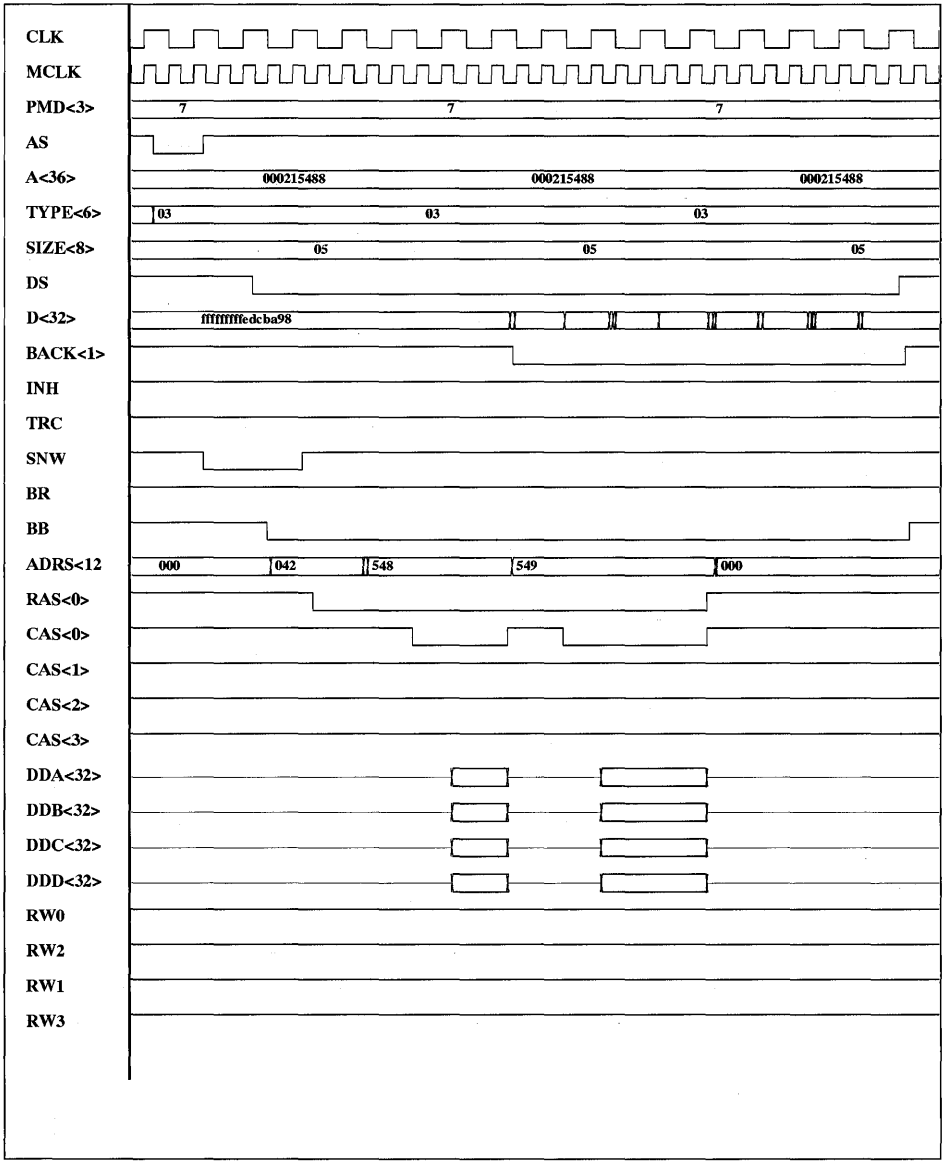
Timing Diagrams (continued)

Read 32 Bytes, Misaligned 32-Bit Bus



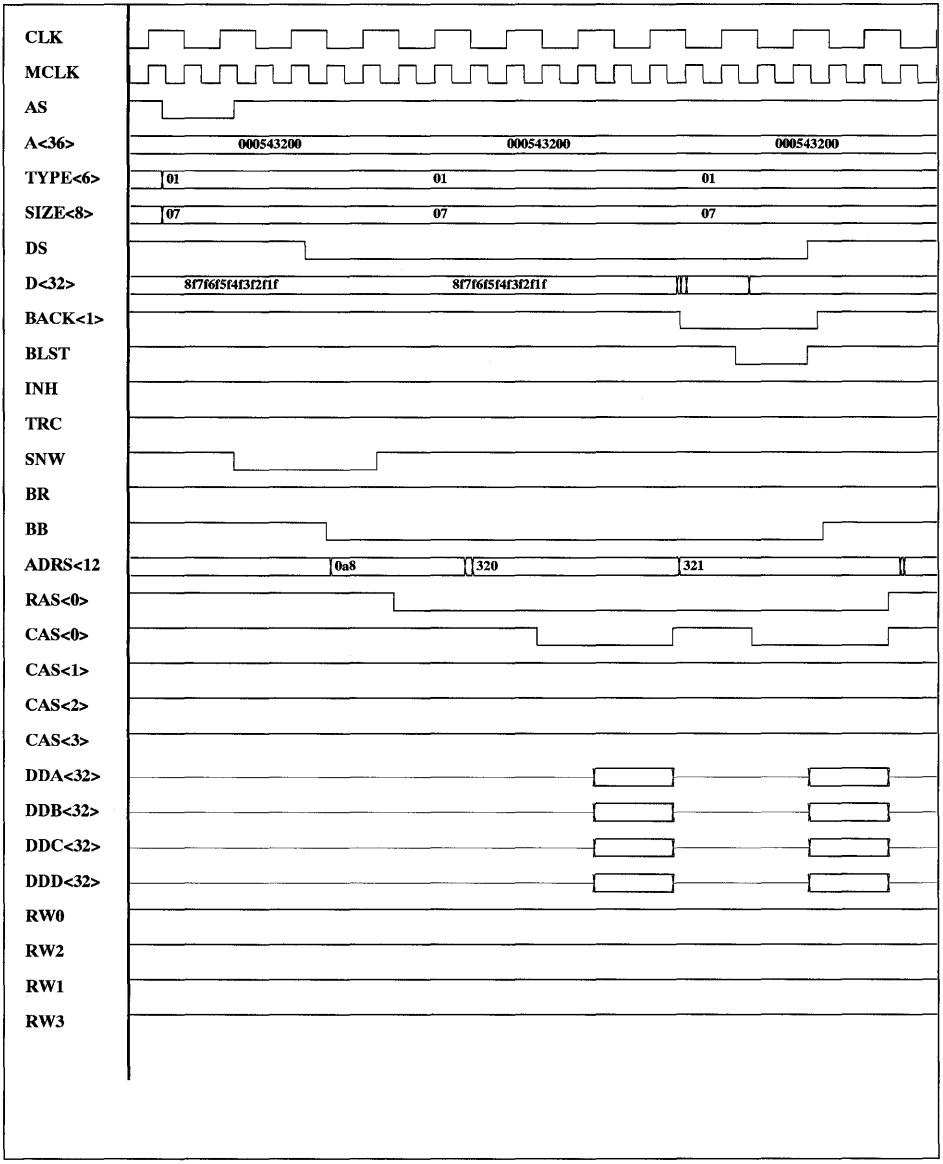
Timing Diagrams (continued)

Read 32 Bytes, Misaligned, Intel Order 32-Bit Bus



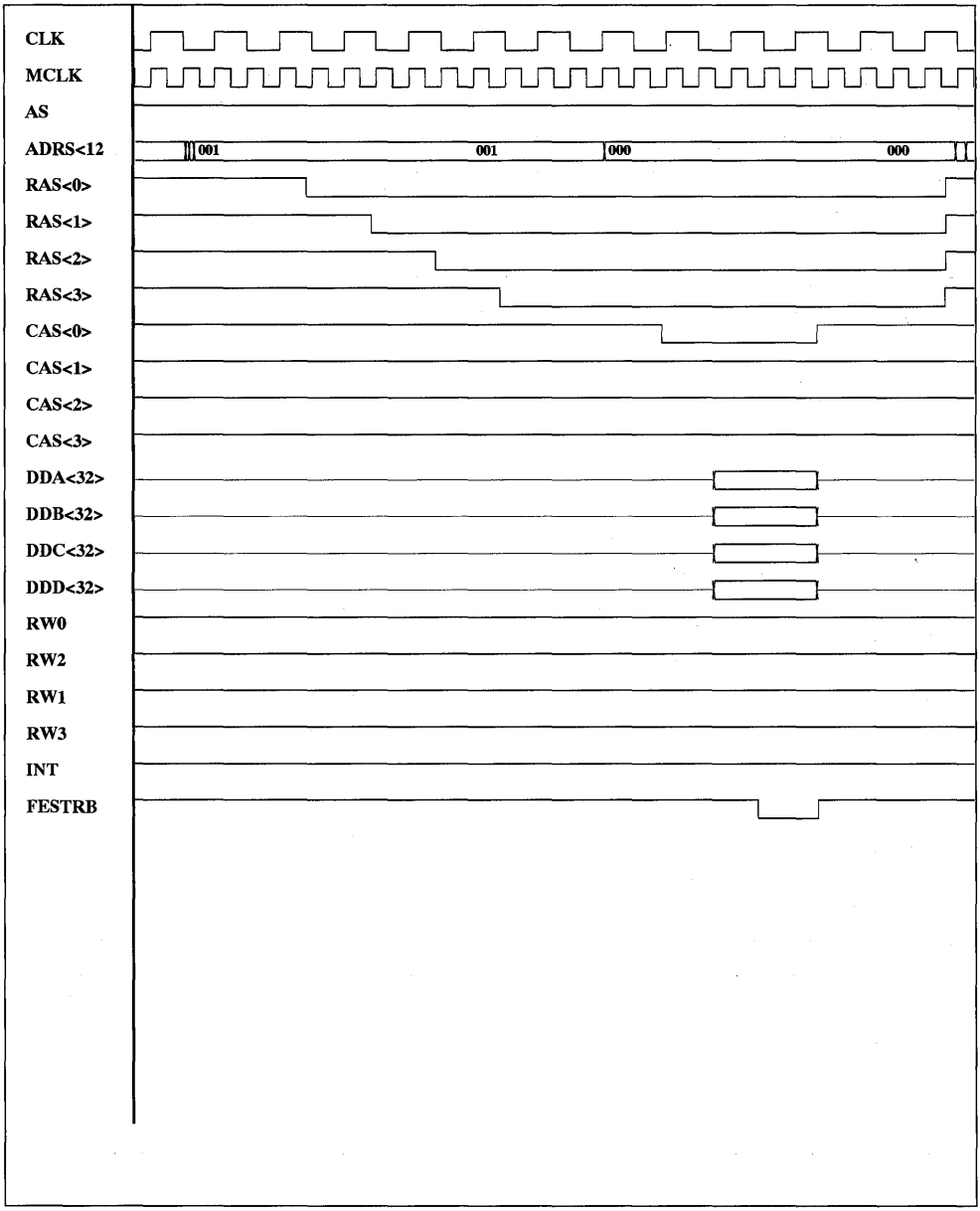
Timing Diagrams (continued)

Read with BLST, 32-Bit Bus



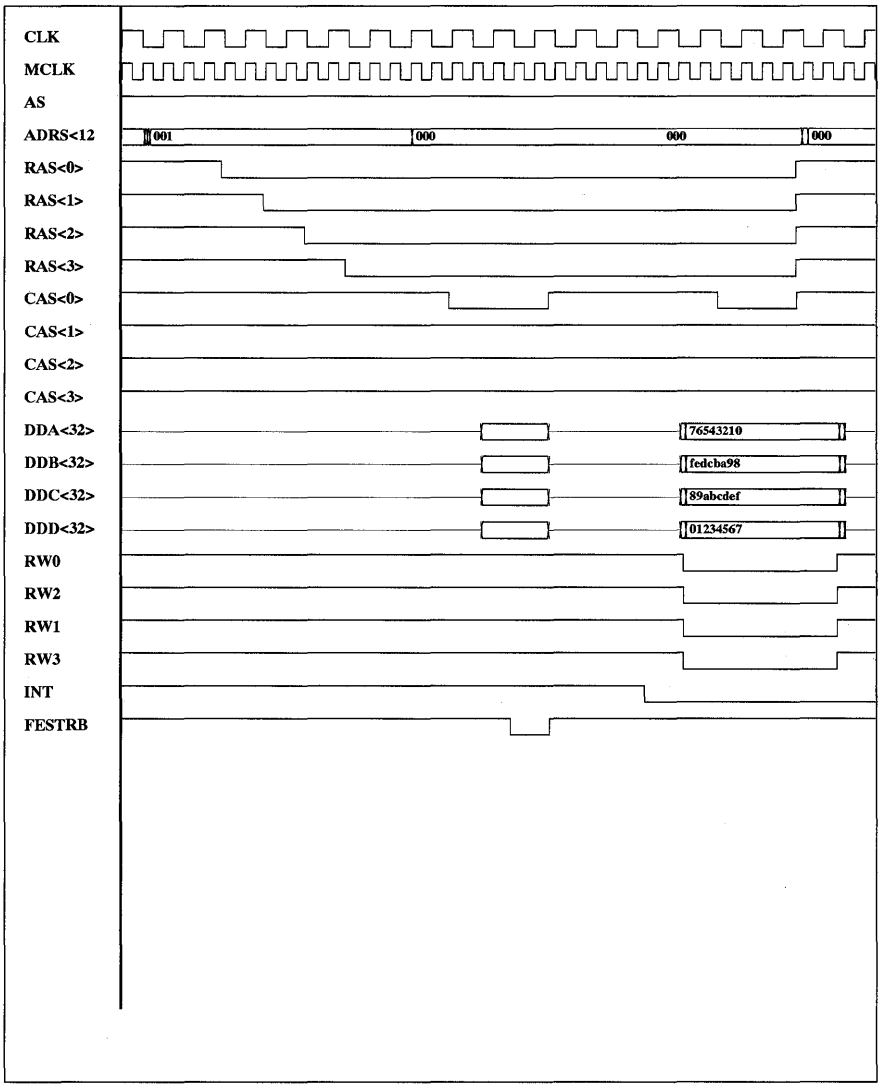
Timing Diagrams (continued)

Refresh, Staggered RAS, No Scrub, No Error in Data



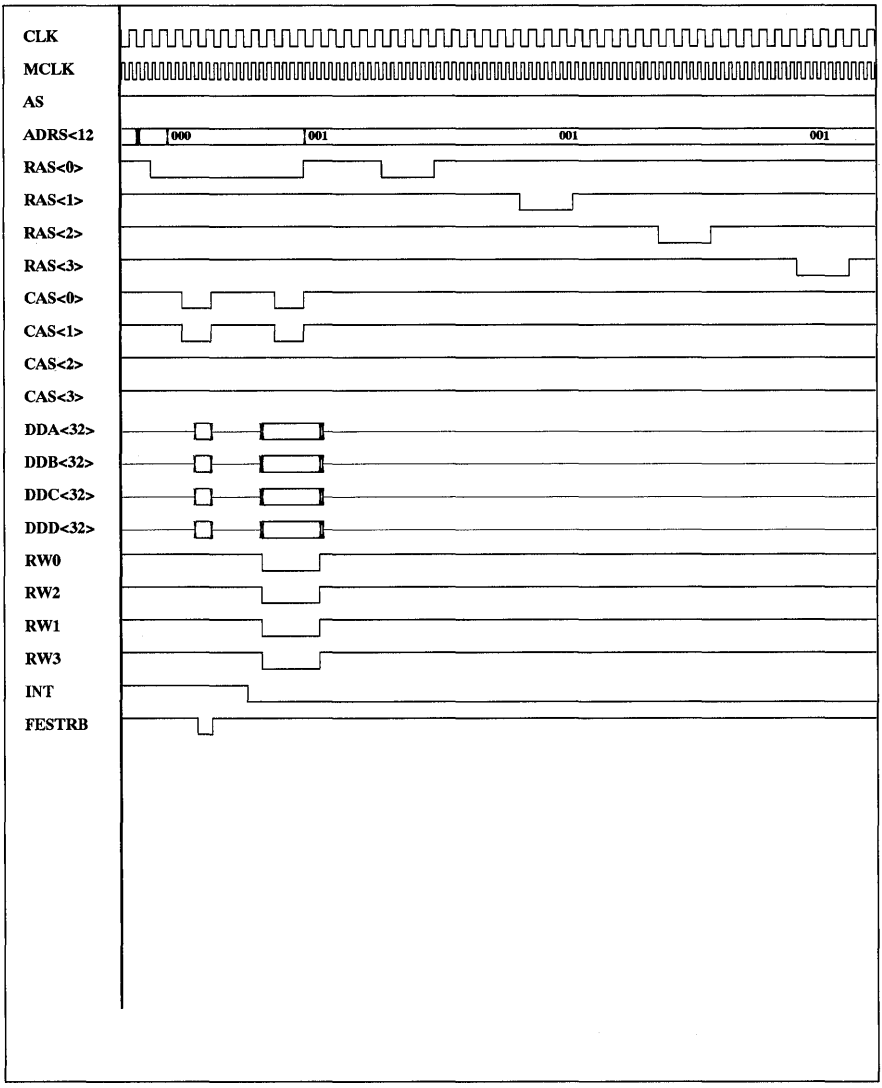
Timing Diagrams (continued)

Refresh, Staggered RAS, Scrub



Timing Diagrams (continued)

Refresh, Mutually Exclusive RAS, Scrub



Power Dissipation

The table below shows the estimated power dissipation for various bus clock frequencies under specific assumptions. The temperatures listed under the air flow column are the maximum ambient air temperature allowed for the frequency at the left and the air flow at the column top.

The assumptions are: DRAM bus load = 50 pF; system bus load = 100 pF; system bus data frequency is ½ of the system clock (NRZ); DRAM bus data frequency is ½ of the system clock (NRZ); and V_{CC} is 5.25V.

The data pattern assumptions are:

Reads: $^2/_3$ of all system bus cycles involve the CYM7232.
$^2/_3$ of all CYM7232 cycles are reads.
½ of the 64-bit system bus will toggle on average.
The CYM7232 drives the system bus $^1/_3$ of the time during a read.

Writes: $^2/_3$ of all system bus cycles involve the CYM7232.
$^1/_3$ of all CYM7232 cycles are writes.
½ of the 64-bit system bus will toggle on average.
The CYM7232 drives the system bus $^1/_6$ of the time during a write.

System Clock Frequency (MHz)	Power (watts)	Air Flow –LFM (C)				
		0	100	200	300	400
25	0.8	70	70	70	70	70
33	1.0	60	60	60	70	70
40	1.2	60	60	60	60	60

Socket Data

Test ZIF Socket: Textool 3M Grid ZIP PGA Kit 25 x 25
Socket Part # 2–0000–06325–170–024–000
PGA Pin (gold plated) Part# 3–0000–02740–006–000–002
PGA Pin (nickel plated) Part# 3–0000–02740–006–000–005

Test Receptacle: Procon Part# 228–401–1001–2525
(uses Millmac 0400 Pins Part# 0400–0–15–01–47–27–0400)

Production Socket: McKenzie Part# PGA401H009B2–2406R

Installation Lubricant: Tech Spray Part# 2111–P (Goldfinger Glove)

Extraction Tool: McKenzie Part# TOLPGAX–41622–001 (CYM7232)
TOLPGAX–41622–002 (CYM7264)

McKenzie, 44370 Old Warm Springs Boulevard, Fremont, CA 94538 (510) 651–2700

Tech Spray, P.O. Box 949, Amarillo, TX 79105 (806) 372–8523

Procon Tech., 1333 Lawrence Expwy., Suite 207, Santa Clara, CA 95051 (408) 246–4456

Textool, 6801 Riverplace Blvd., Austin, TX 78726 (800) 328–0411

Ordering Information

Speed (MHz) Bus/DRAM	Ordering Code	Package Name	Package Type	Operating Range
40/80	CYM7232S–40HGC	HG02	401-Pin PGA Module	Commercial
33/99	CYM7232H–33HGC	HG02	401-Pin PGA Module	Commercial
33/66	CYM7232S–33HGC	HG02	401-Pin PGA Module	Commercial
25/100	CYM7232H–25HGC	HG02	401-Pin PGA Module	Commercial
25/75	CYM7232S–25HGC	HG02	401-Pin PGA Module	Commercial

Speed (MHz) Bus/DRAM	Ordering Code	Package Name	Package Type	Operating Range
40/80	CYM7264S–40HGC	HG03	401-Pin PGA Module	Commercial
33/99	CYM7264H–33HGC	HG03	401-Pin PGA Module	Commercial
33/66	CYM7264S–33HGC	HG03	401-Pin PGA Module	Commercial
25/100	CYM7264H–25HGC	HG03	401-Pin PGA Module	Commercial
25/75	CYM7264S–25HGC	HG03	401-Pin PGA Module	Commercial

Document #: 38–M–00051–C

CYPRESS SEMICONDUCTOR

128K Write-Through Secondary Cache Module

Features

- **128-Kbyte direct-mapped, write-through, zero-wait-state secondary cache module**
- **Operates with 33-MHz Intel 486 processors**
- **Uses low-cost CMOS asynchronous SRAMs as cache data storage and cache tag storage**
- **Supports self-invalidation**
- **64-position dual-read-out SIMM with 128 leads**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

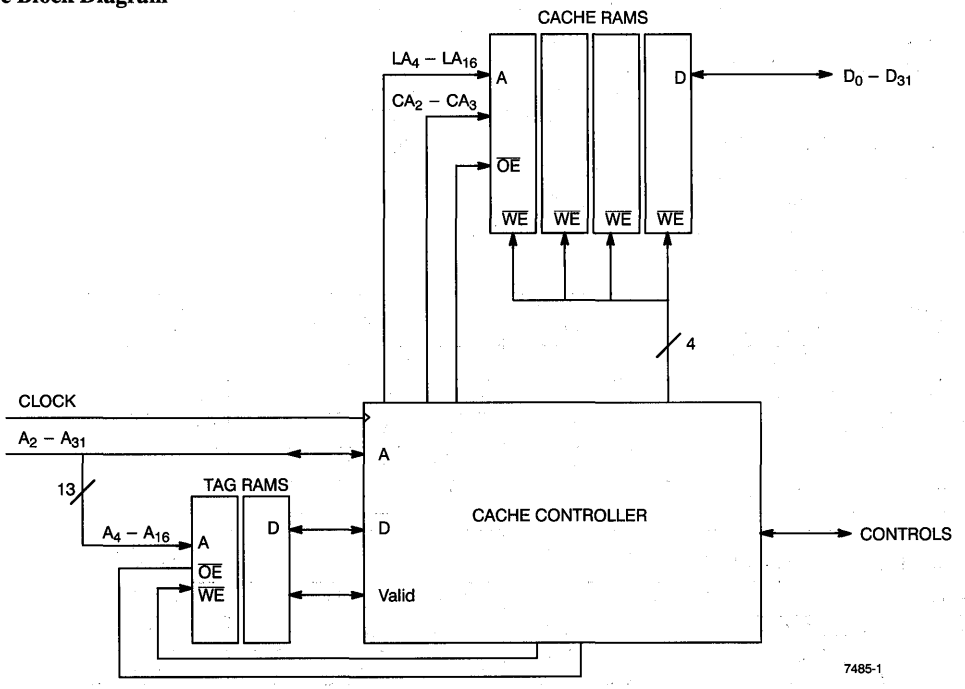
Functional Description

The CYM7485 is a self-contained 128-Kbyte direct-mapped, zero-wait-state, write-through secondary cache module designed for use in Intel 486-based systems. The line size is 16 bytes. Cache data is stored in four 32K by 8 asynchronous SRAMs, and the tag addresses are stored in two 8K by 8 asynchronous SRAMs.The address from the processor is captured by high-speed transparent latches at the beginning of each access and the lowest two address bits are incremented according to the Intel burst sequence during burst reads and cache line fills.

The on-board cache controller coordinates accesses to the cache memory. During a read hit, four 32-bit words are read from the cache RAMs and returned to the processor without wait states. If the read location requested by the processor is not found in the cache, the memory controller will hold the processor and retrieve the missing line from the main memory. During write cycles, the main memory is always updated with the data from the processor. If the write location is found in the cache, then the cache content is updated as well.

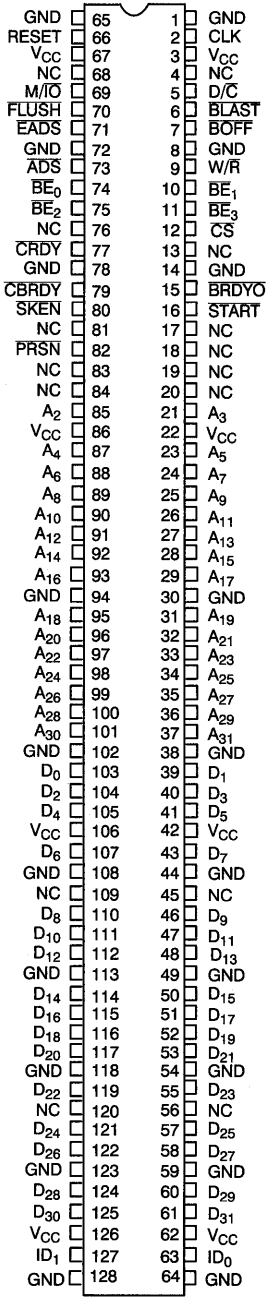
All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board.The package dimensions are 3.85″ x 0.200″ x 1.5″. All inputs and outputs of the CYM7485 are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

Logic Block Diagram



Pin Configuration

SIMM
Top View



7485-2

Pin Descriptions

Symbol	Parameter	Type	Pins	Active	Description
CLK	Clock	I	1	N/A	This input is the timing reference for all module functions. It is the same as the i486 clock.
RESET	Reset the Cache	I	1	HIGH	RESET is sampled at each clock rise. If it is true, the cache logic will be placed in the idle state. RESET will not invalidate the cache contents.
$\overline{ADS}$	Address Strobe	I	1	LOW	$\overline{ADS}$ is connected to the $\overline{ADS}$ signal from the i486. It is used to start read or write cycles. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	Memory/IO	I	1	N/A	This signal is used by the i486 to distinguish between memory and IO accesses. The module will not cache IO accesses.
W/$\overline{R}$	Write/Read	I	1	N/A	A LOW indicates a read cycle. A HIGH indicates a write cycle.
D/$\overline{C}$	Data/Control	N/A	1	N/A	This signal is not used by the CYM7485.
$\overline{START}$	Memory Start	O	1	LOW	$\overline{START}$ is asserted during read miss and write cycles. It signals the main memory to service the current access.
$\overline{BRDYO}$	Burst Ready Out	O	1	LOW	This signal is asserted during read hits only. It indicates to the i486 that valid data from the cache is available. $\overline{BRDYO}$ is deasserted during other accesses.
$\overline{CBRDY}$	Cache Burst Ready In	I	1	LOW	This signal is asserted when burst data from the system is ready to be sampled by the i486 and the cache module.
$\overline{CRDY}$	Cache Ready In	I	1	LOW	This signal is asserted when non-burst data from the system is ready to be sampled by the i486 and the cache module.
$\overline{BLAST}$	Burst Last	I	1	LOW	$\overline{BLAST}$ is asserted by the i486 when the current cycle is the last cycle of a burst access.
$\overline{BOFF}$	Back-off	I	1	LOW	$\overline{BOFF}$ is sampled at each clock rise except the rising edge of T1 in a i486 access. If $\overline{BOFF}$ is asserted, the cache module will place its data lines in a three-stated condition. In addition, $\overline{START}$ and $\overline{BRDYO}$ will be deasserted.
$\overline{PRSN}$	Presence	O	1	LOW	This signal is tied to ground. It indicates to the system that the cache module is present.
$A_2 - A_{31}$	Address Lines	I	30	N/A	Address inputs to the CYM7485.
$\overline{BE}_0 - \overline{BE}_3$	Byte Enables	I	4	LOW	These signals are used during write cycles to determine which byte(s) will be written.
$\overline{CS}$	Chip Select	I	1	LOW	For normal accesses, $\overline{CS}$ must be LOW before $\overline{ADS}$ or $\overline{EADS}$ can be recognized. If $\overline{CS}$ is HIGH and $\overline{ADS}$ is LOW, the cache line selected by the address on $A_2 - A_{31}$ will be invalidated.
$D_0 - D_{31}$	Data Lines	I/O	32	N/A	Data lines to/from the i486, main memory, and other system components. $D_0 - D_7$ is the low byte.
$\overline{SKEN}$	System Cache Enable	I	1	LOW	This signal is generated by the system to inform the i486 and the cache module that the current line is cachable. During a cache line fill, $\overline{SKEN}$ is sampled one clock cycle before the first word is returned and one clock cycle before the last word of the line is returned.
$\overline{FLUSH}$	Cache Flush	I	1	LOW	If $\overline{FLUSH}$ is LOW and $\overline{ADS}$ is LOW, then the cache line selected by the address on $A_2 - A_{31}$ will be invalidated.
$\overline{EADS}$	Valid External Address	I	1	LOW	If $\overline{EADS}$ is asserted together with $\overline{CS}$, then the cache line selected by the address on $A_2 - A_{31}$ will be invalidated if a match is found.
$ID_0 - ID_1$	Cache Size Selector	O	2	N/A	These two lines are not connected on the cache module. They are tied externally to V_{CC} to select a cache size of 128K bytes.

Basic Operation

The CYM7485 is a complete 128-Kbyte, direct-mapped secondary cache subsystem designed to work with 33-MHz Intel 486 processors. The cache memory is divided into 8K 16-byte lines and each line is assigned a dedicated entry in the cache tag RAM. The CYM7485 supports zero-wait-state operations: it can return four words from its cache memory in five clock cycles (i.e., 2-1-1-1). A write-through cache policy is implemented to provide data integrity.

Four 32K by 8 asynchronous SRAMs provide the 128-Kbyte cache storage and two 8K by 8 asynchronous SRAMs store the 8K 16-bit tag entries. Each tag entry is divided into a 15-bit tag field (to support the 4-Gbyte processor address space) and a valid bit. During an access, the contents of the tag entry selected by processor address bits, A_4 – A_{16}, are delivered to two 8-bit comparators where they are matched against the 15 upper order address bits from the i486. A match is declared only if the two set of addresses are identical and the valid bit of the tag entry is set.

Addresses from the processor are captured by transparent latches before they are delivered to the cache memory. The lowest two address bits (A_2 and A_3) are incremented by the cache controller according to the Intel burst order during read hits and line fills (see *Table 1*).

The following functions are not supported in the CYM7485: data parity (DP_0 - DP_3), write protect ($\overline{WP}$), write protect strap ($\overline{WPSTRAP}$), cache enable to CPU ($\overline{CKEN}$), software flushes, and global cache invalidation.

Read Cycles

A read cycle is initiated when $\overline{ADS}$, $\overline{CS}$, and W/$\overline{R}$ are sampled LOW at clock rise with M/$\overline{IO}$ sampled HIGH. The processor address is captured by a set of transparent latches as soon as the access is started. The latch will remain closed until the access is completed or until $\overline{BOFF}$ is asserted (LOW). $\overline{BE_0}$ – $\overline{BE_3}$ are ignored in all read accesses.

Tag look-up begins whenever a valid processor address is available. Processor address lines are connected to the two tag RAMs directly to reduce the tag match delay. If the requested location is found in the cache, the CYM7485 will return the first burst word in the first T2 cycle. This is followed by three more words delivered once every clock until the last word is returned or until $\overline{BLAST}$ is asserted. $\overline{START}$ is pulled HIGH in T2 to signal a cache hit to main memory and $\overline{BRDYO}$ is pulled LOW in T2 to signal the processor that valid data is available from the cache. $\overline{BRDYO}$ remains LOW until the last word is returned.

If the requested location is not in the cache, then the cache controller will assert $\overline{START}$ (LOW) to initiate the main memory access and deassert $\overline{BRDYO}$ (HIGH) to hold the processor.The CYM7485 cannot accept data from main memory in zero wait states.The earliest cycle in which main memory data is accepted is the second clock cycle after $\overline{START}$ is asserted. The minimum cache line fill sequence from main memory is 4/3/3/3.

$\overline{BLAST}$ is sampled concurrently with $\overline{CBRDY}$ and $\overline{CRDY}$. If $\overline{BLAST}$ is sampled LOW before the fourth data transfer, then the line fill operation is aborted. Data from main memory is considered cachable if $\overline{SKEN}$ is sampled LOW at least one clock cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first asserted (LOW). If this condition is satisfied, the data returned from main memory will be written into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. If $\overline{SKEN}$ is sampled HIGH when the first $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW, or if $\overline{SKEN}$ is sampled LOW concurrently with the first $\overline{CBRDY}$ or $\overline{CRDY}$, then the data is considered to be non-cachable and the cache module will not act on the information.

$\overline{SKEN}$ is sampled again at the end of the line fill to validate the cache line. If $\overline{SKEN}$ is sampled LOW one cycle before the fourth time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW, then the cache line will be validated.

In order to process the read miss line fill correctly, A_4–A_{31} from the processor must remain stable throughout the line fill. Otherwise, the cache tag will not be updated properly. In addition, $\overline{SKEN}$ must be LOW t_{14} before the end of T2 and remain LOW until the line fill is completed.

If the read access is not cachable, then $\overline{SKEN}$ will be sampled HIGH after T2. The CYM7485 supports the following types of non-cachable read accesses. If a single read hit is detected, then the data word will be returned with $\overline{BRDYO}$ asserted. If a single read miss is found, $\overline{START}$ will be asserted to begin the main memory access. However, the data returned will not be stored into the cache memory and the selected cache line is not validated. If a burst read hit is detected, the cache module will treat it in the same manner as a cachable burst read hit (i.e., four words will be retrieved from the cache memory with $\overline{BRDYO}$ asserted). On the other hand, if a burst read miss is found, then $\overline{START}$ will be asserted to begin the main memory access. However, the four words returned by the main memory will not be stored into the cache and the selected cache line is not invalidated. *Table 2* illustrates the various cachable/non-cachable and single/burst access combinations.

Table 1. Intel Burst Sequence

First Address	Second Address	Third Address	Fourth Address
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

Table 2. Cachable/Non-cachable and Single/Burst Read Access Combinations

$\overline{SKEN}$	$\overline{BLAST}$ at end of T2	Hit / Miss	Action
0	0	Read hit	Cachable single read access. Cache module will return the word from its memory, assert $\overline{BRDYO}$, and then return to the idle state.
0	1	Read hit	Cachable burst access. This is the normal read hit case. Cache module will return 4 words from its memory with $\overline{BRDYO}$ asserted. Less than 4 words will be returned if $\overline{BLAST}$ is asserted before the end of the burst sequence.
1	0	Read hit	Non-cachable single read access. Cache module will return the word from its memory, assert $\overline{BRDYO}$, and return to the idle state.
1	1	Read hit	Non-cachable burst access. The cache module will process this access like a normal burst read hit. The 4 words in the line will be returned with $\overline{BRDYO}$ asserted. Less than 4 words will be returned if $\overline{BLAST}$ is asserted before the end of the burst sequence.
0	0	Read miss	Cachable single read access. Cache module will assert $\overline{START}$ and wait for $\overline{CBRDY}$ or $\overline{CRDY}$ to complete the cycle. The selected cache line is invalidated.
0	1	Read miss	Cachable burst read access. This is the normal read miss case. The cache module will assert $\overline{START}$ and wait for the 4 words to return from main memory accompanied by $\overline{CBRDY}$ or $\overline{CRDY}$. The words will be written into the cache memory and the cache line will be validated when the fourth word is returned (because $\overline{SKEN}$ is LOW). If $\overline{BLAST}$ is asserted before the fourth word is returned, the line fill is aborted and the selected cache line will remain invalidated.
1	0	Read miss	Non-cachable single read access. The cache module will assert $\overline{START}$ and wait for $\overline{CBRDY}$ or $\overline{CRDY}$ to complete the cycle. The word returned from main memory will not be stored into the cache memory and the valid bit of the selected cache line is not changed.
1	1	Read miss	Non-cachable burst read access. The cache module will process this access like a normal cachable burst read miss. $\overline{START}$ will be asserted but the 4 words returned from main memory not will be stored into the cache. In addition, the valid bit of the selected cache entry is not changed.

Write Cycles

A write cycle is initiated when $\overline{ADS}$ and $\overline{CS}$ are sampled LOW at clock rise with W/$\overline{R}$ and M/$\overline{IO}$ sampled HIGH. The address from the processor is latched for two clock cycles to allow cache RAM update in case of a write hit. The latch then reopens to accept new addresses.

Tag look-up begins as soon as a valid processor address is available. If the location specified by the processor is found in the cache, the cache RAMs are updated with the data from the processor immediately. Byte enable signals $\overline{BE0}$ – $\overline{BE3}$ are used to determine which bytes in the 32-bit words are to be modified. If the location is not found in the cache, the cache RAMs are not modified.

Because the CYM7485 implements the write-through cache policy, write data from the processor is always written into the main memory regardless of cache hits or cache misses. In every write cycle, $\overline{START}$ is asserted (LOW) in T2 to trigger the main memory write operation.This signal will remain LOW until the system indicates write completion by asserting (LOW) $\overline{CBRDY}$ or $\overline{CRDY}$. $\overline{BRDYO}$ is kept HIGH throughout the write cycle. The minimum write cycle contains one wait state (i.e., three clocks in the cycle) and the minimum data-hold time is 6 ns.

All write cycles require one wait state.

Invalidations

Individual tag invalidation is supported in the CYM7485. If $\overline{EADS}$, $\overline{CS}$, and W/$\overline{R}$ are sampled LOW and M/$\overline{IO}$ is sampled HIGH at clock rise, then the tag entry selected by the processor address is invalidated if a tag match is detected. In other words, memory read cycles never cause invalidation. The address must be stable a minimum of 14 ns before the clock edge at which $\overline{EADS}$ is sampled LOW.

The CYM7485 will recognize invalidation requests under two conditions only:

1. Self invalidation during a write cycle (initiated by asserting $\overline{ADS}$). The earliest time at which $\overline{EADS}$ can be asserted is the third clock rise after the one clock cycle in which $\overline{ADS}$ is sampled LOW. For each invalidation, the address to be invalidated must be stable for two full clock cycles after $\overline{EADS}$ is asserted. $\overline{CBRDY}$ or $\overline{CRDY}$ can be asserted as early as the second clock rise after the one in which $\overline{EADS}$ is asserted to complete the write cycle. The CYM7485 can support consecutive $\overline{EADS}$ invalidations once every three clock cycles before $\overline{CBRDY}$ or $\overline{CRDY}$ is returned. For consecutive write cycles with self-invalidation, the CYM7485 can support one such operation every six clock cycles (see Self-Invalidation Timing Diagram).
2. When the cache module is in the "back-off" state ($\overline{BOFF}$ is asserted).The cache module can be placed in the "back-off" state by asserting $\overline{BOFF}$ in all normal access cycles except in T1. Once in the "back-off" state, the module can accept consecutive invalidations via $\overline{CS}$ and $\overline{EADS}$ once every three clock cycles. The earliest time $\overline{CS}$ and $\overline{EADS}$ can be asserted is the clock rise after the one in which $\overline{BOFF}$ is asserted. For each invalidation, the address to be invalidated has to remain stable for two full clock cycles after the $\overline{EADS}$ signal is asserted.

Flush

The CYM7485 cannot support global cache flushes where the entire cache is invalidated by the assertion of the $\overline{FLUSH}$ input. To flush the cache in the CYM7485, the processor has to

1. Assert $\overline{FLUSH}$ and $\overline{ADS}$ at clock rise (i.e., $\overline{FLUSH}$=LOW and $\overline{ADS}$=LOW) with M/$\overline{IO}$ set to HIGH, or assert $\overline{ADS}$ and deassert $\overline{CS}$ at clock rise (i.e., $\overline{ADS}$=LOW and $\overline{CS}$=HIGH) with M/$\overline{IO}$ set to HIGH. Note that $\overline{CS}$, $\overline{ADS}$, and M/$\overline{IO}$ must satisfy the set-up time requirements (i.e., t8, t6, and t6 respectively).
2. Access (read or write) the 8K locations in the cache tag.

During each access, the cache module will invalidate the cache entry selected by the address lines. The CYM7485 can accept new flush accesses no faster than once every three clock cycles (see the Flush Timing Diagrams). $\overline{START}$ and $\overline{BRDY0}$ will remain deasserted (HIGH) during flush cycles. $\overline{CBRDY}$ and $\overline{CRDY}$ are not required to complete the flush cycle.

Back-Off

A cache back-off can be initiated by the assertion of the $\overline{BOFF}$ in any normal access cycles except in T1 where the $\overline{BOFF}$ signal is ignored. Once $\overline{BOFF}$ is sampled LOW at clock rise, the data lines will be placed in a three-stated condition in the same clock cycle. In addition, both $\overline{START}$ and $\overline{BRDYO}$ will be pulled HIGH. When $\overline{BOFF}$ is asserted, the cache module will ignore all cache cycles except RESET, invalidation via $\overline{CS}$, $\overline{EADS}$, and M/$\overline{IO}$, and flush operations via $\overline{FLUSH}$, $\overline{CS}$, $\overline{ADS}$, and M/$\overline{IO}$.

Reset

If RESET is sampled HIGH at clock rise, the cache controller will enter the idle state and all module outputs will be deasserted. The cache contents, however, are not invalidated. Refer to the Flush section for information on cache invalidation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7485−33		Unit
			Min.	Max.	
V_{OHD}	Output HIGH Voltage (Data)	V_{CC}=Min., I_{OH}=−4.0 mA	2.4		V
V_{OLD}	Output LOW Voltage (Data)	V_{CC}=Min., I_{OL}=8.0 mA		0.4	V
V_{OHC}	Output HIGH Voltage (Control)	V_{CC}=Min., I_{OH}=−3.2 mA	2.4		V
V_{OLC}	Output LOW Voltage (Control)	V_{CC}=Min., I_{OL}=16 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC}=Max.	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

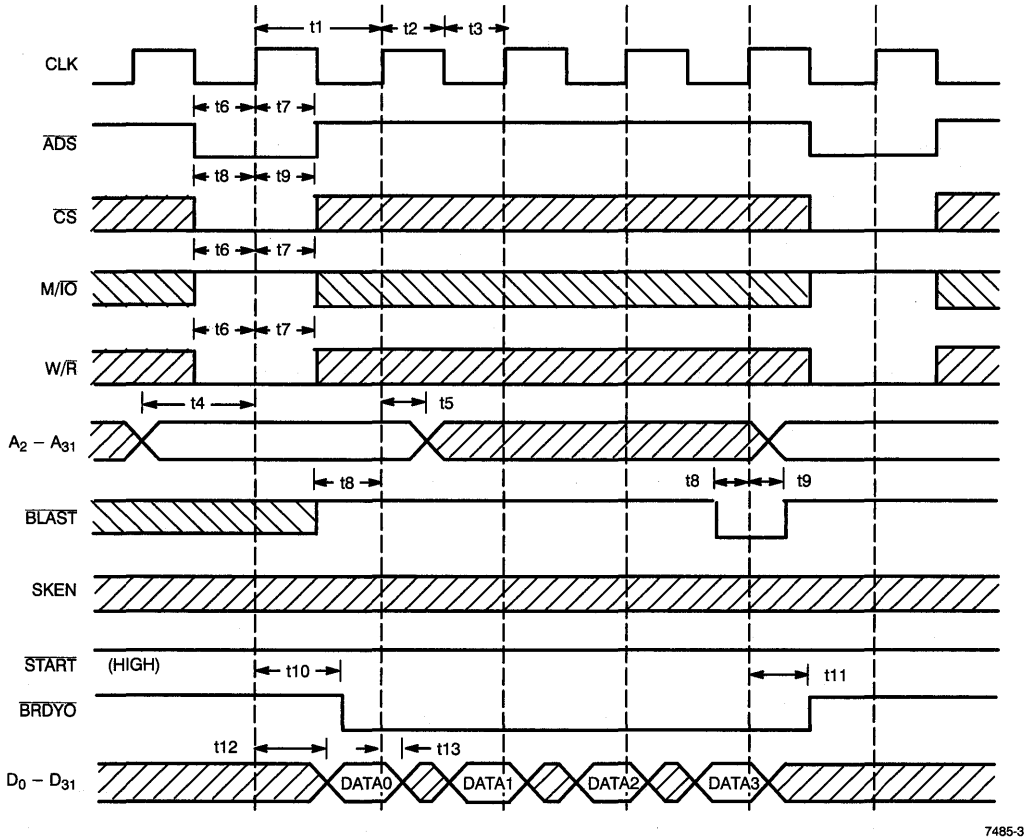
AC Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0° to 70°C, loading on $D_0 - D_{31}$ = 75 pF, loading on all other outputs = 50 pF)

Symbol	Parameter	Min.	Max.	Unit
t1	Clock Period	30		ns
t2	Clock HIGH Time	11		ns
t3	Clock LOW Time	11		ns
t4	$A_2 - A_{31}$, $\overline{BE_0} - \overline{BE_3}$ Set-Up Before Clock Rise	14		ns
t5	$A_2 - A_{31}$, $\overline{BE_0} - \overline{BE_3}$ Hold After Clock Rise	3		ns
t6	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Set-Up Before Clock Rise	14		ns
t7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Hold After Clock Rise	3		ns
t8	$\overline{CS}$, $\overline{BLAST}$ Set-Up Before Clock Rise	9		ns
t9	$\overline{CS}$, $\overline{BLAST}$ Hold After Clock Rise	3		ns
t10	$\overline{BRDYO}$ Valid After Clock Rise		17	ns
t11	$\overline{BRDYO}$ Hold After Clock Rise	3		ns
t12	$D_0 - D_{31}$ Valid After Clock Rise During Read Hit		24	ns
t13	$D_0 - D_{31}$ Hold After Clock Rise	3		ns
t14	$\overline{SKEN}$ Set-Up Before Clock Rise	9		ns
t15	$\overline{SKEN}$ Hold After Clock Rise	3		ns
t16	$\overline{START}$ Valid After Clock Rise		17	ns
t17	$\overline{START}$ Hold After Clock Rise	3		ns
t18	$D_0 - D_{31}$ Set-Up Before Clock Rise During Line Fill	10		ns
t19	$D_0 - D_{31}$ Hold After Clock Rise During Line Fill	15		ns
t20	$\overline{CBRDY}$, $\overline{CRDY}$ Set-Up Before Clock Rise	14		ns
t21	$\overline{CBRDY}$, $\overline{CRDY}$ Hold After Clock Rise	3		ns
t22	$D_0 - D_{31}$ Set-Up Before Clock Rise During Processor Write Cycle	0		ns
t23	$D_0 - D_{31}$ Hold After Clock Rise During Processor Write Cycle	6		ns
t24	$\overline{EADS}$ Set-Up Before Clock Rise	9		ns
t25	$\overline{EADS}$ Hold After Clock Rise	3		ns
t26	$\overline{BOFF}$ Set-Up Before Clock Rise	9		ns
t27	$\overline{BOFF}$ Hold After Clock Rise	3		ns
t28	$\overline{START}$ Go HIGH After Clock Rise During $\overline{BOFF}$ or RESET		18	ns
t29	$\overline{BRDYO}$ Go HIGH After Clock Rise During $\overline{BOFF}$ or RESET		18	ns
t30	D_0-D_{31} High Z During $\overline{BOFF}$		18	ns
t31	RESET Set-Up Before Clock Rise	9		ns
t32	RESET Hold After Clock Rise	3		ns
t33	RESET Duration	2 t2 + 12		ns
t34	$\overline{FLUSH}$ Set-Up Before Clock Rise	9		ns
t35	$\overline{FLUSH}$ Hold After Clock Rise	3		ns

Switching Waveforms

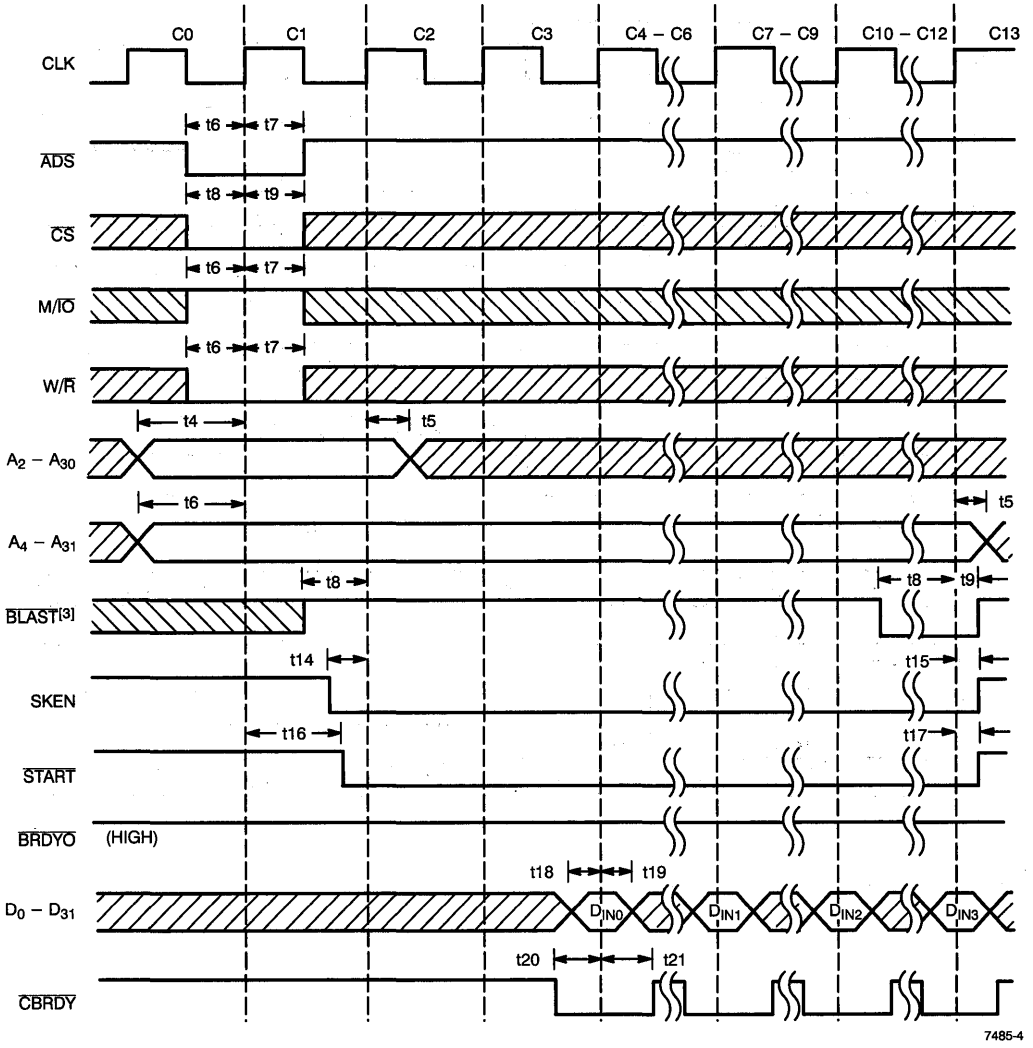
Read Hit[1]



Note:
1. Reset is LOW, $\overline{EADS}$ is HIGH, and $\overline{BOFF}$ is HIGH.

Switching Waveforms (continued)

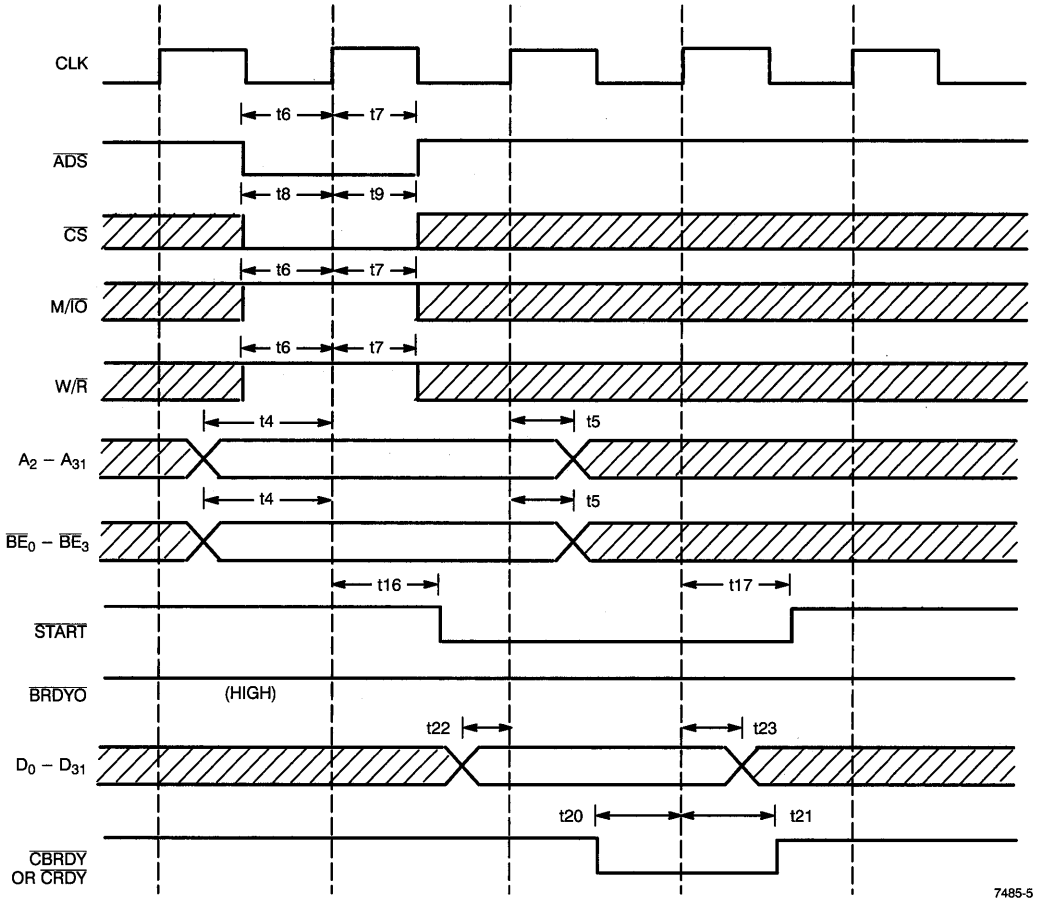
Read Miss, Line Fill (Min. DRAM Access is 4/3/3/3)[2]



Notes:
2. Reset is LOW, $\overline{EADS}$ is HIGH, $\overline{BOFF}$ is HIGH, and $\overline{CRDY}$ is HIGH.
3. $\overline{BLAST}$ is LOW t8 before the rising edge of clock period C11.

Switching Waveforms (continued)

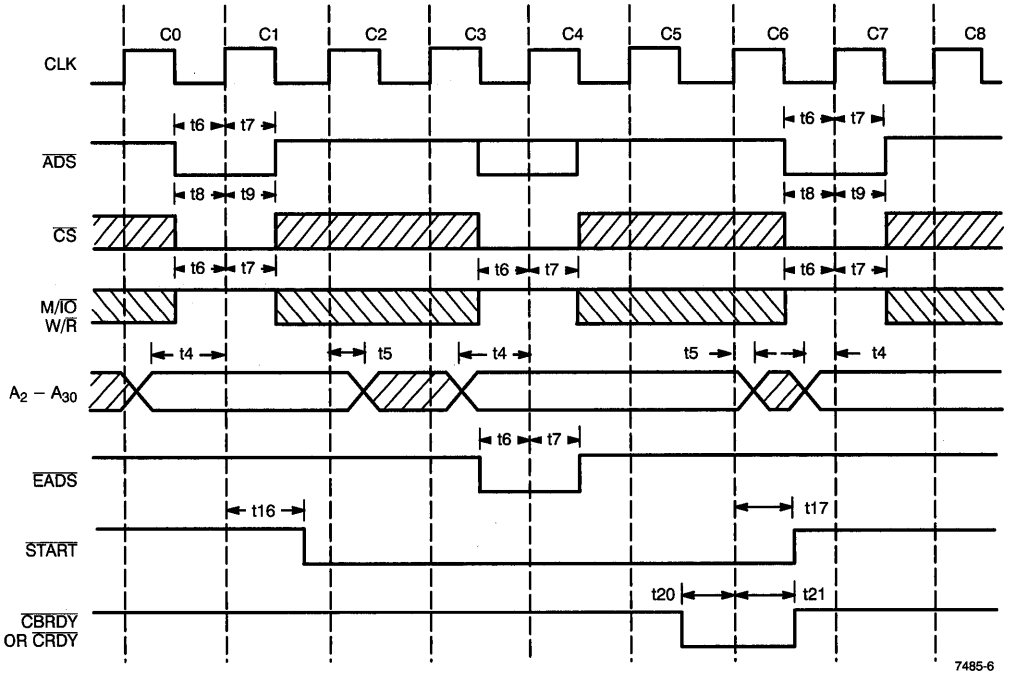
Write Cycle[4]



Note:
4. Reset is LOW, $\overline{\text{CBRDY}}$ is HIGH, $\overline{\text{EADS}}$ is HIGH, $\overline{\text{BOFF}}$ is HIGH. Access to DRAM must be a minimum of 3 cycles.

Switching Waveforms (continued)

Write Cycle with Self-Invalidation[5]

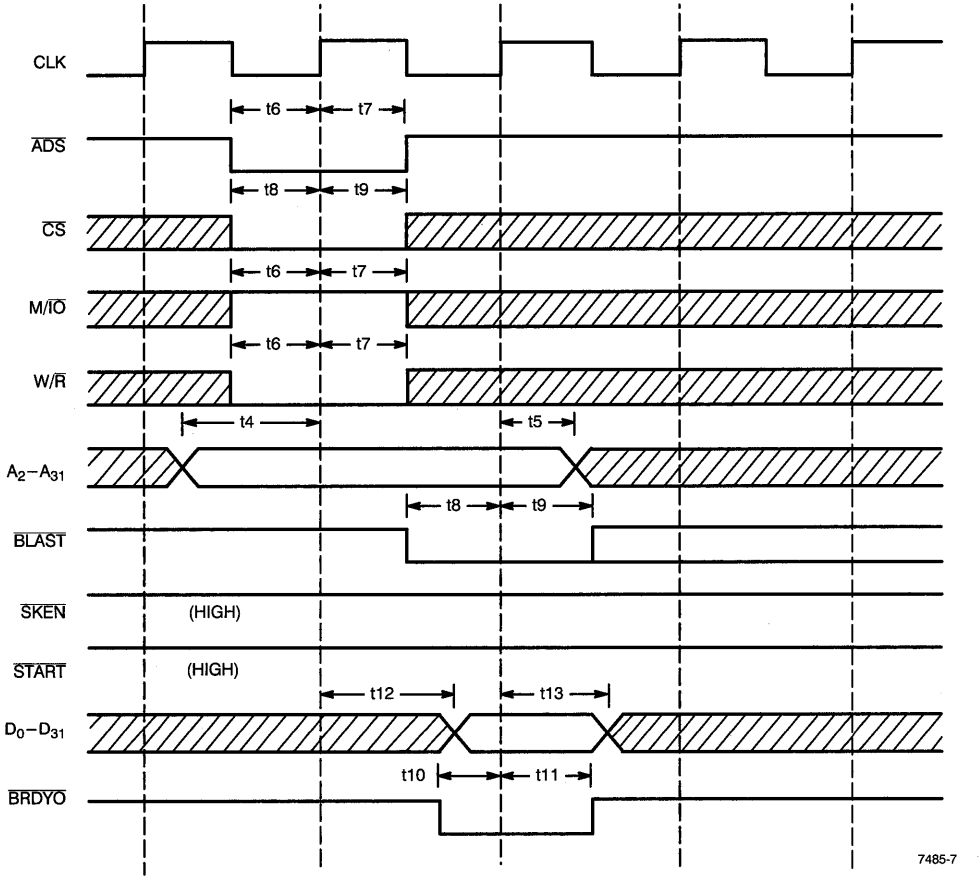


Note:

5. Reset is LOW. There is a minimum of 3 clocks between $\overline{ADS}$ and $\overline{EADS}$, a minimum of two clocks between $\overline{EADS}$ and $\overline{CBRDY}$ or $\overline{CRDY}$, a minimum of three clocks between consecutive $\overline{EADS}$ inside the same write cycle, and a minimum of 6 clocks between consecutive $\overline{ADS}$s.

Switching Waveforms (continued)

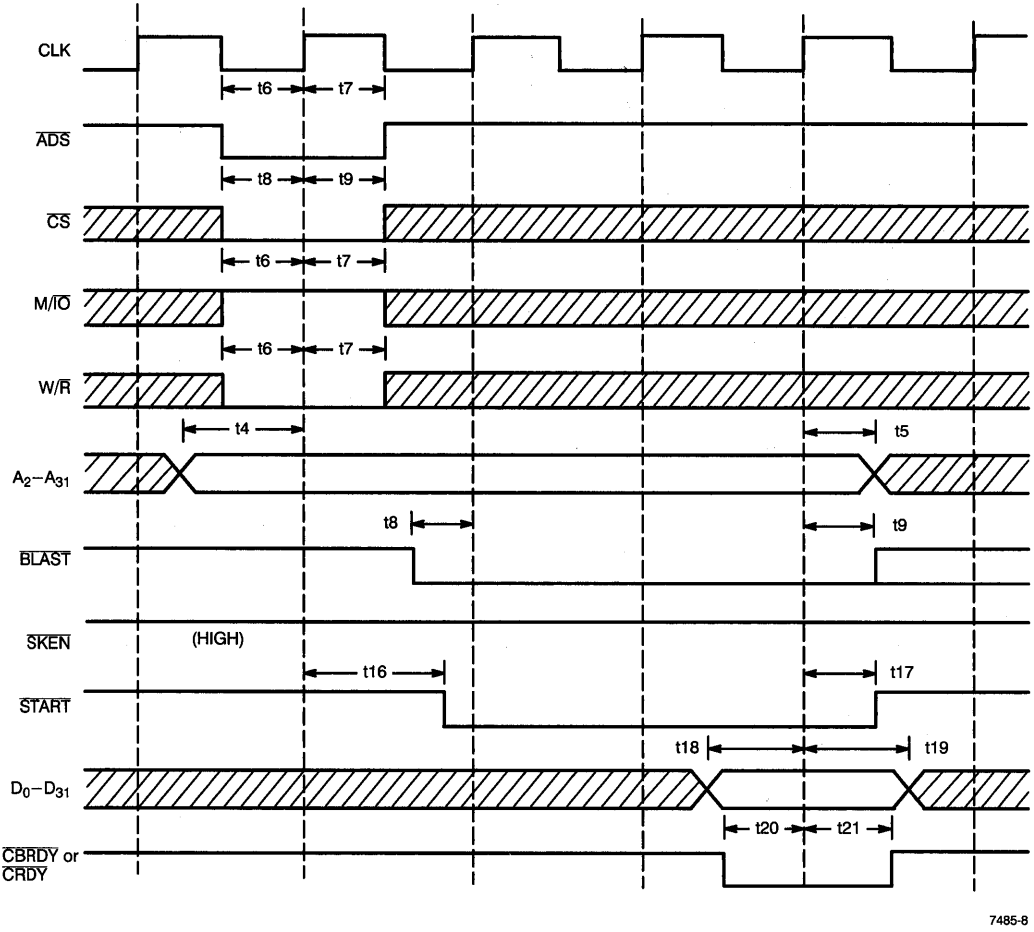
Single Non-Cachable Read (Cache Hit) [6]



Note:
6. Reset is LOW.

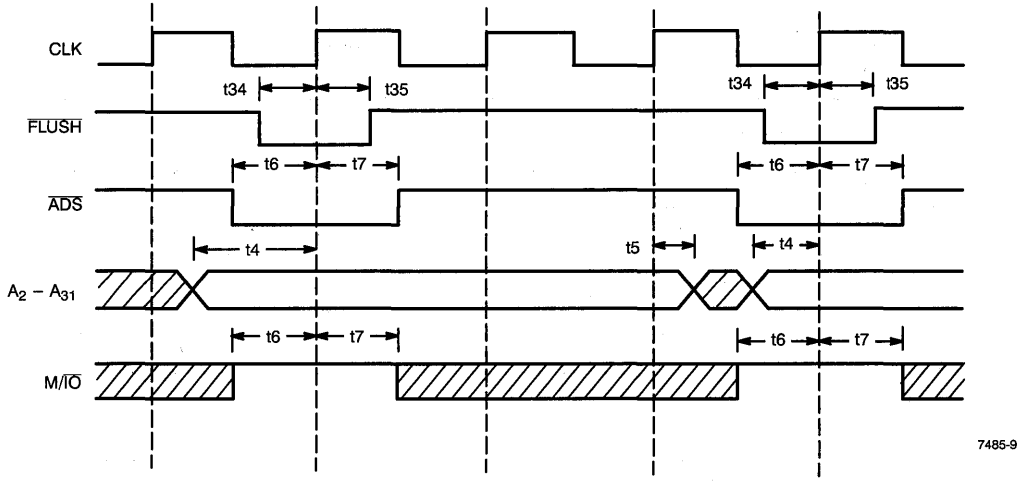
Switching Waveforms (continued)

Single Non-cachable Read (Cache Miss) Showing a Four-Clock Main Memory Access

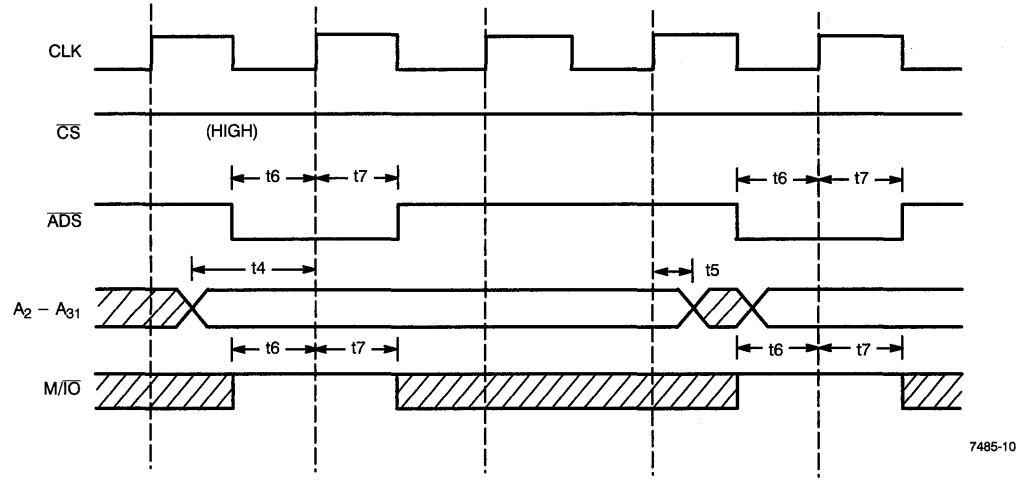


Switching Waveforms (continued)

Flush Cycle 1[7, 8]



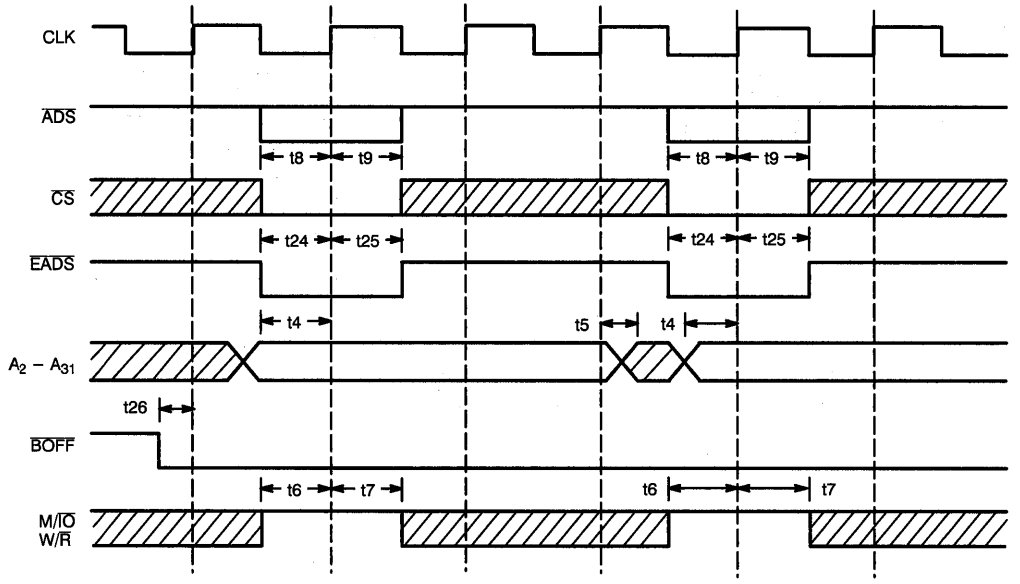
Flush Cycle 2[8, 9]



Notes:
7. Controlled by $\overline{\text{FLUSH}}$, $\overline{\text{ADS}}$, and M/$\overline{\text{IO}}$; $\overline{\text{CS}}$ is a don't care.
8. A minimum of three clocks between consecutive $\overline{\text{ADS}}$ signals is required during Flush cycles. Reset is LOW.
9. Controlled by $\overline{\text{CS}}$, $\overline{\text{ADS}}$, and M/$\overline{\text{IO}}$; $\overline{\text{FLUSH}}$ is a don't care.

Switching Waveforms (continued)

Consecutive Invalidations During $\overline{BOFF}$[10]

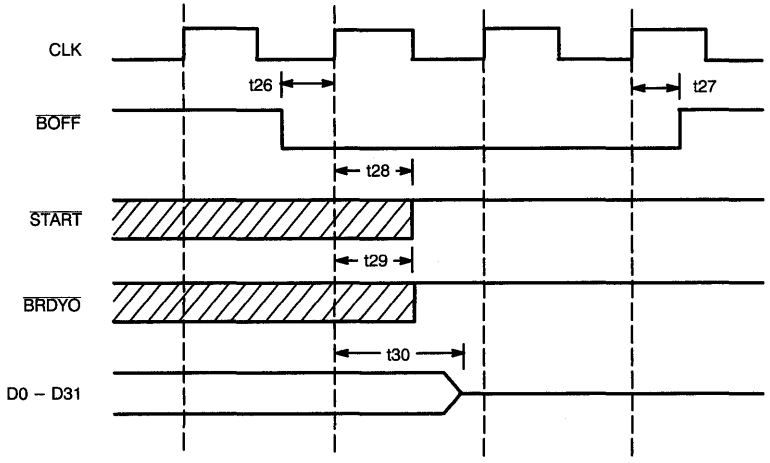


7485-11

Note:
10. Reset is LOW. There is a minimum of three clocks between $\overline{EADS}$, and a minimum of one clock between $\overline{BOFF}$ and $\overline{EADS}$.

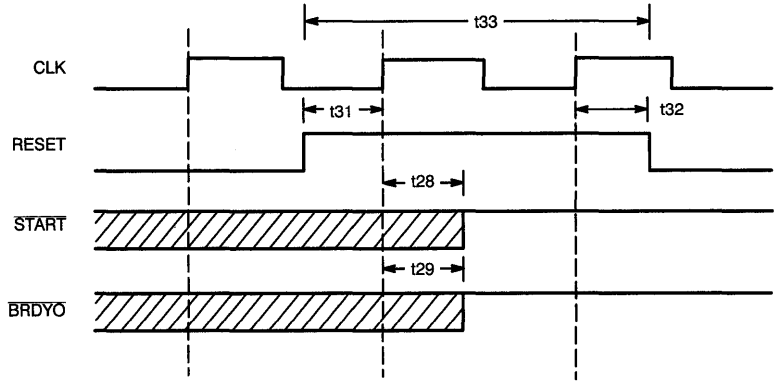
Switching Waveforms (continued)

Backoff Operation[11]



7485-12

Reset Operation



7485-13

Note:
11. Reset is LOW.

Ordering Information

Operating Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
33	CYM7485ZPM–33C	PM08	128-Pin Dual-Readout SIMM	Commercial

Document #: 38-M-00058–A

i486 Level II Cache Module Family

Features

- **Cache sizes of 64 KB, 256 KB, or 1 MB**
- **Tag width of 8 bits**
- **Independent dirty bit**
- **Operates with 33-MHz Intel i486 processors**
- **Zero-wait-state operation**
- **Constructed using standard asynchronous SRAMs**
- **64-position (128-signal) dual-readout SIMM**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

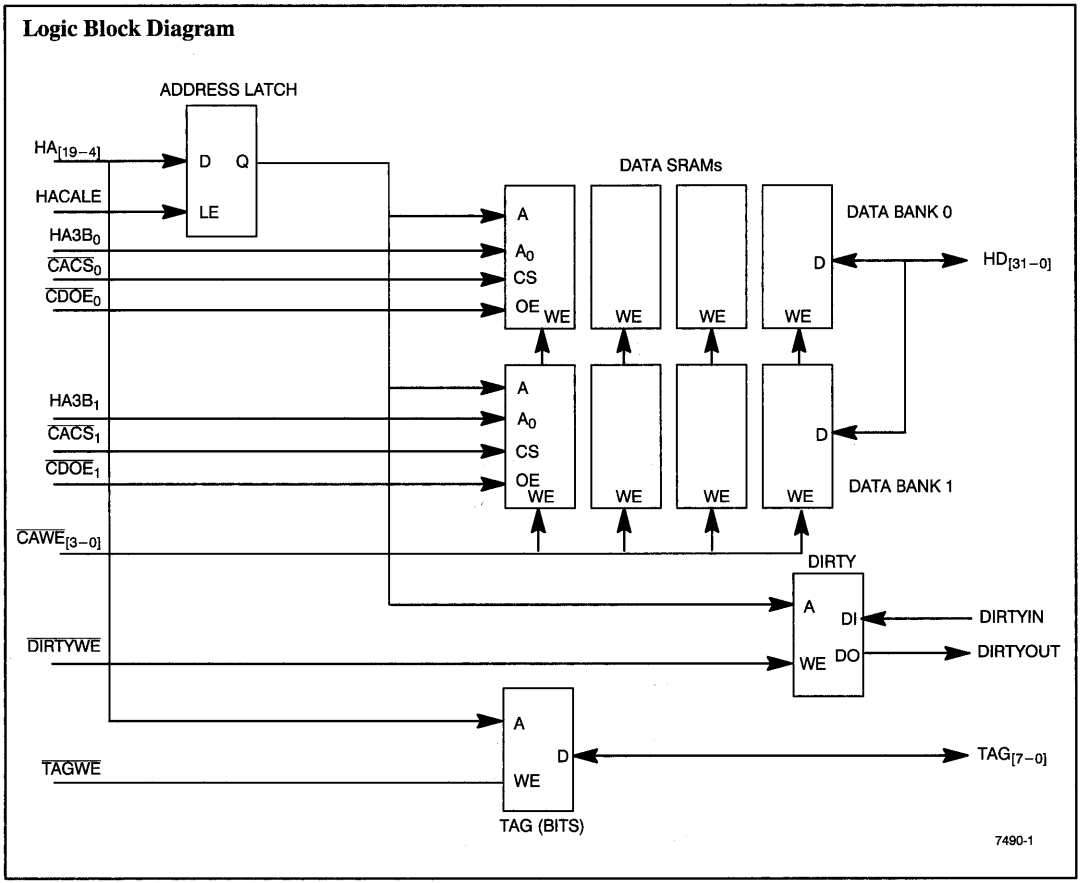
Functional Description

The CYM7490 module series is a family of cache memory subsystems for Intel i486-based systems. Each module contains two banks of 32-bit-wide data SRAM, an 8-bit-wide tag SRAM, and a single-bit-wide, separate I/O dirty SRAM. Bank sizes of 8K x 32, 32K x 32, and 128K x 32 are supported, yielding cache sizes of 64 kilobytes, 256 kilobytes, and 1 megabyte. The address signals for the data and dirty SRAMs are latched.

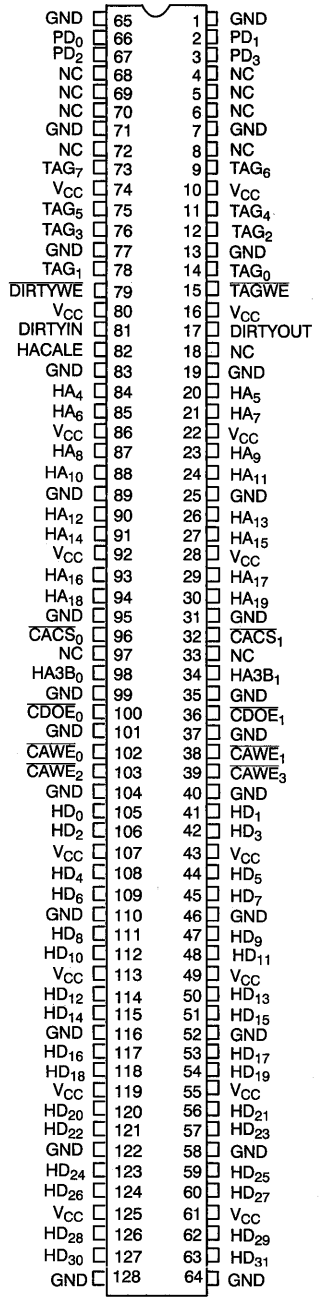
The module is configured as a 128-pin dual-readout single-in-line memory module (SIMM). It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The SIMM contacts are plated with five micro-inches of gold over 100 micro-inches of nickel. Module dimensions are 3.85 inches long by 1.15 inches high by 0.33 inches thick.

These modules are designed for zero-wait-state operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with off-the-shelf cache controllers and chipsets. The 15-ns device is built using data and tag SRAMs with an access time of 15 ns, while the 20-ns version is built with 15-ns tag SRAMs and 20-ns data SRAMs.

Logic Block Diagram



Dual-Readout SIMM
Top View



7490-2

Signal Descriptions

Signal	Type	Description
TAG_{7-0}	I/O	Cache Tag Data Bus
$\overline{TAGWE}$	I	Tag Write Enable
$\overline{DIRTYWE}$	I	Dirty Bit Write Enable
DIRTYIN	I	Dirty Bit In
DIRTYOUT	O	Dirty Bit Out
HACALE	I	Host Address Bus Latch Enable
HA_{19-4}	I	Host Address Bus.
$\overline{CACS}_{1-0}$	I	Cache Memory Chip Selects
$HA3B_{1-0}$	I	Host Address A3 Bank Select
$\overline{CDOE}_{1-0}$	I	Cache Data Output Enable
$\overline{CAWE}_{3-0}$	I	Cache Write Enables
HD_{31-0}	I/O	Host Data Bus
PD_{3-0}	O	Presence Detect Pins (see below)
NC	–	Reserved for future use.

Presence Detect Scheme

Device	PD3	PD2	PD1	PD0
CYM7490	Open	Open	Open	GND
CYM7491	Open	Open	GND	Open
CYM7492	Open	Open	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 55°C to +150°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to +7.0V

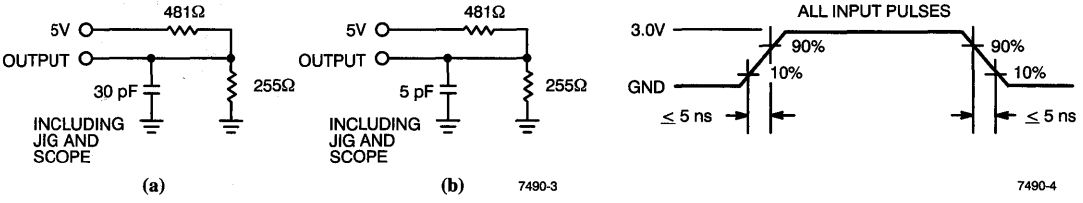
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7490–15, 20 CYM7491–15, 20 CYM7492–15, 20 Min.	Max.	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
T_{AMB}	Ambient Temperature	Commercial	0	70	°C
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 8..0 mA		0.4	V
V_{IH}	Input HIGH Voltage Level		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage Level		−0.5	0.8	V
L_{IN}	Input Leakage Output	V_{CC} = Max., $0 \le V_{IN} \le V_{SS}$		±20	µA
I_{OUT}	Operating Leakage Current	$\overline{CS}$=V_{IH}, V_{CC} =Max., $V_{SS} \le V_{OUT} \le V_{CC}$		±20	µA
I_{CC1}	Operating Current	$\overline{CACSn}$ = V_{IL}, Outputs Open, f=f_{MAX}		1300	mA
I_{SB1}	Standby Current – TTL Levels	$\overline{CACSn} \ge V_{CC}$ −0.2, V_{CC} = Max., V_{CC} −0.2 ≤ V_{IN} ≤ 0.2, Outputs Open		800	mA
I_{SB2}	Standby Current – CMOS Levels	$\overline{CACSn} \ge V_{CC}$ −0.2, V_{CC} = Max., V_{CC}−0.2 ≤V_{IN}≤ 0.2, Outputs Open		400	mA

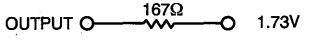
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{ADDR}	Input Capacitance, HA_{19-4}, $CAA3_{1-0}$	f=1 MHz	50	pF
C_{WE}	Input Capacitance, $\overline{CAWE}_{1-0}$, $\overline{TAGWE}$	f=1 MHz	30	pF
C_{WE2}	Input Capacitance, $\overline{DIRTYWE}$, HACALE	f=1 MHz	20	pF
C_{CSOE}	Input Capacitance, $\overline{CACS}_{1-0}$, $\overline{CDOE}_{1-0}$	f=1 MHz	50	pF
C_{DATA}	Input/Output Capacitance, HD_{31-0}	f=1 MHz	90	pF
C_{TAG}	Input/Output Capacitance, TAG_{7-0}, $\overline{DIRTYIN}$, $\overline{DIRTYOUT}$	f=1 MHz	30	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	7490–15 7491–15 7492–15		7490–20 7491–20 7492–20		Unit
		Min.	Max.	Min.	Max.	
ADDRESS LATCH						
t_{LPW}	Latch Pulse Width	5		5		ns
t_{LSD}	Data Set-Up to ALE Positive	2		2		ns
t_{LHD}	Data Hold from ALE Positive	1.5		1.5		ns
READ CYCLE – Data SRAM Read Timing						
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address Access Time (Latch Transparent)		20		25	ns
t_{OE}	Output Enable to Output Valid		10		10	ns
t_{CE}	Chip Enable to Data Valid		15		20	ns
t_{OHA}	Data Hold After Address Change	3		3		ns
t_{LZCE}	Chip Enable to Outputs in Low Z	3		3		ns
t_{HZCE}	Chip Disable to Outputs in High Z		8		10	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		
t_{OHZ}	Output Diable to Outputs in High Z		8		10	ns
READ CYCLE – Tag SRAM Read Timing						
t_{TDRC}	Read Cycle Time	15		20		ns
t_{TAA}	Address Access Time		15		20	ns
t_{TCE}	Chip Enable to Data Valid		15		20	ns
t_{TOHA}	Data Hold After Address Change	3		3		ns
t_{TLZCE}	Chip Enable to Outputs in Low Z	3		3		ns
t_{THZCE}	Chip Disable to Outputs in High Z		8		8	ns
READ CYCLE – Dirty SRAM Read Timing						
t_{DRC}	Read Cycle Time	20		25		ns
t_{DAA}	Address Time		20		25	ns
t_{DOHA}	Data Hold After Address Change	3		3		ns
WRITE CYCLE – Data SRAM Write Timing						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	Chip Enable to End of Write	10		15		ns
t_{AW}	Address Set-up to End of Write	20		25		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{SA}	Address Set-Up from Beginning of Write	5		5		ns
t_{PWE}	Write Pulse Width	10		15		ns
t_{SD}	Data Set-Up to End of Write	7		10		ns
t_{HD}	Data Hold from End of Write	0		0		ns
t_{LZWE}	Write High to Outputs in Low Z	3		3		ns
t_{HZWE}	Write Low to Outputs in High Z		7		10	ns

Switching Characteristics (continued)

Parameter	Description	7490–15 7491–15 7492–15 Min.	7490–15 7491–15 7492–15 Max.	7490–20 7491–20 7492–20 Min.	7490–20 7491–20 7492–20 Max.	Unit
WRITE CYCLE – Tag SRAM Write Timing						
t_{TWC}	Write Cycle Time	15		15		ns
t_{TSCE}	Chip Enable to End of Write	10		10		ns
t_{TAW}	Address Set-Up to End of Write	10		10		ns
t_{TAH}	Address Hold from End of Write	0		0		ns
t_{TSA}	Address Set-Up from Beginning of Write	0		0		ns
t_{TPWE}	Write Pulse Width	10		10		ns
t_{TSD}	Data Set-Up to End of Write	7		7		ns
t_{THD}	Data Hold from End of Write	0		0		ns
t_{TLZWE}	Write High to Outputs in Low Z	3		3		ns
t_{THZWE}	Write Low to Outputs in High Z		7		7	ns
WRITE CYCLE – Dirty SRAM Write Timing						
t_{DWC}	Write Cycle Time	20		20		ns
t_{DAW}	Address Set-Up to End of Write	17		17		ns
t_{DAH}	Address Hold from End of Write	0		0		ns
t_{DSA}	Address Set-Up from Begining of Write	5		5		ns
t_{DPWE}	Write Pulse Width	12		12		ns
t_{DSD}	Data Set-Up to End of Write	10		10		ns
t_{DHD}	Data Hold from End of Write	0		0		ns
t_{DLZWE}	Write High to Outputs in Low Z	5		5		ns
t_{DHZWE}	Write Low to Outputs in High Z		7		7	ns

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
15 (Data and Tag/Dirty)	CYM7490PM–15	PM05	128-Pin Dual-Readout SIMM	64 Kbyte
20 (Data), 15 (Tag/Dirty)	CYM7490PM–20	PM05	128-Pin Dual-Readout SIMM	

Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
15 (Data and Tag/Dirty)	CYM7491PM–15	PM06	128-Pin Dual-Readout SIMM	256 Kbyte
20 (Data), 15 (Tag/Dirty)	CYM7491PM–20	PM06	128-Pin Dual-Readout SIMM	

Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
15 (Data and Tag/Dirty)	CYM7492PM–15	PM07	128-Pin Dual-Readout SIMM	1 Mbyte
20 (Data), 15 (Tag/Dirty)	CYM7492PM–20	PM07	128-Pin Dual-Readout SIMM	

Document #: 38–M–00061

Section Contents

ECL

CY10E383
CY101E383

CYPRESS SEMICONDUCTOR

ECL/TTL/ECL Translator and High-Speed Bus Driver

Features

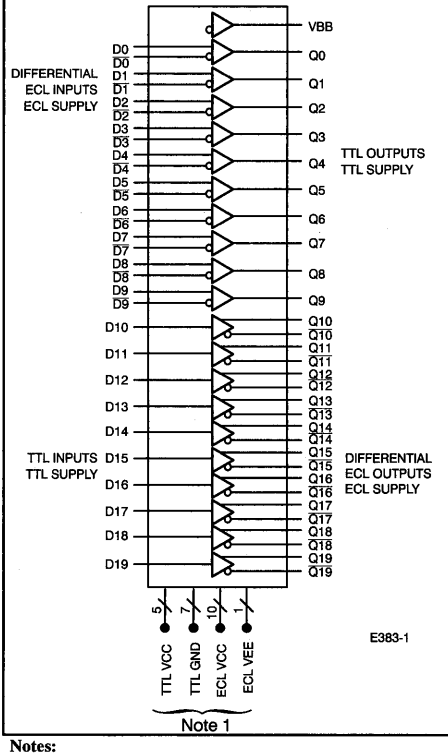
- **BiCMOS for optimum speed/power**
- **High speed (max.)**
  - **—2.5 ns t_{PD} TTL-to-ECL**
  - **—3.5 ns t_{PD} ECL-to-TTL**
- **Low skew < ± 1 ns**
- **Can operate on single +5V supply**
- **Full-duplex ECL/TTL data transmission**
- **Internal 2 kΩ ECL pull-down resistors on each ECL output**
- **80-pin PQFP package**
- **Surface-mount PLCC/CLCC package**
- **V_{BB} ECL reference voltage output**
- **Single- or dual-supply operation**
- **Capable of greater than 2001V ESD**
- **ECL cable/twisted pair driver**

Functional Description

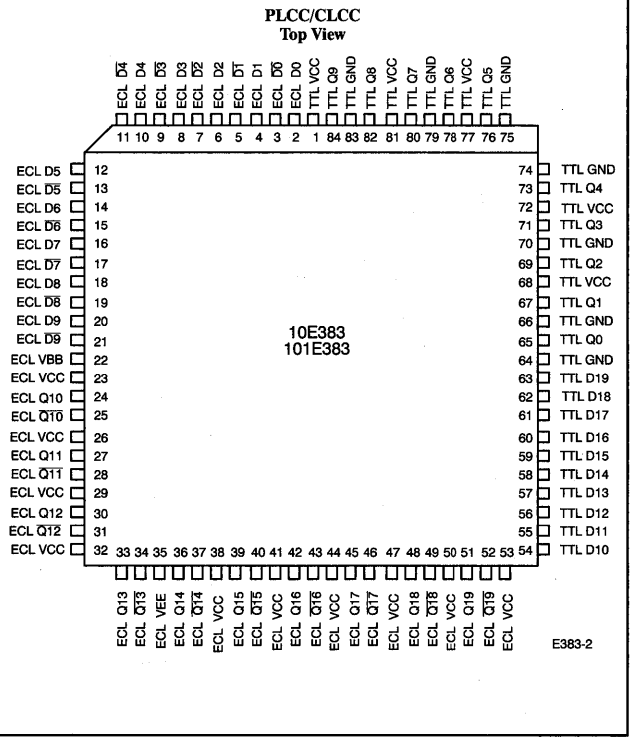
The CY10/101E383 is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains ten independent TTL-to-ECL and ten independent ECL-to-TTL translators for high-speed full-duplex data transmission, mixed logic, and bus applications. The CY10/101E383 is especially suited to drive ECL backplanes between TTL boards. The CY10/101E383 is implemented with differential ECL I/O to provide balanced low noise operation over controlled impedance buses between TTL and/or ECL subsystems. In addition, the device has internal output 2 kΩ pull-down resistors tied to V_{EE} to decrease the number of external components. For system testing purposes or for driving light loads, the 2 kΩ is used as the only termination thereby eliminating up to 20 external resistors. The part meets standard 10K/10KH and 100K logic levels with the internal pull-down while driving 50Ω to −2V.

The device is designed with ample ground pins to reduce bounce, and has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The parts can operate in single- or dual-supply configurations while maintaining absolute 10K/10KH and 100K level swings. The translators are offered in standard 10K/10KH (10E) and 100K (101E) ECL-compatible versions with −5.2V or −4.5V power supply. The TTL I/O is fully TTL compatible. The CY10/101E383 is packaged in 84-pin surface-mountable PLCCs and CLCCs. To save board space, an 80-pin PQFP package with 25-mil-lead pitch is available.

Logic Block Diagram



Pin Configurations



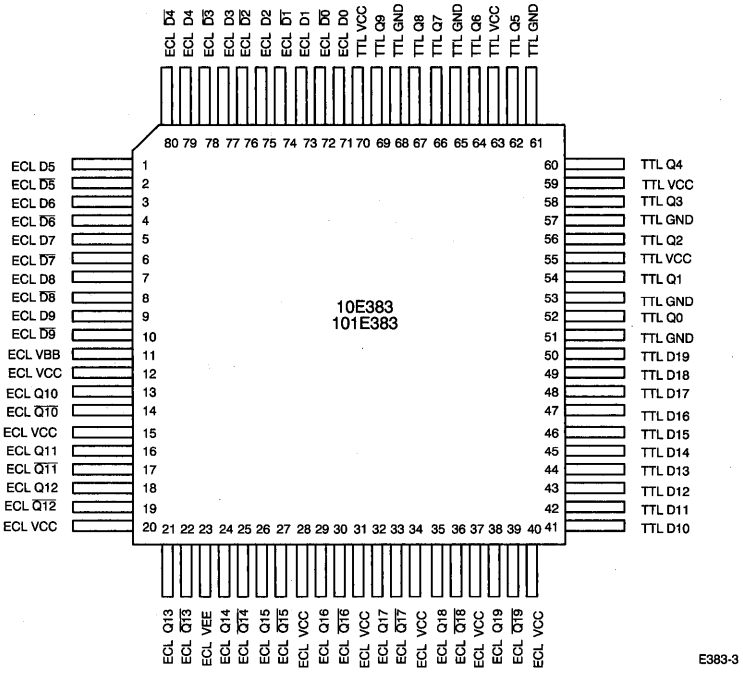
Notes:

1. The PQFP package has one less each TTL V_{CC} and TTL GND pin and two less ECL V_{CC} pins.

9 ECL

Pin Configurations (continued)

PQFP
Top View



E383-3

Selection Guide

	10E383–2 101E383–2	10E383–3 101E383–3
Maximum Propagation Delay Time (ns) (TTL to ECL)	2.5	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	3.5	4
Maximum Operating Current (mA) Sum of I_{EE} and I_{CC}	270	270

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

TTL Supply Voltage to Ground Potential .. − 0.5V to +7.0V

TTL DC Input Voltage ..... − 3.0V to +7.0V

ECL Supply Voltage V_{EE} to ECL V_{CC} .... −7.0V to +0.5V

ECL Input Voltage ..... V_{EE} to +0.5V

ECL Output Current ..... − 50 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V_{EE}	TTL V_{CC}
Commercial	10K 10KH	10E	0°C to +75°C	−5.2V ± 5%	5V ± 5%
Commercial	100K	101E	0°C to +85°C	−4.2V to −5.46V	5V ± 5%
Military	10K 10KH	10E	−55°C to +125°C case	−5.2V ± 5%	5V ± 5%

ECL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	Temperature[3]	10E383 Min.	10E383 Max.	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	10E, R_L = 50Ω to −2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = −55°C	−1140	−900			mV
			T_A = 0°C	−1000	−840			mV
			T_A = +25°C	−960	−810			mV
			T_A = +75°C	−900	−735			mV
			T_C = +125°C	−880	−700			mV
		101E R_L = 50Ω to −2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C			−1025	−880	mV
V_{OL}	Output LOW Voltage	10E, R_L = 50Ω to −2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = −55°C	−1920	−1670			mV
			T_A = 0°C	−1870	−1665			mV
			T_A = +25°C	−1850	−1650			mV
			T_A = +75°C	−1830	−1625			mV
			T_C = +125°C	−1830	−1610			mV
		101E R_L = 50Ω to −2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C			−1810	−1620	mV
V_{IH}	Input HIGH Voltage	10E	T_C = −55°C	−1260	−900			mV
			T_A = 0°C	−1170	−840			mV
			T_A = +25°C	−1130	−810			mV
			T_A = +75°C	−1070	−720			mV
			T_C = +125°C	−1030	−700			mV
		101E	T_A = 0°C to 85°C			−1165	−880	mV
V_{IL}	Input LOW Voltage	10E	T_C = −55°C	−1950	−1540			mV
			T_A = 0°C	−1950	−1480			mV
			T_A = +25°C	−1950	−1475			mV
			T_A = +75°C	−1950	−1450			mV
			T_C = +125°C	−1950	−1450			mV
		101E	T_A = 0°C to 85°C			−1810	−1475	mV
V_{BB}	Output Reference Voltage	10E[4]	T_A = 0°C to 75°C	−1.37	−1.18			V
			T_C = −55°C	−1.46	−1.32			
			T_C = +125°C	−1.29	−1.14			
		101E[4]	T_A = 0°C to 85°C			−1.40	−1.23	
V_{cm}[5]	Common Mode Voltage	±V_{cm} with respect to V_{BB}			1.0		1.0	V
V_{diff}	Input Voltage Differential	Required for Full Output Swing		150		150		mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220		220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.		−0.5	170	−0.5	170	µA
R_{PD}	Pull-Down Resistor	Connected from All ECL Outputs to V_{EE}	T_A = 0°C to 75°C	1.6	2.4			kΩ
			T_C = −55°C to +125°C	1.6	2.4			
			T_A = 0°C to 85°C			1.6	2.4	
I_{EE}	Supply Current (All inputs and outputs open)				−180		−180	mA

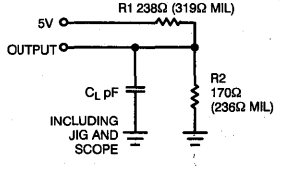
TTL Electrical Characteristics Over the Operating Range[2]

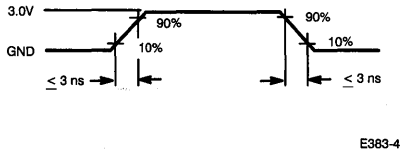
Parameter	Description	Test Conditions	10E383 101E383 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Max., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage[6]		2.0		V
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{CD}	Input Clamp Diode Voltage	I_{IN} = −10 mA	−1.5		V
I_{OS}[7]	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[8]	−180	−40	mA
I_{IX}	Input Load Current[9]	GND ≤ V_I ≤ V_{CC}	−250	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		90	mA

Capacitance

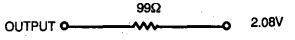
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}[7]	Input Capacitance		4	pF
C_{OUT}[7]	Output Capacitance		5	pF

TTL AC Test Load and Waveform[10]

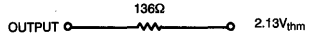




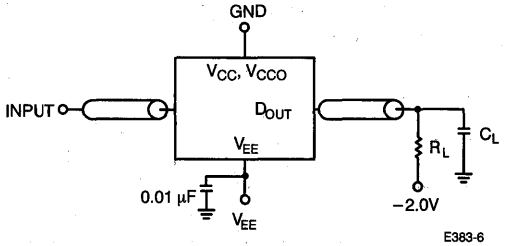
Equivalent to: THÉVENIN EQUIVALENT (Commercial)

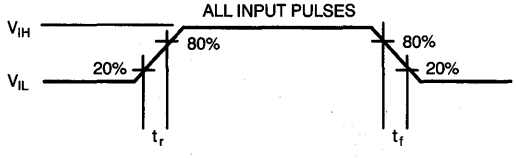


THÉVENIN EQUIVALENT (Military)



ECL AC Test Load and Waveform[11, 12, 13, 14, 15, 16]





Notes:

2. See AC Test Load and Waveform for test conditions.
3. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
4. Max. I_{BB} = −1 mA.
5. The internal gain of the CY101/10E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
6. These are absolute values with respect to device ground.
7. Characterized initially and after any design or process changes that may affect these parameters.
8. Not more than one output should be tested at a time. Duration of the short should not be more than one second.
9. I/O pin leakage is the worst case of I_{IX} (where X = H or L).
10. TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
11. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
12. V_{IL} = −1.7V, V_{IH} = −0.9V on 101E version
13. ECL R_L = 50Ω, C_L < 5 pF (includes fixture and stray capacitance).
14. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
15. t_r = t_f = 0.7 ns
16. All timing measurements are made from the 50% point of all waveforms.

ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E383–2 101E383–2		10E383–3 101E383–3		Unit
			Min.	Max.	Min.	Max.	
t_{pLH}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns
t_{pHL}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

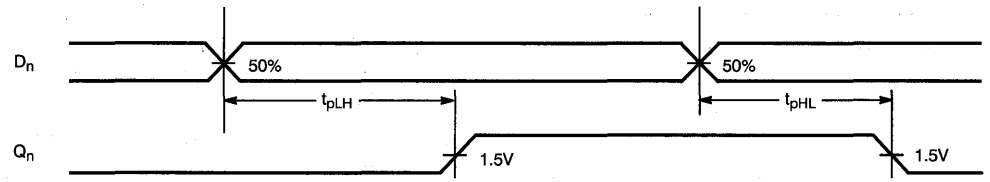
Parameter	Description	Test Conditions	10E383–2 101E383–2		10E383–3 101E383–3		Unit
			Min.	Max.	Min.	Max.	
t_{pLH}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_{pHL}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_r	Output Rise Time	20% to 80%	0.35	1.7	0.35	1.7	ns
t_f	Output Fall Time	20% to 80%	0.35	1.7	0.35	1.7	ns

Skew Time Switching Characteristics (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
t_{SKT}[7]	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		1	ns
t_{SKE}[7]	Data Skew Time TTL-to-ECL	$ECLQ_n$, $\overline{Q}_n$ to $ECLQ_{n+m}$, $\overline{Q}_{n+m}$		1	ns

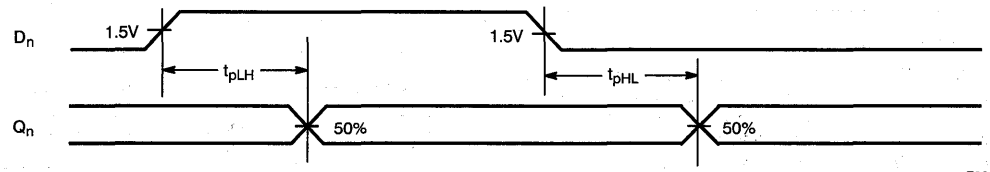
Switching Waveforms

ECL-to-TTL Timing



E383-8

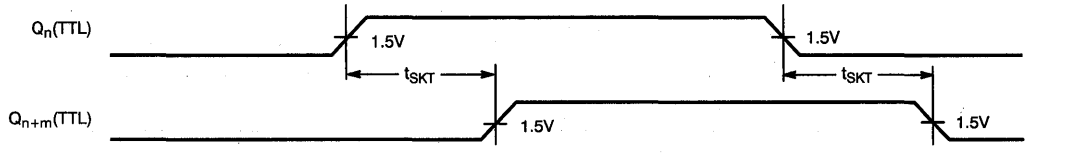
TTL-to-ECL Timing



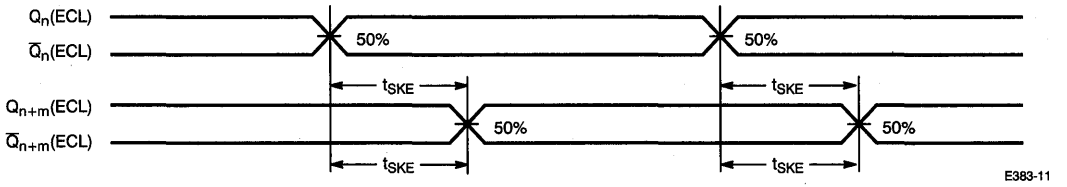
E383-9

Switching Waveforms (continued)

Skew Test (t_{SKT})
TTL_{Qn}-to-TTL_{Qn+m}



Skew Test (t_{SKE})
ECL_{Qn}, $\overline{Q}_n$-to-ECL_{Qn+m}, $\overline{Q}_{n+m}$



ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL $\overline{D}_n$	TTL Q_n
Open[17]	Open[17]	L
L	H	L
H	L	H

Note:
17. The ECL inputs will pull to a known logic level if left open.

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL $\overline{Q}_n$
L	L	H
H	H	L

Nominal Voltages

The CY101/10E383 can be used in dual ±5V or single +5V supply systems. The supply pins should be connected as shown in *Tables 1* and *2*. This connection technique involves shifting up all ECL supply pins by 5V. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding 5V. For example, if the termination is 50 ohms to −2V in a dual-supply system, the single +5V system should have 50 ohms to +3V. If the termination is a thévenin type, then the resistor tied to ground is now at +5V and the resistor tied to −5V is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL +5V supply lines will help to reduce the noise. *Table 3* shows the CY10E383 nominal voltages applied in a 10K system.

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−4.5V

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−5.2V

Table 3. CY10E383 Nominal Voltages Applied in 10K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−5.2V

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY10E383–2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383–2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY10E383–3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383–3NC	N80	80-Lead Plastic Quad Flatpack	
	CY10E383–3YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY101E383–2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383–2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY101E383–3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383–3NC	N80	80-Lead Plastic Quad Flatpack	

Document #: 38–A–00023–F

CY10E384L

CYPRESS SEMICONDUCTOR

ECL/TTL/ECL Translator

Features

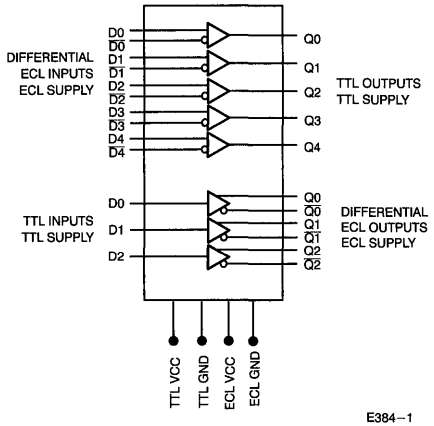
- **BiCMOS for optimum speed/power**
- **High speed (max.)**
  - **—3 ns t_{PD} TTL-to-ECL**
  - **—4 ns t_{PD} ECL-to-TTL**
- **Low skew < ± 1 ns**
- **Operates on single +5V supply**
- **28-pin SOJ package**
- **Capable of greater than 2001V ESD**
- **Low power (110 mA max.)**

Functional Description

The CY10E384L is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains three independent TTL-to-ECL and five independent ECL-to-TTL translators for high-speed data transmission, mixed logic, and bus applications. The CY10E384L functions using differential ECL I/O to provide balanced low-noise operation over controlled-impedance buses between TTL and/or ECL subsystems.

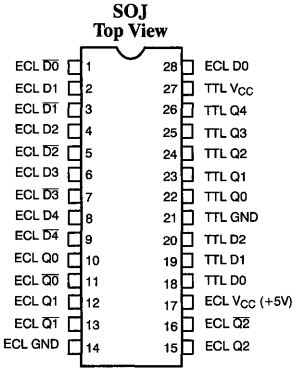
The device has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The translator is offered in ECL-compatible versions with +5.0V power supply. The TTL I/O is fully TTL compatible. The CY10E384L is packaged in 28-pin surface-mountable SOJ.

Logic Block Diagram



E384–1

Pin Configuration



E384–2

Selection Guide

	10E384L–3
Maximum Propagation Delay Time (ns) (TTL to ECL)	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	4
Maximum Operating Current (mA) I_{CC}	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

TTL Supply Voltage to Ground Potential .. – 0.5V to +7.0V

TTL DC Input Voltage ..... – 3.0V to +7.0V

ECL Supply Voltage V_{CC} to ECL GND ... –0.5V to +7.0V

ECL Input Voltage ..... - 0.5V to V_{CC}

ECL Output Current ..... –50 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V_{CC}	TTL V_{CC}
Commercial	10K 10KH	10E	0°C to +75°C	5V ± 5%	5V ± 5%

ECL DC Electrical Characteristics ECL V_{CC} = 5.0V [1, 2]

Parameter	Description	Test Conditions	Temperature[3]	10E384L Min.	10E384L Max.	Unit
V_{OH}	Output HIGH Voltage	10E, R_L = 50Ω to +3V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C	+3950	+4160	mV
			T_A = +25°C	+3990	+4190	mV
			T_A = +75°C	+4050	+4265	mV
V_{OL}	Output LOW Voltage	10E, R_L = 50Ω to +3V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C	+3080	+3285	mV
			T_A = +25°C	+3100	+3300	mV
			T_A = +75°C	+3120	+3325	mV
V_{IH}	Input HIGH Voltage	10E	T_A = 0°C	+3830	+4160	mV
			T_A = +25°C	+3870	+4190	mV
			T_A = +75°C	+3930	+4280	mV
V_{IL}	Input LOW Voltage	10E	T_A = 0°C	+3050	+3520	mV
			T_A = +25°C	+3050	+3525	mV
			T_A = +75°C	+3050	+3550	mV
V_{cm}[4]	Common Mode Voltage	±V_{cm} with respect to V_{BB} (+3.7V)			1.0	V
V_{diff}	Input Voltage Differential	Required for Full Output Swing		150		mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.		−0.5	170	µA

TTL DC Electrical Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions	10E384L Min.	10E384L Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Max., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage[5]		2.0		V
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{CD}	Input Clamp Diode Voltage	I_{IN} = −10 mA	−1.5		V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[6]	−180	−40	mA
I_{IX}	Input Load Current[7]	GND ≤ V_I ≤ V_{CC}	−250	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		110	mA

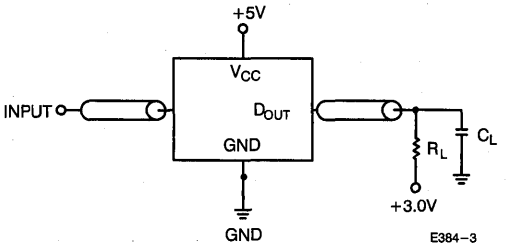
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance		4	pF
C_{OUT}	Output Capacitance		5	pF

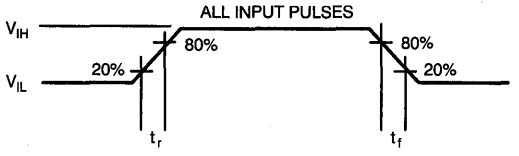
Notes:

1. See AC Test Load and Waveform for test conditions.
2. DC levels are specified with a nominal ECL V_{CC} of 5V. The levels will track the variations in ECL V_{CC}.
3. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
4. The internal gain of the CY10E384L guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
5. These are absolute values with respect to device ground.
6. Not more than one output should be tested at a time. Duration of the short should not be more than one second.
7. I/O pin leakage is the worst case of I_{IX} (where X = H or L).

ECL AC Test Load and Waveform[8, 9, 10, 11, 12]

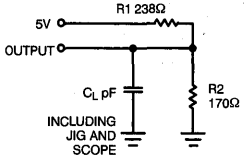


E384–3

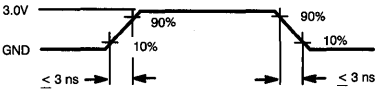


E384–4

TTL AC Test Load and Waveform[13]

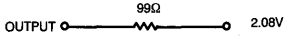


E384–6



E384–5

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E384L–3		Unit
			Min.	Max.	
t_{pLH}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	4	ns
t_{pHL}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E384L–3		Unit
			Min.	Max.	
t_{pLH}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	3	ns
t_{pHL}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	3	ns
t_r	Output Rise Time	20% to 80%	0.35	1.7	ns
t_f	Output Fall Time	20% to 80%	0.35	1.7	ns

Skew Time Switching Characteristics (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

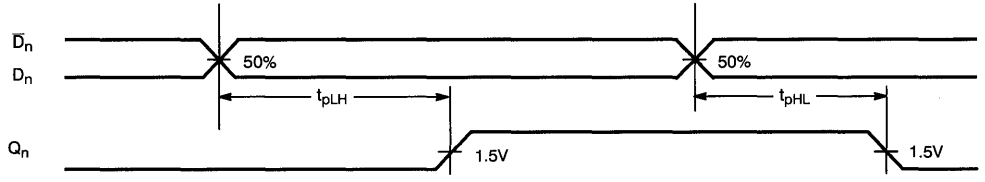
Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
t_{SKT}	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		±1	ns
t_{SKE}	Data Skew Time TTL-to-ECL	$ECLQ_n$, $\overline{Q}_n$ to $ECLQ_{n+m}$, $\overline{Q}_{n+m}$		±1	ns

Notes:

8. $V_{IL} = V_{IL}$ Min., $V_{IH} = V_{IH}$ Max.
9. ECL $R_L = 50\Omega$, $C_L < 5$ pF (includes fixture and stray capacitance).
10. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
11. $t_r = t_f = 0.7$ ns
12. All timing measurements are made from the 50% point of all waveforms.
13. TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and $C_L = 10$ pF.

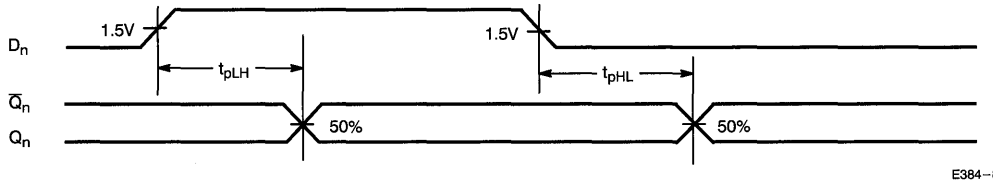
Switching Waveforms

ECL-to-TTL Timing



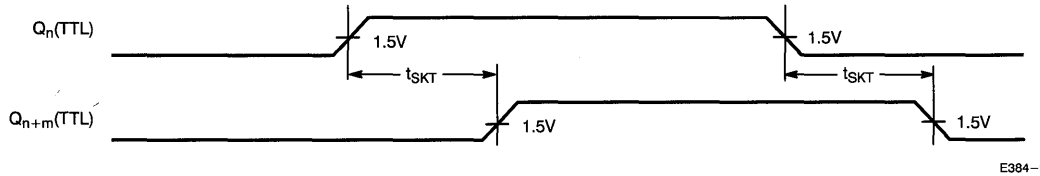
E384–7

TTL-to-ECL Timing



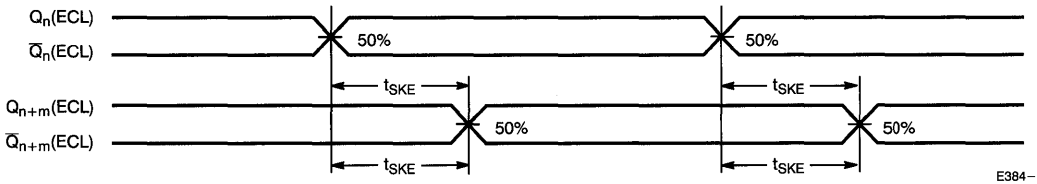
E384–8

Skew Test (t_{SKT})
TTL_{Qn}-to-TTL_{Qn+m}



E384–9

Skew Test (t_{SKE})
ECL_{Qn}, $\overline{Q}_n$-to-ECL_{Qn+m}, $\overline{Q}_{n+m}$



E384–10

9 ECL

ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL $\overline{D}_n$	TTL Q_n
Open	Open	L
L	H	L
H	L	H

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL $\overline{Q}_n$
L	L	H
H	H	L

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3	CY10E384L–3VC	V21	28-Lead Molded SOJ	Commercial

Document #: 38–A–00035

CYPRESS SEMICONDUCTOR

256 x 4 ECL Static RAM

Features

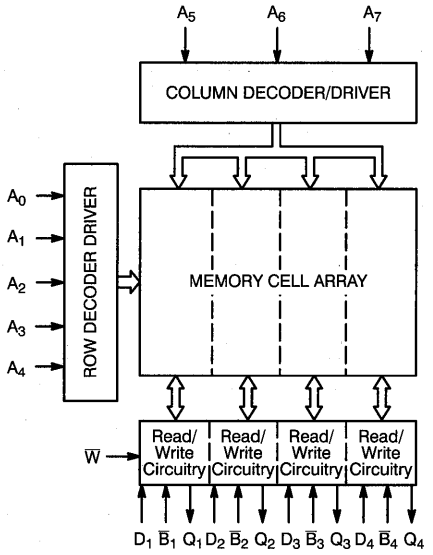
- **256 x 4-bit organization**
- **Ultra high speed/standard power**
  - **t_{AA} = 3.5 ns**
  - **I_{EE} = 220 mA**
- **Low-power version**
  - **t_{AA} = 5 ns**
  - **I_{EE} = 150 mA**
- **Both 10KH/10K- and 100K-compatible I/O versions**
- **10K/10KH military version**
- **Capable of withstanding >2001V ESD**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

The Cypress CY10E422 and CY100E422 are 256 x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. Both parts are fully decoded random access memories organized as 1024 words by 4 bits. The CY10E422 is 10KH/10K compatible and is available in a military version.. The CY100E422 is 100K compatible.

The four independent active LOW block select ($\overline{B}$) inputs control memory selection and allow for memory expansion and reconfiguration. Each block select ($\overline{B}_1$ through $\overline{B}_4$), when active, turns off the corresponding output and memory block. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{B}_X$ LOW, the corresponding data at D_X is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{B}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand or reconfigure the memory.

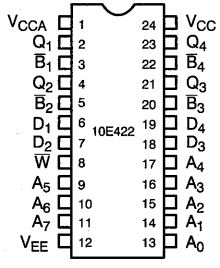
Logic Block Diagram



E422–1

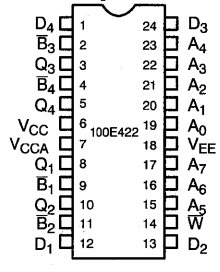
Pin Configurations (continued on next page)

CerDIP
Top View



E422–3

CerDIP
Top View



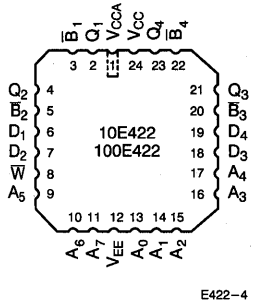
E422–2

Selection Guide

		10E422–4 100E422–3.5	10E422–5 100E422–5	10E422–7 100E422–7
Maximum Access Time (ns)		3.5/4	5	7
I_{EE} Max. (mA)	Commercial	220	220	
	L (Low Power)		150	150
	Military (10K/10KH only)		150	150

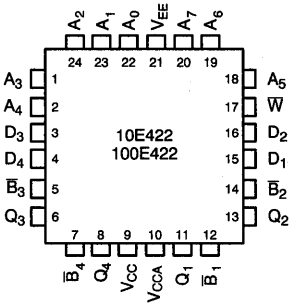
Pin Configurations (continued)

LCC
Top View



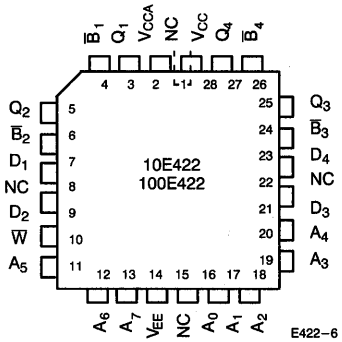
E422–4

Quad Cerpack
Top View



E422–5

PLCC
Top View



E422–6

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... – 7.0V to +0.5V

Input Voltage ..... V_{EE} to +0.5V

Output Current ..... – 50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard, L)	10KH/ 10K	0°C to 75°C	–5.2V±5%
Commercial (Standard, L)	100K	0°C to +85°C	– 4.5V±0.3V
Military (L)	10KH/ 10K	–55°C to +125°C Case	–5.2V±5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50Ω to – 2V V_{EE} = – 5.2V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = – 55°C	– 1140	– 900	mV
			T_A = 0°C	– 1000	– 840	mV
			T_A = +25°C	– 960	– 810	mV
			T_A = +75°C	– 900	– 735	mV
			T_C = +125°C	– 880	– 700	mV
		100K R_L = 50Ω to – 2V, V_{EE} = – 4.5V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	– 1025	– 880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to – 2V V_{EE} = – 5.2V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = – 55°C	– 1920	– 1670	mV
			T_A = +0°C	– 1870	– 1665	mV
			T_A = +25°C	– 1850	– 1650	mV
			T_A = +75°C	– 1830	– 1625	mV
		100K R_L = 50Ω to – 2V, V_{EE} = – 4.5V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = +125°C	– 1830	– 1610	mV
			T_A = 0°C to 85°C	– 1810	– 1620	mV

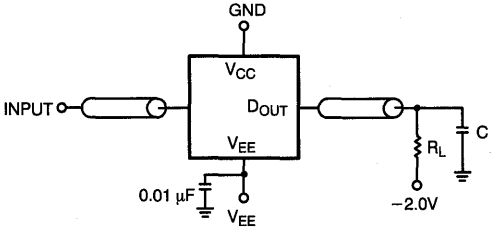
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	10E V_{EE} = − 5.2V V_{CC} = V_{CCA} = GND	T_C = − 55°C	− 1260	− 900	mV
			T_A = 0°C	− 1170	− 840	mV
			T_A = +25°C	− 1130	− 810	mV
			T_A = +75°C	− 1070	− 720	mV
		100K V_{EE} = − 4.5V V_{CC} = V_{CCA} = GND	T_C = +125°C	− 1030	− 700	mV
			T_A = 0°C to 85°C	− 1165	− 880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = − 5.2V V_{CC} = V_{CCA} = GND	T_C = − 55°C	− 1950	− 1540	mV
			T_A = 0°C	− 1950	− 1480	mV
			T_A = +25°C	− 1950	− 1475	mV
			T_A = +75°C	− 1950	− 1450	mV
			T_C = +125°C	− 1950	− 1450	mV
		100K V_{EE} = − 4.5V V_{CC} = V_{CCA} = GND	T_A = 0°C to 85°C	− 1810	− 1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{B}$ inputs[3]	0.5	170	µA
			All other inputs	− 50		
I_{EE}	Supply Current (All inputs and outputs open)	Commercial/Military L (Low Power)		− 150		mA
		Commercial Standard		− 220		mA

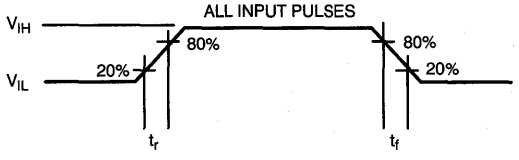
Capacitance[4]

Parameter	Description	Typ.	Max.[5]	Unit
C_{IN}	Input Pin Capacitance	4	5	pF
C_{OUT}	Output Pin Capacitance	5	6	pF

AC Test Loads and Waveforms[6, 7, 8, 9, 10, 11]



E422–7



E422–8

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. 10E specifications support both 10K and 10KH compatibility.
3. $\overline{B}$ inputs have pull-down resistors, all other inputs do not have pull-downs. The value of the resistors is nominally 50 kΩ, so the $\overline{B}$ inputs are active when left floating.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except cerDIP (D40), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.
6. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
7. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
8. R_L = 50Ω, C < 5 pF (3-ns grade) or < 30 pF (5-, 7-ns grade). Includes fixture and stray capacitance.
9. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
10. t_r = t_f = 0.7 ns.
11. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Commercial Operating Range

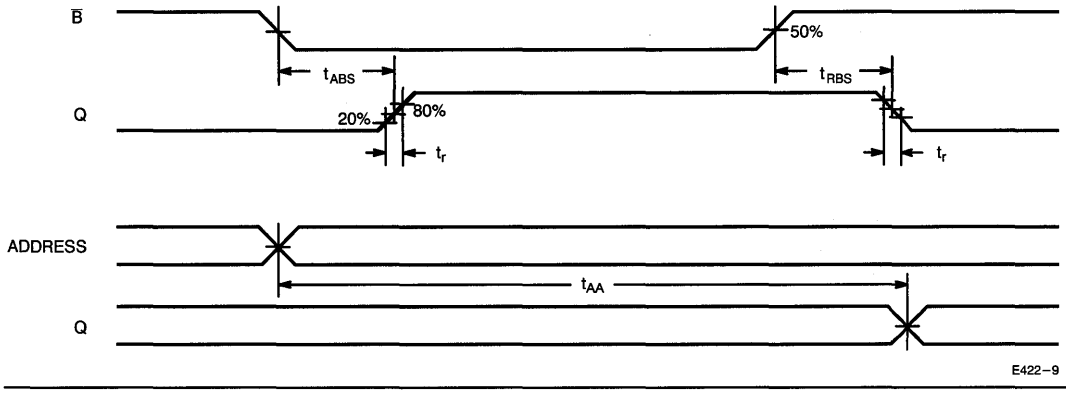
Parameter	Description	100E422–3.5		10E422–4		10E422–5 100E422–5		10E422–7 100E422–7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ABS}	Block Select to Output Delay		2.5		2.5	0.5	3.0	0.5	4.0	ns
t_{RBS}	Block Select Recovery		2.5		2.5	0.5	3.0	0.5	4.0	ns
t_{AA}	Address Access Time		3.5		4.0	1.2	5.0	1.2	7.0	ns
t_W	Write Pulse Width	3.5		3.5		3.5		5.0		ns
t_{WSD}	Data Set-Up to Write	0.5		0.5		0.5		1.0		ns
t_{WHD}	Data Hold to Write	1.0		1.0		1.0		1.0		ns
t_{WSA}	Address Set-Up/Write	0.5		0.5		0.5		1.0		ns
t_{WHA}	Address Hold/Write	1.0		1.0		1.0		1.0		ns
t_{WSBS}	Block Select Set-Up/Write	0.5		0.5		0.5		1.0		ns
t_{WHBS}	Block Select Hold/Write	1.0		1.0		1.0		1.0		ns
t_{WS}	Write Disable	0.3	2.5	0.3	2.5	0.3	3.5	0.3	4.0	ns
t_{WR}	Write Recovery	0.5	3.5	0.5	3.5	0.5	3.5	0.5	8.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	0.35	2.5	1.0	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	2.5	1.0	2.5	ns

Switching Characteristics Over the Military Operating Range

Parameter	Description	10E422–5		10E422–7		Unit
		Min.	Max.	Min.	Max.	
t_{ABS}	Block Select to Output Delay	0.5	4.0	0.5	4.0	ns
t_{RBS}	Block Select Recovery	0.5	4.0	0.5	4.0	ns
t_{AA}	Address Access Time	1.2	5.0	1.2	7.0	ns
t_W	Write Pulse Width	5.0		5.0		ns
t_{WSD}	Data Set-Up to Write	0		0		ns
t_{WHD}	Data Hold to Write	1.0		1.0		ns
t_{WSA}	Address Set-Up/Write	1.0		1.0		ns
t_{WHA}	Address Hold/Write	1.0		1.0		ns
t_{WSBS}	Block Select Set-Up/Write	0		0		ns
t_{WHBS}	Block Select Hold/Write	1.0		1.0		ns
t_{WS}	Write Disable	0.3	4.0	0.3	4.0	ns
t_{WR}	Write Recovery	0.5	5.0	0.5	8.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

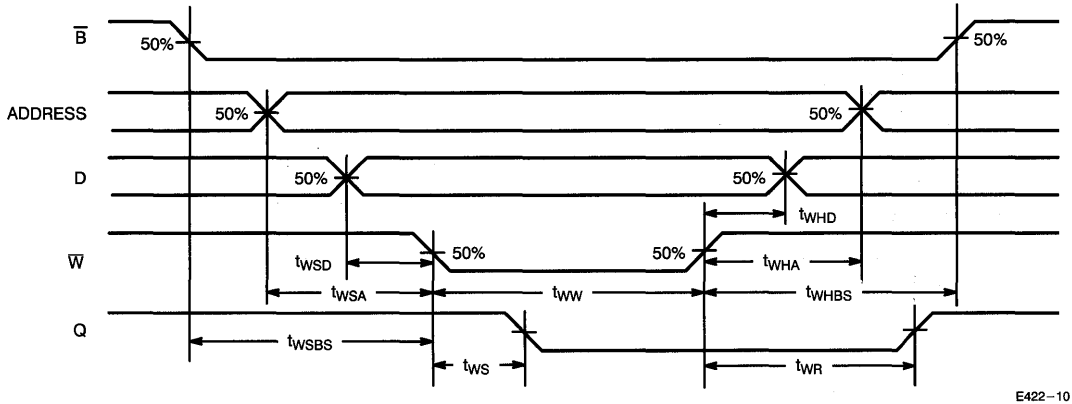
Switching Waveforms

Read Mode



E422–9

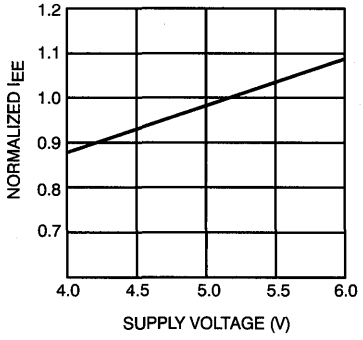
Write Mode



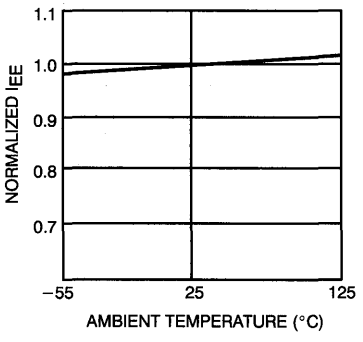
E422–10

Typical DC and AC Characteristics (10E422/10E422L/100E422/100E422L)

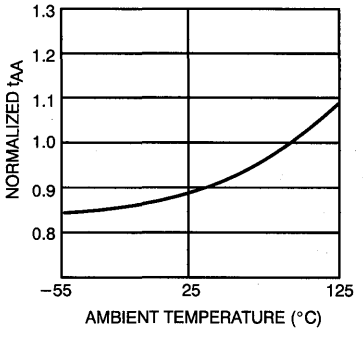
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



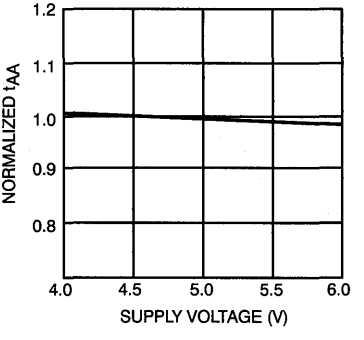
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



Truth Table

Inputs			Output	
$\overline{B}_X$	$\overline{W}$	D_X	Q_X	Mode
H	X	X	L	Disabled
L	L	H	L	Write H
L	L	L	L	Write L
L	H	X	Out	Read

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type	Operating Range
10E[12]	220	4	CY10E422–4KC	K63	24-Lead Square Cerpack	Commercial
			CY10E422–4LC	L63	24-Square Leadless Chip Carrier	
		5	CY10E422–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY10E422–5KC	K63	24-Lead Square Cerpack	
			CY10E422–5LC	L63	24-Square Leadless Chip Carrier	
	150	5	CY10E422L–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY10E422L–5JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY10E422L–5KC	K63	24-Lead Square Cerpack	
			CY10E422L–5LC	L63	24-Square Leadless Chip Carrier	
			CY10E422L–5DMB	D40	24-Lead (400-Mil) Sidebraze DIP	Military
			CY10E422L–5KMB	K63	24-Lead Square Cerpack	
		7	CY10E422L–7DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY10E422L–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY10E422L–7KC	K63	24-Lead Square Cerpack	
			CY10E422L–7LC	L63	24-Square Leadless Chip Carrier	
			CY10E422L–7DMB	D40	24-Lead (400-Mil) Sidebraze DIP	Military
			CY10E422L–7KMB	K63	24-Lead Square Cerpack	
100K	220	3.5	CY100E422–3.5KC	K63	24-Lead Square Cerpack	Commercial
			CY100E422–3.5LC	L63	24-Square Leadless Chip Carrier	
		5	CY100E422–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY100E422–5KC	K63	24-Lead Square Cerpack	
			CY100E422–5LC	L63	24-Square Leadless Chip Carrier	
	150	5	CY100E422L–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY100E422L–5JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY100E422L–5KC	K63	24-Lead Square Cerpack	
			CY100E422L–5LC	L63	24-Square Leadless Chip Carrier	
		7	CY100E422L–7DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY100E422L–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY100E422L–7KC	K63	24-Lead Square Cerpack	
			CY100E422L–7LC	L63	24-Square Leadless Chip Carrier	

Note:
12. 10E specifications support both 10K and 10KH compatibility.

Document #: 38–A–00002–C

CY10E470
CY100E470

CYPRESS SEMICONDUCTOR

4K x 1 ECL Static RAM

Features

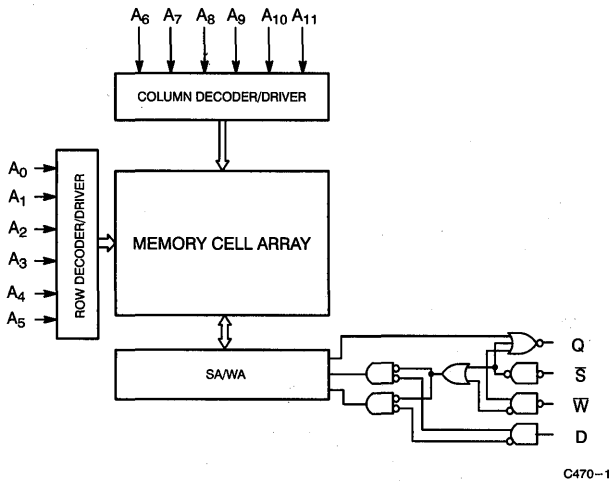
- **4096 x 1—bit organization**
- **High speed/low power**
  - **— t_{AA} = 5 ns**
  - **— I_{EE} = 200 mA**
- **Both 10K- and 100K-compatible versions**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

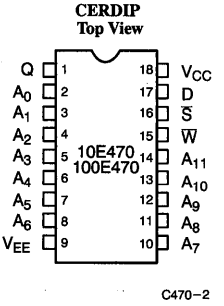
The Cypress CY10E470 and CY100E470 are ECL RAMs designed for scratch pad, control, and buffer storage applications. Both parts are fully decoded random access memories organized as 4096 words by 1 bit. The CY10E470 is 10K-compatible. The CY100E470 is 100K-compatible.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at D is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection in order to expand the memory.

Logic Block Diagram



Pin Configuration



Selection Guide

	10E470-5 100E470-5	10E470-7 100E470-7
Maximum Access Time (ns)	5	7
I_{EE} Max. (mA)	200	200

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... −7.0V to +0.5V

Input Voltage ..... V_{EE} to +0.5V

Output Current ..... −50 mA

Operating Range referenced to V_{CC}

Range	Version	Ambient Temperature	V_{EE}
Commercial	10E	0°C to + 75°C	−5.2V ± 5%
Commercial	100E	0°C to + 85°C	−4.5V ± 0.3V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	10E R_L = 50Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1000	−840	mV
			T_A = +25°C	−960	−810	mV
			T_A = +75°C	−900	−720	mV
		100K R_L = 50Ω to −2V V_{EE} = −4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1870	−1665	mV
			T_A = +25°C	−1850	−1650	mV
			T_A = +75°C	−1830	−1625	mV
		100K R_L = 50Ω to −2V V_{EE} −4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1810	−1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1145	−840	mV
			T_A = +25°C	−1105	−810	mV
			T_A = +75°C	−1045	−720	mV
		100K V_{EE} = −4.5V	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1870	−1490	mV
			T_A = +25°C	−1850	−1475	mV
			T_A = +75°C	−1830	−1450	mV
		100K V_{EE} = −4.5V	T_A = 0°C to 85°C	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	−50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial		−200		mA

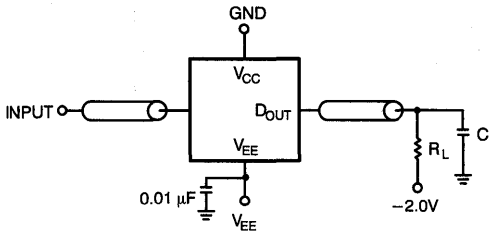
Capacitance[2]

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Pin Capacitance		4		pF
C_{OUT}	Output Pin Capacitance		6		pF

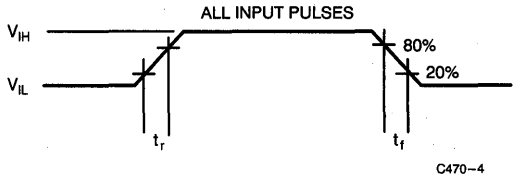
Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3, 4, 5, 6, 7, 8]



C470–3



C470–4

Switching Characteristics Over the Operating Range

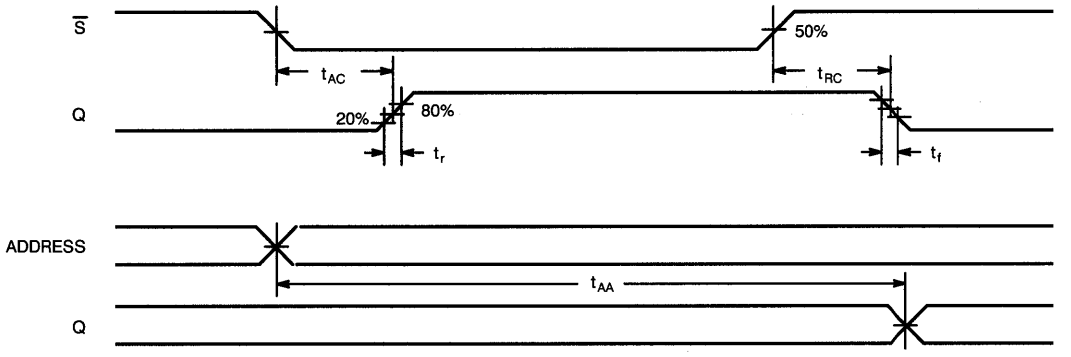
Parameter	Description	10E470–5 100E470–5		10E470–7 100E470–7		Unit
		Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		3.0		3.5	ns
t_{RC}	Chip Select Recovery		3.0		3.5	ns
t_{AA}	Address Access Time		5.0		7.0	ns
t_{WW}	Write Pulse Width	5.0		7.0		ns
t_{SD}	Data Set-Up to Write	0		0		ns
t_{HD}	Data Hold to Write	0		0		ns
t_{SA}	Address Set-Up/Write	0		1.0		ns
t_{HA}	Address Hold/Write	0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0		0		ns
t_{HC}	Chip Select Hold/Write	0		0		ns
t_{WS}	Write Disable		3.0		3.5	ns
t_{WR}	Write Recovery		5.0		8.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

Notes:

3. $V_{IL} = V_{IL}$ Min., $V_{IH} = V_{IH}$ Max. on 10E version.
4. $V_{IL} = -1.7V$, $V_{IH} = -0.9V$ on 100K version.
5. $R_L = 50\Omega$, C < 30 pF (includes fixture and stray capacitance).
6. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
7. $t_r = t_f = 0.7$ ns.
8. All timing measurements are made from the 50% point of all waveforms.

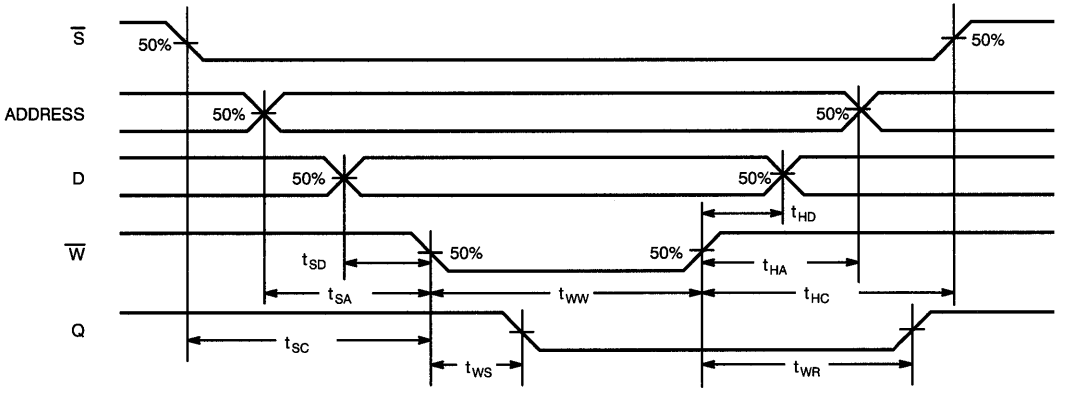
Switching Waveforms

Read Mode



C470–5

Write Mode



C470–6

Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type	Operating Range
10K	200	5.0	CY10E470–5DC	D4	18-Lead (300-Mil) CerDIP	Commercial
		7.0	CY10E470–7DC	D4	18-Lead (300-Mil) CerDIP	
100K	200	5.0	CY100E470–5DC	D4	18-Lead (300-Mil) CerDIP	Commercial
		7.0	CY100E470–7DC	D4	18-Lead (300-Mil) CerDIP	

Document #: 38–A–00003–B

CY10E474
CY100E474

1K x 4 ECL Static RAM

Features

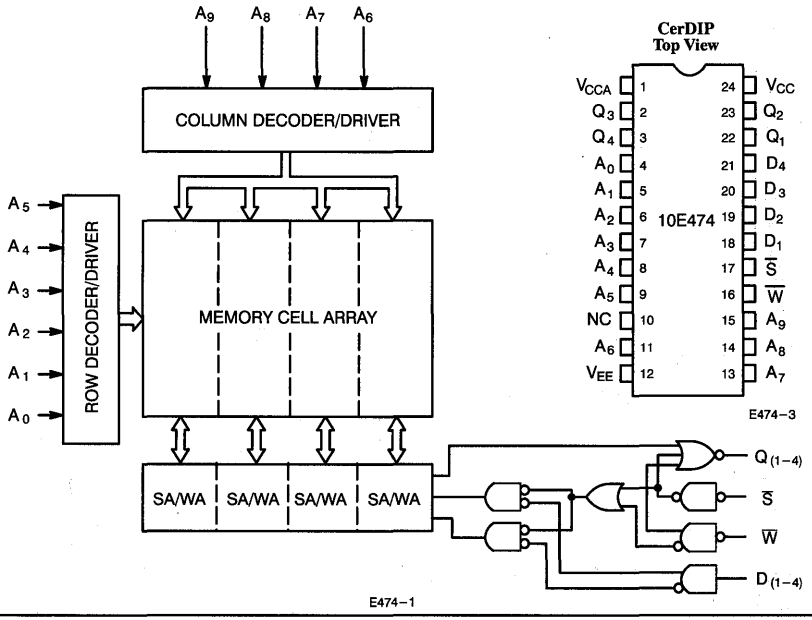
- **1024 x 4-bit organization**
- **Ultra high speed/standard power**
  - **t_{AA} = 3.5 ns**
  - **I_{EE} = 275 mA**
- **Low-power version**
  - **t_{AA} = 5 ns**
  - **I_{EE} = 190 mA**
- **Both 10KH/10K- and 100K-compatible I/O versions**
- **10K/10KH military version**
- **Capable of withstanding >2001V ESD**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

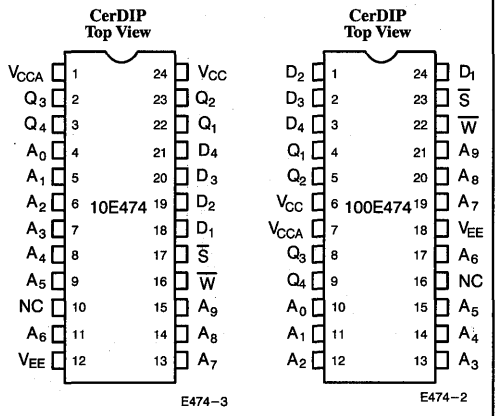
The Cypress CY10E474 and CY100E474 are 1K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 1024 words by 4 bits. The CY10E474 is 10KH/10K compatible and is available in a military version. The CY100E474 is 100K comptaible.

The active LOW chip select (S) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable (W) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, $\overline{W}$ is held HIGH while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

Logic Block Diagram



Pin Configurations (continued next page)

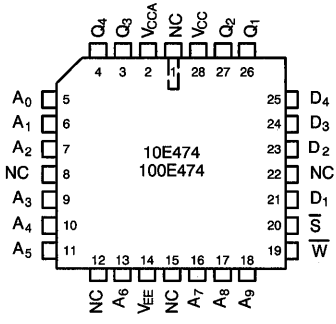


Selection Guide

		10E474-4 100E474-3.5	10E474-5 100E474-5	10E474-7 100E474-7
Maximum Access Time (ns)		3.5/4	5	7
I_{EE} Max. (mA)	Commercial	275	275	
	L		190	190
	Military (10K/10KH only)		190	190

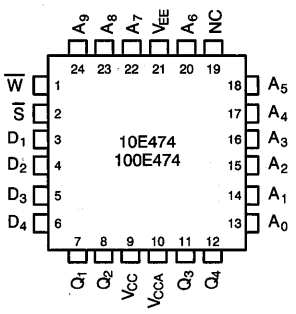
Pin Configurations (continued)

PLCC
Top View



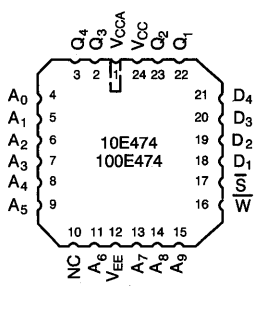
E474–4

Quad Cerpack
Top View



E474–5

LCC
Top View



E474–6

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... − 7.0V to +0.5V

Input Voltage ..... V_{EE} to + 0.5V

Output Current ..... −50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard,L)	10KH/10K	0°C to 75°C	−5.2V ± 5%
Commercial (Standard,L)	100K	0°C to + 85°C	−4.5V ± 0.3V
Military (L)	10KH/10K	−55°C to +125°C Case	−5.2V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50Ω to −2V V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = −55°C	−1140	−900	mV
			T_A = 0°C	−1000	−840	mV
			T_A = +25°C	−960	−810	mV
			T_A = +75°C	−900	−735	mV
			T_C = +125°C	−880	−700	mV
		100K R_L = 50Ω to −2V, V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to −2V V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = −55°C	−1920	−1670	mV
			T_A = +0°C	−1870	−1665	mV
			T_A = +25°C	−1850	−1650	mV
			T_A = +75°C	−1830	−1625	mV
			T_C = +125°C	−1830	−1610	mV
		100K R_L = 50Ω to −2V, V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1810	−1620	mV

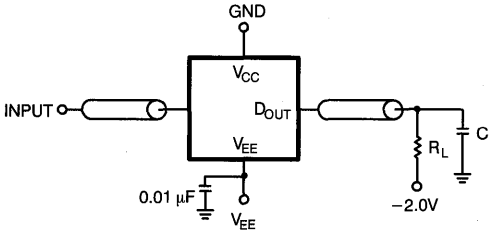
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	10E V_{EE} = −5.2V V_{CC} = V_{CCA} = GND	T_C = −55°C	−1260	−900	mV
			T_A = 0°C	−1170	−840	mV
			T_A = +25°C	−1130	−810	mV
			T_A = +75°C	−1070	−720	mV
			T_C = +125°C	−1030	−700	mV
		100K V_{EE} = −4.5V	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = −5.2V V_{CC} = V_{CCA} = GND	T_C = −55°C	−1950	−1540	mV
			T_A = 0°C	−1950	−1480	mV
			T_A = +25°C	−1950	−1475	mV
			T_A = +75°C	−1950	−1450	mV
			T_C = +125°C	−1950	−1450	mV
		100K V_{EE} = −4.5V V_{CC} = V_{CCA} = GND	T_C = 0°C to 85°C	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	−50		
I_{EE}	Supply Current (All inputs and outputs open)	Commercial/Military Standard L (Low Power)		−190		mA
		Commercial Standard		−275		mA

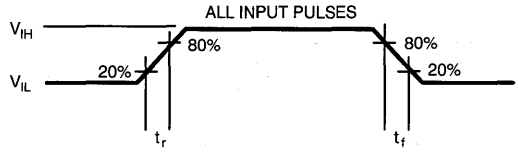
Capacitance[3]

Parameter	Description	Typ.	Max.[4]	Unit
C_{IN}	Input Pin Capacitance	4	5	pF
C_{OUT}	Output Pin Capacitance	5	6	pF

AC Test Loads and Waveforms[5, 6, 7, 8, 9, 10]



E474–7



E474–8

Notes:
1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. 10E specifications support both 10K and 10KH compatibility.
3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except cerDIP (D40), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.
5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
7. R_L = 50Ω, C < 5 pF (3.5/4-ns grade) or < 30 pF (5-, 7-ns grade). Includes fixture and stray capacitance.
8. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. t_r = t_f = 0.7 ns.
10. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Commercial Operating Range

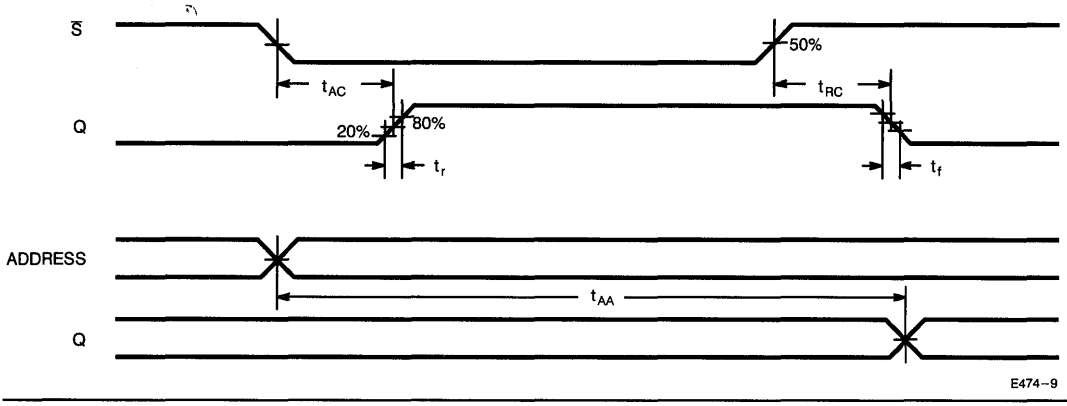
Parameter	Description	100E474–3.5		10E474–4		10E474–5 100E474–5		10E474–7 100E474–7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		2.5		2.5	0.5	3.0	0.5	5.0	ns
t_{RC}	Chip Select Recovery		2.5		2.5	0.5	3.0	0.5	5.0	ns
t_{AA}	Address Access Time		3.5		4.0	1.2	5.0	1.2	7.0	ns
t_{WW}	Write Pulse Width	5.0		5.0		5.0		5.0		ns
t_{SD}	Data Set-Up to Write	0		0		0		0		ns
t_{HD}	Data Hold to Write	0		0		0		1.0		ns
t_{SA}	Address Set-Up/Write	0		0		0		1.0		ns
t_{HA}	Address Hold/Write	0		0		0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0		0		0		0		ns
t_{HC}	Chip Select Hold/Write	0		0		0		1.0		ns
t_{WS}	Write Disable	0.3	2.5	0.3	2.5	0.3	3.0	0.3	6.5	ns
t_{WR}	Write Recovery	0.5	3.5	0.5	3.5	0.5	5.0	0.5	7.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	0.35	2.5	1.0	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	2.5	1.0	2.5	ns

Switching Characteristics Over the Military Operating Range

Parameter	Description	10E474–5		10E474–7		Unit
		Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay	0.5	4.0	0.5	5.0	ns
t_{RC}	Chip Select Recovery	0.5	4.0	0.5	5.0	ns
t_{AA}	Address Access Time	1.2	5.0	1.2	7.0	ns
t_{WW}	Write Pulse Width	5.0		5.0		ns
t_{SD}	Data Set-Up to Write	0		0		ns
t_{HD}	Data Hold to Write	1.0		1.0		ns
t_{SA}	Address Set-Up/Write	1.0		1.0		ns
t_{HA}	Address Hold/Write	1.0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0		0		ns
t_{HC}	Chip Select Hold/Write	1.0		1.0		ns
t_{WS}	Write Disable	0.3	4.0	0.3	6.5	ns
t_{WR}	Write Recovery	0.5	5.0	0.5	7.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

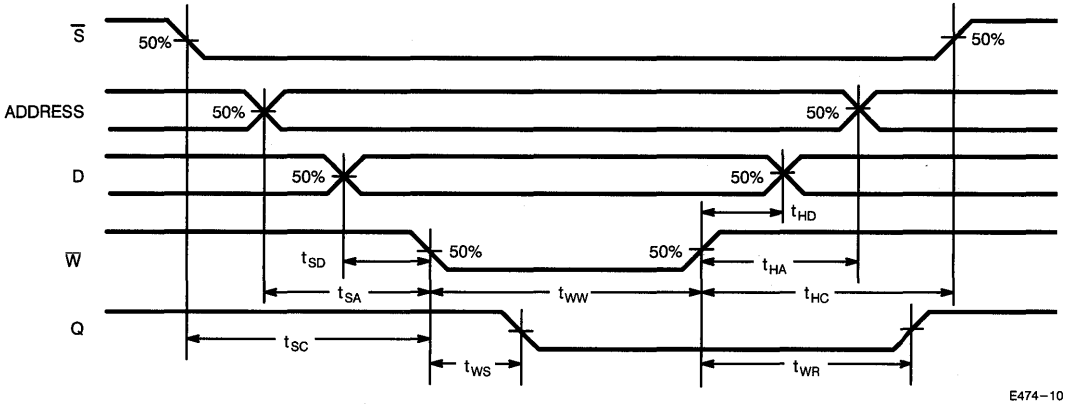
Switching Waveforms

Read Mode



E474–9

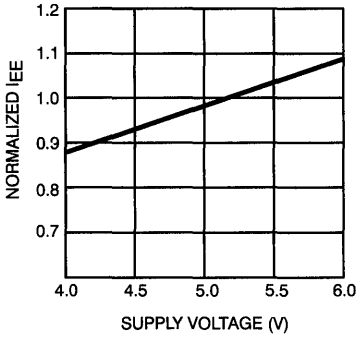
Write Mode



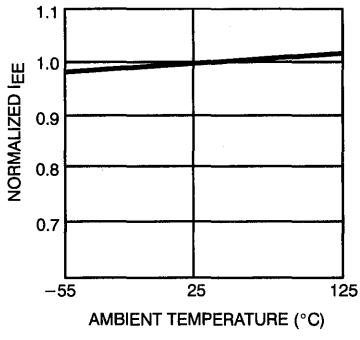
E474–10

Typical DC and AC Characteristics (10E474/10E474L/100E474/100E474L)

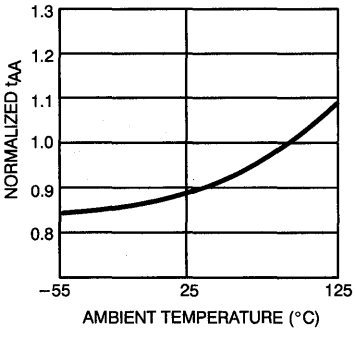
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



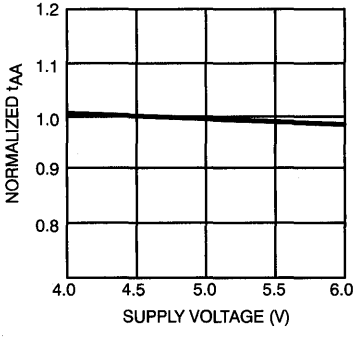
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	$\overline{D}$	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write H
L	L	L	L	Write L
L	H	X	D_{OUT}	Read

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type	Operating Range
100K	275	3.5	CY100E474–3.5KC	K63	24-Lead Square Cerpack	Commercial
			CY100E474–3.5LC	L63	24-Square Leadless Chip Carrier	
		5	CY100E474–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY100E474–5KC	K63	24-Lead Square Cerpack	
			CY100E474–5LC	L63	24-Square Leadless Chip Carrier	
	190	5	CY100E474L–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY100E474L–5JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY100E474L–5KC	K63	24-Lead Square Cerpack	
			CY100E474L–5LC	L63	24-Square Leadless Chip Carrier	
		7	CY100E474L–7DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY100E474L–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY100E474L–7KC	K63	24-Lead Square Cerpack	
			CY100E474L–7LC	L63	24-Square Leadless Chip Carrier	
10E[11]	275	4	CY10E474–4KC	K63	24-Lead Square Cerpack	Commercial
			CY10E474–4LC	L63	24-Square Leadless Chip Carrier	
		5	CY10E474–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	
			CY10E474–5KC	K63	24-Lead Square Cerpack	
			CY10E474–5LC	L63	24-Square Leadless Chip Carrier	
	190	5	CY10E474L–5DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY10E474L–5JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY10E474L–5KC	K63	24-Lead Square Cerpack	
			CY10E474L–5LC	L63	24-Square Leadless Chip Carrier	
			CY10E474L–5DMB	D40	24-Lead (400-Mil) Sidebraze DIP	Military
			CY10E474L–5KMB	K63	24-Lead Square Cerpack	
		7	CY10E474L–7DC	D40	24-Lead (400-Mil) Sidebraze DIP	Commercial
			CY10E474L–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY10E474L–7KC	K63	24-Lead Square Cerpack	
			CY10E474L–7LC	L63	24-Square Leadless Chip Carrier	
			CY10E474L–7DMB	D40	24-Lead (400-Mil) Sidebraze DIP	Military
			CY10E474L–7KMB	K63	24-Lead Square Cerpack	

Notes:
11. 10E specifications support both 10K and 10KH compatibility.

Document #: 38–A–00004–D

CY101E484
CY10E484
CY100E484

CYPRESS SEMICONDUCTOR

4K x 4 ECL Static RAM

Features

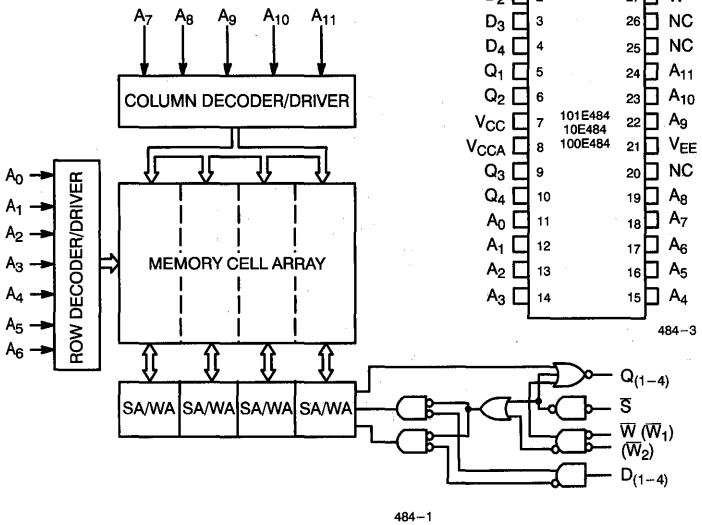
- **4096 x 4-bit organization**
- **Ultra high speed/standard power**
  - **—t_{AA} = 4, 5 ns**
  - **—I_{EE} = 320 mA**
- **Low-power version**
  - **—t_{AA} = 7, 10 ns**
  - **—I_{EE} = 200 mA**
- **Both 10KH/10K- and 100K-compatible I/O versions**
- **On-chip voltage compensation for improved noise margin**
- **Capable of withstanding >2001V ESD**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

The Cypress CY101E484, CY10E484, and CY100E484 are 4K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These parts are fully decoded random access memories organized as 4K words by 4 bits. The CY10E484 is 10KH-/10K-compatible. The CY100E484 is 100K-compatible, and the CY101E484 is 100K-compatible with a −5.2V supply.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, $\overline{W}$ is held HIGH while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory. The 4-ns and 5-ns devices are packaged in 28-pin cerDIPs, CLCCs, and rectangular cerpacks in the high-performance center power-ground version pin configurations. The 7-ns and 10-ns parts are offered with two write enables ($\overline{WE}_1$, $\overline{WE}_2$).

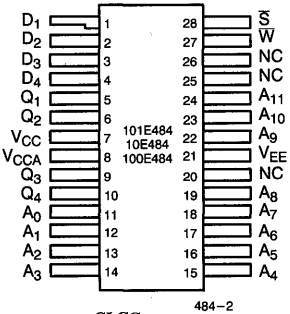
Logic Block Diagram



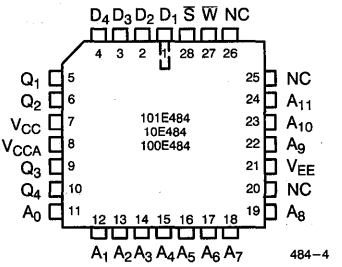
Pin Configurations (4-/5-ns Center Power/Ground Only)

CerDIP
Top View

Rectangular Cerpack
Top View



CLCC
Top View

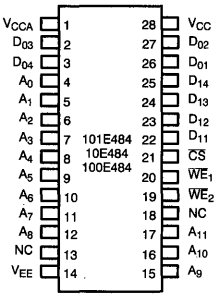


Selection Guide

		101E484−4 10E484−4 100E484−4	101E484−5 10E484−5 100E484−5	101E484−7 10E484−7 100E484−7	101E484−10 10E484−10 100E484−10
Maximum Access Time (ns)		4	5	7	10
I_{EE} Max. (mA)	Standard	320	320		
	Low Power (L)			200	200
	Military (10K/10KH only)		320	200	200

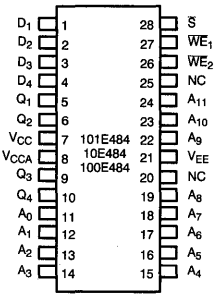
Pin Configurations (7 ns, 10 ns)

CerDIP
Top View



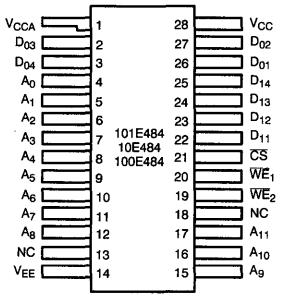
484–5

SOJ
Top View



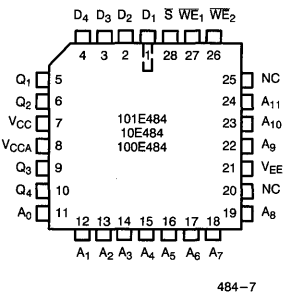
484–8

Rectangular Cerpack
Top View



484–6

PLCC
Top View



484–7

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... – 7.0V to +0.5V

Input Voltage ..... V_{EE} to +0.5V

Output Current ..... – 50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard, L)	10KH/ 10K	0°C to 75°C	– 5.2V ±5%
Commercial (Standard, L)	100K	0°C to +85°C	– 4.5V ±0.3V
Commercial (Standard, L)	101	0°C to 75°C	– 5.2V ±5%
Military (Standard, L)	10KH/ 10K	– 55°C to +125°C Case	– 5.2V ±5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50Ω to – 2V V_{EE} = – 5.2V V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = – 55°C	– 1140	– 900	mV
			T_A = 0°C	– 1000	– 840	mV
			T_A = +25°C	– 960	– 810	mV
			T_A = +75°C	– 900	– 735	mV
			T_C = +125°C	– 880	– 700	mV
		100/101K R_L = 50Ω to – 2V V_{EE} = – 4.5V (5.2V for 101K) V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C (75°C for 101K)	– 1025	– 880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to – 2V V_{EE} = – 5.2V V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = – 55°C	–1920	–1670	mV
			T_A = +0°C	–1870	–1665	mV
			T_A = +25°C	–1850	–1650	mV
			T_A = +75°C	–1830	–1625	mV
			T_C = +125°C	–1830	–1610	mV
		100/101K R_L = 50Ω to – 2V V_{EE} = – 4.5V (5.2V for 101K) V_{CC} = V_{CCA} = GND V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C (75°C for 101K)	–1810	–1620	mV

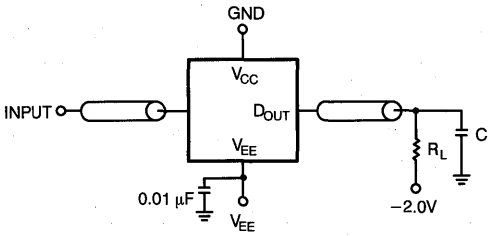
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	10E V_{EE} = − 5.2V V_{CC} = V_{CCA} = GND	T_C = −55°C	−1260	−900	mV
			T_A = 0°C	−1170	−840	mV
			T_A = +25°C	−1130	−810	mV
			T_A = +75°C	−1070	−720	mV
			T_C = +125°C	−1030	−700	mV
		100K V_{EE} = − 4.5V (− 5.2V for 101K), V_{CC} = V_{CCA} = GND	T_A = 0°C to 85°C (75°C for 101K)	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = − 5.2V V_{CC} = V_{CCA} = GND	T_C = −55°C	−1950	−1540	mV
			T_A = 0°C	−1950	−1480	mV
			T_A = +25°C	−1950	−1475	mV
			T_A = +75°C	−1950	−1450	mV
			T_C = +125°C	−1950	−1450	mV
		100/101K V_{EE} = − 4.5V (− 5.2V for 101K), V_{CC} = V_{CCA} = GND	T_A = 0°C to 85°C (75°C for 101K)	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	−50		
I_{EE}	Supply Current (All inputs and outputs open)	Commercial/Military L (Low Power)		−200		mA
		Commercial and Military Standard Power		−320		mA

Capacitance[3]

Parameter	Description	Typ.	Max.[4]	Unit
C_{IN}	Input Pin Capacitance	4	6	pF
C_{OUT}	Output Pin Capacitance	5	7	pF

AC Test Loads and Waveforms[5, 6, 7, 8, 9, 10]



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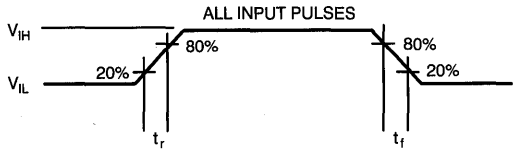

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Notes:
1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. 10E specifications support both 10K and 10KH compatibility.
3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except cerDIP (D42), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.
5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
7. R_L = 50Ω, C < 5 pF (4-, 5-ns grade) or < 30 pF (7-, 10-ns grade). Includes fixture and stray capacitance.
8. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. t_r = t_f = 0.7 ns.
10. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Commercial Operating Range

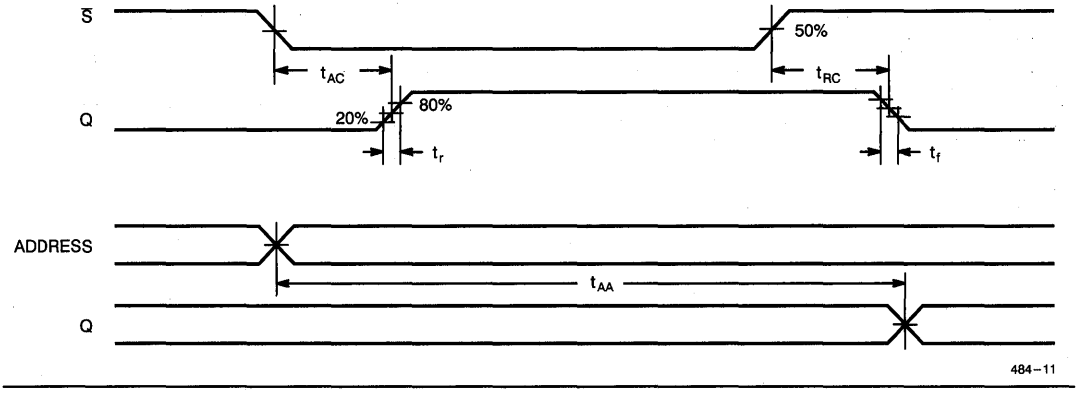
Parameter	Description	101E484–4 10E484–4 100E484–4		101E484–5 10E484–5 100E484–5		101E484–7 10E484–7 100E484–7		101E484–10 10E484–10 100E484–10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		3		3	0.5	4	0.5	5	ns
t_{RC}	Chip Select Recovery		3		3	0.5	4	0.5	5	ns
t_{AA}	Address Access Time		4		5	1.2	7	1.2	10	ns
t_{WW}	Write Pulse Width	5		5		5		6		ns
t_{NWW}	Non-Write Pulse		1.5		1.5		1.5		1.5	ns
t_{SD}	Data Set-Up to Write	0		0		1		2		ns
t_{HD}	Data Hold to Write	0		0		1		2		ns
t_{SA}	Address Set-Up/Write	0		0		1		2		ns
t_{HA}	Address Hold/Write	0		0		1		2		ns
t_{SC}	Chip Select Set-Up/Write	0		0		1		2		ns
t_{HC}	Chip Select Hold/Write	0		0		1		2		ns
t_{WS}	Write Disable	0.3	3	0.3	3	0.3	5	0.3	5	ns
t_{WR}	Write Recovery	0.5	4	0.5	5	0.5	8	0.5	12	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	1	2.5	1	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	1	2.5	1	2.5	ns

Switching Characteristics Over the Military Operating Range

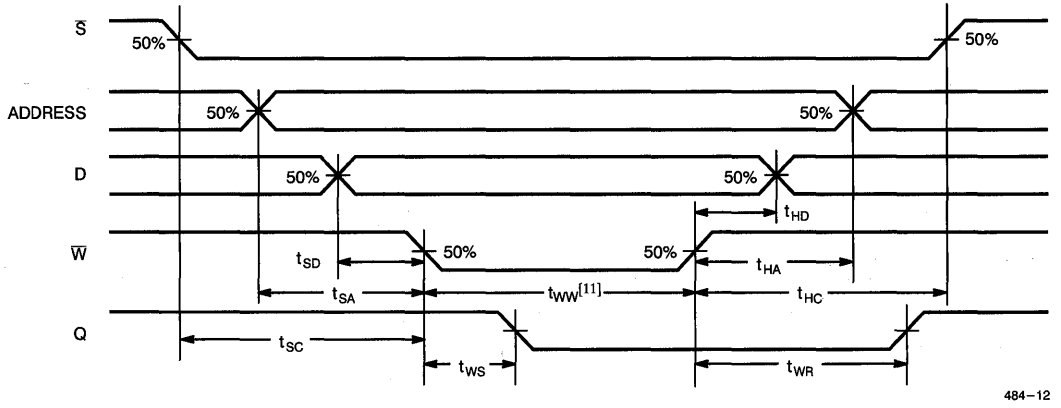
Parameter	Description	10E484–5		10E484–7		10E484–10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		3	0.5	4	0.5	5	ns
t_{RC}	Chip Select Recovery		3	0.5	4	0.5	5	ns
t_{AA}	Address Access Time		5	1.2	7	1.2	10	ns
t_{WW}	Write Pulse Width	5		5		6		ns
t_{NWW}	Non-Write Pulse		1.5		1.5		1.5	ns
t_{SD}	Data Set-Up to Write	1		1		2		ns
t_{HD}	Data Hold to Write	1		1		2		ns
t_{SA}	Address Set-Up/Write	1		1		2		ns
t_{HA}	Address Hold/Write	1		1		2		ns
t_{SC}	Chip Select Set-Up/Write	1		1		2		ns
t_{HC}	Chip Select Hold/Write	1		1		2		ns
t_{WS}	Write Disable	0.3	3	0.3	5	0.3	5	ns
t_{WR}	Write Recovery	0.5	5	0.5	8	0.5	12	ns
t_r	Output Rise Time	0.35	1.5	1	2.5	1	2.5	ns
t_f	Output Fall Time	0.35	1.5	1	2.5	1	2.5	ns

Switching Waveforms

Read Mode



Write Mode



Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write H
L	L	L	L	Write L
L	H[12]	X	D_{OUT}	Read

Notes:
11. If $t_{WW} \leq t_{NWW}$, the device will not write data to the addressed location.
12. The 7-ns and 10-ns parts have two $\overline{WE}$ pins. Both $\overline{WE}_1$ and $\overline{WE}_2$ must be LOW to initiate write operation.

CYPRESS SEMICONDUCTOR

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type/ Pinout	Operating Range
101E[13]	320	4	CY101E484–4DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	Commercial
			CY101E484–4KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY101E484–4YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
		5	CY101E484–5DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	
			CY101E484–5KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY101E484–5YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
	200	7	CY101E484L–7DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Commercial
			CY101E484L–7JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY101E484L–7KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY101E484L–7VC	V21	28-Lead Molded SOJ Center Power/Ground	
		10	CY101E484L–10DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	
			CY101E484L–10JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY101E484L–10KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY101E484L–10VC	V21	28-Lead Molded SOJ Center Power/Ground	

Note:
13. 101E specifications are 100K-compatible with −5.2V supplies.

CYPRESS SEMICONDUCTOR

Ordering Information (continued)

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type/ Pinout	Operating Range
100E	320	4	CY100E484–4DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	Commercial
			CY100E484–4KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY100E484–4YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
		5	CY100E484–5DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	
			CY100E484–5KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY100E484–5YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
	200	7	CY100E484L–7DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Commercial
			CY100E484L–7JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY100E484L–7KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY100E484L–7VC	V21	28-Lead Molded SOJ Center Power/Ground	
		10	CY100E484L–10DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	
			CY100E484L–10JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY100E484L–10KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY100E484L–10VC	V21	28-Lead Molded SOJ Center Power/Ground	

Ordering Information (continued)

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type/ Pinout	Operating Range
10E[14]	320	4	CY10E484–4DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	Commercial
			CY10E484–4KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY10E484–4YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
		5	CY10E484–5DC	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	
			CY10E484–5KC	K80	28-Lead Rectangular Cerpack Center Power/Ground	
			CY10E484–5YC	Y64	28-Pin Ceramic Leaded Chip Carrier Center Power/Ground	
			CY10E484–5DMB	D42	28-Lead (400-Mil) CerDIP Center Power/Ground	Military
			CY10E484–5KMB	K80	28-Lead Rectangular Cerpack Center Power/Ground	
	200	7	CY10E484L–7DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Commercial
			CY10E484L–7JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY10E484L–7KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY10E484L–7VC	V21	28-Lead Molded SOJ Center Power/Ground	
			CY10E484L–7DMB	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Military
			CY10E484L–7KMB	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
		10	CY10E484L–10DC	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Commercial
			CY10E484L–10JC	J64	28-Lead Plastic Leaded Chip Carrier Corner Power/Ground	
			CY10E484L–10KC	K80	28-Lead Rectangular Cerpack Corner Power/Ground	
			CY10E484L–10VC	V21	28-Lead Molded SOJ Center Power/Ground	
			CY10E484L–10DMB	D42	28-Lead (400-Mil) CerDIP Corner Power/Ground	Military
			CY10E484L–10KMB	K80	28-Lead Rectangular Cerpack Corner Power/Ground	

Note:
14. 10E specifications support both 10K and 10KH compatibility.

Document #: 38–A–00005–F

Section Contents

Bus Interface Products

CYPRESS SEMICONDUCTOR

VIC64

VMEbus Interface Controller with D64 Functionality

Features

- **An enhanced VIC068A**
  - **— 64-bit MBLT operation**
  - **— Higher transfer rate**
- **Complete VMEbus interface controller and arbiter**
  - **— 58 internal registers for configuration control and VMEbus and local operations status**
  - **— Drives arbitration, interrupt, address modifier, utility, strobe, address line A[7:1], and data line D[7:0] directly. and provides control signals to drive remaining address and data lines**
  - **— Direct connection to 68K family and mappable to non-68K processors**
- **Complete master/slave capability**
  - **— Supports read, write, write posting, and block transfers**
  - **— Accommodates VMEbus timing requirements with internal digital delay line with half-clock granularity**
  - **— Programmable metastability delay**
  - **— Programmable data acquisition delays**
  - **— Provides programmable timeout timers for local bus and VMEbus transactions**
- **Interleaved block transfers**
  - **— D64 block transfer capability in conformance with VME64 proposal**
  - **— Can act as DMA master on local bus**
  - **— Programmable burst counter, transfer length, and interleave period**
  - **— Allows master and slave transfer to occur during interleave period**
  - **— Also supports local module-based DMA**
- **Arbitration support**
  - **— Supports single-level, priority, and round-robin arbitration**
  - **— Support fair request option as requester**
- **Interrupt support**
  - **— Complete support for the VMEbus interrupts; interrupters and interrupt handler**
  - **— Seven local interrupt lines**
  - **— 8-level interrupt priority encoded**
  - **— Total of 29 interrupts mapped through the VIC64**
- **Miscellaneous features**
  - **— Refresh option for local DRAM**
  - **— Four broadcast location monitors**
  - **— Four module-specific location monitors**
  - **— Eight interprocessor communication registers**
- **See the *VIC64/7C964 Design Notes* for more information**

Functional Description

Cypress's VIC64 VMEbus Interface Controller with D64 functionality is a single chip designed to minimize the cost and board area requirements and to maximize the performance of a VMEbus master/slave module. Data transfers of 70 Mbyte/sec are possible between boards using VIC64.

In addition to D8, D16 and D32 operations, the VIC64 performs D64 data transfer. The VIC64 is designed with an advanced CMOS process using high-performance standard cells. On-chip output buffers are used to provide direct connection to address and data lines.

The VIC64 is based on the industry-standard VIC068A. For most applications, the VIC64 is fully software and plug compatible with the VIC068A. (As VIC64 uses register bits that are unassigned in VIC068A, user code may require simple rework to insure compatibility.)

The local bus interface of the VIC64 emulates Motorola's family of 32-bit 68K processor interfaces. Other processors can easily be adapted to interface to the VIC64 using appropriate logic.

Resetting the VIC64

The VIC64 can be reset by any of three distinct reset conditions:

- Internal Reset. This reset is the most common means of resetting the VIC64. It resets selected register values and logic within the device.
- System Reset. This reset provides a means of resetting the VIC64 through the VMEbus backplane. The VIC64 may also initiate a system reset by writing a configuration register.
- Global Reset. This provides the most complete reset of the VIC64. It resets all of the VIC64's configuration registers.

All three reset options are implemented in a different manner and have different effect on the VIC64 configuration registers.

VIC64 VMEbus System Controller

The VIC64 is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving IACK daisy-chain
- Driving BGiOUT daisy-chain (all four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The system controller functions are enabled by the SCON pin of the VIC64. This pin is sampled during Reset and if LOW, VIC64 performs as system controller. After Reset the pin becomes an output signifying a D64 transfer.

VIC64 VMEbus Master Cycles

The VIC64 is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests a VMEbus transfer. The VIC64 makes a request for the VMEbus. When the VMEbus is granted to the VIC64, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC64 is capable of all four VMEbus request levels. In addition, the following release modes are supported:

- Release On Request (ROR)
- Release When Done (RWD)
- Release On Clear (ROC)
- Release Under RMC Control
- Bus Capture And Hold (BCAP)

Pin Configurations

Pin Grid Array (PGA)
Bottom View

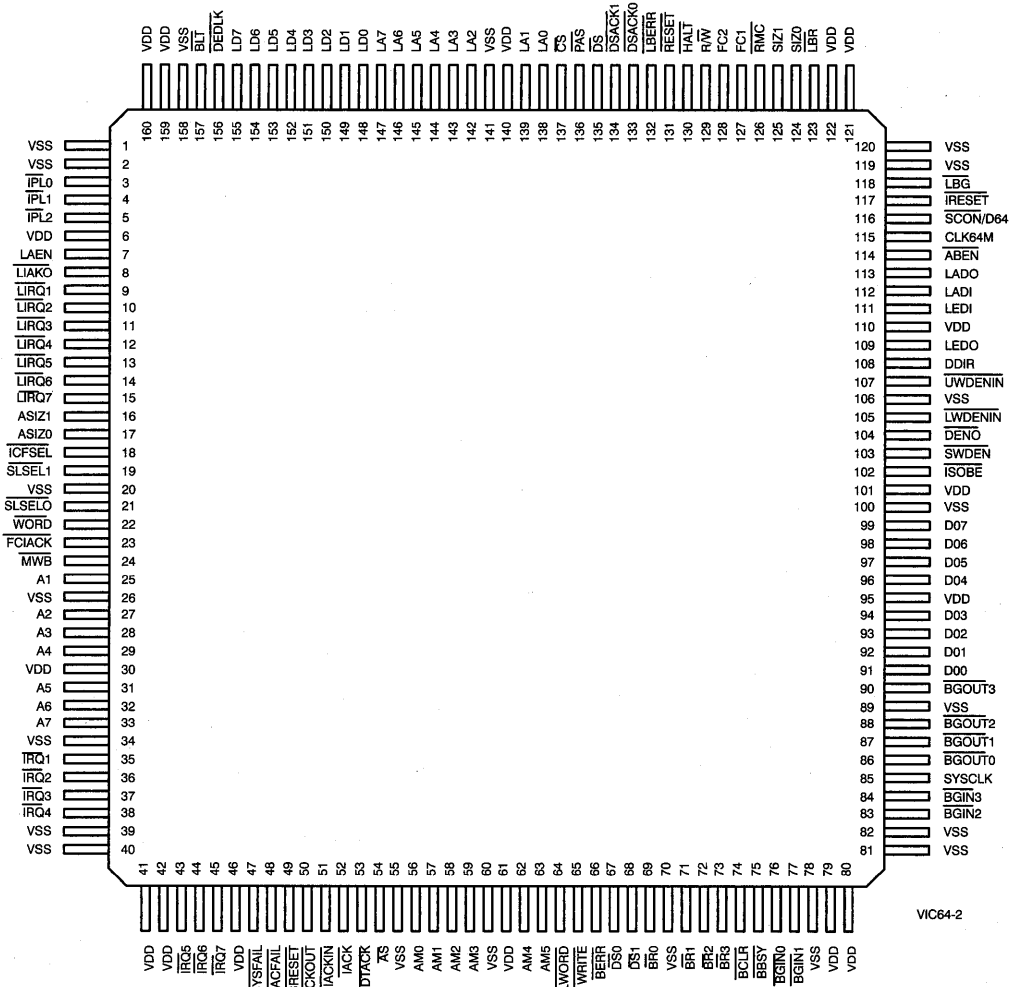
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
VSS	IPL2	LIACKO	LIRQ2	LIRQ5	ASIZ1	ASIZ0	SLSEL1	WORD	FCIACK	A02	A04	VDD	VSS	IRQ4	1
LD6	BLT	IPL1	VDD	LIRQ1	LIRQ4	LIRQ6	ICFSEL	MWB	A01	A03	A05	A07	IRQ3	IRQ7	2
LD2	LD5	DEDLK	IPL0	LAEN	LIRQ3	LIRQ7	VSS	SLSEL0	VSS	A06	IRQ1	IRQ2	IRQ6	ACFAIL	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5	VDD	IACKOUT	4
LA7	LD0	LD4										SYSFAIL	SYSRESET	DTACK	5
LA3	LA5	LA6										IACKIN	IACK	AM0	6
LA2	LA4	VSS										VSS	AS	AM1	7
LA1	LA0	VDD										VSS	AM2	AM3	8
CS	DSACK1	DS										VDD	LWORD	AM4	9
PAS	LBERR	RESET										BERR	WRITE	AM5	10
DSACK0	R/W	FC1										BR2	DS1	DS0	11
HALT	RMC	LBR										BBSY	BR1	BR0	12
FC2	SIZ0	SCON/D64	CLK64M	LADI	VSS	VDD	VSS	VDD	D00	BGOUT1	BGIN2	BGIN0	BR3	VSS	13
SIZ1	IRESET	LADO	LEDI	DDIR	LWDENIN	DENO	D06	D03	D01	VSS	BGOUT0	BGIN3	BGIN1	BCLR	14
LBG	ABEN	VDD	LEDO	UWDENIN	SWDEN	ISOBE	D07	D05	D04	D02	BGOUT3	BGOUT2	SYSCLK	VSS	15

VIC64-1

Pin Configurations (continued)

Quad Flatpack (QFP)

Top View



VIC64-2

Functional Description (continued)

The VIC64 supports A32, A24, and A16, as well as user-defined address spaces.

Master Write-Posting

The VIC64 is capable of performing master write-posting (bus decoupling). In this situation, the VIC64 acknowledges the local resource immediately after the request to the VIC64 is made, thus freeing the local bus. The VIC64 latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC64. Significant control is allowed for:

- Requesting the VMEbus on the assertion of RMC independent of $\overline{\text{MWB}}$ (this prevents any slave access from interrupting local indivisible cycles)
- Stretching the VMEbus $\overline{\text{AS}}$
- Making the above behaviors dependent on the local SIZi signals

Deadlock

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition occurs. The VIC64 signals a deadlock condition by asserting the $\overline{\text{DEDLOCK}}$ signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access

If the VIC64, while it is VMEbus master, has a slave select signaled, a self-access has occurred. The VIC64 asserts $\overline{\text{BERR}}$ and $\overline{\text{LBERR}}$.

VIC64 VMEbus Slave Cycles

The VIC64 is capable of operating as a VMEbus slave controller. The VIC64 contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC64 allows for:

- D64, D32, D16, or D8 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
  - —DMA-type block transfer ($\overline{\text{PAS}}$ and $\overline{\text{DSACKi}}$ held asserted)
  - —Non DMA-type block transfer (toggle $\overline{\text{PAS}}$& and $\overline{\text{DSACKi}}$)
  - —No support for block transfer
- Programmable data acquisition delays
- Programmable $\overline{\text{PAS}}$ and $\overline{\text{DS}}$ timing
- Restricted slave accesses (supervisory accesses only)

When a slave access is required, the VIC64 requests the local bus. When local bus mastership is obtained, the VIC64 reads or writes the data to/from the local resource and asserts the $\overline{\text{DTACK}}$ signal to complete the transfer.

Slave Write-Posting

The VIC64 is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC64 latches the data to be written, and acknowledges the VMEbus (asserts $\overline{\text{DTACK}}$) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC64 encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC64 encodes the appropriate AM codes through the VIC64 FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC64 decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC64 also supports user-defined AM codes; that is, the VIC64 can be made to assert and respond to user-defined AM codes.

VIC64 VMEbus Block Transfers

The VIC64 is capable of both master and slave block transfers. The master VIC64 performs a block transfer in one of two modes:

- The Master Block Transfer with Local DMA (D16, D32, and D64)
- The MOVEM-type Block Transfer (D16 and D32)

In addition to these VMEbus block transfers, the VIC64 is also capable of performing block transfers from one local resource to another in a DMA-like fashion. This is referred to as a module-based DMA transfer.

For D32 block transfers, the VMEbus specification restricts block transfers from crossing 256-byte boundaries without toggling the address strobe, in addition to restricting the maximum length of the transfer to 256 bytes. The VIC64 allows for easy implementation of block transfers that exceed the 256-byte restriction by releasing the VMEbus at the appropriate time and re-arbitrating for the bus at a programmed time later (this in-between time is referred to as the interleave period), while at the same time holding both the local and VMEbus addresses with internal latches. All of this is performed without processor/software intervention until the transfer is complete. For D64 block transfers, the VMEbus specification allows for bursts of up to 2048 bytes.

The VIC64 contains two separate address counters for the VMEbus and local address buses. In addition, a separate address counter is provided for slave block transfers. The VIC64 address counters are 8-bit up-counters that provide for transfers up to 256 bytes. For transfers that exceed the 256 byte limit, the external counters and latches are required.

The VIC64 is capable of performing A32/A16:D64/D32/D16 master block transfers. For D64 transfers, external logic is required for the multiplexing of the data and address signals for the upper 24 address/data lines. Multiplexing for the lower 8 bits is done within the VIC64.

The VIC64 allows slave accesses to occur during the interleave period. Master accesses are also allowed during interleave with programming and external logic. This is referred to as the dual-path option.

MOVEM Master Block Transfer

This mode of block transfer provides the simplest implementation of VMEbus block transfers. For this mode, the local resource simply configures the VIC64 for a MOVEM block transfer and proceeds with the consecutive-address cycles (such as a 68K MOVEM instruction). The local resource continues as the local bus master in this mode.

Master Block Transfers with Local DMA

In this mode, the VIC64 becomes the local bus master and reads or writes the local data in a DMA-like fashion. This provides a much faster interface than the MOVEM block transfer, but with less control and fault tolerance.

D64 block transfers are not supported by MOVEM protocol.

VIC64 Slave Block Transfer

The VIC64 is capable of decoding the address modifier codes to determine that a slave block transfer is desired. In this mode, the VIC64 captures the VMEbus address, and latches it into internal counters. For subsequent cycles, the VIC64 simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both $\overline{PAS}$ and $\overline{DS}$ and expecting $\overline{DSACKi}$ to toggle, or in an accelerated mode in which only $\overline{DS}$ toggles and $\overline{PAS}$ is asserted throughout the cycle.

For D64 slave block transfers, the $\overline{SCON}$/D64 signal is asserted to indicate a D64 transfer is in progress. External logic is required to de-multiplex the data from the VMEbus address bus for the upper 24 address/data lines. The lower 8 bits are done within the VIC64.

Module-Based DMA Transfers

The VIC64 can act as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the source or destination.

VIC64 Interrupt Generation and Handling Facilities

The VIC64 can generate and handle a seven-level prioritized interrupt scheme similar to that used by the Motorola 68K processors. These interrupts include:

- 7 VMEbus interrupts
- 7 local interrupts
- 5 VIC64 error/status interrupts
- 8 interprocessor communication interrupts.

The VIC64 can be configured to act as handler for any of the seven VMEbus interrupts. The VIC64 can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC64 drives the $\overline{IACK}$ daisy chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC64 to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

The VIC64 is also capable of generating local interrupts on certain error or status conditions. These include:

- $\overline{ACFAIL}$ asserted
- $\overline{SYSFAIL}$ asserted
- Failed master write-post ($\overline{BERR}$ asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC64 can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

Interprocessor Communication Facilities

The VIC64 includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general-purpose 8-bit registers
- Four module switches
- Four global switches
- VIC64 version/revision register (read-only)
- VIC64 reset/halt condition (read-only)
- VIC64 interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC64 includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC64/CY7C964 Design Notes
VIC068A/VAC068A User's Guide

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VIC64−BC	B144	145-Pin Plastic Pin Grid Array	Commercial
VIC64−GC	G145	145-Pin Ceramic Pin Grid Array	
VIC64−NC	N160	160-Lead Plastic Quad Flatpack	
VIC64−UC	U162	160-Lead Ceramic Quad Flatpack	
VIC64−GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VIC64−UI	U162	160-Lead Ceramic Quad Flatpack	
VIC64−GM	G145	145-Pin Ceramic Pin Grid Array	Military
VIC64−GMB	G145	145-Pin Ceramic Pin Grid Array	
VIC64−UMB	U162	160-Lead Ceramic Quad Flatpack	
VIC64−UM	U162	160-Lead Ceramic Quad Flatpack	

Document #: 38−00196−A

VIC068A

VMEbus Interface Controller

Features

- **Complete VMEbus interface controller and arbiter**
  - **— 58 internal registers provide configuration control and status of VMEbus and local operations**
  - **— Drives arbitration, interrupt, address modifier utility, strobe, address lines A07through A01 and data lines D07 through D00 directly, and provides signals for control logic to drive remaining address and data lines**
  - **— Direct connection to 68xxx family and mappable to non-68xxx processors**
- **Complete master/slave capability**
  - **— Supports read, write, write posting, and block transfers**
  - **— Accommodates VMEbus timing requirements with internal digital delay line (½-clock granularity)**
  - **— Programmable metastability delay**
  - **— Programmable data acquisition delays**
  - **— Provides timeout timers for local bus and VMEbus transactions.**
- **Interleaved block transfers over VMEbus**
  - **— Acts as DMA master on local bus**
  - **— Programmable burst count, transfer length, and interleaved period interval**
  - **— Supports local module-based DMA.**
- **Arbitration support**
  - **— Supports single-level, priority and round robin arbitration**
  - **— Supports fair request option as requester.**
- **Interrupt support**
  - **— Complete support for the VMEbus interrupts: interrupter and interrupt handler**
  - **— Seven local interrupt lines**
  - **— 8-level interrupt priority encode**
  - **— Total of 29 interrupts mapped through the VIC068A.**
- **Miscellaneous features**
  - **— Refresh option for local DRAM**
  - **— Four broadcast location monitors**
  - **— Four module-specific location monitors**
  - **— Eight interprocessor communications registers**
  - **— PGA or QFP packages**
  - **— Compatible with IEEE Specification 1014, Rev. C**
  - **— Supports RMC operations**
- **See the *VIC068A/VAC068A User's Guide* for more information**

Functional Description

The VMEbus interface controller (VIC068A) is a single chip designed to minimize the cost and board area requirements and to maximize performance of the VMEbus interface of a VMEbus master/slave module. This can be implemented on either a 8-bit, 16-bit, or 32-bit VMEbus system. The VIC068A was designed using high-performance standard cells on an advanced 1-micron CMOS process. The VIC068A performs all VMEbus system controller functions plus many others, which simplify the development of a VMEbus interface. The VIC068A utilizes patented on-chip output buffers. These CMOS high-drive buffers provide direct connection to the address and data lines. In addition to these signals, the VIC068A connects directly to the arbitration, interrupt, address modifier, utility and strobe lines. Signals are provided which control data direction and latch functions needed for a 32-bit implementation.

The VIC068A was developed through the efforts of a consortium of board vendors, under the auspices of the VMEbus International Trade Association (VITA). The VIC068A thus insures compatibility between boards designed by different manufacturers.

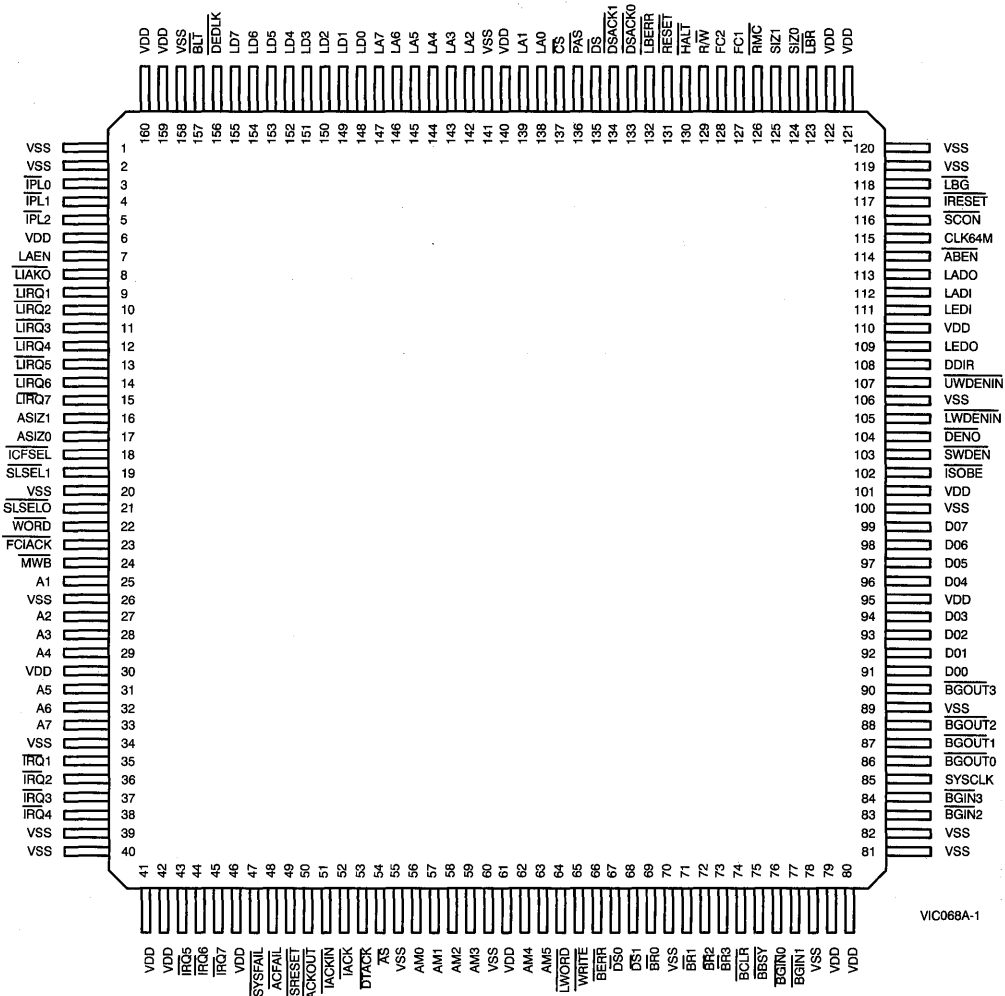
Pin Configurations

Pin Grid Array (PGA)
Bottom View

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
VSS	$\overline{IPL2}$	$\overline{LIACKO}$	$\overline{LIRQ2}$	$\overline{LIRQ5}$	ASIZ1	ASIZ0	$\overline{SLSEL1}$	$\overline{WORD}$	$\overline{FIACK}$	A02	A04	VDD	VSS	$\overline{IRQ4}$	1
LD6	$\overline{BLT}$	$\overline{IPL1}$	VDD	$\overline{LIRQ1}$	$\overline{LIRQ4}$	$\overline{LIRQ6}$	$\overline{ICFSEL}$	$\overline{MWB}$	A01	A03	A05	A07	$\overline{IRQ3}$	$\overline{IRQ7}$	2
LD2	LD5	$\overline{DEDLK}$	$\overline{IPL0}$	LAEN	$\overline{LIRQ3}$	$\overline{LIRQ7}$	VSS	$\overline{SLSEL0}$	VSS	A06	$\overline{IRQ1}$	$\overline{IRQ2}$	$\overline{IRQ6}$	$\overline{ACFAIL}$	3
LD1	LD3	LD7	LOCATOR PIN									$\overline{IRQ5}$	VDD	$\overline{IACKOUT}$	4
LA7	LD0	LD4										$\overline{SYSFAIL}$	$\overline{SYSRESET}$	$\overline{DTACK}$	5
LA3	LA5	LA6										$\overline{IACKIN}$	$\overline{IACK}$	AM0	6
LA2	LA4	VSS										VSS	$\overline{AS}$	AM1	7
LA1	LA0	VDD										VSS	AM2	AM3	8
$\overline{CS}$	$\overline{DSACK1}$	$\overline{DS}$										VDD	$\overline{LWORD}$	AM4	9
$\overline{PAS}$	$\overline{LBERR}$	$\overline{RESET}$										$\overline{BERR}$	$\overline{WRITE}$	AM5	10
$\overline{DSACK0}$	R/$\overline{W}$	FC1										$\overline{BR2}$	$\overline{DS1}$	$\overline{DS0}$	11
$\overline{HALT}$	$\overline{RMC}$	$\overline{LBR}$										$\overline{BBSY}$	$\overline{BR1}$	$\overline{BR0}$	12
FC2	SIZ0	$\overline{SCON}$	CLK64M	LADI	VSS	VDD	VSS	VDD	D00	$\overline{BGOUT1}$	$\overline{BGIN2}$	$\overline{BGIN0}$	$\overline{BR3}$	VSS	13
SIZ1	$\overline{IRESET}$	LADO	$\overline{LEDI}$	DDIR	$\overline{LWDENIN}$	$\overline{DENO}$	D06	D03	D01	VSS	$\overline{BGOUT0}$	$\overline{BGIN3}$	$\overline{BGIN2}$	$\overline{BCLR}$	14
$\overline{LBG}$	$\overline{ABEN}$	VDD	LEDO	$\overline{UWDENIN}$	$\overline{SWDEN}$	$\overline{ISOBE}$	D07	D05	D04	D02	$\overline{BGOUT3}$	$\overline{BGOUT2}$	SYSCLK	VSS	15

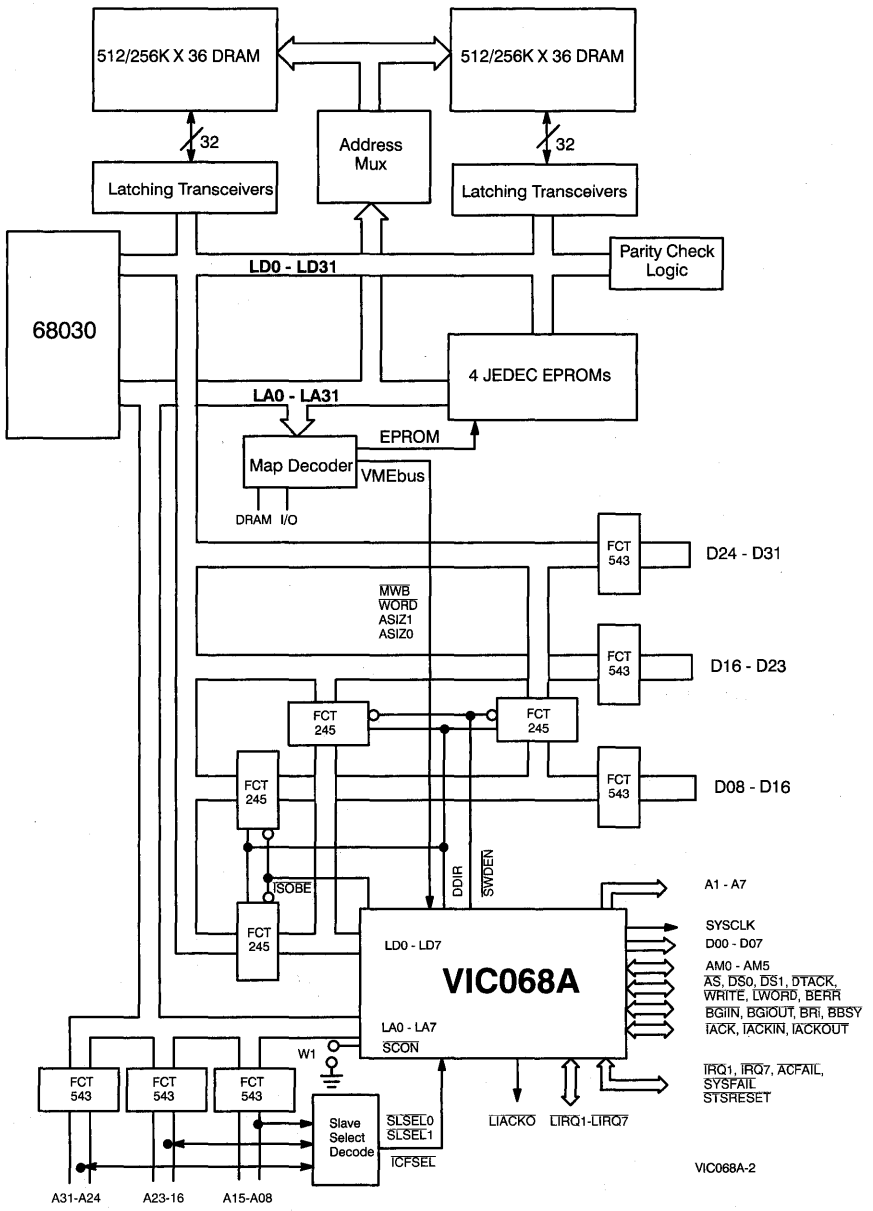
Pin Configurations (continued)

Quad Flatpack (QFP)
Top View



VIC068A-1

VIC068A on 68030 Board



Theory of Operation

The VIC068A is an interface between a local CPU bus and the VMEbus. The local bus interface of the VIC068A emulates Motorola's family of 32-bit CISC processor interfaces. Other processors can easily be adapted to interface to the VIC068A using the appropriate logic.

Resetting the VIC068A

The VIC068A can be reset by any of three distinct reset conditions:

Internal Reset. This reset is the most common means of resetting the VIC068A. It resets select register values and all logic within the device.

System Reset. This reset provides a means of resetting the VIC068A through the VMEbus backplane. The VIC068A may also signal a $\overline{\text{SYSRESET}}$ by writing a configuration register.

Global Reset. This provides a complete reset of the VIC068A. This reset resets all of the VIC068A's configuration registers. This reset should be used with caution since SYSCLK is not driven while a global reset is in progress.

All three reset options are implemented in a different manner and have different effects on the VIC068A configuration registers.

VIC068A VMEbus System Controller

The VIC068A is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving $\overline{\text{IACK}}$ Daisy-Chain
- Driving $\overline{\text{BGiOUT}}$ Daisy-Chain (All four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The System controller functions are enabled by the $\overline{\text{SCON}}$ pin of the VIC068A. When strapped LOW, the VIC068A functions as the VMEbus system controller.

VIC068A VMEbus Master Cycles

The VIC068A is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests that a VMEbus transfer is desired. The VIC068A makes a request for the VMEbus. When the VMEbus is granted to the VIC068A, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC068A is capable of all four VMEbus request levels. The following release modes are supported:

- Release on request (ROR)
- Release when done (RWD)
- Release on clear (ROC)
- Release under $\overline{\text{RMC}}$ control
- Bus capture and hold (BCAP)

The VIC068A supports A32, A24, and A16, as well as user-defined address spaces.

Master Write-Posting

The VIC068A is capable of performing master write-posting (bus decoupling). In this situation, the VIC068A acknowledges the local resource *immediately* after the request to the VIC068A is made, thus freeing the local bus. The VIC068A latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC068A. Significant control is allowed to:

- Requesting the VMEbus on the assertion of $\overline{\text{RMC}}$ independent of $\overline{\text{MWB}}$ (this prevents any slave access from interrupting local indivisable cycles)
- Stretching the VMEbus $\overline{\text{AS}}$
- Making the above behaviors dependent on the local SIZi signals

Deadlock Condition

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition has occurred. The VIC068A will signal a deadlock condition by asserting the $\overline{\text{DEDLK}}$ signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access Condition

If the VIC068A, while it is VMEbus master, has a slave select signaled, a self access is said to have occurred. The VIC068A will issue a $\overline{\text{BERR}}$, which in turn will cause a $\overline{\text{LBERR}}$ to be asserted.

VIC068A VMEbus Slave Cycles

The VIC068A is capable of operating as a VMEbus slave controller. The VIC068A contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC068A allows for:

- D32, D16, or D8 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
  - — DMA-type block transfer ($\overline{\text{PAS}}$ and $\overline{\text{DSACKi}}$ held asserted)
  - — non–DMA-type block transfer (toggle $\overline{\text{PAS}}$ and $\overline{\text{DSACKi}}$)
  - — No support for block transfer
- Programmable data acquisition delays
- Programmable $\overline{\text{PAS}}$ and $\overline{\text{DS}}$ timing
- Restricted slave accesses (supervisory accesses only)

When a slave access is required, the VIC068A will request the local bus. When local bus mastership is obtained, the VIC068A will read or write the data to/from the local resource and assert the $\overline{\text{DTACK}}$ signal to complete the transfer.

Slave Write-Posting

The VIC068A is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC068A latches the data to be written and acknowledge the VMEbus (asserts $\overline{\text{DTACK}}$) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC068A encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC068A encodes the appropriate AM codes through the VIC068A FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC068A decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC068A also supports user-defined AM codes; that is, the

VIC068A can be made to assert and respond to user-defined AM codes.

VIC068A VMEbus Block Transfers

The VIC068A is capable of both master and slave block transfers. The master VIC068A performs a block transfer in one of two modes:

- MOVEM-type Block Transfer
- Master Block Transfer with Local DMA

In addition to these VMEbus block transfers, the VIC068A is also capable of performing block transfers from one local resource to another in a DMA-like fashion. This is referred to as a Module-based DMA transfer.

The VMEbus specification restricts block transfers from crossing 256-byte boundaries without toggling the address strobe, in addition to restricting the maximum length of the transfer to 256 bytes. The VIC068A allows for easy implementation of block transfers that exceed the 256-byte restriction by releasing the VMEbus at the appropriate time and rearbitrating for the bus at a programmed time later (this in-between time is referred to as the interleave period), while at the same time holding both the local and VMEbus addresses with internal latches. All of this is performed without processor/software intervention until the transfer is complete.

The VIC068A contains two seperate address counters for the VMEbus and the local address buses. In addition, a seperate address is counter-provided for slave block transfers. The VIC068A address counters are 8-bit up-counters that provide for transfers up to 256 bytes. For transfers that exceed the 256-byte limit, the Cypress VAC068A or external counters and latches are required.

The VIC068A allows slave accesses to occur during the interleave period. Master accesses are also allowed during interleave with programming and external logic. This is referred to as the "dual path" option.

The VAC068A may be used in conjunction with the VIC068A to provide much of the external logic required for extended block transfer modes, such as the 256-byte boundary crossing and dual path. the VAC068A extends the 8-bit counters in the VIC068A to support full 32-bit incrementing addresses on both the local bus and VMEbus. The VAC068A also contains the latches required for extended address block transfers as well as those required for supporting the dual path feature. The VAC068A is not required to support block transfers, it simply enhances them.

MOVEM Master Block Transfer

This mode of block transfer provides the simplest implementation of VMEbus block transfers. For this mode, the local resource simply configures the VIC068A for a MOVEM block transfer and proceeds with the consecutive-address cycles (such as a 680X0 MOVEM instruction). The local resource continues as the local bus master in this mode.

Master Block Transfers with Local DMA

In this mode, the VIC068A becomes the local bus master and reads or writes the local data in a DMA-like fashion. This provides a much faster interface than the MOVEM block transfer, but with less control and fault tolerence.

VIC068A Slave Block Transfer

The process of receiving a block transfer is referred to as a slave block transfer. The VIC068A is capable of decoding the address modifier codes to determine that a slave block transfer is desired. In this mode, the VIC068A captures the VMEbus address, and latches them into internal counters. For subsequent cycles, the VIC068A simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both $\overline{PAS}$ and $\overline{DS}$ and expecting $\overline{DSACKi}$ to toggle, or in an accelerated mode in which only $\overline{DS}$ toggles and $\overline{PAS}$ is asserted throughout the cycle.

Module-Based DMA Transfers

The VIC068A is capable of acting as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the second source or destination.

VIC068A Interrupt Generation and Handling Facilities

The VIC068A is capable of generating and handling a seven-level prioritized interrupt scheme similar to that used by the Motorola CISC processors. These interrupts include the seven VMEbus interrupts, seven local interrupts, five VIC068A error/status interrupts, and eight interprocessor communication interrupts.

The VIC068A can be configured to act as handler for any of the seven VMEbus interrupts. The VIC068A can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC068 will drive the IACK daisy-chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC068A to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

The VIC068A is also capable of generating local interrupts on certain error or status conditions. These include:

- $\overline{ACFAIL}$ asserted
- $\overline{SYSFAIL}$ asserted
- Failed master write-post ($\overline{BERR}$ asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC068A can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

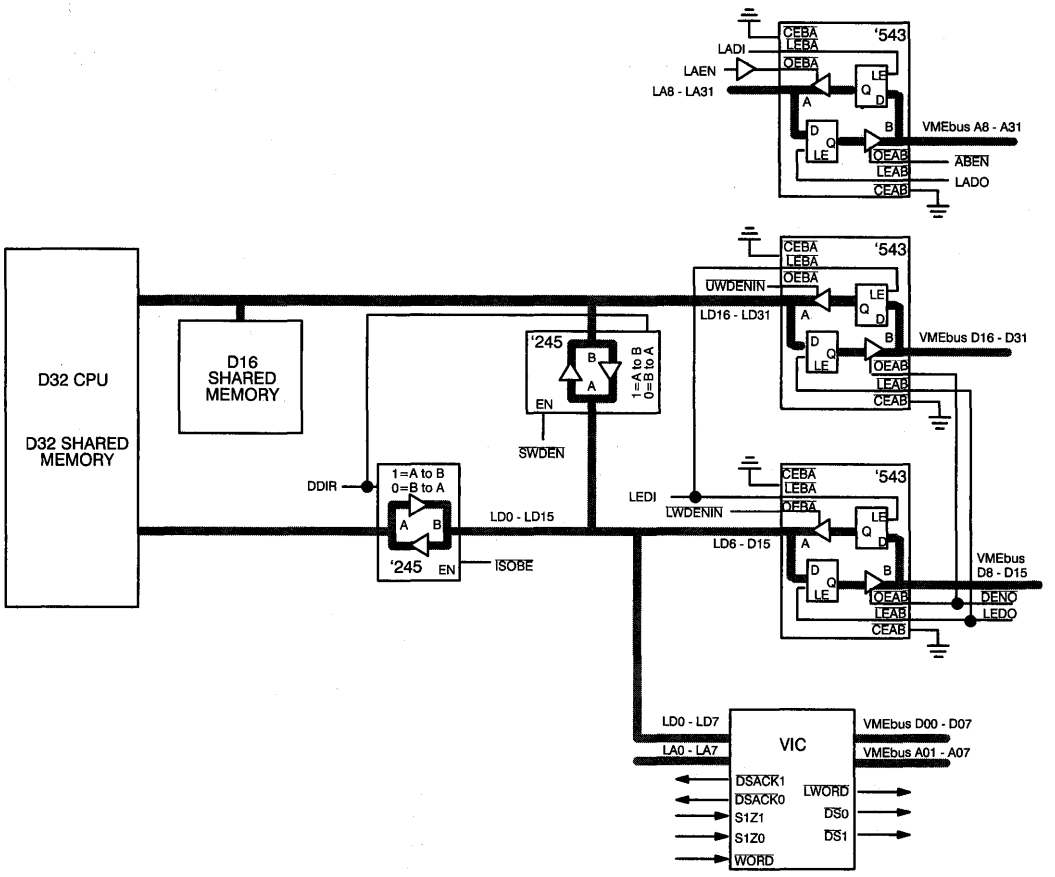
Interprocessor Communication Facilities

The VIC068A includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general purpose 8-bit registers
- Four module switches
- Four global switches
- VIC068A version/revision register (read-only)
- VIC068A Reset/Halt condition (read-only)
- VIC068A interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC068A includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

Buffer Control Signal for Shared Memory Implementation[1]



Note:

1. This configuration can support Slave Block Transfers and Master and Slave Write-Post Operation. This buffer configuration cannot support block transfers with DMA.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC068A/VAC068A User's Guide
VIC64/CY7C964 Design Notes

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VIC068A−BC	B144	145-Pin Plastic Pin Grid Array	Commercial
VIC068A−GC	G145	145-Pin Ceramic Pin Grid Array	
VIC068A−NC	N160	160-Lead Plastic Quad Flatpack	
VIC068A−UC	U162	160-Lead Ceramic Quad Flatpack	
VIC068A−GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VIC068A−UI	U162	160-Lead Ceramic Quad Flatpack	
VIC068A−GM	G145	145-Pin Ceramic Pin Grid Array	Military
VIC068A−GMB	G145	145-Pin Ceramic Pin Grid Array	
VIC068A−UM	U162	160-Lead Ceramic Quad Flatpack	
VIC068A−UMB	U162	160-Lead Ceramic Quad Flatpack	

Document #: 38−00167−B

CYPRESS SEMICONDUCTOR

VAC068A

VMEbus Address Controller

Features

- **Optional companion part to VIC068A**
- **Implements master/slave VMEbus interface in conjunction with the VIC068A**
- **Complete VMEbus and I/O DMA capability for a 32-bit CPU**
- **Complete local and VMEbus memory map decoding**
  - **— Separate segments on local side available for DRAM, VME subsystem bus (VSB), shared resources, VMEbus, local I/O, and EPROM**
  - **— Separate segments for the VMEbus address decode for slave select 0, slave select 1, and interprocessor communication facilities**
  - **— 64-Kbyte resolution for both local and VMEbus memory maps**
- **Supports block transfers over 256 byte boundaries**
  - **— Address counters for both VMEbus A(31–8) and local LA(31–8)**
  - **— Supports dual-path mode**
  - **— Supports implementation of VSB interface with DMA capability**
- **Dual UART channels on board**
  - **— Double-buffered on transmit, quint-buffered on receive**
  - **— Baud rate programmable**
- **Miscellaneous features**
  - **— Pin grid array or quad flatpack package**
  - **— Supports unaligned transfers**
  - **— Programmable DSACKi for local I/O**
  - **— Programmable timer and interrupt controller**
  - **— Programmable I/O (PIO)**
- **See the *VIC068A/VAC068A User's Guide* for more information**

Functional Description

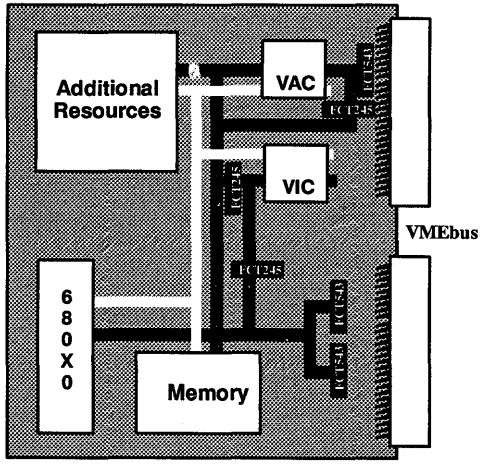
The VMEbus address controller (VAC068A) is a programmable memory map address controller. In conjunction with the VIC068A (VMEbus interface controller), the VAC068A maximizes the VMEbus interface performance of a master/slave module.

The VAC068A contains programmable registers to allow the user to easily define memory maps for both the local and VMEbus address regions. The VAC068A also contains the address counters and handshaking signals to allow easy implementation of block-level transfers over 256-byte boundaries. Additional features include dual internal UART channels, redirection control on the local bus to VSB (VME subsystem bus) or shared resource area, data swapping for unaligned transfers, programmable DSACKi, programmable timer and interrupt controller.

The VAC068A connects directly to the local bus and the VIC068A. VMEbus address lines A8 through A31 are driven directly. The VAC068A output drivers feature patented high-drive outputs and TTL-compatible inputs. The VAC068A was designed using high-performance standard cells on an advanced CMOS process.

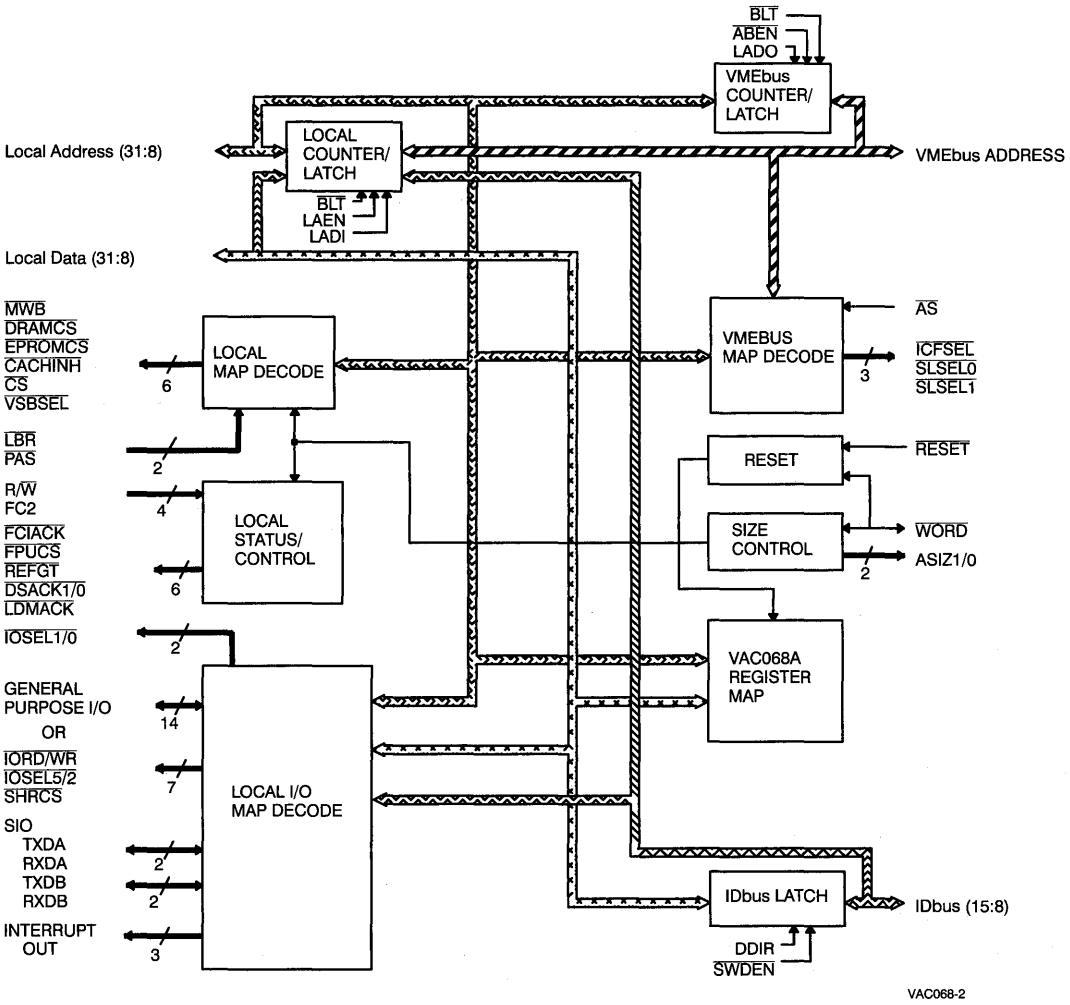
The VAC068A is available in pin grid array (with 122 active signals, 22 power and ground pins, and 1 locator pin) and quad flatpack.

Sample Board Design



VAC068-1

Block Diagram



Pin Configurations

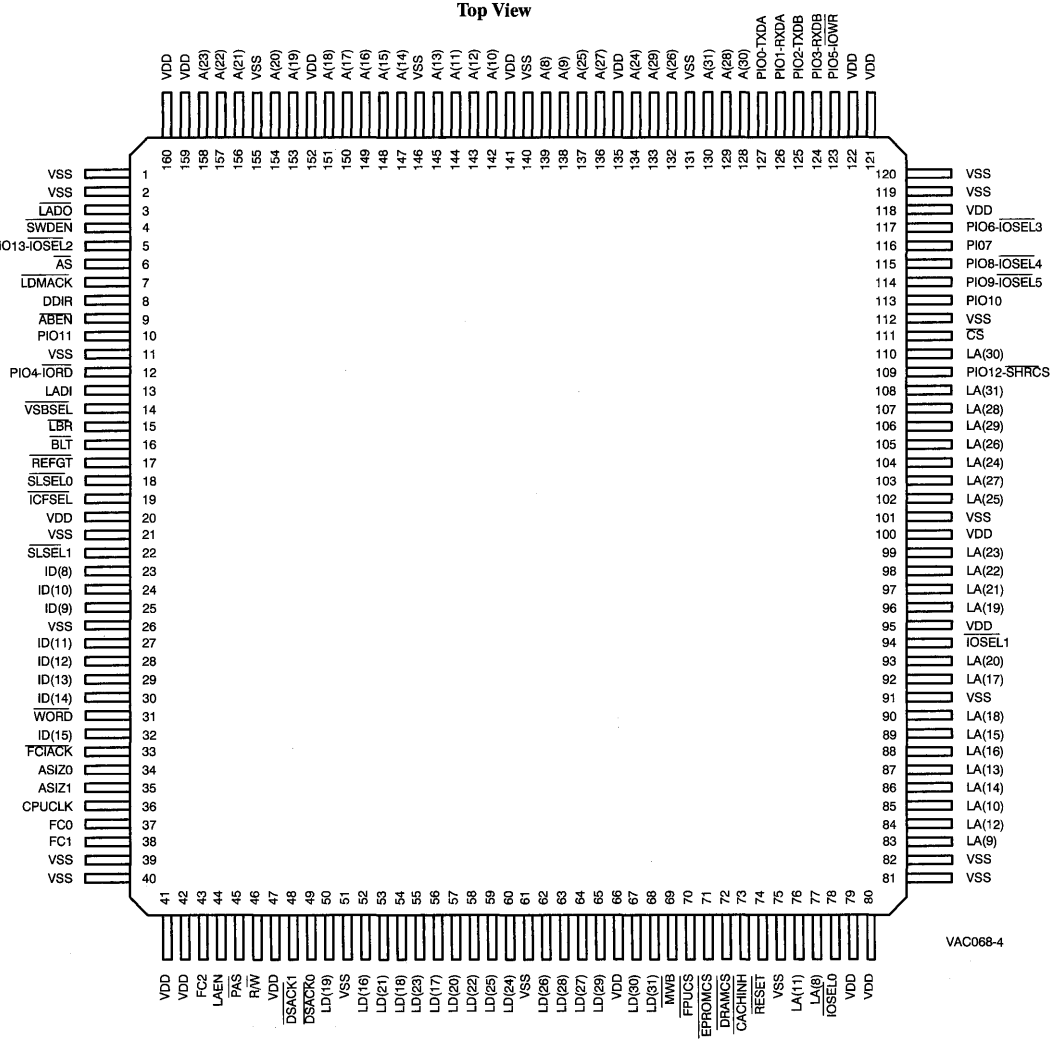
Pin Grid Array (PGA)
Bottom View

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
A23	PIO13/ IOSEL2	DDIR	PIO11	LADI	BLT	REFGT*	ICFSEL	SLSELT	ID8	ID11	ID13	ID14	ASIZ0	FC1	1
A20	A22	SWDEN	VAS	ABEN	PIO4/ IORD	VSBSEL	SLSEL0	IDI0	ID9	ID12	WORD	FCIACK	FC0	PAS	2
A17	A19	A21	LADO	LDMACK	VSS	LBR	VDD	VSS	VSS	ID15	ASIZ1	CPUCLK	LAEN	DSACKT	3
A16	A18	VSS	LOCATOR PIN									FC2	R/W	LD19	4
A14	A15	VDD										VDD	DSACK0	LD21	5
A12	A13	VSS										VSS	LD16	LD17	6
A10	A11	VDD										LD23	LD18	LD20	7
A08	A09	VSS										LD24	LD22	LD25	8
A25	A24	VDD										VSS	LD27	LD26	9
A27	A26	VSS										VDD	LD29	LD28	10
A29	A28	PIO0/ TXDA										DRAMCS	LD31	LD30	11
A31	PIO1/ RXDA	PIO5/ IOWR										VSS	EPROMCS	MWB	12
A30	PIO3/ RXDB	PIO7	PIO8/ IOSEL4	VSS	LA29	VSS	VDD	VDD	VSS	LA13	LA9	LA11	CACHINH	FPUCS	13
P102/ TXDB	PIO6/ IOSEL3	PIO10	CS	LA31	LA26	LA24	LA22	IOSELT	LA17	LA15	LA14	LA12	LA8	RESET	14
VDD	PIO9/ IOSEL5	LA30	PIO12/ SHRCS	LA28	LA27	LA25	LA23	LA21	LA19	LA20	LA18	LA16	LA10	IOSEL0	15

VAC068-3

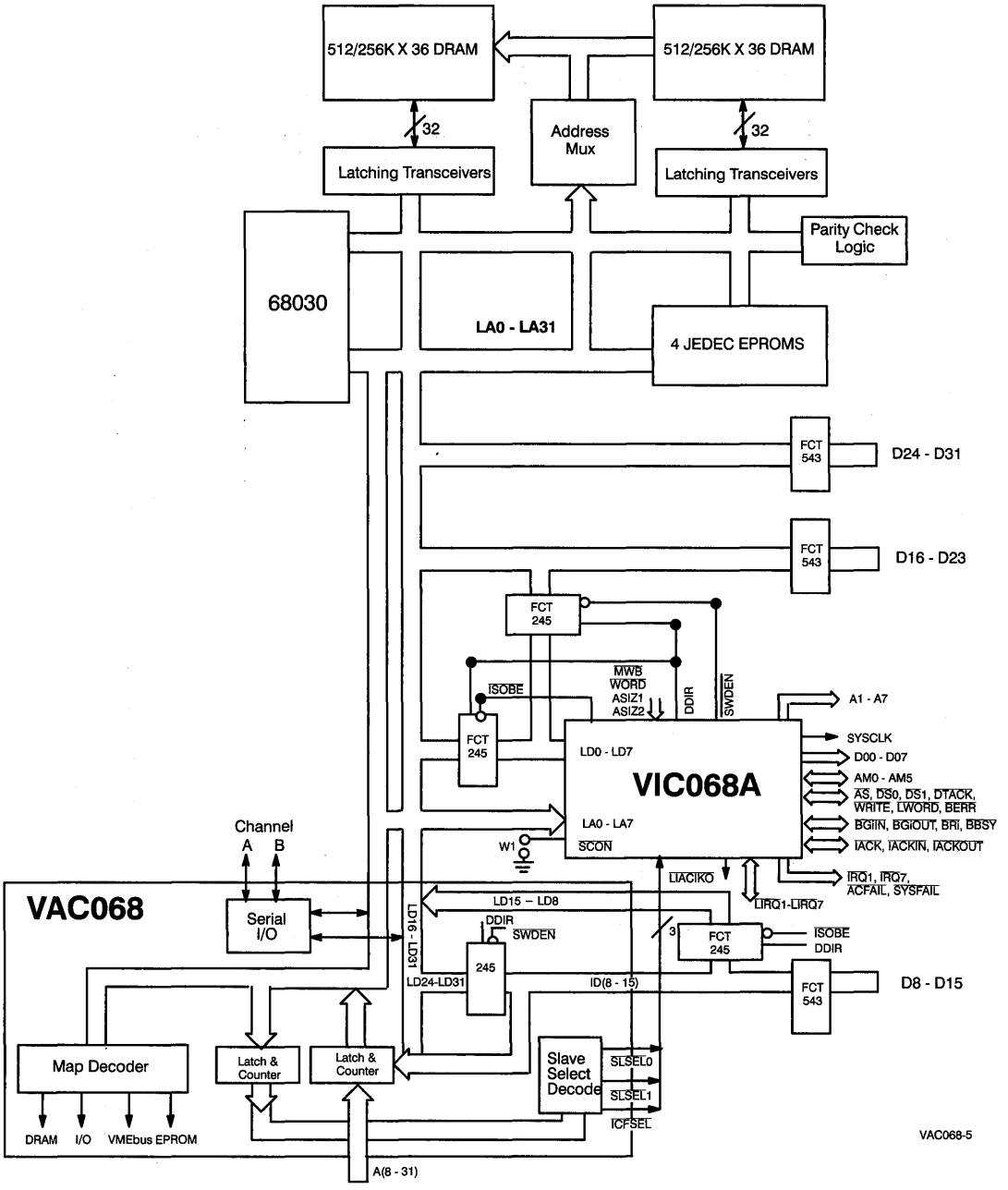
Pin Configurations (continued)

Quad Flatpack (QFP)
Top View



VAC068-4

VIC068A/VAC068A on 68030 Board



Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC068A/VAC068A User's Guide
VIC64/CY7C964 Design Notes

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VAC068A−BC	B144	145-Pin Plastic Pin Grid Array	Commercial
VAC068A−GC	G145	145-Pin Ceramic Pin Grid Array	
VAC068A−NC	N160	160-Lead Plastic Quad Flatpack	
VAC068A−UC	U162	160-Lead Ceramic Quad Flatpack	
VAC068A−GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VAC068A−UI	U162	160-Lead Ceramic Quad Flatpack	
VAC068A−GM	G145	145-Pin Ceramic Pin Grid Array	Military
VAC068A−GMB	G145	145-Pin Ceramic Pin Grid Array	
VAC068A−UM	U162	160-Lead Ceramic Quad Flatpack	
VAC068A−UMB	U162	160-Lead Ceramic Quad Flatpack	

Document #: 38−00169−B

CYPRESS SEMICONDUCTOR

CY7C964

Bus Interface Logic Circuit

Features

- **Comparators, counters, latches, and drivers minimize logic requirements for a variety of multiplexed and non-multiplexed buses**
- **Directly drives VMEbus address and data signals**
- **8-/16-bit comparator for slave address decoding**
- **Flexible interface optimized for VMEbus applications**
- **Companion device to Cypress VMEbus family of components**
- **Replaces multiple SSI/MSI components**
- **Cascadeable**
- **64-pin QFP package**
- **See the *VIC64/7C964 Design Notes* for more information**

Functional Description

The CY7C964 integrates several space-consuming functions into one small package, freeing board space for the implementation of added-value board features. It contains counters, comparators, latches, and drivers configured to be of value to implementors of any backplane interface with address and data buses, particularly VMEbus interfaces. The on-chip drivers are suitable for driving the VMEbus directly. The CY7C964 is ideal in applications where high-performance and real estate are primary concerns.

Although having many applications, the Bus Interface Logic Circuit is an ideal companion part to Cypress's VMEbus family of components, the VIC068A and the VIC64. It is intended to drive the address and data buses (only the three upper bytes, as the VIC068A/VIC64 drives the lower byte of data and address buses), so three of these small devices are needed per controller. The VIC068A/VIC64 provides the control and timing signals to control the Bus Interface Logic Circuit as it acts as a bridge between the VMEbus and the Local bus.

Application with VMEbus Architecture

Use with Cypress VMEbus Controllers

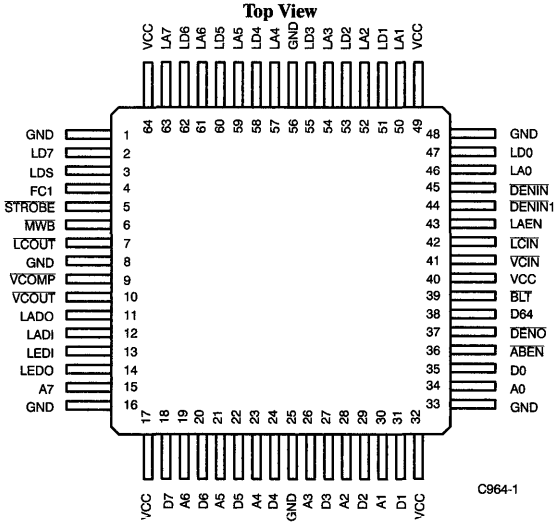
The CY7C964 Bus Interface Logic Circuit is a seamless interface between the VIC068A/VIC64 and the VMEbus signals. The device functions equally well in the established 32-bit VMEbus arena and the emerging 64-bit VMEbus standard. The device contains three 8-bit counters to fulfill the functions of Block counters, and DMA counters as implied by the D64 portion of the VMEbus specification. It also contains the necessary multiplexing logic to allow the 64-bit-wide VMEbus path to be funnelled to and from the 32-bit local bus. Control circuitry is included to manage the switching of the 32-bit address bus during normal (32-bit) operations, and during MBLT (64-bit) operations. All the controls for these operations are directly provided from the VIC068A/VIC64. The on-chip drivers are capable of driving the VMEbus directly (48 mA).

Use in Other VMEbus Controller Implementations

The CY7C964 circuitry is designed to be of use to designers of VMEbus circuitry, including VSB (VME subsystem bus) and designs not requiring the features of the Cypress VIC068A and VIC64. The logic diagram includes general-purpose blocks of comparators, counters, and latches that can be controlled using the flexible control interface to allow many different options to be implemented. Although the device is packaged in a small 64-pin package, the use of multiplexed input and output pins provides access to the many internal functions, thus saving external circuitry.

Pin Configuration

PQFP/CQFP
Top View



C964-1

Application with Other Bus Architectures

The CY7C964 is optimized for applications requiring wide buffers and high-performance multiplexing operations. The architecture can be configured to provide functions such as 16-bit bidirectional three-state latch and 16-bit comparator with mask register, or more complex functions such as 16-to-8 pipelined bidirectional multiplexer with address counter/comparator circuitry. The device can be cascaded to generate counters and comparators suitable for multiple byte address/data buses. The on-chip 48 mA drivers can be directly connected to many standard backplane buses.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C964–NC	N65	64-Lead Plastic Quad Flatpack	Commercial
CY7C964–UC	U64	64-Lead Ceramic Quad Flatpack	
CY7C964–UI	U64	64-Lead Ceramic Quad Flatpack	Industrial
CY7C964–UM	U64	64-Lead Ceramic Quad Flatpack	Military
CY7C964–UMB	U64	64-Lead Ceramic Quad Flatpack	

Related Documents

VIC64/CY7C964 Design Notes
VIC068A/VAC068A User's Guide

Document #: 38–00197–A

Section Contents

CYPRESS SEMICONDUCTOR

Military Overview

Features

Success in any endeavor requires a high level of dedication to the task. Cypress Semiconductor has demonstrated its dedication through its corporate commitment to support the military marketplace. This commitment starts with product design. All products are designed using our state-of-the-art CMOS and BiCMOS processes, and they must meet the full – 55 to +125 degrees Celsius operational criteria for military use. The commitment continues with the 1986 DESC certification of our automated U.S. facility in San Jose, California. The commitment shows in our dedication to meet and exceed the stringent quality and reliability requirements of MIL-STD-883D and MIL-M-38510J. It shows in Cypress's participation in each of the military processing programs: MIL-STD-883D compliant, SMD (Standardized Military Drawing), and JAN. Finally, our commitment shows in our leadership position in special packages for military use.

Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out in our industry-leading 0.65-micron CMOS and BiCMOS processes. Cypress is able to offer a family of products that are industry leaders in density, low operating and standby current, and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCCs and flatpacks so often used in military programs.

DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Class B CMOS Microcircuits. This certification not only allows Cypress to qualify product for JAN use, but also assures our customers that our San Jose Facility has the necessary documentation and procedures to manufacture product to the most stringent of quality and reliability requirements. Our wafer fabrication facilities are Class 10 (San Jose) and Class 1 (Round Rock, TX and Bloomington, MN) manufacturing environments and our assembly facility is also a clean room.

Data Sheet Documentation

Every Cypress final data sheet is a corporate document with a revision history. The document number and revision appears on each final data sheet. Cypress maintains a listing of all data sheet documentation and a copy is available to customers upon request. This gives a customer the ability to verify the current status of any data sheet and it also gives that customer the ability to obtain updated specifications as required.

Every final data sheet also contains detailed Group A subgroup testing information. All of the specified parameters that are tested at Group A are listed in a table at the end of each final data sheet, with a notation as to which specific Group A test subgroups apply.

Assembly Traceability Code™

Cypress Semiconductor places an assembly traceability code on every military package that is large enough to contain the code. The ATC automatically provides traceability for that product to the individual wafer lot. This unique code provides Cypress with the ability to determine which operators and equipment were used in the manufacture of that product from start to finish.

Quality and Reliability

MIL-STD-883D and MIL-M-38510J spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability, and Process Flows for further details.

Military Product Offerings

Cypress offers three levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883, Revision D.

Second, selected products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully MIL-STD-883D compliant, but are also screened to the electrical requirements of the applicable military drawing.

Third, selected products are available as JAN devices. These products are processed in full accordance with MIL-M-38510J and they are screened to the electrical requirements of the applicable JAN slash sheet.

Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader an appreciation of the variety of packages offered. Included are cerDIPs, windowed CerDIPs, leadless chip carriers (LCCs), windowed leadless chip carriers, cerpaks, windowed cerpaks, quad cerpaks, windowed quad cerpaks, bottom-brazed flatpacks, and pin grid arrays.

Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our documentation and traceability, our quality and reliability programs, our support of all levels of military processing, and by our leadership in special packaging.

Static RAMs

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	883 Availability
64	16x4—Inverting	16	CY7C189		t_{AA} = 25	70@25	Now
64	16x4—Non-Inverting	16	CY7C190	5962-89694	t_{AA} = 25	70@25	Now
64	16x4—Inverting	16	CY27S03/A		t_{AA} = 25,35	100@35	Now
64	16x4—Non-Inverting	16	CY27S07/A		t_{AA} = 25,35	100@25	Now
64	16x4—Inverting/Low Power	16	CY27LS03		t_{AA} = 65	38@65	Now
1K	256x4—10K/10KH ECL	24	CY10E422L		t_{AA} = 5,7	150@5/7	Now
1K	256x4	22	CY7C122	5962-88594	t_{AA} = 25,35	90@25	Now
1K	256x4	24S	CY7C123	5962-90696	t_{AA} = 10,12,15	150@15	Now
1K	256x4	22	CY9122/91L22	5962-88594	t_{AA} = 35,45	90@45	Now
1K	256x4	22	CY93422A/93L422A	5962-88594	t_{AA} = 45,55,60,75	90@55	Now
4K	4Kx1—CS Power-Down	18	CY7C147	M38510/289	t_{AA} = 35,45	110/10@35	Now
4K	4Kx1—CS Power-Down	18	CY2147	M38510/289	t_{AA} = 45,55	140/25@45	Now
4K	4Kx1—CS Power-Down	18	CY7C147	5962-88587	t_{AA} = 35,45	110/10@35	Now
4K	4Kx1—CS Power-Down	18	CY2147	5962-88587	t_{AA} = 45,55	140/25@45	Now
4K	1Kx4—10K/10KH ECL	24	CY10E474L	5962-91518	t_{AA} = 5,7	190@5/7	Now
4K	1Kx4—CS Power-Down	18	CY7C148	M38510/289	t_{AA} = 35,45	110/10@35	Now
4K	1Kx4—CS Power-Down	18	CY2148	M38510/289	t_{AA} = 45,55	140/25@45	Now
4K	1Kx4	18	CY7C149		t_{AA} = 35,45	110@35	Now
4K	1Kx4	18	CY2149		t_{AA} = 45,55	140@45	Now
4K	1Kx4—Separate I/O	24S	CY7C150	5962-88588	t_{AA} = 12,15,25,35	100@15	Now
8K	1Kx8—Dual Port	48	CY7C130/31	5962-86875	t_{AA} = 35,45,55	120/40@45	Now
8K	1Kx8—Dual-Port Slave	48	CY7C140/41	5962-86875	t_{AA} = 35,45,55	120/40@45	Now
16K	4Kx4—CS ECL	28	CY10E484L		t_{AA} = 7,10	200@10	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	5962-89690	t_{AA} = 20,25	125@20	Now
16K	2Kx8—CS Power-Down	24	CY6116A/7A	5962-89690	t_{AA} = 20,25	125@20	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	84036	t_{AA} = 35,45,55	125/40@25	Now
16K	16Kx1—CS Power-Down	20	CY7C167A	84132	t_{AA} = 20,25,35,45	70/20@25	Now
16K	4Kx4—CS Power-Down	20	CY7C168A	5962-86705	t_{AA} = 20,25,35,45	100/20@25	Now
16K	4Kx4	20	CY7C169A		t_{AA} = 20,25,35,40	100/20@35	Now
16K	4Kx4—Output Enable	22S	CY7C170A		t_{AA} = 20,25,35,45	120@25	Now
16K	4Kx4—Separate I/O	24S	CY7C171A		t_{AA} = 20,25,35,45	100/20@25	Now
16K	4Kx4—Separate I/O, Power-Down	24S	CY7C172A	5962-89790	t_{AA} = 20,25,35,45	90@20	Now
16K	2Kx8—Dual-Port	48	CY7C132/36	5962-90620	t_{AA} = 35,45,55	170/65@35	Now
16K	2Kx8—Dual-Port Slave	48	CY7C142/46	5962-90620	t_{AA} = 35,45,55	120/40@45	Now
32K	4Kx8—Dual-Port	48	CY7B134	5962-93001	t_{AA} = 25,35	280@25	Now
32K	4Kx8—Dual-Port	52	CY7B135	5962-93001	t_{AA} = 25,35	280@25	Now
32K	4Kx8—Dual-Port Semaphores	52	CY7B1342		t_{AA} = 25,35	280@25	Now
32K	4Kx8—Dual-Port Semaphores Int, Busy	68	CY7B138		t_{AA} = 25,35	280@25	Now
32K	4Kx9—Dual-Port Semaphores Int, Busy	68	CY7B139		t_{AA} = 25,35	280@25	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-38294	t_{AA} = 20,25,35,45	125@20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-89691	t_{AA} = 20,25	125@20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-85525	t_{AA} = 35,45	100/20/1@45	Now
64K	8Kx8—CS Power-Down	28S	CY7B185	5962-91594	t_{AA} = 10,12,15	145/50@15	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-38294	t_{AA} = 20,25,35,45	125@20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-89691	t_{AA} = 20,25	125@20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-85525	t_{AA} = 35,45,55	100/20/1@45	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-89692	t_{AA} = 20,25	90@20	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-86859	t_{AA} = 35	70/20/1@35	Now
64K	16Kx4—CS Power-Down	22S	CY7B164	5962-91593	t_{AA} = 10,12,15	135/50@15	Now
64K	16Kx4—CS Power-Down	24S	CY7C166A	5962-89892	t_{AA} = 20,25	90@20	Now
64K	16Kx4—Output Enable	24S	CY7C166A	5962-86859	t_{AA} = 35	70/20/1@35	Now
64K	16Kx4—Output Enable	24S	CY7B166	5962-91593	t_{AA} = 10,12,15	135/50@15	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7C161A	5962-90594	t_{AA} = 20,25,35	70/20/1@35	Now
64K	16Kx4—Separate I/O	28S	CY7C162A	5962-89712	t_{AA} = 20,25,35	70/20/1@35	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7B161		t_{AA} = 12,15	135/50@15	Now
64K	16Kx4—Separate I/O	28S	CY7B162	5962-92172	t_{AA} = 12,15	135/50@15	Now
64K	64Kx1—CS Power-Down	22S	CY7C187A	5962-86015	t_{AA} = 20,25,35	70/20/1@35	Now
64K	8Kx8—Dual-Port Semaphores Int, Busy	68	CY7B144		t_{AA} = 25,35	280@25	Now
64K	8Kx9—Dual-Port Semaphores Int, Busy	68	CY7B145		t_{AA} = 25,35	280@25	Now

Static RAMs (continued)

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	883 Availability
64K	4Kx18—Cache Tag	68	CY7B180		t_{AA} = 15.20	250 @ 15	Now
64K	4Kx18—Cache Tag	68	CY7B181		t_{AA} = 15,20	250 @ 15	Now
256K	32Kx8—CS Power-Down	28	CY7C198	5962-88662	t_{AA} = 20,25,35,45,55	180/40 @ 20	Now
256K	32Kx8—CS Power-Down	28S	CY7C199	5962-88662	t_{AA} = 20,25,35,45,55	180/40 @ 20	Now
256K	64Kx4—CS Power-Down	24S	CY7C194	5962-88681	t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	64Kx4—CS PD + OE/CE1	28S	CY7C195		t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	64Kx4—CS, OE	28S	CY7C195L	5962-89524	t_{AA} = 25,35,45	120/25 @ 25	Now
256K	64Kx4—CS PD + OE/CE2	28S	CY7C196		t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	64Kx4—Separate I/O, T-write	28S	CY7C191	5962-90664	t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	64Kx4—Separate I/O	28S	CY7C192	5962-89935	t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	256Kx1—CS Power-Down	24S	CY7C197	5962-88725	t_{AA} = 20,25,35,45	150/40 @ 20	Now
256K	32Kx8—CS Power-Down	28	CY7B198		t_{AA} = 15,20	170/60 @ 15	Now
256K	32Kx8—CS Power-Down	28S	CY7B199		t_{AA} = 12,15,20	170/40 @ 12	Now
256K	64Kx4—Separate I/O	28S	CY7B192		t_{AA} = 12,15,20	170/40 @ 12	Now
256K	64Kx4—CS Power-Down	24S	CY7B194		t_{AA} = 12,15,20	170/40 @ 12	Now
256K	64Kx4—CS PD, OE	28S	CY7B195		t_{AA} = 12,15,20	170/40 @ 12	Now
256K	64Kx4—CS PD, OE, 2CE	28S	CY7B196		t_{AA} = 12,15,20	170/40 @ 12	Now
256K	32Kx9—Synchronous Cache	44	CY7B174		t_{AA} = 18,21	250 @ 18	Now
1M	128Kx8—CS Power-Down	32	CY7C109A	5962-89598	t_{AA} = 25,35,45	140/30 @ 25	1Q94
1M	128Kx8—CS Power-Down	32S	CY7C1009		t_{AA} = 15,20,25	180/40 @ 15	1Q94
1M	256Kx4—CS Power-Down/OE	28S	CY7C1006	5962-91612	t_{AA} = 15,20,25	165/40 @ 15	1Q94
1M	256Kx4—Separate I/O, T-Write	32S	CY7C1001		t_{AA} = 15,20,25	165/40 @ 15	1Q94
1M	256Kx4—Separate I/O	32S	CY7C1002		t_{AA} = 15,20,25	165/40 @ 15	1Q94
1M	1Mx1—CS Power-Down	28S	CY7C1007	5962-92316	t_{AA} = 15,20,25	145/40 @ 15	1Q94

PROMs

Size	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	883 Availability
4K	512x8—Registered	24S	CY7C225	5962-88518(O)	$t_{SA/CO}$ = 30/15, 35/20, 40/25	120 @ 30/15	Now
4K	512x8—Registered	24S	CY7C225A	5962-88518(O)	$t_{SA/CO}$ = 25/12, 30/15, 35/20	120	Now
8K	1Kx8—Registered	24S	CY7C235	5962-88636(O)	$t_{SA/CO}$ = 30/15, 40/20	120 @ 30/15	Now
8K	1Kx8—Registered	24S	CY7C235A	5962-88636(O)	$t_{SA/CO}$ = 25/12, 30/15, 40/20	120	Now
8K	1Kx8	24S	CY7C281	5962-87651(O)	t_{AA} = 45	120 @ 45	Now
8K	1Kx8	24S	CY7C281A	5962-87651(O)	t_{AA} = 30,45	120	Now
8K	1Kx8	24	CY7C282	5962-87651(O)	t_{AA} = 45	120 @ 45	Now
8K	1Kx8	24	CY7C282A	5962-87651(O)	t_{AA} = 30,45	120	Now
16K	2Kx8—Registered	24S	CY7C245	5962-87529(W)	$t_{SA/CO}$ = 35/15, 45/25	120 @ 35/15	Now
16K	2Kx8—Registered	24S	CY7C245A	5962-89815(W)	$t_{SA/CO}$ = 18/12, 25/12, 35/15	120 @ 18/12	Now
16K	2Kx8—Registered	24S	CY7C245A	5962-88735(O)	$t_{SA/CO}$ = 18/12, 25/12, 35/15	120 @ 18/12	Now
16K	2Kx8	24S	CY7C291	5962-87650(W)	t_{AA} = 25, 35, 50	120 @ 35	Now
16K	2Kx8	24S	CY7C291A	5962-88734(O)	t_{AA} = 25, 30, 35, 50	120 @ 25	Now
16K	2Kx8—CS Power-Down	24S	CY7C293A	5962-88680(W)	t_{AA} = 25, 30, 35, 50	120/30 @ 25	Now
16K	2Kx8—CS Power-Down	24S	CY7C293A	5962-92341(O)	t_{AA} = 25, 30, 35, 50	120/30 @ 35	Now
16K	2Kx8	24	CY7C292		t_{AA} = 35, 50	120 @ 35	Now
16K	2Kx8	24	CY7C292A	5962-88734(O)	t_{AA} = 25, 30, 35, 45, 50	120 @ 30	Now
16K	2Kx8—Reprogrammable State Machine	28S /44	CY7C258/9	5926-93122(W)	t_{CP} = 12, 15, 18	200 @ 15	Now
16K	2Kx8—Reprogrammable State Machine	28S /44	CY7C258/9	5926-93123(O)	t_{CP} = 12, 15, 18	200 @ 15	Now
64K	8Kx8—CS Power-Down	24S	CY7C261	5962-87515(W)	t_{AA} = 25, 35, 45, 55	140/50 @ 25	Now
64K	8Kx8—CS Power-Down	24S	CY7C261	5962-90803(O)	t_{AA} = 25, 35, 45, 55	120/30 @ 35	Now
64K	8Kx8	24S	CY7C263/4	5962-87515(W)	t_{AA} = 25, 35, 45, 55	140 @ 25	Now
64K	8Kx8	24	CY7C263/4	5962-90803(O)	t_{AA} = 25, 35, 45, 55	120 @ 35	Now
64K	8Kx8—Registered	28S	CY7C265	5962-89967(O)	$t_{SA/CO}$ = 15/12, 25/20, 50/25	140 @ 18/15	Now
64K	8Kx8—Registered	28S	CY7C265	5962-89484(W)	$t_{SA/CO}$ = 15/12, 25/20, 50/25	120 @ 50/25	Now
64K	8Kx8—EPROM Pinout	28	CY7C266	5962-91624(W)	t_{AA} = 25, 45	140/15 @ 25	Now
64K	8Kx8—Registered/Diagnostic	28S	CY7C269	5962-90831(O)	$t_{SA/CO}$ = 15/12, 25/20, 50/25	140 @ 15/12	Now
64K	8Kx8—Registered/Diagnostic	28S	CY7C269	5962-90930(W)	$t_{SA/CO}$ = 15/12, 25/20, 50/25	140 @ 15/12	Now

PROMs (continued)

Size	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	883 Availability
128K	16Kx8—CS Power-Down	28S	CY7C251	5962-89537(W)	t_{AA} = 45, 55, 65	120/35 @ 45	Now
128K	16Kx8	28	CY7C254	5962-89538(W)	t_{AA} = 45, 55, 65	120 @ 45	Now
256K	Processor Specific	44	CY7C270		t_{CP} = 15, 20, 30	250@25	Now
256K	16Kx16	44	CY7C276		t_{AA}=25, 30, 35	250@30	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-89817(W)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-93166(O)	t_{AA}=35, 45, 55	130/40@55	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-89817(W)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-93166(O)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—Registered	28S	CY7C277	5962-91744(W)	$t_{SA/CO}$ = 40/20, 50/25	130 @ 40	Now
256K	32Kx8—Registered	28S	CY7C277	5962-92155(O)	$t_{SA/CO}$ = 40/20, 50/25	130 @ 40	Now
256K	32Kx8—Latched	28S	CY7C279		t_{AA} = 45, 55	130/40 @ 45	Now
512K	64Kx8—Fast Column Access	28S	CY7C285	5962-92322(W)	$t_{AA/FCA}$ = 75/25, 85/35	200 @ 75	Now
512K	64Kx8—EPROM Pinout	28	CY7C286	5962-91637(O)	t_{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—EPROM Pin	28	CY7C286	5962-92071(W)	t_{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—Registered	28S	CY7C287	5962-90913(W)	$t_{SA/CO}$ = 55/20, 65/25	150 @ 65	Now
512K	64Kx8—Registered	28S	CY7C287	5962-92065(O)	$t_{SA/CO}$ = 55/20, 65/25	150 @ 65	Now

PLDs

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
PAL20	16L8, 16R8, 16R6, 16R4	20	PAL16XX	5962-92338(O)	t_{PD} = 7, 10	180 @ 7	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88678(W)	t_{PD} = 20, 30, 40	70 @ 20	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88713(O)	t_{PD} = 20, 30, 40	70 @ 20	Now
PLD20	18G8—Generic	20	PLDC18G8	5962-91568(O)	$t_{PD/S/CO}$ = 15/15/20	110	Now
PLD24	22V10C—Macrocell	24S	PAL22V10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22VP10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-87539(W)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-87539(W)	$t_{PD/S/CO}$ = 20/17/15	100 @ 20	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-88670(O)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-88670(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/507(W)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/508(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10D—Macrocell	24S	PALC22V10D	5962-89841(O)	$t_{PD/S/CO}$=10/6/7	130@10	Now
PLDC24	22V10—Macrocell	24S	PALC22V10D	5962-89841(O)	$t_{PD/S/CO}$ = 10/6/6	150 @ 10	Now
PLDC24	20G10—Generic	24S	PLDC20G10	5962-88637(O)	$t_{PD/S/CO}$ = 20/17/15	80 @ 30	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90555(O)	$t_{PD/SU/CO}$ = 20/10/20	100 @ 25	Now
PLDC28	7C330—State Machine	28S	CY7C330	5962-89546(W)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C330—State Machine	28S	CY7C330	5926-90802(O)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-90754(W)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-89855(O)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C332—Combinatorial	28S	CY7C332	5962-91584(W)	t_{PD} = 20, 25, 30	200 @ 24 MHz	Now
PLD28	7C335—Universal State Machine	28S	CY7C335		f_{MAX5} = 66.6, 50, 83	160 @ 66.6 MHz	Now
MAX28	7C344—32 Macrocell	28S	CY7C344	5962-90611(W)	t_{PD} = 25, 35	220/170	Now
MAX40	7C343—64 Macrocell	40/44	CY7C343	5962-92158(W)	t_{PD} = 25, 30, 35	160/120	Now
MAX68	7C342—128 Macrocell	68	CY7C342	5962-89468(W)	t_{PD} = 30, 35, 40	320/240	Now
MAX84	7C341—192 Macrocell	84	CY7C341	5962-92062(W)	t_{PD} = 30, 35, 40	320/240	Now
PLDC28	7C361—State Machine	28S	CY7C361		100, 83, 66 MHz	150 @ 100 MHz	Now

FIFOs

Organization	Pins	Part Number	JAN/SMD Number	Speed	I_{CC}/I_{SB} (mA @ ns/MHz)	883 Availability
64x4—Cascadable	16	CY3341		1.2, 2 MHz	60 @ 2.0 MHz	Now
64x4—Cascadable	16	CY7C401		10, 15, 25 MHz	90 @ 15 MHz	Now
64x4—Cascadable/OE	16	CY7C403	5962-89523	10, 15, 25 MHz	90 @ 25 MHz	Now
64x5—Cascadable	18	CY7C402		10, 15, 25 MHz	90 @ 15 MHz	Now
64x5—Cascadable/OE	18	CY7C404	5962-86846	10, 15, 25 MHz	90 @ 25 MHz	Now
64x8—Cascadable/OE	28S	CY7C408A	5962-89664	15, 25 MHz	120 @ 25 MHz	Now
64x9—Cascadable	28S	CY7C409A	5962-89661	15, 25 MHz	120 @ 25 MHz	Now
512x9—Cascadable	28	CY7C420	5962-89863	t_A = 25, 30, 40, 65 ns	140/30 @ 30	Now

FIFOs (continued)

Organization	Pins	Part Number	JAN/SMD Number	Speed	I_{CC}/I_{SB} (mA @ ns/MHz)	883 Availability
512x9—Cascadable	28S	CY7C421	5962-89863	t_A = 25, 30, 40, 65 ns	147/30 @ 25	Now
1Kx9—Cascadable	28	CY7C424	5962-91585	t_A = 25, 30, 40, 65 ns	140/30 @ 30	Now
1Kx9—Cascadable	28S	CY7C425	5962-91585	t_A = 25, 30, 40, 65 ns	147/30 @ 25	Now
2Kx9—Cascadable	28	CY7C428	5962-88669	t_A = 25, 30, 40, 65 ns	140/30 @ 30	Now
2Kx9—Cascadable	28S	CY7C429	5962-88669	t_A = 25, 30, 40, 65 ns	147/30 @ 25	Now
2Kx9—Bidirectional	28S	CY7C439	5962-92321	t_A = 30, 40, 65 ns	170/45 @ 30	Now
4Kx9—Cascadable	28	CY7C432	5962-90715	t_A = 30, 40, 65 ns	160/30 @ 30	Now
4Kx9—Cascadable	28S	CY7C433	5962-90715	t_A = 30, 40, 65 ns	160/30 @ 30	Now
512x9—Clocked	28S	CY7C441		t_C = 14, 20, 30 ns	160 @ 14	Now
2Kx9—Clocked	28S	CY7C443		t_C = 14, 20, 30 ns	160 @ 14	Now
512x9—Clocked/Cascadable	32	CY7C451	5962-93173	t_C = 14, 20, 30 ns	160 @ 14	Now
2Kx9—Clocked/Cascadable	32	CY7C453	5962-93124	t_C = 14, 20, 30 ns	160 @ 14	Now
8Kx9—Half Full Flag	28	CY7C460		t_A = 20, 25, 40 ns	165 @ 25	Now
8Kx9—Prog. Flags	28	CY7C470		t_A = 20, 25, 40 ns	165 @ 25	Now
16Kx9—Half Full Flag	28	CY7C462	5962-93008	t_A = 20, 25, 40 ns	165 @ 25	Now
16Kx9—Prog. Flags	28	CY7C472		t_A = 20, 25, 40 ns	165 @ 25	Now
32Kx9—Half Full Flag	28	CY7C464	5962-93152	t_A = 20, 25, 40 ns	165 @ 25	Now
32Kx9—Prog. Flags	28	CY7C474		t_A = 20, 25, 40 ns	165 @ 25	Now
512x18—Prog. Flags	52	CY7C455		t_A = 10, 15, 20 ns	180@70	1Q94
1Kx18—Prog. Flags	52	CY7C456		t_A = 10, 15, 20 ns	180@70	1Q94
2Kx18—Prog. Flags	52	CY7C457		t_A = 10, 15, 20 ns	180@70	1Q94

Logic

Organization	Pins	Part Number	JAN/SMD Number	Speed (ns)	I_{CC} (mA @ ns)	883 Availability
Programmable Skew Clock Buffer (TTL Outputs)	32	CY7B991		f_{REF} = 15 – 80 MHz	75	Now
Programmable Skew Clock Buffer (CMOS Outputs)	32	CY7B992	5962-93112	f_{REF} = 15 – 80 MHz	75	Now
2901—4-Bit Slice	40	CY7C901	5962-88535	t_{CLK} = 27, 32	90 @ 27	Now
2901—4-Bit Slice	40	CY2901C	5962-88535	C	180 @ 32	Now
4x2901—16-Bit Slice	64	CY7C9101	5962-89517	t_{CLK} = 35, 45	85 @ 35	Now
2909—Sequencer	28	CY7C909		t_{CLK} = 30, 40	55 @ 30	Now
2911—Sequencer	20	CY7C911	5962-90609	t_{CLK} = 30, 40	55 @ 30	Now
2909—Sequencer	28	CY2909A		A	90 @ 40	Now
2911—Sequencer	20	CY2911A	5962-90609	A	90 @ 40	Now
2910—Controller (17-Word Stack)	40	CY7C910	5962-87708	t_{CLK} = 46, 51, 99	90 @ 46	Now
2910—Controller (9-Word Stack)	40	CY2910A	5962-87708	A	170 @ 51	Now
16x16 Multiplier	64	CY7C516	5962-86873	t_{MC} = 42, 55, 75	110 @ 10 MHz	Now
16x16 Multiplier	64	CY7C517	5962-87686	t_{MC} = 42, 55, 75	110 @ 10 MHz	Now
16x16 Multiplier/Accumulator	64	CY7C510	5962-88733	t_{MC} = 55, 65, 75	110 @ 10 MHz	Now

VMEbus Interface Products

Organization	Pins	Part Number	JAN/SMD Number	Speed (MHz)	I_{CC} (mA)	883 Availability
VME Interface Controller	144/160	VIC068A	5962-92010	64	250	Now
VME Address Controller	144/160	VAC068A	5962-92009	50	150	Now
64-Bit VIC	144/160	VIC64		64	300	Now

Communication Products

Organization	Pins	Part Number	Speed (Mbps)	I_{CC} (mA)	Packages	883 Availability
HotLink Transmitter	28	CY7B923	160 – 330	TBA	D, L,	4Q93
HotLink Receiver	28	CY7B933	160 – 330	TBA	D, L,	4Q93

Modules

Size	Organization	Pins	Part Number	Packages	Speed (ns)	I_{CC} (mA @ ns)	883 Availability
SRAMs							
2M	64Kx32 SRAM	60	CYM1830	HD06	t_{AA} = 35, 45, 55	880 @ 35	Now
4M	128Kx32 SRAM	66	CYM1838		t_{AA} = 25, 30, 35	720 @ 25	Now
4M	512Kx8 SRAM	32	CYM1466	HD12	t_{AA} = 35, 45, 55, 70 85, 100, 120	350 @ 35	Now
4M	256Kx16 SRAM	48	CYM1641	HD05	t_{AA}=35, 45, 55	1800@35	Now

Notes:

The Cypress facility at 3901 North First Street in San Jose, CA is DESC-certified for JAN class B production.

All of the above products are available with processing to MIL-STD-883D at a minimum. Many of these products are also available either to SMDs (Standardized Military Drawings) or to JAN slash sheets.

The speed and power specifications listed above cover the full military temperature range.

Modules are available with MIL-STD-883D components. These modules are assembled and screened to the proposed JEDEC military processing standard for modules.

W = Windowed Package
O = Opaque Package
HD = Hermetic DIP Module

100K ECL devices are available only to extended temperature range.

22S stands for 22-pin 300-mil DIP.
24S stands for 24-pin 300-mil DIP.
28S stands for 28-pin 300-mil DIP.
32S stands for 32-pin 300-mil DIP.

Cypress Semiconductor fully supports the DESC standardized Military Drawing Program for devices that are compliant to the Class B requirements of MIL-STD-883D.

Listed below are the SMDs for which Cypress is an approved source of supply. Please contact your local Cypress representative for the latest SMD update.

DESC SMD (Standardized Military Drawing) Approvals[1]

SMD Number		Cypress[2] Part Number	Package[3]		Product Description
			Description	Type	
84036	09JX	CY6116A–45DMB	24.6 DIP	D12	2K x 8 SRAM
84036	09KX	CY7C128A–45KMB	24 CP	K73	2K x 8 SRAM
84036	09LX	CY7C128A–45DMB	24.3 DIP	D14	2K x 8 SRAM
84036	09XX	CY6117A–45LMB	32 R LCC	L55	2K x 8 SRAM
84036	09YX	CY7C128A–45LMB	24 R LCC	L53	2K x 8 SRAM
84036	093X	CY6116A–45LMB	28 S LCC	L64	2K x 8 SRAM
84036	11JX	CY6116A–55DMB	24.6 DIP	D12	2K x 8 SRAM
84036	11KX	CY7C128A–55KMB	24 CP	K73	2K x 8 SRAM
84036	11LX	CY7C128A–55DMB	24.3 DIP	D14	2K x 8 SRAM
84036	11XX	CY6117A–55LMB	32 R LCC	L55	2K x 8 SRAM
84036	11YX	CY7C128A–55LMB	24 R LCC	D14	2K x 8 SRAM
84036	113X	CY6116A–55LMB	28 S LCC	L64	2K x 8 SRAM
84036	14JX	CY6116A–35DMB	24.6 DIP	D12	2K x 8 SRAM
84036	14KX	CY7C128A–35KMB	24 CP	K73	2K x 8 SRAM
84036	14LX	CY7C128A–35DMB	24.3 DIP	D14	2K x 8 SRAM
84036	14XX	CY6117A–35LMB	32 R LCC	L55	2K x 8 SRAM
84036	14YX	CY7C128A–35LMB	24 R LCC	L53	2K x 8 SRAM
84036	143X	CY6116A–35LMB	28 S LCC	L64	2K x 8 SRAM
84132	02RA	CY7C167A–45DMB	20.3 DIP	D6	16K x 1 SRAM
84132	02SA	CY7C167A–45KMB	20 CP	K71	16K x 1 SRAM
84132	02YA	CY7C167A–45LMB	20 R LCC	L51	16K x 1 SRAM
84132	05RA	CY7C167A–35DMB	20.3 DIP	D6	16K x 1 SRAM
84132	05SA	CY7C167A–35KMB	20 CP	K71	16K x 1 SRAM
84132	05YA	CY7C167A–35LMB	20 R LCC	L51	16K x 1 SRAM
5962–38294	09MTX	CY7C185A–55KMB	28 CP	K74	8K x 8 SRAM
5962–38294	23MUX	CY7C185A–55LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	09MXX	CY7C186A–55DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	09MYX	CY7C186A–55LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	09MZX	CY7C185A–55DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	11MTX	CY7C185A–45KMB	28 CP	K74	8K x 8 SRAM
5962–38294	25MUX	CY7C185A–45LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	11MXX	CY7C186A–45DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	11MYX	CY7C186A–45LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	11MZX	CY7C185A–45DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	13MTX	CY7C185A–35KMB	28 CP	K74	8K x 8 SRAM
5962–38294	27MUX	CY7C185A–35LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	13MXX	CY7C186A–35DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	13MYX	CY7C186A–35LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	13MZX	CY7C185A–35DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	15MTX	CY7C185A–25KMB	28 CP	K74	8K x 8 SRAM
5962–38294	29MUX	CY7C185A–25LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	15MXX	CY7C186A–25DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	15MYX	CY7C186A–25LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	15MZX	CY7C185A–25DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	17MTX	CY7C185A–20KMB	28 CP	K74	8K x 8 SRAM
5962–38294	30MUX	CY7C185A–20LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	17MXX	CY7C186A–20DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	17MYX	CY7C186A–20LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	17MZX	CY7C185A–20DMB	28.3 DIP	D22	8K x 8 SRAM
5962–85525	05TX	CY7C185A–55KMB	28 CP	K74	8K x 8 SRAM
5962–85525	05UX	CY7C185A–55LMB	28 R TLCC	L54	8K x 8 SRAM
5962–85525	05XX	CY7C186A–55DMB	28.6 DIP	D16	8K x 8 SRAM
5962–85525	05ZX	CY7C185A–55DMB	28.3 DIP	D22	8K x 8 SRAM
5962–85525	06TX	CY7C185A–45KMB	28 CP	K74	8K x 8 SRAM
5962–85525	06UX	CY7C185A–45LMB	28 R TLCC	L54	8K x 8 SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–85525 06XX	CY7C186A–45DMB	28.6 DIP	D16	8K x 8 SRAM
5962–85525 06ZX	CY7C185A–45DMB	28.3 DIP	D22	8K x 8 SRAM
5962–85525 07TX	CY7C185A–35KMB	28 CP	K74	8K x 8 SRAM
5962–85525 07UX	CY7C185A–35LMB	28 R TLCC	L54	8K x 8 SRAM
5962–85525 07XX	CY7C186A–35DMB	28.6 DIP	D16	8K x 8 SRAM
5962–85525 07ZX	CY7C185A–35DMB	28.3 DIP	D22	8K x 8 SRAM
5962–86015 01YX	CY7C187A–35DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015 01ZX	CY7C187A–35LMB	22 R LCC	L52	64K x 1 SRAM
5962–86015 02YX	CY7C187AL–35DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015 02ZX	CY7C187AL–35LMB	22 R LCC	L52	64K x 1 SRAM
5962–86015 03YX	CY7C187A–45DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015 03ZX	CY7C187A–45LMB	22 R LCC	L52	64K x 1 SRAM
5962–86015 04YX	CY7C187AL–45DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015 04ZX	CY7C187AL–45LMB	22 R LCC	L52	64K x 1 SRAM
5962–86705 12RA	CY7C168A–35DMB	20.3 DIP	D6	4K x 4 SRAM
5962–86705 12XA	CY7C168A–35LMB	20 R LCC	L51	4K x 4 SRAM
5962–86846 01VX	CY7C404–10DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 012X	CY7C404–10LMB	20 S LCC	L61	64 x 5 FIFO
5962–86846 01XX	CY7C404–10KMB	18 CP	K70	64 x 5 FIFO
5962–86846 02VX	CY7C404–15DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 022X	CY7C404–15LMB	20 S LCC	L61	64 x 5 FIFO
5962–86846 02XX	CY7C404–15KMB	18 CP	K70	64 x 5 FIFO
5962–86846 03VX	CY7C404–25DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 032X	CY7C404–25LMB	20 S LCC	L61	64 x 5 FIFO
5962–86846 03XX	CY7C404–25KMB	18 CP	K70	64 x 5 FIFO
5962–86859 15KX	CY7C166AL–45KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–86859 15LX	CY7C166AL–45DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 15UX	CY7C166AL–45LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–86859 15XX	CY7C166AL–45LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–86859 16KX	CY7C166A–45KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–86859 16LX	CY7C166A–45DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 16UX	CY7C166A–45LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–86859 16XX	CY7C166A–45LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–86859 17KX	CY7C166AL–35KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–86859 17LX	CY7C166AL–35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 17UX	CY7C166AL–35LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–86859 17XX	CY7C166AL–35LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–86859 18KX	CY7C166A–35KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–86859 18LX	CY7C166A–35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 18UX	CY7C166A–35LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–86859 18XX	CY7C166A–35LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–86859 21KX	CY7C164AL–45KMB	24 CP	K73	16K x 4 SRAM
5962–86859 21YX	CY7C164AL–45DMB	22.3 DIP	D10	16K x 4 SRAM
5962–86859 21ZX	CY7C164AL–45LMB	22 R LCC	L52	16K x 4 SRAM
5962–86859 22KX	CY7C164A–45KMB	24 CP	K73	16K x 4 SRAM
5962–86859 22YX	CY7C164A–45DMB	22.3 DIP	D10	16K x 4 SRAM
5962–86859 22ZX	CY7C164A–45LMB	22 R LCC	L52	16K x 4 SRAM
5962–86859 23KX	CY7C164AL–35KMB	24 CP	K73	16K x 4 SRAM
5962–86859 23YX	CY7C164AL–35DMB	22.3 DIP	D10	16K x 4 SRAM
5962–86859 23ZX	CY7C164AL–35LMB	22 R LCC	L52	16K x 4 SRAM
5962–86859 24KX	CY7C164A–35KMB	24 CP	K73	16K x 4 SRAM
5962–86859 24YX	CY7C164A–35DMB	22.3 DIP	D10	16K x 4 SRAM
5962–86859 24ZX	CY7C164A–35LMB	22 R LCC	L52	16K x 4 SRAM
5962–86873 01XX	CY7C516–42DMB	64 DIP	D30	16 x 16 Multiplier
5962–86873 01YX	CY7C516–42LMB	68 S LCC	L81	16 x 16 Multiplier
5962–86873 01ZX	CY7C516–42GMB	68 PGA	G68	16 x 16 Multiplier
5962–86873 01UX	CY7C516–42FMB	64 Q FP	F90	16 x 16 Multiplier
5962–86873 02XX	CY7C516–55DMB	64 DIP	D30	16 x 16 Multiplier

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962–86873 02YX	CY7C516–55LMB	68 S LCC	L81	16 x 16 Multiplier
5962–86873 02ZX	CY7C516–55GMB	68 PGA	G68	16 x 16 Multiplier
5962–86873 02UX	CY7C516–55FMB	64 Q FP	F90	16 x 16 Multiplier
5962–86873 03XX	CY7C516–75DMB	64 DIP	D30	16 x 16 Multiplier
5962–86873 03YX	CY7C516–75LMB	68 S LCC	L81	16 x 16 Multiplier
5962–86873 03ZX	CY7C516–75GMB	68 PGA	G68	16 x 16 Multiplier
5962–86873 03UX	CY7C516–75FMB	64 Q FP	F90	16 x 16 Multiplier
5962–86875 03XX	CY7C130–55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 03YX	CY7C130–55LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 03ZX	CY7C131–55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 03UX	CY7C130–55FMB	48 QFP	F90	1K x 8 Dual-Port SRAM
5962–86875 04XX	CY7C130–45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 04YX	CY7C130–45LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 04ZX	CY7C131–45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 04UX	CY7C130–45FMB	48 QFP	F90	1K x 8 Dual-Port SRAM
5962–86875 11XX	CY7C140–55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 11YX	CY7C140–55LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 11ZX	CY7C141–55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 11UX	CY7C140–55FMB	48 QFP	F90	1K x 8 Dual-Port SRAM
5962–86875 12XX	CY7C140–45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 12YX	CY7C140–45LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 12ZX	CY7C141–45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 12UX	CY7C140–45FMB	48 QFP	F90	1K x 8 Dual-Port SRAM
5962–86875 19XX	CY7C130–35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 19YX	CY7C130–35LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 19ZX	CY7C131–35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 20XX	CY7C140–35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 20YX	CY7C140–35LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962–86875 20ZX	CY7C141–35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–87515 05KX	CY7C261–45TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 05LX	CY7C261–45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 053X	CY7C261–45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 06KX	CY7C261–55TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 06LX	CY7C261–55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 063X	CY7C261–55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 07KX	CY7C261–35TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 07LX	CY7C261–35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 073X	CY7C261–35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 08JX	CY7C264–35WMB	24.6 DIP	W14	8K x 8 UV EPROM
5962–87515 08KX	CY7C263–35TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 08LX	CY7C263–35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 083X	CY7C263–35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 09JX	CY7C264–45WMB	24.6 DIP	W14	8K x 8 UV EPROM
5962–87515 09KX	CY7C263–45TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 09LX	CY7C263–45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 093X	CY7C263–45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 10JX	CY7C264–55WMB	24.6 DIP	W14	8K x 8 UV EPROM
5962–87515 10KX	CY7C263–55TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 10LX	CY7C263–55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 103X	CY7C263–55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 11JX	CY7C264–25WMB	24.6 DIP	W14	8K x 8 UV EPROM
5962–87515 11KX	CY7C263–25TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 11LX	CY7C263–25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 113X	CY7C263–25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 12KX	CY7C261–25TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 12LX	CY7C261–25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 123X	CY7C261–25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87529 01KX	CY7C245–45TMB	24 CP	T73	2K x 8 Registered UV PROM
5962–87529 01LX	CY7C245–45WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962–87529 013X	CY7C245–45QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962–87529 02KX	CY7C245–35TMB	24 CP	T73	2K x 8 Registered UV PROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–87529 02LX	CY7C245–35WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962–87529 023X	CY7C245–35QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962–87539 01KX	PALC22V10–25TMB	24 CP	T73	24-Pin CMOS UV EPLD
5962–87539 01LX	PALC22V10–25WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 013X	PALC22V10–25QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87539 02KX	PALC22V10–30TMB	24 CP	T73	24-Pin CMOS UV EPLD
5962–87539 02LX	PALC22V10–30WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 023X	PALC22V10–30QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87539 03KX	PALC22V10–40TMB	24 CP	T73	24-Pin CMOS UV EPLD
5962–87539 03LX	PALC22V10–40WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 033X	PALC22V10–40QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87539 04KX	PALC22V10B–20TMB	24 CP	T73	24-Pin CMOS UV EPLD
5962–87539 04LX	PALC22V10B–20WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 043X	PALC22V10B–20QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87650 01KX	CY7C291–50TMB	24 CP	T73	2K x 8 UV EPROM
5962–87650 01LX	CY7C291–50WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 013X	CY7C291–50QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962–87650 03KX	CY7C291–35TMB	24 CP	T73	2K x 8 UV EPROM
5962–87650 03LX	CY7C291–35WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 033X	CY7C291–35QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962–87650 05KX	CY7C291A–25TMB	24 CP	T73	2K x 8 UV EPROM
5962–87650 05LX	CY7C291A–25WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 053X	CY7C291A–25QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962–87651 01JX	CY7C282–45DMB	24.6 DIP	D12	1K x 8 PROM
5962–87651 01KX	CY7C281–45KMB	24 CP	K73	1K x 8 PROM
5962–87651 01LX	CY7C281–45DMB	24.3 DIP	D14	1K x 8 PROM
5962–87651 013X	CY7C281–45LMB	28 S LCC	L64	1K x 8 PROM
5962–87686 01XX	CY7C517–42DMB	64 DIP	D30	16 x 16 Multiplier
5962–87686 01YX	CY7C517–42LMB	68 S LCC	L81	16 x 16 Multiplier
5962–87686 01ZX	CY7C517–42GMB	68 PGA	G68	16 x 16 Multiplier
5962–87686 01UX	CY7C517–42FMB	64 Q FP	F90	16 x 16 Multiplier
5962–87686 02XX	CY7C517–55DMB	64 DIP	D30	16 x 16 Multiplier
5962–87686 02YX	CY7C517–55LMB	68 S LCC	L81	16 x 16 Multiplier
5962–87686 02ZX	CY7C517–55GMB	68 PGA	G68	16 x 16 Multiplier
5962–87686 02UX	CY7C517–55FMB	64 Q FP	F90	16 x 16 Multiplier
5962–87686 03XX	CY7C517–75DMB	64 DIP	D30	16 x 16 Multiplier
5962–87686 03YX	CY7C517–75LMB	68 S LCC	L81	16 x 16 Multiplier
5962–87686 03ZX	CY7C517–75GMB	68 PGA	G68	16 x 16 Multiplier
5962–87686 03UX	CY7C517–75FMB	64 Q FP	F90	16 x 16 Multiplier
5962–87708 01QX	CY2910ADMB	40.6 DIP	D18	Microprogram Controller
5962–87708 01UX	CY2910ALMB	44 LCC	L67	Microprogram Controller
5962–87708 04QX	CY7C910–51DMB	40.6 DIP	D18	Microprogram Controller
5962–87708 04UX	CY7C910–51LMB	44 LCC	L67	Microprogram Controller
5962–87708 05QX	CY7C910–46DMB	40.6 DIP	D18	Microprogram Controller
5962–87708 05UX	CY7C910–46LMB	44 LCC	L67	Microprogram Controller
5962–88518 01LX	CY7C225–30DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 013X	CY7C225–30LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88518 02LX	CY7C225–35DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 023X	CY7C225–35LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88518 03LX	CY7C225–40DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 033X	CY7C225–40LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88535 01QX	CY7C901–32DMB	40.6 DIP	D18	4-Bit Slice
5962–88535 01XX	CY7C901–32LMB	44 LCC	L67	4-Bit Slice
5962–88535 01YX	CY7C901–32FMB	42 FP	F76	4-Bit Slice
5962–88535 02QX	CY7C901–27DMB	40.6 DIP	D18	4-Bit Slice
5962–88535 02XX	CY7C901–27LMB	44 LCC	L67	4-Bit Slice
5962–88535 02YX	CY7C901–27FMB	42 FP	F76	4-Bit Slice
5962–88587 01VX	CY7C147–45DMB	18.3 DIP	D4	4K x 1 SRAM
5962–88587 01XX	CY7C147–45KMB	18 CP	K70	4K x 1 SRAM
5962–88587 01YX	CY7C147–45LMB	18 R LCC	L50	4K x 1 SRAM
5962–88587 02VX	CY7C147–35DMB	18.3 DIP	D4	4K x 1 SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88587 02XX	CY7C147–35KMB	18 CP	K70	4K x 1 SRAM
5962–88587 02YX	CY7C147–35LMB	18 R LCC	L50	4K x 1 SRAM
5962–88588 01KX	CY7C150–35KMB	24 CP	K73	1K x 4 SRAM with Reset
5962–88588 01LX	CY7C150–35DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88588 01XX	CY7C150–35LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962–88588 02KX	CY7C150–25KMB	24 CP	K73	1K x 4 SRAM with Reset
5962–88588 02LX	CY7C150–25DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88588 02XX	CY7C150–25LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962–88588 03KX	CY7C150–15KMB	24 CP	K73	1K x 4 SRAM with Reset
5962–88588 03LX	CY7C150–15DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88588 03XX	CY7C150–15LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962–88594 02WX	CY7C122–35DMB	22.4 DIP	D8	256 x 4 SRAM
5962–88594 02KX	CY7C122–35KMB	24 CP	K73	256 x 4 SRAM
5962–88594 03WX	CY7C122–25DMB	22.4 DIP	D8	256 x 4 SRAM
5962–88594 03KX	CY7C122–25KMB	24 CP	K73	256 x 4 SRAM
5962–88636 01KX	CY7C235–40KMB	24 CP	K73	1K x 8 Registered PROM
5962–88636 01LX	CY7C235–40DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962–88636 013X	CY7C235–40LMB	28 S LCC	L64	1K x 8 Registered PROM
5962–88636 02KX	CY7C235–30KMB	24 CP	K73	1K x 8 Registered PROM
5962–88636 02LX	CY7C235–30DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962–88636 023X	CY7C235–30LMB	28 S LCC	L64	1K x 8 Registered PROM
5962–88637 01KX	PLDC20G10–40KMB	24 CP	K73	Generic CMOS PLD
5962–88637 01LX	PLDC20G10–40DMB	24.3 DIP	D14	Generic CMOS PLD
5962–88637 013X	PLDC20G10–40LMB	28 S LCC	L64	Generic CMOS PLD
5962–88637 02KX	PLDC20G10–30KMB	24 CP	K73	Generic CMOS PLD
5962–88637 02LX	PLDC20G10–30DMB	24.3 DIP	D14	Generic CMOS PLD
5962–88637 023X	PLDC20G10–30LMB	28 S LCC	L64	Generic CMOS PLD
5962–88662 03MX	CY7C199–55KMB	28 CP	K74	32K x 8 SRAM
5962–88662 03NX	CY7C199–55DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 03UX	CY7C199–55LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 03XX	CY7C198–55DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 03YX	CY7C198–55LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 04MX	CY7C199–45KMB	28 CP	K74	32K x 8 SRAM
5962–88662 04NX	CY7C199–45DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 04UX	CY7C199–45LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 04XX	CY7C198–45DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 04YX	CY7C198–45LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 05MX	CY7C199–35KMB	28 CP	K74	32K x 8 SRAM
5962–88662 05NX	CY7C199–35DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 05UX	CY7C199–35LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 05XX	CY7C198–35DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 05YX	CY7C198–35LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 06MX	CY7C199–25KMB	28 CP	K74	32K x 8 SRAM
5962–88662 06NX	CY7C199–25DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 06UX	CY7C199–25LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 06XX	CY7C198–25DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 06YX	CY7C198–25LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 07NX	CY7C199–20DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 07MX	CY7C199–20KMB	28 CP	K74	32K x 8 SRAM
5962–88662 07UX	CY7C199–20LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 07YX	CY7C198–20LMB	32 R LCC	L55	32K x 8 SRAM
5962–88669 02UX	CY7C429–65KMB	28 CP	K74	2K x 9 FIFO
5962–88669 02XX	CY7C428–65DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 02YX	CY7C429–65DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 02ZX	CY7C429–65LMB	32 R LCC	L55	2K x 9 FIFO
5962–88669 03UX	CY7C429–50KMB	28 CP	K74	2K x 9 FIFO
5962–88669 03XX	CY7C428–50DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 03YX	CY7C429–50DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 03ZX	CY7C429–50LMB	32 R LCC	L55	2K x 9 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88669 04UX	CY7C429–40KMB	28 CP	K74	2K x 9 FIFO
5962–88669 04XX	CY7C428–40DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 04YX	CY7C429–40DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 04ZX	CY7C429–40LMB	32 R LCC	L55	2K x 9 FIFO
5962–88669 05UX	CY7C429–30KMB	28 CP	K74	2K x 9 FIFO
5962–88669 05XX	CY7C428–30DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 05YX	CY7C429–30DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 05ZX	CY7C429–30LMB	32 R LCC	L55	2K x 9 FIFO
5962–88670 01KX	PALC22V10–25KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 01LX	PALC22V10–25DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 013X	PALC22V10–25LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 02KX	PALC22V10–30KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 02LX	PALC22V10–30DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 023X	PALC22V10–30LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 03KX	PALC22V10–40KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 03LX	PALC22V10–40DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 033X	PALC22V10–40LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 04KX	PALC22V10B–20KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 04LX	PALC22V10B–20DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 043X	PALC22V10B–20LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 05KX	PALC22V10B–15KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 05LX	PALC22V10B–15DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 053X	PALC22V10B–15LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88678 01RX	PALC16L8–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 01SX	PALC16L8–40TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 01XX	PALC16L8–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 02RX	PALC16R8–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 02SX	PALC16R8–40TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 02XX	PALC16R8–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 03RX	PALC16R6–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 03SX	PALC16R6–40TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 03XX	PALC16R6–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 04RX	PALC16R4–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 04SX	PALC16R4–40TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 04XX	PALC16R4–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 05RX	PALC16L8–30WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 05SX	PALC16L8–30TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 05XX	PALC16L8–30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 06RX	PALC16R8–30WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 06SX	PALC16R8–30TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 06XX	PALC16R8–30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 07RX	PALC16R6–30WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 07SX	PALC16R6–30TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 07XX	PALC16R6–30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 08RX	PALC16R4–30WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 08SX	PALC16R4–30TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 08XX	PALC16R4–30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 09RX	PALC16L8–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 09SX	PALC16L8–20TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 09XX	PALC16L8–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 10RX	PALC16R8–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 10SX	PALC16R8–20TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 10XX	PALC16R8–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 11RX	PALC16R6–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 11SX	PALC16R6–20TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 11XX	PALC16R6–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 12RX	PALC16R4–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 12SX	PALC16R4–20TMB	20 CP	T71	20-Pin CMOS UV EPLD
5962–88678 12XX	PALC16R4–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88680 01LX	CY7C293A–50WMB	24.3 DIP	W14	2K x 8 UV EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-88680 01KX	CY7C293A-50TMB	24 CP	T73	2K x 8 UV EPROM
5962-88680 013X	CY7C293A-50QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-88680 02LX	CY7C293A-35WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962-88680 02KX	CY7C293A-35TMB	24 CP	T73	2K x 8 UV EPROM
5962-88680 023X	CY7C293A-35QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-88680 03LX	CY7C293A-30WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962-88680 03KX	CY7C293A-30TMB	24 CP	T73	2K x 8 UV EPROM
5962-88680 033X	CY7C293A-30QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-88680 04LX	CY7C293A-25WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962-88680 04KX	CY7C293A-25TMB	24 CP	T73	2K x 8 UV EPROM
5962-88680 043X	CY7C293A-25QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-88681 01LX	CY7C194-35DMB	24.3 DIP	D14	64K x 4 SRAM
5962-88681 01XX	CY7C194-35LMB	28 R LCC	L54	64K x 4 SRAM
5962-88681 02LX	CY7C194-45DMB	24.3 DIP	D14	64K x 4 SRAM
5962-88681 02XX	CY7C194-45LMB	28 R LCC	L54	64K x 4 SRAM
5962-88713 01RX	PALC16L8-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 01SX	PALC16L8-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 01XX	PALC16L8-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 02RX	PALC16R8-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 02SX	PALC16R8-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 02XX	PALC16R8-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 03RX	PALC16R6-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 03SX	PALC16R6-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 03XX	PALC16R6-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 04RX	PALC16R4-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 04SX	PALC16R4-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 04XX	PALC16R4-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 05RX	PALC16L8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 05SX	PALC16L8-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 05XX	PALC16L8-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 06RX	PALC16R8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 06SX	PALC16R8-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 06XX	PALC16R8-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 07RX	PALC16R6-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 07SX	PALC16R6-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 07XX	PALC16R6-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 08RX	PALC16R4-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 08SX	PALC16R4-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 08XX	PALC16R4-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 09RX	PALC16L8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 09SX	PALC16L8-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 09XX	PALC16L8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 10RX	PALC16R8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 10SX	PALC16R8-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 10XX	PALC16R8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 11RX	PALC16R6-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 11SX	PALC16R6-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 11XX	PALC16R6-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 12RX	PALC16R4-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 12SX	PALC16R4-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 12XX	PALC16R4-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88725 01LX	CY7C197-35DMB	24.3 DIP	D14	256K x 1 SRAM
5962-88725 01XX	CY7C197-35LMB	28 R LCC	L54	256K x 1 SRAM
5962-88725 02LX	CY7C197-45DMB	24.3 DIP	D14	256K x 1 SRAM
5962-88725 02XX	CY7C197-45LMB	28 R LCC	L54	256K x 1 SRAM
5962-88725 05LX	CY7C197-25DMB	24.3 DIP	D14	256K x 1 SRAM
5962-88725 05XX	CY7C197-25LMB	28 R LCC	L54	256K x 1 SRAM
5962-88733 01XX	CY7C510-55DMB	64 DIP	D30	16 x 16 MAC
5962-88733 01YX	CY7C510-55LMB	68 S LCC	L81	16 x 16 MAC
5962-88733 01ZX	CY7C510-55GMB	68 PGA	G68	16 x 16 MAC
5962-88733 02XX	CY7C510-65DMB	64 DIP	D30	16 x 16 MAC

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88733 02YX	CY7C510–65LMB	68 S LCC	L81	16 x 16 MAC
5962–88733 02ZX	CY7C510–65GMB	68 PGA	G68	16 x 16 MAC
5962–88733 03XX	CY7C510–75DMB	64 DIP	D30	16 x 16 MAC
5962–88733 03YX	CY7C510–75LMB	68 S LCC	L81	16 x 16 MAC
5962–88733 03ZX	CY7C510–75GMB	68 PGA	G68	16 x 16 MAC
5962–88734 02JX	CY7C292A–45DMB	24.6 DIP	D12	2K x 8 EPROM
5962–88734 02KX	CY7C291A–45KMB	24 CP	K73	2K x 8 EPROM
5962–88734 02LX	CY7C291A–45DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 023X	CY7C291A–45LMB	28 S LCC	L64	2K x 8 EPROM
5962–88734 03JX	CY7C292A–35DMB	24.6 DIP	D12	2K x 8 EPROM
5962–88734 03KX	CY7C291A–35KMB	24 CP	K73	2K x 8 EPROM
5962–88734 03LX	CY7C291A–35DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 033X	CY7C291A–35LMB	28 S LCC	L64	2K x 8 EPROM
5962–88734 04JX	CY7C292A–25DMB	24.6 DIP	D12	2K x 8 EPROM
5962–88734 04KX	CY7C291A–25KMB	24 CP	K73	2K x 8 EPROM
5962–88734 04LX	CY7C291A–25DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 043X	CY7C291A–25LMB	28 S LCC	L64	2K x 8 EPROM
5962–88735 01KX	CY7C245–45KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 01LX	CY7C245–45DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 013X	CY7C245–45LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 02KX	CY7C245–35KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 02LX	CY7C245–35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 023X	CY7C245–35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 03KX	CY7C245A–35KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 03LX	CY7C245A–35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 033X	CY7C245A–35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 04KX	CY7C245A–25KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 04LX	CY7C245A–25DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 043X	CY7C245A–25LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–89468 01XX	CY7C342–35RMB	68 SOJ	H81	128-Macrocell UV EPLD
5962–89468 01YX	CY7C342–35HMB	68 PGA	R68	128-Macrocell UV EPLD
5962–89468 01ZX	CY7C342–35TMB	68 QFP	T91	128-Macrocell UV EPLD
5962–89517 01XX	CY7C9101–45DMB	64 DIP	D30	16-Bit Slice
5962–89517 01YX	CY7C9101–45LMB	68 S LCC	L81	16-Bit Slice
5962–89517 01ZX	CY7C9101–45GMB	68 PGA	G68	16-Bit Slice
5962–89517 01UX	CY7C9101–45FMB	64 Q FP	F90	16-Bit Slice
5962–89517 02XX	CY7C9101–35DMB	64 DIP	D30	16-Bit Slice
5962–89517 02YX	CY7C9101–35LMB	68 S LCC	L81	16-Bit Slice
5962–89517 02ZX	CY7C9101–35GMB	68 PGA	G68	16-Bit Slice
5962–89517 02UX	CY7C9101–35FMB	64 Q FP	F90	16-Bit Slice
5962–89523 01EX	CY7C403–10DMB	16.3 DIP	D2	64 x 4 FIFO
5962–89523 012X	CY7C403–10LMB	20 S LCC	L61	64 x 4 FIFO
5962–89523 02EX	CY7C403–15DMB	16.3 DIP	D2	64 x 4 FIFO
5962–89523 022X	CY7C403–15LMB	20 S LCC	L61	64 x 4 FIFO
5962–89524 03XX	CY7C195L–45DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89524 04XX	CY7C195L–35DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89524 05XX	CY7C195L–25DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89537 01UX	CY7C251–65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 01YX	CY7C251–65WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 01ZX	CY7C251–65TMB	28 CP	T74	16K x 8 UV EPROM
5962–89537 02UX	CY7C251–55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 02YX	CY7C251–55WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 02ZX	CY7C251–55TMB	28 CP	T74	16K x 8 UV EPROM
5962–89537 03UX	CY7C251–45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 03YX	CY7C251–45WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 03ZX	CY7C251–45TMB	28 CP	T74	16K x 8 UV EPROM
5962–89538 01UX	CY7C254–65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89538 01XX	CY7C254–65WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962–89538 01ZX	CY7C254–65TMB	28 CP	T74	16K x 8 UV EPROM
5962–89538 02UX	CY7C254–55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89538 02XX	CY7C254–55WMB	28.6 DIP	W16	16K x 8 UV EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-89538 02ZX	CY7C254-55TMB	28 CP	T74	16K x 8 UV EPROM
5962-89538 03UX	CY7C254-45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89538 03XX	CY7C254-45WMB	28.3 DIP	W16	16K x 8 UV EPROM
5962-89538 03ZX	CY7C254-45TMB	28 CP	T74	16K x 8 UV EPROM
5962-89546 01XX	CY7C330-28WMB	28.3 DIP	W22	PLD State Machine
5962-89546 01YX	CY7C330-28TMB	28 CP	T74	PLD State Machine
5962-89546 013X	CY7C330-28QMB	28 S LCC	Q64	PLD State Machine
5962-89546 02XX	CY7C330-40WMB	28.3 DIP	W22	PLD State Machine
5962-89546 02YX	CY7C330-40TMB	28 CP	T74	PLD State Machine
5962-89546 023X	CY7C330-40QMB	28 S LCC	Q64	PLD State Machine
5962-89546 03XX	CY7C330-50WMB	28.3 DIP	W22	PLD State Machine
5962-89546 03YX	CY7C330-50TMB	28 CP	T74	PLD State Machine
5962-89546 033X	CY7C330-50QMB	28 S LCC	Q64	PLD State Machine
5962-89598 34MTX	CY7C108-55FMB	32 FP	F75	128K x 8 SRAM
5962-89598 34MUX	CY7C108-55LMB	32 LCC	L55	128K x 8 SRAM
5962-89598 34MXX	CY7C108-55DMB	32.6 DIP	D20	128K x 8 SRAM
5962-89598 34MYX	CY7C108-55YMB	32 SOJ	Y65	128K x 8 SRAM
5962-89598 34MZX	CY7C109-55DMB	32.4 DIP	D44	128K x 8 SRAM
5962-89598 35MTX	CY7C108-45FMB	32 FP	F75	128K x 8 SRAM
5962-89598 35MUX	CY7C108-45LMB	32 LCC	L55	128K x 8 SRAM
5962-89598 35MXX	CY7C108-45DMB	32.6 DIP	D20	128K x 8 SRAM
5962-89598 35MYX	CY7C108-45YMB	32 SOJ	Y65	128K x 8 SRAM
5962-89598 35MZX	CY7C109-45DMB	32.4 DIP	D44	128K x 8 SRAM
5962-89598 36MTX	CY7C108-35FMB	32 FP	F75	128K x 8 SRAM
5962-89598 36MUX	CY7C108-35LMB	32 LCC	L55	128K x 8 SRAM
5962-89598 36MXX	CY7C108-35DMB	32.6 DIP	D20	128K x 8 SRAM
5962-89598 36MYX	CY7C108-35YMB	32 SOJ	Y65	128K x 8 SRAM
5962-89598 36MZX	CY7C109-35DMB	32.4 DIP	D44	128K x 8 SRAM
5962-89598 37MTX	CY7C108-25FMB	32 FP	F75	128K x 8 SRAM
5962-89598 37MUX	CY7C108-25LMB	32 LCC	L55	128K x 8 SRAM
5962-89598 37MXX	CY7C108-25DMB	32.6 DIP	D20	128K x 8 SRAM
5962-89598 37MYX	CY7C108-25YMB	32 SOJ	Y65	128K x 8 SRAM
5962-89598 37MZX	CY7C109-25DMB	32.4 DIP	D44	128K x 8 SRAM
5962-89661 01XX	CY7C409A-15DMB	28.3 DIP	D22	64 x 9 FIFO
5962-89661 01YX	CY7C409A-15KMB	28 CP	K74	64 x 9 FIFO
5962-89661 013X	CY7C409A-15LMB	28 S LCC	L64	64 x 9 FIFO
5962-89661 02XX	CY7C409A-25DMB	28.3 DIP	D22	64 x 9 FIFO
5962-89661 02YX	CY7C409A-25KMB	28 CP	K74	64 x 9 FIFO
5962-89661 023X	CY7C409A-25LMB	28 S LCC	L64	64 x 9 FIFO
5962-89664 01XX	CY7C408A-15DMB	28.3 DIP	D22	64 x 8 FIFO
5962-89664 01YX	CY7C408A-15KMB	28 CP	K74	64 x 8 FIFO
5962-89664 013X	CY7C408A-15LMB	28 S LCC	L64	64 x 8 FIFO
5962-89664 02XX	CY7C408A-25DMB	28.3 DIP	D22	64 x 8 FIFO
5962-89664 02YX	CY7C408A-25KMB	28 CP	K74	64 x 8 FIFO
5962-89664 023X	CY7C408A-25LMB	28 S LCC	L64	64 x 8 FIFO
5962-89690 01JX	CY6116A-25DMB	24.6 DIP	D12	2K x 8 SRAM
5962-89690 01KX	CY7C128A-25KMB	24 CP	K73	2K x 8 SRAM
5962-89690 01LX	CY7C128A-25DMB	24.3 DIP	D14	2K x 8 SRAM
5962-89690 01XX	CY6117A-25LMB	32 R LCC	L55	2K x 8 SRAM
5962-89690 01YX	CY7C128A-25LMB	24 R LCC	L53	2K x 8 SRAM
5962-89690 013X	CY6116A-25LMB	28 S LCC	L64	2K x 8 SRAM
5962-89690 02JX	CY6116A-20DMB	24.6 DIP	D12	2K x 8 SRAM
5962-89690 02KX	CY7C128A-20KMB	24 CP	K73	2K x 8 SRAM
5962-89690 02LX	CY7C128A-20DMB	24.3 DIP	D14	2K x 8 SRAM
5962-89690 02XX	CY6117A-20LMB	32 R LCC	L55	2K x 8 SRAM
5962-89690 02YX	CY7C128A-20LMB	24 R LCC	L53	2K x 8 SRAM
5962-89690 023X	CY6116A-20LMB	28 S LCC	L64	2K x 8 SRAM
5962-89691 02TX	CY7C185A-25KMB	28 CP	K74	8K x 8 SRAM
5962-89691 02UX	CY7C185A-25LMB	28 R TLCC	L54	8K x 8 SRAM
5962-89691 02XX	CY7C186A-25DMB	28.6 DIP	D16	8K x 8 SRAM
5962-89691 02ZX	CY7C185A-25DMB	28.3 DIP	D22	8K x 8 SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-89691 04TX	CY7C185A-20KMB	28 CP	K74	8K x 8 SRAM
5962-89691 04UX	CY7C185A-20LMB	28 R TLCC	L54	8K x 8 SRAM
5962-89691 04XX	CY7C186A-20DMB	28.6 DIP	D16	8K x 8 SRAM
5962-89691 04ZX	CY7C185A-20DMB	28.3 DIP	D22	8K x 8 SRAM
5962-89692 02KX	CY7C164A-25KMB	24 CP	K73	16K x 4 SRAM
5962-89692 02YX	CY7C164A-25DMB	22.3 DIP	D10	16K x 4 SRAM
5962-89692 02ZX	CY7C164A-25LMB	22 R LCC	L52	16K x 4 SRAM
5962-89692 04KX	CY7C164A-20KMB	24 CP	K73	16K x 4 SRAM
5962-89692 04YX	CY7C164A-20DMB	22.3 DIP	D10	16K x 4 SRAM
5962-89692 04ZX	CY7C164A-20LMB	22 R LCC	L52	16K x 4 SRAM
5962-89694 01EX	CY7C190-25DMB	16.3 DIP	D2	16 x 4 SRAM
5962-89694 01FX	CY7C190-25KMB	16 CP	K69	16 x 4 SRAM
5962-89694 01XX	CY7C190-25LMB	20 S LCC	L61	16 x 4 SRAM
5962-89712 01UX	CY7C162A-45LMB	28 R LCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 01XX	CY7C162A-45DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O
5962-89712 01YX	CY7C162A-45KMB	28 CP	K74	16K x 4 SRAM with Separate I/O
5962-89712 01ZX	CY7C162A-45LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 02UX	CY7C162A-35LMB	28 R LCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 02XX	CY7C162A-35DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O
5962-89712 02YX	CY7C162A-35KMB	28 CP	K74	16K x 4 SRAM with Separate I/O
5962-89712 02ZX	CY7C162A-35LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 03UX	CY7C162A-25LMB	28 R LCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 03XX	CY7C162A-25DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O
5962-89712 03YX	CY7C162A-25KMB	28 CP	K74	16K x 4 SRAM with Separate I/O
5962-89712 03ZX	CY7C162A-25LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 04UX	CY7C162A-20LMB	28 R LCC	L54	16K x 4 SRAM with Separate I/O
5962-89712 04XX	CY7C162A-20DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O
5962-89712 04YX	CY7C162A-20KMB	28 CP	K74	16K x 4 SRAM with Separate I/O
5962-89712 04ZX	CY7C162A-20LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O
5962-89790 02KX	CY7C172A-20KMB	24 CP	K73	4K x 4 SRAM with Separate I/O
5962-89790 02LX	CY7C172A-20DMB	24.3 DIP	D14	4K x 4 SRAM with Separate I/O
5962-89790 023X	CY7C172A-20LMB	28 S LCC	L64	4K x 4 SRAM with Separate I/O
5962-89815 01LX	CY7C245A-35WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962-89815 01KX	CY7C245A-35TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962-89815 013X	CY7C245A-35QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962-89815 02LX	CY7C245A-25WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962-89815 02KX	CY7C245A-25TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962-89815 023X	CY7C245A-25QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962-89815 03LX	CY7C245A-18WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962-89815 03KX	CY7C245A-18TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962-89815 033X	CY7C245A-18QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962-89817 01XX	CY7C271-55WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962-89817 01YX	CY7C271-55TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 01ZX	CY7C271-55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 02XX	CY7C271-45WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962-89817 02YX	CY7C271-45TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 02ZX	CY7C271-45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 03XX	CY7C271-35WMB	28.3 DIP	W22	32K x 8 UV EPROM
5962-89817 03YX	CY7C271-35TMB	28 CP	T74	32K x 8 UV EPROM
5962-89817 03ZX	CY7C271-35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 04UX	CY7C274-55WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 04ZX	CY7C274-55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 05UX	CY7C274-45WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 05ZX	CY7C274-45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89817 06UX	CY7C274-35WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962-89817 06ZX	CY7C274-35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962-89841 01KX	PALC22V10D-30KMB	24 CP	K73	CMOS EE PLD
5962-89841 01LX	PALC22V10D-30DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 013X	PALC22V10D-30LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 02KX	PALC22V10D-20KMB	24 CP	K73	CMOS EE PLD
5962-89841 02LX	PALC22V10D-20DMB	24.3 DIP	D14	CMOS EE PLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–89841 023X	PALC22V10D–20LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 03KX	PALC22V10D–15KMB	24 CP	K73	CMOS EE PLD
5962–89841 03LX	PALC22V10D–15DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 033X	PALC22V10D–15LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 04KX	PALC22V10D–25KMB	24 CP	K73	CMOS EE PLD
5962–89841 04LX	PALC22V10D–25DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 043X	PALC22V10D–25LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 05KX	PALC22V10D–15KMB	24 CP	K73	CMOS EE PLD
5962–89841 05LX	PALC22V10D–15DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 053X	PALC22V10D–15LMB	28 S LCC	L64	CMOS EE PLD
5962–89855 01MXX	CY7C331–40DMB	28.3 DIP	D22	Asynchronous PLD
5962–89855 01MYX	CY7C331–40KMB	28 CP	K74	Asynchronous PLD
5962–89855 01MZX	CY7C331–40YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 01M3X	CY7C331–40LMB	28 S LCC	L64	Asynchronous PLD
5962–89855 02MXX	CY7C331–30DMB	28.3 DIP	D22	Asynchronous PLD
5962–89855 02MYX	CY7C331–30KMB	28 CP	K74	Asynchronous PLD
5962–89855 02MZX	CY7C331–30YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 02M3X	CY7C331–30LMB	28 S LCC	L64	Asynchronous PLD
5962–89855 03MXX	CY7C331–25DMB	28.3 DIP	D22	Asynchronous PLD
5962–89855 03MYX	CY7C331–25KMB	28 CP	K74	Asynchronous PLD
5962–89855 03MZX	CY7C331–25YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 03M3X	CY7C331–25LMB	28 S LCC	L64	Asynchronous PLD
5962–89863 02UX	CY7C421–65KMB	28 CP	K74	512 x 9 FIFO
5962–89863 02XX	CY7C420–65DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 02YX	CY7C421–65DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 02ZX	CY7C421–65LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 03UX	CY7C421–50KMB	28 CP	K74	512 x 9 FIFO
5962–89863 03XX	CY7C420–50DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 03YX	CY7C421–50DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 03ZX	CY7C421–50LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 04UX	CY7C421–40KMB	28 CP	K74	512 x 9 FIFO
5962–89863 04XX	CY7C420–40DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 04YX	CY7C421–40DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 04ZX	CY7C421–40LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 05UX	CY7C421–30KMB	28 CP	K74	512 x 9 FIFO
5962–89863 05XX	CY7C420–30DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 05YX	CY7C421–30DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 05ZX	CY7C421–30LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 06UX	CY7C421–25KMB	28 CP	K74	512 x 9 FIFO
5962–89863 06XX	CY7C420–25DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 06YX	CY7C421–25DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 06ZX	CY7C421–25LMB	32 R LCC	L55	512 x 9 FIFO
5962–89892 02KX	CY7C166A–25KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–89892 02LX	CY7C166A–25DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–89892 02XX	CY7C166A–25LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–89892 02YX	CY7C166A–25LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–89892 04KX	CY7C166A–20KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–89892 04LX	CY7C166A–20DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–89892 04XX	CY7C166A–20LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–89892 04YX	CY7C166A–20LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–89935 01XX	CY7C192–45DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 01YX	CY7C192–45KMB	28 CP	K74	64K x 4 SRAM with Separate I/O
5962–89935 01ZX	CY7C192–45LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89935 02XX	CY7C192–35DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 02YX	CY7C192–35KMB	28 CP	K74	64K x 4 SRAM with Separate I/O
5962–89935 02ZX	CY7C192–35LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89935 03XX	CY7C192–25DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 03YX	CY7C192–25KMB	28 CP	K74	64K x 4 SRAM with Separate I/O
5962–89935 03ZX	CY7C192–25LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89967 01MXX	CY7C265–60DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962–89967 01MYX	CY7C265–60KMB	28 CP	K74	8K x 8 Registered OTP PROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-89967 01M3X	CY7C265-60LMB	28 S LCC	L64	8K x 8 Registered OTP PROM
5962-89967 02MXX	CY7C265-50DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962-89967 02MYX	CY7C265-50KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962-89967 02M3X	CY7C265-50LMB	28 S LCC	L64	8K x 8 Registered OTP PROM
5962-89967 03MXX	CY7C265-25DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962-89967 03MYX	CY7C265-25KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962-89967 03M3X	CY7C265-25LMB	28 S LCC	L64	8K x 8 Registered OTP PROM
5962-89967 04MXX	CY7C265-18DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962-89967 04MYX	CY7C265-18KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962-89967 04M3X	CY7C265-18LMB	28 S LCC	L64	8K x 8 Registered OTP PROM
5962-90555 01KX	PLDC20RA10-35KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962-90555 01LX	PLDC20RA10-35DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90555 013X	PLDC20RA10-35LMB	28 S LCC	L64	Asynchronous CMOS OTP PLD
5962-90555 02KX	PLDC20RA10-25KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962-90555 02LX	PLDC20RA10-25DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90555 023X	PLDC20RA10-25LMB	28 S LCC	L64	Asynchronous CMOS OTP PLD
5962-90555 03KX	PLDC20RA10-20KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962-90555 03LX	PLDC20RA10-20DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90555 033X	PLDC20RA10-20LMB	28 S LCC	L64	Asynchronous CMOS OTP PLD
5962-90594 01XX	CY7C161A-45DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962-90594 01YX	CY7C161A-45KMB	28 CP	K74	16K x 4 SRAM with Separate I/O, TW
5962-90594 01ZX	CY7C161A-45LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O, TW
5962-90594 02XX	CY7C161A-35DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962-90594 02YX	CY7C161A-35KMB	28 CP	K74	16K x 4 SRAM with Separate I/O, TW
5962-90594 02ZX	CY7C161A-35LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O, TW
5962-90594 03XX	CY7C161A-25DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962-90594 03YX	CY7C161A-25KMB	28 CP	K74	16K x 4 SRAM with Separate I/O, TW
5962-90594 03ZX	CY7C161A-25LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O, TW
5962-90594 04XX	CY7C161A-20DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962-90594 04YX	CY7C161A-20KMB	28 CP	K74	16K x 4 SRAM with Separate I/O, TW
5962-90594 04ZX	CY7C161A-20LMB	28 R TLCC	L54	16K x 4 SRAM with Separate I/O, TW
5962-90611 01XX	CY7C344-35WMB	28.3 DIP	W22	32-Macrocell UV EPLD
5962-90611 01YX	CY7C344-35HMB	28 S JCQ	H64	32-Macrocell UV EPLD
5962-90611 02XX	CY7C344-25WMB	28.3 DIP	W22	32-Macrocell UV EPLD
5962-90611 02YX	CY7C344-25HMB	28 S JCQ	H64	32-Macrocell UV EPLD
5962-90620 01MUX	CY7C132-55FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 01MZX	CY7C132-55LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 01MYX	CY7C132-55DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 02MUX	CY7C132-45FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 02MZX	CY7C132-45LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 02MYX	CY7C132-45DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 03MUX	CY7C132-35FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 03MZX	CY7C132-35LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 03MYX	CY7C132-35DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 04MUX	CY7C142-55FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 04MZX	CY7C142-55LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 04MYX	CY7C142-55DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 05MUX	CY7C142-45FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 05MZX	CY7C142-45LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 05MYX	CY7C142-45DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 06MUX	CY7C142-35FMB	48 Q FP	F78	2K x 8 Dual-Port SRAM
5962-90620 06MZX	CY7C142-35LMB	48 LCC	L68	2K x 8 Dual-Port SRAM
5962-90620 06MYX	CY7C142-35DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962-90620 07MXX	CY7C136-55LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962-90620 08MXX	CY7C136-45LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962-90620 09MXX	CY7C136-35LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962-90620 10MXX	CY7C146-55LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962-90620 11MXX	CY7C146-45LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962-90620 12MXX	CY7C146-35LMB	52 LCC	L69	2K x 8 Dual-Port SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–90644 01XX	CY7C191–45DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 01YX	CY7C191–45KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 01ZX	CY7C191–45LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90644 02XX	CY7C191–35DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 02YX	CY7C191–35KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 02ZX	CY7C191–35LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90644 03XX	CY7C191–25DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 03YX	CY7C191–25KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 03ZX	CY7C191–25LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90696 01MKX	CY7C123–15KMB	24 CP	K73	256 x 4 SRAM with Separate I/O
5962–90696 01MLX	CY7C123–15DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90696 01MXX	CY7C123–15LMB	24 R LCC	L53	256 x 4 SRAM with Separate I/O
5962–90696 02MKX	CY7C123–12KMB	24 CP	K73	256 x 4 SRAM with Separate I/O
5962–90696 02MLX	CY7C123–12DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90696 02MXX	CY7C123–12LMB	24 R LCC	L53	256 x 4 SRAM with Separate I/O
5962–90696 03MKX	CY7C123–10KMB	24 CP	K73	256 x 4 SRAM with Separate I/O
5962–90696 03MLX	CY7C123–10DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90696 03MXX	CY7C123–10LMB	24 R LCC	L53	256 x 4 SRAM with Separate I/O
5962–90715 03MUX	CY7C433–65DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 03MXX	CY7C432–65DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 03MYX	CY7C433–65KMB	28 CP	K74	4K x 9 FIFO
5962–90715 03MZX	CY7C433–65LMB	32 R LCC	L55	4K x 9 FIFO
5962–90715 04MUX	CY7C433–50DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 04MXX	CY7C432–50DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 04MYX	CY7C433–50KMB	28 CP	K74	4K x 9 FIFO
5962–90715 04MZX	CY7C433–50LMB	32 R LCC	L55	4K x 9 FIFO
5962–90715 05MUX	CY7C433–40DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 05MXX	CY7C432–40DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 05MYX	CY7C433–40KMB	28 CP	K74	4K x 9 FIFO
5962–90715 05MZX	CY7C433–40LMB	32 R LCC	L55	4K x 9 FIFO
5962–90715 06MUX	CY7C433–30DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 06MXX	CY7C432–30DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 06MYX	CY7C433–30KMB	28 CP	K74	4K x 9 FIFO
5962–90715 06MZX	CY7C433–30LMB	32 R LCC	L55	4K x 9 FIFO
5962–90754 01MXX	CY7C331–40WMB	28.3 DIP	W22	Asynchronous UV PLD
5962–90754 01MYX	CY7C331–40TMB	28 CP	T74	Asynchronous UV PLD
5962–90754 01MZX	CY7C331–40HMB	28 S JCQ	H64	Asynchronous UV PLD
5962–90754 01M3X	CY7C331–40QMB	28 S LCC	Q64	Asynchronous UV PLD
5962–90754 02MXX	CY7C331–30WMB	28.3 DIP	W22	Asynchronous UV PLD
5962–90754 02MYX	CY7C331–30TMB	28 CP	T74	Asynchronous UV PLD
5962–90754 02MZX	CY7C331–30HMB	28 S JCQ	H64	Asynchronous UV PLD
5962–90754 02M3X	CY7C331–30QMB	28 S LCC	Q64	Asynchronous UV PLD
5962–90754 03MXX	CY7C331–25WMB	28.3 DIP	W22	Asynchronous UV PLD
5962–90754 03MYX	CY7C331–25TMB	28 CP	T74	Asynchronous UV PLD
5962–90754 03MZX	CY7C331–25HMB	28 S JCQ	H64	Asynchronous UV PLD
5962–90754 03M3X	CY7C331–25QMB	28 S LCC	Q64	Asynchronous UV PLD
5962–90803 01MKX	CY7C261–55KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 01MLX	CY7C261–55DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 01M3X	CY7C261–55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 02MKX	CY7C261–45KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 02MLX	CY7C261–45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 02M3X	CY7C261–45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 03MKX	CY7C261–35KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 03MLX	CY7C261–35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 03M3X	CY7C261–35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 04MKX	CY7C261–25KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 04MLX	CY7C261–25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 04M3X	CY7C261–25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 05MJX	CY7C264–55DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962–90803 05MKX	CY7C263–55KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 05MLX	CY7C263–55DMB	24.3 DIP	D14	8K x 8 OTP PROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–90803 05M3X	CY7C263–55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 06MJX	CY7C264–45DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962–90803 06MKX	CY7C263–45KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 06MLX	CY7C263–45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 06M3X	CY7C263–45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 07MJX	CY7C264–35DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962–90803 07MKX	CY7C263–35KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 07MLX	CY7C263–35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 07M3X	CY7C263–35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90803 08MJX	CY7C264–25DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962–90803 08MKX	CY7C263–25KMB	24 CP	K73	8K x 8 OTP PROM
5962–90803 08MLX	CY7C263–25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962–90803 08M3X	CY7C263–25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962–90913 01MXX	CY7C287–65WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962–90913 01MYX	CY7C287–65QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962–90913 02MXX	CY7C287–55WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962–90913 02MYX	CY7C287–55QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962–91518 01MXX	CY10E474L–7DMB	24.4	D40	1K x 4 ECL SRAM
5962–91518 01MYX	CY10E474L–7YMB	28 J LCC	Y64	1K x 4 ECL SRAM
5962–91518 01MZX	CY10E474L–7KMB	24 CP	K63	1K x 4 ECL SRAM
5962–91518 02MXX	CY10E474L–5DMB	24.4	D40	1K x 4 ECL SRAM
5962–91518 02MYX	CY10E474L–5YMB	28 J LCC	Y64	1K x 4 ECL SRAM
5962–91518 02MZX	CY10E474L–5KMB	24 CP	K63	1K x 4 ECL SRAM
5962–91568 01MRX	PLDC18G8–20DMB	20.3 DIP	D6	20-Pin Generic PLD
5962–91568 01MSX	PLDC18G8–20KMB	20 CP	K71	20-Pin Generic PLD
5962–91568 01MXX	PLDC18G8–20LMB	20 S LCC	L61	20-Pin Generic PLD
5962–91568 02MRX	PLDC18G8–15DMB	20.3 DIP	D6	20-Pin Generic PLD
5962–91568 02MSX	PLDC18G8–15KMB	20 CP	K71	20-Pin Generic PLD
5962–91568 02MXX	PLDC18G8–15LMB	20 S LCC	L61	20-Pin Generic PLD
5962–91584 01MXX	CY7C332–25WMB	28.3 DIP	W22	Registered Combinatorial UV EPLD
5962–91584 01MYX	CY7C332–25TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962–91584 01MZX	CY7C332–25HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962–91584 01M3X	CY7C332–25QMB	28 S LCC	Q64	Registered Combinatorial UV EPLD
5962–91584 02MXX	CY7C332–20WMB	28.3 DIP	W22	Registered Combinatorial UV EPLD
5962–91584 02MYX	CY7C332–20TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962–91584 02MZX	CY7C332–20HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962–91584 02M3X	CY7C332–20QMB	28 S LCC	Q64	Registered Combinatorial UV EPLD
5962–91593 01MKX	CY7B164–15KMB	24 CP	K73	16K x 4 SRAM
5962–91593 01MYX	CY7B164–15DMB	22.3 DIP	D10	16K x 4 SRAM
5962–91593 01MZX	CY7B164–15LMB	22 R LCC	L52	16K x 4 SRAM
5962–91593 02MKX	CY7B164–12KMB	24 CP	K73	16K x 4 SRAM
5962–91593 02MYX	CY7B164–12DMB	22.3 DIP	D10	16K x 4 SRAM
5962–91593 02MZX	CY7B164–12LMB	22 R LCC	L52	16K x 4 SRAM
5962–91593 03MKX	CY7B164–10KMB	24 CP	K73	16K x 4 SRAM
5962–91593 03MYX	CY7B164–10DMB	22.3 DIP	D10	16K x 4 SRAM
5962–91593 03MZX	CY7B164–10LMB	22 R LCC	L52	16K x 4 SRAM
5962–91593 04MKX	CY7B166–15KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–91593 04MYX	CY7B166–15DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–91593 04MZX	CY7B166–15LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–91593 05MKX	CY7B166–12KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–91593 05MYX	CY7B166–12DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–91593 05MZX	CY7B166–12LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–91593 06MKX	CY7B166–10KMB	24 CP	K73	16K x 4 SRAM w/OE
5962–91593 06MYX	CY7B166–10DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–91593 06MZX	CY7B166–10LMB	28 R LCC	L54	16K x 4 SRAM w/OE
5962–91744 01MXX	CY7C277–50WMB	28.3 DIP	W22	32K x 8 Registered UV PROM
5962–91744 01MYX	CY7C277–50QMB	32 R LCC	Q55	32K x 8 Registered UV PROM
5962–91744 01MZX	CY7C277–50TMB	28 CP	T74	32K x 8 Registered UV PROM
5962–91744 02MXX	CY7C277–40WMB	28.3 DIP	W22	32K x 8 Registered UV PROM
5962–91744 02MYX	CY7C277–40QMB	32 R LCC	Q55	32K x 8 Registered UV PROM
5962–91744 02MZX	CY7C277–40TMB	28 CP	T74	32K x 8 Registered UV PROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-91760 01M3X	PAL22V10C-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 02M3X	PAL22V10C-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 03M3X	PAL22V10C-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 04M3X	PAL22VP10C-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 05M3X	PAL22VP10C-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 06M3X	PAL22VP10C-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-92009 01MXC	VACO68A-GMB	145 PGA	G145	VME Address Controller
5962-92009 01MYC	VACO68A-UMB	160 FP	U162	VME Address Controller
5962-92010 01MXC	VICO68A-GMB	145 PGA	G145	VME Interface Controller
5962-92010 01MYC	VICO68A-UMB	160 FP	U162	VME Interface Controller
5962-92155 01MXX	CY7C277-50DMB	28.3 DIP	D22	32K x 8 Registered OTP PROM
5962-92155 01MYX	CY7C277-50LMB	32 R LCC	L55	32K x 8 Registered OTP PROM
5962-92155 01MZX	CY7C277-50KMB	28 CP	K74	32K x 8 Registered OTP PROM
5962-92155 02MXX	CY7C277-40DMB	28.3 DIP	D22	32K x 8 Registered OTP PROM
5962-92155 02MYX	CY7C277-40LMB	32 R LCC	L55	32K x 8 Registered OTP PROM
5962-92155 02MZX	CY7C277-40KMB	28 CP	K74	32K x 8 Registered OTP PROM
5962-92158 01MXX	CY7C343-40HMB	44 S JCQ	H67	64-Macrocell UV EPLD
5962-92158 02MXX	CY7C343-30HMB	44 S JCQ	H67	64-Macrocell UV EPLD
5962-92321 01MXX	CY7C439-65DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962-92321 01MYX	CY7C439-65KMB	28 CP	K74	2K x 9 BiFIFO
5962-92321 01MZX	CY7C439-65LMB	32 R LCC	L55	2K x 9 BiFIFO
5962-92321 02MXX	CY7C439-40DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962-92321 02MYX	CY7C439-40KMB	28 CP	K74	2K x 9 BiFIFO
5962-92321 02MZX	CY7C439-40LMB	32 R LCC	L55	2K x 9 BiFIFO
5962-92321 03MXX	CY7C439-30DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962-92321 03MYX	CY7C439-30KMB	28 CP	K74	2K x 9 BiFIFO
5962-92321 03MZX	CY7C439-30LMB	32 R LCC	L55	2K x 9 BiFIFO
5962-92338 01MRX	PAL16L8-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 01MSX	PAL16L8-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 01MXX	PAL16L8-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 02MRX	PAL16R8-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 02MSX	PAL16R8-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 02MXX	PAL16R8-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 03MRX	PAL16R6-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 03MSX	PAL16R6-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 03MXX	PAL16R6-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 04MRX	PAL16R4-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 04MSX	PAL16R4-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 04MXX	PAL16R4-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 05MRX	PAL16L8-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 05MSX	PAL16L8-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 05MXX	PAL16L8-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 06MRX	PAL16R8-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 06MSX	PAL16R8-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 06MXX	PAL16R8-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 07MRX	PAL16R6-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 07MSX	PAL16R6-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 07MXX	PAL16R6-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 08MRX	PAL16R4-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 08MSX	PAL16R4-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 08MXX	PAL16R4-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-93122 01MXX	CY7C258-15WMB	28.3 DIP	W22	2K x 8 State Machine UV PROM
5962-93122 01MYX	CY7C258-15HMB	28 S JLCC	H64	2K x 8 State Machine UV PROM
5962-93122 01M3X	CY7C258-15QMB	28 S LCC	Q64	2K x 8 State Machine UV PROM
5962-93122 02MXX	CY7C258-12WMB	28.3 DIP	W22	2K x 8 State Machine UV PROM
5962-93122 02MYX	CY7C258-12HMB	28 S JLCC	H64	2K x 8 State Machine UV PROM
5962-93122 02M3X	CY7C258-12QMB	28 S LCC	Q64	2K x 8 State Machine UV PROM
5962-93122 03MUX	CY7C259-15QMB	44 S LCC	Q67	2K x 8 State Machine UV PROM
5962-93122 03MZX	CY7C259-15HMB	44 S JLCC	H67	2K x 8 State Machine UV PROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-93122 04MUX	CY7C259-12QMB	44 S LCC	Q67	2K x 8 State Machine UV PROM
5962-93122 04MZX	CY7C259-12HMB	44 S JLCC	H67	2K x 8 State Machine UV PROM
5962-93123 01MXX	CY7C258-15DMB	28.3 DIP	D22	2K x 8 State Machine PROM
5962-93123 01MYX	CY7C258-15YMB	28 S JLCC	Y64	2K x 8 State Machine PROM
5962-93123 01M3X	CY7C258-15LMB	28 S LCC	L64	2K x 8 State Machine PROM
5962-93123 02MXX	CY7C258-12DMB	28.3 DIP	D22	2K x 8 State Machine PROM
5962-93123 02MYX	CY7C258-12YMB	28 S JLCC	Y64	2K x 8 State Machine PROM
5962-93123 02M3X	CY7C258-12LMB	28 S LCC	L64	2K x 8 State Machine PROM
5962-93123 03MUX	CY7C259-15LMB	44 S LCC	L67	2K x 8 State Machine PROM
5962-93123 03MZX	CY7C259-15YMB	44 S JLCC	Y67	2K x 8 State Machine PROM
5962-93123 04MUX	CY7C259-12LMB	44 S LCC	L67	2K x 8 State Machine PROM
5962-93123 04MZX	CY7C259-12YMB	44 S JLCC	Y67	2K x 8 State Machine PROM
5962-93166 01MXX	CY7C271-55DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 01MYX	CY7C271-55KMB	28 CP	K74	32K x 8 OTP PROM
5962-93166 01MZX	CY7C271-55LMB	32 R LCC	L55	32K x 8 OTP PROM
5962-93166 02MXX	CY7C271-45DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 02MYX	CY7C271-45KMB	28 CP	K74	32K x 8 OTP PROM
5962-93166 02MZX	CY7C271-45LMB	32 R LCC	L55	32K x 8 OTP PROM
5962-93166 03MXX	CY7C271-35DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 03MYX	CY7C271-35KMB	28 CP	K74	32K x 8 OTP PROM
5962-93166 03MZX	CY7C271-35LMB	32 R LCC	L55	32K x 8 OTP PROM
5962-93166 04MUX	CY7C274-55DMB	28.6 DIP	D16	32K x 8 OTP PROM
5962-93166 04MZX	CY7C274-55LMB	32 R LCC	L55	32K x 8 OTP PROM
5962-93166 05MUX	CY7C274-45DMB	28.6 DIP	D16	32K x 8 OTP PROM
5962-93166 05MZX	CY7C274-45LMB	32 R LCC	L55	32K x 8 OTP PROM
5962-93166 06MUX	CY7C274-35DMB	28.6 DIP	D16	32K x 8 OTP PROM
5962-93166 06MZX	CY7C274-35LMB	32 R LCC	L55	32K x 8 OTP PROM

Notes:

1. Devices listed have been approved by DESC for the SMD indicated as of the date of publication. Contact your local Cypress representative, or the Cypress SMD Hotline at 408/943-2716, for the latest update.
2. Use the SMD part number as the ordering code.
3. Package: 24.3 DIP = 24-pin 0.300″ DIP;
   24.6 DIP = 24-pin 0.600″ DIP;
   28 R LCC = 28 terminal rectangular LCC,
   S = Square LCC, TLCC = Thin LCC
   24 CP = 24-pin ceramic flatpack (Configuration 1);
   FP = brazed flatpack;
   PGA = Pin Grid Array.

SMD Hotline: 408/943-2716

JAN M38510 Qualifications

JAN Number	Cypress[2] Part Number	Package[3]		Product Description	Qualification Status
		Description	Type		
JM 38510/28901BVA	CY7C147–35DMB	18.3 DIP	D4	4K x 1 SRAM	Qualified
JM 38510/28901BYA	CY7C147–35KMB	18 CP	K70	4K x 1 SRAM	Qualified
JM 38510/28903BVA	CY2147–55DMB	18.3 DIP	D4	4K x 1 SRAM	Qualified
JM 38510/28903BYA	CY2147–55KMB	18 CP	K70	4K x 1 SRAM	Qualified
JM 38510/28902BVA	CY7C148–35DMB	18.3 DIP	D4	1K x 4 SRAM	Qualified
JM 38510/28902BYA	CY7C148–35KMB	18 CP	K70	1K x 4 SRAM	Qualified
JM 38510/28904BVA	CY2148–55DMB	18.3 DIP	D4	1K x 4 SRAM	Qualified
JM 38510/28904BYA	CY2148–55KMB	18 CP	K70	1K x 4 SRAM	Qualified
JM 38510/50701BLA	PALC22V10B–30WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50701BKA	PALC22V10B–30TMB	24 CP	T73	CMOS UV PLD	Qualified
JM 38510/50701B3A	PALC22V10B–30QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50702BLA	PALC22V10B–25WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50702BKA	PALC22V10B–25TMB	24 CP	T73	CMOS UV PLD	Qualified
JM 38510/50702B3A	PALC22V10B–25QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50703BLA	PALC22V10B–20WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50703BKA	PALC22V10B–20TMB	24 CP	T73	CMOS UV PLD	Qualified
JM 38510/50703B3A	PALC22V10B–20QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50704BLA	PALC22V10B–15WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50704BKA	PALC22V10B–15TMB	24 CP	T73	CMOS UV PLD	Qualified
JM 38510/50704B3A	PALC22V10B–15QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50801BLA	PALC22V10B–30DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50801BKA	PALC22V10B–30KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50801B3A	PALC22V10B–30LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50802BLA	PALC22V10B–25DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50802BKA	PALC22V10B–25KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50802B3A	PALC22V10B–25LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50803BLA	PALC22V10B–20DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50803BKA	PALC22V10B–20KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50803B3A	PALC22V10B–20LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50804BLA	PALC22V10B–15DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50804BKA	PALC22V10B–15KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50804B3A	PALC22V10B–15LMB	28 S LCC	L64	CMOS PLD	Qualified

SMD Ordering Information

5962–XXXXX 01 _ L X

LEAD FINISH
- A = Solder Dip
- B = Tin Plate
- C = Gold
- X = Don't Care (The letter "X" will not be marked on the device, but will be replaced with the actual lead finish designation.)

PACKAGE TYPE (Not a complete list)

V =	18-pin 0.300 DIP	J =	24-pin 0.600 DIP
R =	20-pin 0.300 DIP	Q =	40-pin 0.600 DIP
S =	20-pin Cerpack	K =	24-pin Cerpack
W =	22-pin 0.400 DIP	2 =	20-pin SQ LCC
L =	24-pin 0.300 DIP	3 =	28-pin SQ LCC

X, Y, Z, U, T, M, N and 4, 5, 6, 7, 8, 9 = Non-dedicated package designations and will vary per drawing.

DEVICE CLASS DESIGNATOR
- No character = Old (Pre March 1990) SMD
- M = New "One Part—One Part Number" System SMD, Class B

DEVICE TYPE

DRAWING NUMBER

DRAWING PREFIX
5962 = Federal Stock Class (FSC) for microcircuits. Pre-1985 drawings do not have this prefix.

Cypress Military Marking Information

Manufacturer's identification:

Cypress Logo, CYPRESS, CYP, and CY are trademarks of Cypress Semiconductor Corporation.

Manufacturer's designating symbol or CAGE CODE:

Designating symbol = CETK or ETK

CAGE CODE/FSCM Number = 65786

Country of origin:

USA = United States of America

THA = Thailand

In general, the codes for all products (except modules) follow the format below.

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	−20 DMB	PAL 20
PAL C	22V10	−15 WMB	PAL 24 VARIABLE PRODUCT TERMS
PLD C	20G10	−20 WMB	GENERIC PLD 24
CY	7C330	−50 DMB	PLD SYNCHRONOUS STATE MACHINE
CY	10E302	−4 DMB	10K ECL PLD

RAM, PROM, FIFO, µP, ECL

PREFIX	DEVICE	SUFFIX	FAMILY
CY	7C128A	−35 D M B	CMOS SRAM
CY	7B185	−10 D M B	BiCMOS SRAM
CY	7C245A	−18 W M B	PROM
CY	7C404	−10 D M B	FIFO
CY	7C901	−27 D M B	µP
CY	10E422L	−5 D M B	10K ECL SRAM

B = BiCMOS
C = CMOS

PROCESSING
B = HI REL MIL STD 883D FOR MILITARY PRODUCT
= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT

TEMPERATURE RANGE
M = MILITARY (−55°C TO +125°C)

PACKAGE
D = CERDIP
F = FLATPAK
G = PIN GRID ARRAY (PGA)
H = WINDOWED LEADED CHIP CARRIER
K = CERPAK (GLASS-SEALED FLAT PACKAGE)
L = LEADLESS CHIP CARRIER
Q = WINDOWED LEADLESS CHIP CARRIER
R = WINDOWED PGA
T = WINDOWED CERPAK
U = CERAMIC QUAD FLATPACK
W = WINDOWED CERDIP
X = DICE (WAFFLE PACK)
Y = CERAMIC LEADED CHIP CARRIER

SPEED (ns or MHz)

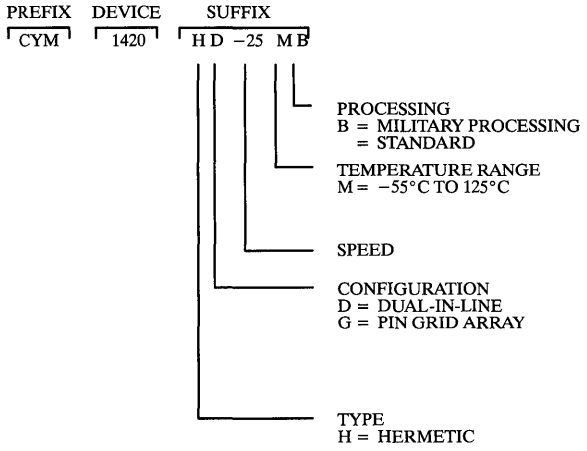
L = LOW-POWER OPTION
A, B, C = REVISION LEVEL

e.g., CY7C128A−35DMB, PALC16R8−20DMB

Cypress FSCM #65786

Military Ordering Information

The codes for module products follow the the format below.



Cypress FSCM #65786

CYPRESS SEMICONDUCTOR

Section Contents

Design and Programming Tools

CYPRESS SEMICONDUCTOR

Warp2 VHDL Compiler for PLDs

Features

- **VHDL (IEEE 1076) high-level language compiler**
  - **— VHDL facilitates device independent design**
  - **— VHDL designs are portable across multiple devices and/or CAD platforms**
  - **— VHDL facilitates the use of industry-standard simulation and synthesis tools for board and system-level design**
  - **— VHDL supports functions and libraries facilitating modular design activity**
- ***Warp2* provides synthesis for a powerful subset of IEEE standard VHDL including:**
  - **— enumerated types**
  - **— opeartor overloading**
  - **— for . . . generate statements**
  - **— integers**
- **State-of-the-art optimizations and reduction algorithms**
  - **— Optimization for flip-flop type (D type/T type)**
  - **— Automatic selection of optimal flip-flop type (D type/T type)**
  - **— Automatic pin assignment**
  - **— Automatic state assignment (grey code, one-hot, binary)**
- **Several design entry methods support multiple levels of abstraction:**
  - **— VHDL Behavioral (IE..THEN...ELSE; CASE...)**
  - **— State tables**
  - **— Boolean**
  - **— VHDL Standard (RTL)**
- **Designs can intermix multipleVHDL entry methods in a single design**
- **Supports all Cypress PLDs, PROMs, and FPGAs including MAX5000, the state machine PROMs (CY7C258/9), FLASH370, and pASIC380.**
- **Functional simulation provided with PLD ToolKit™:**
  - **— Graphical waveform simulator**
  - **— Entry and modification of on-screen waveforms**
  - **— Ability to probe internal nodes**
  - **— Displays inputs, outputs, and High Z signals in different colors**
  - **— Automatic clock and pulse creation**
  - **— Includes waveform to JEDEC test vector conversion utility**
  - **— Provides JEDEC to symbolic disassembly**
- **Hosted on IBM PC-AT**
- **DOS or Windows compatible on PCs**
- **OpenLook or Motif on Sun workstations**

Functional Description

Warp2™ is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design engineer. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map or POF file for the desired device (see *Figure 1*). For simulation, *Warp2* provides the graphical waveform simulator from the PLD ToolKit.

VHDL Compiler

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense and supported by every major vendor of CAE tools. VHDL allows designers to learn a single language that is useful for all facets of the design process.

VHDL offers designers the ability to describe designs at different levels of abstraction. At the highest level, designs can be entered as a description of their behavior. This behavioral description is not tied to any specific target device. As a result, simulation can be done very early in the design to verify correct functionality, which significantly speeds the design process.

Warp2's VHDL syntax also includes support for intermediate level entry modes such as state table and boolean entry. At the lowest level, designs can be described using gate-level RTL (Register Transfer Language). *Warp2* gives the designer the flexibility to intermix all of these entry modes.

In addition, VHDL allows you to design hierarchically, building up entities in terms of other entities. This allows you to work either "top-down" (designing the highest levels of the system and its interfaces first, then progressing to greater and greater detail) or "bottom-up" (designing elementary building blocks of the system,

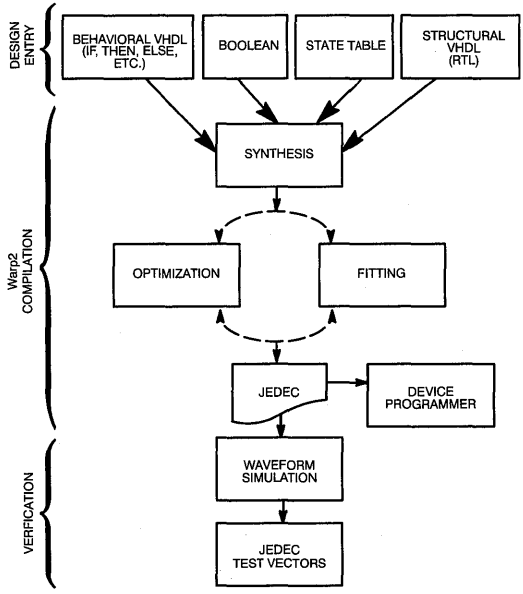


Figure 1. *Warp2* Design Flow

then combining these to build larger and larger parts) with equal ease.

Because VHDL is an IEEE standard, multiple vendors offer tools for design entry, simulation at both high and low levels, and synthesis of designs to different silicon targets. The use of device independent behavioral design entry gives users the freedom to retarget designs to different devices. The wide availability of VHDL tools provides complete vendor independence as well. Designers can begin their project using *Warp2* for Cypress PLDs and convert to high-volume gate arrays using the same VHDL behavioral description with industry-standard synthesis tools.

While design portability and device independence are significant benefits, VHDL has other advantages. The VHDL language allows users to define their own functions. User-defined functions allow users to extend the capabilities of the language and build reusable libraries of tested routines. As a result the user can produce complex designs faster than with ordinary "flat" languages. VHDL also provides control over the timing of events or processes. VHDL has constructs that identify processes as either sequential, concurrent, or a combination of both. This is essential when describing the interaction of complex state machines.

Cypress chose to offer tools that use the VHDL language because of the language's universal acceptance, the ability to do both device and vendor independent design, simulation capabilities at both the chip and system level that improve design efficiency, the wide availability of industry-standard tools with VHDL support for both simulation and synthesis, and the inherent power of the language's syntax.

VHDL is a rich programming language. Its flexibility reflects the nature of modern digital systems and allows designers to create accurate models of digital designs. Because of its depth and completeness, it is easier to describe a complex hardware system accurately in VHDL than in any other hardware description language. In addition, models created in VHDL can readily be transported to other CAD systems. *Warp2* supports a rich subset of VHDL including loops, for...generate statements, full hierarchical designs with packages, as well as synthesis for enumerated types and integers.

Designing with *Warp2*

Design Entry

Warp2 descriptions specify

1. The behavior or structure of a design, and
2. The mapping of signals in a design to the pins of a PLD

The part of a *Warp2* description that specifies the mapping of signals from the design to the pins of a PLD is called a binding architecture. It takes signal names from the design and matches them up with pin names from the PLD's entry in a library.

The part of a *Warp2* description that specifies the behavior or structure of the design is called an entity/architecture pair. Entity/architecture pairs, as their name implies, can be divided into two parts: an entity declaration, which declares the design's interface signals (i.e., tells the world what external signals the design has, and what their directions and types are), and a design architecture, which describes the design's behavior or structure.

Some users prefer to put the binding architecture for a design in one file, and the entity/architecture pair containing the design's behavioral or structural description in a different file. This allows you to isolate the device-dependent pin mapping in one file (the one containing the binding architecture), while leaving the device-independent behavioral or structural description in another (the one containing the entity/architecture pair). *Warp2* makes it easy to do this, offering separate analysis of files and easy reference to previously analyzed files by means of the USE clause.

Design Entity

If the entity/architecture pair is kept in a separate file, that file is usually referred to as the design entity file. The entity portion of a design entity file is a declaration of what a design presents to the outside world (the interface). For each external signal, the entity declaration specifies a signal name, a direction and a data type. In addition, the entity declaration specifies a name by which the entity can be referenced in a design architecture. In this section are code segments from four sample design entity files. The top portion of each example features the entity declaration.

Behavioral Description

The architecture portion of a design entity file specifies the function of the design. As shown in *Figure 1*, multiple design-entry methods are supported in *Warp2*. A behavioral description in VHDL often includes well known constructs such as If...Then...Else, and Case statements. Here is a code segment from a simple state machine design (soda vending machine) that uses behavioral VHDL to implement the design:

```
ENTITY drink IS
  PORT (nickel,dime,quarter,clock:in bit;
    returnDime,returnNickel,giveDrink:outbit);
END drink;


ARCHITECTURE fsm OF drink IS

TYPE drinkState IS (zero,five,ten,fif-
teen,twenty,twentyfive,owedime);
SIGNAL drinkstatus:drinkState;
ATTRIBUTE FSM_synthesis OF drinkStatus:signal
is sequential;


BEGIN

PROCESS BEGIN

 WAIT UNTIL clock = '1';

  giveDrink <= '0';
  returnDime <= '0';
  returnNickel <= '0';

  CASE drinkStatus IS

  WHEN zero =>
    IF (nickel = '1') THEN
      drinkStatus <= drinkStatus'SUCC(drink-
Status);
        -- goto Five
    ELSIF (dime = '1') THEN
      drinkStatus <= Ten;
    ELSIF (quarter = '1') THEN
      drinkStatus <= TwentyFive;
    ENDIF;
  WHEN Five =>
    IF (nickel = '1') THEN
      drinkStatus <= Ten;
    ELSIF (dime = '1') THEN
      drinkStatus <= Fifteen;
    ELSIF (quarter = '1') THEN
```

```
      giveDrink <= '1';
      drinkStatus <= drinkStatus'PRED(drink-
Status);
        -- goto Zero
    ENDIF;

  WHEN oweDime =>
    returnDime <= '1';
    drinkStatus <= zero;

  when others =>
  -- This ELSE makes sure that the state
  -- machine resets itself if
  -- it somehow gets into an undefined state.
    drinkStatus <= zero;
  END CASE;
  END PROCESS;

END FSM;
```

VHDL is a highly typed language. It comes with several predefined operators, such as + and /= (add, not-equal-to). VHDL offers the capability of defining multiple meanings for operators (such as +), which results in simplification of the code written. For example, the following code segment shows that "count = count +1" can be written such that count is a bit vector, and 1 is an integer.

```
ENTITY sequence IS
  port (clk: in bit;
    s : inout bit);
end sequence;

ARCHITECTURE fsm OF sequence IS

SIGNAL count: INTEGER RANGE 0 TO 7;

BEGIN

PROCESS BEGIN

  WAIT UNTIL clk = '1';

    CASE count IS

    WHEN 0 | 1 | 2 | 3 =>
      s <= '1';
      count <= count + 1;
    WHEN 4 =>
      s <= '0';
      count <= count + 1;
    WHEN 5 =>
      s <= '1';
      count <= o"0";
    WHEN others =>
      s <= '0';
      count <= o"0";
    END CASE;

END PROCESS;

END FSM;
```

In this example, the + operator is overloaded to accept both integer and bit arguments. *Warp2* supports overloading of operators.

Functions

A major advantage of VHDL is the ability to implement functions. The support of functions allows designs to be reused by simply specifying a function and passing the appropriate parameters. *Warp2* features some built-in functions such as ttf (truth-table function). The ttf function is particularly useful for state machine or look-up table designs. The following code describes a seven-segment display decoder implemented with the ttf function:

```
ENTITY seg7 IS
  PORT(
    inputs: IN BIT_VECTOR (0 to 3)
    outputs: OUT BIT_VECTOR (0 to 6)
  );
END SEG7;

ARCHITECTURE mixed OF seg7 IS

CONSTANT truthTable:
  x01_table (0 to 11, 0 to 10) := (
-- input   &      output
-- ------------------------
  "0000"   &   "0111111",
  "0001"   &   "0000110",
  "0010"   &   "1011011",
  "0011"   &   "1001111",
  "0100"   &   "1100110",
  "0101"   &   "1101101",
  "0110"   &   "1111101",
  "0111"   &   "0000111",
  "1000"   &   "1111111",
  "1001"   &   "1101111",
  "101x"   &   "1111100", --creates E pattern
  "111x"   &   "1111100"
  );

BEGIN

    outputs <= ttf(truthTable,inputs);

END mixed;
```

Boolean Equations

A third design-entry method available to *Warp2* users is Boolean equations. *Figure 2* displays a schematic of a simple one-bit half adder. The following code describes how this one-bit half adder can be implemented in *Warp2* with Boolean equations:

```
--entity declaration
ENTITY half_adder IS
  PORT (x, y : IN BIT;
    sum, carry : OUT BIT);
END half_adder;
--architecture body
ARCHITECTURE behave OF half_adder IS
BEGIN
```

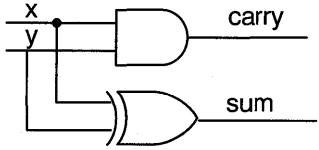


Figure 2. One-Bit Half Adder

```
  sum <= x XOR y;
  carry <= x AND y;
END behave;
```

Structural VHDL (RTL)

While all of the design methodologies described thus far are high-level entry methods, structural VHDL provides a method for designing at a very low level. In structural descriptions (also called RTL), the designer simply lists the components that make up the design and specifies how the components are wired together. *Figure 3* displays the schematic of a simple 3-bit shift register and the following code shows how this design can be described in *Warp2* using structural VHDL:

```
ENTITY shifter3 IS port (
    clk : IN BIT;
    x : IN BIT;
    q0 : OUT BIT;
    q1 : OUT BIT;
    q2 : OUT BIT);
  END shifter3;

ARCHITECTURE struct OF shifter3 IS
  SIGNAL q0_temp, q1_temp, q2_temp : BIT;
  BEGIN
    d1 : DFF PORT MAP(x,clk,q0_temp);
    d2 : DFF PORT MAP(q0_temp,clk,q1_temp);
    d3 : DFF PORT MAP(q1_temp,clk,q2_temp);
    q0 <= q0_temp;
    q1 <= q1_temp;
    q2 <= q2_temp;
  END struct;
```

All of the design-entry methods described can be mixed as desired. The ability to combine both high- and low-level entry methods in a single file is unique to VHDL. The flexibility and power of VHDL allows users of *Warp2* to describe designs using whatever method is appropriate for their particular design.

Binding Architecture

The purpose of a binding architecture is to map external signals of a design to the pins of a physical device. The binding architecture can be in a separate file or appended to the end of the design file.

Here is a binding architecture file for the 3-bit shift register described in the last example:

```
USE work.rtlpkg.all;
USE work.shift3pkg.all;
```

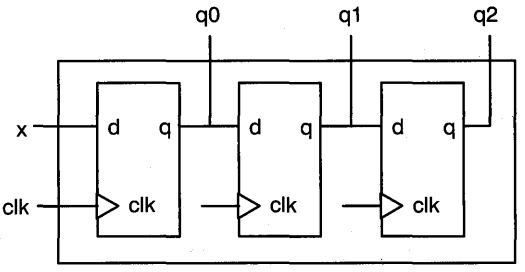


Figure 3. Three-Bit Shift Register Circuit Design

```
ARCHITECTURE shift3 OF c22v10 IS
  BEGIN
    SH1:shifter3 PORT MAP(
      clk     => pin1,
      x       => pin2,
      fbx(q0) => pin14,
      fbx(q1) => pin15,
      fbx(q2) => pin16);
  END shift3;
```

As indicated in the architecture statement, this design targets the Cypress 22V10 for implementing the specified function. By simply changing the architecture statement and appropriately modifying the pin assignments, a binding architecture file targeting other Cypress PLDs can easily be generated.

Compilation

Once a design entity and binding architecture have been completed, a design is compiled using *Warp2*. Although implementation is with a single command, compilation is actually a multistep process (as shown in *Figure 1*). The first step is synthesizing the input VHDL into a logical representation of the design. *Warp2* synthesis is unique in that the input language (VHDL) supports a very high level of abstraction. Competing PLD compilers require very specific and device-dependent information in the design input file.

The second step of compilation is an iterative process of optimizing the design and fitting the logic into the targeted PLD. Logical optimization in *Warp2* is accomplished with the Espresso algorithms. The optimized design is fed to the *Warp2* fitter, which applies the design to the specified target PLD. The *Warp2* fitter supports manual or automatic pin assignments as well as automatic selection of D or T flip-flops. After the optimization and fitting step is complete, *Warp2* automatically creates a JEDEC file for the specified PLD.

Simulation

Warp2 is delivered with Cypress's PLD ToolKit. PLD ToolKit features a graphical waveform simulator that can be used to simulate designs generated in *Warp2*. The ToolKit simulator provides functional simulation and features interactive waveform editing and viewing. The simulator also provides the ability to probe internal nodes, automatically generate clocks and pulses, and to generate JEDEC test vectors from simulator waveforms.

Programming

The result of *Warp2* compilation is a JEDEC file that implements the input design in the targeted PLD. Using the JEDEC file, Cypress PLDs can be programmed on Cypress's QuickPro II programmer or on any qualified third-party programmer.

System Requirements

For PCs

IBM PC-AT or equivalent (386 or higher recommended)

PC-DOS version 3.3 or higher

2 Mbytes of RAM (4 Mbytes recommended)

EGA, VGA, or Hercules monochrome display

20-Mbyte hard disk drive

1.2-Mbyte 5¼-inch or 1.44-Mbyte floppy disk drive

Two or three-button mouse

Windows Version 3.1 or higher (optional)

For Sun Workstations

SPARC CPU
Sun OS 4.1.1 or later
16 Mbytes of RAM
1.44-Mbyte 3½-inch disk drive

Ordering Information

CY3120 *Warp2* PLD Compiler includes:
- 5¼-inch, 1.2-Mbyte floppy disks
- 3½-inch, 1.4-Mbyte floppy disks
- *Warp2* User's Guide
- *Warp2* Workbook
- *Warp2* Reference Manual
- Registration Card

Document #: 38–00218–A

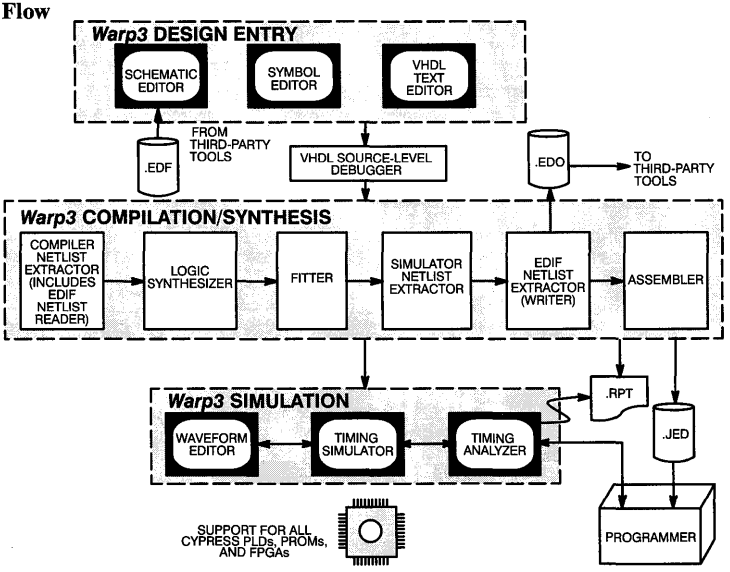
CYPRESS SEMICONDUCTOR

Warp3 VHDL Development System for PLDs and FPGAs

Features

- **Sophisticated PLD/FPGA design and verification system based on VHDL**
- ***Warp3* is based on ViewLogic's Powerview™ environment**
  - **— Advanced graphical user interface for Windows and Sun Workstations**
  - **— Schematic capture (ViewDraw™)**
  - **— Interactive timing simulator (ViewSim™)**
  - **— Waveform stimulus and viewing (ViewTrace™)**
  - **— Textual design entry using VHDL**
  - **— Graphical VHDL debugger**
  - **— Mixed-mode design entry support**
  - **— EDIF input/output capability**
  - **— VHDL to schematic option (ViewGen™)**
- **The core of *Warp3* is an IEEE 1076 standard VHDL compiler**
  - **— VHDL is an open, powerful design language**
  - **— VHDL (IEEE standard 1076) facilitates design portability across devices and/or CAD platforms**
  - **— VHDL facilitates the use of industry-standard simulation and synthesis tools for board and system-level design**
  - **— VHDL facilitates hierarchical design with support for functions and libraries**
- **For synthesis *Warp3* supports a rich subset of VHDL for synthesis including**
  - **— Enumerated types**
  - **— Integers**
  - **— For . . . generate loops**
  - **— Operator overloading**
- **State-of-the-art optimization and reduction algorithms**
  - **— Optimization for flip-flop type (D type/ T type)**
  - **— Automatic pin assignment**
  - **— Automatic state assignment (Gray code, binary, one-hot)**
- **Completely automatic place and route**
  - **— Includes timing back annotation into ViewSim**
- **Support for ALL Cypress PLDs/FPGAs and PROMs, including:**
  - **— Industry-standard 20- and 24-pin devices like the 22V10**
  - **— Cypress 7C33X family of 28-pin PLDs**
  - **— CY7C258/9 State Machine PROMs**
  - **— MAX5000**
  - **— FLASH37X**
  - **— pASIC38X**
- **Sun and PC platforms**

***Warp3* Design Flow**



Document #: 38−00242−A

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PC-AT is a trademark of International Business Machines Corporation.
PowerView, ViewDraw, ViewSim, ViewTrace and ViewGen are trademarks of ViewLogic.

CYPRESS SEMICONDUCTOR

CY3200

PLDS-MAX+PLUS® Design System

Features

- **Unified development system for Multiple Array MatriX (MAX®) EPLDs**
- **Hierarchical design entry methods for both graphical and textual designs**
  - **— Multiple-level schematics and hardware language descriptions**
  - **— Library of 7400 Series TTL and bus macrofunctions optimized for MAX architecture**
  - **— Advanced Hardware Description Language (AHDL) supporting state machines, Boolean equations, truth tables, arithmetic, and relational operations**
  - **— Delay prediction for graphic and text designs**
- **Logic synthesis and minimization for quick and efficient processing**
- **Compiler that compiles a 100% utilized CY7C342 in only 10 minutes**
- **Automatic error location for AHDL text files and schematics**
- **Interactive Simulator with probe assignments for internal nodes**
- **Runs on IBM PC/AT®, PS/2® or compatible machines**
- **Waveform Editor for entering and editing waveforms and viewing simulation results**

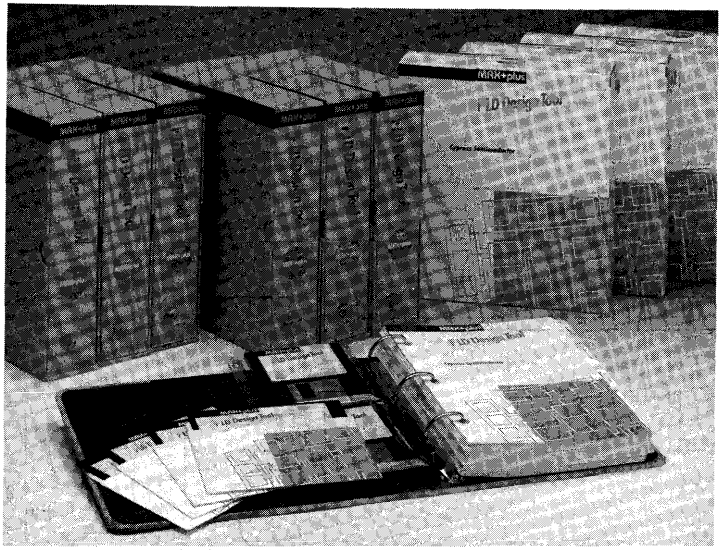
Description

The PLDS-MAX+PLUS (Programmable Logic Development System) is a unified CAE system for designing logic with Cypress's CY7C340 family of EPLDs (*Figure 1*). PLDS-MAX+PLUS includes design entry, design processing, timing simulation, and device programming support. PLDS-MAX+PLUS runs on IBM PS/2, PC-AT, or compatible machines, and provides tools to quickly and efficiently create and verify complex logic designs.

The MAX+PLUS software compiles designs for MAX EPLDs in minutes. Designs may be entered with a variety of design entry mechanisms. MAX+PLUS supports hierarchical entry of both Graphic Design Files (GDFs) with the MAX+PLUS Graphic Editor, and Text Design Files (TDFs) with the Advanced Hardware Description Language (AHDL). The Graphic Editor offers advanced features such as multiple hierarchy levels, symbol editing, and a library of 7400 series devices as well as basic SSI gates. AHDL designs may be mixed into any level of the hierarchy or used on a standalone basis. AHDL is tailored especially for EPLD designs and includes support for complex Boolean and arithmetic functions, relational comparisons, multiple hierarchy levels, state machines with automatic state variable assignment, truth tables, and function calls.

In addition to multiple design entry mechanisms, MAX+PLUS includes a sophisticated compiler that uses advanced logic synthesis and minimization techniques in conjunction with heuristic fitting rules to efficiently place designs within MAX EPLDs. A programming file created by the compiler is then used by MAX+PLUS to program MAX devices with the QP2–MAX programming hardware.

Simulations may be performed with a powerful, event-driven timing simulator. The MAX+PLUS Simulator interactively displays timing results in the MAX+PLUS Waveform Editor. Hardcopy table and waveform output is also available. With the Waveform Editor, input vector waveforms may be entered, modified, grouped,



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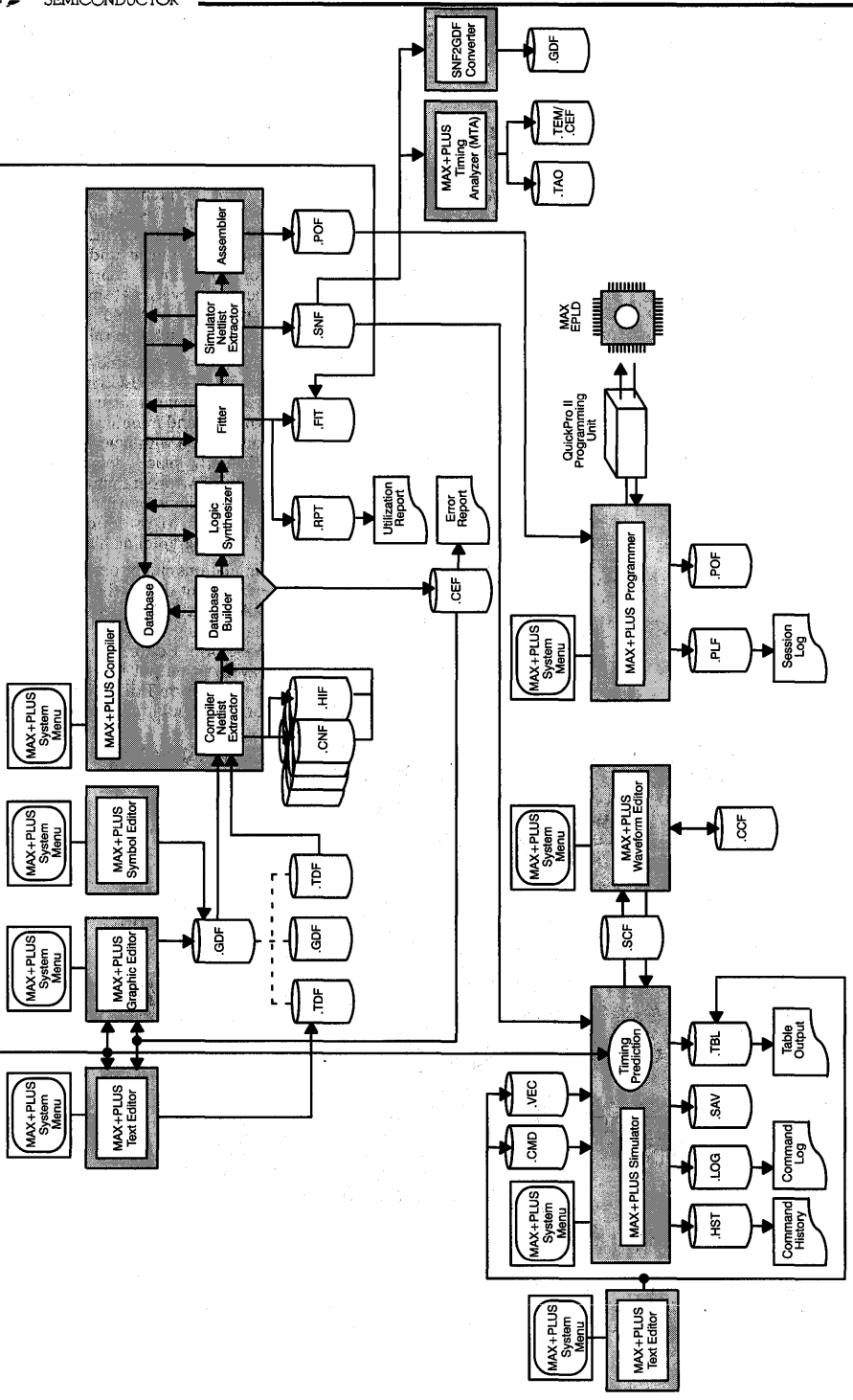

Figure 1. MAX+PLUS Block Diagram

and ungrouped. In addition, the Waveform Editor compares simulation runs and highlights the differences.

The integrated structure of MAX+PLUS provides features such as automatic error location and delay prediction. If a design contains an error in either a schematic or a text file, MAX+PLUS flags the error *and* takes the user to the actual location of the error in the original schematic or text file. In addition, propagation delays of critical paths may be determined in both the Graphic and Text Editors with the delay predictor. After the source and destination nodes are tagged, the shortest and longest timing delays are calculated.

MAX+PLUS provides a seamless design framework using a consistent graphical user interface throughout. This framework simplifies all stages of the design cycle: design entry, processing, verification, and programming. In addition, MAX+PLUS offers online help to aid the user.

Design Entry

MAX+PLUS offers both graphic and text design entry methods. GDFs are entered with the MAX+PLUS Graphic Editor; Boolean equations, state machines, and truth tables may be entered with the MAX+PLUS Test Editor using AHDL. The ability to freely mix graphics and text files at all levels of the design hierarchy and to use either a top-down or bottom-up design method makes design entry simple and versatile.

Graphic Editor

The Graphic Editor provides a mouse-driven, multi-windowed environment in which commands are entered with pop-up menus or simple keystrokes. The Hierarchy Display window, shown at the top, lists all schematics used in a design. The designer navigates the hierarchy by placing the cursor on the name of the design to be edited and clicking the left mouse button. The Total View window (next to the Hierarchy window) shows the entire design. By clicking on an area in this window, the user is moved to that area of the schematic. The Error Report window lists all warnings and errors in the compiled design; selecting an error with the cursor highlights the problem node and symbol. A design is edited in the main area, which may be enlarged by closing the auxiliary windows.

When entering a design, the user may choose from a library of over 200 7400 series and special-purpose macrofunctions that are all optimized for MAX architecture. In addition, the designer my create custom functions that can be used in any MAX+PLUS design.

To take advantage of the hierarchy features, the user first saves the entered design so the Graphic Editor can automatically create a symbol representing the design. This symbol may be used in a higher-level schematic or in another design. It may also be modified with the Symbol Editor.

Tag-and-drag editing is used to move individual symbols or entire areas. Lines stay connected with orthogonal rubberbanding. A design may be printed on an Epson FX-compatible printer, or plotted on an HP- or Houston Instruments–compatible plotter.

Symbol Editor

The MAX+PLUS Symbol Editor enables the designer to create or modify a custom symbol representing a GDF or TDF. It is also possible to modify input and output pin placement of an automatically generated symbol.

The created symbol represents a lower-level design, described by a GDF or TDF. The lower-level design represented by the symbol may be displayed with a single command that invokes either the Graphic Editor for schematics or the Text Editor for AHDL designs.

AHDL

The Advanced Hardware Description Language (AHDL) is a high-level, modular language used to create logic designs for MAX EPLDs. It is completely integrated into MAX+PLUS, so AHDL files may be created, edited, compiled, simulated, and programmed from within MAX+PLUS.

AHDL provides support for state machine, truth tables, and Boolean equations, as well as srithmetic and relational operations. AHDL is hierarchical, which allows frequently used functions such as TTL and bus macrofunctions to be incorporated in a design. AHDL supports complex arithmetic and relational opeartions, such as addition, subtraction, equality, and magnitude comparisons, with the logic functions automatically generated. Standard Boolean functions, including AND, OR, NAND, NOR, XOR, and SNOR are also included. Groups are fully supported so operations may be performed on groups as well as on single variables. AHDL also allows the designer to specify the location of nodes within MAX EPLDs. Together, these features enable complex designs to be implemented in a concise, high-level description.

Text Editor

The MAX+PLUS Text Editor enables the user to view and edit text files within the MAX+PLUS environment. Any ASCII text file, including Vector Files, Table Files, Report Files, and AHDL Text Design Files (TDFs) may be viewed and edited wihtout having to exit to DOS.

The Text Editor parallels the Graphic Editor's menu structure. It has a Hierarchy Display and a Total View window for moving through the hierarchy levels and around the design. It includes automatic error location and hierarchy traversal. If an error is found in a TDF during compilation, the Text Editor is automatically invoked and the line of AHDL code where the error occurred is highlighted. In addition, a design may use both text and graphic files. As the designer t4raverses the hierarchy, the Text Editor is invoked for text files, and the Graphic Editor is invoked for schematics.

Symbol Libraries

The library provided with MAX+PLUS contains the most commonly used 7400 series devices such as counters, decoders, encoders, shift registers, flip-flops, latches, and multipliers, as well as special bus macrofunctions, all of which increase design productivity. Because of the flexible architecture of MAX EPLDs (that includes asynchronous preset and clear), true TTL device emulation is achieved. Cypress also provides special-purpose bus macrofunctions for designs that use buses. All macrofunctions have been optimized to maximize speed and utilization. Refer to the *MAX+PLUS TTL MacroFunctions* manual for more information on TTL macrofunctions.

Design Processing

The MAX+PLUS Compiler processes MAX designs. The Compiler offers options that speed the processing and analysis of a design. The user can set the degree of detail of the Report File and the maximum number of errors generated. In addition, the user may select whether or not to extract a netlist file for simulation.

The Compiler compiles a design in increments. If a design has been previously processed, only the portion of the design that has been changed is re-extracted, which decreases the compilation time. This "Make" facility is an automatic feature of the Compile command.

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist that is used to define the design from each file. At this time, design rules are checked for any errors. If errors are found, the Graphic Editor is invoked when the error appears in a GDF, and the Text Editor is invoked when the error appears in a TDF. The Error Report window in both editors highlights the location of the error. A successfully extracted design is built into a database to be used by the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the MAX architecture. Any unused logic within the design is automatically removed. The Logic Synthesizer uses expert system synthesis rules to factor and map logic within the multilevel MAX architecture. It then chooses the approach that ensures the most efficient use of silicon resources.

The next module, the Fitter, uses heuristic rules to optimally place the synthesized design into the chosen MAX EPLD. For MAX devices that have a Programmable Interconnect Array (PIA), the Fitter also routes the signals across this interconnect structure, so the designer doesn't have to worry about placement and routing issues. A Report File (.RPT) is issued by the Fitter, which shows design implementation as well as any unused resources in the EPLD. The designer can then determine how much additional logic may be placed in the EPLD.

A Simulator Netlist File (.SNF) may be extracted from the compiled design by the Simulator Netlist Extractor if simulation is desired. Finally, the Assembler creates a Programmer Object File (.POF) from the compiled design. This file is used with the QP2–MAX programming hardware to program the desired part.

Delay Prediction and Probes

MAX+PLUS includes powerful analysis tools to verify and analyze the completed design. Delay analysis with the delay predictor may be performed interactively in the Graphic Editor, or in the Simulator. The Simulator is interactive and event-driven, yielding true timing and functional charactersitics of the compiled design.

The delay predictor provides instant feedback about the timing of the processed design. After selecting the start point and end point of a path, the designer may determine the shortest and longest propagation delays of speed-critical paths.

Also, a designer may use probes to mark internal nodes in a design. The designer may enter a probe by placing the cursor on any node in a graphic design, selecting the SPE (Symbol:Probe:Enter) command, and then entering a unique name to define the probe. This name may then be used in the Graphic Editor, Simulator, and Waveform Editor to reference that node, so that lengthy hierarchical path names are avoided.

Simulator

Input stimuli can be defined with a straightforward vector input language, or waveforms can be directly drawn using the Waveform Editor. Outputs may also be viewed in the Waveform Editor, or hardcopy table and waveform files may be printed.

The Simulator used the Simulator Netlist File (SNF) extracted from the compiled design to perform timing simulation with 1/10-nanosecond resolution. A Command File may be used for batch operation, or commands may be entered interactively. Simulator commands allow the user to halt the simulation dependent on user-defined conditions, to force and group nodes, and perform AC detection.

If flip-flop set-up or hold times have been violated, the Simulator warns the user. In addition, the minimum pulse width and period of oscillation may be defined. If a pulse is shorter than the minimum pulse width specified, or if a node oscillates for longer than the specified time, the Simulator issues a warning.

Waveform Editor

The MAX+PLUS Waveform Editor provides a mouse-driven environment in which timing waveforms may be viewed and edited. It functions as a logic analyzer, enabling the user to observe simulation results. Simulated waveforms may be viewed and manipulated at multiple zoom levels. Nodes may be added, deleted, and combined into buses, which may contain up to 32 signals represented in binary, octal, decimal, or hexadecimal format. Logical opeartors may also be performed on pairs of waveforms, so that waveforms may be inverted, ORed, ANDed, or XORed together.

The Waveform Editor includes sophisticated editing features to define and modify input vectors. Input waveforms are created with the mouse and familiar text editing commands. Waveforms may be copied, patterns may be repeated, and blocks may be moved and copied. For example, all or part of a waveform may be contracted to simulate the increase in clock frequency.

The Waveform Editor also compares and highlights the difference between two different simulations. A user may simulate a design, observe and edit the results, and then resimulate the design, and the Waveform Editor will show the results superimposed upon each other to highlight the differences.

MAX+PLUS Timing Analyzer (MTA)

The MAX+PLUS Timing Analyzer (MTA) provides user-configurable reports that assist the designer in analyzing critical delay paths, set-up and hold timing, and overall system performance of any MAX EPLD design. Critical paths identified by these reports may be desplayed and highlighted.

Timing delays between multiple source and destination nodes may be calculated, thus creating a connection matrix giving the shortest and longest delay paths between all source and destination nodes specified. Or, the designer may specify that the detailed paths and delays between specific sources and destinations be shown.

The set-up/hold option provides set-up and hold requirements at the device pins for all pins that feed the D, CLK, or ENABLE inputs of flip-flops and latches. Critical source nodes may be specified individually, or set-up and hold at all pins may be calculated. This information is then displayed in a table, one set of set-up and hold times per flip-flop/latch.

The MTA also allows the user to print a complete list of all accessible nodes in a design; i.e., all nodes that may be displayed during simulation or delay prediction.

All MTA options may be listed in an MTA command file. With this file, the user may specify all information needed to configure the output.

SNF2GDF Converter

SNF2GDF converts the SNF into logic schematics represented with basic gates and flip-flop elements. It uses the SNF's delay and connection information and creates a series of schematics fully annotated with propagation delay and set-up and hold information at each logic gate. Certain speed paths of a design may be specified for conversion, so the user may graphically analyze only the paths considered critical.

If State Machine or Boolean Equation design entry is used, SNF2GDF shows how the high-level description has been synthesized and placed into the MAX architecture.

Device Programming

PLDS-MAX contains the basic hardware and software for programming the MAX EPLD family. Adapters are included for programming the CY7C344 (DIP and PLCC) and CY7C342 (PLCC) devices. Additional adapters supporting other MAX devices may be purchased separately. MAX+PLUS programming software drives the QP2–MAX programming hardware. The designer can use MAX+PLUS to program and verify MAX EPLDs. If the security bit of the device is not set to ON, the designer may also read the contents of a MAX device and use this information to program additional devices.

System Requirements

Minimum System Configuration

IBM PS/2 model 50 or higher, PC/AT or compatible computer.

PC-DOS version 3.1 or higher.

640 kbytes RAM.

EGA, VGA or Hercules monochrome display.

20-MB hard disk drive.

1.2-MB 5¼″ or 1.44-MB 3½″ floppy disk drive.

2-button serial port mouse.

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Recommended System Configuration

IBM PS/2 model 70 or higher, or Compaq 386 20-MHz computer.

PC-DOS version 3.3.

640 kbytes of RAM plus 1 MB of expanded memory with LIM 3.2-compatible EMS driver.

VGA graphics display.

20-MB hard disk drive.

1.2-MB 5¼″ or 1.44-MB 3½″ floppy disk drive.

3-button serial port mouse.

Ordering Information

CY3200	PLDS-MAX+PLUS System including:	
	CY3201	MAX+PLUS software, manuals and key.
	CY3202	QP2–MAX PLD programmer with CY3342 & CY3344 adapters.

Device Adapters

CY3342	Adapter for CY7C342 in PLCC packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY33435	Adapter for CY7C343 in DIP and PLCC packages.
CY3340	Adapter for CY7C341 in PLCC packages.
CY3340R	Adapter for CY7C341 in PGA packages.
CY3342F	Adapter for CY7C342 in flatpack (TMB) packages.

CYPRESS SEMICONDUCTOR

PLS–EDIF Bidirectional Netlist Interface

Features

- **Bidirectional netlist interface between MAX+PLUS® and other major CAE software packages**
- **Supports the industry-standard Electronic Design Interchange Format (EDIF) version 200.**
- **MAX EPLD designs entered on workstation CAE tools can be downloaded to MAX+PLUS for compilation; compile designs can then be returned to the workstation for device- or system-level simulation.**
- **EDIF netlist reader imports EDIF netlists into MAX+PLUS. Library Mapping Files (LMFs) convert CAE library functions to MAX+PLUS library functions.**
- **LMFs allow conversion of common Dazix, Mentor Graphics, Valid Logic, and Viewlogic functions to MAX+PLUS functions.**
- **EDIF netlist writer produces post-synthesis logic and delay information used during device- or board-level simulation with popular CAE tools.**
- **Runs on IBM PS/2®, PC-AT®, or compatible machines.**

Description

The PLS-EDIF tool kit is a bidirectional EDIF netlist interface between workstation-based CAE software packages and the PLDS-MAX+PLUS Design System (*Figure 1*).

PLS-EDIF allows the designer to enter and verify logic designs for MAX EPLDs using third-party CAE tools. The EDIF 200 netlist exchange format is the two-way bridge between MAX+PLUS and third-party schematic capture and simulation tools. PLS-EDIF runs on an IBM PS/2, PC–AT, or compatible machines.

Any CAE software package that produces EDIF 200 netlists can interface to MAX+PLUS with PLS-EDIF. EDIF netlists are imported into MAX+PLUS using the EDIF Design File-to-Compiler Netlist File (EDF2CNF) Converter. Library Mapping Files (LMFs) are used with EDF2CNF to map third-party CAE library functions to the MAX+PLUS library functions. LMFs are provided for Dazix, Mentor Graphics, Valid Logic, and Viewlogic software, but designers may create LMFs to map any CAE software library.

After a design is imported into MAX+PLUS, it is compiled with the sophisticated MAX+PLUS Compiler, which uses advanced logic synthesis and minimization techniques together with heuristic fitting rules to optimize the design for MAX EPLD architecture. A Programmer Object File created by the MAX+PLUS Compiler is then used together with standard Cypress or third-party programming hardware to program MAX devices.

EDIF netlists can be exported from MAX+PLUS using the Simulator Netlist File-to-EDIF Design File (SNF2EDF) Converter. This converter generates an EDIF output file from a compiled MAX+PLUS design. The EDIF file contains the post-synthesis information used by CAE simulators to perform device- or board-level simulation.

PLS-EDIF provides an open environment that allows popular CAE tools to be used to create and simulate MAX EPLD designs. The designer may use a preferred workstation schematic capture package to enter logic designs, and then quickly convert and compile them with EDF2CNF and MAX+PLUS. Likewise, designs compiled in MAX+PLUS and converted with SNF2EDF may be transferred to a workstation for simulation. The PLS-EDIF netlist reader and writer together allow MAX EPLD designs to be entered and simulated on any workstation platform.

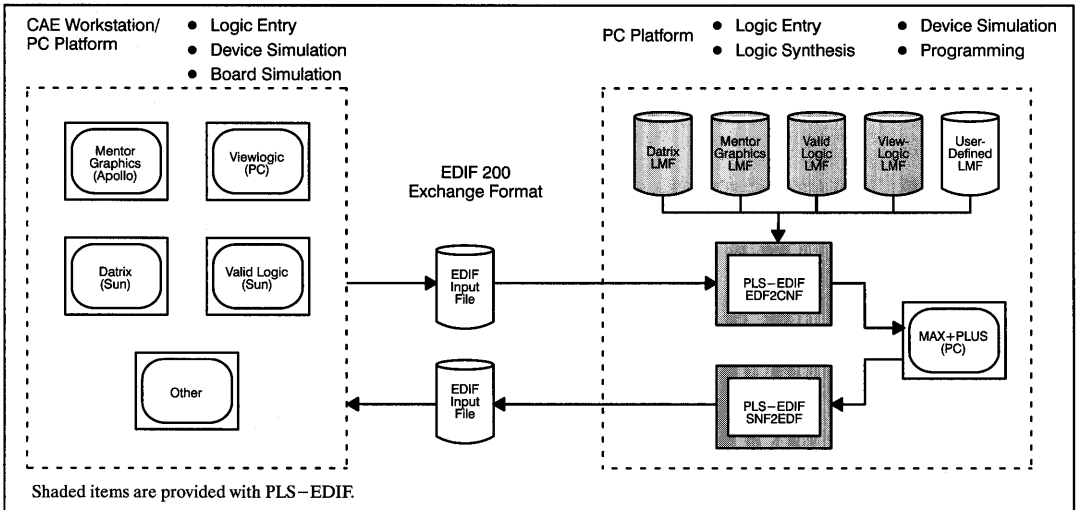

Figure 1. PLS–EDIF Workstation Interface

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EDF2CNF Converter

The EDF2CNF Converter generates one or more MAX+PLUS Compiler Netlist Files (CNFs) from an EDIF file. For each CNF, a Hierarchy Interconnect File (HIF) and a Graphic Design File (GDF) are also generated (see *Figure 2*). The CNF contains the connectivity data for a design file, while the HIF defines the hierarchical connections between design files. The GDF is a symbol that represents the actual design data in the CNF. This symbol may be entered in the MAX+PLUS Graphic Editor and integrated into a logic schematic.

EDF2CNF can convert any EDIF 200 netlist with the following parameters:

EDIF level 0
keyword level 0
view type NETLIST
cell type GENERIC

Library Mapping Files (LMFs) are used with EDF2CNF to convert workstation CAE functions into equivalent MAX+PLUS functions. This direct substitution is beneficial because MAX+PLUS functions are optimized for both logic utilization and performance in MAX EPLD designs.

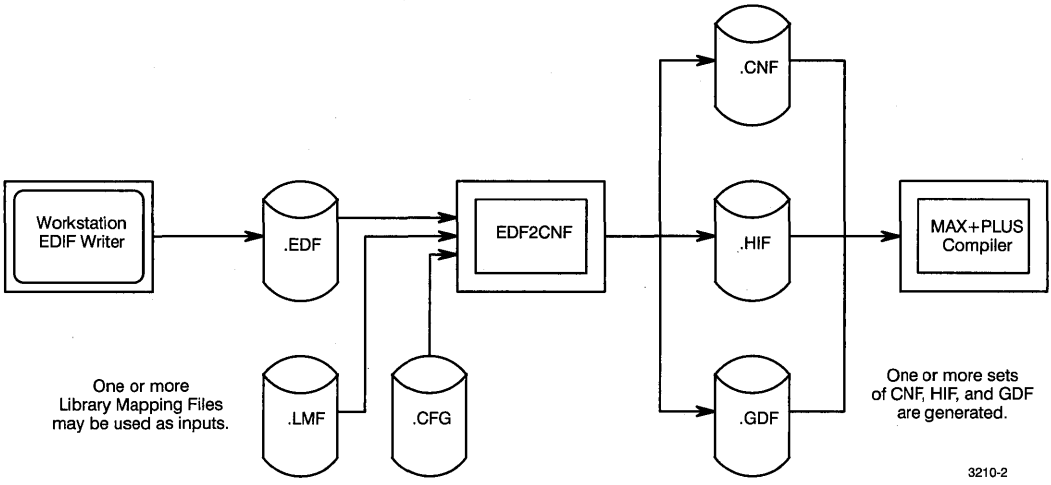


Figure 2. EDF2CNF Block Diagram

Workstation Information

EDF2CNF has been specifically tested for use with the Dazix, Mentor Graphics, Valid Logic, and ViewLogic CAE software packages. In addition, LMFs for these products are provided with the PLS–EDIF tool kit.

Dazix

To design logic and create an EDIF file with Dazix software, the following applications are required:

ACE (Dazix graphics editor)
DANCE and DRINK (Dazix compiler)
ENW verison 1.0 (Dazix EDIF netlist writer)

Table 1 lists the Dazix basic functions that are mapped to MAX+PLUS functions.

Table 1. Dazix Library Mapping File

Dazix Function	MAX+PLUS Function	
R#AND	AND#	(# = 2, 3, 4, 5, 6, 7, 8, 9)
R#ANDD	BNOR#	(# = 2, 3, 4, 5, 6, 7, 8, 9)
R#NAND	NAND#	(# = 2, 3, 4, 6, 7, 8, 9, 13)
R#NANDD	BOR#	(# = 2, 3, 4, 5, 7, 8, 9, 13)
R#NOR	NOR#	(# = 2, 3, 4, 5)
R#NORD	BAND#	(# = 2, 3)
R#OR	OR#	(# = 2, 3, 4, 5)
R#ORD	BNAND#	(# = 2, 3, 4, 5)
R1BUF	MCELL	
R1INV	NOT	
R1INVD	EXP	
R1OCBUF	SCLK	
R1OTBUF	TRIBUF	
R1TINV	TRINOT	
R2XNOR	XNOR	
R2XOR	XOR	
R3UAOI	1A2NOR2	
R4AOI	2A2NOR2	
R4OAI	2OR2NA2	
R8AOI	4A2NOR4	
R13TNAND	TNAND13	
R13TNANDD	TBOR13	
RDFLOP	DFF2	
RDLATCH	RDLATCH	
RJKFLOP	JKFF2	

Mentor Graphics

To design logic and create an EDIF file using Mentor Graphics software, the following applications are required:

NETED (Mentor Graphics graphics editor)
EXPAND (Mentor Graphics compiler)
EDIFNET version 7.0 (Mentor Graphics EDIF netlist writer)

Table 2 lists the Mentor Graphics basic functions that are mapped to MAX+PLUS functions.

Table 2. Mentor Graphics Libary Mapping File

Mentor Graphics Function	MAX+PLUS Function	
AND#	AND#	(# = 2, 3, 4, 5, 6)
BUF	SCLK	
DELAY	MCELL	
DFF	DFF2	
INV	NOT	
JKFF	JKFF2	
LATCH	MLATCH	
NAND#	NAND#	(# = 2, 3, 4, 5, 6, 9)
NOR#	NOR#	(# = 2, 3, 4, 6, 8, 16)
OR#	OR2#	(# = 2, 3, 4, 6, 8)
XNOR2	XNOR	
XOR2	XOR	

Valid Logic

To design logic and create an EDIF file using Valid Logic software, the following applications are required:

ValidGED (Valid Logic graphics editor)
ValidCompiler
GEDIFNET (Valid Logic EDIF netlist writer)

Table 3 lists the Valid Logic basic functions that are mapped to MAX+PLUS functions.

Table 3. Valid Logic Libary Mapping File

Valid Logic Function	MAX+PLUS Function
INV	EXP
LS00	NAND2
LS02	NOR2
LS04	NOT
LS08	AND2
LS10	NAND3
LS11	AND3
LS20	NAND4
LS21	AND4
LS27	NOR3
LS28	NOR2
LS30	NAND8
LS32	OR2
LS37	NAND2
LS40	NAND4
LS74	DFF2
LS86	XOR
LS126	TRI
LS280	DFF2
LS386	XOR

ViewLogic

To design logic and create an EDIF file using ViewLogic software, the following applications are required:

Workview (ViewLogic graphics editor)
EDIFNET2 version 3.02 (Viewlogic EDIF netlist writer)

Table 4 lists the ViewLogic basic functions that are mapped to MAX+PLUS functions.

Table 4. ViewLogic Libary Mapping File

ViewLogic Function	MAX+PLUS Function	
AND#	AND#	(# = 2, 3, 4, 8)
ANDNOR22	2A2NOR2	
BUF	SOFT	
DAND#	DAND#	(# = 2, 3, 4, 8)
DELAY	MCELL	
DOR#	DOR#	(# = 2, 3, 4, 8)
DXOR#	DXOR#	(# = 2, 3, 4, 8)
JKFFRE	JKFFRE	
MUX41	MUX41	
NAND#	NAND#	(# = 2, 3, 4, 8)
NOR#	NOR#	(# = 2, 3, 4, 8)
NOT	NOT	
OR#	OR#	(# = 2, 3, 4, 8)
TRIAND#	TAND#	(# = 2, 3, 4, 8)
TRIBUF	TRIBUF	
TRINAND#	TNAND#	(# = 2, 3, 4, 8)
TRINOR#	TNOR#	(# = 2, 3, 4, 8)
TRINOT	TRINOT	
TRIOR#	TOR#	(# = 2, 3, 4, 8)
UBDEC38	DEC38	
UDFDL	UDFDL	
UJKFF	UJKFF	
XNOR2	XNOR	
XNOR#	XNOR#	(# = 3, 4, 8)
XOR2	XOR	
XOR#	XOR#	(# = 3, 4, 8)

LMF Support for TTL Macrofunctions

In addition to the basic gates, LMFs map various Dazix, Mentor Graphics, Valid Logic, and ViewLogic TTL macrofunctions to their MAX+PLUS equivalents, as shown in *Table 5*.

Table 5. TTL Function Mappings in LMFs

MAX+PLUS	Dazix	Mentor Graphics	Valid Logic	ViewLogic
7442	LS42	74LS42	LS42	74LS42
DFF2	LS74	74LS74A	LS74	74LS74A
7483	LS83	74LS83A	LS83	74LS83A
7485	LS85	74LS85	LS85	74LS85
7491	LS91	74LS91	LS91	74LS91
7493	LS93	74LS93	LS93	74LS93
74138	LS138	74LS138	LS138	74LS138
74139	LS139			
74139M		74LS139A	LS139	74LS139
74151	LS151	74LS151	LS151	74LS151
74153		74LS153		74LS153
74153M	LS153		LS153	
74157	LS157	74LS157		74LS157
74157M				LS157
74160	LS160	74LS160A	LS160	74LS160A
74161	LS161	74LS161A	LS161	74LS161A
74162	LS162	74LS162A	LS162	74LS162A
74163	LS163	74LS163A	LS163	74LS163A
74164	LS164	74LS164	LS164	74LS164
74165	LS165	74LS165	LS165	74LS165
74174	LS174	74LS174		74LS174
74174M			LS174	
74181	LS181	74LS181	LS181	74LS181
74190	LS190	74LS190	LS190	74LS190
74191	LS191	74LS191	LS191	74LS191
74194	LS194	74LS194A	LS194A	74LS194A
74273	LS273	74LS273		74LS273
74174M			LS273	
74279MD	LS279			
74279M		74LS279	LS279	74LS279
74280	LS280	74LS280	LS280	74LS280
74373	LS373	74LS373		74LS373
74373M			LS373	
74374	LS374	74LS374		74LS374
74374M			LS374	
74393M	LS393	74LS393	LS393	74LS393

Custom Library Mapping Files

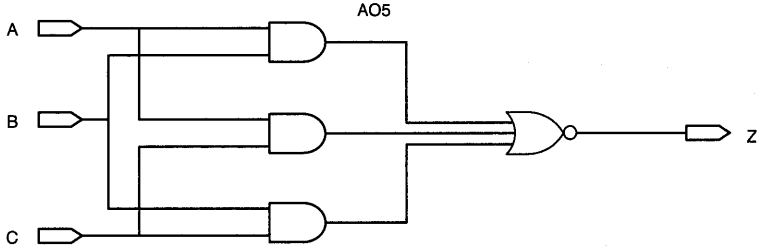
Designers can map their commonly used workstation functions to MAX+PLUS equivalents by modifying an LMF or creating a new one. If no equivalent function currently exists in MAX+PLUS, the user can create the function with the MAX+PLUS Graphic Editor or Text Editor before mapping the function in an LMF. *Figure 3* shows an example of this process.

SNF2EDF Converter

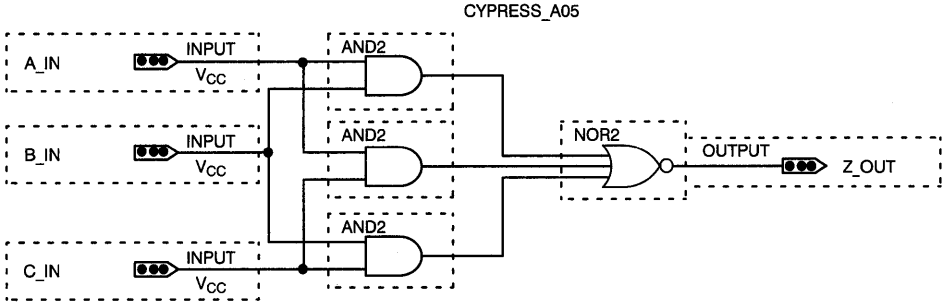
The SNF2EDF Converter creates an industry-standard level 0 EDIF file from a MAX+PLUS Simulator Netlist File (SNF). The SNF, which is optionally generated during compilation of a MAX EPLD design, contains all post-synthesis functional and delay information for the completed design. This design-specific information is also contained in the EDIF output file after conversion so that it may be integrated into a workstation environment for simulation. An optional command file enables the user to customize the output EDIF file for various workstation environments by renaming certain constructs or by changing the EDIF level or keyword level (see *Figure 4*).

The EDIF output file may have one of two formats. The first format expresses all delays with special EDIF property constructs. The second expresses combinatorial delays with portdelay constructs and registered delays as pathdelay constructs—a format that is especially useful for behavioral simulators. Both formats are shown in *Figure 5*.

Step 1: Select a workstation function for mapping



Step 2: Design an equivalent circuit with the MAX+PLUS Graphic Editor



Step 2: Map the workstation function to the MAX+PLUS function in an LMF

```
LIBRARY new_lib

%User Library Mapping File%

BEGIN
FUNCTION MAX_A05 (A_IN, B_IN, C_IN)
RETURNS (Z_OUT)
FUNCTION "A05" ("A", "B", "C")
RETURNS ("Z")
END
```

3210-3

Figure 3. Creating a Library Mapping File

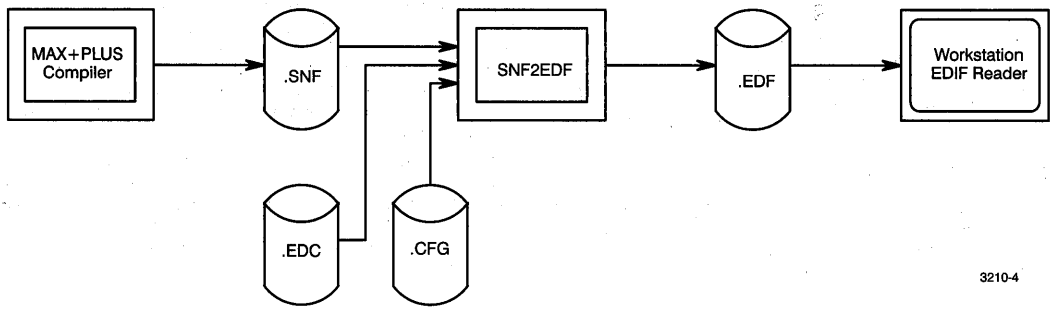


Figure 4. SNF2EDF Block Diagram

Format 1: Delays expressed with property constructs

```
(instance xor2_5
  (viewRef view1
    (cellRef XOR2
  (property TPD(integer 20)(unit TIME)))
```

Format 2: Delays expressed with portdelay and pathdelay constructs

```
(instance xor2_5
  (viewRef view1
    (cellRef XOR2
  (portInstance &1
    (portDelay
      (derivation CALCULATED
      (delay(e 20 - 10)))))
```

Figure 5. EDIF File Formats

System Requirements

- IBM PC/AT or compatible computers; IBM PS/2 models 50, 60, 70, or 80
- MS−DOS version 3.1 or later version
- 640 Kbytes of RAM
- 1 Mbyte of expanded memory compatible with version 3.2 or a later version of the Lotus/Intel/Microsoft Expanded Memory Specification
- EGA, VGA, or Hercules Monochrome display
- 20-Mbyte hard disk drive
- 1.2-Mbyte 5¼″ or 1.44-Mbyte 3½″ floppy disk drive
- MAX+PLUS version 2.01 or a later version
- Workstation-PC network hardware and software with the ability to transfer ASCII files

Package Contents

- Floppy diskettes containing all PLS−EDIF programs and files for both PC/AT and PS/2 platforms
  - — EDF2CNF Converter
  - — SNF2EDF Converter
  - — Library Mapping Files for Dazix, Mentor Graphics, Valid Logic, and Viewlogic
  - — MAX+PLUS macrofunctions for Dazix, Mentor Graphics, Valid Logic, and ViewLogic libraries
  - — Example files
- Documentation

Document #: 38−00144

CYPRESS SEMICONDUCTOR

CY3220

MAX+PLUS® II Design System

Features

- **Unified development system for Multiple Array MatriX (MAX®) CY7C340 EPLDs plus compiler support for all Altera Classic, Max 5000, Max 7000, and STG EPLDs**
- **Microsoft Windows version 3.0 to provide graphical user interface, multi-tasking abilities, efficient memory management, and extensive printer and plotter support**
- **Hierarchical design entry methods for graphical, textual, and waveform designs**
  - **— Graphic Editor for schematic designs**
  - **— Text Editor for Text Design Files (TDFs) in the Advanced Hardware Description Language (AHDL) will support state machines, Boolean equations, truth tables, arithmetic, and relational operations**
  - **— Waveform Editor for waveform entry to define logic and view simulation results**
- **Logic synthesis and minimization for quick and efficient processing**
- **Automatic error location for AHDL text files and schematics**
- **Interactive Simulator with probe assignments for internal nodes**
- **Multichip partitioning to divide large designs into multiple EPLDs**
- **Library of 7400 series TTL and bus macrofunctions optimized for MAX architecture**
- **Bidirectional EDIF 2 0 0 netlist interface compatible with a variety of CAE schematic capture and simulation tools**
- **Runs on IBM PC/AT®, PS/2® or compatible machines**

Description

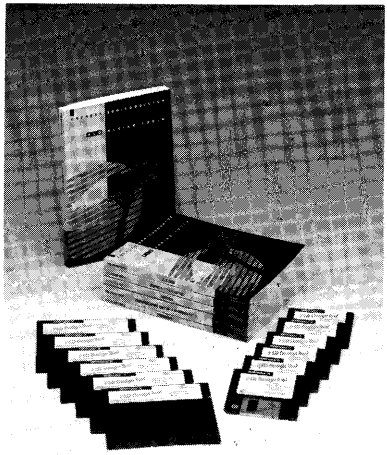
The MAX+PLUS II programmable logic development system is a unified CAE system for designing logic with Cypress's CY7C340 family of EPLDs (*Figure 1*). MAX+PLUS II includes design entry, design processing, timing simulation, and device programming support. MAX+PLUS II runs on IBM PS/2, PC-AT, or compatible machines, and provides tools to quickly and efficiently create and verify complex logic designs.

The MAX+PLUS II software compiles designs for MAX EPLDs in minutes. Designs may be entered with a variety of design entry mechanisms. MAX+PLUS II supports hierarchical entry of Graphic Design Files (GDFs) with the MAX+PLUS II Graphic Editor, Text Design Files (TDFs) with the Advanced Hardware Description Language (AHDL), and waveforms with the Waveform Editor. The Graphic Editor offers advanced features such as multiple hierarchy levels, symbol editing, and a library of 7400 series devices as well as basic SSI gates. AHDL designs may be mixed into any level of the hierarchy or used on a standalone basis. AHDL is tailored especially for EPLD designs and includes support for complex Boolean and arithmetic functions, relational comparisons, multiple hierarchy levels, state machines with automatic state variable assignment, truth tables, and function calls.

MAX+PLUS II includes a sophisticated compiler that uses advanced logic synthesis and minimization techniques in conjunction with heuristic fitting rules to efficiently place designs within MAX EPLDs. A programming file created by the compiler is then used by MAX+PLUS II to program MAX devices.

MAX+PLUS II features multichip partitioning that automatically splits large designs into multiple EPLDs, allowing the user to create large system-level designs. The partitioner lets the user specify speed-critical path for optimum EPLD selection and design placement.

Simulations may be performed with a powerful, event-driven timing simulator. The MAX+PLUS II Simulator interactively



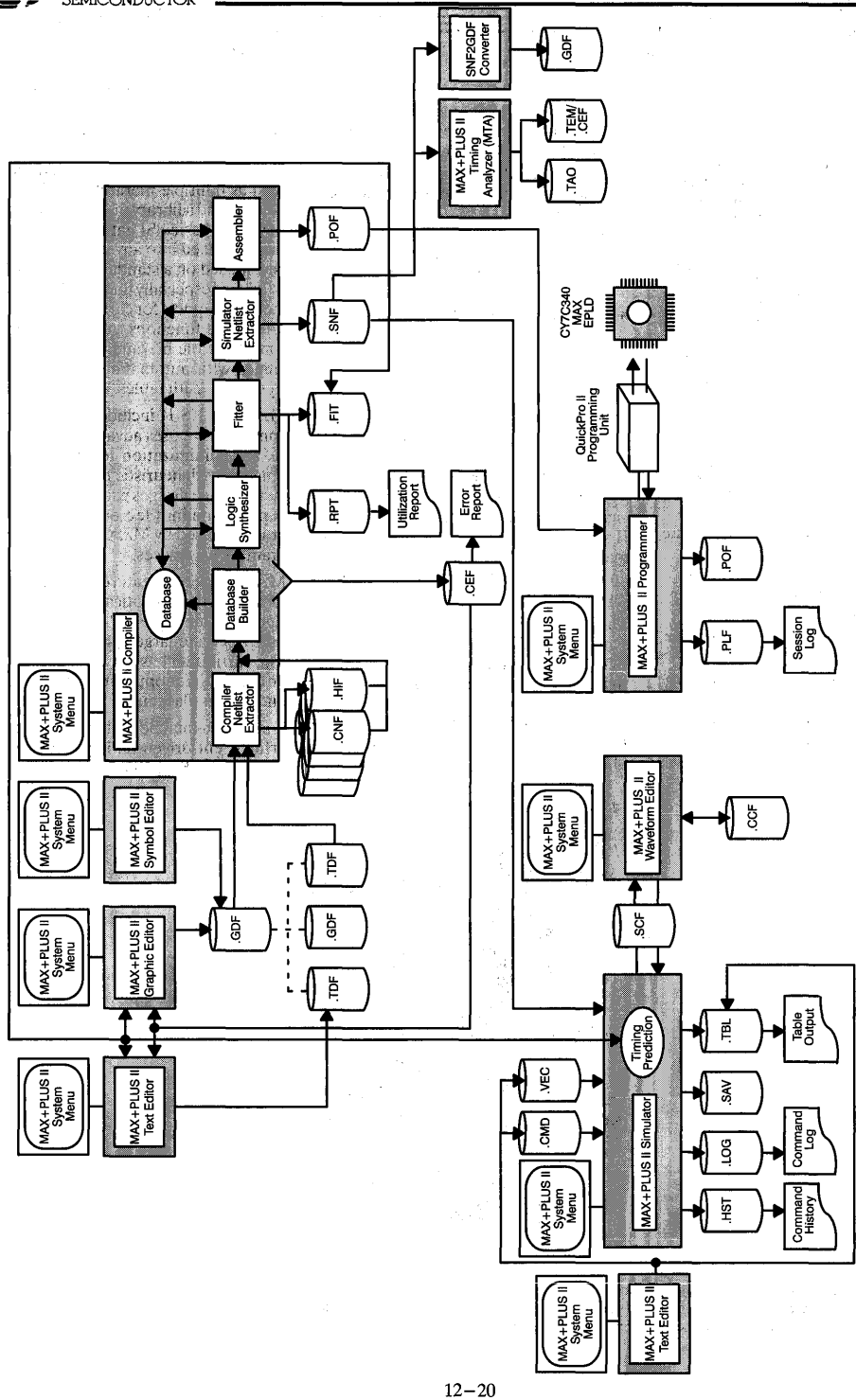


Figure 1. MAX+PLUS II Block Diagram

displays timing results in the MAX+PLUS II Waveform Editor. Hardcopy table and waveform output is also available. With the Waveform Editor, input vector waveforms may be entered, modified, grouped, and ungrouped, and simulation errors may be viewed. In addition, the Waveform Editor compares simulation runs and highlights the differences.

The integrated structure of MAX+PLUS II provides features such as automatic error location and delay prediction. If a design contains an error in either a schematic or a text file, MAX+PLUS II flags the error *and* takes the user to the actual location of the error in the original schematic or text file. The designer uses the Clipboard to quickly copy design information from one editor to another. In addition, propagation delays of critical paths may be determined in both the Graphic and Text Editors with the delay predictor. After the source and destination nodes are tagged, the shortest and longest timing delays are calculated.

MAX+PLUS II provides a seamless design framework using a consistent graphical user interface throughout. This framework simplifies all stages of the design cycle: design entry, processing, verification, and programming. In addition, MAX+PLUS II offers extensive, context-sensitive online help to aid the user.

Design Entry

MAX+PLUS II supports three hierarchical design entry mechanisms: (1) the Graphic Editor is used to enter schematic designs; (2) the Text Editor is used to enter Text Design Files (TDFs) in the Advanced Hardware Description Language (AHDL); and (3) the Waveform Editor is used to enter waveforms to define logic. These design entry methods can be freely mixed within a single project, allowing the designer to specify each logic block in the most appropriate format. In addition, EDIF 2 0 0 netlists with popular CAE schematic tools such as ORCAD, Viewlogic, FutureNet, Mentor Graphics or Valid Logic are easily imported into MAX+PLUS II.

Graphic Editor

The Graphic Editor provides a mouse-driven, multi-windowed environment in which commands are entered with pop-up menus or simple keystrokes. The Hierarchy Display window lists all schematics used in a design. The designer navigates the hierarchy by placing the cursor on the name of the design to be edited and clicking the left mouse button. The Total View window shows the entire design. The Error Report window lists all warnings and errors in the compiled design; selecting an error with the cursor highlights the problem node and symbol. A design is edited in the main area, which may be enlarged by closing the auxiliary windows.

When entering a design, the user may choose from a library of over 300 7400 series and special-purpose macrofunctions that are all optimized for MAX architecture. In addition, the designer may create custom functions that can be used in any MAX+PLUS II design.

To take advantage of the hierarchy features, the user first saves the entered design so the Graphic Editor can automatically create a symbol representing the design. This symbol may be used in a higher-level schematic or in another design. It may also be modified with the Symbol Editor.

The Graphics Editor offers many advanced schematic entry and debugging features. For example, probes can be entered into the schematic so a specific net (e.g., flip-flops, logic outputs) can be easily viewed during simulation; critical paths can be specified in the schematic; and objects can be quickly moved with tag-and-drag editing. Lines stay connected with orthogonal rubberbanding. Designers can also group nodes into buses, quickly locate source and destination of nets, and use the search-and-replace to make changes to the net name. A design may be printed on an Epson FX-compatible printer, or plotted on an HP- or Houston Instruments–compatible plotter.

Symbol Editor

The MAX+PLUS II Symbol Editor enables the designer to create or modify a custom symbol representing a GDF or TDF. It is also possible to modify input and output pin placement of an automatically generated symbol.

The created symbol represents a lower-level design, described by a GDF or TDF. The lower-level design represented by the symbol may be displayed with a single command that invokes either the Graphic Editor for schematics or the Text Editor for AHDL designs.

AHDL

The Advanced Hardware Description Language (AHDL) is a high-level, modular language used to create logic designs for MAX EPLDs. It is completely integrated into MAX+PLUS II, so AHDL files may be created, edited, compiled, simulated, and programmed from within MAX+PLUS II.

AHDL provides support for state machine, truth tables, and Boolean equations, as well as arithmetic and relational operations. AHDL is hierarchical, which allows frequently used functions such as TTL and bus macrofunctions to be incorporated in a design. AHDL supports complex arithmetic and relational operations, such as addition, subtraction, equality, and magnitude comparisons, with the logic functions automatically generated. Standard Boolean functions, including AND, OR, NAND, NOR, XOR, and XNOR are also included. Groups are fully supported so operations may be performed on groups as well as on single variables. AHDL also allows the designer to specify the location of nodes within MAX EPLDs. Together, these features enable complex designs to be implemented in a concise, high-level description.

Text Editor

The MAX+PLUS II Text Editor enables the user to view and edit text files within the MAX+PLUS II environment. Any ASCII text file, including Vector Files, Table Files, Report Files, and AHDL Text Design Files (TDFs) may be viewed and edited without having to exit to DOS.

The Text Editor parallels the Graphic Editor's menu structure. It has a Hierarchy Display and a Total View window for moving through the hierarchy levels and around the design. It includes automatic error location, hierarchy traversal, global search-and-replace, and multiple fonts. If an error is found in a TDF during compilation, the Text Editor is automatically invoked and the line of AHDL code where the error occurred is highlighted. In addition, a design may use both text and graphic files. As the designer traverses the hierarchy, the Text Editor is invoked for text files, and the Graphic Editor is invoked for schematics.

Waveform Editor

The MAX+PLUS II Waveform Editor provides a mouse-driven environment in which waveform algorithms automatically generate logic from user-defined input and output waveforms. It also functions as a logic analyzer, enabling the user to observe simulation results.

Simulated waveforms may be viewed and manipulated at multiple zoom levels. Nodes may be added, deleted, and combined into

buses, which may contain up to 32 signals represented in binary, octal, decimal, or hexadecimal format. Logical operators may also be performed on pairs of waveforms, so that waveforms may be inverted, ORed, ANDed, or XORed together.

The Waveform Editor includes sophisticated editing features to define and modify input vectors. Input waveforms are created with the mouse and familiar text editing commands. Waveforms may be copied, patterns may be repeated, and blocks may be moved and copied. For example, all or part of a waveform may be contracted to simulate the increase in clock frequency.

The Waveform Editor also compares and highlights the difference between two different simulations. A user may simulate a design, observe and edit the results, and then resimulate the design, and the Waveform Editor will show the results superimposed upon each other to highlight the differences.

Symbol Libraries

The library provided with MAX+PLUS II contains the most commonly used 7400 series devices such as counters, decoders, encoders, shift registers, flip-flops, latches, and multipliers, as well as special bus macrofunctions, all of which increase design productivity. Because of the flexible architecture of MAX EPLDs (that includes asynchronous preset and clear), true TTL device emulation is achieved. Cypress also provides special-purpose bus macrofunctions for designs that use buses. All macrofunctions have been optimized to maximize speed and utilization.

EDIF Support

MAX+PLUS II software supports bidirectional EDIF 2 0 0 netlists, providing a convenient way to import popular CAE schematic capture and simulation tools. The Library Mapping Files (LMFs) of MAX+PLUS II converts EDIF 2 0 0 netlists into equivalent primatives and macrofunctions. Users can create their own LMFs to map any CAE software library. MAX+PLUS II then automatically generates a symbol from a translated EDIF file, so that the file can be directly incorporated into a MAX+PLUS II schematic or AHDL design. EDIF netlists can also be exported to the popular simulation tool of the user's choice. The netlist contains all post-synthesis function and delay information for the completed design.

Design Processing

The MAX+PLUS II Compiler processes MAX designs. The Compiler offers options that speed the processing and analysis of a design. The user can set the degree of detail of the Report File and the maximum number of errors generated. In addition, the user may specify for which MAX EPLD the compiler should target the design and select whether or not to extract a netlist file for simulation.

The Compiler compiles a design in increments. If a design has been previously processed, only the portion of the design that has been changed is re-extracted, which decreases the compilation time. This "Make" facility is an automatic feature of the Compile command.

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist that is used to define the design from each file. At this time, design rules are checked for any errors. If errors are found, the Graphic Editor is invoked when the error appears in a GDF, and the Text Editor is invoked when the error appears in a TDF. The Error Report window in both editors highlights the location of the error. A successfully extracted design is built into a database to be used by the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the MAX architecture. Any unused logic within the design is automatically removed. The Logic Synthesizer uses expert system synthesis rules to factor and map logic within the multilevel MAX architecture. It then chooses the approach that ensures the most efficient use of silicon resources.

The next module, the Fitter, uses heuristic rules to optimally place the synthesized design into the chosen MAX EPLD. For MAX devices that have a Programmable Interconnect Array (PIA), the Fitter also routes the signals across this interconnect structure, so the designer doesn't have to worry about placement and routing issues. A Report File (.RPT) is issued by the Fitter, which shows design implementation as well as any unused resources in the EPLD. The designer can then determine how much additional logic may be placed in the EPLD.

For large system-level designs, the logic design is broken up into multiple EPLDs of the same family. The designer does not have to manually split a large design into many smaller designs. The user can control the design's partitioning at the source level by specifying chip assignments to flip-flops and pins.

A Simulator Netlist File (.SNF) may be extracted from the compiled design by the Simulator Netlist Extractor if simulation is desired. Finally, the Assembler creates a Programmer Object File (.POF) from the compiled design. This file is used with the QP2–MAX programming hardware to program the desired CY7C340 family member.

Delay Prediction and Probes

MAX+PLUS II includes powerful analysis tools to verify and analyze the completed design. Delay analysis with the delay predictor may be performed interactively in the Graphic Editor, or in the Simulator. The Simulator is interactive and event-driven, yielding true timing and functional characteristics of the compiled design.

The delay predictor provides instant feedback about the timing of the processed design. After selecting the start point and end point of a path, the designer may determine the shortest and longest propagation delays of speed-critical paths.

Also, a designer may use probes to mark internal nodes in a design. The designer may enter a probe by placing the cursor on any node in a graphic design, selecting the SPE (Symbol:Probe:Enter) command, and then entering a unique name to define the probe. This name may then be used in the Graphic Editor, Simulator, and Waveform Editor to reference that node, so that lengthy hierarchical path names are avoided.

Simulator

The MAX+PLUS II Simulator uses the virtual memory of Windows 3.0 to run simulations of large, multichip EPLDs.

Input stimuli can be defined with a straightforward vector input language, or waveforms can be directly drawn using the Waveform Editor. Outputs may also be viewed in the Waveform Editor, or hardcopy table and waveform files may be printed.

The Simulator uses the Simulator Netlist File (SNF) extracted from the compiled design to perform timing simulation with 1/10-nanosecond resolution. A Command File may be used for batch operation, or commands may be entered interactively. Simulator commands allow the user to halt the simulation dependent on user-defined conditions, to force and group nodes, and perform AC detection.

If flip-flop set-up or hold times have been violated, the Simulator warns the user. In addition, the minimum pulse width and period of oscillation may be defined. If a pulse is shorter than the minimum pulse width specified, or if a node oscillates for longer than the specified time, the Simulator issues a warning.

MAX+PLUS II Timing Analyzer (MTA)

The MAX+PLUS II Timing Analyzer (MTA) provides user-configurable reports that assist the designer in analyzing critical delay paths, set-up and hold timing, and overall system performance of any MAX EPLD design. Critical paths identified by these reports may be displayed and highlighted.

Timing delays between multiple source and destination nodes may be calculated, thus creating a connection matrix giving the shortest and longest delay paths between all source and destination nodes specified. Or, the designer may specify that the detailed paths and delays between specific sources and destinations be shown.

The set-up/hold option provides set-up and hold requirements at the device pins for all pins that feed the D, CLK, or ENABLE inputs of flip-flops and latches. Critical source nodes may be specified individually, or set-up and hold at all pins may be calculated. This information is then displayed in a table, one set of set-up and hold times per flip-flop/latch.

The MTA also allows the user to print a complete list of all accessible nodes in a design; i.e., all nodes that may be displayed during simulation or delay prediction.

All MTA options may be listed in an MTA command file. With this file, the user may specify all information needed to configure the output.

SNF2GDF Converter

SNF2GDF converts the SNF into logic schematics represented with basic gates and flip-flop elements. It uses the SNF's delay and connection information and creates a series of schematics fully annotated with propagation delay and set-up and hold information at each logic gate. Certain speed paths of a design may be specified for conversion, so the user may graphically analyze only the paths considered critical.

If State Machine or Boolean Equation design entry is used, SNF2GDF shows how the high-level description has been synthesized and placed into the MAX architecture.

Device Programming

PLDS-MAX contains the basic hardware and software for programming the CY7C340 MAX EPLD family. Adapters are included for programming the CY7C344 (DIP and PLCC) and CY7C342 (PLCC) devices. Additional adapters supporting other MAX devices may be purchased separately. MAX+PLUS II programming software drives the QP2–MAX programming hardware. The designer can use MAX+PLUS II to program and verify CY7C340 MAX EPLDs. If the security bit of the device is not set to ON, the designer may also read the contents of a MAX device and use this information to program additional devices.

System Requirements

Minimum System Configuration

IBM PS/2 model 70 or higher, PC/AT or compatible 80386-based computer.

PC-DOS version 3.1 or higher.

4 Mbytes RAM.

Microsoft Windows version 3.0.

Microsoft Windows–compatible graphics card and monitor.

EGA, VGA or Hercules monochrome display.

20-MB hard disk drive.

1.2-MB 5¼″ or 1.44-MB 3½″ floppy disk drive.

2-button serial port mouse compatible with Microsoft Windows 3.0.

Parallel port.

Recommended System Configuration

IBM PS/2 model 70 or higher, or compatible 386-based computer.

PC-DOS version 3.3 or higher.

4 Mbytes of RAM plus 10 Mbytes of expanded memory with LIM 3.2-compatible EMS driver.

Microsoft Windows version 3.0.

VGA graphics display.

20-MB hard disk drive.

1.2-MB 5¼″ or 1.44-MB 3½″ floppy disk drive.

3-button serial port mouse compatible with Microsoft Windows 3.0.

Parallel port.

Ordering Information

CY3220	MAX+PLUS II System including:	
	CY3221	MAX+PLUS II software, manuals and key.
	CY3202	QP2–MAX PLD programmer with CY3342 & CY3344 adapters.

Device Adapters

CY3340	Adapter for CY7C341 in PLCC packages.
CY3340R	Adapter for CY7C341 in PGA packages.
CY3342	Adapter for CY7C342 in PLCC packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY3342F	Adapter for CY7C342 in Flatpack (TMB) packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY33435	Adapter for CY7C343 in DIP and PLCC packages.

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CYPRESS SEMICONDUCTOR

CY3300

QuickPro II™

Features

- **Combined PROM, PLD, and EPROM Programmer**
- **Programs all Cypress CMOS & ECL PLDs and PROMs**
- **Easy-to-use, menu-driven software**
- **New device and feature updates via floppy disk and adapters**
- **Plugs into standard IBM PC® parallel port—no need to use up a bus slot**
- **Compatible with IBM PC/AT®, PS/2®, and compatible computers**
- **Programs 20-, 24-, 28-, 32-, 40-, 44-, and 68-pin Cypress PLDs and PROMs via device adapters**
- **Modular design with adapter bus for future device support and future feature enhancements**
- **Comprehensive self-test and automatic calibration software**
- **Supports Vmargin verification for a higher degree of device reliability**

Description

QuickPro II is Cypress's second-generation QuickPro PLD and PROM device programmer. It incorporates new architectural features that enable it to handle all current and future devices through a 96-pin universal bus connector. The QuickPro II hardware can be installed on any IBM PC/AT- or PS/2-compatible computer by simply plugging into a standard parallel port. The software communicates with the QuickPro II electronics via this parallel port and utilizes intelligent programming algorithms to minimize device programming time.

The QuickPro II architecture and feature set were dictated by the needs of Cypress's new-generation PLDs and PROMs. Many of these devices offer very high performance and complexity with large numbers of pins. To meet these needs, the QuickPro II utilizes flexible pin electronics, a universal adapter bus and a carefully engineered system design that minimizes electrical noise. Pin electronics are located as close as possible to the device being programmed. In addition to the V_{PP} and V_{CC} voltage sources needed to program parts, the QuickPro II incorporates a Vmargin voltage source for measuring the relative programming margins to which a device has been programmed and a Vref voltage source for doing self-testing and calibration.

For PLDs, QuickPro II uses the JEDEC standard data format, so present and future design tools such as PLD ToolKit®, ABEL®, CUPL®, and PALASM® can be used. QuickPro II reads Intellec 86®, Motorola S, TEK and space format files. It also reads and writes PROM PC DOS binary files for use with assemblers and compilers. QuickPro II is a low-cost, full-feature programming/verification system with a flexible and extendible architecture. The user interface software is menu-driven with complete on-screen explanations.

Technical Information

Size

The QuickPro II base unit is approximately 10 1/2″ x 8 1/2″ x 1″. Individual device family adapters vary in size from 5″ x 3″ to 6″ x 6″. The parallel port cable and AC power adapter cable are both approximately 6′ in length.

Power

AC Power Adapter: 17 VAC @ 500 mA

Device Adapters

Device adapters are external modules with various pin and socket configurations. Each adapter plugs into the QuickPro II bus connector and maps the pins of particular devices and packages to the pin electronics resources available at the connector. Each adapter has at least one LED that indicates when power is being applied to the socket. In addition to these device adapters, package adapters are also used to accommodate the various package options available for PLDs and PROMs.

Memory

640K of total memory is necessary to operate the QuickPro II software.

Devices Supported

QuickPro II hardware and software supports the programming and verification of all Cypress and Aspen PLDs and PROMs.

Ordering Information

CY3300	QuickPro II system including:
CY3301	QuickPro II base unit
CY3302	QuickPro II parallel port cable
CY3303	QuickPro II AC power adapter
CY3304	QuickPro II software (disk & manual)
CY3202	QP2-MAX version of QuickPro II for PLDS-MAX+PLUS design tool that consists of the CY3300 system and the CY3342 and CY3344 adapters.

International versions (220V) of the CY3300 and the CY3202 are also available.

Device Adapters

CY3320	Adapter for all Cypress 20-, 24-, 28-, and 32-pin devices excluding the MAX parts. Contains 20-, 24, and 28- pin DIP sockets (package adapters required for 32-pin devices).
CY3342	Adapter for the CY7C342—PLCC
CY3342R	Adapter for the CY7C342—PGA
CY3342F	Adapter for the CY7C342—Flatpack
CY3340	Adapter for the CY7C341—PLCC
CY3340R	Adapter for the CY7C341—PGA
CY3344	Adapter for the CY7C344—PLCC & DIP
CY33435	Adapter for the CY7C343—PLCC & DIP

Package Adapters

Package adapters are used with the CY3320 generic device programming adapter on the QuickPro II in order to accommodate Cypress's wide variety of device packaging options. The package adapters used with devices having 28 native pins on the QuickPro II are the same as those used on the original QuickPro®. The number of native pins that a device has refers to the number of actual signal, power and ground pins used—excluding any N/C (No Connects) in a particular package. All devices are programmed in the CY3320 adapter's DIP socket having the same number of pins as the native pins on the device. Therefore, a 22V10 is programmed in the 24-pin DIP socket, regardless of whether it is in a DIP package or a PLCC package, even though the PLCC package has 28 pins (4 are N/Cs). A package adapter between the 28-pin PLCC and the 24-pin DIP sockets is used to accomplish this. The following list summarizes the package adapters used with the CY3320 adapter on the QuickPro II.

Devices with 20 native pins

CY3005 20-pin LCC – Package codes L61 and Q61 – All devices

CY3007 20-pin PLCC – Package code J61 – All devices

CY3031 20-pin SOJ – Package code V5 – All devices

CY3021 20-pin Cerpack – Package code K71

Devices with 24 native pins

CY3004A 28-pin LCC (22V10, CG7C323, CG7C324)

CY3004B 28-pin LCC (7C225, 7C235, 7C245, 7C261/3/4, 7C281/2, 7C291/2, 7C245, 7C291A/2A/3A)

CY3010 28-pin LCC (20G10, 20RA10)

CY3006A 28-pin PLCC and HLCC (22V10, CG7C323, CG7C324)

CY3006B 28-pin PLCC and HLCC (7C225, 7C235, 7C245, 7C261/3/4, 7C281/2, 7C291/2, 7C245, 7C291A/2A/3A)

CY3011 28-pin PLCC and HLCC (20G10, 20RA10)

CY3019 24-pin Cerpack – Package codes K73, T73 – All devices

CY3030 24-pin SOIC – Package code S13 – All devices

Devices with 28 native pins

CY3008 28-pin LCC – Package codes L64 and Q64 – All devices

CY3009 28-pin PLCC and HLCC – Package codes J64 and H64 – All devices

CY3014 28-pin SOIC – Package code S21 – All devices

CY3022 28-pin SOJ – Package code V21 – All devices

CY3020 28-pin Cerpack – Package codes K74, T74 – All devices

CY3017 32-pin rectangular LCC (7C251/4)

CY3024 32-pin rectangular LCC (7C266, 7C271/4, 7C277, 7C279, 7C286)

CY3026 32-pin DIP (7C289)

CY3027 32-pin rectangular LCC (7C285, 7C287)

CY3029 32-pin rectangular LCC (7C289)

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Section Contents

Quality and Reliability **Page Number**

CYPRESS SEMICONDUCTOR

Quality, Reliability, and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability is built into every product design, starting from the initial design conception.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883D and MIL-M-38510J as baseline documents to determine our Test Methods, Procedures and General Specifications for semiconductors.

Customers using our commercial and industrial grade product receive the benefit of a military patterned process flow at no additional charge.

Product Testing Categories

Five different testing categories are offered by Cypress:

1. Commercial operating range product: 0°C to +70°C.
2. Industrial operating range product: – 40°C to +85°C.
3. Military Grade product processed to MIL-STD-883D; Military operating range: – 55°C to +125°C.
4. SMD (Standardized Military Drawing) approved product: Military operating range: – 55°C to +125°C, electrically tested per the applicable Military Drawing.
5. JAN qualified product; Military operating range: – 55°C to +125°C, electrically tested per MIL-M-38510J slash sheet requirements.

Categories 1, 2, and 3 are available on all products offered by Cypress Semiconductor. Categories 4 and 5 are offered on a more limited basis, dependent upon the specific part type in question.

Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in of 12 hours at 150°C.

Tables 1 and *2* list the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet requirements of these programs.

Military Product Assurance Categories

Cypress's Military Grade components and SMD products are processed per MIL-STD-883D using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

JAN, SMD, and Military Grade devices supplied by Cypress are processed for applications where maintenance is difficult or expensive and reliability is paramount. *Tables 3* through *7* list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883D and MIL-M-38510J.

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883D Method	Product Temperature Ranges: Commercial 0°C to +70°C; Industrial −40°C to +85°C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• Hermeticity					
– Fine Leak	1014, Cond A or B (sample)	Does Not Apply	LTPD = 5	Does Not Apply	LTPD = 5
– Gross Leak	1014, Cond C	Does Not Apply	100%	Does Not Apply	100%
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	Per Cypress Specification	Does Not Apply	Does Not Apply	100%[1]	100%[1]
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max)[2]	5% (max)[2]
Final Electrical	Per Device Specification				
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supplies Extremes	Not Performed	Not Performed	100%[1]	100%[1]
	2. At Hot Temperature and Power Supply Extremes	100%	100%	100%	100%
Cypress Quality Lot Acceptance					
• External Visual	2009	Note 3	Note 3	Note 3	Note 3
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3	Note 3	Note 3

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883D Method	Product Temperature Ranges: Commercial 0°C to +70°C; Industrial −40°C to +85°C	
		Level 1	Level 2
Burn-in			
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Burn-in	1015	Does Not Apply	100%
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Percent Defective Allowable (PDA)		Does Not Apply	15%
Final Electrical	Per Device Specification		
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supply Extremes	Not Performed	100%
	2. At Hot Temperature and Power Supply Extremes	100%	100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Per Cypress Module Specification	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3

Notes:
1. Burn-in is performed as a standard for 12 hours at 150°C.
2. Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
3. Lot acceptance testing is performed on every lot to guarantee 200 PPM average outgoing quality.

Table 3. Cypress JAN/SMD/Military Grade Product Screening Flows for Class B

Screen	Screening Per Method 5004 of MIL-STD-883D	Product Temperature Ranges −55°C to +125°C		
		JAN	SMD/Military Grade Product	Military Grade Module
Visual/Mechanical				
• Internal Visual	Method 2010, Cond B	100%	100%	N/A
• Temperature Cycling	Method 1010, Cond C, (10 cycles)	100%	100%	Optional
• Constant Acceleration	Method 2001, Cond E (Min.), Y1 Orientation Only	100%	100%	N/A
• Hermeticity:				
— Fine Leak	Method 1014, Cond A or B	100%	100%	N/A
— Gross Leak	Method 1014, Cond C	100%	100%	N/A
Burn-in				
• Pre-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Burn-in Test	Method 1015, Cond D, 160 Hrs at 125°C Min. or 80 Hrs at 150°C	100%	100%	100% (48 Hours at 125°C)
• Post-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA, for All Lots	5%	5%	10%
Final Electrical Tests				
• Static Tests	Method 5005 Subgroups 1, 2, and 3	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Functional Tests	Method 5005 Subgroups 7, 8A, and 8B	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Switching	Method 5005 Subgroups 9, 10, and 11	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
Quality Conformance Tests				
• Group A[4]	Method 5005, see Tables 4 – 7 for details	Sample	Sample	Sample
• Group B		Sample	Sample	Sample
• Group C[5]		Sample	Sample	Sample
• Group D[5]		Sample	Sample	Sample
External Visual	Method 2009	100%	100%	100%

Notes:

4. Group A subgroups tested for SMD/Military Grade products are 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.
5. Group C and D end-point electrical tests for SMD/Military Grade products are performed to Group A subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.

Table 4. Group A Test Descriptions

Sub-group	Description	Sample Size/Accept No.	
		Components	Modules[6]
1	Static Tests at 25°C	116/0	116/0
2	Static Tests at Maximum Rated Operating Temperature	116/0	116/0
3	Static Tests at Minimum Rated Operating Temperature	116/0	116/0
4	Dynamic Tests at 25°C	116/0	116/0
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	116/0
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	116/0
7	Functional Tests at 25°C	116/0	116/0
8A	Functional Tests at Maximum Temperature	116/0	116/0
8B	Functional Tests at Minimum Temperature	116/0	116/0
9	Switching Tests at 25°C	116/0	116/0
10	Switching Tests at Maximum Temperature	116/0	116/0
11	Switching Tests at Minimum Temperature	116/0	116/0

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military Grade component products have a Group A sample test performed on each inspection lot per MIL-STD-883D and the applicable device specification.

Table 5. Group B Quality Tests

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[6]
2	Resistance to Solvents, Method 2015	3/0	3/0
3	Solderability, Method 2003	10	10
5	Bond Strength, Method 2011	15	NA

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 6. Group C Quality Tests

Sub-group	Description	LTPD	
		Components	Modules[6]
1	Steady State Life Test, End-Point Electricals, Method 1005, Cond D	5	15/0

Group C tests for JAN product are performed on one device type from one inspection for lot representing each technology. Sample tests are performed per MIL-M-38510J from each three month production of devices, which is based upon the die fabrication date code.

Group C tests for SMD and Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-STD-883D from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

Table 7. Group D Quality Tests (Package Related)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[6]
1	Physical Dimensions, Method 2016	15	15/0
2	Lead Integrity, Seal: Fine and Gross Leak, Method 2004 and 1014	5	15/0
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine and Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004 and 1014	15	15/0
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine and Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 and 1014	15	15/0

Note:

6. Military ~~Grade~~ Modules are processed to proposed JEDEC standard flows for MIL-STD-883D compliant modules.

Table 7. Group D Quality Tests (Package Related) (continued)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15 (0)	15/0
6	Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018	3(0) or 5(1)	N/A
7	Adhesion of Lead Finish,[8] Method 2025	15(0)	15/0
8	Lid Torque, Method 2024[9]	5(0)	N/A

Notes:
7. Does not apply to leadless chip carriers.
8. Based on the number of leads.
9. Applies only to packages with glass seals.

Group D tests for JAN product are performed per MIL-M-38510J on each package type from each six months of production, based on the lot inspection identification (or date) codes.

Group D tests for SMD and Military Grade products are performed per MIL-STD-883D on each package type from each six months of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per the applicable device specification.

Product Screening Summary

Commercial and Industrial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and molded packages available
- Incoming mechanical and electrical performance guaranteed:
  - 0.02% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.65% AQL External Visual Sample inspection
- Electrically tested to Cypress data sheet

Ordering Information

Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number
  Ex: CY7C122-15PC, PALC22V10-25PI

Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add 'B' Suffix to Cypress standard part number when ordering to designate burn-in option
- Parts marked the same as ordered part number
  Ex: CY7C122-15PCB, PALC22V10-25PIB

Military Grade Product

- SMD and Military Grade components are manufactured in compliance with paragraph 1.2.1 of MIL-STD-883D. Compliant products are identified by an 'MB' suffix on the part number (CY7C122-25DMB) and the letter "C"
- JAN devices are manufactured in accordance with MIL-M-38510J
- Military grade devices electrically tested to:
  - Cypress data sheet specifications

    OR
  - SMD devices electrically tested to military drawing specifications

    OR
  - JAN devices electrically tested to slash sheet specifications
- All devices supplied in hermetic packages
- Quality conformance inspection: Method 5005, Groups A, B, C, and D performed as part of the standard process flow
- Burn-in performed on all devices
  - Cypress detailed circuit specification for non-Jan devices

    OR
  - Slash sheet requirements for JAN products
- Static functional and switching tests performed at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

Ordering Information

JAN Product:

- Order per military document
- Marked per military document
  Ex: JM38510/28901BVA

SMD Product:

- Order per military document
- Marked per military document
  Ex: 5962-8867001LA

Military Grade Product:

- Order per Cypress standard military part number
- Marked the same as ordered part number
  Ex: CY7C122-25DMB

Military Modules

- Military Temperature Grade Modules are designated with an 'M' suffix only. These modules are screened to standard combined flows and tested at both military temperature extremes.
- MIL-STD-883D Equivalent Modules are processed to proposed JEDEC standard flows for MIL-STD-883D compliant modules. All MIL-STD-883D equivalent modules are assembled with fully compliant MIL-STD-883D components.

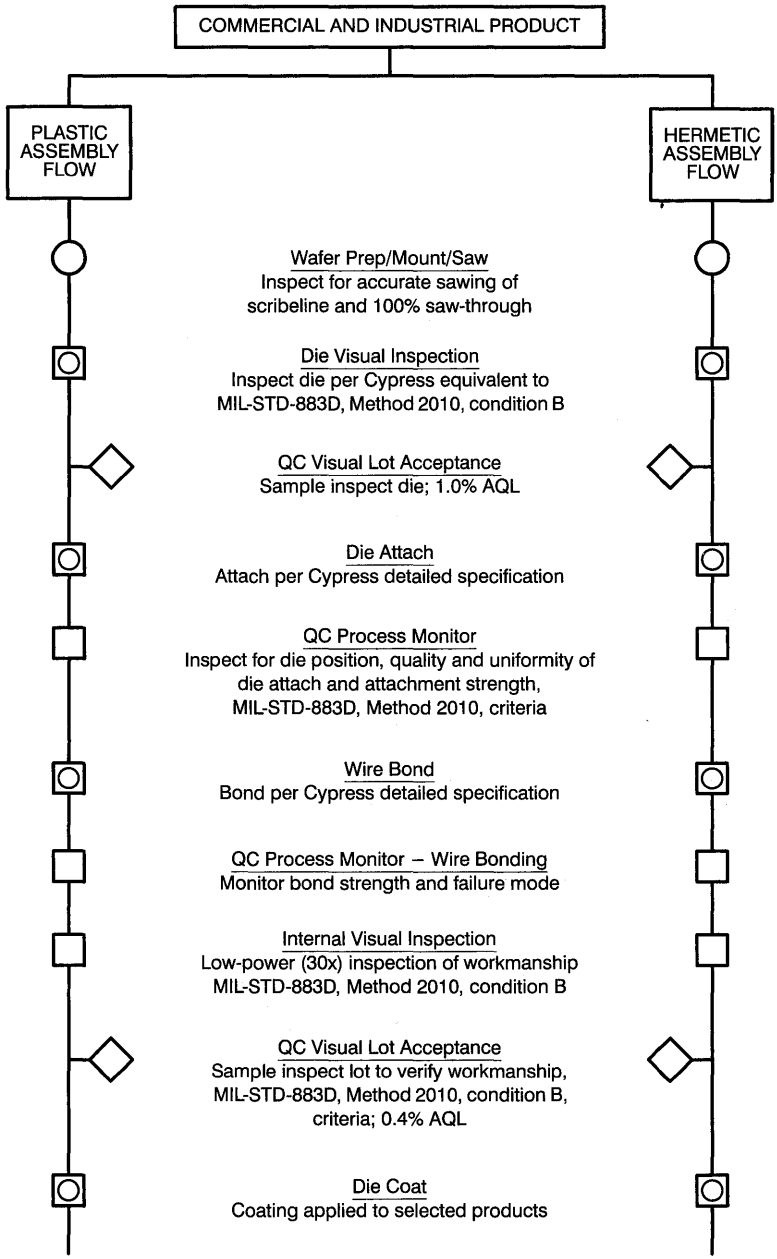
Product Quality Assurance Flow—Components

Area	PROCESS	Process Details
QC	INCOMING MATERIALS INSPECTION	All incoming materials are inspected to documented procedures covering the handling, inspection, storage, and release of raw materials used in the manufacture of Cypress products. Materials inspected are: wafers, masks, leadframes, ceramic packages and/or piece parts, molding compounds, gases, chemicals, etc.
FAB	DIFFUSION/ION IMPLANTATION	Sheet resistance, implant dose, species and CV characteristics are measured for all critical implants on every product run. Test wafers may be used to collect this data instead of actual production wafers. If this is done, they are processed with the standard product prior to collecting specific data. This insures accurate correlation between the actual product and the wafers used to monitor implantation.
FAB	OXIDATION	Sample wafers and sample sites are inspected on each run from various positions of the furnace load to inspect for oxide thickness. Automated equipment is used to monitor pinhole counts for various oxidations in the process. In addition, an appearance inspection is performed by the opeartor to further monitor the oxidation process.
FAB	PHOTOLITHOGRAPHY /ETCHING	Appearance of resist is checked by the operator after the spin operation. Also, after the film is developed, both dimensions and appearance are checked by the operator on a sample of wafers and locations upon each wafer. Final CDs and alignment are also sample inspected on several wafers and sites on each wafer on every product run.
FAB	METALIZATION	Film thickness is monitored on every run. Step coverage cross-sections are performed on a periodic basis to insure coverage.
FAB	PASSIVATION	An outgoing visual inspection is performed on 100% of the wafers in a lot to inspect for scratches, particles, bubbles, etc. Film thickness is verified on a sample of wafers and locations within each given wafer on each run. Pinholes are monitored on a sample basis weekly.
FAB	QC VISUAL OF WAFERS	
FAB	E-TEST	Electrical test is performed for final process electrical characteristics on every wafer.
FAB	QC MONITOR OF E-TEST DATA	Weekly review of all data trends; running averages, minimums, maximums, etc. are reviewed with the process control manager.
TEST	WAFER PROBE/SORT	Verify functionality, electrical characteristics, stress test devices.
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	Pass/fail lot based on yield and correct probe placement.

TO ASSEMBLY AND TEST

(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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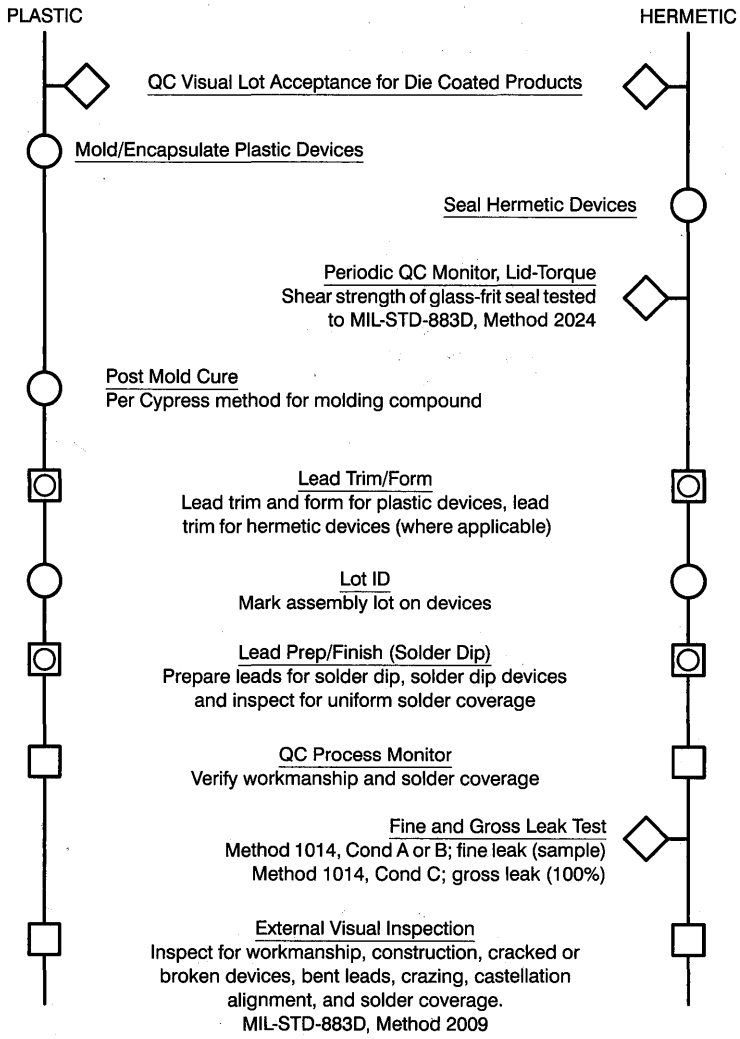
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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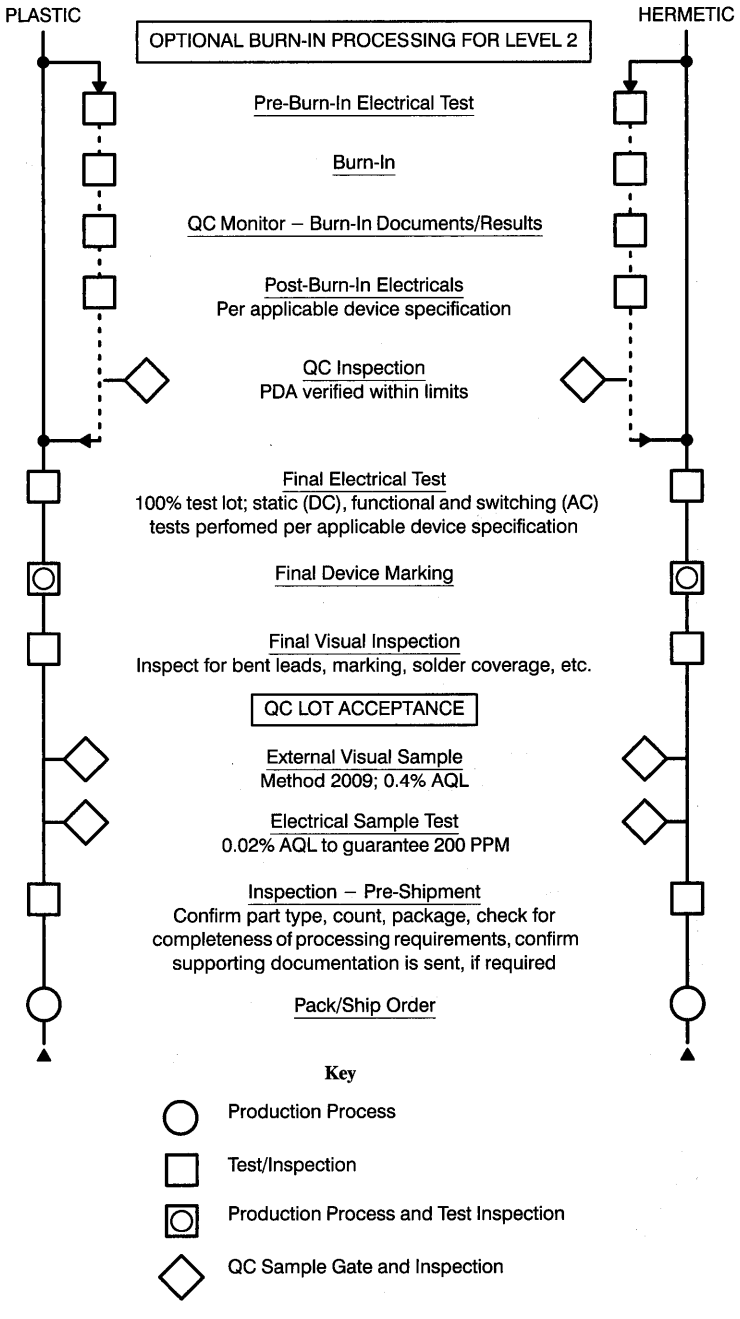
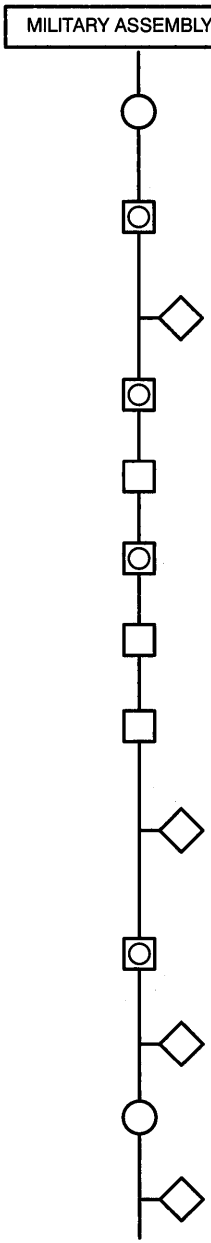
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Components
Military Components



Wafer Prep/Mount/Saw
Inspect for accurate sawing of scribeline and 100% saw-through

Die Visual Inspection
Inspect die per MIL-STD-883D, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect die; 1.0% AQL

Die Attach
Attach per Cypress detailed specification

Die Adherence Monitor
MIL-STD-883D, Method 2019 or Method 2027

Wire Bond
Bond per Cypress detailed specification

Bond Pull Monitor
MIL-STD-883D, Method 2011

Internal Visual Inspection
Low-power and high-power inspection per MIL-STD-883D, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect lot per MIL-STD-883D, Method 2010, condition B, 0.4% AQL

Die Coat
Coating applied to selected products

QC Visual Lot Acceptance for Die Coated Products

Seal

Periodic QC Monitor, Lid-Torque
Shear strength of glass

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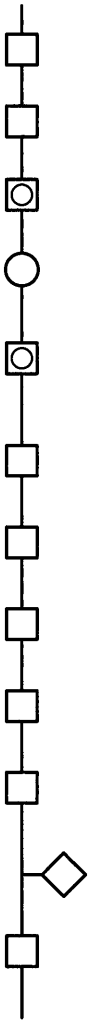
Product Quality Assurance Flow—Components (continued)
Military Components



Temperature Cycle
Method 1010, Cond C, 10 cycles

Constant Acceleration
Method 2001, Cond E, Y1 Orientation

Lead Trim
Lead trim when applicable

Lot ID
Mark assembly lot on devices

Lead Finish
Solder dip or matte tin plate applicable devices and inspect

QC Process Monitor
Verify workmanship and lead finish coverage

External Visual Inspection
Method 2009

Pre-Burn-In Electrical Test
Method 5004, per applicable device specification

Burn-In
Method 1015, condition D

Post-Burn-In Electricals
Method 5004, per applicable device specification

PDA Calculation
Method 5004, 5%

Final Electrical Test
Method 5004; Static, functional and switching tests per applicable device specification

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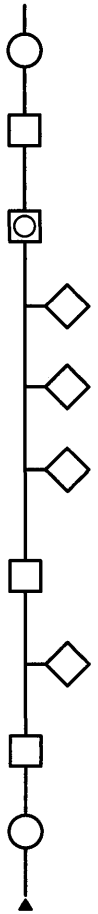
Product Quality Assurance Flow—Components (continued)
Military Components



Lead Finish – Solder Dip
Solder dip applicable devices

Fine and Gross Leak Test
Method 1014, condition A or B, fine leak; condition C, gross leak

Final Device Marking
MIL-STD-883D or applicable device specification

Group B
Method 5005

Group A
Method 5005, per applicable device specification

Group C and D
Method 5005, in accordance with 1.2.1 of MIL-STD-883D; JAN devices in accordance with MIL-M-38510J

External Visual
Method 2009, 100% inspection

External Visual Sample
Method 2009, 0.4% AQL

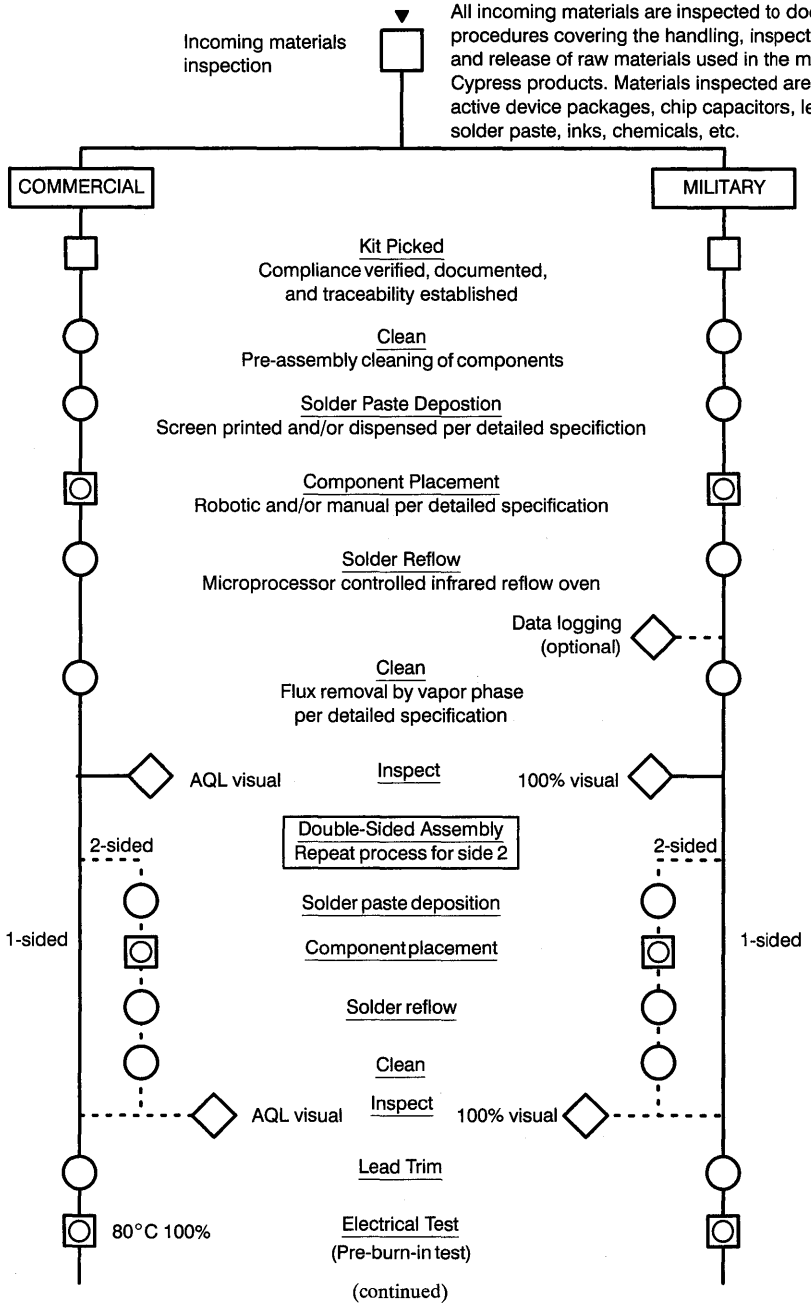
Plant Clearance

Pack/Ship Order

Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Modules



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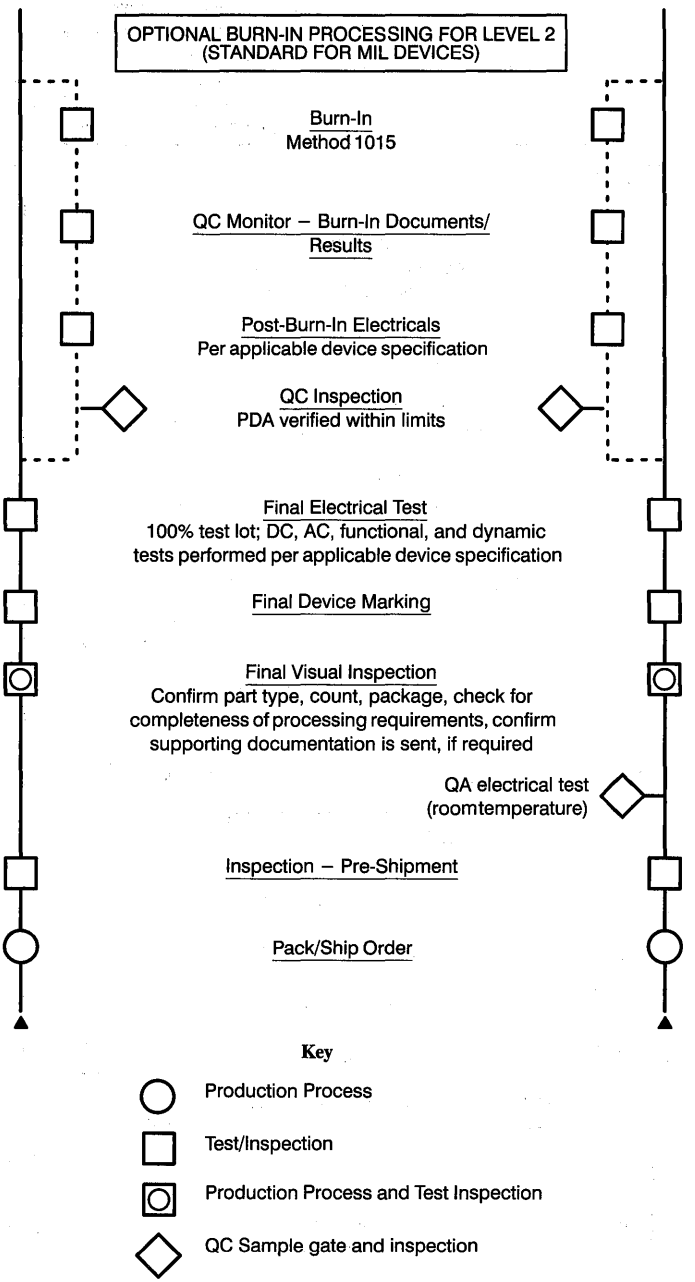
Product Quality Assurance Flow—Modules (continued)



Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008, which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program monitors our most advanced technologies and packages. Every technology produced at a given fabrication site (Tech. – Fab.) and all assembly houses are monitored at least quarterly. If failures occur, detailed failure analyses are performed and corrective actions are implemented. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Quarterly Reliability Monitor Test Matrix

Stress	Devices Tested	# per Quarter
HTOL	Tech. – Fab.	6
	All High Volume	2
HAST	Tech. – Fab.	6
	All High Volume	2
PCT	Plastic Packages	4
TC	Tech. – Fab.	6
	Plastic Packages	3
	Ceramic Packages	5
	All High Volume	2
DRET	FAMOS – San Jose and Texas	2
HTSSL	All Technologies	4
TEV	All Technologies	4
Total		46

Reliability Monitor Test Conditions

Test	Abbrev.	Temp. (°C)	R.H. (%)	Bias	Sample Size	LTPD	Read Points (hrs.)
High-Temperature Operating Life	HTOL	+150	N/A	5.75V Dynamic	116	2	48, 168, 500, 1000
High-Temperature Steady-State Life	HTSSL	+150	N/A	5.75V Static	116	2	48, 168, 500, 1000
Data Retention for Plastic Packages	DRET	+165	N/A	N/A	76	3	168, 1000
Data Retention for Ceramic Packages	DRET2	+250	N/A	N/A	76	3	168, 1000
Pressure Cooker	PCT	+121	100	N/A	76	3	96, 168
Highly Accelerated Stress Test	HAST	+140	85	5.5V Static	76	3	128
Temperature Cycling for Plastic Packages	TC	−40 to +125°C	N/A	N/A	76	3	500, 1000 Cycles
Temperature Cycling for Ceramic Packages	TC2	−65 to +150°C	N/A	N/A	45	5	500, 1000 Cycles
Temperature Extreme Verification	TEV	Commercial Hot & Cold 0 to +70°C	N/A	N/A	116	2	N/A

Tape and Reel Specifications

Description

Surface-mounted devices are packaged in embossed tape and wound onto reels for shipment in compliance with Electronics Industries Association Standard EIA–481 Rev. A.

Specifications

Cover Tape

- The cover tape may not extend past the edge of the carrier tapes
- The cover tape shall not cover any part of any sprocket hole.
- The seal of the cover tape to the carrier tape is uniform, with the seal extending over 100% of the length of each pocket, on each side.
- The force to peel back the cover tape from the carrier tape shall be: 20 gms minimal, 70 gms nominal, 100 gms maximal, at a pull-back speed of 300 ± 10 mm/min.

Loading the Reel

Empty pockets between the first and last filled pockets on the tape are permitted within the following requirements:

- No two consecutive pockets may be left empty
- No more than a total of ten (10) empty pockets may be on a reel

The surface-mount devices are placed in the carrier tape with the leads down, as shown in *Figure 1*.

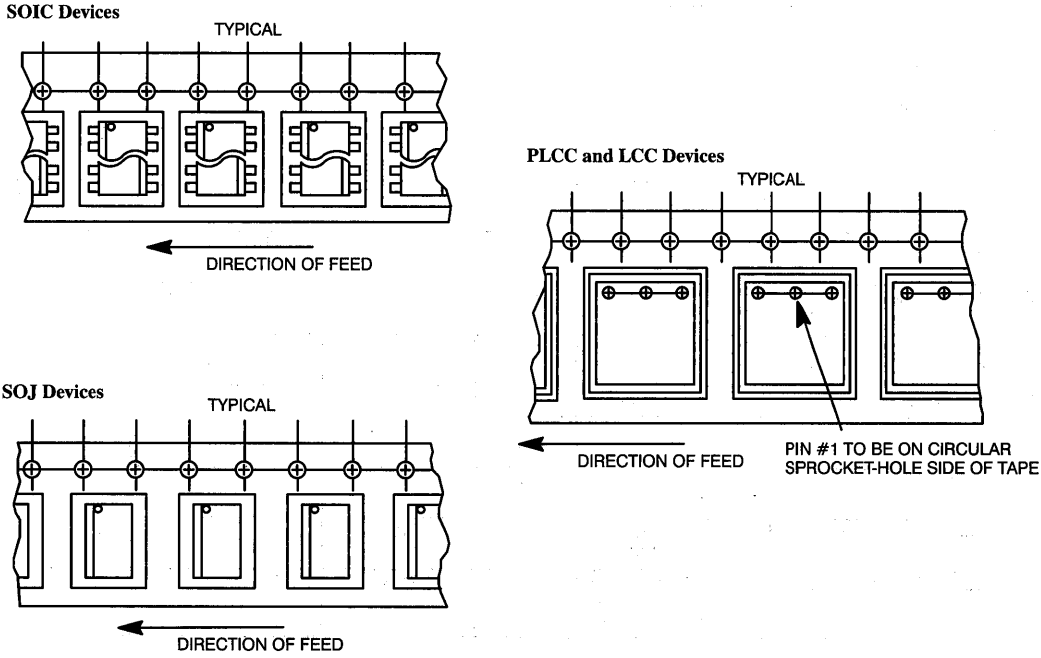


Figure 1. Part Orientation in Carrier Tape

Leaders and Trailers

The carrier tape and the cover tape may not be spliced. Both tapes must be one single uninterrupted piece from end to end.

Both ends of the tape must have empty pockets meeting the following minimum requirements:

- Trailer end (inside hub of reel) is 300 mm minimum
- Leader end (outside of reel) is 500 mm min., 560 mm max.
- Unfilled leader and trailer pockets are sealed
- Leaders and trailers are taped to tape and hub respectively using masking tape

Packaging

- Full reels contain a standard number of units (refer to *Table 1*)
- Reels may contain up to 3 inspection lots.
- Each reel is packed in an anti-static bag and then in its own individual box.
- Labels are placed on each reel as shown in *Figure 2*. The information on the label consists of a minimum of the following information, which complies with EIA 556, "Shipping and Receiving Transaction Bar Code Label Standard":
  - Barcoded Information:
    Customer PO number
    Quantity
    Date code
  - Human Readable Only:
    Package count (number of reels per order)
    Description
    "Cypress–San Jose"
    Cypress p/n
    Cypress CS number (if applicable)
    Customer p/n
- Each box will contain an identical label plus an ESD warning label.

Ordering Information

CY7Cxxx–yyzzz

xxx = part type

yy = speed

zzz = package, temperature, and options

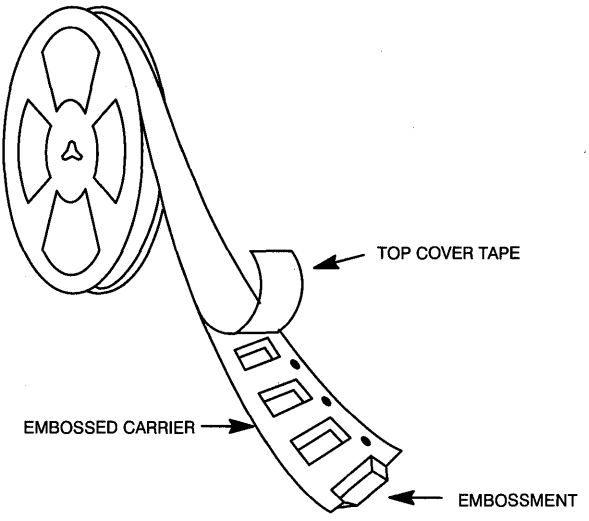
SCT = soic, commercial temperature range
SIT = soic, inductrial temperature range
SCR = soic, commercial temperature plus burn-in
SIR = soic, industrial temperature plus burn-in
VCT = soj, commercial temperature range
VIT = soj, industrial temperature range
VCR = soj, commercial temperature plus burn-in
VIR = soj, industrial temperature plus burn-in
JCT = plcc, commercial temperature range
JIT = plcc, industrial temperature range
JCR = plcc, commercial temperature range plus burn-in
JIR = plcc, industrial temperature range plus burn-in

Notes:

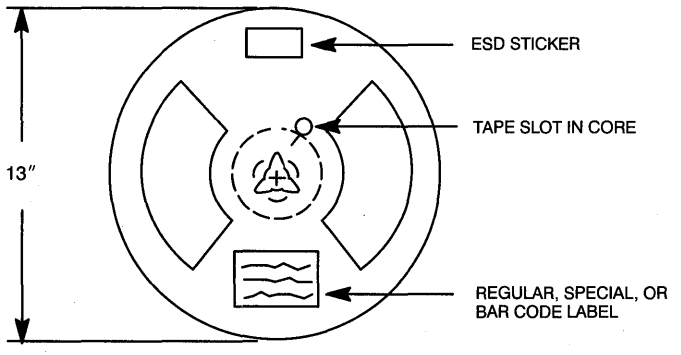
1. The T or R suffix will not be marked on the device. Units will be marked the same as parts in a tube.
2. Order releases must be in full-reel multiples as listed in *Table 1.*

Table 1. Parts Per Reel and Tape Specifications

Package Type	Terminals	Carrier Width (mm)	Pocket Pitch	Parts Per Meter	Parts Per Full Reel
PLCC	18	24	3	83.3	750
	20	16	3	83.3	750
	28(S)	24	4	62.5	500
	32	24	4	62.5	500
	44	32	6	41.6	400
	52	32	6	41.6	400
	68	44	8	31.2	250
	84	44	8	31.2	250
SOIC	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000
SOJ	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000



Tape and Reel Shipping Medium



Label Placement

Figure 2. Shipping Medium and Label Placement

Section Contents

Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (see *Figure 1*).

Typical activation energies for commonly observed failure mechanisms in CMOS devices are shown in *Table 1*.

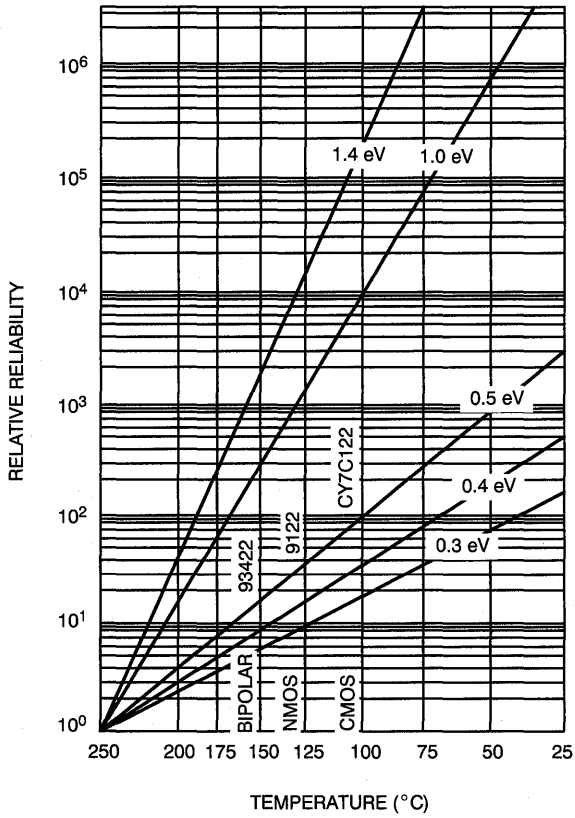


Figure 1. Arrhenius plot, which assumes a failure rate proportional to EXP ($-E_A/kT$) where E_A is the activation energy for the particular failure mechanism

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (Eq)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5–1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power-generating CMOS device fabrication process and their high-heat-dissipation packaging capabilities. *Table 2* demonstrates this optimized thermal performance by comparing bipolar, NMOS, and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I_{CC} (mA)	150	110	60
V_{CC} (V)	5.0	5.0	5.0
P_{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Datasheet P_{MAX}[1]	160	136	91

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0-eV activation energy failure mechanism, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device, and more than one order of magnitude (30x) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside it to the ambient.

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation is room temperature to 70°C.

T_J = Junction temperature of the IC chip.

T_C = Temperature of the case (package).

P = Power at which the device operates.

θ_{JC} = Junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package.

θ_{JA} = Junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment.

θ_{CA} = Case-to-ambient thermal resistance. This is mainly dependent on the surface area available for convection and radiation and the ambient conditions among other factors. This can be controlled at the user end by using heat sinks providing greater surface area and better conduction path or by air or liquid cooling.

Thermal Resistance: Finite Element Model

θ_{JC} and θ_{JA} values given in the following figures and listed in the following tables have been obtained by simulation using the Finite element software ANSYS[2]. SDRC-IDEAS Pre and Post processor software[3] was used to create the finite element model of the packages and the ANSYS input data required for analysis.

SEMI Standard (Semiconductor Equipment and Materials International) method SEMI G30-88[4] states "heat sink" mounting technique to be the "reference" method for θ_{JC} estimation of ceramic packages. Accordingly, θ_{JC} of packages has been obtained by applying the boundary conditions that correspond to the heat sink mounted on the packages in the simulation.

For θ_{JA} evaluation, SEMI standard specification SEMI G38-87 suggests using a package-mounting arrangement that approximates the application environment. So, in evaluating the θ_{JA}, package on-board configuration is assumed.

Notes:

1. $T_{ambient} = 70°C$
2. *ANSYS Finite Element Software User Guides*
3. *SDRC-IDEAS Pre and Post Processor User Guide*
4. *SEMI International Standards*, Vol. 4, Packaging Handbook, 1989.

Model Description

- One quarter of the package is mounted on a FR-4 PC board.
- Leads have been modeled as a continuous metallic plane, and equivalent thermal properties have been used to account for the plastic (or the glass in the case of ceramic packages) that fills the space between the leads.
- 1W power dissipation over the entire chip is assumed.
- 70°C ambient condition is considered.

Comparison of Simulation Data with Measured Data

In the case of ceramic packages, it is not unusual to see significant differences in θ_{JC} values when a heat sink is used in the place of fluid bath.[5] However, SEMI G30-88 test method recommends the heat sink configuration for θ_{JC} evaluation.

θ_{JA} values from simulation compare within 12 percent of the measured values. θ_{JA} values obtained from simulation seem to be *conservative* with an accuracy of about +12 percent.

Measured values given in *Table 3* used the Temperature Sensitive Parameter method described in MIL-STD-883C, method 1012.1. The junction-to-ambient measurement was made in a still-air environment where the device was inserted into a low-cost standard-device socket and mounted on a standard 0.062" G10 PC board.

Table 3. 24-Lead Ceramic and Plastic DIPs

Package	Cavity/PAD Size (mils)	θ_{JA} (°C/W)		
		Measured	Simulation	% Diff.
24LCDIP[6]	170 x 270	64	67	5
24LPDIP[7]	160 x 210	72	82	12

Thermal Resistance of Packages with Forced Convection Air Flow

One of the methods adopted to cool the packages on PC boards at the system level is to used forced air (fans) specified in linear feet per minute or LFM. This helps reduce the device operating temperature by lowering the case to ambient thermal resistance. Available surface area of the package and the orientation of the package with respect to the air flow affect the reduction of thermal resistance that can be achieved. A general rule of thumb is:

- For plastic packages:
  - 200 LFM air flow can reduce θ_{JA} by 20 to 25%
  - 500 LFM air flow can reduce θ_{JA} by 30 to 40%
- For ceramic packages:
  - 200 LFM air flow can reduce θ_{JA} by 25 to 30%
  - 500 LFM air flow can reduce θ_{JA} by 35 to 45%

If θ_{JA} for a package in still air (no air flow) is known, approximate values of thermal resistance at 200 LFM and 500 LFM can be estimated. For estimation, the factors given in *Table 4* can be used as a guideline.

Table 4. Factors for Estimating Thermal Resistance

Package Type	Air Flow Rate (LFM)	Multiplication Factor
Plastic	200	0.77
Plastic	500	0.66
Ceramic	200	0.72
Ceramic	500	0.60

Example:

θ_{JA} for a plastic package in still air is given to be 80°C/W. Using the multiplication factor from *Table 4*:

- θ_{JA} at 200 LFM is (80 x 0.77) = 61.6°C/W
- θ_{JA} at 500 LFM is (80 x 0.66) = 52.8°C/W

θ_{JA} for a ceramic package in still air is given to be 70°C/W. Using *Table 4*:

- θ_{JA} at 200 LFM is (70 x 0.72) = 50.4°C/W
- θ_{JA} at 500 LFM is (70x0.60) = 42.0°C/W

Presentation of Data

The following figures and tables present the data taken using the aforementioned procedures. The thermal resistance values of Cypress standard packages are graphically illustrated in *Figures 2* through *6*. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary=5000 mils^2, lower boundary = 100,000 mils^2) in their thermally optimized packaging environments. These graphs should be used in conjunction with *Table 10*, which lists the die sizes of Cypress devices.

Tables 5 through *9* give the thermal resistance values for other package types not included in the graphs. The letter in the header (*D, P, J*, etc.) of these tables refer to the package designators as detailed in the Package Diagrams section of this catalog. The numeric values given in the table (e.g., 20.3) refer to the lead count (20) and package width in inches (.3). If no decimal appears, the reader must refer to the package diagrams.

Packaging Materials

Cypress plastic packages incorporate

- High thermal conductivity copper lead frame
- Molding compound with high thermal conductivity
- Gold bond wires

Cypress cerDIP packages incorporate

- High conductivity alumina substrates
- Silver-filled glass as die attach material
- Alloy 42-lead frame
- Aluminum bond wires
- Silver-filled conductive epoxy as die attach material

Notes:

5. "Thermal resistance measurements and finite calculations for ceramic hermetic packages." James N. Sweet et. al., *SEMI-Therm*, 1990.
6. 24LCDIP = 24-lead cerDIP
7. 24LPDIP = 24-lead plastic DIP

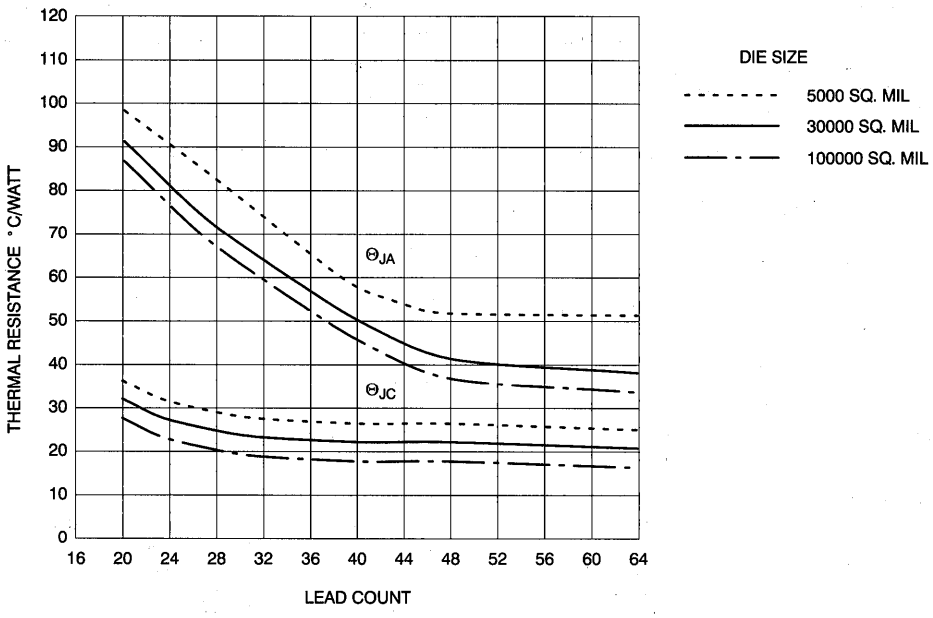


Figure 2. Thermal Resistance of Cypress Plastic DIPs (Package type "P")

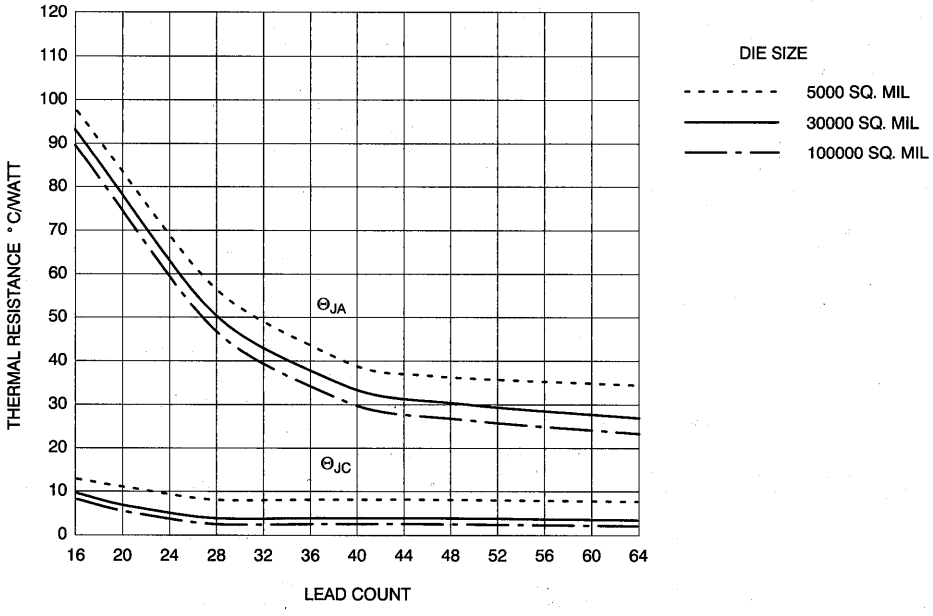


Figure 3. Thermal Resistance of Cypress Ceramic DIPs (Package type "D" and "W")

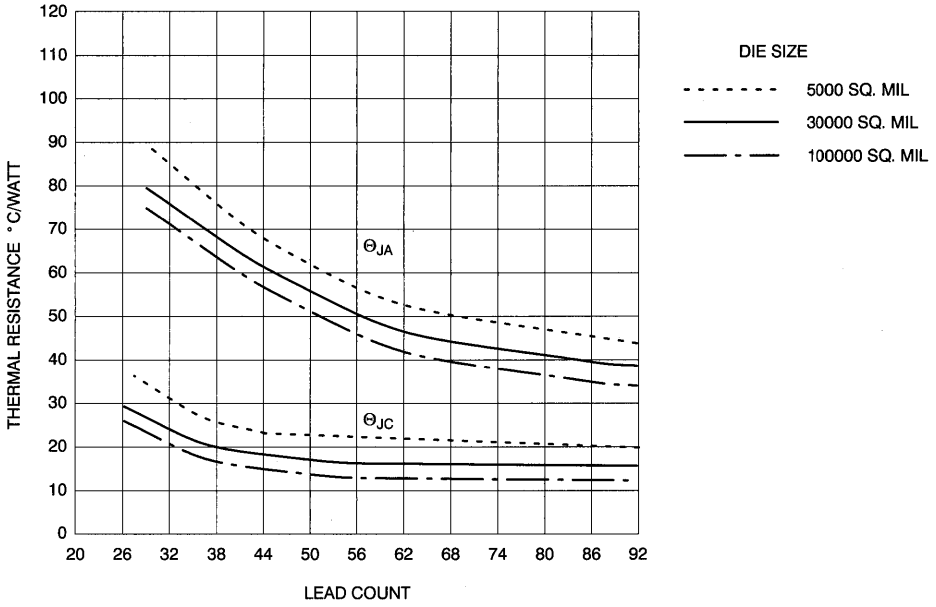


Figure 4. Thermal Resistance of Cypress PLCCs (Package type "J")

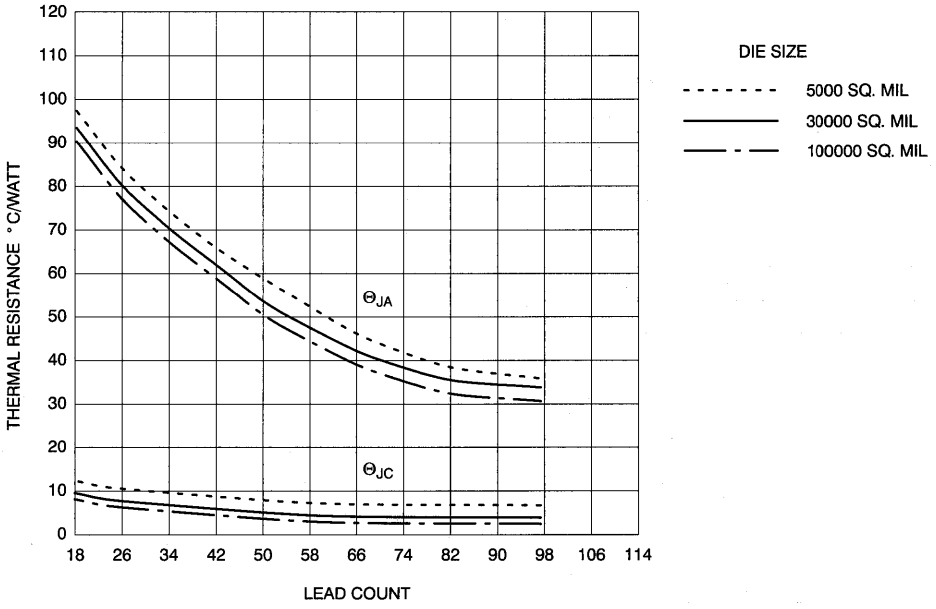


Figure 5. Thermal Resistance of Cypress LCCs (Package type "L" and "Q")

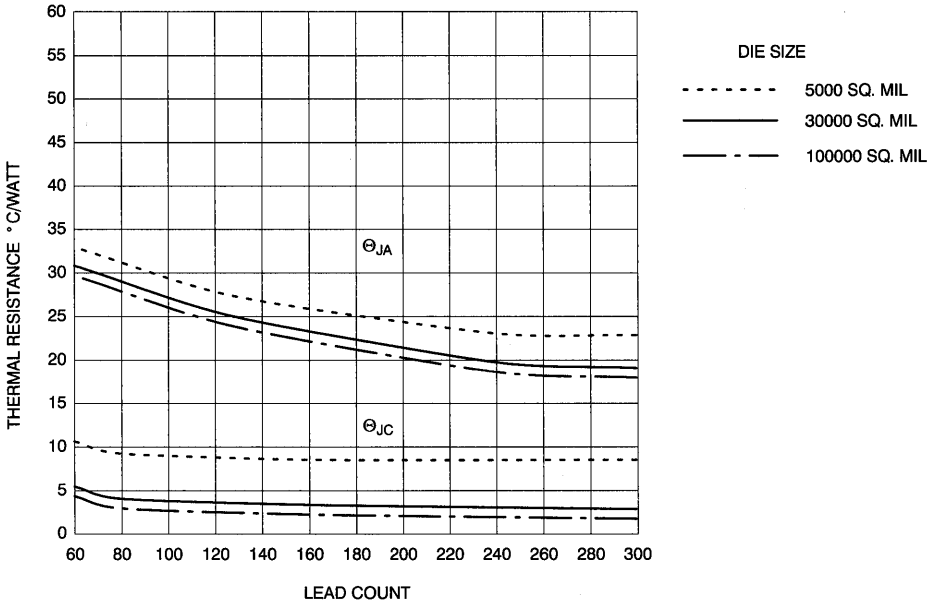


Figure 6. Thermal Resistance of Cypress Ceramic PGAs

Table 5. Plastic Surface Mount SOIC, SOJ[8,9]

Package Type "S" and "V"	Paddle Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 170	Copper	98 x 84	8,232	19.0	120
18	140 x 170	Copper	98 x 84	8,232	18.0	116
20	180 x 250	Copper	145 x 213	30,885	17.0	105
24	180 x 250	Copper	145 x 213	30,885	15.4	88
24	170 x 500	Copper	141 x 459	64,719	14.9	85
28	170 x 500	Copper	145 x 213	30,885	16.7	84
28	170 x 500	Copper	141 x 459	64,719	14.4	80

Table 6. Plastic Quad Flatpacks

Package Type "N"	LF Material	Paddle Size (mil)	Die Size (mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
100	Copper	310 x 310	235 x 235	17	51
144	Copper	310 x 310	235 x 235	18	41
160	Copper	310 x 310	230 x 230	18	40
184	Copper	460 x 460	322 x 311	15	38.5
208	Copper	400 x 400	290 x 320	16	39

Notes:
8. The data in *Table 6* was simulated for SOIC packaging.
9. SOICs and SOJs have very similar thermal resistance characteristics. The thermal resistance values given above apply to SOJ packages also.

Table 7. Ceramic Quad Flatpacks

Package Type "H" and "Y"	Cavity Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
28	250 x 250	Alloy 42	123 x 162	19,926	9.2	96
28	250 x 250	Alloy 42	150 x 180	27,000	8.9	93
32	316 x 317	Alloy 42	198 x 240	47,520	7.5	72
44	400 x 400	Alloy 42	310 x 250	77,500	5.9	55
52	400 x 400	Alloy 42	250 x 310	77,500	5.9	55
68	400 x 400	Alloy 42	310 x 250	77,500	5.4	33
84	450 x 450	Alloy 42	310 x 250	77,500	5.4	29

Table 8. Cerpacks

Package Type "K" and "T"	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 200	Alloy 42	100 x 118	11,800	10	107
18	140 x 200	Alloy 42	100 x 118	11,800	10	104
20	180 x 265	Alloy 42	128 x 170	21,760	9	102
24	170 x 270	Alloy 42	128 x 170	21,760	10	102
28	210 x 210	Alloy 42	150 x 180	27,000	9	98
32	210 x 550	Alloy 42	141 x 459	64,719	7	81

Table 9. Miscellaneous Packaging

Package Type	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
24 VDIP[10]	500 x 275	Alloy 42	145 x 213	30,885	6	57
68 CPGA[11]	350 x 350	Kovar Pins	323 x 273	88,179	3	28

Notes:
10. VDIP = "PV" package.
11. CPGA = "G" package.

Table 10. Die Sizes of Cypress Devices

Part Number	Size (mil^2)
SRAMs	
CY2147	10132
CY2148	9983
CY2149	9983
CY27LS03	4130
CY27S03A	4130
CY27S07A	4130
CY6116	20007
CY6116A	20007
CY6117	20007
CY6117A	20007
CY74S189	4130

Part Number	Size (mil^2)
CY7B134	76152
CY7B1342	76152
CY7B135	76152
CY7B138	76152
CY7B139	76152
CY7B144	76152
CY7B145	76152
CY7B160	27244
CY7B161	27244
CY7B162	27244
CY7B164	27244
CY7B166	27244

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
CY7B173	102200
CY7B174	102200
CY7B180	54600
CY7B181	54600
CY7B185	27244
CY7B186	27244
CY7B191	73152
CY7B192	73152
CY7B194	73152
CY7C122	6300
CY7C123	6300
CY7C128	20007
CY7C128A	17400
CY7C130	36636
CY7C131	36636
CY7C132	36636
CY7C136	36636
CY7C140	36636
CY7C141	36636
CY7C142	36636
CY7C146	36636
CY7C147	10132
CY7C148	9983
CY7C149	9983
CY7C150	6634
CY7C157	86460
CY7C161A	30885
CY7C162A	30885
CY7C164A	30885
CY7C166A	30885
CY7C167	21228
CY7C167A	21228
CY7C168	21228
CY7C168A	21228
CY7C169	21228
CY7C169A	21228
CY7C170	21228
CY7C170A	21228
CY7C171	21228

Part Number	Size (mil^2)
CY7C171A	21228
CY7C172	21228
CY7C172A	21228
CY7C183	65636
CY7C184	65636
CY7C185	30885
CY7C186	30885
CY7C187	30885
CY7C189	4130
CY7C190	4130
CY7C191	68150
CY7C192	68150
CY7C194	68150
CY7C196	68150
CY7C197	68150
CY7C198	68150
CY7C199	68150
CY7C191 (RAM2.5)	51590
CY7C192 (RAM2.5)	51590
CY7C194 (RAM2.5)	51590
CY7C196 (RAM2.5)	51590
CY7C197 (RAM2.5)	51590
CY7C198 (RAM2.5)	51590
CY7C199 (RAM2.5)	51590
CY7C9122	6300
CY93422A	6300
PROMs	
CY7C225	11815
CY7C235	13900
CY7C245	19321
CY7C245A	9394
CY7C251	49536
CY7C254	49536
CY7C261	28290
CY7C263	28290
CY7C264	28290
CY7C265	28290
CY7C266	28290
CY7C268	29400

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
CY7C269	29400
CY7C271	38750
CY7C274	38750
CY7C277	38750
CY7C279	38750
CY7C281	13900
CY7C282	13900
CY7C285	43875
CY7C286	43875
CY7C287	43875
CY7C289	43875
CY7C291	19182
CY7C291A	9394
CY7C292	19321
CY7C292A	9394
CY7C293A	9394
PLDs	
CY7C330	20088
CY7C331	16536
CY7C332	19116
CY7C335	23111
CY7C341	136320
CY7C342	83475
CY7C342B	49104
CY7C343	43953
CY7C344	21977
CY7C361	25872
PAL16L8	13552
PAL16R4	13552
PAL16R6	13552
PAL16R8	13552
PAL22V10C	18834
PAL22VP10C	18834
PALC16L8	9700
PALC16R4	9700
PALC16R6	9700

Part Number	Size (mil^2)
PALC16R8	9700
PALC22V10	19926
PALC22V10B	13284
PALC22V10D	12954
PLD20G10C	18834
PLDC18G8	7744
PLDC20G10	19926
PLDC20G10B	13284
PLDC20RA10	13284
FIFOs	
CY3341	8064
CY7C401	8064
CY7C402	8064
CY7C403	8064
CY7C404	8064
CY7C408A	16268
CY7C409A	16268
CY7C420	41019
CY7C421	41019
CY7C424	41019
CY7C425	41019
CY7C428	41019
CY7C429	41019
CY7C432	50040
CY7C433	50040
CY7C439	47160
CY7C441	44756
CY7C443	44756
CY7C451	44756
CY7C453	44756
CY7C460	89445
CY7C462	89445
CY7C464	89445
CY7C470	89445
CY7C472	89445
CY7C474	89445

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
Logic	
CY2909A	7968
CY2910A	21750
CY2911A	7968
CY7C2901	11800
CY7C510	30704
CY7C516	29000
CY7C517	29000
CY7C901	11800
CY7C909	7968
CY7C910	21750
CY7C9101	36108
CY7C911	7968

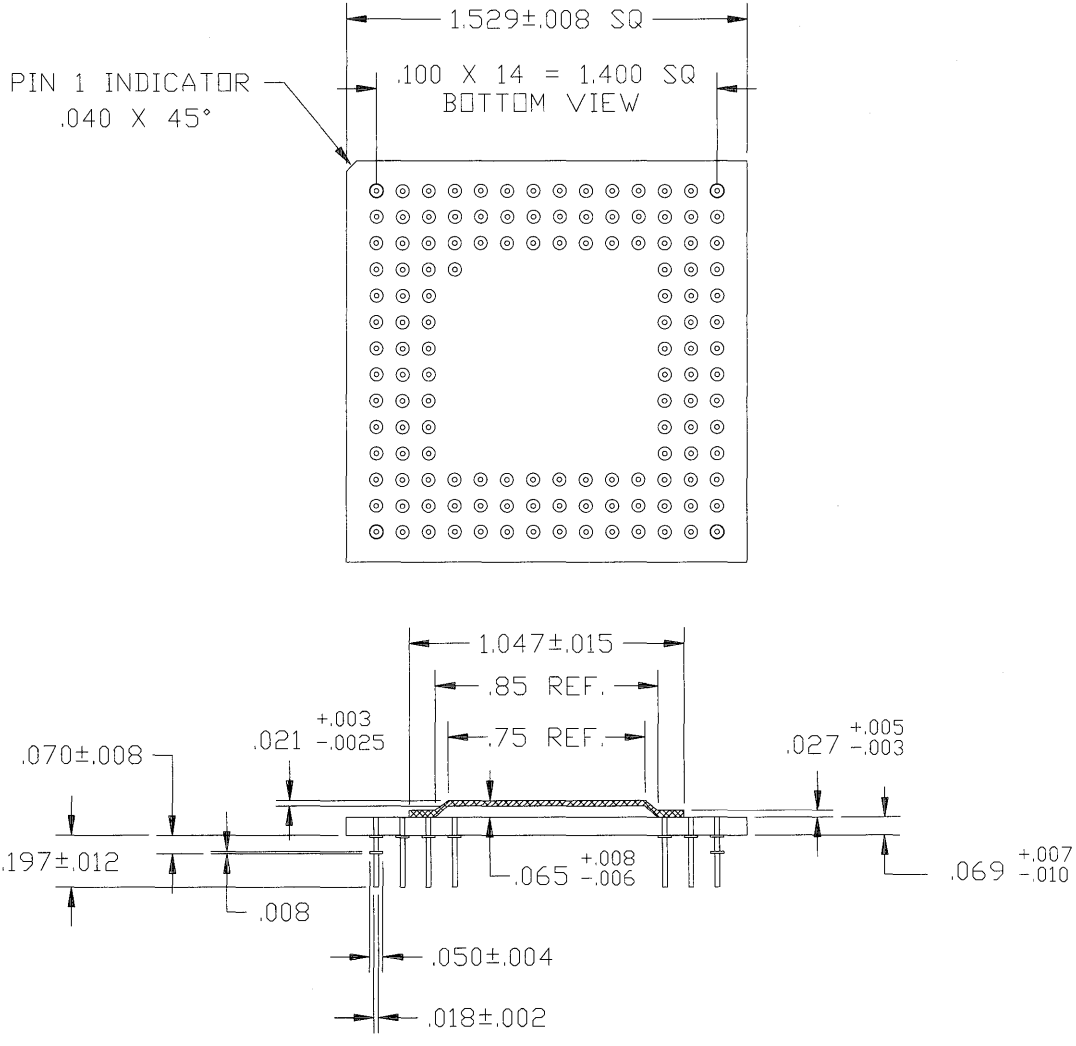
Part Number	Size (mil^2)
ECL	
CY100E301L	14875
CY100E302L	14875
CY100E422	6960
CY100E474	10830
CY100E494	29575
CY10E301L	14875
CY10E302L	14875
CY10E422	6960
CY10E474	10830
CY10E494	29575
Bus Interface	
CY7C964	21460
VAC068	101060
VIC068A	103620
VIC64	103620

Document #: 38–00190

Package Diagrams

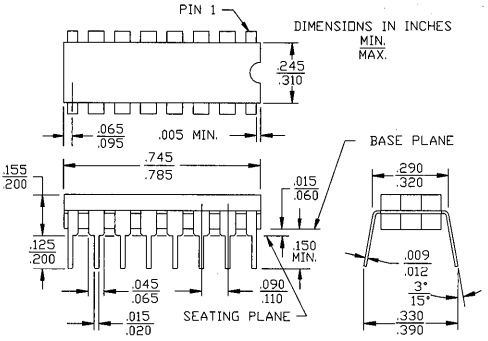
Plastic Pin Grid Arrays

145-Pin Plastic Grid Array (Cavity Up) B144

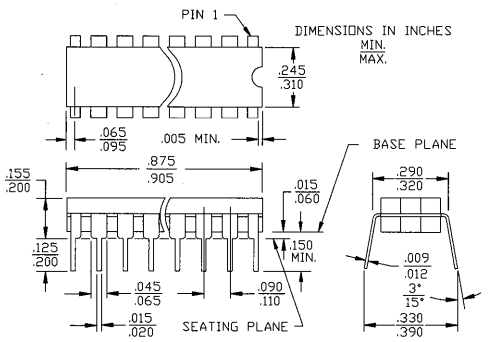


Ceramic Dual-In-Line Packages

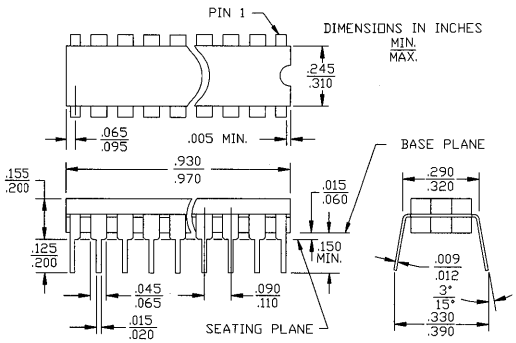
16-Lead (300-Mil) CerDIP D2
MIL–STD–1835 D–2 Config. A



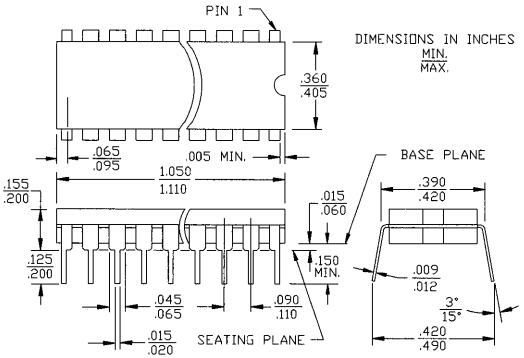
18-Lead (300-Mil) CerDIP D4
MIL–STD–1835 D–8 Config. A



20-Lead (300-Mil) CerDIP D6
MIL–STD–1835 D–8 Config. A

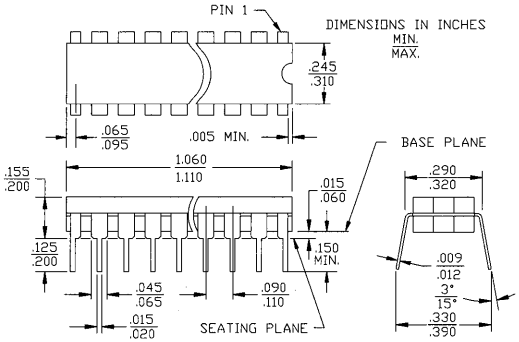


22-Lead (400-Mil) CerDIP D8
MIL–STD–1835 D–7 Config. A

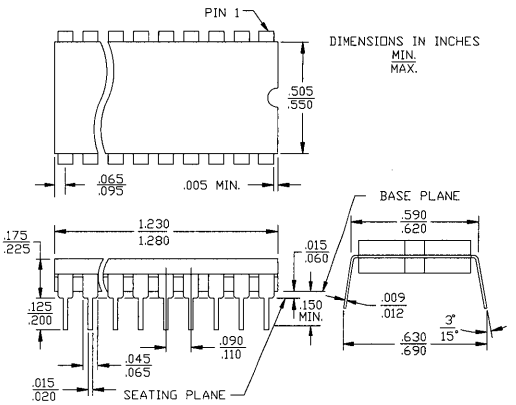


Ceramic Dual-In-Line Packages (continued)

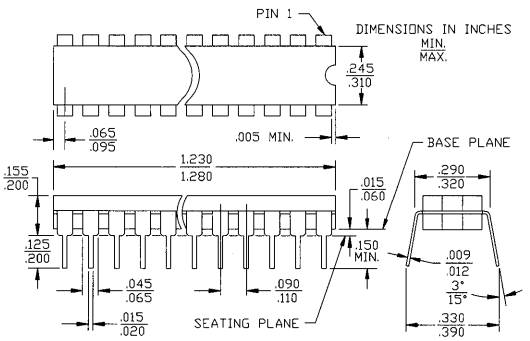
22-Lead (300-Mil) CerDIP D10



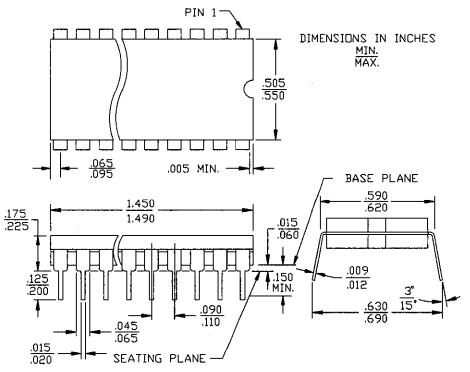
24-Lead (600-Mil) CerDIP D12
MIL–STD–1835 D–3 Config. A



24-Lead (300-Mil) CerDIP D14
MIL–STD–1835 D–9 Config. A

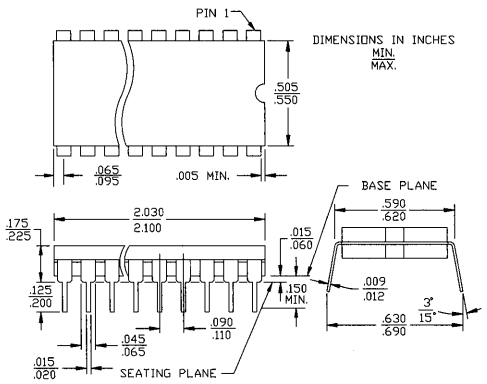


28-Lead (600-Mil) CerDIP D16
MIL–STD–1835 D–10 Config. A

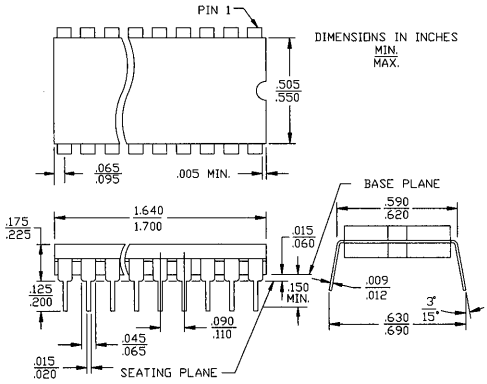


Ceramic Dual-In-Line Packages (continued)

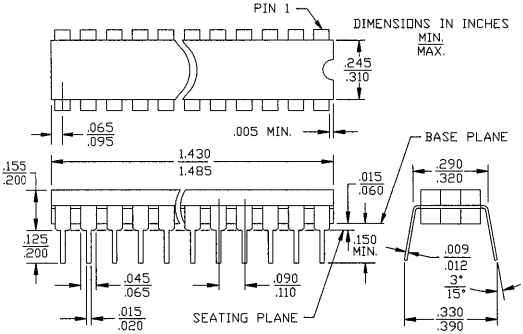
40-Lead (600-Mil) CerDIP D18
MIL–STD–1835 D–5 Config. A



32-Lead (600-Mil) CerDIP D20

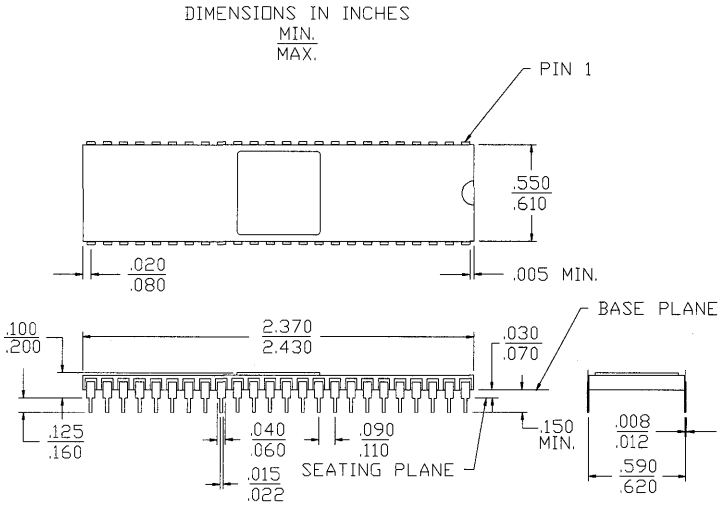


28-Lead (300-Mil) CerDIP D22
MIL–STD–1835 D–15 Config. A

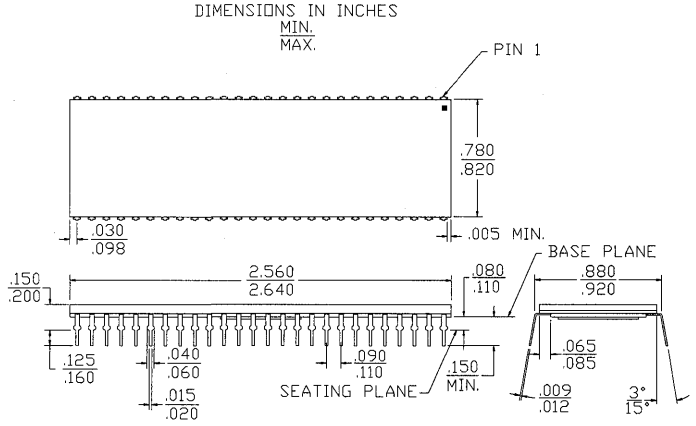


Ceramic Dual-In-Line Packages (continued)

48-Lead (600-Mil) Sidebraze DIP D26
MIL–STD–1835 D–14 Config. C

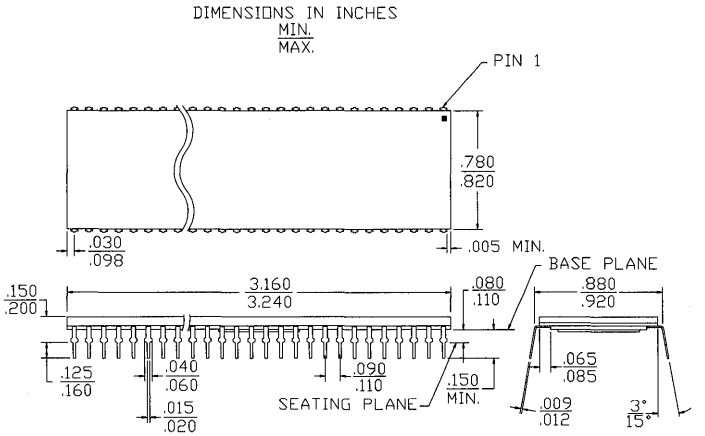


52-Lead (900-Mil) Bottombraze DIP D28

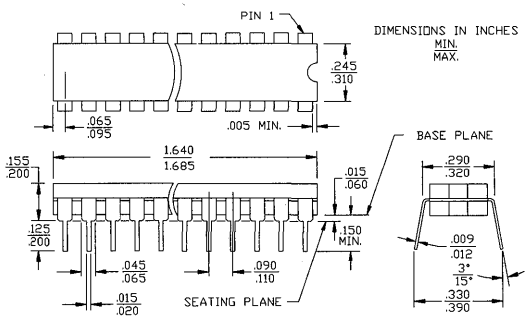


Ceramic Dual-In-Line Packages (continued)

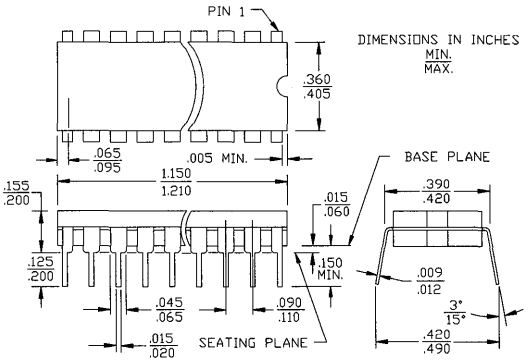
64-Lead (900-Mil) Bottombraze DIP D30



32-Lead (300-Mil) CerDIP D32

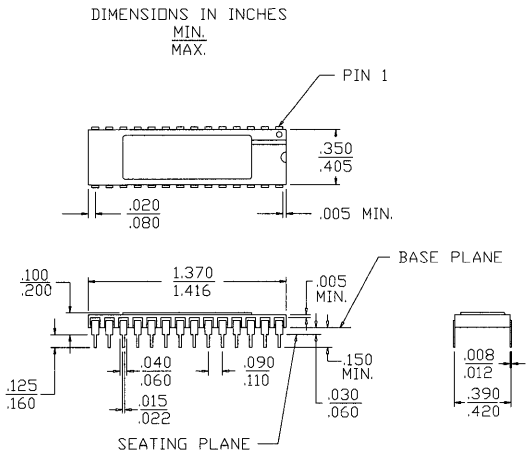


24-Lead (400-Mil) Sidebraze DIP D40
MIL–STD–1835 D–11 Config. A

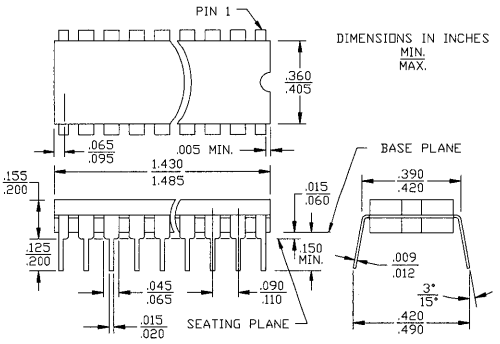


Ceramic Dual-In-Line Packages (continued)

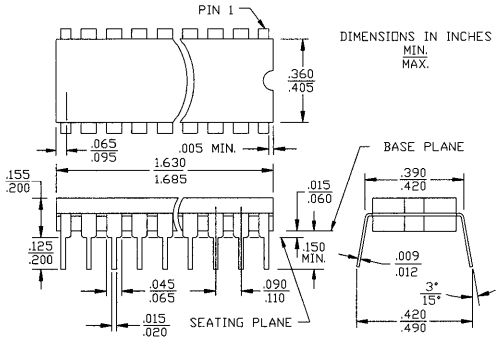
28-Lead (400-Mil) Sidebraze DIP D41



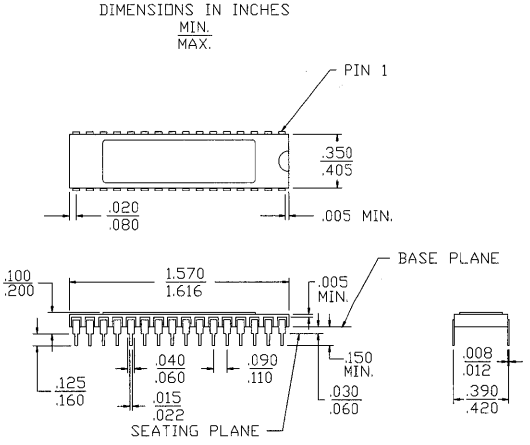
28-Lead (400-Mil) CerDIP D42



32-Lead (400-Mil) CerDIP D44

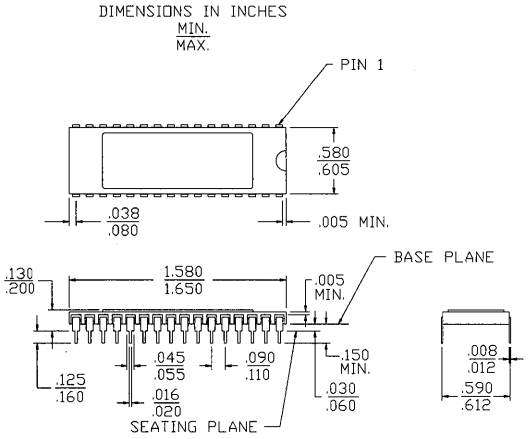


32-Lead (400-Mil) Sidebraze DIP D46



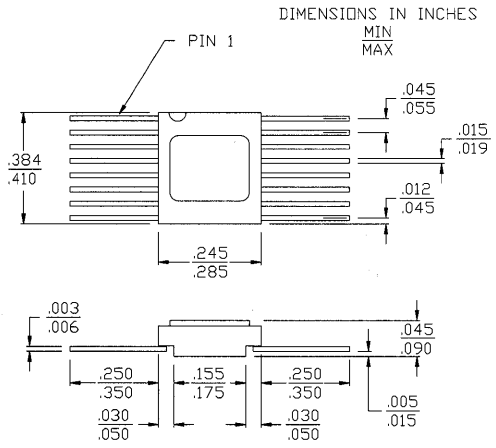
Ceramic Dual-In-Line Packages (continued)

32-Lead (600-Mil) Sidebraze DIP D50

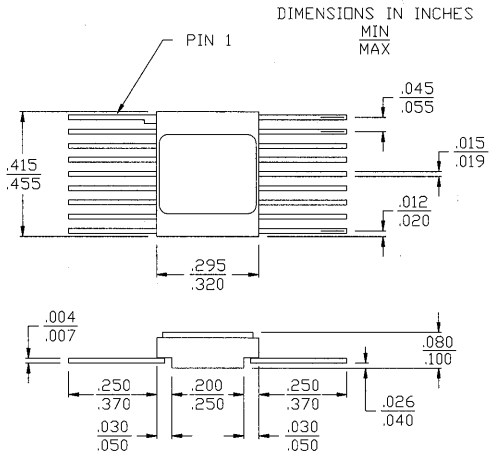


Ceramic Flatpacks

16-Lead Rectangular Flatpack F69
MIL–STD–1835 F–5 Config. B

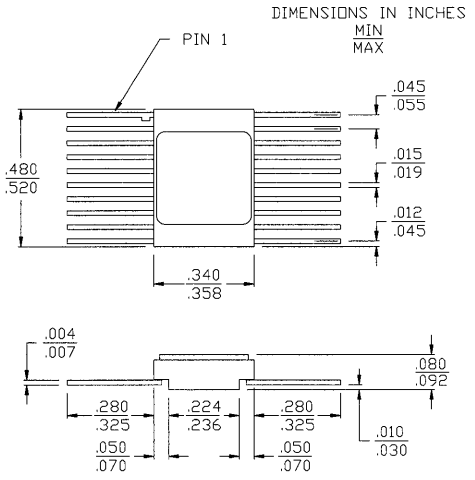


18-Lead Rectangular Flatpack F70

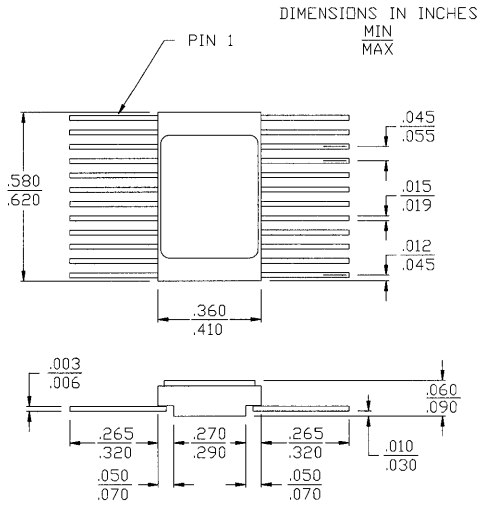


Ceramic Flatpacks (continued)

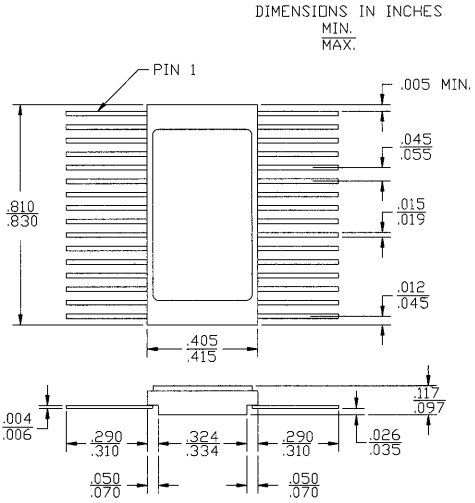
20-Lead Rectangular Flatpack F71



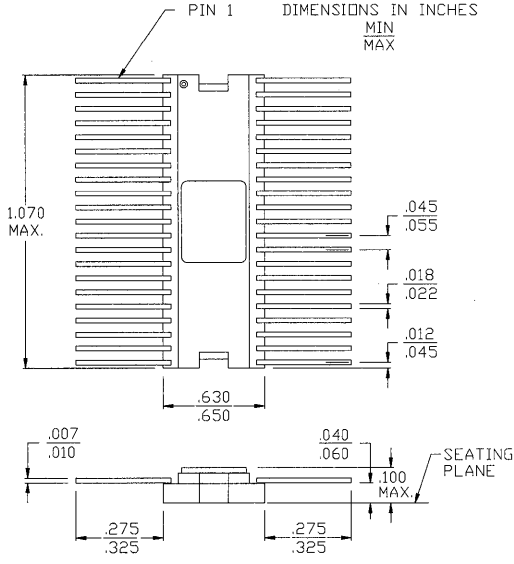
24-Lead Rectangular Flatpack F73
MIL–STD–1835 F–6 Config. B



32-Lead Rectangular Flatpack F75

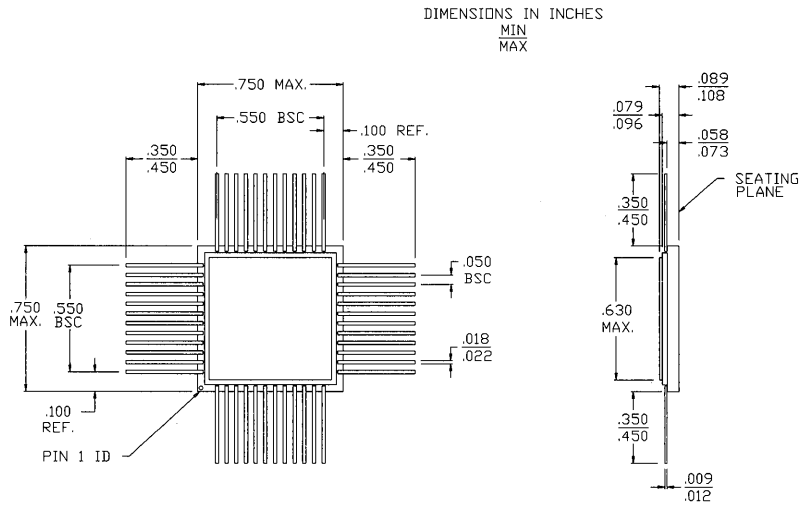


42-Lead Rectangular Flatpack F76

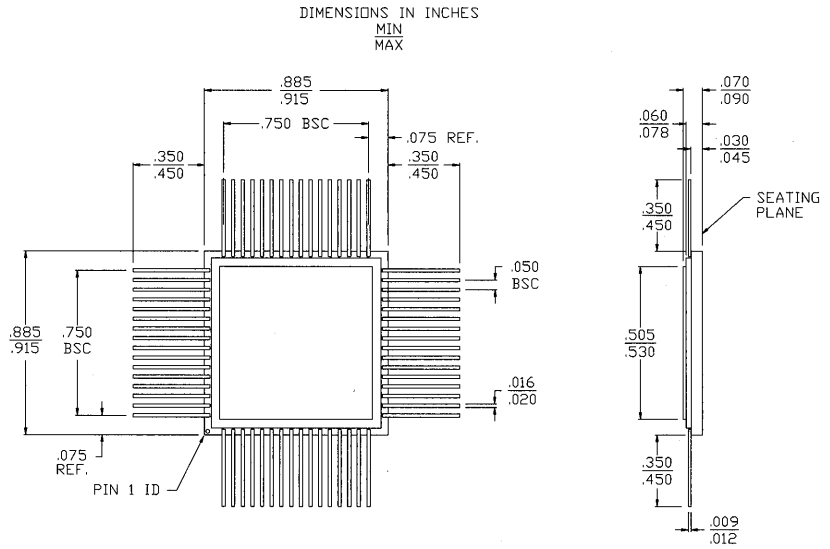


Ceramic Flatpacks (continued)

48-Lead Quad Flatpack F78

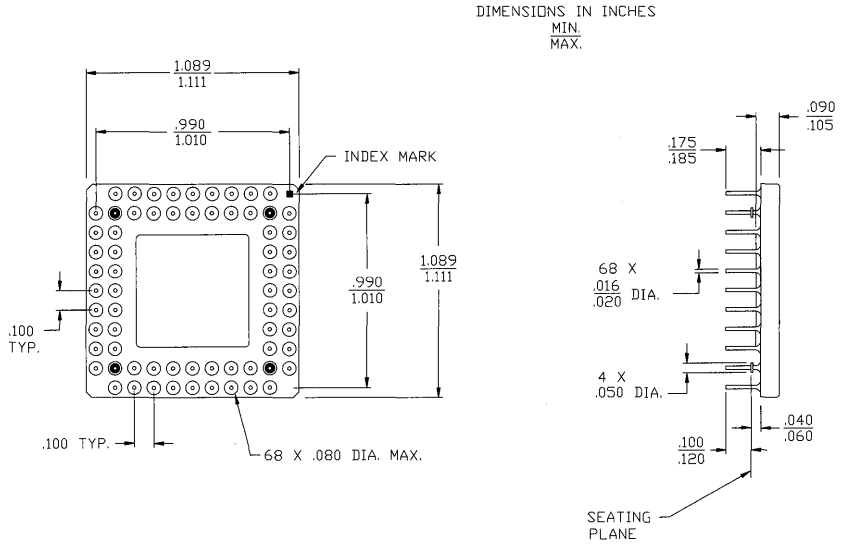


64-Lead Quad Flatpack F90

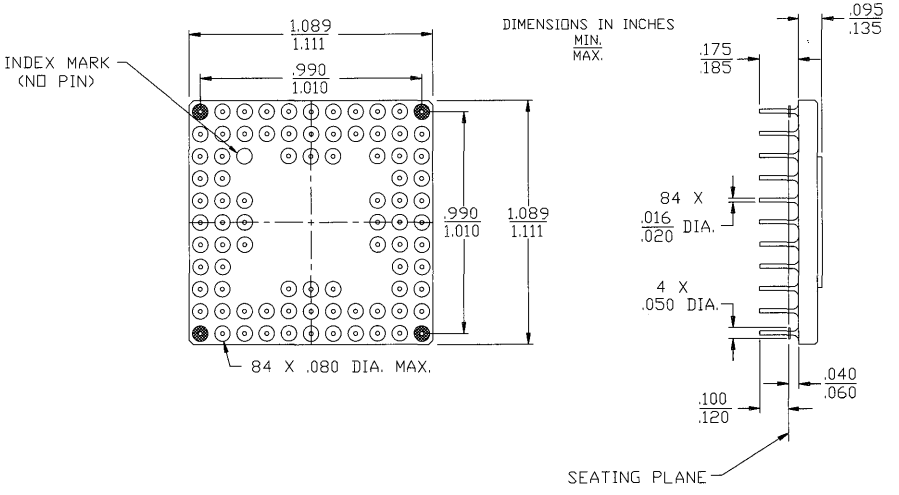


Ceramic Pin Grid Arrays

68-Pin Grid Array (Cavity Down) G68

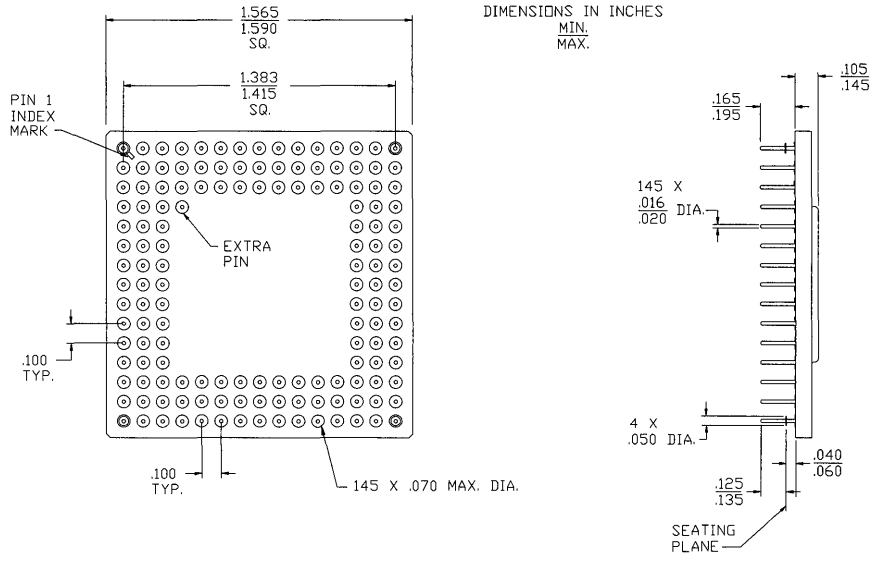


84-Pin Grid Array (Cavity Up) G84

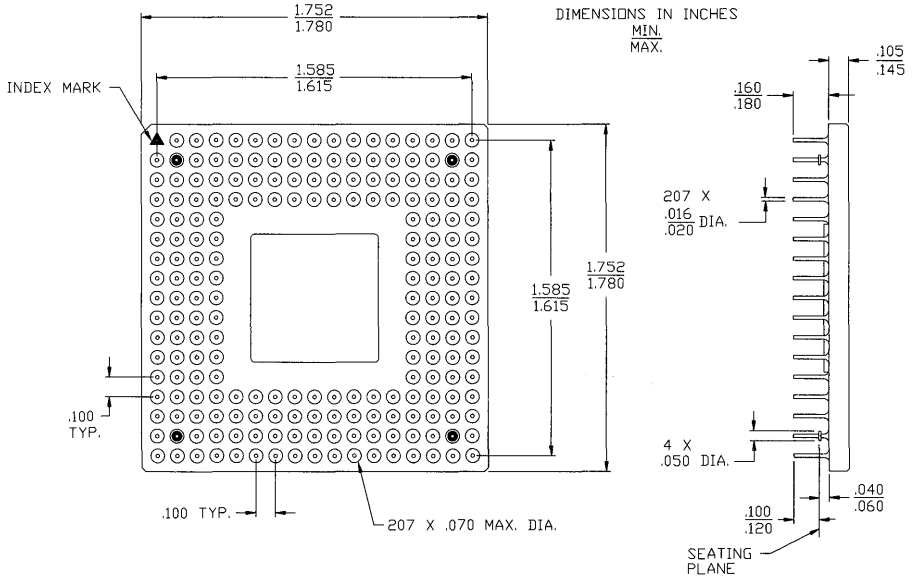


Ceramic Pin Grid Arrays (continued)

145-Pin Grid Array (Cavity Up) G145

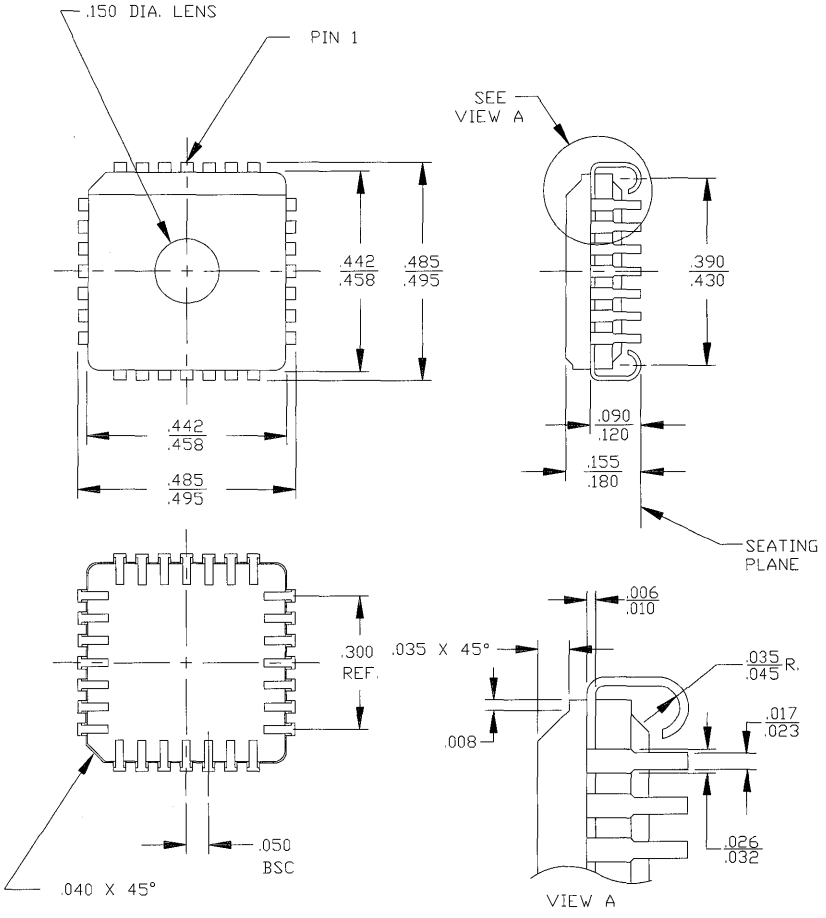


207-Pin Grid Array (Cavity Down) G207



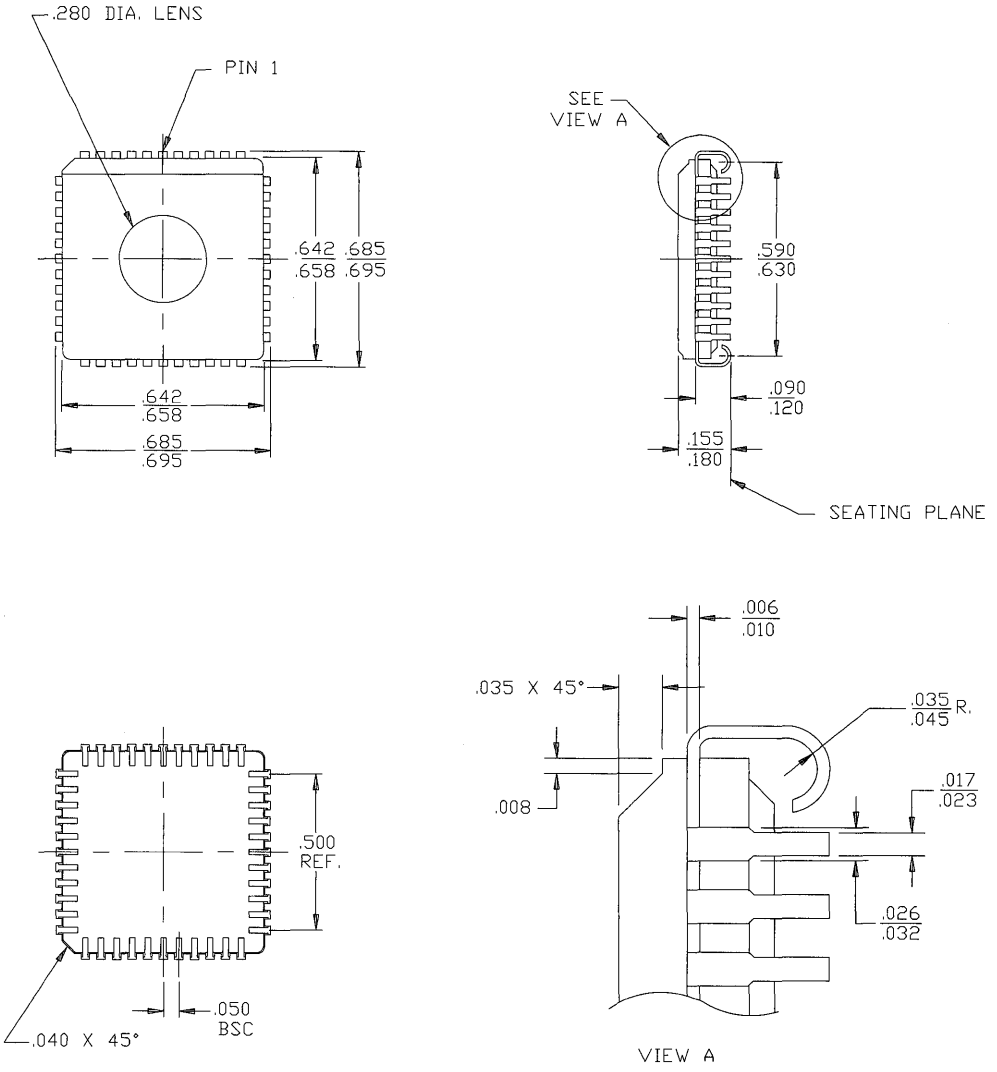
Ceramic Windowed J-Leaded Chip Carriers

28-Pin Windowed Leaded Chip Carrier H64



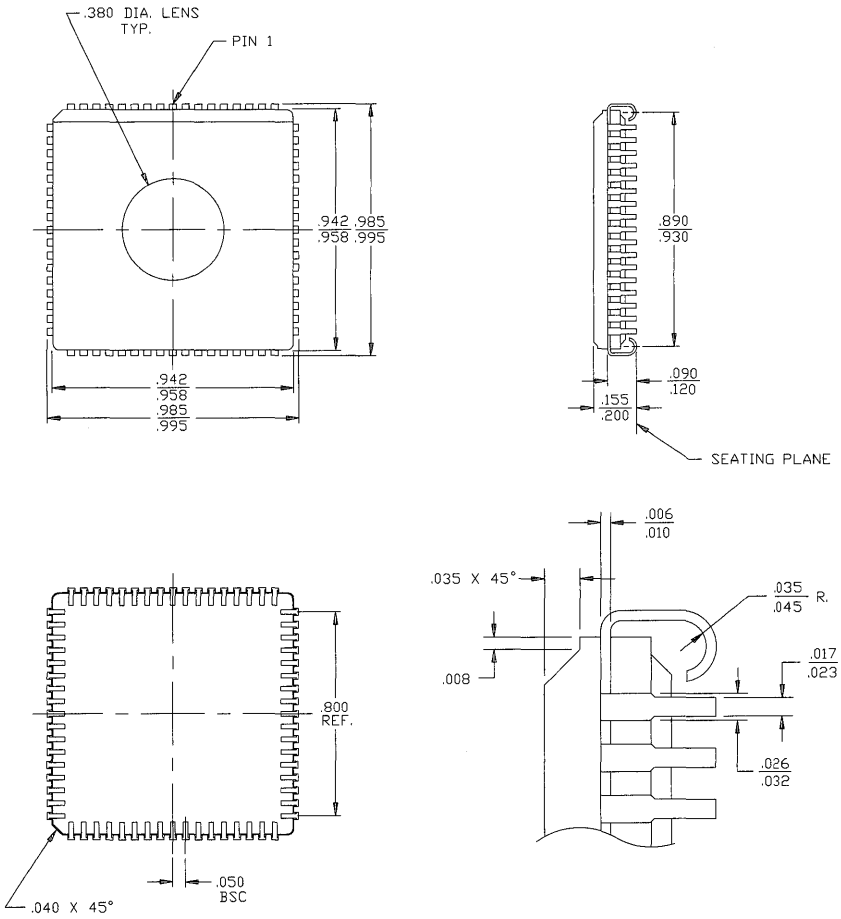
Ceramic Windowed J-Leaded Chip Carriers (continued)

44-Pin Windowed Leaded Chip Carrier H67



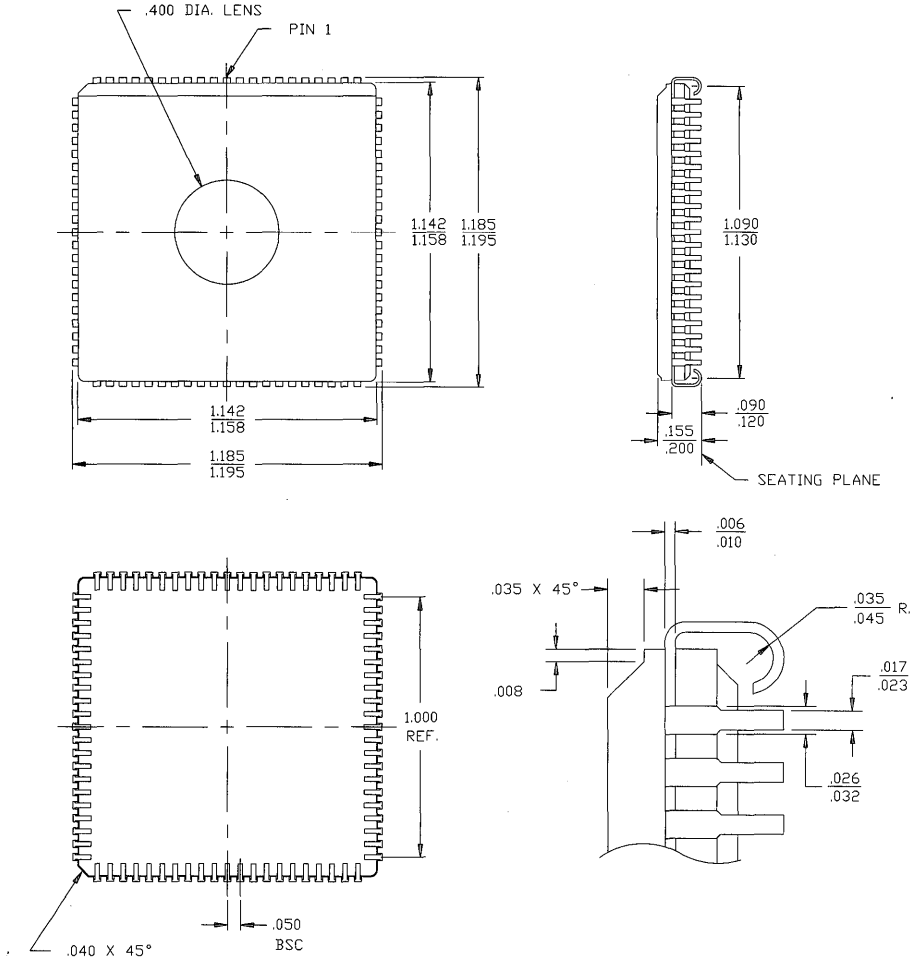
Ceramic Windowed J-Leaded Chip Carriers (continued)

68-Pin Windowed Leaded Chip Carrier H81



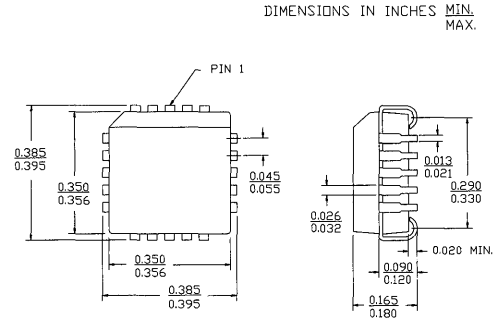
Ceramic Windowed J-Leaded Chip Carriers (continued)

84-Lead Windowed Leaded Chip Carrier H84

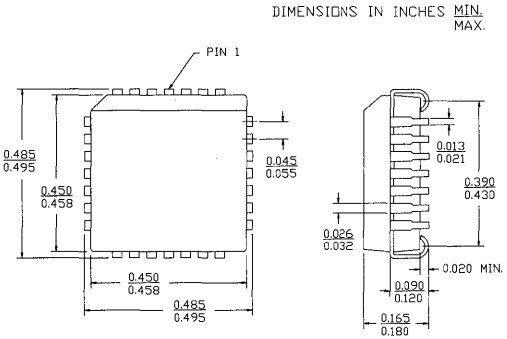


Plastic Leaded Chip Carriers

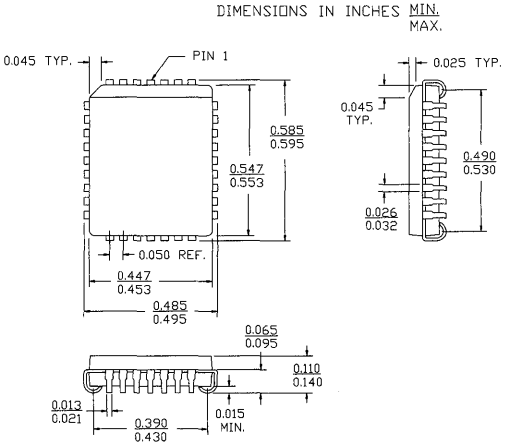
20-Lead Plastic Leaded Chip Carrier J61



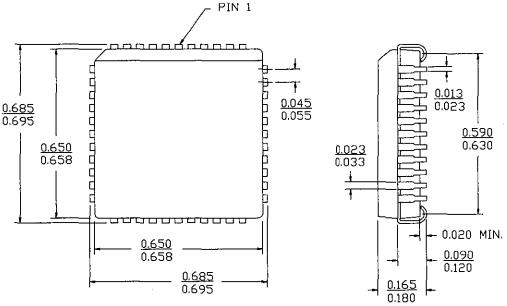
28-Lead Plastic Leaded Chip Carrier J64



32-Lead Plastic Leaded Chip Carrier J65

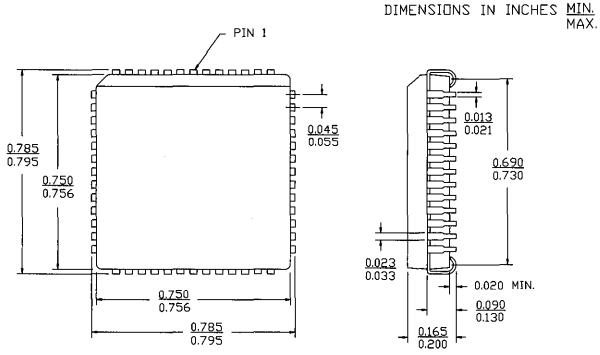


44-Lead Plastic Leaded Chip Carrier J67

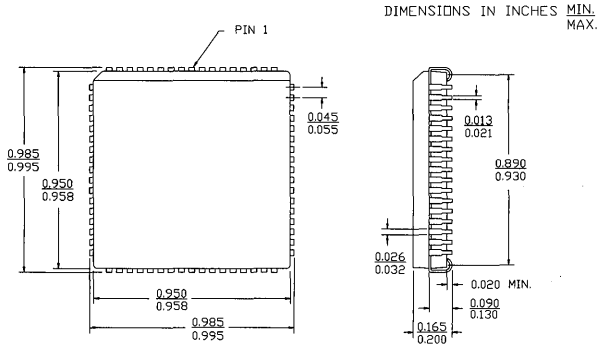


Plastic Leaded Chip Carriers (continued)

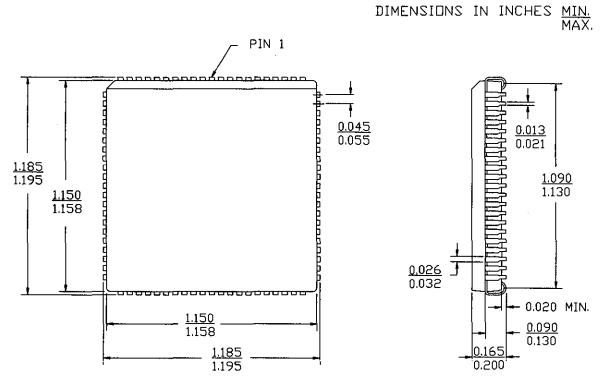
52-Lead Plastic Leaded Chip Carrier J69



68-Lead Plastic Leaded Chip Carrier J81

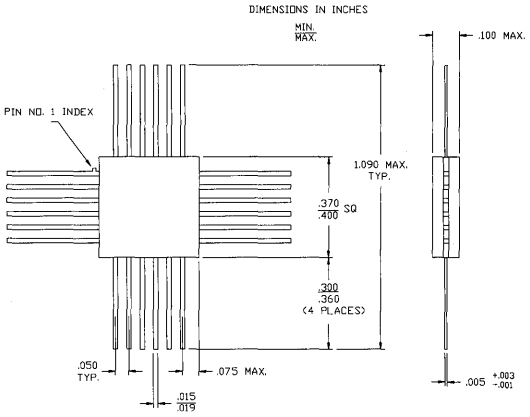


84-Lead Plastic Leaded Chip Carrier J83



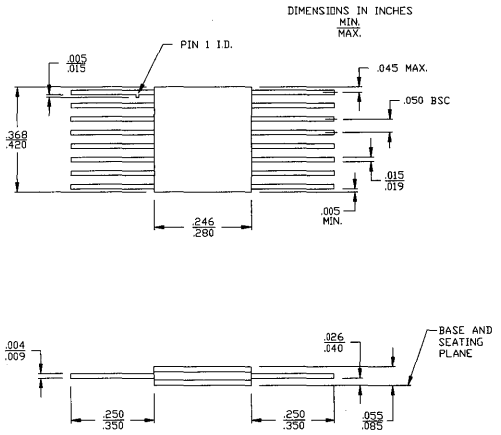
Cerpacks

24-Lead Square Cerpack K63



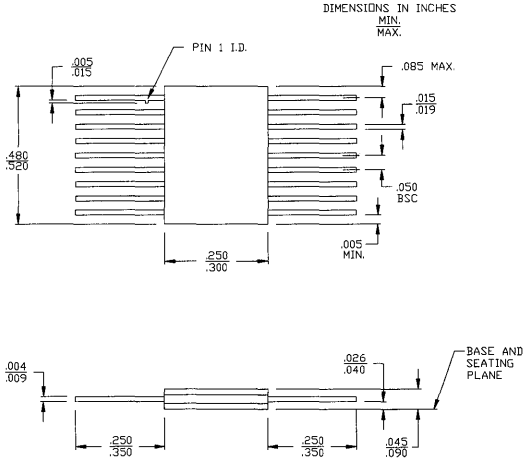
16-Lead Rectangular Cerpack K69

MIL–STD–1835 F–5 Config. A



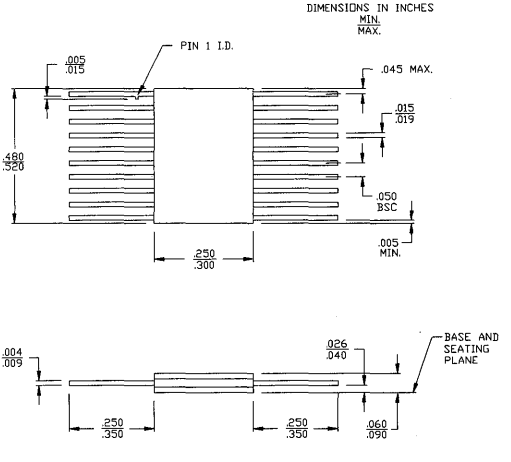
18-Lead Rectangular Cerpack K70

MIL–STD–1835 F–10 Config. A



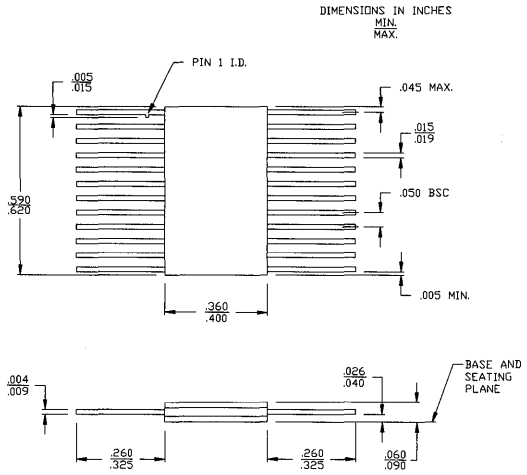
20-Lead Rectangular Cerpack K71

MIL–STD–1835 F–9 Config. A

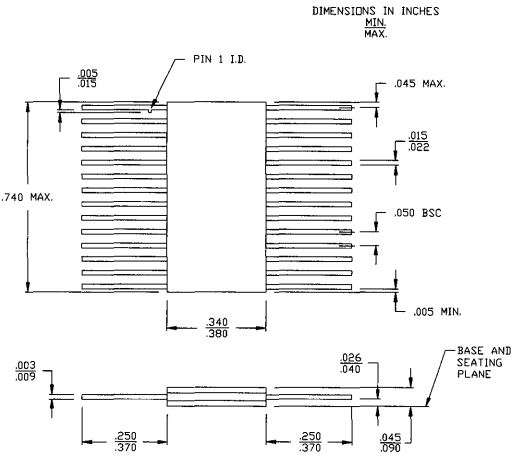


Cerpacks (continued)

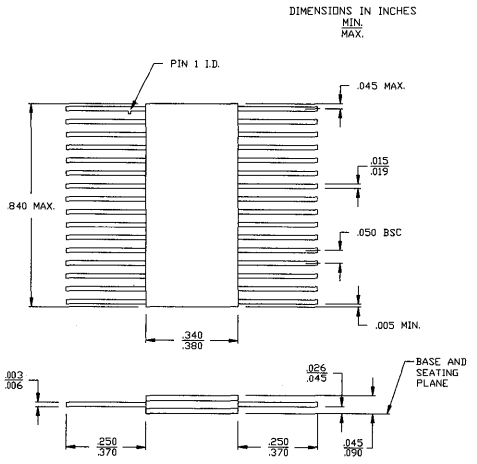
24-Lead Rectangular Cerpack K73
MIL–STD–1835 F–6 Config. A



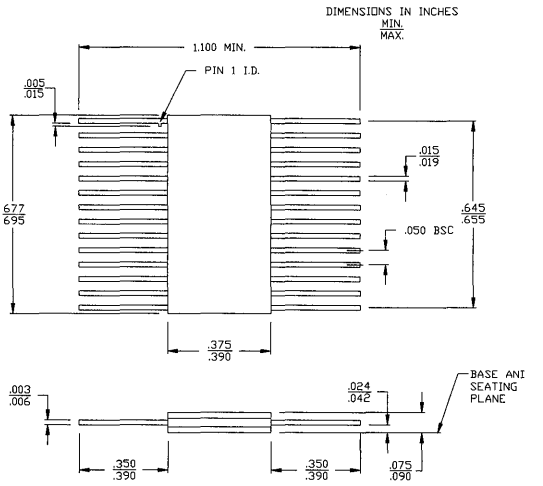
28-Lead Rectangular Cerpack K74
MIL–STD–1835 F–11 Config. A



32-Lead Rectangular Cerpack K75

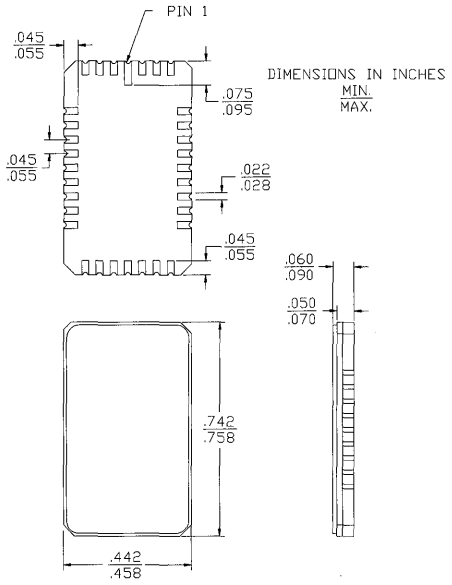


28-Lead Rectangular Cerpack K80

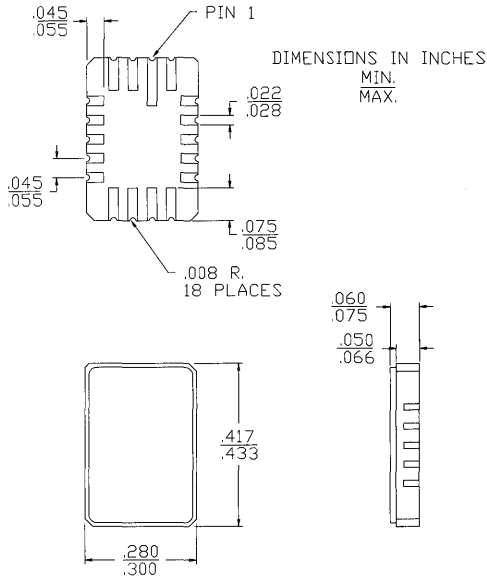


Ceramic Leadless Chip Carriers

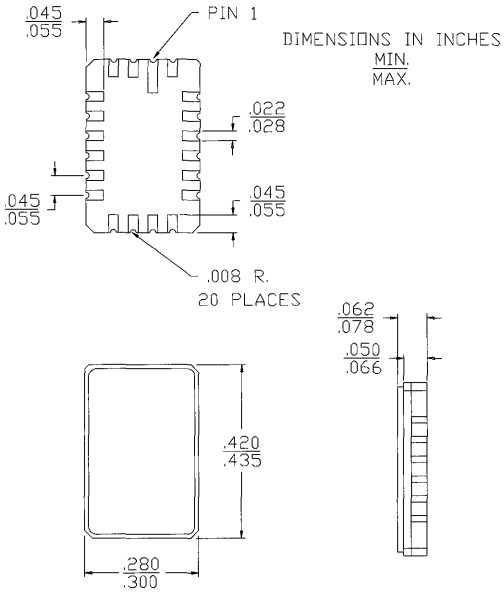
32-Lead Leadless Chip Carrier L45



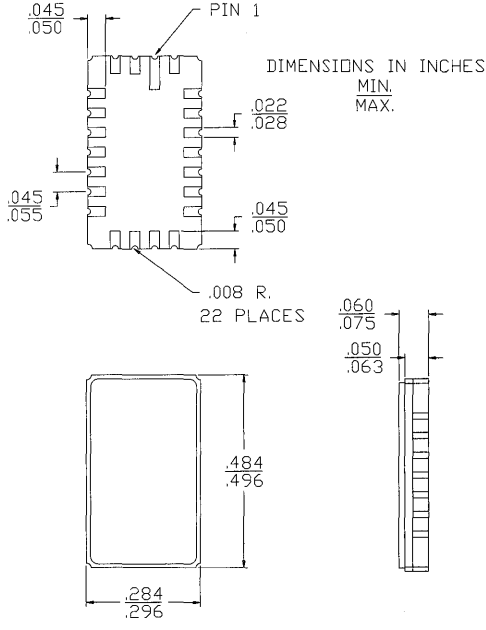
18-Pin Rectangular Leadless Chip Carrier L50
MIL–STD–1835 C–10A



20-Pin Rectangular Leadless Chip Carrier L51
MIL–STD–1835 C–13

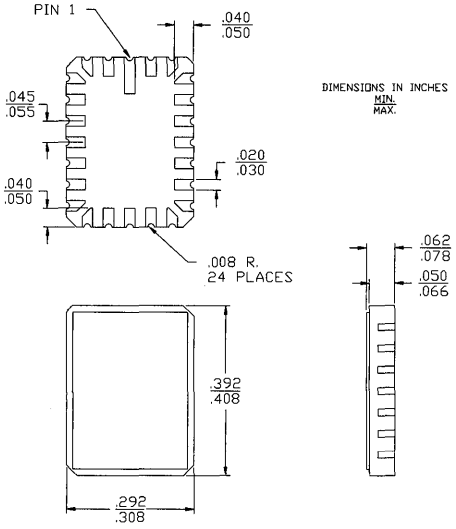


22-Pin Rectangular Leadless Chip Carrier L52

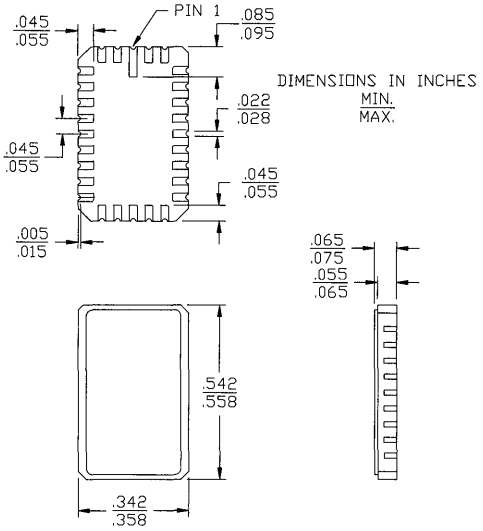


Ceramic Leadless Chip Carriers (continued)

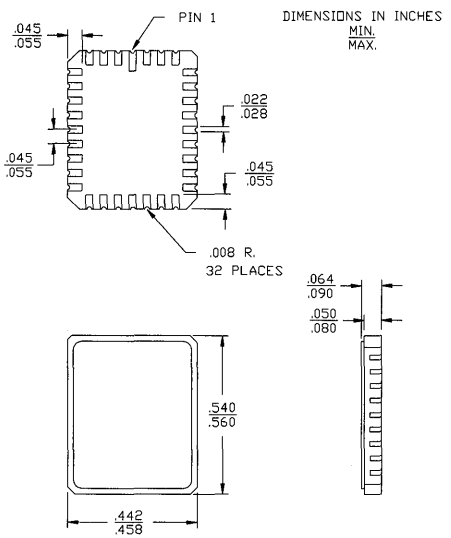
24-Pin Rectangular Leadless Chip Carrier L53



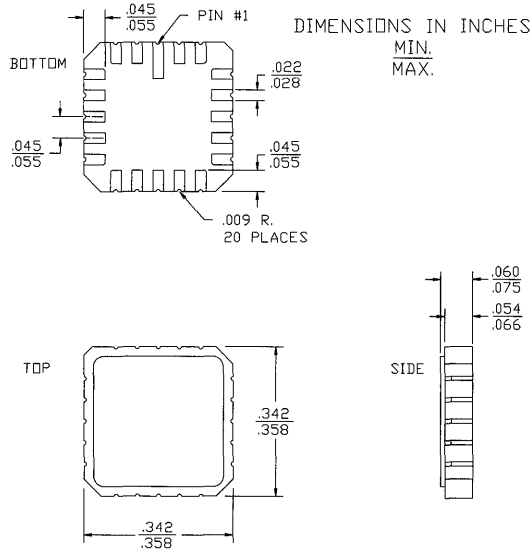
28-Pin Rectangular Leadless Chip Carrier L54
MIL-STD-1835 C-11A



32-Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12

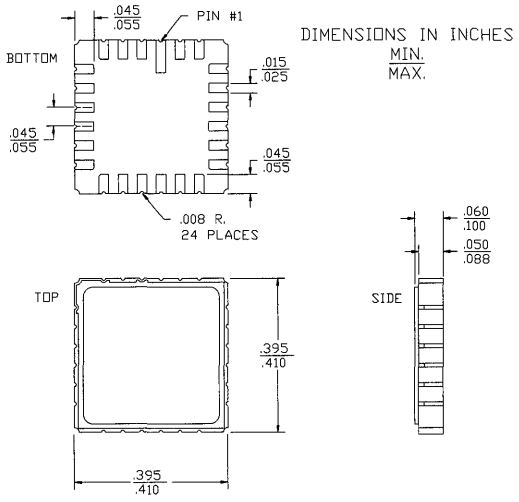


20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

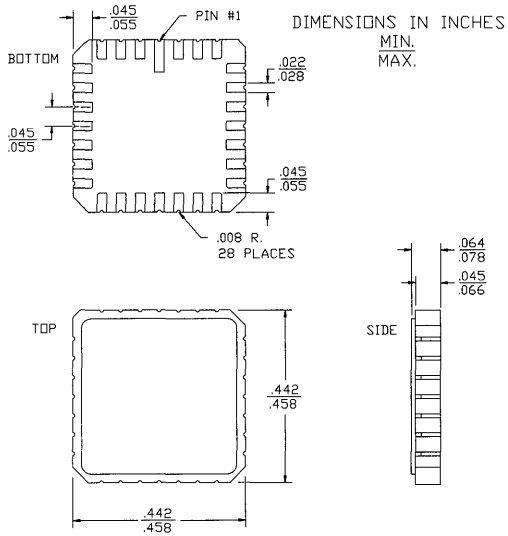


Ceramic Leadless Chip Carriers (continued)

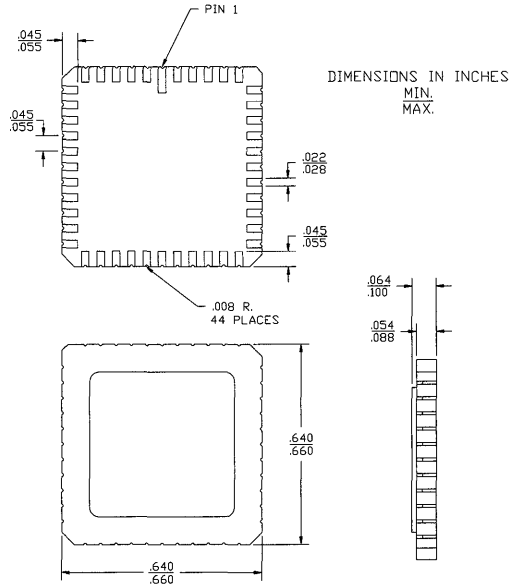
24-Square Leadless Chip Carrier L63



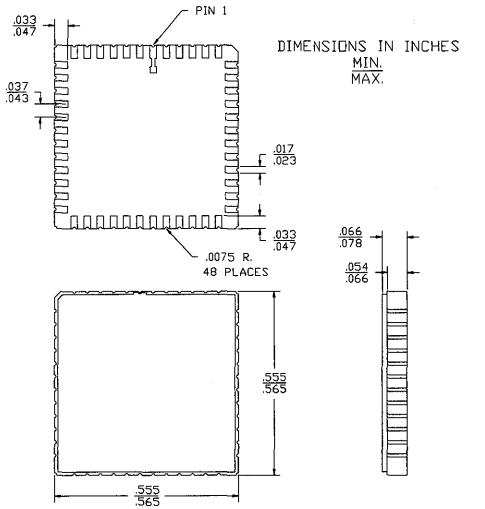
28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



44-Square Leadless Chip Carrier L67
MIL-STD-1835 C-5

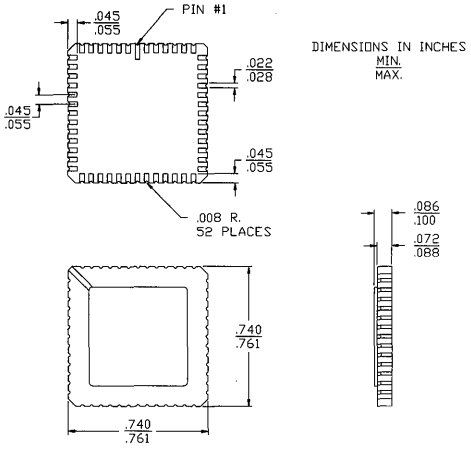


48-Square Leadless Chip Carrier L68

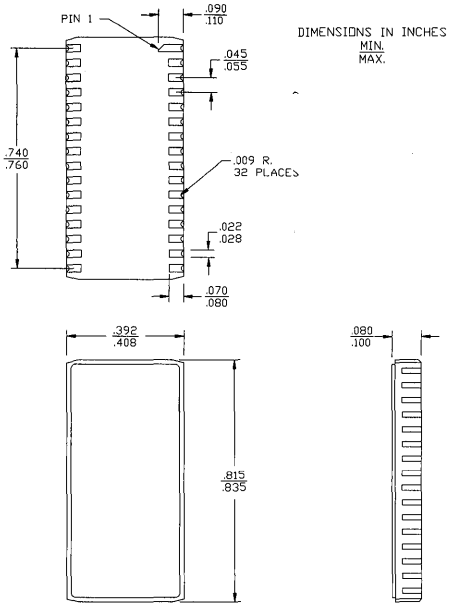


Ceramic Leadless Chip Carriers (continued)

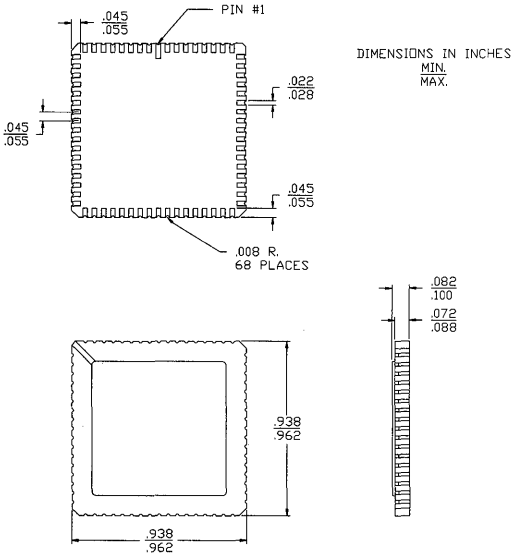
52-Square Leadless Chip Carrier L69



32-Pin Leadless Chip Carrier L75

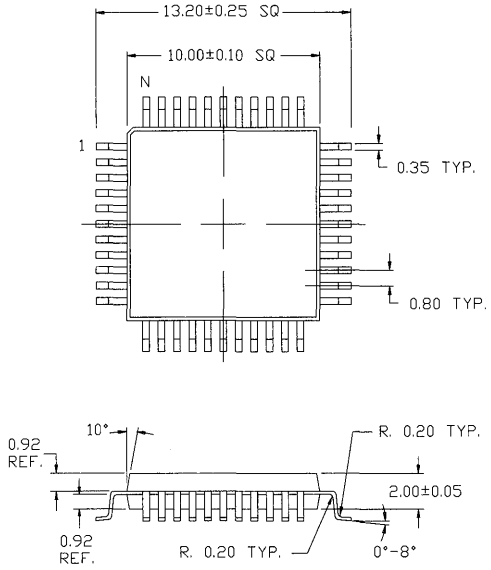


68-Square Leadless Chip Carrier L81
MIL–STD–1835 C–7

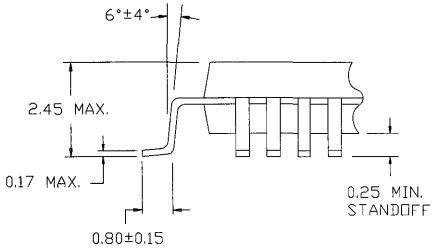


Plastic Quad Flatpacks

44-Lead Plastic Quad Flatpack N44

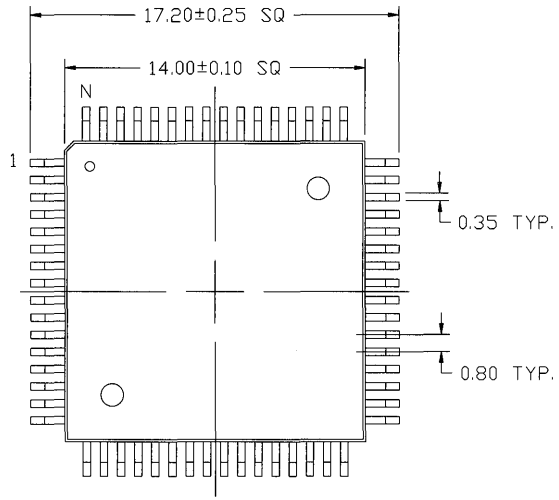


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

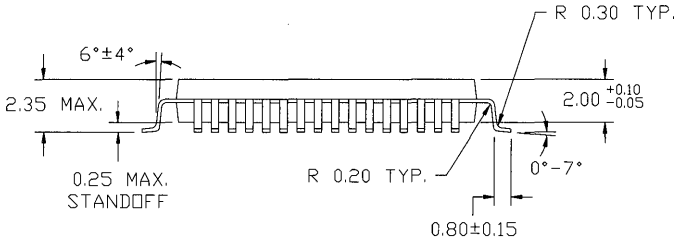


Plastic Quad Flatpacks (continued)

64-Lead Plastic Quad Flatpack N64

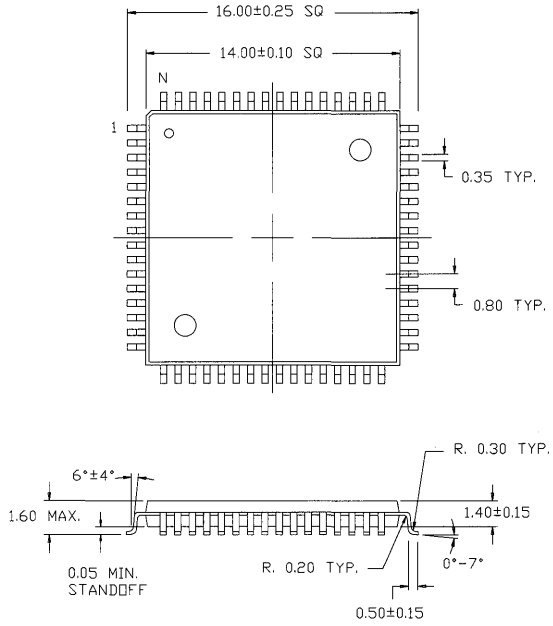


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Plastic Quad Flatpacks (continued)

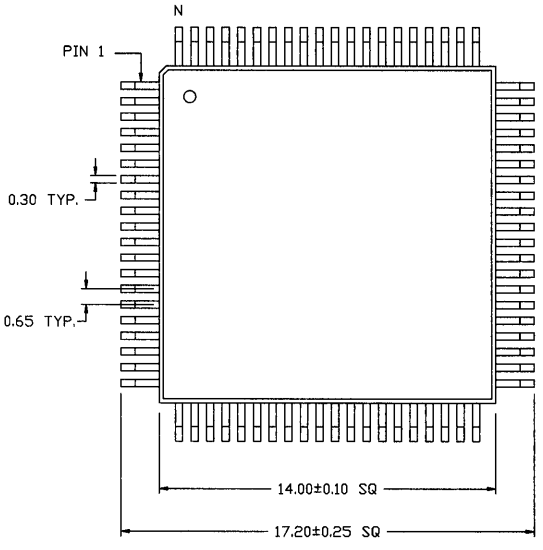
64-Lead Plastic Thin Quad Flatpack N65



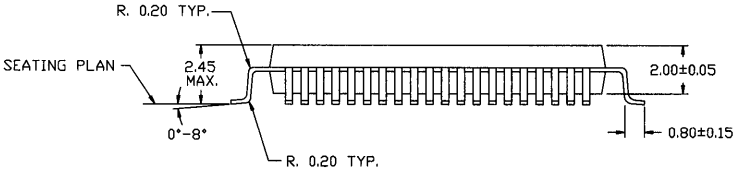
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

Plastic Quad Flatpacks (continued)

80-Lead Plastic Quad Flatpack N80

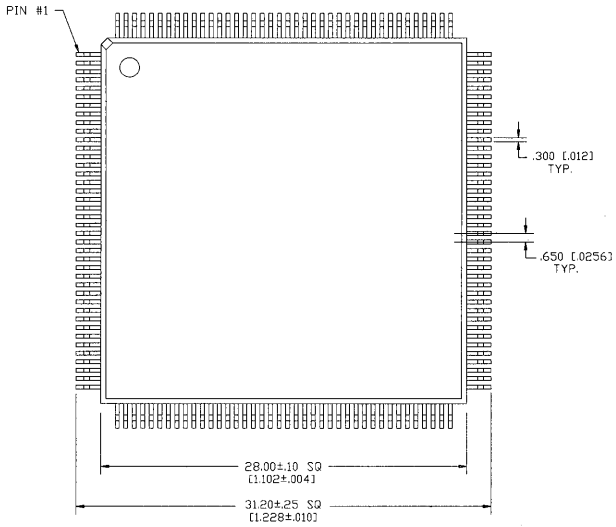


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

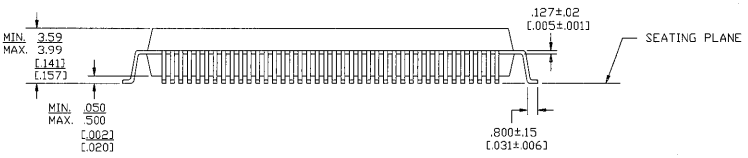


Plastic Quad Flatpacks (continued)

160-Lead Plastic Quad Flatpack N160

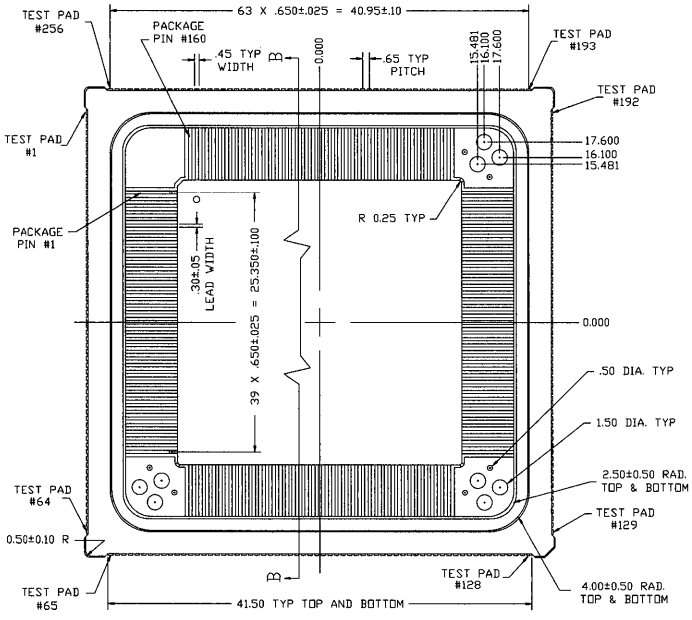


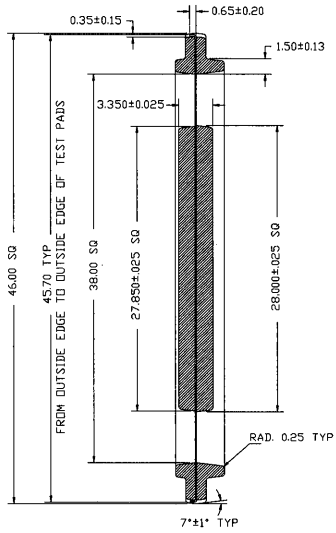
DIMENSION IN mm [INCHES as reference only]
LEAD COPLANARITY .100 [.004]



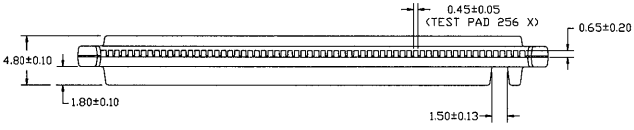
Plastic Quad Flatpacks (continued)

160-Lead Plastic Quad Flatpack with Molded Carrier Ring N161



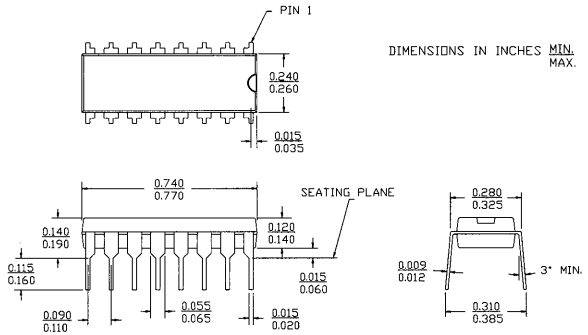


SECTION B-B

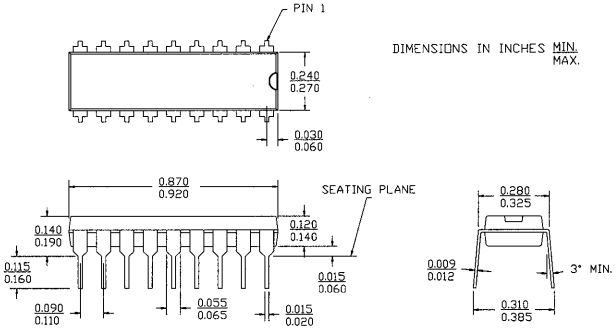


Plastic Dual-In-Line Packages

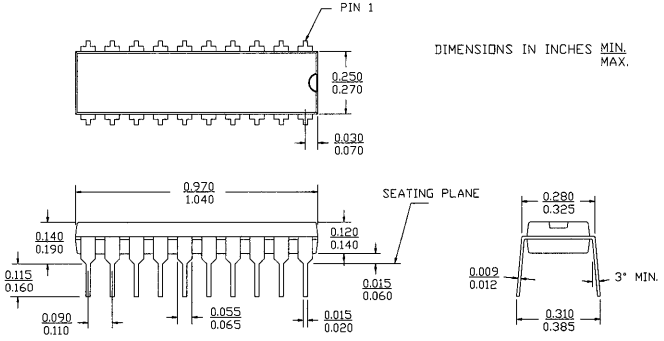
16-Lead (300-Mil) Molded DIP P1



18-Lead (300-Mil) Molded DIP P3

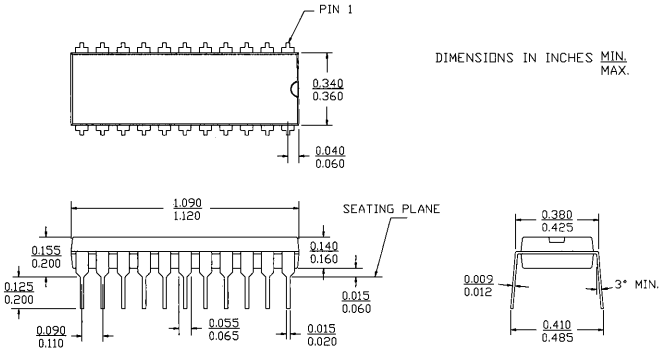


20-Lead (300-Mil) Molded DIP P5

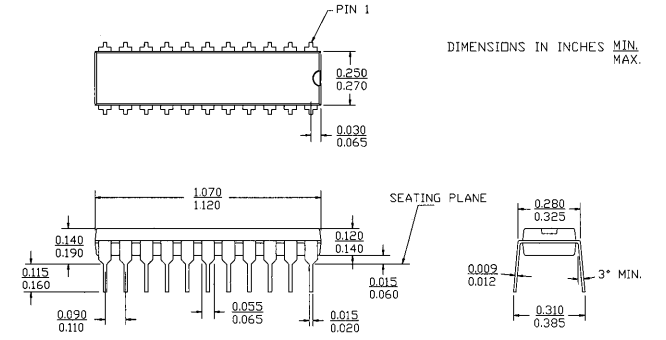


Plastic Dual-In-Line Packages (continued)

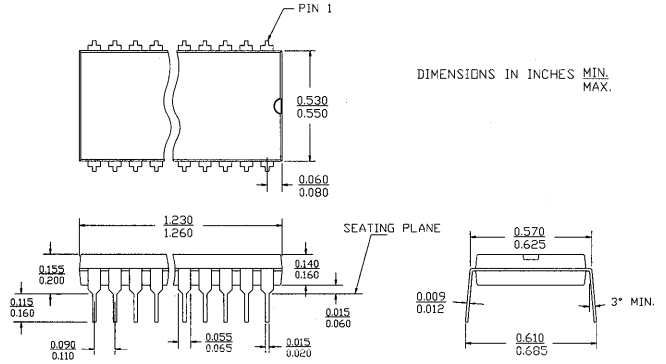
22-Lead (400-Mil) Molded DIP P7



22-Lead (300-Mil) Molded DIP P9

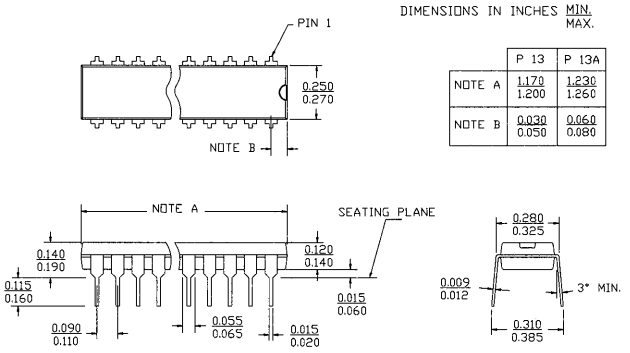


24-Lead (600-Mil) Molded DIP P11



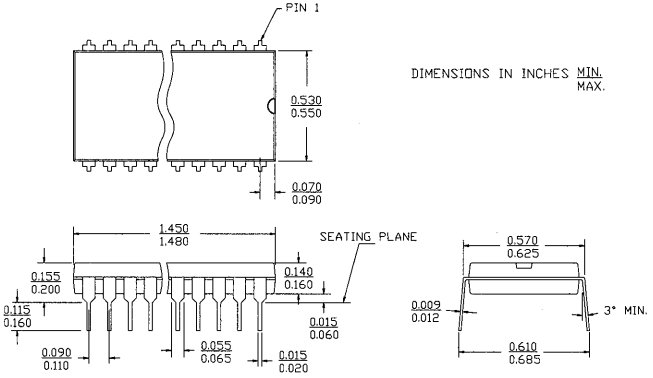
Plastic Dual-In-Line Packages (continued)

24-Lead (300-Mil) Molded DIP P13/P13A

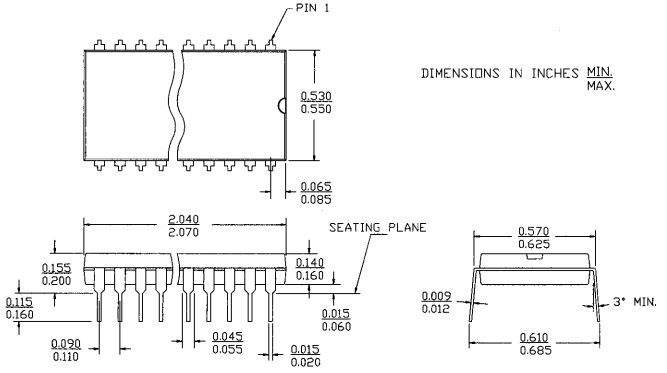


	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

28-Lead (600-Mil) Molded DIP P15

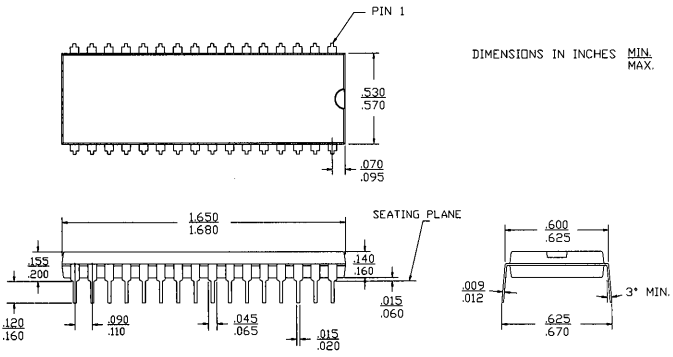


40-Lead (600-Mil) Molded DIP P17

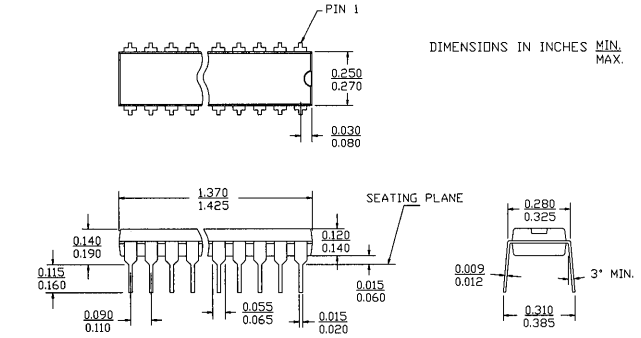


Plastic Dual-In-Line Packages (continued)

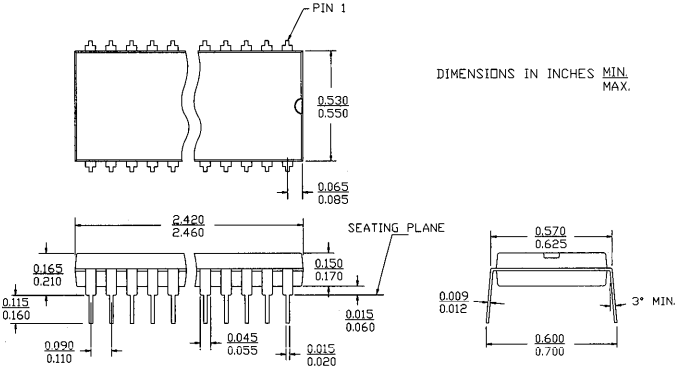
32-Lead (600-Mil) Molded DIP P19



28-Lead (300-Mil) Molded DIP P21

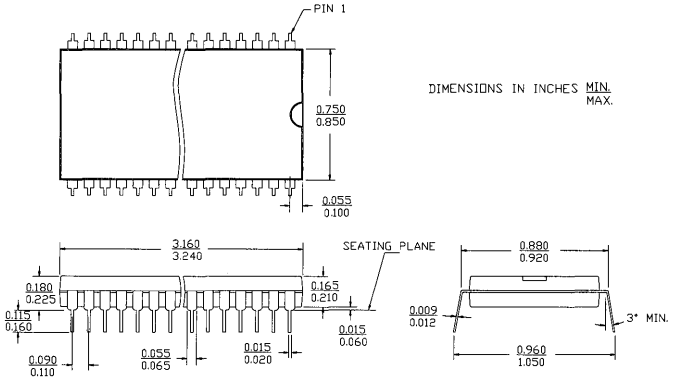


48-Lead (600-Mil) Molded DIP P25

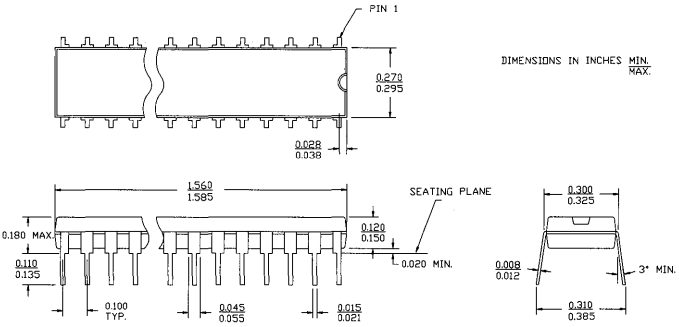


Plastic Dual-In-Line Packages (continued)

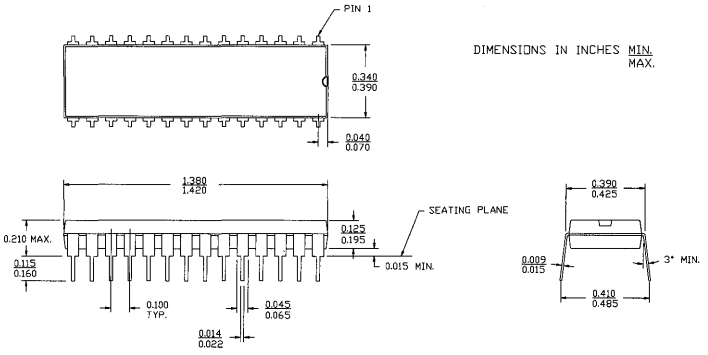
64-Lead (900-Mil) Molded DIP P29



32-Lead (300-Mil) Molded DIP P31

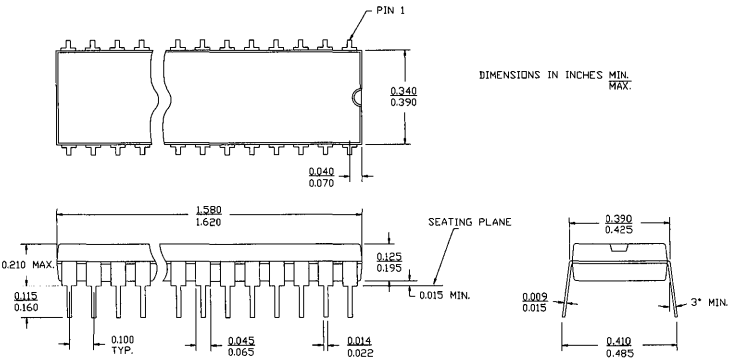


28-Lead (400-Mil) Molded DIP P41



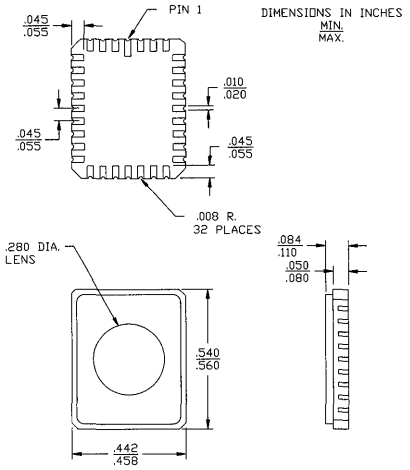
Plastic Dual-In-Line Packages (continued)

32-Lead (400-Mil) Molded DIP P43

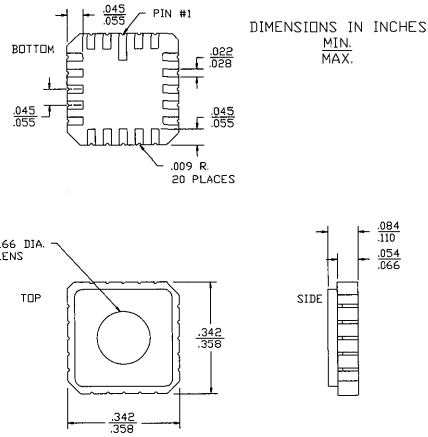


Ceramic Windowed Leadless Chip Carriers

32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL-STD-1835 C-12

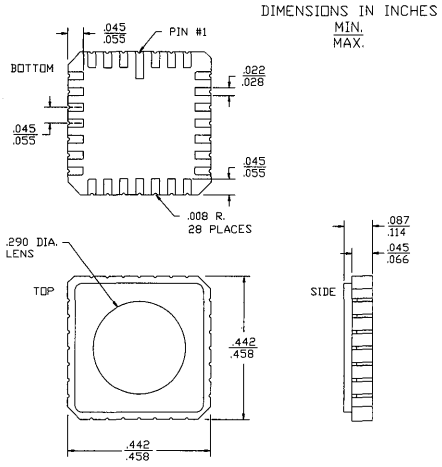


20-Pin Windowed Square Leadless Chip Carrier Q61
MIL-STD-1835 C-2A

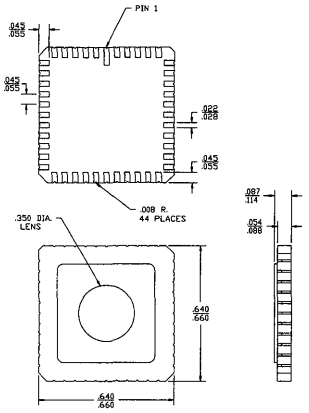


Ceramic Windowed Leadless Chip Carriers (continued)

28-Pin Windowed Leadless Chip Carrier Q64
MIL–STD–1835 C–4

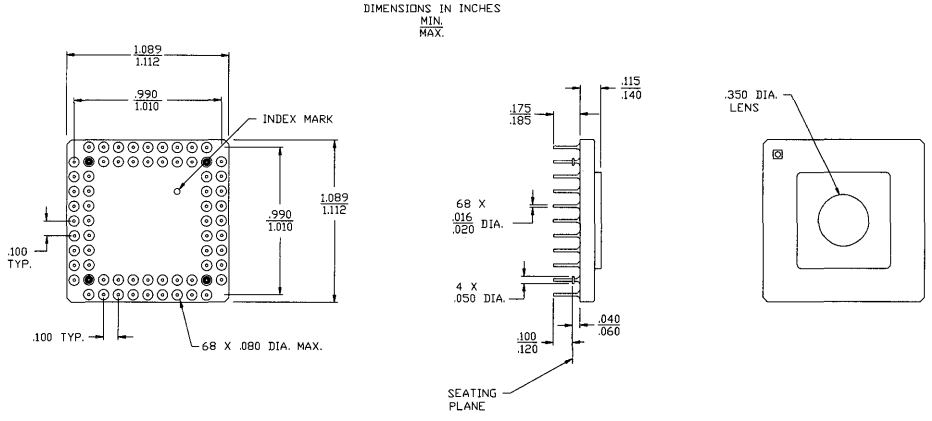


44-Pin Windowed Leadless Chip Carrier Q67
MIL–STD–1835 C–5



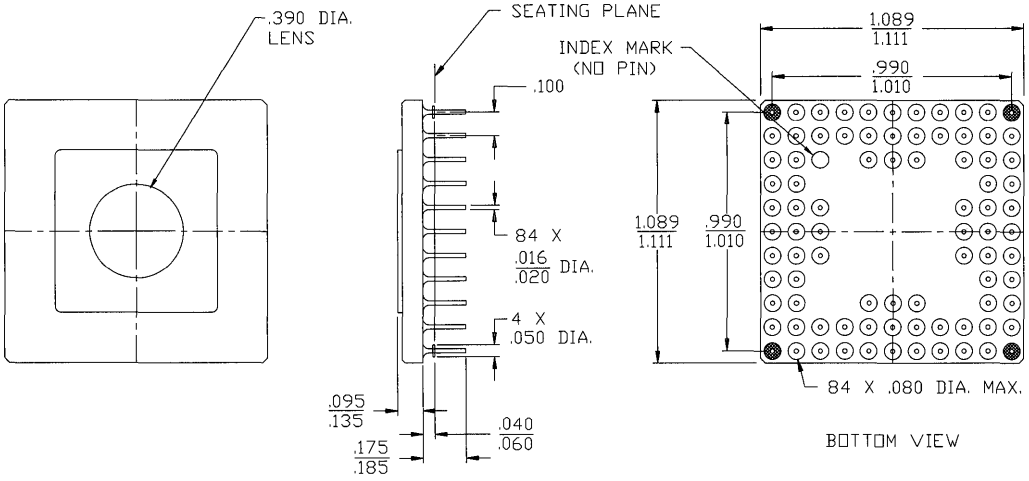
Ceramic Windowed Pin Grid Arrays

68-Pin Windowed PGA Ceramic R68



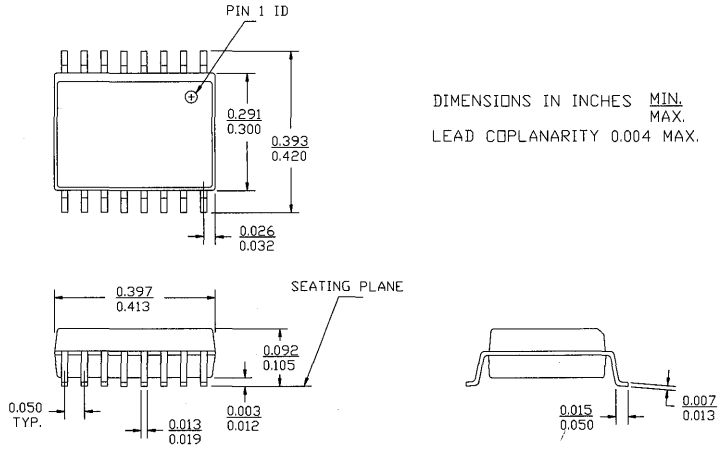
Ceramic Windowed Pin Grid Arrays (continued)

84-Lead Windowed Pin Grid Array R84



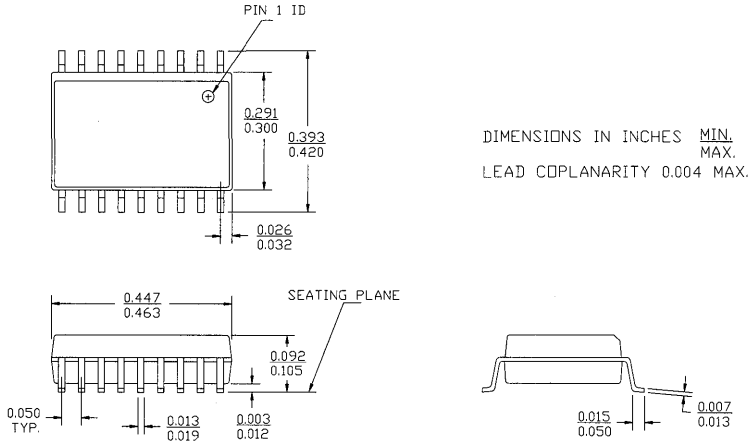
Plastic Small Outline ICs

16-Lead Molded SOIC S1

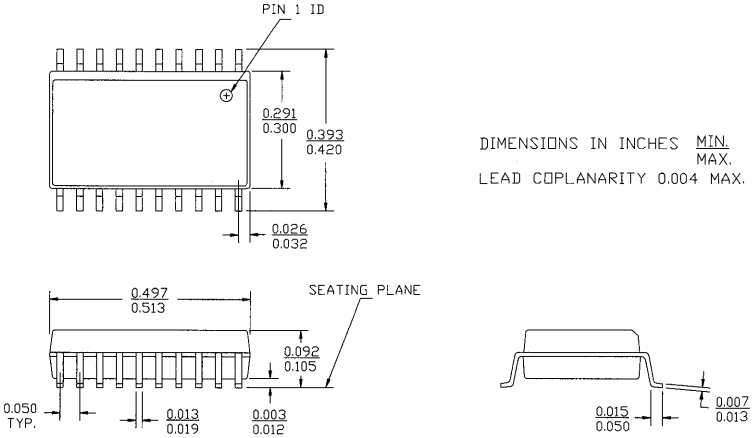


Plastic Small Outline ICs (continued)

18-Lead (300-Mil) Molded SOIC S3

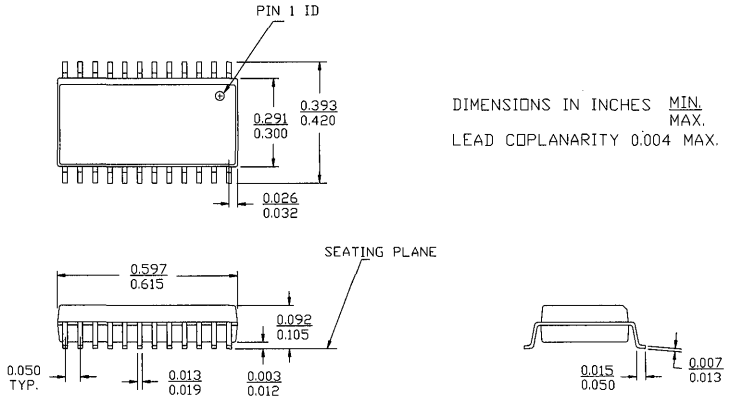


20-Lead (300-Mil) Molded SOIC S5

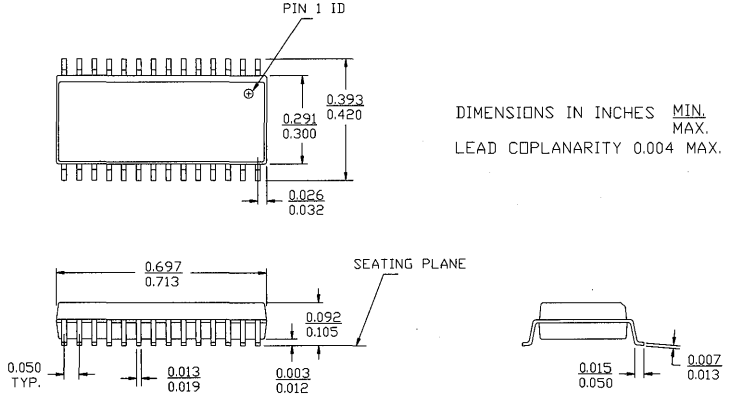


Plastic Small Outline ICs (continued)

24-Lead (300-Mil) Molded SOIC S13

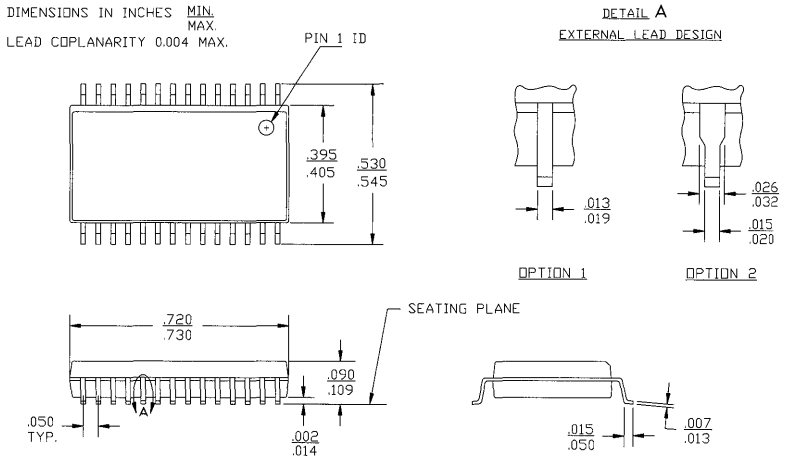


28-Lead (300-Mil) Molded SOIC S21

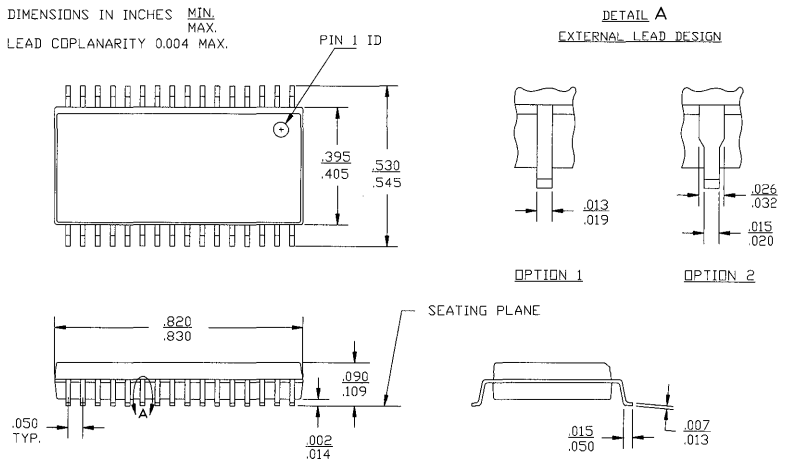


Plastic Small Outline ICs (continued)

28-Lead (400-Mil) Molded SOIC S28

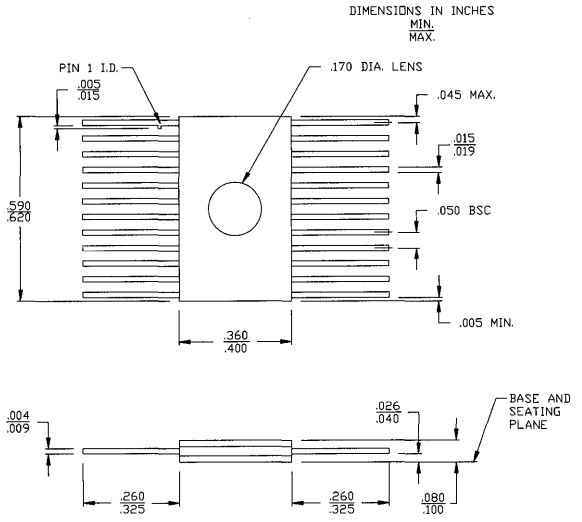


32-Lead (400-Mil) Molded SOIC S33

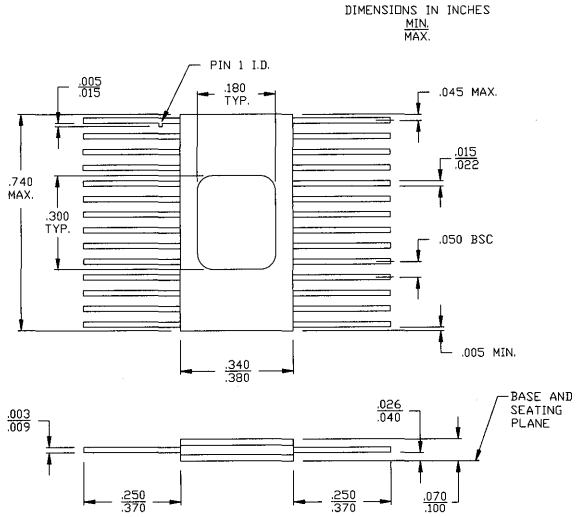


Windowed Cerpacks

24-Lead Windowed Cerpack T73

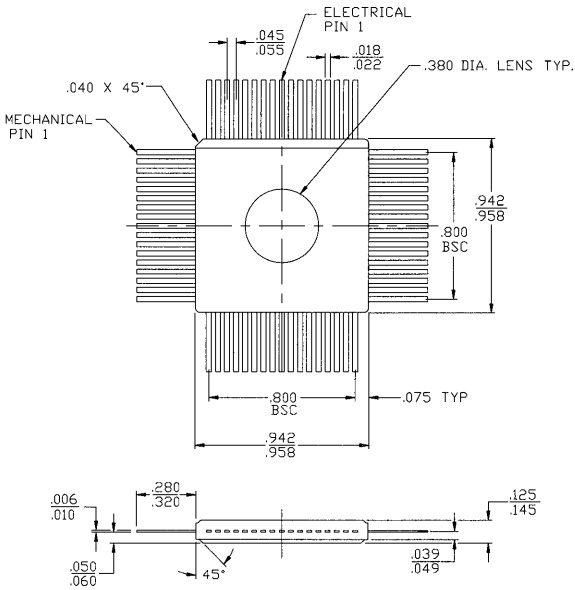


28-Lead Windowed Cerpack T74



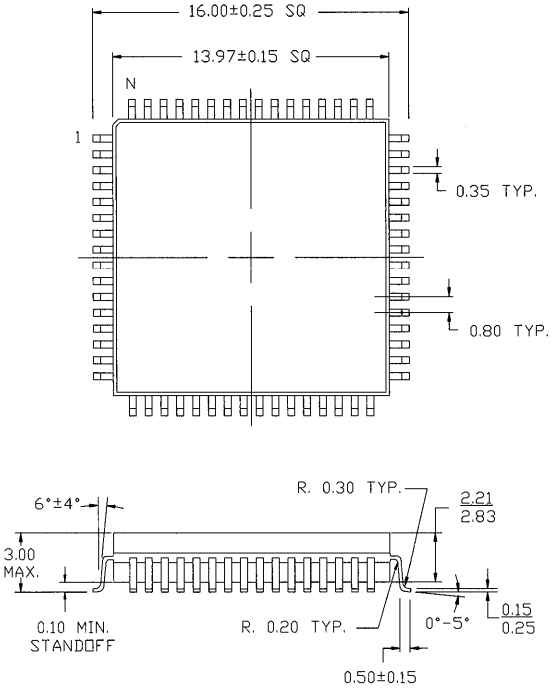
Windowed Cerpacks (continued)

68-Lead Windowed Cerquad Flatpack T91



Ceramic Quad Flatpacks

64-Lead Ceramic Quad Flatpack (Cavity Up) U65

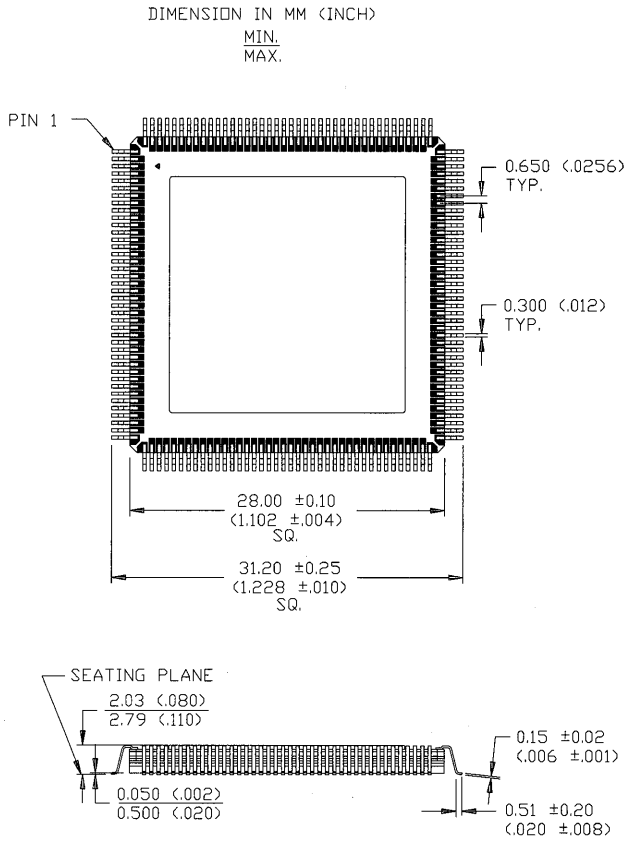


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

DIMENSION	MIN. / MAX.

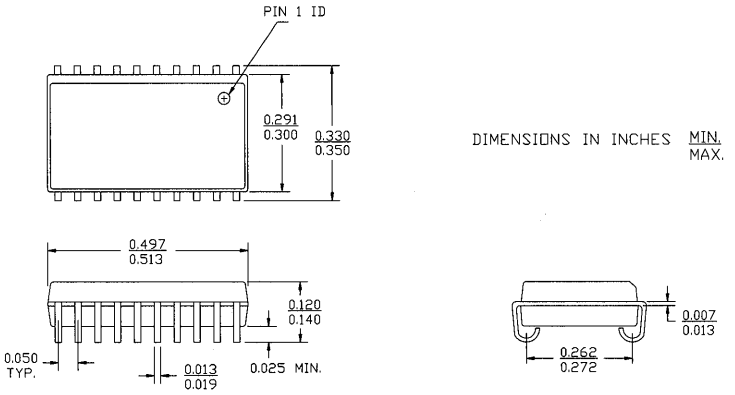
Ceramic Quad Flatpacks (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162

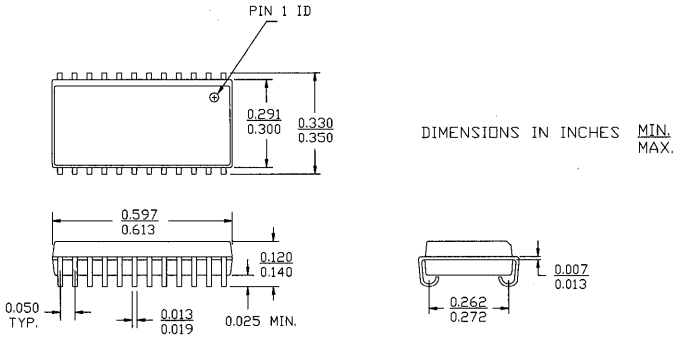


Plastic Small Outline J–Bend

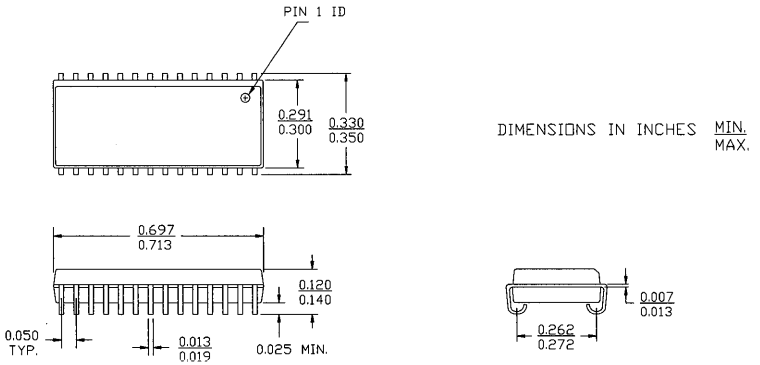
20-Lead (300-Mil) Molded SOJ V5



24-Lead (300-Mil) Molded SOJ V13

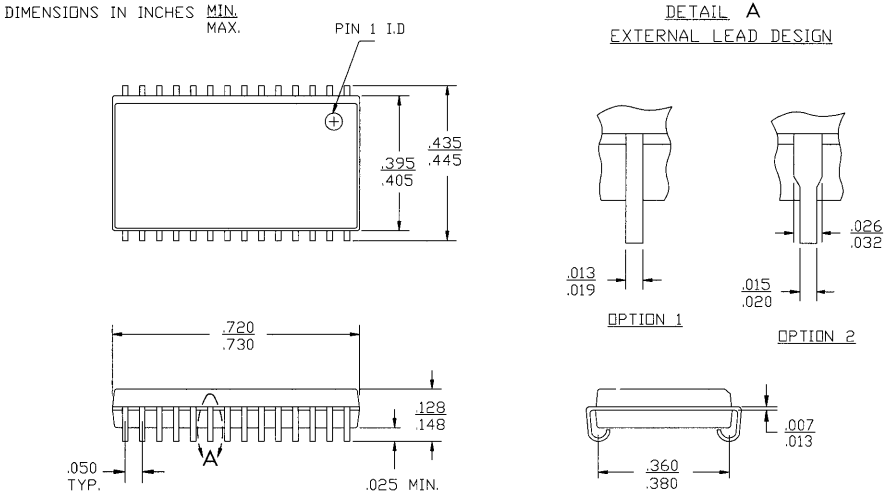


28-Lead (300-Mil) Molded SOJ V21

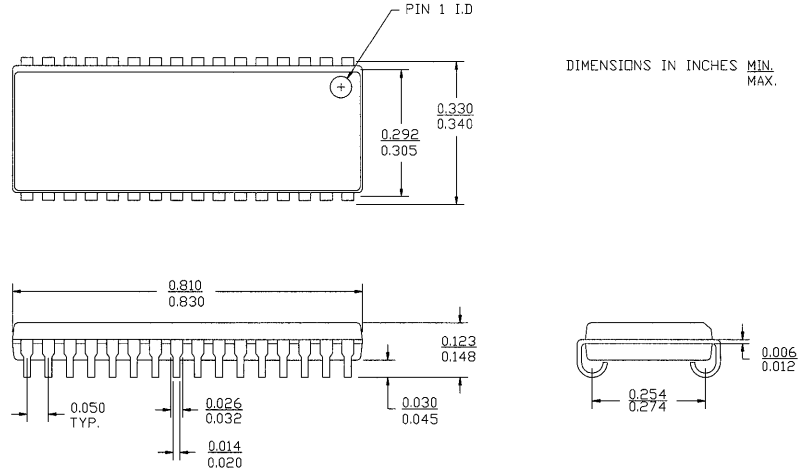


Plastic Small Outline J−Bend (continued)

28-Lead (400-Mil) Molded SOJ V28

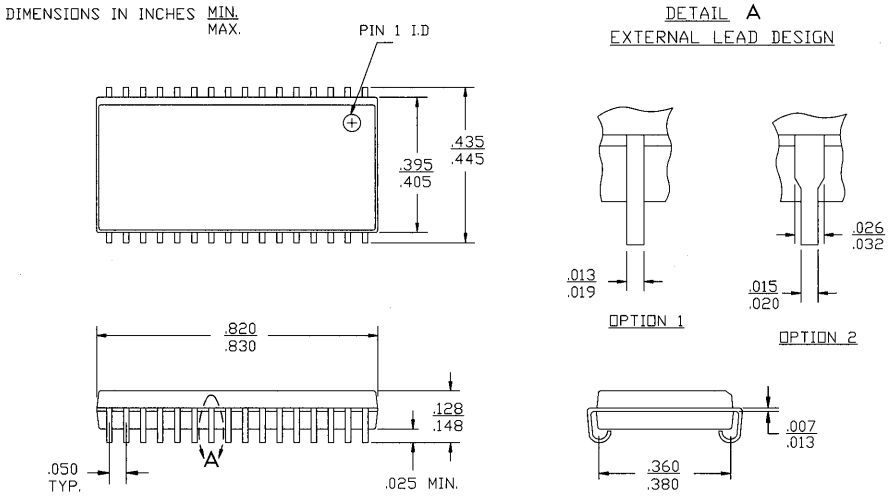


32-Lead (300-Mil) Molded SOJ V32



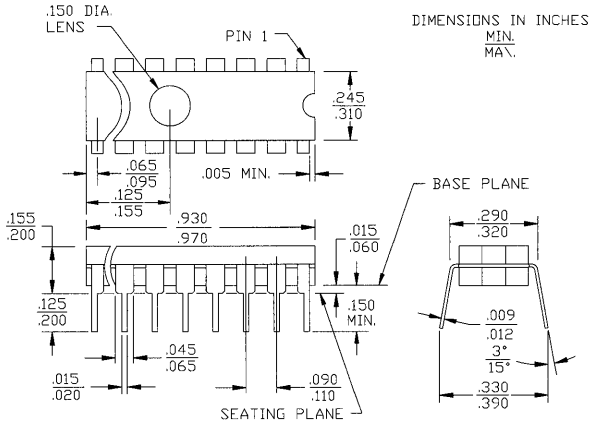
Plastic Small Outline J–Bend (continued)

32-Lead (400-Mil) Molded SOJ V33

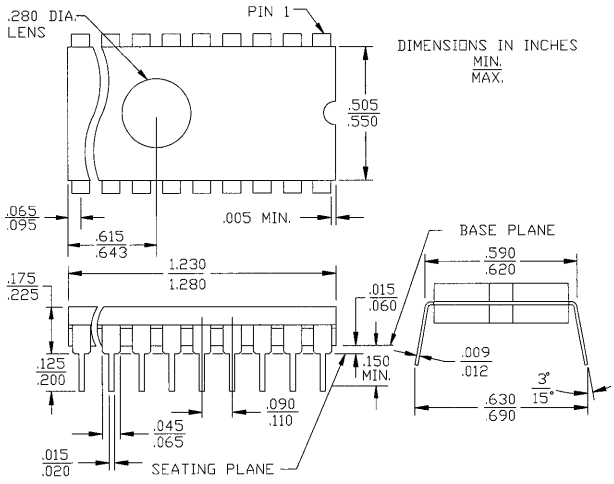


Ceramic Windowed Dual-In-Line Packages

20-Lead (300-Mil) Windowed CerDIP W6
MIL–STD–1835 D–8 Config. A

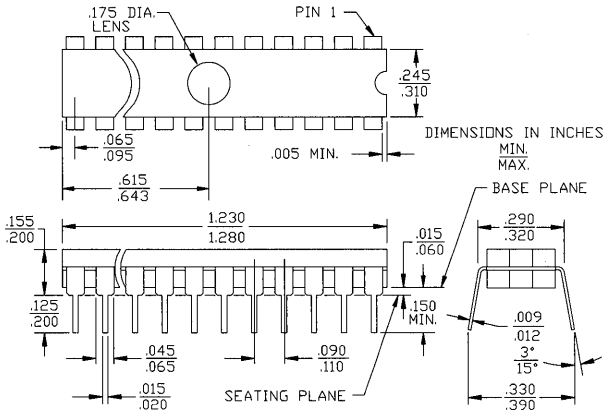


24-Lead (600-Mil) Windowed CerDIP W12
MIL–STD–1835 D–3 Config. A

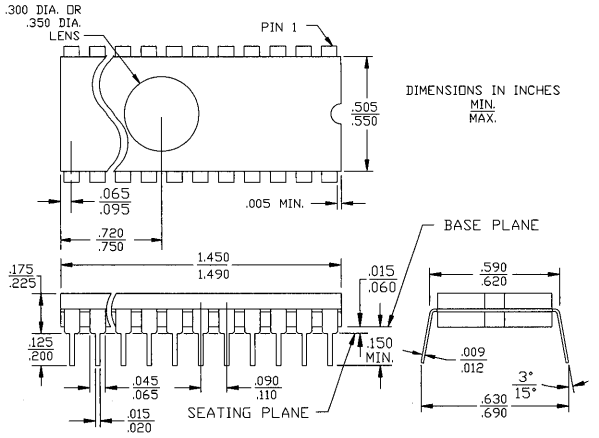


Ceramic Windowed Dual-In-Line Packages (continued)

24-Lead (300-Mil) Windowed CerDIP W14
MIL–STD–1835 D–9 Config. A

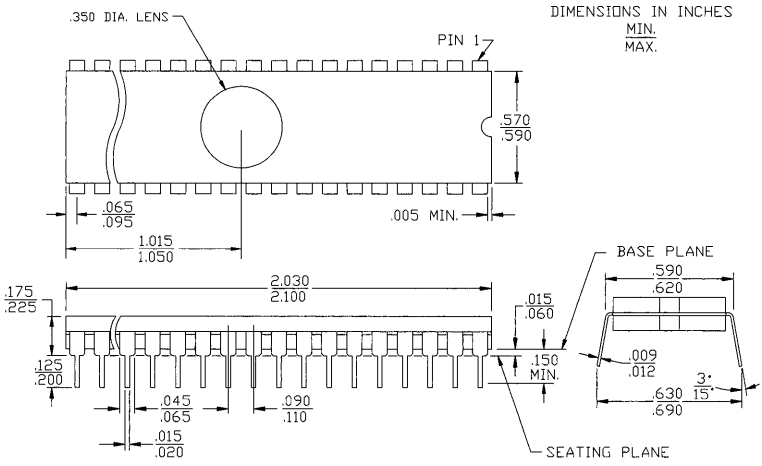


28-Lead (600-Mil) Windowed CerDIP W16
MIL–STD–1835 D–10 Config. A

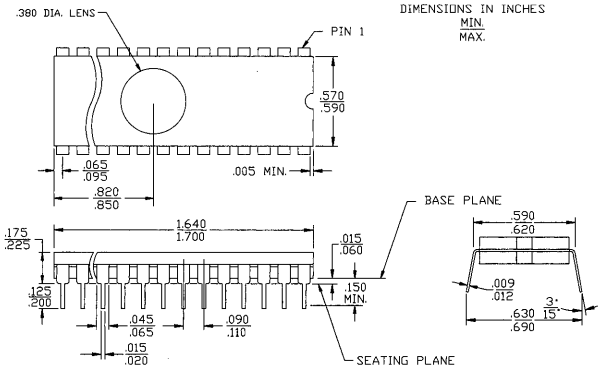


Ceramic Windowed Dual-In-Line Packages (continued)

40-Lead (600-Mil) Windowed CerDIP W18

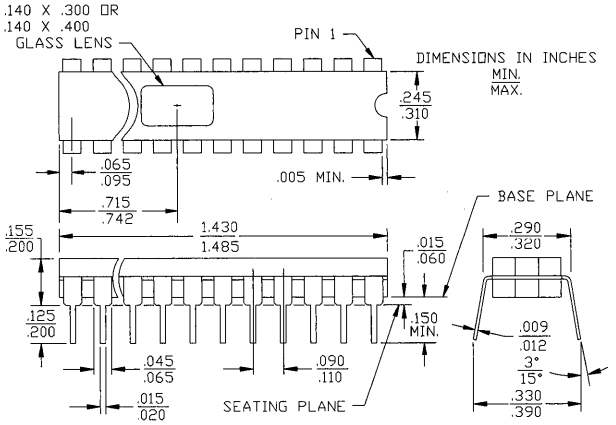


32-Lead (600-Mil) Windowed CerDIP W20

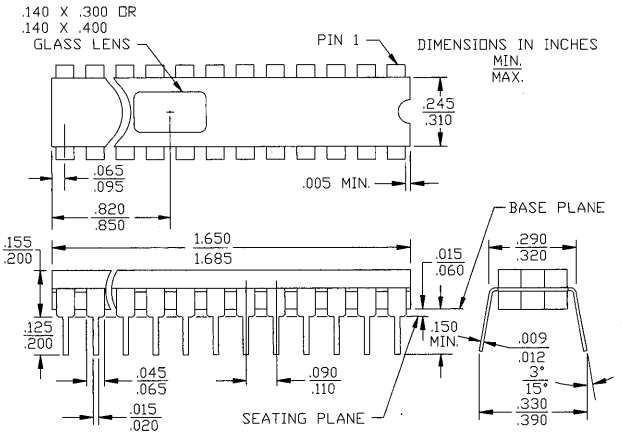


Ceramic Windowed Dual-In-Line Packages (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A

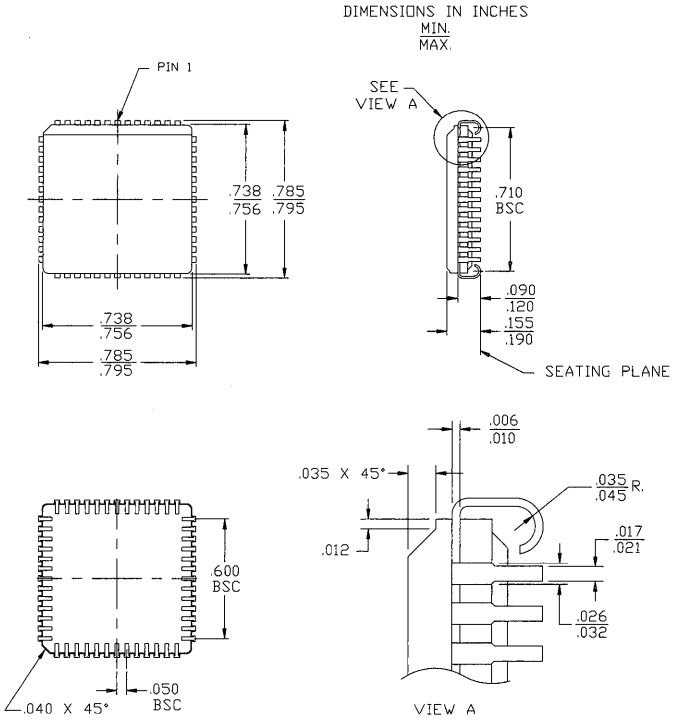


32-Lead (300-Mil) Windowed CerDIP W32



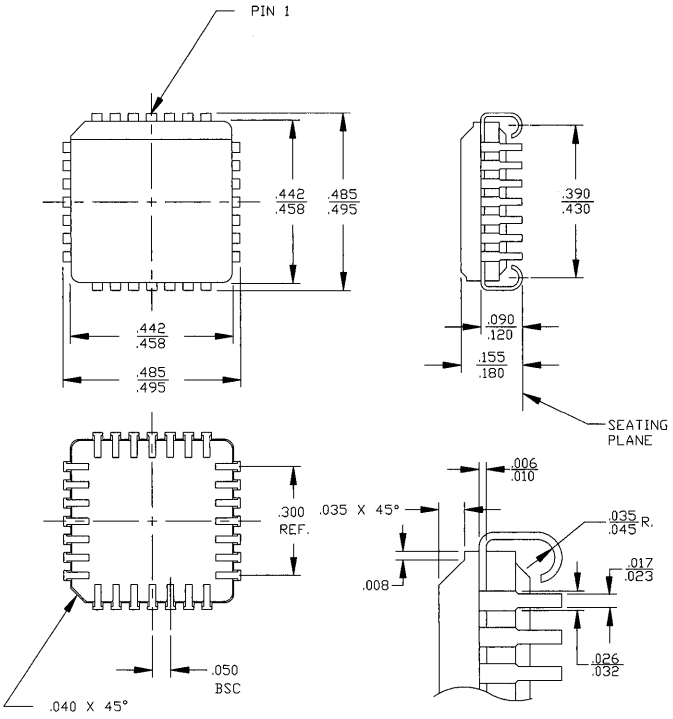
Ceramic J-Leaded Chip Carriers

52-Pin Ceramic Leaded Chip Carrier Y59



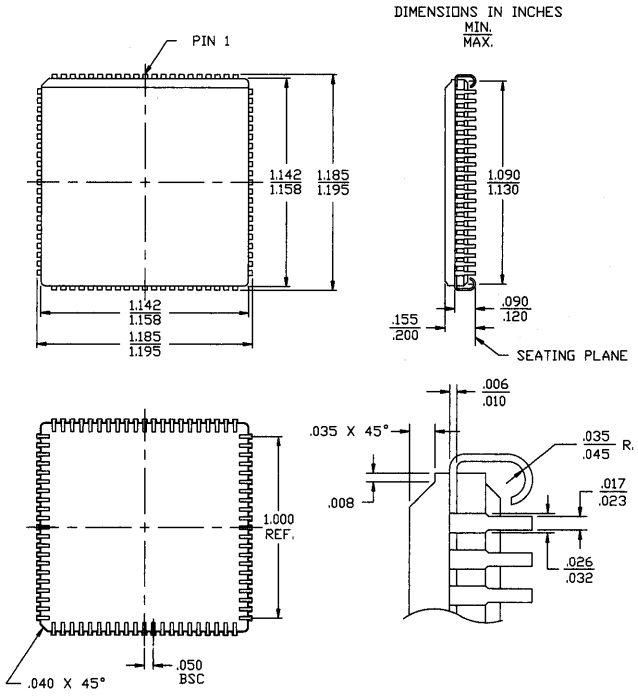
Ceramic J-Leaded Chip Carriers (continued)

28-Pin Ceramic Leaded Chip Carrier Y64

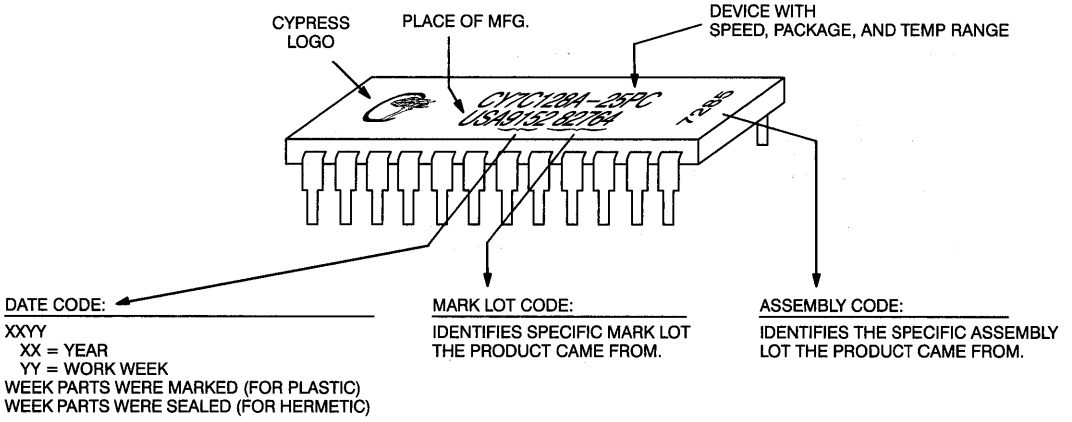


Ceramic J-Leaded Chip Carriers (continued)

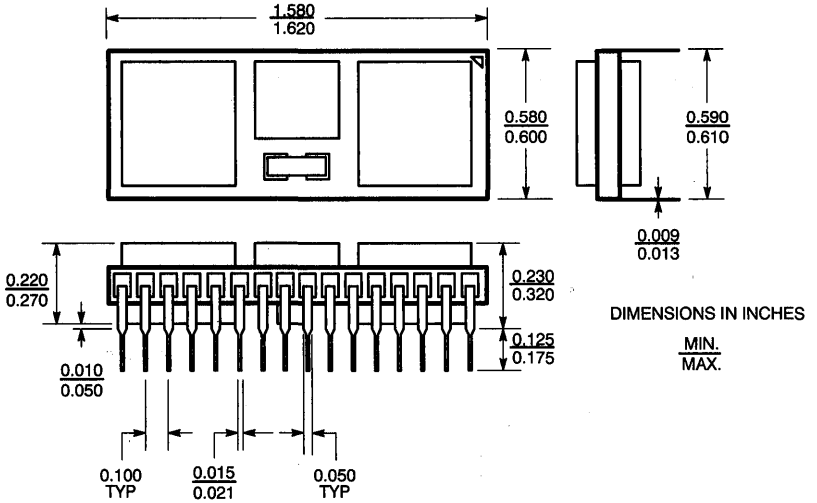
84-Pin Ceramic Leaded Chip Carrier Y84



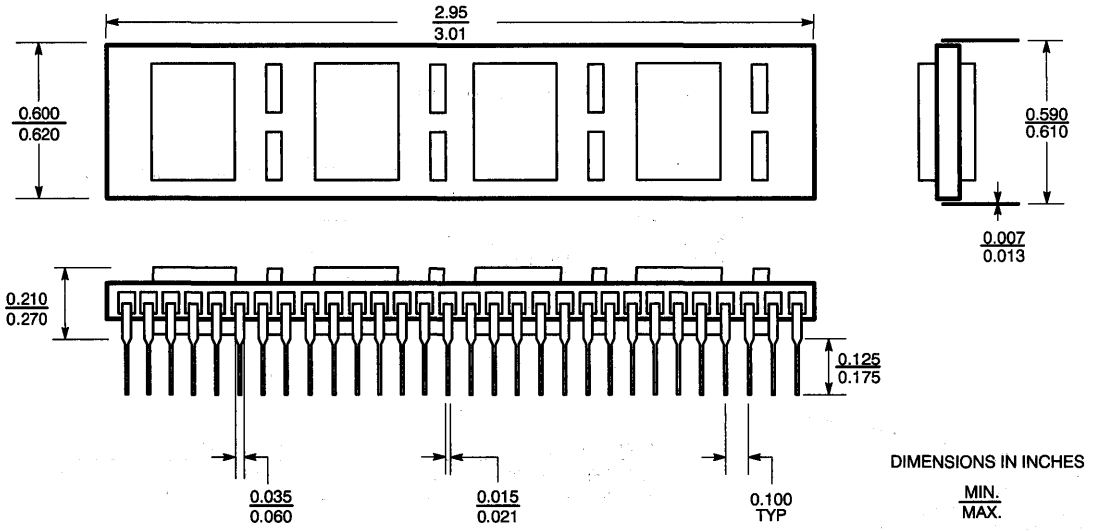
Typical Marking for DIP Packages (P and D Type)



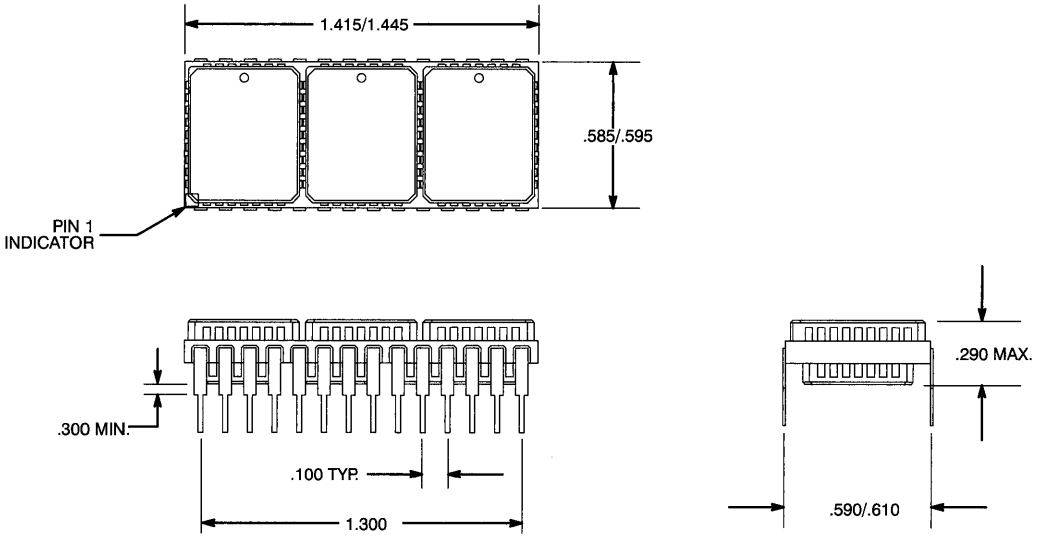
32-Pin DIP Module HD04



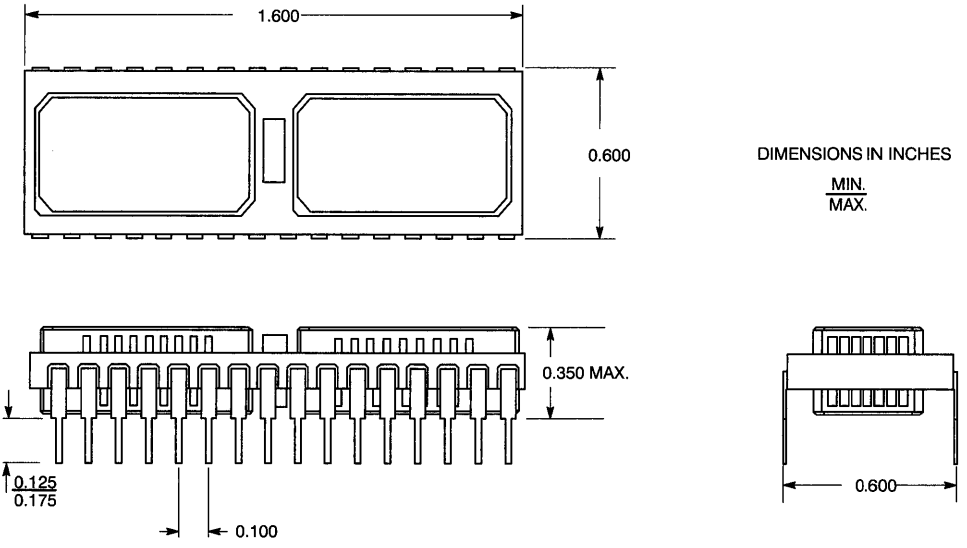
60-Pin Ceramic DIP Module HD06



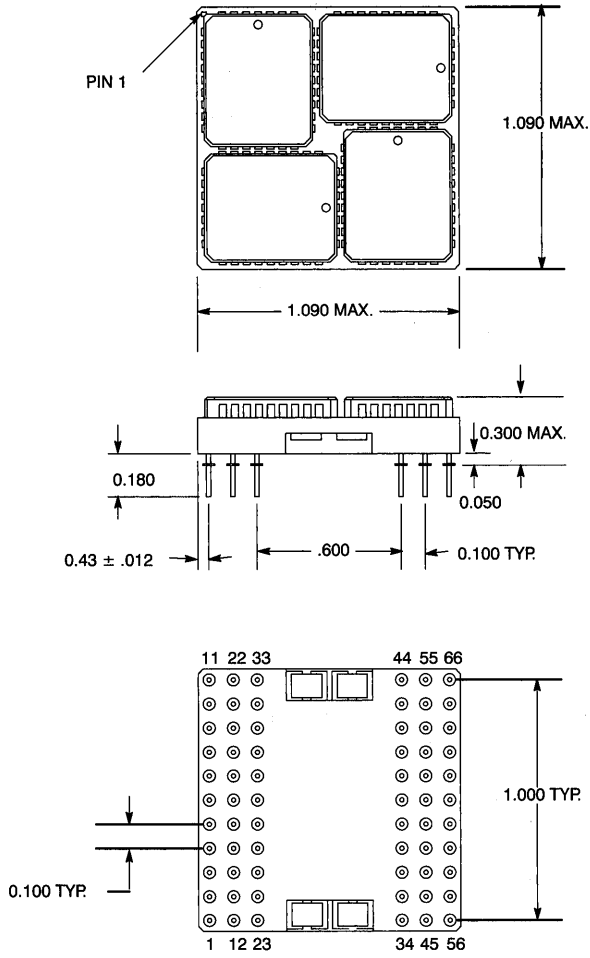
28-Pin Ceramic DIP Module HD10



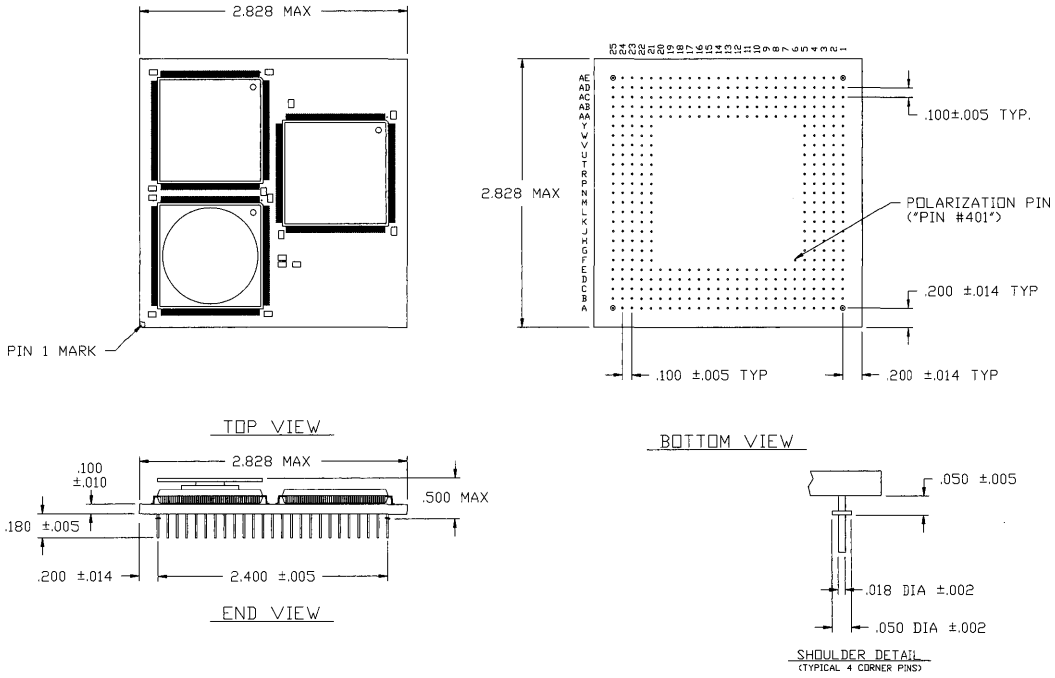
32-Pin DIP Module HD12



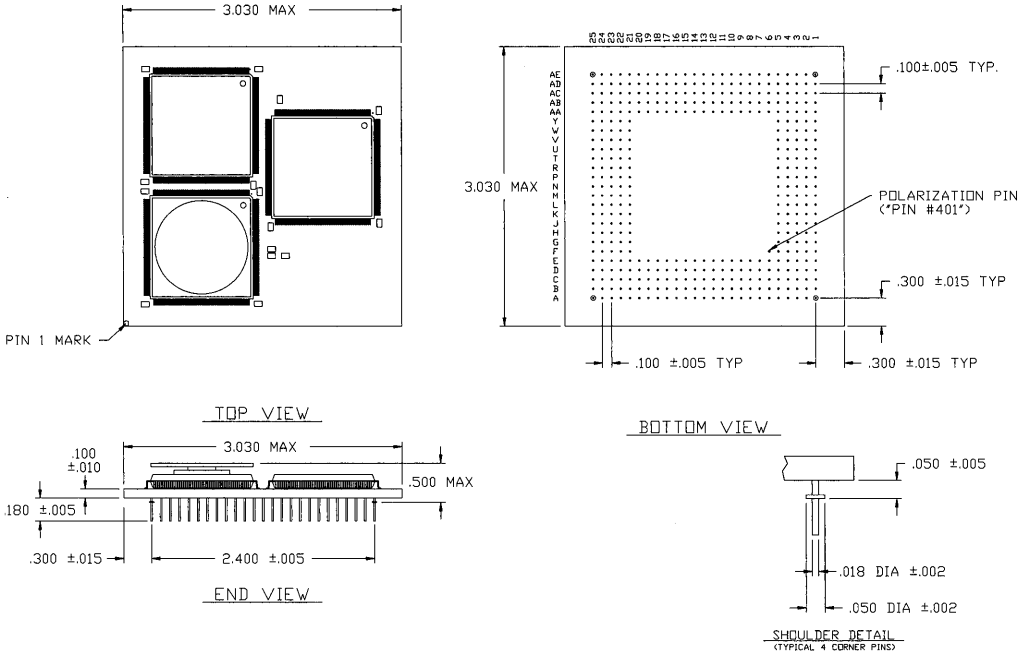
66-Pin PGA Module HG01



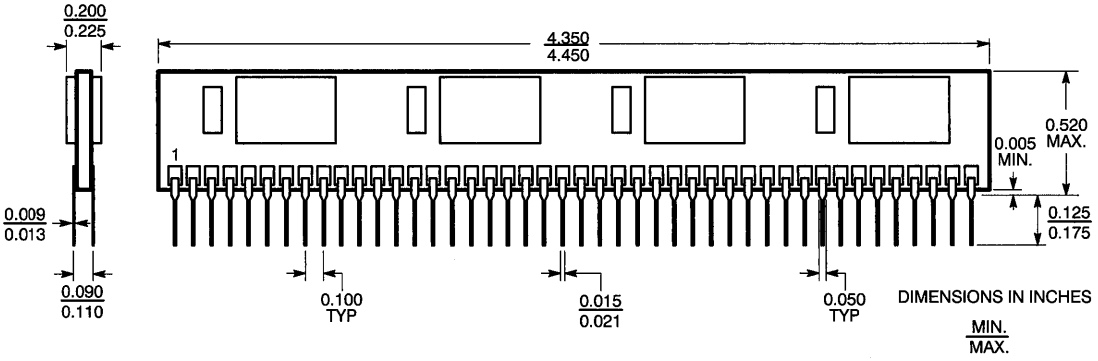
401-Pin PGA Module HG02



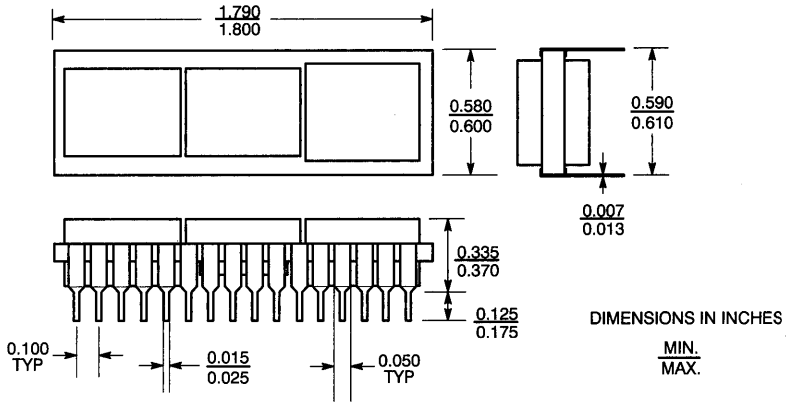
401-Pin PGA Module HG03



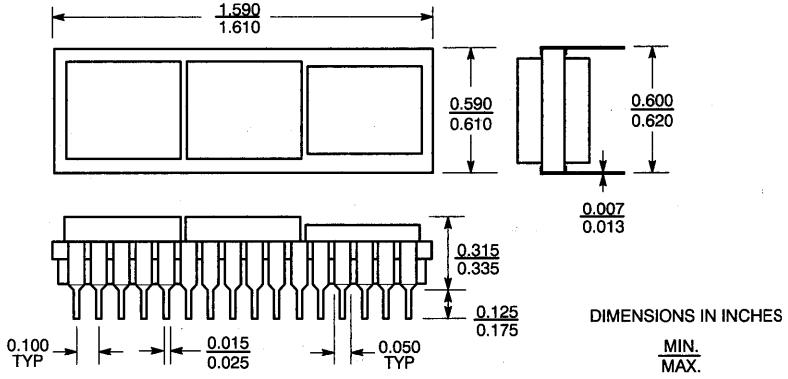
88-Pin Vertical DIP Module HV02



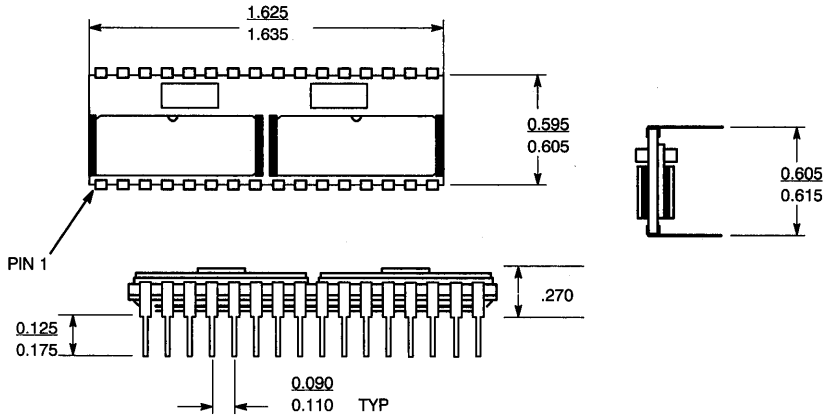
32-Pin DIP Module PD01



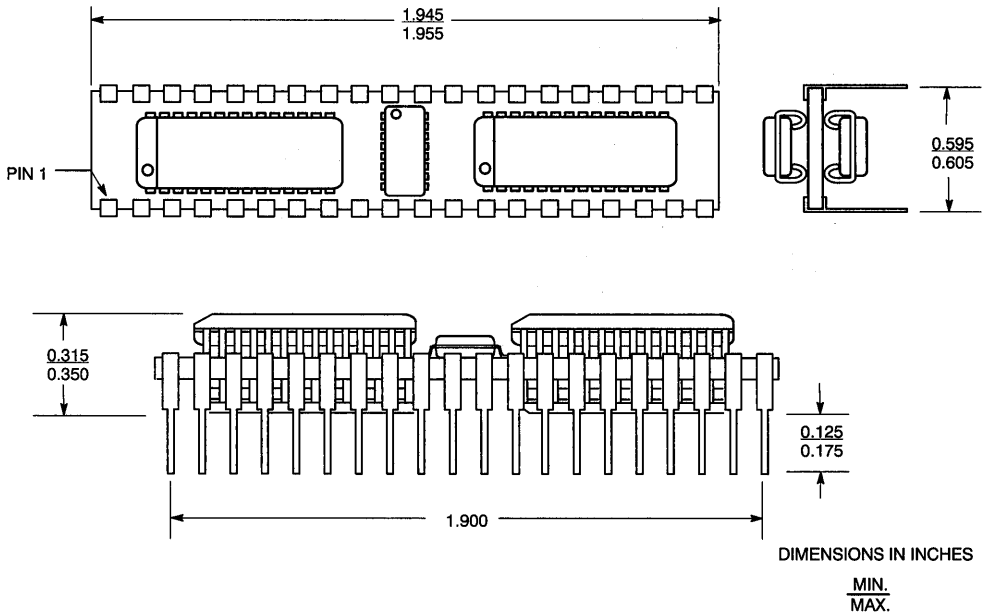
32-Pin DIP Module PD02



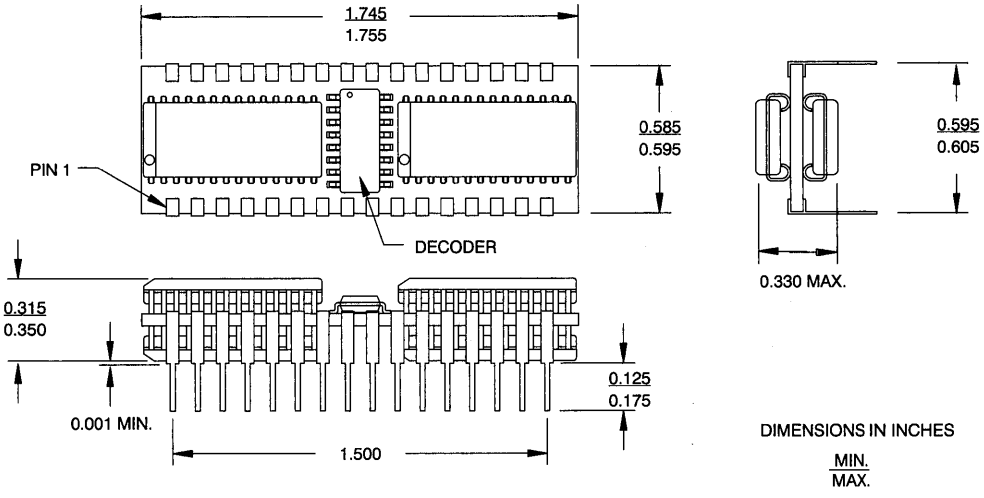
32-Pin DIP Module PD03



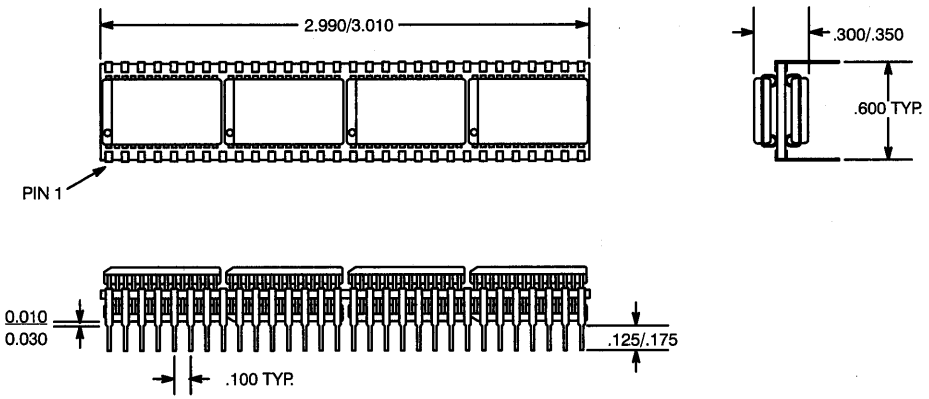
40-Pin DIP Module PD04



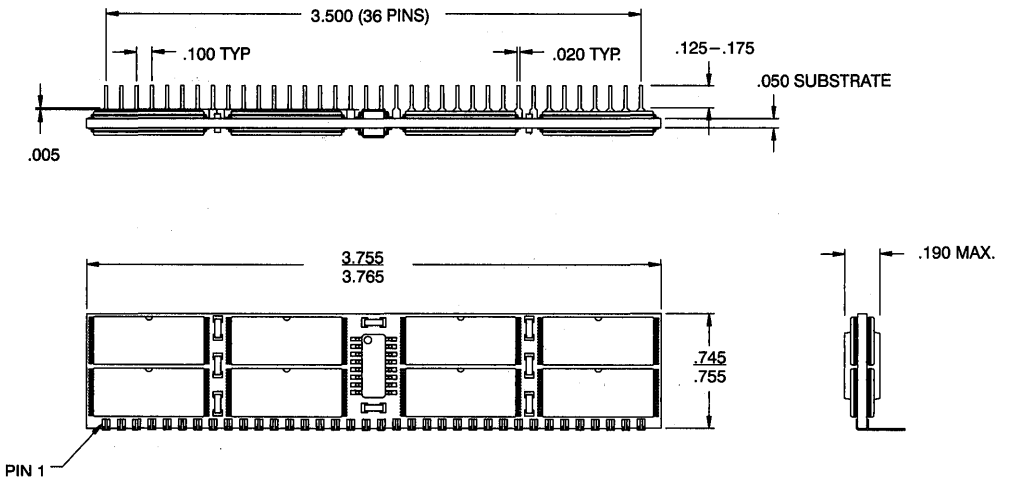
32-Pin DIP Module PD05



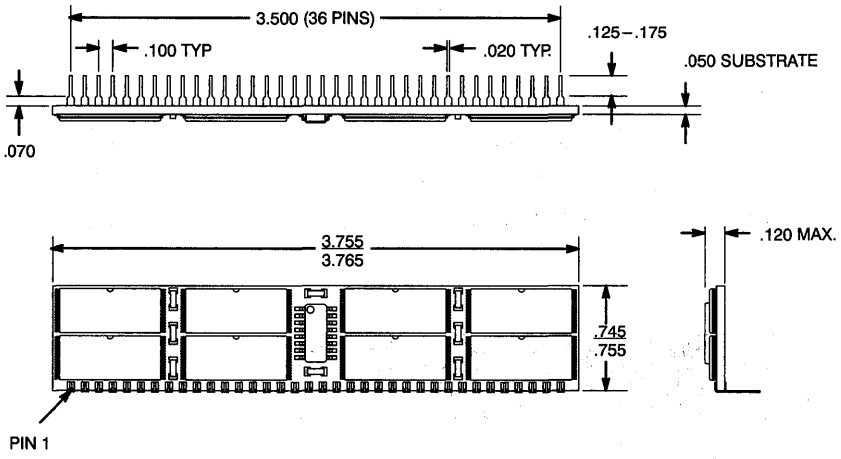
60-Pin DIP Module PD06



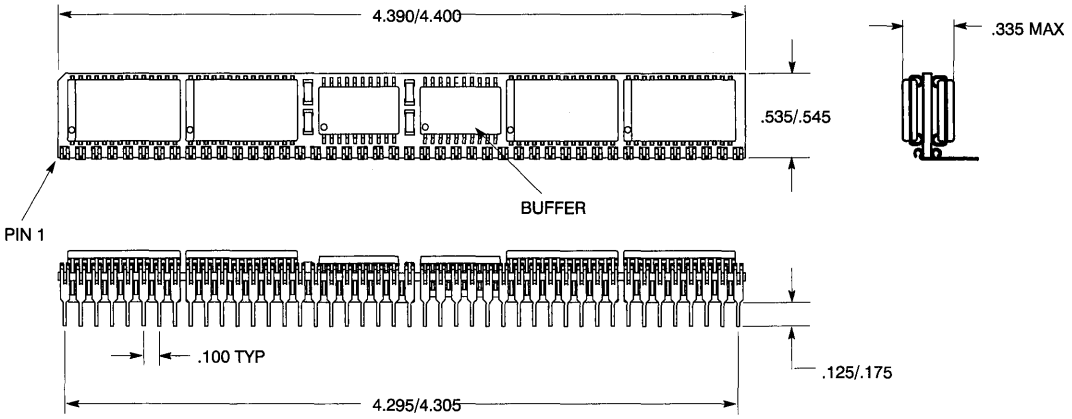
36-Pin Flat SIP Module PF04



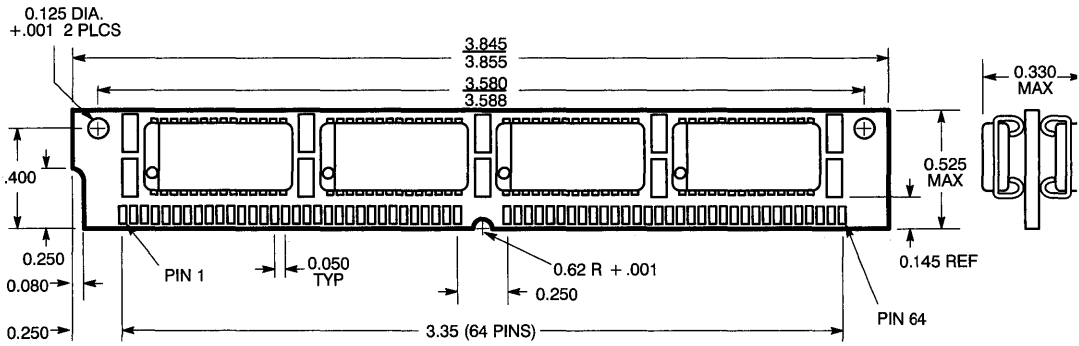
36-Pin Flat SIP Module PF05



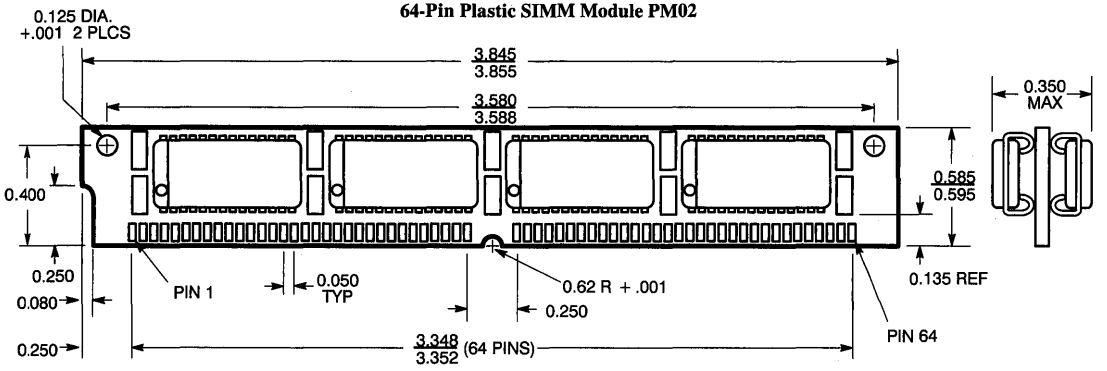
44-Pin Flat SIP Module PF06



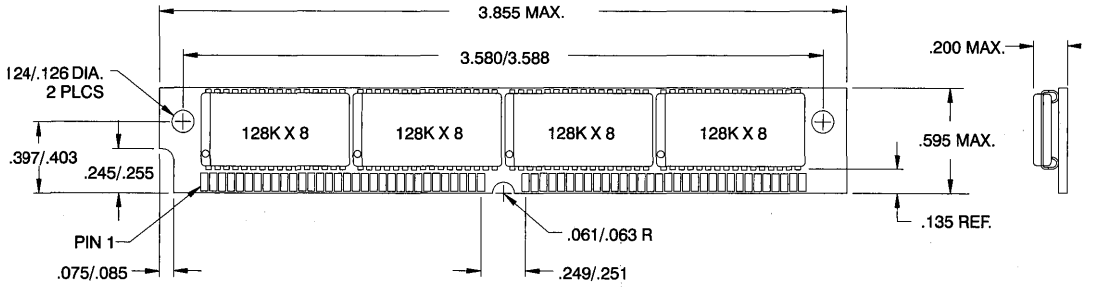
64-Pin Plastic SIMM Module PM01



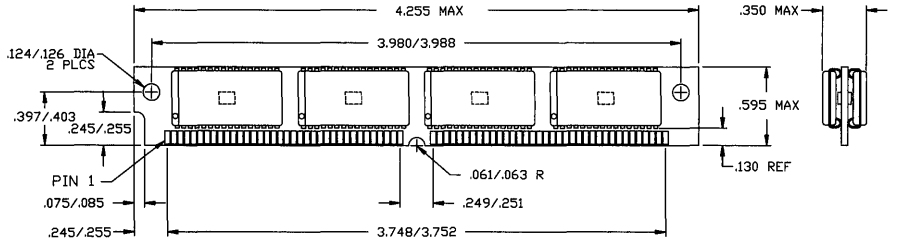
64-Pin Plastic SIMM Module PM02



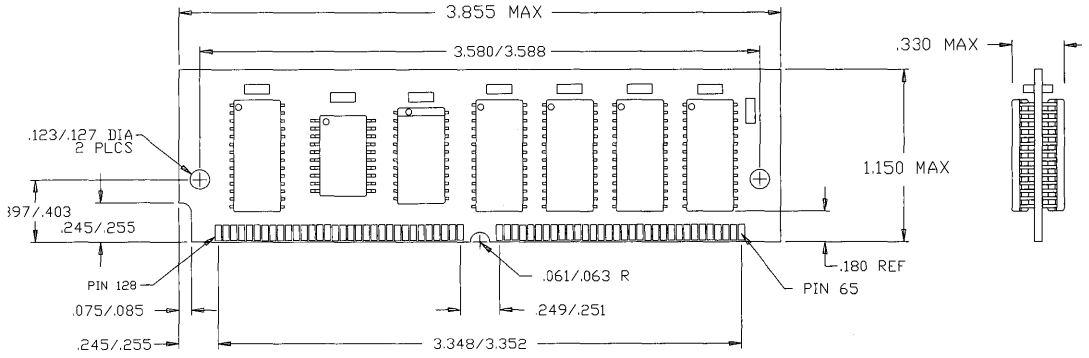
64-Pin SIMM Module PM03



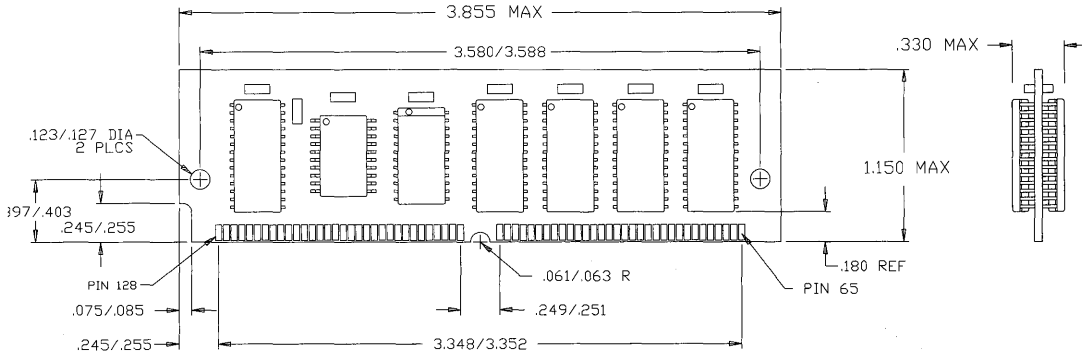
72-Pin Plastic SIMM Module PM04



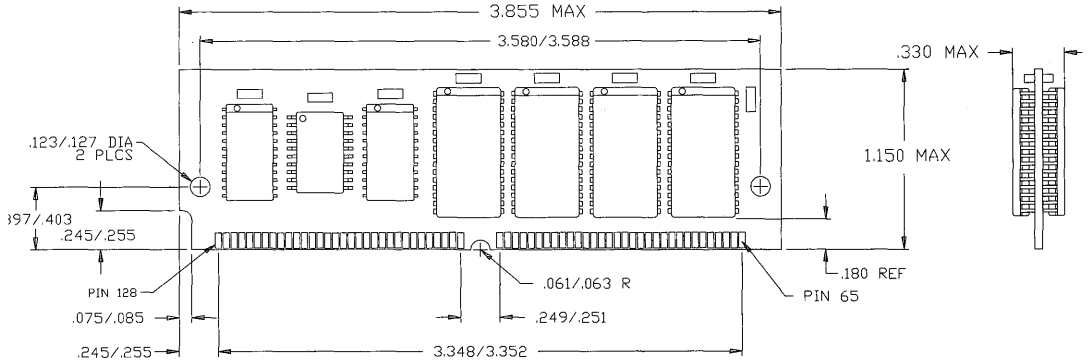
128-Pin Dual-Readout SIMM Module PM05



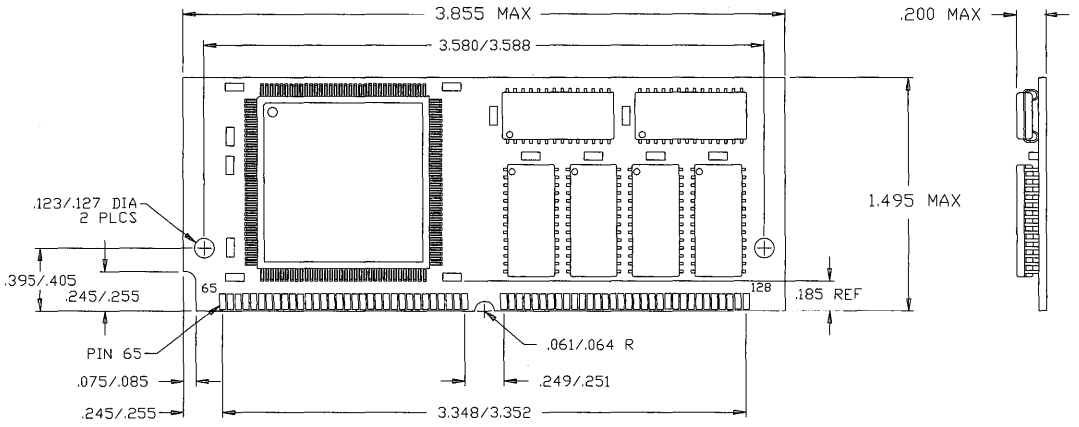
128-Pin Dual-Readout SIMM Module PM06



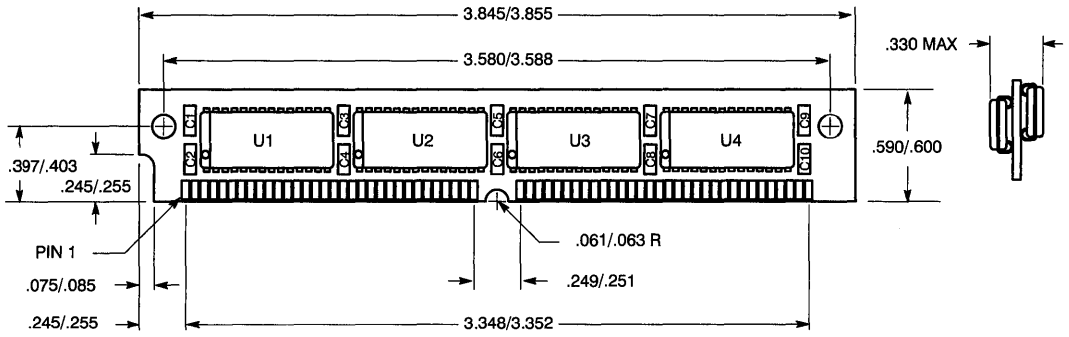
128-Pin Dual-Readout SIMM Module PM07



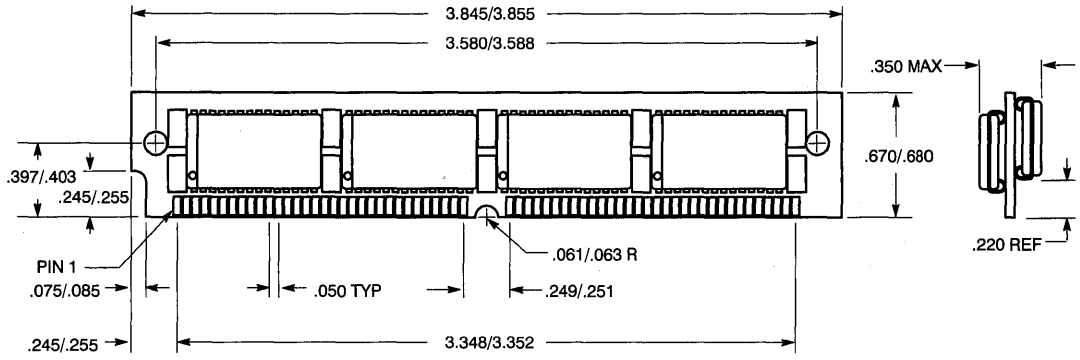
128-Pin Dual-Readout SIMM PM08



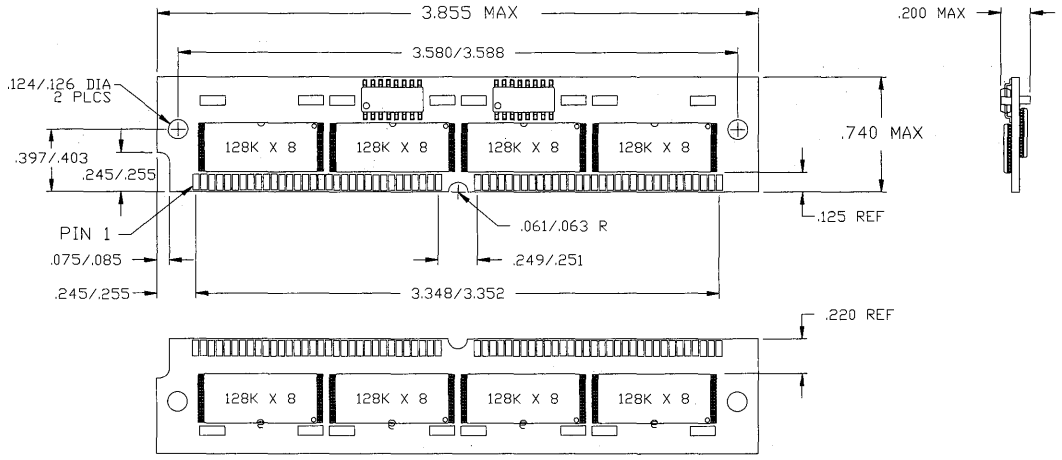
64-Pin Plastic Angled SIMM Module PN01



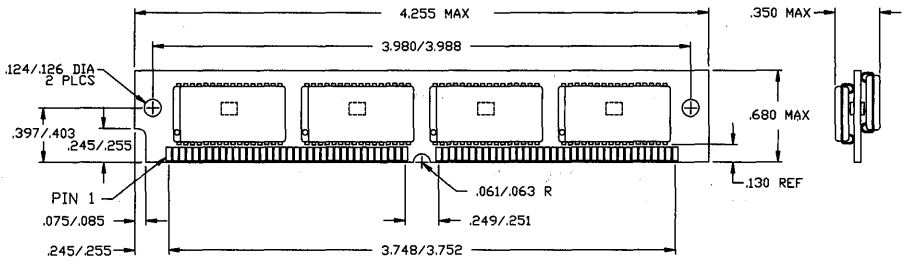
64-Pin Plastic Angled SIMM Module PN02



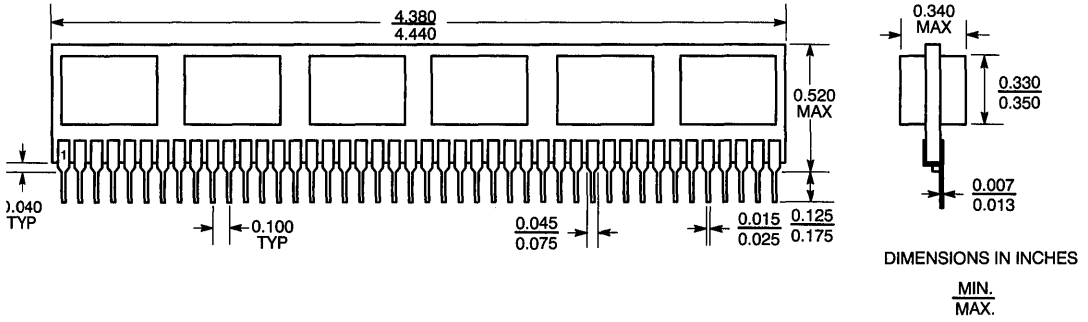
64-Pin Plastic Angled SIMM Module PN03



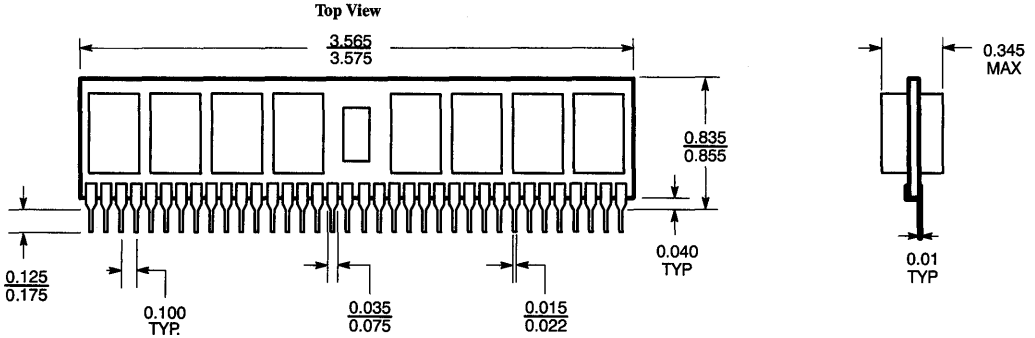
72-Pin Plastic Angled SIMM Module PN04



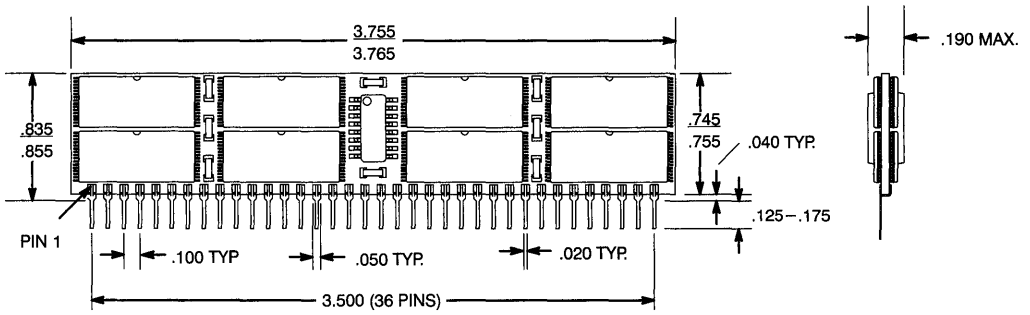
44-Pin Plastic SIP Module PS04



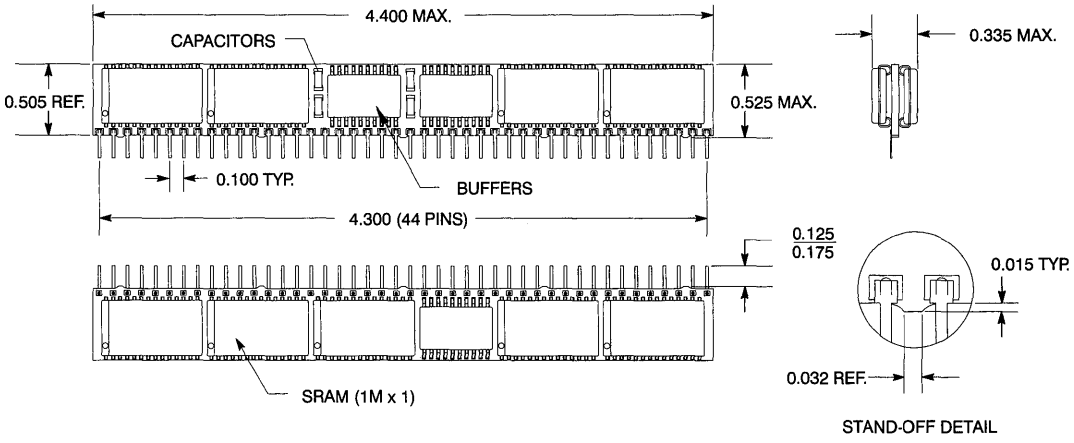
36-Pin SIP Module PS05



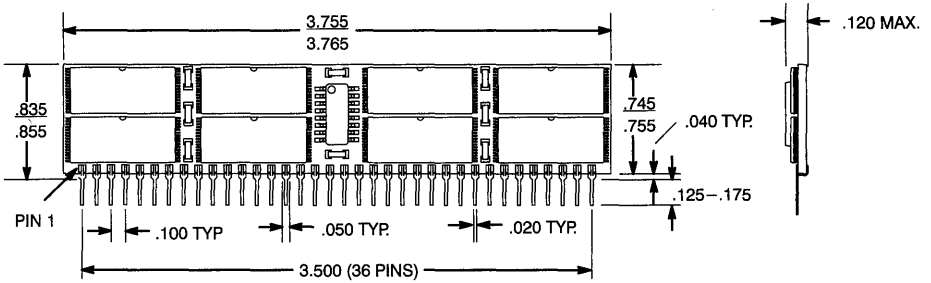
36-Pin SIP Module PS06



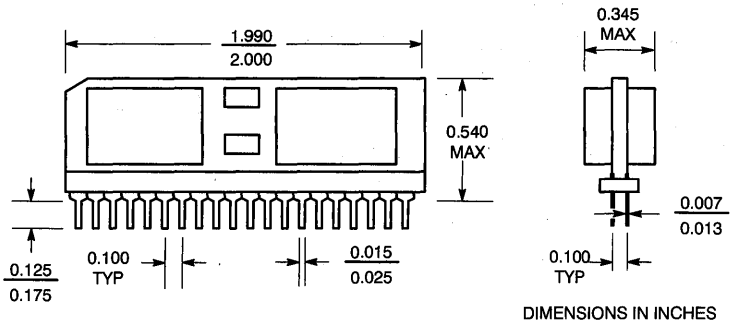
44-Pin Plastic SIP Module PS07



36-Pin SIP Module PS08



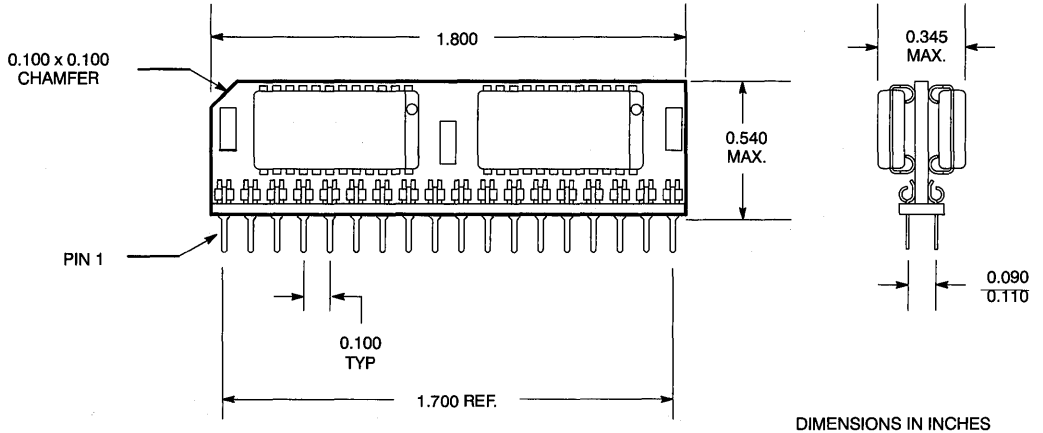
40-Pin VDIP Module PV01



DIMENSIONS IN INCHES

MIN.
MAX.

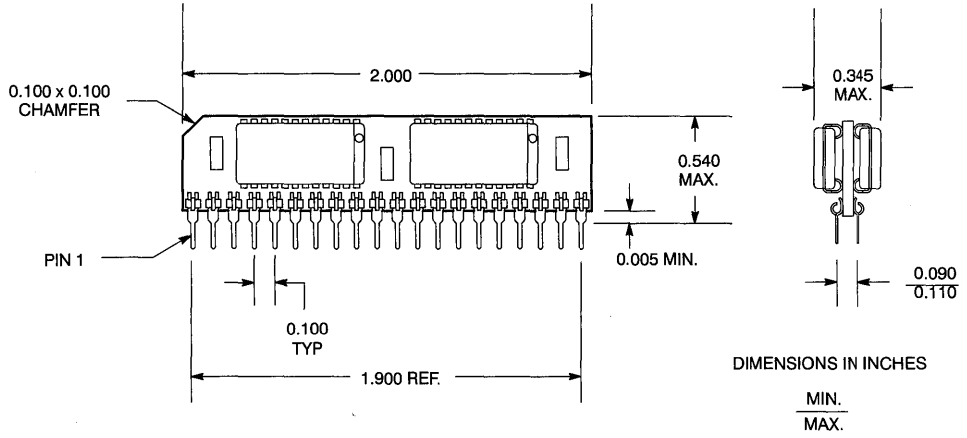
36-Pin Plastic Vertical DIP Module PV03



DIMENSIONS IN INCHES

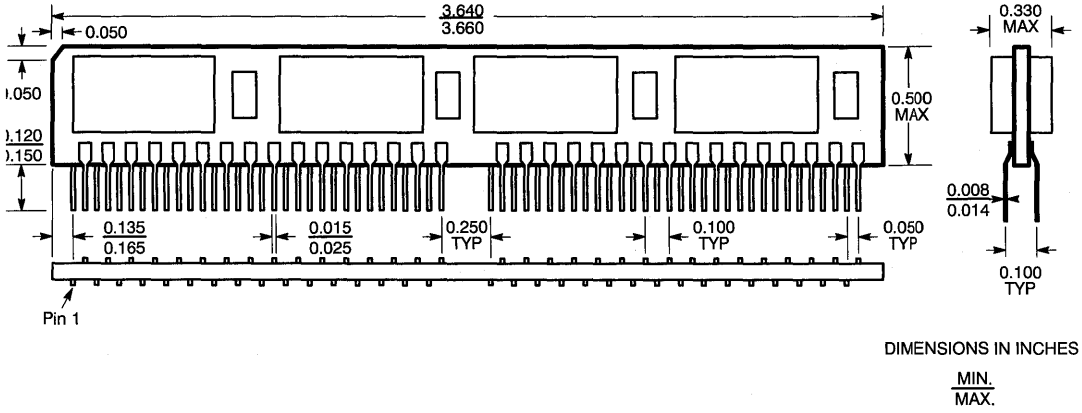
MIN.
MAX.

40-Pin Plastic VDIP Module PV04

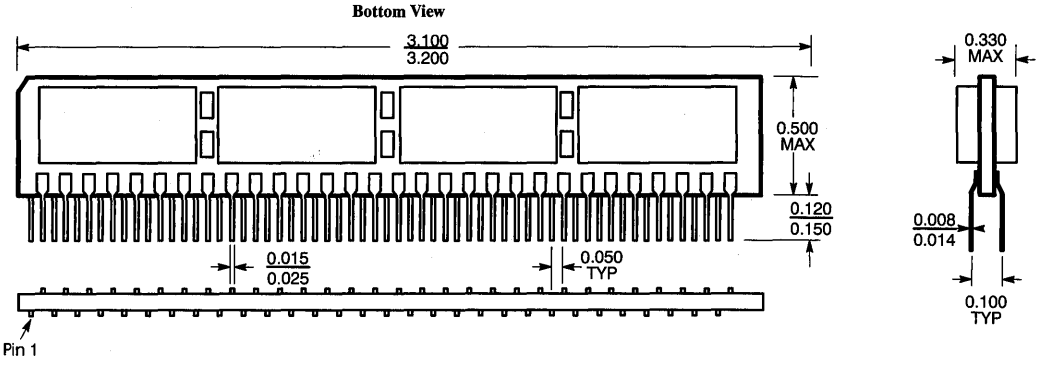


64-Pin Plastic ZIP Module PZ01

Bottom View



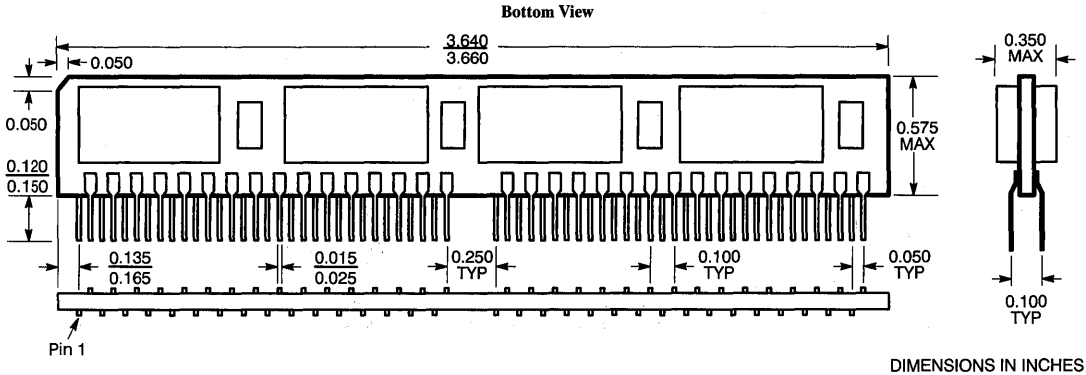
60-Pin Plastic ZIP Module PZ02



DIMENSIONS IN INCHES

MIN.
MAX.

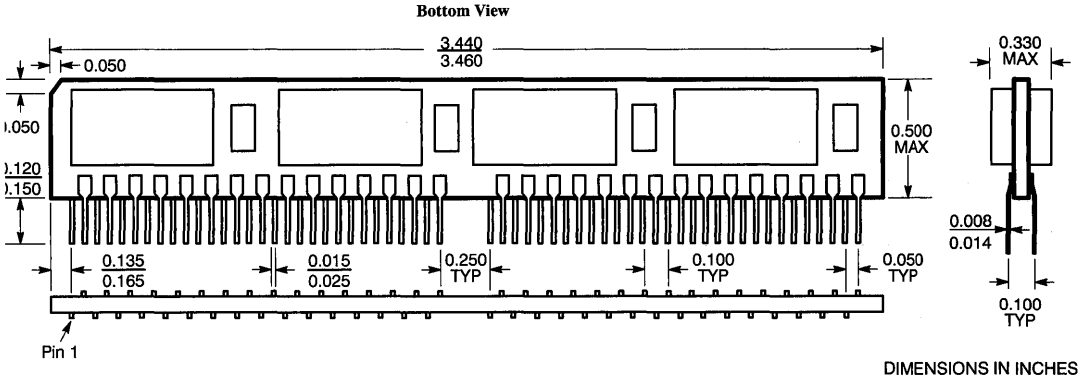
64-Pin Plastic ZIP Module PZ03



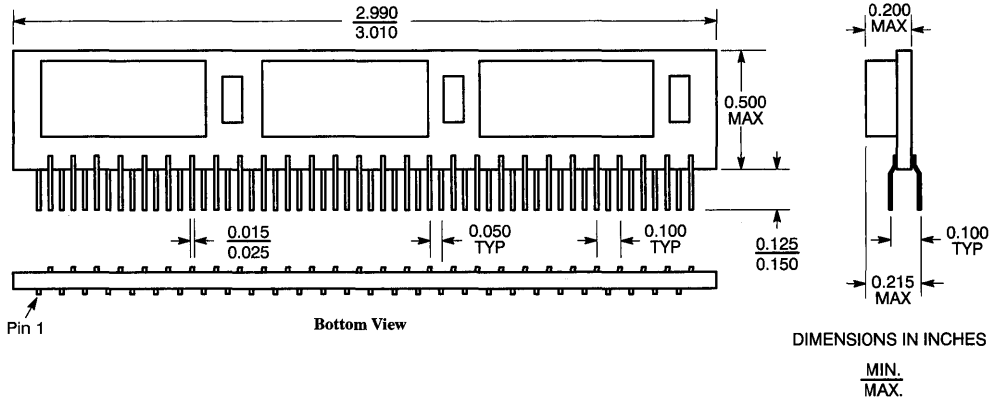
DIMENSIONS IN INCHES

MIN.
MAX.

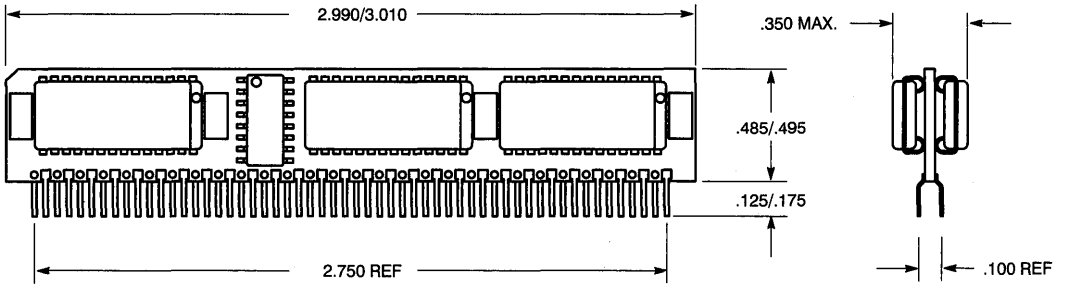
60-Pin ZIP Module PZ04



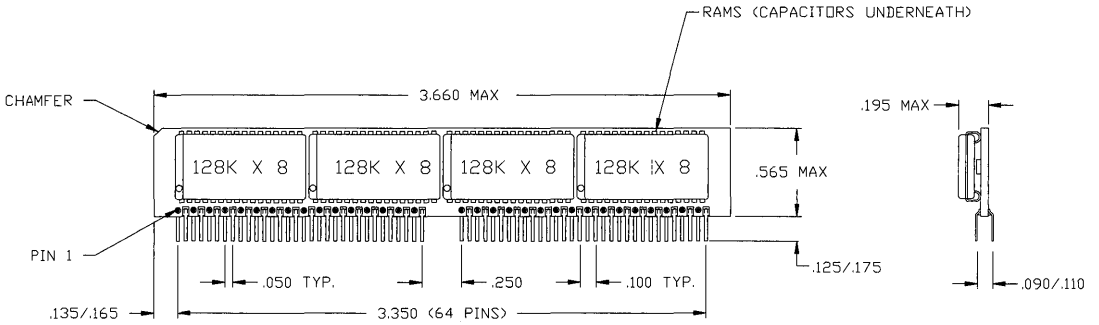
56-Pin ZIP Module PZ05



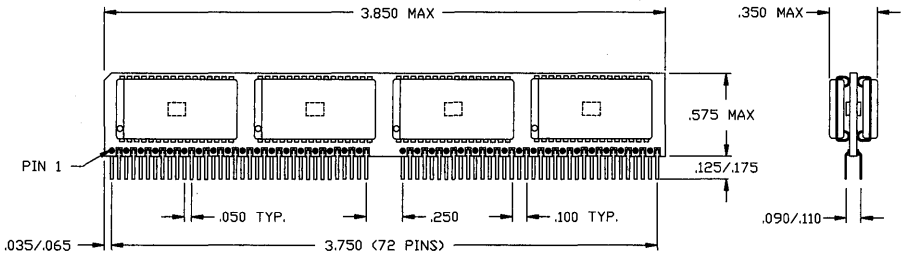
56-Pin ZIP Module PZ07



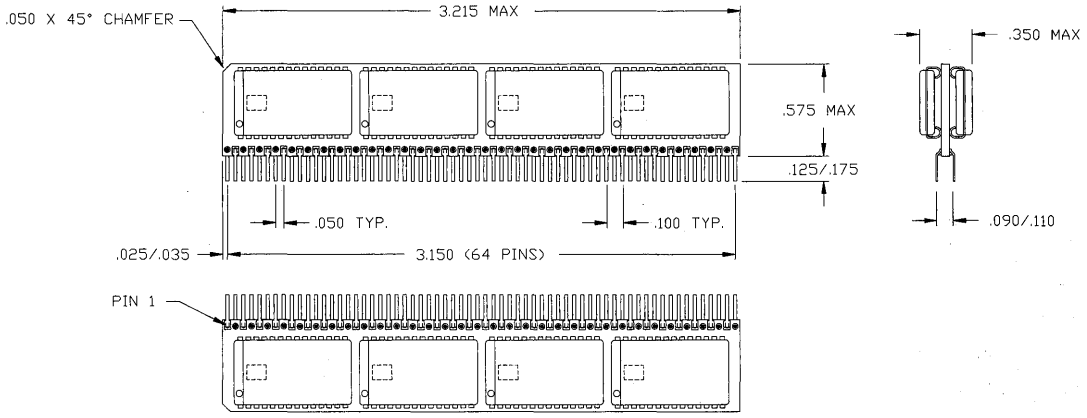
64-Pin ZIP Module PZ08



72-Pin Plastic ZIP Module PZ09



64-Pin ZIP Module PZ10



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(215) 639–6663
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Cypress Semiconductor
333 West Campbell Rd., Ste. 240
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(214) 437–0496
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Great Hills Plaza
9600 Great Hills Trail, Ste. 150W
Austin, TX 78759
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FAX: (512) 338–0865

Cypress Semiconductor
20405 SH 249, Ste. 216
Houston, TX 77070
(713) 370–0221
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Cypress Semiconductor
3151C Anchorway Court
Falls Church, VA 22042
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Alabama

Giesting & Associates
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Arizona

Thom Luke Sales, Inc.
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FAX: (602) 451–0172

California

TAARCOM
451 N. Shoreline Blvd.
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TAARCOM
735 Sunrise Ave., Suite 200
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Canada

bbd Electronics, Inc.
6685–1 Millcreek Dr.
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bbd Electronics, Inc.
298 Lakeshore Rd., Ste. 203
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(514) 697–0801
FAX: (514) 697–0277

bbd Electronics, Inc. — Ottawa
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FAX: (416) 821–4092

bbd Electronics, Inc. — Winnipeg
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HLM
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CM Marketing
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CM Marketing
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Giesting & Associates
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Technology Mktg. Corp.
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Technology Mktg. Corp.
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Technology Marketing Corp.
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Midwest Technical Sales
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Syracuse, NY 13203
(315) 432–8232
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Reagan/Compar
3301 Country Club Road
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Electronic Technical Sales
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Cypress Semiconductor Manchester
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FAX: (32) 2–460–1200

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FAX: (49) 711 7655181

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Metronik GmbH
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8500 Nurnberg 70, Germany
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SASCO GmbH
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SASCO GmbH
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SASCO GmbH
Hainer Weg 48
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SASCO GmbH
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SASCO GmbH
Am Uhrturm 7
3000 Hannover 81, Germany
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Telex: 921123
FAX: (0511) 8 43 76 18

SASCO GmbH
Europaallee 3
2000 Norderstedt, Germany
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Telex: 2165623
FAX: (040) 5 23 23 78

Hong Kong

Tekcomp Electronics, Ltd.
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Kowloon, Hong Kong
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Telex: 38513 TEKHL
FAX: (852) 7–805-871

India

Spectra Innovations Inc.
Manipal Centre, Unit No. S–822
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Bangalore–560,042
Karnataka, India
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Telex: 845 2696 or 8055
(Attn: ICTP–705)
FAX: 80–586–872

Israel

Talviton Electronics
P.O. Box 21104, 9 Biltmore Street
Tel Aviv 61 210, Israel
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Telex: 33400 VITKO
FAX: (972) 3–544–2085

Italy

Dott. Ing. Guiseppe De Mico s.p.a.
V. Le Vittorio Veneto, 8
I–20060 Cassina d'Pechi
Milano, Italy
Tel: (39) 29–53–43–600
Telex: 330869 DEMICO I
FAX: (39) 29–52–19–12

Silverstar Ltd. SPA
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20126 Milano, Italy
Tel: (39) 2 661251
Teles: 33 2189 SIL 7I
FAX: (39) 2 66101359

Japan

Tomen Electronics Corp.
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Tokyo, 100 Japan
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Telex: 23548 TMELCA
FAX: (81) 3–3506–3497

CTC Components Systems Co. Ltd.
4–8–1, Tsuchihashi,
Miyamae–Ku, Kawasaki–Shi,
Kanagawa, 213 Japan
Tel: (81) 44–852–5121
Telex: 3842272 CTCEC J
FAX: (81) 44–877–4268

Fuji Electronics Co., Ltd.
Ochanomizu Center Bldg.
3–2–12 Hongo, Bunkyo–Ku
Tokyo, 113 Japan
Tel: (81) 3–3814–1411
Telex: J28603 FUJITRON
FAX: (81) 3–3814–1414

N.D.A. Co. Ltd.
The Second Preciza Bldg.
4–8–3 Iidabashi Chiyoda–Ku
Tokyo, 102 Japan
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Telex: J29503 ISI JAPAN
FAX: (81) 3–3264–3419

Fujitsu Devices, Inc.
Osaki West Bldg.
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Shinagawa–ku
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FAX: (81) 3–3490–7274

Japan Electronics
Materials Co., Ltd (JEMCO)
2–20–10 Minamikaneda, Suita-shi,
Osaka 564 Japan
Tel: (81) 6–385–6707
FAX: (81) 6–330–6814

Ryoyo Electro Corporation
Knowa Bldg., 1–12–22 Tsukiji,
Chuo–ku, Tokyo 104 Japan
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Logicom Inc.
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FAX: (822) 888–7040

superCHIP Inc.
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Norway

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Singapore

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ATD Electronica
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08029 Barcelona, Spain
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TH:s Elektronik AB
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Switzerland

Basix für Elektronik A. G.
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Telex: 822762 BAEZ CH
FAX: (41) 1–276–14–48

Taiwan R.O.C.

Prospect Technology Corp.
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Arrow Electronics (UK) Ltd.
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Tel: (44) 234 270272
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Pronto Electronic System Ltd.
City Gate House
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Essex, U. K. IG2 6LR
Tel: (44) 81–554–62–22
Telex: 8954213 PRONTO G
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