CIRRUS LOGIC

CL-SH370

Product Bulletin

FEATURES

Microcontroller Interface:

- Supports high-speed multiplexed/nonmultiplexed microcontroller interfaces (e.g., 16-MHz 8051, 12-MHz 68HC11, 30-MHz HPC460X3, HPL460X3, Intel® 80188 and Motorola® 68H000)
- Supports direct microcontroller access to the SCSI bus, emulating-target or initiator device, buffer memory and external switches
- Supports power-down mode with auto-wakeup
- On-chip oscillator with clock output

SCSI Interface:

- Supports SCSI-2 Initiation and Target modes
- Supports asynchronous DMA/PIO transfers up to 3 MBytes/sec.
- Supports synchronous DMA/PIO transfers up to 5 MBytes/sec.
- Supports up to 15-byte synchronous transfer offsets and 12 programmable transfer periods
- Controls synchronous transfer overrun/underrun
- Controls arbitration, selection, and reselection in hardware
- Detects selected and reselected conditions automatically
- Integrates 48-mA and active pull-up SCSI bus drivers

(cont.)

Integrated SCSI Disk Controller

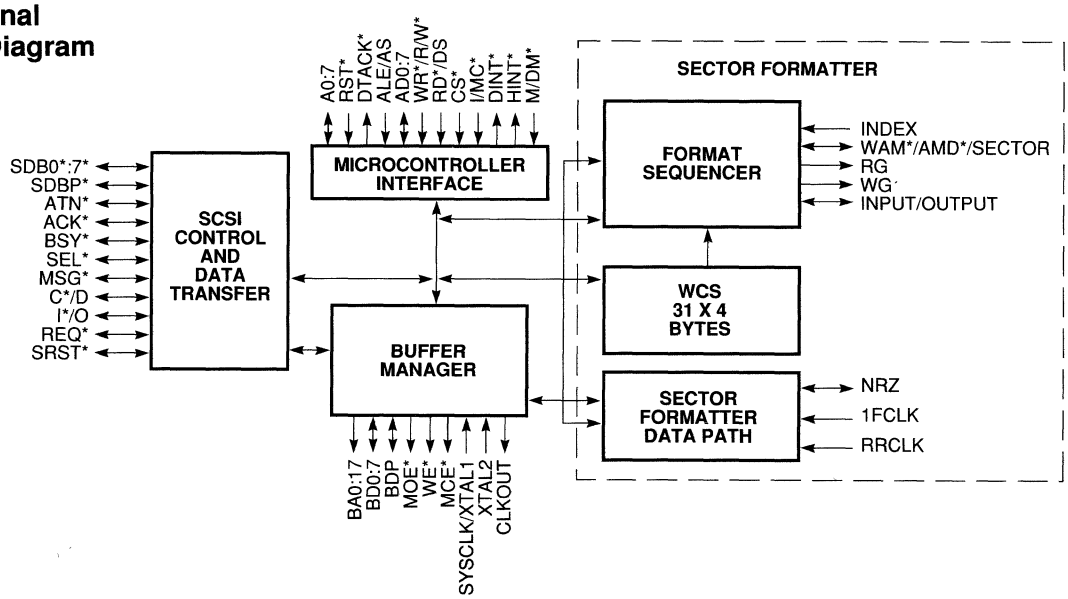
OVERVIEW

The CL-SH370 is a VLSI component that provides the majority of the hardware necessary to build a Small Computer System Interface (SCSI) Winchester disk controller. The CL-SH370 design combines a high-speed local microcontroller port, extensive hardware support for the SCSI interface, a four-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SH370, along with a local microcontroller, system ROM and RAM, and an optional data separator, completes a disk controller subsystem with high performance at a low overall cost.

A local microcontroller provides the CL-SH370 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host control.

(cont.)

Functional Block Diagram



FEATURES (cont.)

Sector Formatter:

- Full-track multi-sector transfer capability
- Transfers SCSI information to/from the microcontroller through a 16-byte FIFO under Automatic Programmed I/O (PIO)
- Programmable Format Sequencer Writable Control Store (WCS-31 x 4 bytes)
- Supports up to 24-MHz NRZ data rates
- Allows split data field processing for embedded servo and zoned designs
- Provides 16-bit CRC and 88-bit Reed-Solomon ECC with on-the-fly correction
- Programmable on-the-fly error burst length

Buffer Manager:

- Quad-channel, circular buffer control with priority resolution
- Direct buffer addressing up to 256 KBytes of SRAM
- Supports streaming mode and automatic host and disk operation in the same circular buffer simultaneously, with a pacing mechanism to prevent overrun and underrun
- Supports multi-track, minimal-latency operations
- Permits concurrent buffer memory throughput of up to 12 MBytes/sec.
- Odd-parity data verification between the SCSI bus and the Sector Formatter
- Flexible buffer segmentation logic
- Automatic SCSI disconnect/reconnect with local interrupt for programmable buffer threshold and buffer empty/full conditions

Technology:

- 100-pin Quad Flat Pack (QFP) package
- Advanced, low-power, double-metal CMOS technology

OVERVIEW (cont.)

During data transfer operations, the CL-SH370 requires only minimal intervention from the local microcontroller. The microcontroller- to-CL-SH370 communication path is a multiplexed/nonmultiplexed address and data bus similar to that provided by the Intel® 8051- and the Motorola® 68HC11-class of controllers. (There is a configuration signal available to allow for either family of data control signal methods). The CL-SH370 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The SCSI Host interface is designed for compliance with the proposed SCSI-2 specification. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SH370. The SCSI interface logic includes integrated high-current (48-mA) drivers and programmable active pullups for the single-ended option. Both the asynchronous and synchronous transfer protocols are supported in either Initiator or Target mode. Routine bus control operations, such as arbitration, selection and reselection, are automatically sequenced in hardware. This method of implementing the SCSI interface makes the SCSI protocol firmware extremely flexible and very efficient.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 24 MHz and can perform automatic multi-sector transfers up to a complete track, while handling multiple data-segments per sector. The Sector Formatter is subdivided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter Data path consists of the NRZ-data-handling circuitry that includes the serializer/deserializer (SERDES), the 88-bit Reed-Solomon ECC and 16-bit CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The actual buffer memory may be implemented with static or dynamic RAM devices. The CL-SH370 Buffer Manager is programmable to provide all of the necessary address and control signals for RAM devices of varying access times. Up to 256 KBytes of SRAM can be directly addressed by the CL-SH370. The buffer manager allows fully automatic host-to-media and media-to-host multisector transfers, while monitoring the state of the buffer to identify buffer full/empty conditions, and programmable data thresholds. These conditions can be monitored to automatically disconnect or reconnect from the SCSI bus.

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PIN DESCRIPTION

Symbol	*Pin Number*	*Type*	*Description*
Microcontroller Interface Pins			
DINT*	16	O, OD, Z	Disk Interrupt
CS	17	I	Chip Select
WR*/R/W*	18	I	Write Strobe/Read/Write
RD*/DS	19	I	Read Strobe/Data Strobe
DTACK*	20	OD	Data Transfer Acknowledge
I/MC*	23	I	Intel/Motorola
HINT*	27	O, OD, Z	Host Interrupt
AD0:7	33-28, 22-21	I/O	Local Microcontroller Address/Data Bus
A0:7	36-39, 41-44	I/O	Local Microcontroller Address Bus
M/DM*	26	I	Multiplexed/Demultiplexed Address Configuration
ALE/AS	34	I	Address Latch Enable/Address Strobe
RST*	45	I	Reset
SCSI Bus Interface Pins			
SDB0*:7*	58-59, 61-63, 65-67	I/O, OD	SCSI Data Bus
SDBP*	69	I/O, OD	SCSI Data Bus Parity
ATN*	70	I/O, OD	SCSI Attention
BSY*	71	I/O, OD	SCSI Busy
ACK*	74	I/O	SCSI Acknowledge
SRST*	80	I/O, OD	SCSI Reset
MSG*	76	I/O, OD	SCSI Message
SEL*	75	I/O, OD	SCSI Select
C*/D*	77	I/O, OD	SCSI Command/Data
REQ*	72	I/O	SCSI Request
I*/O	79	I/O, OD	SCSI Input/Output
Buffer Manager Interface Pins			
BD0:7	81-85, 87-89	I/O	Buffer Memory Data Bus
BDP	92	I/O	Buffer Memory Data Parity
BA0:15	93-100, 2-9	O	Buffer Memory Address Lines
BA16	11	O	Buffer Memory Address 16
BA17	12	O	Buffer Memory Address 17
MCE*	13	O	Memory Chip Enable
MOE*	14	O	Memory Output Enable
WE*	15	O	Write Enable
SYSCLK/XTAL1	46	I	System Clock or XTAL1 (crystal input 1)
XTAL2	47	I	XTAL2 (crystal input 2)
CLKOUT	48	I	Clock Output
Sector Formatter Interface Pins			
INPUT/OUTPUT	57	I	Format Sequencer Input/Output
INDEX	49	I	Index
WAM*/AMD*/SECTOR	50	I/O	Write Address Mark/Address Mark Detect/Sector
RG	54	O	Read Gate
WG	55	I	Write Gate
RRCLK	52	I	Read Reference Clock
NRZ	53	I/O	Non-return to Zero
1FCLK	56	I	1FCLK (clocks ECC correction circuitry)
Power and Ground Pins			
BGND	1, 10, 86	N/A	Buffer Ground Pins
LGND	24, 25, 40	N/A	Logic Ground Pins
+5V	35, 51, 90, 91	N/A	Power Supply (+5) Pins
SGND	60, 64, 68, 73, 78	N/A	High Current SCSI Ground Pins

Note: (*) denotes negative true signal. I indicates input pin; O indicates output pin; I/O indicates input/output pin; OD indicates open drain output pin; Z indicates tri-state output or input/output pins. All unused input pins must be tied to GND or VDD appropriately. SGND, BGND and LGND are connected to three separate ground rings internally.

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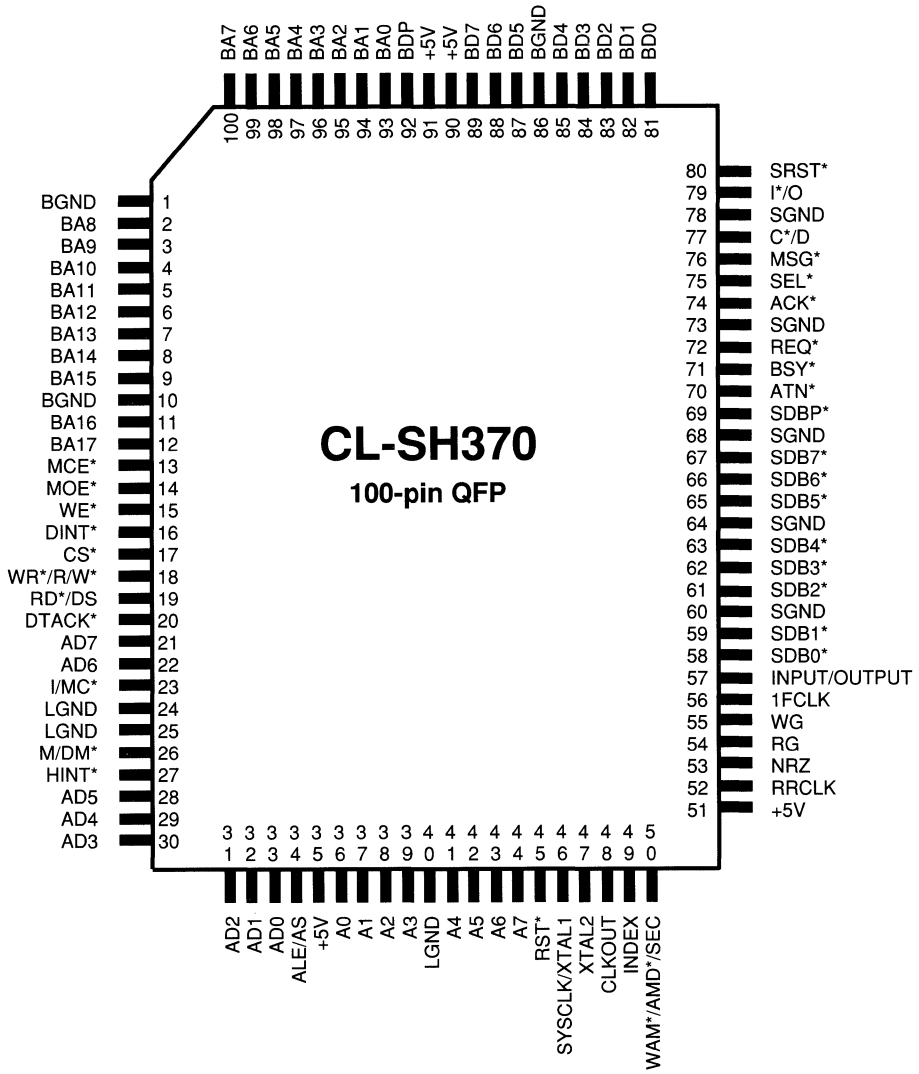
ADVANTAGES

Unique Features	Benefits
• *Programmable wait states for microcontroller*	Allows the fastest microcontrollers to operate without degrading bus performance.
• *Pin-configurable microcontroller data control interface*	Allows for direct connect to Intel- or Motorola-style microcontrollers.
• *Separate disk and host microcontroller interrupts*	Supports faster, more direct interrupt processing by microcontroller.
• *15-byte offset in synchronous mode*	Greater flexibility for synchronous data transfer negotiations.
• *16-byte FIFO for automatic PIO transfers*	Decreases command and information transfer overhead.
• *Four Buffer Manager DMA channels*	Enables read-look-ahead for high performance.
• *Direct 256K SRAM addressing*	Increases buffer size alternatives to support caching.
• *Odd through parity buffer verification*	Improves data integrity between host and disk data transfers.
• *Variable buffer segmentation logic*	Allows protected data segments in buffer.
• *Advanced-programmable branch conditions in the Writable Control Store (WCS) program*	Supports flexible, automated defect management and retry algorithms.
• *Conditional Format Sequencer execution of up to four paths*	Supports end-of-track, retry and defect management code.
• *Programmable read synchronization timeout*	Simplifies ID and Data Field searches.
• *"On-the-fly" error correction circuitry*	Enables high-speed ECC correction within half a sector time period.
• *Multiple data field processing within the ECC*	Provides support for embedded servo drives, zoned drives and large defect skipping.
• *Automatic disconnect/reconnect with local interrupt on programmable buffer empty/full threshold*	Optimizes SCSI Bus utilization.
• *Automatic multisector transfer between host and disk*	Reduces local microcontroller real-time response.
• *Minimal latency support*	Reduces the rotational latency by an average of one-half revolution.



100-pin Quad Flat Pack (QFP) Pin Diagram

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

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