CIRRUS LOGIC

PRELIMINARY DATA SHEET
June, 1987

FEATURES

- Disk interfaces supported include: ST506/412, ST412HP, ESDI, SA1000 and SMD
- Controls custom drive interfaces
- Works with all disk encoding schemes
- User-programmable internal 32-bit ECC polynomial or variable length external polynomial
- Up to 20 Mbps maximum transfer rate
- User-modifiable RAM-based control store
- User-programmable sector length up to a full track, soft or hard sector
- Multiple sector transfer
- Non-interleaved operation
- Sector-level defect handling
- High speed search capability
- Single +5V power supply
- 44-pin PLCC and 40-pin P-DIP packages
- 2-Micron double metal CMOS technology

CL – SH 130

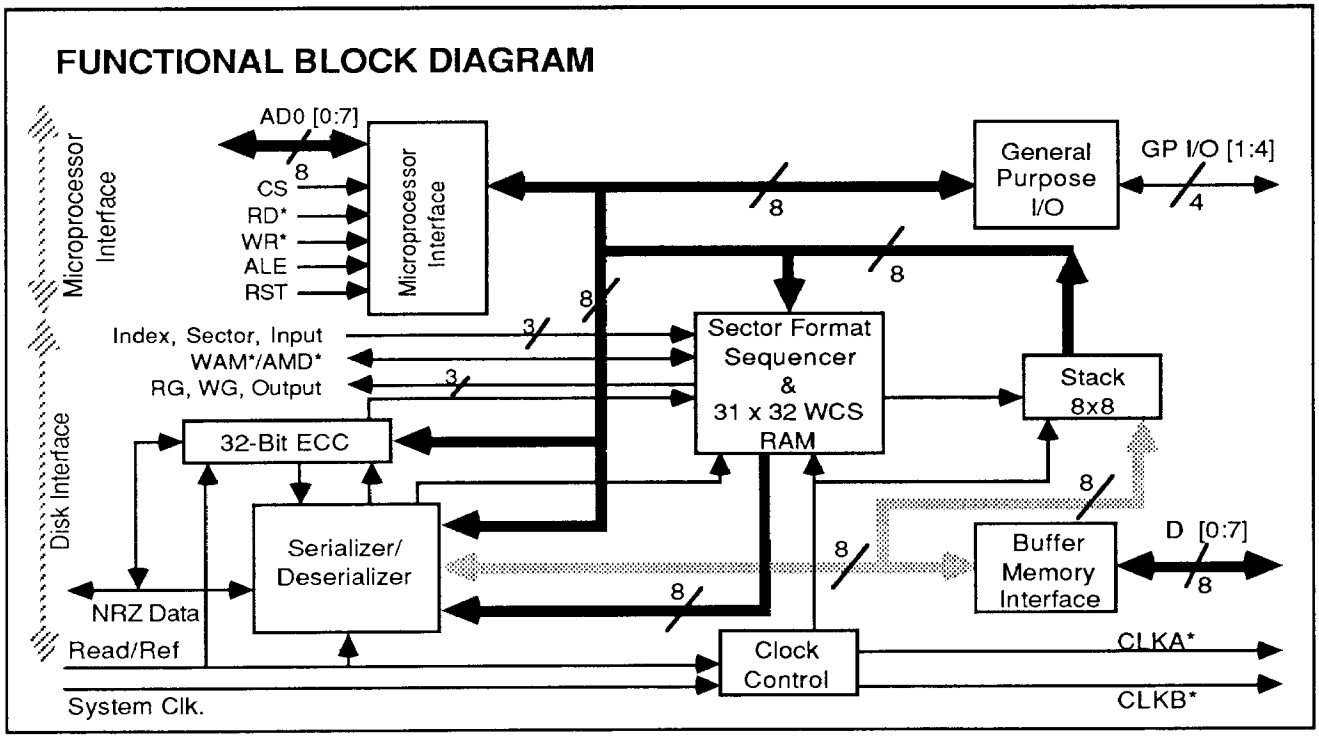
Winchester Hard Disk Formatter

OVERVIEW

The CL–SH130 is a VLSI component that provides the major portion of hardware necessary to build an intelligent Winchester disk controller. It is designed to handle non-interleaved data transfer to, or from the drive with speeds up to 20 Mbps.

The CL–SH130 is capable of supporting most drive interfaces with minimum external hardware. This component is designed to work with the CIRRUS LOGIC CL–SH120, a dual-ported buffer controller for systems requiring a buffer between controller and host bus. In conjunction with the CL–SH120, the CL–SH130 design eases the implementation of the SCSI interface, since a majority of the functionality needed for this is inherent in the overall architecture.

FUNCTIONAL BLOCK DIAGRAM



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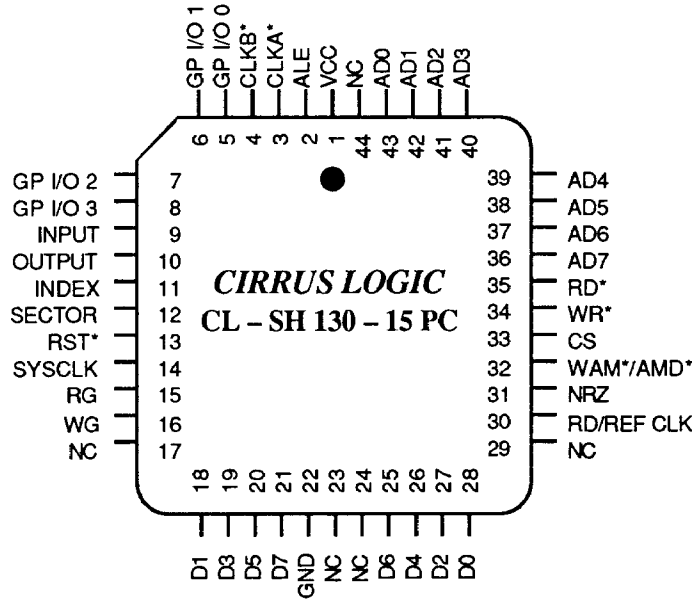
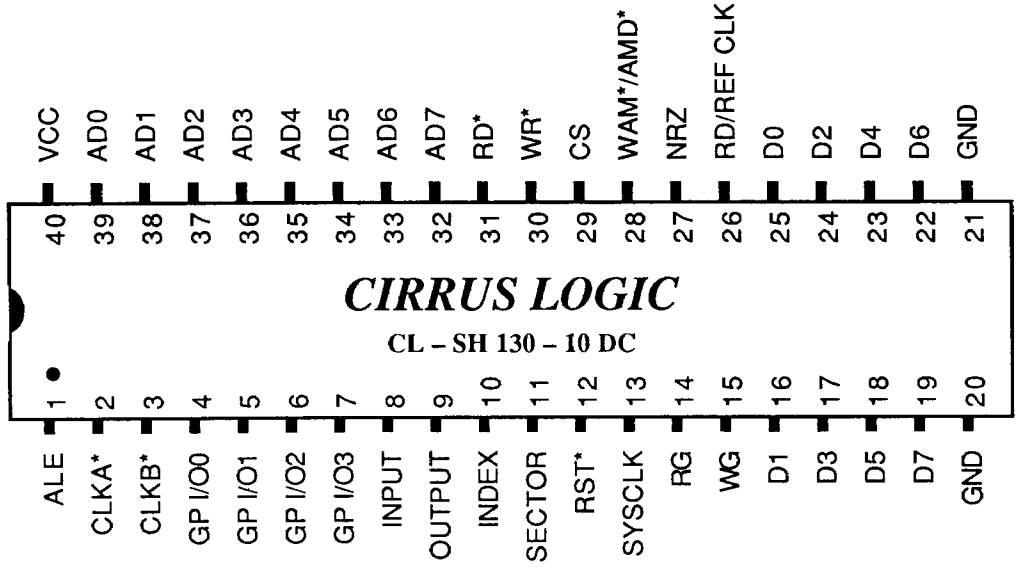


1.2 Pin Diagram For 40-Pin P-DIP



(*) Denotes negative true signal.

1.3 Pin Assignments – 44-Pin PLCC

SYMBOL	NUM.	TYPE	DESCRIPTION
VCC	1	I	POWER SUPPLY
ALE	2	I	ADDRESS LATCH ENABLE: This control signal latches the address on the AD lines.
CLKA*	3	O	CLOCK A: Used to synchronize data to and from the parallel data bus. During disk data access, this clock is derived from the RD/REF clock. Otherwise, it is derived from the input SYSCLK. The relationship of both of these clocks to CLKA* is controlled by the contents of Register 7FH.
CLKB*	4	O	CLOCK B: A pulse which overlaps the negative going edge of the CLKA* to signify the disk transfer cycle on the following negative going edge of the CLKA*.
GP I/O 0	5	I/O	GENERAL PURPOSE I/O LINE 0: A user-programmable I/O line to be used as an input or an output. This pin can also be programmed to generate a negative true strobe on a write to address 6EH.
GP I/O 1	6	I/O	GENERAL PURPOSE I/O LINE 1: A user-programmable I/O line to be used as an input or an output. This pin can also be programmed to generate a negative true strobe on a read from address 6EH.
GP I/O 2	7	I/O	GENERAL PURPOSE I/O LINE 2: A user-programmable I/O line to be used as an input or an output. This pin can also be programmed to generate a negative true strobe on a write to address 6FH.
GP I/O 3	8	I/O	GENERAL PURPOSE I/O LINE 3: A user-programmable I/O line to be used as an input or an output. This pin can also be programmed to generate a negative true strobe on a read from address 6FH.
INPUT	9	I	INPUT PIN: This pin is available to synchronize the Sector Format Sequencer to an external event. The status of this pin is available as a sequencer branch condition. The microprocessor can also sample this bit by reading Register 7EH, Bit 4.
OUTPUT	10	O	OUTPUT PIN: Controlled by Bit 2 of the Control Field (A0H thru BBH) of the sequencer RAM.
INDEX	11	I	INDEX: Input for index pulse received from the drive. Must be a minimum of one byte time. The leading edge of the index pulse sets the INDEX PAST bit (Register 7AH, Bit 0).
SECTOR	12	I	SECTOR: Input for sector pulse received from hard-sectored drives. Must be a minimum of one byte time. The leading edge of the sector pulse sets the SECTOR PAST bit (Register 7AH, Bit 1).

(*) Denotes negative true signal.

SYMBOL	NUM.	TYPE	DESCRIPTION
RST*	13	I	RESET: Asserting this pin sets Register 71H, Bit 5. This stops all operations within the chip and deasserts RG,WG,WAM and NRZ outputs. All internal registers are reset. All special outputs are set to high impedance state.
SYSCLK	14	I	SYSTEM CLOCK: A 1.5 to 16 MHz clock input which is used to derive CLKA* when not reading or writing disk data.
RG	15	O	READ GATE: This pin is asserted when the CL–SH130 is reading NRZ data-in coming from the disk.
WG	16	O	WRITE GATE: This pin is asserted when the CL–SH130 is writing NRZ data-out to the disk.
D0-D7	18-21 25-28	I/O	DATA BUS: Byte parallel data lines to/from the Buffer Memory and/or parallel host interface, i.e. SCSI.
GND	22	I	GROUND: The electrical ground connection.
RD/REF	30	I	READ / REFERENCE CLOCK: A multiplexed input sourced from the VFO oscillator during read gate, otherwise from the write oscillator. This is the primary clock for the chip and must be present at all times, including during the reset operation.
NRZ	31	I/O	NRZ: Read data input from the disk when RG is active; write data to the disk when WG is active.
WAM*/ AMD*	32	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT: A one-bit-wide pulse is output when WG is active and an address mark is to be written. When RG is active, a low level input to indicate address mark detect.
CS	33	I	CHIP SELECT: This pin must be asserted to access the CL–SH130.
WR*	34	I	WRITE: WR* and CS active causes the data on the AD lines to be written into the specified register.
RD*	35	I	READ: RD* and CS active causes the data from the specified register to be read on to the AD lines.
AD0-AD7	36-43	I/O	MULTIPLEXED ADDRESS/DATA: These are 3-state Address/Data lines which interface with a multiplexed microprocessor Address/Data bus.

(*) Denotes negative true signal.

NOTE: The above pin assignment is for the 44-pin PLCC package. The following pins are not connected: 17,23,24, 29 and 44.

2. REGISTER TABLES

2.1 Internal Registers

REGISTER(S)	ACCESS	DESCRIPTION/FUNCTION
4DH	R	SHADOW LATCH: Data register for Register 70H read access.
71H	R/W	ECC CONTROL: Register to specify the size of the ECC polynomial and its associated controls. Also Bit 5, is available to clear hardware resets or generate software resets.
72H-73H	R	ECC STATUS: Status of ECC Bits 0 through 31.
74H-77H	R/W	ECC POLYNOMIAL: ECC Polynomial programmed feedback registers.
78H	R/W	BRANCH ADDRESS: Next executable address for the sequencer.
79H	R	SEQUENCER STATUS
79H	W	SEQUENCER START ADDRESS
7AH	R/W	OPERATION CONTROL / STATUS
7BH	R/W	WAM CONTROL: WAM output timing control register.
7CH	R/W	SYNC PATTERN: This register to be compared with NRZ read data when Address Mark Detect is active. Number of bits to be compared is controlled by Register 7FH.
7DH	R/W	GP I/O CONTROL: Controls operation of GP I/O pins.
7EH	R/W	GP I/O: Register whose directions are controlled by Register 7DH.
7FH	R	TOP-OF-STACK: When reading this register, content of the Top of Stack is presented to the bus and the stack is popped.
7FH	W	CLOCK CONTROL: Specifies number of bits to be compared for SYNC and controls CLKA* operation.

2.2 External Registers

REGISTER(S)	ACCESS	DESCRIPTION/FUNCTION
50H	R/W	HOST BUS ACCESS: Register 50H decode allows microprocessor access to host data bus. A read of this register causes BIE* (CL–SH120) to be asserted. A write causes LO and BOE* (CL–SH120) to be asserted. Also, access to this register will internally bridge buffer memory data bus to microprocessor data bus.
51H	R/W	HOST BUS ACCESS: Same as 50H for 16-bit data bus.
70H	R/W	BUFFER MEMORY ACCESS: 70H decode internally bridges the buffer memory data bus and microprocessor bus (allowing the microprocessor to access buffer memory) and causes the CL–SH120 to assert buffer memory address, MOE*, and WE*. Read data from the buffer memory will also be locked into Register 4DH.
6EH & 6FH	R/W	GP I/O CONTROL: Reads and Writes to these generate pulses on the GP I/O Pins, which can be used to enable buffers and clock latches to accommodate different drive interfaces. See Register 7EH.

2.3 Writable Control Store (WCS)

REGISTER(S)	ACCESS	FUNCTION/DESCRIPTION
80H-9EH	R/W	NEXT ADDRESS FIELD: The sequencer goes to this address after the down counter has reached zero and a branch has not been taken.
A0H-BEH	R/W	CONTROL FIELD: Control Field of the control store word.
C0H-DEH	R/W	COUNT FIELD: Sets initial value of sequencer counter when a new state is entered.
E0H-FEH	R/W	DATA FIELD: Source for all overhead bytes of data used by the disk during write operations. During read operations, it is one of the operands to the comparison logic.

2.4 Sequencer Registers

REGISTER(S)	ACCESS	FUNCTION/DESCRIPTION
49H-4CH	R/W	CURRENT SEQUENCER WORD: The WCS word being executed is stored in these registers. **The microprocessor must not access these registers during sequencer operation.**

3. FUNCTIONAL DESCRIPTION

The CL–SH130 is designed to be used with a low cost microprocessor, which allows it to maintain a "loose" synchronization with the real time disk operation. The CL–SH130, itself, maintains "close" synchronization with the data to and from the drive and provides the signals necessary to control this path. In addition, it handles data synchronously to and from the buffer memory and provides some of the required signals to operate with the SCSI bus. Using the CL–SH130 means a lower total part count for the intelligent disk drive design while maintaining the same or greater performance than that of a bit slice processor design.

The CL-SH130 is divided into six major functional blocks:

- Microprocessor Interface
- Sector Format Sequencer
- Data Flow Control
- Buffer Memory Interface
- Stack
- General Purpose I/O

3.1 Microprocessor Interface

The microprocessor interface is based on an eight-bit multiplexed address and data bus found on popular Intel processors such as the 8085 and 8051. The CL–SH130 decodes addresses 48H-51H and 70H-FFH. To prevent erroneous operations, the controller board design must reserve the decoding of these addresses for the CL–SH130.

3.2 Sector Format Sequencer

Under microprocessor control, the CL–SH130 can be made to sequence through different types of operations. The user can control the timing relationships between various output signals and can monitor the different input lines to branch to different sequencer locations. The operation of the sequencer revolves around the SEQUENCER START/STATUS REGISTER (79H) and the BRANCH ADDRESS REGISTER (78H). Register 79H is first loaded with the starting address where the sequencer is to begin execution.

The basic operations of the controller chip are programmed by the contents of the Writable Control Store (WCS). The WCS consists of 112 bytes, organized as 31 words, each four bytes wide. The four bytes can be broken down into DATA, COUNT, NEXT ADDRESS and CONTROL FIELDS. The DATA FIELD contains data which may be used to initialize the track layout, including gap, ID field, and sector data fill characters. It can also be compared to the NRZ data-in to identify various fields in a sector. The CL–SH130 has other registers that can be used to control the composition of the track format such as sync characters, and the ECC polynomial. The COUNT FIELD specifies the initial value of the sequencer counter for the current word. The sequencer counter is decremented once every eight READ/-REFERENCE CLOCK (RD/REF) cycles. When the count reaches zero, the sequencer will go into the next state. The next address will be based on the contents of the NEXT ADDRESS FIELD of the current sequencer word, unless a branch condition has been programmed and met. If a branch condition has been programmed and met, then the next address to be executed is based on the contents of the BRANCH ADDRESS REGISTER (78H). Thus, by setting up different branch conditions which are based on external or internal events, the chip can be made to sequence through different operations. The CONTROL FIELD is used to generate and initiate all synchronous NRZ data handling operations.

3.3 Data Flow Control

The data flow portion of the CL–SH130 consists of an ECC generator and a serializer/deserializer. Data to be written to the disk enters the CL–SH130 in a byte-wide format. It is serialized and runs through an ECC generator. The NRZ serial bit stream also includes sequencer-generated fields (such as Address Marks, Gaps and Sector ID) and ECC-generated output along with the serialized data. Data read from the disk enters the CL–SH130 as a NRZ serial bit stream. The input data stream is run through the ECC generator and deserialized into a byte-wide format.

The ECC polynomial is fully user-programmable for optimum error coverage according to the media and encoding scheme being used. The internal ECC length can be programmed from 16 to 32 bits, or it can be fully suppressed when using external ECC circuitry.

3.4 Buffer Memory Interface

Byte-wide data transferred by the CL–SH130 is passed to and from the buffer memory on the BUFFER DATA Bus. One buffer memory cycle must be initiated for each byte transferred by the serializer/deserializer. The CLKA* output signal defines the buffer memory access cycles and the CLKB* output signal reserves the next CLKA* cycle for the CL–SH130 data. There must be a minimum of two memory cycles per byte-serialization time (eight READ/REFERENCE CLOCK [RD/REF] cycles), to maintain simultaneous transfer between the disk and buffer memory, and between the host and buffer memory. Four memory cycles per byte-serialization time allow more host accesses for each disk access of the buffer memory. The CL–SH120 Buffer Storage Manager chip is designed to take advantage of this burst speed for high SCSI throughput. The number of buffer memory access cycles (CLKA* cycles) per byte-serialization time is programmed in Register 7FH, bit 4. If this bit is set, there will be two CLKA* cycles per byte-serialization time. This is the Two Window Mode. If this bit is reset, then there will be four CLKA* cycles per byte-serialization time. This is the Four Window Mode. If the CL–SH130 is not performing a data transfer operation, then the source of the CLKA* output signal is the SYSTEM CLOCK (SYSCLK) input, which is divided per Register 7FH, bits 6,7.

3.5 Stack

The CL–SH130 also has a stack that is eight bytes deep. By enabling the stack during the Read Operation, information read from the drive can be pushed on to the stack to be examined later at a lower speed by the microprocessor (Register 7FH). The stack may be used to store header information for sector identification or defect management.

3.6 General Purpose I/O

The CL–SH130 provides four general purpose I/O lines which can be programmed individually as input, output, or external register decode signals. With these lines, several drive/host interfaces such as SMD, ST506, ESDI, SCSI, etc. can be easily implemented. The general purpose I/O lines can also be used to provide strobe signals to read or write external registers and buffers at addresses 6EH and 6FH and thus simplify the external logic needed for accessing these registers. The GP I/O block also allows flexibility in the programming of the SCSI communication scheme.

4. FUNCTIONAL OPERATION

The CL–SH130 performs two basic operations, reading NRZ DATA in and writing NRZ DATA out. These two operations can be combined easily into the following four major functions:

- Read ID or Sector Identification
- Read ID and Write Data or Sector Write
- Read ID and Read Data or Sector Read
- Write ID and Write Data or Format Sector

These can be further modified to perform the Search Data and Verify Data functions.

Read Operation

One of the fundamental requirements of the Read Operation is to synchronize the incoming data on byte boundaries and then either respond to the data or pass the data through to the buffer memory. The CL–SH130 uses a bit-ring to maintain this synchronization at byte boundaries and to synchronize its internal activities. The bit-ring is an eight-bit shift register. The bit of the bit-ring which is set specifies where the MSB of the current byte is in the serializer/deserializer. When bit 7 of the bit-ring is set (denoted as bit-ring 7), then a complete byte is in the serializer/deserializer.

Data synchronization and bit ring initialization occurs when a specific data stream is detected and the ADDRESS MARK DETECT (WAM*/AMD*) input is active. The process begins when the CONTROL FIELD of the current sequencer word activates READ GATE (RG). The serial data passes through a programmable synchronization comparator until a match is found with the contents of the AMD Control (Register 7CH) along with a simultaneous active low signal on the WAM*/-AMD* pin. The number of bits that are used in the synchronization comparison is specified by the contents of the CLOCK CONTROL (Register 7FH), bits 0-2.

Typically, for MFM-encoded data, the first byte after the synchronization byte is used to differentiate between Sector ID and Data Fields. After synchronization, the sequencer has the ability to enable the comparison of the incoming data against the DATA FIELD of the WCS and also to capture the incoming data on the stack. The comparison and branch capability of the sequencer allows the incoming data to be recognized and acted upon. The programmable compare capability can be used to automatically access the correct sector by recognizing the proper Sector ID. If the Sector ID does not match the DATA FIELD of the current sequencer word then the sequencer can be programmed to stop, and can be restarted by the microprocessor to find the sector again. Note that a delay will often be implemented before the microprocessor restarts this operation. This is done to minimize the danger of false synchronization, particularly during Write splices.

If an ECC error is detected after the Read Operation, the syndrome is saved in the ECC registers and will not be reset until a new Read Operation is started. The microprocessor can then use Registers 71H, 72H and 73H to determine if the error is correctable and can calculate the error pattern and displacement from the beginning of the sector. After this, the error can be corrected in the data in the buffer memory.

Write Operation

The other fundamental operation of the CL–SH130 is writing NRZ DATA and WRITE ADDRESS MARKs (WAM*/AMD*). This operation begins when the CONTROL FIELD in the current sequencer word activates WRITE GATE (WG). WG is typically switched on at a specific place in the track layout: during a write splice after the sector ID ECC (for a write sector data operation), or after INDEX (for a track format operation). Data from the current sequencer word's DATA FIELD or from the buffer memory data bus is passed through the serializer, then through the ECC circuitry, and then out the NRZ DATA pin.

4.1 Sector Identification

The Sector Identification function consists of reading the Sector ID Field to identify to the microprocessor the current sector address. This

function is typically performed with a comparison of the Sector ID Field Address Mark, a capture of the Sector ID Field in the stack, and finally an ECC verification of data integrity. Any of the incoming data bytes may be captured in the stack, by programming the stack enable bit in the current sequencer word. Also, any of the incoming data bytes may be compared against the DATA FIELD by programming both it and the COMPARE ENABLE BIT in the CONTROL FIELD of the current sequencer word.

After the Sector Identification function is complete, the microprocessor can then read the SEQUENCER STATUS (Register 79H) and ECC STATUS (Registers 72H-73H). If there was no ECC error, the microprocessor may then read the stack to identify the current sector address. Otherwise, it may repeat the function or may attempt to correct the ECC errors found in the Sector ID Field just read.

4.2 Sector Read

Sector Read function typically consist of two parts. The first is reading and identifying the desired Sector ID Field. This is described in the Sector Identification function above, however, the desired sector address will also be included in the comparison. A branch condition is often programmed at the end of the Sector Identification function such that if the compared bytes match and there was no ECC error, the sequencer will automatically branch to the second half of the Sector Read function.

The second half of the Sector Read function, after the sector has been positively identified, is to transfer the Data Field portion of the sector to the buffer memory. Before transferring the data field, the source of CLKA* must be changed from SYS CLK to RD/REF CLK for proper synchronization of the data. This change is accomplished by setting SWITCH (COUNT FIELD, Bit 5). CLKA* source will continue to be synchronized to SYS CLK until SYNC PATTERN (Register 7CH) is detected. After the read, the microprocessor may then read the SEQUENCER STATUS (Register 79H) and ECC STATUS (Registers 72H-73H) to determine the completion status of the Sector Read. If the read was successful, then the microprocessor will typically instruct the Buffer Manager chip (CL–SH120) to free this sector in buffer memory for transfer to the host. If the read was not successful, the microprocessor may try to correct the data or attempt to re-read this sector.

4.3 Sector Write

Sector Write functions also typically consist of two parts. The first is identical with the first part of the Sector Read, namely reading the Sector ID Field. The same sequencer routine should be used. The only difference is that after a successful Sector ID read, the BRANCH REGISTER (78H), should be set to the address of the write sector routine.

The second half of the Sector Write function, after the sector has been positively identified, is to transfer the data from the buffer memory to the disk as explained in the Write Operation described above. Before transferring the data field, the source of CLKA* must be changed from SYS CLK to RD/REF CLK for proper synchronization of the data. This change is accomplished by setting SWITCH (COUNT FIELD, Bit 5). For the Sector Write function this change occurs immediately upon setting this bit.

4.4 Format Sector

This function consists of a Write Operation that will write both the Sector ID Field and the Sector Data Field. This function is normally started with the sequencer waiting for the INDEX pulse to branch into the Write Operation routine. The microprocessor can update the Sector ID Field information in the WCS while the Sector Data Field is being written on the disk. This allows a full track format with a minimum of microprocessor intervention.

The CL–SH130 allows the Sector Data Field to be generated from the WCS, instead of buffer memory, through the use of SUPPRESS TRANSFER (Register 7AH, Bit 5).

4.5 Search Data

The Sector Read function can be modified into a Search Data function. When the second half of the Sector Read function is entered, the contents of the buffer memory will be compared, byte-for-byte, with the incoming data from the drive. This comparison of the DATA FIELD is enabled by setting the SEARCH OPERATION bit of the OPERATION CONTROL REGISTER, (7AH, Bit 4) and the COMPARE ENABLE bit (Bit 1) in the CONTROL FIELD of the WCS which starts the data transfer.

The result of this comparison is latched into the STATUS REGISTER (79H, Bits 0 and 1). Be sure to reset both the SEARCH OPERATION (Register 7AH, Bit 4) and COMPARE ENABLE (CONTROL FIELD, Bit 1) bits after the completion of the Search Data function.

4.6 Verify Sector

By setting the SUPPRESS TRANSFER bit in the OPERATION CONTROL REGISTER, (7AH, Bit 4) and performing a Read Sector function, the incoming data will be verified for good ECC, but will not be transferred to the buffer memory.

4.7 Extended Data Handling

Variable Sector Size

The CL–SH130 has an eight-bit Sector Data Field length counter loadable from the COUNT FIELD of the WCS. The COUNT FIELD is programmable, and by setting it to any value from 00H to FFH, any sector length up to 256 bytes can be transferred. The value of the COUNT FIELD should be one less than the actual sector length. For sector sizes greater than 256 bytes two different methods can be used.

The first approach uses the INHIBIT CARRY bit in the OPERATION CONTROL REGISTER (7AH, Bit 7). By setting this bit before data transfer begins or before the first count has expired during the data transfer, the CL–SH130 will be inhibited from going on to the next sequencer word, the INHIBIT CARRY bit will be reset, and another 256 bytes of data will be transferred. Additional counts of 256 byte segments may be transferred by setting this bit after each automatic reset.

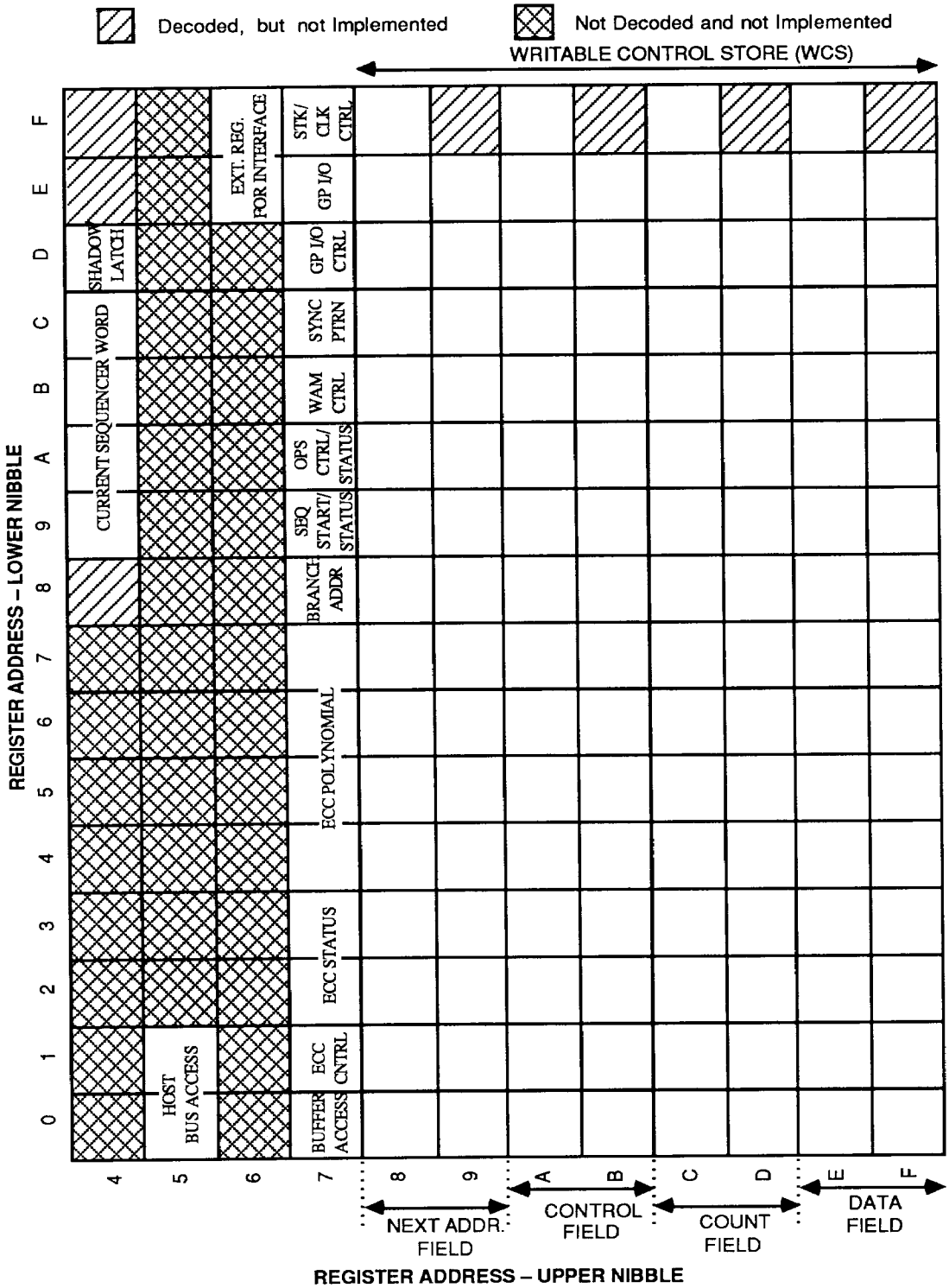
The second approach uses as many WCS words as required to implement the count for the data field.

Multi-Sector Read or Write

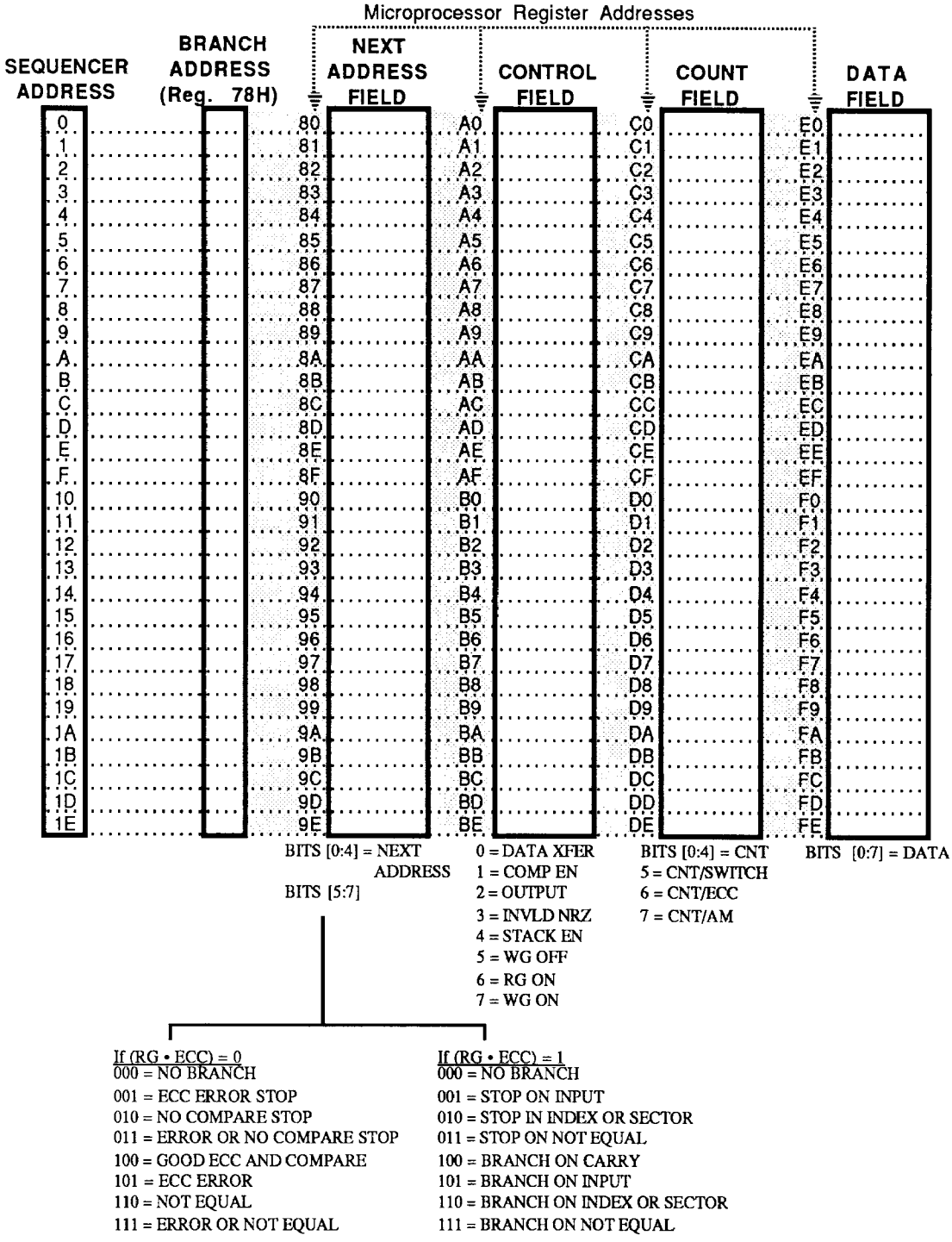
Multi-Sector Reads or Writes are accomplished by loading the next sector ID to be found while DATA TRANSFER Bit (Register 79H, Bit 6) is active for the present sector, then restarting the read or write immediately after evaluating the completion status of the present sector.

5. REGISTER ADDRESSES

5.1 Memory Map



5.2 WCS Worksheet



6. INTERNAL REGISTER DESCRIPTION

6.1 4DH – Shadow Latch (Read Only)

Bit 0-7	DATA: When the microprocessor reads Register 70H, the contents of the Buffer Memory data bus (D[0:7]) will be captured in this register for future reference.

6.2 71H – ECC Control (Read/Write)

Bit 0	SERIAL ECC INPUT: ECC Bit 0 will be loaded with the content of this bit when the ECC SHIFT CONTROL bit is set. Note that for proper operation the RD/REF pin must be cycling; the RG and WG must be deasserted.
Bit 1	ECC SHIFT CONTROL: Each time this bit is set, a single shift pulse will be sent to the 32-bit ECC register. This bit is automatically cleared after the shift pulse occurs.
Bit 2	DISABLE ECC FEEDBACK: Setting this bit will cause the ECC Polynomial to function as a 32-bit shift register.
Bit 3	CLEAR ECC: ECC syndrome will be cleared when this bit is set and no read or write operation is in progress. If this bit is set during a read or write operation, the ECC syndrome will be cleared at the end of that operation.
Bit 4	ENABLE SECTOR BRANCH: When set, will cause the SECTOR input to be ORed with the INDEX so that operation may begin at INDEX or SECTOR.
Bit 5	CHIP RESET: Assertion of the RST* pin will set this bit and generate a hardware reset condition. When the microprocessor sets this bit, a software reset condition is generated. Either reset condition will stop all operations within the chip, and deassert all output-only pins. In addition, a hardware reset condition will reset all internal registers. The software reset condition will reset all registers except 74H-77H and 7DH-7FH and will change NRZ, WAM*/AMD*, D0-D7, and AD0-AD7 to a high impedance state. In either case, the chip will remain in the reset condition as long as this bit is set, and the reset condition will be removed only when the microprocessor clears this bit.
Bits 6-7	POLYNOMIAL LENGTH: Controls the length of the ECC polynomial. 00 = 16-bit polynomial (16-31) enabled. 01 = 24-bit polynomial (8-31) enabled. 10 = Undefined. 11 = 32-bit polynomial (0-31) enabled.

6.3 72H – ECC Status [0:23] (Read Only)

Bit 0	An OR of ECC Bits 0-16. This OR is gated by the appropriate polynomial length selected in Register 71H, Bits 6-7.
Bit 1	ECC Bit 17
Bit 2	ECC Bit 18
Bit 3	ECC Bit 19
Bit 4	ECC Bit 20
Bit 5	ECC Bit 21
Bit 6	ECC Bit 22
Bit 7	ECC Bit 23

6.4 73H – ECC Status [24:31] (Read Only)

Bit 0	ECC Bit 24
Bit 1	ECC Bit 25
Bit 2	ECC Bit 26
Bit 3	ECC Bit 27
Bit 4	ECC Bit 28
Bit 5	ECC Bit 29
Bit 6	ECC Bit 30
Bit 7	ECC Bit 31

6.5 74H – ECC Polynomial [1:8] (Read/Write)

Bit 0	Sets feedback path to the input of ECC Bit 1. ECC Bit 31 will be XORed with serial data in and ECC Bit 0. It also becomes the input to ECC Bit 1.
Bit 1	Sets feedback path to the input of ECC Bit 2.
Bit 2	Sets feedback path to the input of ECC Bit 3.
Bit 3	Sets feedback path to the input of ECC Bit 4.
Bit 4	Sets feedback path to the input of ECC Bit 5.
Bit 5	Sets feedback path to the input of ECC Bit 6.
Bit 6	Sets feedback path to the input of ECC Bit 7.
Bit 7	Sets feedback path to the input of ECC Bit 8.

NOTE: This register is not reset by a software reset condition.

6.6 75H – ECC Polynomial [9:16] (Read/Write)

Bit 0	Sets feedback path to the input of ECC Bit 9. ECC Bit 31 will be XORed with serial data in and ECC Bit 8. It also becomes the input to ECC Bit 9.
Bit 1	Sets feedback path to the input of ECC Bit 10.
Bit 2	Sets feedback path to the input of ECC Bit 11.
Bit 3	Sets feedback path to the input of ECC Bit 12.
Bit 4	Sets feedback path to the input of ECC Bit 13.
Bit 5	Sets feedback path to the input of ECC Bit 14.
Bit 6	Sets feedback path to the input of ECC Bit 15.
Bit 7	Sets feedback path to the input of ECC Bit 16.

NOTE: This register is not reset by a software reset condition.

6.7 76H – ECC Polynomial [17:24] (Read/Write)

Bit 0	Sets feedback path to the input of ECC Bit 17. ECC Bit 31 will be XORed with serial data in and ECC Bit 16. It also becomes the input to ECC Bit 17.
Bit 1	Sets feedback path to the input of ECC Bit 18.
Bit 2	Sets feedback path to the input of ECC Bit 19.
Bit 3	Sets feedback path to the input of ECC Bit 20.
Bit 4	Sets feedback path to the input of ECC Bit 21.
Bit 5	Sets feedback path to the input of ECC Bit 22.
Bit 6	Sets feedback path to the input of ECC Bit 23.
Bit 7	Sets feedback path to the input of ECC Bit 24.

NOTE: This register is not reset by a software reset condition.

6.8 77H – ECC Polynomial [25:31] (Read/Write)

Bit 0	Sets feedback path to the input of ECC Bit 25. ECC Bit 31 will be XORed with serial data in and ECC Bit 24. It also becomes the input to ECC Bit 25.
Bit 1	Sets feedback path to the input of ECC Bit 26.
Bit 2	Sets feedback path to the input of ECC Bit 27.
Bit 3	Sets feedback path to the input of ECC Bit 28.
Bit 4	Sets feedback path to the input of ECC Bit 29.
Bit 5	Sets feedback path to the input of ECC Bit 30.
Bit 6	Sets feedback path to the input of ECC Bit 31.
Bit 7	NOT USED: Status indeterminate.

NOTE: This register is not reset by a software reset condition.

6.9 78H – Branch Address (Read/Write)

Bits 0-4	BRANCH ADDRESS: Writing Bits 0-4 will preload a sequencer branch address to be used when a branch condition is met. A read of this register will gate Bits 0-4 of the WCS NEXT ADDRESS FIELD on the microprocessor data bus (AD[0:7]).
Bits 5-7	Bits 5,6, and 7 are test points.

6.10 79H – Sequencer Status (Read Only)

Bit 0	COMPARE EQUAL: Is set when the result of the compare operation is equal. The comparison is done between the Read Data and either the Buffer Memory Data or the WCS DATA FIELD (as determined by the SEARCH OPERATION bit – Register 7AH, Bit 7), on all bytes where comparison was enabled in the COMPARE ENABLE bit (Bit 1) of the WCS CONTROL FIELD. COMPARE EQUAL is not valid until the sequencer is in the ECC FIELD.
Bit 1	COMPARE LOW: Same as Bit 0 above, but is set when the Read Data is lower.
Bit 2	ECC ERROR: Will be set if, after the last ECC DATA bit is read, any bit on ECC Status (Registers 72H, 73H) is set.
Bit 3	NOT USED: Status indeterminate.
Bit 4	STOPPED: Indicates the sequencer is at address 1FH. The ECC contents have not been reset. The RG and WG are reset. The bit ring is not affected.
Bit 5	BRANCH ACTIVE: Is set when a branch condition is met. Reading this register should reset this bit, but due to the asynchronous relationship between sequencer operations, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset.
Bit 6	DATA TRANSFER STATUS: Status of DATA TRANSFER bit (WCS CONTROL FIELD, Bit 0). Set during data transfer between buffer memory and disk.
Bit 7	AM ACTIVE: Is set when DATA TRANSFER bit (WCS CONTROL FIELD, Bit 0) is reset and AM/COUNT bit (WCS COUNT FIELD, Bit 7) is set. Is reset after reading or writing the ECC bytes. Is also reset when the sequencer stops.

6.11 79H – Sequencer Start Address (Write Only)

Bits 0-4	START ADDRESS: A write to this register will start the sequencer at the latched address. This register should only be used to start the sequencer while in the stopped condition (i.e. Register 79H, Bit 4 is active).
Bits 5-7	NOT USED: Status indeterminate.

NOTE: This register can be used to stop the sequencer by writing 1FH to this register.

6.12 7AH – Operation Control Status (Read/Write)

Bit 0	INDEX PAST: Is set by the leading edge of the index pulse from the disk. Reading the register should reset this bit, but due to the asynchronous relationship between the INDEX signal and the microprocessor, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset.
Bit 1	SECTOR PAST: Is set by the leading edge of the sector pulse from the disk. Reading the register should reset this bit, but due to the asynchronous relationship between the SECTOR signal and the microprocessor, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset.
Bit 2	NRZ DATA IN: Is set when a Zero To One transition is detected at the NRZ Data pin during READ GATE activity. Reading the register should reset this bit, but due to the asynchronous relationship between the NRZ signal and the microprocessor, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset.
Bit 3	NOT USED: Status indeterminate.
Bit 4	SEARCH OPERATION: Selects the source of the data for the Compare Operation. When set, Read Data is compared to Buffer Memory Data. When reset, Read Data is compared to WCS DATA FIELD.
Bit 5	SUPPRESS TRANSFER: Port A Transfer REQ (CLKB*) will not be generated when this bit is set. During Write Operation, the data field will be written with the contents of the WCS DATA FIELD. During Read Operation, the incoming data will be compared with contents of WCS DATA FIELD.
Bit 6	NOT USED: Status indeterminate.
Bit 7	INHIBIT CARRY: When set, the load of the next WCS COUNT FIELD for the data transfer will be inhibited. Used in variable sector size transfer. See Section 4.7, Variable Sector Size. Automatically reset whenever the count is over.

6.13 7BH – WAM Control (Read/Write)

Bits 0-7	WRITE ADDRESS MARK CONTROL: WAM*/AMD* pin is asserted during a Write Operation one bit cell time for each corresponding bit set in this register. Output at the WAM*/AMD* pin will be shifted two bit cell times toward MSB.

6.14 7CH Sync Pattern (Read/Write)

Bits 0-7	SYNC PATTERN: This register is compared with NRZ read data when Address Mark Detect (AMD* pin) input is active. Only bits enabled by SYNC COMPARE CONTROL (Register 7FH, Bits 0-2) will be used for comparison.

6.15 7DH – GP I/O Control (Read/Write)

Bits 0-3	GP I/O DIRECTION CONTROL: When set, the corresponding GP I/O pins are configured as outputs. When these bits are reset, the corresponding GP I/O pins are configured as inputs.
Bit 4	W6E CONTROL: This bit is valid only when GP I/O DIRECTION CONTROL Bit 0 is set. When W6E CONTROL is set, GP I/O (Register 7EH) Bit 0 will be disabled as an output, and an output pulse will be generated on the GP I/O 0 Pin when the microprocessor writes to Register 6EH. When W6E CONTROL is reset, GP I/O Bit 0 is enabled on the GP I/O 0 Pin, as defined in GP I/O DIRECTION CONTROL, Bit 0.
Bit 5	R6E CONTROL: This bit is valid only when GP I/O DIRECTION CONTROL Bit 1 is set. When R6E CONTROL is set, GP I/O (Register 7EH) Bit 1 will be disabled as an output, and an output pulse will be generated on the GP I/O 1 Pin when the microprocessor reads Register 6EH. When R6E CONTROL is reset, GP I/O Bit 1 is enabled on the GP I/O 1 Pin, as defined in GP I/O DIRECTION CONTROL, Bit 1.
Bit 6	W6F CONTROL: This bit is valid only when GP I/O DIRECTION CONTROL Bit 2 is set. When W6F CONTROL is set, GP I/O (Register 7EH) Bit 2 will be disabled as an output, and an output pulse will be generated on the GP I/O 2 Pin when the microprocessor writes to Register 6F. When W6F CONTROL is reset, GP I/O Bit 2 is enabled on the GP I/O 2 Pin, as defined in GP I/O DIRECTION CONTROL, Bit 2.
	NOTE: This register is not reset by a software reset condition.

6.15 7DH – GP I/O Control (Read/Write) (cont'd)

Bit 7	R6F CONTROL: This bit is valid only when GP I/O DIRECTION CONTROL Bit 3 is set. When R6F CONTROL is set, GP I/O (Register 7EH) Bit 3 will be disabled as an output, and an output pulse will be generated on the GP I/O 3 Pin when the microprocessor reads Register 6F. When W6E CONTROL is reset, GP I/O Bit 3 is enabled on the GP I/O 3 Pin, as defined in GP I/O DIRECTION CONTROL, Bit 3.

NOTE: This register is not reset by a software reset condition.

6.16 7EH – GP I/O (Read/Write)

Bits 0-3	GP I/O BITS 0-3: These bits are independently programmed for data on the four GP I/O pins and each bit has a flip-flop that holds the data for output purpose only. For the SCSI application these output flip-flops are programmed for the expected states of the MSG, C/D, I/O, and ATN lines during information transfer phase. A read of this register will gate the status of the GP I/O pins which are programmed as inputs in Register 7DH.
Bit 4	INPUT PIN STATUS: Indicates the status of INPUT PIN.
Bit 5	OUTPUT PIN STATUS: Indicates the status of OUTPUT PIN.
Bit 6-7	NOT USED: Status inderterminate.

NOTE: This register is not reset by a software reset condition.

6.17 7FH – Clock Control (Write Only)

Bits 0-2	SYNC COMPARE CONTROL: Specifies the number of bits to be used in the compare for the sync byte. 000 = Only Bit 7 is compared. 001 = Only Bits 7 and 6 are compared. 010 = Only Bits 7 – 5 are compared. 011 = Only Bits 7 – 4 are compared. 100 = Only Bits 7 – 3 are compared. 101 = Only Bits 7 –2 are compared. 110 = Only Bits 7 –1 are compared. 111 = All Bits are compared.
Bit 3	When set, CLKA* and CLKB* outputs are high impedance
Bit 4	Specifies CLKA* frequency during sequencer data transfer. 0 = 1/2 of RD/REF (Four Window Mode) 1 = 1/4 of RD/REF (Two Window Mode)
Bit 5	NOT USED: Status indeterminate.
Bits 6-7	Specify CLKA* frequency during non-sequencer data transfer. 00 = 1/4 of SYSCLK 01 = 1/2 of SYSCLK 10 = SYSCLK 11 = Not valid

NOTE: This register is not reset by a software reset condition.

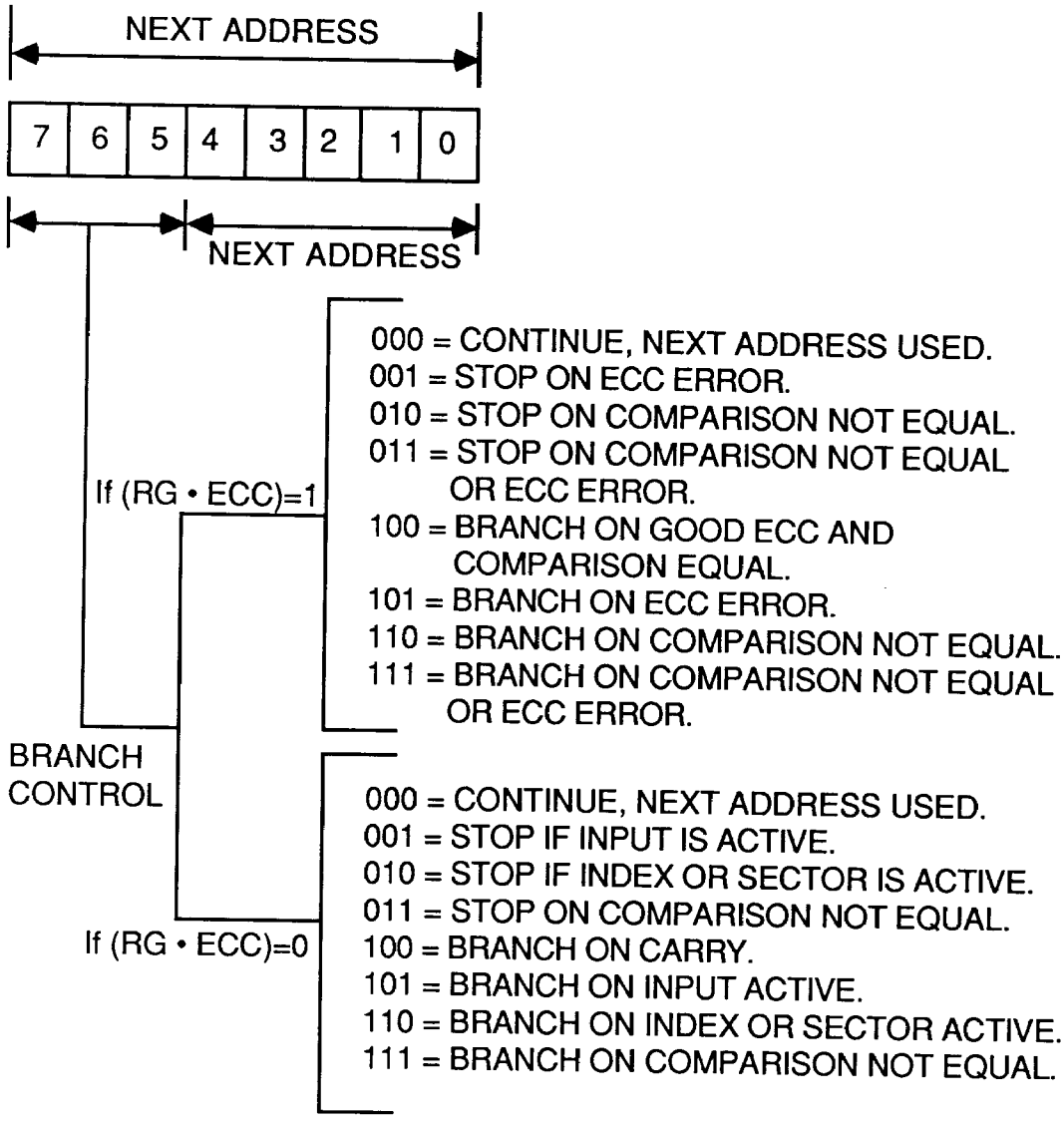
6.18 7FH – Top-Of-Stack (Read Only)

Bits 0-7	STACK: A read of this register will read the Top Of Stack and pop the stack.

7. WRITABLE CONTROL STORE (WCS) FIELD DESCRIPTION

The WCS (addresses 80H-9EH, A0H-BEH, C0H-DEH, and E0H-FEH) may only be accessed by the support microprocessor when there is no risk of the contents being accessed by the sequencer. This is normally true only during long data transfers or when the sequencer is stopped.

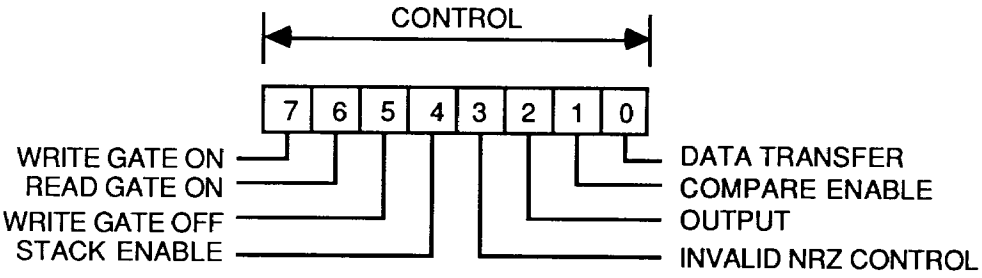
7.1 Next Address Field (80H - 9EH)



80H-9EH – Next Address Field – Read/Write

Bits 0-4	NEXT ADDRESS: This is the address the sequencer will go to after the down counter has reached zero and a branch has not been taken. There are 31 possible next-address locations (00H-1EH). Address 1FH establishes the stopped condition.
Bits 5-7	BRANCH CONDITION: These are the BRANCH CONDITIONS when both COUNT/ECC (COUNT FIELD, Bit 6) and READ GATE are active (If (RG • ECC)=1): 000 = Continue, next address used. 001 = Stop on ECC error. 010 = Stop on comparison not equal. 011 = Stop on comparison not equal or ECC error. 100 = Branch on good ECC and comparison equal. 101 = Branch on ECC error. 110 = Branch on comparison not equal. 111 = Branch on comparison not equal or ECC error. (These branches are taken at the completion of the ECC Field.) These are the BRANCH CONDITIONS at all other times (If (RG • ECC)=0): 000 = Continue, next address used. 001 = Stop if INPUT is active. 010 = Stop if INDEX or SECTOR is active. 011 = Stop on comparison not equal. 100 = Branch on carry. 101 = Branch on INPUT active. 110 = Branch on INDEX or SECTOR active. 111 = Branch on comparison not equal. (These branches are taken when the operations specified by the current sequencer word are completed.)

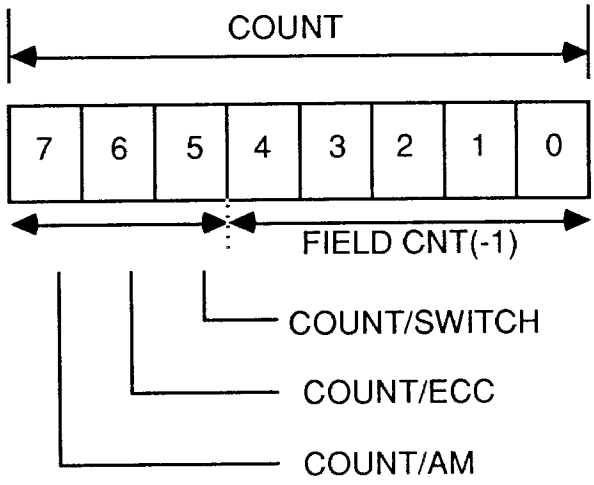
7.2 Control Field (A0H - BEH)



A0H-BEH – Control Field – Read/Write

Bit 0	DATA TRANSFER: When set, this bit will cause Port A REQ (CLKB*) to be generated synchronously with CLKA* and a byte of data will either be read or written onto the buffer memory data bus, depending on whether WG or RG is active.
Bit 1	COMPARE ENABLE: Setting this bit, along with RG, will allow a comparison between read data and the WCS DATA FIELD, or the buffer memory data (if SEARCH OPERATION bit is set - Register 7AH, Bit 4).
Bit 2	OUTPUT: This bit is connected to the OUTPUT pin and is used to synchronize external logic functions with the state of the WCS.
Bit 3	INVALID NRZ CONTROL: When this bit is set with RG, the NRZ DATA input will be ignored.
Bit 4	STACK ENABLE: When set, NRZ DATA read in is pushed on the eight-byte recirculating stack.
Bit 5	WRITE GATE OFF: When the last count of the WCS word with this bit set is executed, WG latch will be reset during bit ring 4. WG latch is also reset when the sequencer comes to the stopped state.
Bit 6	READ GATE ON: When the first count of the WCS word with this bit set is executed, RG latch will be set. The output of the RG latch is connected to the RG pin. The RG latch will be reset at the end of ECC or when the sequencer goes to the stopped state. The RG latch will not be set if WG latch is already set.
Bit 7	WRITE GATE ON: When the first count of the WCS word with this bit set is executed, WG latch will be set during bit ring 4. The output of the WG latch is connected to the WG pin. WG latch will not be set if RG latch is already set.

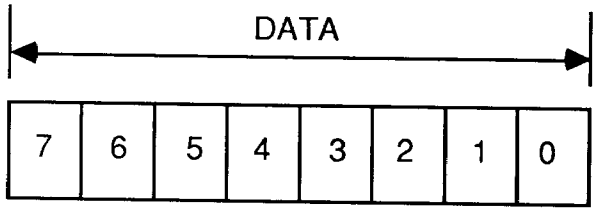
7.3 Count Field (COH - DEH)



C0H-DEH – Count Field – Read/Write

Bits 0-4	COUNT: These bits are the initial value of the sequencer counter when a new state is entered. The counter is decremented on bit ring 7. When it reaches zero, a new state will be accessed from the WCS.
Bit 5	COUNT/SWITCH: When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) of the WCS is set, this is bit 5 of the count. This bit is used to switch the source of CLKA* from the SYSTEM CLOCK to the READ/REFERENCE CLOCK. During Read operation the switch occurs when this bit is set and the data pattern specified in AMD CONTROL (Register 7CH) has been detected. During Write operation, the switch occurs on setting this bit.
Bit 6	COUNT/ECC: When the DATA TRANSFER bit (Control Field, Bit 0) of the WCS is set, this is bit 6 of the count. When the DATA TRANSFER bit of the WCS is reset, setting this bit will cause the sequencer to process the ECC bytes.
Bit 7	COUNT/AM: When the DATA TRANSFER bit (Control Field, Bit 0) of the WCS is set, this is bit 7 of the count. When the DATA TRANSFER bit of the WCS is reset, setting this bit sets AM ACTIVE (Register 79H, Bit7). If WRITE GATE is active, setting this bit also resets the ECC circuit and enables the WAM circuit.

7.4 Data Field (EOH - FEH)



EOH-FEH – Data Field – Read/Write

Bits 0-7	DATA: This register is the source for all overhead bytes of data used by the disk during write operations. During read operations, it is one of the operands to the comparison logic. When DATA TRANSFER (CONTROL FIELD, Bit 0) bit is set along with WRITE GATE, the source for write data will be the external Buffer Memory. When SUPPRESS TRANSFER (Register 7AH, Bit 5) is set along with Write Gate, the source for write data will be the content of this register.

8. SEQUENCER REGISTER DESCRIPTION

NOTE: Must only be accessed by the microprocessor when there is no risk of the contents being accessed by the sequencer.

8.1 49H – Current Sequencer Word [Next Address Field] (Read/Write)

Allows the microprocessor to access the NEXT ADDRESS FIELD of the current sequencer word.

8.2 4AH – Current Sequencer Word [Count Field] (Read/Write)

Allows the microprocessor to access the CONTROL FIELD of the current sequencer word.

8.3 4BH – Current Sequencer Word [Control Field] (Read/Write)

Allows the microprocessor to access the COUNT FIELD of the current sequencer word.

8.4 4CH – Current Sequencer Word [Data Field] (Read/Write)

Allows the microprocessor to access the DATA FIELD of the current sequencer word.

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... -65° C to 150° C
Voltage On Any Pin With Respect To Ground..... GND-0.5 to VCC+0.5 Volts
Power Dissipation ..... 0.500 Watt
Power Supply Voltage ..... 7 Volts
Injection Current (Latch-up) ..... 100 mA

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the disk. These are stress ratings only and functional operation of the disk at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect disk reliability.

9.2 D.C. Characteristics (VCC= 5V±5%, TA= 0° to 70° C, unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
VCC	Power Supply Voltage	4.75	5.25	V	Operating
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC+0.5	V	
VOL	Output Low Voltage		0.4	V	IOL=2mA
VOH	Output High Voltage	2.4		V	IOH=400uA
ICCS	Standby Supply Current		TBD	µA	All inputs at GND or VCC
ICC	Operating Supply Current		50	mA	@15Mbps, 5V nominal
IL	Input Leakage	-10	10	µA	0<VIN<VCC
CIN	Input Capacitance		10	pf	
COUT	Output Capacitance		10	pf	

NOTE: IOL=4mA for RG and WG

9.3 A.C. Characteristics

The following timings are operating under the assumption that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ±5% and an ambient temperature of 0C to70C.

Buffer Memory Read/WriteTiming Table

SYMBOL	PARAMETER	10 MHZ MIN	10 MHZ MAX	15 MHZ MIN	15 MHZ MAX	20 MHZ MIN	20 MHZ MAX	UNITS
T	CLKA* Period	200		125		100		ns
T/2	CLKA* Assert/Deassert	95		50		40		ns
Tba	CLKB*⬇ to CLKA*⬇	100		62.5		50		ns
Tab	CLKA*⬇ to CLKB*⬆	100		62.5		50		ns
Dov	CLKA*⬆ to Data Out valid	10	50	10	50	10	50	ns
Doh	CLKA*⬆ to Data Out invalid	0	50	0	50	0	50	ns
Dis	Data In Valid to CLKA*⬇	30		25		25		ns
Dih	CLKA*⬇ to Data In invalid	10		10		10		ns

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

Buffer Memory Read/WriteTiming:

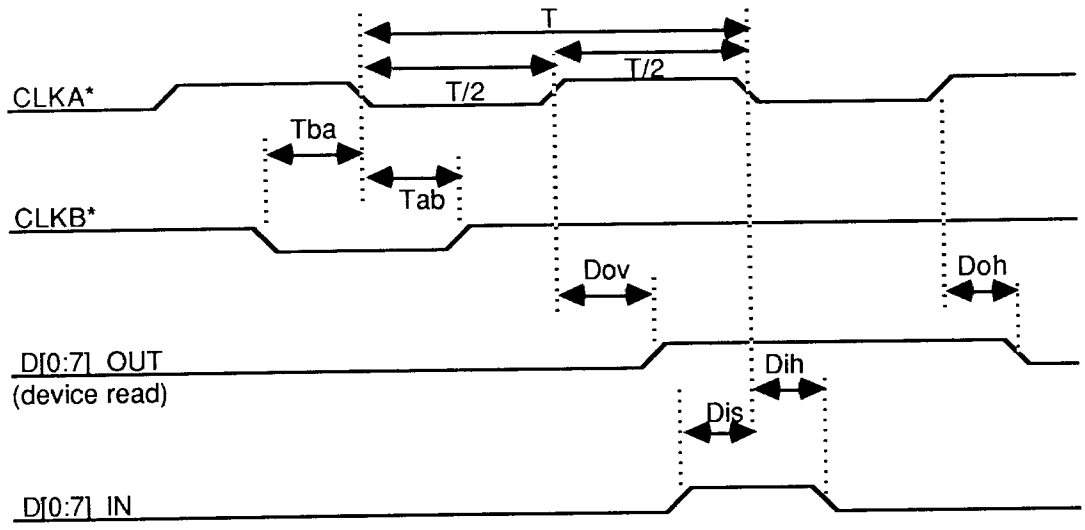


FIGURE 9.1

Microprocessor Interface Timing Table

SYMBOL	PARAMETER	10 MHZ MIN	10 MHZ MAX	15 MHZ MIN	15 MHZ MAX	20 MHZ MIN	20 MHZ MAX	UNITS
S	System Clock Period	60		60		50		ns
S/2	System Clock Assert/Deassert	23		23		18		ns
Sr = Sf	System Rise and Fall Time (@ S=60ns)		5		5		5	ns
Ta	ALE Width	45		45		45		ns
Taw	ALE⬇ to WRITE*⬇	25		25		25		ns
Tar	ALE⬇ to READ*⬇	25		25		25		ns
Tw	WRITE* Width	200		200		200		ns
Tr	READ* Width	200		200		200		ns
As	Address valid to ALE⬇	7.5		7.5		7.5		ns
Ah	ALE⬇ to Address invalid	20		20		20		ns
Cs	CHIP SELECT valid to ALE⬇	0		0		0		ns
Ch	READ*⬆ or WRITE*⬆ to CS⬇	0		0		0		ns
Wds	Write Data valid to WRITE*⬆	70		70		70		ns
Wdh	WRITE*⬆ to Write Data invalid	10		10		10		ns
Tda	READ*⬇ to Read Data valid		145		145		145	ns
Tdh	READ*⬆ to Read Data invalid		50		50		50	ns

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

System Clock Timing:

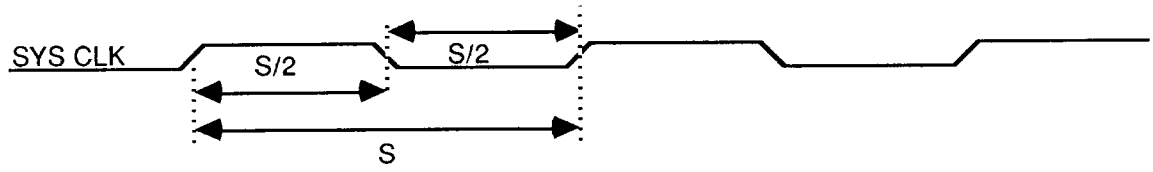


FIGURE 9.2

Microprocessor Read Timing:

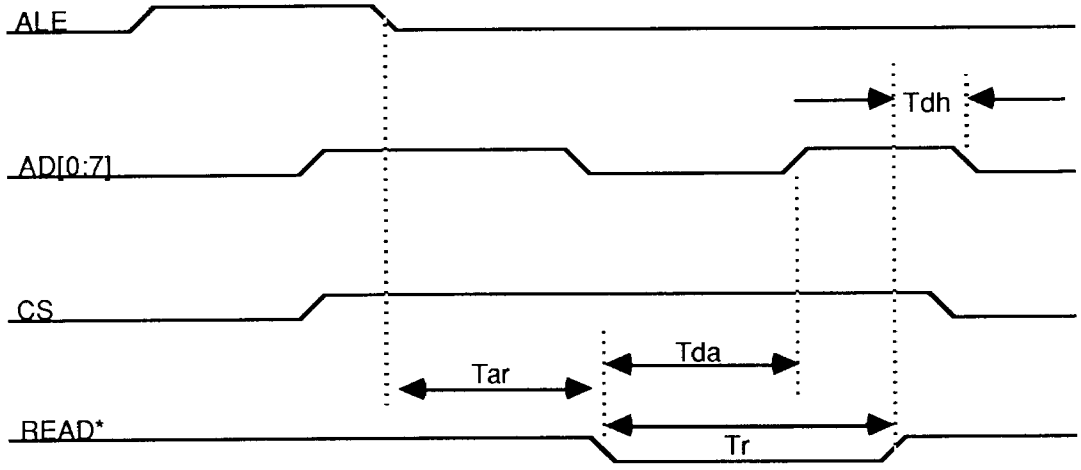


FIGURE 9.3

Microprocessor Write Timing:

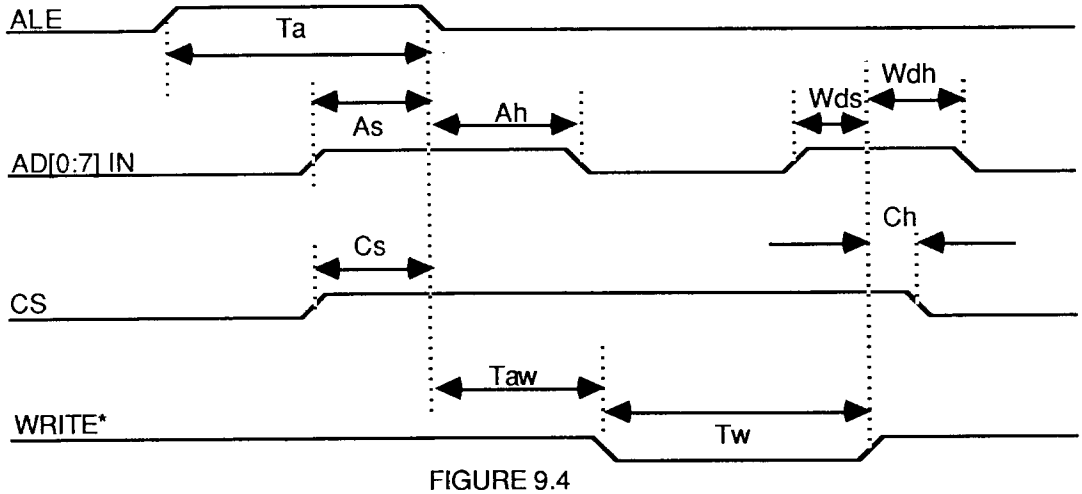


FIGURE 9.4

Disk Read/Write Timing Table

SYMBOL	PARAMETER	10 MHZ MIN	10 MHZ MAX	15 MHZ MIN	15 MHZ MAX	20 MHZ MIN	20 MHZ MAX	UNITS
T	RD/REF Period	100		62.5		50		ns
T/2	RD/REF Assert-Deassert	40		23		18		ns
Tr	RD/REF Rise Time (@ T=62.5ns)		10		5		5	ns
Tf	RD/REF Fall Time (@ T=62.5ns)		10		5		5	ns
Ds	Data In valid to RD/REF⬆	20		15		10		ns
Dh	RD/REF⬆ to Data In invalid	10		10		7		ns
As	AMD* valid to RD/REF⬆	20		15		10		ns
Dv	RD/REF⬆ to Data Out	10	40	10	40	10	40	ns
Wv	RD/REF⬆ to WAM* Out	10	40	10	40	10	40	ns

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

Disk Read Timing:

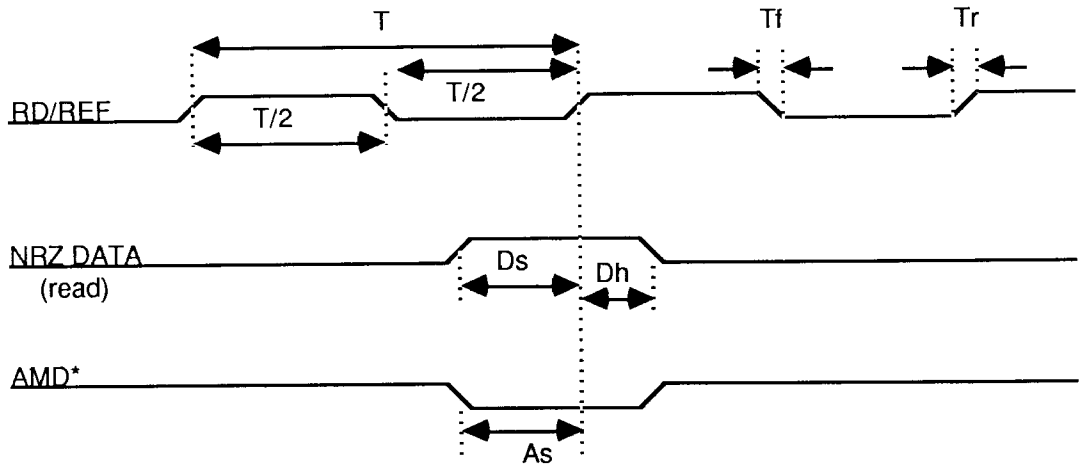
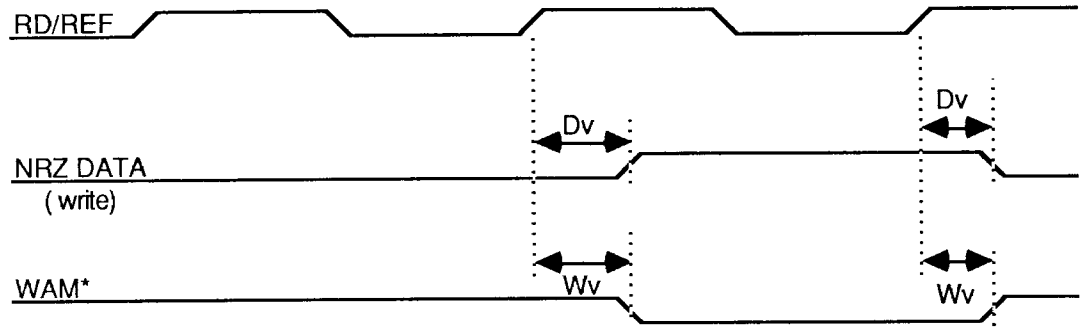


FIGURE 9.5

Disk Write Timing:



NOTE: Data is changed after rising edge

FIGURE 9.6

Register 50, 51, And 70 Timing Table

SYMBOL	PARAMETER	10 MHZ MIN	10 MHZ MAX	15 MHZ MIN	15 MHZ MAX	20 MHZ MIN	20 MHZ MAX	UNITS
Tda	D[0:7] In valid to AD[0:7] Out		55		55		55	ns
Tra†	RD*⬇ to Data Path Established		60		60		60	ns
Trh	RD*⬆ to ADDRESS/DATA invalid		50		50		50	ns
Tad	AD[0:7] In valid to D[0:7] Out		55		55		55	ns
Twd†	WR*⬇ to Data Path Established		60		60		60	ns
Twh	WR*⬆ to DATA OUT invalid	50		50		50		ns

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

† The Tra and Twd specifications refer to the delay in creating the D[0:7] to AD[0:7] path. The given specifications are for reference and assume the D[0:7] bus has been stable well before the falling edge of RD*. In the typical implementation (see Section 10 – Typical Application), when used with the CL–SH120, the delay from the falling edge of RD* to valid data on AD[0:7] is affected by the CL–SH120 response (and the Buffer Memory output data timing - for Register 70 reads). If D[0:7] is not valid within 5 ns after the falling edge of RD*, then Tda and Tad specifications should be used by the system designer to predict when valid data will be available.

Read Timing:

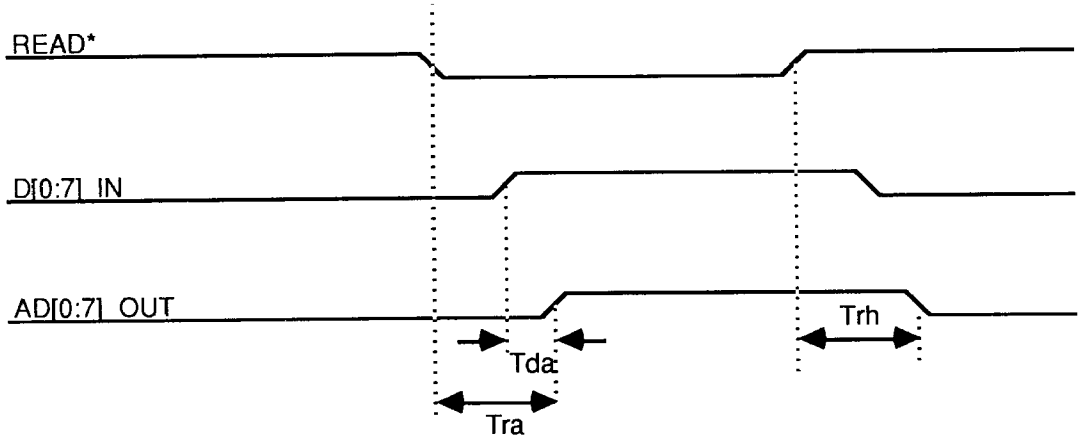


FIGURE 9.7

Write Timing:

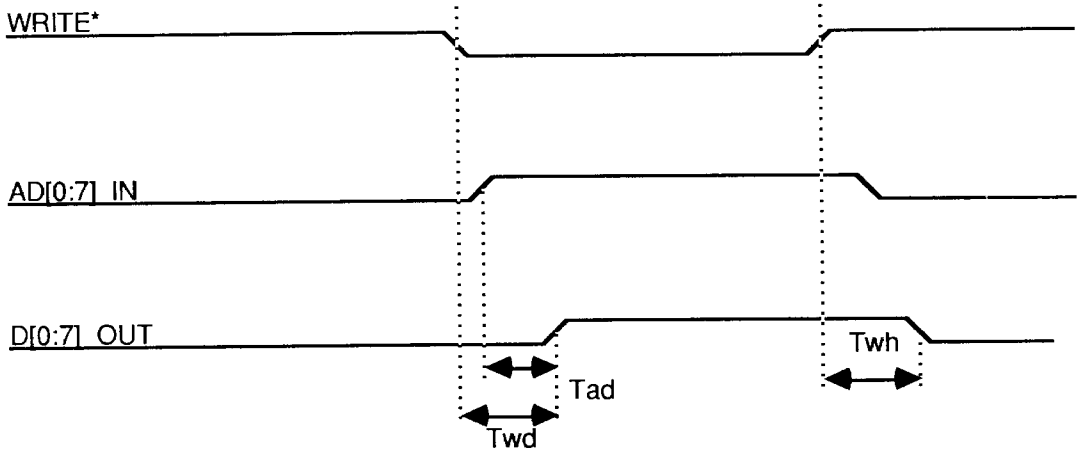


FIGURE 9.8

Address Decode 6E And 6F Read/Write Timing Table

SYMBOL	PARAMETER	10 MHZ MIN	10 MHZ MAX	15 MHZ MIN	15 MHZ MAX	20 MHZ MIN	20 MHZ MAX	UNITS
Tdf	RD* or WR* ⬇ to 6E or 6F ⬇		40		40		40	ns
Tdr	RD* or WR* ⬆ to 6E or 6F ⬆		40		40		40	ns

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

Read/Write Timing:

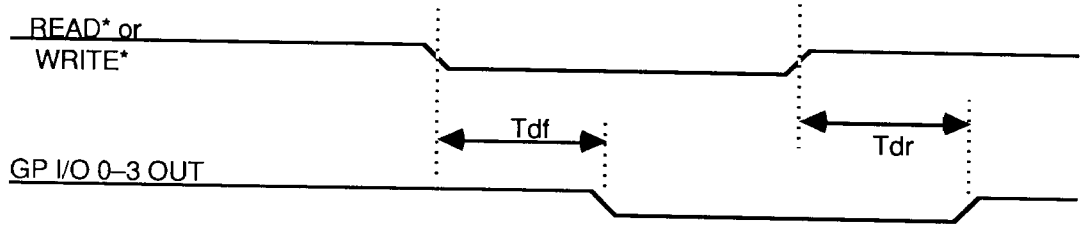
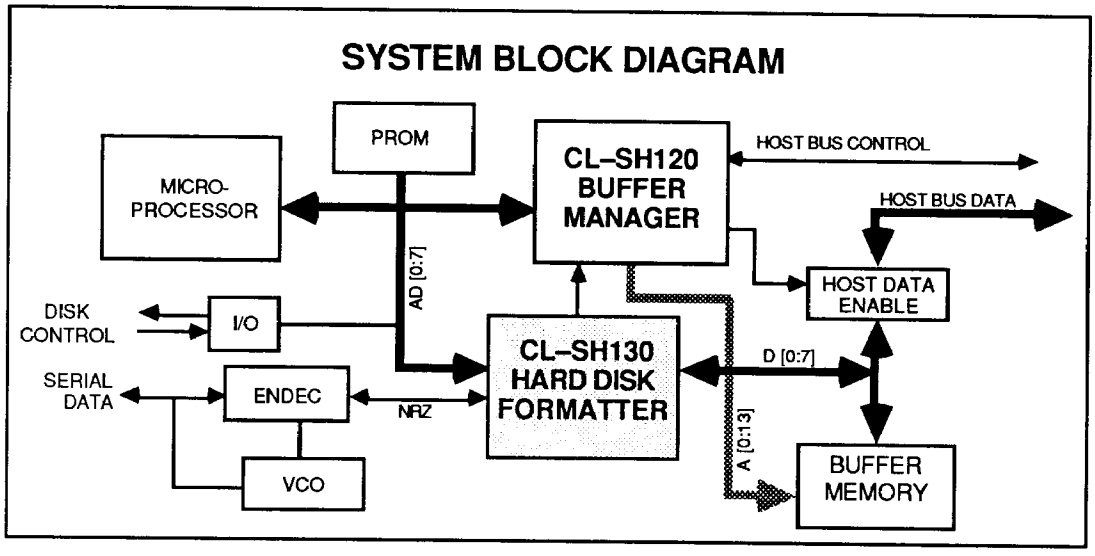


FIGURE 9.9

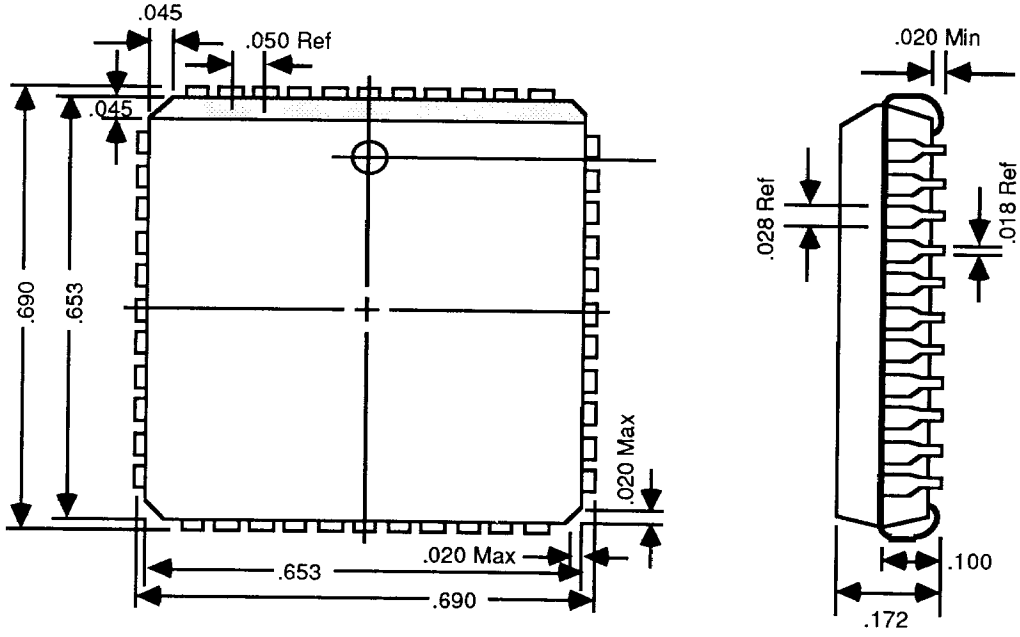
Notes:

10. TYPICAL APPLICATION



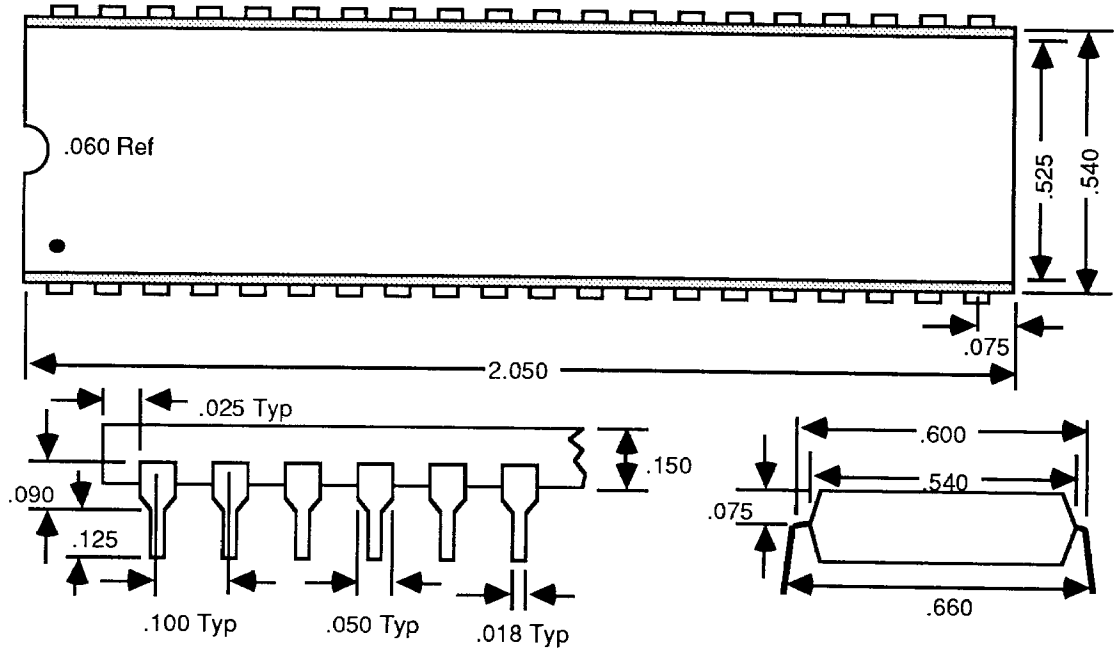
11. SAMPLE PACKAGES

11.1 44-Pin PLCC



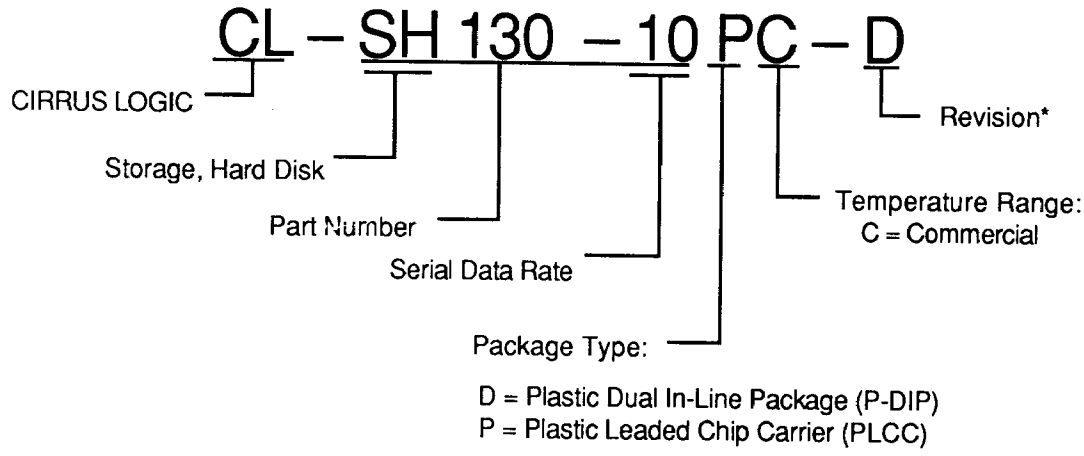
All dimensions are in inches and are nominal unless otherwise stated.

11.2 40-Pin P-DIP



12. ORDERING INFORMATION

CIRRUS LOGIC Numbering Guide



* Contact CIRRUS LOGIC for up-to-date information on Revisions.

Notes:

ABOUT CIRRUS LOGIC

CIRRUS LOGIC makes proprietary VLSI circuits in three product lines. The CD line is Data Communications circuits, the SH line is Hard Disk Controllers, and the GD line is Graphics Display Controllers.

A variety of redefinable products are offered in each line. These are not "standard products." Through the Redefinable IC CIRRUS LOGIC provides a unique solution that is custom-tailored to your system requirements. You are invited to start with our Data Sheet, and consider changes you would like to see in order to provide an optimal component for your system product. CIRRUS LOGIC will supply you the exact IC that your system requires.

It is more than a "standard product." You will receive a VLSI circuit that is specific to your application. But you are relieved of the burden of specifying and designing the IC. If you can critique a data sheet, you can have a custom VLSI component.

Our own internally developed proprietary silicon compilation technology* makes it possible for us to offer this level of VLSI product for the first time.

Look at our products. Redefine them to fit your system. We know of no other way to integrate so much sophisticated system-specific function onto an IC. It's the best of both the standard and custom worlds.

* U.S. Patent No. 4,293,783

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