CIRRUS LOGIC

CL-CD180

Data Sheet

FEATURES

Performance Enhancement Features:

- 8 full-duplex asynchronous channels
- Baud rates to 38.4K baud per transmitter and receiver
- On-chip scanner for handling channel interrupts
- 24-bytes of FIFO for each channel consisting of:
  - 8-byte transmit FIFO
  - 8-byte receive FIFO with programmable threshold
  - 8-byte status FIFO
- Improved interrupt schemes:
  - Vectored interrupts to allow direct jump into proper service routines
  - *Good data interrupts* to eliminate the need for status checks
  - *Fair share interrupts* to ensure equal service for all channels
  - External user-defined priorities
- User-programmable and automatic flow control modes
  - In-Band (software) via single or double character Xon, Xoff
  - Out-of-Band (hardware) via RTS/CTS, DTR/DSR
- Special character recognition and generation
- Line break detection and generation
- Cascadable to multiple CL-CD180s using Fair Share daisy chain scheme
- Insertion of transmit delays in data stream
- Baud rate selection via loading a divisor
- One timer per channel for receive data interrupt generation

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Intelligent Octal-Channel Asynchronous Communications Controller

OVERVIEW

The CL-CD180 is an intelligent asynchronous controller capable of supporting eight full duplex channels that transfer data simultaneously at 38.4 Kbps. The uniqueness of the CL-CD180 lies in its ability to move data efficiently from the channels to the host, resulting in a multi-fold improvement in system-level throughput. The CL-CD180's feature set is developed to specifically address the system-level performance bottlenecks in the areas of data throughput and real-time tasking.

To increase the overall data throughput of the system, special features such as on-chip scanner, on-chip data buffering and programmable receive FIFO thresholds are used to reduce the number of interrupts to the host; vectored interrupts, context switching technique and Good Data Transfer scheme are used to reduce the number of microprocessor cycles needed to fetch a byte of data.

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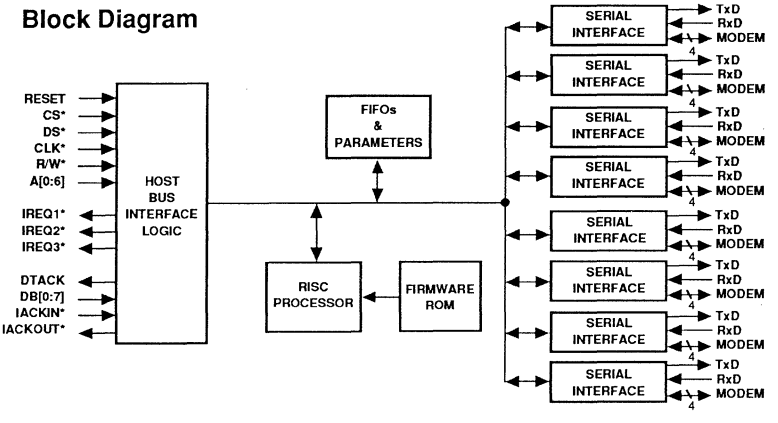
Functional Block Diagram



FEATURES (cont.)

Other Features:

- Ability to transmit and receive independently at different baud rates
- Local and remote maintenance loopback modes
- 4 modem control signals per channel - DTR/CD,DSR, RTS, CTS
- Selectable 68000 and 80x86 bus interfaces
- 5- to 8-bit character plus optional parity
- Odd, even, no parity or forced parity
- 1, 1 1/2, and 2 stop bits
- System clock of up to 10 MHz
- S/LA™ design technology
- Packaged in an 84-pin PLCC
- Advanced low-power CMOS process technology

Application Areas:

- Communications Processors
- Statistical/T1 Mux
- Terminal servers
- Data Concentrators
- Protocol converters/Pads
- Cluster controllers

OVERVIEW (cont.)

To support real-time tasking, the CL-CD180 performs time-critical functions, such as data flow control, in hardware. Automatic In-Band (Xon, Xoff) and Out-of-Band (RTS/CTS) flow control modes are supported. An automatic mode is implemented for the case of a remote unit flow controlling the CL-CD180 and a programmed-controlled mode is implemented for the case of CL-CD180 flow controlling the remote. This feature not only allows the data flow to be controlled in real time with minimum or no host intervention, it also prevents any loss of valuable data.

Other special features of the CL-CD180 reside in the fair share scheme that ensures equal service for all channel interrupts; special timers on each channel detect delays between received characters and detect and generate delays and breaks. A daisy chain scheme is used to allow easy implementation of multi-CL-CD180 systems.

The CL-CD180 is fabricated in a 2µ CMOS process and contains both the 68000- or 80x86-type microprocessor bus interfaces. Thus system designs with minimum configurations, maximum performance at lowest power can be achieved when using the CL-CD180.

ADVANTAGES

Unique Features	Benefits
On-chip scanner	Distributes interrupt services fairly among all channels.
On-chip FIFO and RxFIFO threshold	Reduces the number of interrupts to the host and allows the host to dynamically adjust the frequency of interrupts according to the system's interrupt service latency. This allows the host to better utilize its resources.
Good Data Interrupt™	Allows "bursting" of multiple good data bytes into the host without the need to check for status for each byte. This frees up needed host bandwidth to perform higher level system tasks.
Vectored interrupt	Allows direct jump into proper interrupt service routines without need to test for the cause of interrupt first. Saves host cycles.
Automatic flow control	Performs time-critical software tasks in hardware; performs tasks in real time and prevents loss of valuable data.
Advanced CMOS process	Provides high performance with low power consumption.

CIRRUS LOGIC

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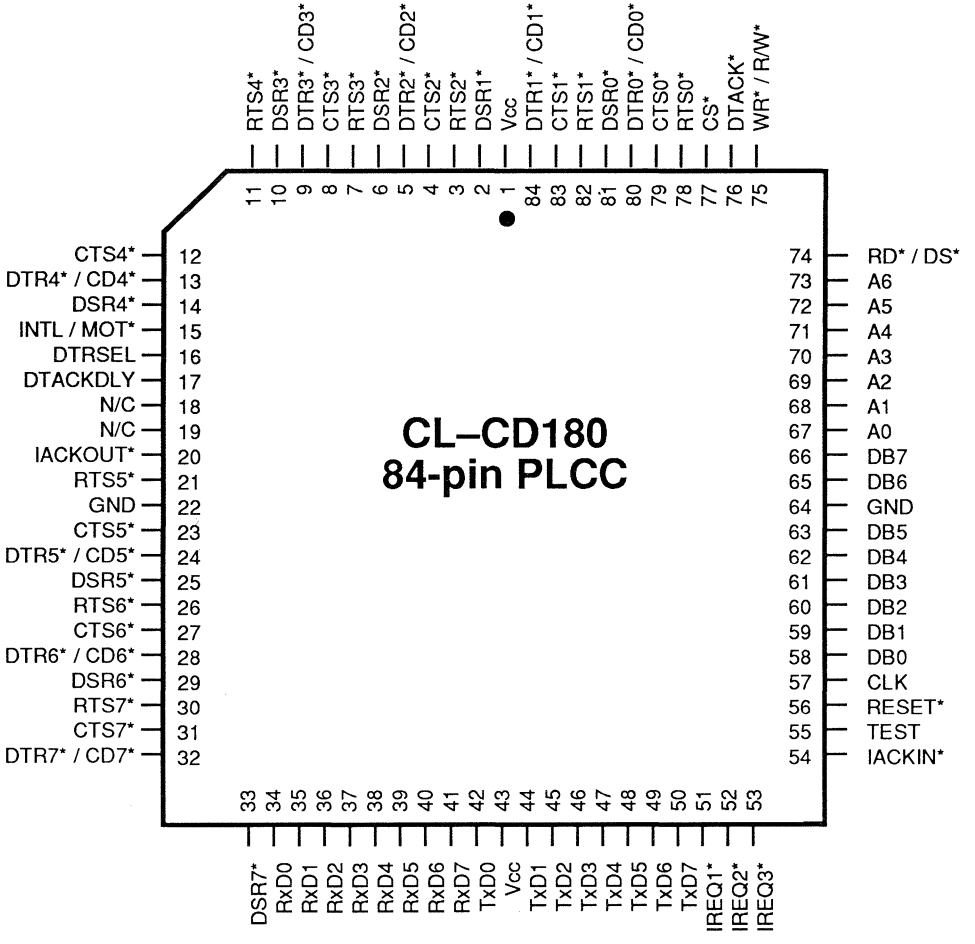
1. PIN INFORMATION

1.1 Pin Diagram



1.2 Pin Descriptions

Microprocessor Interface

SYMBOL	NUM.	TYPE	DESCRIPTION
Vcc	2	I	Power Supply
GND	2	I	Ground
A [0:6]	7	I	ADDRESS bits 0-6. Selects one of the internal registers of the selected channel. When A6 is high, it selects a Global register. When A6 is low, it selects a channel register.
CLK	1	I	SYSTEM CLOCK input. An 8- to 10-Mhz clock can be used as the master clock for the CD180
CS*	1	I	CHIP SELECT*. When low, an internal register is read or written. When high, sets the DB[0:7] to three-state condition.
DB [0:7]	8	I/O	DATA BUS 0-7. 8-bit bidirectional data bus for transfer of data, status and commands between the CD180 and the host.
DTACK*	1	O	DATA TRANSFER ACKNOWLEDGE*. Open-drain output. Asserted by the CD180 during any processor initiated read or write operation to the CD180. Also asserted by the CD180 to indicate a valid interrupt vector on the data bus during an IACK* initiated read operation.
DTACKDLY	1	I	DTACK DELAY. This signal selects the proper DTACK timing required. An active "low" input selects the 68010 compatible DTACK* timing. Data on the data bus pins are valid within 50 ns of DTACK* low on a read cycle. An active "high" signal on this pin selects the 68020 compatible DTACK* timing by delaying DTACK* assertion by 1/2 clock period. Data on the data bus pins are valid within 10 ns of DTACK* low on a read cycle.
RD*/DS*	1	I	READ*/ DATA STROBE*. An active-low signal strobes the data off the data bus and latches it on the trailing edge. When the 80x86 (Intel) bus interface is selected, this signal acts as the RD*. When 680x0 (Motorola) bus interface is selected, this signal acts as the DS*.
IACKIN*	1	I	INTERRUPT ACKNOWLEDGE INPUT*. This signal is connected to either the IACK* signal generated by the microprocessor to the first CD180 in a chain, or to the IACKOUT* of the previous CD180 in a chain.
IACKOUT*	1	O	INTERRUPT ACKNOWLEDGE OUTPUT*. This signal is an output to be connected to the IACKIN* input of the next CD180 in the daisy chain. When low, it signifies that the current CD180 is passing on the interrupt Acknowledge signal to the next CD180 in line.
INTL/MOTO*	1	I	INTEL / MOTOROLA*. This signal selects the microprocessor interface to be used. When "high", selects the Intel 80x86 bus interface. When "low", selects the 680x0 bus interface.

(*) denotes active low signal

1.2 Pin Descriptions

Microprocessor Interface *(cont.)*

SYMBOL	NUM.	TYPE	DESCRIPTION
IREQ[1:3]*	3	O	INTERRUPT REQUEST [1:3]*. Active low, open drain outputs. Types of interrupts within the CD180 are grouped into three groups. When active low, each of the IREQ signals indicates that an interrupt is pending for that group. IREQ1* is assigned to Modem Signal Change, IREQ2* to Transmit Data and IREQ3* to Receive Data interrupts.
RESET*	1	I	RESET*. An active-low signal asynchronously resets any device activity and clears the mode, command and status registers. During RESET*, CLK must be active. A minimum of five CLK periods is required.
WR*/ R/W*	1	I	WRITE* / READ/WRITE*. When the 80x86 bus interface is selected, this signal acts as the WR* signal. A " low "signal on this pin indicates a WRITE operation. When the 680x0 bus interface is selected, this signal acts as R/W*. A "high" on this input indicates a READ operation; a "low" on this input indicates a WRITE operation.
Test	1	I	TEST. This is a test function pin and is an active-high signal. This pin is not intended for customer use and should be tied low at all times.

Communications Interface

SYMBOL	NUM.	TYPE	DESCRIPTION
RTS[0:7]*	8	O	REQUEST TO SEND* / GENERAL PURPOSE OUTPUT 0 [0:7]*.
GPO0 [0:7]*			Modem outputs or General Purpose Outputs 0.
CTS [0:7]*	8	I	CLEAR TO SEND / GENERAL PURPOSE INPUT 1 [0:7]*. Modem
GPI1[0:7]*			inputs or General Purpose Input 1.
DTR[0:7]*/	8	I/O	DATA TERMINAL READY/ CARRIER DETECT / GENERAL PUR-
CD[0:7]*			POSE OUTPUT 2 [0:7]*. These signals can be configured to be either
GPI/0 2[0:7]*			inputs or outputs depending on the state of the DTRSEL signal. When DTRSEL is "low", these signals are configured to be inputs. If used as modem signals, these signals are then CD[0:7]*. When DTRSEL is "high", these signals are configured to be outputs. If used as modem signals, these signals are then DTR[0:7]*.
DSR[0:7]*	8	I	DATA SET READY* / GENERAL PURPOSE INPUT 3 [0:7]*.
GPI3[0:7]*			Modem inputs or General Purpose Input 3
DTRSEL	1	I	DTR SELECT. This signal configures the DTR/DCD[0:7]* pins to be either an input or an output. When this signal is "low", the DTR*/CD* signal is configured to be an input (CD*). When this signal is "high", the DTR*/CD* signal is configured to be an output (DTR*).
RxD [0:7]	8	I	RECEIVE DATA 0-7. Receiver serial data inputs. One for each channel. "Mark" is high and "Space" is low.
TxD [0:7]	8	O	TRANSMIT DATA 0-7. Transmitter serial data outputs. One for each channel. When idle, data outputs are in "Mark" condition.

(*) denotes active low signal

2. REGISTER TABLES

The CD180 contains two types of registers:

- Global registers - registers not specific to a particular channel
- Channel registers - registers specific to each channel

The channel registers are used to store parameters specific to each channel and the global registers are mostly used to store information specific to interrupt service. Some of the global registers are virtual registers and are valid only during interrupt.

Individual registers are addressed via a 7-bit address contained in Address bus bits A6 -A0. Address bit A6=1 selects the Global registers and A6=0 selects the Channel registers. When not servicing an interrupt, to access any of the channel registers, the host must first write the desired channel number into the Channel Access Register (CAR). Content of the CAR then becomes part of the address field needed to access the channel register file.

During interrupt service a context switching technique is used by the CD180 to reduce the number of cycles needed by the host to transfer data to and from the CD180. The CD180 makes available all the registers pertaining to the interrupting channel to the host. In an interrupt context, the CD180 automatically furnishes the interrupting channel number as part of any channel register address. The Channel Access Register content is preserved but is not used in an interrupt context. FIFO information is channeled through either the Receive Data Register, Receive Character Status Register or through the Transmit Data Register of the global register set.

2.1 Global Registers

(Used for basic timing and interrupt service)

Symbol	Register Name	R/W	Address (A6-A0)
GIVR	Global Interrupt Vector Register	R/W	1 0 0 0000
GICR	Global Interrupting Channel Register	R/W	1 0 0 0001
PILR1	Priority Interrupt Level Register 1	R/W	1 1 0 0001
PILR2	Priority Interrupt Level Register 2	R/W	1 1 0 0010
PILR3	Priority Interrupt Level Register 3	R/W	1 1 0 0011
CAR	Channel Access Register	R/W	1 1 0 0100
GFRCR	Global Firmware Revision Code Register	R	1 1 0 1011
PPRH	Prescaler Period Register High	R/W	1 1 1 0000
PPRL	Prescaler Period Register Low	R/W	1 1 1 0001
RDR	Receiver Data Register	R	1 1 1 1000
RCSR	Receiver Character Status Register	R	1 1 1 1010
TDR	Transmit Data Register	W	1 1 1 1011
EOIR	End of Interrupt Register	W	1 1 1 1111

2.2 Channel Registers

(used for defining channel specific parameters)

Symbol	Register Name	R/W	Address (A6-A0)
CCR	Channel Command Register	R/W	0 0 0 0001
IER	Interrupt Enable Register	R/W	0 0 0 0010
COR1	Channel Option Register 1	R/W	0 0 0 0011
COR2	Channel Option Register 2	R/W	0 0 0 0100
COR3	Channel Option Register 3	R/W	0 0 0 0101
CCSR	Channel Control Status Register	R	0 0 0 0110
RDCR	Receive Data Count Register	R	0 0 0 0111
SCHR1	Special Character Register 1	R/W	0 0 0 1001
SCHR2	Special Character Register 2	R/W	0 0 0 1010
SCHR3	Special Character Register 3	R/W	0 0 0 1011
SCHR4	Special Character Register 4	R/W	0 0 0 1100
MCOR1	Modem Change Option 1 Register	R/W	0 0 1 0000
MCOR2	Modem Change Option 2 Register	R/W	0 0 1 0001
MCR	Modem Change Register	R/W	0 0 1 0010
RTPR	Receive Timeout Period Register	R/W	0 0 1 1000
MSVR	Modem Signal Value Register	R/W	0 1 0 1000
RBPRH	Receive Baud Rate Period Register High	R/W	0 1 1 0001
RBPRL	Receive Baud Rate Period Register Low	R/W	0 1 1 0010
TBPRH	Transmit Baud Rate Period Register High	R/W	0 1 1 1001
TBPRL	Transmit Baud Rate Period Register Low	R/W	0 1 1 1010

3. FUNCTIONAL DESCRIPTION

The CD180 contains the following major functional blocks:

- Microprocessor Interface and System Configurations
- System Clock Requirements and Baud Rate Generation
- Channel and Register Addressing
- CD 180 Initialization
- Interrupt Scheme and Arbitration
- Transmitter Operation
- Receiver Operation
- Modem and GP I/O Pin Functions
- Flow Control
- Counter/Timer Functions
- Diagnostic Functions

3.1 Microprocessor Interface and System Configurations

The CD180 supports both the Motorola 680x0 and the Intel 80x86 bus interfaces. Bus interface selection is achieved via the INTL/MOTO* signal. When this signal is "high," the Intel bus interface is selected. When this signal is "low", the Motorola bus interface is selected.

Two signals have dual meaning - RD*/DS* and WR* / R/W* and are controlled by the INTL/MOTO* signal. When the Intel bus interface is selected, these two pins function as RD* and WR*. These pins can be connected to either the IOR* and IOW* or to MEMRD* and MEMWR* depending on which part of the memory the CD180 is mapped into. When the Motorola bus interface is selected, these two signals function as DS* and R/W*.

Diagrams in the System Configuration section illustrate typical applications using single or multiple CD180s with 680x0- or 80x86-microprocessor based systems.

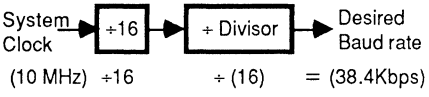
3.2 System Clock Requirements and Baud Rate Generation

System Clock Requirement

System clock is a high frequency clock used by the CD180 to derive all the necessary timing needed for proper operation. System clock must be supplied by the user. The CD180 is designed to accept the same clock used by the host. Maximum clock frequency is 10 Mhz and should have a minimum high time and low time of 45 nsec. The CD180 is capable of handling system clock levels of TTL compatible voltage swings.

Baud Rate Generation

The CD180 supports independent transmitter and receiver baud rates on each of its eight channels. The baud rate is determined by a 16-bit period value (divisor) stored in the Transmitter Baud Rate Period Registers (TBPRH and TBPRL) or in the Receiver Baud Rate Period Registers (RBPRH and RBPRL). These registers establish the period of the corresponding transmitter and receiver baud rate counters.



The value to be loaded to set a given baud rate is determined by the following equation:

Baud Rate Period (divisor) =
CLK (system clock) frequency
÷ (16 x desired baud rate)

The above equation will in general yield a non-integer result. The nearest integer value is the optimum choice for that baud rate and system clock combination. The value loaded in the Baud rate Period Registers must be that integer expressed as a 16-bit binary value. The baud rate error is the difference between the integer value and the ideal value expressed as a percentage.

For minimum tolerance on the baud rates, a system clock frequency of 9.8304 Mhz is recommended. The popular baud rates and their corresponding divisors are shown as follows for system clocks of 10 Mhz and 9.8304 Mhz:

Baud Rate	Divisor @ 10 Mhz	Error @ 10 Mhz
110	5682	-0.003%
150	4167	-0.008%
300	2083	+0.016%
600	1042	-0.030%
1,200	521	-0.030%
2,400	260	+0.160%
4,800	130	+0.160%
9,600	65	+0.160%
19,200	33	+1.350%
38,400	16	+1.725%

Baud Rate	Divisor @ 9.8304Mhz	Error @ 9.8304Mhz
110	5585	+0.008%
150	4096	0.000%
300	2048	0.000%
600	1024	0.000%
1,200	512	0.000%
2,400	256	0.000%
4,800	128	0.000%
9,600	64	0.000%
19,200	32	0.000%
38,400	16	0.000%

3.3 Channel and Register Addressing

The CD180 is addressed through an active low chip select (CS*) in conjunction with seven (7) address inputs A[0:6] which are mapped to CD180 internal addresses in two addressing modes, global and channel. In channel addressing mode, the bits defining the channel to be accessed are provided from the Channel Address Register within the CD180.

The most significant address input A6 performs the selection between global and channel specific addresses. If this bit is a "1", the address is global and is not associated with any specific channel. If this bit is a 0, the address is channel-related.

When not in an interrupt service routine, the Channel Access Register supplies a channel number to address the CD180's channel specific registers. The C0 - C2 bits contain the desired channel number. The A7 bit is used for both global- and channel-oriented access and is provided to give complete access to the CD180's registers for test purposes. In ordinary operation, the host does not require access to registers in that portion of the internal address space. Thus this bit should always be 0.

The host never needs to perform address computation to correctly access the CD180 during interrupt service. This is because the only channel specific registers accessible to the host within an interrupt service routine are those of the channel for which the interrupt occurred.

Certain registers only have meaning within an interrupt context. For example, the Receiver Data Register, Receiver Data Count Register and the Receiver Character Status Register are only useful when configured for receive FIFO support within a receive data interrupt context. If read outside the receive data interrupt context, the results will be unpredictable and may cause loss of data and CD180 functional errors. Similarly, the Global Interrupting Channel Register only supplies a meaningful channel number within an interrupt service routine.

3.4 CD180 Initialization

CD180 initialization begins with a mandatory hardware reset applied through the active low RESET* input. The system clock CLK input must be active during the hardware reset and the reset duration must be at least five (5) clock periods. It is not necessary to synchronize RESET* with CLK.

Immediately following the hardware reset, the CD180 goes through a firmware initialization, reaching an idle mode within 500 µsecs of the end of hardware reset. This may be verified by the host by reading the Global Interrupt Vector register and finding its contents to be FF hex. Upon reset, the user may then configure the CD180 for the desired channel functions as described in other sections of the specification.

Before starting normal operations on the CD180 ports, the user must initialize the chip by programming several global registers: Prescaler Period Registers, the Global Interrupt Vector Register, and Priority Interrupt Level Registers.

Set Prescaler Period Registers

The PPR determines the fundamental "tick" rate for all the CD180's on-chip timers - receiver data

timeouts and transmitter real-time delay timers. The PPR counts clock (CLK) periods and the minimum PPR value used must guarantee a "tick" length of at least 0.5 msec. This requires a minimum value of 1333h for 9.830 Mhz CLK or 1388h for 10 Mhz CLK.

Set Global Interrupt Vector Register

The Global Interrupt Vector Register consists of 5 MSBs of user supplied information and 3 LSBs CD180 supplied interrupt group information. This modified interrupt vector supplied by the CD180 during interrupt acknowledgement cycle will direct the host to the proper interrupt service subroutine.

The host writes the 5 MSBs into the GIVR during initialization. These five bits may be a Chip ID number or whatever code that is appropriate for interrupt handling.

Set Priority Interrupt Level Registers

Three registers in the global set, PIL1-3, stores the priority interrupt levels for the three groups of interrupts. These levels are used to match with the priority levels put out on the address bus by the host during an interrupt acknowledgement cycle. Since these levels are system dependent, the user must initialize these registers with the proper priority levels.

Channel Initialization

Prior to enabling the individual channels, the user must program the channel registers with desired channel options and parameters such as character lengths, parity type, receive FIFO thresholds, modem signal detection levels, baud rates, enable interrupts prior to start of normal operation.

Channel initialization is accomplished by first writing to the Channel Access Register (CAR) with the number of the channel to be programmed. This channel number will automatically become part of the address for subsequent channel register programming. Thus the host can use the same set of register addresses for all channels.

3.5 Interrupt Scheme and Arbitration

To efficiently support a potentially large number of interrupts in a multiple CD180 system, The CD180 divides the interrupt handling tasks into three functions :

- Interrupt grouping inside each CD180
- Interrupt arbitration between multiple CD180's
- Interrupt sequence with the microprocessor

Interrupt Grouping Within the CD180

Each transmitter and receiver require service from the microprocessor from time to time due to certain conditions happening. Typical conditions for interrupts tend to fall into three basic categories:

- Data is received from the remote terminals and needs to be transferred to the microprocessor
- Character needs to be given to the transmitter before the transmission is interrupted
- Specific conditions occurring such as a modem signal changing state, excessive time delay between character reception etc.

Each category of interrupt conditions can tolerate different time delays in being serviced, thus the categories of interrupts are grouped by type . The CD180 groups these conditions as follows:

- Group 3 - Receive Data
- Group 2 - Transmit Data
- Group 1 - Modem Signal Change

An Interrupt Request (IREQ*) signal is assigned to each group. Group 1 interrupt is assigned to IREQ1*. Group 2 interrupt is assigned to IREQ2* and Group 3 interrupt is assigned to IREQ3*. All three interrupts could occur at the same time. No priority is assigned by the CD180 internally. Prioritization of these three groups can be assigned externally by the user depending on the individual system needs.

Group 3 Interrupts - Receive Data

Each receiver has eight bytes of FIFO to buffer received data and 8 bytes of FIFO to buffer received data status. In addition to the FIFO, each channel also contains a data holding register and a data shift register. Effectively each transmitter and receiver has 10 bytes of storage.

The Receive Data FIFO (RxFIFO) has a programmable threshold to set the amount of data to be received prior to raising an interrupt to the host. When this threshold is reached, a Receive Data interrupt is asserted.

For data transfer, Group 3 interrupt conditions are subdivided into two types:

- Type 1 - Receive Good Data
- Type 2 - Receive Exception

Receive Good Data - A Receive Good Data interrupt is raised for one of the following conditions:

- RxFIFO threshold reached and the FIFO contains good data
- RxFIFO threshold not reached but the FIFO contains good data when the receive data timer times out
- RxFIFO threshold not reached but the FIFO contains good data when the newly arrived data contains an exception condition

A Receive Good Data interrupt must first be raised to take the good data away before a receive exception interrupt can be raised for the exception data.

When any of these conditions occur, the modified interrupt vector will indicate to the host that the interrupt is for good data.

Receive Exception Interrupt - Unusual or exception conditions are reported to the host one character at a time through the Receive Exception interrupt. The host must determine the interrupting channel by reading the GICR. It must determine the specific exception(s) by reading the Receive Character Status Register. For many exceptions it will not be necessary to read the Receive Data Register. If special character detection in enabled, the interrupt may be for the recognition of a special character. The exception code will indicate which character or character sequence was detected. The exception may also be for detection of a parity or framing error, or recognition of a line break condition. A receiver overrun may have occurred and this status may be noted in addition to most other exceptions.

An exception may be for the first receive data timeout following the transfer of all data from the channel to the host. This timeout interrupt is useful to the host for managing data transfer from its buffer to its host or to recognize that the arriving data stream has concluded or has been interrupted. This receive exception timeout interrupt can be enabled or disabled by controlling the RET bit in the Interrupt Enable Register.

Group 2 Interrupts - Transmit Data

Each transmitter contains 8 bytes of transmit FIFO in addition to the transmit holding register and the transmit shift register. As data is being transmitted, the FIFO status is being monitored by the CD180. An interrupt request is raised for one of the following conditions:

- Transmit FIFO Empty - When the transmit FIFO is empty, there is still one character in the transmit holding register and one character in the transmit shift register. The host has two character times to respond to this request without interrupting the transmit data stream.
- Transmitter Empty - The transmit FIFO, transmit holding register and the transmit shift registers are now all empty. This signifies that all characters written to the FIFO have been completely transmitted.

The host can select which of these causes for transmit interrupt will be used by programming the options in the Interrupt Enable Register (IER).

Group 1 Interrupt - Modem Signal Change

The CD180 may be programmed to assert a Group 1 interrupt when a channel's modem input signals have changed states. The change detect options are programmed in the Modem Change Option Registers. Individual modem pin interrupts are enabled by setting the corresponding bits in the Interrupt Enable Register.

The host may read the Modem Change Register to determine which modem signal changes were detected. The Modem Change Register must be reset to zero before exiting the interrupt.

Interrupt Arbitration Among Multiple CD180s

In a multiple CD180 environment, a passive interrupt arbitration is accomplished via a daisy chain scheme in conjunction with monitoring the common IREQ signals. Interrupt arbitration is accomplished via a set of interrupt signals as follows:

- IREQ[1:3]* 3-bit open drain Interrupt Request bus. Each IREQ signal reflects one group of interrupt condition. IREQ1* is assigned to group 1 interrupts, IREQ2* is assigned to group 2 interrupts and IREQ3* is assigned to group 3 interrupts.

- IACKIN* This signal is either the IACK* signal generated by the microprocessor or the IACKOUT* signal from the previous CD180 in a chain.

- IACKOUT* This signal is the interrupt acknowledgement passed on by an CD180 without a pending interrupt of the type being acknowledged.

Each CD180, when requiring service from the host, asserts its requests onto the IREQ[1:3]* bus. If the CD180 has an interrupt from one group, it will assert the corresponding IREQ* signal for that group. If the CD180 has interrupt requests from all three groups, it will assert all three IREQ* signals.

All CD180s in the chain assert their interrupt requests simultaneously, thus all CD180s with interrupt requests for that one group of interrupt conditions will pull the corresponding IREQ signal low. The IREQ[1:3]* signals can be connected to an external priority encoder for priority assignment. Exactly how these priorities are assigned is a system level function and is left entirely to the user. The external priority encoder in turn provides the IREQ signal and the proper priority level to microprocessor.

The microprocessor, when servicing the interrupt will then issue an IACK* signal in conjunction with issuing the priority level it is currently servicing on the address bus. The priority level on the address bus A[0:6] is compared internally by all the CD180s to values stored in the three Priority Interrupt Level Registers (PILR1-3). Each PILR value must be unique. The first CD180, receiving the IACK* signal on its IACKIN* input, will compare its interrupt acknowledge level comparison results with its internal interrupt requests. If there is a match, the CD180 accepts this interrupt acknowledge. If the CD180 recognizes the acknowledgement type but does not have the corresponding interrupt request pending, it will pass this interrupt acknowledge to the next CD180 in the chain by lowering the IACKOUT* signal.

In an Intel 80x86 bus interface system, the user must generate the IACKIN* signal and the Priority Interrupt Level code predefined by the user for the type of interrupt being acknowledged. This may be done by mapping the interrupt acknowledge function into the I/O address space. Using this scheme, the PIL code is supplied by the low order address A[0:6] of the Address bus and the IACKIN* signal is decoded off the high order address bits of the Address bus. The data read by the host from the CD180 will be the interrupt vector.

Fair Share Scheme - To avoid the strict positional priority of a conventional daisy chain, a "fair share" scheme is used to grant equal interrupt service to all CD180s.

If an CD180 has requested access to interrupt service in a given group, it sets an internal flip flop to inhibit additional requests for this service group. It will monitor the IREQ* signal for that group. Once the IREQ* signal for that group is seen to be inactive, the CD180 clears its corresponding fair share flip flop, re-enabling its interrupt request logic. The effect is that all

CD180's in a chain may request service simultaneously. None of the CD180's may request interrupt service again until all outstanding requests for that interrupt group have been serviced.

Interrupt Service

At the time the microprocessor issues the IACK* signal, it is passed down the interrupt acknowledge chain to the first CD180 in the chain requesting service for the interrupt group being acknowledged. The CD180 accepting the acknowledgment will then place a modified interrupt vector onto the data bus. The vector conveys to the host the exact nature of interrupt and the chip ID number previously written to the Global Interrupt Vector Register (GIVR). This vector allows the host to go directly to the proper interrupt subroutine. Once in the subroutine, the next byte of information needed will be the channel number. The host then can address the Global Interrupting Channel Register to find out which channel has requested service.

If the Interrupt Vector indicates that it is a receive data interrupt for good data, then the host will read the Receive Data Count Register (RDCR) to find out how many bytes of consecutive good data are ready for transfer. Once this information is obtained, the host will read from the Receive Data Register for the number of bytes. The RDCR facilitates the data transfer by eliminating the usual status checks and decision branches normally required for each byte of data transferred.

If the Vector indicates that the interrupt is a transmit interrupt, the host may then write, up to 8 bytes of data directly one after another, to the Transmit Data Register.

If the Vector indicates that the interrupt is a receive character with exception status or is for a modem signal change, the host will then either access the Receive Character Status Register or the modem Change Register to determine the exact cause for the interrupt.

End of interrupt service must be signalled to the CD180 by writing to End Of Interrupt Register (EOIR). This action "pops" the CD180's internal interrupt context stack. A new interrupt context is pushed onto the stack each time the host acknowledges an interrupt. The CD180's interrupts may be nested and may be acknowledged in any order.

3.6 Transmitter Operation

Upon power on reset, all transmitters are disabled with their Tx output held in the "MARK" or logic "1" condition. After initialization of the appropriate registers selecting baud rates, character parameters and issuing the channel command to enable transmission, the transmitter of the enabled channels will be conditioned to transmit. Once the transmitter and the transmit interrupt is enabled for a channel, an interrupt will be asserted for that channel requesting data for transmission. As soon as a character is written into the transmit FIFO, the transmitter starts to transmit by first sending the START bit (logic "0") followed by the data character according to predefined character length, least significant bit first. An optional parity bit (none, odd, even or forced) is appended followed by the final STOP bit(s) (logic "1" or "Mark"). The number of STOP bit(s) can be one, one-and-a-half, or two bit times long.

The transmitter will continue sending characters one after the other as long as the transmit FIFO is not empty. When the transmit FIFO becomes empty, the transmitter will stop transmission and will hold the TxD output in the MARK condition. Transmission will resume as soon as there is another character in the FIFO.

Automatic flow control features are supported and are described in the Flow Control section.

Break generation for a timed interval and inter-character transmission delays are supported through escape sequences embedded in the transmit data stream.

Transmitter Interrupt

An eight-byte FIFO is provided for each transmitter. In addition to the 8-byte FIFO, the CD180 also contains a transmit holding register and a transmit shift register. Generating a transmit interrupt depends on control bits in the Interrupt Enable Register. Setting the TxRdy bit of the IER specifies that a transmit interrupt be generated when the FIFO is empty. When this condition occurs, there is still one character in the transmit holding register and another character in the

transmit shift register. The CPU therefore has up to two character times to respond before the transmitter output goes into the idle (MARK) condition.

When servicing a transmit interrupt, up to eight characters can be written into the Transmit Data Register (TDR) consecutively.

Setting the TxMpty bit of the IER specifies that a transmit interrupt be generated only when the FIFO is empty, the transmit holding register is empty and the transmit shift register is empty. When this condition occurs, it means that all characters have been completely transmitted and the channel can now be reconfigured .

End of interrupt service must be signalled to the CD180 by writing to End Of Interrupt Register (EOIR).

Special Transmitter Commands

The CD180 may be enabled to recognize certain "escape" sequences as commands embedded in the transmit data stream. These commands are issued to introduce a time delay between characters or to insert an idle period during LINE BREAK.

These capabilities are enabled on a per channel basis by setting the Embedded Transmit Command (ETC) bit in the Channel Option Register 2 (COR2). The "null" (all zero) character is used as the ESCape character. The following functions are supported:

ESC ESC	Send one ESC character as normal data
ESC 81h	Send BREAK - enter line break condition for at least one character time. If the insert delay special character sequence immediately follows the Send Break sequence, the duration of the break transmission is extended by the amount of the programmed delay.
ESC 82h xxh	Insert Delay. Insert a delay of "xx" (interpreted as an unsigned binary number) times the programmed timer "tick" set by the Prescaler Period Registers. Multiple insert delay commands can be executed consecutively by the CD180. If "xx" is zero, no delay is inserted.
ESC 83h	Stop Break. Must follow the Send Break sequence. Optional Insert Delay sequence may precede the Stop Break sequence

Special Character Generation

Selected special Character or two-character sequence may be sent pre-emptively by setting the appropriate bits in the Channel Command Register (CCR). Send SP CH bit of the CCR , when set, initiates the Send Special Character Command. SSPC0-2 bits of the CCR then specify which character or two-character sequence is to be used. Two character sequence is defined by bits XonCH and XoffCH of COR3.

When this command is given, the CD180 will insert the special character(s) into the data stream immediately following the current character in the transmit holding register, preempting all other characters in the TxFIFO.

The CCR is reset by the CD180 as an acknowledgement of the command. A new command must not be issued if the CCR contents are non-zero. A send special character command will be recognized and cleared within two character times.

3.7 Receiver Operation

Upon master reset, all receivers are disabled. To condition any receiver to receive, it must be correctly initialized and enabled. Any conditioned receiver waits for a high-to-low transition on its corresponding RxD input. Once a transition is detected, the receiver checks the state of the RxD input again one half bit time later to validate the START bit. A valid START bit is defined to be a "SPACE " or logic "0". If the RxD input is no longer a "SPACE", then a false START bit is assumed and the receiver resumes the search for a high-to-low transition. If a valid START bit is detected, the RxD is now sampled at one bit time intervals in the middle of the bit to ensure stable data. Characters are assembled according to the programmed content of the Channel Option Register (COR1). Valid character framing (presence of a Stop bit) and optional parity bit are checked. After a character is assembled, the

receiver checks for special character compares and overrun condition before placing the character and its corresponding status into the receive FIFO (and Status FIFO if applicable).

An overrun condition occurs when the new data has arrived but the RxFIFO and the receive holding register are both full. The new data is lost and the overrun indication is flagged on the character in the holding register. That character and its status including the overrun indication will eventually be transferred to the host by a Receive Exception interrupt.

When a line break condition is recognized (zero data with zero parity and STOP bit) , one NULL character is loaded into the receive FIFO and a Break status is recorded in the Status FIFO. No further FIFO entries will be made until normal character reception is resumed. Note, a Receive Exception interrupt for Receiver Timeout may occur during a line break condition.

Receiver Interrupt

Receiver interrupts can be invoked under several conditions:

- Receive FIFO threshold reached or exceeded
- Receiver timer timeout - interval between character reception exceeds timeout value
- Receive exception data
- Special character detection

Receive FIFO Threshold

Eight bytes of FIFO is assigned to each receiver, in addition to the Receive Holding register and the Receive Shift register, for data storage. The CD180 can be programmed to generate an interrupt once the number of bytes of data received and stored in the FIFO reaches a programmed threshold. The RxFIFO interrupt threshold can be selected by programming the RxTH3-0 bits in the Channel Option Register 3. An interrupt threshold of 1 to 8 characters can be selected. Once this threshold is defined, an interrupt will be automatically triggered when the condition is met.

Receiver interrupts are enabled or disabled via the RxData bit in the Interrupt Enable Register. RxData bit, when set to "1" enables interrupts to be asserted for the above causes.

Timer Timeout

A software timer with its duration set by the Receive Timeout Period Register (RTPR) value, is implemented for each receiver to monitor time elapsed between characters. An eight-bit value can be programmed into this register to define the duration of the timeout. The timer is decremented on each "tick" of the prescaler counter. The timer is reloaded with the RTPR value whenever a character is placed in the FIFO. If the Receive Timeout counter reaches zero and receiver interrupts are enabled, a receiver data interrupt will be asserted. If there is data in the FIFO (it must be good data or a receive exception interrupt would have occurred), a receive good data interrupt will be given to the host. If the Receive Exception Timeout is enabled in the Interrupt Enable Register, and if there is no data in the FIFO, a Receive Exception interrupt will be given to the host with status indicating the timer timeout. This interrupt will only occur the first time the timer expires after the FIFO is emptied.

The Prescaler Period counter is a 16-bit counter clocked by the system clock. If the system clock is a 10 Mhz clock, the maximum count will establish a "tick" every 6.5536 msec. The prescaler period must be set to generate a minimum "tick" period of 0.5 msec.The Receive Timeout counter is an 8-bit counter decremented on every "tick" of the prescaler counter. At the maximum count per "tick", the maximum timeout period is 1.671 sec.

The receive timeout is always enabled to cause data transfer when the receive data interrupt is enabled. From the system applications point of view, this timeout function is important for asynchronous data transmission. This is especially true when a FIFO is in use and an interrupt threshold for the FIFO is set greater than one character. The timer interrupt will eliminate long response times when excessive delay between characters occurs caused either by the remote operator or due to the line being disabled. The optional timer interrupt which occurs after all data is transferred to the host may be used to manage transfers from the host's receive data buffers.

Receive Exception Data

The CD180 monitors the integrity of received characters during incoming character assembly.

Exception Data conditions monitored are framing error, parity error, FIFO overrun and line break conditions. Any of these conditions will cause a corresponding bit in the Receive Character Status FIFO to be set.

Special Character Recognition

The user may individually enable a CD180's channel to recognize Special Characters by setting the Special Character Detect Enable (SCDE) bit in the Channel Option Register 3 (COR3). XonCH and XoffCH bits in COR3 define whether single character compare or 2-character sequence compare is required for Xon and Xoff characters.

Four Special Characters registers are provided per channel for this purpose. If single character compare is enabled, the CD180 will compare data in the data stream against the four special characters stored in the Special Character Registers (SCHR1-4).

If double-character sequence compare is enabled, the COR3 will be programmed to define which double-character sequence is to be compared with the data in the data stream.

Special character options such as four individual characters or two two-character pairs may be recognized. Two two-character pairs may share a common first character, however, the same character must be programmed in both SCHR1 and SCHR3.

Upon detection of the special characters, the user can elect to receive or not to receive a status by controlling the Receive Special Character (RxSC) in the Interrupt Enable Register (IER) and the Flow Control Transparency (FCT) bit in COR3. If FCT is set, the CD180 will process flow control characters and discard them. If it is not set, received flow control characters will be processed and passed on to the host. The RxSC bit applies to all special characters while the FCT bit controls the status generation for the automatic flow control modes.

When the CD180 receives a character or character sequence that matches one of these codes and FCT is zero, it will set a corresponding Special Character Compare code in the Receive Character Status Register if Receive Special Character (RxSC) bit is set in the IER. Since there is a one-to-one correspondence between the status FIFO and the RxFIFO, the special character detected will also be stored in the RxFIFO. If the special character is a two-character sequence, then only the second character of the special character sequence is stored in the RxFIFO.

In the event that a special condition (e.g. framing error or parity error) occurred on a special character, the CD180 will not interpret this character as a matched character. However, if an overrun condition occurred after a special character is detected, the new character is lost and the overrun status is set in the Receiver Character Status Register. Under this condition, the CD180 will give both an overrun exception status and a special character recognition status.

The user may enable or disable special character recognition by programming SDCE in the COR3 register. In-Band transmit flow control is enabled and disabled by programming the TxIBE bit of COR2. If fewer than four special characters are required, the unused Special Character register(s) may be disabled by duplicating the pattern of one of the special characters used.

A summary of the special character detection functions is shown as follows:

SCDE	RxSC	FCT	Function
0	x	x	Special character detection function disabled for the channel.
1	0	x	Special character detection function enabled for the channel. Special character interrupt generation is disabled; thus no interrupt will be generated.
1	1	0	Special character detection function enabled for the channel. Flow control transparency mode disabled. Interrupt will be generated for any special character or character sequence detected. The special character detected will be stored in the RxFIFO. In the case of a two-character sequence, only the second character will be stored in the RxFIFO. The character itself does not have much meaning, but is required to provide meaning to the corresponding status byte in the status FIFO.
1	1	1	Special character detection function enabled for the channel. With the flow control transparency mode enabled, interrupts will only be generated for the special characters that are not used for flow control. Characters used for flow control will not be stored in the RxFIFO upon detection. Only non-flow control characters will be stored in the RxFIFO.If all four special characters are used for flow control, no interrupt will be generated.

3.8 Modem and GPI/O Pin Functions

Each channel of the CD180 has four modem control or general purpose pins:

RTS*/GPO0*	Request to Send / General Purpose Output 0
CTS*/GPI1*	Clear to Send / General Purpose Input 1
DTR*/CD*/GPIO2*	Data Terminal Ready / Carrier Detect / General Purpose Input/Output 2
DSR*/GPI3*	Data Set Ready / General Purpose Input 3

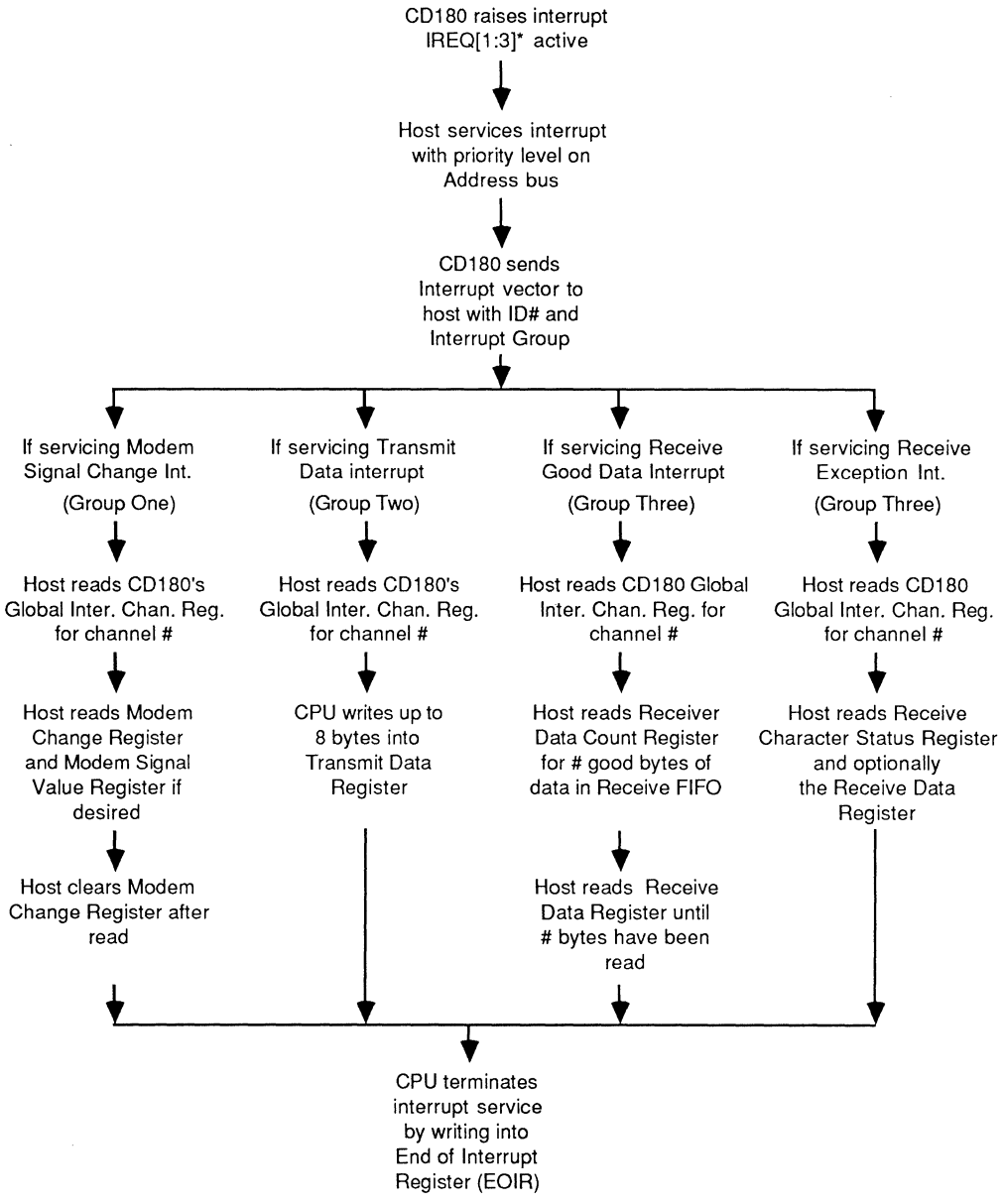
The user has direct control over the RTS* and DTR* outputs and can sense the state of inputs CTS*, CD* and DSR* through the Modem Signal Value Register (MSVR). Note that the values presented in MSVR are positive true (active high), while these pin functions are all active low.

DTR*/CD*/GPIO2* is a bi-directional signal. This signal can be programmed to be either an output (DTR*), or as an input (CD*) by controlling the DTRSEL signal. When DTRSEL input is "high", this signal is programmed to act as an output (DTR*). When DTRSEL is "low", this signal is programmed to act as an input (CD*).

The CD180 can generate interrupts when any of the input pins changes state. Either or both edges maybe detected by setting bits in the two Modem Change Option Registers (MCOR1 and MCOR2). For each pin, the user can individually enable on-to-off or off-to-on transition detection of the inputs. When the CD180 detects such a transition, it sets the corresponding bit in the Modem Change Register. If the corresponding bit in the channel's Interrupt Enable Register is set, the CD180 will assert its IREQ1* output when instructed to do so by the scanner. The user must clear the Modem Change Register during the interrupt service routine before writing to the EOIR.

The modem inputs are examined for input level changes at intervals of less than 250 µsec.

CD180 Interrupt Sequence



The user can control the modem output signals RTS and DTR directly by writing to the Modem Signal Value Register. The user can also program "auto-output" modes for a channel's transmitter by setting the RtsAO bit of the COR2 register.

When the RtsAO bit is set, the user puts the RTS signal into auto-enable mode. In this mode, the CD180 will assert the channel's RTS* pin whenever the channel is enabled and data is available for transmission.

When the CtsAE bit is set in Channel Option Register 2 (COR2), the user puts the CTS into auto-enable mode. In this mode, the transmitter will not send data unless the CTS* input is asserted.

If the DTRSEL pin is high, the user selects the DTR* output mode of the DTR*/CD* pins. In this mode, the user must directly control both RTS* and DTR*. The RtsAO option should not be used.

The DsrAE is used as the receiver enable or disable. When the DsrAE bit is set in the COR2 register, if DSR is high, the receiver is enabled. If DSR is low, the receiver is disabled and the RxD input is ignored.

All changes to the Channel Option Registers must be accompanied by setting the appropriate Channel Option Registers "changed" bits in the Channel Command Register (CCR). The CD180 regularly samples the Channel Command Register for any value that is not zero. If the CCR is not zero, the CD180 decodes the command or commands, acts on them and clears the CCR to signify acceptance of the commands.

3.9 Flow Control

The CD180 provides both programmed controlled and automatic In-Band (Xon/Xoff)) and Out-of-Band flow control functions. In-Band flow control recognizes special characters or character sequences for Xon and Xoff control embedded in the data stream. Out-of-Band flow control uses the modem handshake signals, RTS/CTS, or DTR/DSR to control the flow of data. Automatic flow control functions are controlled by bits in Channel Option Register 2 (COR2).

Channel enable and flow control status is stored in the Channel Control Status Register (CCSR). Two bits, RxEn and TxEn show the enabled status of the channel's receiver and transmitter. Four bits are used to indicate the current state of the channels regarding flow control. These status bits are: TxFloff, TxFlon, RxFloff, RxFlon.

TxFloff, TxFlon apply to the channel status when the remote device is flow controlling the CD180's channel transmitter. When the remote requests the CD180 to stop transmission, the CD180 will set the TxFloff status bit in the CCSR. When the remote requests the CD180 to restart transmission, the CD180 will reset the TxFoff bit and sets the TxFlon bit. As soon as transmission resumes, the TxFlon bit will be reset.

Transmit flow status bits will also be reset by enabling or disabling the transmitter or resetting the channel.

RxFloff and RxFlon apply to the channel status when the CD180 is flow controlling the remote. There is no automatic mode for this function. The host will flow control the remote device by the Send Xon and Send Xoff commands. The RxFloff bit is set when the Send Xoff command is processed by the CD180. The RxFlon bit is set when the Send Xon command is processed by the CD180 . RxFlon will reset the RxFloff bit. The RxFlon bit will be reset when the CD180 receives a new non flow control character.

In-Band (Software) Flow Control - uses host defined Xon, Xoff characters embedded in the data stream

The CD180 supports automatic In-Band flow control in one direction only - transmit flow control. Transmit flow control is defined to be that the CD180 is transmitting data and is flow controlled by the remote unit.

Receive flow control can be supported under programmed control. Receive flow control is defined to be the host flow controlling the remote.

Transmit In-Band Flow Control

The user enables this automatic mode by setting Transmit In-Band Enable (TxIBE) bit in COR2 register. In this mode, the remote unit will transmit an Xoff character to the CD180 when it wants the CD180 to suspend transmission. The CD180, upon receiving the Xoff character(s), will terminate the transmission as soon as the current character in the transmit shift register and the character in the transmit holding register are completely shifted out . The remote device can signal the CD180 to resume transmission in one of two ways depending on the setting of the Implied Xon Mode (IXM) option bit COR2.

The CD180 will resume transmission upon receipt of an Xon character. When the IXM bit is set, the CD180 will resume transmission upon receipt of any character (each character carries an implied Xon interpretation). When the IXM bit is not set, the CD180 will only resume transmission upon receipt of an Xon character. In addition, the host may force a resumption of transmission by issuing a transmit enable command which will clear the TxFloff bit.

Receive In-Band Flow Control

The host implements In-Band flow control through use of the Send Special Character command. The CD180 records receive flow control status as described in the beginning of this section. Receive In-Band flow control is not an automatic function.

Out-of-Band (hardware) Flow Control - Transmit

The CD180 supports automatic transmit Out-of-Band flow control via modem signals - RTS/CTS.

The automatic mode is configured by setting the RtsAO and CtsAE bits of the COR2 register. When in this mode, the CD180 automatically monitors the CTS signal during data transmission. Upon detection of a CTS drop, the CD180 will terminate transmission after finishing the transmission of the current character in the Transmit shift register and the character in the transmit holding register, if any.

Out-of-Band (hardware) Flow Control – Receive

An Out-of-Band automatic flow control mode has been implemented using the DTR pin, and the Modem Control Option Register 1 (MCOR1). To use the DTR option, the DTR/CD* pins must be programmed in the DTR* (output) mode via the DTRSEL pin. The lower 4 bits in MCOR1 can be programmed to set a receive FIFO threshold at which the DTR pin will be deactivated to flow control the remote transmitter. The lower four bits of MCOR1 follow the same format as the receive interrupt threshold bits in COR3, with the exception that the all zero pattern is used to disable the DTR option.

Whenever a character is received and the receive FIFO interrupt threshold has been reached the DTR threshold is checked and if it has been reached the DTR pin will be deactivated. Whenever a receive data interrupt has been serviced and the DTR option is enabled (DTRth {3:0} non zero), if the receive fifo is below the DTR threshold the DTR pin is reactivated. This feature can be used to automatically flow control the remote transmitter when the Host is slow responding to a receive interrupt or when the receive interrupt has been temporarily disabled.

When the channel is enabled, disabled or reset via the Channel Command Register (CCR) the appropriate action is taken on the DTR pin, by the CL-CD180. In the case of channel receive enable command if the DTR option is enabled the DTR pin is activated. If the channel receive disable or channel reset commands are issued and the DTR option is enabled the DTR pin is deactivated. Similarly if the channel is transmit disabled or reset and the RTS Automatic Output Enable Mode is active the RTS pin will be deactivated, when the current character is transmitted. When the CD180 is reset all the modem output pins are deactivated.

Flow Control Status

Once the automatic flow control modes are invoked by the host, all actions will be transparent to the host. If receipt of flow control characters by the host is not desired, the Flow Control Transparency bit of COR3 may be set to cause the CD180 not to pass received flow control characters onto the host. If TxIBE is set, the CD180 will implement the flow control function on the transmitter regardless of the FCT mode. The host can review the status of the channel by reading the Channel Control Status Register.

If flow control status is needed by the host, the SCDE and RxSC control bits must be set and the FCT bit must not be set. A special character detect status and the special character will be presented to the host by a Receive Exception interrupt.

3.10 Counter / Timer Functions

Each of the CD180's channels has two associated timers. The CD180 uses one of these, the "receive FIFO " timer to generate "Receive Data" interrupt requests and "Receive Exception Timeout " interrupt during an interruption in data flow to the CD180 from a remote device. The generation of a Receive Exception Timeout interrupt can be disabled by clearing the RET bit in the Interrupt Enable Register.

Each time the CD180 moves a character into a channel's receive FIFO, it resets the channel's receive FIFO timer to the value contained in the channel's Receive Timeout Period Register (RTPR). If the timer expires before new data arrives, the Receive Data interrupt will be asserted for the channel if the RxData Interrupt Enable Register (IER) bit is set . The receive timeout is also started following the transfer of the last byte of data from the channel to the host. If the timer timeouts before new data arrives, a Receive Exception interrupt is given with the Timeout Exception status set. There is no data character associated with the Timeout Exception status.

If enough data arrives to fill the RxFIFO to the level set by the RxTh bits in COR3, or if a special character arrives in the RxFIFO and the RxSC bit of IER is set, the channel will assert the Receive Data interrupt request without waiting for the timer to expire.

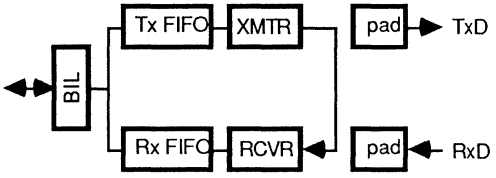
The CD180 uses the "Transmit timer" to generate real-time delays between characters in the output data stream. It is also used to extend the duration of a Line Break transmit condition when the delay is inserted between the Start Break and Stop Break embedded transmit commands. All of the timers count "ticks" determined by the prescaler counter. The two 8-bit Prescaler Period Registers (PPRH and PPRL) determine the real-time length of a "tick". A "tick" is the period of the CD180's system clock input (CLK) multiplied by the PPR contents.

The user embeds an escape sequence into the output data stream to generate real-time delays between output characters and to hold the TxD output in BREAK (space) condition for a timed period. When the CD180 encounters such an escape sequence, it sets the transmit timer to the value contained in the escape sequence. When the timer expires, the CD180 loads the next character into the transmit shift register and resumes output (unless the next character begins another escape sequence). The escape sequence for an inserted delay consists of three characters: "00", "82h" and "tt". "tt" is the timeout value. The Embedded Transmit Command (ETC) control bit in COR2 must be set to enable these functions. If the host must transmit an ETC escape character as data, the ETC mode must be disabled or the escape character must be "escaped" (ESC ESC).

3.11 Diagnostic Functions

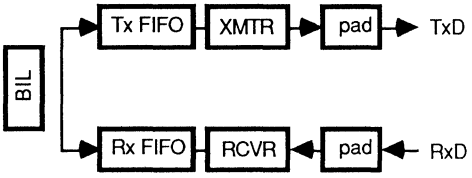
Two channel modes are provided by the CD180 in addition to the normal mode of independent transmitter and receiver operation. The channel modes are selected by programming the LLM (Local Loopback Mode) or the RLM(Remote Loopback Mode) bits in Channel Option Register 2.

Local Loopback Mode



Local Loopback mode is invoked by setting the LLM bit in the Channel Option Register 2 (COR2). When in this mode, the channels TxD output is internally looped back to the channel's RxD input, and the channel's TxD output pin is held in the "mark" condition. However, all other channel parameters and interrupt functions continue to work independently and normally. Receiver special character recognition, overflow handling etc may also be tested by using the local loopback mode and transmitting appropriate character sequences.

Remote Loopback



Remote Loopback mode is invoked by setting the RLM bit in the Channel Option Register 2 (COR2). When in this mode, the CD180 will echo the received data to the transmitter for transmission back to the sender. The received data will not be passed on to the host. The character will be transmit with parity and stop bit options as defined in COR1. Note that a mismatch of receive baud rate and transmit baud rate can cause overrun and loss of echoed characters.

4. REGISTER DESCRIPTIONS

The CD180 contains two types of registers - Global and Channel registers. Global registers contain information common to all channels, and are used mostly for interrupt handling.

Channel registers contain information that is specific for a channel. Each channel can be operated independently of the other channels. When not in interrupt service, channel registers can be accessed by first writing the number of the channel to be accessed into the Channel Access Register. The channel number in the CAR is used by the CD180 as part of the channel register address.

4.1 Global Registers

Global registers are registers which provide a function common to all channels. Most global registers are used to support interrupt searching of the channels. During interrupt service, the CD180 supplies the channel number of the interrupting channel as part of the interrupt context. The CAR is not used for channel register access in interrupt service routines.

GIVR - Global Interrupt Vector Register (1 0 0 0000) - Read / Write

7	6	5	4	3	2	1	0
X	X	X	X	X	IT2	IT 1	IT0

Bits 7-3 Bits written by the CPU for interrupt handling purpose. These 5 bits may be used as the CD180's chip ID number.

Bits 2-0 Interrupt type 2-0. These three bits indicate the group/type of interrupt occurring.

IT2	IT1	IT0	Group/Type
0	0	0	Not used
0	0	1	Group 1: Modem Signal Change Interrupt
0	1	0	Group 2: Transmit Data Interrupt
0	1	1	Group 3: Receive Good Data Interrupt
1	0	0	Not used
1	0	1	Not used
1	1	0	Not used
1	1	1	Group 3: Receive Exception Interrupt

Global Interrupting Channel Register (GICR) (1 0 0 0001) - Read/Write

7							0
X	X	X	C2	C1	C0	X	X

This Global register contains the channel number of the interrupting channel being served. The channel number is always that of the current acknowledged interrupt. If no interrupt is acknowledged, the channel number is undefined.

Bit 7-5 User Defined

Bit 4-2 Defines the interrupting channel number

C2	C1	C0	Channel #
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

Bit 1-0 User Defined

Priority Interrupt Level Register 1 (PILR1) (1 1 0 0001) - Read/Write

7	6	0
1	Binary Value	

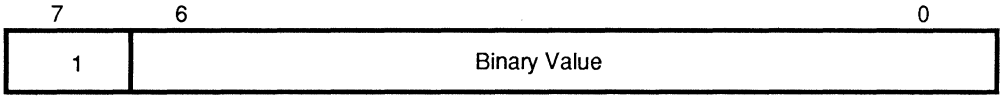
This register contains the Priority Interrupt Level code for Group 1 Modem Signal Change Interrupts that will be presented on the address bus A[0:6] by the host to indicate which interrupt type is being acknowledged when IACKIN* is asserted. Bit 7 must be programmed to a "1" . The CD180 compares all eight bits internally. The 7-bit PIL code is compared with the address bus. Bit 6 of the register is compared to bit 6 of the address bus etc. Bit 7 of the register is compared with a logic "1".

Priority Interrupt Level Register 2 (PILR2) (1 1 0 0010) - Read/Write

7	6	0
1	Binary Value	

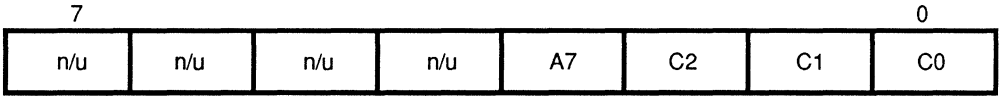
This register must contain the code for Group 2 Transmit Data Interrupt that will be presented on the address bus by the host to indicate which interrupt type is being acknowledged by the host when the IACKIN* is asserted. Bit 7 must be programmed to a "1". The CD180 compares all eight bits internally. The 7-bit PIL code is compared with the address bus. Bit 6 of the register is compared to bit 6 of the address bus etc. Bit 7 of the register is compared with a logic "1".

Priority Interrupt Level Register 3 (PILR3) (1 1 0 0011) - Read/Write



This register must contain the code for Group 3 Receive Data Interrupt that will be presented on the address bus by the host to indicate which interrupt type is being acknowledged by the host when the IACKIN* is asserted. Bit 7 must be programmed to a "1". The CD180 compares all eight bits internally. The 7-bit PIL code is compared with the address bus. Bit 6 of the register is compared to bit 6 of the address bus etc. Bit 7 of the register is compared with a logic "1".

Channel Access Register (CAR) (1 1 0 0100) - Read / Write



This register contains the channel number used for channel oriented host read or write operations when the host is not in an interrupt service routine. The CD180 supplies the interrupting channel number during all interrupt service operations. The Channel Access Register contents are not used during interrupt service. Note that this means that an interrupt service routine is restricted to accessing only the register set of the interrupting channel and global registers.

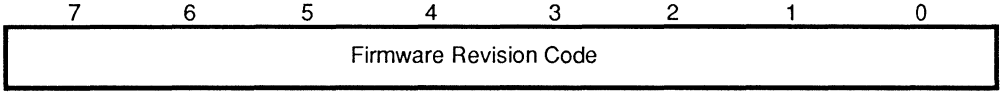
Bit 7-4 Not Used

Bit 3 Address Bit 7. This bit completes the external to internal CD180 register address mapping and is used for test purposes. In normal user operation, this bit should always be zero.

Bit 2-0 Channel Number

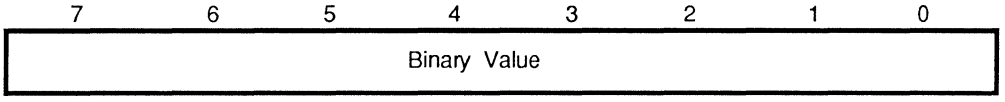
C2	C1	C0	Channel Number
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

GFRCR - Global Firmware Revision Code Register (1 1 0 1011) - Read Only

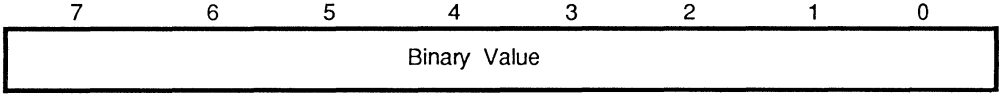


This register is initialized by the CD180's firmware during the power on reset initialization routine to contain the current firmware version code for the CD180.

Prescaler Period Register High (PPRH) (1 1 1 0000) - Read/Write



Prescaler Period Register Low (PPRL) (1 1 1 0001) - Read/Write



These two registers provide the initialization value for the timer prescaler which is clocked by the system clock. This establishes the clock for the various on-chip timers.

The value loaded into these registers should establish a clock period of at least 0.1 ms. The values of these registers will be programmed to be FFh automatically upon a hardware reset.

Virtual Registers

Certain registers in the Global register file are specially designed to facilitate interrupt handling. These registers do not exist as distinct registers and can be considered to be "Virtual Registers". These registers provide functions which are valid only during interrupt service routines and must not be accessed at other times.

The CD180 maintains all channel specific information. During data transfer between the host and the CD180, the CD180 uses a context switching technique to switch the proper channel specific information into the Global registers for use by the host.

Receive Data Register (RDR) (1 1 1 1000) - Read only

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This register accesses the receive data FIFO for the channel. This register is used for all channels to transfer receive FIFO data to the host. Successive reads transfer successive bytes from the FIFO to the host. Reading this register increments an internal pointer to the data and status FIFOs. If both the RCSR and RDR are to be read, the RCSR must be read first.

Receive Character Status Register (RCSR) (1 1 1 1010) - Read only

7	6	5	4	3	2	1	0
Timeout	SC Det2	SC Det1	SC Det0	Break	PE	FE	OE

When this register is read, the receive character status FIFO entry corresponding to the current receive data FIFO character is read.

Bits 7 — Timeout - indicates that the Rx FIFO is empty and no data has been received within the receive timeout period. There is no data character associated with this status and no other status bits are valid if Timeout bit is set.

Bit 6-4 — Special Character Detect

SC Det2	SC Det1	SC Det0	Status
0	0	0	None Detected
0	0	1	Special Character 1 matched or Special Character 1 & 3 sequence matched
0	1	0	Special Character 2 matched or Special Character 2 & 4 sequence matched
0	1	1	Special Character 3 (only if Special Character 1 & 3 sequence is not enabled)
1	0	0	Special Character 4 (only if Special Character 2 & 4 sequence is not enabled)

Note: no special character match is performed if PE or FE = 1. The second character of a 2-character sequence cannot cause a receiver overrun.

Bit 3 — Break - indicates that a Break has been detected

Bit 2 — Parity Error - indicates that a parity error has occurred

Bit 1 — Framing Error- indicates that a bad stop bit has been detected

Bit 0 — Overrun Error - indicates that new data has arrived but the CD180's FIFO and holding registers are full. The new data is lost and the overrun indication is flagged on the last character received before the overrun occurred.

Transmit Data Register (TDR) (1 1 1 1011) - Write only

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

When servicing a Transmit Data Interrupt, the Transmit Data Register accesses the transmit FIFO of the interrupting channel. Data is written into the Transmit Data Register by the host and the CD180 will write into the interrupting channel's transmit character FIFO. Up to eight (8) bytes of data may be written into the TDR during transmit data interrupt.

End of Interrupt Register (EOIR) (1 1 1 1111) - Write only

7							0
n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u

This is a dummy register. This register must be written to by each interrupt service subroutine to signal to the CD180 that the current interrupt service is concluded. This must be the last access to the CD180 during an interrupt service routine. Writing to this register will generate an internal End of Interrupt signal which pops the CD180's interrupt context stack.

4.2 Channel Registers

The following registers are duplicated for each channel. These registers define the operating parameters, modes, data and status for each channel.

Channel Command Register (CCR) - (0 0 0 0001) - Read / Write

The Channel Command Register must only be written to when its content is already zero. When the CD180 processes a command, it will clear the command bits as a signal to the host that it is ready to accept another channel command. All eight Channel Command registers are independent.

7							0
RESET CHAN	COR CHNG	SEND SP CH	CHAN CTL	D3	D2	D1	D0

Bits 7-4 specifies the commands. A different set of D3-D0 bits are associated with each of the commands to further specify the mode of operation.

a) Reset Channel Command

7							0
Reset Chan	0	0	0	0	0	0	Type

This is a software reset command. When this command is issued, the CD180 disable the transmitter and receiver and clear the data and status FIFOs of the channel. Channel parameters will not be affected by a Channel Reset (Type = 0).

Bit 7 Reset Channel Command, must be "1"

Bits 6-1 Not Used. Must be zero

Bit 0 Reset Type - If the Reset Type bit is zero, a software reset of the channel is performed. The transmitter and receiver are disabled and all FIFOs are cleared(flushed). If the Reset Type bit is a one, an on-chip firmware initialization of ALL CHANNELS is performed. All channel and global parameters are reset to their power on reset condition.

b) Channel Option Register Change Command

7							0
0	COR CHG	0	0	COR3	COR2	COR1	n/u

Changes made to Channel Option Registers must be signalled to the CD180 by this command. Any combination of COR changes may be indicated by one command.

Bit 7 Must be zero

Bit 6 Channel Option Register Change Command, must be "1"

Bit 5,4 Must be zero

Bit 3 Channel Option Register 3 changed

Bit 2 Channel Option Register 2 changed

Bit 1 Channel Option Register 1 changed

Bit 0 Not Used

c) Send Special Character(s) Command

7							0
0	0	SEND SP CH	0	0	SSPC2	SSPC1	SSPC0

Bit 7,6 Must be zero

Bit 5 Send Special Character(s) Command, must be "1"

Bit 4-3 Must be zero

Bit 2-0 Special Character Select

SSPC2	SSPC1	SSPC0	Function
0	0	0	Not Used
0	0	1	Send Special Character #1 or characters 1&3 in sequence if COR3 [XonCH] defines a two-character sequence
0	1	0	Send Special Character #2 or characters 2&4 in sequence if COR3 [XoffCH] defines a two-character sequence
0	1	1	Send Special Character 3
1	0	0	Send Special Character 4
1	0	1	Not Used
1	1	0	Not Used
1	1	1	Not Used

d) Channel Control Command

7							0
0	0	0	CHAN CTL	XMTR EN	XMTR DIS	RCVR EN	RCVR DIS

Bit 7 -5 Must be zero

Bit 4 Channel Control Command, must be "1"

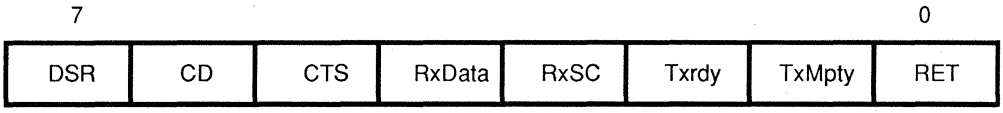
Bit 3 Transmitter Enable

Bit 2 Transmitter Disable

Bit 1 Receiver Enable

Bit 0 Receiver Disable

Interrupt Enable Register (IER) (0 0 0 0010) - Read / Write



A logic "1" in each bit position enables the interrupt generation for the associated cause.

Bit 7 DSR - Enable Data Set Ready Interrupt. When enabled, generates a modem change interrupt on the selected level(s) change of the DSR input.

Bit 6 CD - Enable Carrier Detect Interrupt. When enabled, generates a modem change interrupt on the selected level(s) change of the CD input.

Bit 5 CTS - Enable Clear -To-Send Interrupt. When enabled, generates a modem change interrupt on the selected level(s) change of the CTS input.

Bit 4 RxData - Enable Receive Data Interrupt. When enabled, the receive data interrupt is generated for received data and data exceptions.

Bit 3 RxSC - Enable Receive Special Character Interrupt. When enabled, the receive data exception interrupt is generated when received character(s) matches one of the four user defined special characters.

Bit 2 TxRdy - Transmit Ready. When enabled, the transmitter will generate an interrupt when the transmit FIFO becomes empty.

Bit 1 TxMpty - Transmitter Empty. When enabled, an interrupt is generated when the transmit FIFO, the transmit holding register and the transmit shift register are all empty.

Bit 0 RET - Receive Exception Timeout Interrupt Enable. When enabled, a receive exception interrupt is generated following transfer of all data from CD180 to host. The RET interrupt follows the data transfer by a delay equal to the Receive Timeout Period.

Channel Option Register 1 (COR1) (0 0 0 0011) - Read / Write

7	6	5	4	3	2	1	0
Parity	ParM1	ParM0	Ignore	Stop 1	Stop 0	CHL1	CHL0

Bit 7 Parity - "1" = odd parity
"0" = even parity

Bit 6,5 Parity Mode 1 & 0 - Defines parity mode for both transmitter and receiver:

ParM1	ParM0	Parity
0	0	no parity
0	1	force parity (odd parity = force 1, even = force 0)
1	0	normal parity
1	1	not used

Bit 4 Ignore - Ignore Parity
0 = evaluate parity on received characters
1 = do not evaluate parity on received characters

Bit 3, 2 Stop Bit Length - Specifies the length of the STOP bit

Stop1	Stop0	Stop bit
0	0	1 stop bit
0	1	1 1/2 stop bits
1	0	2 stop bits
1	1	not used (2 1/2 stop bits)

Bit 1,0 Character Length

CHL1	CHL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Channel Option Register 2 (COR2) (0 0 0 0100) - Read / Write

7							0
IXM	TxIBE	ETC	LLM	RLM	RtsAO	CtsAE	DsrAE

Bit 7 Implied Xon Mode This bit only has meaning when in the automatic Transmit In-Band flow control mode. During Transmit In-Band flow control mode, the CD180 stops transmission upon detection of an Xoff character or character sequence. The IXM bit determines whether the CD180 should restart transmission based on receipt of an Xon character or any character.

When IXM is set, the CD180 will restart transmission upon detection of any character. When IXM bit is not set, the CD180 will wait for the Xon character to restart the transmission.

Bit 6 Enable Automatic Transmit In-Band (Xon/Xoff) Flow Control. The CD180 is in the transmitting mode and is being flow controlled by the remote. The CD180 , upon receipt of the Xoff character, will terminate transmission after the current character in the transmit shift register and the character in the transmit holding register are sent. The CD180 will resume transmission upon receipt of the Xon character, or any character, depending on the state of the IXM bit.

Bit 5 Embedded Transmitter Command Enable. If set, the embedded special transmitter command functions are enabled. (See section 3.6 for detailed description)

Bit 4 Local Loopback Mode.

"1" enables the local loopback mode
"0" disables the local loopback mode

Bit 3 Remote Loopback Mode

"1" enables the remote loopback mode
"0" disables the remote loopback mode

Bit 2 RTS Automatic Output Enable. When set, if the channel is enabled, the CD180 will automatically assert the RTS* output when it has characters to send. If CtsAE is also set, it will wait for CTS* to respond prior to transmission.

Bit 1 CTS Automatic Enable. Enables CTS* input to be used as automatic transmitter enable or disable.

Bit 0 DSR Automatic Enable. Enable the DSR* input as automatic receiver enable/disable

Channel Option Register 3 (COR3) (0 0 0 0101) - Read / Write

7							0
Xon CH	Xoff CH	FCT	SCDE	RxTH3	RxTH2	RxTH1	RxTH0

Bit 7 Xon Character Definition
0 = Xon Character is a single character code and is defined by Special Character 1
1 = Xon Character is a double character sequence and is defined by Special characters 1 & 3

Bit 6 Xoff Character Definition
0 = Xoff Character is a single character code and is defined by Special Character 2
1 = Xoff Character is a double character sequence and is defined by Special characters 2 & 4

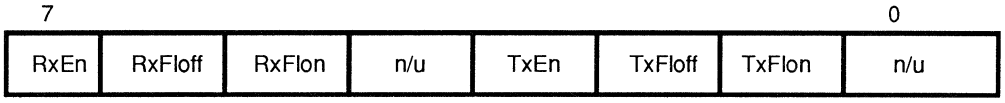
Bit 5 FCT-Flow Control Transparency Mode
0 = Flow control characters received will be given to the host by receive exception interrupts.
1 = Flow control characters received will not be given to the host by receive exception interrupts.

Bit 4 Special Character Detection Enable
0 = Special character status detection is disabled
1 = Special character status detection is enabled

Bit 3-0 RxFIFO Threshold

RxTh3	RxTh2	RxTh1	RxTH0	
0	0	0	0	Not Used
0	0	0	1	1 character
0	0	1	0	2 characters
0	0	1	1	3 characters
0	1	0	0	4 characters
0	1	0	1	5 characters
0	1	1	0	6 characters
0	1	1	1	7 characters
1	0	0	0	8 characters
1001 to 1111				Not used

Channel Control Status Register (CCSR) (0 0 0 0110) - Read only



This status register stores the current state of the channel. It may be read by the host at any time. If the host determines that a flow control state is inappropriate, it may be cleared by enabling or disabling the transmitter or receiver by CCR command.

Bit 7 Receiver Enable
0 = Receiver is disabled
1 = Receiver is enabled

Bit 6 Receive Flow Off
0 = Normal
1 = The CD180 has requested the remote to stop transmission (Send Xoff command has been given to the channel). This bit will be reset when the CD180 has requested the remote to restart transmission or when the receiver is enabled or disabled or the channel is reset.

Bit 5 Receive Flow On
0 = Normal
1 = CD180 has requested the remote to restart character transmission (Send Xon command has been given to the channel). This bit is reset when the next (non-flow control) character is received or when the receiver is enabled or disabled or the channel is reset.

Bit 4 Not Used

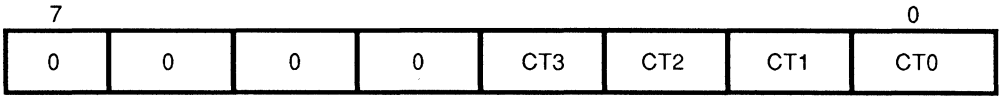
Bit 3 Transmitter Enable
0 = Transmitter is disabled
1 = Transmitter is enabled

Bit 2 Transmit Flow Off
0 = normal
1 = The CD180 has been requested by the remote to stop transmission. This bit is reset when the CD180 receives a request to resume transmission or when the transmitter is enabled or disabled or the channel is reset.

Bit 1 Transmit Flow On
0 = Normal
1 = CD180 has been requested by the remote to resume transmission. This bit is reset once character transmission is resumed or when the transmitter is enabled or disabled or the channel is reset.

Bit 0 Not Used.

Receive Data Count Register (RDCR) (0 0 0 0111) - Read only

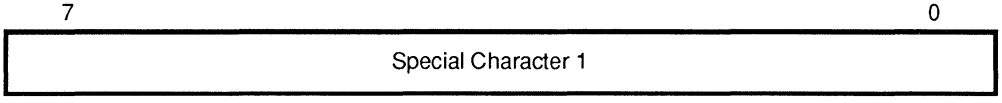


Bit 7-4 Zero

Bits 3-0 Specifies the number of good data bytes for transfer from the RxFIFO at the time of interrupt

CT3	CT2	CT1	CT0	#Good Bytes
0	0	0	0	Not used
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	0	Not used
1	0	0	1	Not used
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

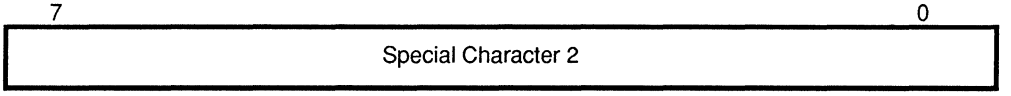
Special Character Register 1 (SCHR1) (0 0 0 1001) - Read / Write



This register stores the right justified bit pattern for Special Character one. Unused bits must be zero. During receive, this character is one of the four characters compared with the received data for special character recognition. If a match occurs with one of these four characters, it is noted in the receiver status FIFO entry accompanying the received character unless a double character compare is enabled. In this case, the receive status FIFO entry will not be made until both characters are compared.

Special character one defines the Xon character or the first half of the Xon character sequence.

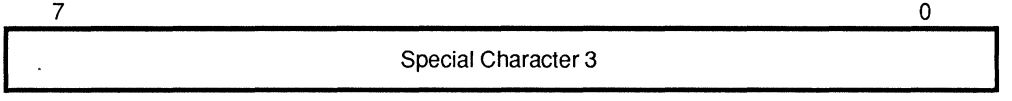
Special Character Register 2 (SCHR2) (0 0 0 1010) - Read / Write



This register stores the right justified bit pattern for Special Character two. Unused bits must be zero. During receive, this character is one of the four characters compared with the received data for special character recognition . If a match occurs with one of these four characters, it is noted in the receiver status FIFO entry accompanying the received character unless a double character compare is enabled. In this case, the receive status FIFO entry will not be made until both characters are compared.

Special character two defines the Xoff character or the first half of the Xoff character sequence.

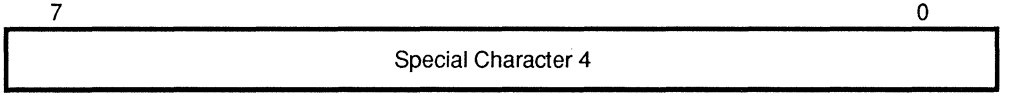
Special Character Register 3 (SCHR3) (0 0 0 1011) - Read / Write



This register stores the right justified bit pattern for Special Character three. Unused bits must be zero. During receive, this character is one of the four characters compared with the received data for special character recognition. If a match occurs with one of these four characters, it is noted in the receiver status FIFO entry accompanying the received character unless a double character compare is enabled. In this case, the receive status FIFO entry will not be made until both characters are compared.

Special character 3 may be the second half of the Xon character sequence.

Special Character Register 4 (SCHR4) (0 0 0 1100) - Read / Write



This register stores the right justified bit pattern for Special Character four. Unused bits must be zero. During receive, this character is one of the four characters compared with the received data for special character recognition. If a match occurs with one of these four characters, it is noted in the receiver status FIFO entry accompanying the received character unless a double character compare is enabled. In this case, the receive status FIFO entry will not be made until both characters are compared.

Special character four may be the second half of the Xoff character sequence.

Modem Change Option Register 1 (MCOR1) (0 0 1 0000) - Read / Write

7							0
DSRzd	CDzd	CTSzd	0	DTRth3	DTRth2	DTRth1	DTRth0

This register is used to define the current state change options to be monitored.

Bit 7 DSRzd = 1
Detect one to zero transition on DSR* input (zero to one transition of DSR (MSVR) bit)

Bit 6 CDzd = 1
Detect one to zero transition on CD* input (zero to one transition of CD (MSVR) bit)

Bit 5 CTSzd = 1
Detect one to zero transition on CTS* input (zero to one transition of CTS (MSVR) bit)

Bits 4 Must be zero

Bits 3-0 Automatic DRT flow control theshold

DTRth3	DTRth2	DTRth1	DTRth0	
0	0	0	0	Automatic DTR mode disabled
0	0	0	0	1 character
0	0	1	0	2 characters
0	0	1	1	3 characters
0	1	0	0	4 characters
0	1	0	1	5 characters
0	1	1	0	6 characters
0	1	1	1	7 characters
1	0	0	0	8 characters
1001 to 1111				not used

Note: The DTR feature is available only in Revision 'B' and later CD180s.

Modem Change Option Register 2 (MCOR2) (0 0 1 0001) - Read / Write

7							0
DSRod	CDod	CTSod	0	0	0	0	0

This register is used to define the current state change options to be monitored

Bit 7 DSRod = 1
Detect zero to one transition on DSR* input (one to zero transition DSR (MSVR) bit)

Bit 6 CDod = 1
Detect zero to one transition on CD* input (one to zero transition of CD (MSVR) bit)

Bit 5 CTSod = 1

Detect zero to one transition on CTS* input (one to zero transition of CTS (MSVR) bit)

Bits 4-0 Must be zero

Modem Change Register (MCR) (0 0 1 0010) - Read / Write

7							0
DSR chg	CDchg	CTSchg	0	0	0	0	0

Bits are set by recognition of a level change as programmed by the Modem Change Option Registers. Changes detected will be cause for asserting the Modem Interrupt if corresponding interrupt enable bits are set. Once the interrupt is asserted, updates to this register are inhibited until End of Interrupt Register (EOIR) is written at the end of the modem interrupt service routine. The host must clear these register bits during the service routine.

Bit 7 DSR Changed
A logic "1" denotes that the Data Set Ready input has changed state

Bit 6 CD changed
A logic "1" denotes that the Carrier Detect input has changed state

Bit 5 CTS changed
A logic "1" denotes that the Clear to Send input has changed state

Bits 4-1 Must be zero

Receive Timeout Period Register (RTPR) (0 0 1 1000) - Read / Write

7	0
Receiver Data Timeout Period	

This value sets the receive data timeout period. As each character is moved to the received FIFO or the last data is transferred from the FIFO to the host, the Receive Timer (an internal timer) is reloaded with the Receive Data Timeout Period. The Receive Timer is decremented on each "tick of the prescaler counter. If the Receive Timer reaches zero, it is cause for a receive data interrupt.

Modem Signal Value register (MSVR) (0 1 01000) - Read / Write

7							0
DSR	CD	CTS	n/u	n/u	n/u	DTR	RTS

This register is read to determine the current input levels on the input modem pins. It is written to supply an output value for the RTS and DTR pins. The CD and DTR functions are mutually exclusive options and are selected for all channels by the DSRSEL input.

NOTE: The register bits have the opposite polarities from the actual states on the individual pins.

The pin functions are active low, the register values are active high (positive true).

Bit 7 DSR - Current state of Data Set Ready input

Bit 6 CD - Current state of Carrier Detect input

Bit 5 CTS - Current state of Clear to Send input

Bits 4-2 Not Used

Bit 1 DTR - Current state of Data Terminal Ready output

Bit 0 RTS - Current state of Request-to-Send output

Receive Baud Rate Period Register High (RBPRH) (0 1 1 0001) - Read / Write

7	0
Receiver Baud Rate Divisor High Byte	

Receive Baud Rate Period Register Low (RBPRL) (0 1 1 0010) - Read / Write

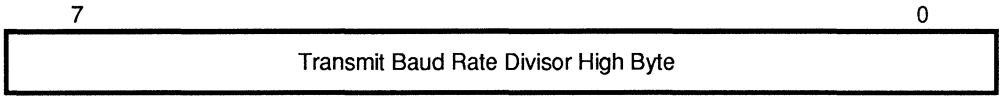
7	0
Receiver Baud Rate Divisor Low Byte	

These two registers contain the 16 bit preload value for the receive baud rate counter. This count establishes the basic receiver clock rate which must be the 16x the desired receiver baud rate.

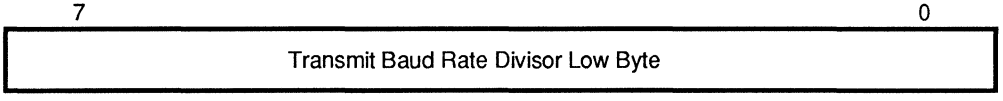
These registers are reset to zero by RESET*.

The period established for the 16x receiver clock rate is the RBPR 16 bit binary value times the system clock (CLK) period.

Transmit Baud Rate Period Register High (TBPRH) (0 1 1 1001) - Read / Write



Transmit Baud Rate Period Register Low (TBPRL) (0 1 1 1010) - Read / Write



These two registers contain the 16 bit preload value for the transmit baud rate counter . This count establishes the transmitter clock rate which must be 16x the desired transmitter baud rate.

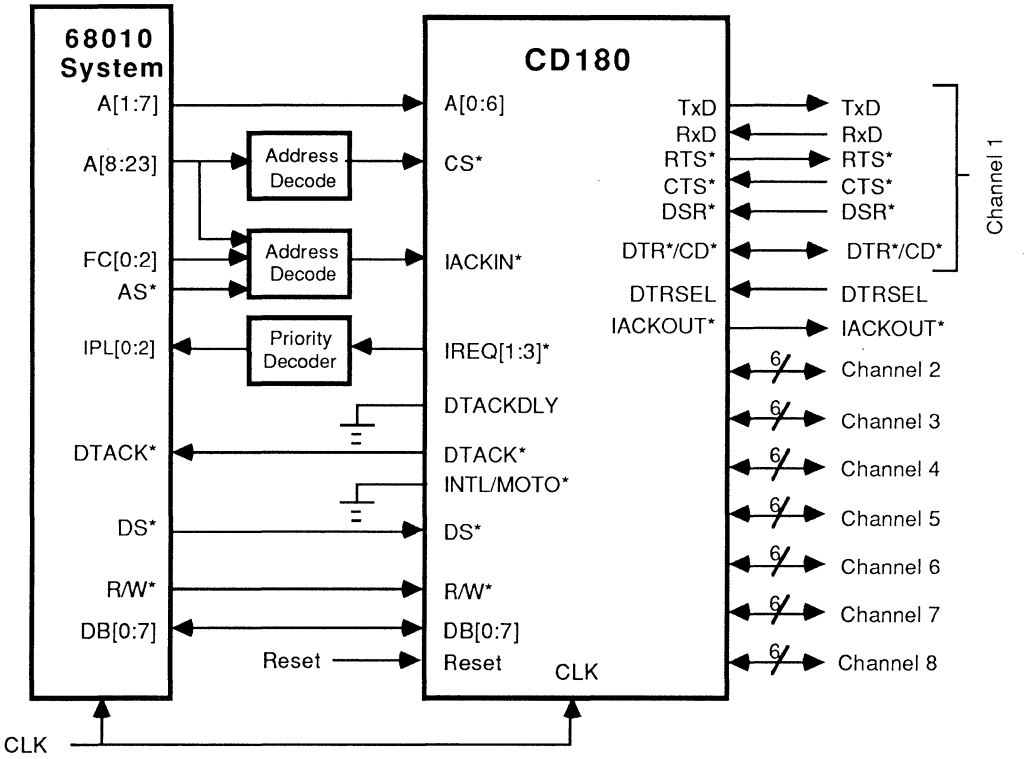
The precise period established for the 16x transmitter clock is equal to the RBPR 16-bit binary value times the system clock (CLK) period.

These registers are reset to zero by RESET*.

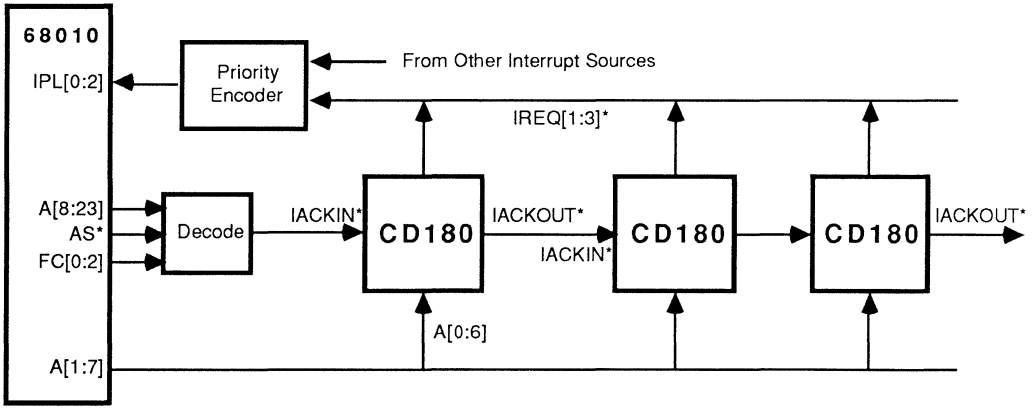
5. SYSTEM CONFIGURATIONS

5.1 68010-Based

68010-Based Single-CD180 System Configuration

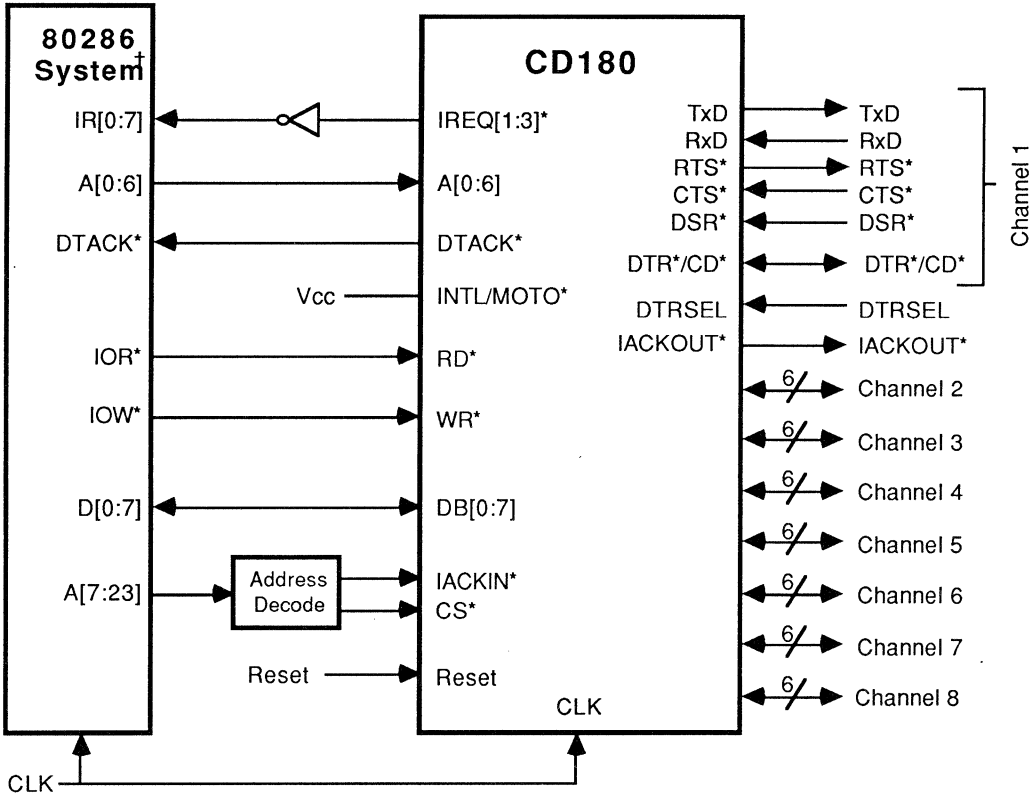


68010-Based Multi-CD180 System Configuration

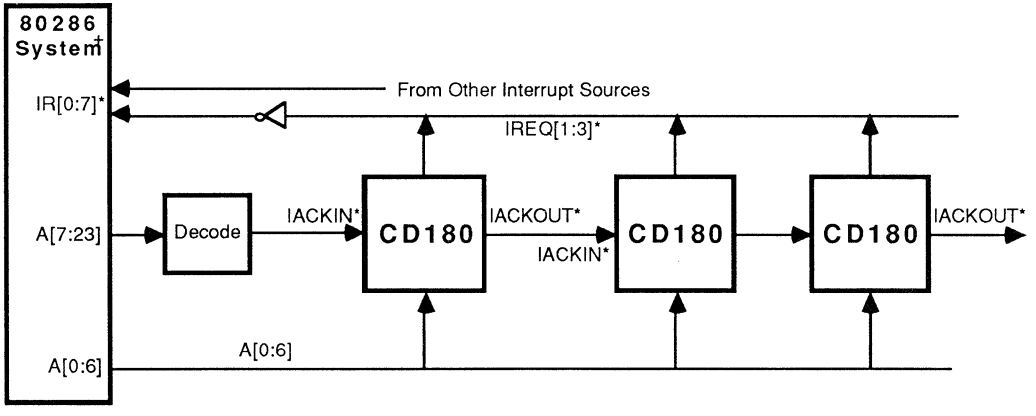


5.2 80286-Based

80286-Based Single-CD180 System Configuration



80286-Based Multi-CD180 System Configuration



†Note: For these purposes, the 80286 System consists of the 80286, 82284, 82288, and 8259A.

6. Electrical Specifications

6.1 Absolute Maximum Ratings

Operating Ambient Temperature ..... 0°C to 70°C
Storage Temperature ..... -65°C to 150°C
All voltages, with respect to ground ..... -0.5 to Vcc +0.5 Volts
Supply voltage (Vcc) ..... +7.0 Volts
Power Dissipation ..... 0.75 Watt

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Electrical Characteristics

(@ V_{cc}=5V± 5%, T_A =0°C to 70°C)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{cc}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 10 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 10 mA
I_{IL}	Input Leakage Current	-10	10	µA	$0 < V_{in} < V_{cc}$
I_{LL}	Data Bus 3-state Leakage current	-10	10	µA	$0 < V_{out} < V_{cc}$
I_{OC}	Open Drain Output Leakage	-10	10	µA	$0 < V_{out} < V_{cc}$
I_{CC}	Power Supply Current		100	mA	CLK = 9.830 Mhz
C_{in}	Input Capacitance		10	pF	
C_{out}	Output Capacitance		10	pF	

6.3 AC Electrical Specification

(@Vcc = 5V±5%, TA = 0°C to 70°C. Unless otherwise noted, all input transition times ≤ 10 ns)

General Timing Characteristics

The CL-CD180 is a static, unclocked (i.e., asynchronous) interface. Except for RESET*, no signal is referenced to the clock. In general, bus cycles may be as long as desired.

No.	Fig.	Parameters	Min	Max	Units
1	1	Reset Low Pulse Width	5		Tclk
15	1	Clock Period	100	125	ns
16	1	Clock Width Low	45		ns
17	1	Clock Width High	45		ns
18	1	Clock Transition Time		5	ns

The INTL/MOT* control pin affects the nomenclature and active level of two input pins, but does not alter the AC characteristics. In the timing tables, these pins are referred to by the "MOT" name, with the "INTL" equivalent in square brackets [].

		INTL/MOT*=0	INTL/MOT*=1
DS*[RD*]	pin 74	DS*	RD*
R/W*[WR*]	pin 75	R/W*	WR*

General Timing Characteristics *(cont.)*

The INTL/MOT* pin is intended to be permanently strapped high or low. If it is changed after the start of the RESET* low interval, operation of the CL-CD180 is unpredictable and not guaranteed. When the CD180 is operated in "INTL" mode, RD* and WR* should never be low at the same time.

Timing Characteristics

No.	Figs.	Parameters	Min	Max	Units	Notes
2	2,4,5,7	Address Setup Time to CS* or DS* [RD*]	5		ns	1
3	2,3,4	R/W* Setup Time to CS* or DS* [RD*]	0		ns	1
4	2-7	Address Hold Time after CS*	0		ns	3
5	2,3,4,6	R/W* Hold Time after CS* and DS* [RD*]	0		ns	3
6	2,3,5,6	DTACK* Low to Valid Read Data				
		(if DTACKDLY=0)		50	ns	
		(if DTACKDLY=1)		10	ns	
7	2-7	DTACK* Low from CS* or DS* [RD*] (@10 Mhz)		210	ns	1,2
8	2,3,5,6	Read Data Hold Time after CS* and DS* [RD*], high		40	ns	3
9	2-7	CS* or DS* [RD*] high from DTACK*, low	50		ns	10
10	2-7	DTACK* Hi-Z from (CS* or IACKIN*) or DS*, high		40	ns	3
11	2-7	DS* [RD*] High Pulse Width	25		ns	
12	3,6	Address Setup Time to IACKIN*	10		ns	
13	3,4,7	Write Data Valid to DS* [or WR*] Low	10		ns	
14	3,4,7	Write Data Hold Time After DS* [or WR*] High	10		ns	
19	3,6	IREQ(x)* Negation after DTACK* Assertion		2Tclk+50	ns	
20	3,6	R/W* [WR*], CS* to DS* [RD*] setup time	0		ns	11
21	4,7	IREQ(x)* Assertion delay after write to EOIR		2Tclk	ns	12
22	3,6	IACKIN* to IACKOUT* propagation delay				

Notes on timing:

1. During read cycles, CS* and DS* (or RD*) are gated together internally. This specification is with respect to whichever goes active (low) last.
2. The value given is for 10-Mhz operation and DTACKDLY=0. This time depends on system clock rate and the chosen DTACKDLY option. The actual time in any case can be determined from the formula:

   If DTACKDLY=0 **1.5(Tclk) + 60 ns**
   If DTACKDLY=1 **2.0(Tclk) + 60 ns**

3. During read cycles, CS* and DS* (or RD*) are gated together internally. This specification is with respect to whichever goes inactive (high) first.
4. During Interrupt Acknowledge Cycles, IACKIN* is asserted instead of CS*; CS* should remain high. Please note that IACKIN* timing is not always the same as CS*.
5. During Interrupt Acknowledge Cycles, IACKIN* is gated together with DS* (or RD*) to control activity on the data bus, in a manner analagous to ordinary read cycles. However, Address Setup to IACKIN* is not dependent on DS* (or RD*) timing.
6. This specification is with respect to IACKIN* only.
7. This specification is with respect to whichever of IACKIN* and DS* (or RD*) goes active (low) last.
8. This specification is with respect to whichever goes inactive (high) first.
9. In multiple CD180 designs, the Interrupt Acknowledge Cycle must be long enough to accomodate the IACKIN*/IACKOUT* daisy chain propagation delay. IACKIN* should remain low until after DTACK* asserts as specified.

Notes on timing *(cont.)*:

10. For Interrupt Acknowledge cycles, this specification refers to IACKIN* instead of CS*.
11. This specification is with respect to DS*. CS* and R/W* must be high before the assertion of DS* to avoid the possibility that the CD180 will interpret the cycle as a read or write cycle, rather than an interrupt acknowledge cycle.
12. This is the time required to re-assert IREQ(x)* if the internal conditions of the CD180 are such that IREQ(x) should be asserted.

CD180 Timing Waveforms

Clock/Reset

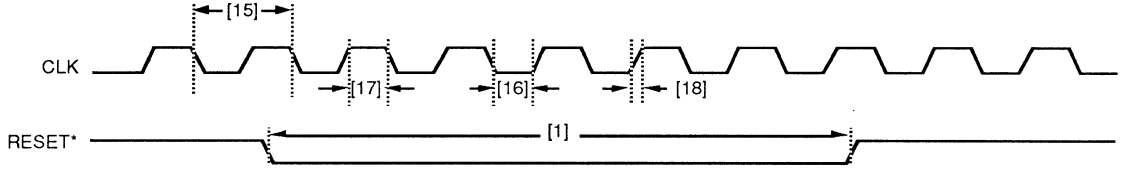


Figure 1

Motorola Read Cycle

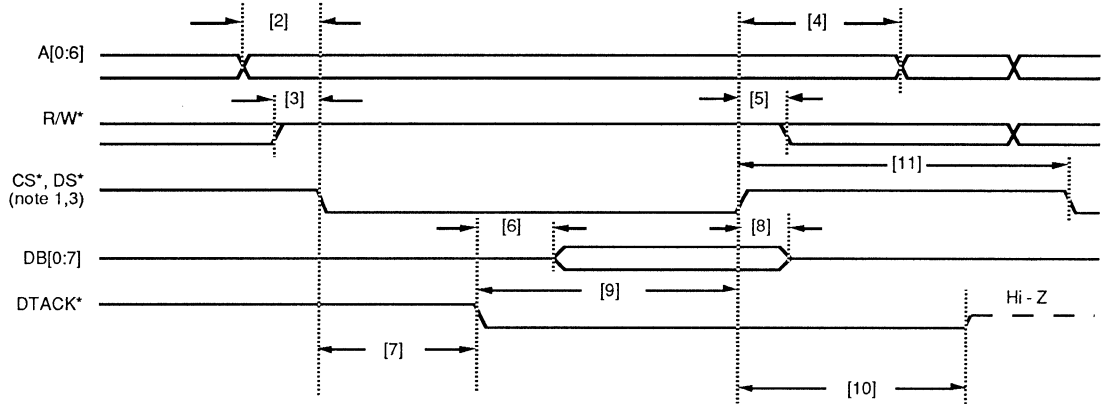


Figure 2

Motorola Interrupt Acknowledge Cycle

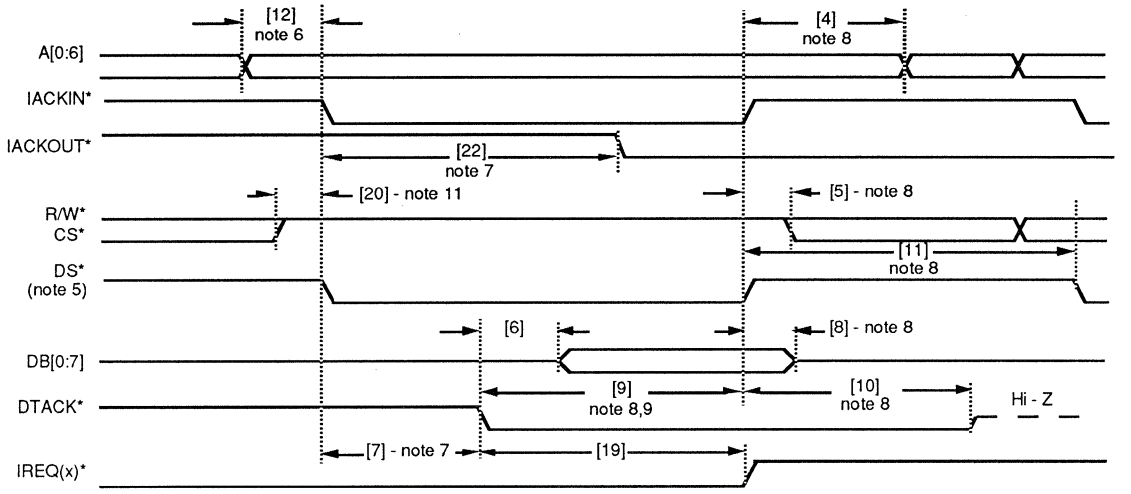


Figure 3

Motorola Write Cycle

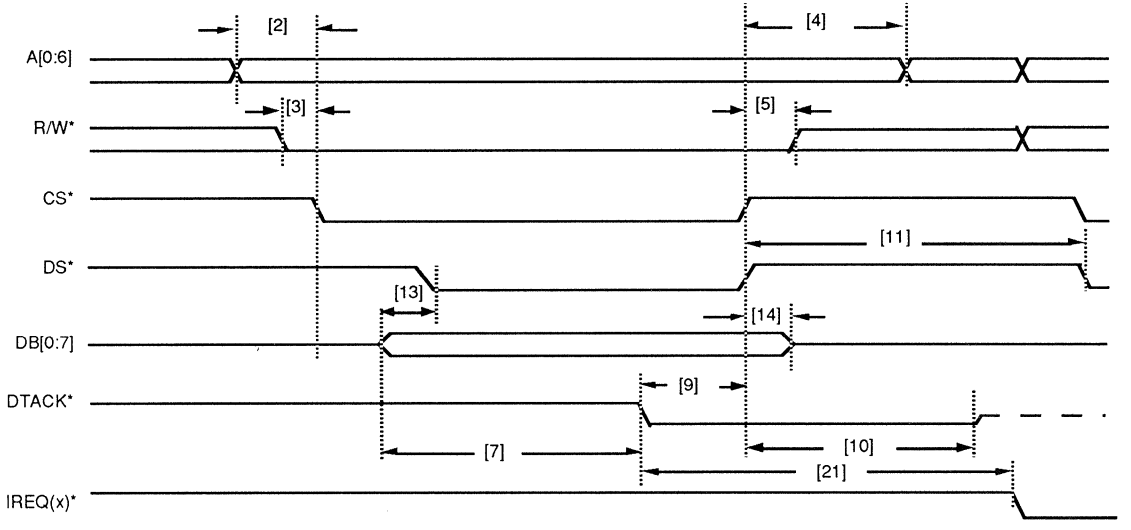


Figure 4

Intel Read Cycle

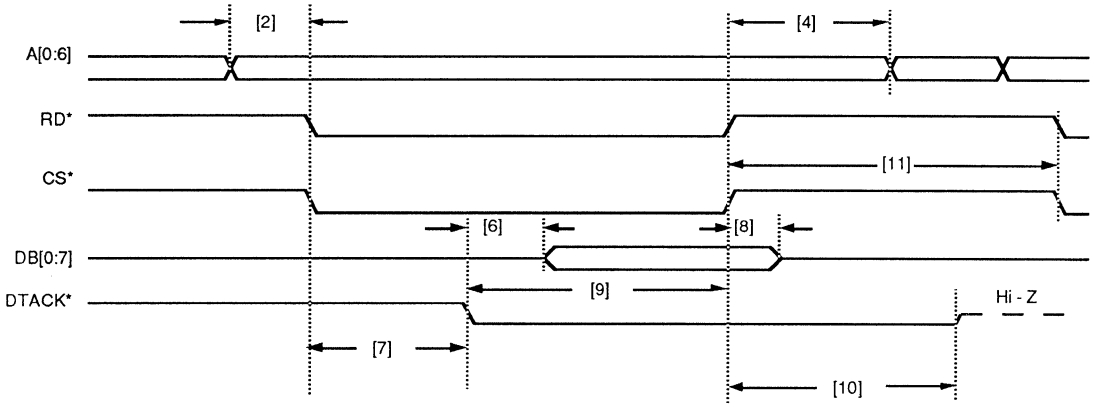


Figure 5

Intel Interrupt Acknowledge Cycle

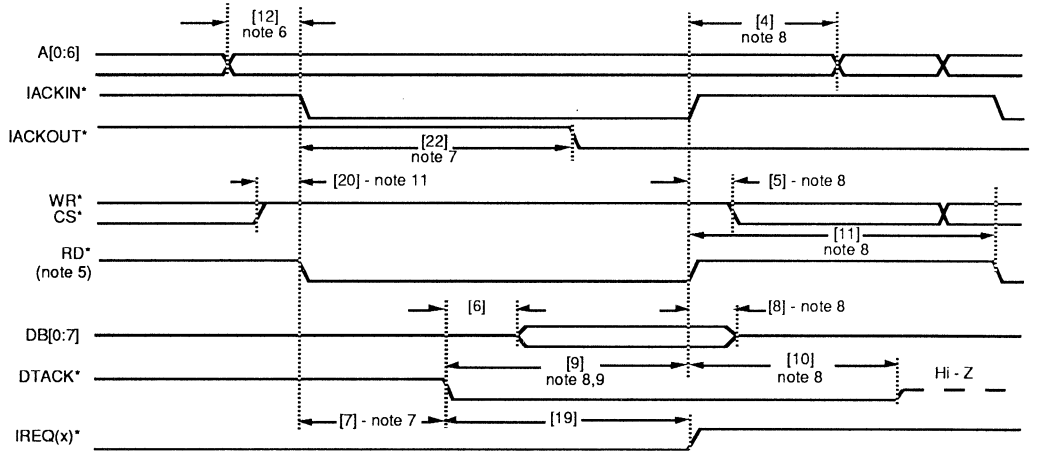


Figure 6

Intel Write Cycle

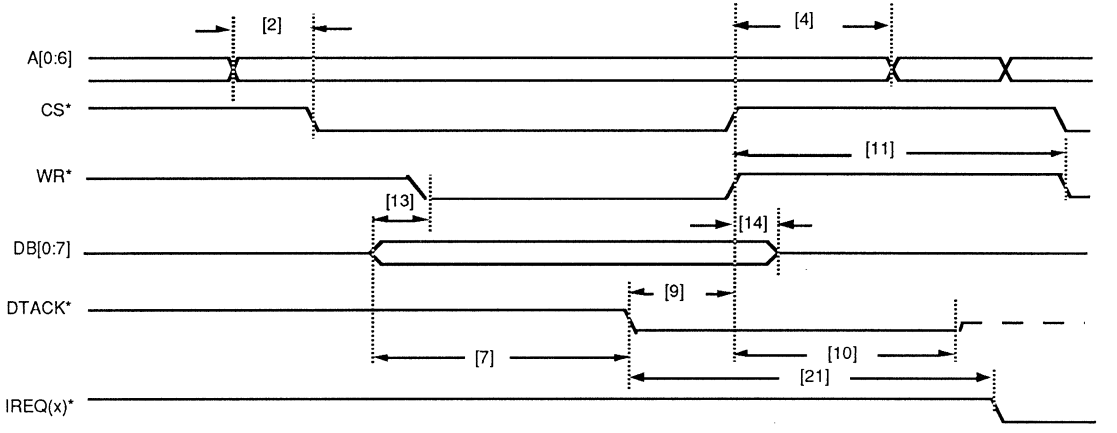
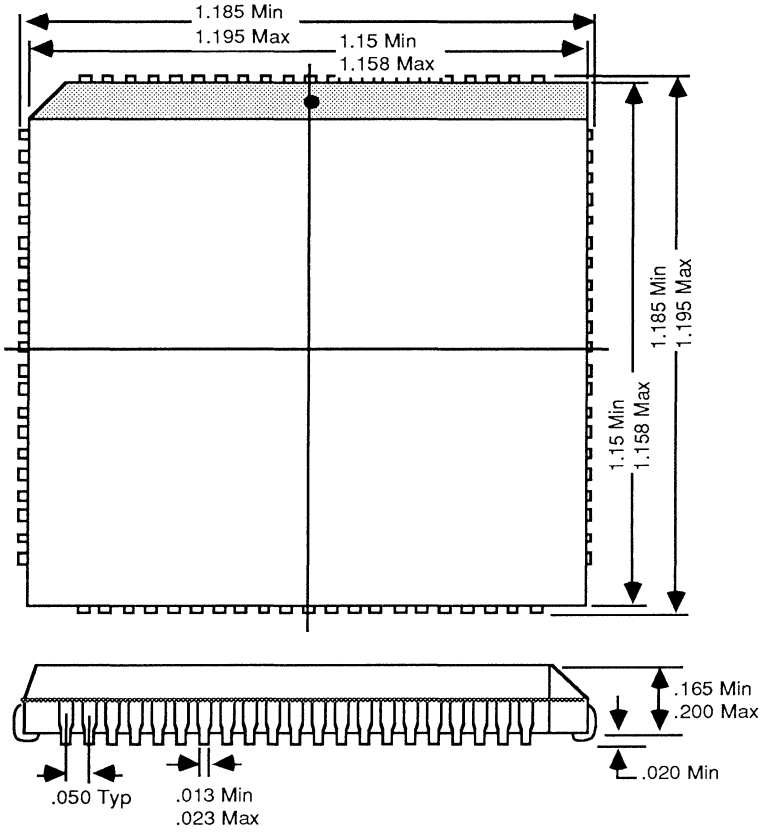


Figure 7

7. SAMPLE PACKAGE



8. ORDERING INFORMATION

CL – CD 180 – 10 PC – B

- CIRRUS LOGIC
- Product Line: (Communications, Data)
- Part Number
- Performance Grade: (Not Applicable)
- Package Type: P = Plastic Leaded Chip Carrier (PLCC)
- Temperature Range: C = Commercial
- Revision†

†Contact CIRRUS LOGIC for up-to-date information on revisions.

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The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™ † IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

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Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783