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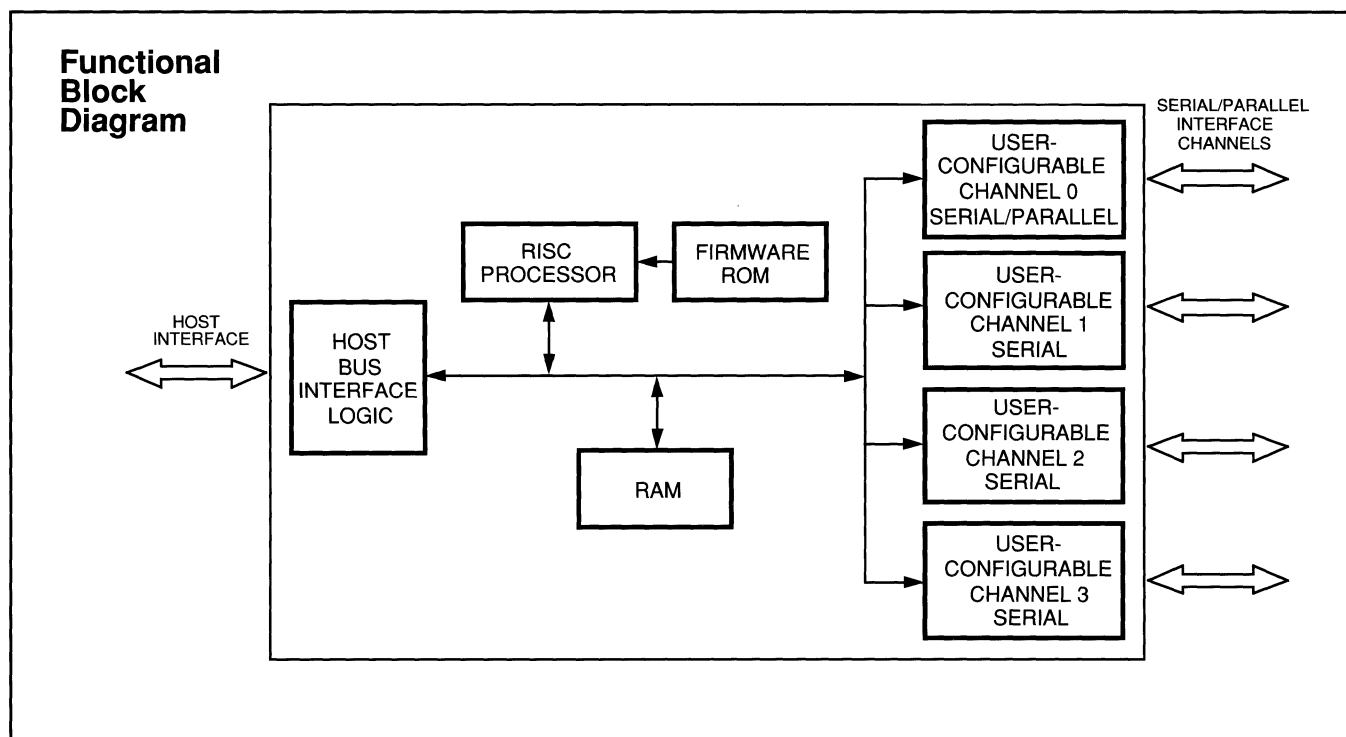
CL-CD1400
Product Bulletin

FEATURES

Asynchronous Features:

■ Software-programmable serial data rates up to 115.2 Kbit/sec. full-duplex[1]

■ Twelve bytes of FIFO for each transmitter and each receiver, with programmable threshold for receive-FIFO-interrupt generation

■ Improved interrupt schemes: *Good data interrupts* eliminate the need for character status check

■ Special character processing, particularly useful for UNIX-line-driver applications, optionally handled automatically by the CL-CD1400:
 — Automatic Expansion of NL to CR-NL
 — Supports LNEXT and ISTRIP
 — Ignore Break
 — UNIX parity handling options:
  ● Character removed from stream
  ● Passed as good data
  ● Replaced with null (00 hex)
  ● Preceded with FF-00 hex
  ● Passed as is with exception flagged

■ Independent bit rate selection for transmit and receive on each channel   *(cont.)*

Four-channel Serial/Parallel Communications Engine with UNIX® Character Processing

OVERVIEW

The CL-CD1400 is a flexible asynchronous receiver/transmitter with four full-duplex serial channels, or three full-duplex serial channels and one high-speed bidirectional parallel channel. With optional special character processing capabilities, it is especially well-suited to UNIX® applications. The CL-CD1400 is fabricated in an advanced-CMOS process and operates on a system clock of up to 20.2752 MHz. Packaged in a 68-pin PLCC, its high throughput, low-power consumption and high level of integration permit system designs with minimum part-count, maximum performance and maximum reliability.
(cont.)

Functional Block Diagram

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[1] 100% throughput is guaranteed up to 70K baud for full-duplex operation on all four channels simultaneously. 115.2K baud is achievable at reduced throughput. Refer to the CL-CD1400 data sheet for details.

FEATURES (cont.)

- User-programmable and automatic flow control modes for the serial channels:
  - In-band (software) flow control via single character (XON/XOFF)
  - Out-of-band (hardware) flow control via RTS/CTS and DTR/DSR
- Line-break detection and generation
- Insertion of transmit delays in data stream
- Local and remote maintenance loopback modes

- Six modem control signals-per-channel
- Odd, even, no or forced parity

Parallel Features:

- Parallel data rate up to 20 Kbyte/sec.
- Thirty-byte FIFO
- Automatic generation and recognition of handshake control signals
- Compatible with Centronics®-interface specifications

OVERVIEW (cont.)

The CL-CD1400's ability to move data efficiently from the serial channels to the host system results in an order-of-magnitude improvement in system-level throughput, and a reduction in overhead on the host system. Improved system throughput is attributed to a combination of features, most important of which are the transmit and receive data buffers. Each serial channel has two 12-byte FIFOs, one each for transmit and receive, and the parallel channel has 30 bytes. The receive FIFOs have programmable thresholds to minimize interrupt-latency requirements.

The CL-CD1400 communicates with the host system via service requests and acknowledgements. There are features to minimize both the number of requests to be serviced and the time required to service them. Required service requests have been reduced by the FIFOs, with only one needed every 12 characters. To reduce the time required per request, the CL-CD1400 supplies separate vectors for four different types of service requests. This reduces the time required by the host system to determine what action to take. For instance, there is a unique vector for "good data", so that the host wastes no time checking status bits or error conditions. If there is an error condition, the CL-CD1400 supplies a unique vector pointing to the error-handling routine. Other vectors report transmit status and modem signal change.

The CL-CD1400 is based on a high-performance proprietary RISC processor architecture developed by Cirrus Logic specifically for data communication applications. This internal CPU executes all instructions in one clock cycle and uses a register window architecture to ensure zero-overhead context switching for each type of internal interrupt. The on-chip RISC processor is transparent to the user, and no programming is required.

Because the on-chip processor is handling every character, such features as automatic flow control and special

character recognition are easily implemented, further reducing host system load. Both in-band (XON, XOFF) and out-of-band (RTS/CTS, DSR/DTR) flow control modes are supported. For in-band flow control, the CL-CD1400 automatically starts and stops its transmitter when the remote computer sends flow control characters. The CL-CD1400 also makes it easy for the local host to flow-control the remote computer, via the "Send Special Character" command. For out-of-band flow control, the transmitter asserts RTS and monitors CTS for permission to send. The receiver asserts and negates DTR when the receive FIFO reaches a user-definable threshold.

Character processing demands significant host CPU power and real-time responses. In addition to the in-band flow control, the CL-CD1400 provides features that off-load host CPU overhead in UNIX® terminal-interface software. For example, the CL-CD1400 can expand the 'linefeed' character to 'carriage return-linefeed' automatically.

Multiple-CL-CD1400 systems are easily implemented via a daisy-chain scheme. A Fair Share™ feature ensures equal access for service requests, across multiple devices.

What makes the CL-CD1400 so much better than conventional dumb UARTs is its efficiency, even when operating in a polled environment. The CL-CD1400 is truly intelligent; it is "thinking" about what is going on. For example, with a dumb UART, the host has to ask each channel, in turn, whether it has any data. The host system asks the CL-CD1400, as a whole, whether is has data. The chip tells the host whether there is any data, which channel, and whether it is good or erroneous, rather than the host testing each channel. Thus, the host-peripheral interface is easier to implement, faster, and more efficient.

CONFIGURATION EXAMPLES
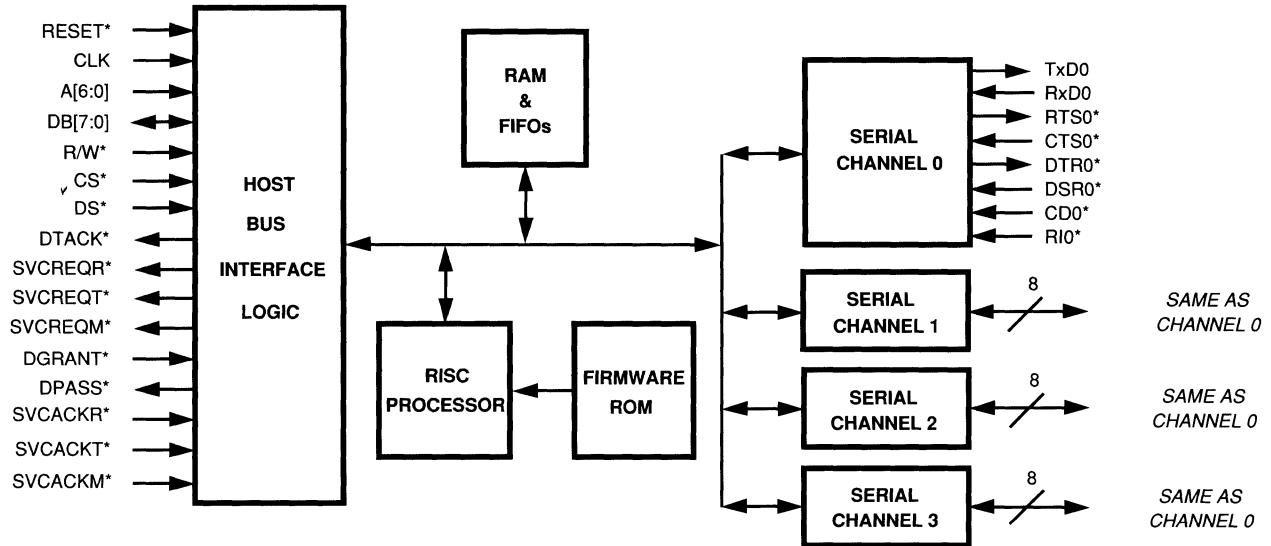
Four Full-modem Serial Channels
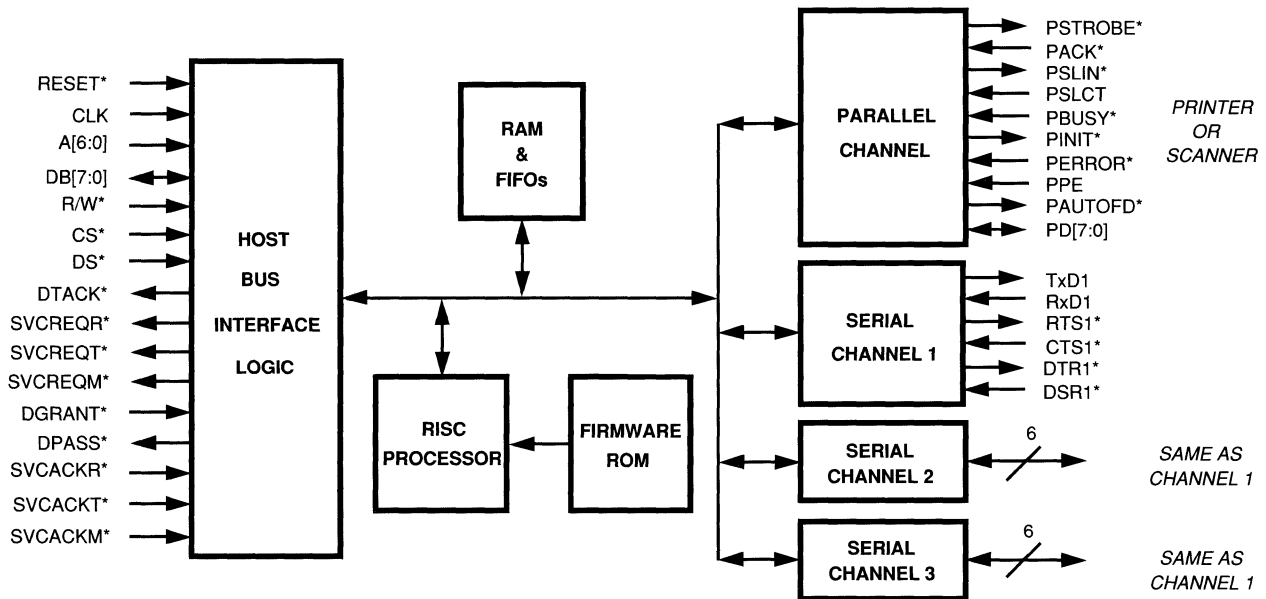
Three Serial Channels and One Parallel Channel

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

CL-CD1400

Benchmark Report

Version 1.0

Data Communications Products Group
Cirrus Logic, Inc.

Scope
This report presents a performance evaluation of the Cirrus Logic, Inc. CL-CD1400 intelligent, four-channel, asynchronous communications controller, also known as an UXART ("The UART for UNIX®"). It is the product of an ongoing test program at Cirrus Logic.

This document also includes a glossary of terms used in testing the CL-CD1400.

Related Documents
— CL-CD1400 Data Sheet

INTRODUCTION

The CL-CD1400 is a four-channel UART operating at a maximum speed of 115.2 Kbps. This high sustainable throughput makes it one of the fastest UARTs available. Sustainable throughput is a key specification that is often ignored or misrepresented. Sustainable throughput refers to the average data rate that can be maintained over a long period of time, not the 'peak' rate at which the device can be clocked.

The CL-CD1400 is a CMOS design with four full-duplex serial channels, each having separate 12-byte transmit and receive FIFOs. In addition, one channel can be configured as a parallel Centronics®-compatible interface. Because it moves data more efficiently from the serial channels to the host system than a conventional UART, the CL-CD1400 reduces host-system overhead and yields a ten-fold improvement in system throughput.

The CL-CD1400 is based on a high-speed, integrated RISC CPU developed by Cirrus Logic for communication applications. This on-chip processor is transparent to the user, and no programming is required. Because the on-chip processor is handling every character, automatic flow control and special character recognition are easily implemented, further reducing host system load.

This report is a summary of the performance capabilities of the CL-CD1400 as measured on the bench in 'real world' (and worse) conditions.

PERFORMANCE RESULTS

Four Channels, Simultaneous Transmit and Receive

The CL-CD1400 is capable of supporting four simultaneous full-duplex channels at 115.2 kbps. UARTs are typically used either to drive terminals, or for machine-to-machine file transfers. Of these two uses, the worst-case operating environment for a UART is machine-to-machine file transfer, because the machines are able to 'type' far faster than humans can. To simulate this, all receivers were operated at 115.2 kbps with 100 percent throughput and loading; the transmitters were driven at the same speed. The transmitters were then measured to ascertain the throughput they could sustain. The results of this test are summarized in Table 1.

Table 1. CL-CD1400 Throughput at 115.2 kbps

Number of active receive channels	Transmitter throughput
0	>99 percent
1	>99 percent
2	60 percent
3	40 percent
4	25 percent

This worst-case test scenario is more severe than the real world; most of the high-speed serial link protocols used for machine-to-machine file transfers, such as UUCP, are effectively half-duplex. At any given instant, the bulk of data flow is in one direction, contrary to true simultaneous full-duplex operation. When the receivers are lightly loaded, the CL-CD1400 easily drives all four transmitters at 115.2 kbps with greater than 99 percent throughput. Specifically, the CL-CD1400 can sustain full transmitter output at up to 20 percent receive loading on all four channels, depending on the burst level of the traffic received.

Because of its sustainable throughput, the CL-CD1400 is ideal not only for terminal-server connections to terminals, but also terminal-server connections to personal computers, and host-to-host connections.

Four Channels, Transmit-Only

This Transmit-Only Mode simulates a typical terminal server application. In terminal servers, most data movement is to the terminal, with only low duty cycle input from the terminal keyboard.

Transmit-Only Mode was tested at both half and full speed. In both cases, a continuous stream of capital 'U's were transmitted, eight bits per character, one stop bit and no parity. This character pattern results in a square wave bit stream that facilitates the noting of irregularities in bit timing and character assembly. Gaps seen in the character spacing indicate transmitter underrun or incorrectly disassembled and transmitted bits.

Transmission efficiency for up to three channels was nearly 100 percent; no gaps were noted. Activating the fourth channel caused a less-than-1-percent drop in efficiency. Gaps of one or two bit times after a character in the transmit data were occasionally found. This condition was rare and impossible to quantify. No available terminal can operate at 115.2 kbps, so some tests were done at half-speed, allowing the connection of a 57.6 kbps terminal. The terminal showed that all data was error-free. Operating the CL-CD1400 at a full clock rate did not produce any detectable changes in the behavior noted in the half-speed transmit-only test. This was confirmed under full-speed operation by examining the data with a logic analyzer to verify that there were no missing or erroneous bits.

Four Channels, Simultaneous Transmit and Receive with Loopback

Though not the worst-case scenario for UART operation, loopback in the CL-CD1400 was carefully examined. Loopback represents a 'typical' situation of heavy but not continuous loading. To determine if CL-CD1400 behavior under increasing load was predictable and linear, the bit rate was steadily increased and the effective throughput monitored for errors. The results of this test are shown in Figure 1. As shown, the overall throughput (transmit and receive) at 115.2 kbps is about 56 percent.
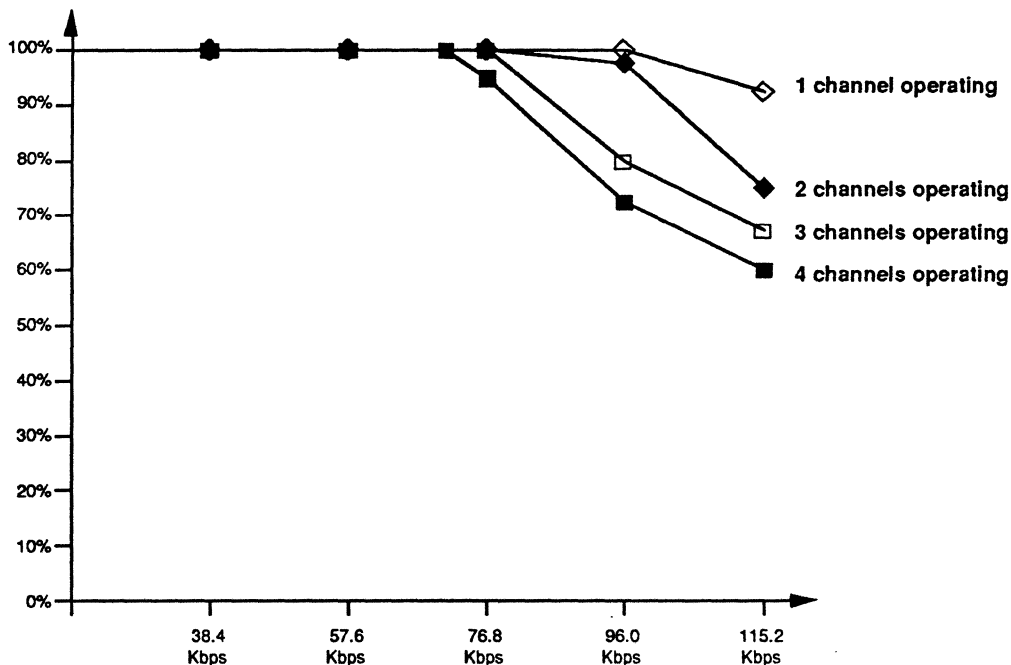
Figure 1. CL-CD1400 Performance

CL-CD1400 FIRMWARE ARCHITECTURE

CL-CD1400 operation can be better understood by focusing on firmware tasks and structure. CL-CD1400 firmware, comprising both foreground and background tasks, has been designed to optimize performance and handle overload conditions without dropping bits or characters. Foreground tasks are driven by individual bit interrupts from the bit engines, and are responsible for assembling bits into characters or disassembling characters into bits. They communicate with the background via one-character holding registers and event-posting mechanisms shown in Figures 2a and 2b.

Background tasks are responsible for FIFO management, special character processing, and identifying conditions such as FIFO full or FIFO empty, which require the assertion of an outbound interrupt. The background code is a polling system, and its various tasks are prioritized into inner-loop and outer-loop functions (see Figure 3). The inner loop is responsible for moving transmit characters to the holding register, and moving received characters from the holding register to the FIFO. Receive is favored over transmit. For this reason, when the CL-CD1400 CPU is fully loaded, it will service receive over transmit, and occasional-to-frequent gaps will occur between transmit characters as the CPU loads down. This is a desirable feature; as the CL-CD1400 processor becomes increasingly busy, it limits itself in an non-erroneous way. The gaps are also an effective way to assess the CPU load.

As shown in Figure 3, for each pass through the outer loop, the inner loop executes four times, checking the four channels for either receive or transmit activity. Note that if a channel receiver needs service, the channel transmitter is not serviced on that pass through the loop. This is the mechanism that favors receiving over transmitting.

The inner loop must execute four passes in the minimum character time. If it cannot do this, receive overflow errors will occur. When the CL-CD1400 is heavily loaded, every pass through the loop will result in a receive character being handled; this is performance limit of the device.

The outer loop scans for conditions that require the notification of the host, such as full or empty FIFOs, modem signals, and lower-priority tasks. This is when conditions requiring the CL-CD1400 to interrupt the host are detected and acted upon .
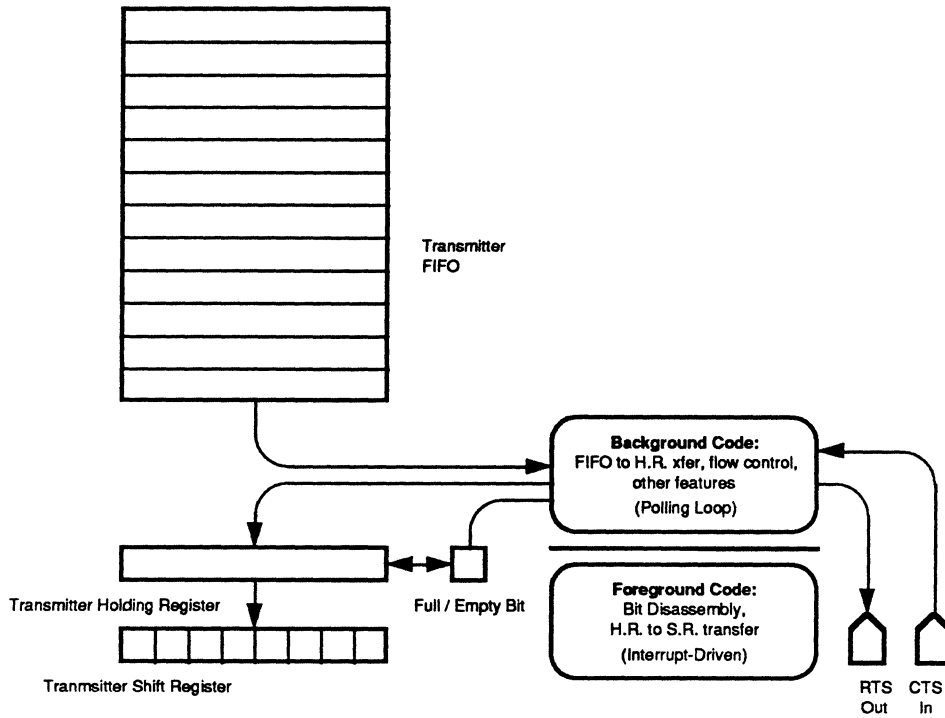
TEST CONDITIONS

Clock Speed

Bench testing was performed at the rated clock speed of 20 MHz, equivalent to 10 MIPS (million instructions per second). For several reasons, however, lower clock speeds were also tested; it's important to understand why.
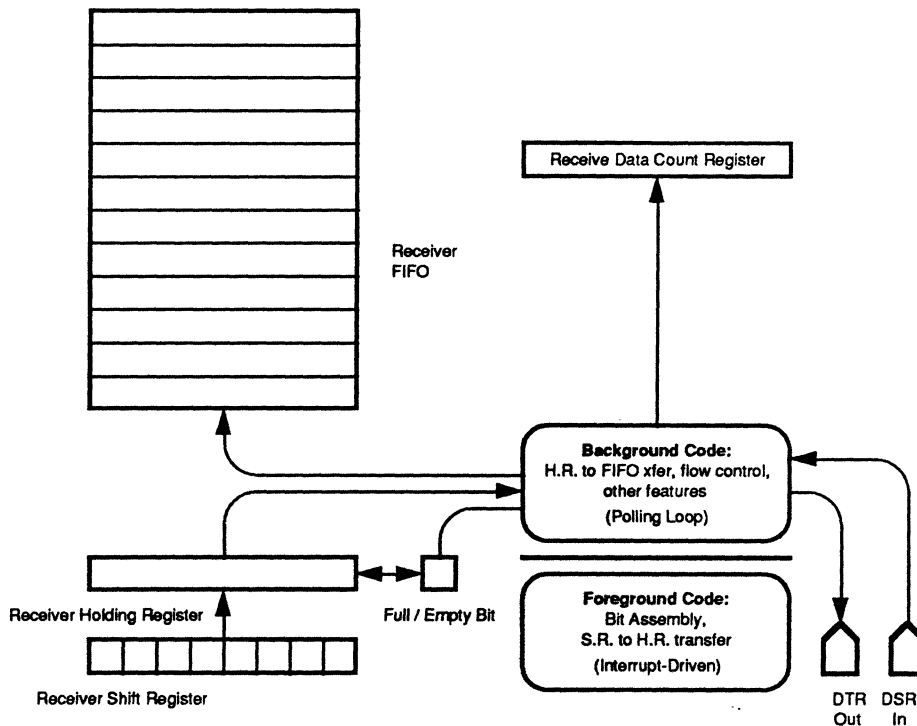
A problem in testing at high data rates is that there are few other sources of asynchronous data capable of operating at 115.2 kbps. Many common protocol testers, for example, can operate only up to 64 kbps. To test in loopback is one approach, but as the CL-CD1400 becomes busy, the transmitter throughput drops. The device automatically limits itself. With 'test characters' that supply a continuous stream of characters at 57.6 kbps, tests were run at half-speed; that is, the CL-CD1400 at a five-MIPS rate (10 MHz oscillator), supporting a true baud rate of 57.6 kbps. This is the same internal loading, or 'Bits-per-MIPS,' as 10 MIPS and 115.2 kbps. Other testing was performed at true full speed.

In some tests, the I/O speed of the AT bus limited the ability of a /AT386 to service the CL-CD1400. The effect of this can be measured by running the CL-CD1400 at half-speed, which has the effect of doubling the apparent speed of the /AT386 system. Several of the tests were run at both full and half speed to quantify and factor this effect. For example, at full speed, when one channel was set to receive its own transmission, the transmitter showed gaps of 1.5 character times every 12 characters — when the FIFO empties. However, this degradation was completely attributable
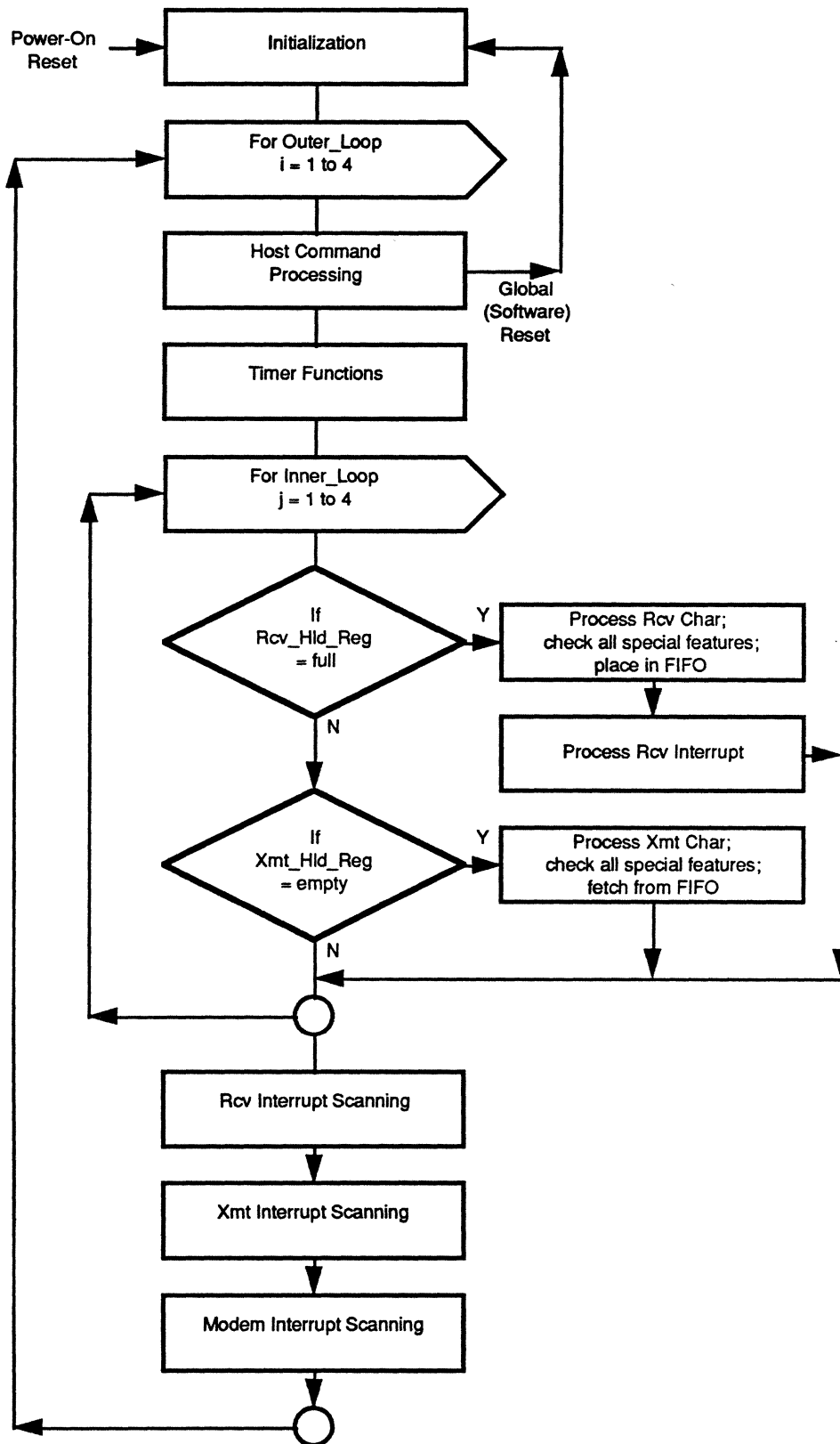
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Transmitter
FIFO

Background Code:
FIFO to H.R. xfer, flow control,
other features
(Polling Loop)

Transmitter Holding Register

Full / Empty Bit

Foreground Code:
Bit Disassembly,
H.R. to S.R. transfer
(Interrupt-Driven)

RTS   CTS
Out   In

Tranmsitter Shift Register

Figure 2a. CL-CD1400 Transmit Firmware Foreground and Background Tasks

Receiver
FIFO

Receive Data Count Register

Background Code:
H.R. to FIFO xfer, flow control,
other features
(Polling Loop)

Receiver Holding Register

Full / Empty Bit

Foreground Code:
Bit Assembly,
S.R. to H.R. transfer
(Interrupt-Driven)

DTR   DSR
Out   In

Receiver Shift Register

Figure 2b. CL-CD1400 Transmit Firmware Foreground and Background Tasks

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Figure 3. CL-CD1400 Flow

CIRRUS LOGIC

to the PC/AT interrupt service latency, and this was verified by testing at half speed. The PC/AT processed the interrupts, and no 1.5-character/time gaps occurred. The performance drop was in the transmit data stream only, and no errors were encountered in either transmit or receive characters. See section titled *Measurement Techniques* for more details.

System Environment

All testing was done on a PC/AT386-compatible computer using a CL-CD1400 evaluation board. The PC operated at 25 MHz and its standard AT bus ran at one-third the processor speed. The processor speed proved to be a limiting factor in some tests because the slow AT bus cannot support the aggregate demand of multiple CL-CD1400 channels.

Input (data to be received) was generated either by UARTs running in other machines, or by a pulse generator. Data format for both transmit and receive was eight bits, no parity, one stop bit. Testing was performed with both minimal and maximal character processing.

Measurement Techniques

Efficiency measurements, such as active transmission and idle times, were accomplished with a logic analyzer. The results indicated whether or not the measured idle time was due to host-imposed interrupt service limitations or CL-CD1400 internal constraints.

Idle time can be caused by either of two conditions: transmitter underrun due to internal chip performance, or transmitter underrun caused by interrupt latency in the PC/AT interrupt service routine. To eliminate the second condition from impacting measurements, a logic analyzer was used (when transmitter underruns occurred) to determine the placement of the interrupt signal with respect to the underrun. It was also used to determine whether the PC was in its idle loop, or was servicing another CL-CD1400 interrupt at the time. To test for slowdowns attributable to the PC, the CL-CD1400 was run at half speed, making the PC/AT twice as fast (relatively), and halving its effective overhead.

Underruns due to interrupt latency and CL-CD1400 internal delays were also determined. At 115.2 kbps, the CL-CD1400 transmitter consistently underruns after the transmit-FIFO-empty interrupt is posted (when one or more channels was set for receive and all four channels set for transmit). This is due to PC limitations, specifically the inability to move enough data over the slow AT bus. By running tests at both half and full speed, underruns due to PC/AT performance limitations could be factored out of the analysis.

Software

Cirrus Logic-developed, CL-CD1400 evaluation board software was used in the tests described in this report. The software has not been optimized for maximum performance.

Higher Speed Testing

When the CL-CD1400 receivers were tested at 230.4 kbps, one channel operated properly, but the PC/AT became saturated. An attempt to drive a second channel overloaded the PC/AT and no meaningful data was obtained.

CONCLUSION

The CL-CD1400 is highly reliable when supporting 115.2 kbps data transmission rates, either half- or full-duplex. When transmitting, or transmitting with some receive data, it can maintain 100 percent throughput. It also will receive data on multiple channels at 115.2 kbps, reducing its transmission automatically to service the demand.

TEST TERMINOLOGY

Bits-per-MIP
The maximum baud rate that can be supported at a given processor clock speed. Testing at different clock rates has shown that the ratio is scalable. For example, if a UART ran 38.4 kbps at 10 MHz, it could be assumed that it runs 76.8 at 20 MHz because the CL-CD1400 is a fully synchronous design.

Character Time
The time spent sending a character. For instance, when sending a character at 38.4 kbps, the bit time is 26.04 microseconds. If the character is defined as eight bit, one parity bit, one stop bit, then the total number of bits is 11, so the character time is 286.5 microseconds.

Efficiency
The ratio of character time to the sum of character time plus idle time. This value was obtained by noting the amount of idle time on the output versus the amount of active transmission over an arbitrary time period.

Fatal Error
A dropped bit parity or framing error, presumably caused by a bit rate too fast for the CL-CD1400.

Half-channel
A transmitter or receiver. Two half-channels make up a full channel. We use this term because in the CL-CD1400, the software considers the eight half channels as eight processes, not four processes.

Idle time
The 'gap', if any, between characters. Though not a true physical gap, it manifests itself as a stretched stop bit, that is, one longer than the programmed value (typically 1 bit). This idle time causes no problems in system operation, and so is not considered an error condition.

True Baud Rate
The actual bits-per-second rate on the line. During testing, it was desirable to run some tests at half clock speed because most other terminals cannot operate fast enough to fully test the CL-CD1400. By slowing down the CL-CD1400, we can be sure we are loading it to the maximum amount. When the CL-CD1400 is operated at half the normal processor speed, the baud rate divisor is kept the same, so the results will scale. This means that the true baud rate is one-half the programmed value.

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The Company

Cirrus Logic®, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783