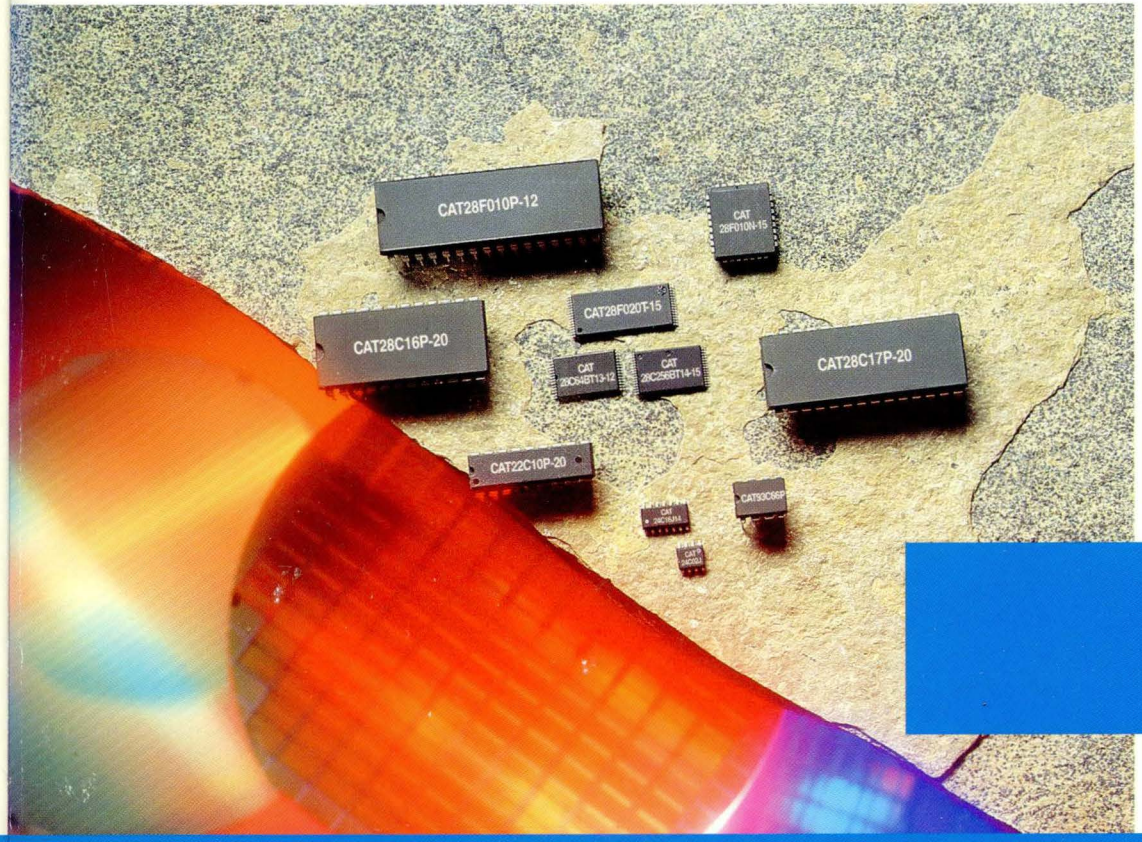
CATALYST SEMICONDUCTOR

CATALYST SEMICONDUCTOR

Flash Memory • E²PROM • Mixed Signal



Data Book 1996/1997

CATALYST SEMICONDUCTOR

1996/1997 Data Book

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Product Features

SERIAL E²PROMs

I²C Bus (Data Book Section 2)

Device	Temp. Range	Density (Organization)	ICC (Active/Standby)	Max. Clock Freq.	Lead Count	Pkg Types	Oprtg Vltg. Range
24C01	C, I	1Kb (128X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC01	C, I	1Kb (128X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C02	C, I	2Kb (256X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC02	C, I	2Kb (256X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C04	C, I	4Kb (512X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC04	C, I	4Kb (512X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C08	C, I	8Kb (1024X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC08	C, I	8Kb (1024X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C16	C, I	16Kb (2048X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC16	C, I	16Kb (2048X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C32	C, I	32Kb (4096X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC32	C, I	32Kb (4096X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24C64	C, I	64Kb (8192X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V
24WC64	C, I	64Kb (8192X8)	3mA/0µA	400kHz	8 14	PDIP, SOIC SOIC	1.8 -6.0V

SERIAL E²PROMs

Microwire Bus (Data Book Section 3)

Device	Temp. Range	Density (Organization)	ICC (Active/Standby)	Max. Clock Freq.	Lead Count	Pkg Types	Oprtg Vltg. Range
93C46	C, I	1Kb (64X16/128X8)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C46A	C, I	1Kb (64X16)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C56	C, I	2Kb (128X16/256X8)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C56A	C, I	2Kb (128X16)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C66	C, I	4Kb (256X16/512X8)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C66A	C, I	4Kb (256X16)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C86	C, I	16Kb (1024X16/2048X8)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C86A	C, I	16Kb (1024X16)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V
93C57	C, I	2Kb (128X16/256X8)	3mA/50µA	1MHZ	8	PDIP, SOIC	1.8 - 6.0V

SERIAL E²PROMs

SPI Bus (Data Book Section 4)

Device	Temp. Range	Density (Organization)	ICC (Active/Standby)	Max. Clock Freq.	Lead Count	Pkg Types	Oprtg Vltg
64LC10	C, I	1Kb (64X16)	1mA/0µA	1MHZ	8	PDIP, SOIC	2.5-6.0V
64LC20	C, I	2Kb (128X16)	1mA/0µA	1MHZ	8	PDIP, SOIC	2.5-6.0V
64LC40	C, I	4Kb (256X16)	1mA/0µA	1MHZ	8	PDIP, SOIC	2.5-6.0V

SERIAL E²PROMs

Secure Access (Data Book Section 5)

Device	Temp. Range	Protocol	Density (Organization)	ICC (Active/Standby)	Max. Clock Freq.	Lead Count	Pkg Types	Oprtg Vltg
35C704	C, I	Synchronous	4Kb (256X16/512X8)	3mA/250µA	3MHZ	8	PDIP, SOIC	4.5-5.5V
33C704	C, I	Synchronous	4Kb (256X16/512X8)	3mA/250µA	1MHZ	8	PDIP, SOIC	2.7-3.3V
35C804A	C, I	UART Compatible	4Kb (256X16/512X8)	3mA/250µA	5MHZ	8 16	PDIP, SOIC SOIC	4.5-5.5V
33C804A	C, I	UART Compatible	4Kb (256X16/512X8)	3mA/250µA	5MHZ	8 16	PDIP, SOIC SOIC	2.7-3.3V

NVRAMs
(Data Book Section 6)

Device	Temp. Range	Density (Organization)	Access Time (ns)/ Max. CLK Freq	ICC (Active/Standby)	Lead Count	Pkg Types	Oprtg Vltg Range
22C10	C, I	256b	200, 300 (64X4)	40mA/30µA	18 16	PDIP SOIC	4.5-5.5V
24C44	C, I	256b	1MHZ (16X16)	3mA/30µA	8	PDIP, SOIC	4.5-5.5V

Flash Memories
(Data Book Section 7)

Device	Temp. Range	Density (Organization)	Access Time (ns)	ICC (Active/Standby)	Lead Count	Pkg Types	Oprtg Vltg Range
28F512	C, I	512Kb (64KX8)	90/120/150	30mA/100µA	32	PDIP, PLCC, TSOP	12V
28F010	C, I	1Mb (128KX8)	90/120/150	30mA/100µA	32	PDIP, PLCC, TSOP	12V
28F020	C, I	2Mb (256KX8)	120/150/200	30mA/100µA	32	PDIP, PLCC, TSOP	12V
28F102	C, I	1Mb (64KX16)	90/120/150	30mA/100µA	40 44	PDIP, TSOP PLCC	12V
28F202	C, I	2Mb (128KX16)	120/150/200	30mA/100µA	40 44	PDIP, TSOP PLCC	12V
28F001	C,I	1Mb (128KX8)	90/120/150	-	32	PDIP, PLCC, TSOP	12V
28F002	C,I	2Mb (256KX8)	120/150/200	-	32 40 44	PDIP, PLCC, TSOP TSOP PSOP	12V

PARALLEL E²PROMs
(Data Book Section 8)

Device	Temp. Range	Compatibility	Density (Organization)	Access Time (ns)	ICC (Active/Standby)	Lead Count	Pkg Types	Oprtg Vltg
28C16A	C, I	Industry	16Kb (2KX8)	200, 250	35mA/100µA	24 32	PDIP, SOIC PLCC	4.5-5.5V
28C17A	C, I	Industry	16Kb (2KX8)	200, 250	35mA/100µA	28 32	PDIP, SOIC PLCC	4.5-5.5V
28C64B	C, I	Industry	64Kb (8KX8)	120, 150, 200	30mA/100µA	28 32	PDIP, SOIC, TSOP TSOP, PLCC	4.5-5.5V
28C65B	C, I	Industry	64Kb (8KX8)	120, 150, 200	30mA/100µA	28 32	PDIP, SOIC, TSOP TSOP, PLCC	4.5-5.5V
28C256	C, I	Industry	256Kb (32KX8)	150, 200, 250	30mA/150µA	28 32	PDIP, TSOP TSOP, PLCC	4.5-5.5V

PARALLEL E²PROMs

Low Voltage (Data Book Section 8)

Device	Temp. Range	Density (Organization)	Access Time (ns)	ICC (Active/Standby)	Lead Count	Pkg Types	Oprtg Vltg
28LV64	C, I	64Kb (8KX8)	200, 250, 300	8mA/150µA	28 32	PDIP, SOIC, TSOP TSOP, PLCC	3.0-3.6V
28LV65	C, I	64Kb (8KX8)	200, 250, 300	8mA/150µA	28 32	PDIP, SOIC, TSOP TSOP, PLCC	3.0-3.6V
28LV256	C, I	256Kb (32KX8)	200, 250, 300	15mA/150µA	28 32	PDIP, TSOP TSOP, PLCC	3.0-3.6V

Mixed Signal Products

(Data Book Section 9)

Device	Temp	Bits Resolution	Linearity Error(LSB)	Data Latch	NV MEM.	#DACs/Pkg	Pkg Types	Settling Time(ns)
104A	C, I	12	1/2 LSB	No	No	1	CerDIP	40
104B	C, I	12	1LSB	No	No	1	CerDIP	40
105A	C, I	12	1/2 LSB	Yes	No	1	CerDIP	40
105B	C, I	12	1 LSB	Yes	No	1	CerDIP	40
504	C, I	8	1LSB	Yes	Yes	4	PDIP, SOIC	10µs
505	C, I	8	1LSB	Yes	Yes	4	PDIP, SOIC	10µs
506A	C	12	1/2 LSB	Yes	No	1	CerDIP	25
506B	C	12	1LSB	Yes	No	1	CerDIP	25

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CAT24C01/02/04/08/16

1K/2K/4K/8K/16K-Bit Serial E²PROM

FEATURES

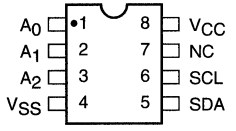
- 400 KHZ I²C Bus Compatible*
- 1.8 to 6.0 Volt Operation
- Low Power CMOS Technology
- Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin DIP, 8-pin SOIC or 14-pin SOIC Package
- Commercial and Industrial Temperature Ranges

DESCRIPTION

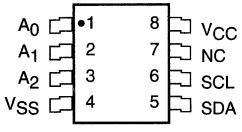
The CAT24C01/02/04/08/16 is a 1K/2K/4K/8K/16K-bit Serial CMOS E²PROM internally organized as 128/256/512/1024/2048 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C01/02 features an 8-byte page write buffer, and the CAT24C04/08/16 features an 16-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP, 8-pin SOIC or 14-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)

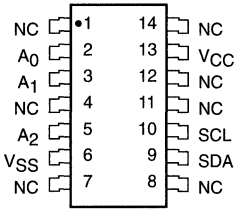


SOIC Package (J)



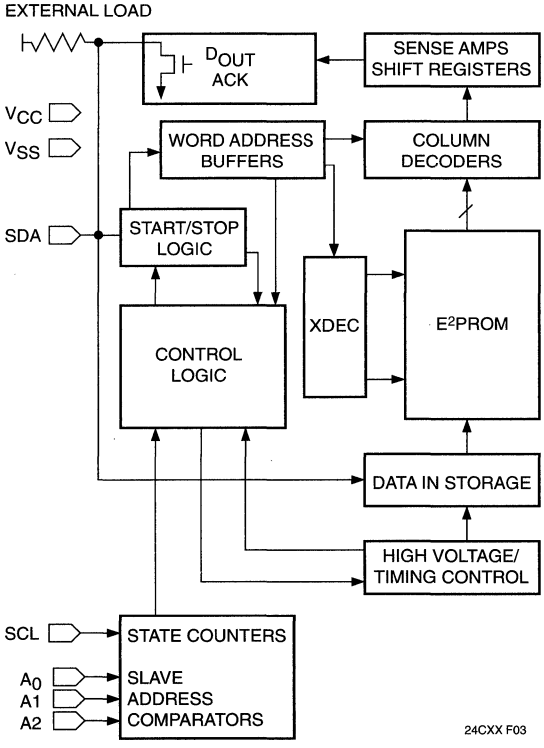
24CXX F01

SOIC Package (J14)



24CXX F02

BLOCK DIAGRAM



24CXX F03

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
NC	No Connect
VCC	+1.8V to +6.0V Power Supply
VSS	Ground

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V
V_{CC} with Respect to Ground ..... –2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

2

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}(5)	Standby Current (V_{CC} = 5.0V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)			0.4	V	I_{OL} = 3 mA
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SB}) = 0µA (<900nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	V_{CC}=1.8V - 6V		V_{CC}=4.5V - 5.5V		Units
		Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C01/02/04/08/16 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C01/02/04/08/16 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices (24C01 and 24C02), 4 devices (24C04), 2 devices (24C08) and 1 device (24C16) may be connected to the bus as determined by the device address inputs A0, A1, and A2.

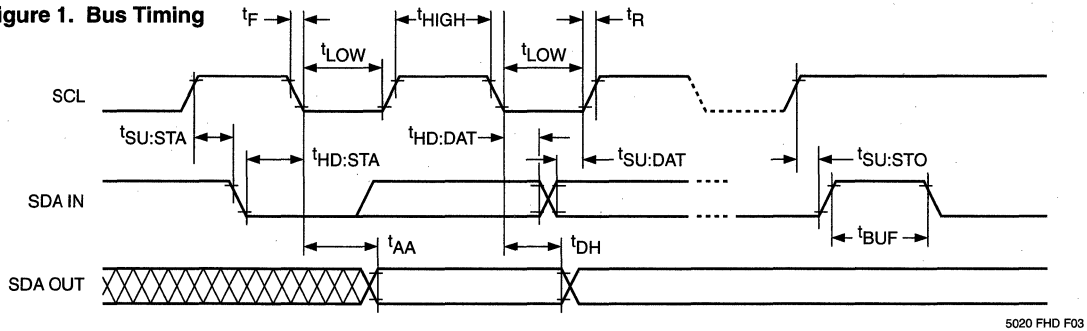
PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24C01/02/04/08/16 serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24C01/02/04/08/16 bidirectional serial data/address pin used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

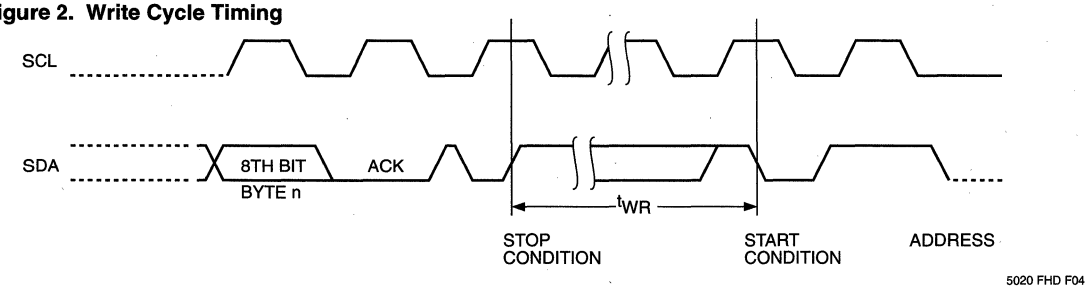
A0, A1, A2: Device Address Inputs
These inputs set device address when cascading multiple devices. A maximum of eight devices can be cascaded when using either 24C01 or 24C02 device. All three address pins are used for these densities.

Figure 1. Bus Timing



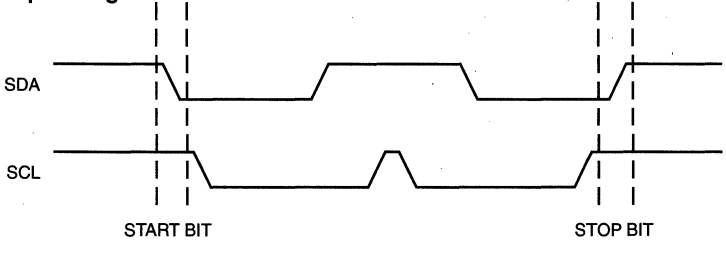
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

A total of four devices can be addressed on a single bus when using 24C04 device. Only A1 and A2 address pin are used with this device. The A0 address pin must be tied to V_{SS}.

Only two devices can be cascaded when using 24C08. The only address pin used with this device is A2. The other two address pins (A0, A1) must be tied to V_{SS}.

The 24C16 is a stand alone device. In this case, all address pins (A0, A1, A2) must be tied to V_{SS}.

I^2C BUS PROTOCOL

The following defines the features of the I^2C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C01/02/04/08/16 monitor the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C01/02/04/08/16 (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device or which part of the device the Master is accessing. Up to eight CAT24C01/02, four CAT24C04, two CAT24C08, and one CAT24C16 may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

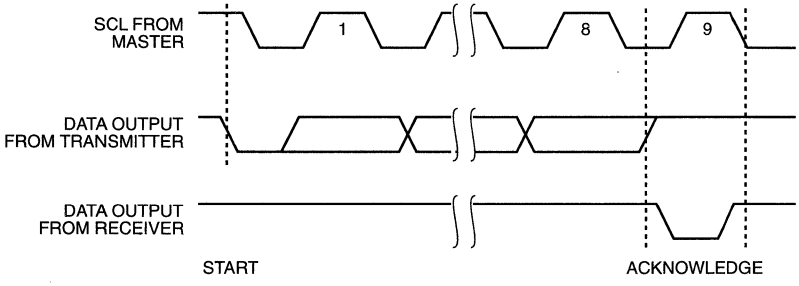
After the Master sends a START condition and the slave address byte, the CAT24C01/02/04/08/16 monitor the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C01/02/04/08/16 then perform a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

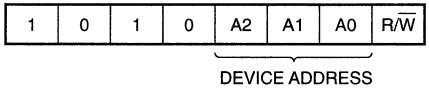
The CAT24C01/02/04/08/16 respond with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5022 FHD F07

When the CAT24C01/02/04/08/16 begins a READ mode, it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C01/02/04/08/16 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

2

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C01/02/04/08/16. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C01/02/04/08/16 acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C01/02 writes up to 8 bytes of data, CAT24C04/08/16 writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to P (P = 7 for 24C01/02 and P = 15 for 24C04/08/16) additional bytes. After each byte has been transmitted the CAT24C01/02/04/08/16 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

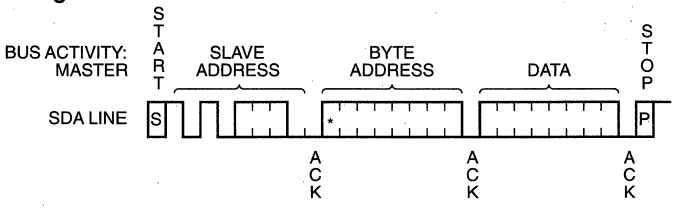
If the Master transmits more than P+1 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all P+1 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C01/02/04/08/16 in a single write cycle.

Acknowledge Polling

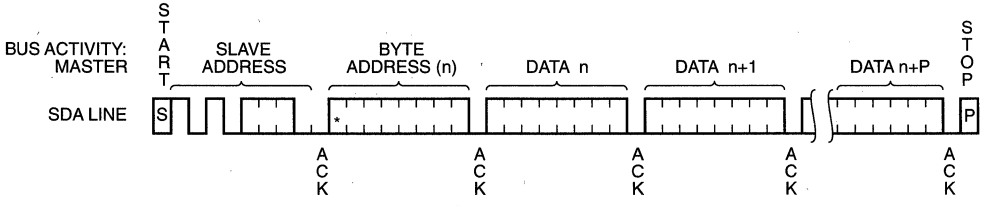
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C01/02/04/08/16 initiate the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C01/02/04/08/16 is still busy with the write operation, no ACK will

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

P=7 for CAT24C01/02 and P=15 for CAT24C04/08/16
* = Don't care for 24C01

5020 FHD F09

be returned. If the CAT24C01/02/04/08/16 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

The READ operation for the CAT24C01/02/04/08/16 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C01/02/04/08/16's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E = 127 for 24C01, 255 for 24C02, 511 for 24C04, 1023 for 24C08, and 2047 for 24C16), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C01/02/04/08/16 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

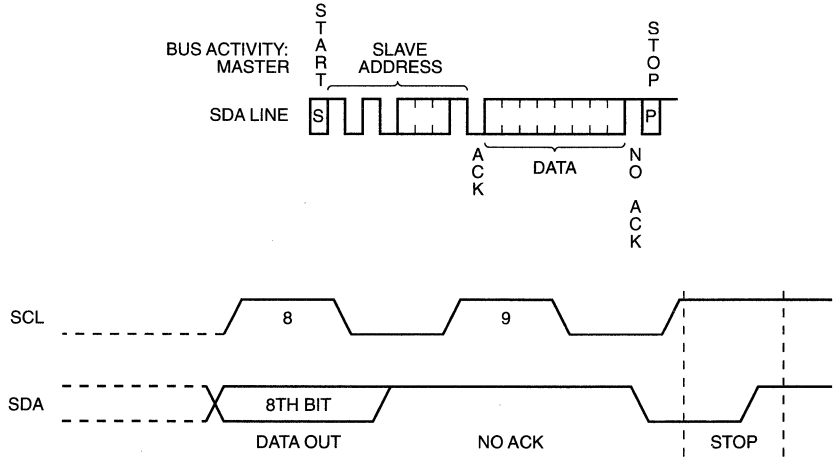
Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C01/02/04/08/16 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C01/02/04/08/16 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C01/02/04/08/16 sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C01/02/04/08/16 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

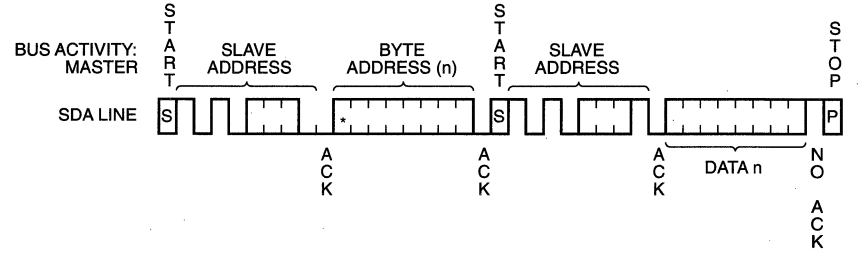
The data being transmitted from the CAT24C01/02/04/08/16 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C01/02/04/08/16 address bits so that the entire memory array can be read during one operation. If more than the E bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



5020 FHD F10

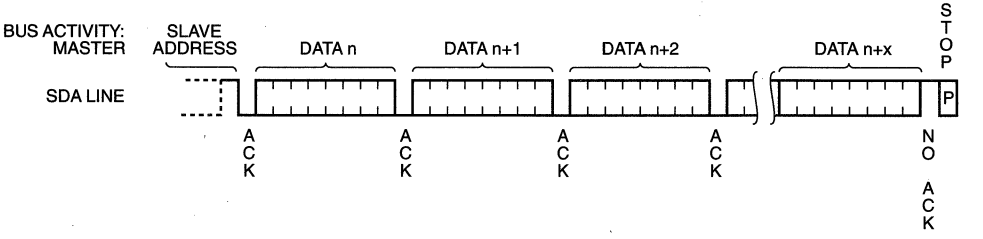
Figure 9. Selective Read Timing



* = Don't care for 24C01

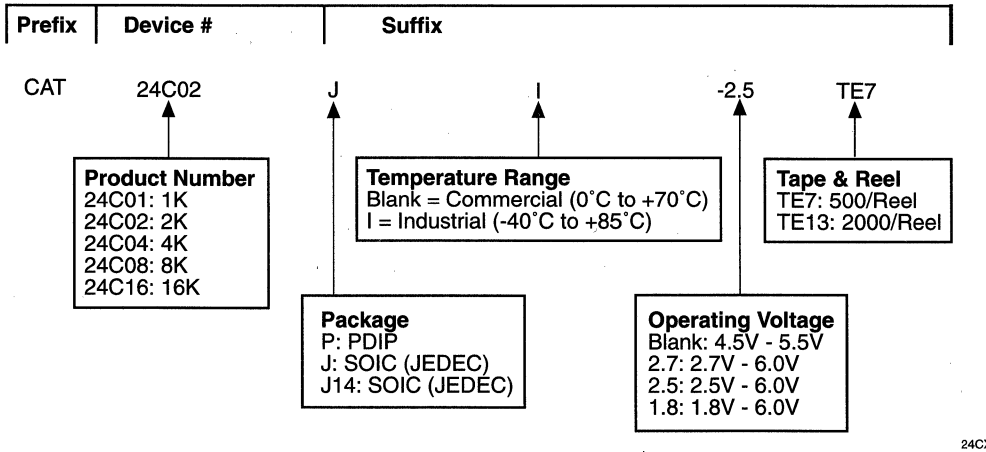
5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

ORDERING INFORMATION



24CXX F14

Notes:
(1) The device used in the above example is a 24C02JI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CAT24WC01/02/04/08/16

1K/2K/4K/8K/16K-Bit Serial E²PROM

FEATURES

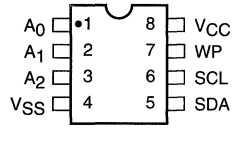
- 400 KHZ I²C Bus Compatible*
- 1.8 to 6.0Volt Operation
- Low Power CMOS Technology
- Hardware Write Protect
- Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin DIP, 8-pin SOIC or 14-pin SOIC Package
- Commercial and Industrial Temperature Ranges

DESCRIPTION

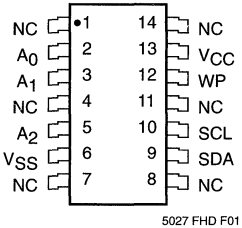
The CAT24WC01/02/04/08/16 is a 1K/2K/4K/8K/16K-bit Serial CMOS E²PROM internally organized as 128/256/512/1024/2048 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24WC01/02 features an 8-byte page write buffer, and the CAT24WC04/08/16 features an 16-byte page write buffer. The device operates via the I²C bus serial interface, has a special write protection feature, and is available in 8-pin DIP, 8-pin SOIC or 14-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (J14)



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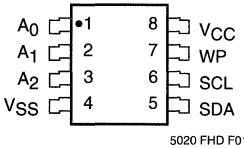
SOIC Package (J)

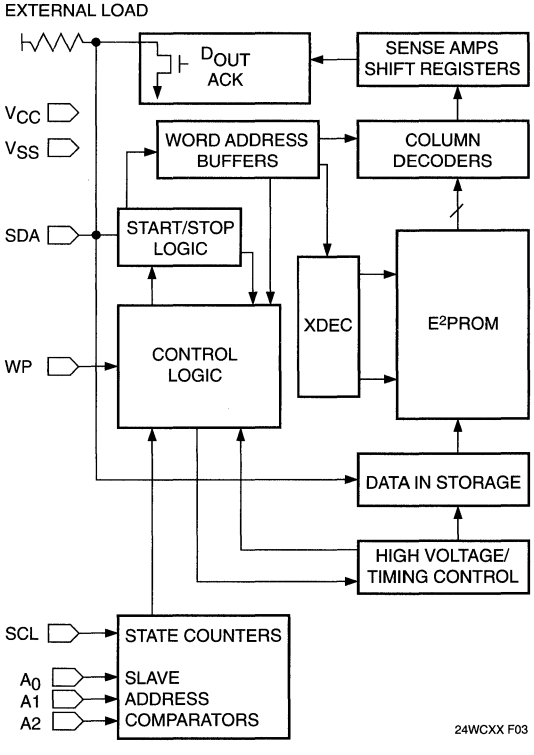


5020 FHD F01

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
VCC	+1.8V to +6.0V Power Supply
VSS	Ground

BLOCK DIAGRAM



24WCXX F03

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V
V_{CC} with Respect to Ground ..... –2.0V to +7.0V
Package Power Dissipation
Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

2

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_S(5)	Standby Current (V_{CC} = 5.0V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)			0.4	V	I_{OL} = 3 mA
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL, WP)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SB}) = 0µA (<900nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	V_{CC}=1.8V - 6V		V_{CC}=4.5V - 5.5V		Units
		Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24WC01/02/04/08/16 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC01/02/04/08/16 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices (24WC01 and 24WC02), 4 devices (24WC04), 2 devices (24WC08) and 1 device (24WC16) may be connected to the bus as determined by the device address inputs A0, A1, and A2.

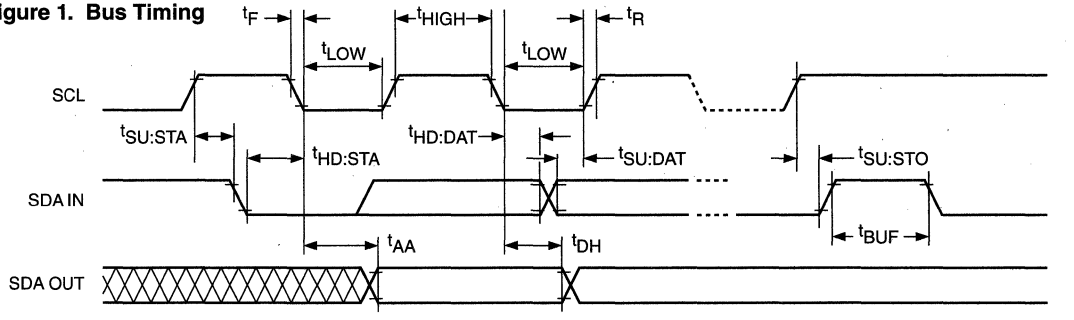
PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24WC01/02/04/08/16 serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24WC01/02/04/08/16 bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

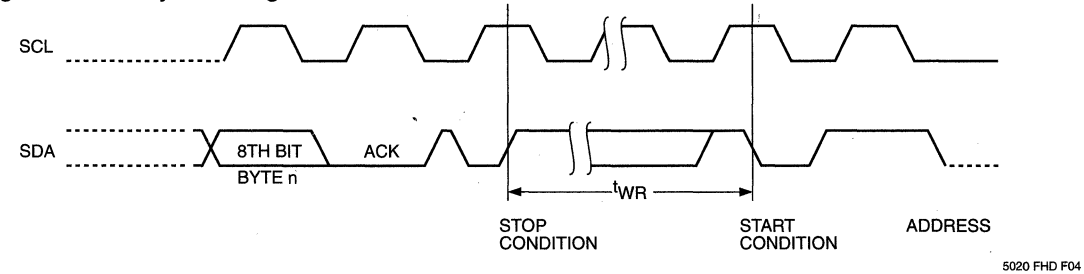
A0, A1, A2: Device Address Inputs
These inputs set device address when cascading multiple devices. A maximum of eight devices can be cascaded when using either 24WC01 or 24WC02 device. All three address pins are used for these densities.

Figure 1. Bus Timing



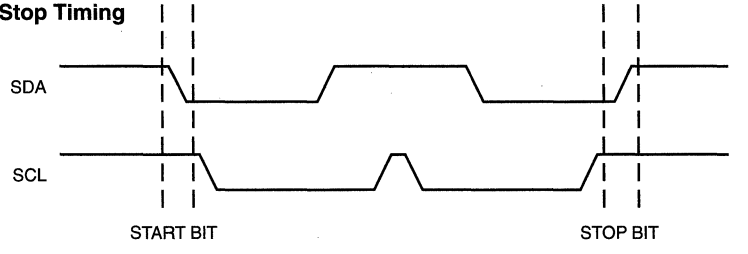
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

A total of four devices can be addressed on a single bus when using 24WC04 device. Only A1 and A2 address pins are used with this device. The A0 address pin must be tied to V_{SS}.

Only two devices can be cascaded when using 24WC08. The only address pin used with this device is A2. The other two address pins (A0, A1) must be tied to V_{SS}.

The 24WC16 is a stand alone device. In this case, all address pins (A0, A1, A2) must be tied to V_{SS}.

WP: Write Protect
If the WP pin is tied to V_{CC} the entire memory array becomes Write Protected (READ only). When the WP pin is tied to V_{SS} normal read/write operations are allowed to the device.

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC01/02/04/08/16 monitor the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

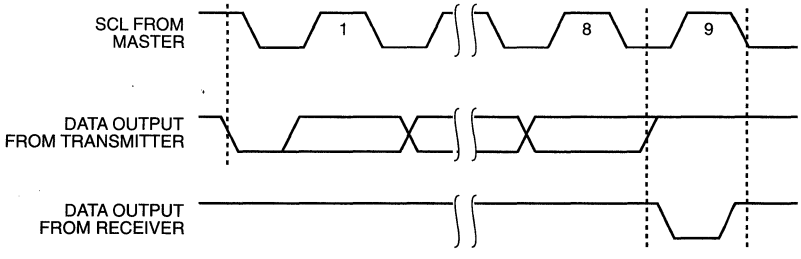
A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24WC01/02/04/08/16 (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device or which part of the device the Master is accessing. Up to eight CAT24WC01/02, four CAT24WC04, two CAT24WC08, and one CAT24WC16 may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

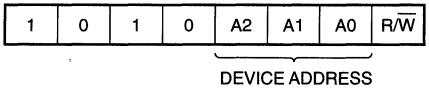
After the Master sends a START condition and the slave address byte, the CAT24WC01/02/04/08/16 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC01/02/04/08/16 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



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Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC01/02/04/08/16 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24WC01/02/04/08/16 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC01/02/04/08/16 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24WC01/02/04/08/16. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24WC01/02/04/08/16 acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

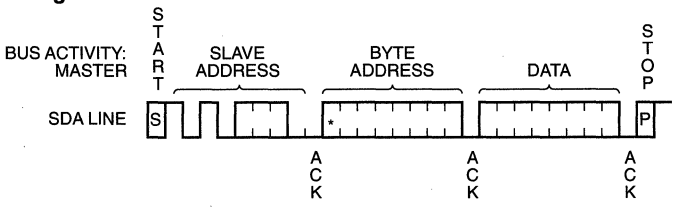
Page Write

The CAT24WC01/02 writes up to 8 bytes of data, and CAT24WC04/08/16 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to P (P=7 for 24WC01/02 and P=15 for CAT24WC04/08/16) additional bytes. After each byte has been transmitted the CAT24WC01/02/04/08/16 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than P+1 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

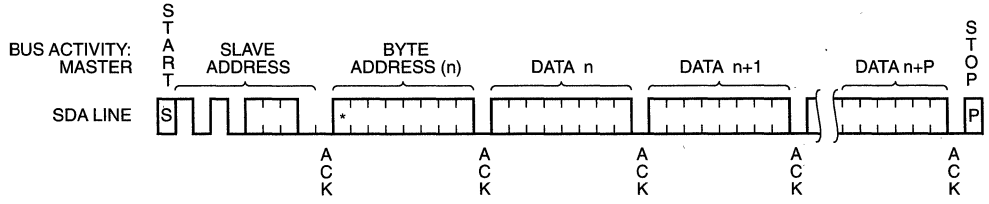
Once all P+1 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24WC01/02/04/08/16 in a single write cycle.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

P=7 for CAT24WC01/02 and P=15 for CAT24WC04/08/16
* = Don't care for CAT24WC01

24WCXX F09

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24WC01/02/04/08/16 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24WC01/02/04/08/16 is still busy with the write operation, no ACK will be returned. If the CAT24WC01/02/04/08/16 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24WC01/02/04/08/16 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT24WC01/02/04/08/16 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24WC01/02/04/08/16's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E = 127 for 24WC01, 255 for 24WC02, 511 for 24WC04, 1023 for 24WC08, and 2047 for 24WC16), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24WC01/02/04/08/16 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

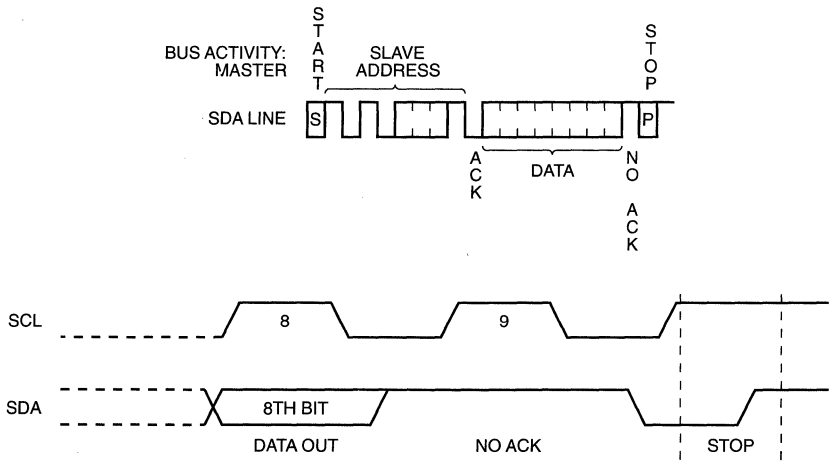
Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24WC01/02/04/08/16 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24WC01/02/04/08/16 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24WC01/02/04/08/16 sends

Figure 8. Immediate Address Read Timing



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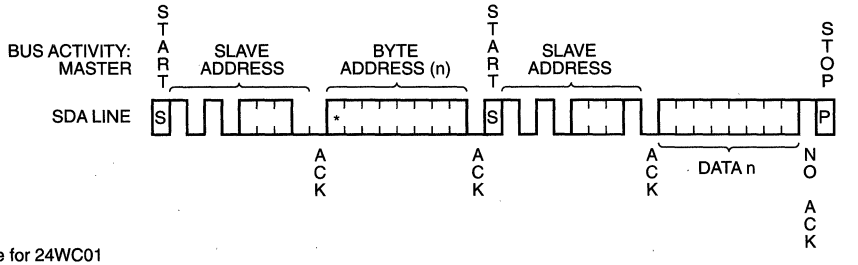
the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC01/02/04/08/16 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation is terminated when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24WC01/02/04/08/16 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC01/02/04/08/16 address bits so that the entire memory array can be read during one operation. If more than the E bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

2

Figure 9. Selective Read Timing



* = Don't Care for 24WC01

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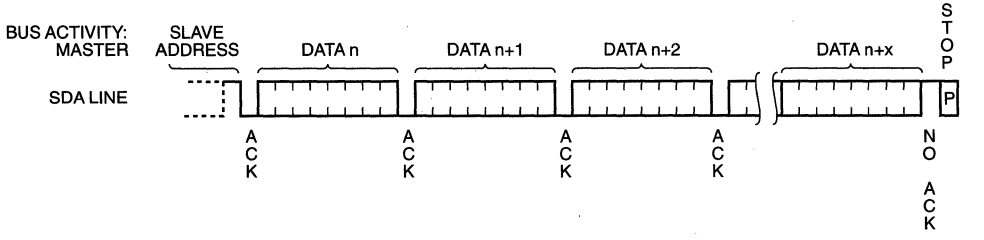
Figure 10. Sequential Read Timing



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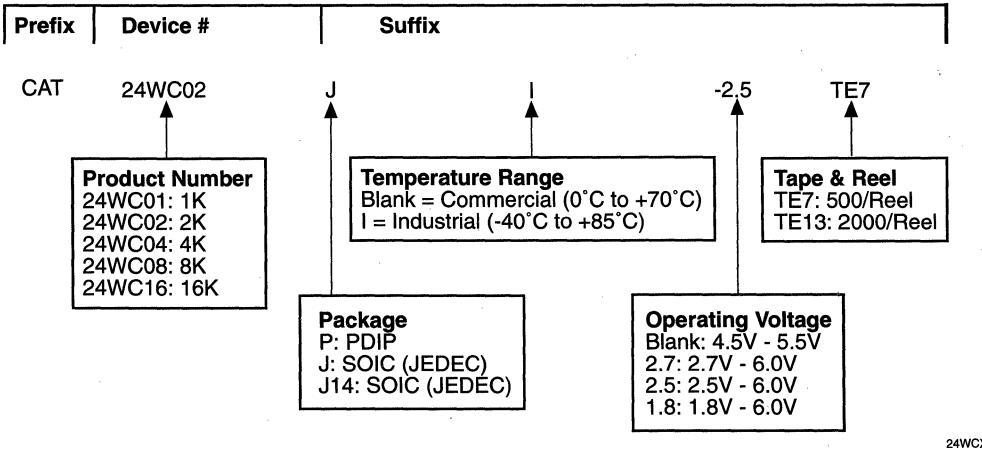
ORDERING INFORMATION



24WCXX F14

Notes:

(1) The device used in the above example is a 24WC02JI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CAT24C32/64

32K/64K-Bit Serial CMOS E²PROM

FEATURES

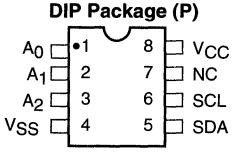
- 400 KHz I²C Bus Compatible*
- 1.8 to 6 Volt Operation
- Low Power CMOS Technology
- 32-Byte Page Write Buffer
- Commercial and Industrial Temperature Ranges
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-Pin DIP or 8-Pin SOIC

DESCRIPTION

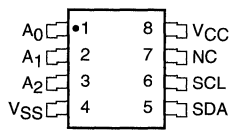
The CAT24C32/64 is a 32K/64K-bit Serial CMOS E²PROM internally organized as 4096/8192 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C32/64 features a 32-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP or 8-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (J,K)



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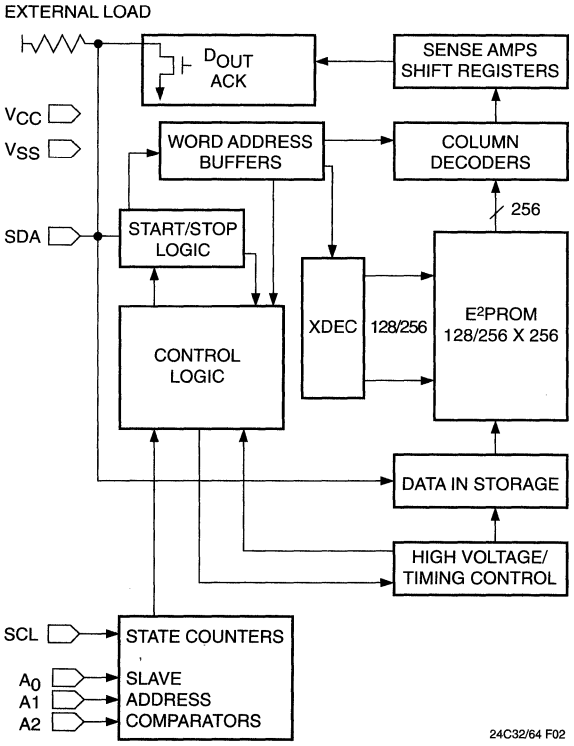
PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
NC	No Connect
VCC	+1.8V to +6V Power Supply
VSS	Ground

BLOCK DIAGRAM



24C32/64 F02

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}(5)	Standby Current (V_{CC} = 5V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = +3.0V)			0.4	V	I_{OL} = 3.0 mA
V_{OL2}	Output Low Voltage (V_{CC} = +1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby current (I_{SB}) = 0 µA (<900 nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6V, unless otherwise specified.
Output Load is 1 TTL Gate and 100pF

Read & Write Cycle Limits

Symbol	Parameter	V_{CC} = 1.8V - 6V		V_{CC} = 4.5V - 5.5V		Units
		Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing (1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	1	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

FUNCTIONAL DESCRIPTION

The CAT24C32/64 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C32/64 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

2

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These pins are hardwired or left unconnected (for hardware compatibility with CAT24C16). When hardwired, up to eight CAT24C32/64s may be addressed on a single bus system (refer to Device Addressing). When the pins are unconnected, the default values are zeros.

Figure 1. Bus Timing

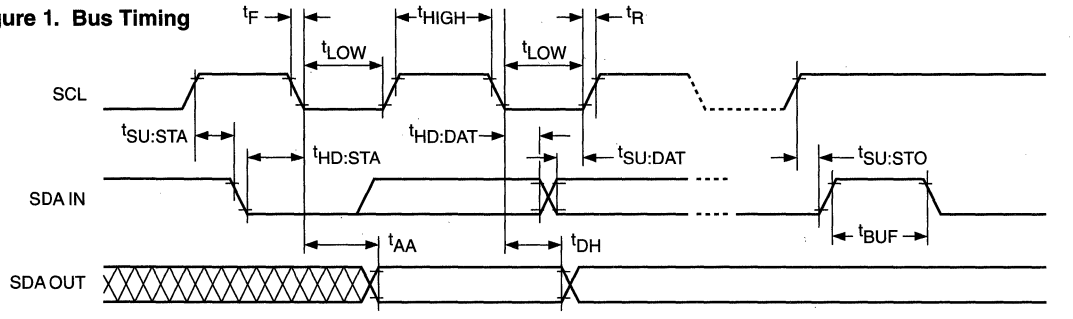

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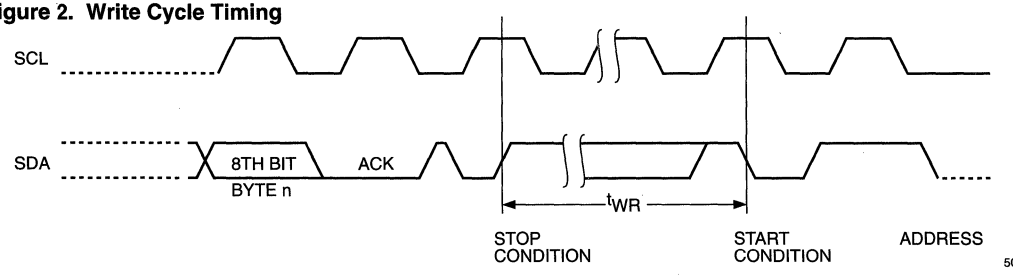
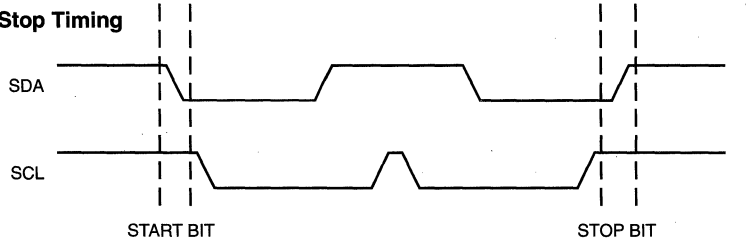
Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



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I²C BUS PROTOCOL

The features of the I²C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C32/64 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 (Fig. 5). The next three bits (A2, A1, A0) are the device address bits; up to eight 32K/64K devices may be connected to the same bus. These bits must compare to the hardwired input pins, A2, A1 and A0. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24C32/64 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C32/64 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

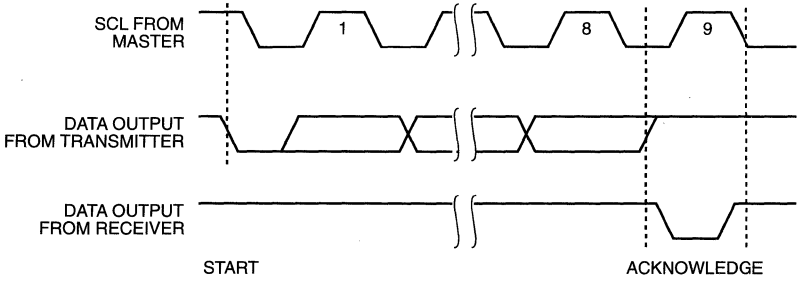
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24C32/64 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24C32/64 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C32/64 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

5027 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8-bit address words that are to be written into the address pointers of the CAT24C32/64. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24C32/64 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C32/64 writes up to 32 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 31 additional bytes. After each byte has been transmitted, CAT24C32/64 will respond with an acknowledge, and internally increment the five low order address bits by one. The high order bits remain unchanged.

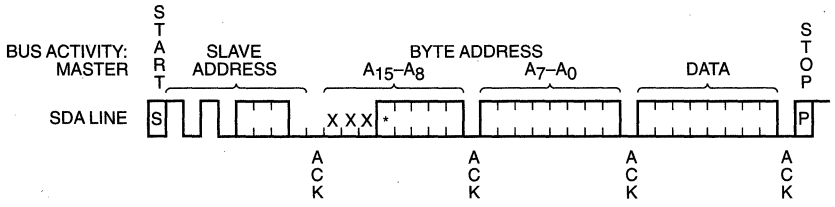
If the Master transmits more than 32 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 32 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24C32/64 in a single write cycle.

Acknowledge Polling

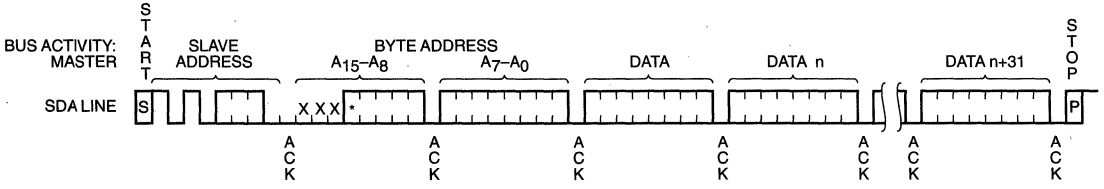
Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, CAT24C32/64 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24C32/64 is still busy with the write operation, no ACK will be returned. If CAT24C32/64 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



24C32/64 F08

Figure 7. Page Write Timing



*** = Don't care for 24C32**

24C32/64 F09

READ OPERATIONS

The READ operation for the CAT24C32/64 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Immediate/Current Address Read

The CAT24C32/64's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E=4095 for 24C32 and E=8191 for 24C64), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C32/64 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

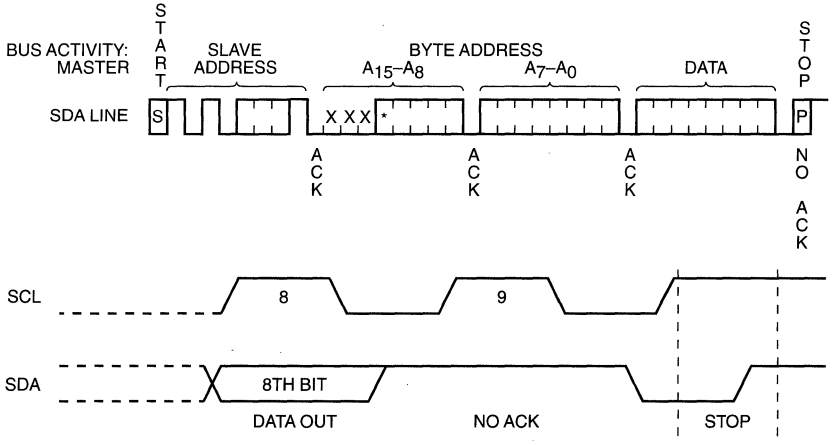
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24C32/64 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT24C32/64 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C32/64 sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C32/64 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from CAT24C32/64 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C32/64 address bits so that the entire memory array can be read during one operation. If more than E (where E=4095 for 24C32 and E=8191 for 24C64) bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

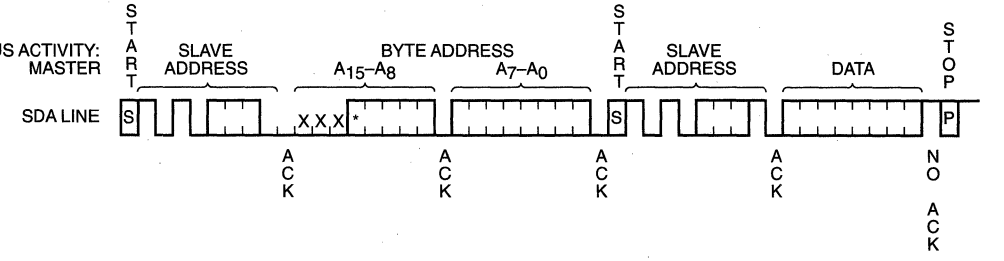
Figure 8. Immediate Address Read Timing



24C32/64 F10

*** = Don't care for 24C32**

Figure 9. Selective Read Timing

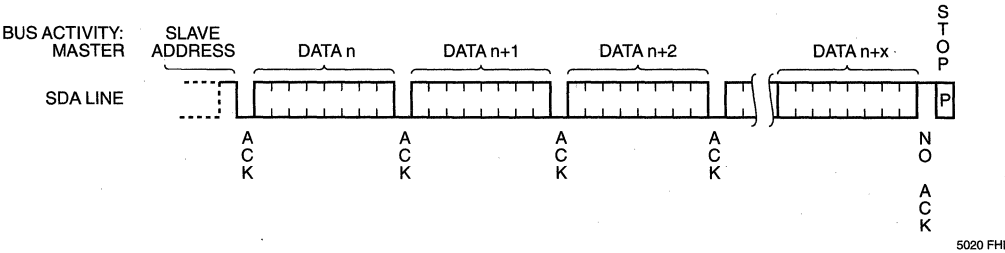


2

* = Don't care for 24C32

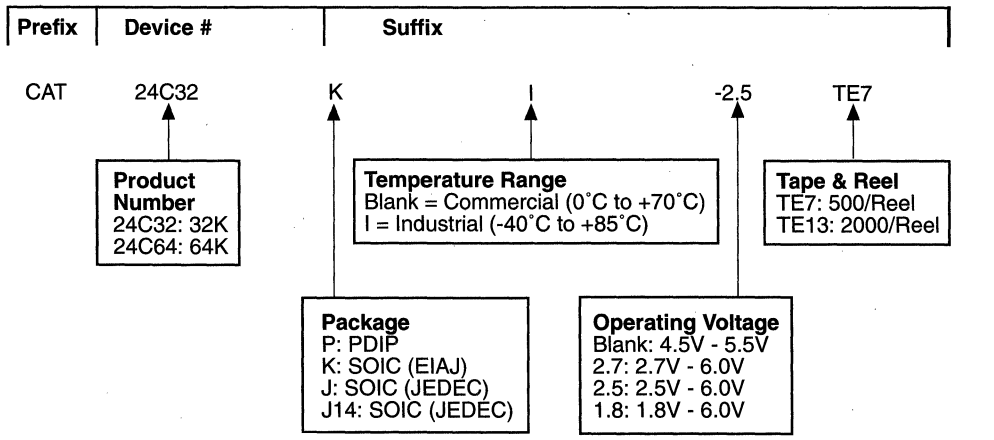
24C32/64 F11

Figure 10. Sequential Read Timing



5020 FHD F12

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 24C32KI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CAT24WC32/64

32K/64K-Bit Serial CMOS E²PROM

FEATURES

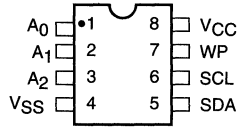
- 400 KHz I²C Bus Compatible*
- 1.8 to 6 Volt Operation
- Low Power CMOS Technology
- 32-Byte Page Write Buffer
- Commercial and Industrial Temperature Ranges
- Self-Timed Write Cycle with Auto-Clear
- Write Protect Feature
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-Pin DIP or 8-Pin SOIC

DESCRIPTION

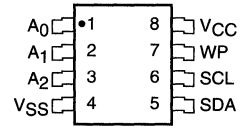
The CAT24WC32/64 is a 32K/64K-bit Serial CMOS E²PROM internally organized as 4096/8192 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24WC32/64 features a 32-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP or 8-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (J,K)

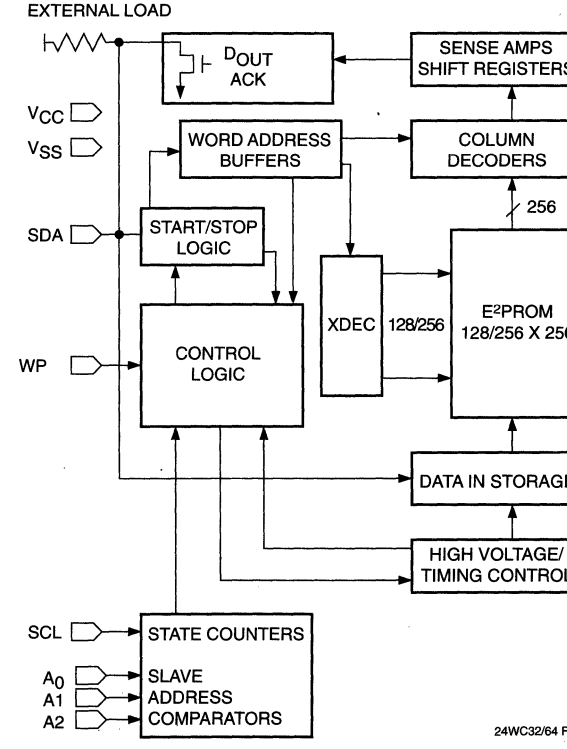


24WC32/64 F01

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+1.8V to +6V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



24WC32/64 F02

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

2

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}(5)	Standby Current (V_{CC} = 5V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = +3.0V)			0.4	V	I_{OL} = 3.0 mA
V_{OL2}	Output Low Voltage (V_{CC} = +1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL, WP)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby current (I_{SB}) = 0 µA (<900 nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6V, unless otherwise specified
Output Load is 1 TTL Gate and 100pF

Read & Write Cycle Limits

Symbol	Parameter	V_{CC}=1.8V - 6V		V_{CC}=4.5V - 5.5V		Units
		Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing (1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	1	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

FUNCTIONAL DESCRIPTION

The CAT24WC32/64 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC32/64 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

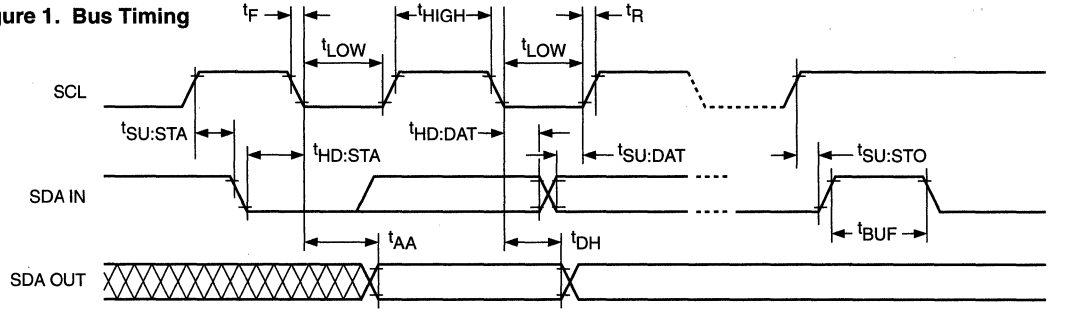
SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These pins are hardwired or left unconnected (for hardware compatibility with CAT24WC16). When hardwired, up to eight CAT24WC32/64s may be addressed on a single bus system (refer to Device Addressing). When the pins are left unconnected, the default values are zeros.

WP: write protect

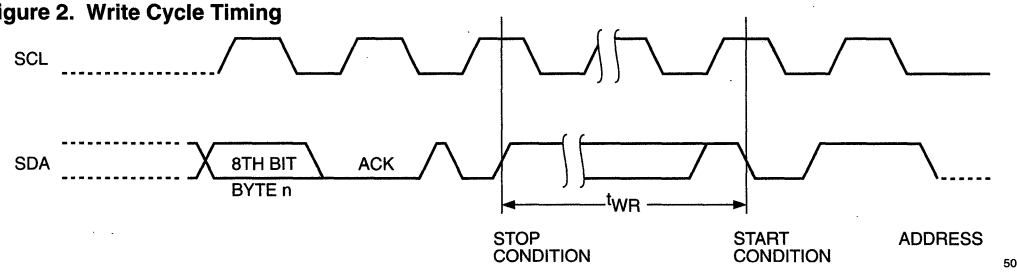
This input, when tied to GND, allows write operations to the entire memory. When this pin is tied to Vcc, the entire memory is write protected. When left floating, memory is unprotected.

Figure 1. Bus Timing



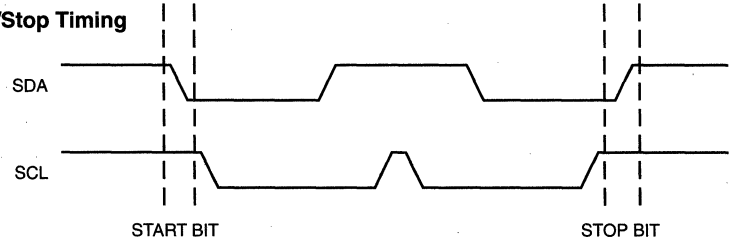
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The features of the I²C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC32/64 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 (Fig. 5). The next three bits (A2, A1, A0) are the device address bits; up to eight 32K/64K devices may to be connected to the same bus. These bits must compare to the hardwired input pins, A2, A1 and A0. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24WC32/64 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC32/64 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

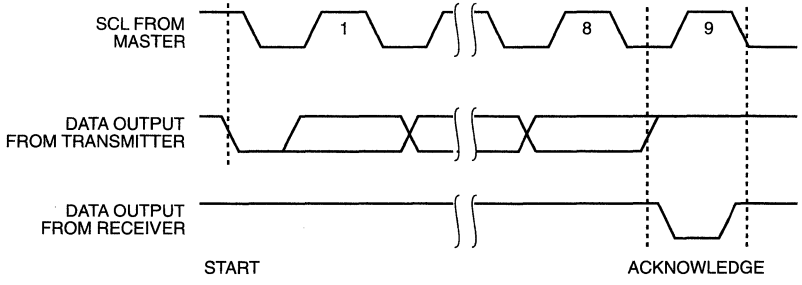
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC32/64 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24WC32/64 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC32/64 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

5027 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8-bit address words that are to be written into the address pointers of the CAT24WC32/64. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24WC32/64 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24WC32/64 writes up to 32 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 31 additional bytes. After each byte has been transmitted, CAT24WC32/64 will respond with an acknowledge, and internally increment the five low order address bits by one. The high order bits remain unchanged.

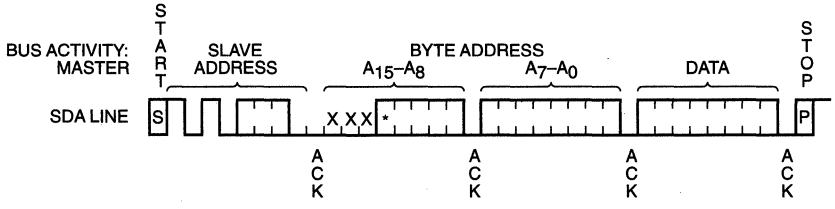
If the Master transmits more than 32 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 32 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24WC32/64 in a single write cycle.

Acknowledge Polling

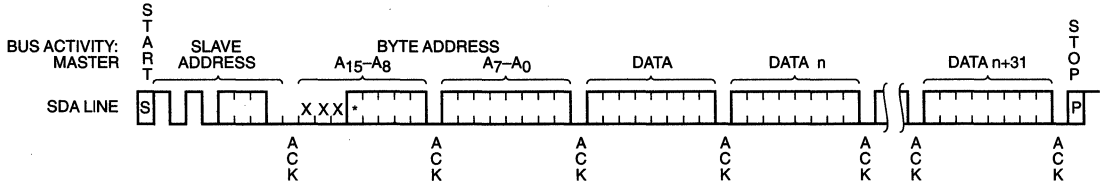
Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, CAT24WC32/64 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24WC32/64 is still busy with the write operation, no ACK will be returned. If CAT24WC32/64 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



24WC32/64 F08

Figure 7. Page Write Timing



*** = Don't care for 24WC32**

24WC32/64 F09

READ OPERATIONS

The READ operation for the CAT24WC32/64 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Immediate/Current Address Read

The CAT24WC32/64's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E=4095 for 24WC32 and E=8191 for 24WC64), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24WC32/64 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8 bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

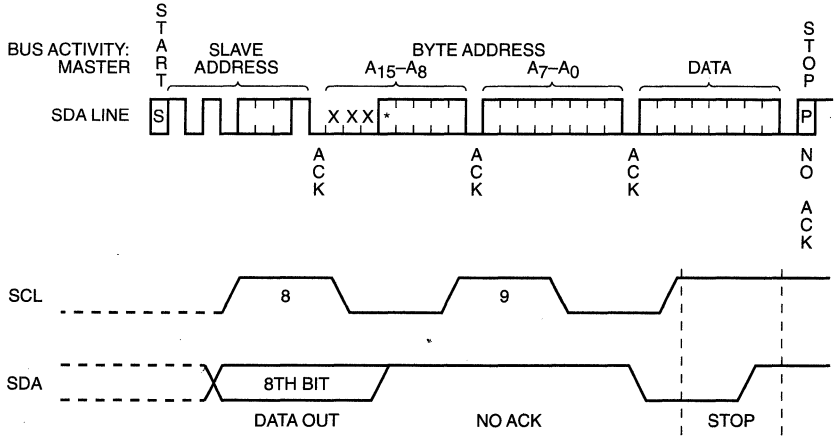
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24WC32/64 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT24WC32/64 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24WC32/64 sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC32/64 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from CAT24WC32/64 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC32/64 address bits so that the entire memory array can be read during one operation. If more than E (where E=4095 for 24WC32 and E=8191 for 24WC64) bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

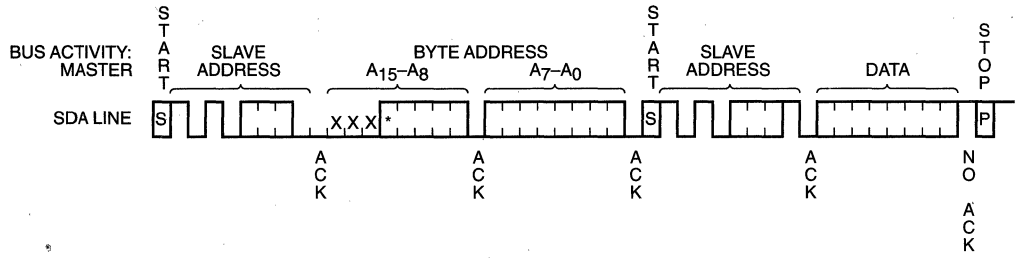
Figure 8. Immediate Address Read Timing



24WC32/64 F10

*** = Don't care for 24WC32**

Figure 9. Selective Read Timing

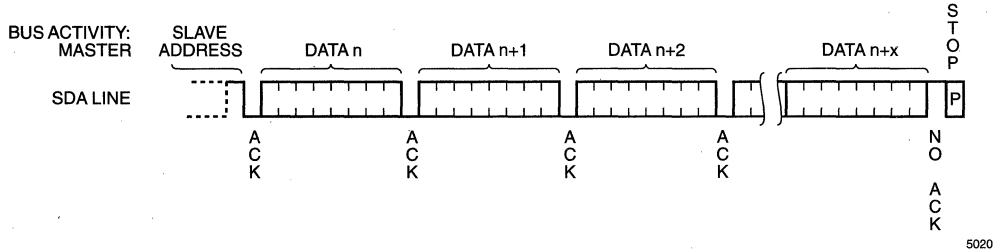


2

*** = Don't care for 24WC32**

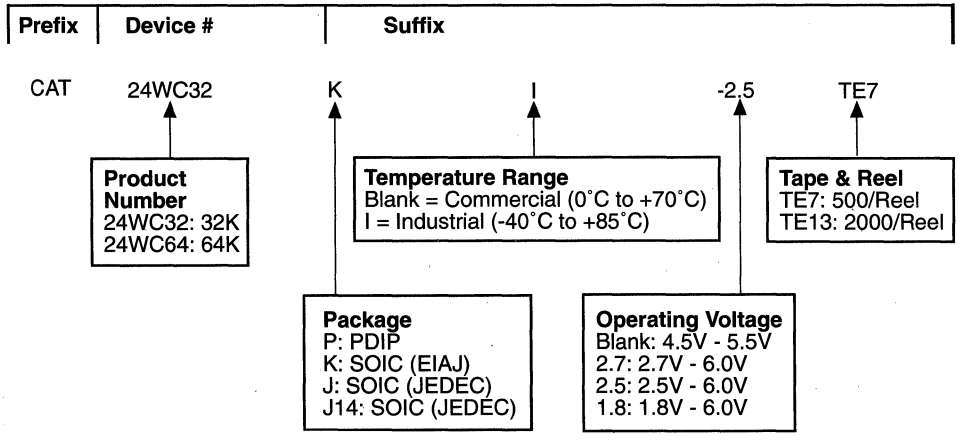
24WC32/64 F11

Figure 10. Sequential Read Timing



5020 FHD F12

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 24WC32KI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CATALYST SEMICONDUCTOR

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Section 3 Microwire Bus Serial E²PROMs

CAT93C46/56/66/86 ..... 1K/2K/4K/16K-Bit 3-1

CAT93C46A/56A/66A/86A ..... 1K/2K/4K/16K-Bit No ORG Pin 3-9

CAT93C57 ..... 2K-Bit 3-17

CAT93C46/56/66/86

1K/2K/4K/16K-Bit Serial E²PROM

FEATURES

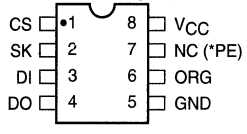
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Wide Operating Voltage Range
  - V_{cc} = 4.5V to 5.5V
  - V_{cc} = 2.7V to 6.0V
  - V_{cc} = 2.5V to 6.0V
  - V_{cc} = 1.8V to 6.0V
- Selectable x8 or x16 Memory Organization
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial and Industrial Temperature Ranges

DESCRIPTION

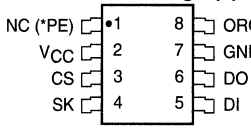
The CAT93C46/56/66/86 are 1K/2K/4K/16K-bit Serial E²PROM memory devices which are configured as either registers of 16 bits (ORG pin at V_{CC}) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46/56/66/86 are manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. The devices are designed to endure 100,000 program/erase cycles and have a data retention of 100 years. The devices are available in 8-pin DIP or SOIC packages.

PIN CONFIGURATION

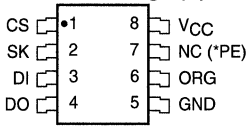
DIP Package (P)



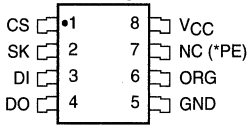
SOIC Package (J)



SOIC Package (S)



SOIC Package (K)



*PE (only for 93C86)

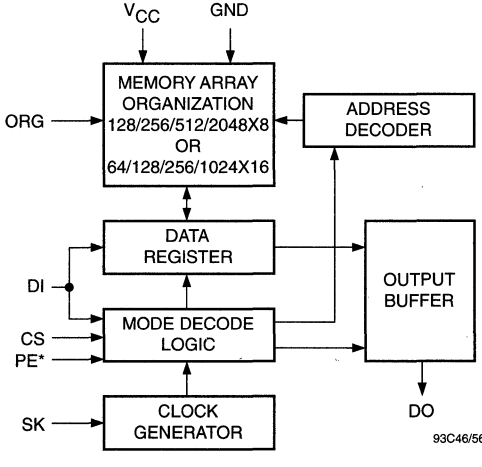
93C46/56/66 F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8 to 6.0V Power Supply
GND	Ground
ORG	Memory Organization
PE*	Program Enable
NC	No Connection

Note: When the ORG pin is connected to VCC, the X16 organization is selected. When it is connected to ground, the X8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the X16 organization.

BLOCK DIAGRAM



93C46/56/66 F02

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

3

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f_{SK} = 1MHz V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{SB}	Power Supply Current (Standby)			50	µA	CS = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (Including ORG pin)			10	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V_{CC}+1	V V	4.5V≤V_{CC}<5.5V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 V_{CC}X0.7		V_{CC}X0.2 V_{CC}+1	V V	1.8V≤V_{CC}<2.7V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	 2.4		0.4	V V	4.5V≤V_{CC}<5.5V I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	 V_{CC}-0.2		0.2	V V	1.8V≤V_{CC}<2.7V I_{OL} = 1mA I_{OH} = -100µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}(1)	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}(1)	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V_{IN}=OV

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

INSTRUCTION SET

Instruction	Device Type	Start Bit	Opcode	Address		Data		PE(1)	Comments
				x8	x16	x8	x16		
READ	93C46	1	10	A6–A0	A5-A0				Read Address AN–A0
	93C56(2)	1	10	A8–A0	A7-A0				
	93C66	1	10	A8–A0	A7-A0				
	93C86	1	10	A10-A0	A9-A0			X	
ERASE	93C46	1	11	A6–A0	A5-A0				Clear Address AN–A0
	93C56(2)	1	11	A8–A0	A7-A0				
	93C66	1	11	A8–A0	A7-A0				
	93C86	1	11	A10-A0	A9-A0			1	
WRITE	93C46	1	01	A6–A0	A5-A0	D7-D0	D15-D0		Write Address AN–A0
	93C56(2)	1	01	A8–A0	A7-A0	D7-D0	D15-D0		
	93C66	1	01	A8–A0	A7-A0	D7-D0	D15-D0		
	93C86	1	01	A10-A0	A9-A0	D7-D0	D15-D0	1	
EWEN	93C46	1	00	11XXXXX	11XXXX				Write Enable
	93C56	1	00	11XXXXXXX	11XXXXXX				
	93C66	1	00	11XXXXXXX	11XXXXXX				
	93C86	1	00	11XXXXXXXXX	11XXXXXXXX			X	
EWDS	93C46	1	00	00XXXXX	00XXXX				Write Disable
	93C56	1	00	00XXXXXXX	00XXXXXX				
	93C66	1	00	00XXXXXXX	00XXXXXX				
	93C86	1	00	00XXXXXXXXX	00XXXXXXXX			X	
ERAL	93C46	1	00	10XXXXX	10XXXX				Clear All Addresses
	93C56	1	00	10XXXXXXX	10XXXXXX				
	93C66	1	00	10XXXXXXX	10XXXXXX				
	93C86	1	00	10XXXXXXXXX	10XXXXXXXX			1	
WRAL	93C46	1	00	01XXXXX	01XXXX	D7-D0	D15-D0		Write All Addresses
	93C56	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0		
	93C66	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0		
	93C86	1	00	01XXXXXXXXX	01XXXXXXXX	D7-D0	D15-D0	1	

Note:
(1) Only applicable to 93C86
(2) Address bit A8 for 256x8 ORG and A7 for 128x16 ORG are "Don't Care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits						UNITS	Test Conditions
		V_{CC} = 1.8V-6V*		V_{CC} = 2.7V -6V V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSS}	CS Setup Time	200		100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	400		200		100		ns	
t_{DIH}	DI Hold Time	400		200		100		ns	
t_{PD1}	Output Delay to 1		1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		1		0.5		0.25	µs	
t_{HZ}(1)	Output Delay to High-Z		400		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	KHZ	

* Preliminary data for 93C56/66/86.

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

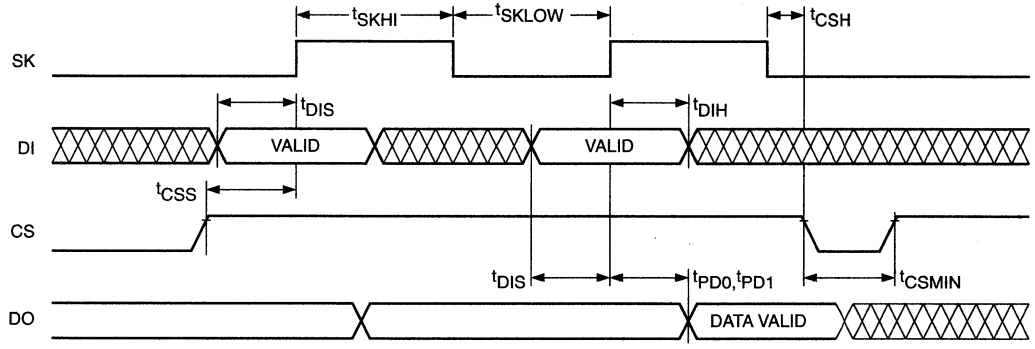
DEVICE OPERATION

The CAT93C46/56/66/86 is a 1024/2048/4096/16384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46/56/66/86 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions for 93C46; seven 11-bit instructions for 93C56 and 93C66; seven 13-bit instructions for 93C86, control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions for 93C46; seven 12-bit instructions for 93C56 and 93C66; seven 14-bit instructions for 93C86, control the reading, writing and erase operations of the device. The CAT93C46/56/66/86 operates on a single 1.8V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

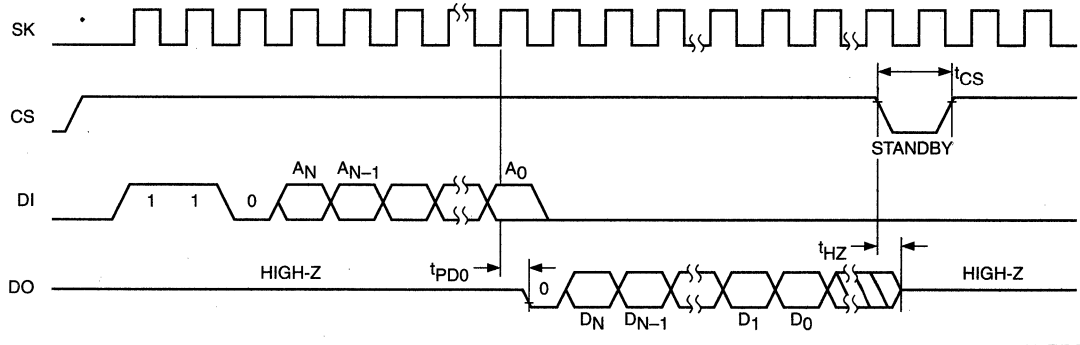
The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

Figure 1. Sychronous Data Timing



5040 FHD F03

Figure 2. Read Instruction Timing



5040 FHD F04

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit (93C46)/ 8-bit (93C56 or 93C66)/10-bit (93C86) (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46/ 56/66/86 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/66/86 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/ busy status of the CAT93C46/56/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Figure 3. Write Instruction Timing

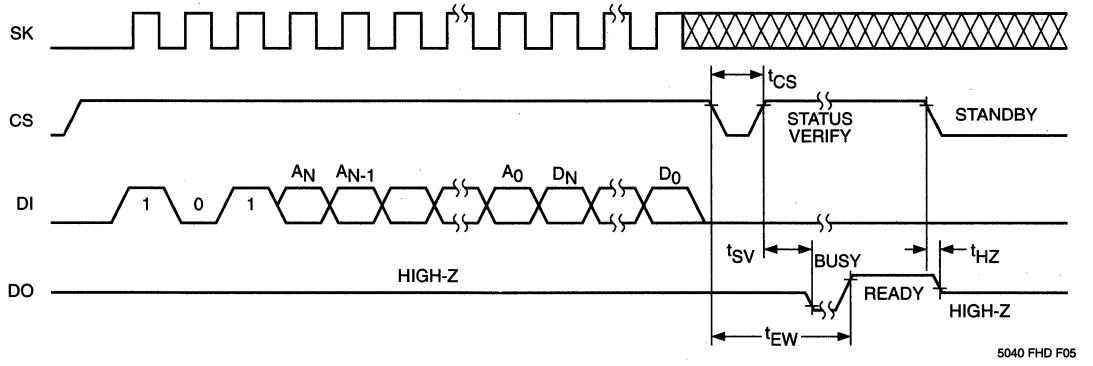
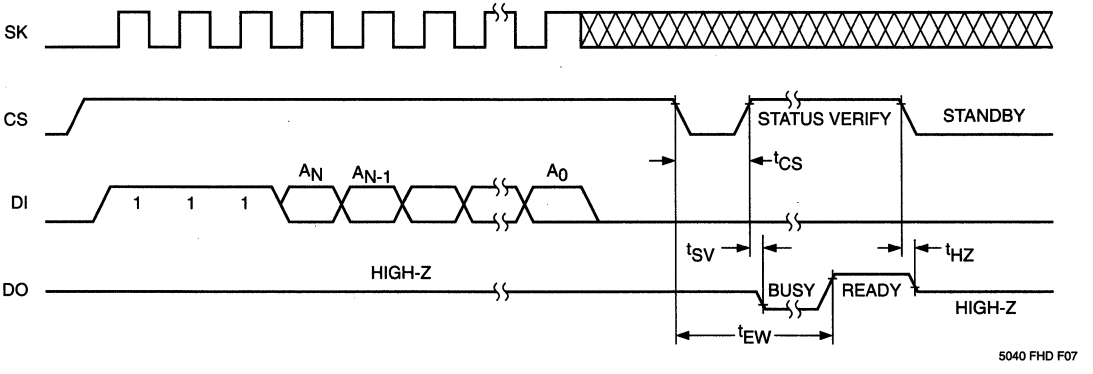


Figure 4. Erase Instruction Timing



Erase/Write Enable and Disable

The CAT93C46/56/66/86 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46/56/66/86 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

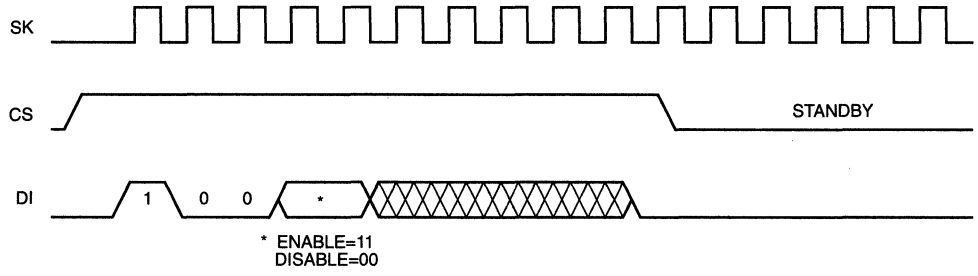
Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/66/86 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note: This note is applicable only to 93C86. The write, erase, write all and, erase all instruction requires PE=1 for 93C86. If PE is left floating, 93C86 is in program enabled mode.

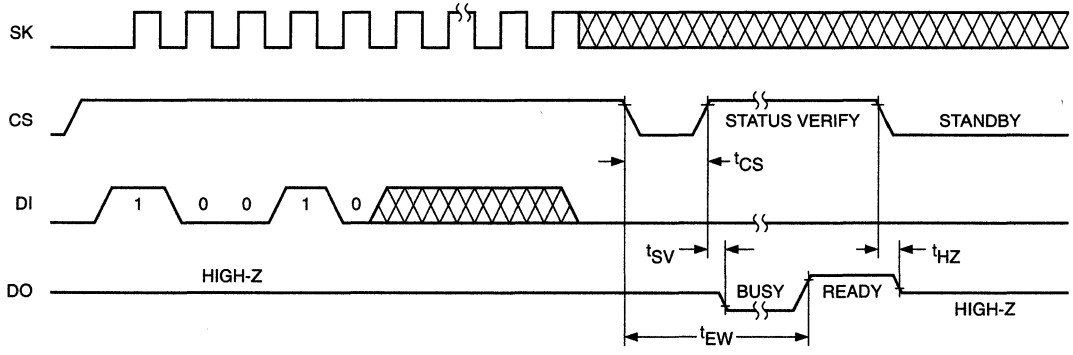
3

Figure 5. EWEN/EWDS Instruction Timing



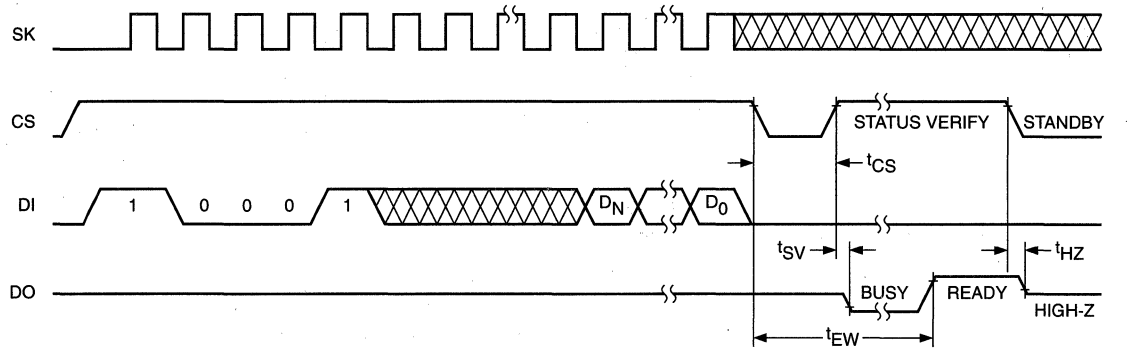
93C46/56/66 F07

Figure 6. ERAL Instruction Timing



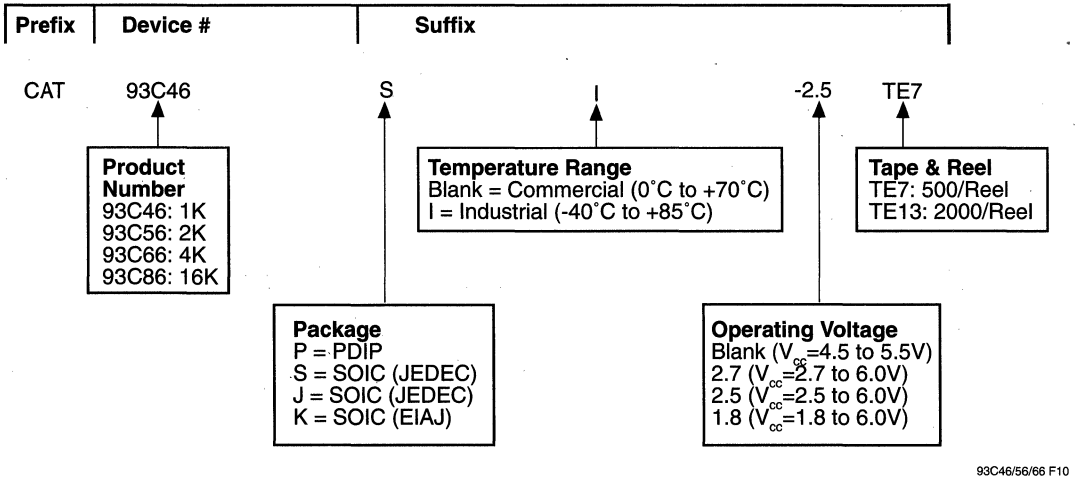
5040 FHD F08

Figure 7. WRAL Instruction Timing



93C46/56/66 F09

ORDERING INFORMATION



93C46/56/66 F10

Notes:
(1) The device used in the above example is a 93C46SI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CAT93C46A/56A/66A/86A

1K/2K/4K/16K-Bit Serial E²PROM

FEATURES

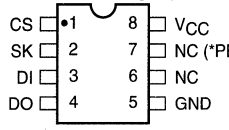
- **High Speed Operation: 1MHz**
- **Low Power CMOS Technology**
- **Wide Operating Voltage Range**
  - V_{CC} = 4.5V to 5.5V
  - V_{CC} = 2.7V to 6.0V
  - V_{CC} = 2.5V to 6.0V
  - V_{CC} = 1.8V to 6.0V
- **Self-Timed Write Cycle with Auto-Clear**
- **Hardware and Software Write Protection**
- **Power-Up Inadvertant Write Protection**
- **100,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial and Industrial Temperature Ranges**
- **x16 Serial Memory**

DESCRIPTION

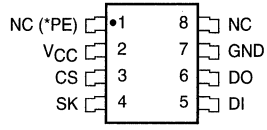
The CAT93C46A/56A/66A/86A is a 1K/2K/4K/16K-bit Serial E²PROM memory devices which are configured as registers of 16-bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46A/56A/66A/86A are manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. The devices are designed to endure 100,000 program/erase cycles and have a data retention of 100 years. The devices are available in 8-pin DIP or SOIC packages.

PIN CONFIGURATION

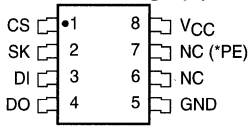
DIP Package (P)



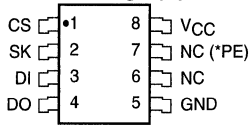
SOIC Package (J)



SOIC Package (S)



SOIC Package (K)



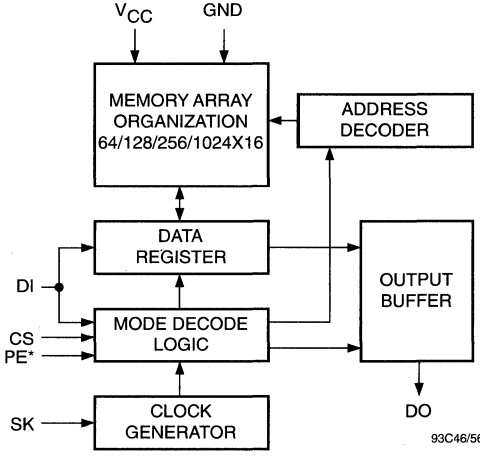
*PE (only for 93C86A)

93CXXA F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8V to 6.0V Power Supply
GND	Ground
PE*	Program Enable
NC	No Connect

BLOCK DIAGRAM



93C46/56/66 F02

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

3

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f_{SK} = 1MHz V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{SB}	Power Supply Current (Standby)			50	µA	CS = 0V
I_{LI}	Input Leakage Current			2	µA	
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V_{CC}+1	V V	4.5V≤V_{CC}<5.5V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 V_{CC}X0.7		V_{CC}X0.2 V_{CC}+1	V V	1.8V≤V_{CC}<2.7V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	 2.4		0.4	V V	4.5V≤V_{CC}<5.5V I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	 V_{CC}-0.2		0.2	V V	1.8V≤V_{CC}<2.7V I_{OL} = 1mA I_{OH} = -100µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}[1]	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}[1]	INPUT CAPACITANCE (CS, SK, DI)	5	pF	V_{IN}=OV

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

INSTRUCTION SET

Instruction	Device Type	Start Bit	Opcode	Address x16	Data x16	PE[1]	Comments
READ	93C46A	1	10	A5-A0			Read Address AN–A0
	93C56A[2]	1	10	A7-A0			
	93C66A	1	10	A7-A0			
	93C86A	1	10	A9-A0		X	
ERASE	93C46A	1	11	A5-A0			Clear Address AN–A0
	93C56A[2]	1	11	A7-A0			
	93C66A	1	11	A7-A0			
	93C86A	1	11	A9-A0		1	
WRITE	93C46A	1	01	A5-A0	D15-D0		Write Address AN–A0
	93C56A[2]	1	01	A7-A0	D15-D0		
	93C66A	1	01	A7-A0	D15-D0		
	93C86A	1	01	A9-A0	D15-D0	1	
EWEN	93C46A	1	00	11XXXX			Write Enable
	93C56A	1	00	11XXXXXX			
	93C66A	1	00	11XXXXXX			
	93C86A	1	00	11XXXXXXXX		X	
EWDS	93C46A	1	00	00XXXX			Write Disable
	93C56A	1	00	00XXXXXX			
	93C66A	1	00	00XXXXXX			
	93C86A	1	00	00XXXXXXXX		X	
ERAL	93C46A	1	00	10XXXX			Clear All Addresses
	93C56A	1	00	10XXXXXX			
	93C66A	1	00	10XXXXXX			
	93C86A	1	00	10XXXXXXXX		1	
WRAL	93C46A	1	00	01XXXX	D15-D0		Write All Addresses
	93C56A	1	00	01XXXXXX	D15-D0		
	93C66A	1	00	01XXXXXX	D15-D0		
	93C86A	1	00	01XXXXXXXX	D15-D0	1	

Note:
(1) Only applicable to 93C86A
(2) Address bit A7 is "Don't Care" bit, but must be kept at either a "1" or "0" for Read, Write and Erase Commands.

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits						UNITS	Test Conditions
		V_{CC} = 1.8V-6V*		V_{CC} = 2.7V -6V V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSS}	CS Setup Time	200		100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	400		200		100		ns	
t_{DIH}	DI Hold Time	400		200		100		ns	
t_{PD1}	Output Delay to 1		1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		1		0.5		0.25	µs	
t_{HZ}(1)	Output Delay to High-Z		400		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	KHZ	

* Preliminary data for 93C56A/66A/86A.

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT93C46A/56A/66A/86A is a 1024/2048/4096/16384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46A/56A/66A/86A is organized as registers of 16-bits. Therefore, seven 9-bit instructions for 93C46A; seven 11-bit instructions for 93C56A and 93C66A; seven 13-bit instructions for 93C86A, control the reading, writing and erase operations of the device. The CAT93C46A/56A/66A/86A operates on a single supply and will generate on chip, the high voltage required during any write operation.

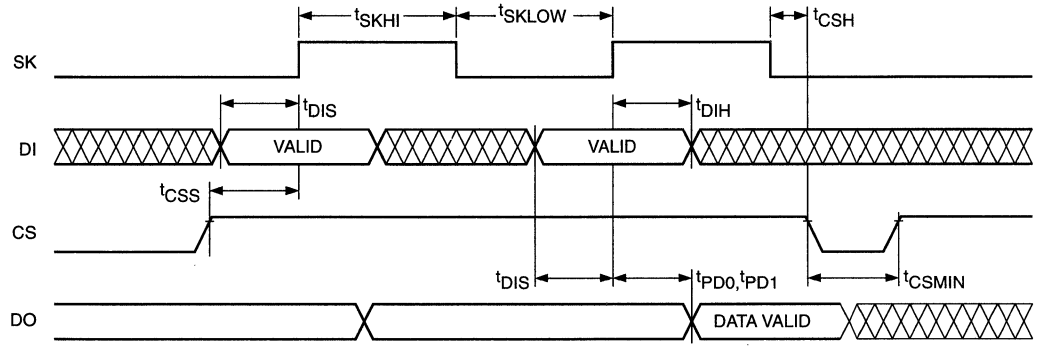
Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit (93C46A)/8-bit (93C56A or 93C66A)/10-bit (93C86A) and for write operations a 16-bit data field.

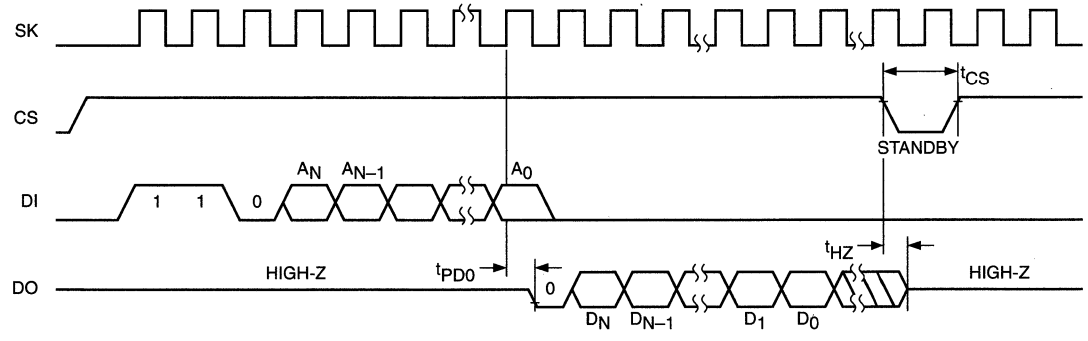
3

Figure 1. Sychronous Data Timing



5040 FHD F03

Figure 2. Read Instruction Timing



5040 FHD F04

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46A/56A/66A/86A will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Figure 3. Write Instruction Timing

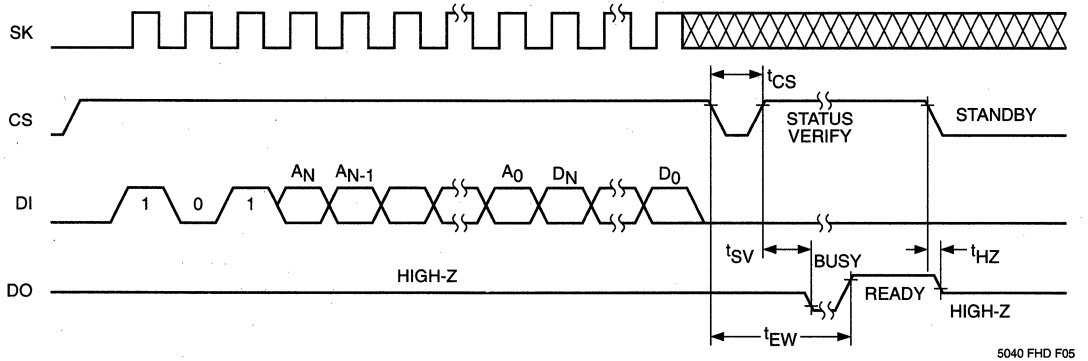
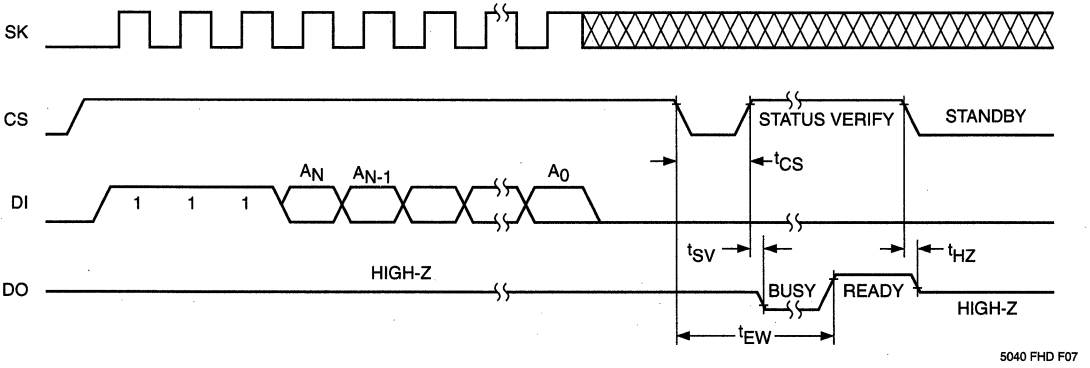


Figure 4. Erase Instruction Timing



Erase/Write Enable and Disable

The CAT93C46A/56A/66A/86A powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

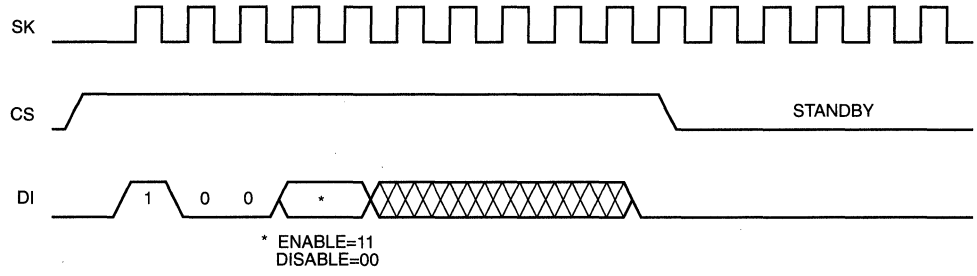
Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/56A/66A/86A can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note: This note is applicable only to 93C86A. The write, erase, write all and erase all instruction requires PE=1 for 93C86A. If PE is left floating, 93C86A is in program enabled mode.

3

Figure 5. EWEN/EWDS Instruction Timing



93C46/56/66 F07

Figure 6. ERAL Instruction Timing

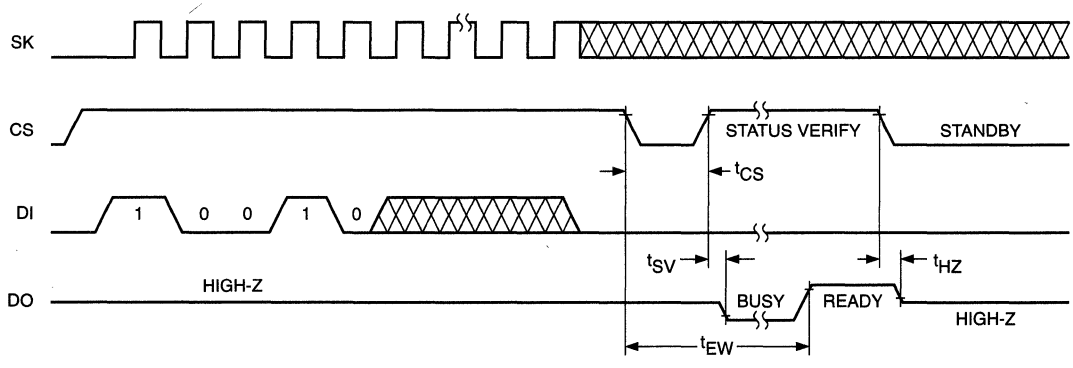


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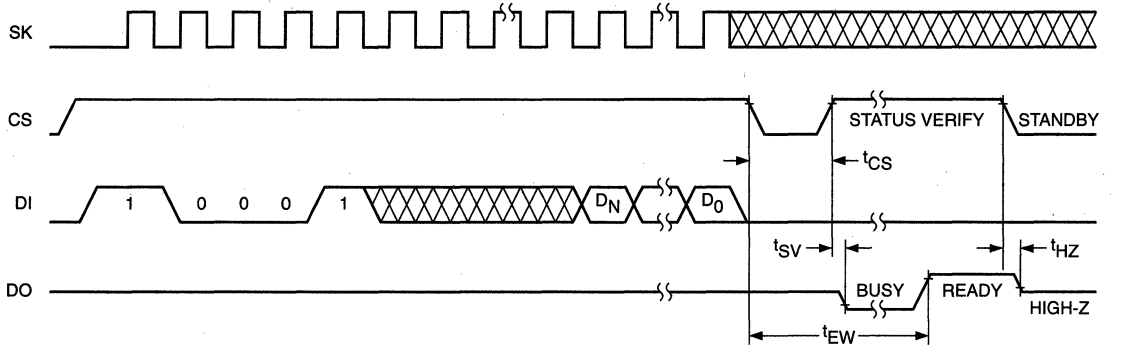
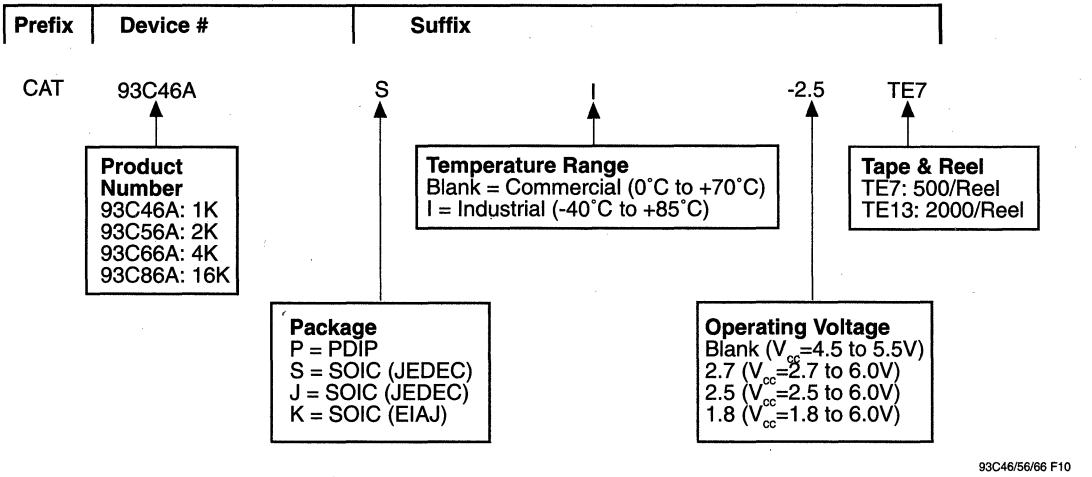
Figure 7. WRAL Instruction Timing



93C46/56/66 F09

3

ORDERING INFORMATION



93C46/56/66 F10

Notes:
(1) The device used in the above example is a 93C46ASI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CAT93C57

2K-Bit Serial E²PROM

FEATURES

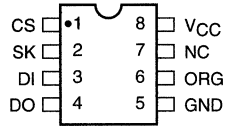
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Wide Operating Voltage Range
  - V_{CC} = 4.5V to 5.5V
  - V_{CC} = 2.7V to 6.0V
  - V_{CC} = 2.5V to 6.0V
  - V_{CC} = 1.8V to 6.0V
- Selectable x8 or x16 Memory Organization
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read Operation
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial and Industrial Temperature Ranges

DESCRIPTION

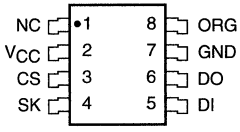
The CAT93C57 is 2K-bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C57 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP or SOIC packages.

PIN CONFIGURATION

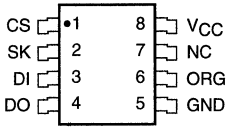
DIP Package (P)



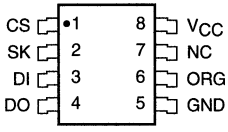
SOIC Package (J)



SOIC Package (S)



SOIC Package (K)



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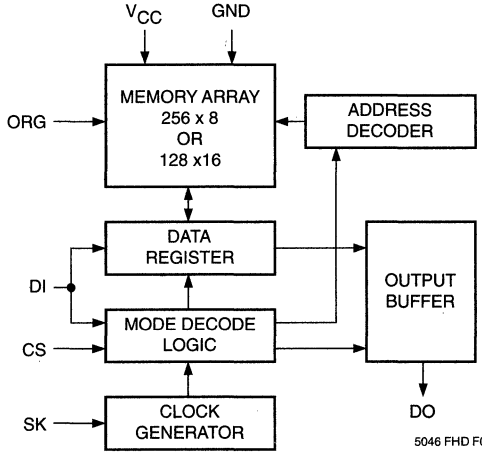
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	1.8V to 6.0V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

3

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to 6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f_{SK} = 1MHz V_{CC} = 5.0V, CS = 5.0V Output Open
I_{SB}	Power Supply Current (Standby)			50	µA	CS = 0V
I_{LO}	Input Leakage Current			2	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{ILI} V_{IHI}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V_{CC}+1	V V	4.5V≤V_{CC}<5.5V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 V_{CC}X0.7		V_{CC}X0.2 V_{CC}+1	V V	1.8V≤V_{CC}<2.7V
V_{OLI} V_{OHI}	Output Low Voltage Output High Voltage	 2.4		0.4	V V	4.5V≤V_{CC}<5.5V I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	 V_{CC}-0.2		0.2	V V	1.8V≤V_{CC}<2.7V I_{OL} = 1mA I_{OH} = -100µA

(1) The minimum DC input is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0	A7–A0	A6–A0			Read Address AN–A0
ERASE	1	1 1	A7–A0	A6–A0			Clear Address AN–A0
WRITE	1	0 1	A7–A0	A6–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXX	11XXXXX			Write Enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Write Disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Clear All Addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	D7–D0	D15–D0	Write All Addresses

3

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}(1)	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}(1)	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V_{IN}=OV

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits						UNITS	Test Conditions
		V_{CC} = 1.8V-6V*		V_{CC} = 2.7V -6V V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSS}	CS Setup Time	200		100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	400		200		100		ns	
t_{DIH}	DI Hold Time	400		200		100		ns	
t_{PD1}	Output Delay to 1		1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		1		0.5		0.25	µs	
t_{HZ}(3)	Output Delay to High-Z		400		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	KHZ	

Note:
* Preliminary data
(1) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

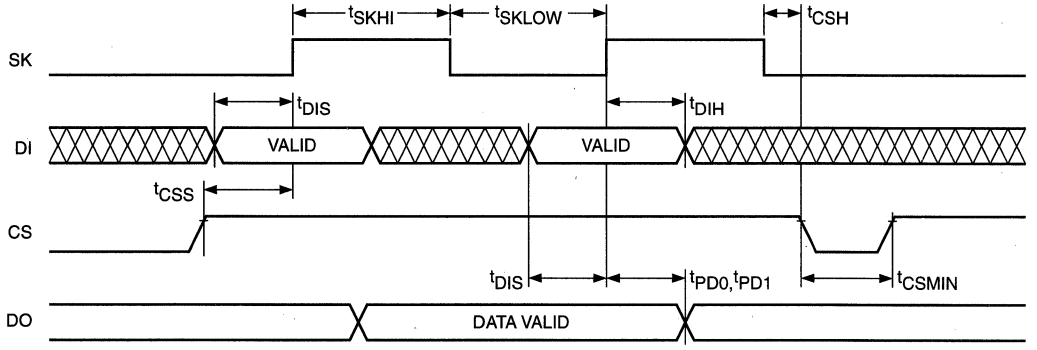
The CAT93C57 is a 2048-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C57 can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 10-bit instructions (11-bit instruction in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT93C57 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT93C57 is a logical "1" start bit, a 2-bit (or 4-bit) op code, a 7-bit address (8-bit address when organized as 256 x 8), and for write operations a 16-bit data field (8-bit data field when organized as 256 x 8).

Figure 1. Sychronous Data Timing (1)



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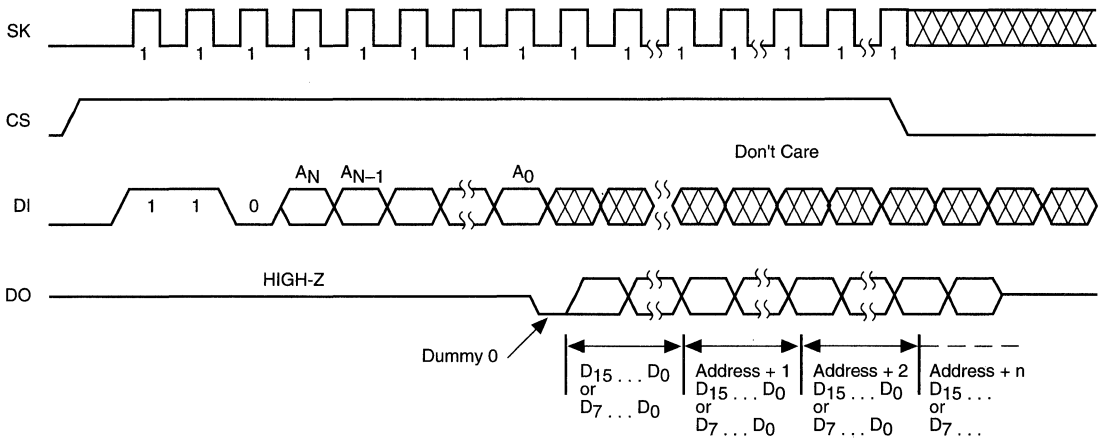
Note:
(1) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Figure 2. Read Instruction Timing (1)



Note:
(1) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C57 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C57 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Figure 3. Write Instruction Timing (1)

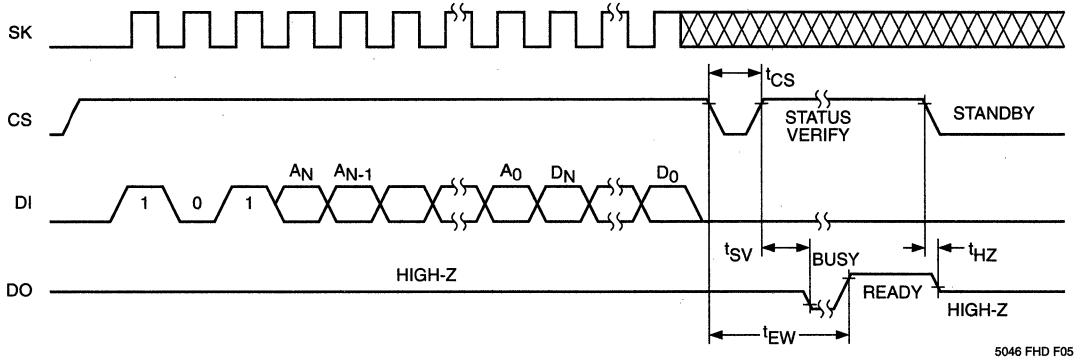
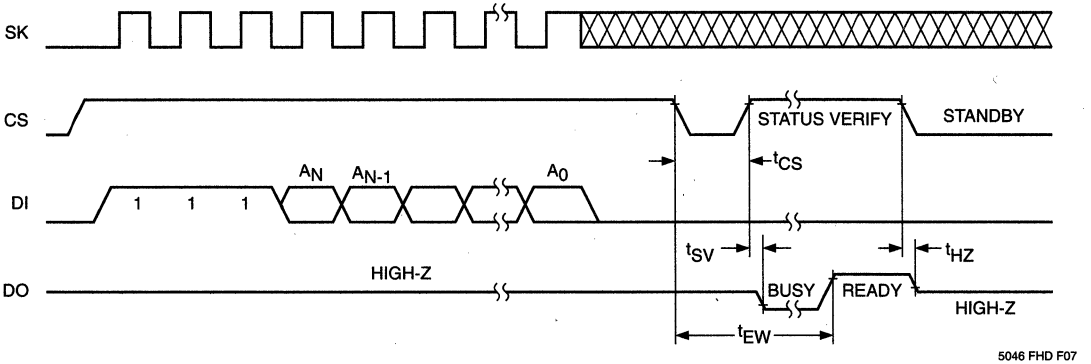


Figure 4. Erase Instruction Timing (1)



Note:
(1) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C57 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C57 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C57 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C57 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

3

Figure 5. EWEN/EWDS Instruction Timing (1)

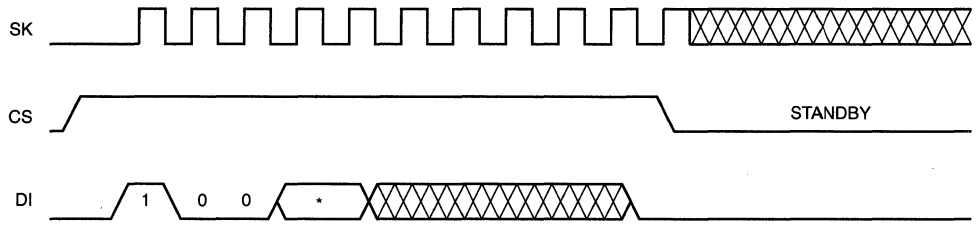
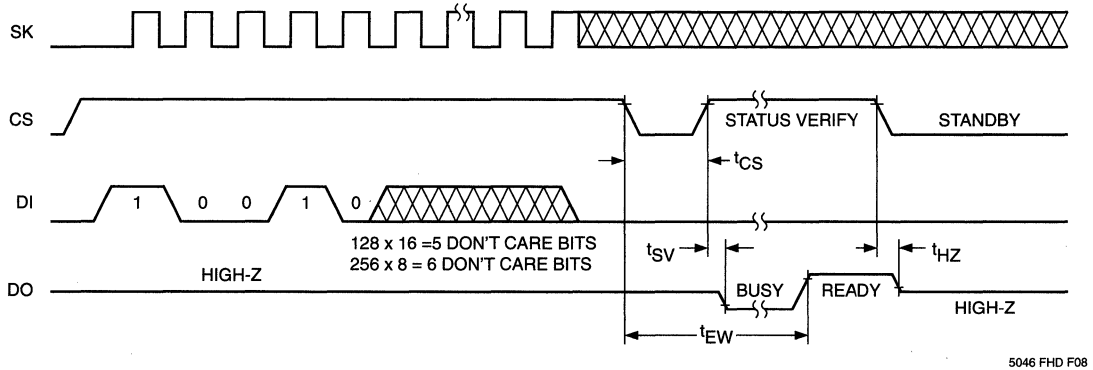


Figure 6. ERAL Instruction Timing (1)

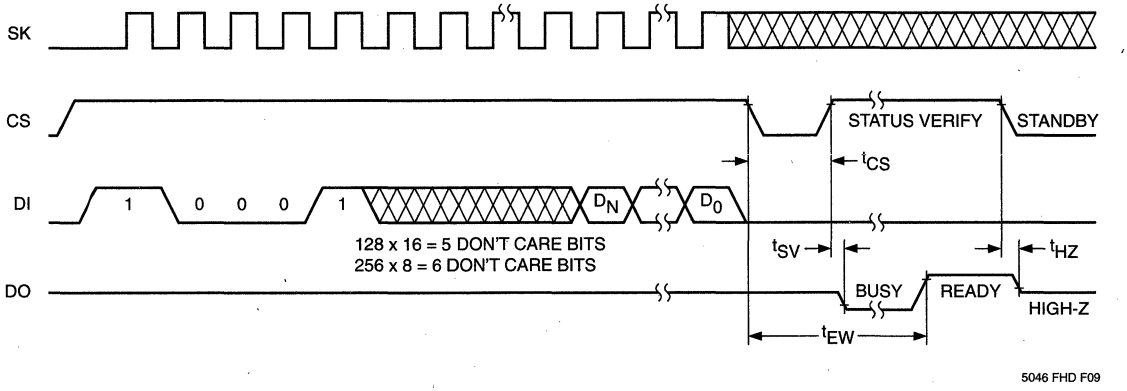


Note:
(1) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Write All

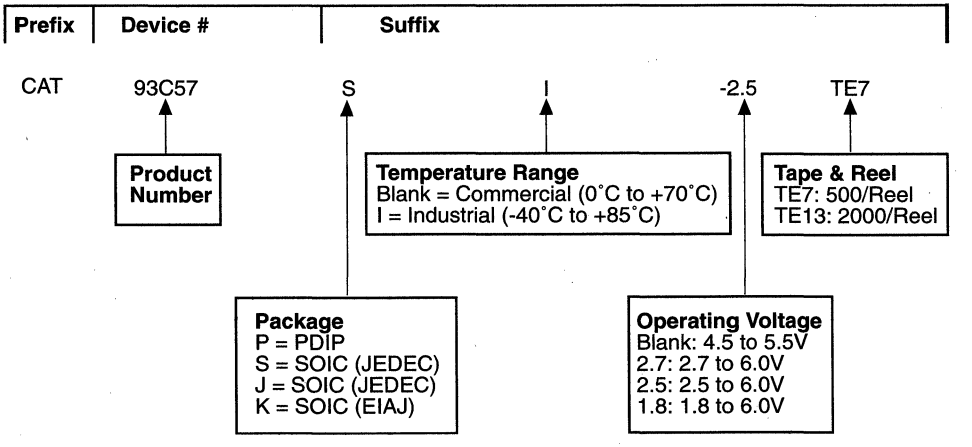
Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C57 can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (1)



Note:
(1) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

PIN CONFIGURATION



Notes:
(1) The device used in the above example is a 93C57SI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CATALYST SEMICONDUCTOR

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CAT64LC10/20/40 ..... 64/128/256 x 16 ..... 1K/2K/4K-Bit 4-1

CAT64LC10/20/40

1K/2K/4K-Bit Serial E²PROM

FEATURES

- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5V to 6.0V Operation
- Self-Timed Write Cycle with Auto-Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Commercial and Industrial Temperature Ranges
- Power-Up Inadvertant Write Protection
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Indication
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

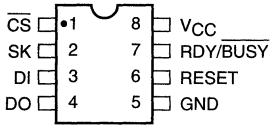
4

DESCRIPTION

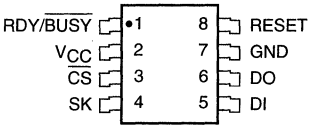
The CAT64LC10/20/40 is a 1K/2K/4K-bit Serial E²PROM which is configured as 64/128/256 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC10/20/40 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP or SOIC packages.

PIN CONFIGURATION

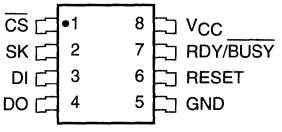
DIP Package (P)



SOIC Package (J)



SOIC Package (S)



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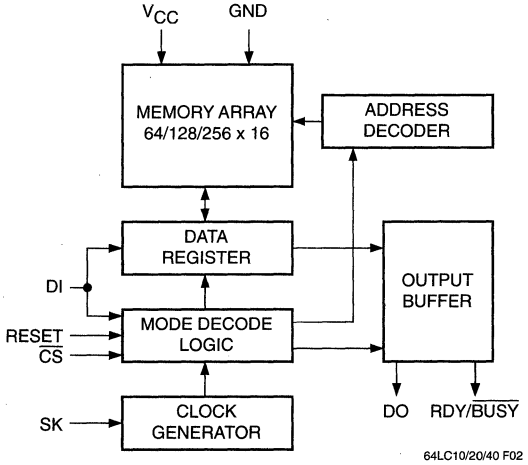
PIN FUNCTIONS

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.5V to +6.0V Power Supply
GND	Ground
RESET	Reset
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{BUSY}}$ Status

BLOCK DIAGRAM



64LC10/20/40 F02

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE (T_A = 25°C, f= 1.0 MHz, V_{CC} =6.0V)

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (DO, RDY/$\overline{BUSY}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance ($\overline{CS}$, SK, DI, RESET)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +6.0V, unless otherwise specified.

Sym.	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC}	Operating Current	2.5V			0.4	mA	f_{SK} = 250 kHz
	EWEN, EWDS, READ	6.0V			1	mA	f_{SK} = 1 MHz
I_{CCP}	Program Current	2.5V			2	mA	
		6.0V			3	mA	
I_{SB}(1)	Standby Current				0	µA	V_{IN} = GND or V_{CC} $\overline{CS}$ = V_{CC}
I_{LI}	Input Leakage Current				2	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Low Level Input Voltage, DI		–0.1		V_{CC} x 0.3	V	
V_{IH}	High Level Input Voltage, DI		V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage, $\overline{CS}$, SK, RESET		–0.1		V_{CC} x 0.2	V	
V_{IH}	High Level Input Voltage, $\overline{CS}$, SK, RESET		V_{CC} x 0.8		V_{CC} + 0.5	V	
V_{OH}(2)	High Level Output Voltage	2.5V	V_{CC} – 0.3			V	I_{OH} = –10µA
		6.0V	V_{CC} – 0.3				I_{OH} = –10µA
			2.4				I_{OH} = –400µA
V_{OL}(2)	Low Level Output Voltage	2.5V			0.4	V	I_{OL} = 10µA
		6.0V			0.4	V	I_{OL} = 2.1mA

Note:
(1) Standby Current (I_{SB}) = 0µA (<900nA) ____
(2) V_{OH} and V_{OL} spec applies to READY/BUSY pin also

A.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +6.0V, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units
t_{CSS}	$\overline{CS}$ Setup Time		100			ns
t_{CSH}	$\overline{CS}$ Hold Time		100			ns
t_{DIS}	DI Setup Time		200			ns
t_{DIH}	DI Hold Time		200			ns
t_{PD1}	Output Delay to 1				300	ns
t_{PD0}	Output Delay to 0				300	ns
t_{HZ}(2)	Output Delay to High Impendance				500	ns
t_{CSMIN}	Minimum $\overline{CS}$ High Time		250			ns
t_{SKHI}	Minimum SK High Time	2.5V	1000			ns
		4.5V–6.0V	400			
t_{SKLOW}	Minimum SK Low Time	2.5V	1000			ns
		4.5V–6.0V	400			
t_{SV}	Output Delay to Status Valid				500	ns
f_{SK}	Maximum Clock Frequency	2.5V	250			kHz
		4.5V–6.0V	1000			
t_{RESS}	Reset to $\overline{CS}$ Setup Time		0			ns
t_{RESMIN}	Minimum RESET High Time		250			ns
t_{RESH}	RESET to READY Hold Time		0			ns
t_{RC}	Write Recovery		100			ns

POWER-UP TIMING(1)(3)

Symbol	Parameter	Min.	Max.	Units
t_{PUR}	Power-Up to Read Operation		10	µs
t_{PUW}	Power-Up to Program Operation		1	ms

WRITE CYCLE LIMIITS

Symbol	Parameter		Min.	Max.	Units
t_{WR}	Program Cycle Time	2.5V		10	ms
		4.5V–6.0V		5	

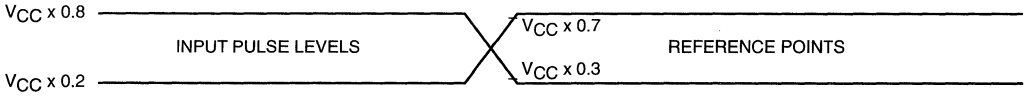
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) This parameter is sampled but not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

INSTRUCTION SET

Instruction		Opcode	Address	Data
Read	64LC10	10101000	A5 A4 A3 A2 A1 A0 0 0	D15 - D0
	64LC20	10101000	A6 A5 A4 A3 A2 A1 A0 0	D15 - D0
	64LC40	10101000	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0
Write	64LC10	10100100	A5 A4 A3 A2 A1 A0 0 0	D15 - D0
	64LC20	10100100	A6 A5 A4 A3 A2 A1 A0 0	D15 - D0
	64LC40	10100100	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0
Write Enable		10100011	X X X X X X X X	
Write Disable		10100000	X X X X X X X X	
[Write All Locations](1)		10100001	X X X X X X X X	D15–D0

4

Figure 1. A.C. Testing Input/Output Waveform (2)(3)(4) (C_L = 100 pF)



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Note:
(1) (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.
(2) Input Rise and Fall Times (10% to 90%) < 10 ns.
(3) Input Pulse Levels = V_{CC} x 0.2 and V_{CC} x 0.8.
(4) Input and Output Timing Reference = V_{CC} x 0.3 and V_{CC} x 0.7.

DEVICE OPERATION

The CAT64LC10/20/40 is a 1K/2K/4K-bit nonvolatile memory intended for use with all standard controllers. The CAT64LC10/20/40 is organized in a 64/128/256 x 16 format. All instructions are based on an 8-bit format. There are four 16-bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC10/20/40 operates on a single power supply ranging from 2.5V to 6.0V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{\text{BUSY}}$ status when polled during a WRITE operation.

The format for all instructions sent to this device includes a 4-bit start sequence, 1010, a 4-bit op code and an 8-bit address field or dummy bits. For a WRITE operation,

Figure 2. Sychronous Data Timing

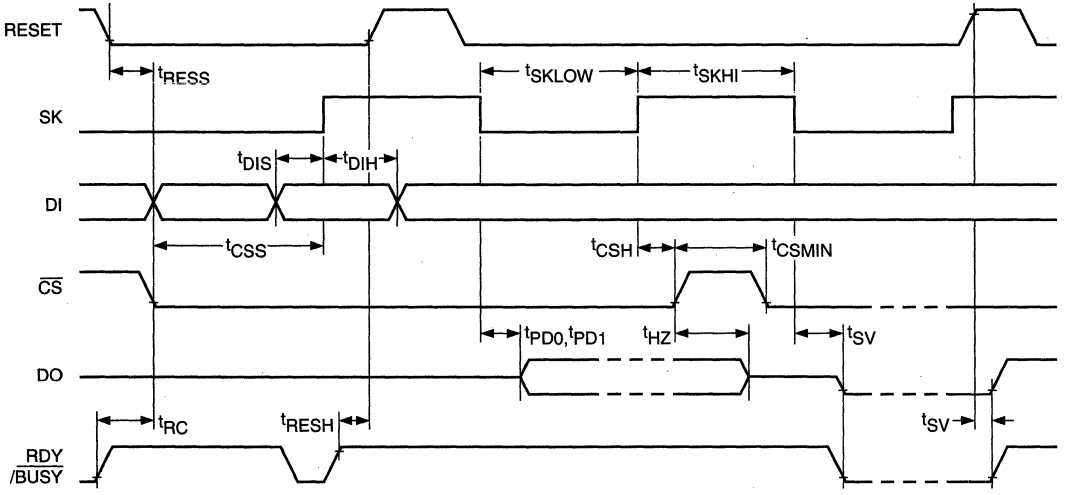

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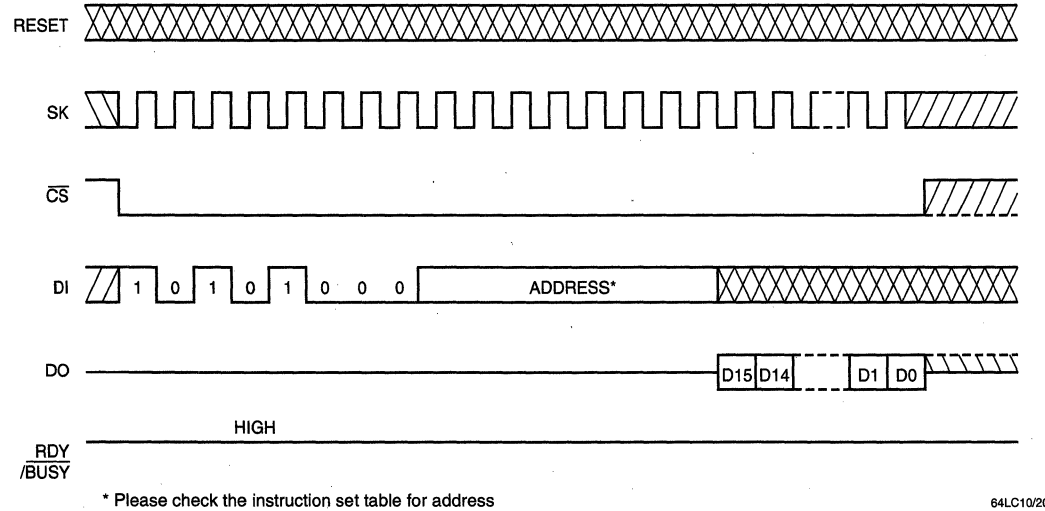
Figure 3. Read Instruction Timing



* Please check the instruction set table for address

64LC10/20/40 F05

a 16-bit data field is also required following the 8-bit address field.

The CAT64LC10/20/40 requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4-bit start sequence. Prior to the 4-bit start sequence (1010), the device will ignore inputs of all other logical sequence.

Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the

Figure 4. Write Instruction Timing

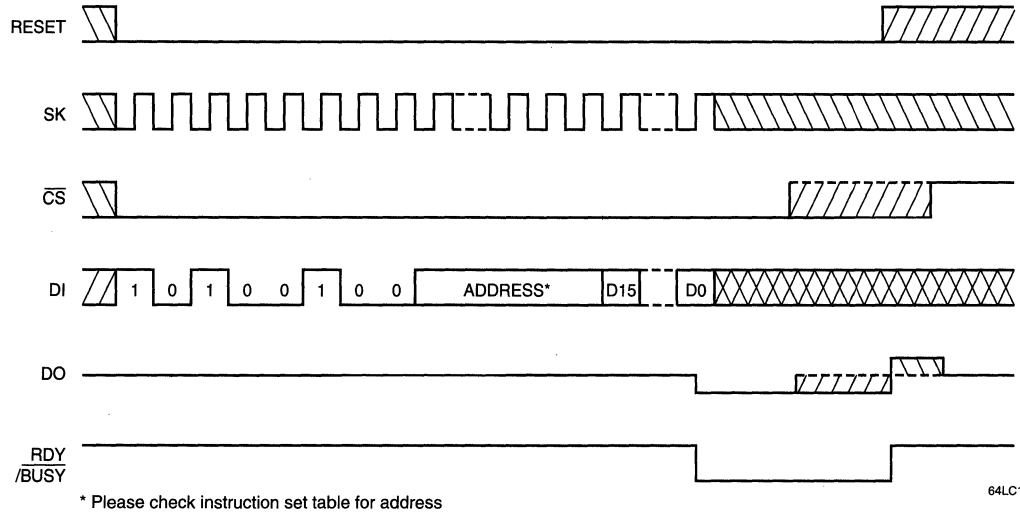
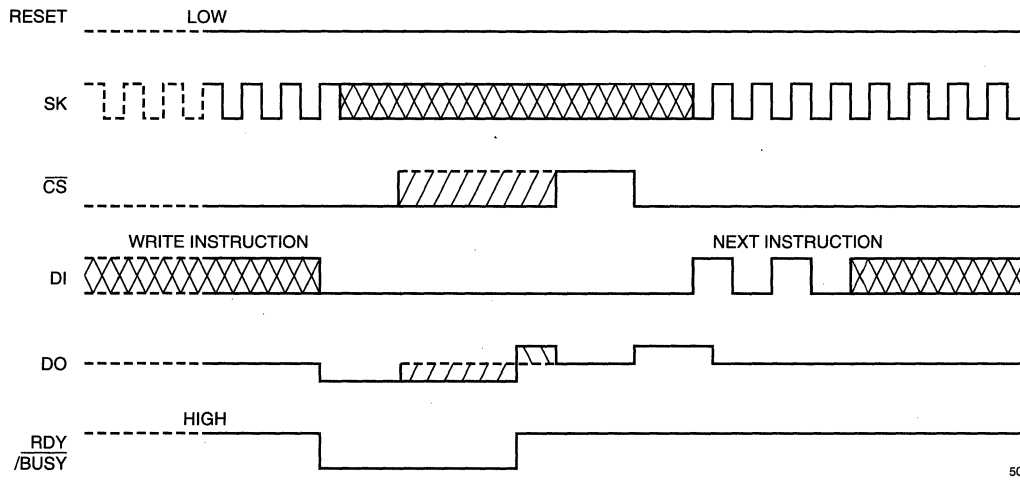


Figure 5. Ready/$\overline{BUSY}$ Status Instruction Timing



WRITE cycle. The RDY/$\overline{\text{BUSY}}$ pin will output the $\overline{\text{BUSY}}$ status (LOW) one t_{SV} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/$\overline{\text{BUSY}}$ output is not affected by the input of $\overline{\text{CS}}$.

An alternative to get RDY/$\overline{\text{BUSY}}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{\text{CS}}$ pin will cause the DO pin to output the RDY/$\overline{\text{BUSY}}$ status. Bringing $\overline{\text{CS}}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is $\overline{\text{BUSY}}$. If the reset occurs before the $\overline{\text{BUSY}}$ period, no writing will be initiated. However, if RESET occurs after the $\overline{\text{BUSY}}$ period, new data will have been written over the old data.

Figure 6. RESET During $\overline{\text{BUSY}}$ Instruction Timing

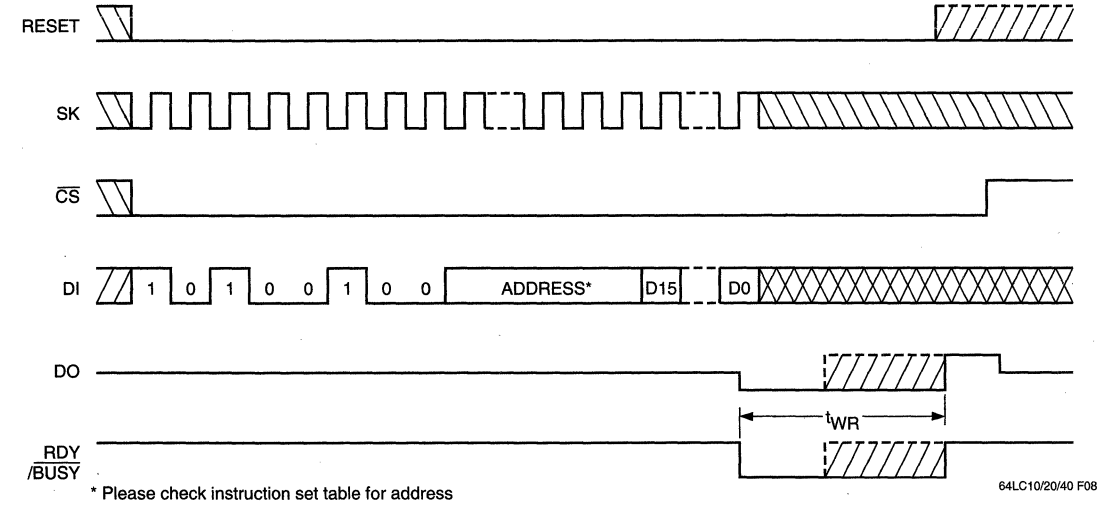
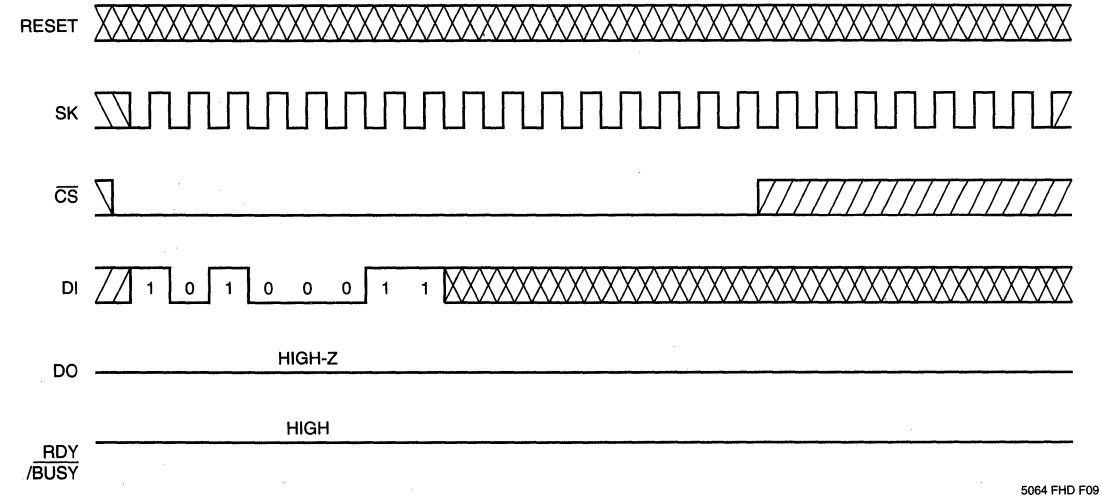


Figure 7. EWEN Instruction Timing



RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

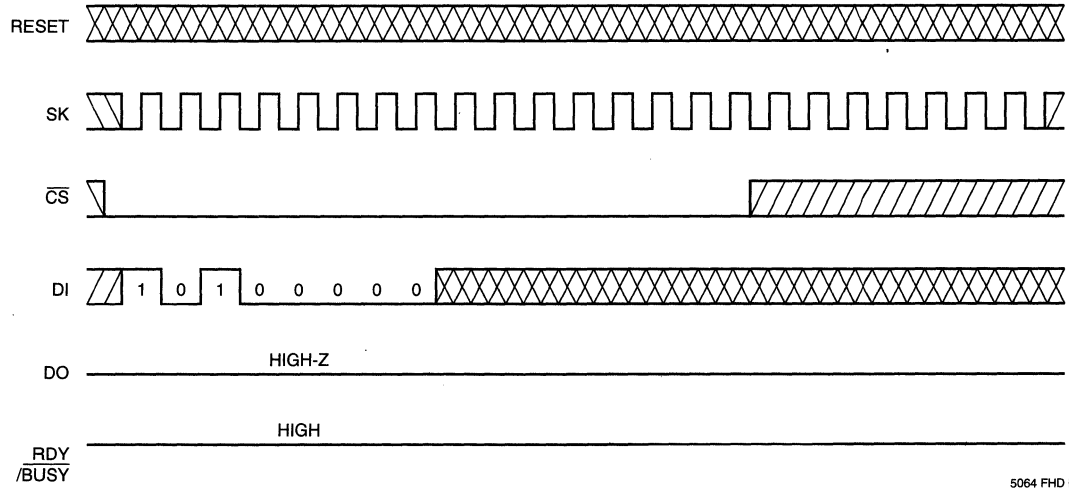
When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{BUSY}$ pin and on the DO pin if $\overline{CS}$ is low.

The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations such as READ, EWEN and EWDS.

ERASE/WRITE ENABLE and DISABLE

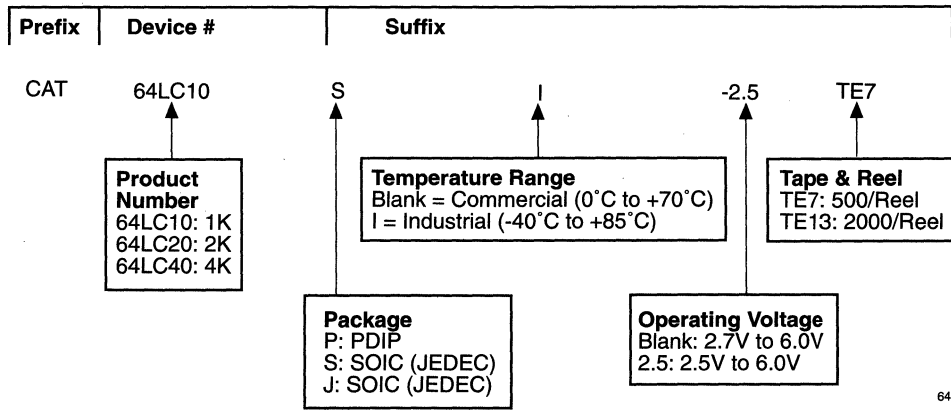
The CAT64LC10/20/40 powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occured. The EWDS is used to prevent any inadvertent over-writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

Figure 8. EWDS Instruction Timing



5064 FHD F10

ORDERING INFORMATION



64LC10/20/40 F11

Notes:
(1) The device used in the above example is a 64LC10SI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

CATALYST SEMICONDUCTOR

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Microwire Bus Serial E²PROMs 3

SPI Bus Serial E²PROMs 4

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Section 5 Secure Access Serial E²PROMs

CAT35C704 ..... 256 x 16, 512 x 8 ..... 4K-Bit 5-1

CAT33C704 ..... 256 x 16, 512 x 8 ..... 4K-Bit 5-15

CAT35C804A ..... 256 x 16, 512 x 8 ..... 4K-Bit 5-29

CAT33C804A ..... 256 x 16, 512 x 8 ..... 4K-Bit 5-43

CAT35C704

4K-Bit Secure Access Serial E²PROM

FEATURES

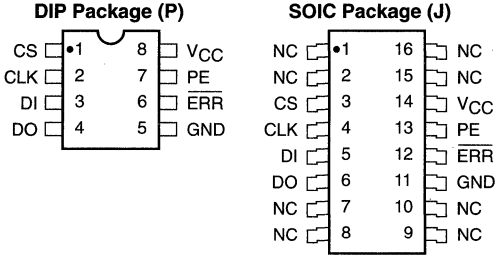
- Single 5V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- High Speed Synchronous Protocol
- Commercial and Industrial Temperature Ranges
- Operating Frequency: DC–3MHz
- Low Power Consumption:
  –Active: 3 mA
  –Standby: 250 µA
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

5

DESCRIPTION

The CAT35C704 is a 4K-bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT35C704 uses a unique serial-byte synchronous communication protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8-pin DIP or 16-pin SOIC packages.

PIN CONFIGURATION



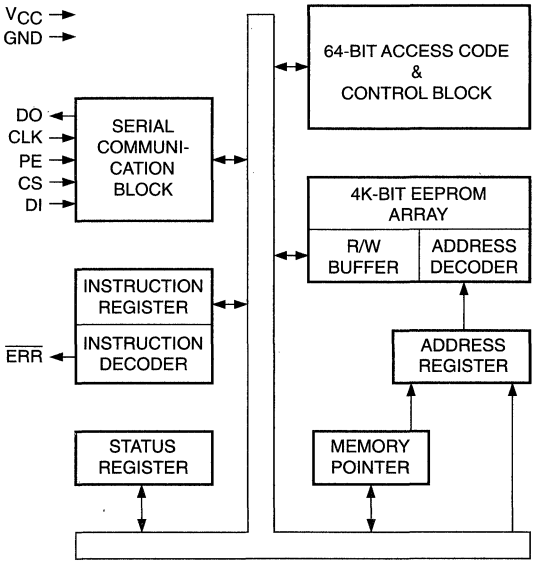
5074 FHD F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+5V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



35C704 F02

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptability	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

5

D.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 5.5V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(5)	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V, CS = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	150			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	50			ns	$V_{IN} = V_{IH}$ or V_{IL}
t_{DIH}	DI Hold Time	0			ns	$V_{OUT} = V_{OH}$ or V_{OL}
t_{PD}	CLK to DO Delay			150	ns	
t_{HZ}(1) (2)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	200			ns	
t_{CKH}	CLK High Pulse Width	165			ns	
t_{CKL}	CLK Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(1)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
t_{CSZ}(1)	CS to DO High-Z Delay			50	ns	
t_{CSD}	CS to DO Busy Delay			150	ns	
f_{CLK}	Clock Frequency	DC		3	MHz	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

The CAT35C704 is a 4K-bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT35C704 is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

5

Figure 1. A.C. Timing

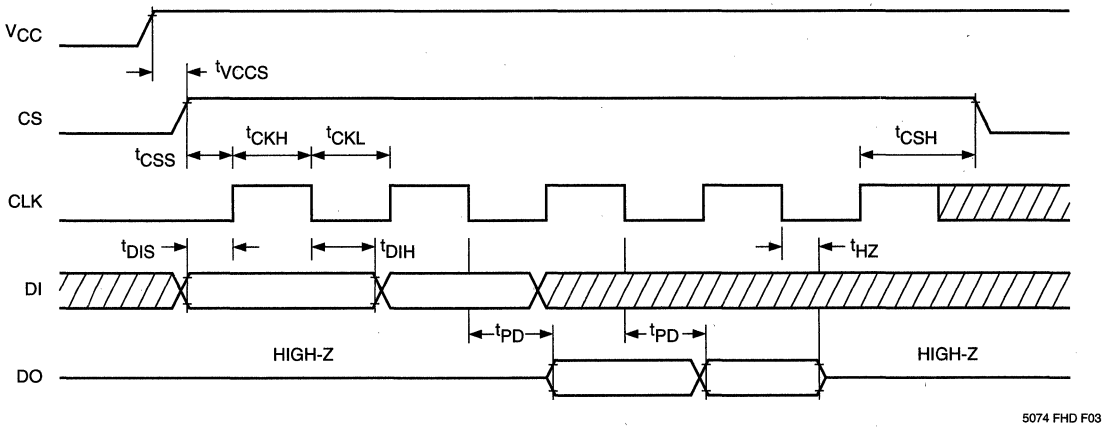
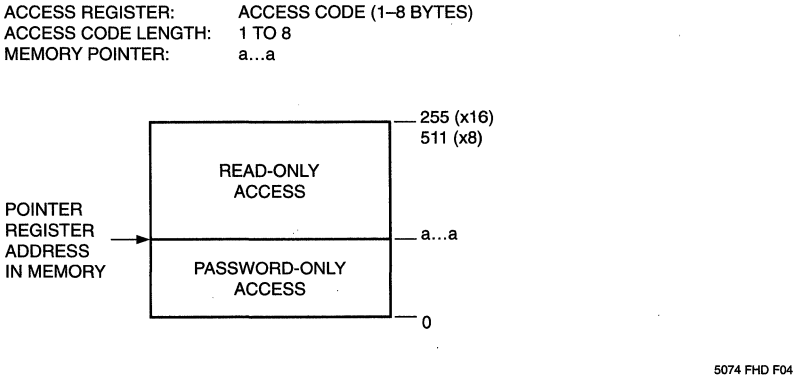


Figure 2. Secure Mode



READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT35C704 communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 3 MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

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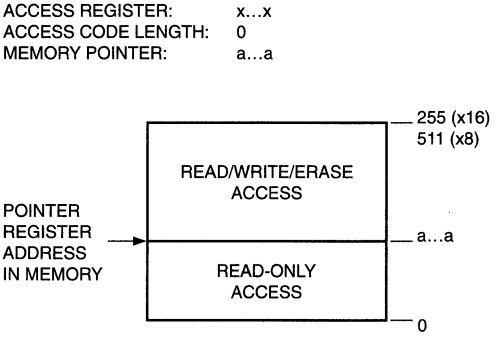
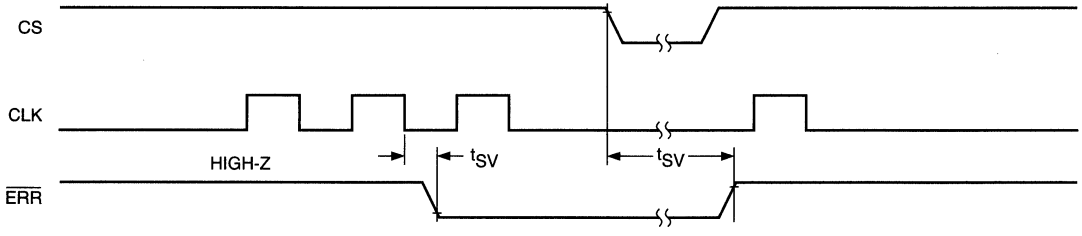
Figure 3. Unprotected Mode(1)



5074 FHD F05

Figure 4. $\overline{ERR}$ Pin Timing



5074 FHD F06

Note:
(1) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 3 MHz.

DI

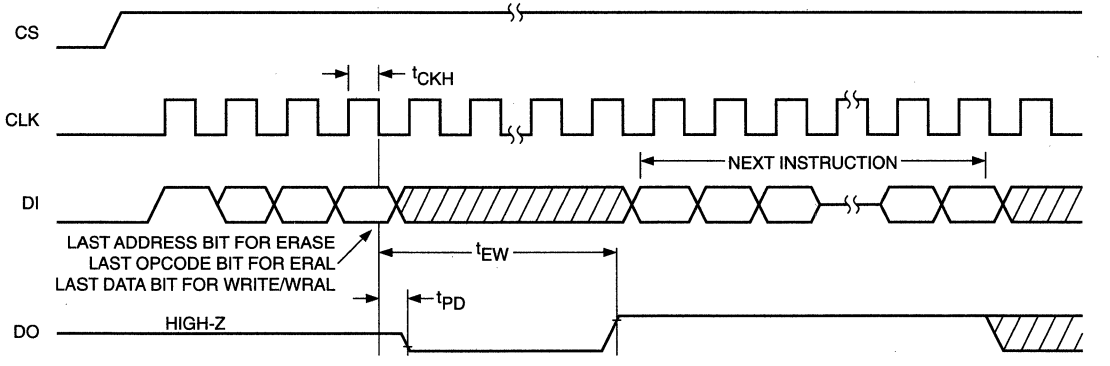
The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. With the SECS protocol, extra bits will be disregarded if they are "0"s and misinterpreted as the next instruction if they are "1"s. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

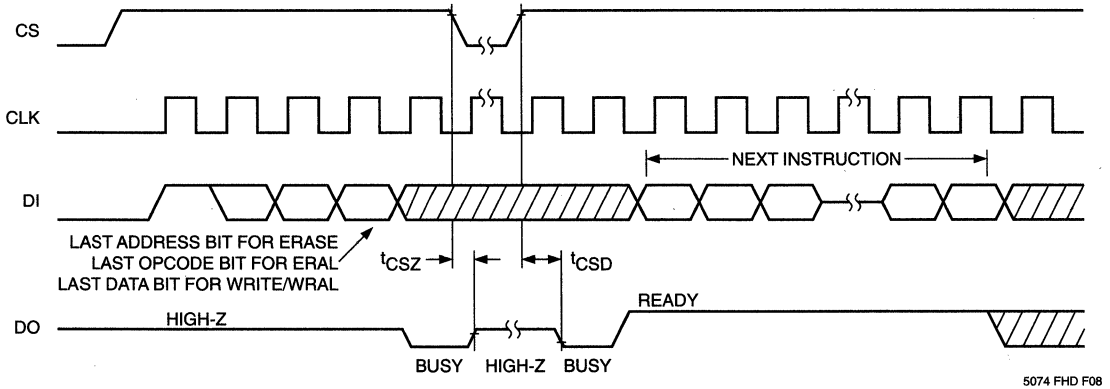
5

Figure 5. Program/Erase Timing



5074 FHD F07

Figure 6. CS to DO Status Timing



5074 FHD F08

also go to the high impedance state if an error condition is detected. If the ENABLE BUSY instruction has not been executed, to determine whether the device is in a program/erase cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a program/erase cycle it will output an 8-bit status word. If it does not, it is in an error condition.

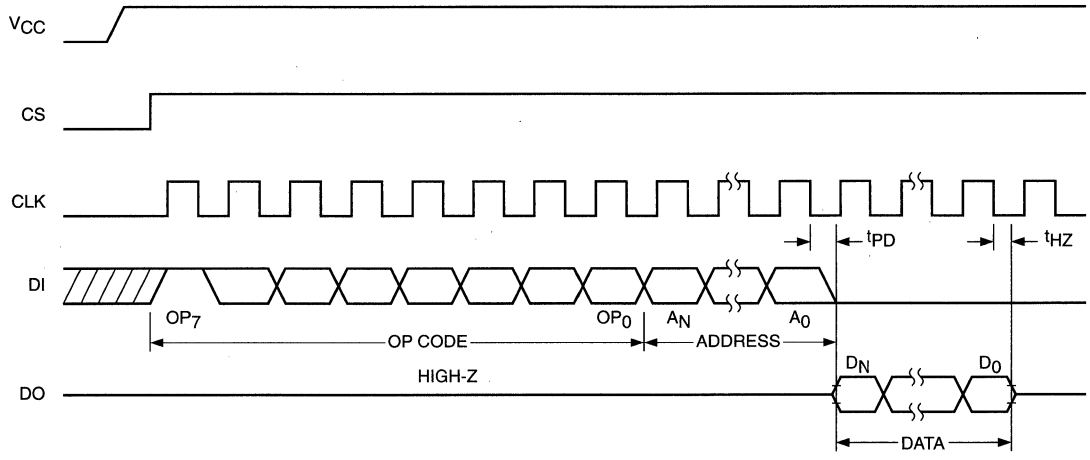
PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

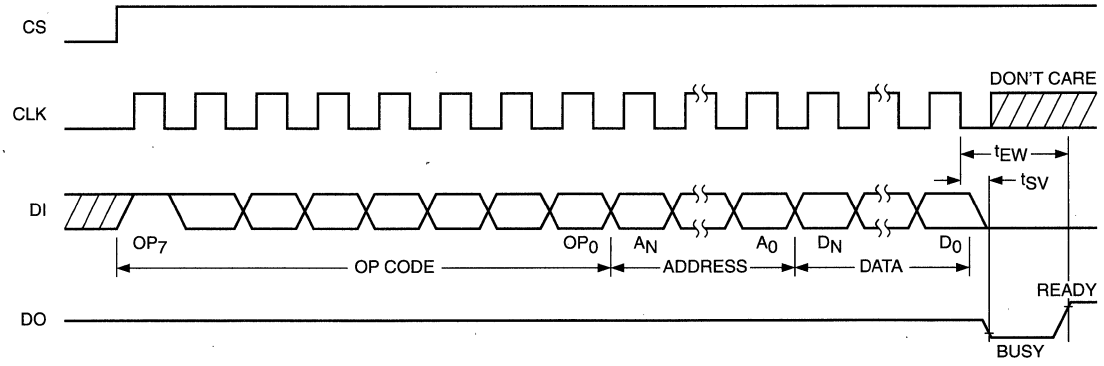
The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 7. Read Timing



5074 FHD F10

Figure 8. Write Timing



5074 FHD F11

DEVICE OPERATION

INSTRUCTIONS

The CAT35C704 instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

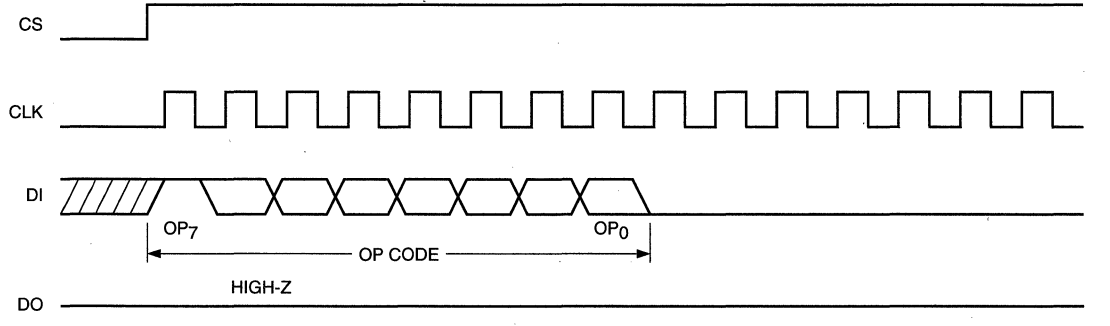
DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operations
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT35C704 is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

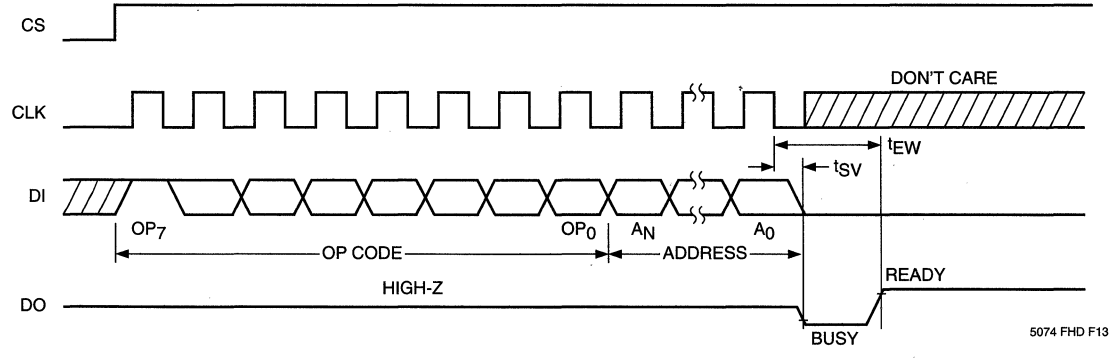
WMPR [address]

Figure 9. EWEN/EWDS Timing



5074 FHD F12

Figure 10. Erase Timing



5074 FHD F13

As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT35C704 will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

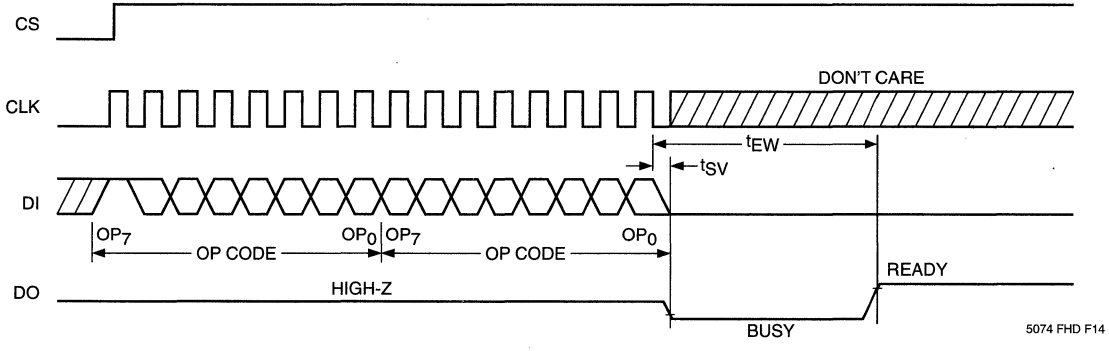
ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

5

Figure 11. ERAL Timing



As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E²PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E²PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

SECS PROTOCOL

The CAT35C704 implements the SECS communication protocol which uses an 8-bit transmission format. As shown in Figures 7–13, all instructions are 8 bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. Each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) pin of the CAT35C704 may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the $\overline{ERR}$ output will be set LOW and the CAT35C704 will stop receiving and sending data until CS is toggled from HIGH to LOW to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, the DO (Data Output) pin will not respond. DO may be programmed to become tri-stated or to output a RDY/$\overline{BUSY}$ status flag during program/erase cycles (see ENBSY instruction).

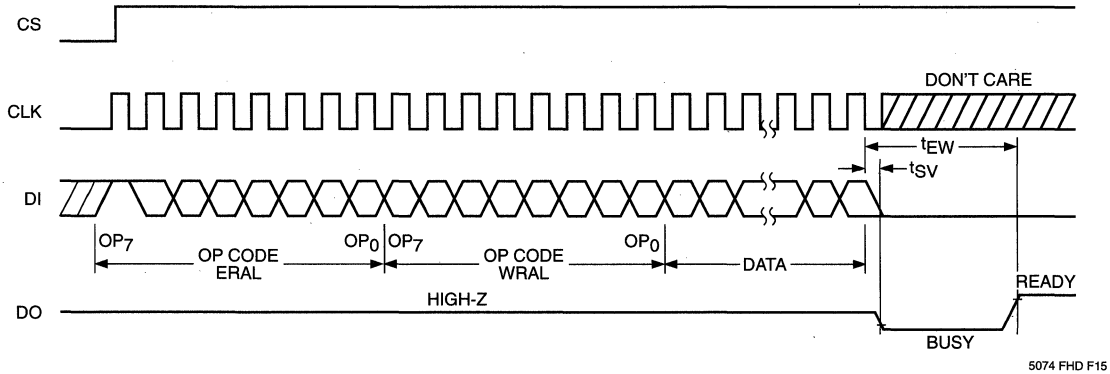
STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C704. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT35C704 will accept

Figure 12. WRAL Timing



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the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C704 expects a parity bit at the end of every incoming instruction packet. For example, the RSEQ instruction will look like this:

1100 1011
A15...A8
A7...A0 P

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit calculated over the entire transmitted data packet. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

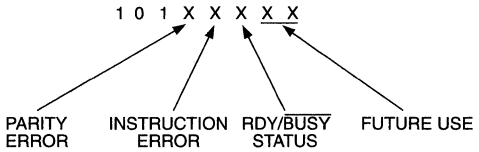

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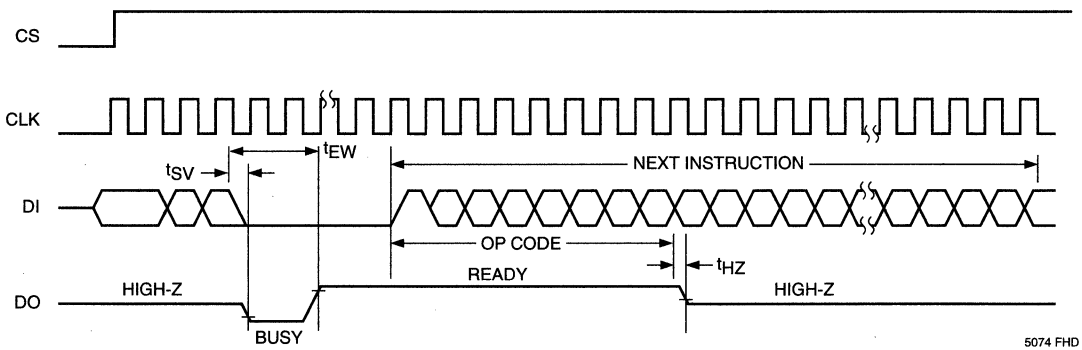
Figure 13. Next Instruction Timing(1)



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Note:
(1) DO will be high impedance after the last instruction bit has been clocked in, unless the instruction is RSR or RMPR, in which case, DO will become active.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT35C704 will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the

WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8-bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

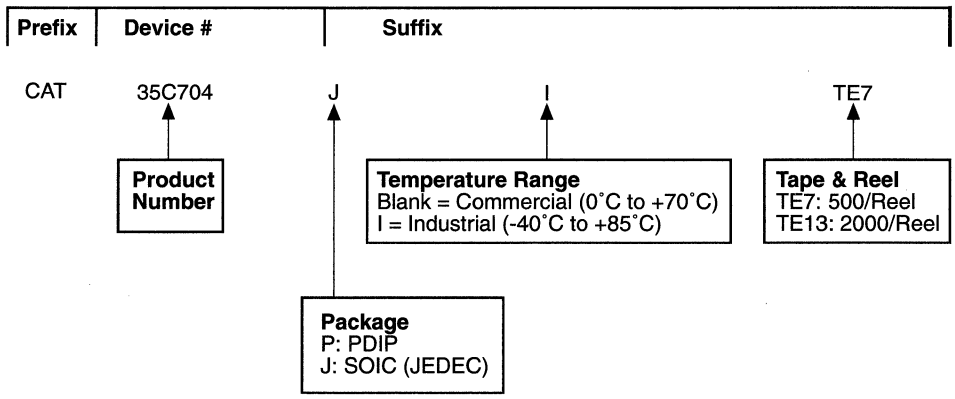
NOP No Operation

1000	0000

No Operation.

5

ORDERING INFORMATION



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Notes:
(1) The device used in the above example is a 35C704JI-TE7 (SOIC, Industrial Temperature, Tape & Reel)

CAT33C704

4K-Bit Secure Access Serial E²PROM

FEATURES

- Single 3V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- High Speed Synchronous Protocol
- Operating Frequency: DC–1MHz
- Low Power Consumption:
  Active: 3 mA
  Standby: 250 µA
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial and Industrial Temperature Ranges

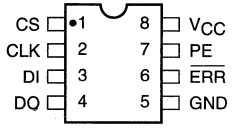
5

DESCRIPTION

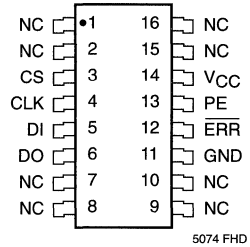
The CAT33C704 is a 4K-bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT33C704 uses a unique serial-byte synchronous communication protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8-pin DIP or 16-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



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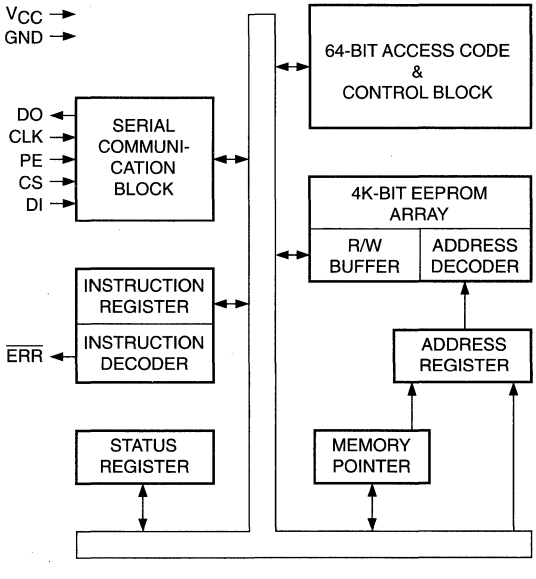
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+3V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



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TD 5072

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 3.3V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 3.3V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(5)	Input Leakage Current			2	µA	V_{IN} = 3.3V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 3.3V, CS = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	150			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	50			ns	V_{IN} = V_{IH} or V_{IL}
t_{DIH}	DI Hold Time	0			ns	V_{OUT} = V_{OH} or V_{OL}
t_{PD}	CLK to DO Delay			150	ns	
t_{HZ}(1) (2)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	300			ns	
t_{CKH}	CLK High Pulse Width	300			ns	
t_{CKL}	CLK Low Pulse Width	140			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(1)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
t_{CSZ}(1)	CS to DO High-Z Delay			50	ns	
t_{CSD}	CS to DO Busy Delay			150	ns	
f_{CLK}	Frequency	DC		1	MHz	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

The CAT33C704 is a 4K-bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT33C704 is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

5

Figure 1. A.C. Timing

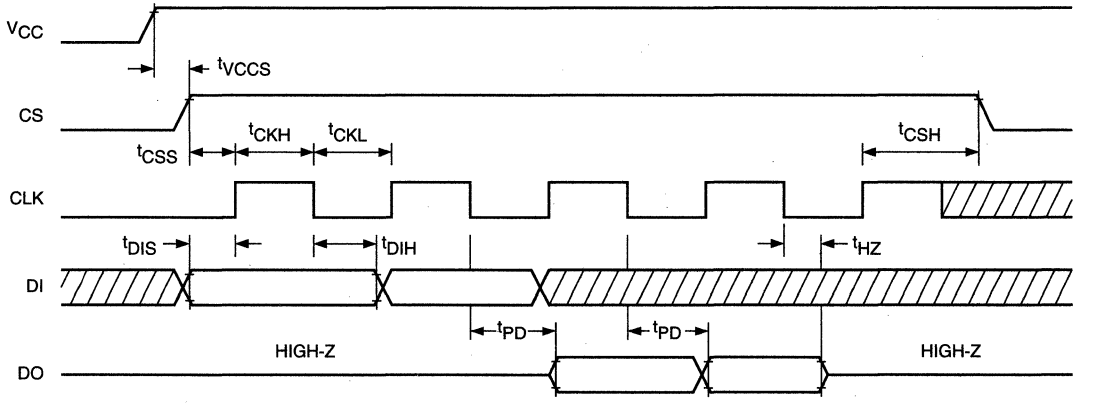
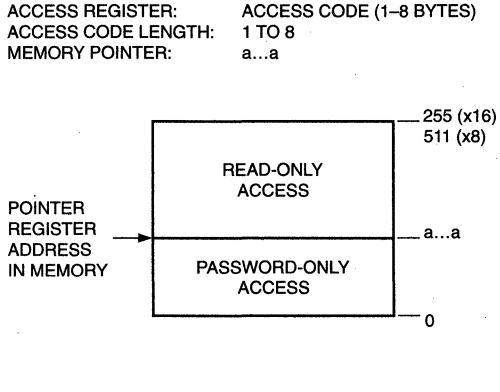


Figure 2. Secure Mode



READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT33C704 communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 1 MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

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Figure 3. Unprotected Mode(1)

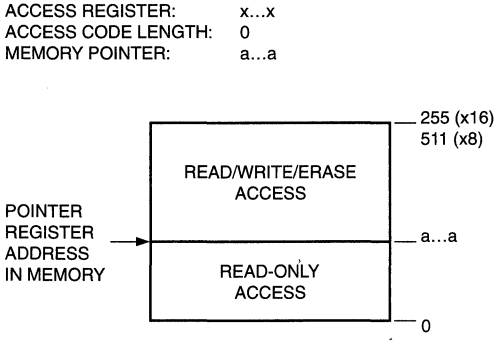

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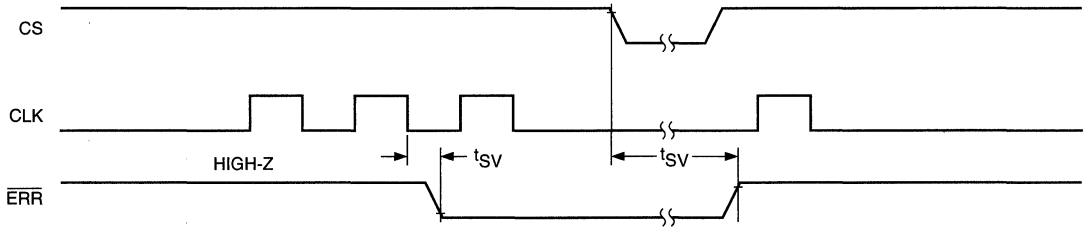
Figure 4. $\overline{ERR}$ Pin Timing



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Note:
(1) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 1 MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. With the SECS protocol, extra bits will be disregarded if they are "0"s and misinterpreted as the next instruction if they are "1"s. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

5

Figure 5. Program/Erase Timing

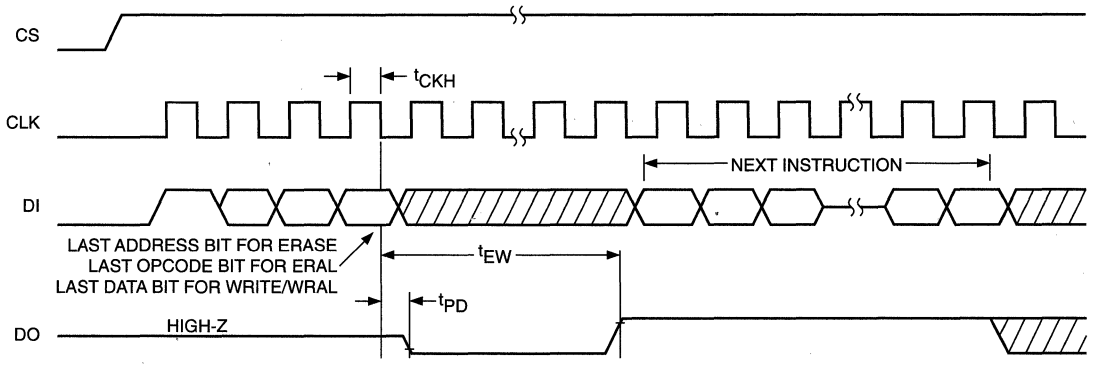
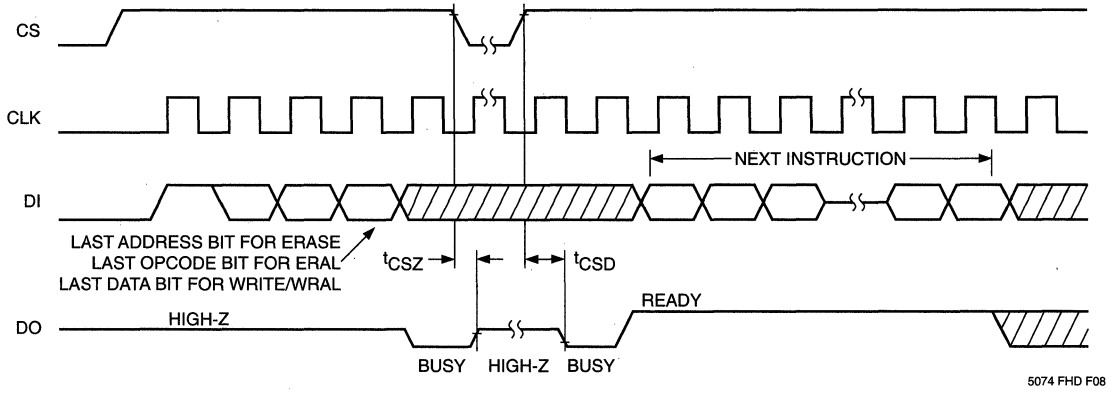


Figure 6. CS to DO Status Timing



also go to the high impedance state if an error condition is detected. If the ENABLE BUSY instruction has not been executed, to determine whether the device is in a program/erase cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a program/erase cycle it will output an 8-bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 7. Read Timing

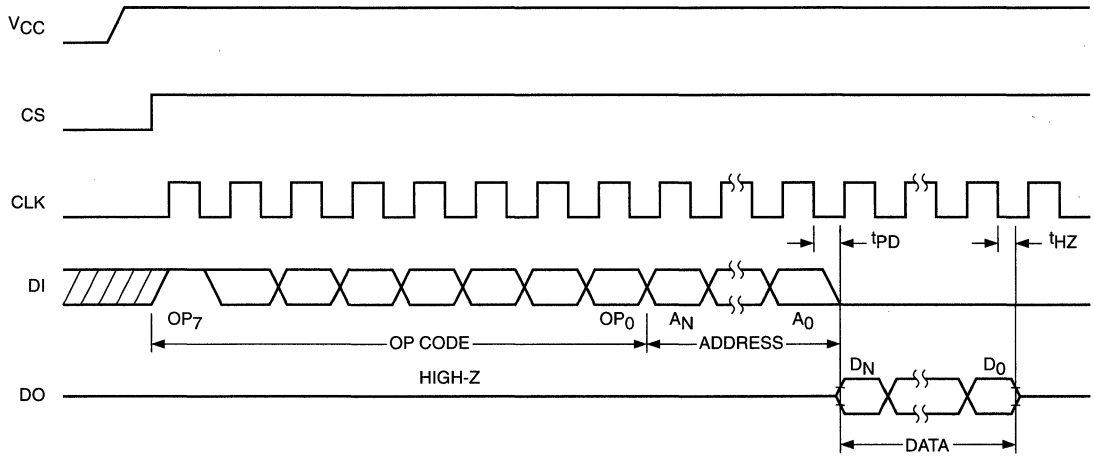


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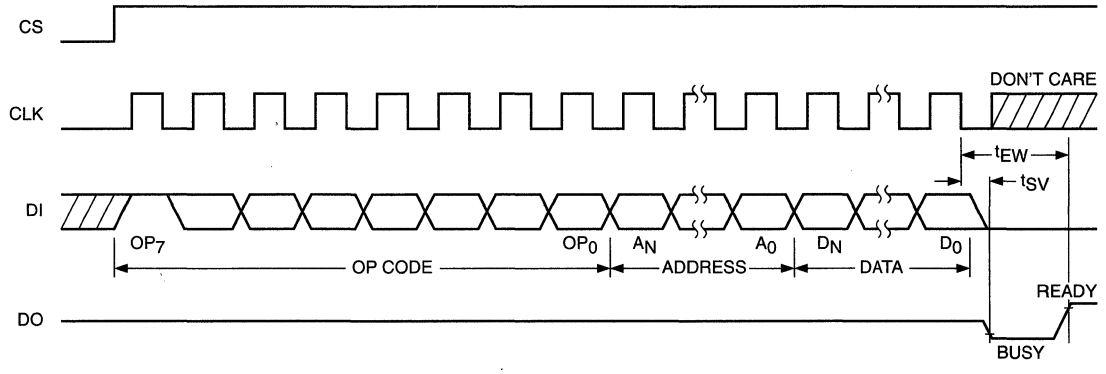
Figure 8. Write Timing



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DEVICE OPERATION

INSTRUCTIONS

The CAT33C704 instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operations
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT33C704 is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

WMPR [address]

Figure 9. EWEN/EWDS Timing

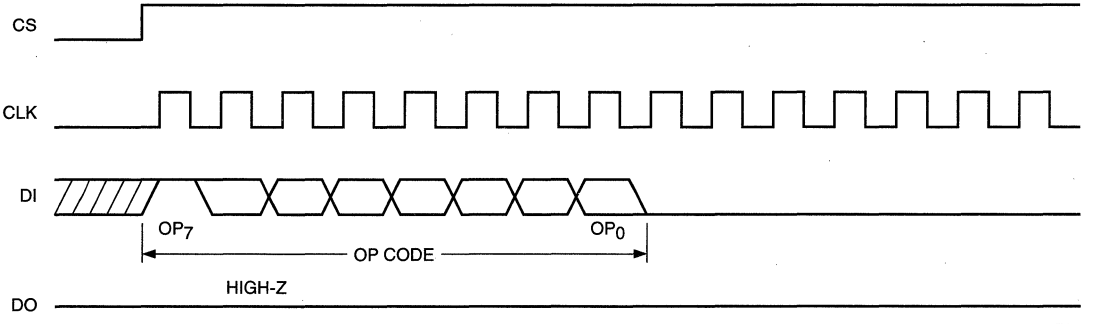
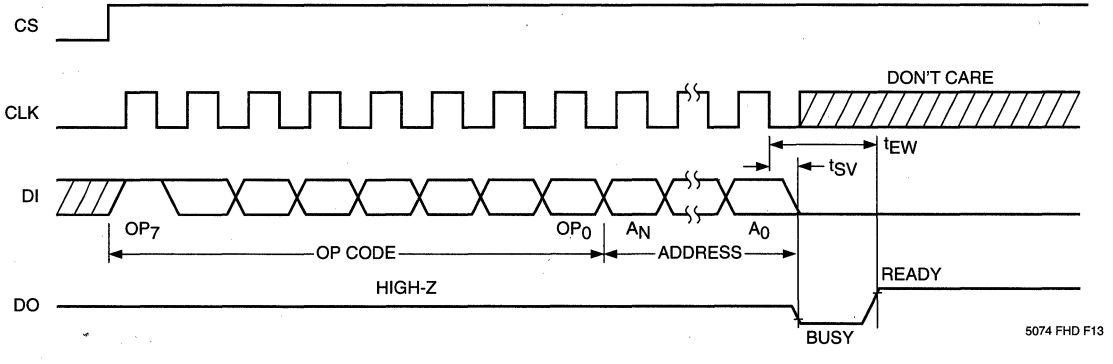


Figure 10. Erase Timing



As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT33C704 will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

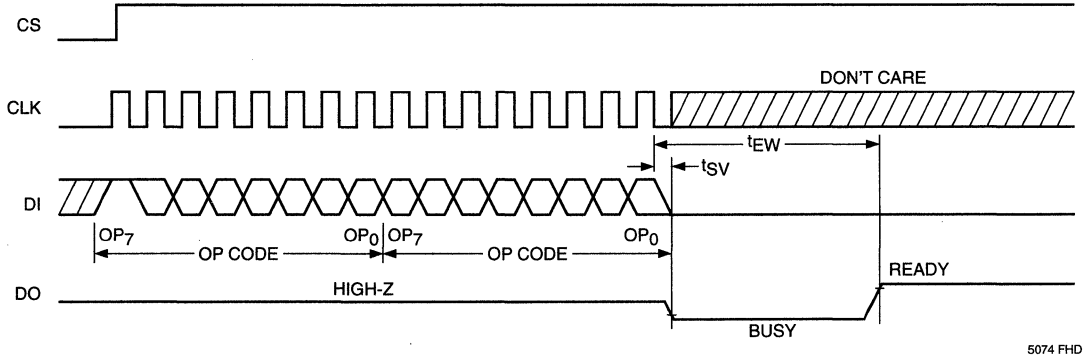
ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

5

Figure 11. ERAL Timing



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As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E²PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E²PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

SECS PROTOCOL

The CAT33C704 implements the SECS communication protocol which uses an 8-bit transmission format. As shown in Figures 7–13, all instructions are 8 bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. Each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) pin of the CAT33C704 may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the $\overline{ERR}$ output will be set LOW and the CAT33C704 will stop receiving and sending data until CS is toggled from HIGH to LOW to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, the DO (Data Output) pin will not respond. DO may be programmed to become tri-stated or to output a RDY/$\overline{BUSY}$ status flag during program/erase cycles (see ENBSY instruction).

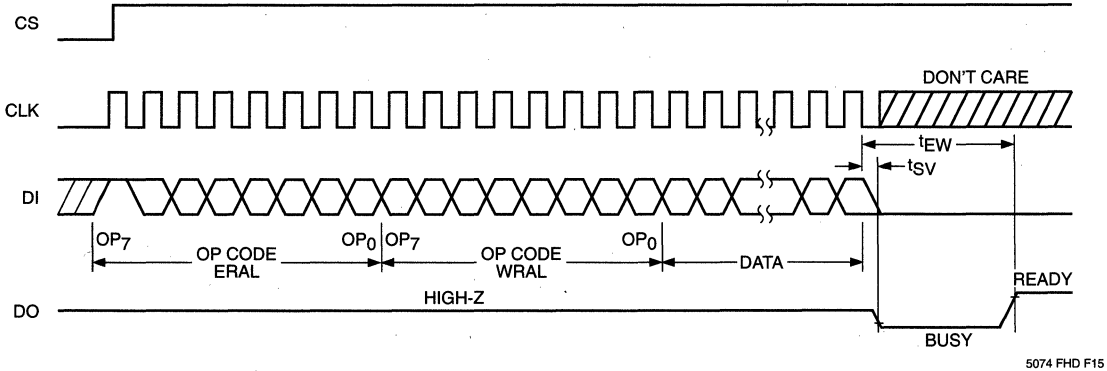
STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT33C704. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT33C704 will accept

Figure 12. WRAL Timing



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the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT33C704 expects a parity bit at the end of every incoming instruction packet. For example, the RSEQ instruction will look like this:

1100 1011
A15...A8
A7...A0 P

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit calculated over the entire transmitted data packet. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

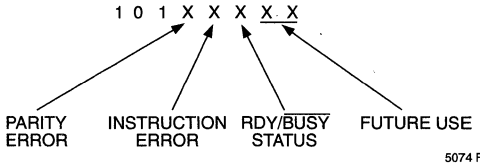

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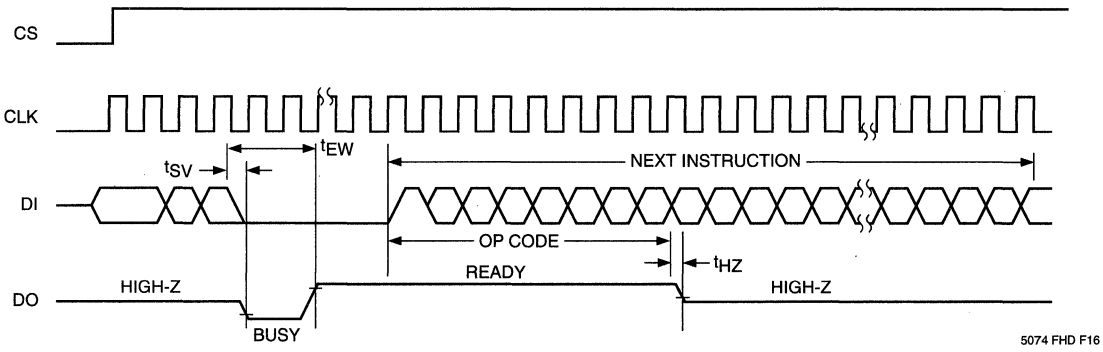
Figure 13. Next Instruction Timing(1)



Note:
(1) DO will be high impedance after the last instruction bit has been clocked in, unless the instruction is RSR or RMPR, in which case, DO will become active.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT33C704 will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the

WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8-bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

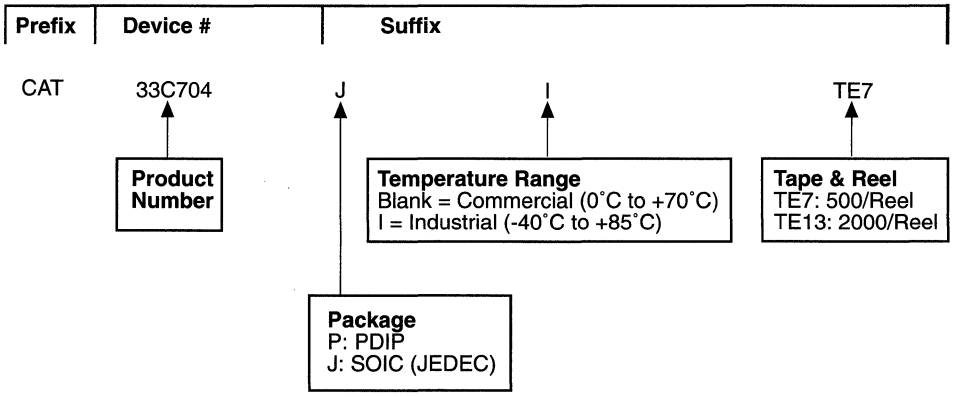
NOP No Operation

1000	0000

No Operation.

5

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 33C704JI-TE7 (SOIC, Industrial Temperature, Tape & Reel)

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CAT35C804A

4K-Bit Secure Access Serial E²PROM

FEATURES

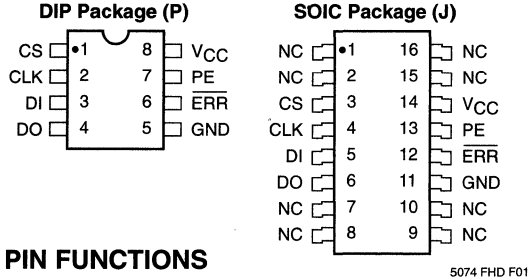
- Single 5V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- UART Compatible Asynchronous Protocol
- 100,000 Program/Erase Cycles
- Commercial and Industrial Temperature Ranges
- I/O Speed: 9600 Baud
  –Clock Frequency: 4.9152 MHz Xtal
- Low Power Consumption:
  –Active: 3 mA
  –Standby: 250 µA
- 100 Year Data Retention

5

DESCRIPTION

The CAT35C804A is a 4K-bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT35C804A uses a UART compatible asynchronous protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8-pin DIP or 16-pin SOIC packages.

PIN CONFIGURATION

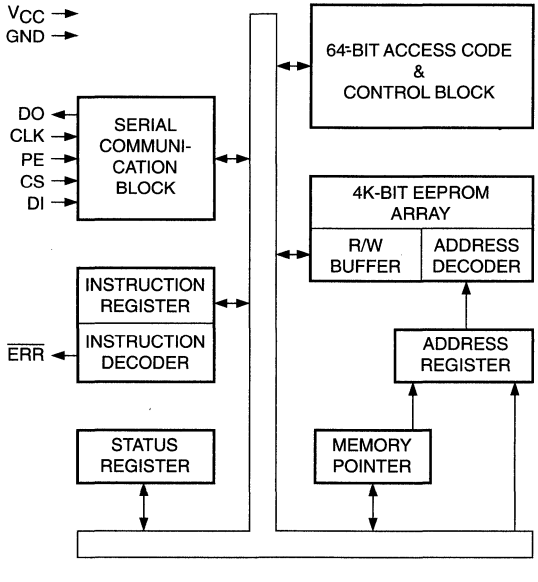


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
V_{CC}	+5V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

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D.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 5.5V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(5)	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V, CS = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_D	CLK to DO Delay		104		µs	$V_{IN} = V_{IH}$ or V_{IL}
t_{PD}	CLK to DO Delay			150	ns	$V_{OUT} = V_{OH}$ or V_{OL}
t_{HZ}(1) (2)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(1)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
f_{CLK}	Clock Frequency	DC		4.9152	MHz	

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

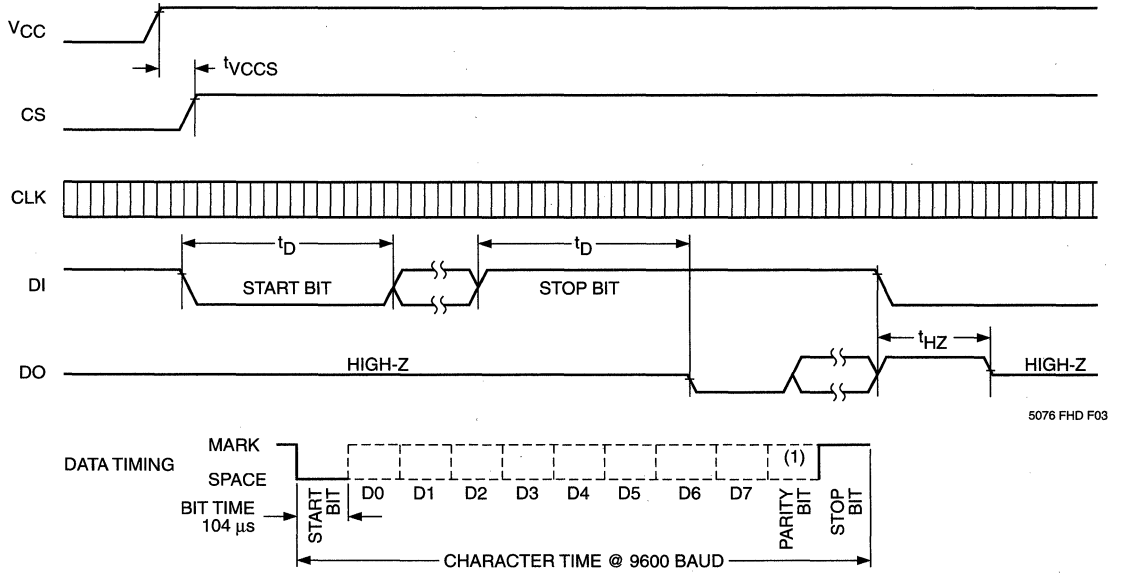
The CAT35C804A is a 4K-bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT35C804A is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

5

Figure 1. A.C. Timing



Note:
(1) If PE pin = 1.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT35C804A communicates with external devices via an asynchronous serial communication protocol. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

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Figure 2. Secure Mode

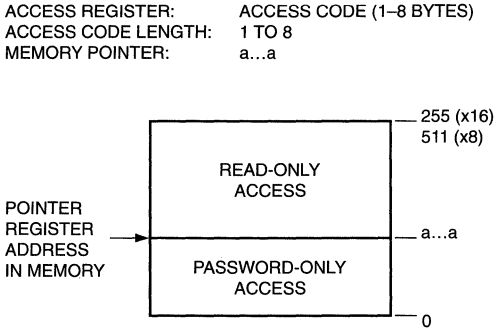

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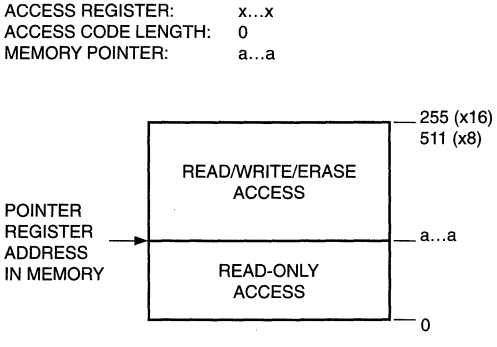
Figure 3. Unprotected Mode(1)



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Note:
(1) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device at a specified frequency. The CAT35C804A is designed with an internal divider to produce a 9600 baud output for an input clock frequency of 4.9152 MHz.

DI

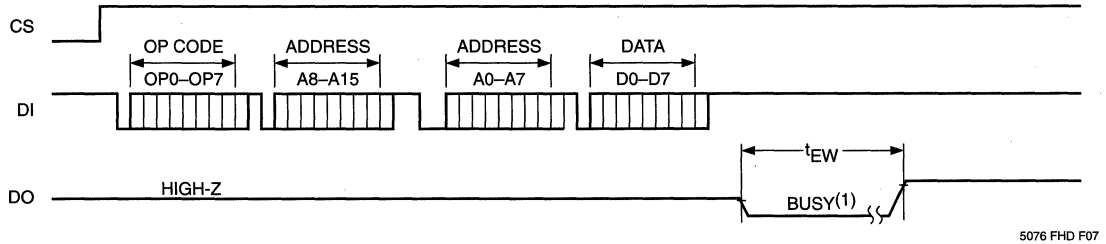
The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each byte must begin with "0" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. Extra bits will be disregarded if they are "1"s and extra "0"s will be misinterpreted as the start bit of the next instruction. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

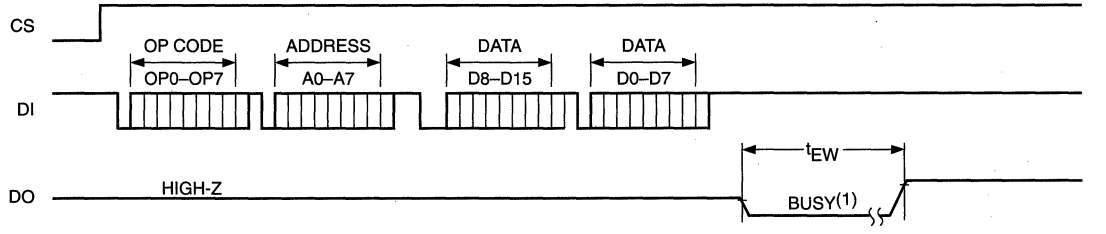
5

Figure 4. Program/Erase Timing (x8 Format)



5076 FHD F07

Figure 5. Program/Erase Timing (x16 Format)



5076 FHD F08

Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

also go to the high impedance state if an error condition is detected. In the event an ENABLE BUSY instruction has not been sent, a READ STATUS register instruction can be executed. This also tells the user whether the part is in a program/erase cycle or an error condtion. When the device is in a program/erase cycle it will output an 8-bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{\text{ERR}}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{\text{ERR}}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 6. Read Timing (x8 Format)

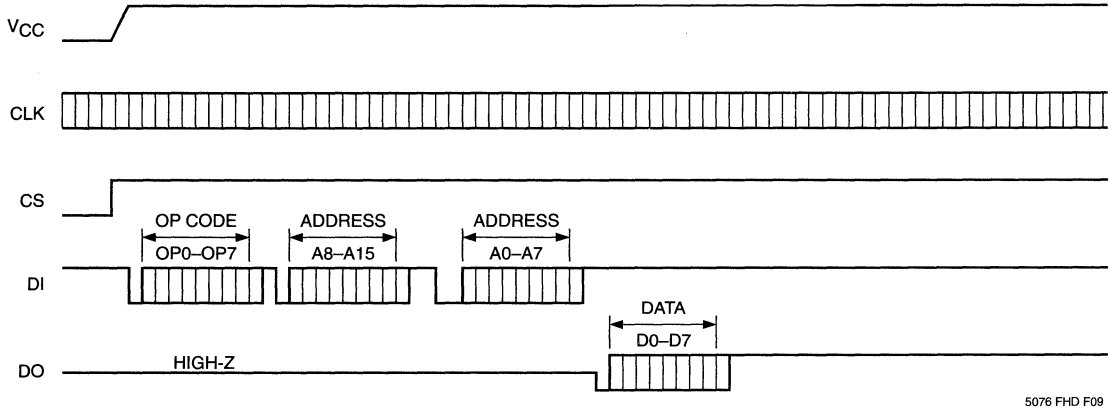
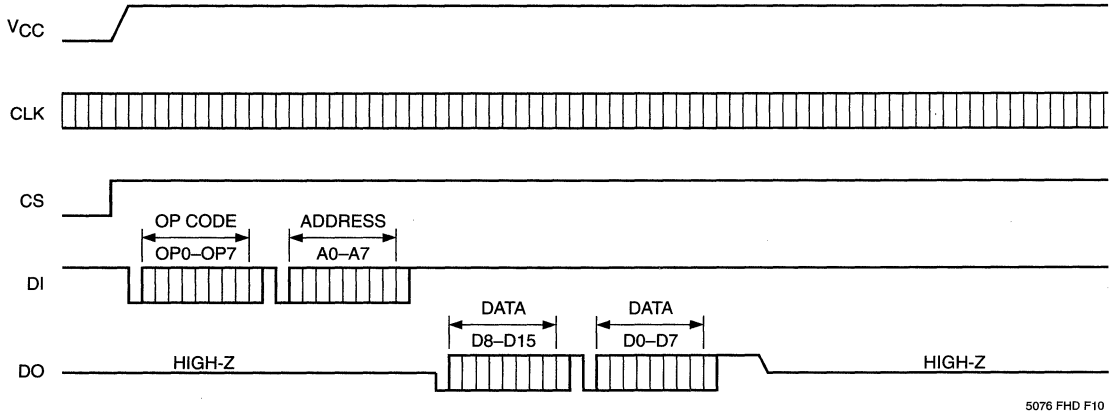


Figure 7. Read Timing (x16 Format)



DEVICE OPERATION

INSTRUCTIONS

The CAT35C804A instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

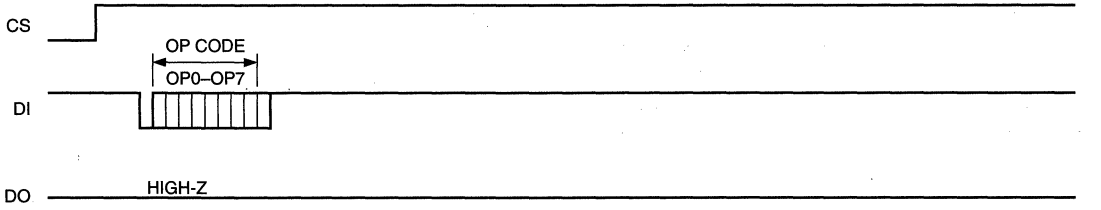
DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operation
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT35C804A is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

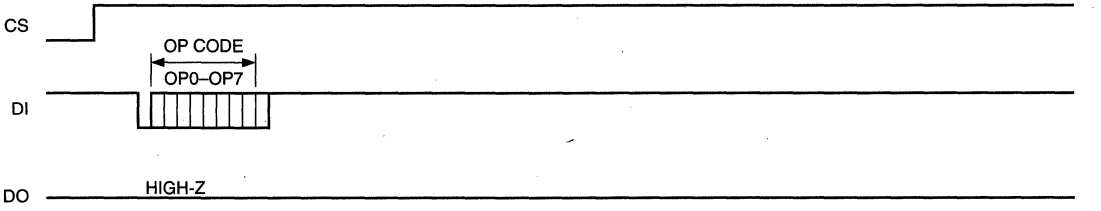
WMPR [address]

Figure 8. EWEN/EWDS Timing (x8 Format)



5076 FHD F11

Figure 9. EWEN/EWDS Timing (x16 Format)



5076 FHD F11

As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

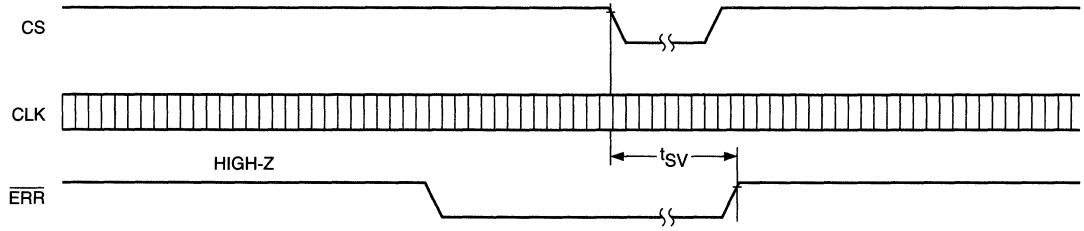
A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT35C804A will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

Figure 10. $\overline{ERR}$ Pin Timing



5076 FHD F06

As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> $1.84x10^{19}$ combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C804A. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and

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Figure 11. Erase Timing (x8 Format)

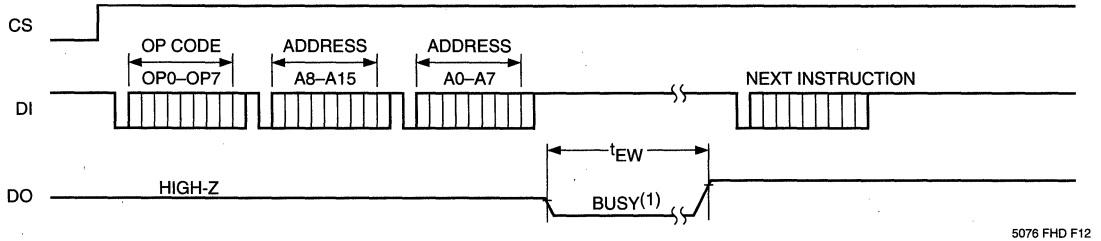
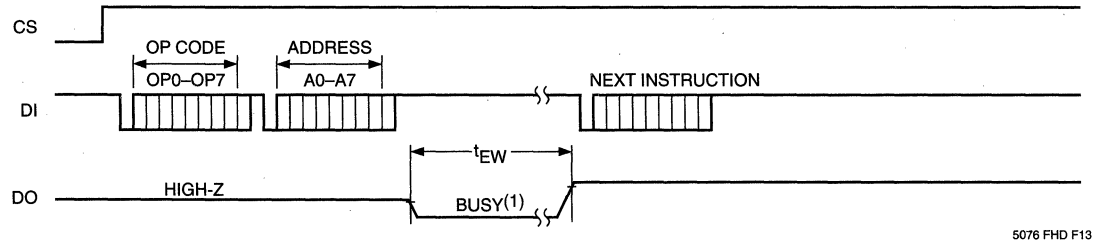


Figure 12. Erase Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in High-Z condition.

then the WRAL instruction. The CAT35C804A will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the stop bit. When PE is HIGH, the CAT35C804A expects a parity bit at the end of every byte. For example, the RSEQ instruction will look like this:

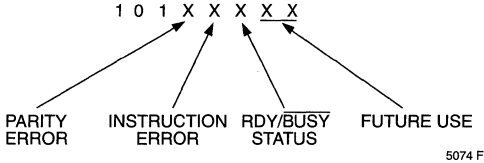
0 1100 1011 11
0 A15...A8 P1
0 A7...A0 P1

The device then outputs data continuously until it reaches the end of the memory. Each byte of data contains 9 bits with the ninth bit being the parity bit. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

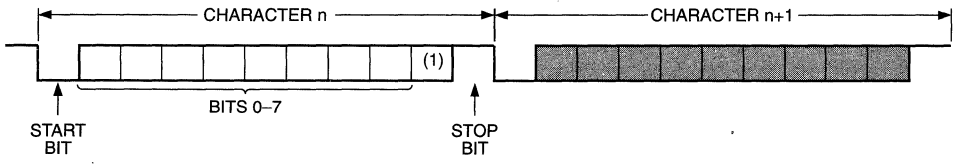
Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8-bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".



5074 FHD F09

Figure 13. Asynchronous Communication Protocol



5076 FHD F14

Note:
(1) Parity bit if enabled; skipped if parity disabled.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*

1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT35C804A will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

Figure 14. ERAL Timing (x8 Format)

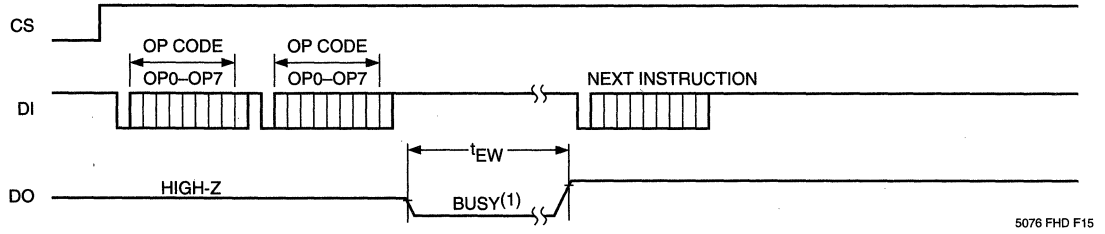
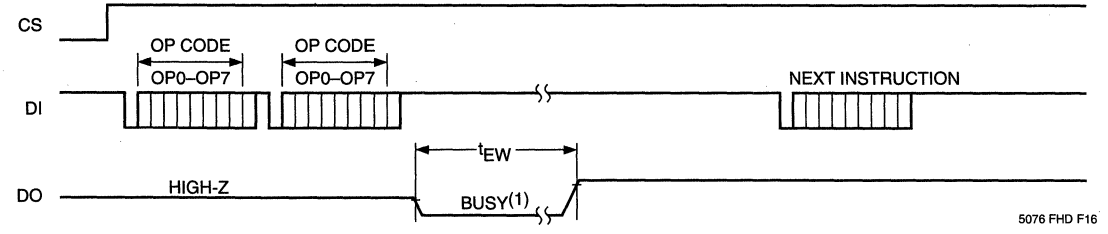


Figure 15. ERAL Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8-bit or 16-bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

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Figure 16. WRAL Timing (x8 Format)

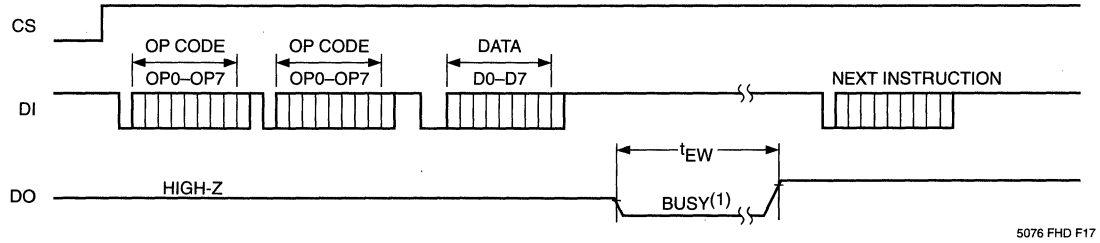
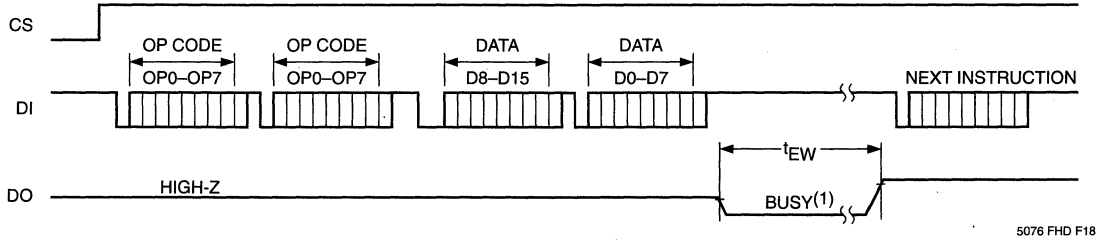


Figure 17. WRAL Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

5

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

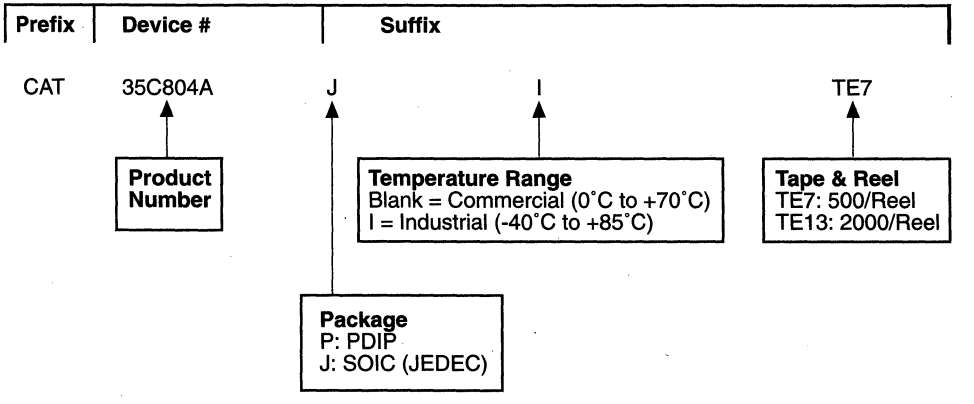
Output the contents of the 8-bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 35C804AJI-TE7 (SOIC, Industrial Temperature, Tape & Reel)

33C804 F19

CAT33C804A

4K-Bit Secure Access Serial E²PROM

FEATURES

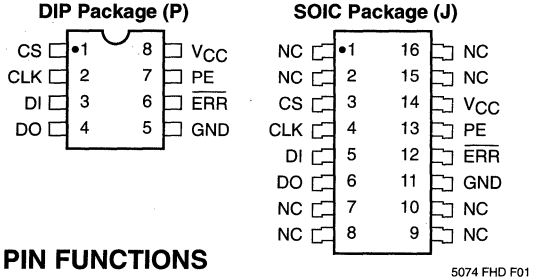
- Single 3V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x 16 or 512 x 8 Selectable Serial Memory
- UART Compatible Asynchronous Protocol
- Commercial and Industrial Temperature Ranges
- 100,000 Program/Erase Cycles
- I/O Speed: 9600 Baud
  –Clock Frequency: 4.9152 MHz Xtal
- Low Power Consumption:
  –Active: 3 mA
  –Standby: 250 µA
- 100 Year Data Retention

5

DESCRIPTION

The CAT33C804A is a 4K-bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT33C804A uses a UART compatible asynchronous protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8-pin DIP or 16-pin SOIC packages.

PIN CONFIGURATION



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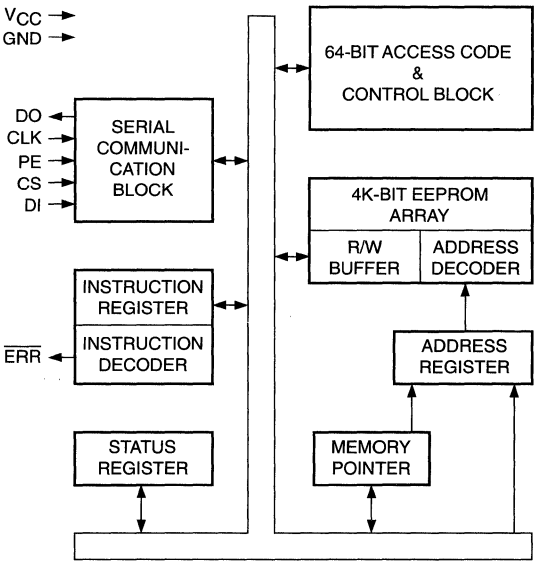
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+3V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



33C804 F02

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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

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D.C. CHARACTERISTICS

V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 3.3V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 3.3V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(5)	Input Leakage Current			2	µA	V_{IN} = 3.3V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 3.3V, CS = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_D	CLK to DO Delay		104		µs	V_{IN} = V_{IH} or V_{IL}
t_{PD}	CLK to DO Delay			150	ns	V_{OUT} = V_{OH} or V_{OL}
t_{HZ}(1) (2)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(1)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
f_{CLK}	Clock Frequency	DC		4.9152	MHz	

5

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

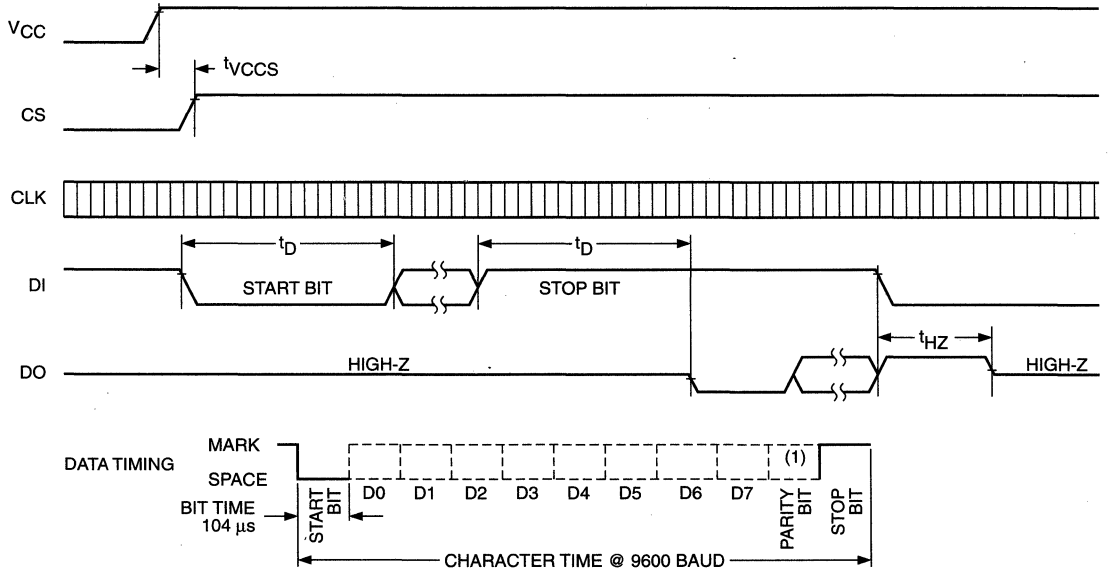
The CAT33C804A is a 4K-bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT33C804A is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

5

Figure 1. A.C. Timing



33C804 F03

Note:
(1) If PE pin = 1.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT33C804A communicates with external devices via an asynchronous serial communication protocol. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

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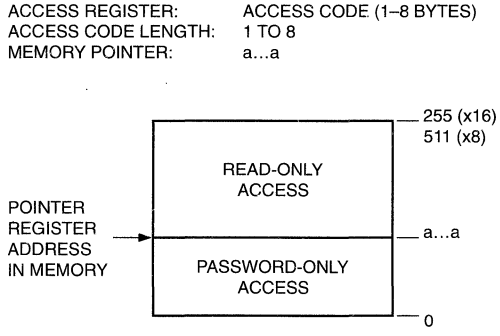
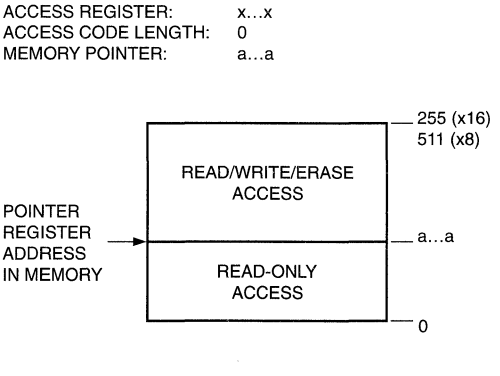
Figure 2. Secure Mode



5074 FHD F04

Figure 3. Unprotected Mode(1)



5074 FHD F05

Note:
(1) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device at a specified frequency. The CAT33C804A is designed with an internal divider to produce a 9600 baud output for an input clock frequency of 4.9152 MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each byte must begin with "0" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. Extra bits will be disregarded if they are "1"s and extra "0"s will be misinterpreted as the start bit of the next instruction. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

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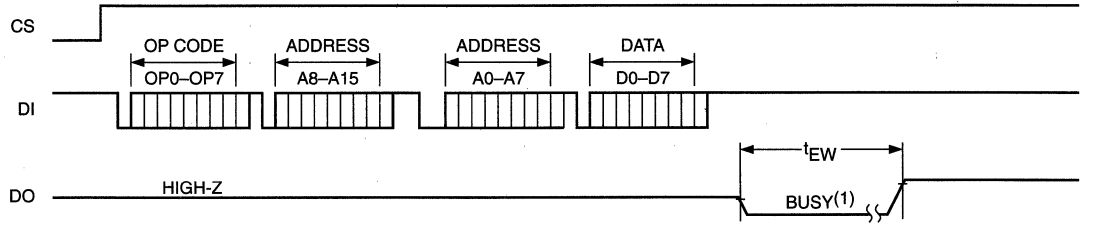
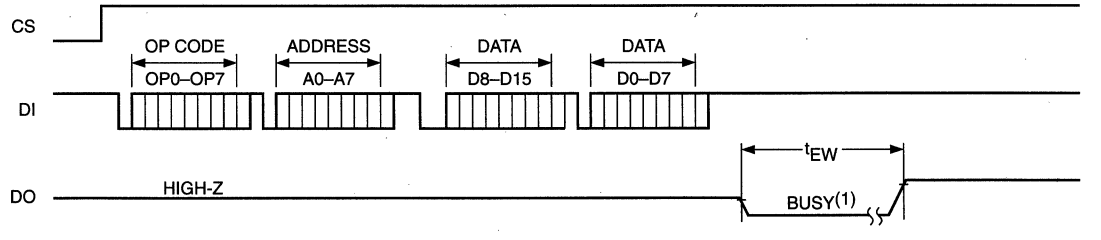
Figure 4. Program/Erase Timing (x8 Format)



5076 FHD F07

Figure 5. Program/Erase Timing (x16 Format)



5076 FHD F08

Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

also go to the high impedance state if an error condition is detected. In the event an ENABLE BUSY instruction has not been sent, a READ STATUS register instruction can be executed. This also tells the user whether the part is in a program/erase cycle or an error condtion. When the device is in a program/erase cycle it will output an 8 bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 6. Read Timing (x8 Format)

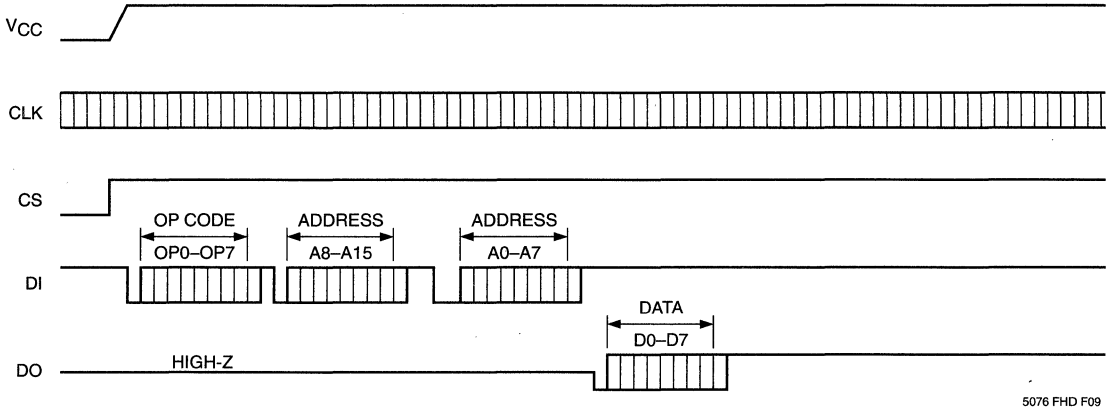
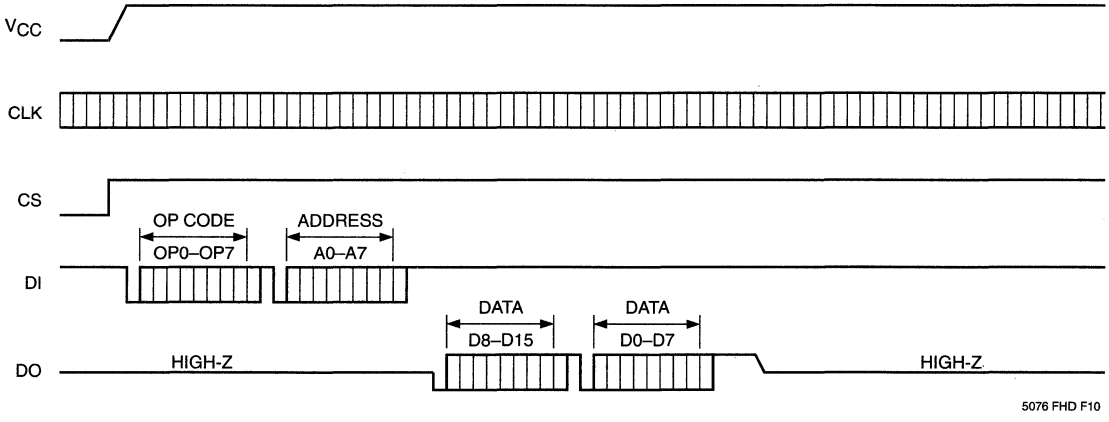


Figure 7. Read Timing (x16 Format)



DEVICE OPERATION

INSTRUCTIONS

The CAT33C804A instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

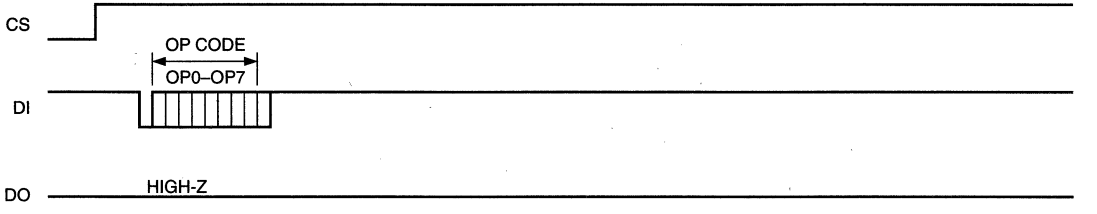
DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operation
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT33C804A is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

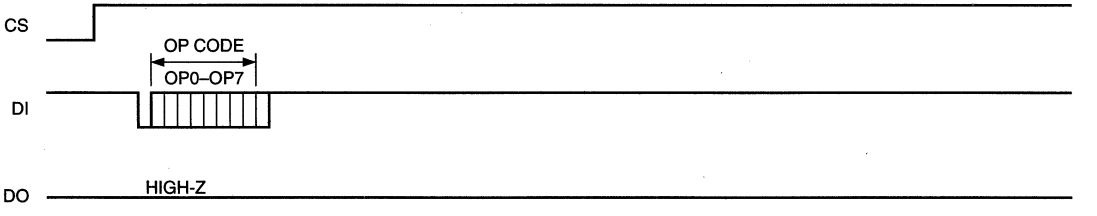
WMPR [address]

Figure 8. EWEN/EWDS Timing (x8 Format)



5076 FHD F11

Figure 9. EWEN/EWDS Timing (x16 Format)



5076 FHD F11

As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

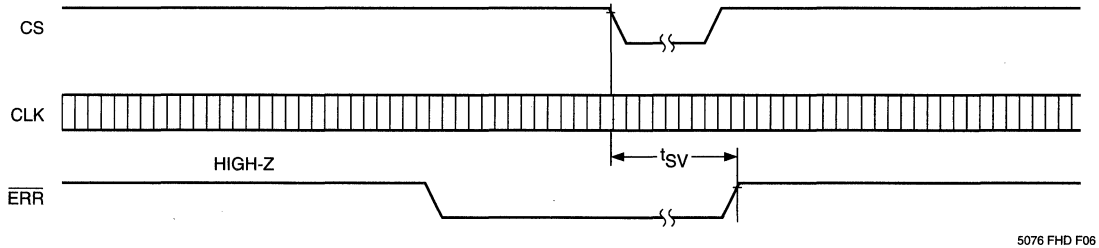
A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT33C804A will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

Figure 10. $\overline{ERR}$ Pin Timing



5076 FHD F06

As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT33C804A. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and

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Figure 11. Erase Timing (x8 Format)

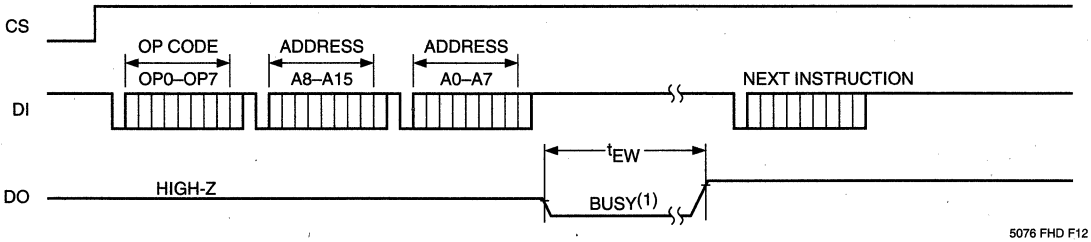
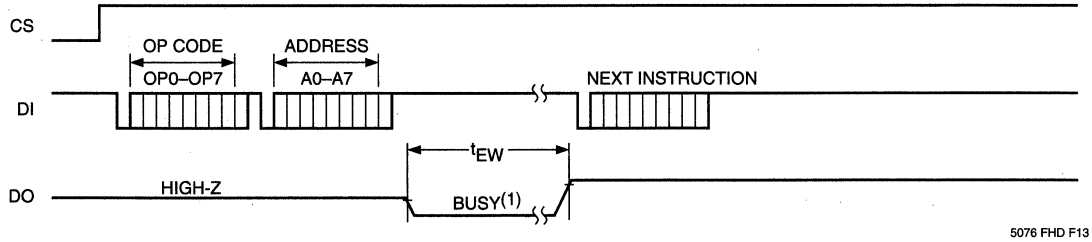


Figure 12. Erase Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in High-Z condition.

then the WRAL instruction. The CAT33C804A will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the stop bit. When PE is HIGH, the CAT33C804A expects a parity bit at the end of every byte. For example, the RSEQ instruction will look like this:

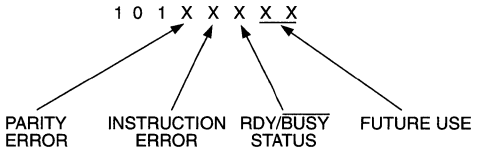
0 1100 1011 11
0 A15...A8 P1
0 A7...A0 P1

The device then outputs data continuously until it reaches the end of the memory. Each byte of data contains 9 bits with the ninth bit being the parity bit. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

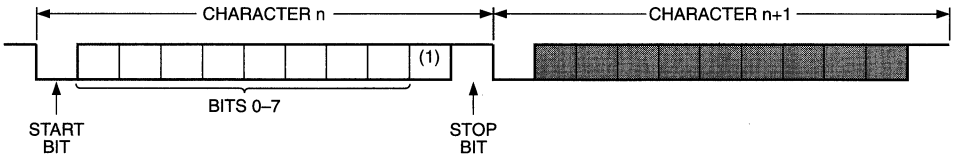
Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8-bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".



5074 FHD F09

Figure 13. Asynchronous Communication Protocol



5076 FHD F14

Note:
(1) Parity bit if enabled; skipped if parity disabled.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT33C804A will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

Figure 14. ERAL Timing (x8 Format)

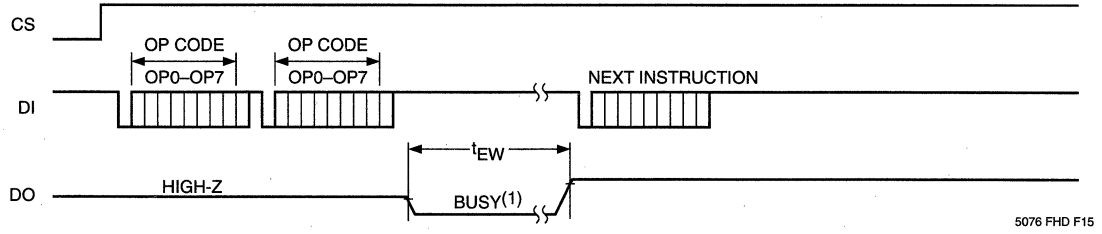
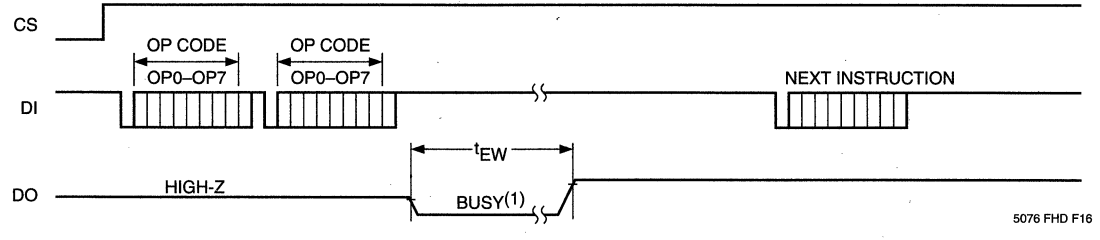


Figure 15. ERAL Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8-bit or 16-bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

Figure 16. WRAL Timing (x8 Format)

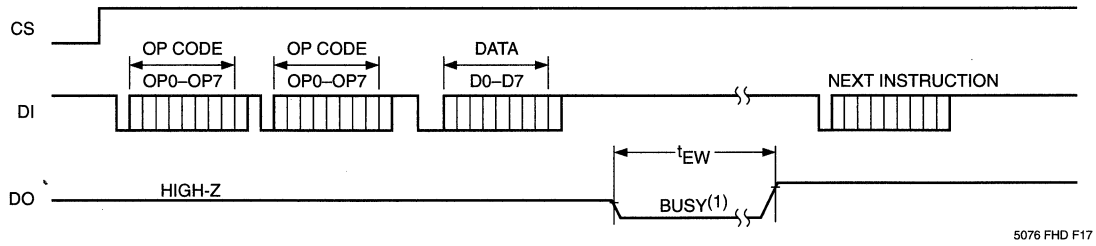
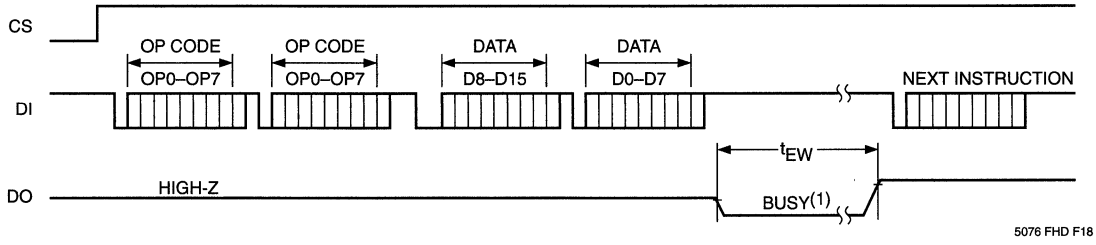


Figure 17. WRAL Timing (x16 Format)



Note:
(1) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

5

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

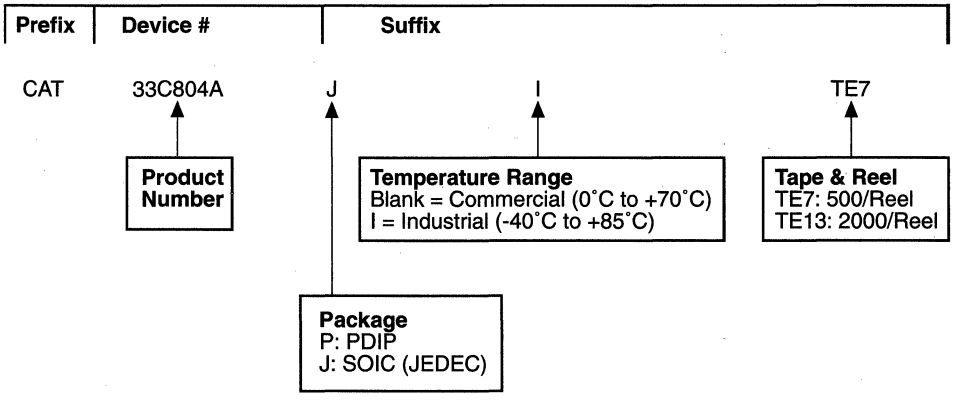
Output the contents of the 8-bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 33C804AJI-TE7 (SOIC, Industrial Temperature, Tape & Reel)

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CATALYST SEMICONDUCTOR

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Contents

Section 6 NVRAMs

CAT22C10 ..... 64 x 4 ..... 256-Bit 6-1

CAT24C44 ..... 16 x 16 ..... 256-Bit 6-11

CAT22C10

256-Bit Nonvolatile CMOS Static RAM

FEATURES

- Single 5V Supply
- Fast RAM Access Times:
  - –200ns
  - –300ns
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Power Up/Down Protection
- Low CMOS Power Consumption:
  - –Active: 40mA Max.
  - –Standby: 30 µA Max.
- JEDEC Standard Pinouts:
  - –18-pin DIP
  - –16-pin SOIC
- 10,000 Program/Erase Cycles (E²PROM)
- 10 Year Data Retention
- Commercial and Industrial Temperature Ranges

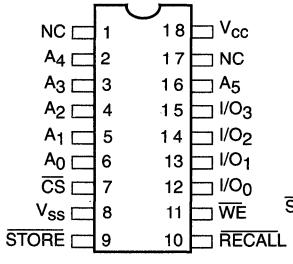
DESCRIPTION

The CAT22C10 NVRAM is a 256-bit nonvolatile memory organized as 64 words x 4 bits. The high speed Static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5µs. The CAT22C10 features unlimited RAM write operations either through external RAM writes or internal recalls from E²PROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.0V.

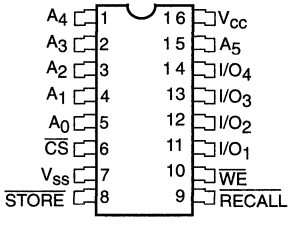
The CAT22C10 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in JEDEC approved 18-pin plastic DIP and 16-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



PIN FUNCTIONS

Pin Name	Function
A_0–A_5	Address
I/O_0–I/O_3	Data In/Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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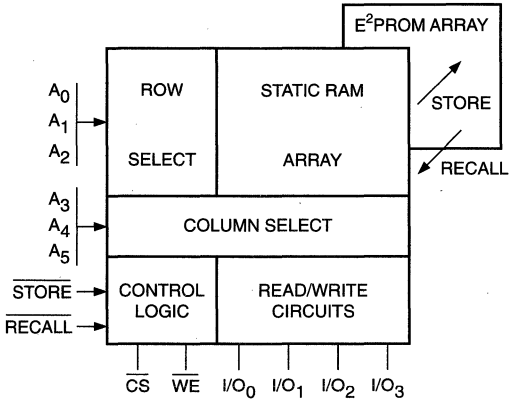
BLOCK DIAGRAM



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MODE SELECTION(1)(2)(3)

Mode	Input				I/O
	$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	
Standby	H	X	H	H	Output High-Z
RAM Read	L	H	H	H	Output Data
RAM Write	L	L	H	H	Input Data
(E^2PROM→RAM)	X	H	L	H	Output High-Z RECALL
(E^2PROM→RAM)	H	X	L	H	Output High-Z RECALL
(RAM→E^2PROM)	X	H	H	L	Output High-Z STORE
(RAM→E^2PROM)	H	X	H	L	Output High-Z STORE

POWER-UP TIMING(4)

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	0.5	0.005	V/ms

Note:
(1) $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time.
(2) $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active.
(3) The store operation is inhibited when V_{CC} is below ≈ 3.0V.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... -2.0 to +VCC +2.0V

V_{CC} with Respect to Ground ..... -2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CC}	Current Consumption (Operating)			40	mA	All Inputs = 5.5V T_A = 0°C All I/O's Open
I_{SB}	Current Consumption (Standby)			30	µA	$\overline{CS}$ = V_{CC} All I/O's Open
I_{LI}	Input Current			10	µA	0 ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			10	µA	0 ≤ V_{OUT} ≤ 5.5V
V_{IH}	High Level Input Voltage	2		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA
V_{DH}	RAM Data Holding Voltage	1.5		5.5	V	V_{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C10-20		22C10-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	200		300		ns	
t_{CW}	$\overline{CS}$ Write Pulse Width	150		150		ns	
t_{AS}	Address Setup Time	50		50		ns	C_L = 100pF
t_{WP}	Write Pulse Width	150		150		ns	+1TTL gate
t_{WR}	Write Recovery Time	25		25		ns	V_{OH} = 2.2V
t_{DW}	Data Valid Time	100		100		ns	V_{OL} = 0.65V
t_{DH}	Data Hold Time	0		0		ns	V_{IH} = 2.2V
t_{WZ}(1)	Output Disable Time		100		100	ns	V_{IL} = 0.65V
t_{OW}	Output Enable Time	0		0		ns	

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A.C. CHARACTERISTICS, Read Cycle

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C10-20		22C10-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		300		ns	C_L = 100pF
t_{AA}	Address Access Time		200		300	ns	+1TTL gate
t_{CO}	$\overline{CS}$ Access Time		200		300	ns	V_{OH} = 2.2V
t_{OH}	Output Data Hold Time	0		0		ns	V_{OL} = 0.65V
t_{LZ}(1)	$\overline{CS}$ Enable Time	0		0		ns	V_{IH} = 2.2V
t_{HZ}(1)	$\overline{CS}$ Disable Time		100		100	ns	V_{IL} = 0.65V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS, Store Cycle
V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{STC}	Store Time		10	ms	C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V
t_{STP}	Store Pulse Width	200		ns	
t_{STZ}(1)	Store Disable Time		100	ns	
t_{OST}(1)	Store Enable Time	0		ns	

A.C. CHARACTERISTICS, Recall Cycle
V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{RCC}	Recall Cycle Time	1.4		µs	C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V
t_{RCP}	Recall Pulse Width	300		ns	
t_{RCZ}	Recall Disable Time		100	ns	
t_{ORC}	Recall Enable Time	0		ns	
t_{ARC}	Recall Data Access Time		1.1	µs	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The configuration of the CAT22C10 allows a common address bus to be directly connected to the address inputs. Additionally, the Input/Output (I/O) pins can be directly connected to a common I/O bus if the bus has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) pin goes low, the device is activated. When $\overline{CS}$ is forced high, the device goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) pin selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0–A_5), and that byte will be read or written to through the Input/Output pins (I/O_0–I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ input high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

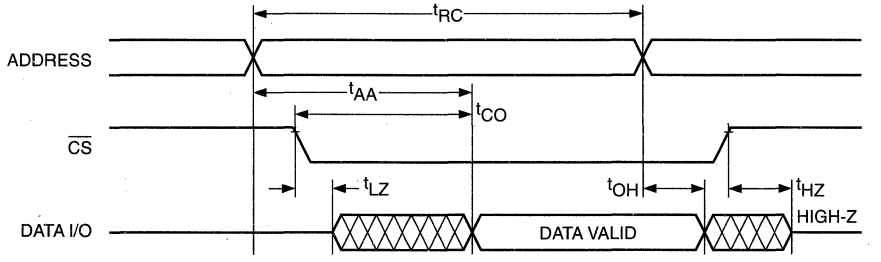
Standby Mode

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10. When a high level is supplied to the $\overline{CS}$ pin, the device goes into the standby mode where the outputs are put into a high impendance state and the power consumption is drastically reduced. With I_{SB} less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

Read

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). With the Write Enable ($\overline{WE}$) pin held high, the data in the Static RAM array may be accessed by selecting an address with input pins A_0–A_5. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

Figure 1. Read Cycle Timing



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Write

With the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) pin will select the write mode when driven to a low level. In this mode, the address must be supplied for the byte being written. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0–I/O_3. When these conditions, including the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the Static RAM. A write function may also be initiated from the standby mode by driving $\overline{WE}$ low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

Figure 2. Write Cycle Timing

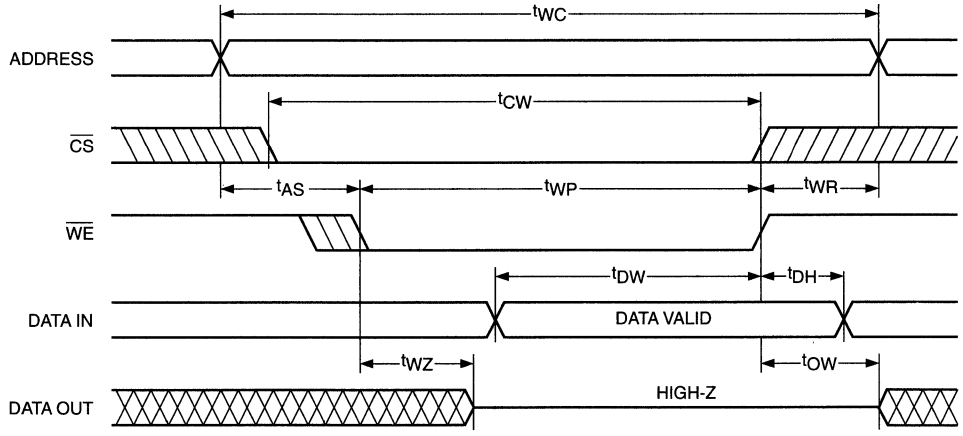

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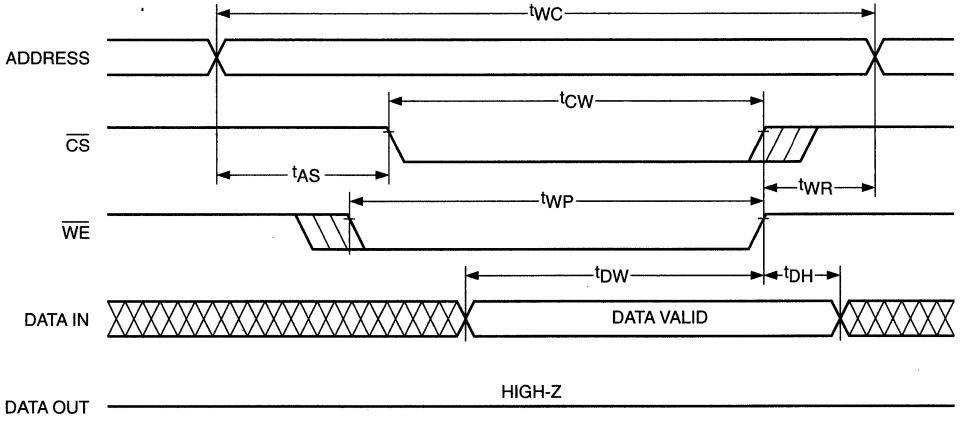
Figure 3. Early Write Cycle Timing



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Recall

At anytime, except during a store operation, taking the RECALL pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0–A_5. After the RECALL pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire contents of the E²PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}) is met. After this, any other byte may be accessed by using the normal read mode.

If the $\overline{RECALL}$ pin is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data.

The outputs I/O_0–I/O_3 will go into the high impedance state as long as the $\overline{RECALL}$ signal is held low.

Store

At any time, except during a recall operation, taking the $\overline{STORE}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{CS}$, $\overline{WE}$ or A_0–A_5. The STORE pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{STORE}$ pin becomes a "Don't Care", and the store operation will complete its transfer of the entire contents of the Static RAM array into the E²PROM array within the Store Cycle time (t_{STC}). If a store operation is initiated during a write cycle, the contents of the addressed Static RAM byte and its corresponding byte in the E²PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. A minimum of 10,000 store operations can be performed reliably and the data written into the E²PROM array has a minimum data retention time of 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.0V typ. This function eliminates the potential hazard of spurious signals initiating a store operation when the system power is below 3.0V typ.

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Figure 4. Recall Cycle Timing

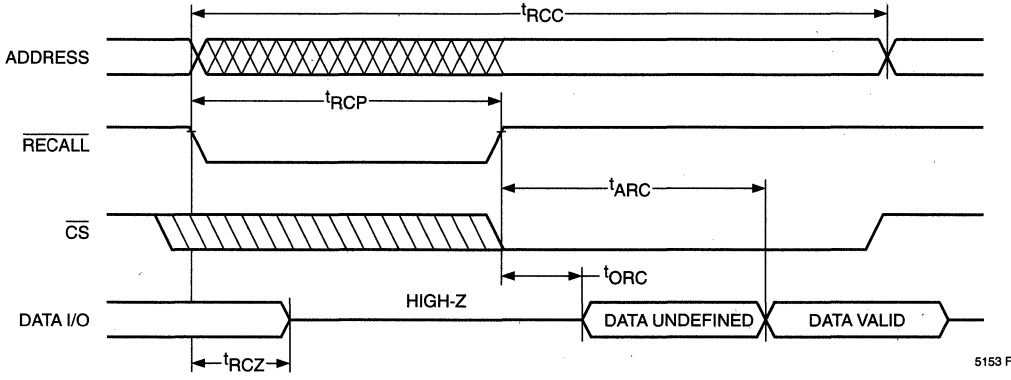
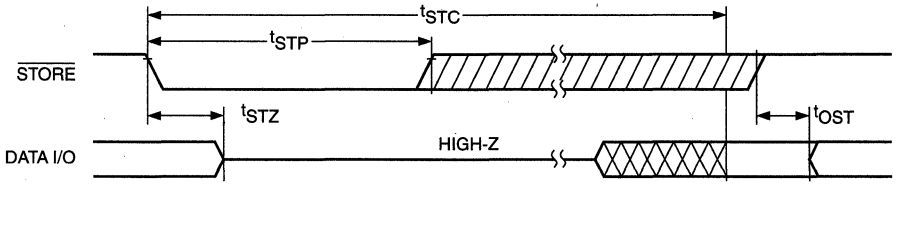
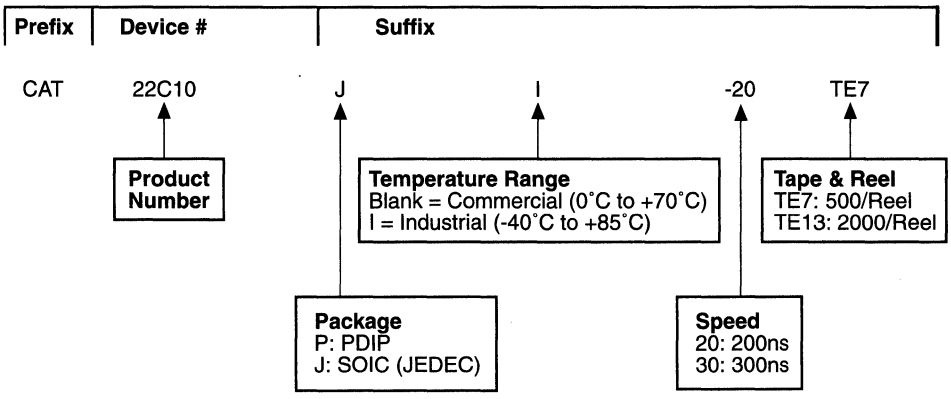


Figure 5. Store Cycle Timing



ORDERING INFORMATION



22C10 F08

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Notes:
(1) The device used in the above example is a 22C10JI-20TE7 (SOIC, Industrial Temperature, 200ns Access Time, Tape & Reel)

CAT24C44

256-Bit Serial Nonvolatile CMOS Static RAM

FEATURES

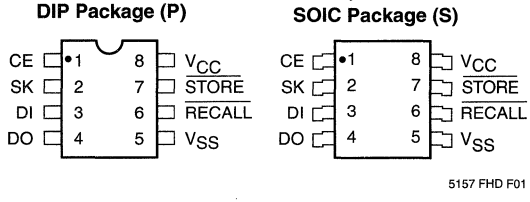
- Single 5V Supply
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Low CMOS Power Consumption:
  - –Active: 3 mA Max.
  - –Standby: 30 μA Max.
- Power Up/Down Protection
- Commercial and Industrial Temperature Ranges
- JEDEC Standard Pinouts:
  - –8-pin DIP
  - –8-pin SOIC
- 10,000 Program/Erase Cycles (E²PROM)
- 10 Year Data Retention
- Auto Recall on Power-up

DESCRIPTION

The CAT24C44 Serial NVRAM is a 256-bit nonvolatile memory organized as 16 words x 16 bits. The high speed Static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5μs. The CAT24C44 features unlimited RAM write operations either through external RAM writes or internal recalls from E²PROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.5V (typical) ensuring E²PROM data integrity.

The CAT24C44 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in JEDEC approved 8-pin plastic DIP and SOIC packages.

PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
SK	Serial Clock
DI	Serial Input
DO	Serial Data Output
CE	Chip Enable
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	+5V
V_{SS}	Ground

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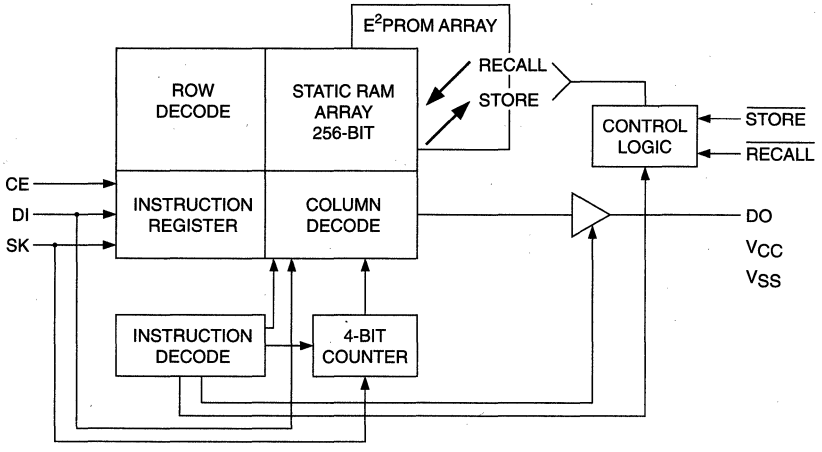
BLOCK DIAGRAM



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MODE SELECTION[1][2]

Mode	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch	Previous Recall Latch
Hardware Recall[3]	1	0	NOP	X	X
Software Recall	1	1	RCL	X	X
Hardware Store[3]	0	1	NOP	SET	TRUE
Software Store	1	1	STO	SET	TRUE

X = Don't Care

POWER-UP TIMING[4]

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	0.5	0.005	V/m
t_{pur}	Power-Up to Read Operations		200	µs
t_{puw}	Power-Up to Write or Store Operation		5	ms

Note:
(1) The store operation has priority over all the other operations.
(2) The store operation is inhibited when V_{CC} is below ≈ 3.5V.
(3) NOP designates that the device is not currently executing an instruction.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0 to +VCC +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CCO}	Current Consumption (Operating)			3	mA	Inputs = 5.5V, T_A = 0°C All Outputs Unloaded
I_{SB}	Current Consumption (Standby)			30	µA	CE = V_{IL}
I_{LI}	Input Current			2	µA	$0 \le V_{IN} \le 5.5V$
I_{LO}	Output Leakage Current			10	µA	$0 \le V_{OUT} \le 5.5V$
V_{IH}	High Level Input Voltage	2		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

A.C. CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
F_{SK}	SK Frequency	DC	1	MHz	
t_{SKH}	SK Positive Pulse Width	400		ns	
t_{SKL}	SK Negative Pulse Width	400		ns	C_L = 100pF + 1TTL gate
t_{DS}	Data Setup Time	400		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{DH}	Data Hold Time	80		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{PD}	SK Data Valid Time		375	ns	Input rise and fall times = 10ns
t_Z	CE Disable Time		1	µs	
t_{CES}	CE Enable Setup Time	800		ns	
t_{CEH}	CE Enable Hold Time	400		ns	
t_{CDS}	CE De-Select Time	800		ns	

A.C. CHARACTERISTICS, Store Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

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Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{ST}	Store Time		10	ms	C_L = 100pF + 1TTL gate
t_{STP}	Store Pulse Width	200		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{STZ}	Store Disable Time		100	ns	V_{IH} = 2.2V, V_{IL} = 0.65V

A.C. CHARACTERISTICS, Recall Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RCC}	Recall Cycle Time	2.5		µs	
t_{RCP}	Recall Pulse Width	500		ns	C_L = 100pF + 1TTL gate
t_{RCZ}	Recall Disable Time		500	ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{ORC}	Recall Enable Time	10		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{ARC}	Recall Data Access Time		1.5	µs	

INSTRUCTION SET

Instruction	Format			Operation
	Start Bit	Address	OP Code	
WRDS	1	XXXX	0 0 0	Reset Write Enable Latch (Disables, Writes and Stores)
STO	1	XXXX	0 0 1	Store RAM Data in E^2PROM
WRITE	1	AAAA	0 1 1	Write Data into RAM Address AAAA
WREN	1	XXXX	1 0 0	Set Write Enable Latch (Enables, Writes and Stores)
RCL	1	XXXX	1 0 1	Recall E^2PROM Data into RAM
READ	1	AAAA	1 1 X	Read Data From RAM Address AAAA

X = Don't care
A = Address bit

DEVICE OPERATION

The CAT24C44 is intended for use with standard microprocessors. The CAT24C44 is organized as 16 registers by 16 bits. Seven 8-bit instructions control the device's operating modes, the RAM reading and writing, and the E^2PROM storing and recalling. It is also possible to control the E^2PROM store and recall functions in hardware with the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins. The CAT24C44 operates on a single 5V supply and will generate, on chip, the high voltage required during a RAM to E^2PROM storing operation.

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The $\overline{\text{CE}}$ (Chip Enable) pin must remain high during the entire data transfer.

The format for all instructions sent to the CAT24C44 is a logical '1' start bit, 4 address bits (data read or write operations) or 4 "Don't Care" bits (device mode operations), and a 3-bit op code (see Instruction Set). For data write operations, the 8-bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "Don't Care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to form a common DI/DO line. A word of caution while clocking data to and from the device: If the CE pin is prematurely deselected while shifting in an instruction, that instruction will not be executed, and the shift register internal to the CAT24C44 will be cleared. If there are more than or less than 16 clocks during a memory data transfer, an improper data transfer will result. The SK clock is completely static allowing the user to stop the clock and restart it to resume shifting of data.

Read

Upon receiving a start bit, 4 address bits, and the 3-bit read command (clocked into the DI pin), the DO pin of the CAT24C44 will come out of the high impedance state and the 16 bits of data, located at the address specified in the instructions, will be clocked out of the device. When clocking data from the device, the first bit clocked out (DO) is timed from the falling edge of the 8th clock, all succeeding bits (D1–D15) are timed from the rising edge of the clock.

Write

After receiving a start bit, 4 address bits, and the 3-bit WRITE command, the 16-bit word is clocked into the device for storage into the RAM memory location specified. The CE pin must remain high during the entire write operation.

6

Figure 1. RAM Read Cycle Timing

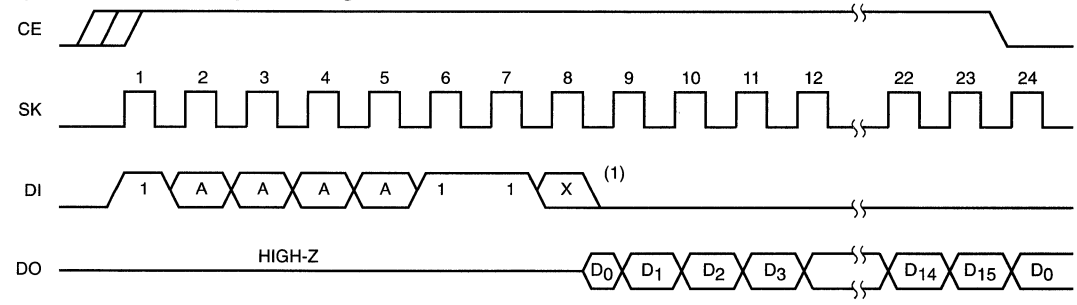

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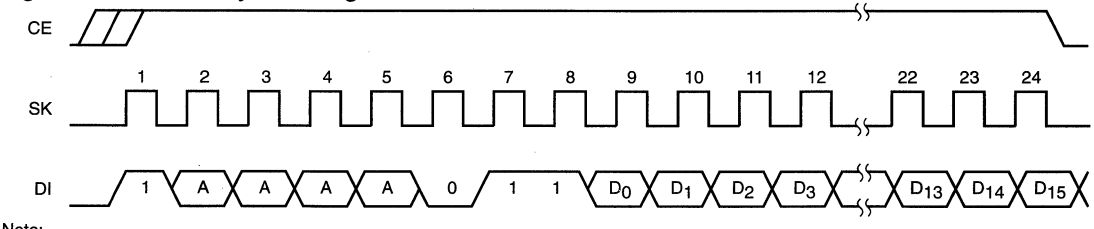
Figure 2. RAM Write Cycle Timing



Note:
(1) Bit 8 of READ instruction is "Don't Care".

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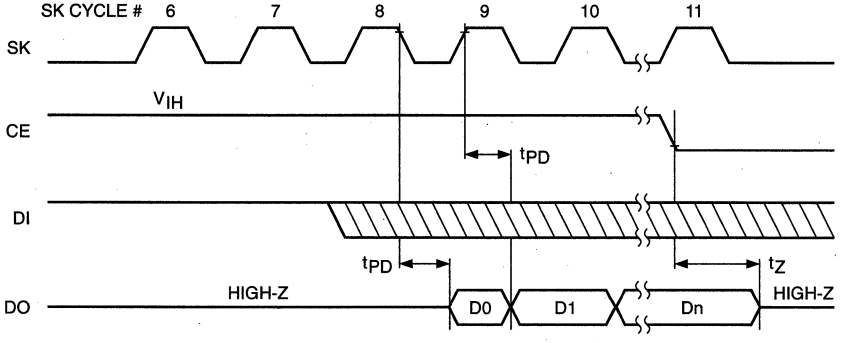
WREN/WRDS

The CAT24C44 powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/E²PROM store disable) instruction must first be preceded by the WREN (RAM write/E²PROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an E²PROM store has been executed (STO). The WRDS (write/store disable) can be used to disable all CAT24C44 programming functions, and will prevent any accidental writing to the RAM, or storing to the E²PROM.

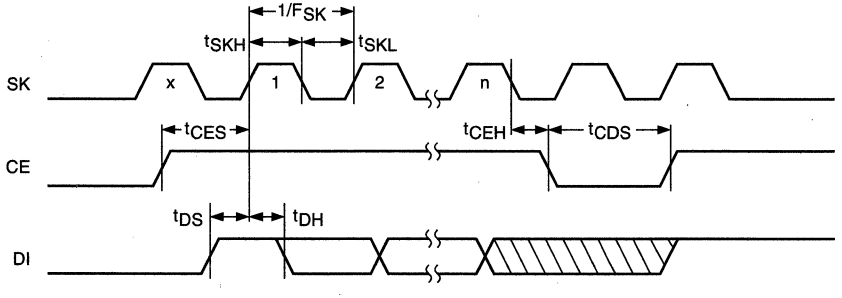
Data can be read normally from the CAT24C44 regardless of the "write enable latch" status.

Figure 3. Read Cycle Timing



5157 FHD F04

Figure 4. Write Cycle Timing



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RCL/$\overline{\text{RECALL}}$

Data is transferred from the E^2PROM data memory to RAM by either sending the RCL instruction or by pulling the $\overline{\text{RECALL}}$ input pin low. A recall operation must be performed before the E^2PROM store, or RAM write operations can be executed. Either a hardware or software recall operation will set the "previous recall" latch internal to the CAT24C44.

POWER-ON RECALL

The CAT24C44 has a power-on recall function that transfers the E^2PROM data to the RAM. After Power-up, all functions are inhibited for at least 200ns (T_{pur}) from stable V_{CC}.

STO/$\overline{\text{STORE}}$

Data in the RAM memory area is stored in the E^2PROM memory either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low. As security against any inadvertent store operations, the following conditions must each be met before data can be transferred into nonvolatile storage:

- The "previous recall" latch must be set (either a software or hardware recall operation).
- The "write enable" latch must be set (WREN instruction issued).
- STO instruction issued or $\overline{\text{STORE}}$ input low.

During the store operation, all other CAT24C44 functions are inhibited. Upon completion of the store operation, the "write enable" latch is reset. The device also provides false store protection whenever V_{CC} falls below a 3.5V level. If V_{CC} falls below this level, the store operation is disabled and the "write enable" latch is reset.

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Figure 5. Recall Cycle Timing

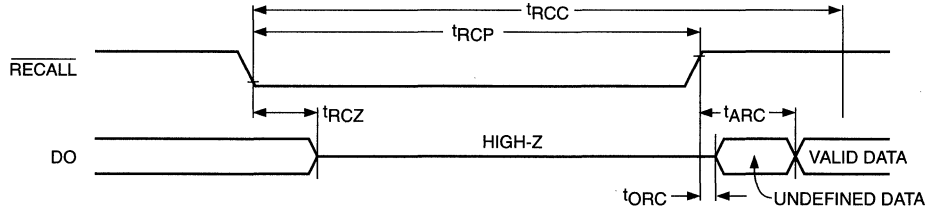

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Figure 6. Hardware Store Cycle Timing

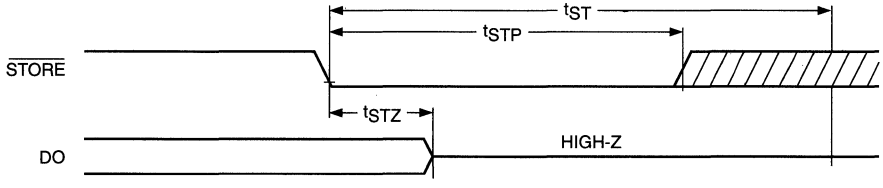

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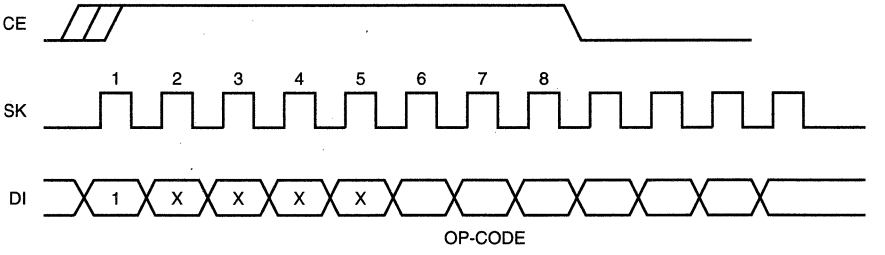
Figure 7. Non-Data Operations



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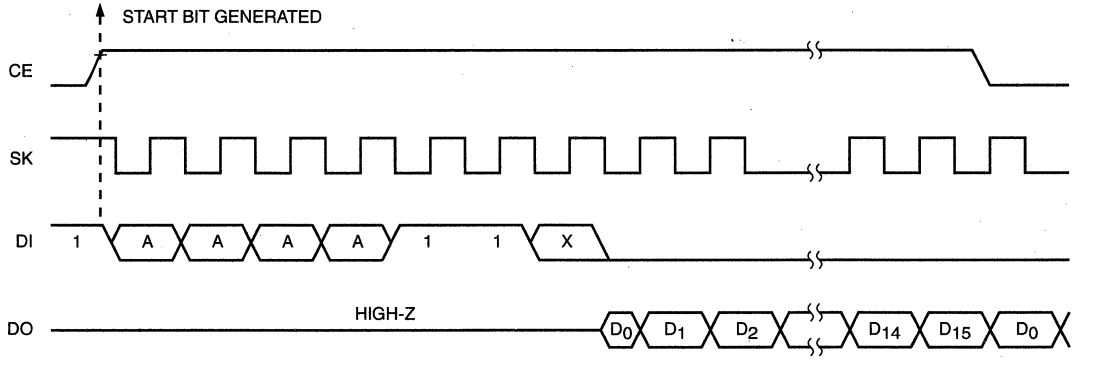
Start Bit Timing

The CAT24C44 features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CE (see Figure 8). Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 8. Alternate Start Bit Timing Example: Read Instruction



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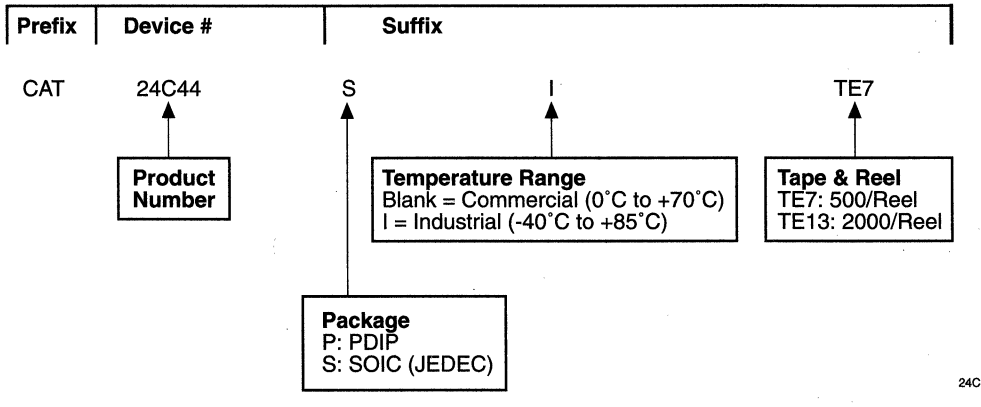
ORDERING INFORMATION



24C44 F11

Notes:
(1) The device used in the above example is a 24C44SI-TE7 (SOIC, Industrial Temperature, Tape & Reel)

CATALYST SEMICONDUCTOR

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CAT28F010 ..... 1 M-Bit 8-Bit Data Bus 7-15

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CAT28F001 ..... 1 M-Bit Boot Block 7-71

CAT28F002 ..... 2 M-Bit Boot Block 7-73

CAT28F512

512K-Bit CMOS Flash Memory

FEATURES

- **Fast Read Access Time: 90/120/150 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 30 mA max (CMOS/TTL levels)**
  - **–Standby: 1 mA max (TTL levels)**
  - **–Standby: 100 μA max (CMOS levels)**
- **High Speed Programming:**
  - **–10 μs per byte**
  - **–1 Sec Typ Chip Program**
- **12.0V ± 5% Programming and Erase Voltage**
- **Commercial and Industrial Temperature Ranges**
- **Stop Timer for Program/Erase**
- **On-Chip Address and Data Latches**
- **JEDEC Standard Pinouts:**
  - **–32-pin DIP**
  - **–32-pin PLCC**
  - **–32-pin TSOP (8 x 14; 8 x 20)**
- **100,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Electronic Signature**

DESCRIPTION

The CAT28F512 is a high speed 64K x 8-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F512 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin plastic DIP, 32-pin PLCC or 32-pin TSOP packages.

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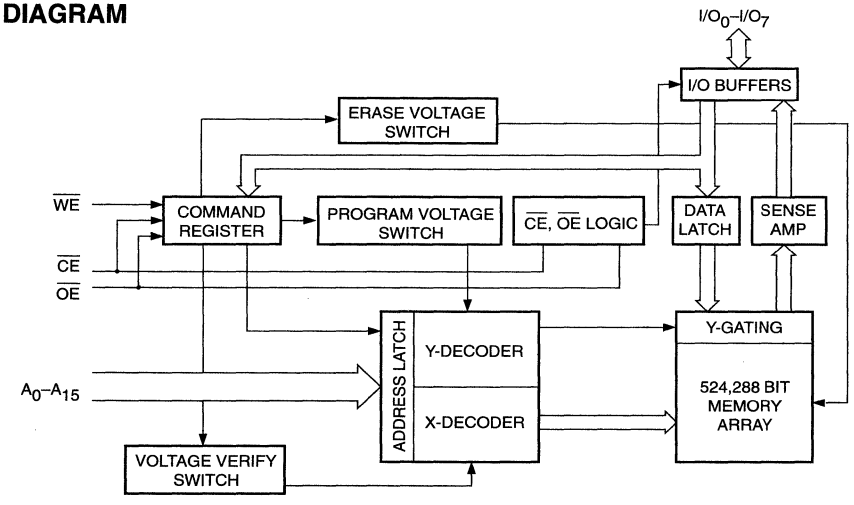
BLOCK DIAGRAM



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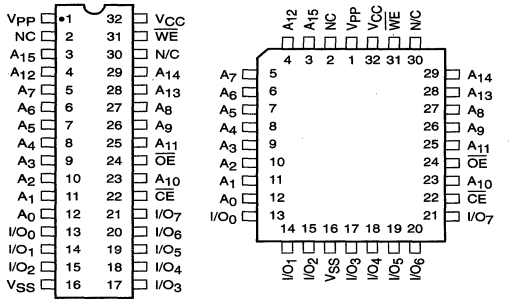
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P) **PLCC Package (N)**



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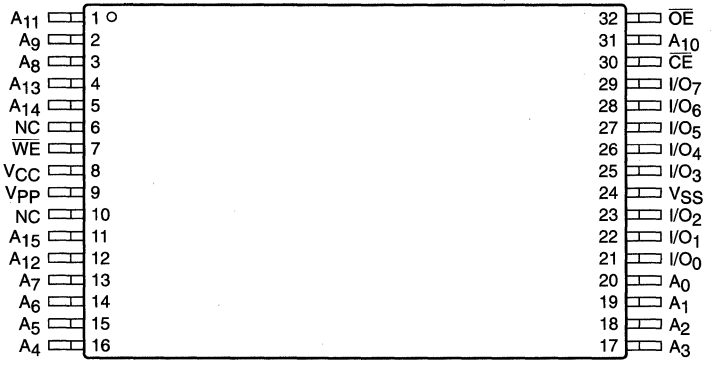
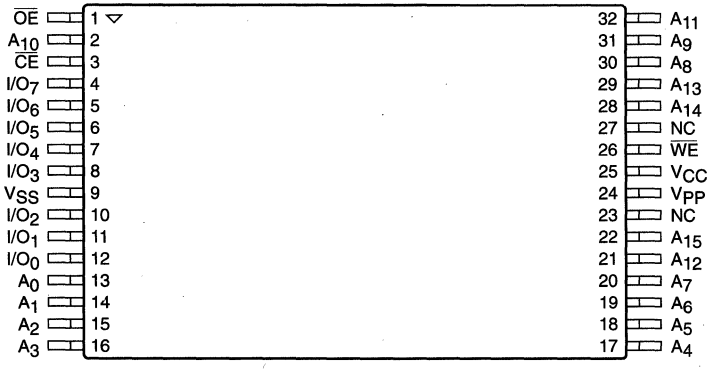
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{15}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout 8mm x 20mm) (T)
TSOP Package (Standard Pinout 8mm x 14mm) (T14)



TSOP Package (Reverse Pinout) (TR)



5108 FHD F14

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) ..... –2.0V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

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CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±1	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current		15	mA	V_{CC} = 5.5V, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	V_{CC}*0.7	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13	V	$A_9 = V_{ID}$
I_{ID}(1)	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

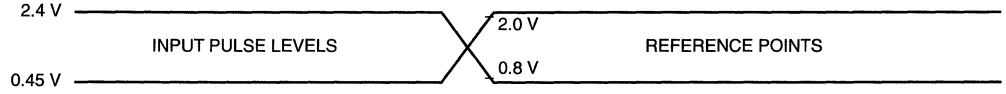
Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified.

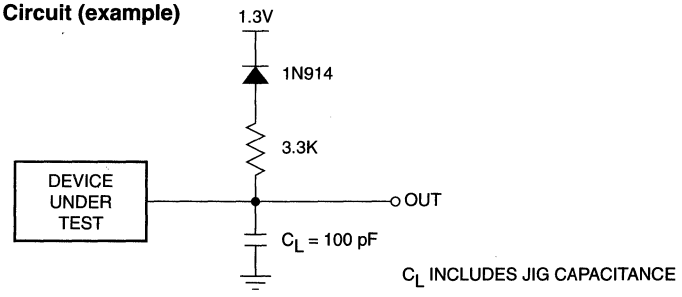
JEDEC Symbol	Standard Symbol	Parameter	28F512-90		28F512-12		28F512-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	90		120		150		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		90		120		150	ns
t_{AVQV}	t_{ACC}	Address Access Time		90		120		150	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		35		50		55	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		20		30		35	ns
t_{EHQZ}	t_{DF}(1)(2)	$\overline{CE}$ High to Output High-Z		30		40		45	ns
t_{WHGL}(1)	-	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)



5108 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



5108 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F512-90		28F512-12		28F512-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	40		40		40		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}(2)	-	Program Pulse Width	10		10		10		µs
t_{WHWH2}(2)	-	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

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ERASE AND PROGRAMMING PERFORMANCE(1)

Parameter	28F512-90			28F512-12			28F512-15			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(3)(5)		0.5	10		0.5	10		0.5	10	sec
Chip Program Time(3)(4)		1	6		1	6		1	6	sec

Note:
(1) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(2) Program and Erase operations are controlled by internal stop timers.
(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(5) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(1)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	B8H	$A_0 = V_{IH}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	A_{IN}		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B8H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	A_{IN}	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512 Code = 1011 1000 (B8H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F512 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

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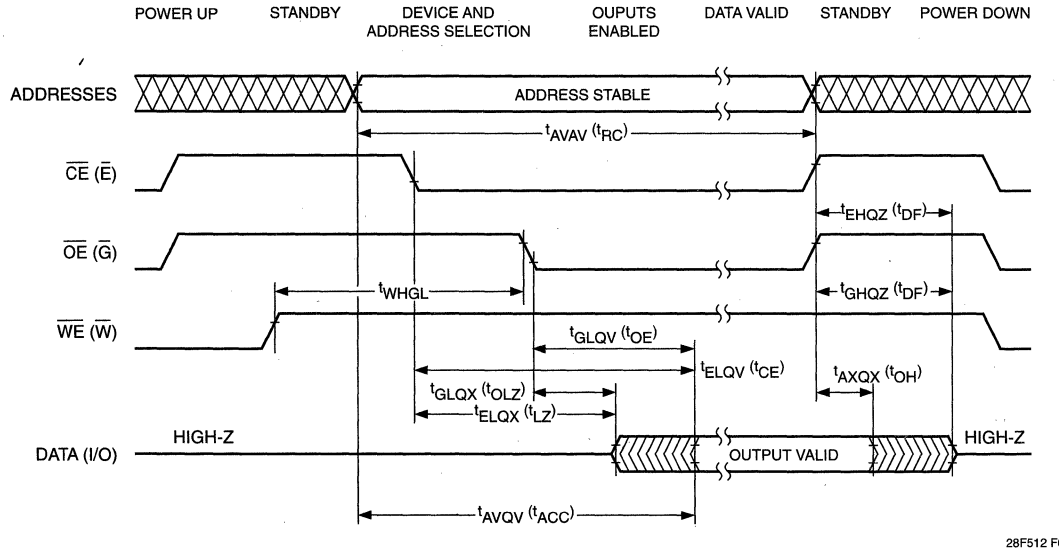
Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E²PROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and OE low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512 Code = 1011 1000 (B8H)

Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 4. A.C. Timing for Erase Operation

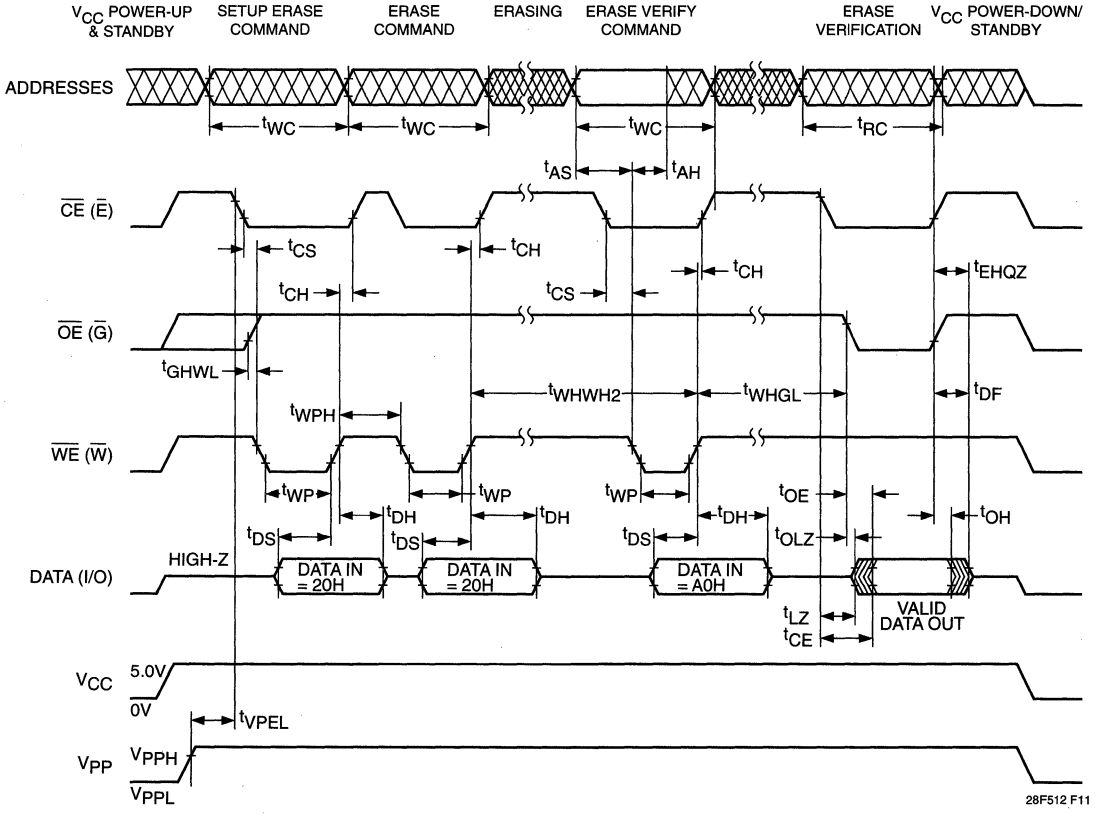
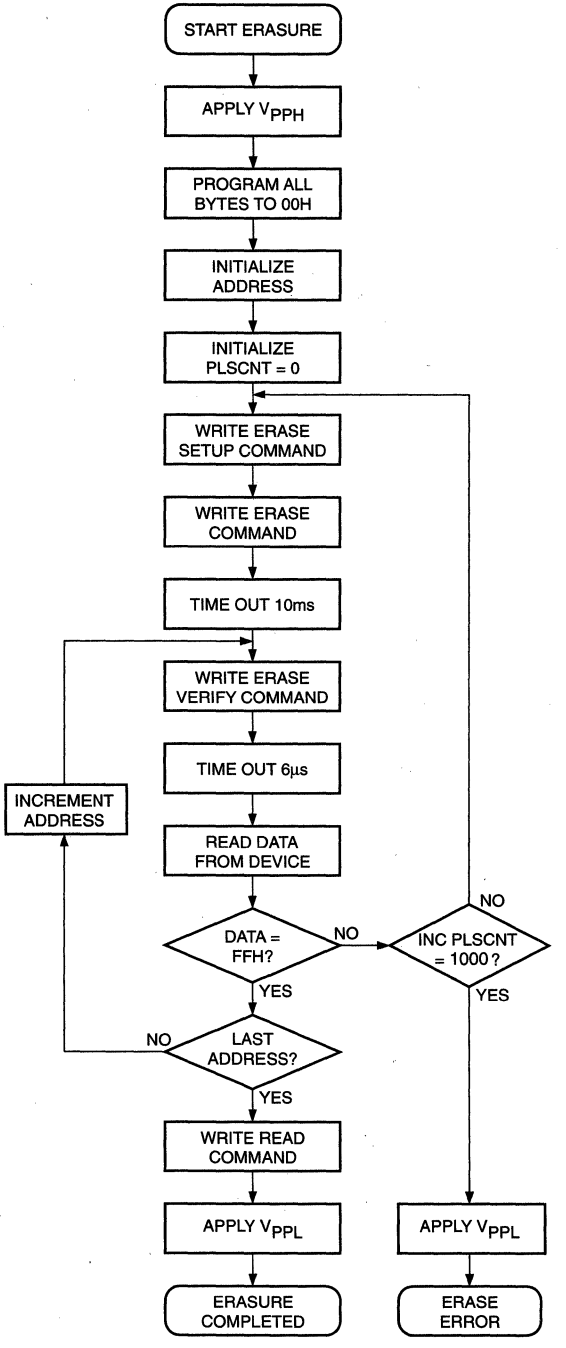


Figure 5. Chip Erase Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	DATA = 20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = A0H STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation

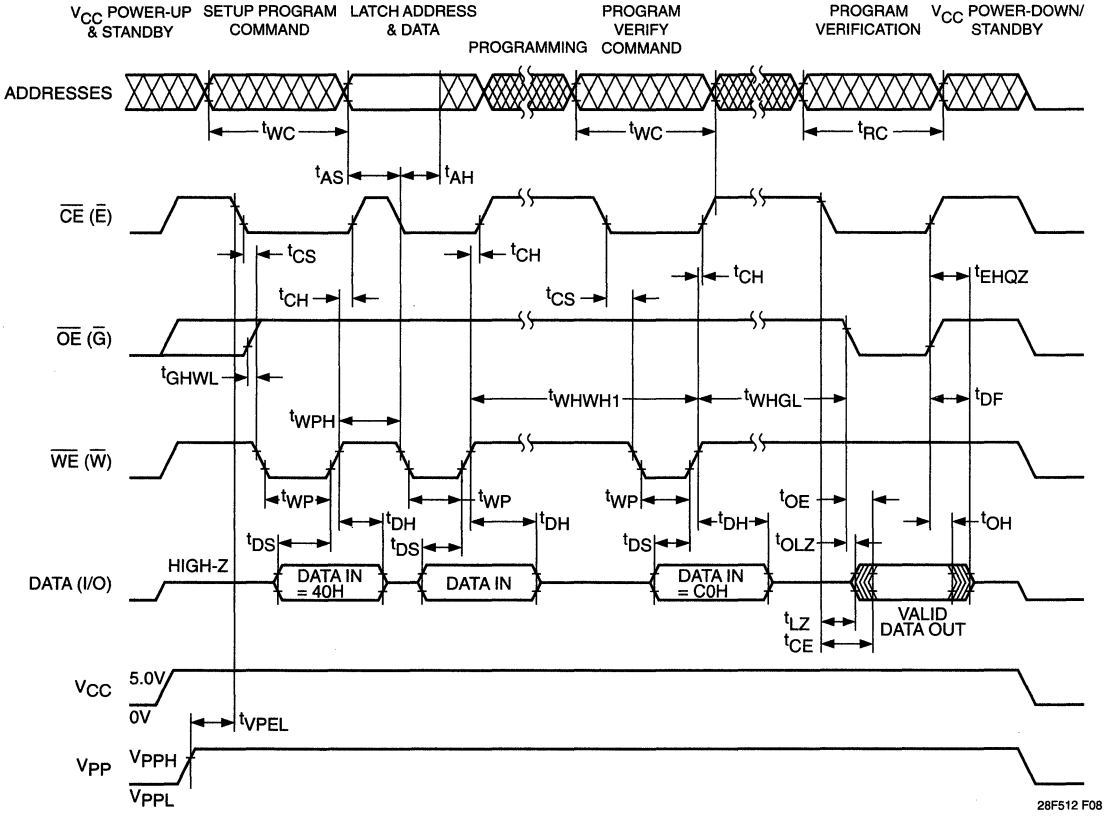
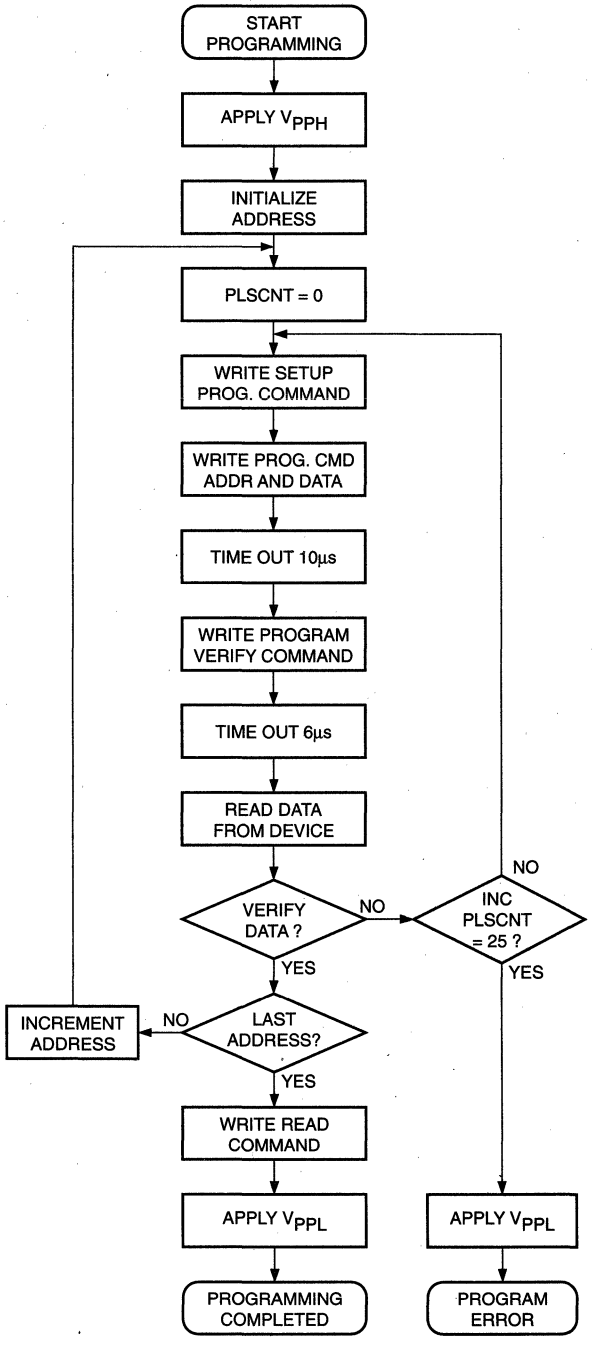


Figure 7. Programming Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

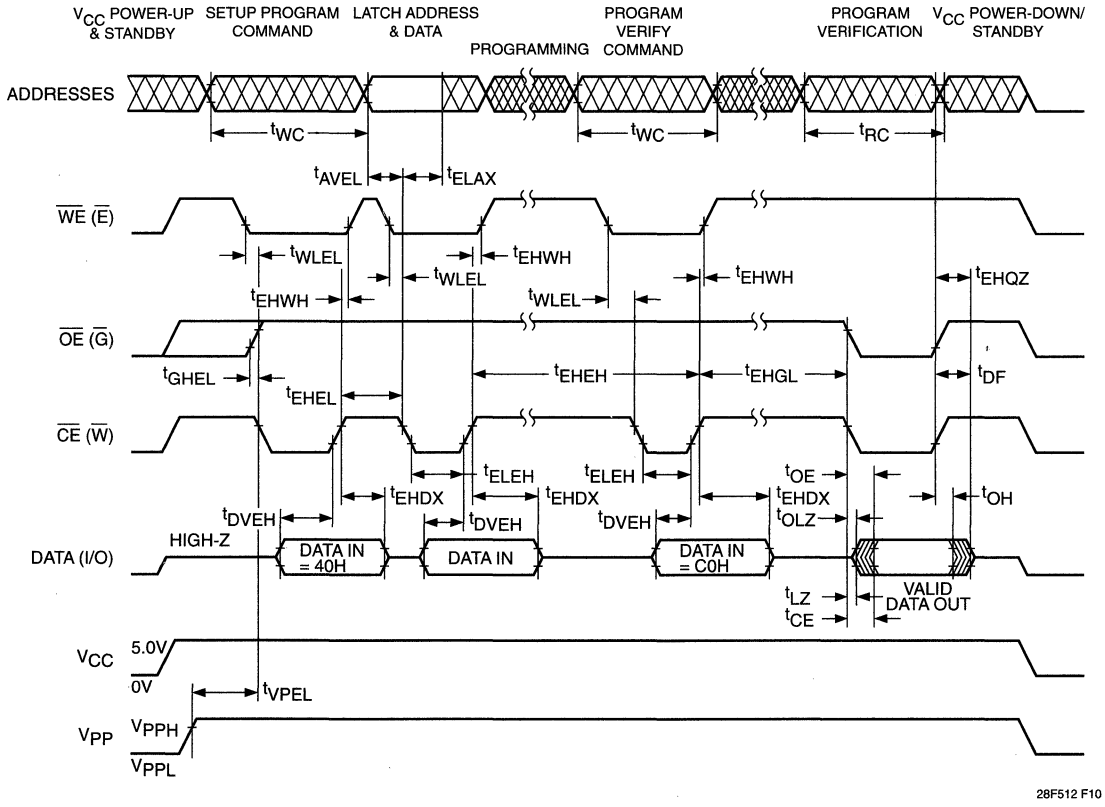
POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

POWER UP/DOWN PROTECTION

The CAT28F512 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F512 is reset to the Read Mode on power up.

Figure 8. Alternate A.C. Timing for Program Operation



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ALTERNATE $\overline{CE}$-CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	28F512-90		28F512-12		28F512-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		120		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{EHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	-	$\overline{WE}$ Hold Time After $\overline{CE}$	0		0		0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	40		40		40		ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$ Low	100		100		100		ns

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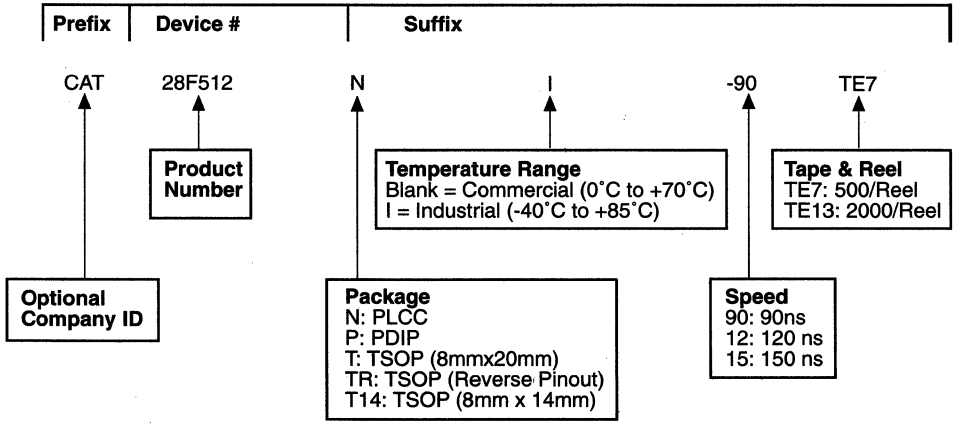
ORDERING INFORMATION



28F512 F12

Notes:
(1) The device used in the above example is a CAT28F512NI-90TE7 (PLCC, Industrial Temperature, 90ns Access Time, Tape & Reel)

CAT28F010

1 Megabit CMOS Flash Memory

FEATURES

- **Fast Read Access Time: 90/120/150 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 30 mA max (CMOS/TTL levels)**
  - **–Standby: 1 mA max (TTL levels)**
  - **–Standby: 100 μA max (CMOS levels)**
- **High Speed Programming:**
  - **–10 μs per byte**
  - **–2 Sec Typ Chip Program**
- **0.5 Seconds Typical Chip-Erase**
- **12.0V ± 5% Programming and Erase Voltage**
- **Commercial and Industrial Temperature Ranges**
- **Stop Timer for Program/Erase**
- **On-Chip Address and Data Latches**
- **JEDEC Standard Pinouts:**
  - **–32-pin DIP**
  - **–32-pin PLCC**
  - **–32-pin TSOP (8 x 14; 8 x 20)**
- **100,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Electronic Signature**

DESCRIPTION

The CAT28F010 is a high speed 128K x 8-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F010 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin plastic DIP, 32-pin PLCC or 32-pin TSOP packages.

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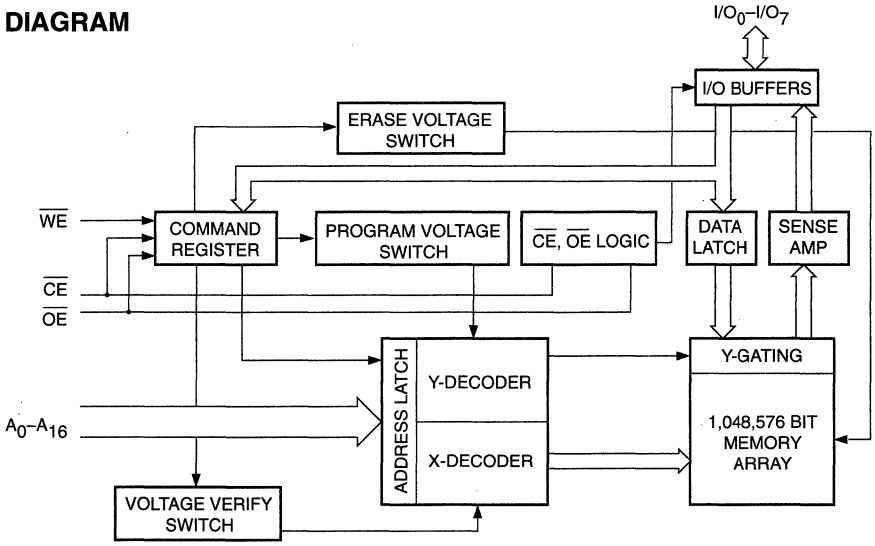
BLOCK DIAGRAM



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TD 5108

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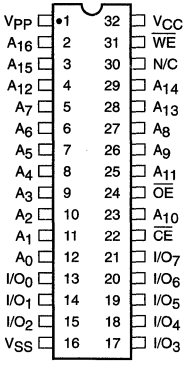
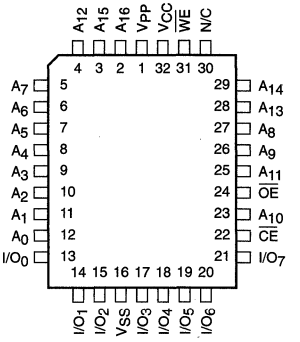
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



PLCC Package (N)



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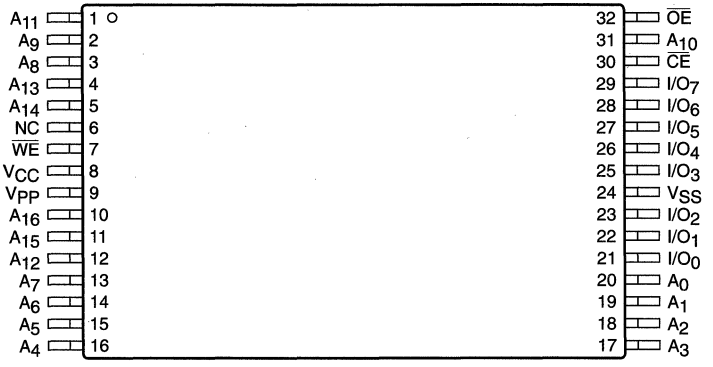
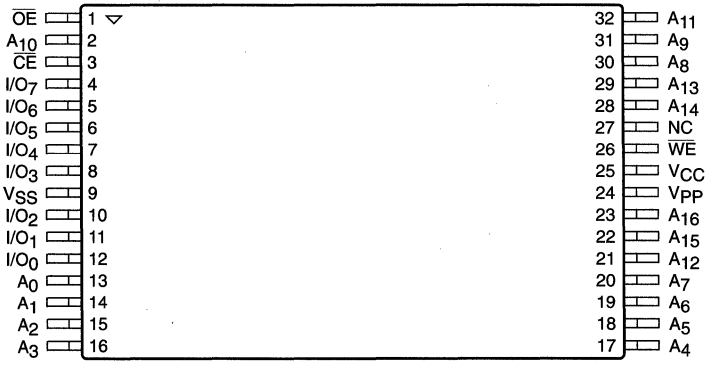
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{16}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout 8mm x 20mm) (T)
TSOP Package (Standard Pinout 8mm x 14mm) (T14)



TSOP Package (Reverse Pinout) (TR)



5108 FHD F14

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) ..... –2.0V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±1	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current		15	mA	V_{CC} = 5.5V, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	V_{CC}*0.7	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13	V	$A_9 = V_{ID}$
I_{ID}(1)	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F010-90		28F010-12		28F010-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	90		120		150		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		90		120		150	ns
t_{AVQV}	t_{ACC}	Address Access Time		90		120		150	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		35		50		55	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		20		30		35	ns
t_{EHQZ}	t_{DF}(1)(2)	$\overline{CE}$ High to Output High-Z		30		40		45	ns
t_{WHGL}(1)	-	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)

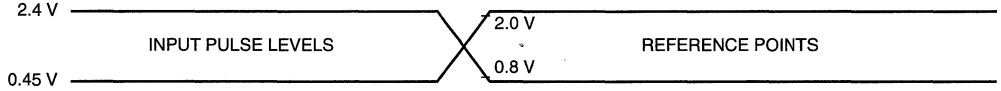


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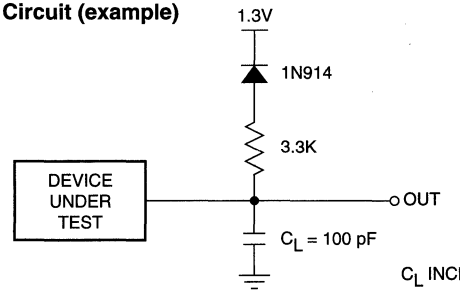
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F010-90		28F010-12		28F010-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	40		40		40		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}(2)	-	Program Pulse Width	10		10		10		µs
t_{WHWH2}(2)	-	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

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ERASE AND PROGRAMMING PERFORMANCE(1)

Parameter	28F010-90			28F010-12			28F010-15			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(3)(5)		0.5	10		0.5	10		0.5	10	sec
Chip Program Time(3)(4)		2	12.5		2	12.5		2	12.5	sec

Note:
(1) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(2) Program and Erase operations are controlled by internal stop timers.
(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(5) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(1)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	B4H	$A_0 = V_{IH}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	A_{IN}		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B4H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	A_{IN}	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010 Code = 1011 0100 (B4H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F010 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

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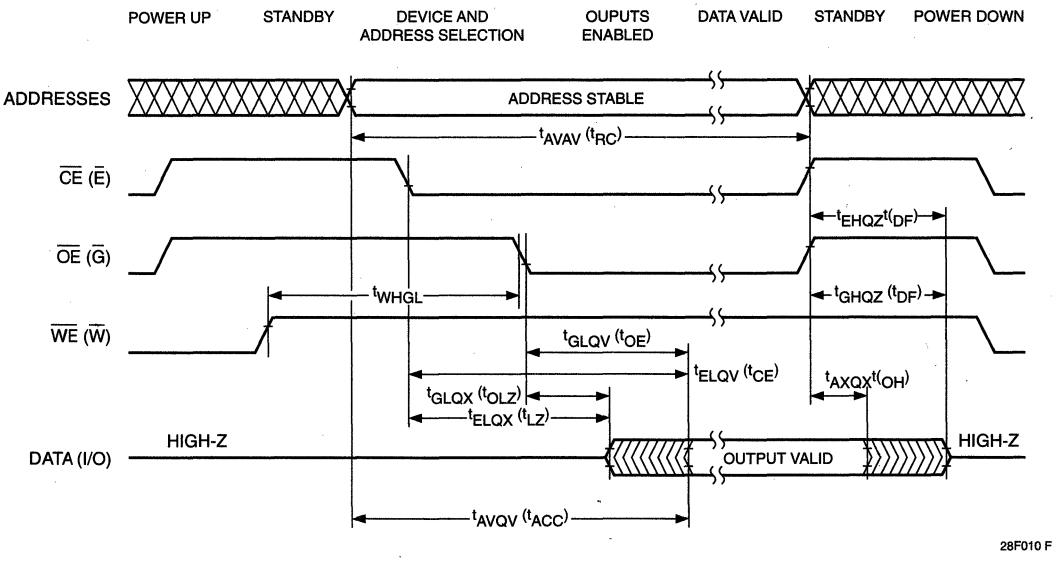
Figure 3. A.C. Timing for Read Operation



WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E²PROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010 Code = 1011 0100 (B4H)

Figure 4. A.C. Timing for Erase Operation

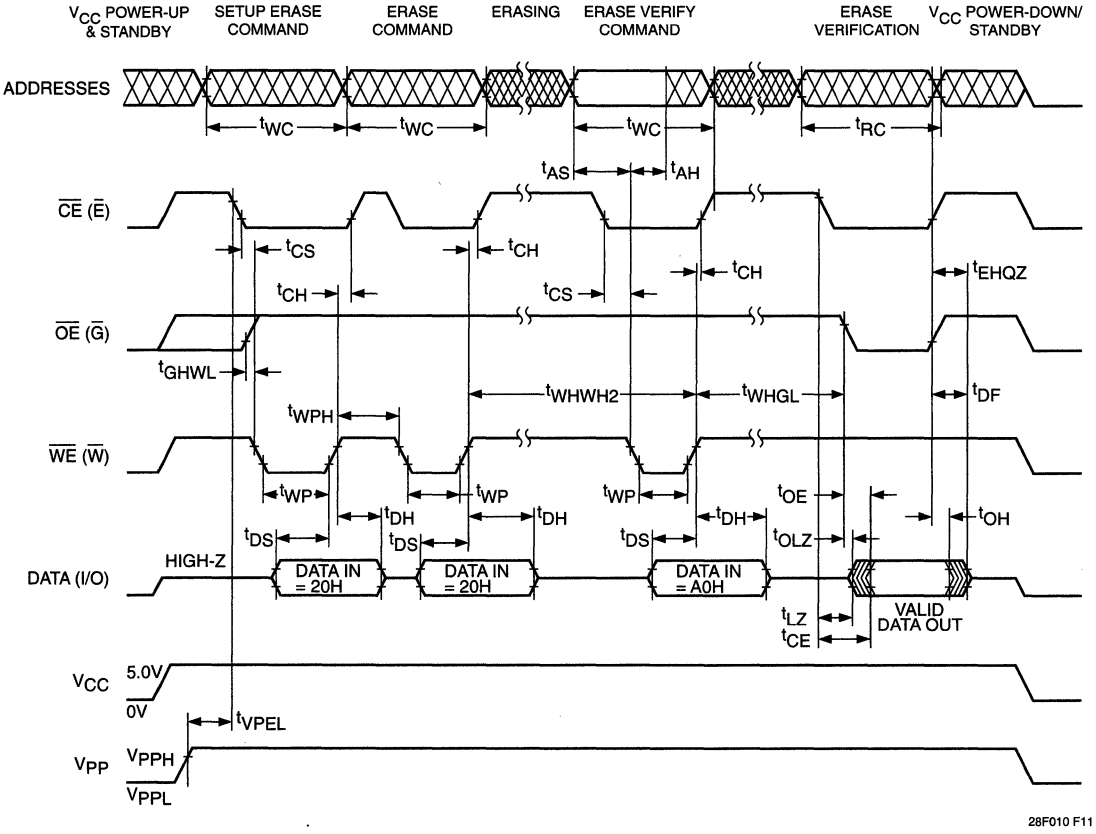


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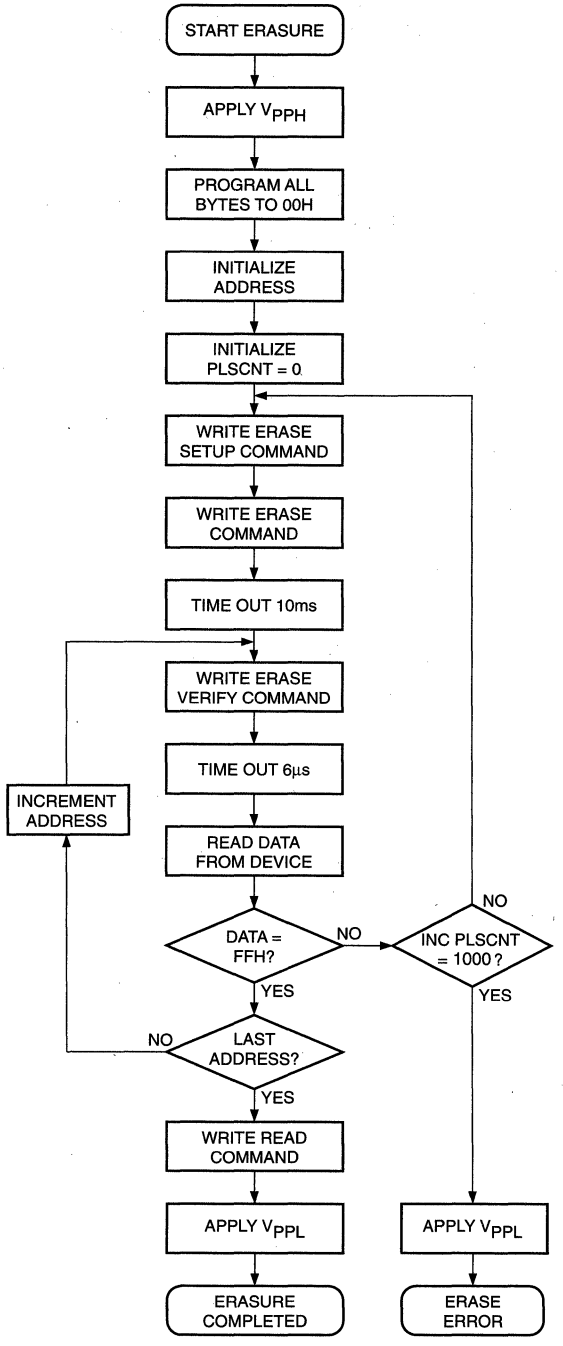
Figure 5. Chip Erase Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	DATA = 20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = A0H STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation

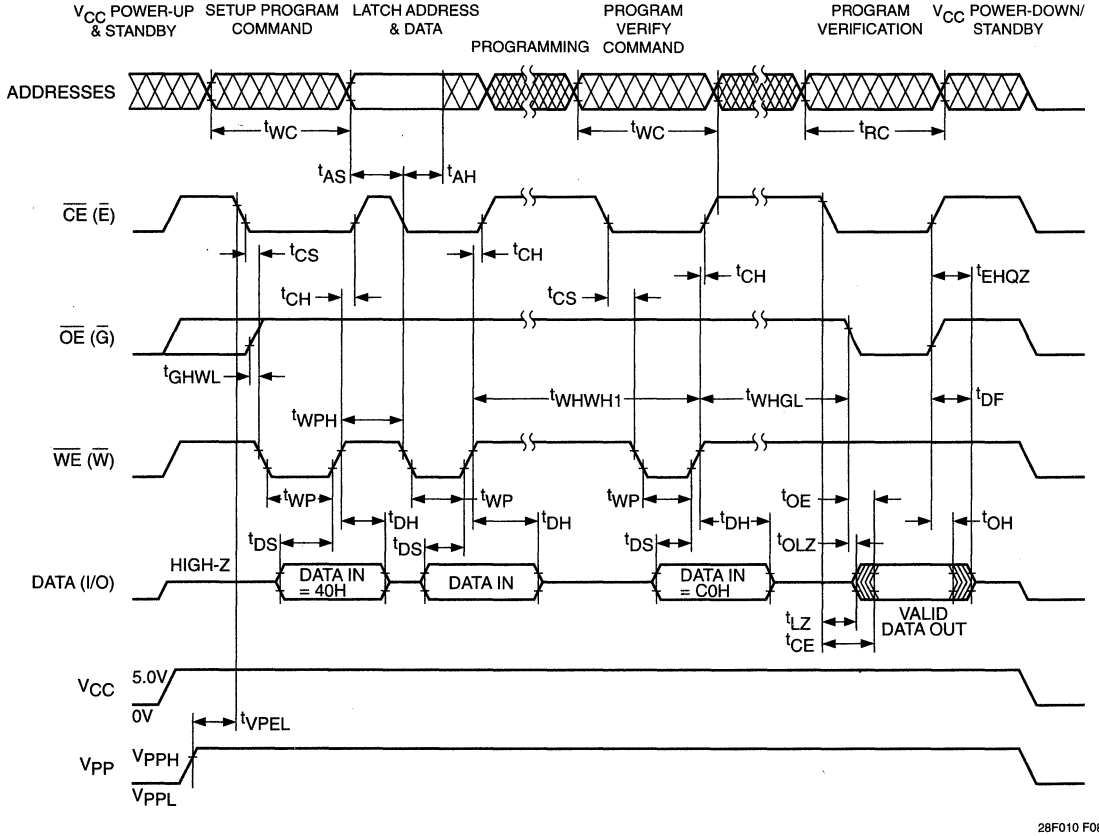
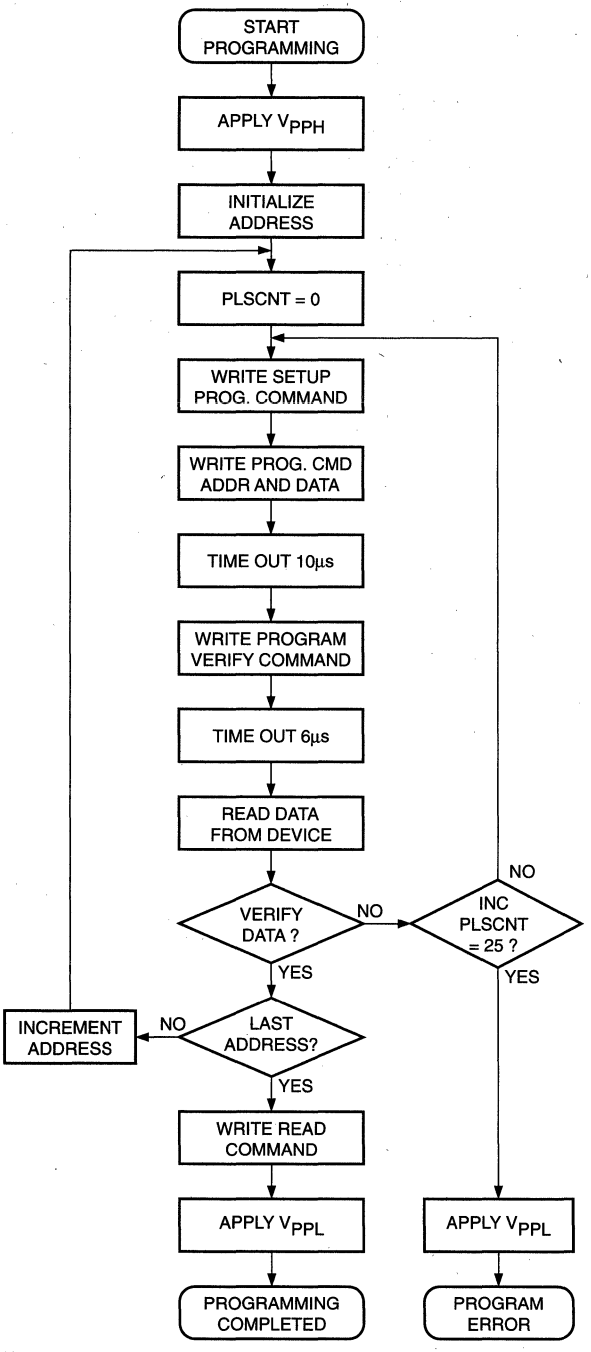


Figure 7. Programming Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

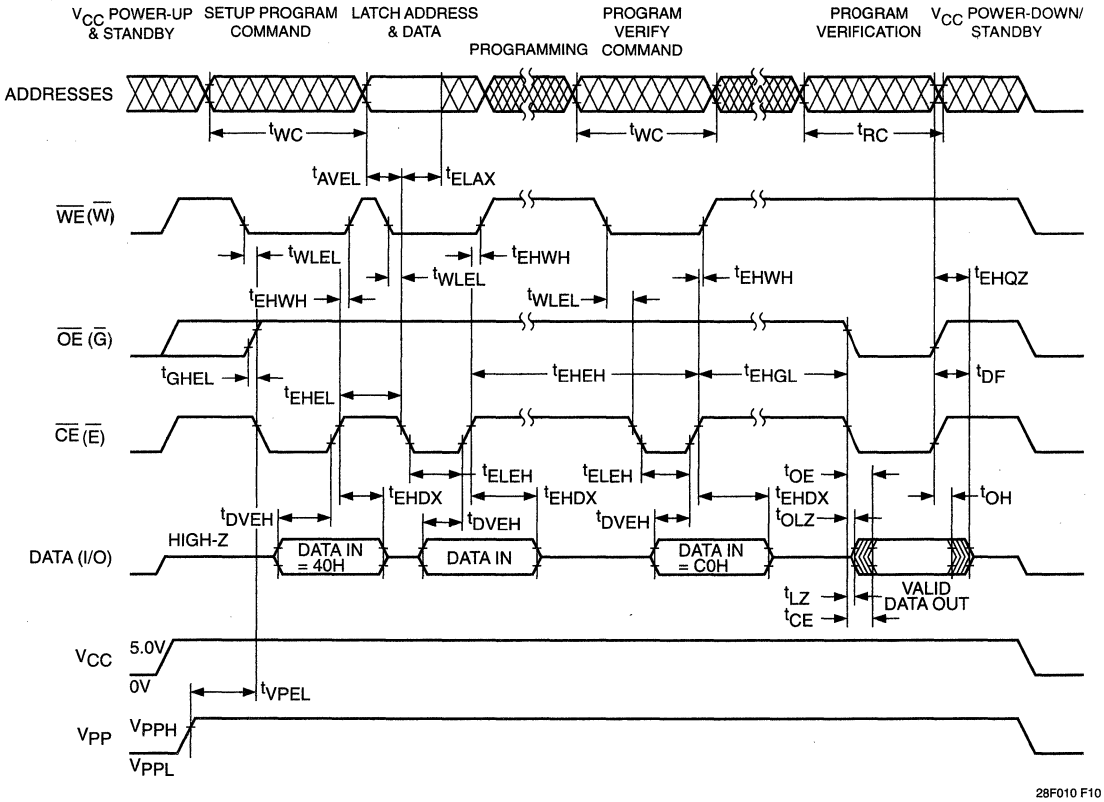
POWER UP/DOWN PROTECTION

The CAT28F010 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F010 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

Figure 8. Alternate A.C. Timing for Program Operation



ALTERNATE $\overline{CE}$-CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	28F010-90		28F010-12		28F010-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		120		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{EHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	-	$\overline{WE}$ Hold Time After $\overline{CE}$	0		0		0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	40		40		40		ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$ Low	100		100		100		ns

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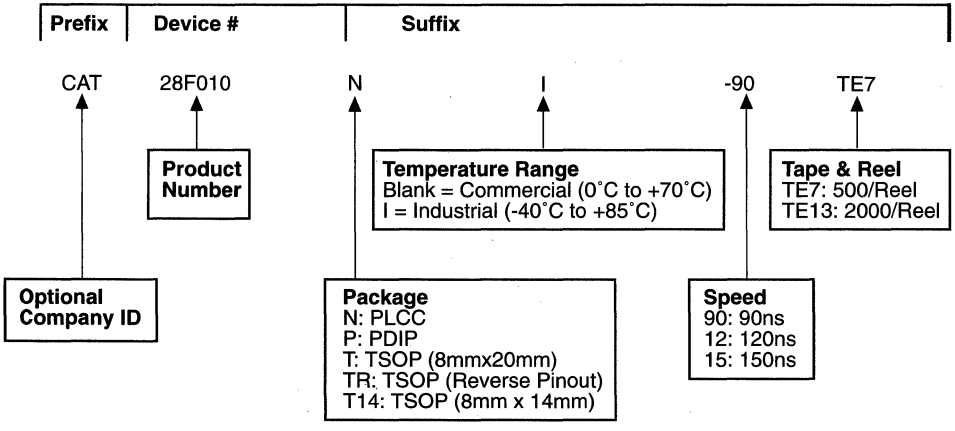
ORDERING INFORMATION



28F010 F12

Note:
(1) The device used in the above example is a CAT28F010NI-90TE7 (PLCC, Industrial Temperature, 90 ns access time, Tape & Reel).

CAT28F020

2 Megabit CMOS Flash Memory

FEATURES

- **Fast Read Access Time: 120/150/200 ns**
- **Low Power CMOS Dissipation:**
  - **Active: 30 mA max (CMOS/TTL levels)**
  - **Standby: 1 mA max (TTL levels)**
  - **Standby: 100 μA max (CMOS levels)**
- **High Speed Programming:**
  - **10 μs per byte**
  - **4 Seconds Typical Chip Program**
- **0.5 Seconds Typical Chip-Erase**
- **12.0V ±5% Programming and Erase Voltage**
- **Commercial and Industrial Temperature Ranges**
- **Stop Timer for Program/Erase**
- **On-Chip Address and Data Latches**
- **JEDEC Standard Pinouts:**
  - **32-pin DIP**
  - **32-pin PLCC**
  - **32-pin TSOP (8 x 20)**
- **100,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Electronic Signature**

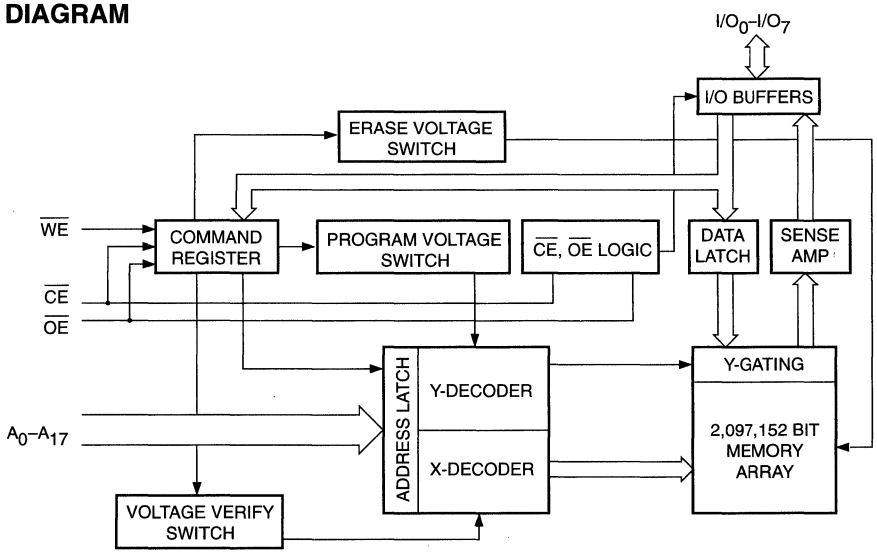
DESCRIPTION

The CAT28F020 is a high speed 256K x 8-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F020 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin plastic DIP, 32-pin PLCC or 32-pin TSOP packages.

BLOCK DIAGRAM



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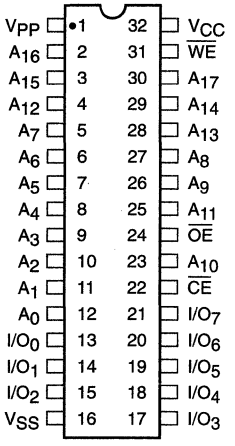
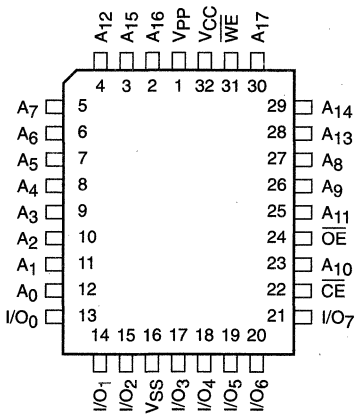
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



PLCC Package (N)



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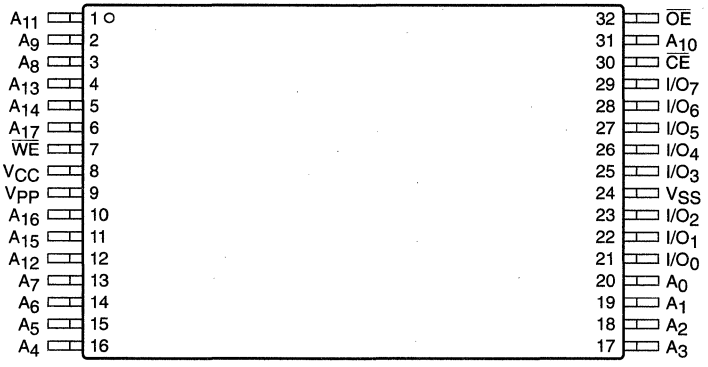
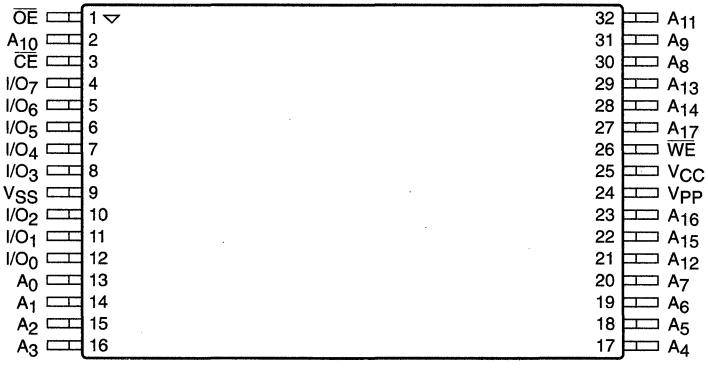
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{17}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout) (T)



TSOP Package (Reverse Pinout) (TR)



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) ..... –2.0V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±1	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current		15	mA	V_{CC} = 5.5V, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	V_{CC}*0.7	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13	V	$A_9 = V_{ID}$
I_{ID}(1)	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F020-12		28F020-15		28F020-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	120		150		200		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AVQV}	t_{ACC}	Address Access Time		120		150		200	ns
t_{GLQV}	t_{OE}	OE Access Time		50		55		60	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		30		35		35	ns
t_{EHQZ}	t_{DF}(1)(2)	$\overline{CE}$ High to Output High-Z		40		45		45	ns
t_{WHGL}(1)	-	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)

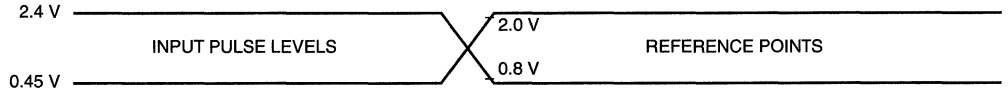

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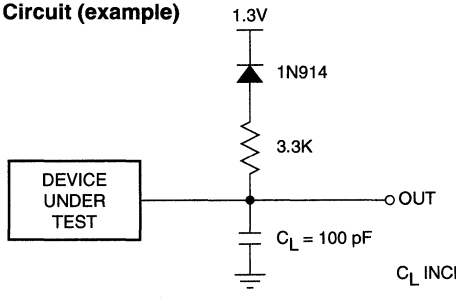
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F020-12		28F020-15		28F020-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	40		40		40		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}(2)	-	Program Pulse Width	10		10		10		µs
t_{WHWH2}(2)	-	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

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ERASE AND PROGRAMMING PERFORMANCE(1)

Parameter	28F020-12			28F020-15			28F020-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(3)(5)		0.5	10		0.5	10		0.5	10	sec
Chip Program Time(3)(4)		4	25		4	25		4	25	sec

Note:
(1) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(2) Program and Erase operations are controlled by internal stop timers.
(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(5) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(1)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	BDH	$A_0 = V_{IH}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	A_{IN}		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		BDH
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	A_{IN}	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 18 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F020 Code = 1011 1101 (BDH)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F020 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

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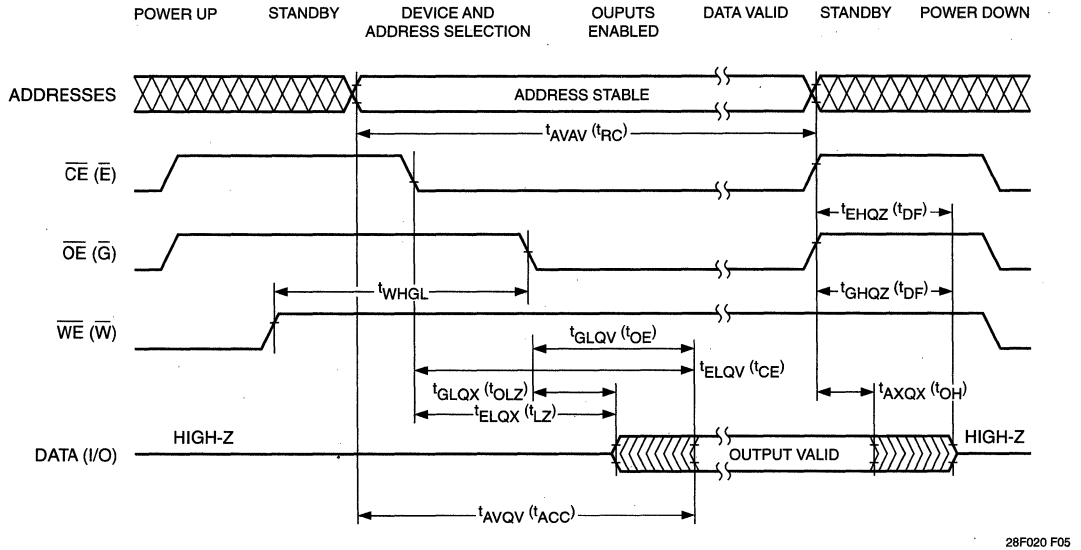
Figure 3. A.C. Timing for Read Operation



28F020 F05

WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E^2PROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F020 Code = 1011 1101 (BDH)

Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 4. A.C. Timing for Erase Operation

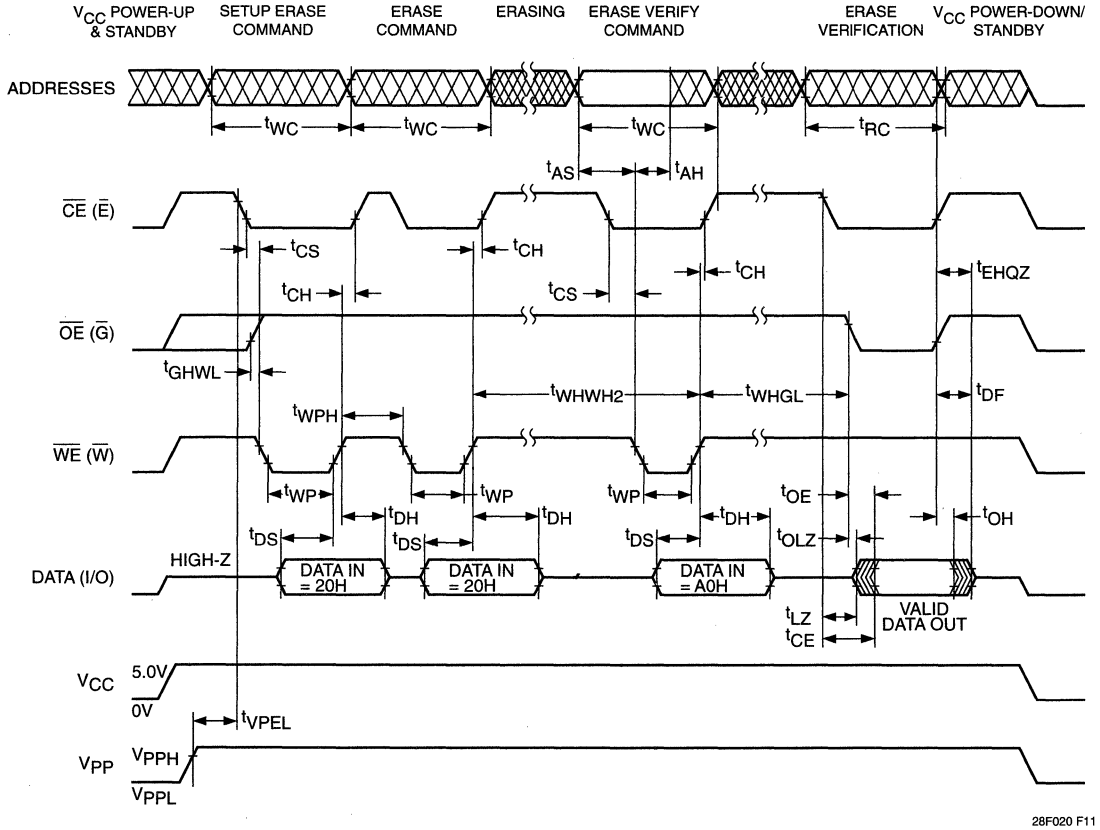
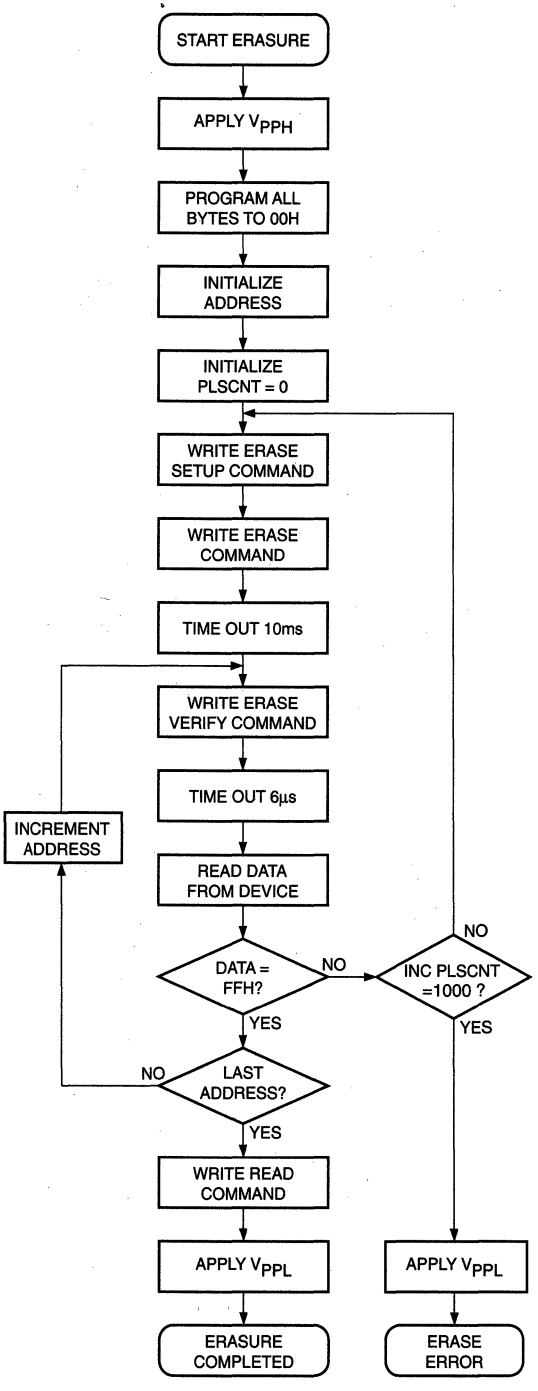


Figure 5. Chip Erase Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	DATA=20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = A0H STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation

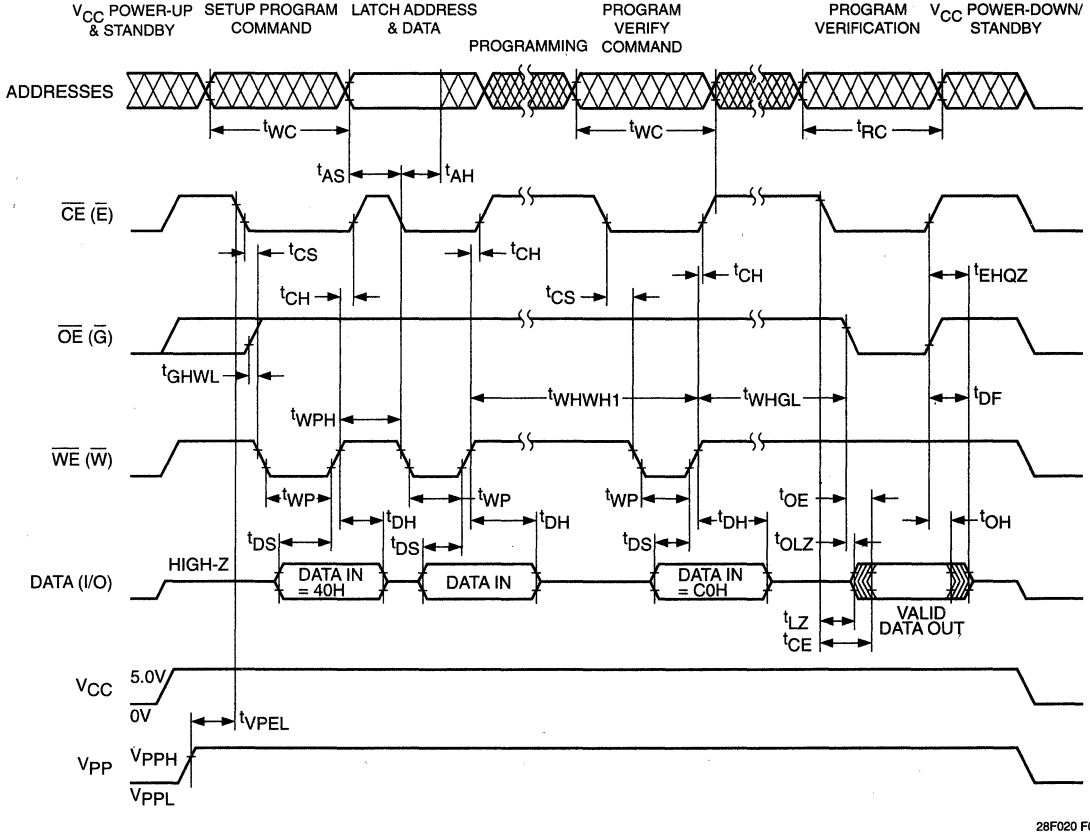

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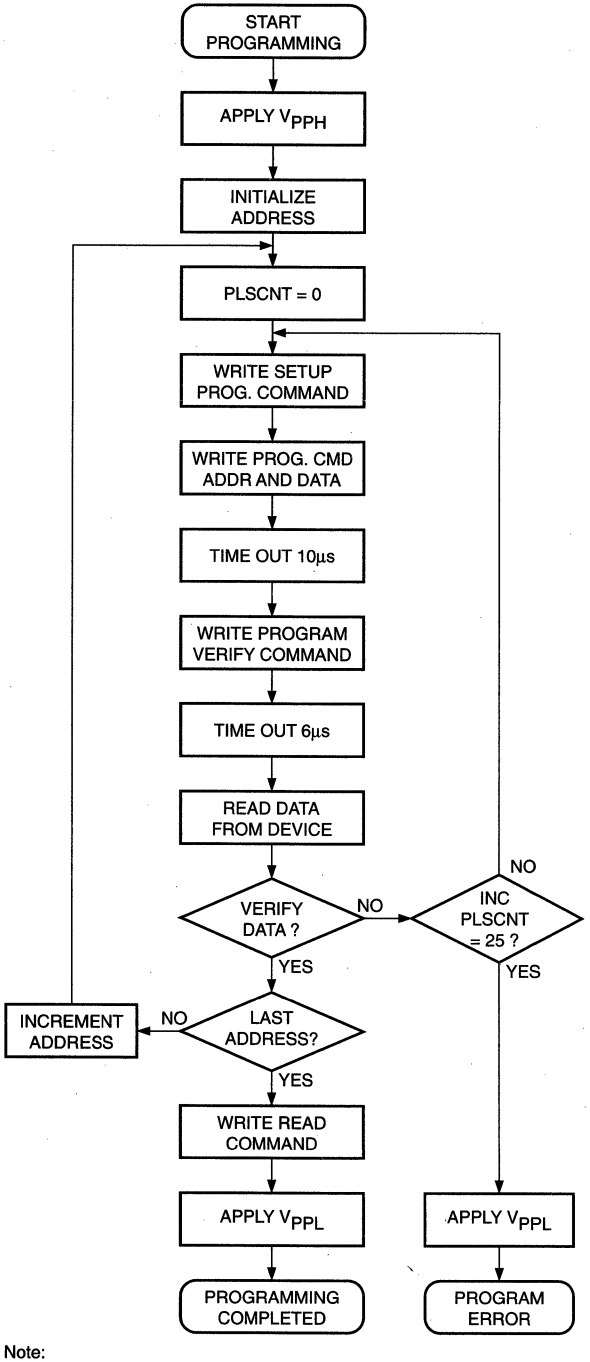
Figure 7. Programming Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

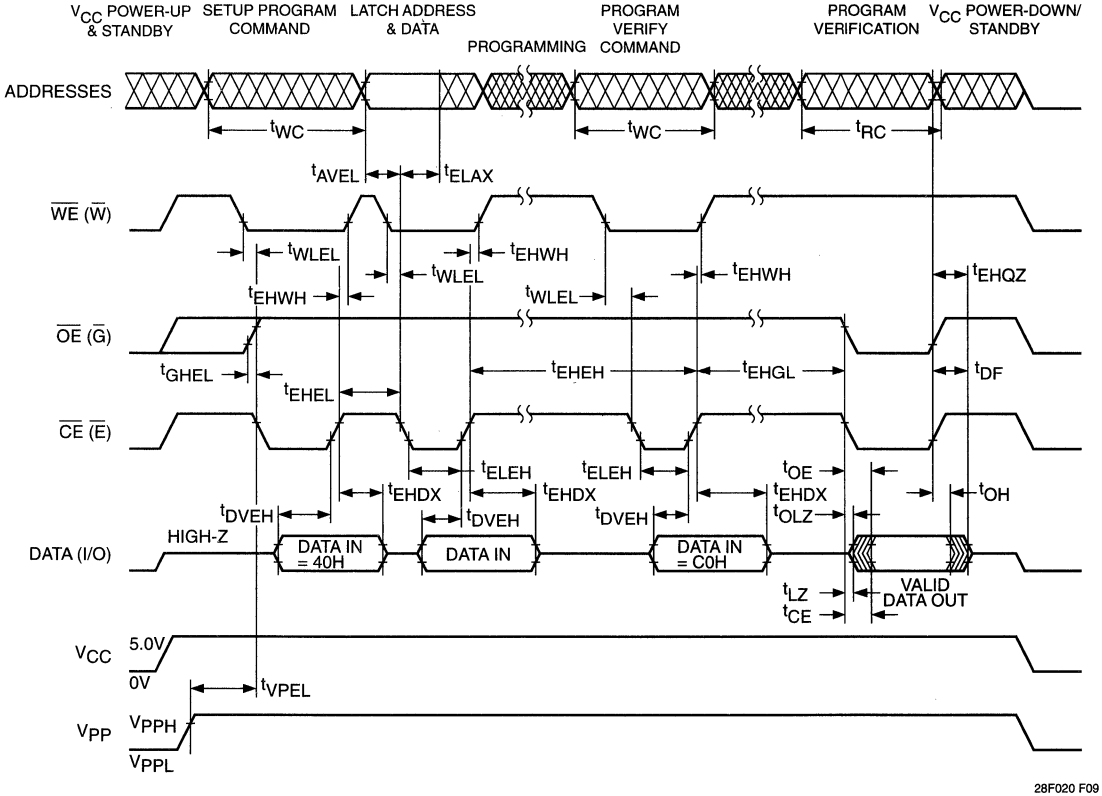
POWER UP/DOWN PROTECTION

The CAT28F020 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F020 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

Figure 8. Alternate A.C. Timing for Program Operation



ALTERNATE $\overline{CE}$-CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	28F020-12		28F020-15		28F020-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{EHGL}	—	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	—	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	—	$\overline{WE}$ Hold Time After $\overline{CE}$	0		0		0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	40		40		40		ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	—	V_{PP} Setup Time to $\overline{CE}$ Low	100		100		100		ns

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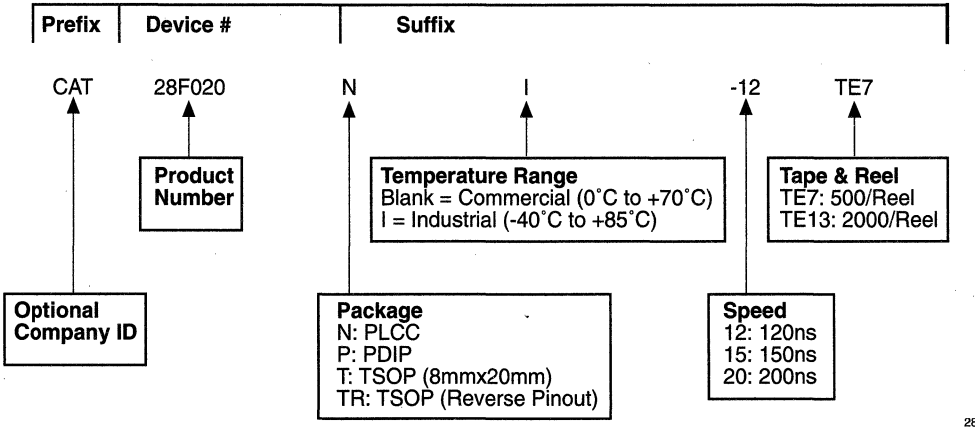
ORDERING INFORMATION



28F020 F12

Note:
(1) The device used in the above example is a CAT28F020NI-12TE7 (PLCC, Industrial Temperature, 120 ns access time, Tape & Reel).

CAT28F102

1 Megabit CMOS Flash Memory

FEATURES

- Fast Read Access Time: 90/120/150 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 μA max (CMOS levels)
- High Speed Programming:
  - –10 μs per byte
  - –1 Sec Typ Chip Program
- 0.5 Seconds Typical Chip-Erase
- 12.0V ±5% Programming and Erase Voltage
- Commercial and Industrial Temperature Ranges
- 64K x 16 Word Organization
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –40-pin DIP
  - –44-pin PLCC
  - –40-pin TSOP
- 100,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

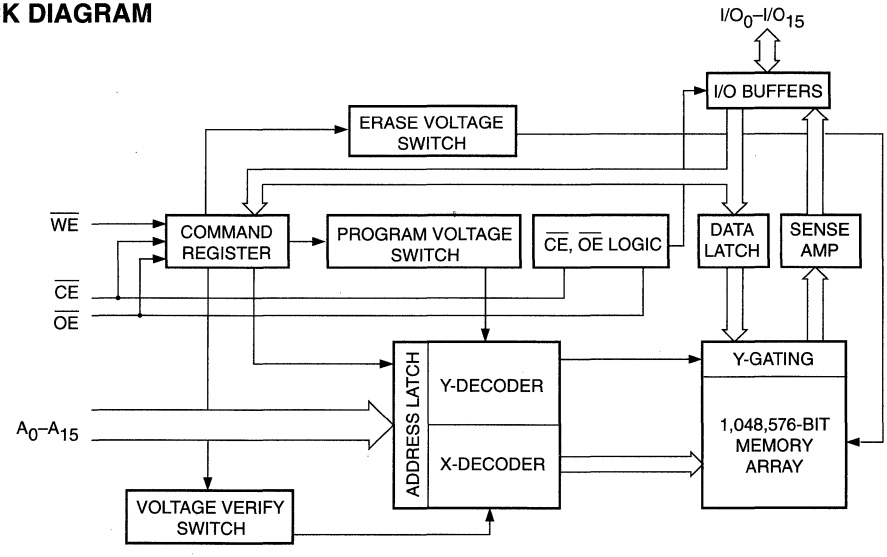
DESCRIPTION

The CAT28F102 is a high speed 64K x 16-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F102 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 40-pin DIP, 44-pin PLCC, or 40-pin TSOP packages.

BLOCK DIAGRAM



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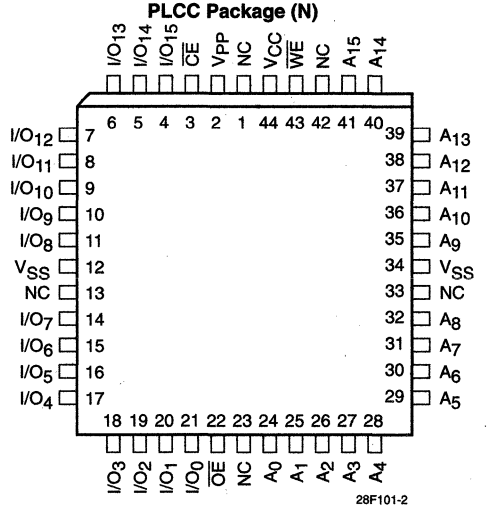
Characteristics subject to change without notice

PIN CONFIGURATION

PLCC Package (N)



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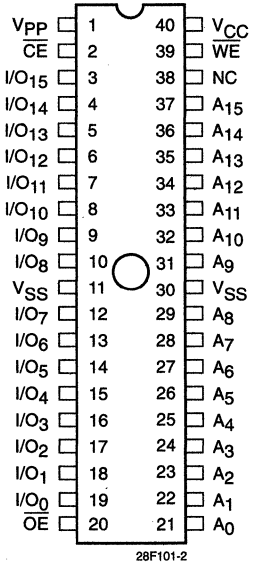
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{15}	Input	Address Inputs for memory addressing
I/O_0–I/O_{15}	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply
NC		No Connect

DIP Package (P)



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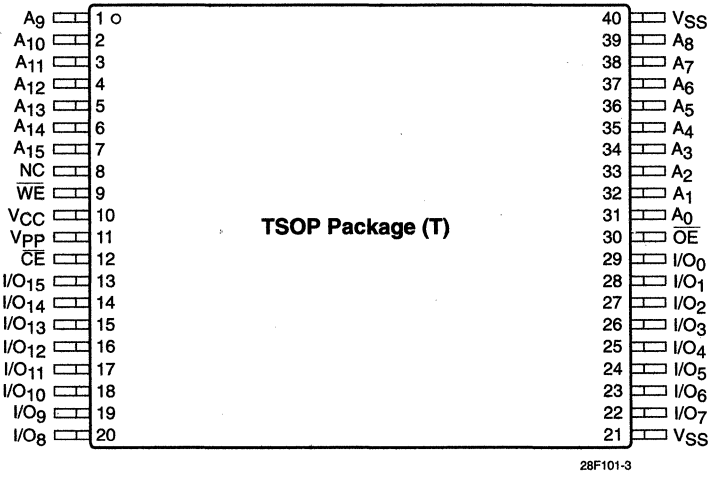

28F101-3

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –0.6V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) ..... –0.6V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

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CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±1	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		50	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current		30	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current		30	mA	V_{CC} = 5.5V, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		100	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		50	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	V_{CC}*0.7	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}-0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}(1)	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F102-90		28F102-12		28F102-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	90		120		150		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		90		120		150	ns
t_{AVQV}	t_{ACC}	Address Access Time		90		120		150	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		45		50		55	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		20		30		35	ns
t_{EHQZ}(1)(2)	-	$\overline{CE}$ High to Output High-Z		30		40		45	ns
t_{WHGL}(1)	-	Write Recovery Time Before Read	6		6		6		µs

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Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)

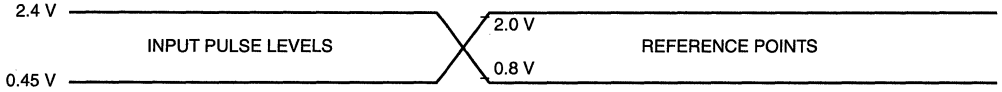

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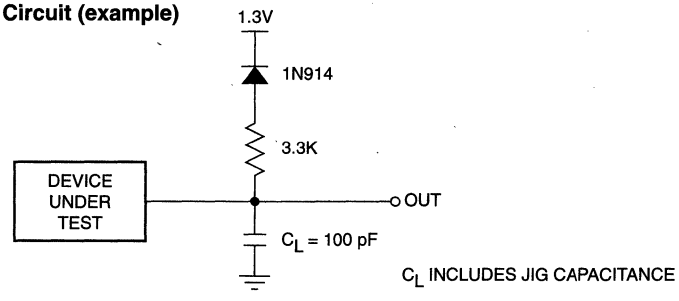
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F102-90		28F102-12		28F102-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	40		40		40		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}(2)	-	Program Pulse Width	10		10		10		µs
t_{WHWH2}(2)	-	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

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ERASE AND PROGRAMMING PERFORMANCE(1)

Parameter	28F102-90			28F102-12			28F102-15			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(3)(5)		0.5	10		0.5	10		0.5	10	sec
Chip Program Time(3)(4)		1	6.5		1	6.5		1	6.5	sec

Note:
(1) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(2) Program and Erase operations are controlled by internal stop timers.
(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(5) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(1)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	0031H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	0051H	$A_0 = V_{IH}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle
O/P Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	High-Z	During Write Cycle
Standby	V_{IH}	X	X	V_{PPH}	High-Z	During Write Cycle

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WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	XX00H	Read	A_{IN}		D_{OUT}
Read Sig. (MFG)	Write	X	XX90H	Read	0000		0031H
Read Sig. (Device)	Write	X	XX90H	Read	0001		0051H
Erase	Write	X	XX20H	Write	X	XX20H	
Erase Verify	Write	A_{IN}	XXA0H	Read	X		D_{OUT}
Program	Write	X	XX40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	XXC0H	Read	X		D_{OUT}
Reset	Write	X	XXFFH	Write	X	XXFFH	

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_{15}:

CATALYST Code = 0000 0000 0011 0001 (0031H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_{15}.

28F102 Code = 0000 0000 0101 0001 (0051H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F102 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

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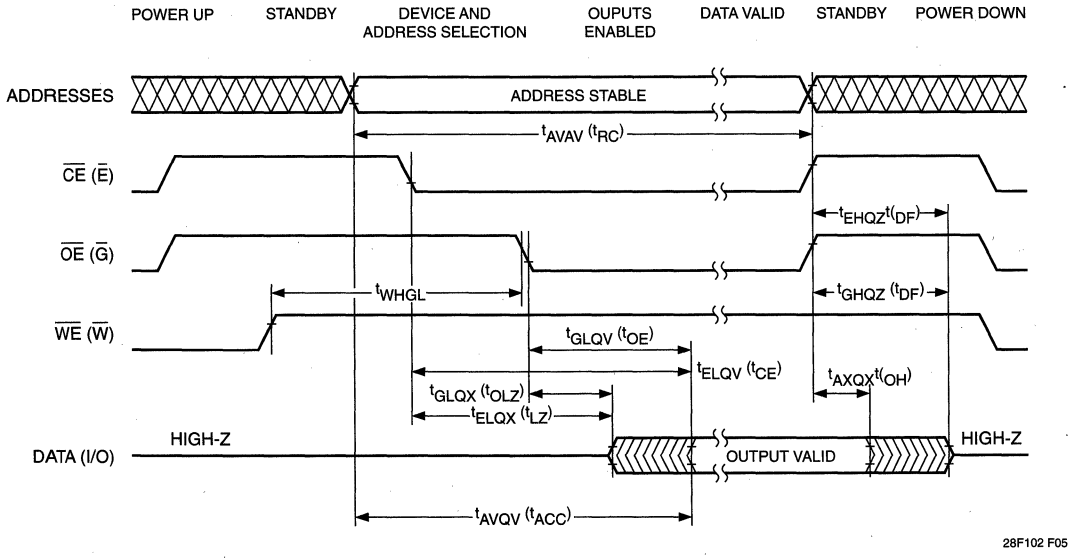
Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with XX00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E^2PROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code XX90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 0000 0000 0011 0001 (0031H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F102 Code = 0000 0000 0101 0001 (0051H)

Erase Mode

During the first Write cycle, the command XX20H is written into the command register. In order to commence the erase operation, the identical command of XX20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (XXA0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 4. A.C. Timing for Erase Operation

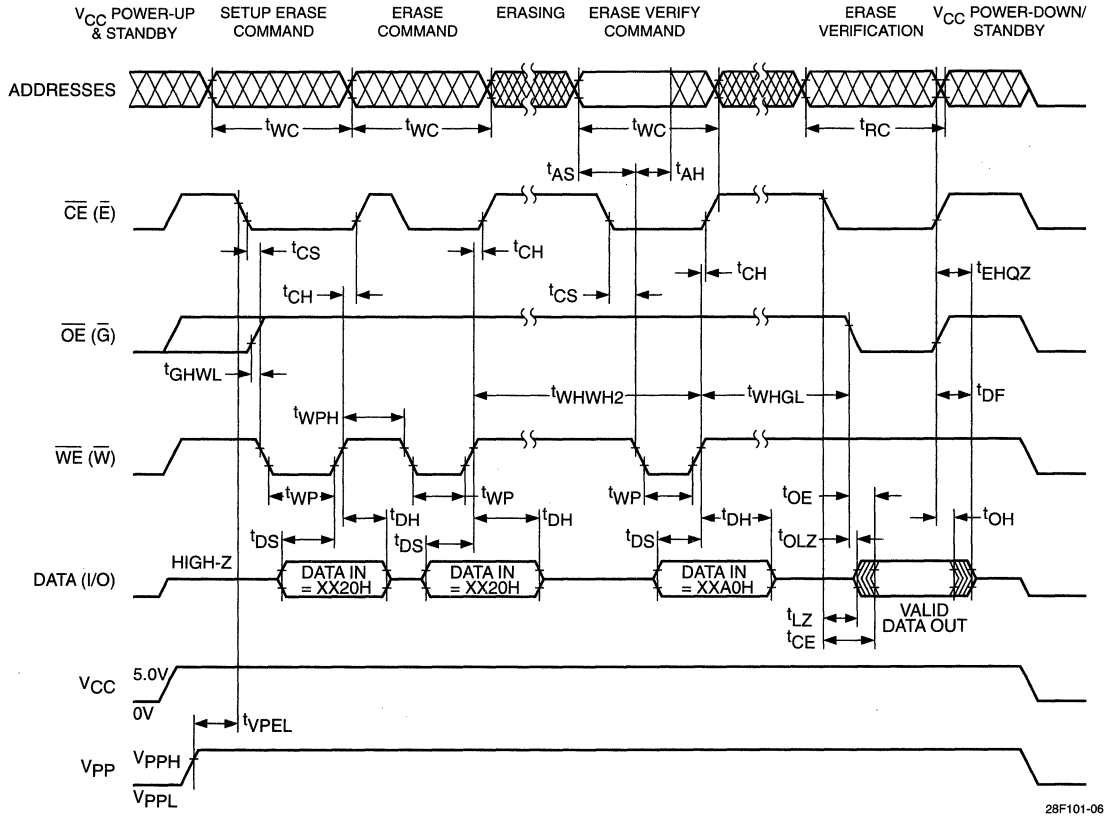
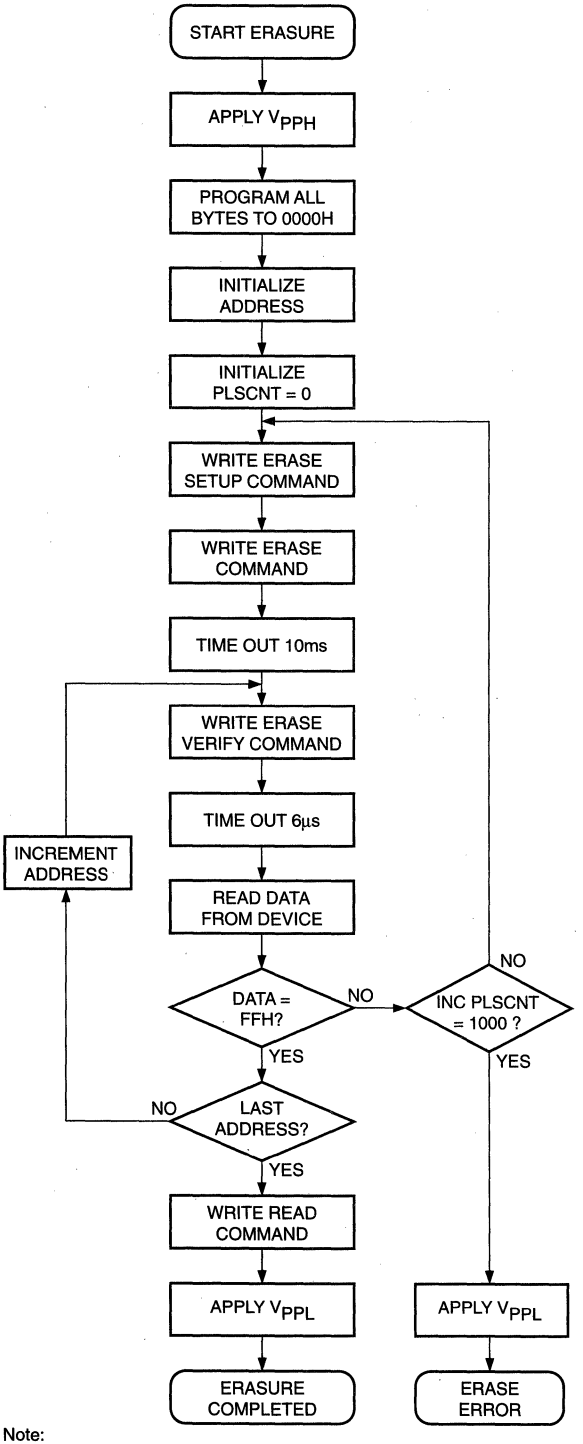


Figure 5. Chip Erase Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	DATA = XX20H
WRITE	ERASE	DATA = XX20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = XXA0H STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 0000H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

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Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command XX40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing XXC0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation

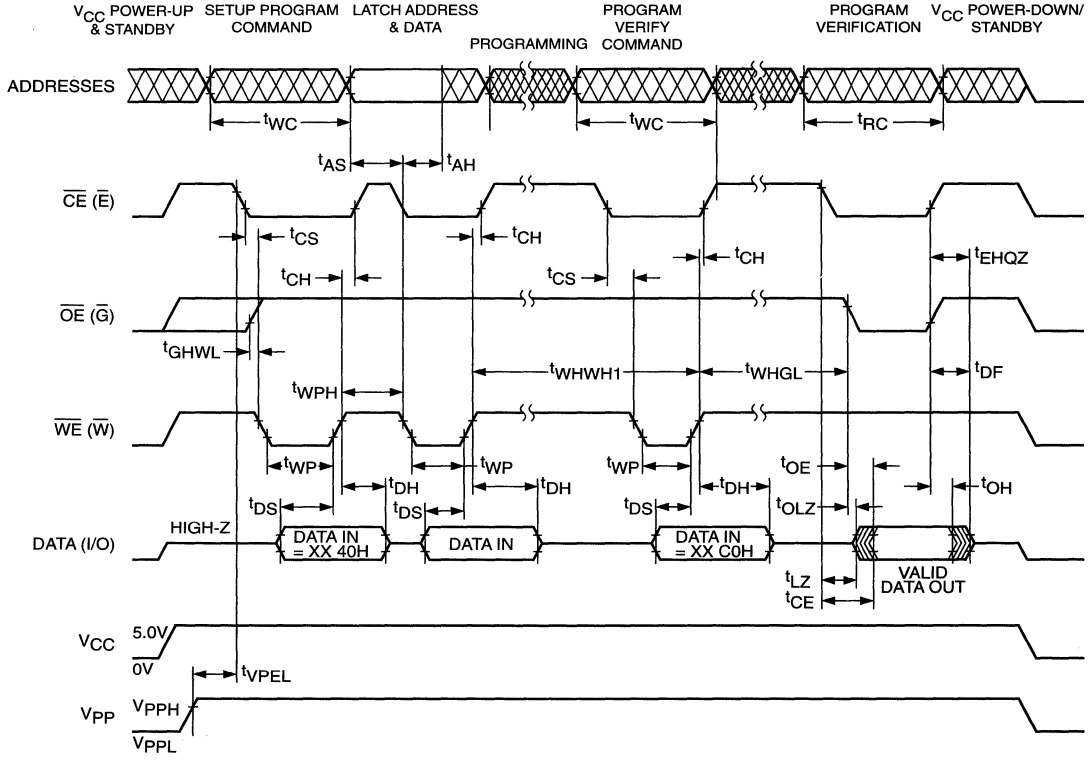

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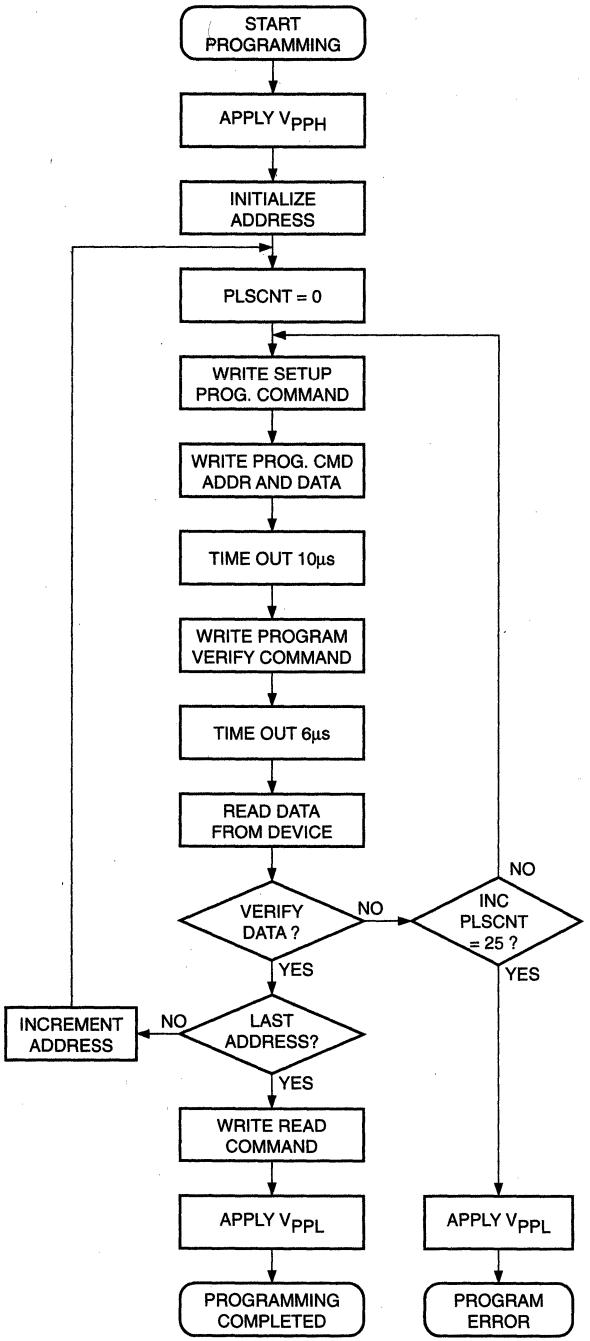
Figure 7. Programming Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = XX40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = XXC0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = XX00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with XXFFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

DATA PROTECTION

1. Power Supply Voltage

When the power supply voltage (V_{CC}) is less than 2.5V, the device ignores $\overline{WE}$ signal.

2. Write Inhibit

When $\overline{CE}$ and $\overline{OE}$ are terminated to the low level, write mode is not set.

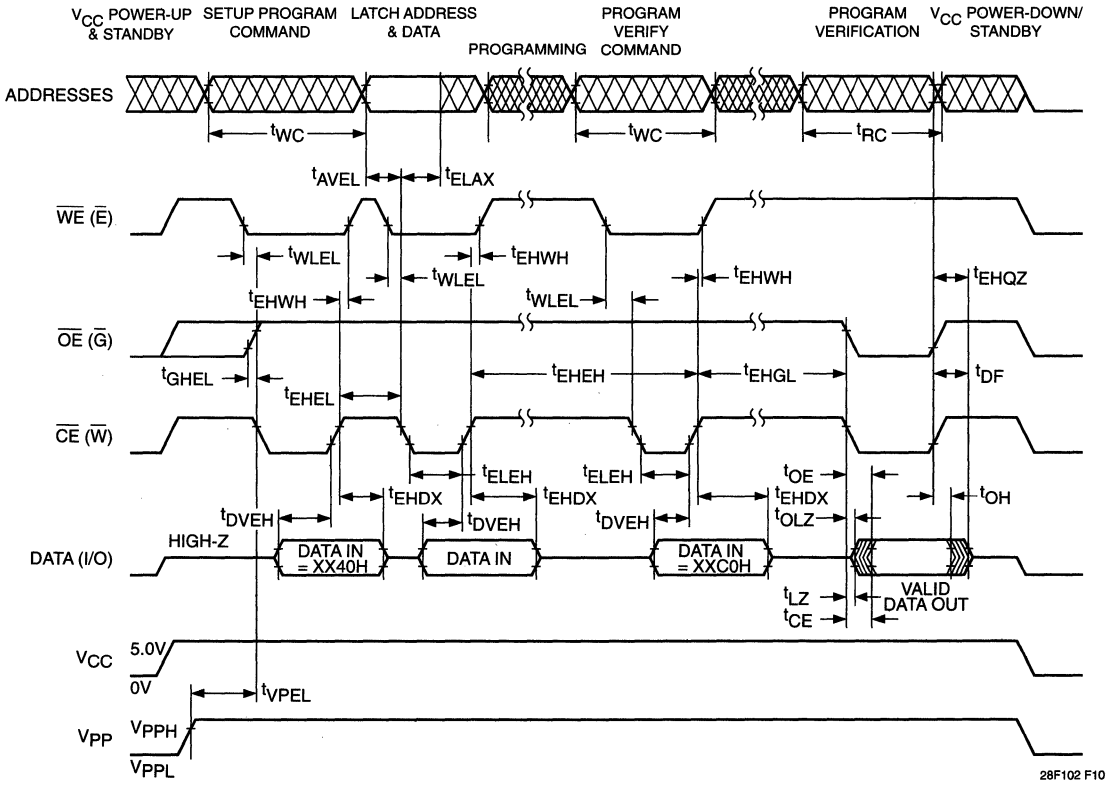
POWER UP/DOWN PROTECTION

The CAT28F102 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F102 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

Figure 8. Alternate A.C. Timing for Program Operation



ALTERNATE $\overline{CE}$-CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	28F102-90		28F102-12		28F102-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{EHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time After $\overline{CE}$	0		0		0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	40		40		40		ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$ Low	100		100		100		ns

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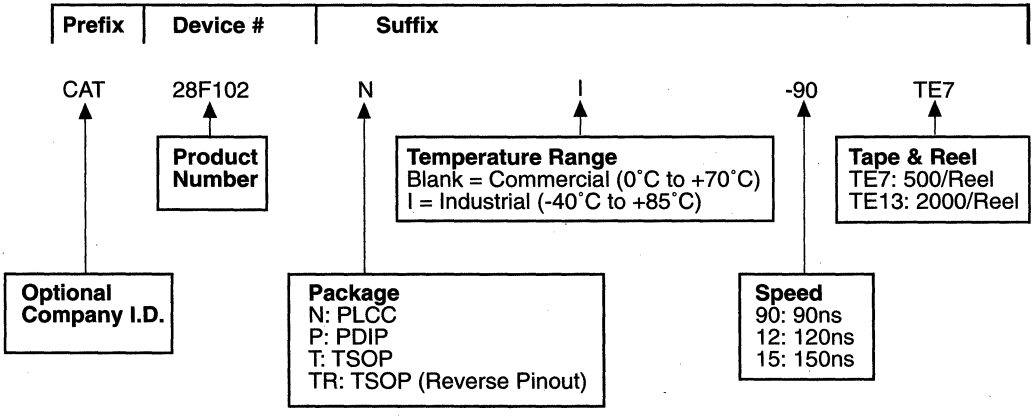
ORDERING INFORMATION



Note:
(1) The device used in the above example is a CAT28F102NI-90TE7 (PLCC, Industrial Temperature, 90 ns access time, Tape & Reel).

CAT28F202

2 Megabit CMOS Flash Memory

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 μA max (CMOS levels)
- High Speed Programming:
  - –10 μs per byte
  - –2 Sec Typ Chip Program
- 0.5 Seconds Typical Chip-Erase
- 12.0V ± 5% Programming and Erase Voltage
- Commercial and Industrial Temperature Ranges
- 128K x 16 Word Organization
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –40-pin DIP
  - –44-pin PLCC
  - –40-pin TSOP
- 100,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

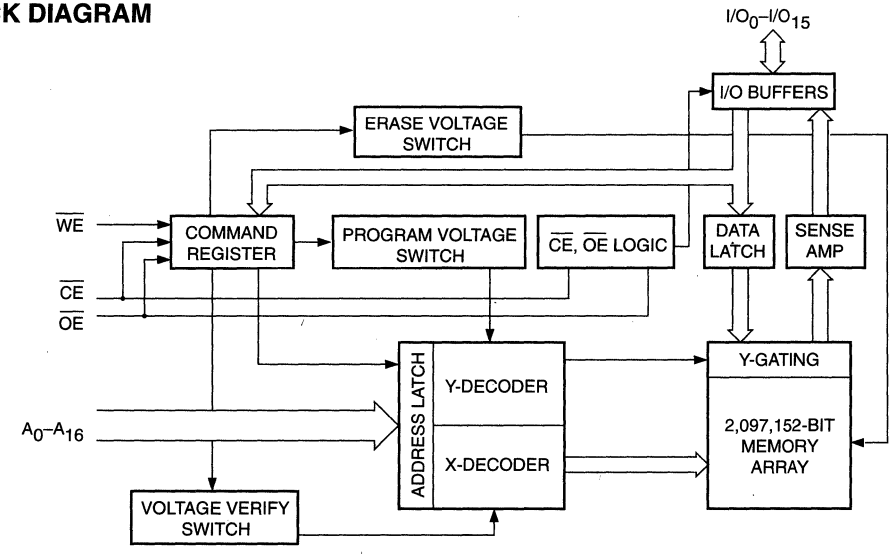
DESCRIPTION

The CAT28F202 is a high speed 128K x 16-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F202 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 40-pin DIP, 44-pin PLCC, or 40-pin TSOP packages.

BLOCK DIAGRAM



28F202-1

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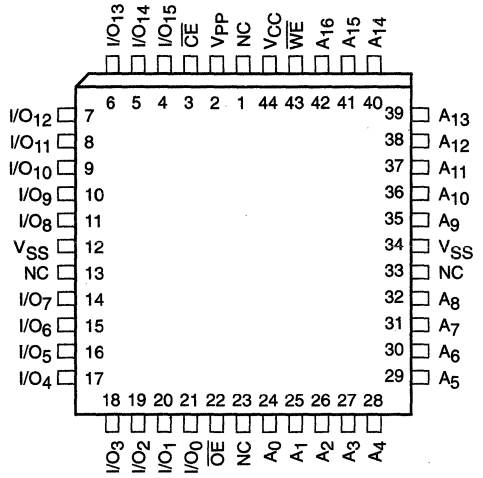
Characteristics subject to change without notice

PIN CONFIGURATION

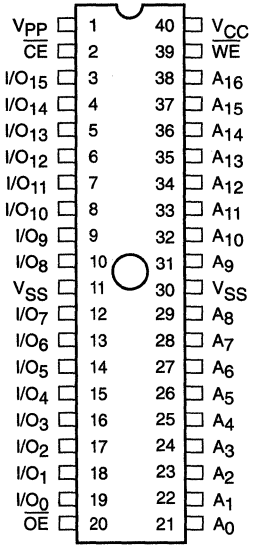
PLCC Package (N)

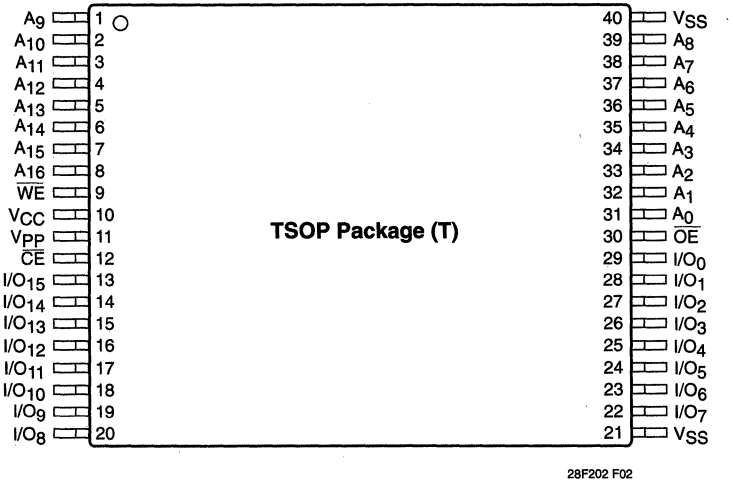


PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{16}	Input	Address Inputs for memory addressing
I/O_0–I/O_{15}	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply
NC		No Connect

DIP Package (P)





28F202 F02

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –0.6V to +V_{CC} + 2.0V

Voltage on Pin A_9 with Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground during Program/Erase(1) ..... –0.6V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±1	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		50	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current		30	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current		30	mA	V_{CC} = 5.5V, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		100	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		50	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	V_{CC}*0.7	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13	V	$A_9 = V_{ID}$
I_{ID}(1)	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F202-12		28F202-15		28F202-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	120		150		200		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AVQV}	t_{ACC}	Address Access Time		120		150		200	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		50		55		55	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		30		35		35	ns
t_{EHQZ}(1)(2)	-	$\overline{CE}$ High to Output High-Z		40		45		45	ns
t_{WHGL}(1)	-	Write Recovery Time Before Read	6		6		6		µs

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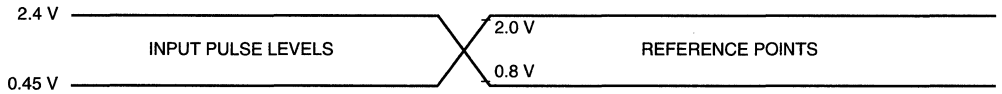
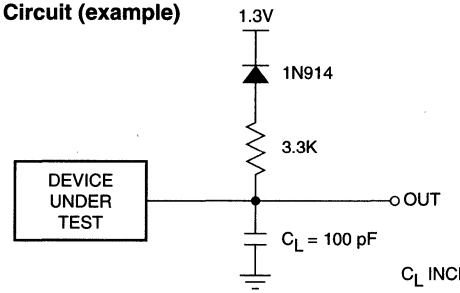
Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)



5108 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



5108 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F202-12		28F202-15		28F202-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	40		40		40		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}(2)	-	Program Pulse Width	10		10		10		µs
t_{WHWH2}(2)	-	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

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ERASE AND PROGRAMMING PERFORMANCE(1)

Parameter	28F202-12			28F202-15			28F202-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(3)(5)		0.5	10		0.5	10		0.5	10	sec
Chip Program Time(3)(4)		2	12.5		2	12.5		2	12.5	sec

Note:
(1) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(2) Program and Erase operations are controlled by internal stop timers.
(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(5) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(1)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	0031H	$A_0 = V_{IL}$, A_9 = 12V
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	0051H	$A_0 = V_{IH}$, A_9 = 12V
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle
O/P Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	High-Z	During Write Cycle
Standby	V_{IH}	X	X	V_{PPH}	High-Z	During Write Cycle

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WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	XX00H	Read	A_{IN}		D_{OUT}
Read Sig. (MFG)	Write	X	XX90H	Read	0000		0031H
Read Sig. (Device)	Write	X	XX90H	Read	0001		0051H
Erase	Write	X	XX20H	Write	X	XX20H	
Erase Verify	Write	A_{IN}	XXA0H	Read	X		D_{OUT}
Program	Write	X	XX40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	XXC0H	Read	X		D_{OUT}
Reset	Write	X	XXFFH	Write	X	XXFFH	

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_{15}:

CATALYST Code = 0000 0000 0011 0001 (0031H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_{15}.

28F202 Code = 0000 0000 0101 0010 (0052H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F202 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

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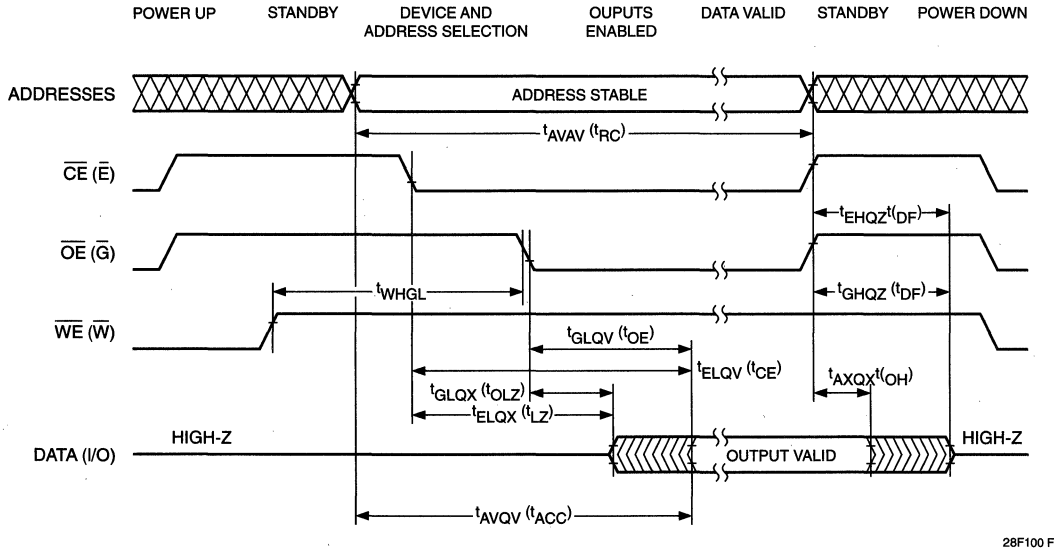
Figure 3. A.C. Timing for Read Operation



28F100 F05

WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with XX00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E²PROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code XX90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 0000 0000 0011 0001 (0031H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F202 Code = 0000 0000 0101 0010 (0052H)

Erase Mode

During the first Write cycle, the command XX20H is written into the command register. In order to commence the erase operation, the identical command of XX20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (XXA0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 4. A.C. Timing for Erase Operation

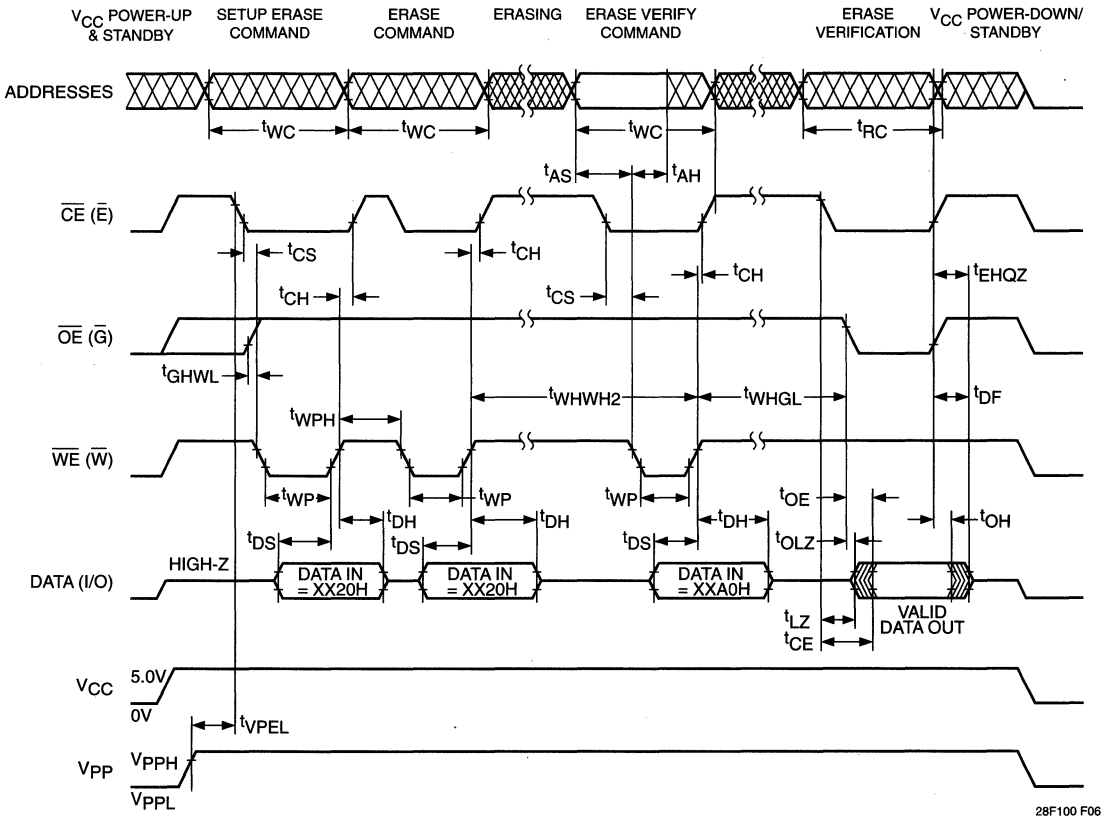
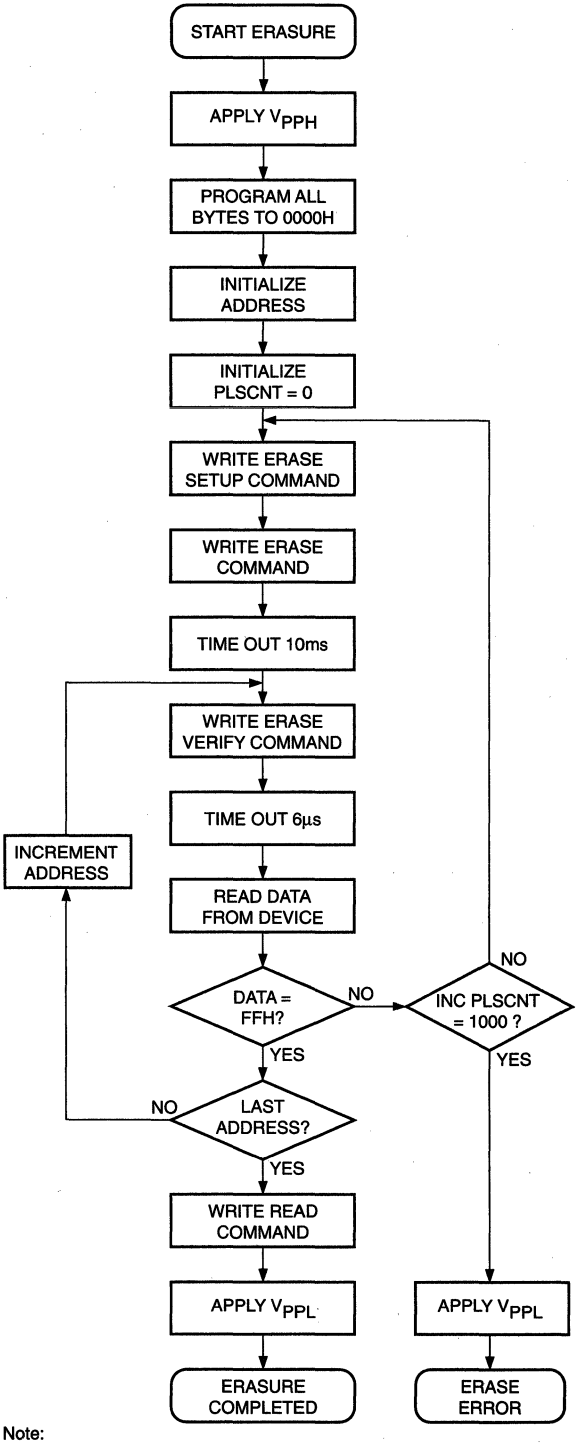


Figure 5. Chip Erase Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	DATA = XX20H
WRITE	ERASE	DATA = XX20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = XXA0H STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 0000H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

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Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

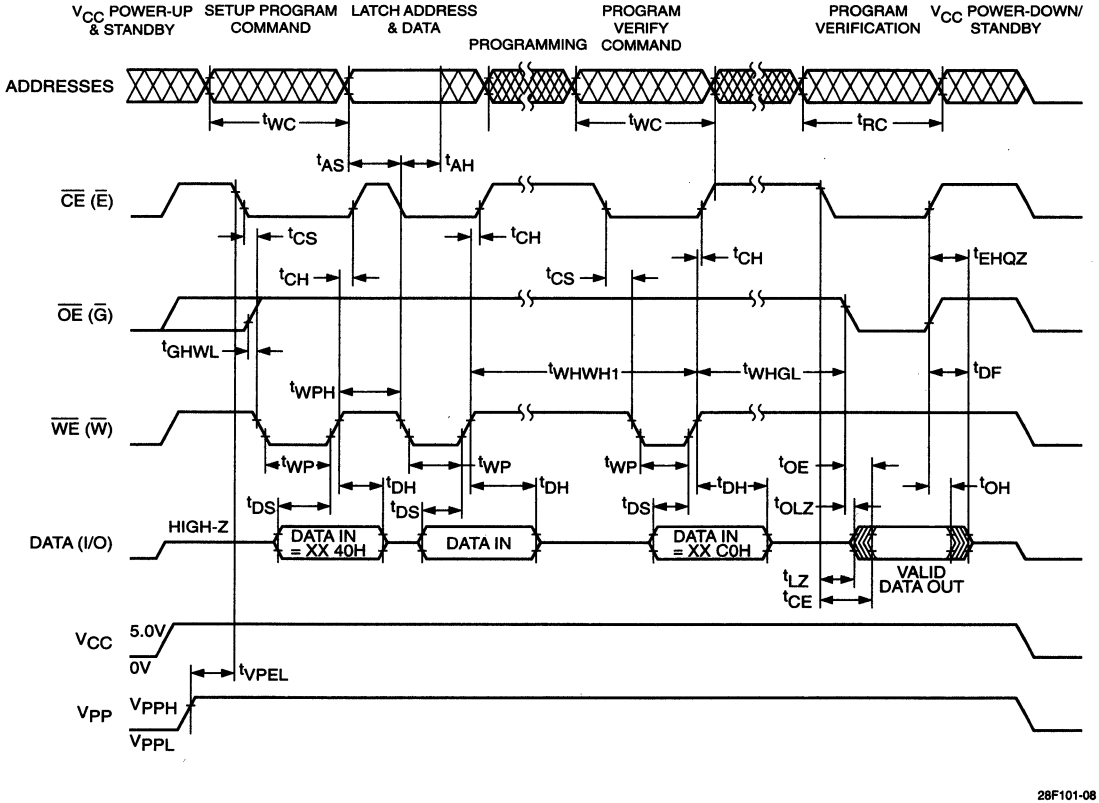
Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command XX40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Program-Verify Mode

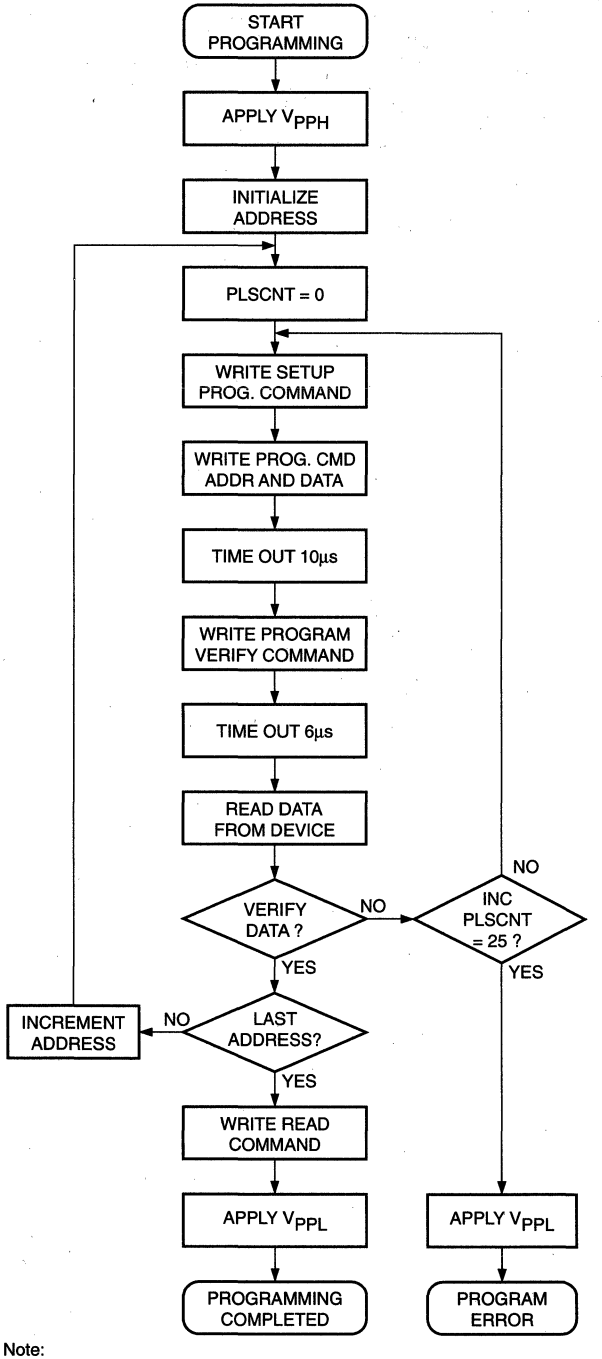
A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing XXC0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation



28F101-08

Figure 7. Programming Algorithm(1)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = XX40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = XXC0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = XX00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with XXFFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

POWER UP/DOWN PROTECTION

The CAT28F202 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F202 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

DATA PROTECTION

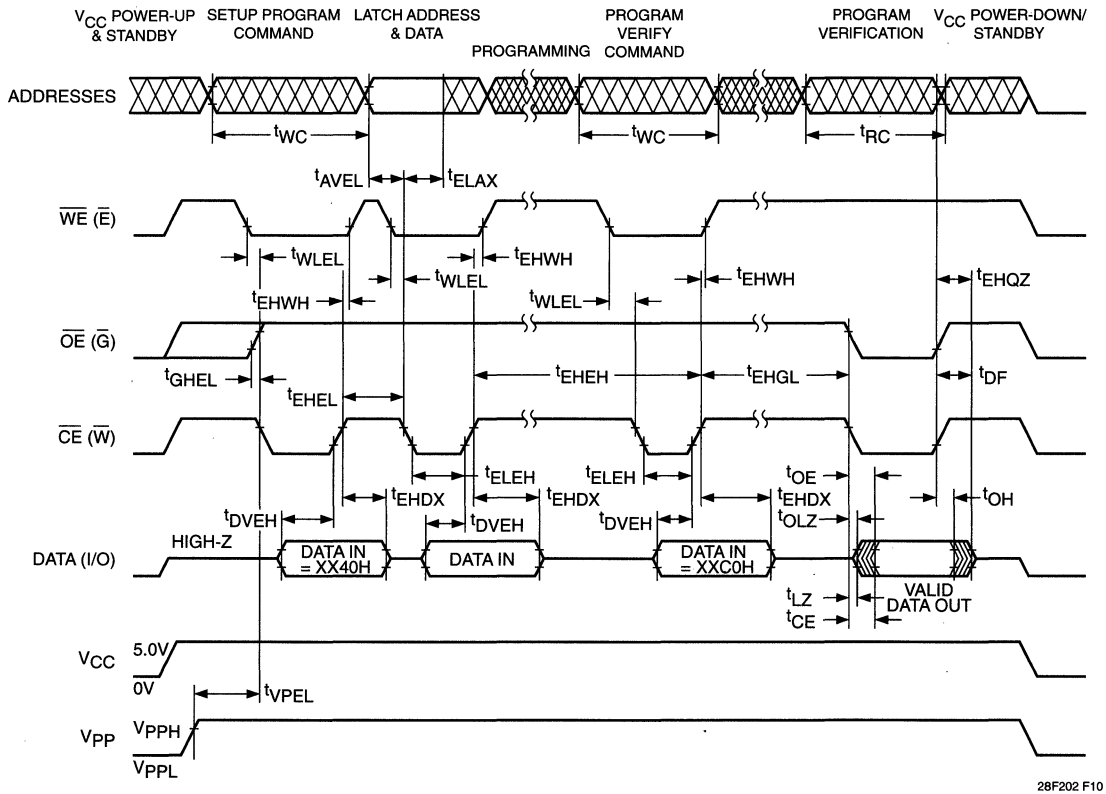
1. Power Supply Voltage

When the power supply voltage (V_{CC}) is less than 2.5V, the device ignores $\overline{WE}$ signal.

2. Write Inhibit

When $\overline{CE}$ and $\overline{OE}$ are terminated to the low level, Write Mode is not set.

Figure 8. Alternate A.C. Timing for Program Operation



ALTERNATE $\overline{CE}$-CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	28F202-12		28F202-15		28F202-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup Time	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time	10		10		10		ns
t_{EHGL}	-	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	-	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time After $\overline{CE}$	0		0		0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	40		40		40		ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	-	V_{PP} Setup Time to $\overline{CE}$ Low	100		100		100		ns

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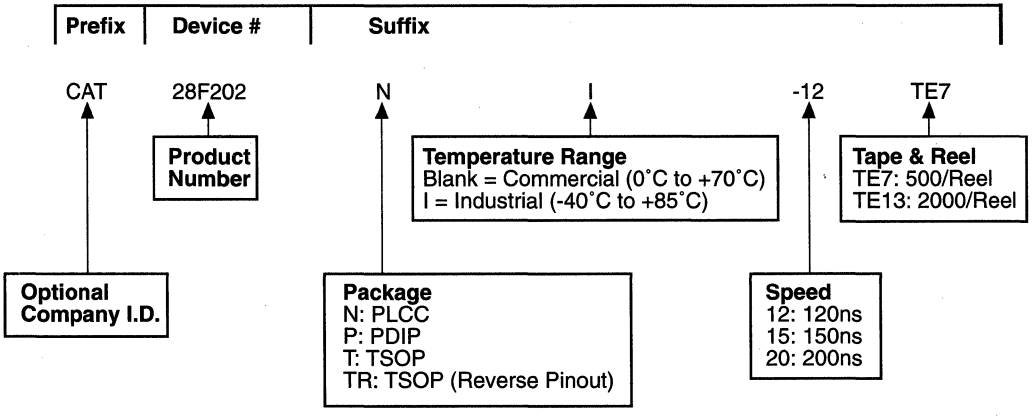
ORDERING INFORMATION



Note:
(1) The device used in the above example is a CAT28F202NI-12TE7 (PLCC, Industrial Temperature, 120 ns access time, Tape & Reel).

CAT28F001

1 Megabit CMOS Boot Block Flash Memory

FEATURES

- Fast Read Access Time: 90/120/150 ns
- On-Chip Address, Data Latches, Programming and Erase Algorithms
- Blocked Architecture:
  - One 8 KB Boot Block w/ Lock Out
  - Two 4 KB Parameter Blocks
  - One 112 KB Main Block
- Low Power CMOS Operation
- 12.0V ± 5% Programming and Erase Voltage
- Embedded Algorithms Program & Erase
- High Speed Programming
- Deep Powerdown Mode
  - 0.05 μA I_{CC} Typical
  - 0.8 μA I_{PP} Typical
- Electronic Signature
- 100,000 Program/Erase Cycles and 10 Year Data Retention
- JEDEC Standard Pinouts:
  - 32 pin DIP
  - 32 pin PLCC
  - 32 pin TSOP
- Commercial and Industrial Temperature Ranges

DESCRIPTION

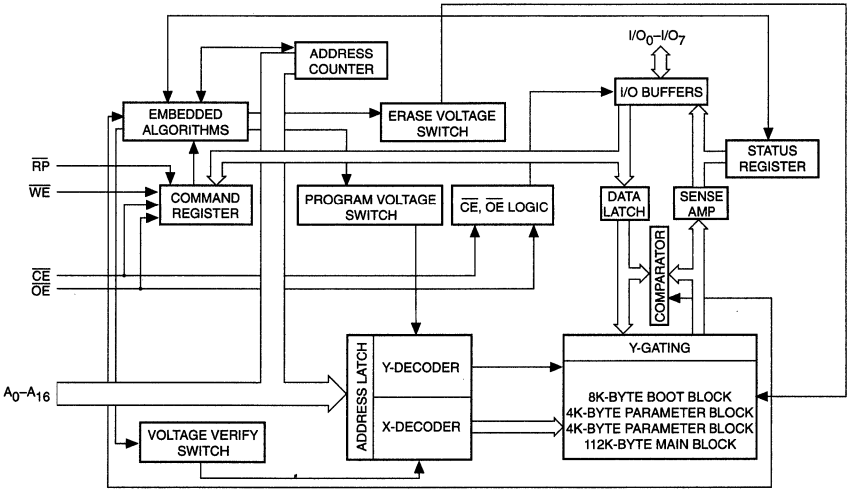
The CAT28F001 is a high speed 128K X 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after sale code updates.

The CAT28F001 has a blocked architecture with one 8 KB Boot Block, two 4 KB Parameter Blocks and one 112 KB Main Block. The Boot Block section optionally can be at the top or bottom of the memory map and includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to other locations of CAT28F001.

The CAT28F001 is designed with a signature mode which allows the user to identify the IC manufacturer and device type. The CAT28F001 is also designed with on-Chip Address Latches, Data Latches, Programming and Erase Algorithms.

The CAT28F001 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin PDIP, PLCC or TSOP packages.

BLOCK DIAGRAM



28F001 F01

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CAT28F002

2 Megabit CMOS Boot Block Flash Memory

FEATURES

- **Fast Read Access Time: 120/150/200 ns**
- **On-Chip Address, Data Latches, Programming and Erase Algorithms**
- **Blocked Architecture:**
  - **— One 16 KB Boot Block**
  - **— Two 8 KB Parameter Blocks**
  - **— One 96 KB Main Block**
  - **— One 128 KB Main Block**
- **Low Power CMOS Operation**
- **12.0V ± 5% Programming and Erase Voltage**
- **Electronic Signature**
- **100,000 Program/Erase Cycles and 10 Year Data Retention**
- **JEDEC Standard Pinouts:**
  - **— 32-pin DIP**
  - **— 32-pin PLCC**
  - **— 32-pin TSOP**
  - **— 40-pin TSOP, 44-pin PSOP**
- **High Speed Programming**
- **Commercial and Industrial Temperature Ranges**

DESCRIPTION

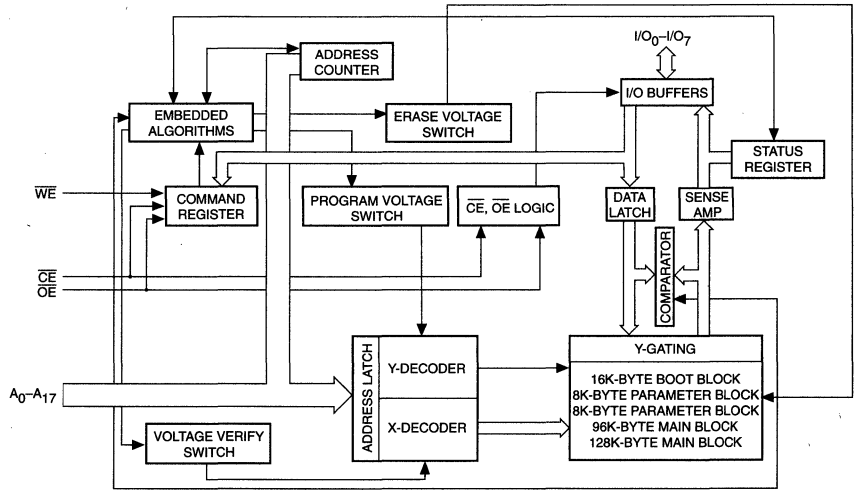
The CAT28F002 is a high speed 256K X 8-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after sale code updates.

The CAT28F002 has a blocked architecture with one 16 KB Boot Block, two 8 KB Parameter Blocks, one 96 KB Main Block and one 128 KB Main Block. The Boot Block section optionally can be at the top or bottom of the memory map. The Boot Block section includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to other locations of CAT28F002.

The CAT28F002 is designed with a signature mode which allows the user to identify the IC manufacturer and device type. The CAT28F002 is also designed with on-Chip Address Latches, Data Latches, Programming and Erase Algorithms.

The CAT28F002 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin PDIP, PLCC or TSOP packages, 40-pin TSOP packages and 44-pin PSOP packages.

BLOCK DIAGRAM



28F002 F01

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NVRAMs 6
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CAT28LV64 ..... 64K-Bit 8-51

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CAT28C16A

16K-Bit CMOS E²PROM

FEATURES

- **Fast Read Access Times: 200 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 25 mA Max.**
  - **–Standby: 100 µA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Write Cycle Time: 10ms Max**
- **End of Write Detection: $\overline{\text{DATA}}$ Polling**
- **Hardware Write Protection**
- **CMOS and TTL Compatible I/O**
- **10,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Commercial and Industrial Temperature Ranges**

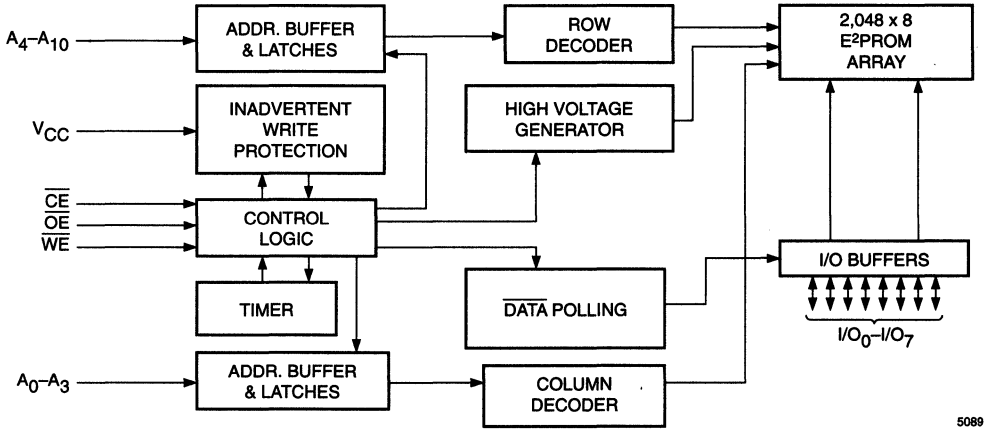
DESCRIPTION

The CAT28C16A is a fast, low power, 5V-only CMOS E²PROM organized as 2K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C16A features hardware write protection.

The CAT28C16A is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 24-pin DIP and SOIC or 32-pin PLCC packages.

8

BLOCK DIAGRAM



5089 FHD F02

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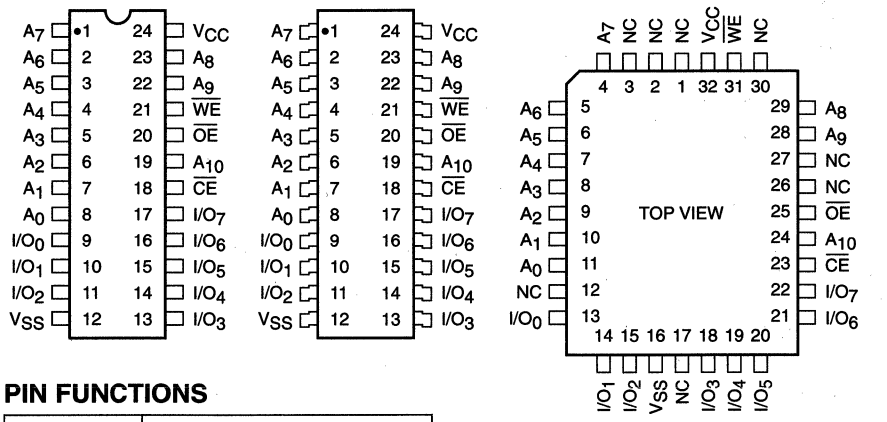
PIN CONFIGURATION

DIP Package (P) SOIC Package (J,K) PLCC Package (N)



5089 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

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MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			35	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

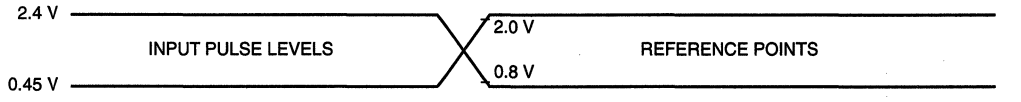
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

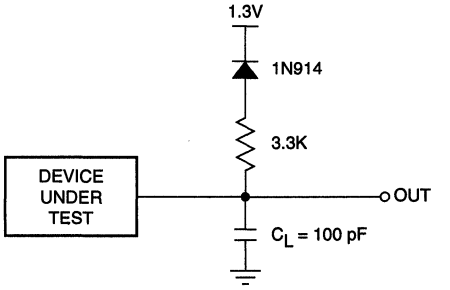
Symbol	Parameter	28C16A-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	200		ns
t_{CE}	$\overline{CE}$ Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	$\overline{OE}$ Access Time		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		55	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		55	ns
t_{OH}(1)	Output Hold from Address Change	0		ns

Figure 1. A.C. Testing Input/Output Waveform(3)



5089 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5089 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C16A-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	150		ns
t_{OES}	$\overline{OE}$ Setup Time	15		ns
t_{OEH}	$\overline{OE}$ Hold Time	15		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	150		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{DL}	Data Latch Time	50		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.

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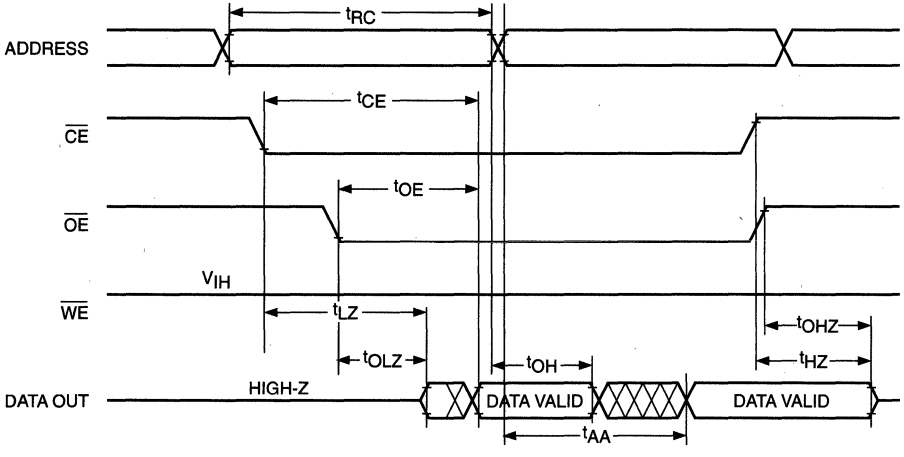
DEVICE OPERATION

Read

Data stored in the CAT28C16A is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Figure 3. Read Cycle



28C16A F05

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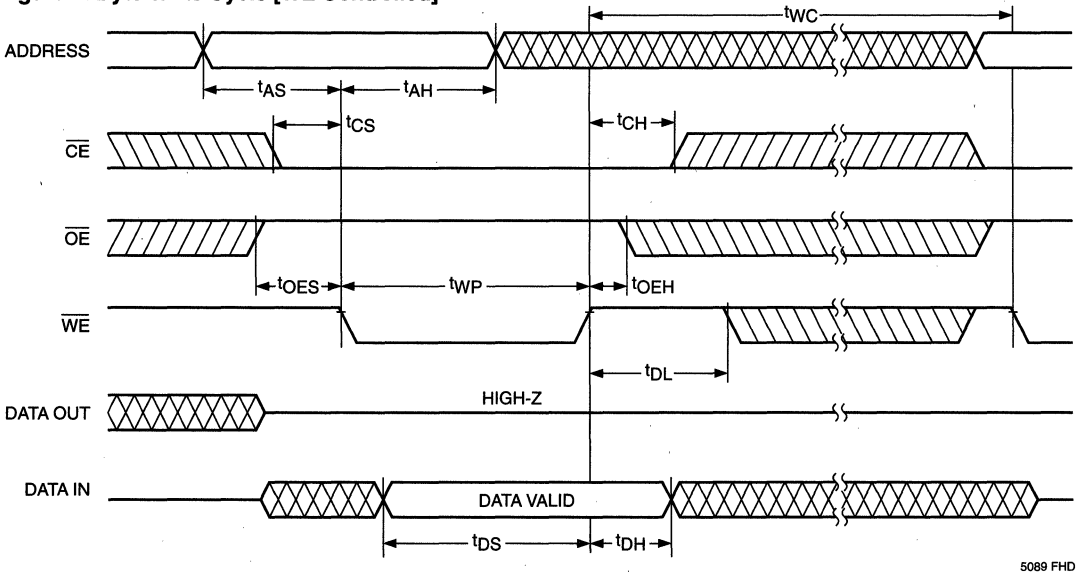
Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5089 FHD F06

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

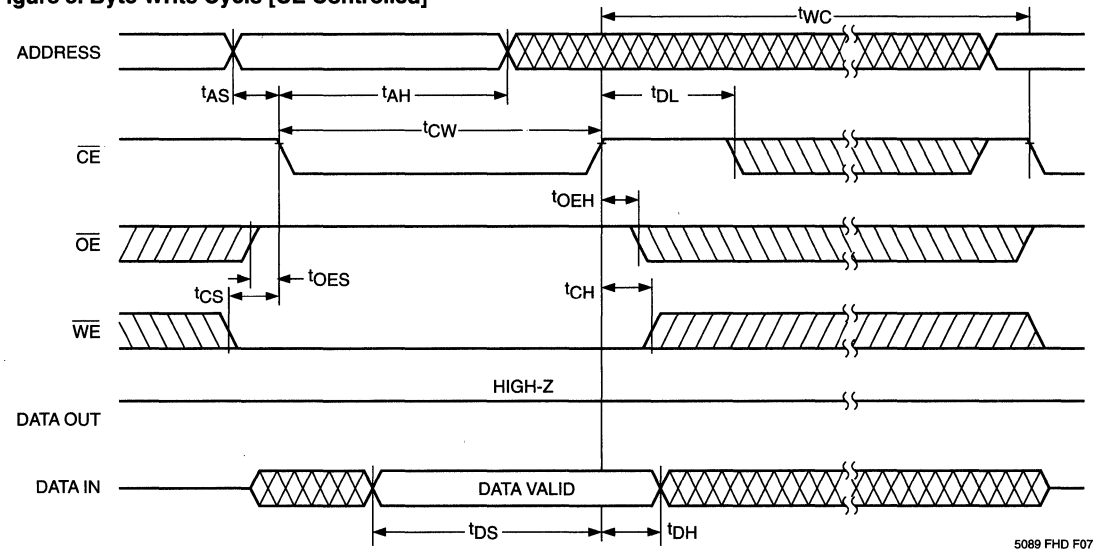
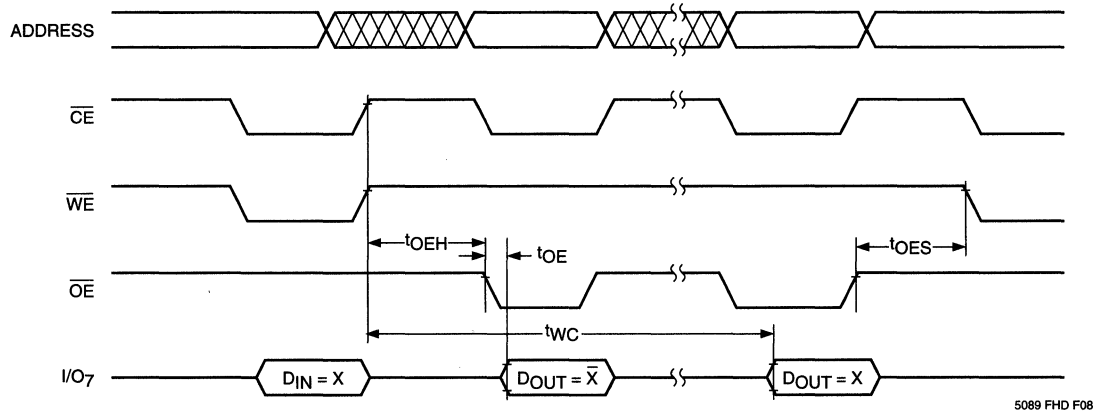


Figure 6. $\overline{DATA}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C16A.

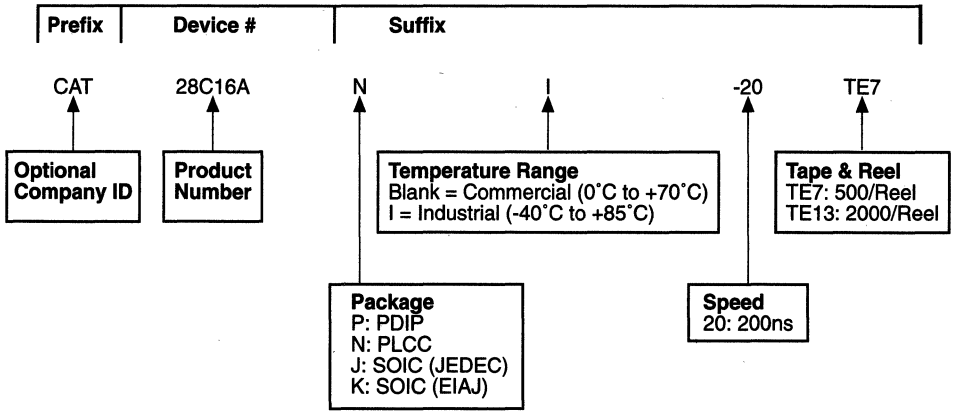
(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

ORDERING INFORMATION



28C16A F09

Notes:
(1) The device used in the above example is a CAT28C16ANI-20TE7 (PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

8

CAT28C17A

16K-Bit CMOS E²PROM

FEATURES

- **Fast Read Access Times: 200 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 25 mA Max.**
  - **–Standby: 100 µA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Write Cycle Time: 10ms Max**
- **End of Write Detection:**
  - **–$\overline{\text{DATA}}$ Polling**
  - **–RDY/$\overline{\text{BUSY}}$ Pin**
- **Hardware Write Protection**
- **CMOS and TTL Compatible I/O**
- **10,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Commercial and Industrial Temperature Ranges**

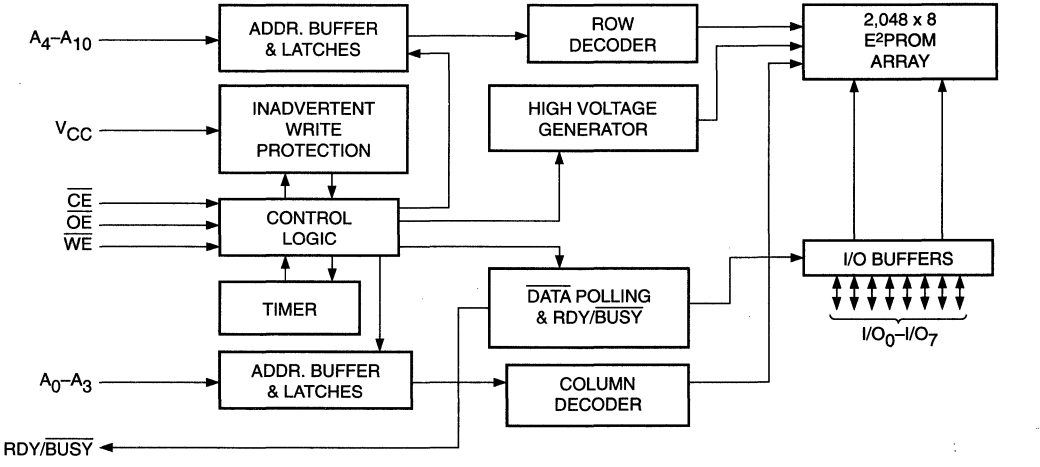
DESCRIPTION

The CAT28C17A is a fast, low power, 5V-only CMOS E²PROM organized as 2K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and a RDY/$\overline{\text{BUSY}}$ pin signal the start and end of the self-timed write cycle. Additionally, the CAT28C17A features hardware write protection.

The CAT28C17A is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28-pin DIP and SOIC or 32-pin PLCC packages.

8

BLOCK DIAGRAM



5091 FHD F02

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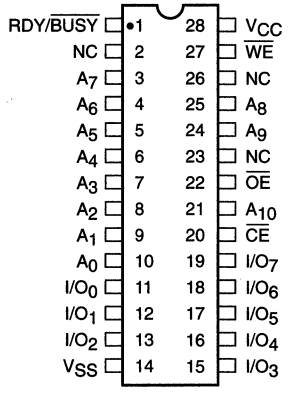
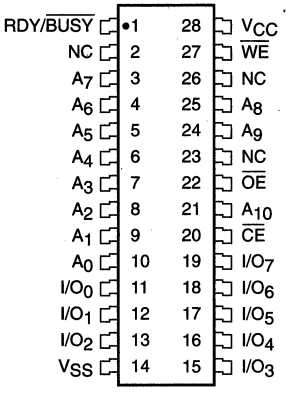
PIN CONFIGURATION

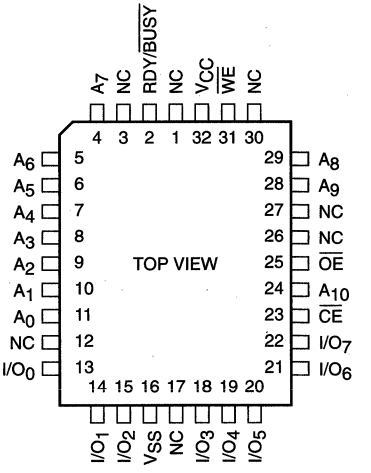
DIP Package (P)



SOIC Package (J,K)



PLCC Package (N)



5091 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

8

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			35	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C17A-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	200		ns
t_{CE}	$\overline{CE}$ Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	$\overline{OE}$ Access Time		80	ns
t_{LZ}[1]	$\overline{CE}$ Low to Active Output	0		ns
t_{OLZ}[1]	$\overline{OE}$ Low to Active Output	0		ns
t_{HZ}[1][2]	$\overline{CE}$ High to High-Z Output		55	ns
t_{OHZ}[1][2]	$\overline{OE}$ High to High-Z Output		55	ns
t_{OH}[1]	Output Hold from Address Change	0		ns

Figure 1. A.C. Testing Input/Output Waveform(3)

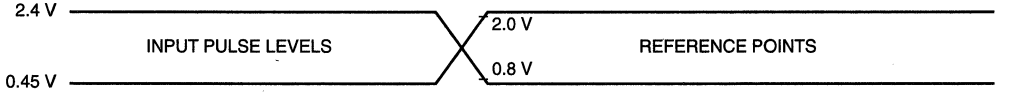


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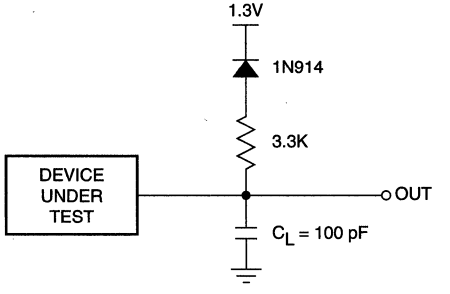
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C17A-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	150		ns
t_{OES}	$\overline{OE}$ Setup Time	15		ns
t_{OEH}	$\overline{OE}$ Hold Time	15		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	150		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{DL}	Data Latch Time	50		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	ms
t_{DB}	Time to Device Busy		80	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.

DEVICE OPERATION

Read

Data stored in the CAT28C17A is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Ready/$\overline{BUSY}$ (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

Figure 3. Read Cycle

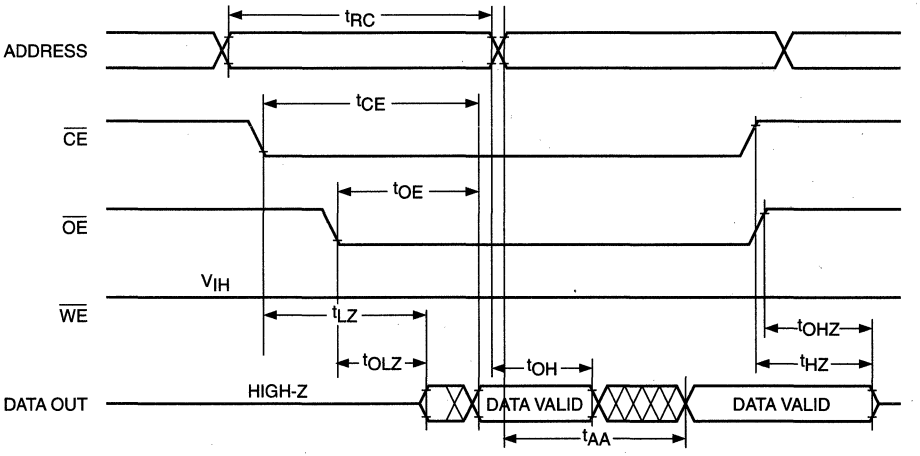
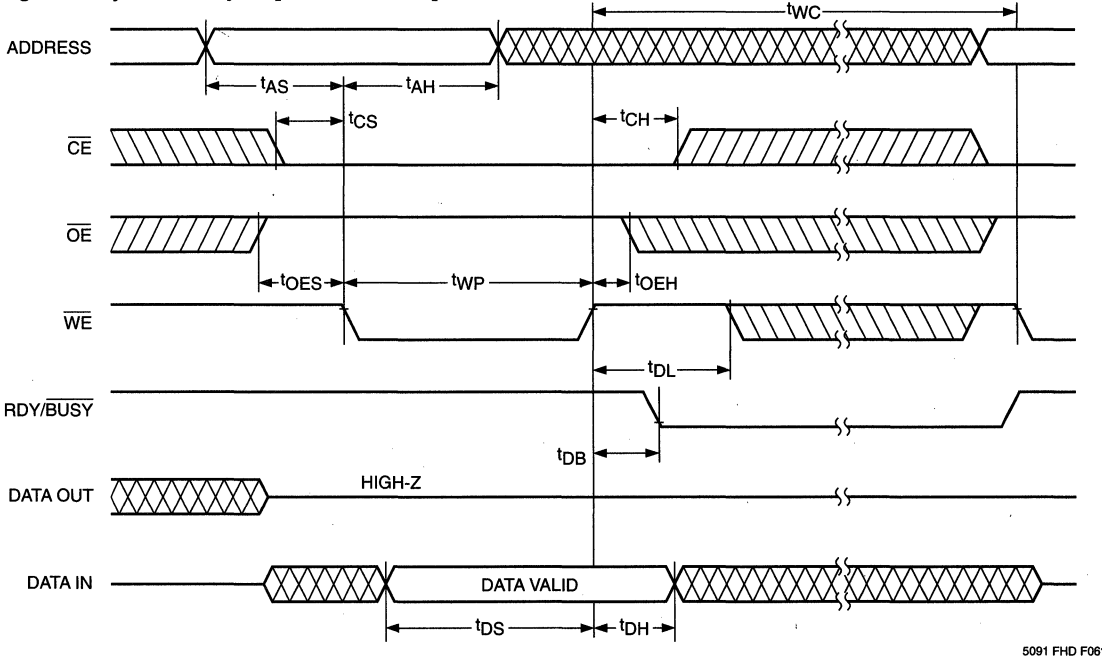


Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

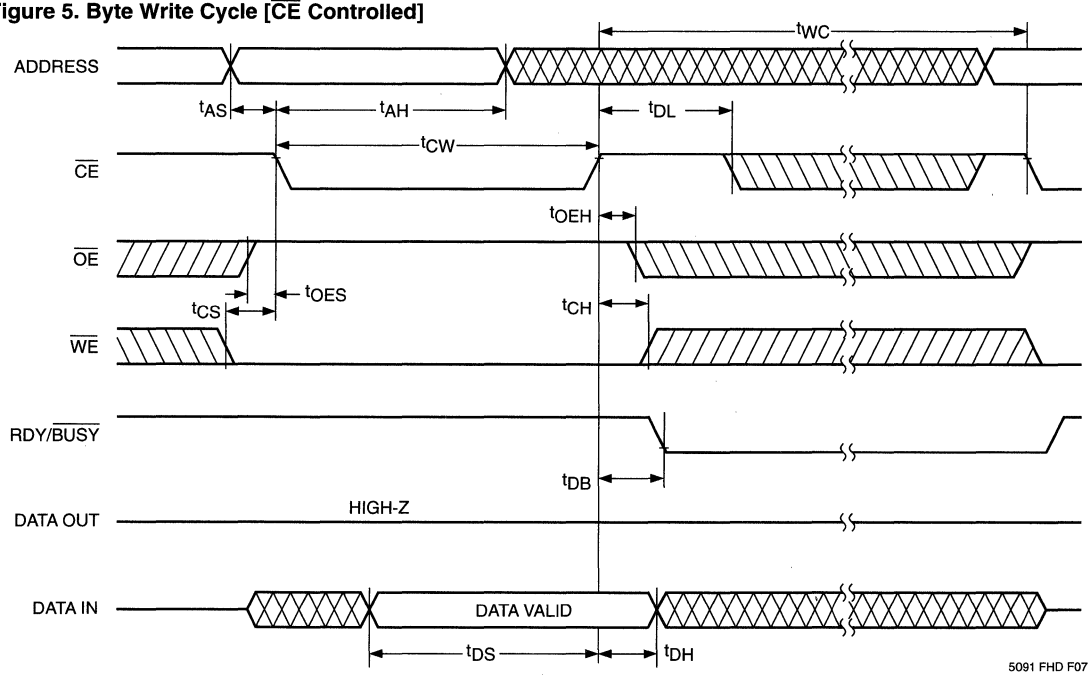
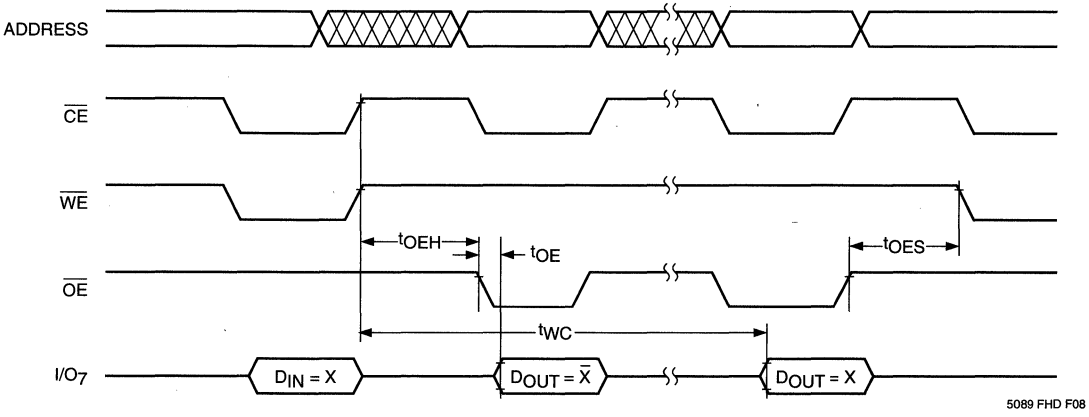


Figure 6. $\overline{DATA}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C17A.

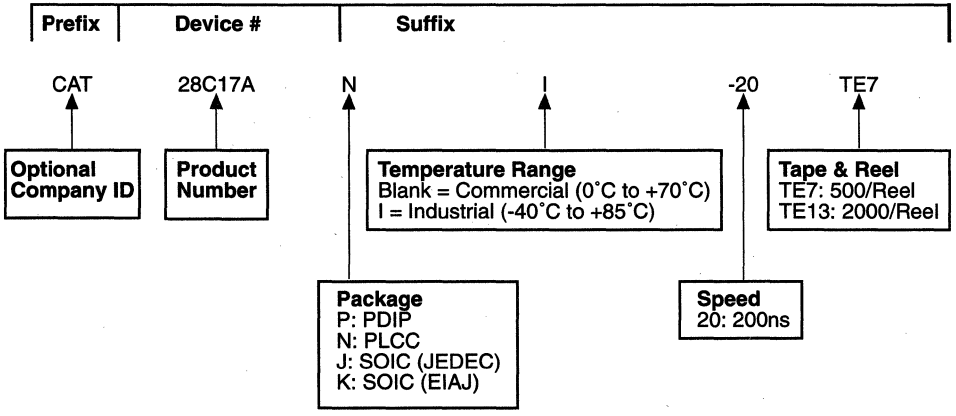
(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT28C17ANI-20TE7 (PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

CAT28C64B

64K-Bit CMOS E²PROM

FEATURES

- **Fast Read Access Times:**
  - **120/150/200ns**
- **Low Power CMOS Dissipation:**
  - **Active: 25 mA Max.**
  - **Standby: 100 μA Max.**
- **Simple Write Operation:**
  - **On-Chip Address and Data Latches**
  - **Self-Timed Write Cycle with Auto-Clear**
- **Fast Write Cycle Time:**
  - **5ms Max. (3ms available)**
- **CMOS and TTL Compatible I/O**
- **Commerical and Industrial Temperature Ranges**
- **Automatic Page Write Operation:**
  - **1 to 32 Bytes in 5ms**
  - **Page Load Timer**
- **End of Write Detection:**
  - **Toggle Bit**
  - **$\overline{\text{DATA}}$ Polling**
- **Hardware and Software Write Protection**
- **100,000 Program/Erase Cycles**
- **100 Year Data Retention**

DESCRIPTION

The CAT28C64B is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C64B features hardware and software write protection.

The CAT28C64B is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC-approved 28-pin DIP, TSOP and SOIC, or, 32-pin PLCC and TSOP packages.

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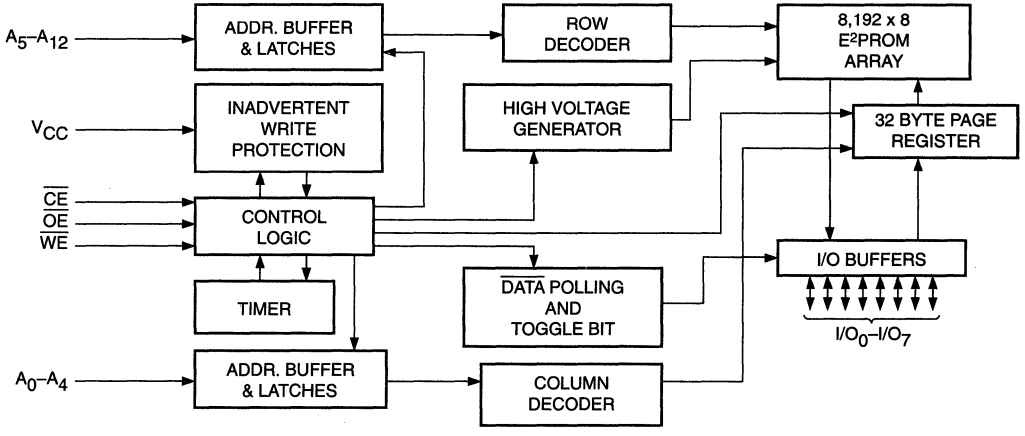
BLOCK DIAGRAM



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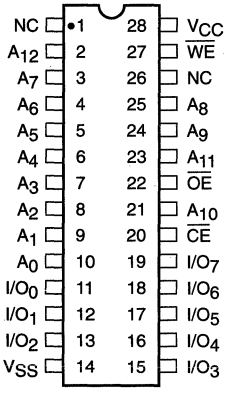
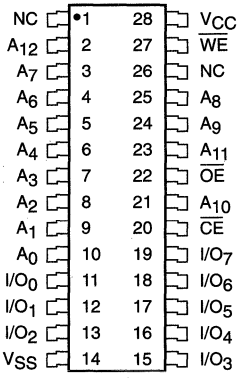
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



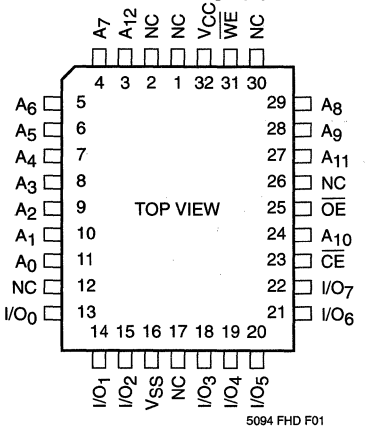
SOIC Package (J, K)



PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

PLCC Package (N)



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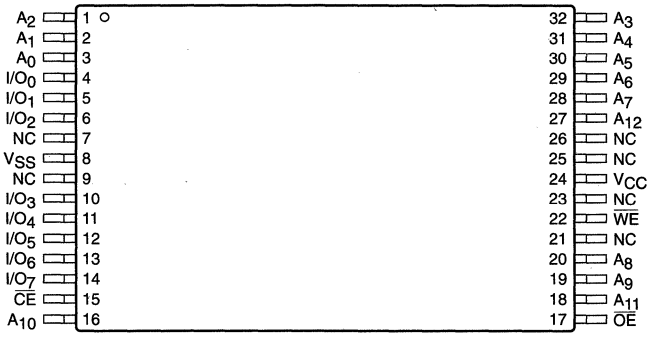
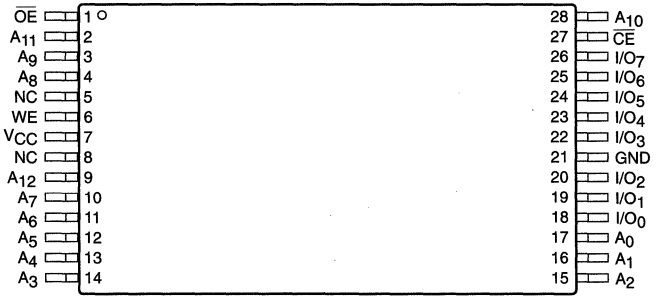
TSOP Package (8mm x 14mm) (T14)
TSOP Package (8mm x 20mm) (T)



TSOP Package (8mm x 13.4mm) (T13)



28C64B F03

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = $1/t_{RC}$ min, All I/O's Open
I_{CCC}(1)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = $1/t_{RC}$ min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(2)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(2)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}(1)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

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Note:
(1) V_{ILC} = –0.3V to +0.3V.
(2) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64B-12		28C64B-15		28C64B-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AA}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		60		70		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(3)

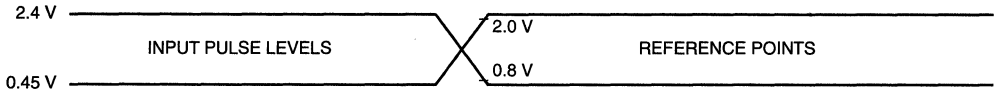

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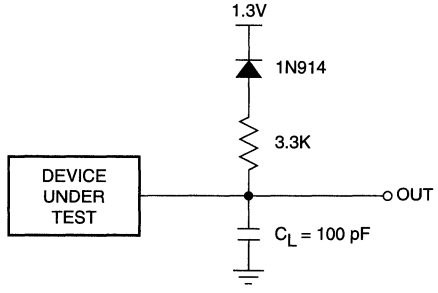
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64B-12		28C64B-15		28C64B-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	110		110		110		ns
t_{OES}	$\overline{OE}$ Setup Time	0		0		0		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		0		0		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	110		110		110		ns
t_{DS}	Data Setup Time	60		60		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(3)	Byte Load Cycle Time	.05	100	.05	100	.05	100	µs

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

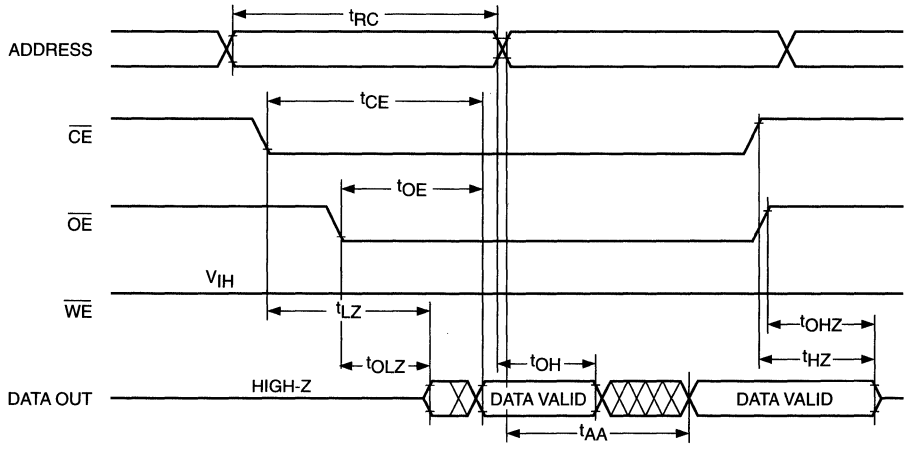
Read

Data stored in the CAT28C64B is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

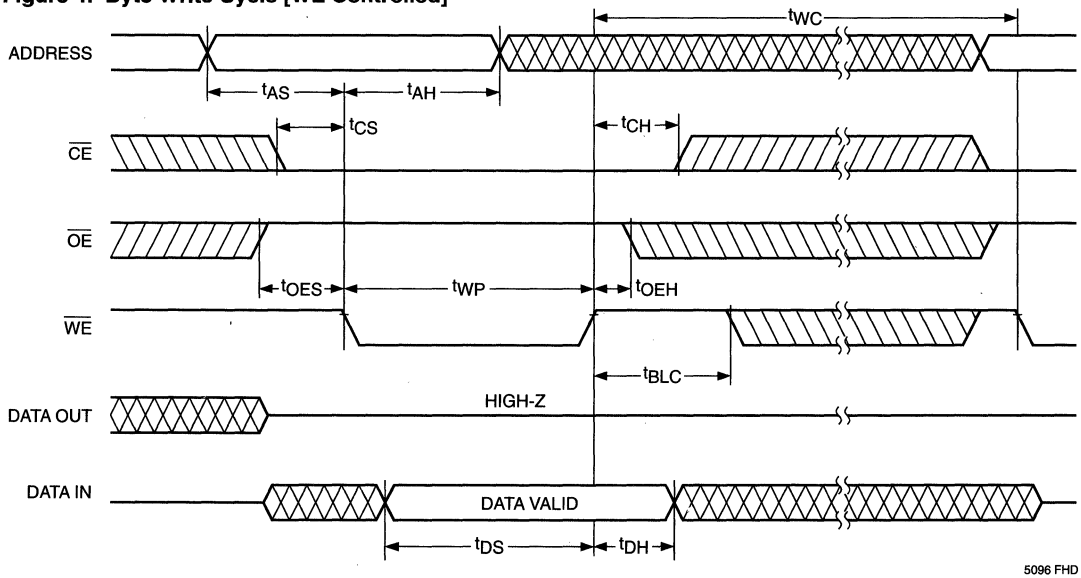
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle



28C64B F06

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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Page Write

The page write mode of the CAT28C64B (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

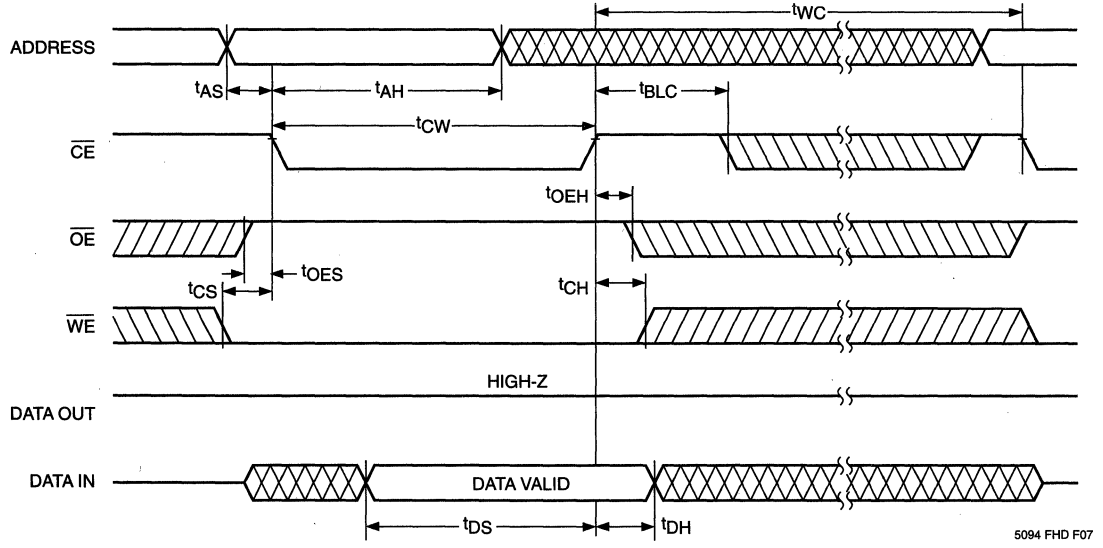
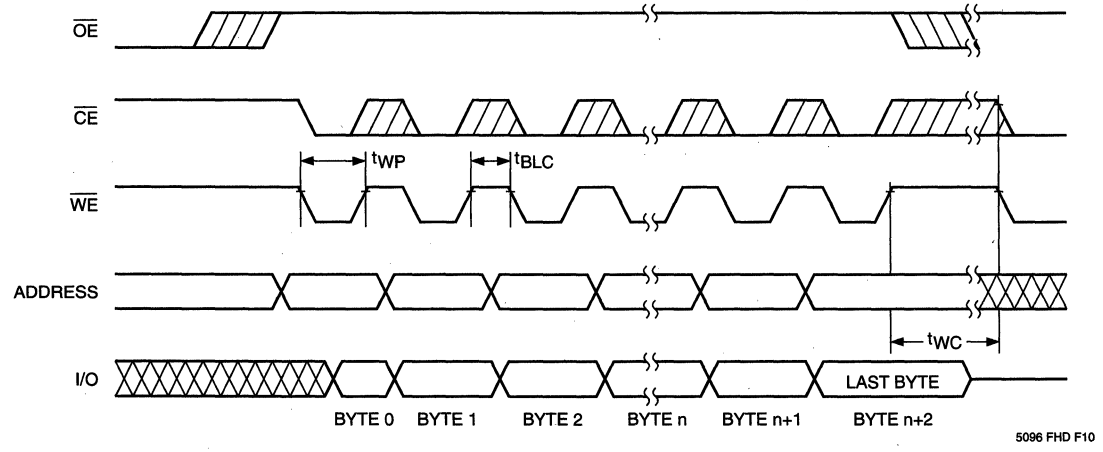


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling

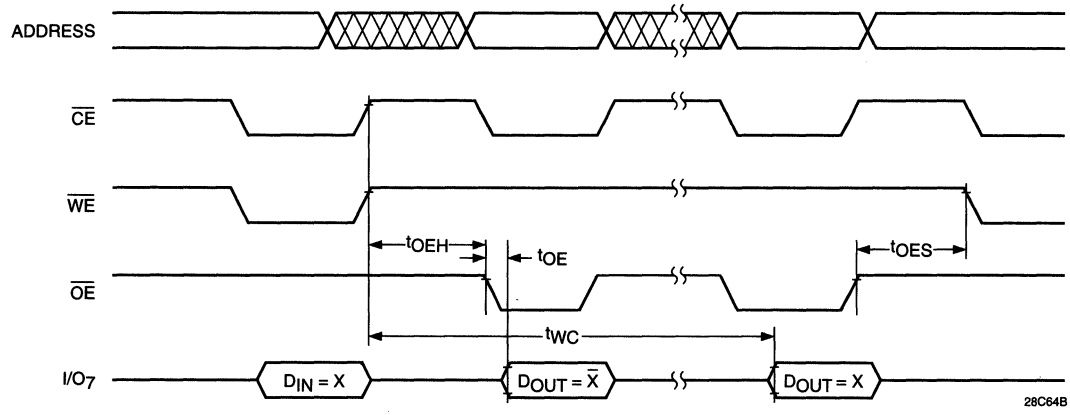
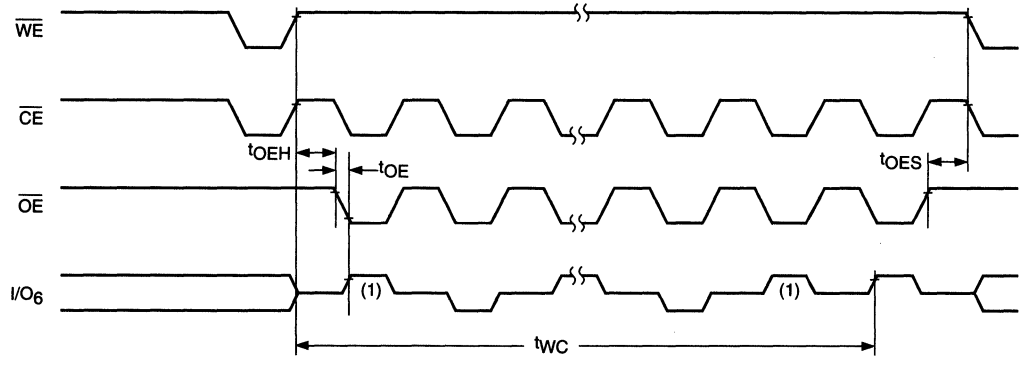


Figure 8. Toggle Bit



Note:
(1) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C64B.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28C64B features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C64B is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

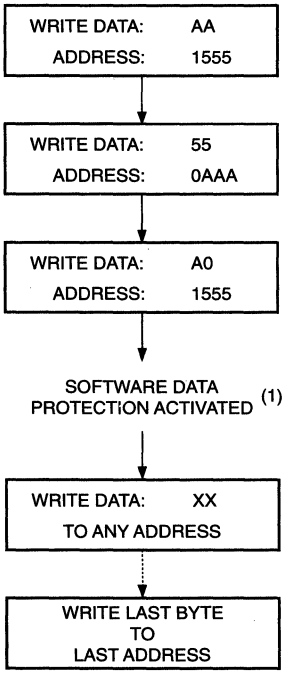


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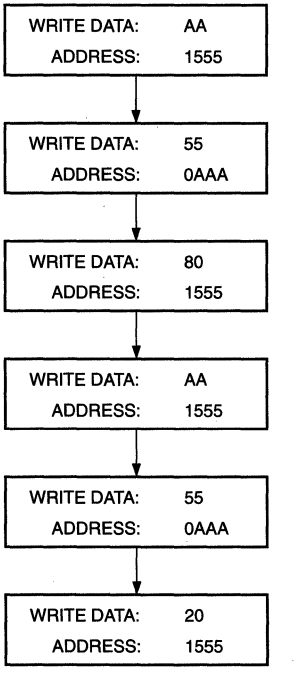
Figure 10. Write Sequence for Deactivating Software Data Protection



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Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

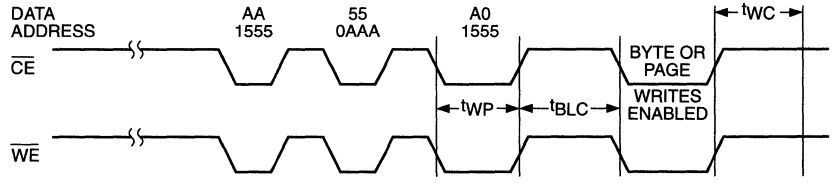

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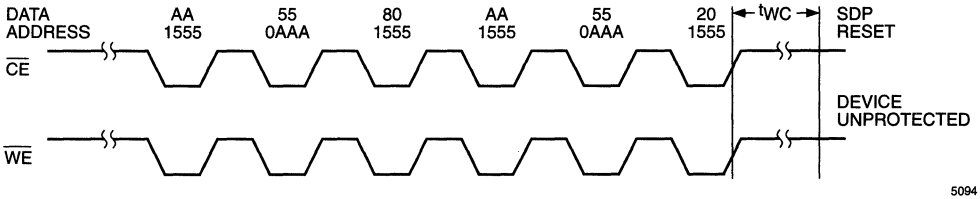
Figure 12. Resetting Software Data Protection Timing



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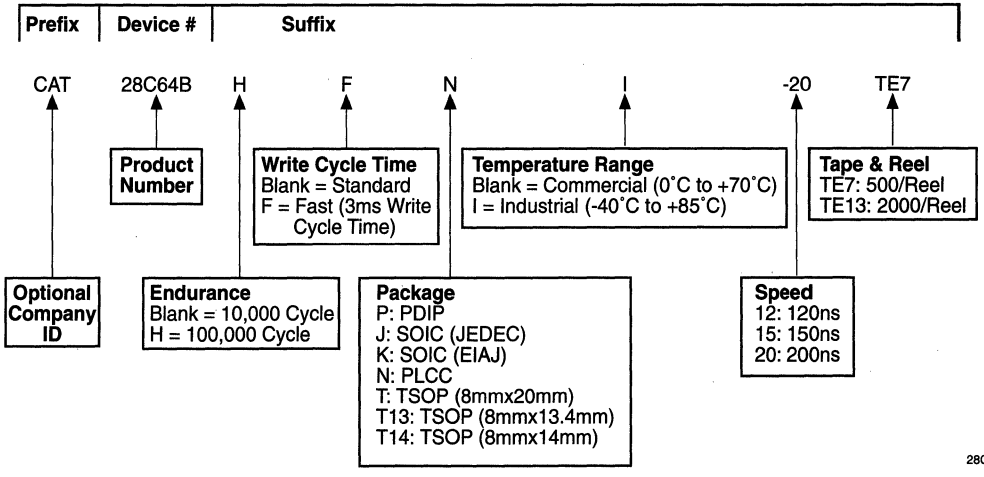
ORDERING INFORMATION



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Notes:

(1) The device used in the above example is a CAT28C64BHFNI-20TE7 (100,000 Cycle Endurance, 3ms Write Cycle Time, PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

CAT28C65B

64K-Bit CMOS E²PROM

FEATURES

- **Fast Read Access Times:**
  - **120/150/200ns**
- **Low Power CMOS Dissipation:**
  - **Active: 25 mA Max.**
  - **Standby: 100 µA Max.**
- **Simple Write Operation:**
  - **On-Chip Address and Data Latches**
  - **Self-Timed Write Cycle with Auto-Clear**
- **Fast Write Cycle Time:**
  - **5ms Max. (3ms available)**
- **CMOS and TTL Compatible I/O**
- **Commercial and Industrial Temperature Ranges**
- **Automatic Page Write Operation:**
  - **1 to 32 Bytes in 5ms**
  - **Page Load Timer**
- **End of Write Detection:**
  - **Toggle Bit**
  - **$\overline{\text{DATA}}$ Polling**
  - **RDY/$\overline{\text{BUSY}}$**
- **Hardware and Software Write Protection**
- **100,000 Program/Erase Cycles**
- **100 Year Data Retention**

DESCRIPTION

The CAT28C65B is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling, a RDY/$\overline{\text{BUSY}}$ pin and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C65B features hardware and software write protection.

The CAT28C65B is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC-approved 28-pin DIP, TSOP and SOIC, or 32-pin PLCC and TSOP packages.

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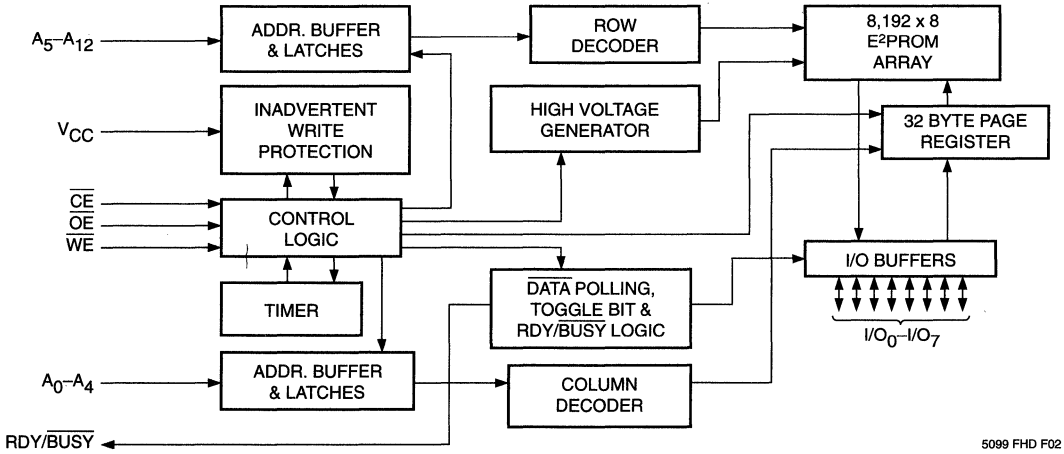
BLOCK DIAGRAM



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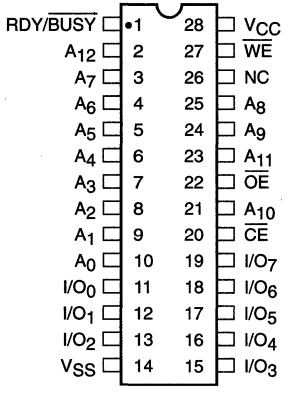
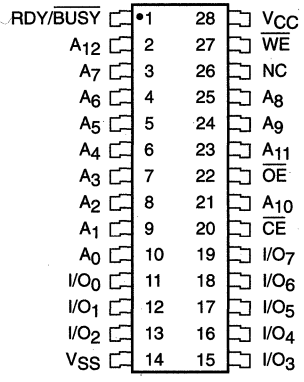
Characteristics subject to change without notice

PIN CONFIGURATION

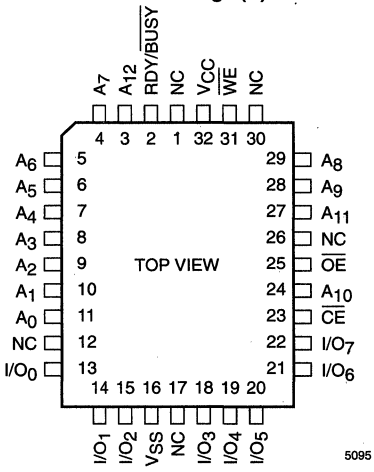
DIP Package (P)



SOIC Package (J, K)



PLCC Package (N)



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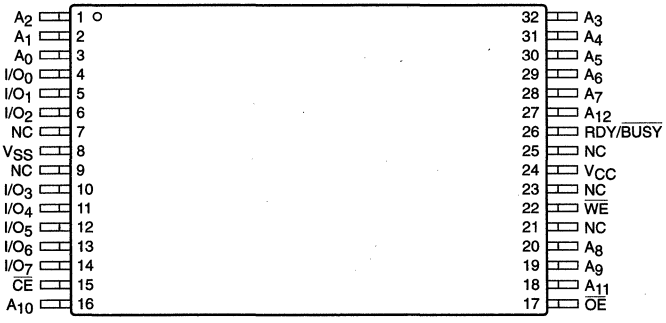
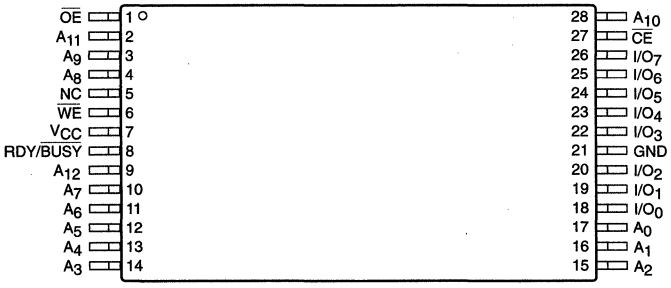
TSOP Package (8mm x 14mm) (T14)
TSOP Package (8mm x 20mm) (T)



TSOP Package (8mm x 13.4mm) (T13)



28C65B F03

PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

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MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE $T_A = 25°C$, F = 1.0 MHZ, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
C_{IN}(1)	Input Capacitance	6	pF	$V_{IN} = 0V$

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) . 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(1)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(2)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(2)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}(1)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

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Note:
(1) V_{ILC} = –0.3V to +0.3V.
(2) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C65B-12		28C65B-15		28C65B-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AA}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		60		70		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(3)

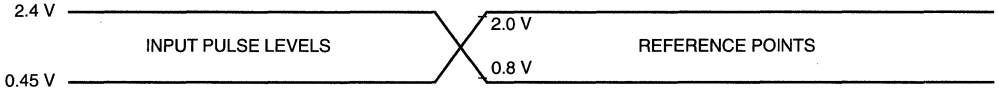

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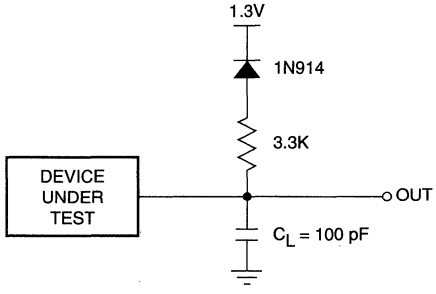
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C65B-12		28C65B-15		28C65B-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	110		110		110		ns
t_{OES}	$\overline{OE}$ Setup Time	0		0		0		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		0		0		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	110		110		110		ns
t_{RB}	$\overline{WE}$ Low to RDY/$\overline{BUSY}$ Low		120		120		120	ns
t_{DS}	Data Setup Time	60		60		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(3)	Byte Load Cycle Time	.05	100	.05	100	.05	100	µs

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

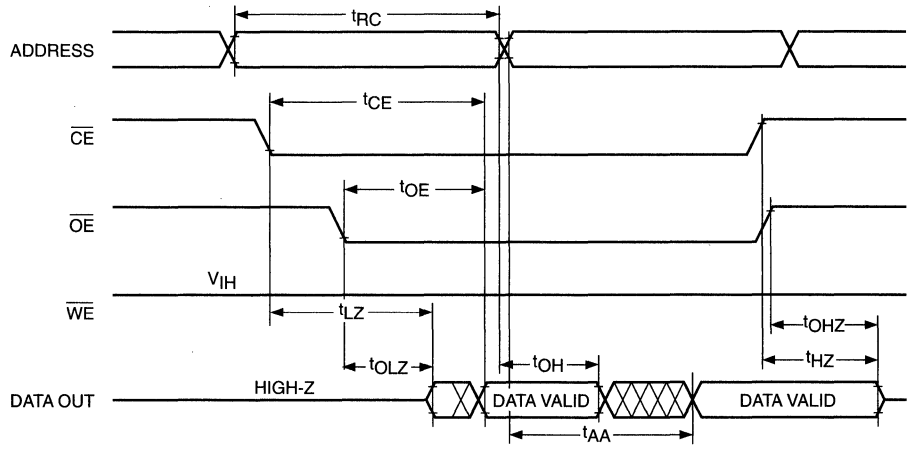
Read

Data stored in the CAT28C65B is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the

Figure 3. Read Cycle



28C65B F05

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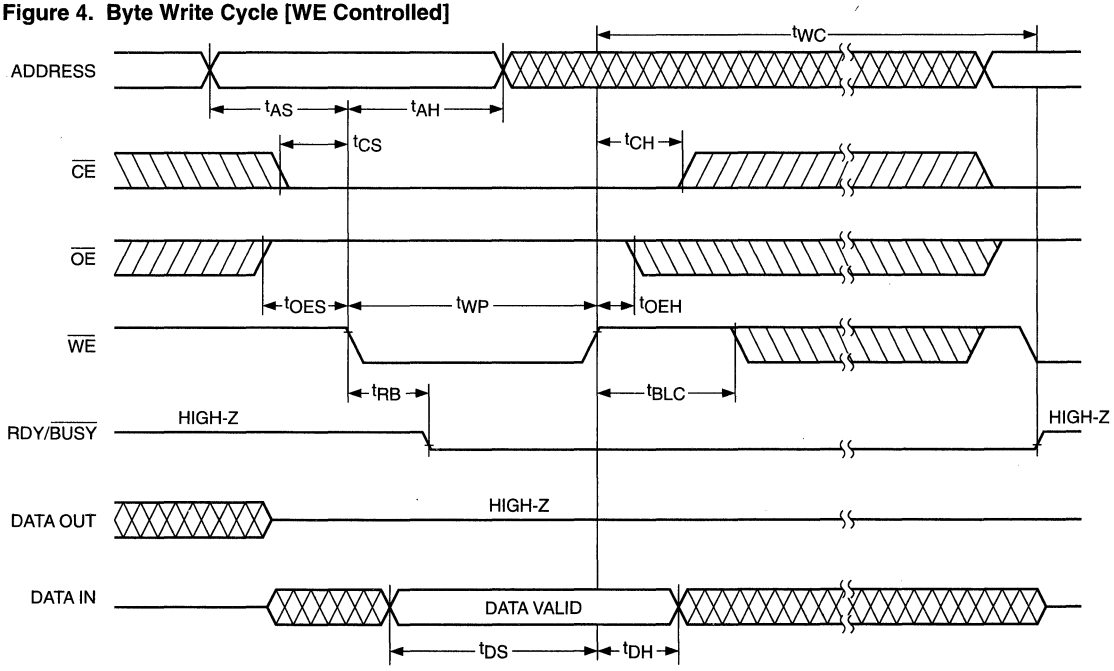
Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Page Write

The page write mode of the CAT28C65B (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation (WE pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

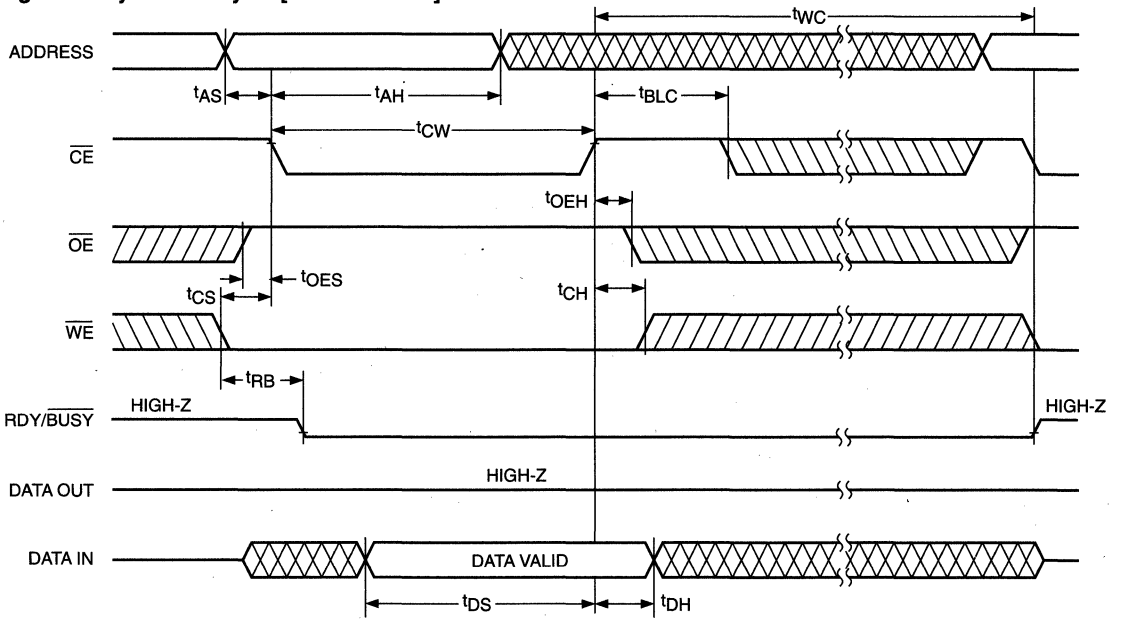

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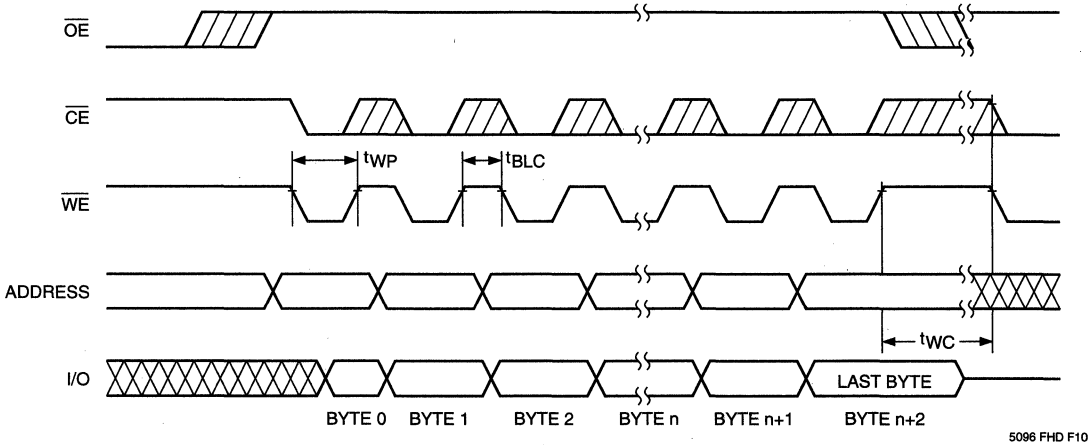
Figure 6. Page Mode Write Cycle



5096 FHD F10

(which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{DATA}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Ready/$\overline{BUSY}$ (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

Figure 7. $\overline{DATA}$ Polling

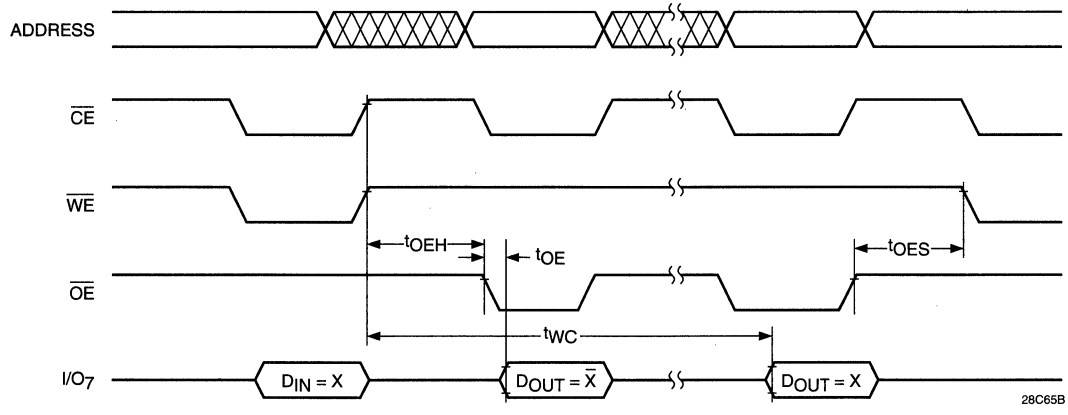
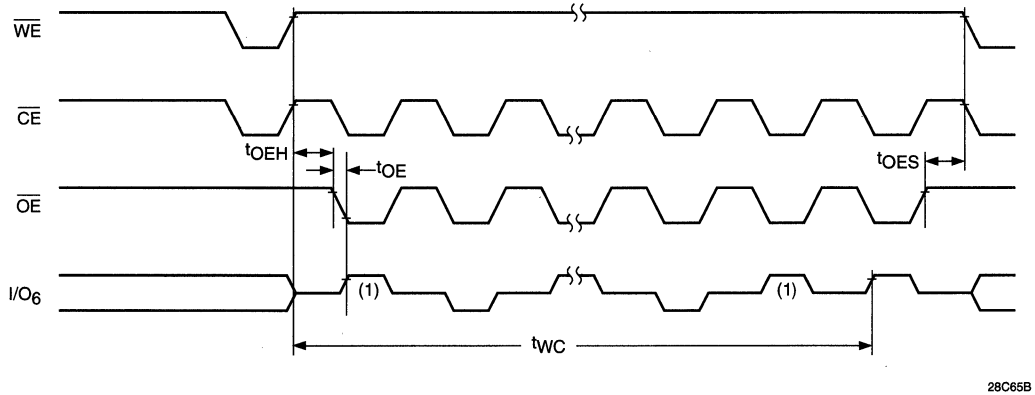


Figure 8. Toggle Bit



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C65B.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28C65B features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C65B is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

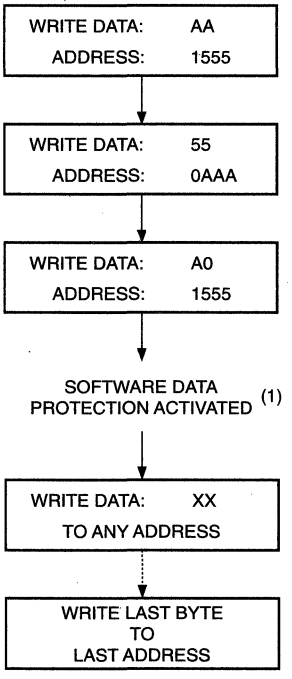


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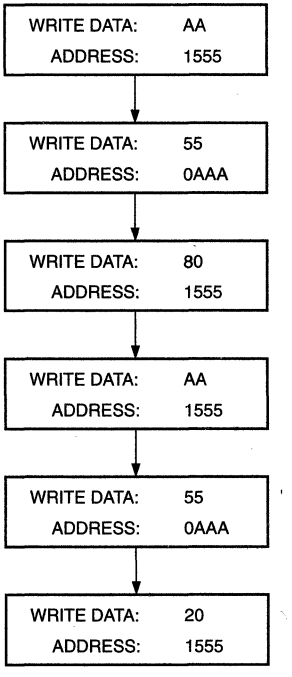
Figure 10. Write Sequence for Deactivating Software Data Protection



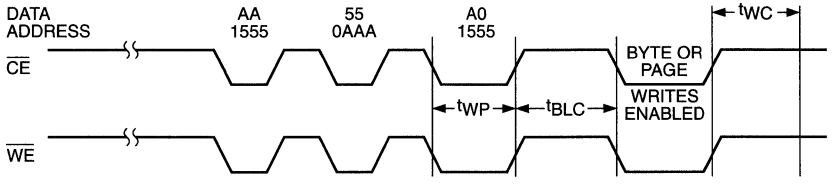
5094 FHD F09

Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

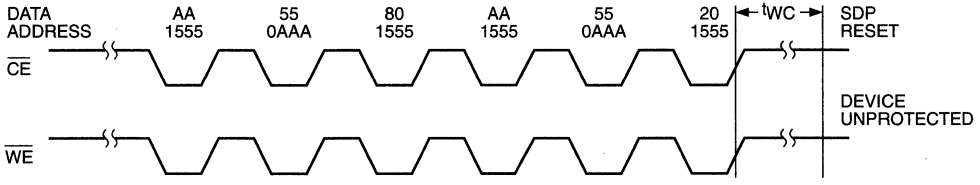
To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing



5094 FHD F13

Figure 12. Resetting Software Data Protection Timing



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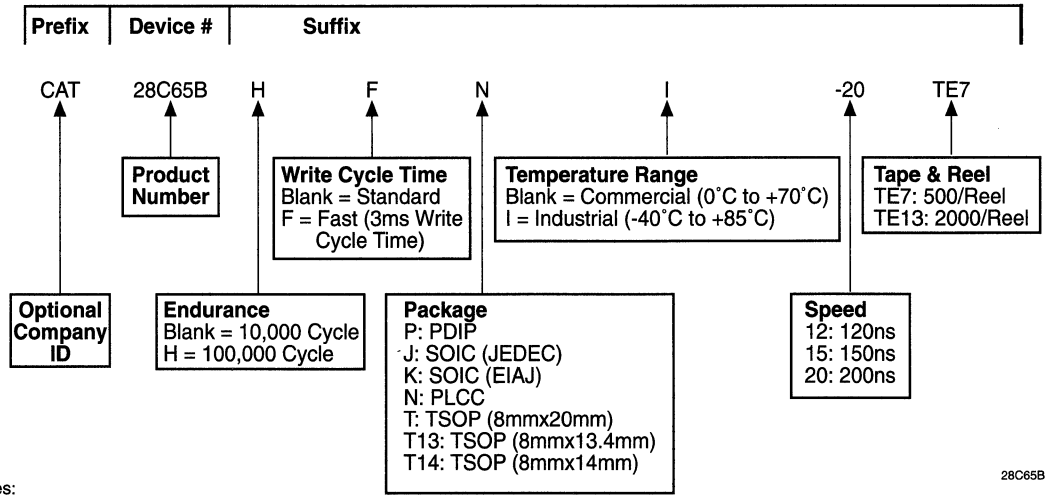
ORDERING INFORMATION



28C65B F15

Notes:

(1) The device used in the above example is a CAT28C65BHFNI-20TE7 (100,000 Cycle Endurance, 3ms Write Cycle Time, PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

CAT28C256

256K-Bit CMOS E²PROM

FEATURES

- Fast Read Access Times: 150/200/250 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA Max.
  - –Standby: 150 µA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time:
  - –10ms Max (5ms available)
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - –1 to 64 Bytes in 10ms
  - –Page Load Timer
- End of Write Detection:
  - –Toggle Bit
  - –$\overline{\text{DATA}}$ Polling
- Hardware and Software Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial and Industrial Temperature Ranges

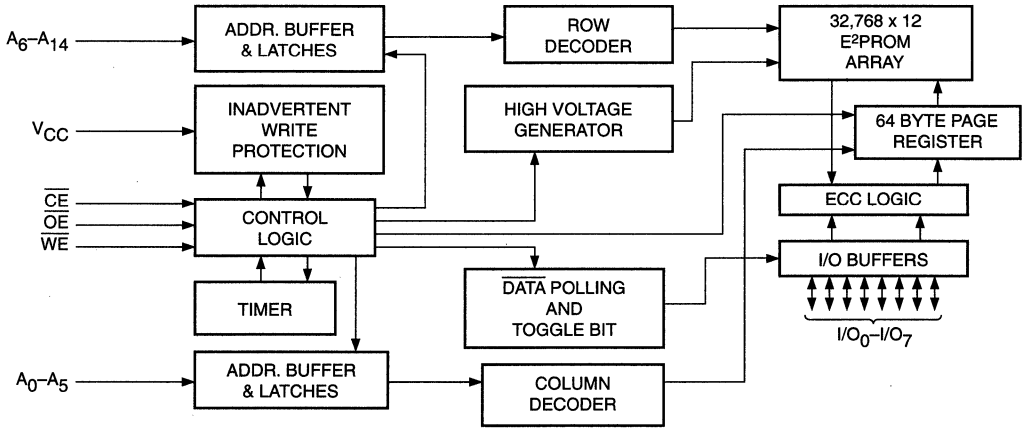
DESCRIPTION

The CAT28C256 is a fast, low power, 5V-only CMOS E²PROM organized as 32K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C256 features hardware and software write protection as well as an internal Error Correction Code (ECC) for extremely high reliability.

The CAT28C256 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, 28-pin TSOP, 32-pin TSOP or 32-pin PLCC packages.

8

BLOCK DIAGRAM



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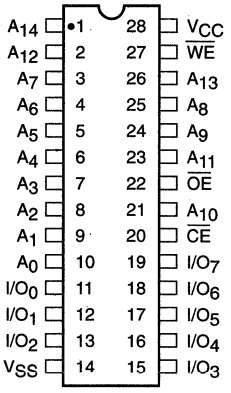
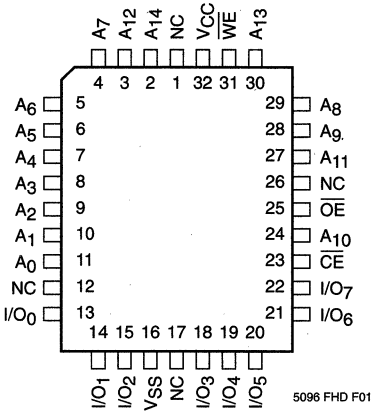
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



PLCC Package (N)

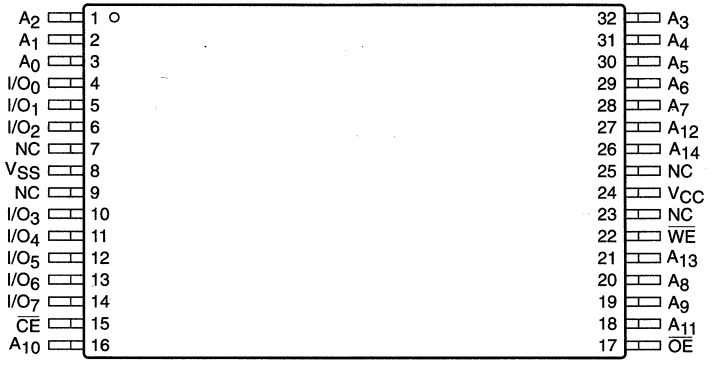


5096 FHD F01

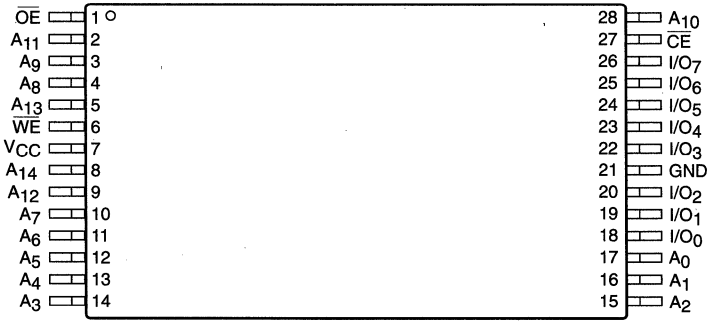
PIN FUNCTIONS

Pin Name	Function
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

TSOP Package (8mm X 14mm) (T14)



TSOP Package (8mm X 13.4mm) (T13)



28C256 F03

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			150	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

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Symbol	Parameter	28C256-15		28C256-20		28C256-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	$\overline{CE}$ Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	$\overline{OE}$ Access Time		70		80		100	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		50		50		50	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		50		50		50	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

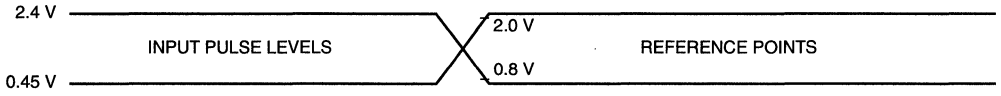
A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C256-15		28C256-20		28C256-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	75		75		75		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(3)	$\overline{CE}$ Pulse Time	100		100		100		ns
t_{OES}	$\overline{OE}$ Setup Time	0		0		0		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		0		0		ns
t_{WP}(3)	$\overline{WE}$ Pulse Width	100		100		100		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(4)	Byte Load Cycle Time	0.1	100	0.1	100	0.1	100	µs

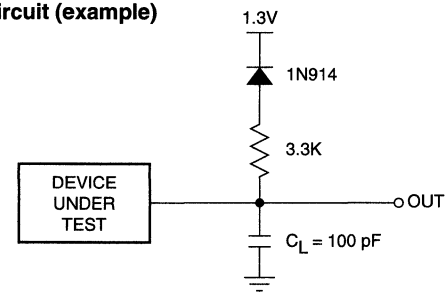
8

Figure 1. A.C. Testing Input/Output Waveform(2)



5096 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



5096 FHD F04

C_L INCLUDES JIG CAPACITANCE

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Input rise and fall times (10% and 90%) < 10 ns.
(3) A write pulse of less than 20ns duration will not initiate a write cycle.
(4) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

Read

Data stored in the CAT28C256 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

Figure 3. Read Cycle

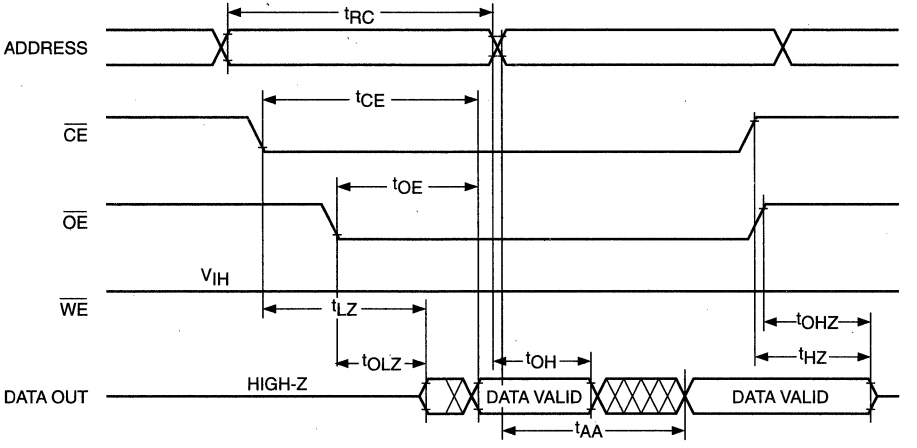
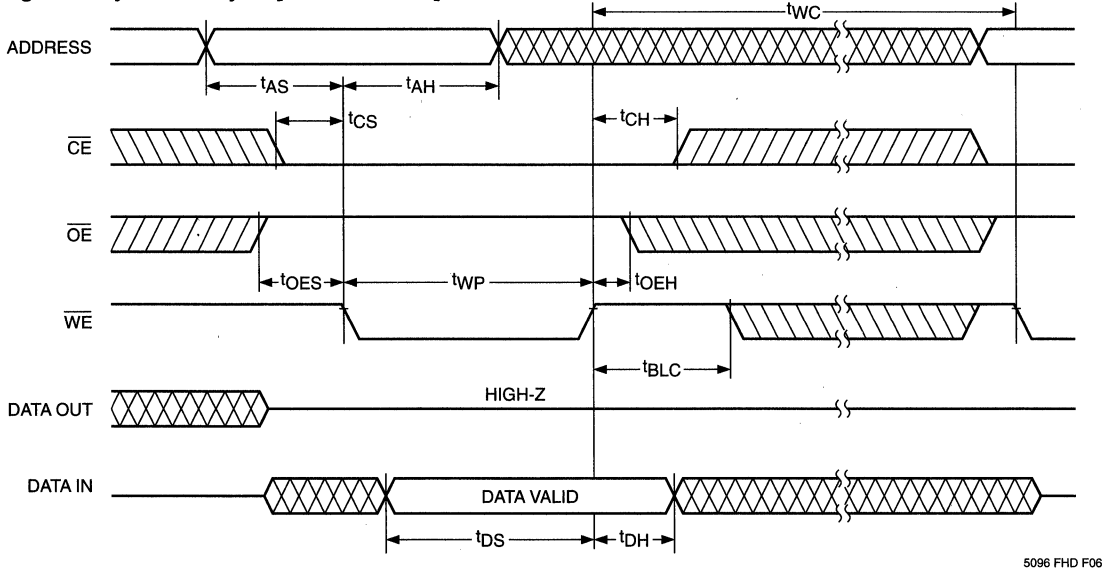


Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5096 FHD F06

Page Write

The page write mode of the CAT28C256 (essentially an extended BYTE WRITE mode) allows from 1 to 64 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 64.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 64 byte temporary buffer. The page address where data is to be written, specified by bits A_6 to A_{14}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_5 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

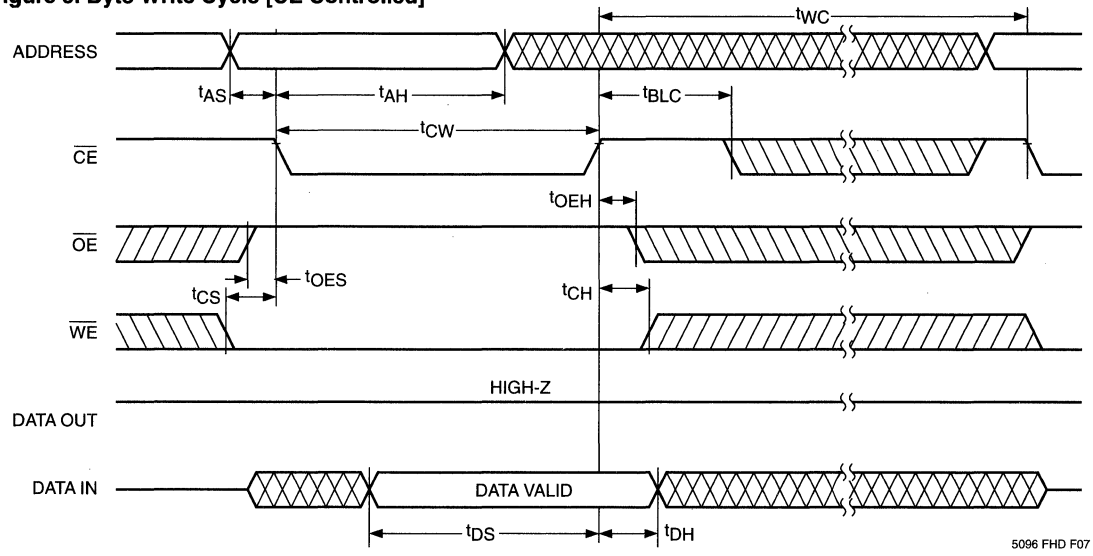
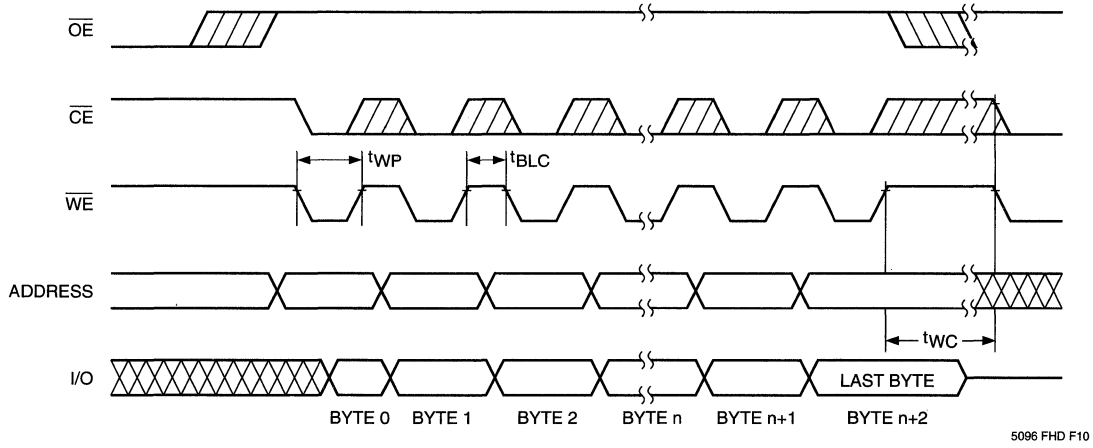


Figure 6. Page Mode Write Cycle



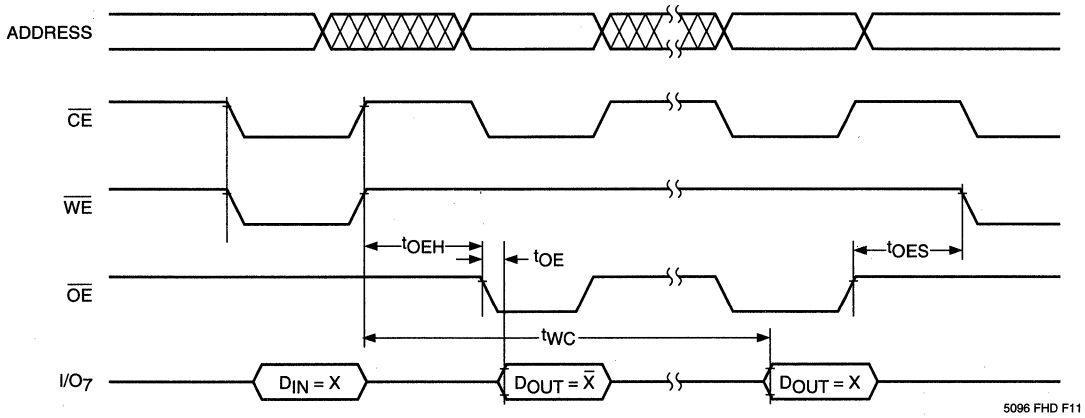
$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

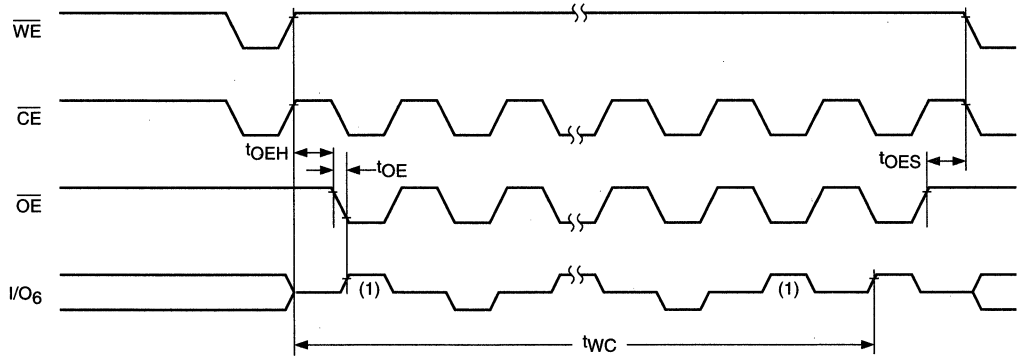
In addition to the $\overline{\text{DATA}}$ Polling feature of the CAT28C256, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling



5096 FHD F11

Figure 8. Toggle Bit



5096 FHD F12

Note:
(1) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C256.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

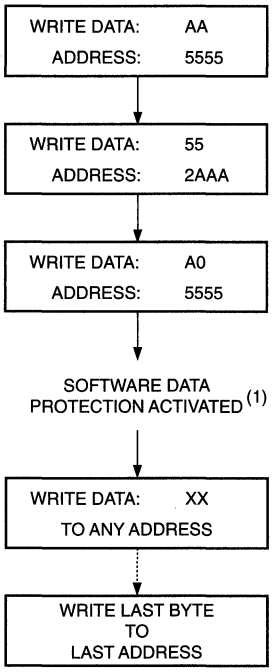
(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

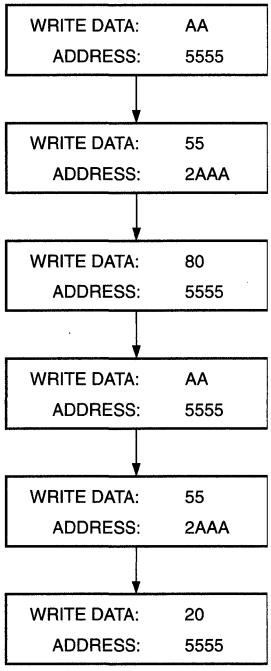
The CAT28C256 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C256 is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection



5096 FHD F08

Figure 10. Write Sequence for Deactivating Software Data Protection



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Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^{2}PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

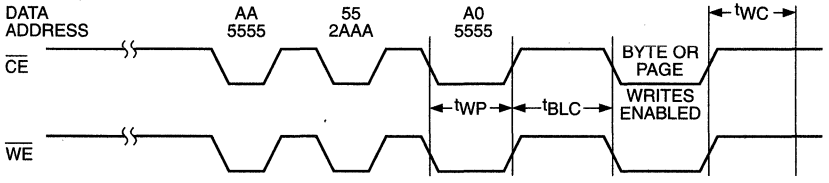
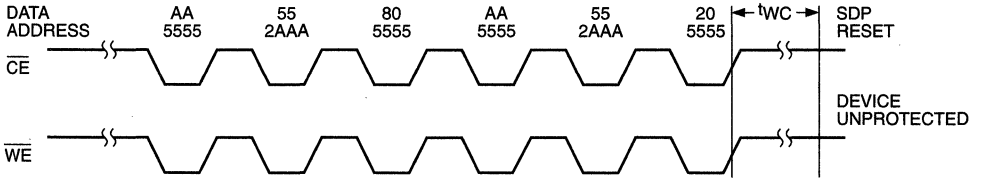
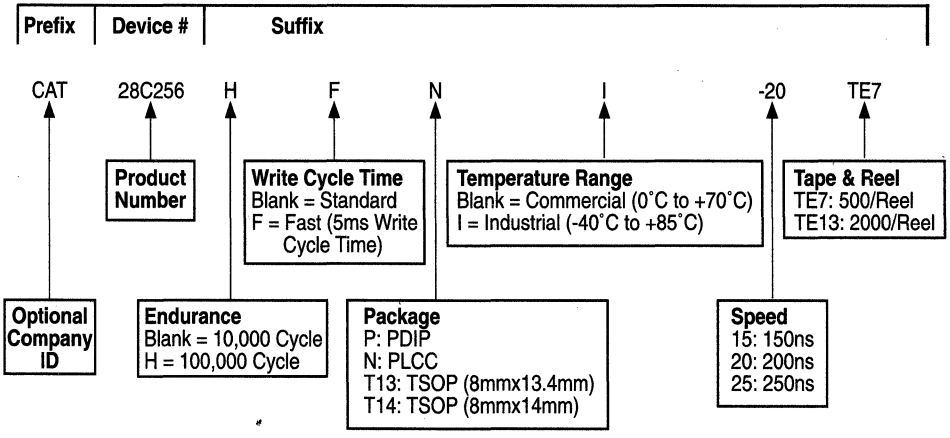


Figure 12. Resetting Software Data Protection Timing



8

ORDERING INFORMATION



Notes:

(1) The device used in the above example is a CAT28C256HFNI-20TE7 (100,000 Cycle Endurance, 5ms Write Cycle Time, PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

CAT28LV64

64K-Bit CMOS E²PROM

FEATURES

- 3.0V to 3.6 V Supply
- Read Access Times:
  - 250/300/350ns
- Low Power CMOS Dissipation:
  - Active: 8 mA Max.
  - Standby: 100 µA Max.
- Simple Write Operation:
  - On-Chip Address and Data Latches
  - Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time:
  - 5ms Max.
- Commercial and Industrial Temperature Ranges
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - 1 to 32 Bytes in 5ms
  - Page Load Timer
- End of Write Detection:
  - Toggle Bit
  - $\overline{\text{DATA}}$ Polling
- Hardware and Software Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

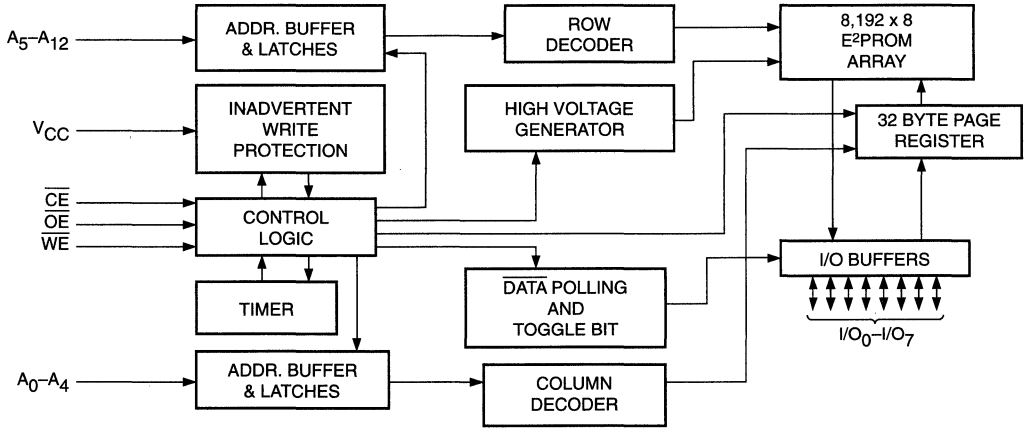
DESCRIPTION

The CAT28LV64 is a low voltage, low power, CMOS E²PROM organized as 8K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bit signal the start and end of the self-timed write cycle. Additionally, the CAT28LV64 features hardware and software write protection.

The CAT28LV64 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, TSOP and SOIC or 32-pin PLCC and TSOP packages.

8

BLOCK DIAGRAM



5094 FHD F02

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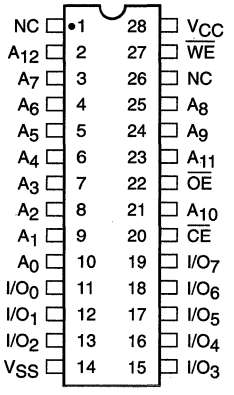
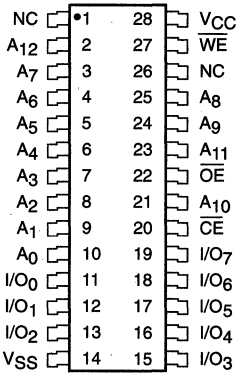
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



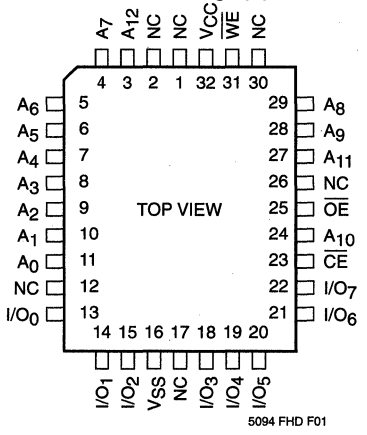
SOIC Package (J, K)



PIN FUNCTIONS

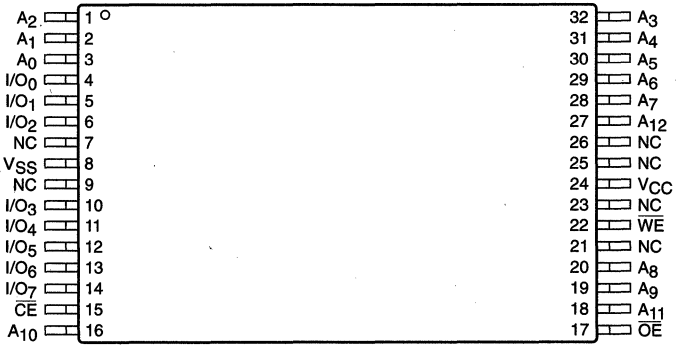
Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	3.0 to 3.6 V Supply
V_{SS}	Ground
NC	No Connect

PLCC Package (N)

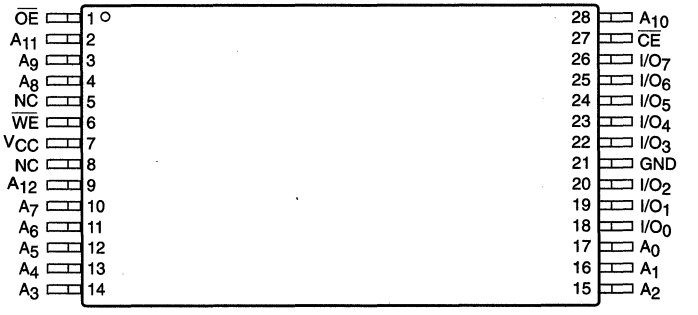


5094 FHD F01

TSOP Top View (8mm x 14mm) (T14)
TSOP Top View (8mm x 20mm) (T)



TSOP Top View (8mm x 13.4mm) (T13)



28LV64 F03

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Operating, TTL)			8	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{SBC}(1)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–5		5	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(1)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}	Low Level Input Voltage	–0.3		0.6	V	
V_{OH}	High Level Output Voltage	2			V	I_{OH} = –100µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 1.0mA
V_{WI}	Write Inhibit Voltage	2			V	

Note:
(1) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

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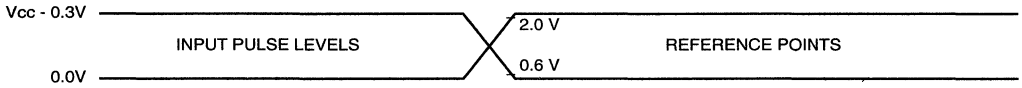
A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

		28LV64-25		28LV64-30		28LV64-35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	250		300		350		ns
t_{CE}	$\overline{CE}$ Access Time		250		300		350	ns
t_{AA}	Address Access Time		250		300		350	ns
t_{OE}	$\overline{OE}$ Access Time		100		150		150	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		55		60		60	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		55		60		60	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

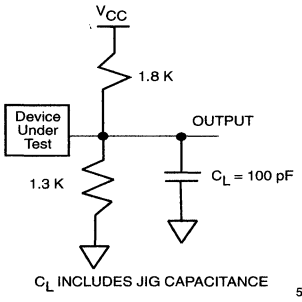
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

Figure 1. A.C. Testing Input/Output Waveform(1)



Note:
(1) Input rise and fall times (10% and 90%) < 10 ns.

Figure 2. A.C. Testing Load Circuit (example)



A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

Symbol	Parameter	28LV64-25		28LV64-30		28LV64-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	100		100		100		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(3)	Byte Load Cycle Time	0.1	100	0.1	100	0.1	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

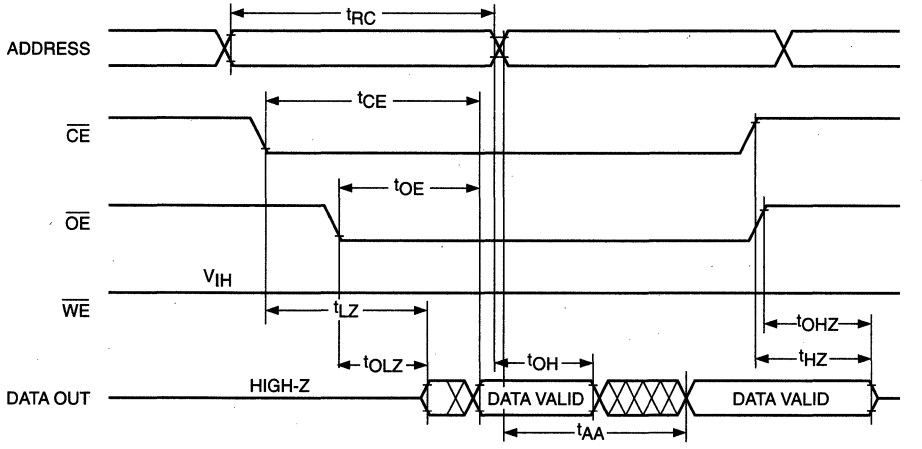
Read

Data stored in the CAT28LV64 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

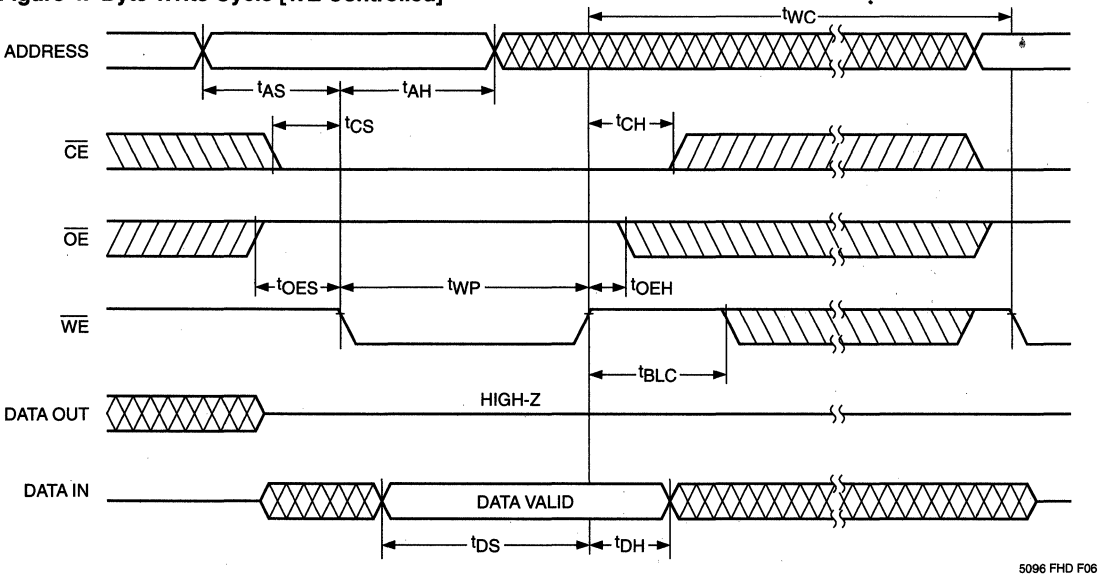
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle



28LV64 F06

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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Page Write

The page write mode of the CAT28LV64 (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

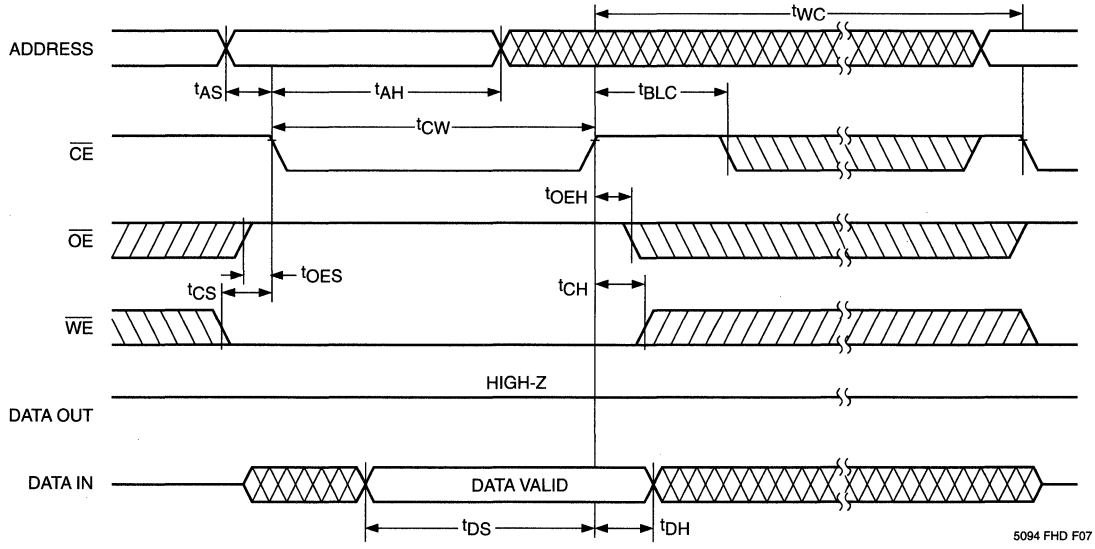
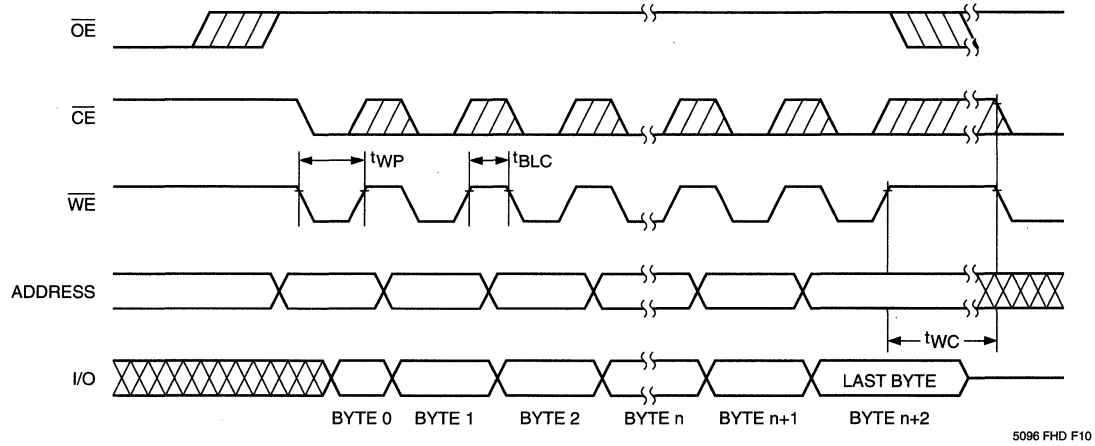


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling

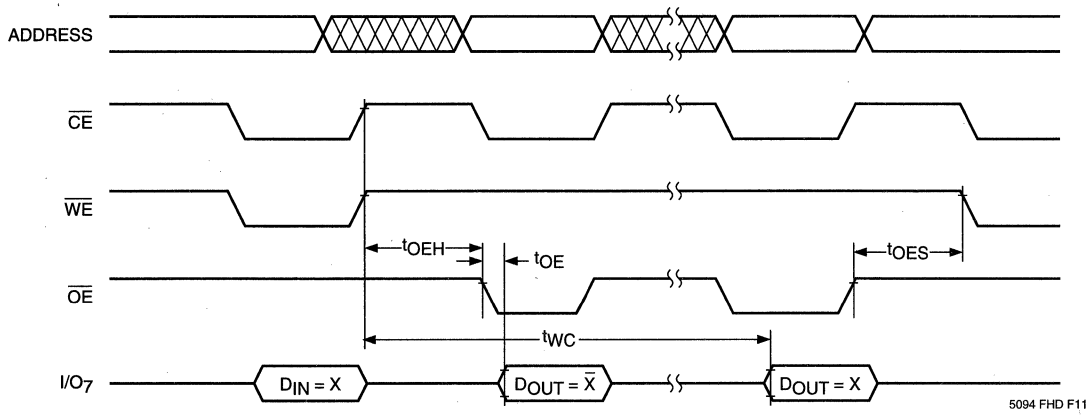
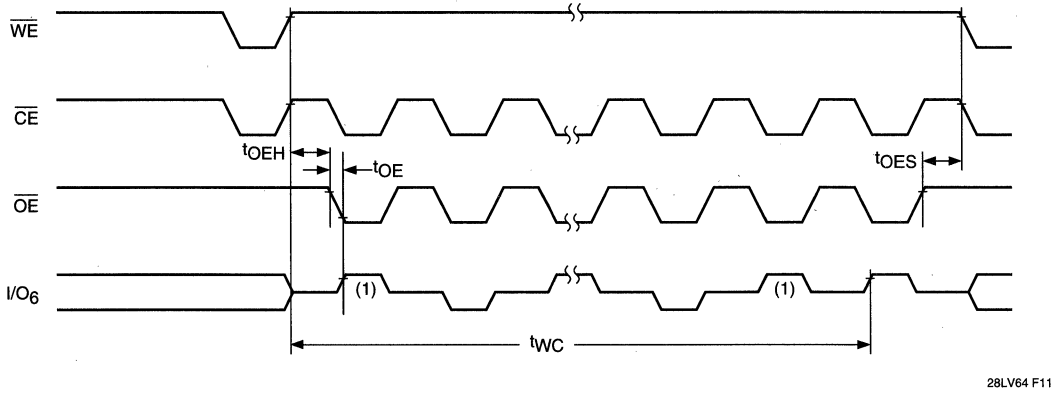


Figure 8. Toggle Bit



Note:
(1) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28LV64.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 2.40V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28LV64 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28LV64 is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

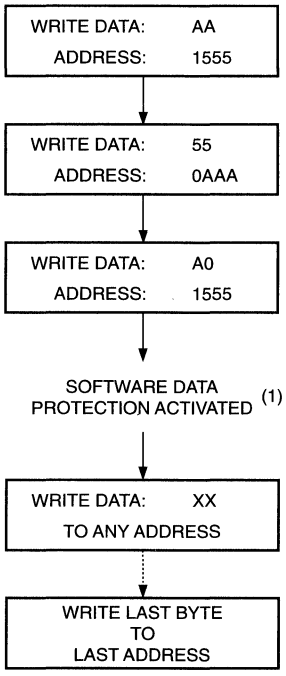


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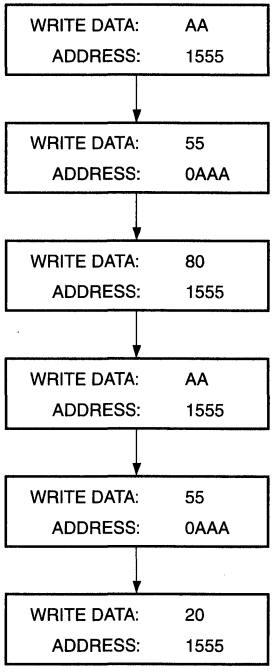
Figure 10. Write Sequence for Deactivating Software Data Protection



5094 FHD F09

Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

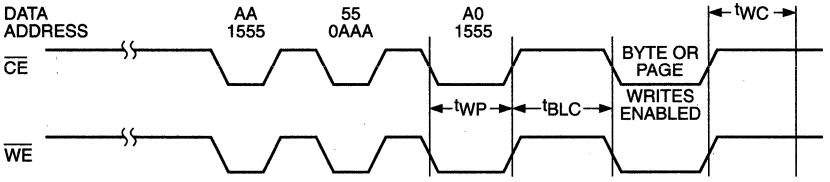


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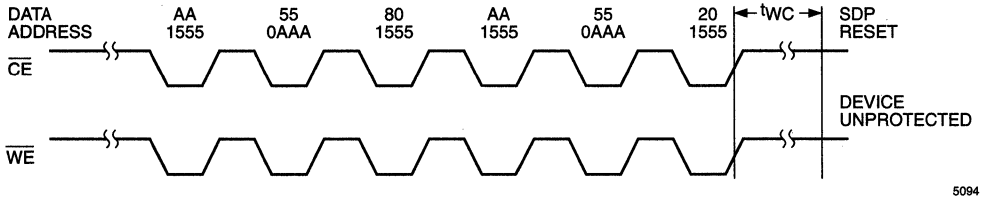
Figure 12. Resetting Software Data Protection Timing



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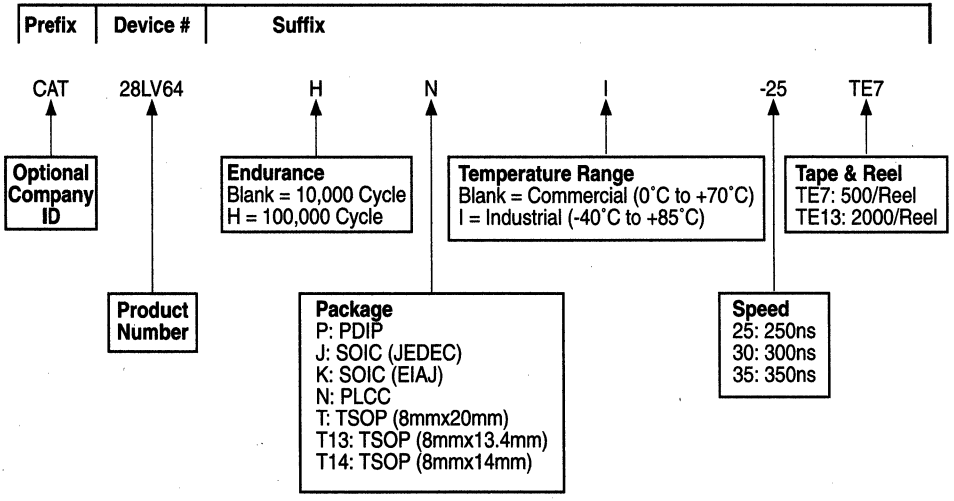
ORDERING INFORMATION



28LV64 F17

Notes:
(1) The device used in the above example is a CAT28LV64HNI-25TE7 (100,000 Cycle Endurance, PLCC, Industrial temperature, 250 ns Access Time, Tape & Reel).

CAT28LV65

64K-Bit CMOS E²PROM

FEATURES

- 3.0V to 3.6V Supply
- Read Access Times:
  - 250/300/350ns
- Low Power CMOS Dissipation:
  - Active: 8 mA Max.
  - Standby: 100 µA Max.
- Simple Write Operation:
  - On-Chip Address and Data Latches
  - Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time:
  - 5ms Max.
- Commercial and Industrial Temperature Ranges
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - 1 to 32 Bytes in 5ms
  - Page Load Timer
- End of Write Detection:
  - Toggle Bit
  - $\overline{\text{DATA}}$ Polling
  - RDY/$\overline{\text{BUSY}}$
- Hardware and Software Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

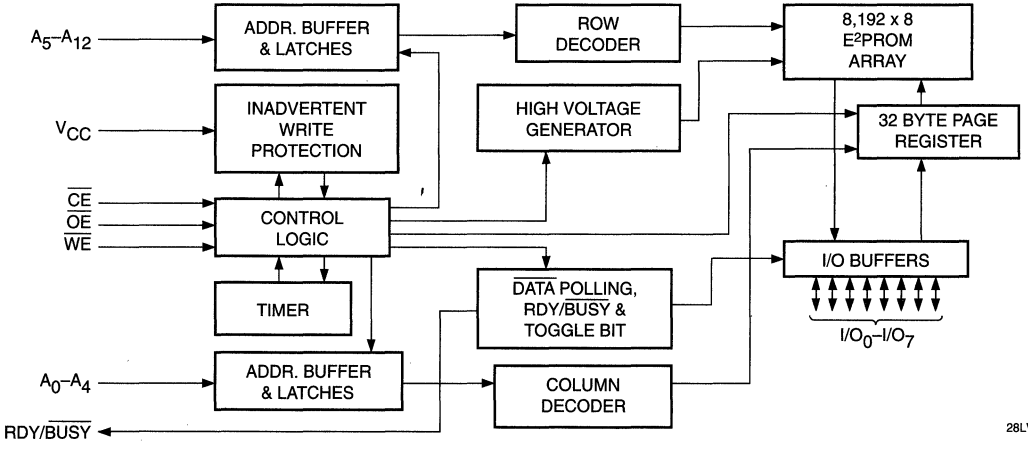
DESCRIPTION

The CAT28LV65 is a low voltage, low power, CMOS E²PROM organized as 8K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling RDY/$\overline{\text{BUSY}}$ and Toggle status bit signal the start and end of the self-timed write cycle. Additionally, the CAT28LV65 features hardware and software write protection.

The CAT28LV65 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, TSOP and SOIC or 32-pin PLCC and TSOP packages.

8

BLOCK DIAGRAM



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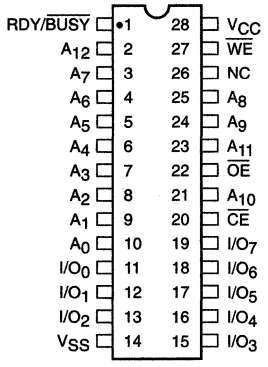
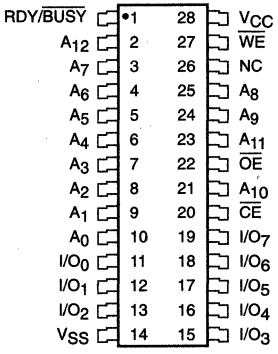
Characteristics subject to change without notice

PIN CONFIGURATION

DIP Package (P)



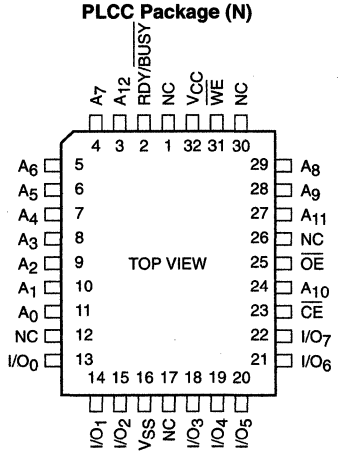
SOIC Package (J, K)



PIN FUNCTIONS

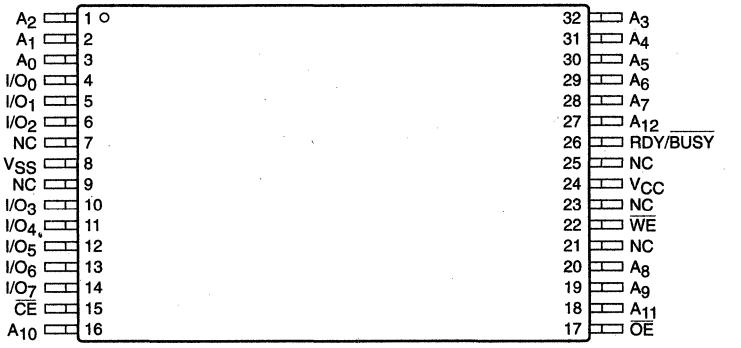
Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	3.0 to 3.6 V Supply
V_{SS}	Ground
NC	No Connect
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status

PLCC Package (N)



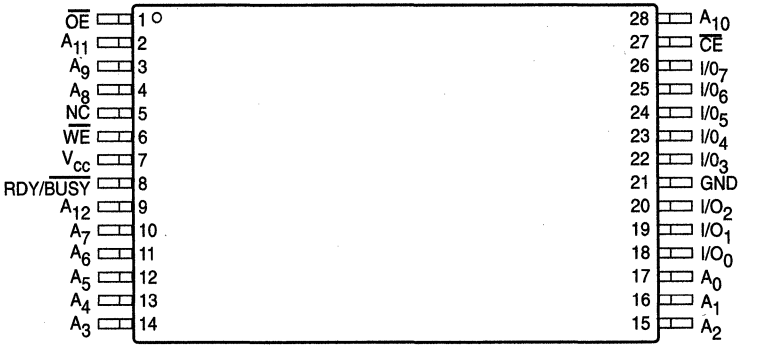
28LV65 F02

TSOP Top View (8mm x 14mm) (T14)
TSOP Top View (8mm x 20mm) (T)



28LV65 F03

TSOP Top View (8mm x 13.4mm) (T13)



28LV65 F04

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Operating, TTL)			8	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{SBC}(1)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–5		5	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(1)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}	Low Level Input Voltage	–0.3		0.6	V	
V_{OH}	High Level Output Voltage	2			V	I_{OH} = –100µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 1.0mA
V_{WI}	Write Inhibit Voltage	2			V	

Note:
(1) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

8

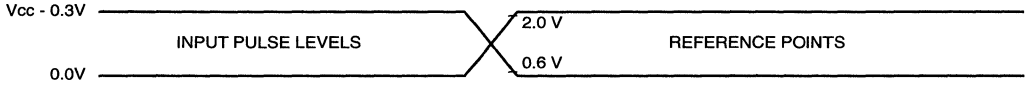
A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

		28LV65-25		28LV65-30		28LV65-35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	250		300		350		ns
t_{CE}	$\overline{CE}$ Access Time		250		300		350	ns
t_{AA}	Address Access Time		250		300		350	ns
t_{OE}	$\overline{OE}$ Access Time		100		150		150	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		55		60		60	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		55		60		60	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

Figure 1. A.C. Testing Input/Output Waveform(1)



Note:
(1) Input rise and fall times (10% and 90%) < 10 ns.

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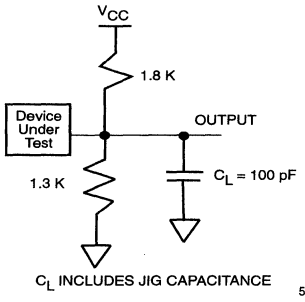
Figure 2. A.C. Testing Load Circuit (example)



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A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified.

Symbol	Parameter	28LV65-25		28LV65-30		28LV65-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	100		100		100		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(3)	Byte Load Cycle Time	0.1	100	0.1	100	0.1	100	µs
t_{RB}	$\overline{WE}$ Low to RDY/$\overline{BUSY}$ Low		220		220		220	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

Read

Data stored in the CAT28LV65 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle

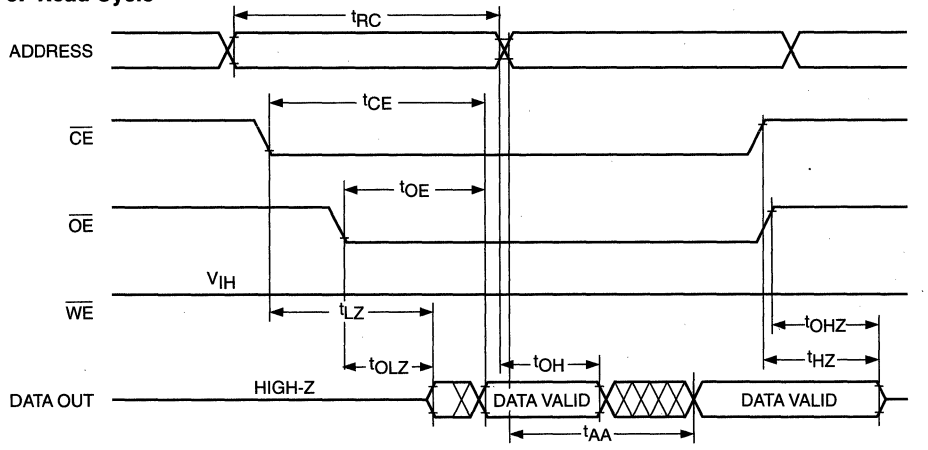
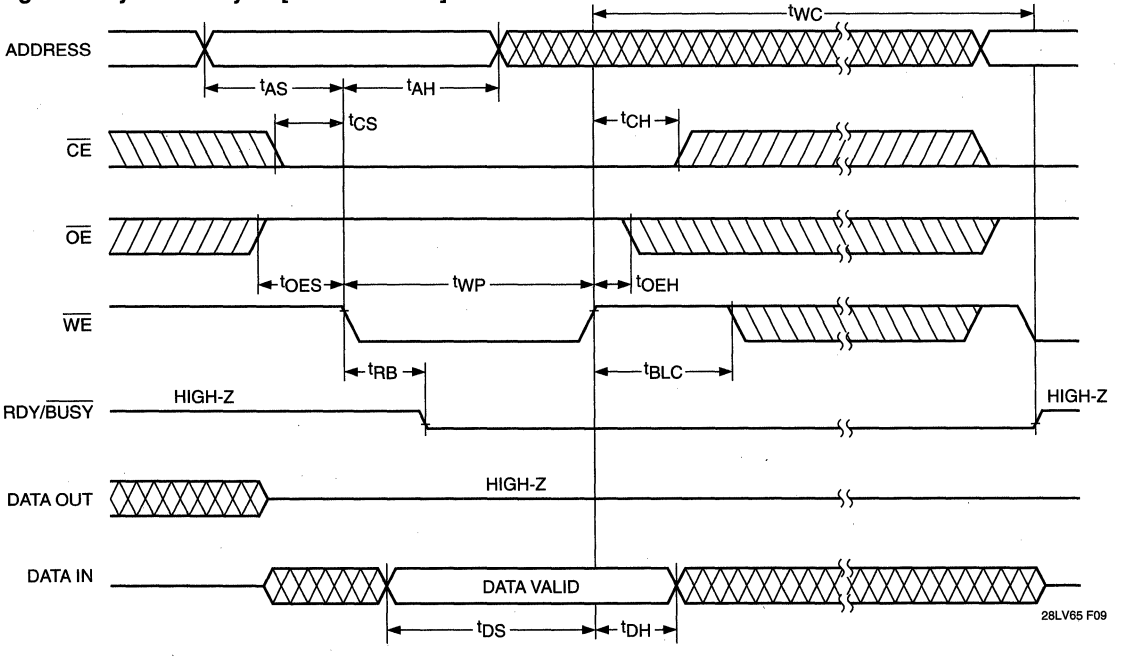


Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



Page Write

The page write mode of the CAT28LV65 (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

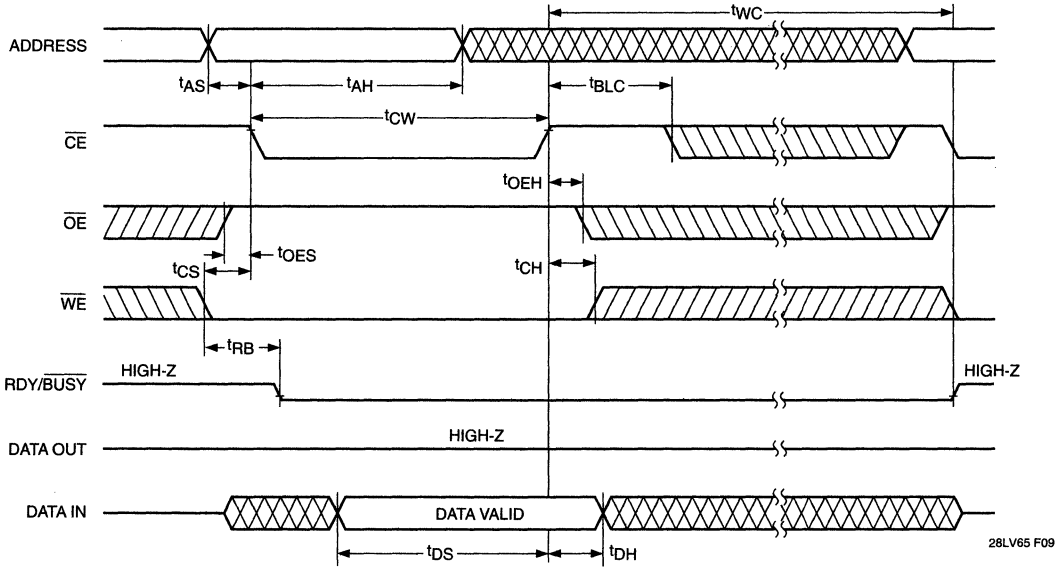
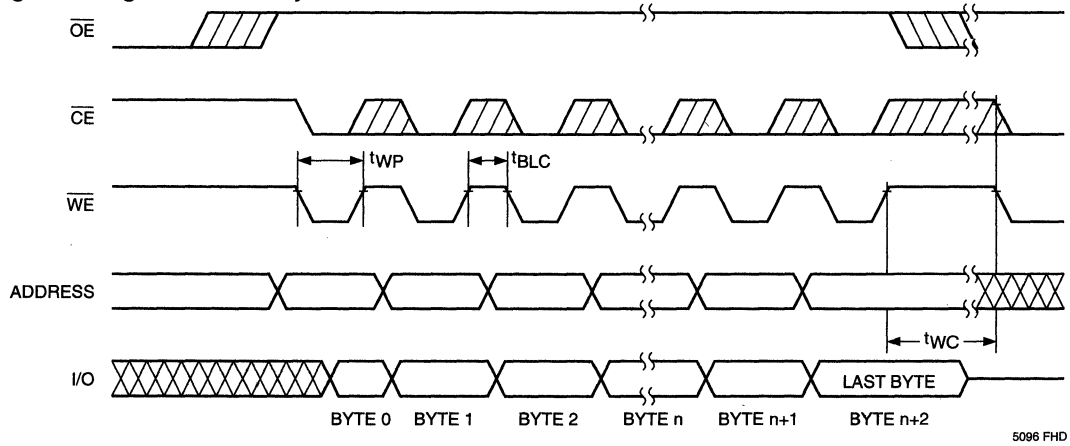


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Ready/$\overline{\text{BUSY}}$ (RDY/$\overline{\text{BUSY}}$)

The RDY/$\overline{\text{BUSY}}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{\text{BUSY}}$ line.

Figure 7. $\overline{\text{DATA}}$ Polling

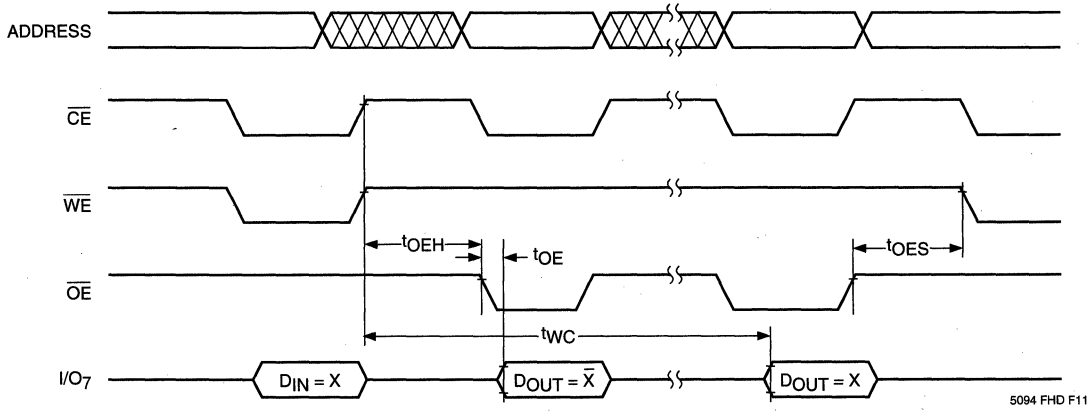
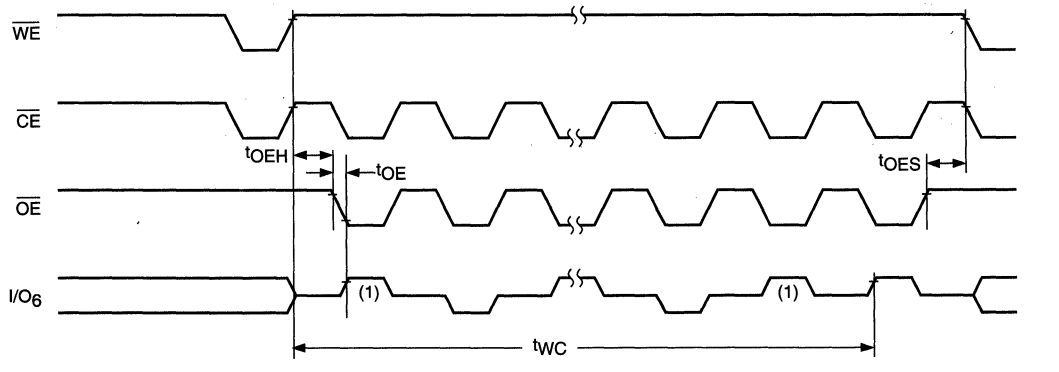


Figure 8. Toggle Bit



Note:
(1) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28LV65.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 2.40V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28LV65 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28LV65 is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

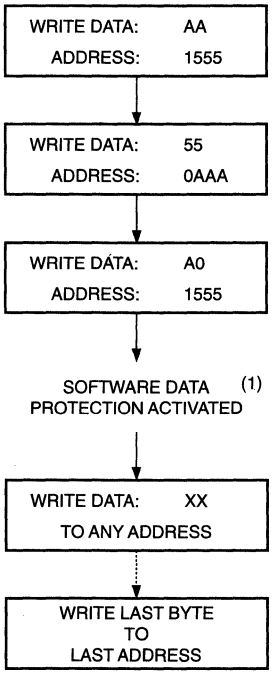


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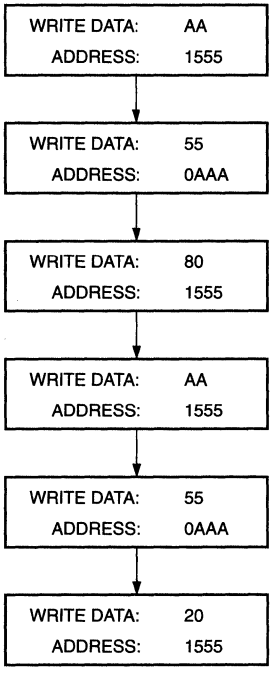
Figure 10. Write Sequence for Deactivating Software Data Protection



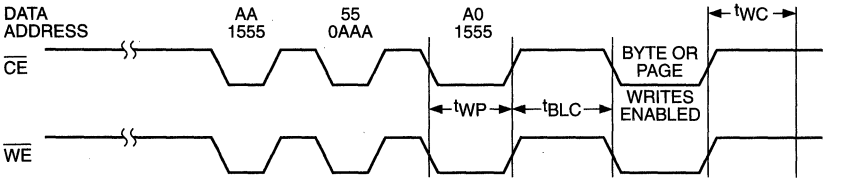
5094 FHD F09

Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

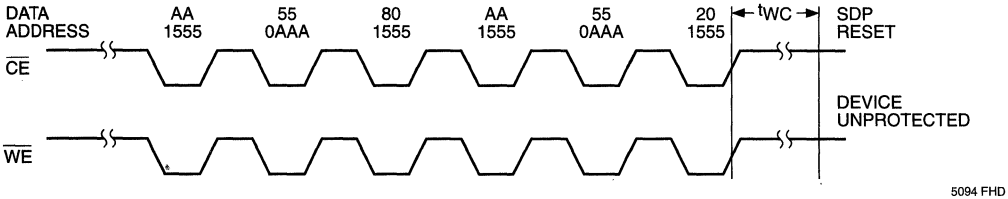
To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing



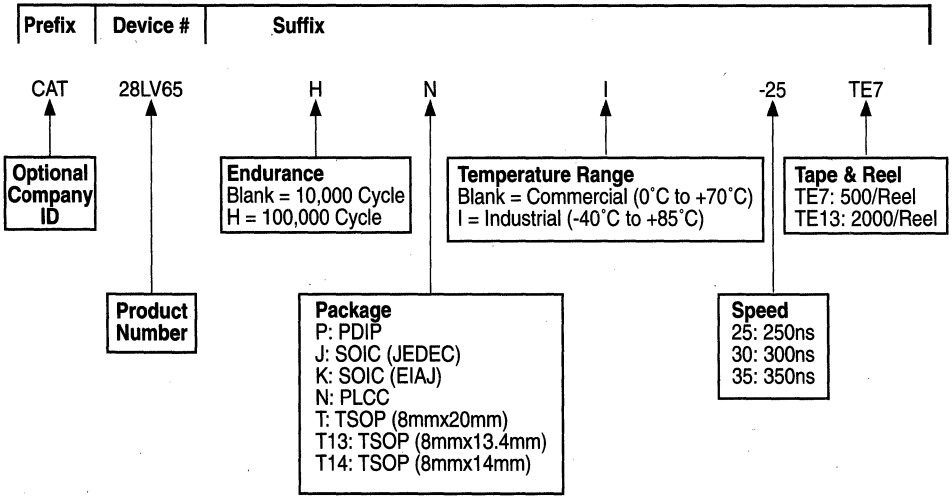
5094 FHD F13

Figure 12. Resetting Software Data Protection Timing



5094 FHD F14

ORDERING INFORMATION



28LV65 F17

Notes:
(1) The device used in the above example is a CAT28LV65HNI-25TE7 (100,000 Cycle Endurance, PLCC, Industrial temperature, 250 ns Access Time, Tape & Reel).

CAT28LV256

256K-Bit CMOS E²PROM

FEATURES

- 3.0V to 3.6V Supply
- Read Access Times: 250/300/350 ns
- Low Power CMOS Dissipation:
  - Active: 8 mA Max.
  - Standby: 100 µA Max.
- Simple Write Operation:
  - On-Chip Address and Data Latches
  - Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time:
  - 10ms Max.
- Commercial and Industrial Temperature Ranges
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - 1 to 64 Bytes in 10ms
  - Page Load Timer
- End of Write Detection:
  - Toggle Bit
  - $\overline{\text{DATA}}$ Polling
- Hardware and Software Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

DESCRIPTION

The CAT28LV256 is a fast, low power, low voltage CMOS E²PROM organized as 32K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28LV256 features hardware and software write protection and an internal Error Correction Code (ECC) for extremely high reliability.

The CAT28LV256 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC-approved 28-pin DIP, 28-pin TSOP, 32-pin PLCC or 32-pin PLCC, and TSOP, packages.

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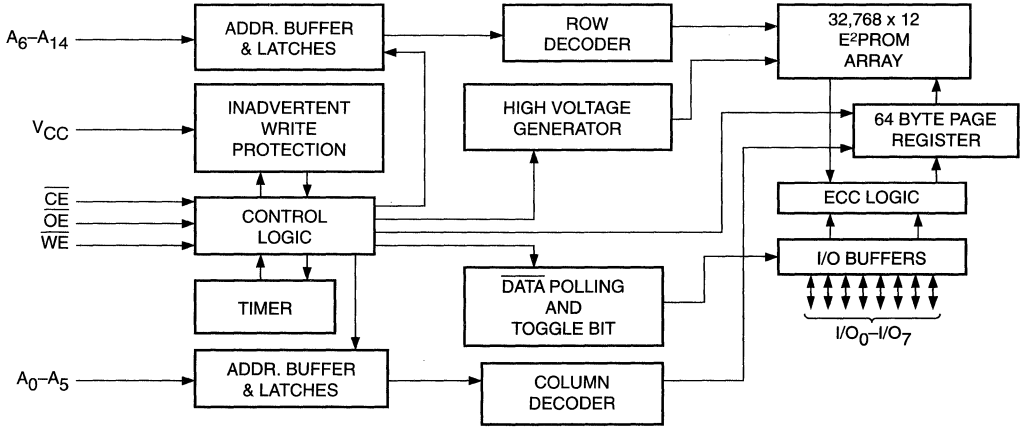
BLOCK DIAGRAM



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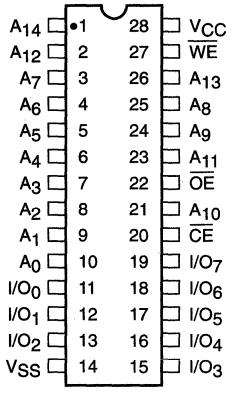
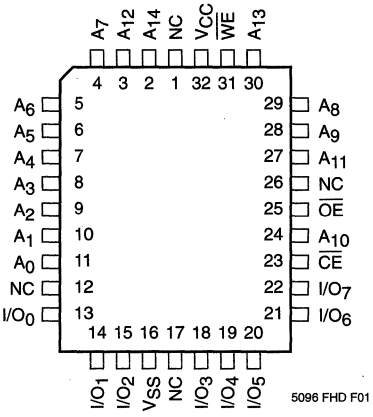
PIN CONFIGURATION

DIP Package (P)



PLCC Package (N)



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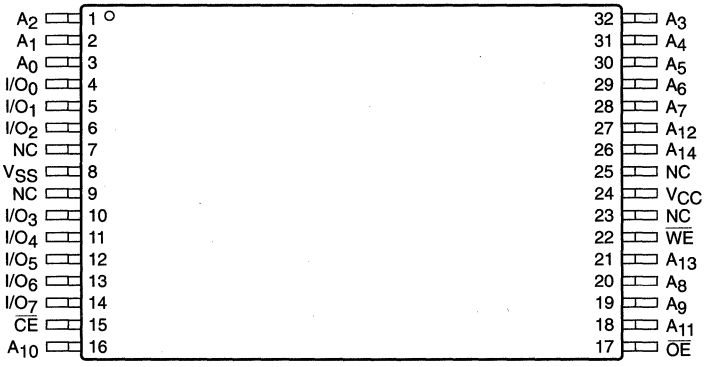
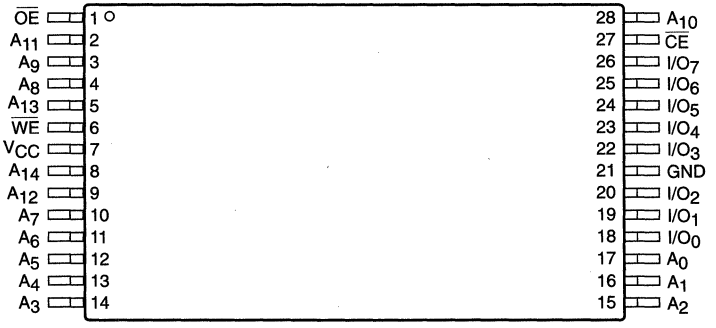
PIN FUNCTIONS

Pin Name	Function
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	3.0V - 3.6V Supply
V_{SS}	Ground
NC	No Connect

TSOP Top View (8mm X 14mm) (T14)



TSOP Top View (8mm X 13.4mm) (T13)



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CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10^4 or 10^5		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 3.0V to 3.6V, unless otherwise specified

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Operating, TTL)			15	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = $1/t_{RC}$ min, All I/O's Open
I_{SBC}(1)	V_{CC} Current (Standby, CMOS)			150	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–5		5	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(1)	High Level Input Voltage	2		V_{CC} +0.3	V	
V_{IL}	Low Level Input Voltage	–0.3		0.6	V	
V_{OH}	High Level Output Voltage	2			V	I_{OH} = –100µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 1.0mA
V_{WI}	Write Inhibit Voltage	2			V	

Note:
(1) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

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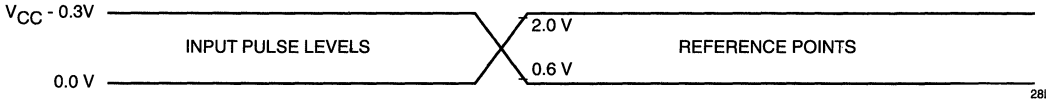
A.C. CHARACTERISTICS, Read Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified

		28LV256-25		28LV256-30		28LV256-35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	250		300		350		ns
t_{CE}	$\overline{CE}$ Access Time		250		300		350	ns
t_{AA}	Address Access Time		250		300		350	ns
t_{OE}	$\overline{OE}$ Access Time		100		110		110	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(2)	$\overline{CE}$ High to High-Z Output		55		60		60	ns
t_{OHZ}(1)(2)	$\overline{OE}$ High to High-Z Output		55		60		60	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

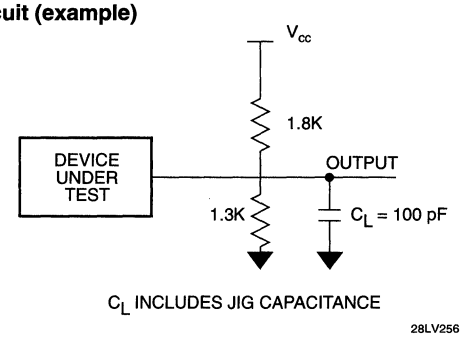
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

Figure 1. A.C. Testing Input/Output Waveform(1)



Note:
(1) Input rise and fall times (10% and 90%) < 10 ns.

Figure 2. A.C. Testing Load Circuit (example)



A.C. CHARACTERISTICS, Write Cycle

V_{CC} = 3.0V to 3.6V, unless otherwise specified

		28LV256-25		28LV256-30		28LV256-35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW}(2)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	0		0		0		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		0		0		ns
t_{WP}(2)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(3)	Byte Load Cycle Time	0.15	100	0.15	100	0.15	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) A write pulse of less than 20ns duration will not initiate a write cycle.
(3) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

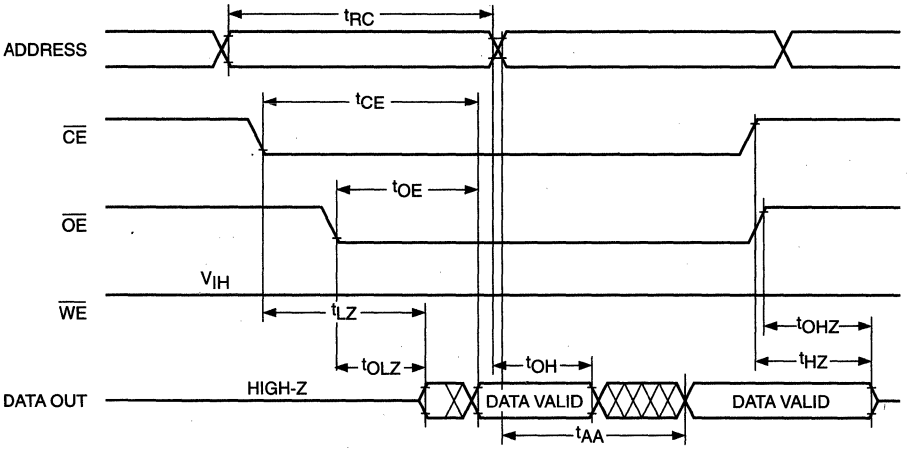
Read

Data stored in the CAT28LV256 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

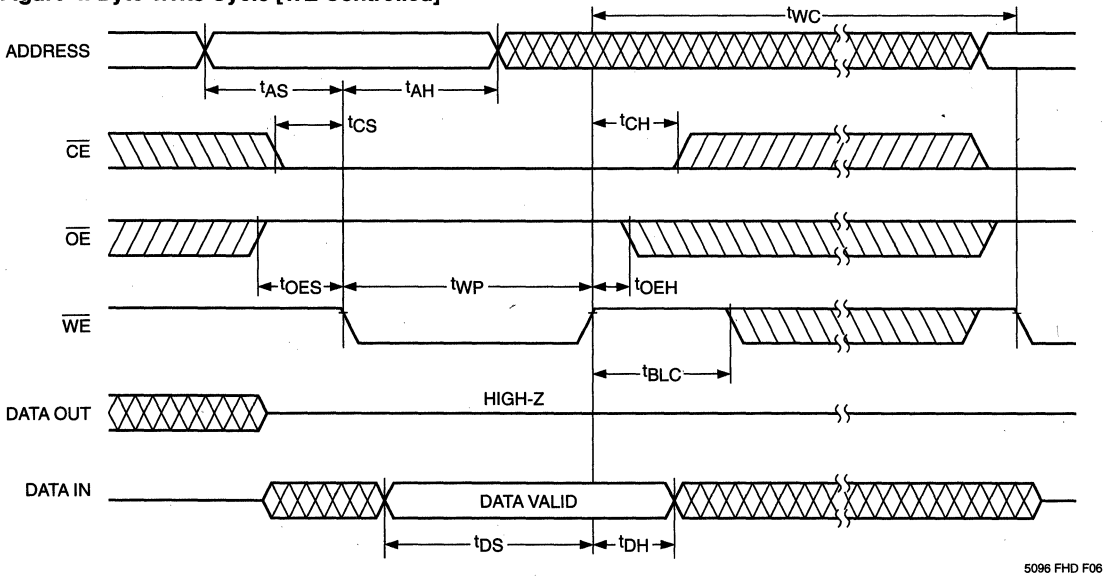
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

Figure 3. Read Cycle



28LV256 F06

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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Page Write

The page write mode of the CAT28LV256 (essentially an extended BYTE WRITE mode) allows from 1 to 64 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 64.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 64 byte temporary buffer. The page address where data is to be written, specified by bits A_6 to A_{14}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_5 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

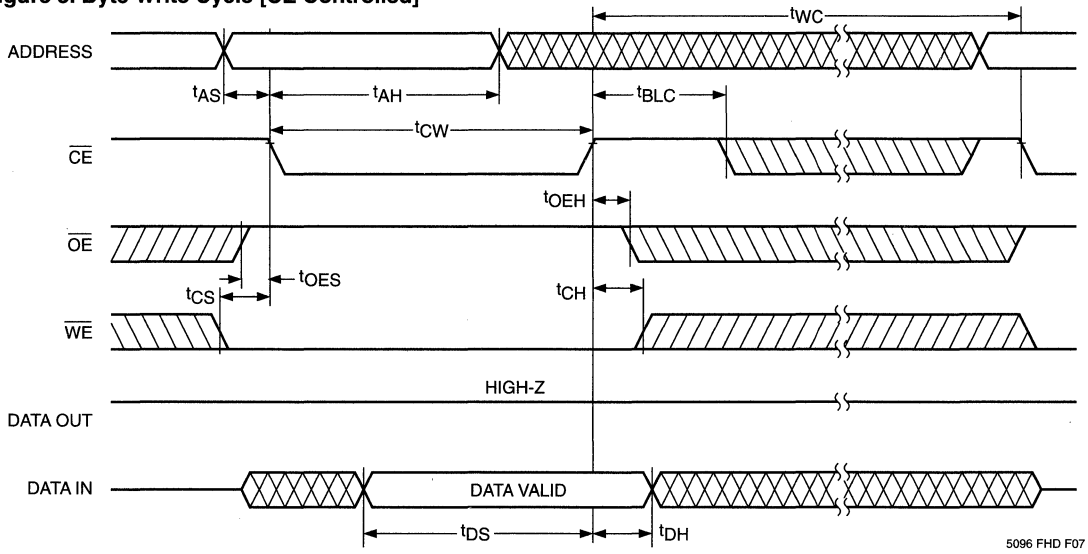
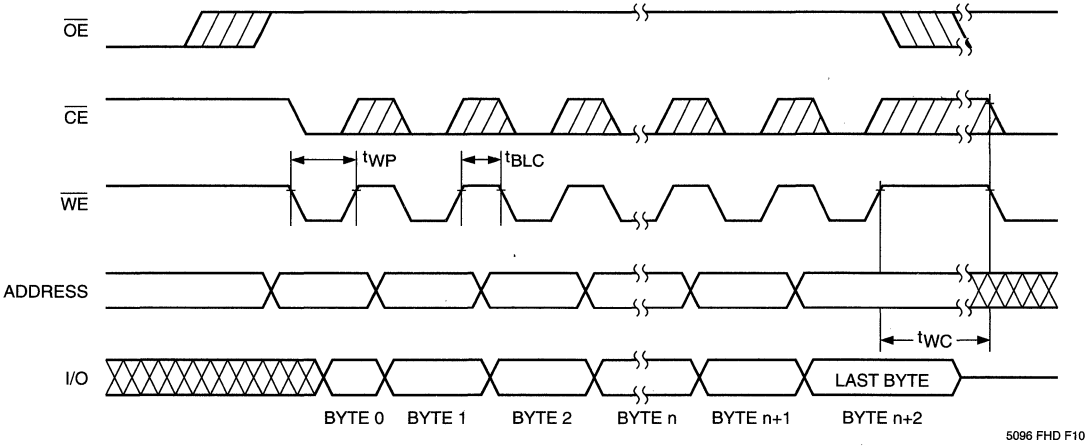


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device can determine the completion of a write cycle, while a write cycle is in progress, by reading data from the device. This results in I/O_6 toggling between one and zero. Once the write is complete, however, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling

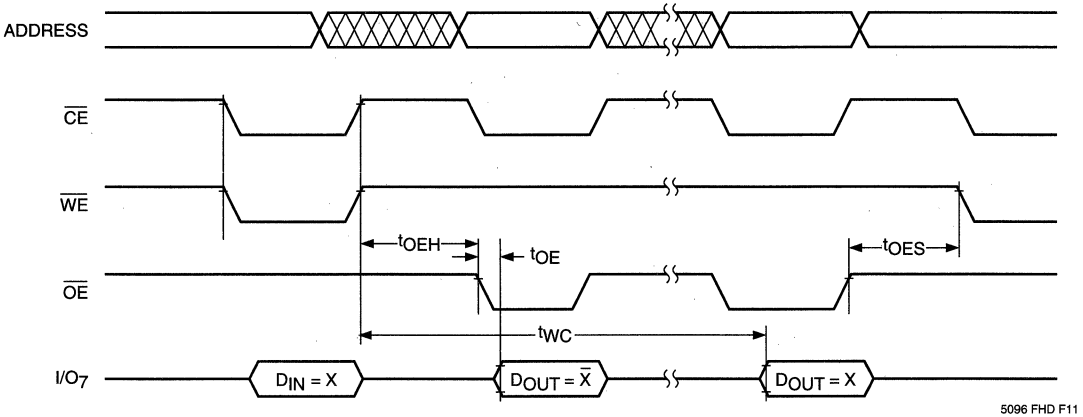


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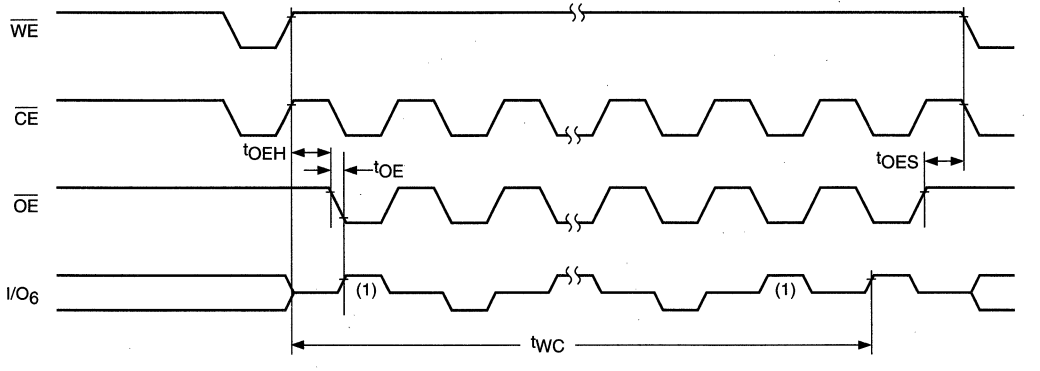
Figure 8. Toggle Bit



28LV256 F11

Note:
(1) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following hardware data protection features are incorporated into the CAT28LV256.

(1) V_{CC} sense provides write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 2.4V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28LV256 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28LV256 is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

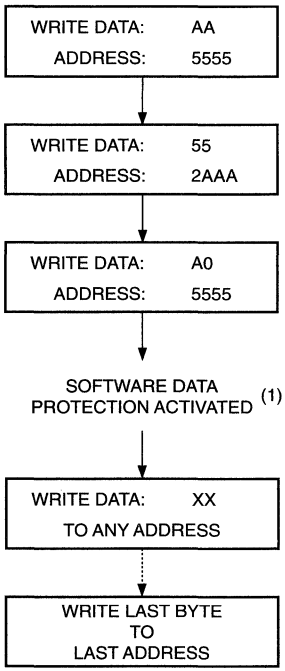


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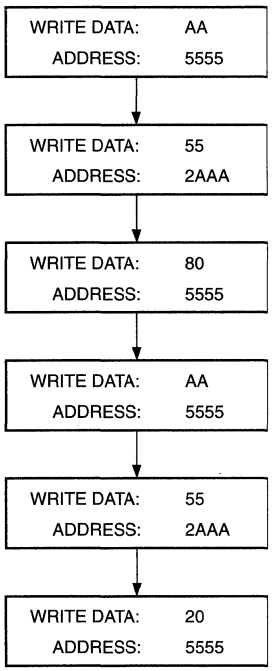
Figure 10. Write Sequence for Deactivating Software Data Protection



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Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

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To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued, regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

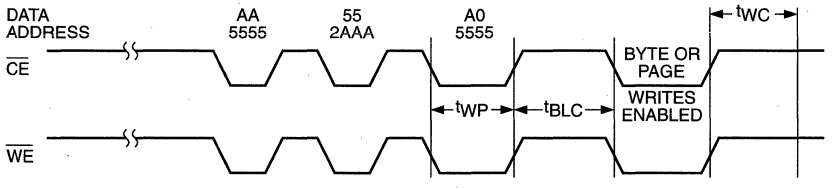

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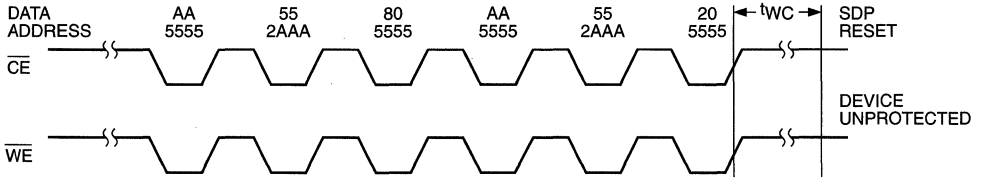
Figure 12. Resetting Software Data Protection Timing



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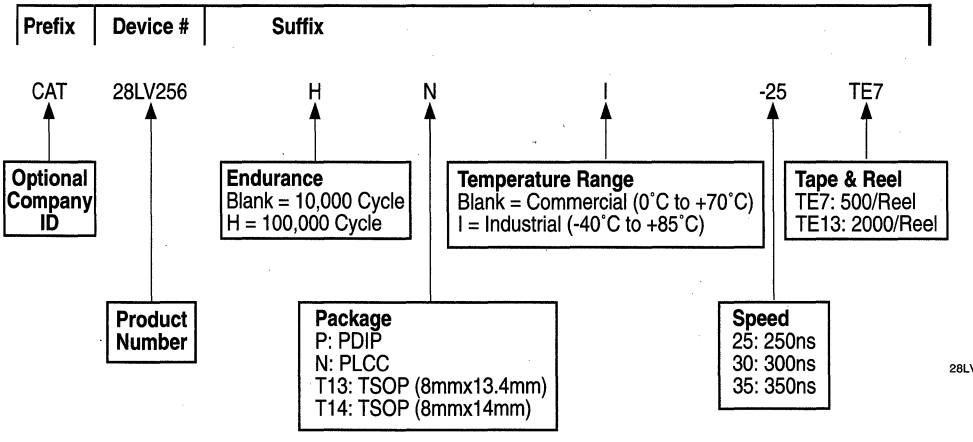
ORDERING INFORMATION



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Notes:
(1) The device used in the above example is a CAT28LV256HNI-25TE7 (100,000 Cycle Endurance, PLCC, Industrial temperature, 250 ns Access Time, Tape & Reel).

Product Information 1
I²C Bus Serial E²PROMs 2
Microwire Bus Serial E²PROMs 3
SPI Bus Serial E²PROMs 4
Secure Access Serial E²PROMs 5
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CAT504 ..... 8-Bit Quad DACpot 9-13

CAT505 ..... 8-Bit Quad DACpot 9-25

CAT506 ..... 12 Bit, 40MHz D/A Converter 9-37

CAT104/105

12 Bit, 25MHz D/A Converter

FEATURES

- 40 ns maximum settling time (1/2 LSB)
- 25 MHz update rate
- 1/2 LSB Integral Non-Linearity
- 1/2 LSB Differential Non-Linearity
- 25 ppm/ºC internal voltage reference
- Low Power BiCMOS construction
- Single Supply operation (+5 V)

APPLICATIONS

- Arbitrary Waveform Generators
- Direct Digital Synthesis (DDS)
- High Resolution A/D Converters
- Automatic Test Equipment
- High Definition Video

DESCRIPTION

The CAT104 and CAT105 are monolithic 12-bit current output D/A converters designed for precision high speed data conversion applications. Powered from a single +5 Volt supply the CAT104 and CAT105 will source 40 mA of current into a 25 Ohm load at clock speeds of 25 MHz while maintaining 1/2 LSB accuracy. Settling time is 40 ns to .012% of Full Scale.

Fabricated in a 2.0 micron BiCMOS process, the CAT104 and CAT105 incorporate on-chip EEPROM driven trim circuitry for factory correction of all silicon and package induced errors. Gain error is adjusted to below <0.2 % and linearity to .012 %. Monotocity is guaranteed over the full operating temperature range. The CAT104 and CAT105 include an on-chip voltage reference which is EEPROM trimmed to achieve a typical drift with temperature of 25 ppm/°C.

Data interface is via a 12 bit parallel bus and directly accesses the D/A in the CAT104, while the CAT105 provides a clocked data input register.

The CAT104 and CAT105 are pin compatible with Brooktree's Bt 104 & Bt 105 while offering improved performance. The device is available in 24-pin Ceramic DIP package.

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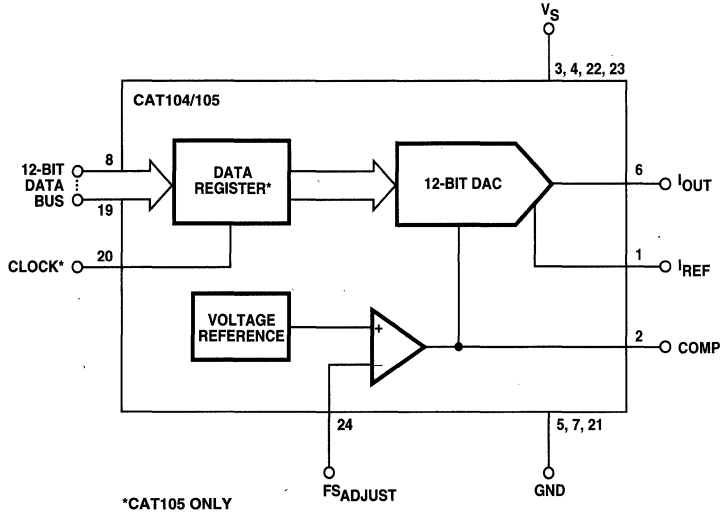
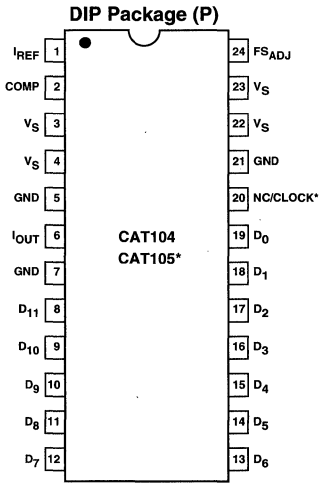
FUNCTIONAL DIAGRAM



PIN CONFIGURATION



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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
- V_S to GND ..... −0.5V to +7V

Inputs
- D_0-D_{11} to GND ..... −0.5V to V_S +0.5V
- FS_{ADJUST} to GND ..... −0.5V to V_S +0.5V
- COMP to GND ..... −0.5V to V_S +0.5V
- CLOCK to GND ..... −0.5V to V_S +0.5V
- I_{REF} ..... ±10 mA

Outputs
- Analog Output Current (I_{OUT}) ..... 50 mA
- Analog Output Voltage (I_{OUT}) ... V_S^- 7V to V_S^+ 0.5V
- Analog Output Short Circuit Duration ..... Infinite

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C

Storage Temperature ..... −65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions if NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from −1V to V_{CC} + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = +5V ±0.25V; I_{OUT} (FS) = 40mA, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Resolution			12	—	—	Bits
Accuracy						
INL	Integral Linearity Error	CAT104A/105A	—	—	±1/2	LSB
		CAT104B/105B	—	—	±1	LSB
DNL	Differential Linearity Error		—	—	±1/2	LSB
	Zero Offset Error		—	—	1	µA
	Gain Error	Internal Reference	—	±0.15	±0.3	%FS
		External Reference	—	—	±1	%FS
	Monotocity		Guaranteed			
Coding						
	I_{OUT}	D_0-D_{11} = 0	0	—	—	
	I_{OUT}	D_0-D_{11} = 1	—	—	Full Scale	
Data Inputs						
V_{IH}	High Level Input Voltage		2	—	—	V
V_{IL}	Low Level Input Voltage		—	—	0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V	—	—	1	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	—	—	−1	µA
Analog Output						
I_{OUT}	Output Current		10	—	40	mA
V_{OUT}	Output Compliance		−1	—	+1	V
R_{OUT}	Output Impedance		—	1	—	MΩ
Reference						
$I_{REF\ (Pin\ 1)}$	Operating Voltage Range		−0.3	0.68	1	V
V_{REF}	Internal Reference Voltage		0.67	0.68	0.69	V
TC_{VREF}	Temperature Coefficient		—	25	—	ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont.): V_S = +5V ±0.25V; I_{OUT} (FS) = 40mA, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Supply						
V_S	Supply Voltage Range		4.5	5	6	V
I_S	Supply Current	25 MHz, I_{OUT} = 40 mA	—	60	75	mA
PSRR	Power Supply Rejection Ratio	COMP = 0.01 µF, f = 1 kHz	—	0.02	0.5	%/%ΔV_S

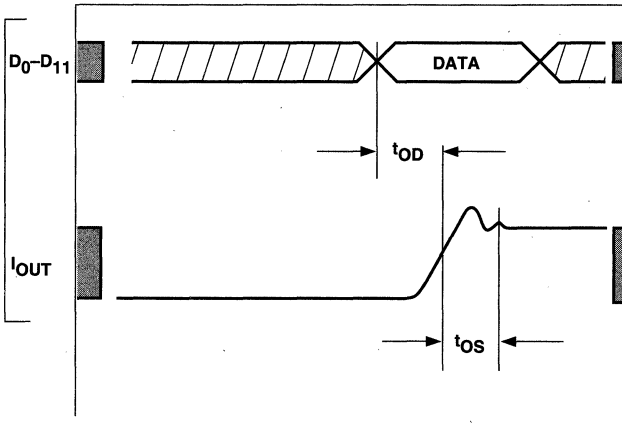
AC ELECTRICAL CHARACTERISTICS: V_S = 5V ±0.25V; R_L = 25Ω; I_{OUT} (FS) = 40 mA.
Logic inputs: 0V-3V; t_r and t_f< 3 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Data Inputs						
f_{MAX}	Register Clock Rate		—	—	25	MHz
t_{CC}	Clock Cycle Time		40	—	—	ns
t_{PWH}	Clock Pulse Width High Time		10	—	—	ns
t_{PWL}	Clock Pulse Width Low Time		10	—	—	ns
t_{DS}	Data Setup Time		10	—	—	ns
t_{DH}	Data Hold Time		2	—	—	ns
	Pipeline Delay	CAT105 Only	1	1	1	Clock
Analog Output						
t_{OD}	Output Delay		—	25	—	ns
t_R	Output Rise Time		—	8	—	ns
t_F	Output Fall Time		—	8	—	ns
t_{OS}(1)	Output Settling Time	To 0.012% of FS	—	30	40	ns
		To 0.025% of FS	—	20	40	ns
		To 0.10% of FS	—	15	—	ns
	Clock and Data Feedthrough(1)		—	– 40	—	dB
	Glitch Impulse(1)		—	100	—	pV-sec
	Differential Gain Error		—	1.5	—	%FS
	Differential Phase Error		—	1.5	—	Degrees
Pin Capacitance						
C_{IN}	Input Capacitance, D_0-D_{11}, CLK	V_{IN} = 2.4V, f = 1 MHz	—	10	—	pF
C_{OUT}	Output Capacitance, Pin 6	I_{OUT} = 0 mA, f= 1 MHz	—	25	—	pF

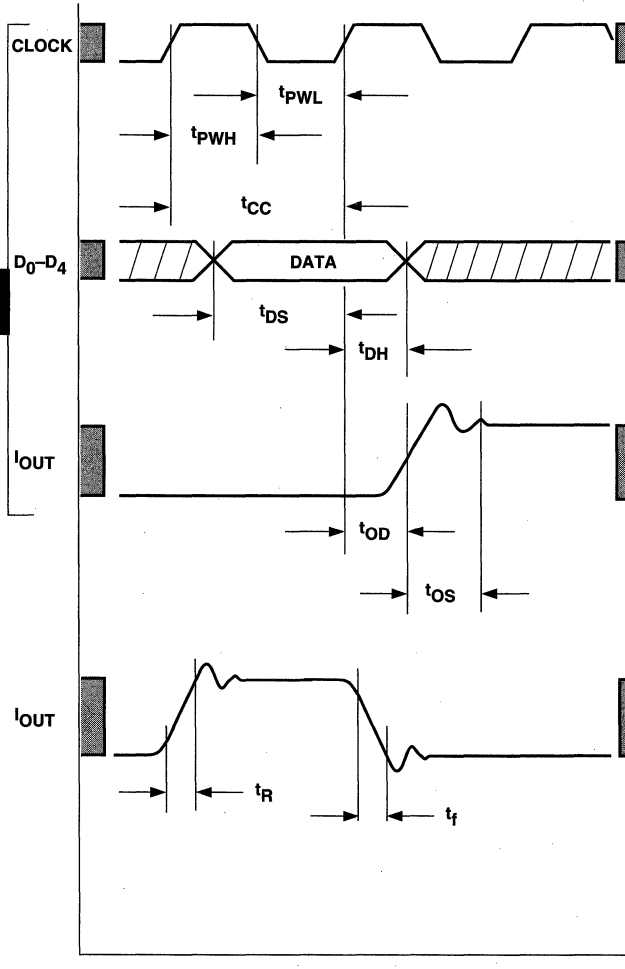
NOTES: 1. Clock and Data feedthrough is function of the magnitude of overshoot and undershoot on the digital inputs. While testing, the digital inputs have a 1k ohm resistor connected to the regular PCB ground plane and are driven by 74 HC logic. Clock and data feedthrough are excluded from the settling time, where as they are included in glitch impulse. (Test bandwidth = 50 MHz.)

AC TIMING DIAGRAM

CAT104



CAT105



PARAMETER NAME	MEASURED FROM	MEASURED TO	MIN MAX
t_{OD}	FROM:	Data Valid	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	
t_{PWL}	FROM:	50% point of falling edge	Min
	TO:	50% point of rising edge	
t_{PWH}	FROM:	50% point of rising edge	Min
	TO:	50% point of falling edge	
t_{CC}	FROM:	50% point of rising edge	Min
	TO:	50% point of next rising edge	
t_{DS}	FROM:	Data valid	Min
	TO:	50% point of clock's next rising edge	
t_{DH}	FROM:	End of t_{DS} period	Min
	TO:	data invalid	
t_{OD}	FROM:	50% point of clock's rising edge	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	
t_R	FROM:	10% point of FS output	Max
	TO:	90% point of FS output	Max
t_F	FROM:	90% point of FS output	
	TO:	10% point of FS output	

Pin Descriptions

Pin No.	Name	Function
1	I_{REF}	Reference Current Output. The DAC's full scale output current is set by I_{REF}, which is normaly connected to FS_{ADJUST} and a resistor, R_{SET}. The full scale output current is then determined by the value of R_{SET}.
2	COMP	Compensation pin. This pin must be connected to the V_S pin through a ceramic capacitor. This capacitor provides power supply noise rejection and reduces the random noise of the internal bandgap reference. The capacitor can be between 0.01 µF and 0.1 µF, with 0.01µF being the recommended value. When an external reference voltage is used COMP is used in conjunction with FS_{ADJUST} to set I_{REF}.
3, 4, 22, 23	V_S	The positive supply voltage, nominally +5V.
5, 7,21	GND	Ground return for all signals (digital and analog) and V_S.
6	I_{OUT}	Analog Current Output. This high impedance current source is capable of sourcing up to 40 mA of current.
8-19	D_0-D_{11}	TTL compatible Data Inputs. Pin D_0 is the least significant data bit. For CAT105, the inputs are latched on the rising edge of clock. All unused inputs must be tied to V_S or GND.
20	Clock or N/C	Clock Input for CAT105. The rising edge of Clock latches the D_0-D_{11} inputs. Ideally, this pin should be driven by a dedicated TTL/CMOS buffer. This pin is not used on CAT104 and may be left floating without affecting performance.
24	FS_{ADJUST}	Full Scale Adjust Control. When the internal reference voltage is used, the full scale output current is controlled by the resistor R_{SET}, connected between this input pin and GND. When an external voltage reference is used, FS_{ADJUST} is tied to V_S.

TERMS AND DEFINITIONS

Differential Non-Linearity (DNL): The maximum deviation from an ideal LSB step, between any two adjacent output levels. A DNL error more negative than -1 LSB implies non-monotonic output performance.

Full Scale Output Current: The output current at I_{out} resulting from all 1's at the data inputs.

Gain Error: The variation in the slope (gain) of the transfer function of a converter with respect to an established ideal transfer function. This error is expressed in % of FS (Full Scale) or LSB, when all bits are on, and may be eliminated by adjusting the reference current applied to the device.

Glitch Impulse Area: The analog output transient occurring between two adjacent codes as a result of unequal turn-on and turn-off times for the internal current sources. Glitch impulse is calculated as the area of the largest excursion, about the final value, and is specified as the net area of the glitch in nV-sec or pA-sec.

Integral Non-Linearity (INL): The maximum deviation between the actual output level and a best straight line fit. This excludes gain and offset errors.

Least-Significant Bit (LSB): The ideal output increment between two adjacent codes. Also, the data bit with the smallest effect on the output level.

Monotonicity: Implies that for an increase in digital code value that the output will either increase or remain unchanged. In mathematical terms the output is a single valued function of the input code, and the derivative of the output transfer function must not change signs.

Most-Significant Bit (MSB):The data bit with the largest effect on the output level. The MSB, for a linear DAC output, ideally equals the combined output weight of all other data bits, plus 1 LSB.

Offset Error: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

Output Compliance Range: The output voltage range over which a stated linearity specification is maintained. Integral linearity errors tend to be exaggerated with increasing output voltage levels.

Settling Time :The time from an initial full-scale output level change to the point where the output level is less than -1/2 LSB from its final value, for a full-scale step transition.

CURRENT VS VOLTAGE OUTPUT

The CAT104/105 has been carefully designed to work equally well in both current and voltage output applications, a claim not all DACs can make. When using other DACs, designers may be forced to use additional circuitry or be obliged to accept reduced performance when voltage output is required.

High speed DACs give their best performance in current output mode. This is because in current output operation the DAC's output is tied to a summing junction, such as the negative input of an op amp, and feedback around the op amp holds the junction voltage constant (usually 0 volts). Since no voltage change occurs at the DAC's output of the DAC is uneffected by load resistance, R_L, or any other impedances internal or external to the DAC.

When generating a voltage output, however, R_L can have a significant effect on the DAC's performance. The problem is caused by the DAC's own output impedance. As shown in Fig1 a DAC's output can be modeled as a current source in parallel with an internal resistance. When an external load is connected to I_{OUT}, it is in parallel with the internal resistance and the actual load seen by the DAC is the combination of their values. In developing an output voltage, I_{OUT} is split between internal and external loads, producing an apparent error in V_{OUT}. The degree of error is determined by the ratio of R_L to the internal shunt resistance. For ideal current sources the shunt resistance is infinite, but in typical high speed DACs it ranges from 200 to 20,000 Ω. This will produce a significant loading effect, even with the 50 Ω or 25 Ω loads commonly used in high speed systems.

To combat this problem, Catalyst has taken special care to create a true current source output structure for the CAT104/105. The CAT104/105's 1 MΩ output impedance frees designers from concerns about voltage induced errors and voltage outputs can be had with no penalty in performance.

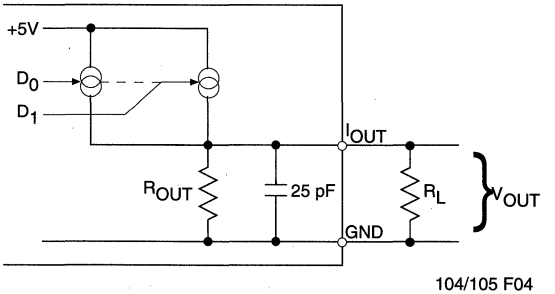


Figure 1. DAC Output Equivalent Circuit

OUTPUT VOLTAGE COMPLIANCE

The maximum voltage that may be realized at the DAC's output, while maintaining rated accuracy and performance, is 1.0 Volts. Care should be taken when selecting R_L and I_{OUT} that the resulting Full Scale voltage does not exceed this value. Also, when operating into a summing junction (current mode), be sure the DC voltage of the summing node is below 1.0 volts.

BUFFERED VOLTAGE OUTPUTS

For applications requiring output voltages greater than 1.0 volts a buffering amplifier will be required. Figure 2 illustrates a typical buffered output application.

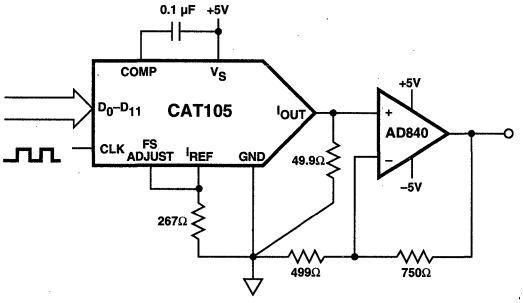


Figure 2. Buffer Voltage Output 0 to +2.5V

FULL SCALE ADJUST

The CAT104/105's output can be adjusted for any desired level between 0–1.0V or 0–40 mA via the FS_{ADJUST} pin. Referring to Figure 3, I_{REF}, which sets the DAC's Full Scale output current, is controlled by op amp A1. The control loop is configured so that A1 will maintain a constant 0.68 volts at the FS_{ADJUST} pin. As I_{REF} has a maximum compliance voltage of 1.0 Volts, it is best to use R_{TRIM} as a variable resistor in series with R_{SET} and tie FS_{ADJUST} directly to I_{REF}. This avoids the possibility of the voltage across the combination of $R_{TRIM}$and R_{SET} exceeding I_{REF}'s compliance range.

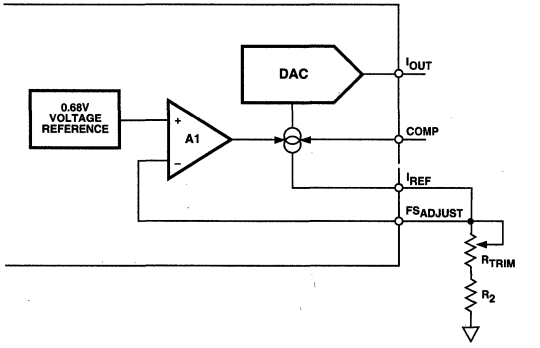


Figure 3. FS_{ADJUST} Equivalent Circuit

USING THE INTERNAL VOLTAGE REFERENCE

A precision voltage reference is provided by the CAT104/105 to allow for easy adjustment and control of I_{REF}, which sets the DAC full scale output current, I_{OUT}. The relationship between I_{OUT} and I_{REF} is:

$$I_{OUT} = 7.892 * I_{REF}$$

R_{SET} is then calculated from the equation:

$$R_{SET} = \frac{7.892 * V_{REF}}{I_{OUT}}$$

Where $V_{REF} = 0.68$ V.

The internal reference is factory trimmed to compensate for variations in the transfer ratio of I_{REF} to I_{OUT}, making the full scale output voltage accurate to within 0.3% for the transfer function:

$$V_{OUT} = 5.367 * \frac{R_L}{R_{SET}}$$

Full scale output voltage variation from device to device will be ±0.3% when there is perfect tracking between the load and reference current resistors. For Catalyst performance, R_{SET} and R_L should be a trimmed resistor network with ratio tracking better than ±0.1% and temperature coefficient tracking better than 5 ppm/°C.

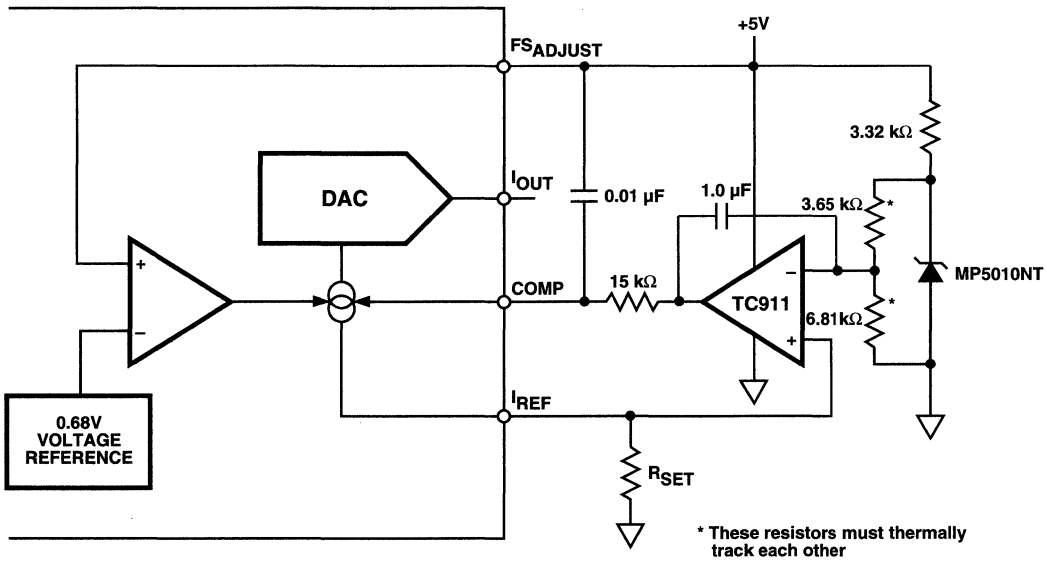


Figure 4a. External Voltage Reference, Single Supply

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USING AN EXTERNAL VOLTAGE REFERENCE

The precision voltage reference contained in the CAT104 and CAT105 is factory trimmed by EEPROM circuitry to guarantee a maximum temperature drift of 10 ppm/ºC. For most applications this is more than adequate, however, there may arise occasions when system requirements dictate that an external reference be used. In such cases the on-chip reference can be disabled and control of I_{REF} can be taken off chip.

When using an external reference, the control amplifier's offset and offset drift cannot be ignored. The D/A's output stability is dependent upon not only the reference but the control circuitry around it. For this reason it is recommended that the control amplifier be of the ultra low offset variety, typically < 25µV with a drift of less than 0.1 µV/ºC.

Figure 4a shows an example of the CAT104/105 being used with an external reference in a single supply application. In this circuit, a low drift 1.2 V bandgap reference has been chosen and its voltage divided to 0.8 V by a pair of resistors. This is done to insure that I_{REF} does not exceed its voltage compliance range. The op amp, a low drift chopper stabilized type, replaces the internal control amplifier, which has been de-activated by tying FS_{ADJUST} to the positive supply rail. Control of I_{REF} is effected through the COMP pin which adds an inversion to the control loop (I_{REF} current increases as V_{COMP} -> 0 V).

A simpler circuit can be used to incorporate an external voltage reference if a negative supply voltage is available, as shown in Figure 4b. Here, a precision -10V reference and R_{SET} combine with the CAT104/105's internal reference and amplifier to set and control I_{REF}. V_{REF} becomes the sum of the internal and external references, and R_{SET} is calculated from the equation

$$R_{SET} = 7.892 * \frac{V_{REF} + 0.68}{I_{OUT}}$$

Since V_{REF} is now the sum of the two references, a large value voltage is chosen for the external reference so that its characteristics will be dominant. Any noise or drift exhibited by the internal reference is now reduced in its effect by the ratio of the two reference voltages.

The internal reference is not precisely 0.68 V, as stated in the equation above, because it is factory adjusted to compensate for variations in the current transfer ratio of I_{OUT} to I_{REF}. To compensate for this, the external voltage reference can be offest by a corresponding amount using the Fine Adjustment feature. For references without this adjustment feature, R_{SET} can be trimmed instead.

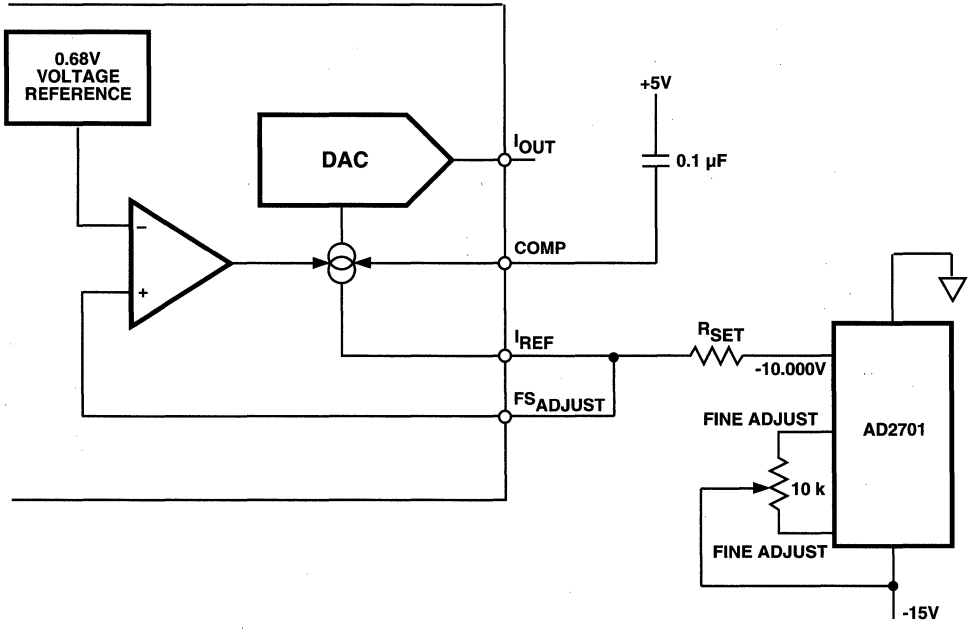
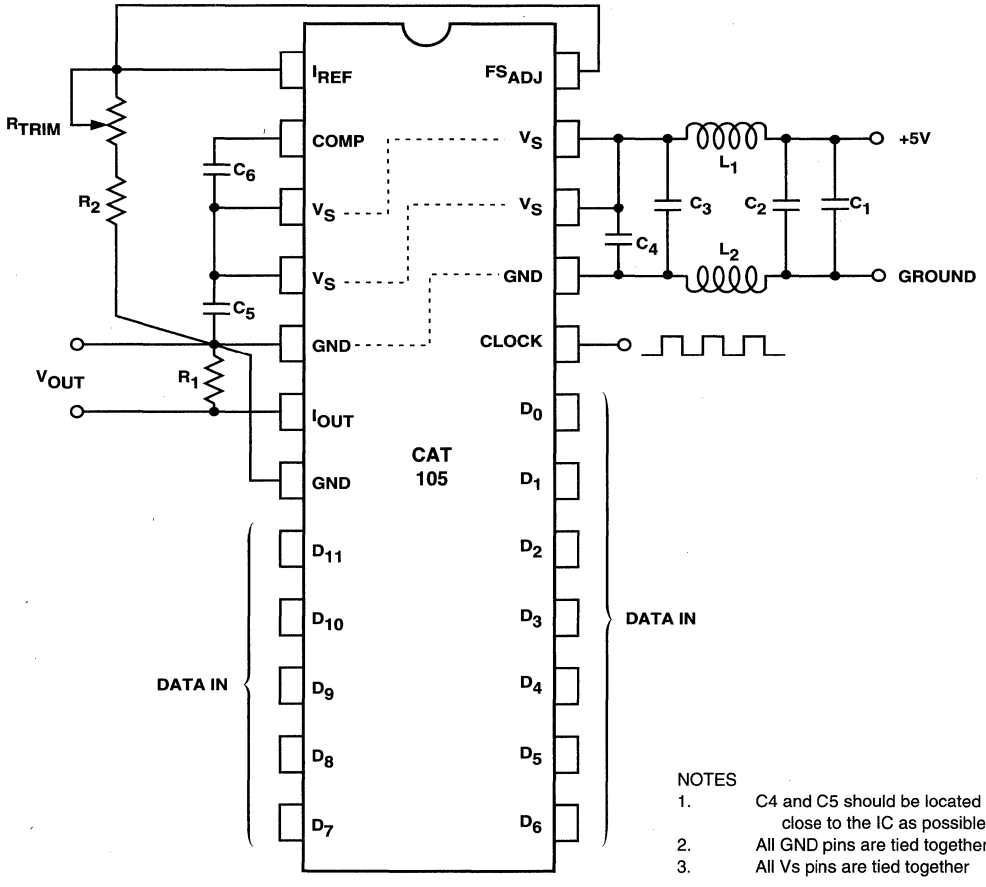


Figure 4b. External Voltage Reference, Dual Supply

SUPPLY DECOUPLING

It is essential to decouple the power and ground supply lines from the system's main power bus. This prevents glitches and noise spikes generated elsewhere in the system from getting into the DAC and showing up on its output.

Decoupling is best achieved through a filter network placed in series with the DAC's power supply lines. The filter is comprised of two inductors, one in each supply line , combined with several bypass capacitors. An example of this is shown in Figure 5.



COMPONENT	DESCRIPTION	SUPPLIER	PART NUMBER
C_6	0.1 µF Ceramic Capacitor	Erie	RPE112Z5U104M50V
C_2	0.01 µF Ceramic Capacitor	Erie	RPE110Z5U103M50V
C_4, C_5	0.01 µF Ceramic Chip Capacitor	Johanson Dielectrics	X7R500S41W103KP
C_1, C_3	22 µF Tantalum Capacitor	Mallory	CSR13G226KM
R_1	24.9Ω !% Metal Film Resistor	Dale	CMF-55C
L_1, L_2	Ferrite Bead	Fair-Rite	2743001111
R_2	121Ω 1% Metal Film Resistor	Dale	CMF-55C
R_{TRIM}	50Ω Cermet Trim Pot	Bourns	3386W

Figure 5. Typical Application: Unbuffered Voltage Output, 0–1V

SUPPLY CURRENT

The maximum supply current drawn by the CAT104/105 can be calculated from the equation:

I_S = Full Scale Output Current (in mA) + 1.2mA per MHz of operating speed.

P.C. BOARD LAYOUT

Combining high speed with high precision presents a formidable challenge to system designers. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding and measurement if Catalyst performance is to be realized.

BYPASS CAPACITORS

The most important external components associated with any high-speed design are the power supply bypass capacitors. Selection and placement of these capacitors is critical, and to a large extent, dependent upon the specifics of the system's configuration. The key consideration in selection of bypass capacitors is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and metal film capacitors generally feature lower series inductance than the tantalum or electrolytic types.

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Bypass capacitors should be installed on the printed circuit board as close to the IC as is physically possible, and with the shortest possible leads in order to minimize series lead inductance. Chip capacitors are optimal in this respect and thus highly recommended.

CRITICAL CONNECTIONS

In using the CAT104/105 it is of the utmost importance to be sure ***all*** V_S and GND pins are connected to to their respective supplies. Failure to do so will result in improper DAC operation, and may result in damage to the IC.

HIGH-SPEED INTERCONNECT

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. All connections should be short and direct and as physically close to the package as possible. Any conduction path shared by external components should be minimized. When runs exceed an inch or so in length, some type termination resistor may be required. This is true of both the analog and digital sections. For digital signals the termination resistor will be dependent upon the logic family used.

Ground planes should be connected at or near the DAC. Care should be taken to insure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the DAC output signal as well as the supply feeders. The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane.

For maximum AC performance, the DAC should be mounted directly to the circuit board; sockets should not be used as they increase lead inductance and capacitance. Any additional lead inductance or capacitance at the supply pins can seriously undermine dynamic performance. Even Teflon or "pin" sockets can create unwanted results, so soldering directly to the circuit board is highly recommended.

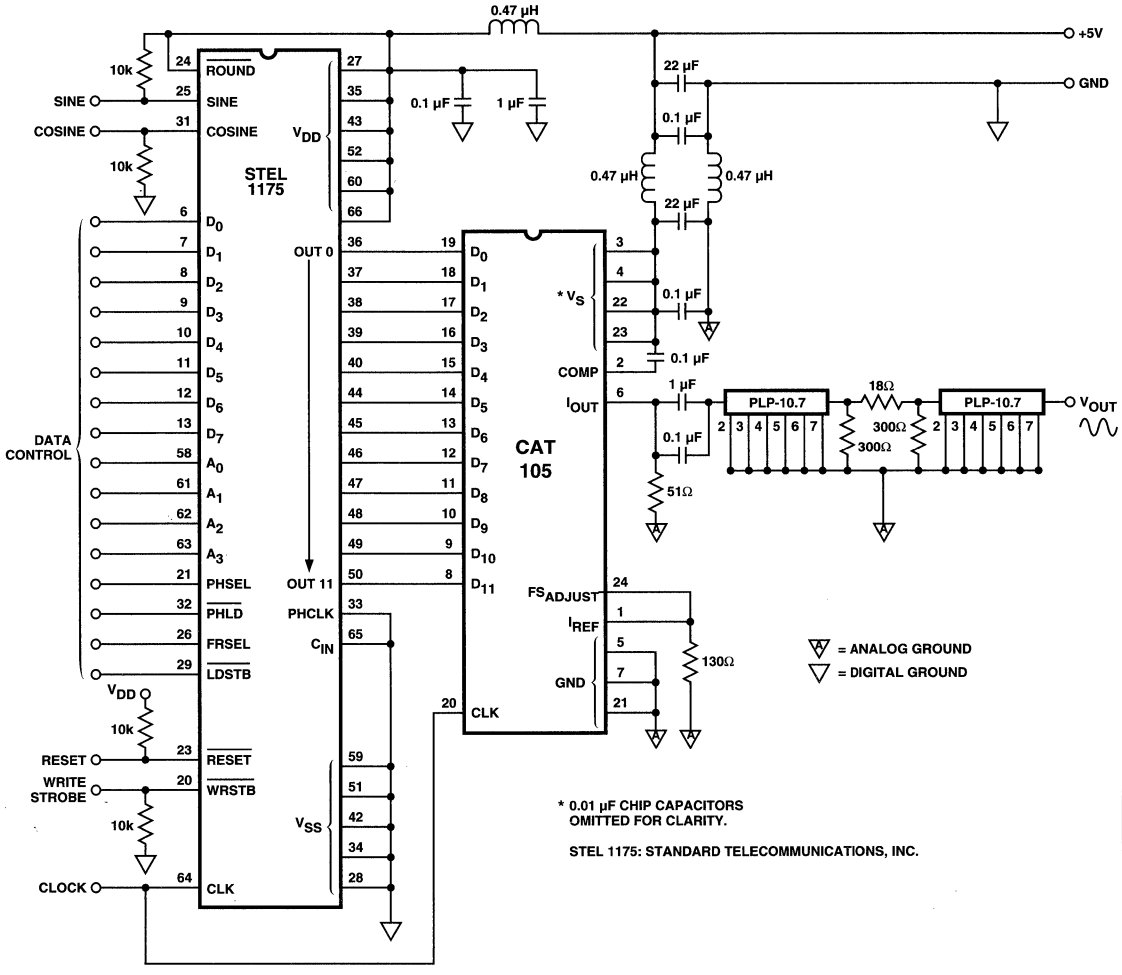
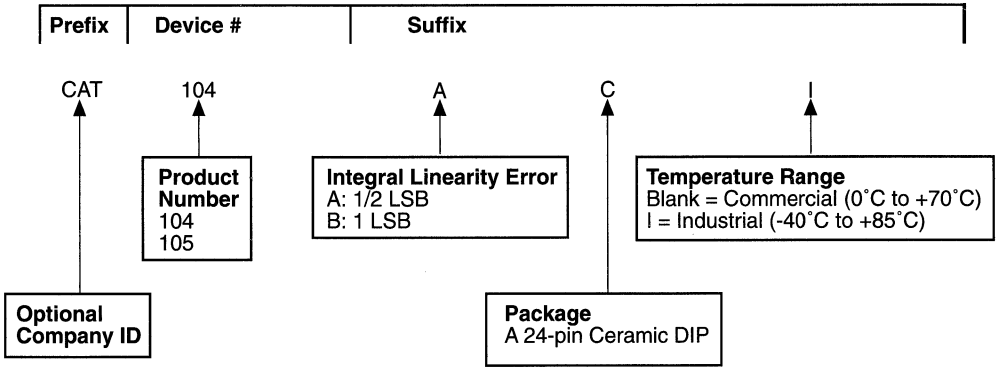


Figure 6. Direct Digital Synthesis (DDS) Using the CAT105

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT104ACI (1/2 Integrated Linearity Error, Ceramic DIP, Industrial Temperature)

CAT504

8-Bit Quad DACpot

FEATURES

- Output settings retained without power
- Output range includes both supply rails
- 4 independently addressable outputs
- 1 LSB Accuracy
- Serial µP interface
- Single supply operation: 3–5 Volts
- Setting read-back without effecting outputs

APPLICATIONS

- Automated product calibration.
- Remote control adjustment of equipment
- Offset, gain and zero adjustments in Self-Calibrating and Adaptive Control systems.
- Tamper-proof calibrations.

DESCRIPTION

The CAT504 is a quad 8-Bit Memory DAC designed as an electronic replacement for mechanical potentiometers and trim pots. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for systems capable of self calibration, and applications where equipment which is either difficult to access or in a hazardous environment, requires periodic adjustment.

The 4 independently programmable DAC's have an output range which includes both supply rails. Output settings, stored in non-volatile EEPROM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each output can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DAC's output.

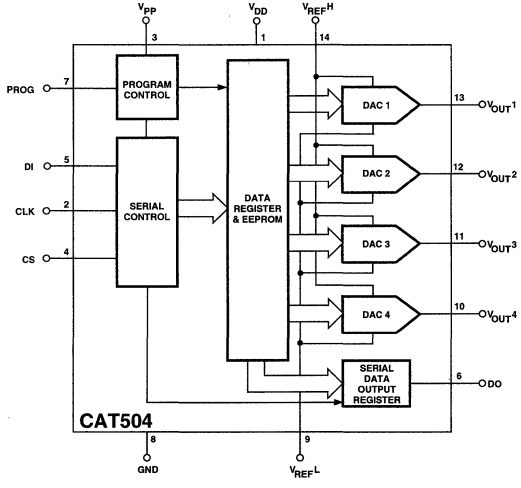
Control of the CAT504 is accomplished with a simple 3 wire serial interface. A Chip Select pin allows several CAT504s to share a common serial interface and communication back to the host controller is via a single serial data line thanks to the CAT504's Tri-Stated Data Output pin.

The CAT504 operates from a single 3–5 volt power supply drawing just a few milliwatts of power. When storing data in EEPROM memory an additional 20 volt low current supply is required.

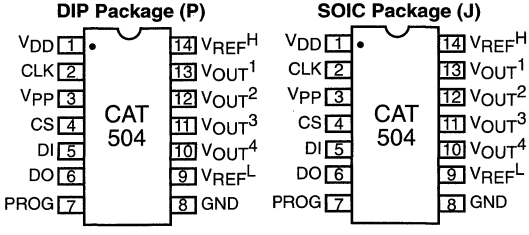
The CAT504 is available in the 0 to 70° C Commercial and –40° C to + 85° C Industrial operating temperature ranges and offered in 14-pin plastic DIP and Surface mount packages.

9

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
- V_{DD} to GND ..... –0.5V to +7V
- V_{PP} to GND ..... –0.5V to +22V

Inputs
- CLK to GND ..... –0.5V to V_{DD} +0.5V
- CS to GND ..... –0.5V to V_{DD} +0.5V
- DI to GND ..... –0.5V to V_{DD} +0.5V
- PROG to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}H$ to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}L$ to GND ..... –0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... –0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... –0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

DC ELECTRICAL CHARACTERISTICS:

V_{DD} = +3V to +5V ±10%, $V_{REF}H$ = V_{DD}, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8	—	—	Bits
Accuracy						
INL	Integral Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	—	±1	LSB
		T_R = I	—	—	±1	LSB
		I_{LOAD} = 1 µA, T_R = C	—	—	±2	LSB
		T_R = I	—	—	±2	LSB
DNL	Differential Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	—	±0.5	LSB
		T_R = I	—	—	±0.5	LSB
		I_{LOAD} = 1 µA, T_R = C	—	—	±1.5	LSB
		T_R = I	—	—	±1.5	LSB
Logic Inputs						
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V
References						
V_{RH}	$V_{REF}H$ Input Voltage Range		2.7	—	V_{DD}	V
V_{RL}	$V_{REF}L$ Input Voltage Range		GND	—	V_{DD} -2.7	V
Z_{IN}	$V_{REF}H$–$V_{REF}L$ Resistance		—	7k	—	Ω
Logic Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = – 40 µA	V_{DD} –0.3	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

DC ELECTRICAL CHARACTERISTICS (Cont.):
V_{DD} = +3V to +5V ±10%, $V_{REF}H$ = +V_{DD}, $V_{REF}L$ = 0V, unless otherwise specified

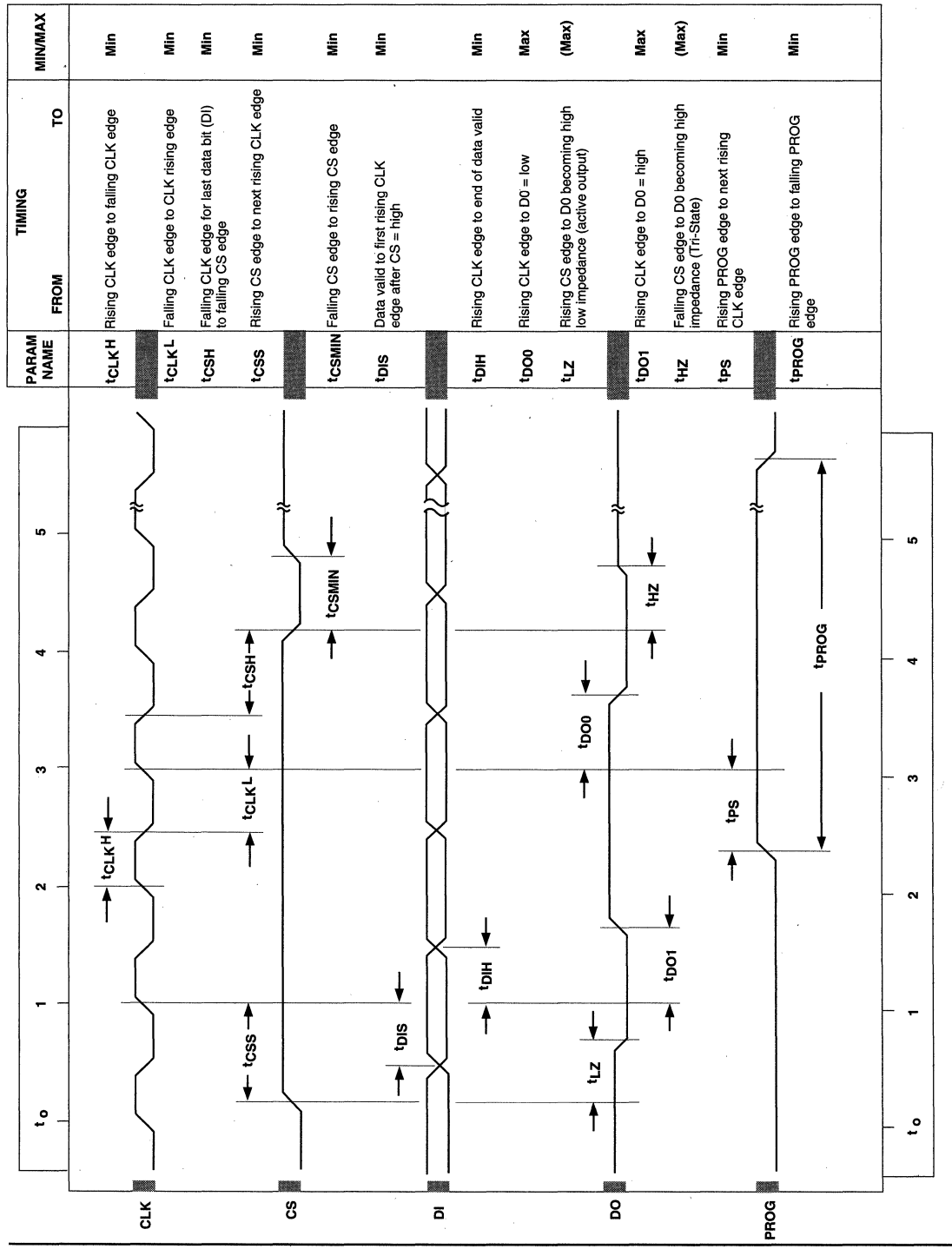
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Analog Output						
FSO	Full-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	0.99 V_R	0.995 V_R	—	V
ZSO	Zero-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	—	0.005 V_R	0.10 V_R	V
I_L	DAC Output Load Current		—	—	1	µA
R_{OUT}	DAC Output Impedance	V_{DD} = +5V	—	—	20k	Ω
		V_{DD} = +3V	—	—	40k	Ω
PSSR	Power Supply Rejection	I_{LOAD} = 250 nA	—	—	1	LSB / V
Temperature						
TC_O	V_{OUT} Temperature Coefficient	$V_{REF}H$ = +5V, $V_{REF}L$ = 0V V_{DD} = +5V, I_{LOAD} = 250nA	—	—	200	µV/ °C
TC_{REF}	Temperature Coefficient of V_{REF} Resistance	$V_{REF}H$ to $V_{REF}L$	—	700	—	ppm / °C
Power Supply						
I_{DD}	Supply Current	Excludes V_{REF}	—	—	50	µA
I_{PP}	Programming Current	V_{PP} = +19V	—	200	500	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V
V_{PP}	Programing Voltage Range		18	19	20	V

AC ELECTRICAL CHARACTERISTICS:
V_{DD} = +3V to +5V ±10%, $V_{REF}H$ = +V_{DD}, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time		0	—	—	ns
t_{DIS}	DI Setup Time	C_L = 100 pF,	50	—	—	ns
t_{DIH}	DI Hold Time	see note 1	50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{PROG}	Erase/Write Pulse Width		3	5	—	ms
t_{PS}	PROG Setup Time		150	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DAC Settling Time to 1/2 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs
Pin Capacitance						
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, (2)	—	8	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz, (2)	—	6	—	pF

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive.
2	CLK	Clock input pin.Clock input pin.
3	V_{PP}	EEPROM Programming Voltage
4	CS	Chip Select
5	DI	Serial data input pin.
6	DO	Serial data output pin.
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground.
9	$V_{REF}L$	Minimum DAC output voltage.
10	$V_{OUT}4$	DAC output channel 4.
11	$V_{OUT}3$	DAC output channel 3.
12	$V_{OUT}2$	DAC output channel 2.
13	$V_{OUT}1$	DAC output channel 1.
14	$V_{REF}H$	Maximum DAC output voltage.

DAC addressing is as follows:

DAC OUTPUT	A0	A1
$V_{OUT}1$	0	0
$V_{OUT}2$	1	0
$V_{OUT}3$	0	1
$V_{OUT}4$	1	1

DEVICE OPERATION

The CAT504 is a quad 8-bit Digital to Analog Converter (DAC) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile EEPROM memory and will not be lost when power is removed from the chip. Upon power up the DACs return to the settings stored in EEPROM memory. Each DAC can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be temporarily adjusted without changing the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT504 employs a standard 3 wire serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic "1" as a start bit. The DAC address and data are clocked into the DI pin on the clock's rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT504's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DAC control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DAC outputs to the settings stored in EEPROM memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been equipped with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT504's clock controls both data flow in and out of the IC and EEPROM memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to EEPROM memory, even though the data being saved may already be resident in the DAC control register.

No clock is necessary upon system power-up. The CAT504's internal power-on reset circuitry loads data from EEPROM to the DACs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins $V_{REF}H$ and $V_{REF}L$, sets the DAC's Zero to Full Scale output range where $V_{REF}L$ = Zero and $V_{REF}H$ = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications $V_{REF}H$ and $V_{REF}L$ are connected across the power supply rails. When using less than the full supply voltage $V_{REF}H$ is restricted to voltages between V_{DD} and $V_{DD}/2$ and $V_{REF}L$ to voltages between GND and $V_{DD}/2$.

V_{PP}

When saving data to non-volatile EEPROM memory an external voltage of 18–20 volts must be applied to the V_{PP} pin. This voltage need only be present during the programming cycle and may be removed or turned off the remainder of the time. While it is not necessary to remove or power down V_{PP} between programming cycles, some power sensitive applications may choose to do so. In such cases, the V_{PP} supply must be given sufficient time to come up and stabilize before issuing the PROG command.

DATA OUTPUT

Data is output serially by the CAT504, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 504s to share a single serial data line and simplifies interfacing multiple 504s to a microprocessor.

9

WRITING TO MEMORY

Programming the CAT504's EEPROM memory is accomplished through the application of an externally generated programming voltage, V_{PP}, and the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DAC address and eight data bits are clocked into the DAC control register via the DI pin. Data enters on the clock's rising edge. The DAC output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is achieved by bringing PROG high for a minimum of 3 ms while supplying 18 to 20 volts to the V_{PP} pin. PROG must be brought high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DAC control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of ramping the programming voltage for data transfer to the EEPROM cells. The CAT504's EEPROM memory cells will endure over 100,000 write cycles and will retain data for a minimum of 20 years without being refreshed.

READING DATA

Each time data is transferred into a DAC control register currently held data is shifted out via the DI pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DAC's output. This feature allows µPs to poll DACs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in EEPROM so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the EEPROM's setting is reloaded into the DAC control register. Since this value is the same as that which had been there previously no change in the DAC's output is noticed. Had the value held in the control register been different from that stored in EEPROM then *a change would occur* at the read cycle's conclusion.

Figure 1. Writing to Memory

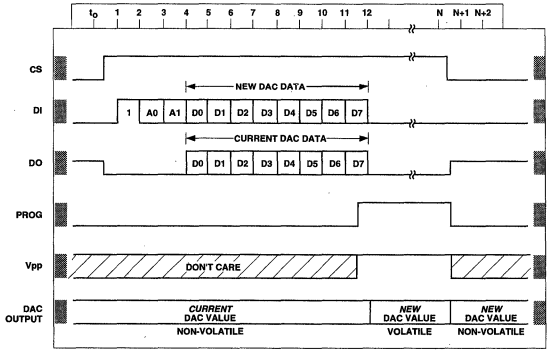
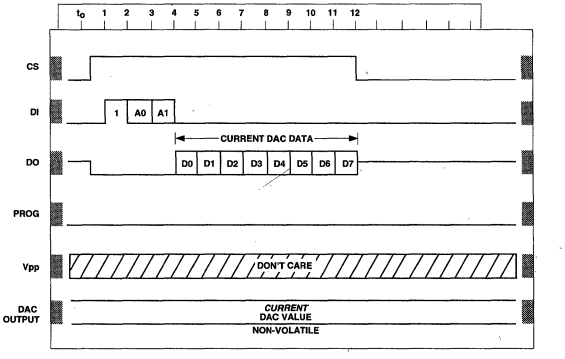


Figure 2. Reading from Memory



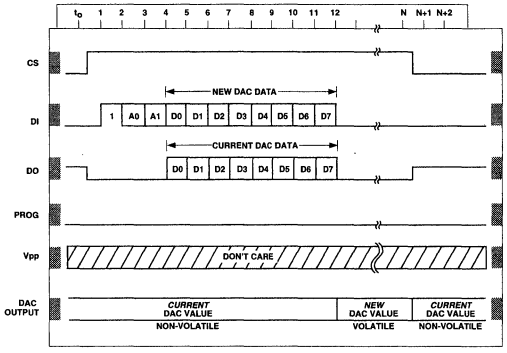
TEMPORARILY CHANGE OUTPUT

The CAT504 allows temporary changes in DAC's output to be made without disturbing the settings retained in EEPROM memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

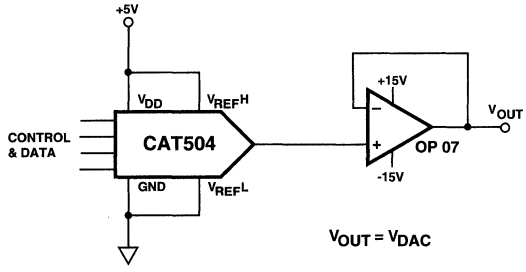
Figure 3 shows the control and data signals needed to effect a temporary output change. DAC settings may be changed as many times as required and can be made to any of the four DACs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all four DACs will return to the output values stored in EEPROM memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DAC control register prior to programming. This is because the CAT504's internal control circuitry discards the new data from the programming register two clock cycles after receiving it (after reception is complete) if no PROG signal is received.

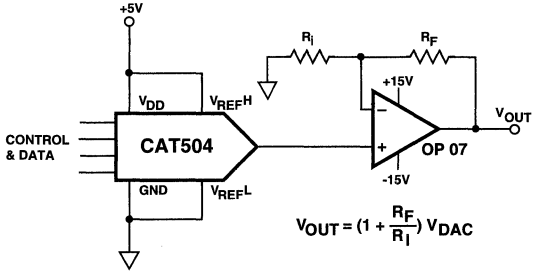
Figure 3. Temporary Change in Output



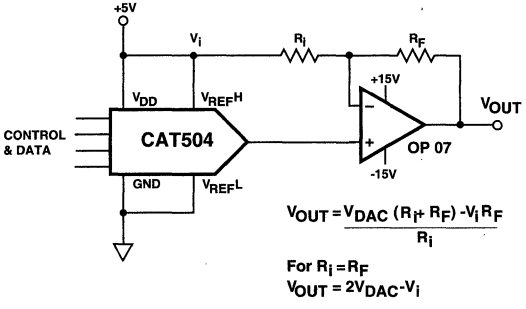
APPLICATION CIRCUITS



Buffered DAC Output



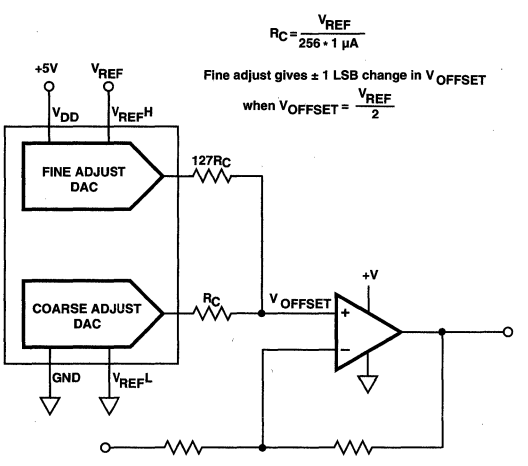
Amplified DAC Output



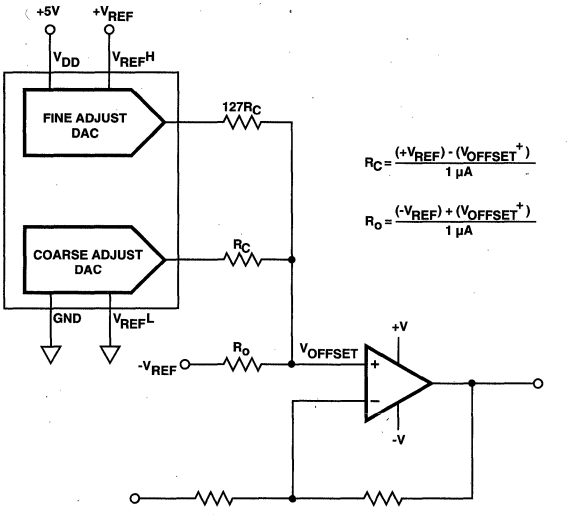
DAC INPUT		DAC OUTPUT	ANALOG OUTPUT
		$V_{DAC} = \frac{CODE}{255} (V_{FS} - V_{ZERO}) + V_{ZERO}$	
		$V_{FS} = 0.99\ V_{REF}$	$V_{REF} = 5V$
MSB	LSB	$V_{ZERO} = 0.01\ V_{REF}$	$R_I = R_F$
1111	1111	$\frac{255}{255}(.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\ V_{REF}) + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90V$

Bipolar DAC Output

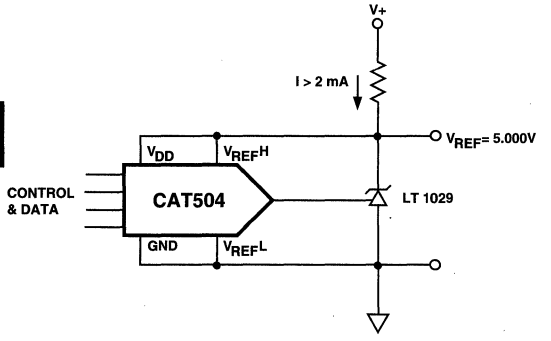
APPLICATION CIRCUITS (Cont.)



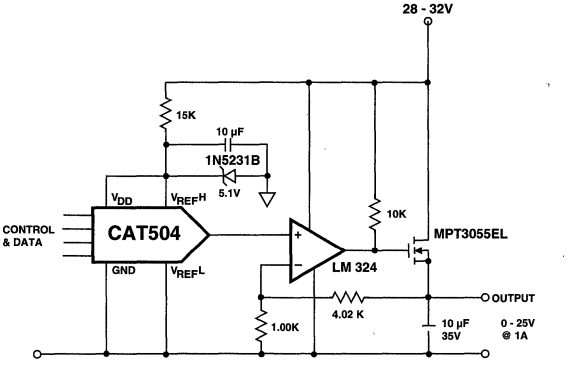
Coarse-Fine Offset Control by Averaging DAC Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DAC Outputs for Dual Power Supply Systems

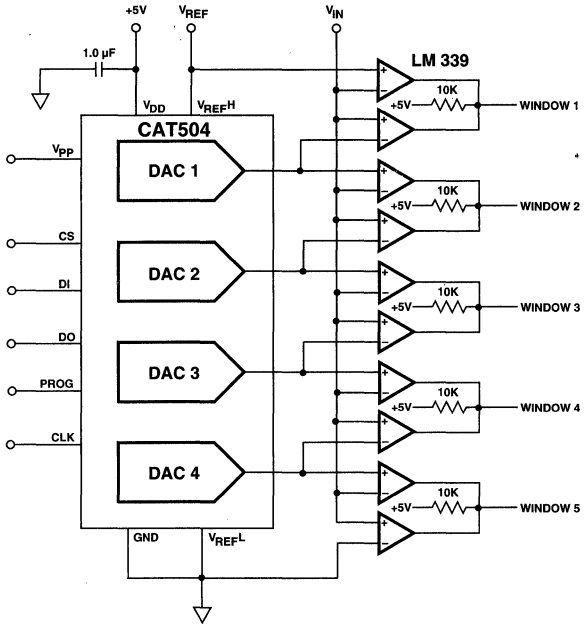


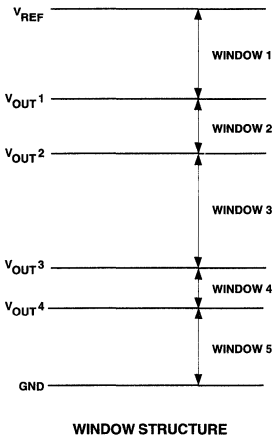
Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

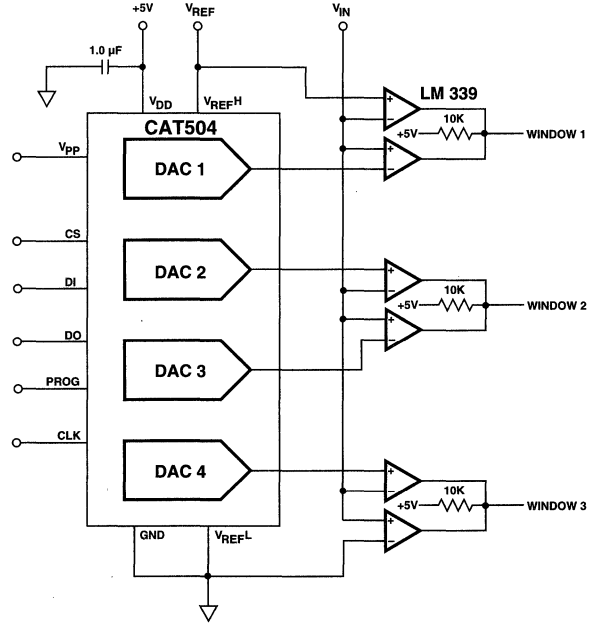
APPLICATION CIRCUITS (Cont.)

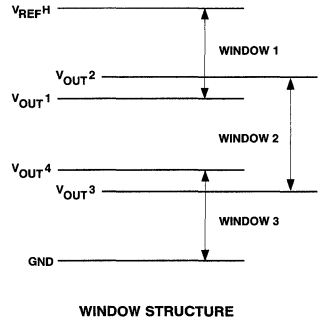




WINDOW STRUCTURE

Staircase Window Comparator

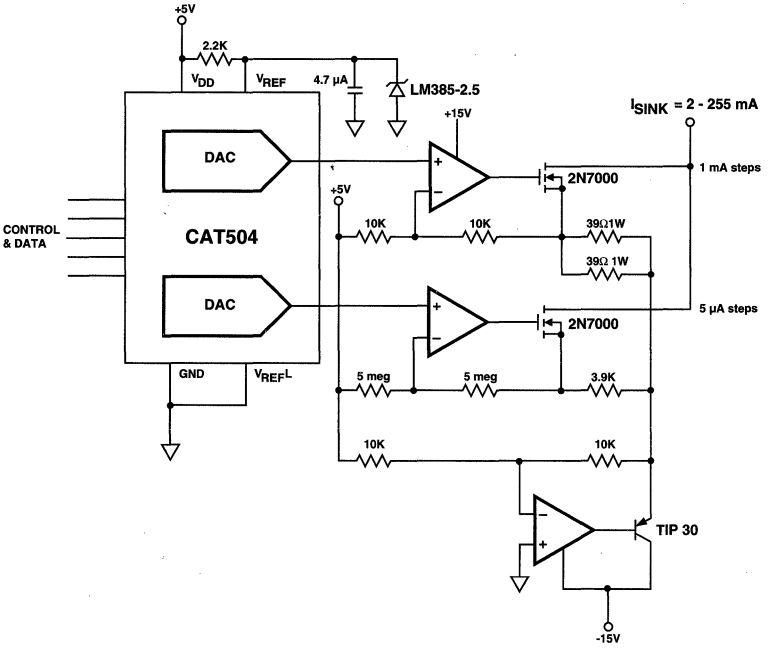




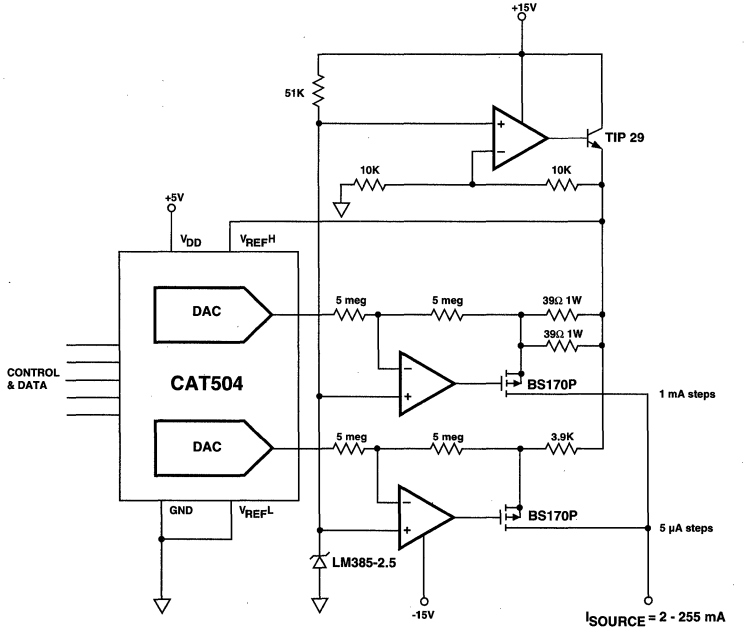
WINDOW STRUCTURE

Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

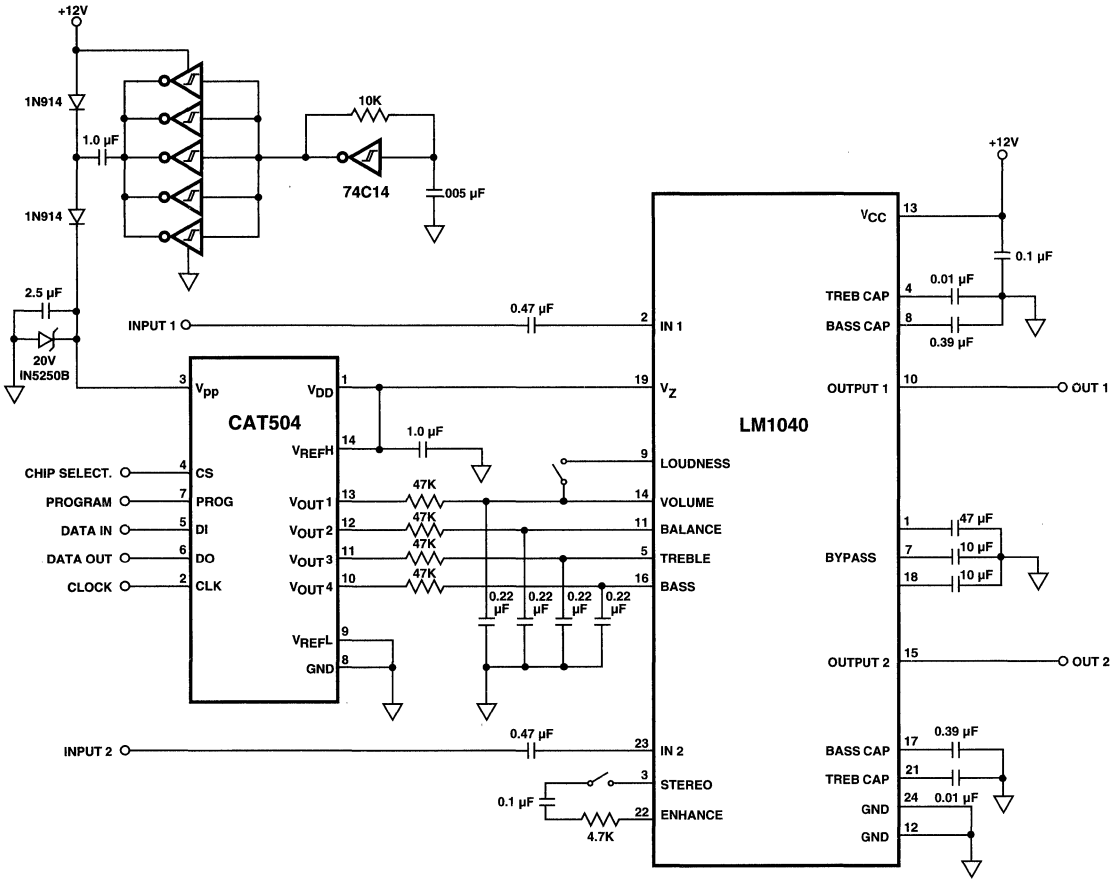


Current Sink with 4 Decades of Resolution



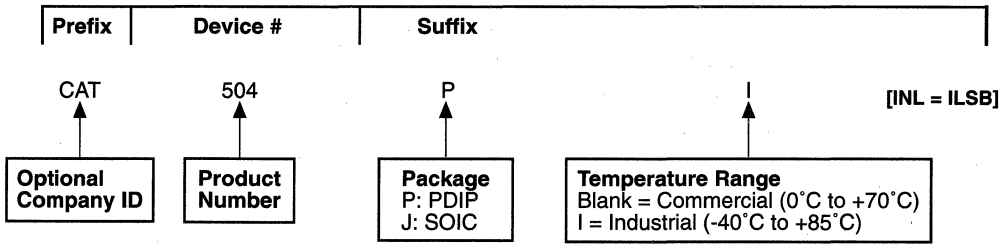
Current Source with 4 Decades of Resolution

APPLICATION CIRCUITS (Cont.)



Digital Stereo Control

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT504PI (Plastic DIP, Industrial Temperature)

9

CAT505

8-Bit Quad DACpot with RDY/BUSY and IND. Reference Inputs

FEATURES

- Output settings retained without power
- Independent Reference Inputs
- Output range includes both supply rails
- Programming voltage generated on-chip
- 4 independently addressable outputs
- Serial µP interface
- Single supply operation: 3–5 Volts

APPLICATIONS

- Automated product calibration.
- Remote control adjustment of equipment
- Offset, gain and zero adjustments in Self-Calibrating and Adaptive Control systems.
- Tamper-proof calibrations.

DESCRIPTION

The CAT505 is a quad 8-Bit Memory DAC designed as an electronic replacement for mechanical potentiometers and trim pots. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines and systems capable of self calibration, it is also well suited for applications were equipment requiring periodic adjustment is either difficult to access or located in a hazardous environment.

The CAT505 offers 4 independently programmable DACs each having its own reference inputs and each capable of rail to rail output swing. Output settings, stored nonvolatile EEPROM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each output can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DAC's output.

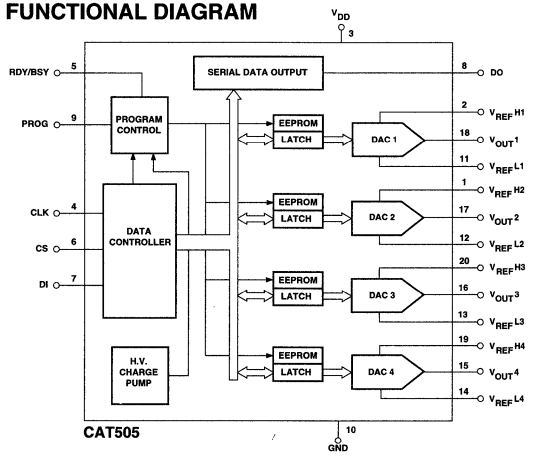
Control of the CAT505 is accomplished with a simple 3 wire serial interface. A Chip Select pin allows several CAT505s to share a common serial interface and communications back to the host controller is via a single serial data line thanks to the CAT505's Tri-Stated Data Output pin. A Rdy/Bsy output working in concert with an internal low voltage detector signals proper operation of EEPROM Erase/Write cycle.

The CAT505 operates from a single 3–5 volt power supply. The high voltage required for EEPROM Erase/Write operations is generated on-chip.

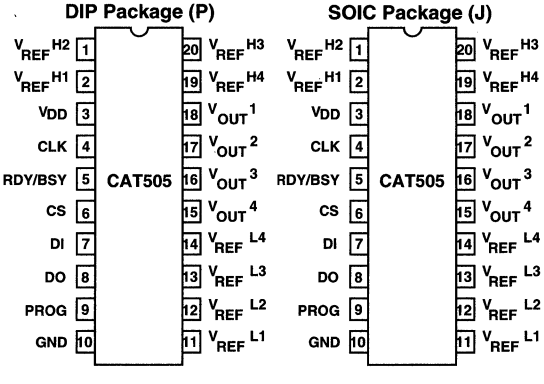
The CAT505 is available in the 0°C to 70°C Commercial and –40°C to +85°C Industrial operating temperature ranges and offered in 20-pin plastic DIP and Surface mount packages.

9

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltage*
- V_{DD} to GND ..... –0.5V to +7V
- V_{PP} to GND ..... –0.5V to +22V

Inputs
- CLK to GND ..... –0.5V to V_{DD} +0.5V
- CS to GND ..... –0.5V to V_{DD} +0.5V
- DI to GND ..... –0.5V to V_{DD} +0.5V
- RDY/BSY to GND ..... –0.5V to V_{DD} +0.5V
- PROG to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}H$ to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}L$ to GND ..... –0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... –0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... –0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

DC ELECTRICAL CHARACTERISTICS: V_{DD} = +3V to +5V ±10%, $V_{REF}H$ = V_{DD}, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8	—	—	Bits
Accuracy						
INL	Integral Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	0.6	± 1	LSB
		T_R = I	—	0.6	± 1	LSB
		I_{LOAD} = 1 µA, T_R = C	—	1.2	—	LSB
		T_R = I	—	1.2	—	LSB
DNL	Differential Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	0.25	± 0.5	LSB
		T_R = I	—	0.25	± 0.5	LSB
		I_{LOAD} = 1 µA, T_R = C	—	0.5	—	LSB
		T_R = I	—	0.5	—	LSB
Logic Inputs						
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V
References						
V_{RH}	$V_{REF}H$ Input Voltage Range		2.7	—	V_{DD}	V
V_{RL}	$V_{REF}L$ Input Voltage Range		GND	—	V_{DD} -2.7	V
Z_{IN}	$V_{REF}H$–$V_{REF}L$ Resistance		—	28K	—	Ω
ΔV_{IN} / R_{IN}	Input Resistance Match		—	± 0.5	± 1	%
Logic Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = – 40 µA	V_{DD} –0.3	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

DC ELECTRICAL CHARACTERISTICS (Cont.):
V_{DD} = +3V to +5V ±10%, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

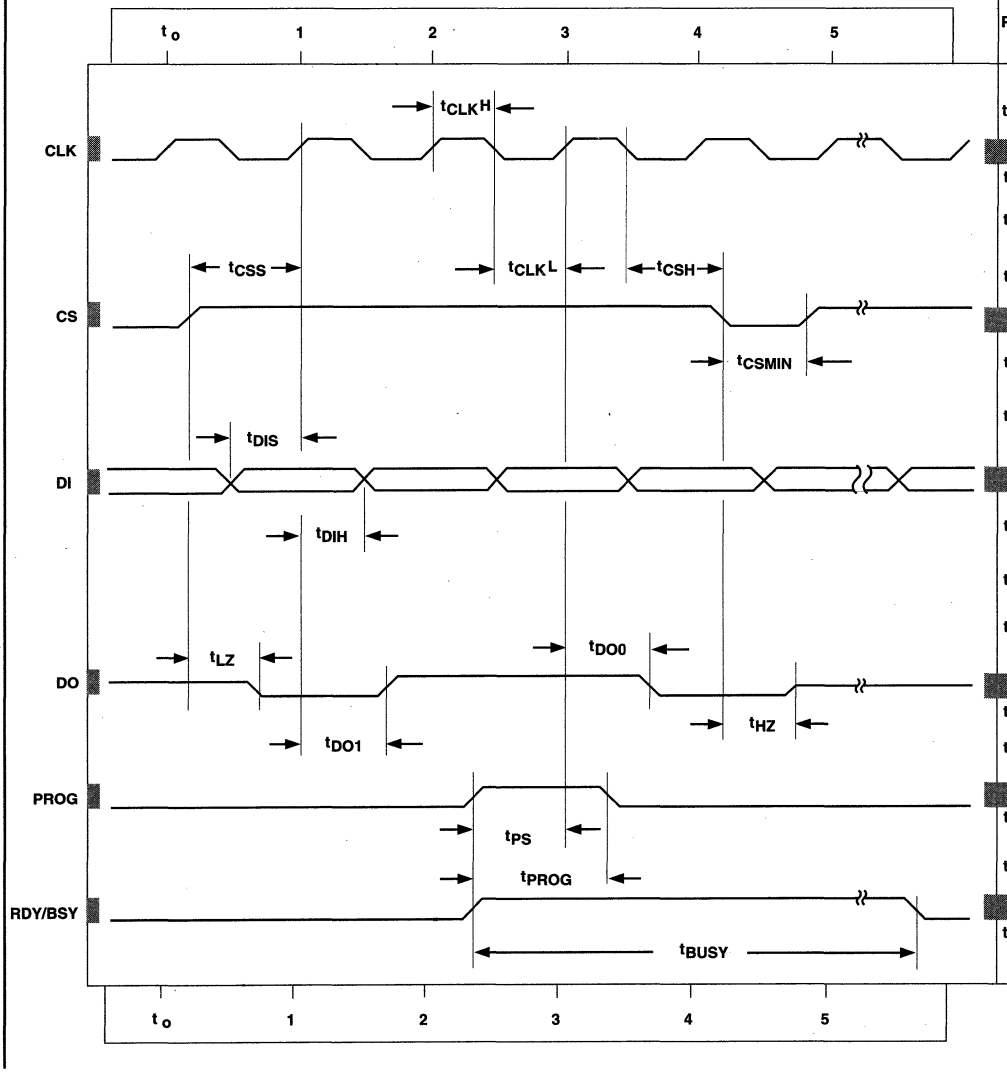
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Analog Output						
FSO	Full-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	0.99 V_R	0.995 V_R	—	V
ZSO	Zero-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	—	0.005 V_R	0.10 V_R	V
I_L	DAC Output Load Current		—	—	1	µA
R_{OUT}	DAC Output Impedance	$V_{DD} = V_{REF}H$ = +5V	—	—	25K	Ω
		$V_{DD} = V_{REF}H$ = +3V	—	—	40K	Ω
PSSR	Power Supply Rejection	I_{LOAD} = 1 µA	—	—	1	LSB / V
Temperature						
TC_O	V_{OUT} Temperature Coefficient	V_{DD} = +5V, I_{LOAD} = 250nA $V_{REF}H$= +5V, $V_{REF}L$ = 0V	—	—	200	µV/ °C
TC_{REF}	Temperature Coefficient of V_{REF} Resistance	$V_{REF}H$ to $V_{REF}L$	—	700	—	ppm / °C
Power Supply						
I_{DD}	Supply Current (Excludes V_{REF})	Normal Operating	—	18	50	µA
		Programming, V_{DD} = 5V	—	1200	2000	µA
		V_{DD} = 3V	—	600	1200	µA
		CS = 0	—	300	250	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

AC ELECTRICAL CHARACTERISTICS:
V_{DD} = +3V to +5V ±10%, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L = 100 pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	3.3	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		500	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DAC Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs
Pin Capacitance						
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, (2)	—	8	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz, (2)	—	6	—	pF

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PARAM NAME	TIMING FROM	TIMING TO	MIN/MAX
t_{CLKH}	Rising CLK edge	to falling CLK edge	Min
t_{CLKL}	Falling CLK edge	to CLK rising edge	Min
t_{CSH}	Falling CLK edge for last data bit (DI)	to falling CS edge	Min
t_{CSS}	Rising CS edge	to next rising CLK edge	Min
t_{CSMIN}	Falling CS edge	to rising CS edge	Min
t_{DIS}	Data valid	to first rising CLK edge after CS = high	Min
t_{DIH}	Rising CLK edge	to end of data valid	Min
t_{DO0}	Rising CLK edge	to D0 = low	Max
t_{LZ}	Rising CS edge	to D0 becoming high low impedance (active output)	(Max)
t_{DO1}	Rising CLK edge	to D0 = high	Max
t_{HZ}	Falling CS edge	to D0 becoming high impedance (Tri-State)	(Max)
t_{PS}	Rising PROG edge	to next rising CLK edge	Min
t_{PROG}	Rising PROG edge	to falling PROG edge	Min
t_{BUSY}	Rising PROG edge	to falling RDY/BSY edge	Max

PIN DESCRIPTION

Pin	Name	Function
1	$V_{REF}H2$	Maximum DAC 2 output voltage
2	$V_{REF}H1$	Maximum DAC 1 output voltage
3	V_{DD}	Power supply positive
4	CLK	Clock input pin
5	RDY/BSY	Ready/Busy output
6	CS	Chip select
7	DI	Serial data input pin
8	DO	Serial data output pin
9	PROG	EEPROM Programming Enable Input
10	GND	Power supply ground
11	$V_{REF}L1$	Minimum DAC 1 output voltage
12	$V_{REF}L2$	Minimum DAC 2 output voltage
13	$V_{REF}L3$	Minimum DAC 3 output voltage
14	$V_{REF}L4$	Minimum DAC 4 output voltage
15	$V_{OUT}4$	DAC 4 output
16	$V_{OUT}3$	DAC 3 output
17	$V_{OUT}2$	DAC 2 output
18	$V_{OUT}1$	DAC 1 output
19	$V_{REF}H4$	Maximum DAC 4 output voltage
20	$V_{REF}H3$	Maximum DAC 3 output voltage

DAC addressing is as follows:

DAC OUTPUT	A0	A1
$V_{OUT}1$	0	0
$V_{OUT}2$	1	0
$V_{OUT}3$	0	1
$V_{OUT}4$	1	1

DEVICE OPERATION

The CAT505 is a quad 8-bit Digital to Analog Converter (DAC) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile EEPROM memory and will not be lost when power is removed from the chip. Upon power up the DACs return to the settings stored in EEPROM memory. Each DAC can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT505 employs a standard 3 wire serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic "1" as a start bit. The DAC address and data are clocked into the DI pin on the clock's rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT505's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DAC control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DAC outputs to the settings stored in EEPROM memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT505's clock controls both data flow in and out of the IC and EEPROM memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to EEPROM memory, even though the data being saved may already be resident in the DAC control register.

No clock is necessary upon system power-up. The CAT505's internal power-on reset circuitry loads data from EEPROM to the DACs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins $V_{REF}H$ &$V_{REF}L$, sets the DAC's Zero to Full Scale output range where $V_{REF}L$ = Zero and $V_{REF}H$ = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications $V_{REF}H$ &$V_{REF}L$ are connected across the power supply rails. When using less than the full supply voltage be mindfull of the limits placed on $V_{REF}H$ and $V_{REF}L$ as specified in the **References** section of **DC Electrical Characteristics.**

READY/BUSY

When saving data to non-volatile EEPROM memory, the Ready/Busy ouput (RDY/BSY) signals the start and duration of the EEPROM erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/BSY goes low and remains low until the programming cycle is complete. During this time the CAT505 will ignore any data appearing at DI and no data will be output on DO.

RDY/BSY is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for EEPROM programming, RDY/BSY will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT505, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 505s to share a single serial data line and simplifies interfacing multiple 505s to a microprocessor.

WRITING TO MEMORY

Programming the CAT505's EEPROM memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DAC address and eight data bits are clocked into the DAC control register via the DI pin. Data enters on the clock's rising edge. The DAC output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DAC control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the EEPROM cells. The CAT505's EEPROM memory cells will endure over 100,000 write cycles and will retain data for a minimum of 20 years without being refreshed.

READING DATA

Each time data is transferred into a DAC control register currently held data is shifted out via the DI pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DAC's output. This feature allows µPs to poll DACs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in EEPROM so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the EEPROM's

Figure 1. Writing to Memory

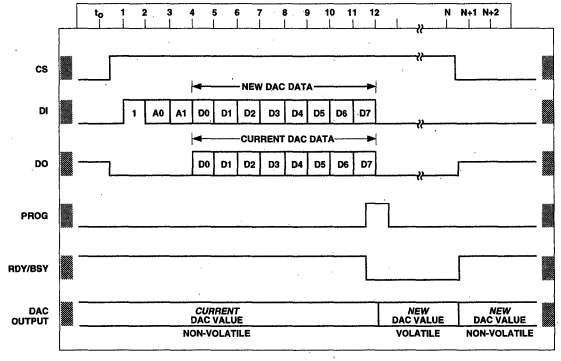
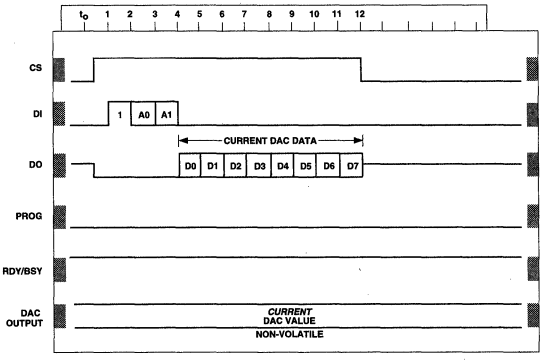


Figure 2. Reading from Memory



setting is reloaded into the DAC control register. Since this value is the same as that which had been there previously no change in the DAC's output is noticed. Had the value held in the control register been different from that stored in EEPROM then *a change would occur* at the read cycle's conclusion.

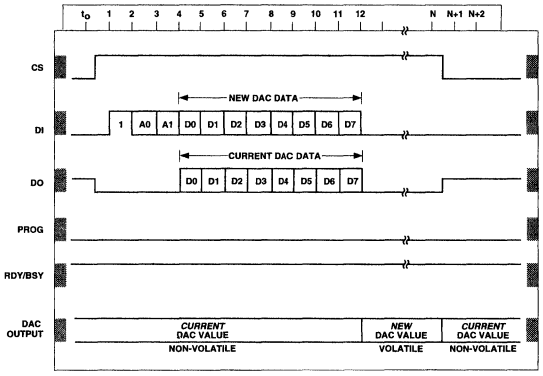
TEMPORARILY CHANGE OUTPUT

The CAT505 allows temporary changes in DAC's output to be made without disturbing the settings retained in EEPROM memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

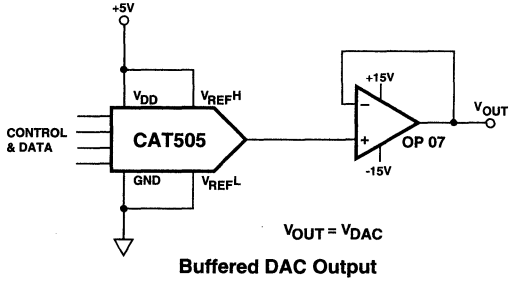
Figure 3 shows the control and data signals needed to effect a temporary output change. DAC settings may be changed as many times as required and can be made to any of the four DACs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all four DACs will return to the output values stored in EEPROM memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DAC control register prior to programming. This is because the CAT505's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output

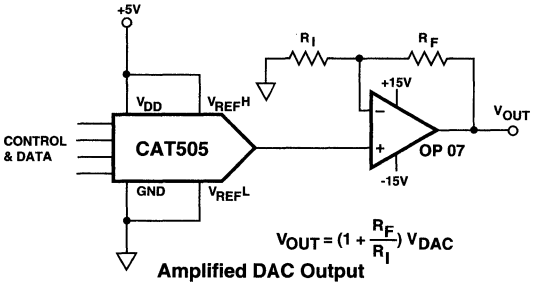


APPLICATION CIRCUITS



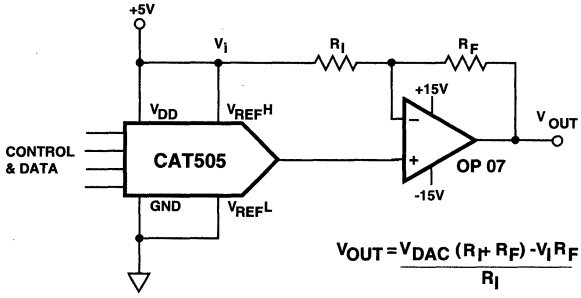
$V_{OUT} = V_{DAC}$

Buffered DAC Output



$V_{OUT} = (1 + \frac{R_F}{R_I}) V_{DAC}$

Amplified DAC Output



$$V_{OUT} = \frac{V_{DAC}(R_I + R_F) - V_I R_F}{R_I}$$

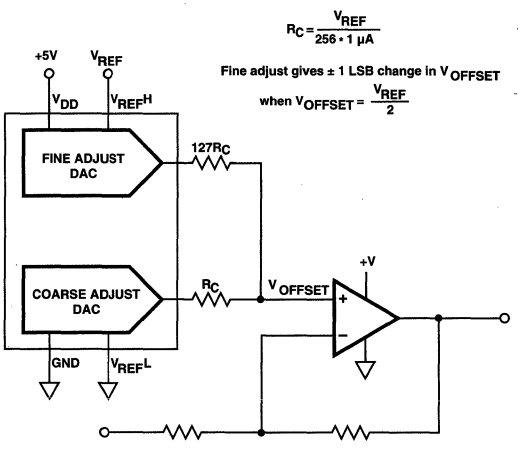
For $R_I = R_F$

$V_{OUT} = 2V_{DAC} - V_I$

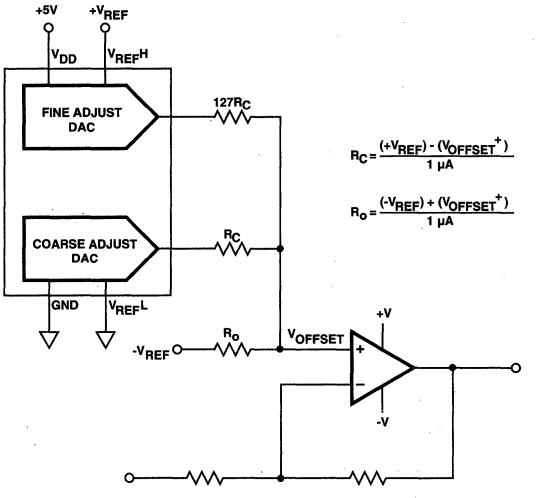
Bipolar DAC Output

DAC INPUT		DAC OUTPUT	ANALOG OUTPUT
		$V_{DAC} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$	
		$V_{FS} = 0.99\ V_{REF}$	$V_{REF} = 5V$
MSB	LSB	$V_{ZERO} = 0.01\ V_{REF}$	$R_I = R_F$
1111	1111	$\frac{255}{255}(.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\ V_{REF}) + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90V$

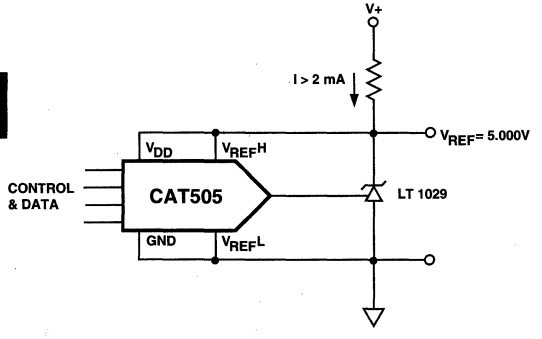
APPLICATION CIRCUITS (Cont.)



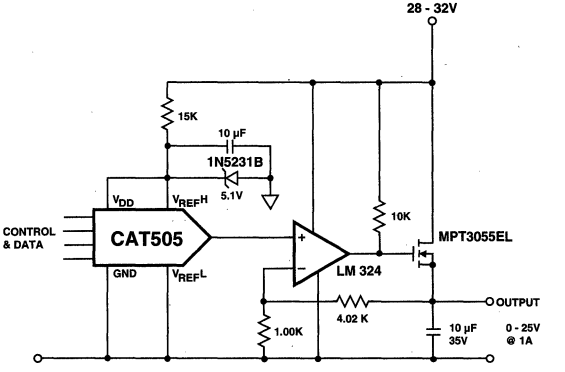
Coarse-Fine Offset Control by Averaging DAC Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DAC Outputs for Dual Power Supply Systems

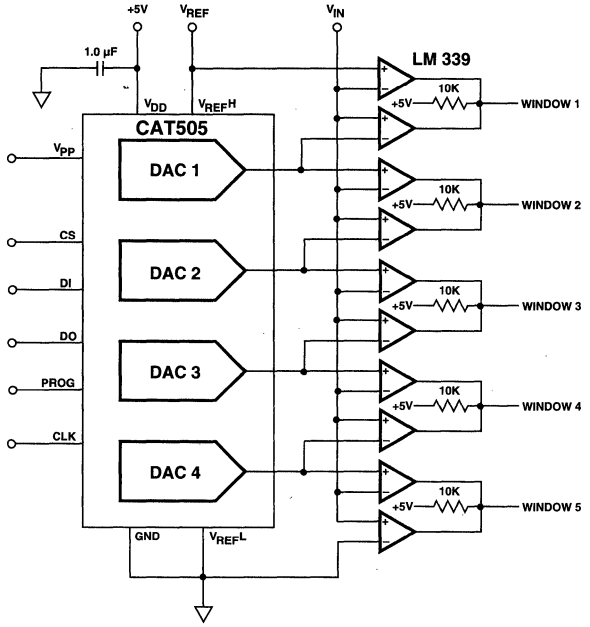


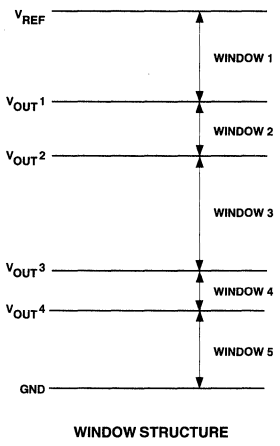
Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

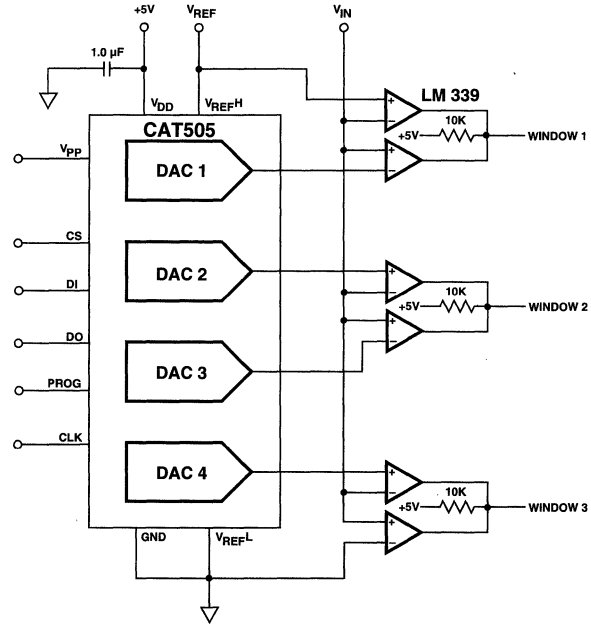
APPLICATION CIRCUITS (Cont.)

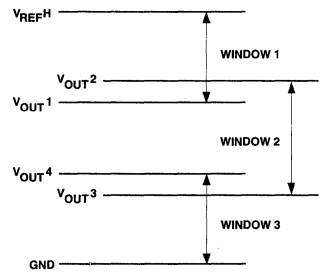




WINDOW STRUCTURE

Staircase Window Comparator

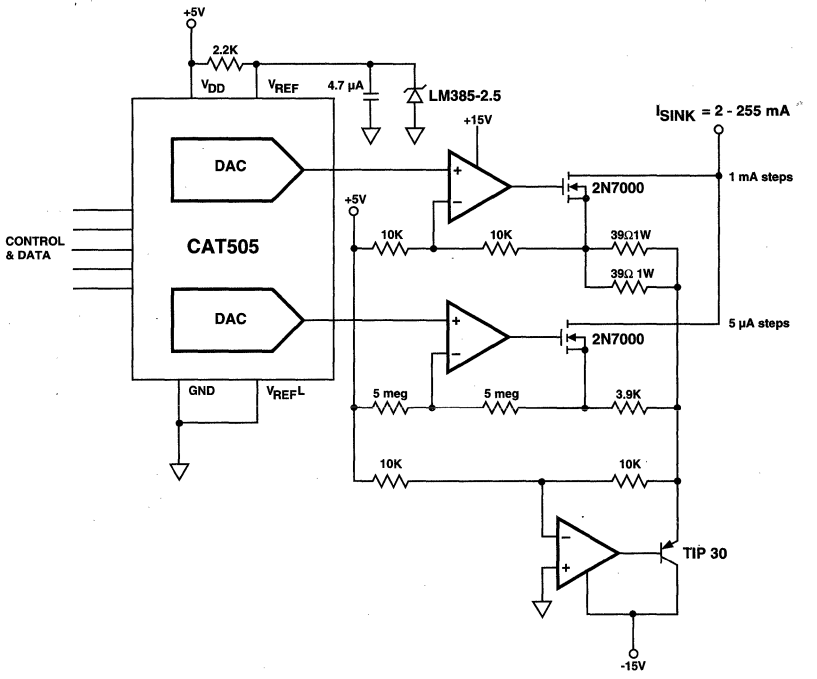




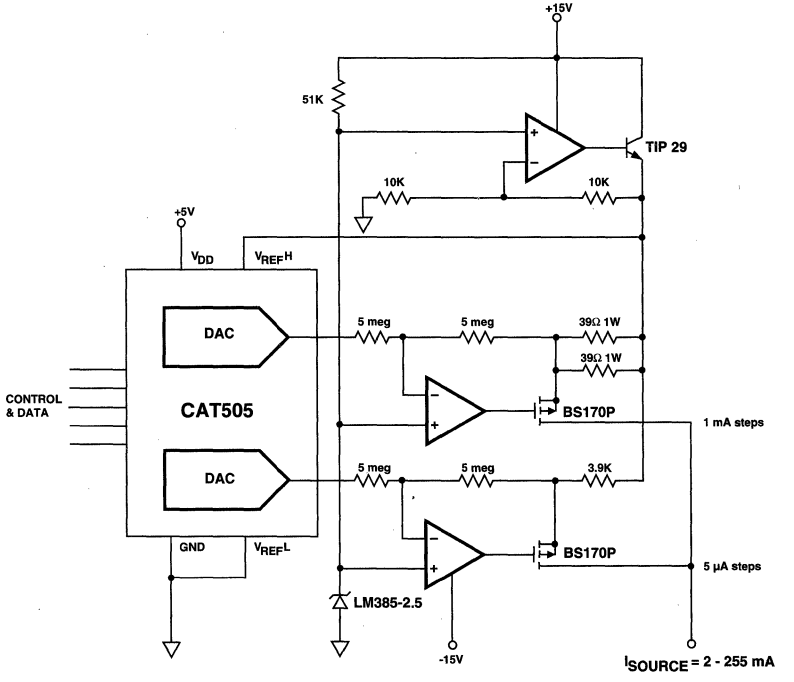
WINDOW STRUCTURE

Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

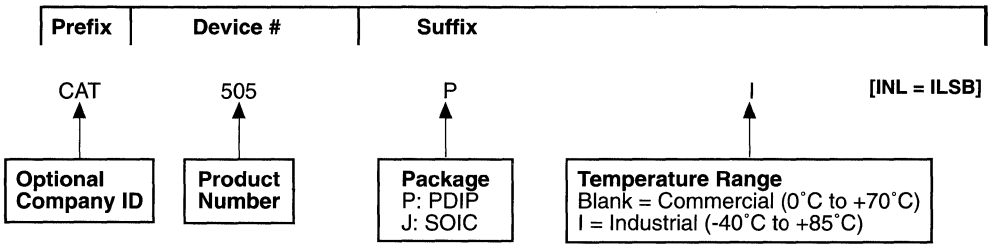


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT505PI (Plastic DIP, Industrial Temperature)

CAT506

12 Bit, 40MHz D/A Converter

FEATURES

- 25 ns maximum settling time (1/2 LSB)
- 40 MHz update rate
- 1/2 LSB Integral Non-Linearity
- 1/2 LSB Differential Non-Linearity
- 25 ppm/°C internal voltage reference
- Low Power BiCMOS construction
- Single Supply operation (+5 V)

APPLICATIONS

- Arbitrary Waveform Generators
- Direct Digital Synthesis (DDS)
- High Resolution A/D Converters
- Automatic Test Equipment
- High Definition Video

DESCRIPTION

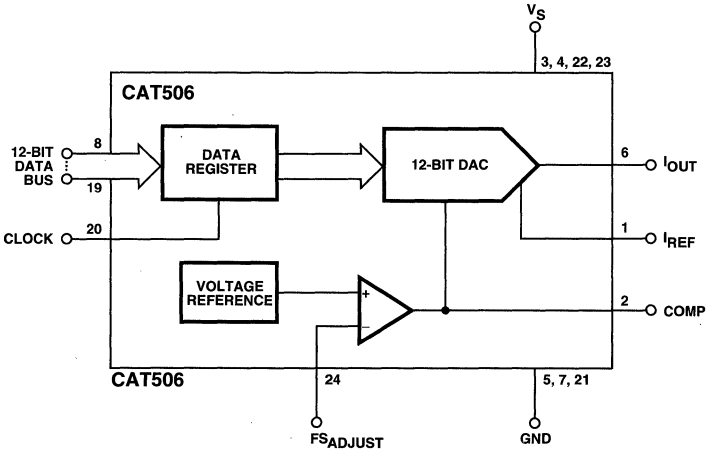
The CAT506 is a monolithic 12-bit current output D/A converter designed for precision high speed data conversion applications. Powered from a single +5 Volt supply the CAT506 will source 40 mA of current into a 25 Ohm load at clock speeds of 40 MHz while maintaining 1/2 LSB accuracy. Settling time is 25 ns to .012% of Full Scale.

Fabricated in a 2.0 micron BiCMOS process, the CAT506 incorporate on-chip EEPROM driven trim circuitry for factory correction of all silicon and package induced errors. Gain error is adjusted to below <0.2% and linearity to .012%. Monotocity is guaranteed over the full operating temperature range. The CAT506 includes an on-chip voltage reference which is EEPROM trimmed to achieve a typical drift with temperature of 25 ppm/°C.

The CAT506 is pin compatible with Brooktree's Bt 105 while offering significantly improved performance. Packaged in 24-pin Ceramic DIPs the CAT506 is specified for operation over the 0°C to +70°C Commercial temperature range.

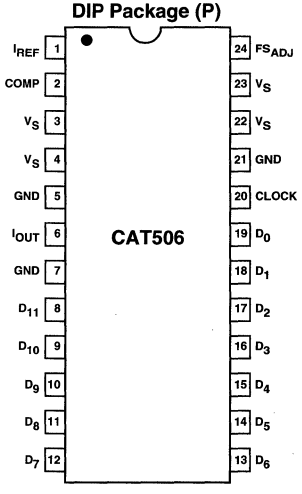
9

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

DIP Package (P)



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Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
- V_S to GND ..... –0.5V to +7V

Inputs
- D_0-D_{11} to GND ..... –0.5V to V_S +0.5V
- FS_{ADJUST} to GND ..... –0.5V to V_S +0.5V
- COMP to GND ..... –0.5V to V_S +0.5V
- CLOCK to GND ..... –0.5V to V_S +0.5V
- I_{REF} ..... ±10 mA

Outputs
- Analog Output Current (I_{OUT}) ..... 50 mA
- Analog Output Voltage (I_{OUT}) .. V_S^- 7V to V_S^+ 0.5V
- Analog Output Short Circuit Duration ..... Infinite

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions if NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = +5V ±0.25V; T_A = 0°C to +70°C; I_{OUT} (FS) = 40mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Resolution			12	—	—	Bits
Accuracy						
INL	Integral Linearity Error	CAT506A	—	—	±1/2	LSB
		CAT506B	—	—	±1	LSB
DNL	Differential Linearity Error		—	—	±1/2	LSB
	Zero Offset Error		—	—	1	µA
	Gain Error	Internal Reference	—	±0.15	±0.3	%FS
		External Reference	—	—	±1	%FS
	Monotocity		Guaranteed			
Coding						
	I_{OUT}	D_0-D_{11} = 0	0	—	—	
	I_{OUT}	D_0-D_{11} = 1	—	—	Full Scale	
Data Inputs						
V_{IH}	High Level Input Voltage		2	—	—	V
V_{IL}	Low Level Input Voltage		—	—	0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V	—	—	1	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	—	—	–1	µA
Analog Output						
I_{OUT}	Output Current		10	—	40	mA
V_{OUT}	Output Compliance		–1	—	+1	V
R_{OUT}	Output Impedance		—	1	—	MΩ
TC_{GAIN}	Gain Temperature Coefficient		—	—	30	ppm/°C
Reference						
$I_{REF\ (Pin\ 1)}$	Operating Voltage Range		–0.3	0.68	1	V
V_{REF}	Internal Reference Voltage		0.67	0.68	0.69	V
TC_{VREF}	Temperature Coefficient		—	+25	—	ppm/°C

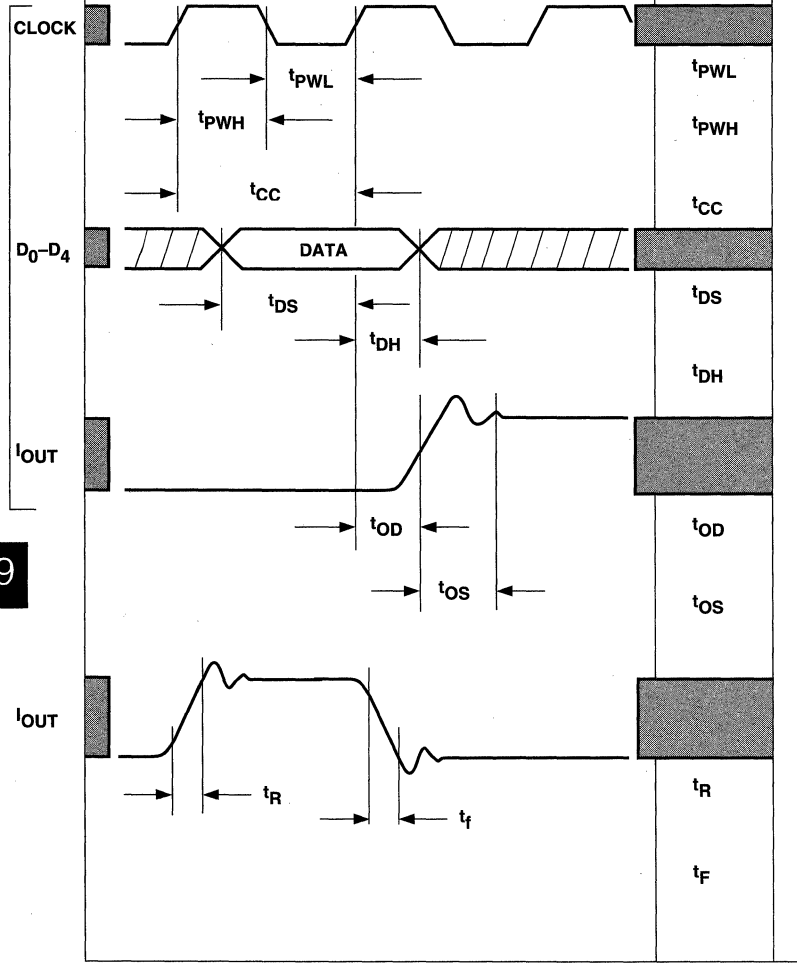
AC ELECTRICAL CHARACTERISTICS: V_S = 5V ±0.25V; R_L = 25Ω; I_{OUT} (FS) = 40 mA.
Logic inputs: 0V-3V; t_r and t_f < 3 ns; T_A = 0°C to +70°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Data Inputs						
f_{MAX}	Register Clock Rate		—	—	40	MHz
t_{CC}	Clock Cycle Time		25	—	—	ns
t_{PWH}	Clock Pulse Width High Time		10	—	—	ns
t_{PWL}	Clock Pulse Width Low Time		10	—	—	ns
t_{DS}	Data Setup Time		10	—	—	ns
t_{DH}	Data Hold Time		2	—	—	ns
	Pipeline Delay	CAT506 Only	1	1	1	Clock
Analog Output						
t_{OD}	Output Delay		—	18	—	ns
t_R	Output Rise Time		—	5	—	ns
t_F	Output Fall Time		—	5	—	ns
t_{OS}(1)	Output Settling Time	To 0.012% of FS	—	22	35	ns
		To 0.025% of FS	—	20	30	ns
		To 0.10% of FS	—	12	25	ns
	Clock and Data Feedthrough(1)		—	– 40	—	dB
	Glitch Impulse(1)		—	100	—	pV-sec
	Differential Gain Error		—	1.5	—	%FS
	Differential Phase Error		—	1.5	—	Degrees
SINAD	f_{CLK} = 20 MHz f_{OUT} = 500 KHz		—	59	—	dB
	f_{OUT} = 1 MHz		—	58	—	dB
	f_{CLK} = 5 MHz f_{OUT} = 500 KHz		—	65	—	dB
	f_{OUT} = 1 MHz		—	64	—	dB
Pin Capacitance						
C_{IN}	Input Capacitance, D_0-D_{11}, CLK	V_{IN} = 2.4V, f = 1 MHz	—	10	—	pF
C_{OUT}	Output Capacitance, Pin 6	I_{OUT} = 0 mA, f= 1 MHz	—	25	—	pF

NOTES: 1. Clock and Data feedthrough is function of the magnitude of overshoot and undershoot on the digital inputs. While testing, the digital inputs have a 1k ohm resistor connected to the regular PCB ground plane and are driven by 74 HC logic. Clock and data feedthrough are excluded from the settling time, where as they are included in glitch impulse. (Test bandwidth = 100 MHz.)

AC TIMING DIAGRAM

CAT506



PARAMETER NAME	MEASURED FROM	MEASURED TO	MIN MAX
t_{PWL}	FROM:	50% point of falling edge	Min
	TO:	50% point of rising edge	
t_{PWH}	FROM:	50% point of rising edge	Min
	TO:	50% point of falling edge	
t_{CC}	FROM:	50% point of rising edge	Min
	TO:	50% point of next rising edge	
t_{DS}	FROM:	Data valid	Min
	TO:	50% point of clock's next rising edge	
t_{DH}	FROM:	End of t_{DS} period	Min
	TO:	data invalid	
t_{OD}	FROM:	50% point of clock's rising edge	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	
t_R	FROM:	10% point of FS output	Max
	TO:	90% point of FS output	
t_F	FROM:	90% point of FS output	Max
	TO:	10% point of FS output	

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PIN DESCRIPTIONS

Pin No.	Name	Function
1	I_{REF}	Reference Current Output. The DAC's full scale output current is set by I_{REF}, which is normaly connected to FS_{ADJUST} and a resistor, R_{SET}. The full scale output current is then determined by the value of R_{SET}.
2	COMP	Compensation pin. This pin must be connected to the V_S pin through a ceramic capacitor. This capacitor provides power supply noise rejection and reduces the random noise of the internal bandgap reference. The capacitor can be between 0.01 µF and 0.1 µF, with 0.01µF being the recommended value. When an external reference voltage is used COMP is used in conjunction with FS_{ADJUST} to set I_{REF}.
3, 4, 22, 23	V_S	The positive supply voltage, nominally +5V.
5, 7,21	GND	Ground return for all signals (digital and analog) and V_S.
6	I_{OUT}	Analog Current Output. This high impedance current source is capable of sourcing up to 40 mA of current.
8-19	D_0-D_{11}	TTL compatible Data Inputs. Pin D_0 is the least significant data bit. For CAT506, the inputs are latched on the rising edge of clock. All unused inputs must be tied to V_S or GND.
20	Clock	Clock Input for CAT506. The rising edge of Clock latches the D_0-D_{11} inputs. Ideally, this pin should be driven by a dedicated TTL/CMOS buffer.
24	FS_{ADJUST}	Full Scale Adjust Control. When the internal reference voltage is used, the full scale output current is controlled by the resistor R_{SET}, connected between this input pin and GND. When an external voltage reference is used, FS_{ADJUST} is tied to V_S.

TERMS AND DEFINITIONS

Differential Non-Linearity (DNL): The maximum deviation from an ideal LSB step, between any two adjacent output levels. A DNL error more negative than –1 LSB implies non-monotonic output performance.

Full Scale Output Current: The output current at I_{out} resulting from all 1's at the data inputs.

Gain Error: The variation in the slope (gain) of the transfer function of a converter with respect to an established ideal transfer function. This error is expressed in % of FS (Full Scale) or LSB, when all bits are on, and may be eliminated by adjusting the reference current applied to the device.

Glitch Impulse Area: The analog output transient occurring between two adjacent codes as a result of unequal turn-on and turn-off times for the internal current sources. Glitch impulse is calculated as the area of the largest excursion, about the final value, and is specified as the net area of the glitch in nV-sec or pA-sec.

Integral Non-Linearity (INL): The maximum deviation between the actual output level and a best straight line fit. This excludes gain and offset errors.

Least-Significant Bit (LSB): The ideal output increment between two adjacent codes. Also, the data bit with the smallest effect on the output level.

Monotonicity: Implies that for an increase in digital code value that the output will either increase or remain unchanged. In mathematical terms the output is a single valued function of the input code, and the derivative of the output transfer function must not change signs.

Most-Significant Bit (MSB):The data bit with the largest effect on the output level. The MSB, for a linear DAC output, ideally equals the combined output weight of all other data bits, plus 1 LSB.

Offset Error: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

Output Compliance Range: The output voltage range over which a stated linearity specification is maintained. Integral linearity errors tend to be exaggerated with increasing output voltage levels.

Settling Time :The time from an initial full-scale output level change to the point where the output level is less than –1/2 LSB from its final value, for a full-scale step transition.

CURRENT vs VOLTAGE OUTPUT

The CAT506 has been carefully designed to work equally well in both current and voltage output applications, a claim not all DACs can make. When using other DACs, designers may be forced to use additional circuitry or be obliged to accept reduced performance when voltage output is required.

High speed DACs give their best performance in current output mode. This is because in current output operation the DAC's output is tied to a summing junction, such as the negative input of an op amp, and feedback around the op amp holds the junction voltage constant (usually 0 volts). Since no voltage change occurs at the DAC's output of the DAC is uneffected by load resistance, R_L, or any other impedances internal or external to the DAC.

When generating a voltage output, however, R_L can have a significant effect on the DAC's performance. The problem is caused by the DAC's own output impedance. As shown in Fig1 a DAC's output can be modeled as a current source in parallel with an internal resistance. When an external load is connected to I_{OUT}, it is in parallel with the internal resistance and the actual load seen by the DAC is the combination of their values. In developing an output voltage, I_{OUT} is split between internal and external loads, producing an apparent error in V_{OUT}. The degree of error is determined by the ratio of R_L to the internal shunt resistance. For ideal current sources the shunt resistance is infinite, but in typical high speed DACs it ranges from 200 to 20,000 Ω. This will produce a significant loading effect, even with the 50 Ω or 25 Ω loads commonly used in high speed systems.

To combat this problem, Optimum has taken special care to create a true current source output structure for the CAT506. The 1 MΩ output impedance of the CAT506 frees designers from concerns about voltage induced errors and voltage outputs can be had with no penalty in performance.

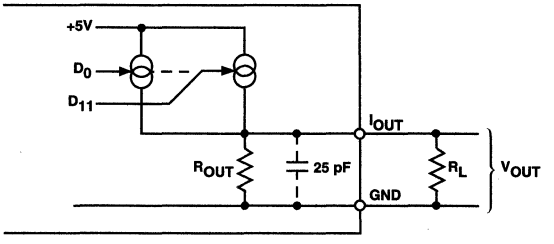


Figure 1. DAC Output Equivalent Circuit

OUTPUT VOLTAGE COMPLIANCE

The maximum voltage that may be realized at the DAC's output, while maintaining rated accuracy and performance, is 1.0 volts. Care should be taken when selecting R_L and I_{OUT} that the resulting Full Scale voltage does not exceed this value. Also, when operating into a summing junction (current mode), be sure the DC voltage of the summing node is below 1.0 Volt.

BUFFERED VOLTAGE OUTPUTS

For applications requiring output voltages greater than 1.0 volts a buffering amplifier will be required. Figure 2 illustrates a typical buffered output application.

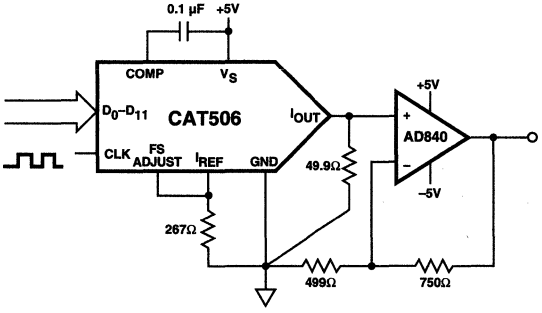


Figure 2. Buffer Voltage Output 0 to +2.5V

FULL SCALE ADJUST

The CAT506 output can be adjusted for any desired level between 0–1.0V or 0–40 mA via the FS_{ADJUST} pin. Referring to Figure 3, I_{REF}, which sets the DAC's Full Scale output current, is controlled by op amp A1. The control loop is configured so that A1 will maintain a constant 0.68 Volts at the FS_{ADJUST} pin. As I_{REF} has a maximum compliance voltage of 1.0 Volt, it is best to use R_{TRIM} as a variable resistor in series with R_{SET} and tie FS_{ADJUST} directly to I_{REF}. This avoids the possibility of the voltage across the combination of $R_{TRIM}$and R_{SET} exceeding I_{REF}'s compliance range.

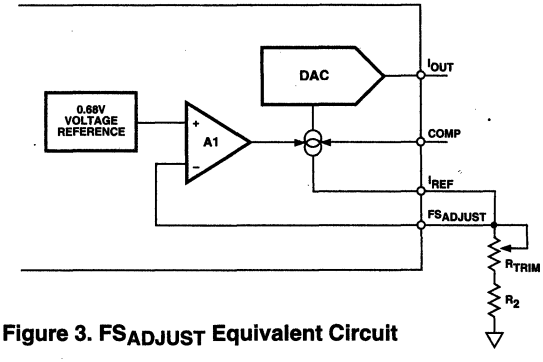


Figure 3. FS_{ADJUST} Equivalent Circuit

USING THE INTERNAL VOLTAGE REFERENCE

A precision voltage reference is provided by the CAT506 to allow for easy adjustment and control of I_{REF}, which sets the DAC full scale output current, I_{OUT}. The relationship between I_{OUT} and I_{REF} is:

$$I_{OUT} = 7.892 * I_{REF}$$

R_{SET} is then calculated from the equation:

$$R_{SET} = \frac{7.892 * V_{REF}}{I_{OUT}}$$

Where $V_{REF} = 0.68$ V.

The internal reference is factory trimmed to compensate for variations in the transfer ratio of I_{REF} to I_{OUT}, making the full scale output voltage accurate to within 0.3% for the transfer function:

$$V_{OUT} = 5.367 * \frac{R_L}{R_{SET}}$$

Full scale output voltage variation from device to device will be ±0.3% when there is perfect tracking between the load and reference current resistors. For optimum performance, R_{SET} and R_L should be a trimmed resistor network with ratio tracking better than ±0.1% and temperature coefficient tracking better than 5 ppm/°C.

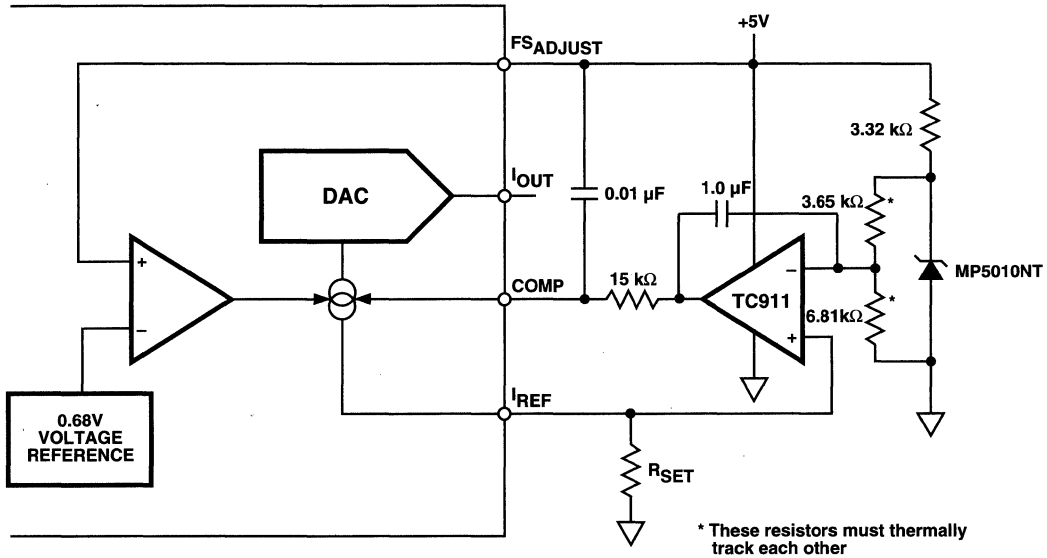


Figure 4a. External Voltage Reference, Single Supply

USING AN EXTERNAL VOLTAGE REFERENCE

The precision voltage reference contained in the CAT506 is factory trimmed by EEPROM circuitry to guarantee a maximum temperature drift of 10 ppm/ °C. For most applications this is more than adequate, however, there may arise occasions when system requirements dictate that an external reference be used. In such cases the on-chip reference can be disabled and control of I_{REF} can be taken off chip.

When using an external reference, the control amplifier's offset and offset drift cannot be ignored. The D/A's output stability is dependent upon not only the reference but the control circuitry around it. For this reason it is recommended that the control amplifier be of the ultra low offset variety, typically < 25μV with a drift of less than 0.1 μV/°C.

Figure 4a shows an example of the CAT506 being used with an external reference in a single supply application. In this circuit, a low drift 1.2 V bandgap reference has been chosen and its voltage divided to 0.8 V by a pair of resistors. This is done to insure that I_{REF} does not exceed its voltage compliance range. The op amp, a low drift chopper stabilized type, replaces the internal control amplifier, which has been de-activated by tying FS_{ADJUST} to the positive supply rail. Control of I_{REF} is effected through the COMP pin which adds an inversion to the control loop (I_{REF} current increases as V_{COMP} -> 0 V).

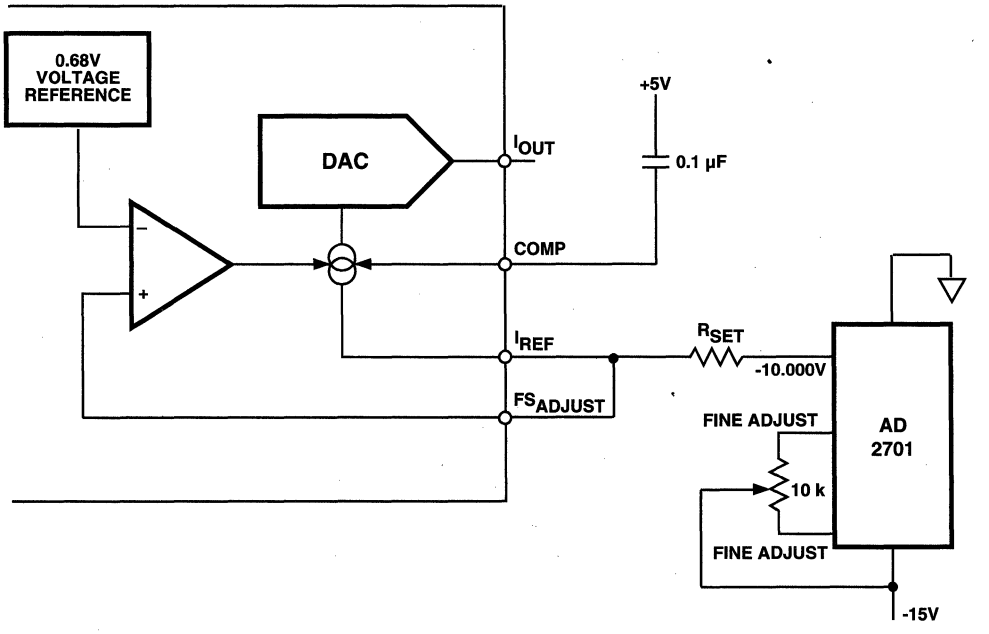
A simpler circuit can be used to incorporate an external voltage reference if a negative supply voltage is available, as shown in Figure 4b. Here, a precision - 10V reference and R_{SET} combine with the CAT506's internal reference and amplifier to set and control I_{REF}. V_{REF} becomes the sum of the internal and external references, and R_{SET} is calculated from the equation

$$R_{SET} = 7.892 * \frac{V_{REF} + 0.68}{I_{OUT}}$$

Since V_{REF} is now the sum of the two references, a large value voltage is chosen for the external reference so that its characteristics will be dominant. Any noise or drift exhibited by the internal reference is now reduced in its effect by the ratio of the two reference voltages.

The internal reference is not precisely 0.68 V, as stated in the equation above, because it is factory adjusted to compensate for variations in the current transfer ratio of I_{OUT} to I_{REF}. To compensate for this, the external voltage reference can be offest by a corresponding amount using the Fine Adjustment feature. For references without this adjustment feature, R_{SET} can be trimmed instead.

Figure 4b. External Voltage Reference, Dual Supply

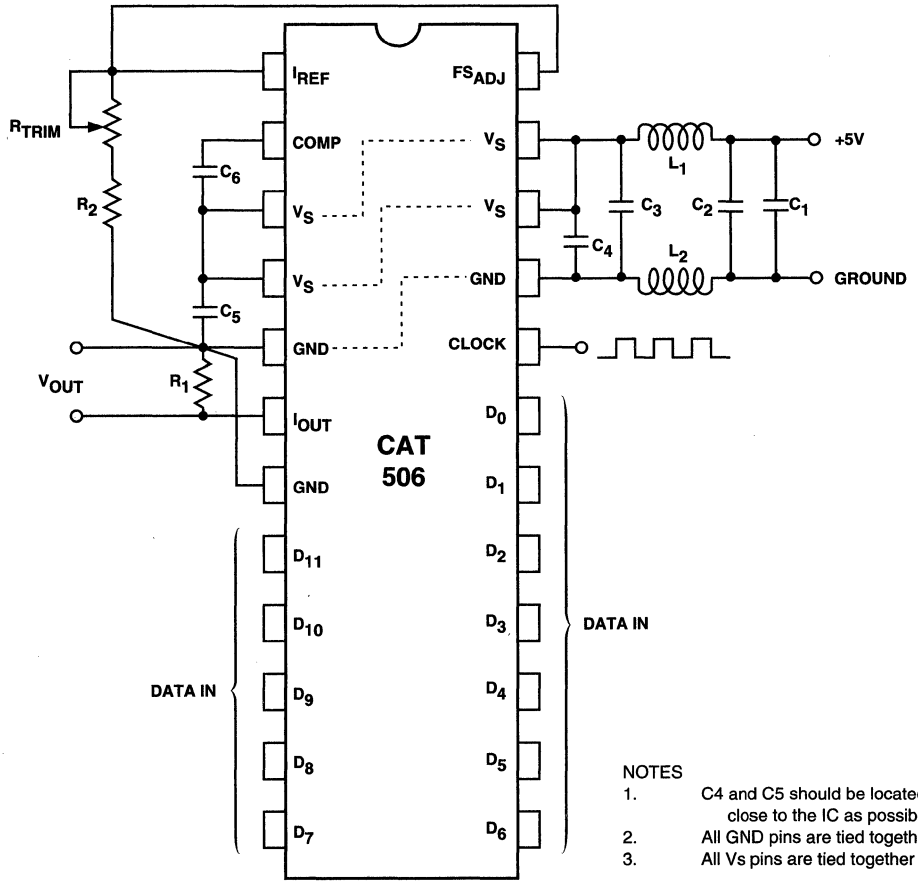


SUPPLY DECOUPLING

It is essential to decouple the power and ground supply lines from the system's main power bus. This prevents glitches and noise spikes generated elsewhere in the system from getting into the DAC and showing up on its output.

Decoupling is best achieved through a filter network placed in series with the DAC's power supply lines. The filter is comprised of two inductors, one in each supply line, combined with several bypass capacitors. An example of this is shown in Figure 5.

Figure 5. Typical Application: Unbuffered Voltage Output, 0–1V



NOTES
1. C4 and C5 should be located as close to the IC as possible
2. All GND pins are tied together
3. All Vs pins are tied together

COMPONENT	DESCRIPTION	SUPPLIER	PART NUMBER
C_6	0.1 µF Ceramic Capacitor	Erie	RPE112Z5U104M50V
C_2	0.01 µF Ceramic Capacitor	Erie	RPE110Z5U103M50V
C_4, C_5	0.01 µF Ceramic Chip Capacitor	Johanson Dielectrics	X7R500S41W103KP
C_1, C_3	22 µF Tantalum Capacitor	Mallory	CSR13G226KM
R_1	24.9Ω !% Metal Film Resistor	Dale	CMF-55C
L_1, L_2	Ferrite Bead	Fair-Rite	2743001111
R_2	121Ω 1% Metal Film Resistor	Dale	CMF-55C
R_{TRIM}	50Ω Cermet Trim Pot	Bourns	3386W

SUPPLY CURRENT

The maximum supply current drawn by the CAT506 can be calculated from the equation:

I_S = Full Scale Output Current (in mA) + 1.2mA per MHz of operating speed.

P.C. BOARD LAYOUT

Combining high speed with high precision presents a formidable challenge to system designers. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding and measurement if optimum performance is to be realized.

BYPASS CAPACITORS

The most important external components associated with any high-speed design are the power supply bypass capacitors. Selection and placement of these capacitors is critical, and to a large extent, dependent upon the specifics of the system's configuration. The key consideration in selection of bypass capacitors is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and metal film capacitors generally feature lower series inductance than the tantalum or electrolytic types.

Bypass capacitors should be installed on the printed circuit board as close to the IC as is physically possible, and with the shortest possible leads in order to minimize series lead inductance. Chip capacitors are optimal in this respect and thus highly recommended.

CRITICAL CONNECTIONS

In using the CAT506 it is of the utmost importance to be sure ***all*** V_S and GND pins are connected to to their respective supplies. Failure to do so will result in improper DAC operation, and may result in damage to the IC.

HIGH-SPEED INTERCONNECT

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. All connections should be short and direct and as physically close to the package as possible. Any conduction path shared by external components should be minimized. When runs exceed an inch or so in length, some type termination resistor may be required. This is true of both the analog and digital sections. For digital signals the termination resistor will be dependent upon the logic family used.

Ground planes should be connected at or near the DAC. Care should be taken to insure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the DAC output signal as well as the supply feeders. The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane.

For maximum AC performance, the DAC should be mounted directly to the circuit board; sockets should not be used as they increase lead inductance and capacitance. Any additional lead inductance or capacitance at the supply pins can seriously undermine dynamic performance. Even Teflon or "pin" sockets can create unwanted results, so soldering directly to the circuit board is highly recommended.

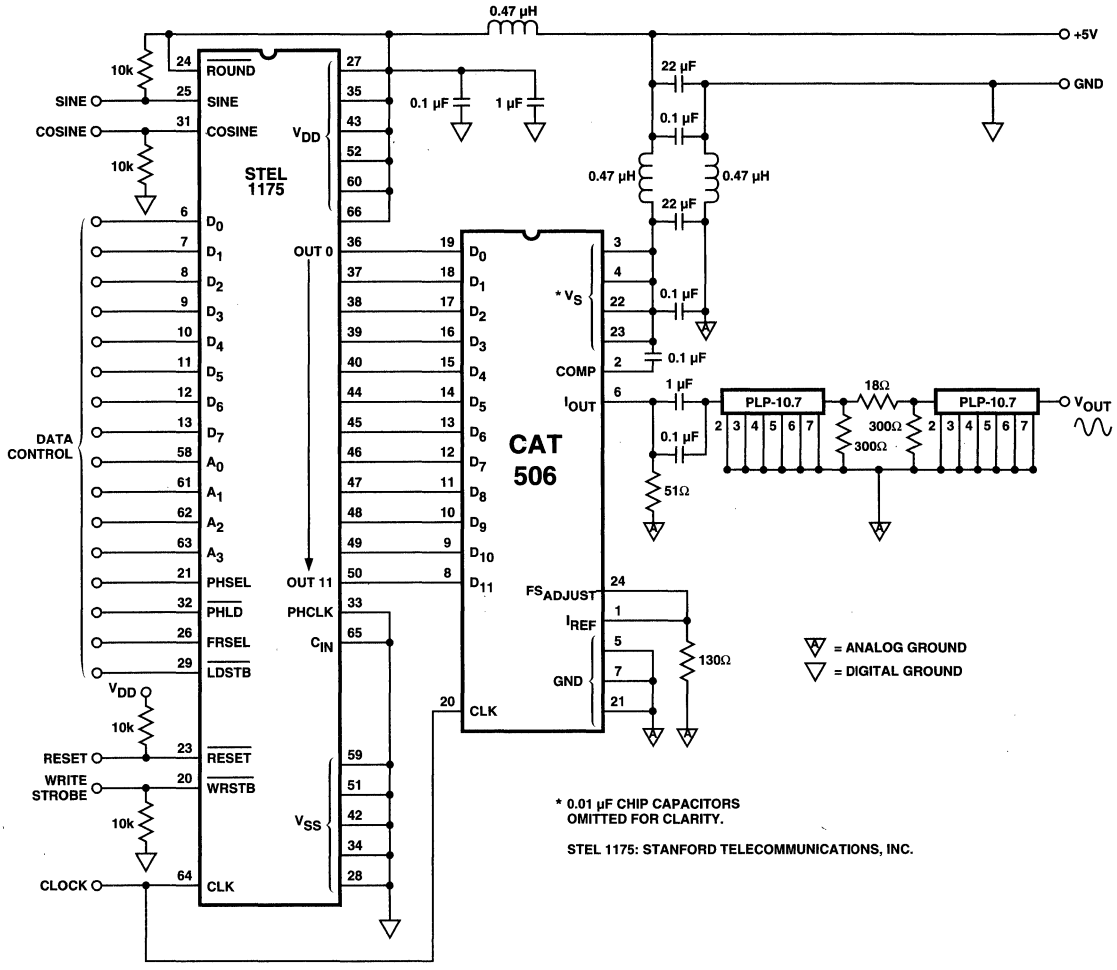
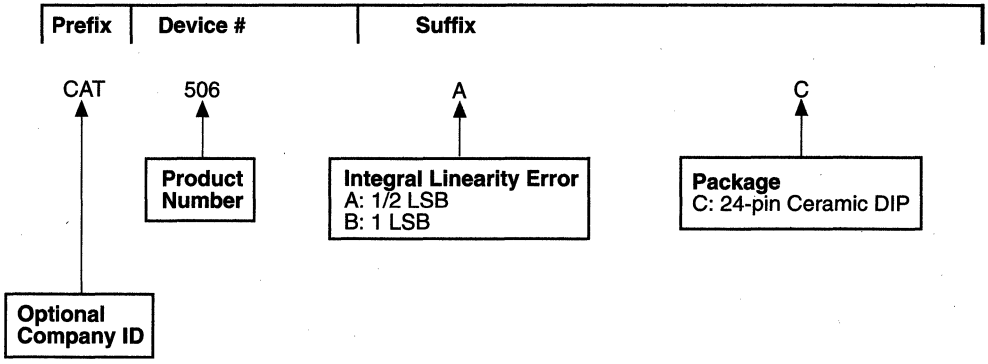


Figure 6. Direct Digital Synthesis (DDS) Using the CAT506

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT506AC (1/2 LSB Integral Linearity Error, Ceramic DIP)

9

CATALYST SEMICONDUCTOR

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Microwire Bus Serial E²PROMs 3

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Using Catalyst's Serial E²PROMs in Shared Input/Output Configuration

Application Staff

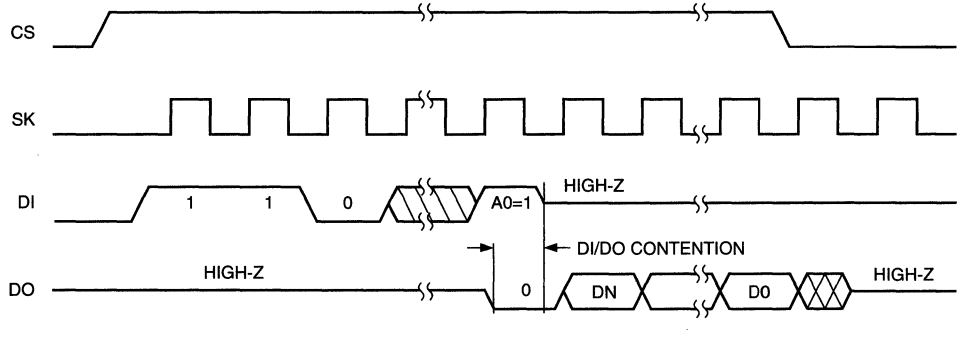
Catalyst Semiconductor's family of serial E²PROMs utilizes 4 signals for the communication interface; Chip Select (CS) for device selection, Serial Clock (SK or CLK) for synchronizing serial data to and from the device, Data Input (DI) to input serial data to the device and Data Output (DO) to output serial data from the device. This interface can be reduced to 3 signals by sharing DI and DO as a common input/output signal. However, the following precautions should be taken to prevent problems due to DI/DO contention:

1) READ instruction in shared DI/DO configuration:
(applies to 93C46, 93C56, 93C57, 93C66 and 93C86)

Data Output Pin (DO) remains in high impedance state while most of the READ instruction (i.e. start bit, opcode and address) is being input and offers no contention to the Data Input Pin (DI) driver in a shared DI/DO configuration (Figure 1a). However, typically 50ns after the rising edge of the serial clock shifts in the least significant bit of the address stream (A0), DO outputs the dummy '0' bit to flag the beginning of the output data stream. If A0 is a '1' and the DI driver has not been disabled by the time the '0' dummy bit becomes valid, a low impedance path between the system power supply and ground is created through the DI driver pullup and DO pulldown device (Figure 1b).

Unless this condition causes excessive noise on the

Figure 1a. DI/DO Contention Timing During Read Cycle



5192 FHD F01

system power supply (which may in turn cause noisy or spurious signals to the device), the READ instruction will continue and complete normally since A0 is already shifted into the device.

To minimize potential problems during this low impedance condition, a current limiting resistor should be placed between the DI driver and the DO pin when in shared DI/DO configuration (Figure 2).

Alternatively, an open drain (or open collector) DI driver with pullup resistor could be used (Figure 2).

In either case, the clocking rate should be slow enough to ensure that the resistor can charge or discharge the shared DI/DO bus capacitance before the appropriate clock edge. For example, if the resistor used is 10KΩ, and the bus capacitance is 100pF, then a safe clock rate is calculated to be:

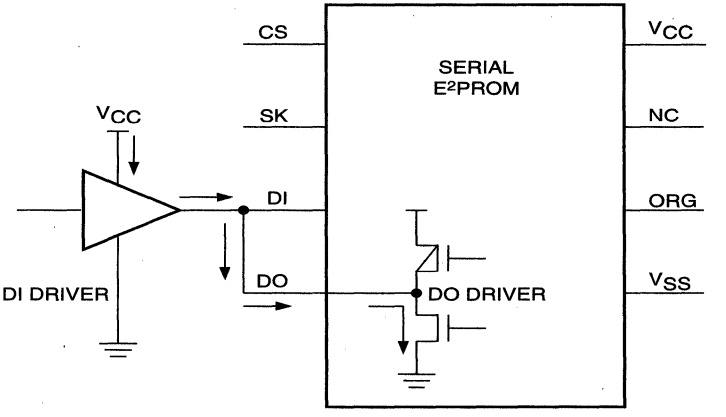
Clock Period (T) = 2 x 3RC
= 2 x 3 x 10kΩ x 100pF
= 6μsec

Frequency (f) = 1 / T
= 167KHz

2) Programming Instructions in shared DI/DO configuration:
(93C46, 93C56, 93C57, 93C66 and 93C86 only)

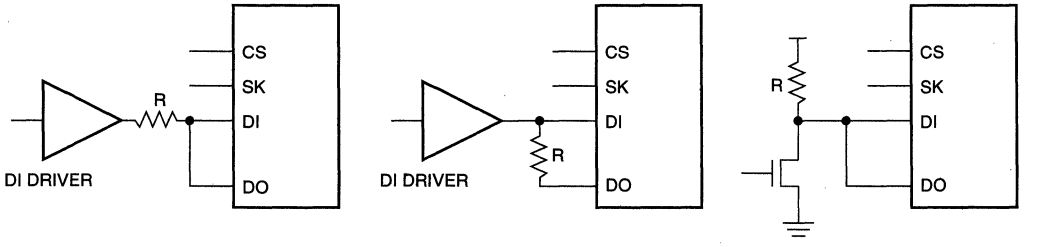
All 3-Wire devices feature self-timed programming cycles. A programming status signal indicates whether the self-timed programming cycle is still in progress or has been completed. A '0' status signal indicates that the device is still programming mode, while a '1' status signal indicates that the programming cycle has been completed and the device is ready to receive the next instruction. This feature will allow a user to minimize the programming time (t_{EW}).

Figure 1b. Current Path



5192 FHD F02

Figure 2. Possible Configurations to Minimize Problems Due to READ Contention



5192 FHD F03

On the 93C46, 93C56, 93C57, 93C66 and 93C86 serial E²PROMs, the programming status signal can be read on the DO pin by bringing CS high after initiating a programming cycle. In a 4-signal interface, after a programming cycle is complete, the status signal is reset to high impedance by the start bit of the next instruction (Figure 3).

In a shared DI/DO configuration, the '1' status signal on DO can be clocked into the device as a start bit and reset the status signal before it can be read. This can interfere with the DI signal of the next instruction cycle. The following steps are recommended to avoid these conditions for a 3-signal interface (Figure 4):

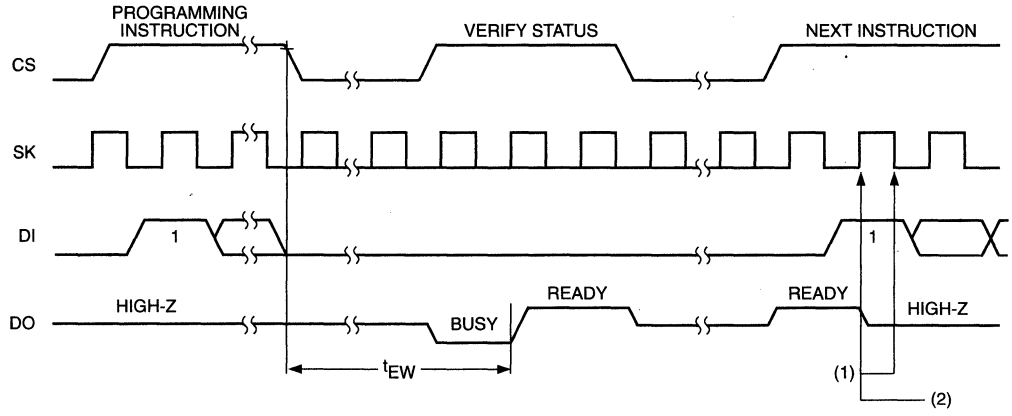
1) The clock (SK) should be stopped after shifting in the programming instruction. This prevents the '1' ready status from resetting the status signal before it can be read.

2) After reading the '1' ready status, at least one clock pulse should be input to the device while the DI/DO signal is '1' in order to reset the status signal.

3) CS should then be brought low to reset the instruction logic.

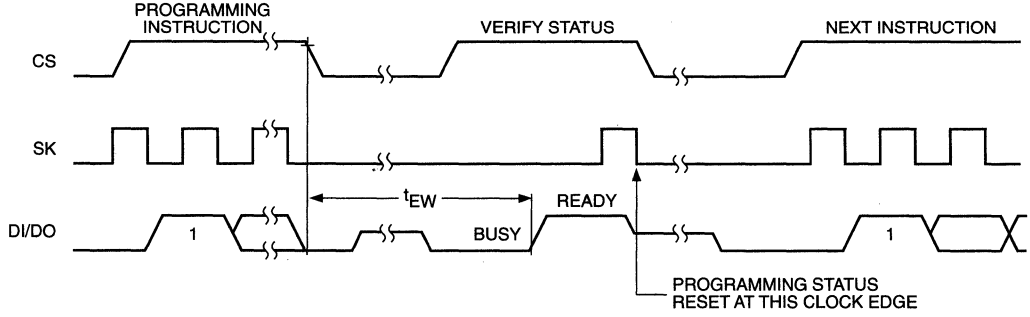
The next instruction can now be executed without any contention from the DO signal.

Figure 3. Programming Instruction and Status Reset with 4-Signal Interface



5192 FHD F04

Figure 4. Programming Instruction and Status Reset with 3-Signal Interface



5192 FHD F05

Notes:
(1) Programming status reset on falling clock edge (93C46).
(2) Programming status reset on rising clock edge (93C46, 93C57, 93C66 and 93C86).

I²C Interface to 8051 Microcontroller

Application Staff

Introduction to I²C

The I²C (Inter-Integrated Circuit) bus is a 2-wire serial bus which provides a small networking system for circuits sharing a common bus. The devices on the bus can vary from microcontrollers to LCD drivers to E²PROMs.

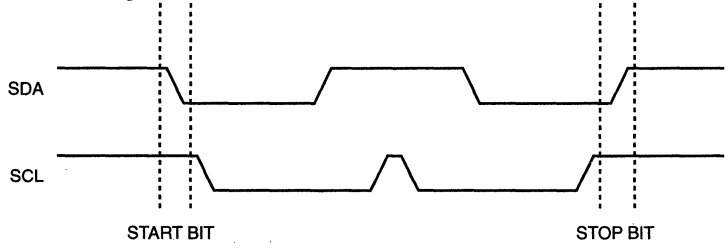
Two bi-directional lines, a serial data (SDA) and a serial clock (SCL) line, transmit data between the devices connected to the bus. Each device has a unique address to differentiate it from the other devices on the bus, and each is configured either as a master or a slave when performing data transfers (see Table 1). A master is the device which initiates a data transfer and generates the clock signals necessary for the transfer. Any device that is addressed is considered a slave. The I²C bus is a multi-master bus, which means that more than one device that is capable of controlling the bus can be connected to it.

Each transmission on the bus begins with the Master sending a Start condition and ends with a Stop condition (see Figure 1). The Master then sends the address of the particular slave device it is requesting. The first four bits of this slave address are fixed as 1010. The next three bits specify a combination of the device address bit(s) and which 2K array of the memory is being addressed (see Figure 2). The last bit of the slave address specifies whether a read or write operation is to be performed. When this bit is a "1", a read operation is performed, and when it is a "0", a write operation is performed.

Table 1. Definition of I²C Bus Terminology

Term	Description
Transmitter	The device which sends the data to the bus.
Receiver	The device which receives the data from the bus.
Master	The device which initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by a master.
Multi-Master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so, and the message is not corrupted.
Synchronization	Procedure to synchronize the clock signals of two or more devices.

Figure 1. START/STOP Timing



5194 FHD F01

Figure 2. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

5194 FHD F07

After the Master sends a Start condition, the slave (E^2PROM) monitors the bus and responds with an acknowledge when its address matches the transmitted slave address (see Figure 3). The device then performs a read or write operation depending on the state of the R/$\overline{W}$ bit.

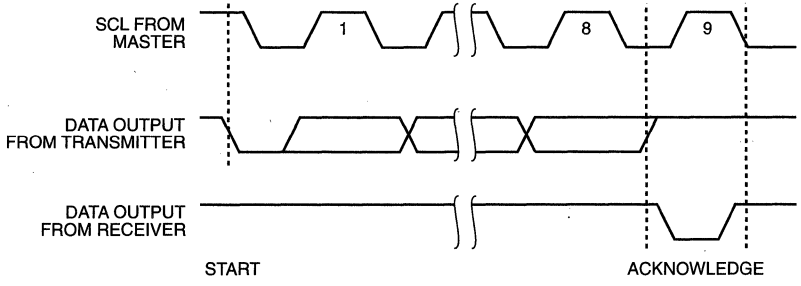
CAT24CXX Interface to 8051 Microcontroller

Catalyst's I^2C family of devices interfaces directly with industry standard microcontrollers such as the Intel MCS-51 family. This family includes 8031/8051 and 8032/8052 (ROMless/ROM) family types.

Catalyst I^2C E^2PROMs are 2-wire interface, nonvolatile memories ranging from 2K bits (CAT24WC02) to 64K bits (CAT24WC64) in density. They adhere to the I^2C protocol which uses 2 lines, a data (SDA) and serial clock (SCL) line for all transmissions, as described above.

The CAT24WC02 E^2PROM has an 8 byte page write buffer and a write protect pin for inadvertent write protection. The CAT24WC04, CAT24WC08 and CAT24WC16 devices have 16 byte page write buffers. Up to eight CAT24WC02 devices, four CAT24WC04 devices, two CAT24WC08 devices and one CAT24WC16 device may be connected to an I^2C bus and addressed independently. The CAT24WC32/64 has a 32-byte Page Write buffer and up to eight devices may be connected to an I^2C bus and addressed independently. Unique addressing is accomplished through hard-wiring address pins A0, A1 and A2 on each device. An example program follows that demonstrates simple byte write and byte read routines as well as page mode and sequential read routines using an 8051 microcontroller. Figure 4 shows a simple hardware interface.

Figure 3. ACKNOWLEDGE Timing



5194 FHD F02

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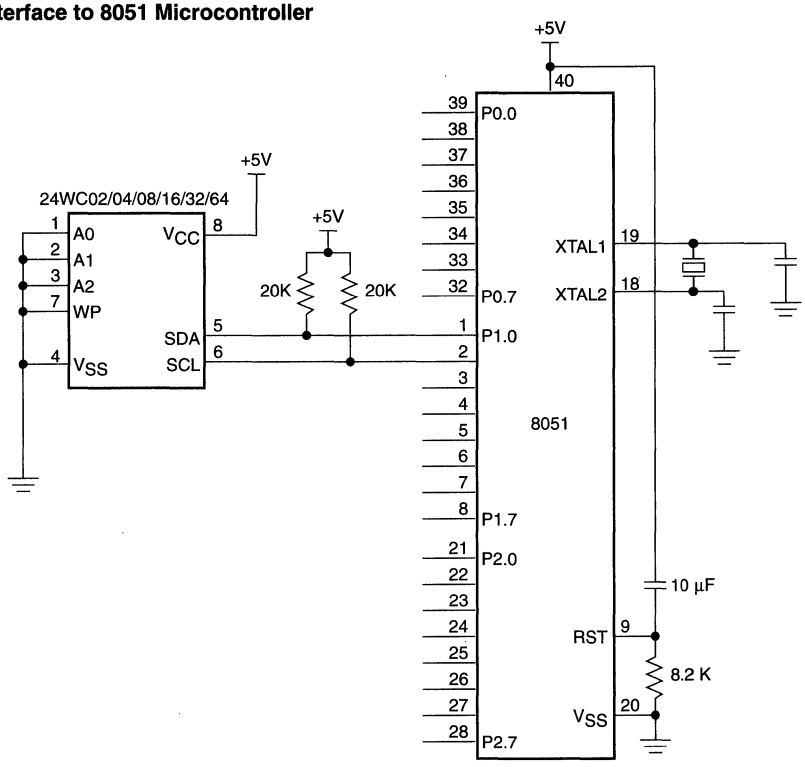
Figure 4. I²C Interface to 8051 Microcontroller



```
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   1

 LOC. OBJECT            LINE    STATEMENT                        I2C_8051.ASM

                         1
;*********************************************************************
                         2    ; THE FOLLOWING CODE SHOWS AN INTERFACE BETWEEN AN 8051
MICROCONTROLLER
                         3    ; AND CATALYST'S I2C FAMILY OF EEPROMS.
                         4    ;
                         5    ; IT DEMONSTRATES A BYTE WRITE/BYTE READ ROUTINE AND A PAGE MODE
                         6    ; WRITE/SEQUENTIAL READ ROUTINE.  IT USES TWO LINES FROM PORT 1
                         7    ; (P1.0 AND P1.1) OF THE 8051 TO COMMUNICATE WITH THE CAT24CXX.
                         8    ;
                         9    ; THIS PROGRAM WILL WORK WITH THE CAT24WC02/04/08/16 DEVICES.
NOTE:
                        10    ; THE 24WC02 HAS AN 8 BYTE PAGE BUFFER AND 24WC04/08/16 HAVE A
                        11    ; 16-BYTE PAGE
BUFFER.;*********************************************************************
                        12
    0090                13    SCL         BIT     P1.0                ;SCL BIT IS PORT 1,
BIT 0
    0091                14    SDA         BIT     P1.1                ;SDA BIT IS PORT 1,
BIT 1
    0005                15    SLV_ADDR    EQU     0101B               ;FIXED SLAVE ADDRESS
BITS
    REG                  16    DATAOUT     EQU     R5                      ;DATA READ
FROM DEVICE
    0085                17    ACK_READ    EQU     10000101B           ;READ FOR ACK POLLING
                        18
 —                      19                DSEG
 0030                   20                ORG     0030H
                        21
 0030                   22    PAGE_DATA:  DS      1
 0031                   23    BLK_ADDR:   DS      1
 0032                   24    BYTE_ADDR:  DS      1
 0033                   25    BYTE_DATA:  DS      1
                        26
 0040                   27                ORG     40H
 0040                   28    STACK:      DS      31
                        29
 —                      30                CSEG
 0040                   31                ORG     0040H
 0040 02 01 00           32                LJMP    BEGIN
                        33
 0100                   34                ORG     0100H
 0100 75 81 40           35    BEGIN:      MOV     SP,#STACK               ;INITIALIZE
STACK POINTER
                        36
 0103 75 31 00           37                MOV     BLK_ADDR,#000B          ;INITIALIZE 2K
BLOCK
 0106 75 33 55           38                MOV     BYTE_DATA,#55H          ;BYTE DATA
 0109 75 32 00           39                MOV     BYTE_ADDR,#00H          ;BYTE ADDRESS
 010C 75 30 AA           40                MOV     PAGE_DATA,#0AAH         ;PAGE DATA
                        41
 010F 31 45 [0145]      42                ACALL   PAGE_WR                 ;CALL PAGE WRITE
ROUTINE
 0111 51 1D [021D]      43                ACALL   SEQ_RD                  ;CALL SEQ. READ
ROUTINE
 0113 31 1A [011A]      44                ACALL   BYTE_WR                 ;CALL BYTE WRITE
ROUTINE
 0115 31 D6 [01D6]      45                ACALL   SELECT_RD               ;CALL BYTE READ
```

```
ROUTINE
 0117 02 01 17              46     DONE:       LJMP    DONE                    ;LOOP UNTIL
RESET OCCURS
                           47
                           48     ;****************************************
                           49
                           50     ;************** BYTE WRITE *****************
                           51
 011A 31 95 [0195]         52     BYTE_WR:    ACALL   START_BIT               ;SEND START BIT
 011C 74 05                53                 MOV     A,#SLV_ADDR             ;FIRST 4 SLAVE AD-
DRESS
 011E 7F 04                54                 MOV     R7,#4H                  ;BITS
 0120 31 89 [0189]         55                 ACALL   SHFTO
 0122 E5 31                56                 MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
 0124 7F 03                57                 MOV     R7,#3H
 0126 31 89 [0189]         58                 ACALL   SHFTO
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   2

 LOC. OBJECT            LINE     STATEMENT                          I2C_8051.ASM

 0128 74 00                59                 MOV     A,#00H                  ;R/W BIT SET TO 0 FOR
 012A 7F 01                60                 MOV     R7,#1H                  ;WRITE
 012C 31 89 [0189]         61                 ACALL   SHFTO
 012E 31 AA [01AA]         62                 ACALL   SLAVE_ACK
                           63
 0130 E5 32                64                 MOV     A,BYTE_ADDR             ;BYTE ADDRESS
 0132 7F 08                65                 MOV     R7,#8H
 0134 31 89 [0189]         66                 ACALL   SHFTO
 0136 31 AA [01AA]         67                 ACALL   SLAVE_ACK
 0138 E5 33                68                 MOV     A,BYTE_DATA             ;BYTE DATA
 013A 7F 08                69                 MOV     R7,#8H
 013C 31 89 [0189]         70                 ACALL   SHFTO
 013E 31 AA [01AA]         71                 ACALL   SLAVE_ACK
 0140 31 A1 [01A1]         72                 ACALL   STOP_BIT                ;STOP BIT
 0142 31 74 [0174]         73                 ACALL   ACK_POL                 ;CALL ACK POLLING,
WAIT
 0144 22                   74                 RET                             ;FOR END OF WRITE
CYCLE
                           75     ;****************************************
                           76
                           77     ;************** PAGE WRITE *****************
                           78
 0145 31 95 [0195]         79     PAGE_WR:    ACALL   START_BIT               ;SEND START BIT
 0147 74 05                80                 MOV     A,#SLV_ADDR             ;FIRST 4 SLAVE AD-
DRESS
 0149 7F 04                81                 MOV     R7,#4H                  ;BITS
 014B 31 89 [0189]         82                 ACALL   SHFTO
 014D E5 31                83                 MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
 014F 7F 03                84                 MOV     R7,#3H
 0151 31 89 [0189]         85                 ACALL   SHFTO
 0153 74 00                86                 MOV     A,#00H                  ;R/W BIT SET TO 0 FOR
 0155 7F 01                87                 MOV     R7,#1H                  ;WRITE
 0157 31 89 [0189]         88                 ACALL   SHFTO
 0159 31 AA [01AA]         89                 ACALL   SLAVE_ACK
 015B E5 32                90                 MOV     A,BYTE_ADDR             ;BYTE ADDRESS
 015D 7F 08                91                 MOV     R7,#8H
 015F 31 89 [0189]         92                 ACALL   SHFTO
 0161 31 AA [01AA]         93                 ACALL   SLAVE_ACK
 0163 7C 0F                94                 MOV     R4,#0FH
                           95     NEXT_DATA:                                  ;WRITE 16 BYTES TO
 0165 E5 30                96                 MOV     A,PAGE_DATA             ;EEPROM
 0167 7F 08                97                 MOV     R7,#8H
```

```
 0169 31 89 [0189]    98                ACALL   SHFTO
 016B 31 AA [01AA]    99                ACALL   SLAVE_ACK
 016D DC F6 [0165]   100                DJNZ    R4,NEXT_DATA
 016F 31 A1 [01A1]   101                ACALL   STOP_BIT
 0171 31 74 [0174]   102                ACALL   ACK_POL                 ;CALL ACK
POLLING,WAIT
 0173 22             103                RET                             ;FOR END OF WRITE
CYCLE
                     104    ;****************************************
                     105
                     106    ;************** ACK_POL ********************
                     107
 0174 7B 40          108    ACK_POL:    MOV     R3,#40H                 ;# OF TIMES TO POLL
 0176 DB 02 [017A]   109    ACK_LOOP:   DJNZ    R3,DONE_YET             ;DEVICE
 0178 80 0C [0186]   110                SJMP    DN_ACKPOL
 017A 31 95 [0195]   111    DONE_YET:   ACALL   START_BIT               ;SEND START BIT
 017C 74 85          112                MOV     A,#ACK_READ             ;SEND READ
 017E 7F 08          113                MOV     R7,#8H
 0180 31 89 [0189]   114                ACALL   SHFTO
 0182 31 AA [01AA]   115                ACALL   SLAVE_ACK               ;SEND ACKNOWLEDGE
 0184 40 F0 [0176]   116                JC      ACK_LOOP                ;LOOP IF NO ACK RCVD,
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   3

 LOC. OBJECT            LINE    STATEMENT                          I2C_8051.ASM

                     117                                                ;JUMP IF ACK RCVD
 0186 31 A1 [01A1]   118    DN_ACKPOL:  ACALL   STOP_BIT                ;SEND STOP BEFORE
RETURN
 0188 22             119                RET
                     120    ;****************************************
                     121
                     122    ;************** SHFTO **********************
                     123
 0189 C2 90          124    SHFTO:      CLR     SCL
 018B C2 90          125    NXTSHF:     CLR     SCL
 018D 13             126                RRC     A                       ;ROTATE DATA INTO
CARRY
 018E 92 91          127                MOV     SDA,C                   ;SEND CARRY TO SDA
 0190 D2 90          128                SETB    SCL
 0192 DF F7 [018B]   129                DJNZ    R7,NXTSHF
 0194 22             130                RET
                     131    ;****************************************
                     132
                     133    ;************** START BIT ******************
                     134
 0195 D2 90          135    START_BIT:  SETB    SCL                     ;START BIT
 0197 00             136                NOP
 0198 D2 91          137                SETB    SDA
 019A 00             138                NOP
 019B C2 91          139                CLR     SDA
 019D 00             140                NOP
 019E C2 90          141                CLR     SCL
 01A0 22             142                RET
                     143    ;****************************************
                     144
                     145    ;************** STOP BIT ******************
                     146
 01A1 C2 91          147    STOP_BIT:   CLR     SDA                     ;STOP BIT
```

```
 01A3 00            148                NOP
 01A4 D2 90         149                SETB   SCL
 01A6 00            150                NOP
 01A7 D2 91         151                SETB   SDA
 01A9 22            152                RET
                    153    ;*****************************************
                    154
                    155    ;************** SLAVE ACKNOWLEDGE **********
                    156
 01AA 00            157    SLAVE_ACK:  NOP
 01AB 00            158                NOP
 01AC C2 90         159                CLR    SCL                      ;SLAVE ACKNOWLEDGE
BIT
 01AE 00            160                NOP
 01AF D2 91         161                SETB   SDA
 01B1 00            162                NOP
 01B2 00            163                NOP
 01B3 D2 90         164                SETB   SCL
 01B5 00            165                NOP
 01B6 00            166                NOP
 01B7 00            167                NOP
 01B8 A2 91         168                MOV    C,SDA                    ;READ STATE OF SDA,
 01BA C2 90         169                CLR    SCL                      ;SAVE TO CARRY
 01BC 22            170                RET
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   4

 LOC. OBJECT            LINE    STATEMENT                        I2C_8051.ASM

                    171    ;*****************************************
                    172
                    173    ;************** MASTER ACKNOWLEDGE *********
                    174
                    175    MSTR_ACK:
 01BD C2 90         176                CLR    SCL                      ;MASTER ACKNOWLEDGE
BIT
 01BF 00            177                NOP
 01C0 C2 91         178                CLR    SDA
 01C2 00            179                NOP
 01C3 00            180                NOP
 01C4 D2 90         181                SETB   SCL
 01C6 00            182                NOP
 01C7 C2 90         183                CLR    SCL
 01C9 00            184                NOP
 01CA D2 91         185                SETB   SDA
 01CC 22            186                RET
                    187    ;*****************************************
                    188
                    189    ;************** NO ACKNOWLEDGE *************
                    190
 01CD D2 91         191    NO_ACK:     SETB   SDA                      ;NO ACKNOWLEDGE
 01CF 00            192                NOP
 01D0 D2 90         193                SETB   SCL
 01D2 00            194                NOP
 01D3 C2 90         195                CLR    SCL
 01D5 22            196                RET
                    197    ;*****************************************
                    198
                    199    ;************** SELECTIVE READ *************
```

```
                    200
                    201     SELECT_RD:
 01D6 31 95 [0195]  202                 ACALL   START_BIT               ;START BIT
                    203
 01D8 74 05         204                 MOV     A,#SLV_ADDR             ;DUMMY WRITE TO FIRST
 01DA 7F 04         205                 MOV     R7,#4H                  ;2K BLOCK
 01DC 31 89 [0189]  206                 ACALL   SHFTO
 01DE E5 31         207                 MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
 01E0 7F 03         208                 MOV     R7,#3H
 01E2 31 89 [0189]  209                 ACALL   SHFTO
 01E4 74 00         210                 MOV     A,#00H                  ;R/W BIT SET TO 0
 01E6 7F 01         211                 MOV     R7,#1H                  ;FOR WRITE
 01E8 31 89 [0189]  212                 ACALL   SHFTO
 01EA 31 AA [01AA]  213                 ACALL   SLAVE_ACK               ;SEND ACKNOWLEDG
                    214
 01EC E5 32         215                 MOV     A,BYTE_ADDR             ;ADDRESS TO READ
 01EE 7F 08         216                 MOV     R7,#8H
 01F0 31 89 [0189]  217                 ACALL   SHFTO
 01F2 31 AA [01AA]  218                 ACALL   SLAVE_ACK
                    219
 01F4 31 95 [0195]  220                 ACALL   START_BIT               ;NEW START BIT
                    221
 01F6 74 05         222                 MOV     A,#SLV_ADDR
 01F8 7F 04         223                 MOV     R7,#4H
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   5

 LOC. OBJECT            LINE    STATEMENT                       I2C_8051.ASM

 01FA 31 89 [0189]  224                 ACALL   SHFTO
 01FC E5 31         225                 MOV     A,BLK_ADDR              ;2K BLOCK TO READ
 01FE 7F 03         226                 MOV     R7,#3H
 0200 31 89 [0189]  227                 ACALL   SHFTO .
 0202 74 01         228                 MOV     A,#1H                   ;R/W BIT SET TO 1
 0204 7F 01         229                 MOV     R7,#1H                  ;FOR READ
 0206 31 89 [0189]  230                 ACALL   SHFTO
 0208 31 AA [01AA]  231                 ACALL   SLAVE_ACK
                    232
 020A 7F 08         233                 MOV     R7,#8H
 020C D2 90         234     CLOCK8:     SETB    SCL                     ;CLOCK IN DATA
 020E 00            235                 NOP
 020F A2 91         236                 MOV     C,SDA
 0211 C2 90         237                 CLR     SCL
 0213 ED            238                 MOV     A,DATAOUT
 0214 33            239                 RLC     A                       ;ROTATE NEXT BIT
 0215 FD            240                 MOV     DATAOUT,A               ;SAVE ROTATED DATA
 0216 DF F4 [020C]  241                 DJNZ    R7,CLOCK8               ;READ 8 BITS OF DATA
 0218 31 CD [01CD]  242                 ACALL   NO_ACK
 021A 31 A1 [01A1]  243                 ACALL   STOP_BIT
 021C 22            244                 RET
                    245     ;*****************************************
                    246
                    247     ;************** SEQUENTIAL READ ************
                    248
                    249     SEQ_RD:
 021D 31 95 [0195]  250                 ACALL   START_BIT               ;START BIT
                    251
 021F 74 05         252                 MOV     A,#SLV_ADDR             ;DUMMY WRITE TO FIRST
 0221 7F 04         253                 MOV     R7,#4H                  ;2K BLOCK
 0223 31 89 [0189]  254                 ACALL   SHFTO
 0225 E5 31         255                 MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
 0227 7F 03         256                 MOV     R7,#3H
```

```
 0229 31 89 [0189]   257                ACALL   SHFTO
 022B 74 00          258                MOV     A,#00H                  ;R/W BIT SET TO 0
 022D 7F 01          259                MOV     R7,#1H                  ;FOR WRITE
 022F 31 89 [0189]   260                ACALL   SHFTO
 0231 31 AA [01AA]   261                ACALL   SLAVE_ACK
                     262
 0233 E5 32          263                MOV     A,BYTE_ADDR             ;ADDRESS TO READ
 0235 7F 08          264                MOV     R7,#8H
 0237 31 89 [0189]   265                ACALL   SHFTO
 0239 31 AA [01AA]   266                ACALL   SLAVE_ACK
                     267
 023B 31 95 [0195]   268                ACALL   START_BIT               ;NEW START BIT
                     269
 023D 74 05          270                MOV     A,#SLV_ADDR
 023F 7F 04          271                MOV     R7,#4H
 0241 31 89 [0189]   272                ACALL   SHFTO
 0243 E5 31          273                MOV     A,BLK_ADDR              ;2K BLOCK TO READ
 0245 7F 03          274                MOV     R7,#3H
 0247 31 89 [0189]   275                ACALL   SHFTO
 0249 74 01          276                MOV     A,#1H                   ;R/W BIT SET TO 1
 024B 7F 01          277                MOV     R7,#1H                  ;FOR READ
 024D 31 89 [0189]   278                ACALL   SHFTO
 024F 31 AA [01AA]   279                ACALL   SLAVE_ACK
                     280
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   6

 LOC. OBJECT            LINE    STATEMENT                          I2C_8051.ASM

 0251 7E 0F          281                MOV     R6,#0FH
 0253 7F 08          282    NXT_BYTE:   MOV     R7,#8H
 0255 D2 90          283    ONE_BYTE:   SETB    SCL                     ;READ 16 BYTES OF
DATA
 0257 00             284                NOP
 0258 C2 90          285                CLR     SCL
 025A 00             286                NOP
 025B DF F8 [0255]   287                DJNZ    R7,ONE_BYTE
 025D 31 BD [01BD]   288                ACALL   MSTR_ACK                ;ACKNOWLEDGE
 025F DE F2 [0253]   289                DJNZ    R6,NXT_BYTE
                     290
 0261 7F 08          291                MOV     R7,#8H
 0263 D2 90          292    LST_BYTE:   SETB    SCL
 0265 00             293                NOP                             ;READ LAST BYTE
 0266 C2 90          294                CLR     SCL
 0268 00             295                NOP
 0269 DF F8 [0263]   296                DJNZ    R7,LST_BYTE
 026B 31 CD [01CD]   297                ACALL   NO_ACK                  ;NO ACKNOWLEDGE
 026D 31 A1 [01A1]   298                ACALL   STOP_BIT                ;STOP BIT
 026F 22             299                RET
                     300    ;****************************************
                     301    END



ASSEMBLY END , ERRORS:0
LAST CODE ADDRESS:026F
```

CAT64LC10: A User-Friendly Serial E²PROM

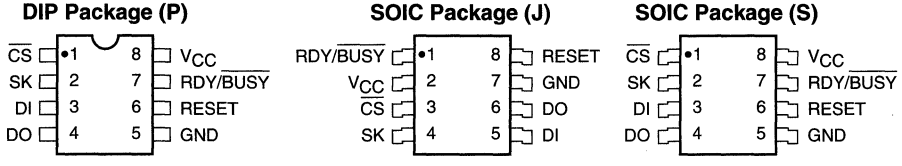
Application Staff

INTRODUCTION

The CAT64LC10, a 1K bit serial E²PROM device, has a configuration of 64 registers by 16 bits(1). Pin configurations are provided in Figure 1. The features that separate this particular device from 2-Wire, 3-Wire and 4-Wire Catalyst serial E²PROMs include:

- RESET pin which can inhibit any write/erase operation from being executed. It can also abort a write/erase operation that is in progress. This feature adds data protection from inadvertent write in addition to the erase/write enable (EWEN) instruction.
- Instructions and data are latched into the input of the device at the rising-edge of the SK clock. Data output from the device is clocked out at the falling-edge of the SK clock. This is useful for interfacing to the SPI bus of Motorola microprocessors.
- $\overline{CS}$ (Chip select) must be low to select the device. This is also useful for interfacing to the SPI bus of Motorola microprocessors.
- Two methods for displaying Ready/$\overline{BUSY}$ status:
  1. RDY/$\overline{BUSY}$ pin which normally outputs a logic low when the device is in a programming cycle.
  2. Enable $\overline{CS}$ which will cause DO to output a logic low while the device is programming. As soon as the programming cycle is completed, the DO pin will output a logic high if $\overline{CS}$ is enabled. This "READY" status will be available from the DO pin any time $\overline{CS}$ is enabled. To reset the "READY" status on the DO pin, simply enable $\overline{CS}$, and then enter a logic high on the DI pin. The first rising edge of the SK clock after DI has become "high" will cause the DO pin to return to high impedance.
- Every instruction is a multiple of 16 bits (8 bits of opcode and an 8 bit address or 8 dummy bits). READ or WRITE instructions require an additional 16 bits of data.
- Every instruction begins with a start sequence of "1010". Prior 4 bit sequences other than "1010" will be ignored. For example, starting sequences such as "1000", "1100", "1001" or "1111", etc. will be ignored.

Figure 1. Pin Configurations for CAT64LCXX Devices



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Note:
(1) Catalyst SPI bus serial E²PROMs are available in densities of 1K, 2K and 4K bits. See Section 4 of this data book.

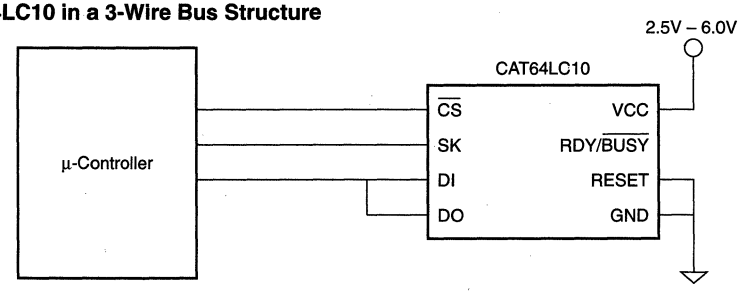
WHY IS THE CAT64LC10 USER-FRIENDLY?

- Can be configured in a Microwire 3-wire bus structure by simply connecting the DI and DO pins together (see Figure 2). The Ready/$\overline{\text{BUSY}}$ status is obtained from the DO pin.
- Can be configured in a 4-wire bus structure (see Figure 3). In this instance, the Ready/$\overline{\text{BUSY}}$ status is available directly from the RDY/$\overline{\text{BUSY}}$ pin.
- Shifts data in and out at opposite edges of the clock, which makes it easy to interface to microcontrollers by using the system clock instead of having to internally generate a separate clock for serial data transfer. This feature saves code space and effort in terms of software development.
- Protocol is compatible with SPI interface.
- Pin-controlled data protection.

HOW IS THE CAT64LC10 COMPATIBLE WITH THE SPI BUS?

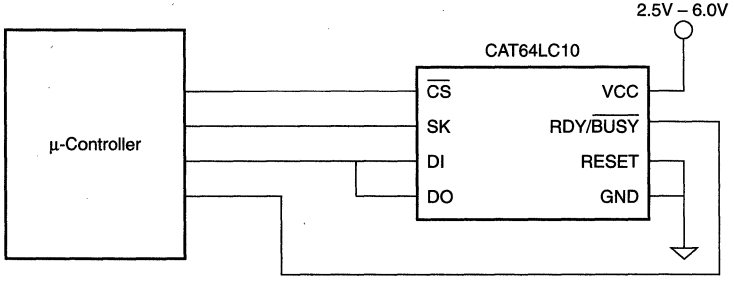
- The CAT64LC10 accepts a logic low on $\overline{\text{CS}}$ to be selected. Input of instructions and data are clocked in from the DI pin at the rising edge of the clock. When outputting data, the device will shift out data at the falling edge of the clock (see Figure 4). This interface complies with Motorola's SPI interface.

Figure 2. CAT64LC10 in a 3-Wire Bus Structure



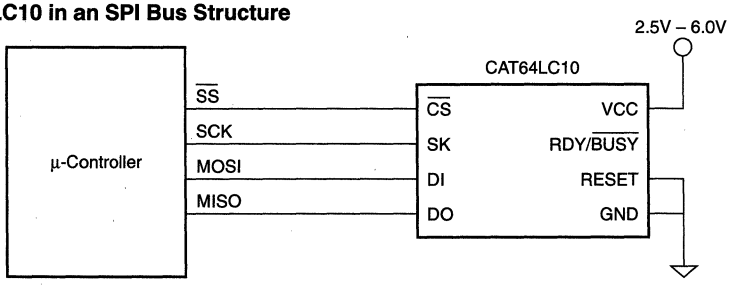
5197 FHD F01

Figure 3. CAT64LC10 in a 4-Wire Bus Structure



5197 FHD F02

Figure 4. CAT64LC10 in an SPI Bus Structure



5197 FHD F03

DATA PROTECTION

- Software Protection: EWEN/EWDS instructions are erase/write enabling and disabling instructions which can protect the device from inadvertently writing over the data.
- Pin Controlled Protection: By setting the RESET pin high, write instructions cannot be executed. The device will ignore the input of a WRITE or WRAL instruction if the RESET pin is held high anywhere during the input of instructions or addresses for more than one clock. However, if the RESET pin is held high after the input of the last address bit for more than one clock, the device will abort the WRITE or WRAL instruction and output a READY status.

CAUTION: Interrupting a programming cycle which is in progress can have unpredictable results in terms of data integrity and is therefore not recommended.

How to Use Catalyst Secure Access Serial E²PROMs

Applications Staff

INTRODUCTION

This application note is intended to be a tutorial on the use of CAT35C704A/35C804A Secure Access Serial E²PROMs. Device operation and typical applications for the device are shown as well as examples for each of the instructions available.

DEVICE OPERATION

The CAT35C704A/35C804A is a 4K bit Secure Access Serial E²PROM that can be used in applications that require nonvolatile memory storage and a need to protect the contents of that memory from unauthorized access. Two basic modes of operation are available, protected and unprotected. In the unprotected mode, with the memory pointer set to "0", the device operates like a standard E²PROM, allowing full read/write access to the entire array.

Using the memory pointer the user can determine how much memory needs protection. With the WMPR command, a pointer value can be set to split the memory array into two blocks. Addresses above the pointer value offer full Read/Write access; addresses below and including the pointer are Read only (see Figure 1).

In the protected mode, up to 8 bytes of password security are available. Once the password has been set and a disable access (DISAC) command (or power down) has been executed, the device becomes inaccessible with only the portion of the array not protected by memory pointer readable (see Figure 2). Upon power up, the correct password must be sent to the device before any writing or moving of the memory pointer can be done. This scheme lends itself to applications where users are allowed to view only those portions of memory that is intended for them to see. For example, an application where data is uncovered in the array (by moving the memory pointer) to make available to the user certain features/options that they require, as in the cable TV industry (see Figure 3).

Among the 19 instructions available with the CAT35C704A/35C804A is a Read Status Register (RSR) instruction, which lets a system interrogate the device and determine its working status. The 8 bit status register displays information regarding parity errors, instruction errors and RDY/$\overline{\text{BUSY}}$ status. An organization instruction (ORG) is also available for organizing the memory into either 512x8 or 256x16 configurations depending on the application.

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Figure 1. Access Control Using No Access Code

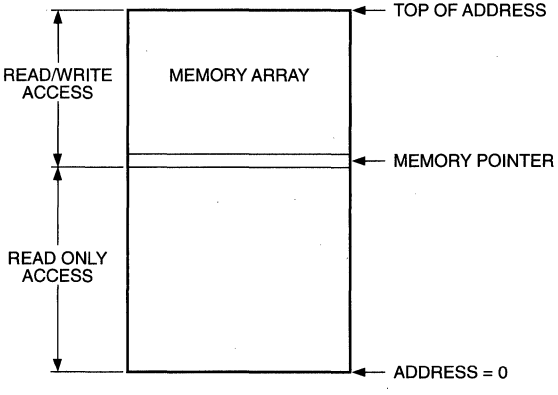

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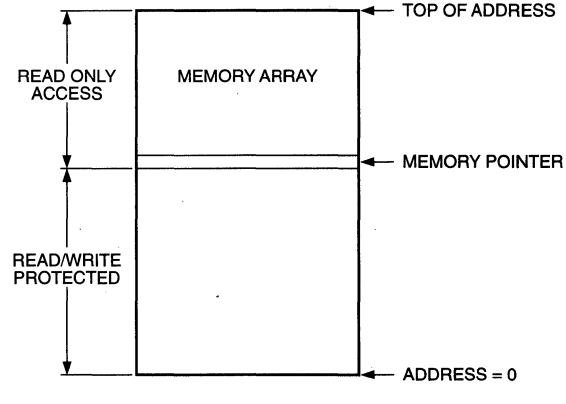
Figure 2. Access Control Using Access Code



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In addition, to allow for reading multiple words from the memory and minimize the overhead of repeated Read instructions, a Read Sequential (RSEQ) instruction allows you to specify a starting location and then continuously shift out data to the end of the array.

The security code is entered/modified by sending the Modify Access Code (MACC) instruction followed by the length of the access code (1 to 8 bytes), the old access code (if needed), and then the new access code twice (for verification). Once power has been removed (or the DISAC instruction sent), the Enable Access (ENAC) instruction, followed by the correct access code, must be sent to the device or the memory array's protected portion cannot be accessed, and the memory contents above the pointer remain Read only.

A simple interface is shown in Figure 4 where the CAT35C704 is used in an electronic key application. The device interfaces directly to a microprocessor and is used as the security portion of a door lock mechanism. The lock is only activated when the key's (hotel key, car key, etc.) access code matches the one stored in the CAT35C704.

Figure 3. Using CAT35C704A/35C804A for Protected Features

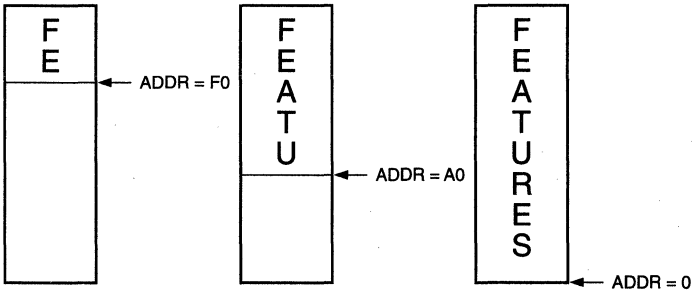

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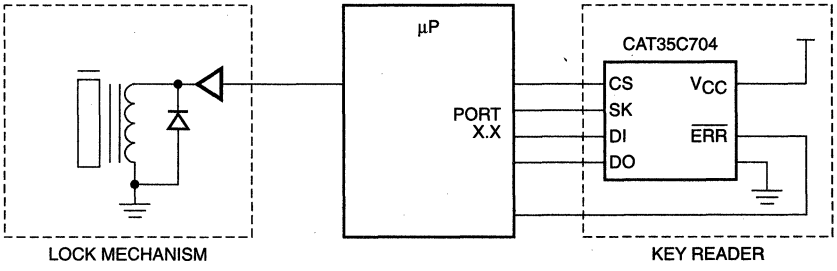
Figure 4. CAT35C704 in an Electronic Key



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INSTRUCTION SET

The following section describes the 19 instructions available for the device and examples of each.

SECURITY OR WRITE PROTECT INSTRUCTIONS

1. **MACC**–Modify Access Code

This instruction allows the user to issue a new password to the device or modify an existing one. The password is issued in the following manner:

1101	[Length of new pswrd]	[old pswrd]	[new pswrd]	[new pswrd]

For example, to issue the device a password for the first time, send the following:

1101	3	AA 55 D2	AA 55 D2
Instruction Code	*Length*	*3-Byte Pswrd*	*Repeat 3-Byte Pswrd*

The device now has a 3 byte password of AA 55 D2. To change this password to a 5 byte password, send the following:

1101	5	AA 55 D2	01 02 03 04 05	01 02 03 04 05
Instruction Code	*Length of New Pswrd*	*Old Pswrd*	*New Pswrd*	*Repeat New Pswrd*

The device now has a 5 byte password equal to 01 02 03 04 05. This password can be modified in the same manner to any length password you choose, up to 8 bytes.

Finally, to modify the password back to a 0 length (no password), send the device the following instruction:

1101	0	01 02 03 04 05
Instruction Code	*Length of New Pswrd*	*Old Pswrd*

The device is now in the unprotected mode.

2. **ENAC/DISAC**—Enable/Disable Access

These two instructions permit the user to turn on or off the password protection to the device. To disable any access to the device, send the following instruction:

1000 | 1000
Instruction Code

The device will give no indication that it has been disabled other than you now cannot Read or Write to the array.

To enable the device operation, send the following instruction:

1100 | 0101	[Access Code]

For example, to enable access to a device that has an 8 byte password stored in the access code register, send the following:

1100 | 0101	01 02 03 04 AA BB CC DD
Instruction Code	*8-Byte Pswrd*

Again, the device gives no indication that you have entered the correct password, however you now have full Read/Write capabilities.

3. **WMPR**—Write Memory Pointer Register

The Write Memory Pointer Register instruction allows you to modify the contents of the memory pointer register. The value of the register determines what portion of the memory array is protected from byte-writes during unprotected operation and what portion you are allowed to read during protected operation.

For example, if there is no password protection and the memory pointer is set to 00AA, then no byte-writes from address 0000 to address 00AA are allowed (unless the OVMPR instruction has been entered previously). In the protected mode, with the memory pointer set to the same value (00AA), a Read Sequential (RSEQ) instruction from address 0000 will not allow the user to read any of the array. The RSEQ instruction must begin at 00AA and will then allow read access from 00AA to the end of the array. Note: The memory pointer contents will not block Erase All or Write All operations.

To change the contents of the register, send the following:

1100 | 0100	[A15–A8] [A7–A0] *x8*
	[A7–A0] *x16*

This instruction is operational only after an ENAC instruction (if a password has been set) and an EWEN (see EWEN section) instruction have been sent to the device. Once this is done, you can modify the register contents to the desired value. For example, to change the contents from 0000 to 0123, send the following:

1100 | 0100	0123
Instruction Code	*New Memory Pointer Value*

The memory pointer register now has a value of 0123 (x8).

4. **RMPR**—Read Memory Pointer Register

The Write Memory Pointer Register instruction allows you to read the location in memory where the memory pointer resides. This tells you which portions of the memory are divided between read only and full read/write access. To read the value of the register, send the following:

1100	1010
Instruction Code	

The device will then return the hex value of the memory pointer location.

5. OVMPR—Override Memory Pointer Register

This instruction allows the user to write data to a protected area of memory on a one time basis, without having to uncover that area with the memory pointer. For example, to write data to an area protected by the memory pointer the OVMPR instruction would be issued, followed immediately by a write instruction. After the write has been completed, the area of memory is again protected.

1000	0011
Instruction Code	

READ/WRITE/ERASE INSTRUCTIONS

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1. **READ**—Read Memory

This instruction outputs the data from memory at the specified location.

1100	0101	[A15–A8] [A7–A0] *x8* [A7–A0] *x16*
Instruction Code		*Address*

For example, to Read the contents of address 1AH, send the following:

1100	1001	00011010

The device then outputs data located at this address on the DO pin.

2. **WRITE**—Write Memory

The Write instruction writes an 8 or 16 bit data word into a specified address of memory. Once the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location is erased before data is written. For example, to write the data 5A2D Hex to address C8, send the following:

1100	0001	11001000	0101101000101101
Instruction Code		*Address (x16)*	*Data (x16)*

After the specified Program/Erase pulse width, the data 5A2D is written to address C8 Hex.

3. **ERASE**—Clear Memory

The Erase instruction clears the specified memory location by setting all cells to a logic "1". Once the instruction and address have been entered, the self-timed erase cycle will start. For example, to erase the data located at address 1234 Hex, send the following:

1100	0000	0001001000110100
Instruction Code		*Address (x8)*

After the specified Erase pulse width, the contents of address 1234 Hex will be FF Hex.

4. **ERAL**—Erase All

The Erase All instruction clears the data from all locations in the memory. To erase the entire device, send the following:

1000	1001	1000	1001
Instruction Code		*Instruction Code*	

The code is required to be sent twice (to protect against inadvertent chip clear) and, once sent, clears all locations to the FF Hex state.

5. **WRAL**—Write All

The Write All instruction is used to write the same data byte to all locations in the memory. For example, to write the data AA Hex to all locations, send the following:

1000	1001	1100	0011	10101010
Instruction Code		*Instruction Code*		*Data (x8)*

After the specified Program/Erase pulse width, all locations in the device will now have AA Hex written to them.

6. **RSEQ**—Read Sequential

The Read Sequential instruction allows the user to sequentially clock out data starting at a specified address continuing until the end of memory or Chip Select

is brought low. For example, to read memory starting at address 4D Hex continuing to the end of the array, send the following:

1100	1011	01001101
Instruction Code		*Address (x16)*

The device will now clock out (SK pin must be clocked by user) the contents of memory starting at address 4D and continuing to the end of memory.

STATUS AND CONTROL INSTRUCTIONS

1. **EWEN**—Erase/Write Enable

This instruction is required to be entered before any program/erase instruction will be carried out. Once it is entered, it remains valid until a power down or a EWDS instruction is sent. To enable the device for writing/erasing, send the following:

1000	0001
Instruction Code	

The device is now ready to be erased or written to.

2. **EWDS**—Erase/Write Disable

This instruction disables all writing or erasing of the device. Once sent, the device must be sent an EWEN instruction before any erase/write instruction will be performed. To disable erase/write instructions, send the following:

1000	0010
Instruction Code	

The device is now protected from any erase or write instructions.

3. **ORG**—Select Memory Organization

This instruction allows the user to select a x16 or x8 memory organization. For example, to configure the device with a word length of 8 bits, send the following:

1000	0110
Instruction Code	

To configure the device with a word length of 16 bits, send the following:

1000	0111
Instruction Code	

4. **RSR**—Read Status Register

The Read Status Register instruction allows the user to determine the state of the device. To determine if the device is in an error condition, send the following:

1100	1000
Instruction Code	

The device then responds with an 8 bit status word that gives the following information:

10100000 - the device is operating normally
10110000 - the device has a parity error
10101000 - the device has an instruction error
10100100 - the device is in the program/erase cycle

5. **DISBSY**—Disable Busy

The Disable Busy instruction disables the RDY/$\overline{\text{BUSY}}$ status on the DO (data out) pin. To disable the RDY/$\overline{\text{BUSY}}$ function, send the following:

1000	0101
Instruction Code	

The RDY/$\overline{\text{BUSY}}$ status is now no longer available on the DO pin.

6. **ENBSY**—Enable Busy

The Enable Busy instruction enables the RDY/$\overline{\text{BUSY}}$ status on the DO pin. To enable this status, send the following:

1000	0100
Instruction Code	

The RDY/$\overline{\text{BUSY}}$ status is now enabled on the DO pin. This allows the user to tell if the device is in the program/erase cycle (DO low) or has completed it (DO high).

7. **NOP**—No Operation

The NOP instruction leaves the device in an idle mode; no operation is executed.

Catalyst Parallel E²PROMs Feature Software Data Protection

Applications Staff

A common concern among E²PROM users is data integrity during power on/off transitions and system glitches that may cause inadvertent writes to the memory array. Hardware data protection schemes have been around for some time to reduce this problem. They include:

1. V_{CC} lockout voltage below which writes are inhibited.
2. Power on delay mechanism where writing is inhibited a fixed time after V_{CC} is stable.
3. Write inhibits by holding $\overline{CE}$, $\overline{OE}$ or $\overline{WE}$ high.
4. Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs are ignored.

Despite these hardware protection features, additional protection is being required by industry users. Catalyst has added Software Data Protection (SDP) to its 64K-bit and 256K-bit E²PROMs. The CAT28C64B/65B/256 and CAT28LV64/65/256 parallel E²PROMs feature software controlled data protection that once enabled, requires a set write sequence to be sent to the device prior to any writes being performed. Figures 1 and 2 provide the software sequence required to activate Software Data Protection for both devices:

Figure 1. CAT28C64B/65B and CAT28LV64/65 Write Sequence for Activating Software Data Protection

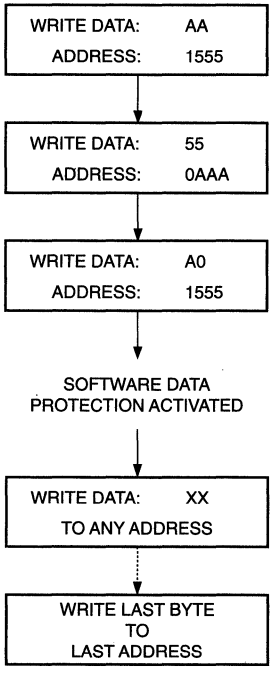

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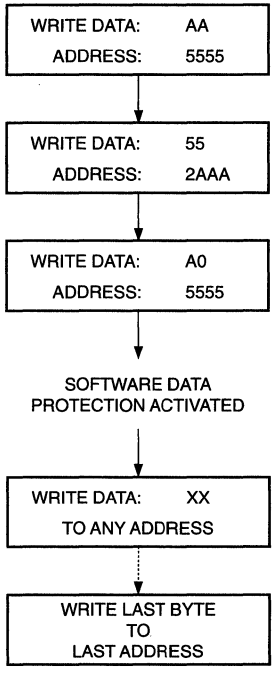
Figure 2. CAT28C256 and CAT28LV256 Write Sequence for Activating Software Data Protection



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Once Software Data Protection has been activated, it remains activated through any power on/off transitions and, prior to any writing, the user must send the device this same algorithm. The addresses used are located on different page boundaries so that the data bytes used in the SDP algorithm are not actually written to the device.

In the event the user wishes to deactivate the SDP feature a six step algorithm is provided. Figures 3 and 4 provide this algorithm for both devices.

Once issued the device returns to a normal operating condition and data already written to the device remains unchanged.

Figure 3. CAT28C64B/65B and CAT28LV64/65 Write Sequence for Deactivating Software Data Protection

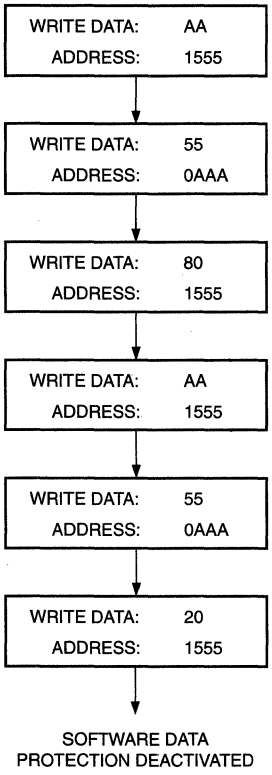

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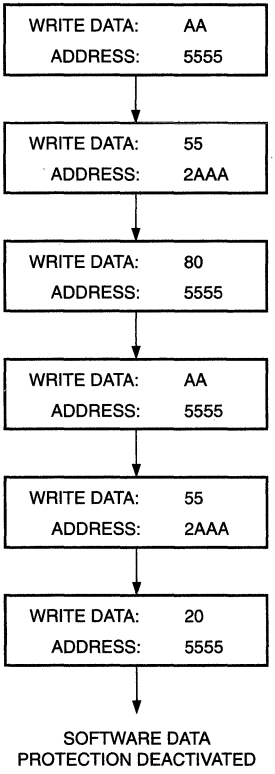
Figure 4. CAT28C256 and CAT28LV256 Write Sequence for Deactivating Software Data Protection



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Programmer Vendors

Application Staff

Below is a list of programmers that support Catalyst's products. Please contact the programmer manufacturers for additional information.

Ascend
1328 Concannon Boulevard
Livermore CA 94550-6004
Ph (510) 606-2000
Fax (510)606-2006

Advin
1050-L East Duane Avenue,
Sunnyvale, CA 94086
Ph (408)243-7000
Fax (408)736-2503

BP Microsystems
100 North Post Oak Road
Houston, Texas 77055-7237
Ph (713)688-4600
Fax (713)688-0920

Data I/O Corp
10525 Willows Road N.E.
P.O.Box 97046
Redmond, Washington 98073-9746
Ph (206)881-6444
Fax(206)882-1043

Hi-Lo Systems Research Co., Ltd
4F, No.2, Sec 5
Ming-Shen E. Rd.
Taipe, Taiwan, ROC
Ph (886) 2 764 0215
Fax (886) 2 756 6403

ICE Technology Ltd.
Unit 4, Penistone Court
Stations Buildings
Penistone
S.Yorks. S30 6HG. UK
Ph (44) 1226 767404
Fax (44) 1226 370434

International Microsystems Inc
521 Valley Way
Milpitas CA 95035
Ph (408)942-1001
Fax (408) 942-1051

Link Instruments
369 Passaic Ave.,
Suite 100,
Fairfield, NJ 07004
Ph (201) 808-8990
Fax (201) 808-8786

Logical Devices Inc(Stag)
130 Capital Drive
Golden, CO 80401
Ph (303) 279-6868
Fax (303)279-6869

Needham's Electronics Inc
4630 Beloit Dr.,
Suite 20,
Sacramento, CA 95838
Ph (916)924-8037
Fax (916)924-8065

Sunrise Electronics Inc.
675 Brea Canyon Road,
Unit 6
Walnut, CA 91789
Ph (909)595-7774
Fax (909)594-7009

System General Corp.
1603A South Main St.,
Milpitas, CA 95035
Ph (800)967-4776
Fax (408)262-9220

Tribal Microsystems Inc.
44388 S. Grimmer Blvd.,
Fremont CA 94538
Ph (510)623-8859
Fax (510)623-9925

Xeltek
3563 Ryder St.
Santa Clara, CA 95051
Ph (408)524-1929
Fax (408)245-7084

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Catalyst Quality and Reliability

The Catalyst Quality and Reliability Policy Manual (available on request) contains the methods and philosophies to implement the corporate mission. Catalyst is utilizing a quality system in accordance with the requirements of ISO-9001 "Quality Systems — Model for Quality Assurance in Design/Development, Production, Installation, and Servicing" and the criteria of MIL-M-38510, appendix A "Product Assurance Program".

MANUFACTURING TECHNOLOGY

Catalyst fabricates all memory devices using a CMOS process. The fundamental storage element in all Catalyst reprogrammable nonvolatile memories is a floating gate memory transistor. Details of various memory cells operation are included in the Catalyst Quality and Reliability Application Notes in this section.

All wafer fabrication and package assembly processes have flow charts and baselines as controlled documents. Basic descriptions of all Catalyst device construction are available on request. Detailed descriptions are proprietary; however, a nondisclosure agreement may be used, if required.

QUALIFICATION METHODOLOGIES

Catalyst qualifies reprogrammable nonvolatile memories in accordance with the guidelines of the IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays (IEEE Std 1005–1991, available from IEEE), MIL-STD-883, and JEDEC Standard 22 (JESD-22).

Devices are qualified by either a specific product and package or by generic Design/Process and Package families. Generic qualifications reduce time and overall cost of qualification, while providing assurance that each combination of design, process, and package meets minimum reliability requirements. Worst case combinations would be used.

A Design/Process family consists of those devices using similar logic, layout, and design rules using the same wafer fabrication process and location.

A Package family consists of those devices using the same assembly package configuration, materials, and location.

Once a representative device is qualified, other members of the Design/Process families are qualified in that package family. Thus, each possible combination of design, process, and package does not require stressing, in order to have each combination fully qualified or requalified after changes. Reference Catalyst specifications (available on request) for Qualification Requirements and Critical Process Change Notification.

For example: If a serial E^2PROM, built on a 1.5 µ process is qualified in a SOIC package; then, other serial E^2PROMs (using the similar logic, layout, and design rules) built on the same 1.5µ process, are also qualified in the same SOIC package.

Catalyst provides Reliability Summaries (upon request) for all devices. Reliability Summaries contain three sections: Design/Process Family, Package Family, and Device Specific.

The Design/Process Family data summary includes the following sections: Reliability Stress, Stress Conditions, Device Hours, # Failures, Failure Rate at 60% C.I. (i.e., at the stress temperature in %/1000 hours) and a Cause category for any failures. The Summary includes: the Device Hours (at the deaccelerated temperature of 55°C), the Apparent Activation Energy and the failure rate at 60% C.I. in FITs (or FICs for endurance). The "Endurance Cycles to Time Conversion Nomograph" is included for the demonstrated endurance failure rate. This format is used for reporting Life Test, Data Retention and Endurance.

The Package Family data summary includes the following sections: Reliability Stress, Stress Conditions, # Lots, Failures/Timepoint. This format is used for reporting: Solder Heat Resistance, including subsequent Life Test and Data Retention, HAST, Pressure Pot, Biased 85/85, Temperature Cycles, Thermal Shock, Marking Permanency, Lead Fatigue and Physical Dimensions.

The Device Specific data summary includes the following sections: Reliability Stress, Stress Conditions, # Lots, Failures/Timepoint. The data reported includes: Machine Model and Human Body Model ESD results and latch-up data.

ENDURANCE AND DATA RETENTION GUARANTEE

Endurance

Endurance is the measure of the ability of a reprogrammable nonvolatile memory device to meet its data sheet specifications as a function of accumulated program/erase cycles. A device program/erase cycle is the act of changing data from original (e.g., erased) to opposite (e.g., programmed) back to original for all bits of the memory array.

Catalyst provides an endurance lot acceptance guarantee of a 1% AOQL (LTPD 5/1) for the number of program/erase cycles per byte as specified by the applicable data sheet. The endurance is independent of the program or erase method, e.g., byte, page, sector, block, chip. Endurance is verified by the customer with the Endurance, Data Retention and Steady State Life Test Methodology.

Data Retention

Data Retention is the measure of the integrity of the stored data as a function of time. Data retention is the time from data storage to the time at which a repeatable data error is detected.

Catalyst provides a data retention lot acceptance guarantee of a 1% AOQL (LTPD 5/1) for the number of years per device as specified by the applicable data sheet. This applies across the operating temperature range and after the specified minimum number of endurance cycles. Data retention is verified by the customer with the Endurance, Data Retention and Steady State Life Test Methodology.

ENDURANCE, DATA RETENTION, AND STEADY STATE LIFE TEST METHODOLOGY

An endurance test, reference Method 1033 of MIL-STD-883, shall be added before performing the steady state life test and extended data retention test. Cycling may be chip, sector, block, byte or page on finished devices. The following conditions shall be met:

(1) All bytes shall be cycled for a minimum of the specified number of cycles at equipment room ambient.

(2) Perform parametric, functional and timing tests at room temperature, after cycling. Devices having bits not in the proper state after functional testing shall constitute a device failure. Separate the devices into two groups for extended data retention and steady state life test, then write applicable data patterns.

(3) Perform the extended data retention, consisting of a high temperature unbiased storage for 1000 hours minimum at 150°C minimum. The storage time may be accelerated by using a higher temperature according to the Arrhenius relationship and an apparent activation energy of .6eV. The maximum storage temperature in an Nitrogen environment shall not exceed 175°C for hermetic or 160°C for plastic devices. All devices shall be programmed with a charge on all memory cells in each device, such that a loss of charge can be detected (e.g., worst case pattern).

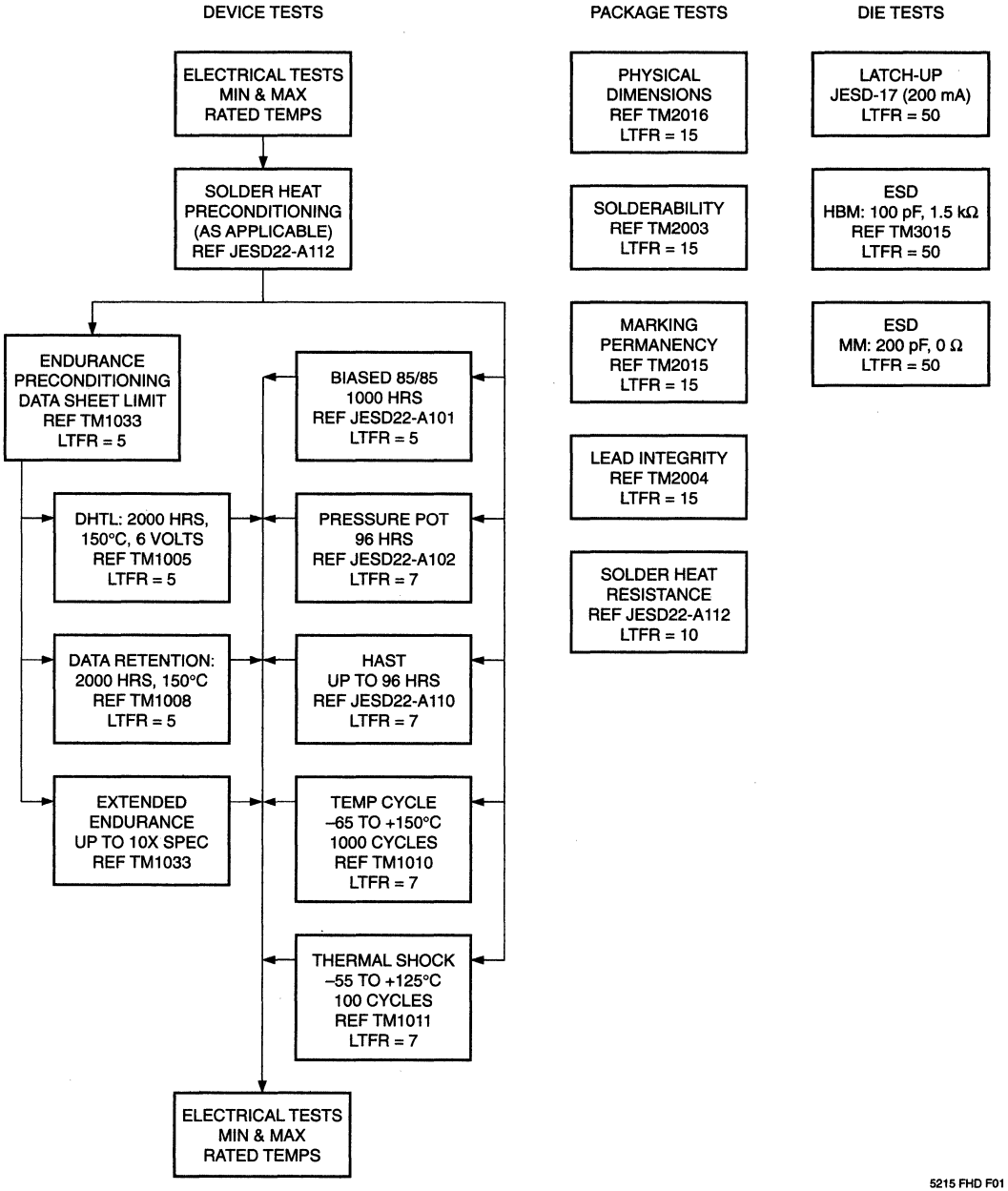
(4) Read the data retention pattern and perform parametric and functional tests at room temperature, after cycling and bake. Devices having bits not in the proper state after functional testing shall constitute a device failure.

(5) Perform steady state life, reference method 1005 condition D of MIL-STD-883, for 1000 hours at 125°C in an Nitrogen environment. The steady state life time may be accelerated by using an Arrhenius relationship and apparent activation energy of .4 eV. The maximum operating junction temperature shall not exceed 175°C. All devices shall be written with a checkerboard or equivalent topological alternating bit pattern.

(6) Read the steady state life pattern and perform parametric and functional tests at room temperature, after cycling and steady state life. Devices having bits not in the proper state after functional testing shall constitute a device failure.

(7) The endurance, data retention, and steady state life tests shall individually pass a sample plan to an LTPD of 5/1 (sample size = 77, accept = 1), equivalent to an AOQL = 1%.

Figure 1. Qualification Requirements (Commercial Plastic Package)



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Note:
(1) LTFR = Lot Tolerant Failure Rate or LTPD, sample sizes per MIL-M-38510, appendix B.
(2) TMxxxx refers to Test Methods per MIL-STD-883.
(3) JESD22 refers to the test methods per JEDEC Standard 22.

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Table 1. General Requirements

Stress Codes	Names of Stress Methods	Standard Conditions
DHTL	Dynamic High Temperature Operating Life	1000 hours @ 150°C
DRSL	Data Retention Storage Life	1000 hours @ 150°C
ENDR	Endurance	10X Data Sheet @ 25°C
THBS	Temperature Humidity Bias Stress	1000 hours 85°C/85%RH
PPOT	Pressure Pot	500 hours @ 121°C
HAST	Highly Accelerated Stress Test	168 hours @ 140°C
TMCL	Temperature Cycling (air-to-air)	1000 cycles –65°C/150°C
TMSK	Thermal Shock (liquid-to-liquid)	100 cycles –55°C/125°C

RELIABILITY STRESS METHODS

DHTL—Dynamic High Temperature Operating Life

Description: This stress accurately replicates the users operating conditions for a device. All inputs are toggled in the read mode and outputs are loaded with an appropriate worst case load. This stress maximizes the number of nodes subjected to changing electric fields in order to optimize detection of latent failures caused by such problems as oxide faults, pinholes, or leaky junctions.

Minimum Duration: 1000 hours at an ambient temperature of 150°C. Catalyst CMOS devices have a small junction temperature rise in this stress, thus there is no concern for elevated temperatures creating packaging or silicon problems.

DRSL—Data Retention Storage Life

Description: This stress exposes the parts to unbiased storage at an elevated temperature, normally 150°C for plastic packages and 250°C for hermetic packages. These are the highest practical temperatures the applicable package can sustain to accelerate the loss of charge off the floating gate.

Temperature: For plastic packages, 165°C is at the maximum safe storage temperature, because the glass transition temperature of most epoxies is below 165°C. Above 165°C, the mechanical and chemical stability of the plastic is uncertain, thus prolonged exposure can create failure mechanisms that would otherwise not be observed. For solder seal hermetic packages, 260°C is the maximum temperature before damaging the solder seal. For glass frit seal hermetic packages, 300°C is the maximum prolonged storage temperature before introducing unpredictable effects in the silicon.

Minimum duration: 1000 hours at 150°C.

ENDR—Endurance

Description: This stress replicates the user's writing conditions for the device. All bits are erased and programmed. The stress detects failures due to oxide rupture or charge trapping of the tunnel dielectric or failures in peripheral oxides.

Minimum Duration: The data sheet specified number of cycles must be performed before DHTL or DRSL. Extended endurance will be to at least 10 times the specified number of cycles.

THBS—Temperature Humidity Bias Stressing

Description: This accelerated temperature and humidity bias stress is performed at 85°C and 85% Relative Humidity, reference JESD-22, Test Method A102. In general, the worst-case bias condition is the one that minimizes the device power dissipation and maximizes the applied voltage. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

Minimum Duration: 1000 hours. As HAST becomes more widely accepted, it may supplement or replace THBS stressing.

PPOT—Pressure Pot

Description: This stress exposes the devices to saturated steam at an elevated temperature and pressure. The standard condition is 15 PSIG, at a temperature of 121°C, reference JESD-22, Test Method A102. The plastic encapsulant is not a permanent moisture barrier and will eventually saturate with moisture. Since the chip is not biased, the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached.

Effectivity: The steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, thus is effective at detecting corrosion problems, contamination-induced leakage problems, general glassivation stability and integrity, package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die; also, the moisture causes leakage paths in the crack itself.)

Minimum Duration: 96 hours for surface mount packages and 168 hours for DIL packages.

HAST—Highly Accelerated Stress Test

Description: This highly accelerated biased humidity temperature test combines the worst-case characteristics of 85/85 stressing and the high temperature, high pressure characteristics of PPOT testing. The ambient is saturated steam. The stress condition is 130°C and 85% RH, reference JESD-22, Test Method A110. HAST is often used in process control as a rapid test for moisture reliability assessment. Optimum bias conditions are the same as used for 85/85.

Temperature: Bond integrity may be compromised for extended HAST stressing at junction temperatures in excess of 150°C.

Minimum Duration: 96 hours for surface mount packages and 168 hours for DIL packages.

TMCL-Temperature Cycling, Air-to-air

Description: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are –65°C and +150°C with a minimum 10 minute dwell and 5 minute transition, per MIL-STD-883, Method 1010, Condition C. This is a good test to measure the overall package to die mechanical compatibility.

Minimum Duration: 1000 cycles.

TMSK-Thermal Shock, Liquid-to-liquid

Description: Heating and cooling are done by immersing the units in a hot and cold inert liquid. Normal temperature extremes are –55°C to +125 with a minimum 5 minute dwell and less than a 10 second transition per MIL-STD-883, Method 1011, Condition C.

Temperature: Heat transfer by conduction is much faster than by convection, thus causing rapid temperature changes in the part. This rapid changing in temperature creates temperature gradients across the part, which will produce additional mechanical stress compared with temperature cycling. This additional stress will accelerate mechanisms such as bond cratering and wire creep.

Minimum Stress Duration: 100 cycles.

Solderability Testing

Description: This method, per MIL-STD-883, Method 2003, is designed to determine the solderability of the device leads using a standardized soldering procedure after a specified pre-conditioning (steam aging). Rejection criteria are based on physical appearance of the finished leads (porosity, pinholes, non-wetting, dewetting, foreign material, etc.)

Lead Integrity

Description: This method tests the leads of a device by bending them in a prescribed manner and rejecting the device if the specified stress results in a broken or loosened lead, or damage to the device hermeticity, per MIL-STD-883, Method 2004.

Latch-up

Description: CMOS devices contain parasitic PNPN structures which may act as SCR's, given the appropriate triggering event. The triggering event may be Gamma radiation or a voltage spike on the power bus or an input pin. Under normal operating conditions, these PNPN structures are reverse biased and quiescent. The latch-up may result in a temporary malfunction or permanent damage. Reference JESD-17 Latch-up in CMOS Integrated Circuits and Catalyst Specification #22009.

ESD Testing

ESD Specs: Catalyst ESD test standards are presented in Specification #22010. This specification includes the human body model based on MIL-STD-883, Method 3015, Electrostatic Discharge Sensitivity Classification; and the machine model.

The human body model uses a 100 pf capacitor with a 1.5 KΩ series resistor. The machine model uses a 200 pf capacitor with no resistor.

Surface Mount Package Solder Heat Preconditioning

Industry Standards: Reference JESD-22, Test Method A112 proposal.

The samples from each pin count of each applicable package family shall be subjected to the following stressing sequences:

Note: Packages containing larger die-attach pads are expected to exhibit less durability when subjected to these same sequences of environmental exposures. Therefore, within a package/pin-count family, only the largest die-pad dimensions need be tested to establish the durability of that package family.

Example: 28 pin SOIC having three different die-attach pad dimensions. Only the largest die size need to be tested to ensure the integrity of the 28 pin SOIC family.

Saturated samples: Samples which have been saturated to a given level of humidity shall be subjected to the sequence listed below. Successful completion of these sequences represents the minimum durability requirement for packages, which can be shipped without special dry-packing precautions.

Sample 1

125°C bake for 24 hours to dry the package
168 hour 85/85 no bias to saturate the package
2 60 second passes through vapor phase furnace at 217°C
Samples to DHTL, DRSL, and 85/85

Sample 2

125°C bake for 24 hours to dry the package
168 hour 85/85 no bias to saturate the package
2 60 second passes through infrared furnace at 240°C
Samples to DHTL, DRSL, and 85/85
Electrical test

Acceptable Performance: There should be NO failures from package degradation, cracks or internal corrosion.

Crack and Damage Inspection: Acoustical microscopy and cross sections may be used to analyze samples for evidence of damage.

After electrical test and visual inspection, the samples shall be exposed to DHTL, DRSL, and THBS for a minimum of 1000 hours.

Acceptable performance: Devices in each stress shall meet the applicable sample plan.

Sequence for HUMIDITY-PRECONDITIONED SAMPLES (moisture content = 0.4% to 0.6%)

50 samples
Precondition this sample as follows:
Weigh a sample of 10 devices (record weight)
Bake in dry storage @ 150°C for 48 hours
Weigh the sample of 10 devices again (record weight)
Subject the sample to 85/85 (no bias) for 168 hours
Weigh a sample of 10 devices (record weight)

Acceptable Performance: There should be NO failures from package degradation, cracks or internal corrosion.

Crack and Damage Inspection: Additional sequences and inspection techniques: Multiple exposures to vapor phase and infrared reflow profiles may be conducted. Acoustical microscopy and cross sections may be used to analyze samples for evidence of damage.

RELIABILITY STRESS RESULTS

Available upon request.

Warranty Procedure

PURPOSE

To define procedures to implement Catalyst lot acceptance guarantee criteria (applicable at customer's incoming inspection) and product warranty. To define the product warranties, lot acceptance guarantees, warranty periods and Catalyst's limitation of obligation under those guarantees and warranties for all Catalyst integrated circuits and die.

SCOPE

This procedure applies to all Catalyst manufactured devices and die.

REFERENCE DOCUMENTS AND STANDARDS

Catalyst Standard Terms & Conditions of Sale.

Catalyst Returned Material Authorization Procedure.

Applicable Catalyst Data Sheets.

Applicable Customer Specifications, Contracts or Purchase Orders as accepted by a duly authorized Catalyst representative.

DEFINITIONS AND TERMS

AOQ (Average Outgoing Quality)—The mean proportion non-conforming, often expressed in PPM, shipped by the manufacturer. JEDEC Standard No. 16 describes how to assess AOQ in PPM for microcircuits.

AOQL (Average Outgoing Quality Limit)—The maximum average proportion non-conforming shipped using a given sampling system.

LTPD (Lot Tolerant Percent Defective)—Where the consumer's risk, i.e., probability of having a bad lot accepted equals 10%. Often used as a single sampling procedure for isolated lots or reliability stress evaluation.

EQUIPMENT AND MATERIALS

Not applicable.

CALIBRATION

Not applicable.

RECORDS AND FORMS

Catalyst Return Material Authorization (RMA) Form. Catalyst Customer Failure Analysis Request (CFAR) Form.

WARRANTY PROVISIONS/SEMICONDUCTOR DEVICES

Warranty

Catalyst warrants that standard integrated circuits delivered pursuant to this procedure shall, at the time of shipment, and for a period of one year thereafter, be free from defects in material(s) and shall conform to Catalyst specifications or such specifications agreed upon by Catalyst in writing. Under this warranty, Catalyst obligations, with respect to losses, and at Catalyst's option, shall be limited to; either replacement (by delivery F.O.B., Santa Clara, CA.) or refund of the purchase price of the non-conforming product. This warranty is subject to the following conditions and procedures:

Customer Complaint. In the event a customer believes that product purchased from Catalyst is not in conformance with the Catalyst warranty for that product, the customer should notify Catalyst and, upon request from Catalyst, return a sample of the allegedly non-conforming devices. Following receipt of the sample of allegedly non-conforming devices, Catalyst will issue a CFAR number. Thereafter, failure analysis will be performed to determine whether the device is nonconforming to the applicable Catalyst specification and, if so, whether the non-conformance is covered by Catalyst warranty or whether the warranty is not applicable for some reason (e.g., the non-conformance resulted from misuse, neglect, improper installation, repair, alteration, accident or improper product handling, the warranty period has expired, the product was not purchased from Catalyst, etc.).

Warranty Determination. Final determination of warranty coverage of all returns shall be by Catalyst Semiconductor, Santa Clara, CA. Issuance of a CFAR number does not imply acceptance of any warranty obligation with respect to the returned material by Catalyst. An RMA number will be issued when Catalyst agrees that

Note:
(1) This Warranty Procedure is Catalyst Specification #31000.

material, other than the CFAR sample, should be returned. Issuance of an RMA number also does not imply acceptance of any warranty obligation, but an RMA number may be issued by Catalyst for any reason deemed by Catalyst to be appropriate.

Responsibility. Catalyst's Sales/Marketing department shall notify the customer if a warranty claim is not accepted. Should the customer return product without an authorized RMA number, the product will be returned to the customer, freight collect, or if such request is not forthcoming when requested by Catalyst, then Catalyst shall be entitled to scrap the product at Catalyst without liability to the customer.

The customer will be responsible for payment of product purchase price, and returned freight and handling costs.

If the warranty claim is accepted, after verifying non-conformance, Catalyst will replace product or refund cost, within 90 days. Warranty replacement or refund will be based on final product count at Catalyst.

Disclaimer

This express warranty shall extend only to the customer and not the customer's end user; and is in lieu of all other warranties, express or implied, including the implied warranties being specifically disclaimed by Catalyst. In no event shall Catalyst's liability for any breach or alleged breach of an order by either party exceed the total extended price or prices shown on the goods in question; Catalyst shall not be liable for any special, incidental or consequential damages resulting from such breach or alleged breach. Furthermore, Catalyst shall, in no event, be obligated for any cost incidental to the replacement of non-conforming products.

Commercial Incoming Inspection

Incoming inspection, if any, must be completed by the customer within the warranty period. Product not rejected as a result of incoming inspection and notice thereof given to Catalyst on or before the expiration of the warranty period shall be conclusively deemed accepted. If the customers's incoming inspection is based on lot acceptance sampling, then the following establish the agreed upon sample plan levels. Any lot failing to meet the sample plan is eligible for return to Catalyst, provided an RMA is obtained.

Data Sheets/Control Specifications

Catalyst data sheets are controlled specifications applicable to product at the time of shipment. Catalyst reserves the right to revise published data sheets and/or make changes in the product. Catalyst assumes no responsibility for the use of any circuits described in published data sheets, and conveys no license under any patent. Applications for any integrated circuits contained in publications are for illustration purposes only, and Catalyst makes no representation or warranty that such applications will be suitable for the use specified.

Third Party Warranty Restrictions

Unless previously reviewed and accepted in writing by a duly authorized Catalyst representative, environmental screening or testing, or failure analysis of products by the customer or a third party laboratory voids the warranty of those devices.

Unsalable or Untestable Product

Returned product received in an unsalable or untestable condition, or such condition that verification of the reported discrepancy is impractical or impossible, voids the warranty.

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Table 1. Lot Acceptance Guarantee Criteria for Commercial Standard Integrated Circuits

Condition	Reference	Sample Plan
Timing, parametric and functional functional electrical, cumulative across temperature	Data Sheet	1% AOQL
Mechanical/Visual	Ext. Vis. Spec	1% AOQL
Endurance/Data Retention	Coml End/DR Spec	1% AOQL
One-time Programmability	Data Sheet	2.5% AOQL

Critical Components/Life Support Systems

Catalyst products are not authorized for use as critical components in Life Support Devices or Systems. If any such use is intended then provision must be made in a separate agreement, signed by the President and Vice President of Quality & Reliability of Catalyst, which will provide for special terms and provisions relating to testing required because of the nature of such use.

A critical component is defined as any component whose failure to perform an intended function, could possibly lead to loss of life or bodily harm.

Life Support Systems that may include critical components, are defined as, but not necessarily limited to:

(1) Surgical implants in a human body,

(2) Equipment used to sustain human life, or

(3) Equipment used to monitor and/or measure human body conditions.

Incoming Inspection

Incoming inspection, if any, must be completed by the customer within the warranty period. Product not rejected as a result of incoming inspection and notice thereof given to Catalyst on or before the expiration of the warranty period shall be conclusively deemed accepted. If the customers's incoming inspection is based on lot acceptance sampling, then the following establish the agreed upon sample plan levels. Any lot failing to meet the sample plan is eligible for return to Catalyst, provided an RMA is obtained.

Manufactured Devices

Military devices are manufactured in accordance with the applicable detail specification, (i.e., Catalyst compliant device specification for MIL-STD-883 compliant devices, or the Standardized Military Drawing) as acknowledged and accepted by Catalyst in the customer's purchase order.

DIE WARRANTY POLICY

Warranty Limitations

The warranty on die is limited to 90 days from the date of shipment.

Die lots will, at incoming inspection, meet the visual requirements of Catalyst Second Optical Inspection Criteria of MIL-STD-883, Method 2010 Condition B, to a 1% AOQL sample plan.

Die lots not rejected as a result of incoming inspection and notice thereof given to Catalyst on or before the expiration of the warranty period shall be conclusively deemed accepted. Any lot failing to meet the sample plan is eligible for return to Catalyst, provided an RMA is obtained.

The warranty on die is not applicable to die that receive any additional electrical, mechanical or environmental testing, processing or other handling by the customer or a third party.

Catalyst does not grant reliability approval on die because of additional assembly and test processing required when die are integrated into the customer's product where testing and assembly is performed by, or contracted out by the customer, unless it is expressly defined in a customer specification, and accepted in writing by a duly authorized Catalyst representative.

NON-STANDARD PRODUCT

Development

Any product designated for "developmental" or "experimental use" is sold "as is" with no warranty whatsoever except the warranty of title; the implied warranties of fitness for a particular purpose and merchantability are expressly disclaimed. The customer shall indemnify Catalyst from any claim that the product infringes upon in any United States patent, copyright or mask work right.

Development product shall be marked with the standard Catalyst marking plus block letters ES instead of the date code.

Pre-Production

Pre-production product is lot guaranteed per paragraph Commercial Incoming Inspection to electrical parameters of the preliminary data sheet or errata sheet specifications only. Reliability testing is in progress, but no reliability approvals are offered to the customer.

Pre-production product shall be marked with the standard Catalyst marking and an MS instead of the date code.

Custom Products

Custom products are manufactured to meet non-standard requirements as specified in a customer's specification,which is accepted in writing by Catalyst.

Any lot failing the specified sample plan and/or failing a customer's screen to a specified test criteria, an agreed to in writing by a duly authorized Catalyst representative is eligible for return to Catalyst in accordance with return provisions.

WARRANTY POLICY FOR DISTRIBUTORS

Products shipped by distributors are subject to a one year warranty by Catalyst from the date of first shipment from the distributor. This warranty by Catalyst expires if the distributor does not ship product within two years from data of shipment from Catalyst.

Distributor returns will be honored only if an RMA form or RMA number is issued by a duly authorized Catalyst representative within the applicable warranty period.

Where distributors remark product, the Catalyst symbol and date code shall not be altered. A record of any remarking operation must accompany material returned to enable traceability to the original shipment.

All distributor returns for stock rotation, obsolete product or other policy reasons must be received with an RMA form or RMA number issued by the responsible Catalyst sales representative.

Distributors must return devices, in accordance with the Return Provisions within 30 days of the issuance of an RMA form or RMA number, otherwise returned devices will not be honored for credit or replacement.

RETURN PROVISIONS

Condition of Received Returned Materials

Returned material must be packed in a manner to prevent damage to the device(s) (electrical or mechanical) under normal commercial carrier handling conditions. Products received in a damaged condition due to improper packing for shipment by the customer are the customer's responsibility.

All products, manufactured by Catalyst, must be returned in containers that prevent static damage. Failure to provide static handling protection, or material found damaged as the result of user negligence, are the responsibility of the customer.

Rework Costs

In the event the customer unilaterally elects to rework material which fails customer incoming inspection, the cost and liability of such rework shall be the sole responsibility of the customer. Rework of material by the customer shall nullify the Catalyst warranty.

When a customer requests authorization and reimbursement for rework costs, prior written approval shall be obtained from Catalyst Marketing and the Q & R Vice President before the customer rework commences.

RETURNS METHODOLOGY:

Refer to Catalyst's Returned Material Authorization (RMA) Procedure for instructions on completion of the Returned Material Authorization Form and instructions on material return.

DISQUALIFICATION OF CATALYST PRODUCT BY PURCHASER

In the event that the customer determines incoming Catalyst product to be unacceptable and establishes that the product is disqualified, the responsible salesperson must communicate specifically if the return is for nonconformance to agreed specifications or being returned for other reasons.

Other reasons for disqualification may include:

(A) Unapproved vendor.

(B) Disqualification for repeated delinquencies by Catalyst.

(C) Non-performance in the customer's system, although the product meets Catalyst's electrical specifications.

If the customer purchases products for production prior to completion of his own qualification tests, such products cannot be classified as "disqualified".

Reliability Considerations for E²PROMs

When acquiring a microcircuit, many considerations above and beyond the purchase price are important. Among these are quality, reliability, delivery, service and product assurance. The lowest cost of ownership for the user is a result of the proper balance and specification of the above considerations. E²PROMs contain reliability considerations that can significantly affect the cost of ownership if the E²PROM is incorrectly used in the application.

For E²PROMs, whether serial, parallel, flash or other, reliability is the summation of the factors of operating life (read), data retention and endurance.

E²PROM Device Failure Rate

$F.R._{DEVICE} = F.R._{READ} + F.R._{ENDURANCE} + F.R._{RETENTION}$

F.R. = FAILURE RATE

Read, Endurance, and Retention mechanisms are thermally accelerated; therefore, failure rates must be stated with temperature, confidence interval, and apparent activation energy.

Endurance is the most important because the endurance reliability is a direct function of the application, i.e., the number of times the device is rewritten during system operation. In other words, the total system life can be compromised by the endurance capability of the E²PROM. (Figure 1). For applications not requiring many rewrites or that must have byte clear, e.g., program storage, flash E²PROMs provide the best combination of cost and reliability. For applications requiring many rewrites, e.g., data storage or configuration, parallel E²PROMs provide the best combination. For applications requiring direct access to the controller, e.g., traceability, and lowest cost per device, serial E²PROMs are appropriate. Quality, delivery, service and product assurance are identical for all Catalyst E²PROMs.

Endurance is defined as: "The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes," per IEEE "Standard Definitions and Characterization of Floating Gate Semiconductor Arrays." The data sheet specifications include write functionality, data retention and read access time. For a Catalyst E²PROM, a nonvolatile data change is the completion of a program/erase cycle for each byte, i.e., transferring charge to and from the floating gate in the memory storage transistor.

Endurance has two primary failure mechanisms (Figure 2), which can result in any of three failure modes, i.e., data retention degradation, access time degradation or loss of write functionality. The charge is transferred on and off the floating gate through an oxide, resulting in the failure mechanisms of oxide damage and charge trapping. These mechanisms are caused by the cumulative effects of passing a current through a nominal insulator and placing a high electric field across an oxide. Thicker

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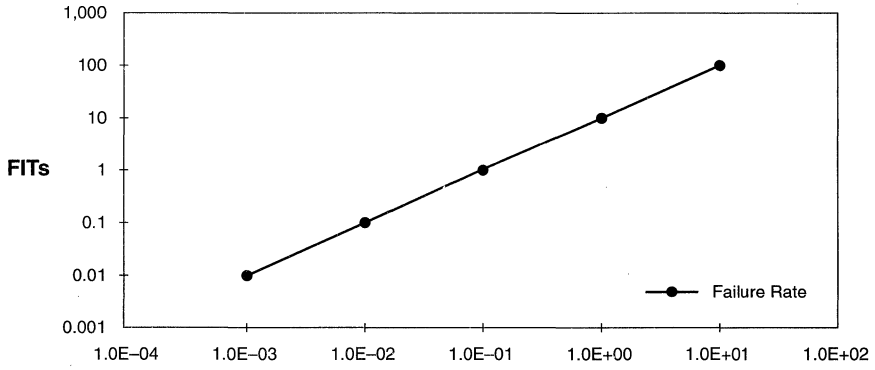
Figure 1. Endurance Cycles to Time Conversion Nomograph



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Endurance = .001%/1000 cycles

oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce initial oxide defects, which cause yield loss. Endurance cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design and processing must be such to minimize initial defects and reduce generated defects to the lowest possible level.

When a high number of endurance cycles before the onset of wearout is desired, error correction is suitable for oxide damage induced failures. Catalyst uses a byte error correction method to achieve extended endurance for high density parallel E²PROMs, e.g., the CAT28C256. Error correction is unnecessary for flash E²PROMs, which have a lower total number of endurance cycles specification or serial E²PROMs of low density. Error correction is not practical for charge trapping induced failures. A low failure rate during the useful life region is achieved by proper design, processing, and screening.

Endurance follows the "bathtub" curve, with a known infant mortality region, a useful life region, and a predictable wearout region. Endurance cycling has historically been the preferred method for screening and for periodic qualification testing. Cycling can be performed in real time and is the actual operating mode of the device.

Although intrinsic data retention is essentially infinity, the extrinsic data retention is a function of endurance. The endurance failure rate contains the extrinsic data retention failure rate induced by endurance. The intrinsic data retention failure fate is reported independent of endurance.

Test Method 1033 of MIL-STD-883 (Figure 3) describes the procedures to be used when performing endurance cycling for screening or endurance performance verification. Various means exist to eliminate infant mortality, which will be a function of product design and the dominant failure mechanism of the process. For example, floating gate devices usually contain an infant mortality data retention unbiased bake screen. Normal reliability monitoring on E²PROMs verifies operating life, data retention and endurance.

Random defects, occurring naturally in the wafer fabrication process, will cause infant mortality endurance or data retention failures. In neither case is there an explicit relationship that correlates infant mortality with device performance in the useful life or wearout regions. To improve yields, redundant memory in the device is used to repair initial or infant mortality failures in large or complex memory arrays. Due to the localized nature of the random defects that cause initial or infant mortality failures, the reliability of repaired and non-repaired devices is equivalent.

The endurance failure rate of the E²PROMs in a system will increase in importance as a function of the number of times the system rewrites the E²PROM during system life. System reliability is a function of the failure rate in the specified useful life region of the device, not when the onset of wearout occurs. Given the operating life failure rate of an MOS memory is in the order of 100 FITs (.01%/1000 hours), the endurance failure rate contribution should be an order of magnitude or more lower, (Figure 1). Catalyst serial, parallel and flash E²PROMs will meet system reliability requirements by providing the lowest endurance and total device failure rate for the specified system lifetime. The greater system reliability lowers the cost of ownership of a Catalyst E²PROM.

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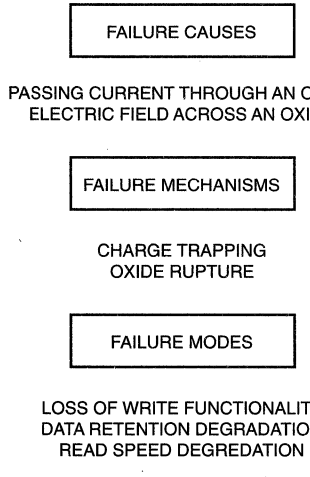
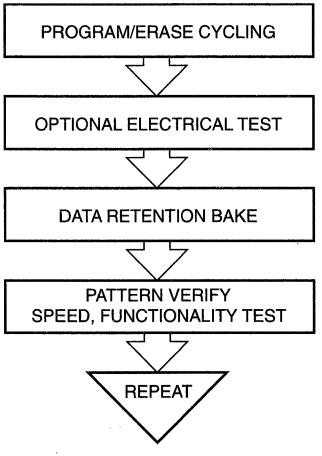
Figure 2. Endurance Failure Definition



5206 FHD F03

Figure 3. Endurance Testing Procedure MIL-STD-883, Method 1033



5206 FHD F04

E²PROM Reliability: On-Chip Error Code Correction for E²PROMs

INTRODUCTION

E²PROMs are reprogrammable nonvolatile rewritable semiconductor memories suitable for applications requiring in system periodic writing of new data. A write cycle requires standard TTL (transistor-transistor logic) levels available from the system 5 volt power supply. E²PROMs have electrical timing and parametric characteristics similar to other CMOS memories.

In addition to the read failure rate, the reliability of the E²PROM is a function of the data retention and endurance failure rates. The read failure rate is less than the read failure rate of comparable density volatile memories and intrinsic data retention is essentially infinite, i.e., hundreds to thousands of years. Endurance is the failure rate component that varies across technology and manufacturer.

Endurance, defined as the number of program/erase cycles before failure of any data sheet parameter, is limited by the mechanisms which transfer charge within the device. For a given design and technology, the E²PROM will have a predictable endurance failure rate and a finite limit to the useful life region (i.e., measurable onset of wearout). Thus, the reliability of the system is a function of the endurance capability of the E²PROM.

In order to enhance endurance for high reliability applications, E²PROM on-chip ECC (Error Code Correction) can be used. The benefits and constraints of the ECC method used for the CAT28C256 will be discussed.

FAILURE MECHANISMS

Various works have demonstrated that intrinsic E²PROM memory transistor endurance is limited by the build-up of negative charge in the tunnel dielectric and the time breakdown of the tunnel dielectric. The initial fabricated level of defects, the tunnel dielectric composition and structure, and memory circuit design will affect the generation rate of failing memory transistors during clear/write cycling. The endurance of the floating gate memory transistor follows the classic bathtub curve, with infant mortality, useful life, and wearout regions. The ability of ECC to improve endurance can be predicted during the useful life region when the memory transistor failure rate is constant.

The charge trapping and/or oxide damage mechanisms will eventually cause loss of functionality of the memory transistor, degradation in read access time, or extrinsic data retention degradation. These effects will occur randomly during the useful life of the E²PROM, prior to the onset of wearout. The failures (i.e., bit errors) are correctable by ECC. ECC will also correct normal MOS failures that affect the memory transistor.

Peripheral failures caused by endurance cycling are not correctable by on-chip ECC. Examples include failure in the charge pump, an address decoder, or output buffer. Test method 1033 of MIL-STD-883 provides the framework for establishing and verifying the endurance characteristics of E²PROMs, with or without ECC.

ERROR CORRECTION CODES

ECC is implemented using an element of length n consisting of k data bits and p check bits. When the element is accessed during a read cycle, the data and check bits are compared through an algorithm (ECC tree) to determine if an error exists and then to correct the error. Catalyst uses a modified Hamming code scheme to correct a single memory transistor error per byte.

The CAT28C256 memory element is a byte which consists of n = 12 bits, with k = 8 data bits and p = 4 check bits. During a read access all 12 bits are sensed and latched. The latched data is decoded to correct any single-bit error to provide to the 8 bit output byte. Similar circuitry is used to generate the check bits during write. The 8 bits of data in the input byte are latched and the 4 check bits are generated. The total of 12 bits per byte are loaded into registers for transfer to the memory transistors during the write cycle.

ECC MODEL

The ECC model calculates the probability of a device exhibiting no errors after some number of endurance caused memory transistor errors. Although, there may be some initial errors after manufacturing screening, these are usually replaced with redundancy; thus, at the beginning of the user's system life the device has no memory transistor errors. The purpose of ECC is to improve reliability, not manufacturing yield.

The device contains a number of ECC elements as a function of the device density, organization, and ECC scheme. All single bit errors within each memory element (byte) are correctable, regardless if the error occurs in the data or the check bits. An element with 2 or more errors is not correctable. If a memory element should have 2 or more memory transistor errors, the byte could read up to 8 bit errors. This requires that any *system* error detection and/or correction scheme not use the E²PROM byte as the basic element for ECC.

Given that:

B = number of bytes (ECC elements) in a device
n = number of bits in an ECC element (data + check)
c = number of endurance (program/erase) cycles
τ = constant memory transistor failure rate

The device hazard rate in %/1000 cycles is approximated by:

$$h(c) = n \times (n-1) \times B \times c \times \tau^2$$

The cumulative per cent failed is approximated by:

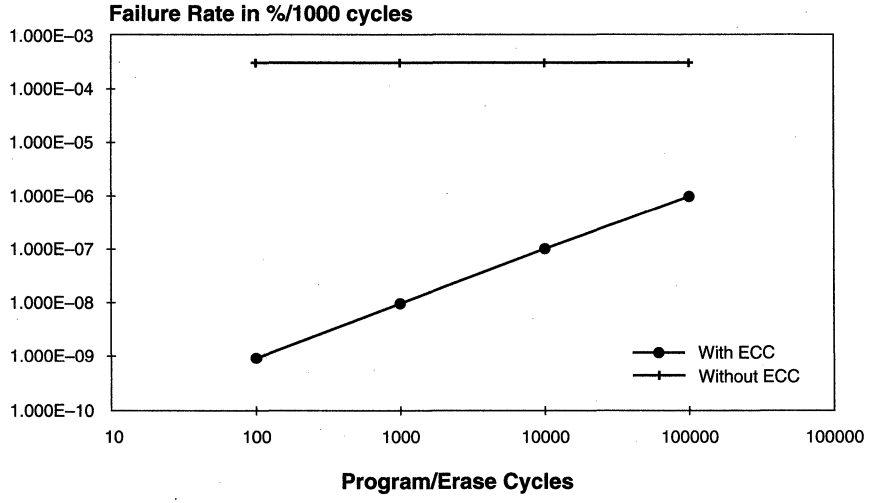
$$H(c) = (1/2) \times n \times (n-1) \times B \times (\tau \times c)^2$$

For Catalyst, the appropriate values are:

B = 32K = 32 x 1024 = 32768
n = 12
$\tau \approx 1.4 \times 10^{-7}$ %/1000 cycles

Figures 1 and 2 show the predicted memory array failure rates and cumulative per cent failures for a CAT28C256 E²PROM with and without ECC, as a function of program/erase cycles. The historical Catalyst memory transistor failure rate is lower than what has been reported by others, thus a Catalyst device with or without ECC has superior endurance reliability.

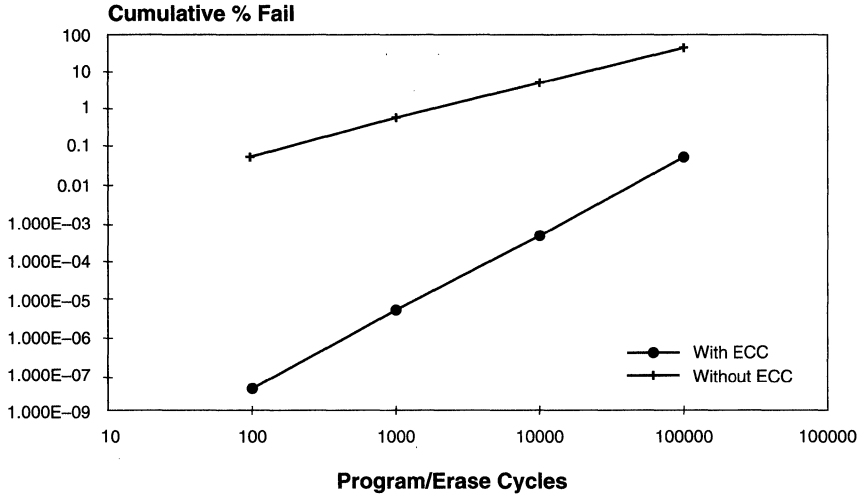
Figure 1. Predicted CAT28C256 Endurance Rate With and Without ECC



Constant transistor failure rate of 1.4E–7 %/1000 cycles

5207 FHD F01

Figure 2. Predicted CAT28C256 Cumulative Endurance With and Without ECC



Constant transistor failure rate of 1.4E–7 %/1000 cycles

5207 FHD F02

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Procurement Considerations for Reprogrammable Nonvolatile Microcircuit Memories

OVERVIEW

When procuring a microcircuit, many considerations are important. These may be divided into two categories: administrative and technical. Administrative issues, such as price, delivery, service and product assurance are not topics for discussion herein. Technical issues, such as performance, quality, and reliability will be addressed.

The performance of a microcircuit is evaluated on parameters specified in a data sheet. Quality is a measure of conformance to specification, typically expressed in PPM (Parts Per Million) nonconforming. Quality levels, as maximum PPM lot acceptance guarantees, are usually provided in manufacturers' warranty policies. Reliability is an expectation of quality over time, typically expressed as a failure rate in %/1000 hours or FITs (Failures In Time), or as an MTBF (Mean Time Between Failure). Reliability expectations are usually provided in manufacturers' reliability reports for device or process families.

Reprogrammable nonvolatile semiconductor memories have performance values, data sheets, and quality levels similar to other microcircuits. Reliability expectations are complicated by considerations of endurance and data retention, which have failure mode characteristics not applicable to other microcircuits. Thus, nonvolatile memories have additional procurement considerations that will affect manufacturing methods, data sheet specifications, quality levels and reliability.

The following sections discuss the elements necessary for a complete data sheet, critical parameters for evaluating the quality of a device and a reliability evaluation methodology.

COMMERCIAL SPECIFICATION PRACTICES

DATA SHEETS

Microcircuit electrical performance is specified by a data sheet. Data sheets may be very simple expressions of "nominal" performance levels or extensive listing of minimum and/or maximum performance levels under all allowed conditions. The magnitude of testing by the manufacturer usually correlates with the stringency of the specification. The most thorough and detailed device specifications are military (MIL-M-38510) slash sheets.

The device data sheet contains a description of how the device performs its intended function, e.g., how to write and to read from a memory; and a list of parameters with performance limits and conditions that define and specify how each function is implemented. Testing is utilized to validate the circuit performs as specified. Data sheet limits and values are based on considerations of device performance, system requirements and test capability. The ability to test parameter performance is critical in understanding various data sheet limits and values.

Device performance will predictably change as a function of environmental parameters. For example, with MOS devices, speed will be slower at high temperatures and power supply current will be higher at low temperatures. Therefore, the environment is specified. Device testing is performed at worst case conditions by the manufacturer to assure the user of device conformance to the data sheet under all allowable conditions. The power supply level directly affects the performance to the device; a lower value is worst case for most parameters because of the poorer conductivity of the MOS transistor. This is most evident for access times, which are generally slower at low V_{CC}.

Temperature is typically specified as: commercial 0 to 70 °C; industrial –40 to +85 °C; or military –55 to +125 °C, reflecting the severity of the expected application. Commercial and industrial temperatures are ambient temperatures; therefore, the junction temperature of an operating device will be higher than the ambient and the device must be tested at other than the specified limits. The test temperature can be calculated as a function of the specified temperature, the device power dissipation at the temperature limit, and the thermal resistance of the package. Military temperatures are case temperatures; therefore, the junction temperature will be the same as the case test temperature, e.g., the test temperature and the specified case temperature are the same, excluding guardbands. Ambient humidity is a test concern because at low temperatures condensation can freeze up in the equipment or cause leakage paths.

MOS devices are typically specified with ± 10% power supplies; however, both extremes need not be tested for all parameters. A worst case power supply condition, based on characterization, can be stipulated for most parameters. That is the only condition that should be tested in production.

MOS nonvolatile memory test parameters fall into three categories: AC or timing, DC or parametric, and functional. AC parameters are the maximum or minimum timing conditions needed for the device to function, e.g., address set-up times, data hold times; as well as the minimum/maximum responses from the device, e.g., access times. DC parameters are the static levels on each pin in the various operational modes, e.g., power supply current, input levels, output leakage. Functional includes those timing and static conditions, i.e., AC and DC parameters, necessary for the device to function in a given mode, e.g., read or write. The conditions, under which each parameter is specified, are usually included in the data sheet and should reflect how the device is tested.

Conventions for measuring parameters should be clearly stated, as device performance can change significantly for apparently minor differences in measuring methods. The most critical reference points are for AC or timing measurements. Timing limits are minimum and/or maximum timing values for each parameter. Input requirements for the device are specified from the external system point of view, i.e., what the system must provide to the device. Responses from the device are specified from the device point of view, i.e., what the device provides to the system. Timing edge reference points are required to differentiate between the input pulse levels or output levels and their respective (as recognized by the device) valid reference points. Edge reference points must be specified relative to where the device recognizes a valid signal level. Actual test specification edge reference points will generally indicate those points that the tester recognizes as the beginning of a transition for timing measurement, not where the device recognizes a valid signal. The difference provides a built-in guardband between test conditions and actual performance requirements. The levels specified for DC or static performance may not be the same levels specified for AC or timing performance.

Integral to the testing of an integrated circuit is the test philosophy utilized to determine which parameters are tested and in what manner. Included in the philosophy will be guardbanding methodologies, interface hardware design rules, test routine algorithms and characterization requirements.

Guardbanding is the off-setting of a parameter, condition, or attribute acceptance level from the specified value. This is done to account for variability in equipment and device performance or to make test programs more efficient and effective. Machine guardbands, implemented in the forcing, measured or external conditions, are required to account for the accuracy and precision capabilities of testers, interface hardware and handlers. Device guardbands are implemented where device performance greatly exceeds the parameter limit; thus, an early warning of a change in performance is available. Test program guardbands are implemented to speed up device testing, where worst case conditions can be applied based on predictable device behavior, e.g., for pattern sensitivities.

Parameter conformance to specification can be measured in a variety of ways. In variate testing, which is usually only used for characterization, the actual value of the parameter is determined. For DC parameters, this is relatively simple because the measurement is effectively the output of a voltmeter or ammeter. For AC parameters, this can be very complex, depending on the timing signal measured, because a narrow strobe must be continuously repositioned until the desired transition is detected or the reference edge must be continuously repositioned until the desired output is obtained. Variate testing, whether on an automated tester or a bench setup, is used primarily to validate the design and performance models for initial device release or after design changes.

Attribute testing is the comparison of a measured parameter under given conditions to a specified limit. The tested parameter then either passes or fails—go/no go. Some parameters are directly compared with the limit, while others must be "tested by inference" or "tested by the application of specified signals and conditions". Tested by inference is the validation of the performance of a parameter by the measurement of the correct performance of a correlated parameter or function. *Tested by inference* also applies when testing a worst case condition; therefore, all other conditions need not be tested. *Tested by the application of specified signals and conditions* is the applying of input parameters at their specified minimum or maximum and measuring the correct performance of a dependent parameter or function. Parameters that are outputs from the device are compared with standards or measured. Inputs to the device are tested by inference or application of specified signals and conditions.

Data sheets usually reference mechanical specifications for the packages containing the microcircuits. Most packages conform with either JEDEC Publication 95 or MIL-STD-1835. Otherwise, the manufacturer should have a similar specification providing all dimensional and material requirements. Visual and mechanical performance criteria per applicable specification are usu-

ally inspected for by the manufacturer before shipment of the devices. Dimensions, such as package thickness and lead spacing, may be critical for automatic insertion equipment operation. Composition, such as lead finish, may be critical for solderabilty. Explicit methodology for validating mechanical and visual performance is contained in MIL-STD-883, which is generally used as the baseline for all mechanical or visual inspection criteria.

RELIABILITY PARAMETERS

Reliability evaluation may be divided into two categories: mechanical and electrical. Nonvolatile semiconductor memories are assembled in packages using similar materials and processes as other microcircuits; thus, the mechanical reliability is the same. Mechanical reliability evaluations typically use JEDEC Standard 22 or MIL-STD-883 for test methods.

Electrical reliability for nonvolatile semiconductor memories is different from reliability for other microcircuits because reprogrammable nonvolatile memory reliability is the summation of the factors of operating life (read), data retention and endurance.

$$F.R._{device} = F.R._{read} + F.R._{endurance} + F.R._{data\ retention}$$

F.R. = Failure Rate

The read, endurance and data retention failure rates are thermally accelerated; therefore, must be given stating the temperature, confidence interval and apparent activation energy or alternative deacceleration technique.

Endurance is the most important because the endurance reliability is a direct function of the application, i.e., the number of times the device is rewritten during system operation. In other words, the total system life can be compromised by the endurance capability of the E^2PROM. Floating gate devices have a known endurance wearout mechanism, which is not a factor in normal operation, but can affect system performance if the specified number of endurance cycles is greatly exceeded.

Endurance is defined as: "The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes", per IEEE STD-1005-1991 "Standard Definitions and Characterization of Floating Gate Semiconductor Arrays". The data sheet specifications include write functionality, data retention, and read access time. Typically, a nonvolatile data change is the completion of a program/erase cycle for each byte, i.e., transferring charge to and from the storage node in the memory transistor.

Endurance has two primary failure mechanisms, charge trapping or oxide damage, which can result in any of three failure modes, data retention degradation, access time degradation, or loss of write functionality. The charge is transferred to and from the storage node through an oxide, resulting in the failure mechanisms of oxide damage and charge trapping. These are caused by the cumulative effects of passing a current through a nominal insulator and placing a high electric field across an oxide. Thicker oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce initial oxide defects, which cause yield loss. Endurance cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design and processing by the manufacturer must be such to minimize initial defects and reduce generated defects to the lowest possible level. Stressing and testing must be performed to separate devices with various levels of endurance performance.

When a high number of endurance cycles or a very low endurance cycle failure rate is desired, error correction is suitable for oxide damage induced failures. Bit or byte error correction methods are used to extend the endurance of devices whose dominant failure mode is oxide damage in the storage node. Error correction is not practical for uniform charge trapping induced failures. However, a low failure rate during the stipulated useful life region may be achieved by proper design, processing and screening.

Endurance follows the "bathtub" curve, with an infant mortality region governed by defects, a useful life region governed by the intrinsic integrity of the design and process, and a predictable wearout region governed by the cumulative effects of transferring charge through an oxide. Infant mortality is eliminated by the manufacturer during screening and testing. The useful life region failure rate level is assessed by way of product monitors. The onset of wearout is determined by extended endurance cycling, including stressing devices past the initial failure. Endurance cycling as a periodic qualification test has historically been considered the preferred means of verifying capability because cycling can be performed in real time and is the actual operating mode of the device.

Data retention has infant mortality, which must be screened in the manufacturing flow. There is a useful life region that is governed by the intrinsic integrity of the design and process. Wearout does not occur (in the sense that permanent, nonreversable degradation is present) because the storage node may be refreshed. Intrinsic data retention, the time the storage node is capable of retaining charge independent of the application, may vary by device design and process technology, but is essentially very long compared with real world operating conditions. The extrinsic data retention is a function of endurance. Endurance failure rate expecta-

tions should contain the extrinsic data retention failure rate induced by endurance. The intrinsic data retention failure rate should be considered independent of endurance.

Test Method 1033 of MIL-STD-883 describes the procedures to be used when performing endurance cycling for screening or endurance performance verification. Various means exist to eliminate infant mortality, which will be a function of product design and the dominant failure mechanism of the process. For example, some devices use endurance cycling and others use a margin test to screen out infant mortality. Most device manufacturing flows contain an infant mortality data retention unbiased bake screen. Military requirements contain a periodic Quality Conformance Inspection (QCI) which must be performed on JAN, SMD, or 883 compliant E^2PROMs to verify operating life, data retention and endurance. A similar requirement could be added for other reprogrammable nonvolatile devices.

Random defects, occurring naturally in the wafer fabrication process, will cause infant mortality endurance or data retention failures. In neither case is there an explicit relationship that correlates infant mortality with device performance in the useful life or wearout regions. To improve yields, manufacturers may include redundant memory in the device, used to repair initial or infant mortality failures. For large and complex memory arrays, e.g., RAMs, EPROMs, or E^2PROMs, few devices are shipped that do not include some level of redundancy repair. Due to the localized nature of the random defects that cause initial or infant mortality failures, the reliability of repaired and non-repaired devices is equivalent.

The endurance failure rate of the reprogrammable nonvolatile memories in a system will increase in importance as a function of the number of times the system rewrites the memory during system life. System reliability is a function of the failure rate in the specified useful life region of the device, not when the onset of wearout occurs. Given the operating life failure rate of an MOS memory is in the order of 100 FITs (.01%/1000 hours), the endurance and intrinsic data retention failure rate contributions should be an order of magnitude or more lower.

WARRANTY POLICIES

All microcircuit manufacturers provide warranty policies. These documents are typically broken into three categories: the warranty, the guarantee and the applicable conditions.

The warranty typically states that any nonconforming device may be returned to the manufacturer for credit or replacement. Conformance is to the data sheet or other applicable specification and is usually for a term of one year from date of shipment.

The guaranty is for lot acceptance and typically states that any lot that fails the lot acceptance sampling plan per the applicable specification may be returned to the manufacturer for credit or replacement, within one year from shipment.

The warranty policy will define those conditions under which devices may be returned, including administrative and technical requirements. Administrative requirements define the logistics and methodology of documenting and returning the affected devices, e.g., so that credit may be applied to the correct order. Technical requirements include: defining the condition of returned devices, e.g., must be testable, and the amount of correlation needed to validate nonconformance.

Lot acceptance guaranties, specified per the applicable lot acceptance sampling plan, will define guaranteed quality levels. Typically the quality level applies to all data sheet electrical parameters and the applicable mechanical/visual requirements but does not apply to reliability expectations. Parameters such as data retention and endurance, which although reliability expectations, can be treated as quality parameters; thus, often have a quality level or lot acceptance guaranty.

Quality levels, measured in PPM nonconforming, are estimates of the AOQ (Average Outgoing Quality) of the manufacturers' production line, post all screening, testing and sampling. JEDEC Standard 16 defines how to assess AOQ in PPM for microcircuit manufacturing. Transformation of AQL (Acceptable Quality Level) or LTPD (Lot Tolerant Percent Defective) sampling plans and lot guaranty levels to AOQ values are treated in standard texts on acceptance sampling.

The warranty policy should contain a definition and statement of guaranty for endurance and data retention. An example:

Endurance is the measure of the ability of a reprogrammable nonvolatile memory device to meet its data sheet specifications as a function of accumulated program/erase cycles. A program/erase cycle is the act of changing data from original (e.g., erased) to opposite (e.g., programmed) back to original for all bits of the memory array.

The memory shall be capable of the specified number of program/erase cycles per specified memory element, e.g., byte sector, page, independent of the programming or erase method, e.g., byte, page, sector, chip.

Data retention is the measure of the integrity of the stored data as a function of time. Data retention time is the time from data storage to the time at which a

repeatable data error is detected.

The device shall be capable of the specified number of years of data retention. This applies across the operating temperature range and after the specified minimum number of endurance cycles.

The memory has a lot acceptance guaranty of a 1% AOQL (LTPD 5/1) for the specified number of endurance cycles and data retention years, as verified by the specified test methodology (see the Verification section in Qualification Testing).

CRITICAL DEVICE PARAMETERS

ELECTRICAL

All electrical parameters are important for the correct functioning of the device in the application; however, a few tend to be more visible because they are the parameters that most often appear to fail.

Critical DC parameters are input/output leakage and power supply currents. High input/output leakage levels, typically caused by ESD (Electro-Static Discharge) or EOS (Electrical Over-Stress) will cause non-functionality by address lines, control pins or outputs being unable to go to correct levels. High power supply currents, either active or standby, typically caused by EOS, may overload supply lines and damage other components.

Critical AC parameters are access timing values and input/output level conditions. Access times are sensitive to data and address patterns; if the device is inadequately tested by the manufacturers, i.e., not using worst case data and address patterns, the device may occasionally read incorrectly in the application. Input/output level test conditions differ widely from device to device and manufacturer to manufacturer. Timing values are extremely sensitive to the applied input/output levels; thus, devices with supposedly the same timing value may function differently in the application because of different levels used during manufacturer's testing.

All parameters should be controlled by the manufacturer's internal documentation for how they are tested. Some parameters, e.g., capacitance, are only tested initially and after a design change that affects capacitance. Others should indicate if tested by inference or application of specified signals and conditions. The address and data patterns used for verifying write and read functionality as well as appropriate machine, test or device guardbands should be included in the documentation.

MECHANICAL/VISUAL

Critical mechanical parameters are: the package dimensions of thickness and lead spacing, which can affect how devices interact with automatic insertion equipment or the dimensions of the application; and solderability, which affects the mechanical, thermal and electrical connection of the device to the application.

Critical visual parameters are the marking of the device and the marking permanency. These are important to clearly and permanently identify the device, e.g., part number, date code, orientation.

RELIABILITY

Critical reliability parameters include endurance, data retention and package integrity. Endurance will be application dependent, i.e., how often the device is rewritten, will affect the overall failure rate. Data retention will be application sensitive, i.e., the intrinsic data retention failure rate of some devices or technologies may preclude some applications. Package integrity is not unique to nonvolatile memories but is also application sensitive, i.e., concerns with hermeticity especially for glass sealed packages and concerns with cumulative exposure to temperature and humidity for plastic packages.

Although not exactly reliability concerns, two other issues may be of concern when using nonvolatile memories: radiation tolerance and declassification ability. Radiation tolerance is a measure of how much radiation a device may receive and continue functioning. In some cases for similar technologies, radiation tolerance correlates with reliability performance, but is not always a means for comparing different nonvolatile technologies for reliability. Declassification ability is a measure of the difficulty or possibility of recovering information supposedly removed from the device.

MANUFACTURER'S SCREENING

ELECTRICAL

Manufacturing of microcircuits consists of three major steps: fabrication, assembly and test. Fabrication consists of various physical, chemical, photolithographic and inspection operations to form die on the microcircuit wafer. Assembly consists of placing microcircuit die in a package for connection to other elements. Test consists of identifying the conformance level of each microcircuit.

Normal microcircuit manufacturing practices include one or more 100% electrical tests, e.g., each device is tested for DC, AC and functional parameters, separating devices by performance level. For complex microcircuits such as nonvolatile memories, electrical testing before assembly is done at room temperature and electrical testing post assembly is at high and/or cold temperature. Military devices require testing at high, low, and room temperatures. MOS devices are worst case at higher temperatures; thus, commercial devices

may have a single insertion at high temperature and be guardbanded for parameters that are adversely affected by lower temperatures.

Complex devices are tested using automated testers (ATE—Automated Test Equipment) and test handlers with suitable interface hardware. The ATE is controlled by software, called a test program, which contains the various algorithms for testing a device. These will include the forced and measured values, guardbands, data and address patterns in a sequence sufficient to exercise all functions at applicable data sheet limits. In addition, manufacturer's test programs typically include special modes that allow operation of the device in a non-data sheet specified manner to improve test effectiveness or efficiency, e.g., apply an accelerating stress or reduce test time. Handlers will control the ambient temperature for test and segregate devices to various bins by test results.

Users should verify the manufacturer has fully documented the test program, interface hardware, the accuracy and precision of the test setup and the operating procedures for performing test.

RELIABILITY

Although microcircuits are designed for reliability, variability in the manufacturing processes could cause sooner than expected degradation of performance. This infant mortality is usually the result of random defects in manufacturing material or processes and may be detected by accelerated stresses.

Nonvolatile memories have two reliability parameters, endurance and data retention, which require evaluation and possible additional screening to remove infant mortalities. Screening of other reliability parameters should be consistent with that of other microcircuits fabricated with similar processes and assembled in similar packages. Test methods should reference MIL-STD-883 for hermetic devices or JEDEC Standards for plastic devices.

The manufacturer's test flow should include screens for endurance and data retention. Endurance screening is typically performing some number of endurance (program/erase) cycles or other oxide stress to accelerate defects in the charge transmission oxide. This is usually followed by a data retention stress, e.g., a high temperature unbiased bake, for a data retention screen. The manufacturer should be able to provide a methodology and data to support whatever endurance and data retention screens are used. Test Method 1033 of MIL-STD-883 provides a format for defining the requirements for an endurance and data retention screen.

QUALIFICATION TESTING

CHARACTERIZATION

Upon identification of a potential device for an application, the adequacy of the device for the application must be verified. Given the application constraints are known, this usually consists of characterizing the electrical and reliability performance of the proposed device. Before embarking on the very expensive effort of device characterization, several other activities should be performed.

The manufacturer should be audited by the user or users' representative, e.g., DESC or the NSI (National Supervising Inspectorate for the ISO-9000 series Quality Systems), for general capability to manufacture consistently a device that conforms to applicable specifications. This will include system capability as well as specific technical abilities. Then the manufacturer should provide information to the user, detailing the manufacturing technology and device performance specifications and reliability expectations.

Once satisfied that the manufacturer and device comply with the application requirements, the user should obtain some devices for validation of promised results. User testing should verify performance to the data sheet or other applicable specification and should be used to establish correlation between the manufacturer's inspection and the user's application. Critical electrical and mechanical/visual parameters should require extra attention to assure consistency in measurement.

Reliability parameters should receive characterization, in particular endurance and data retention. Program/erase cycling and data retention bake should continue until the onset of endurance wearout, i.e., where the endurance failure rate increases with additional cycles. Verification of the intrinsic data retention failure rate should establish, using standard deacceleration techniques, that the MTBF of the nonvolatile memory is greater than the application's required storage time. Other reliability parameters, such as life test, may use data provided by the manufacturer.

A typical endurance and data retention characterization test would consist of choosing two samples; then: subject the first sample to the number of endurance cycles at the temperature used in the application followed by a data retention bake that correlates to the storage time required of the application. Subject the second sample to increasing numbers of program/erase cycles, interleaved periodically with short data retention bakes until the majority of devices have failed two or more bits. Analysis of this data in conjunction with the manufacturers supplied data should validate the feasibility of the proposed device in the application.

VERIFICATION

After characterization verifies the microcircuit is capable of meeting the application requirements, some ongoing testing will be required to assure production deliveries continue to conform to specification. Commonly used methods include: source inspection, incoming inspection, regular audits and periodic monitors.

Source inspection requires the user or designate to witness critical manufacturing or quality assurance operations to verify shipped product conforms to the applicable specification. Incoming inspection accomplishes a similar purpose by having the user inspect production material upon receipt.

Regular audits are the occasional assessment of the manufacturer by the user to assure that manufacturing methods, systems, procedures and specifications are being adhered to in the ongoing production of the purchased microcircuits. Periodic monitors are the subjecting of a sample to an incoming test or a characterization evaluation.

Incoming inspection is probably the least productive of the various verification methodologies and certainly the most expensive. Regular audits, combined with periodic monitors is probably the most effective but requires a skilled and trained audit and evaluation team to implement. Source inspection is the simplest and probably least expensive means to verify product conformance to specification. The means that are most appropriate to situation depend on the relationship of manufacturer and user, the capabilities of both parties, and any other overriding considerations, e.g., government requirements. In all cases, regular communication between manufacturer and user is vital to assure ongoing performance improvement.

Reliability parameters should be monitored by the manufacturer's reliability reports. In addition, endurance, data retention, and steady state life performance can be periodically validated by the following methodology:

An endurance test, reference Method 1033 of MIL-STD-883, shall be added before performing the steady state life test and extended data retention test. Cycling may be chip, sector, block, byte or page on finished devices. The following conditions shall be met:

1. All bytes shall be cycled for a minimum of the specified number of cycles at equipment room ambient.
2. Perform parametric, functional and timing tests at room temperature, after cycling. Devices having bits not in the proper state after functional testing shall constitute a device failure. Separate the devices into two groups for extended data retention and steady state life test, then write correct data patterns.
3. Perform the extended data retention, consisting of a high temperature unbiased storage for 1000 hours minimum at +150°C minimum. The storage time may be accelerated by using a higher temperature according to the Arrhenius relationship and an apparent activation energy of .6eV. The maximum storage temperature in a Nitrogen environment shall not exceed +175°C for hermetic or +160°C for plastic devices. All devices shall be programmed with a charge on all memory cells in each device, such that a loss of charge can be detected e.g., worst case pattern.
4. Read the data retention pattern and perform parametric, functional and timing tests at room temperature, after cycling and bake. Devices having bits not in the proper state after functional testing shall constitute a device failure.
5. Perform steady state life, reference method 1005 condition D of MIL-STD-883, for 1000 hours at +125°C in a Nitrogen environment. The steady state life time may be accelerated by using an Arrhenius relationship and apparent activation energy of .4 eV. The maximum operating junction temperature shall not exceed +175°C. All devices shall be written with a checkerboard or equivalent topological alternating bit pattern.
6. Read the steady state life pattern and perform parametric, functional and timing tests at room temperature, after cycling and steady state life. Devices having bits not in the proper state after functional testing shall constitute a device failure.
7. The endurance, data retention and steady state life tests shall individually pass a sample plan to an LTPD of 5/1 (sample size = 77, accept = 1), equivalent to an AOQL = 1%.

SUMMARY

Reprogrammable nonvolatile memories should be procured with the same care as other microcircuits. The additional application dependent reliability parameters of endurance and data retention require careful consideration of device design, manufacturing methodology, reliability criteria and documented performance.

Full-Featured E²PROM Cell Operation

The Catalyst full-featured E²PROM memory cell, used for both serial and parallel devices, consists of an MOS floating gate memory transistor, a select transistor and support circuitry (Figure 1). The memory cell defines a logic state, either a "1" or a "0," by storing negative or positive charge on the floating polysilicon gate of Q1. The status of the gate is sensed during the read operation.

Charge is transferred to and from the floating gate through the thin tunnel dielectric by Fowler-Nordheim tunneling; i.e., the quantum-mechanical transmission of an electron through the oxide bandgap. Tunneling occurs when a high voltage, generated within the die, is placed across the tunnel dielectric region of the memory transistor.

For a logic "1," electrons are stored on the floating gate, using the conditions defined for "erase" (Table 1). Q1 has the high voltage placed on the top polysilicon gate, via the sense line through Q4 and Q5. The source and drain are grounded, through array Vss, Q2 and Q3 respectively. Fowler-Nordheim tunneling, generated by the high field from the top gate to the drain, will transfer electrons to the floating gate. The net negative charge will raise the Q1 threshold to a value greater than the reference voltage.

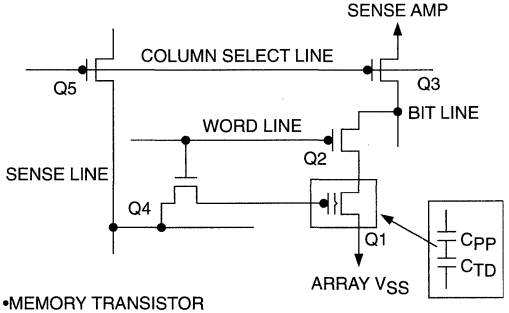
For a logic "0," holes (absence of negative charge) are stored on the floating gate, using the conditions defined for "program" (see attached table). Q1 has a high voltage place on the drain, via the bit line through Q2 and Q3. The top gate is grounded through Q4 and Q5, and the source is floating. Fowler-Nordheim tunneling transfers electrons off the floating gate. The net positive charge will lower the Q1 threshold to a value less than the reference voltage.

During the read operation, the reference voltage is applied to the top gate of Q1 via the sense line. For Q1 thresholds greater than the reference voltage, the selected Q1 will not conduct. The cell current on the bit line is detected by the sense amplifier and the resulting output is a logic "1".

Q2 isolates unselected memory transistors on the same bit line, eliminating program and read disturb. Q4 isolates unselected bytes on the same sense line, eliminating DC program, DC erase and read disturbs.

Support circuitry is used to input and output data to and from the memory in various modes, e.g., serial, parallel, page. Error correction can be implemented using multiple cells and an ECC algorithm.

Figure 1. Generic Full-Featured E²PROM Memory Cell



Q1•MEMORY TRANSISTOR
Q2•ROW SELECT TRANSISTOR
Q3•COLUMN SELECT TRANSISTOR
Q4•BYTE SELECT TRANSISTOR
Q5•SENSE SELECT TRANSISTOR

Table 1. Full-Featured E²PROM Memory Cell

	ERASE	PROGRAM	READ
Bit Line	0	20 V	1.5 V
Column Select	0	0	5V
Word Line	20 +Vt V	20 +Vt V	5 V
Sense Line	20 V	0	2 V
Array VSS	Ground	Floating	Ground

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Flash Memory Cell Operation

The patented Catalyst flash memory cell consists of an MOS Floating Gate memory transistor and support circuitry (Figure 1). The memory cell defines a logic state, either a "1" or a "0," by storing two different levels of negative charge on the floating polysilicon gate of Q1. The status of the gate is sensed during the read operation.

Charge is transferred to the floating gate through the gate oxide by channel hot electron injection. Charge is transferred from the floating gate by Fowler-Nordheim tunneling; i.e., the quantum-mechanical transmission of an electron through the oxide bandgap. Both transmission mechanisms require the application of a high voltage, which may be supplied externally or generated within the die.

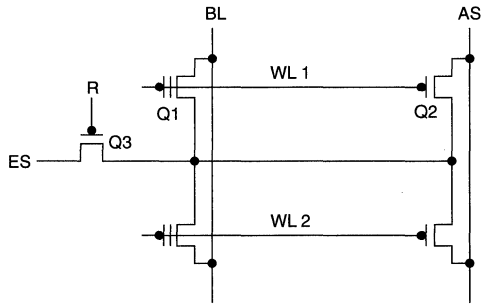
For a logic "0," electrons are stored on the floating gate, using the conditions defined for "program" (Table 1). Q1 has the high voltage placed on the top polysilicon gate, via the word line, and the drain, via the bit line. Q1's source is connected to array source, which is at ground, through Q2. Channel hot electrons, generated by the source-drain potential, are swept to the floating gate by the top gate to substrate field. The excess negative charge will raise the Q1 threshold to a value greater than the reference voltage.

For a logic "1," a reduced quantity of electrons is stored on the floating gate, using the conditions defined for "erase" (see attached table). Q1 has a high voltage placed on the source, via the erase source through Q3. The top gate is grounded, via the word line, and the drain is floating. Fowler-Nordheim tunneling transfers electrons off the floating gate. The Q1 threshold is lowered to a value less than the reference voltage.

During the read operation, the reference voltage is applied to the top gate of Q1, via the word line. For Q1 thresholds greater than the reference voltage, the selected Q1 will not conduct. The cell current on the bit line is detected by the sense amplifier and the resulting output is a logic "0".

Q2 isolates unselected memory transistors on the same bit line, eliminating program disturb. Q2 also isolates every 16 memory transistors along the word line, preventing DC program and DC erase disturbs. Q3 isolates each sector for erasure, preventing overerase of unselected sectors.

Figure 1. Generic Flash Memory Cell



Q1 • MEMORY TRANSISTOR
Q2 • PASS GATE (EACH 16 COLUMNS)
Q3 • SECTOR SELECT (EACH 16 ROWS)
EVERY 16 ROWS • 2K BYTES • 1 SECTOR

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Table 1. FLASH Memory Cell

	PROGRAM	ERASE	READ
BL (Bit Line)	≈7 V	Floating	≈1 V
WL (Word Line)	V_{pp}	0	V_{CC}
AS (Array Source)	0	0	0
ES (Erase Source)	0	V_{pp}+	0
R (Sector Select)	OFF (0)	V_{pp}+Vt	OFF (0)

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Failure Rate Prediction

Integrated circuits have no moving parts, yet like all functional devices have a possibility of failure. Although the future of an individual device cannot be predicted, the lifetime of a population of devices will have predictable behavior. The expected lifetime will be a function of the design, manufacturing, screening and testing history of the population.

Failure rate predictions are used to estimate the longevity of applications using the devices. Reliability is often described as device performance over time; thus, the behavior of populations of devices is mathematically described using probability models. Probability density functions and cumulative distribution functions are used for predictions of failure. Some commonly used terms and definitions are:

1. Mortality Function (Probability Density Function of Time-to-Failure); f(t):

The rate at which devices are failing referenced to the original population. f(t)dt is the probability the device will fail in the interval "t" to "t + dt."

2. Cumulative Mortality Function (Cumulative Distribution Function of Time-to-Failure), F(t):

[a] the integral of f(t).
[b] the probability that a device will have failed by time "t";
[c] the fraction of units that have failed by time "t."

3. Cumulative Reliability Function; R(t) = 1 – F(t):

[a] the probability that a device will function at time "t";
[b] the fraction of units that have survived to time "t."

4. Hazard Rate (Instantaneous Failure Rate); h(t):

The rate at which devices are failing referenced to the survivors.

h(t) = f(t) / R(t).

5. Cumulative Hazard Function; H(t):

The integral of h(t).

6. FIT:

***F**ailure **I**n **T**ime: the number of failures per 10^9 hours. Typically used to express the failure rate.*

7. %/1000 hours:

An alternative expression of the failure rate.

Many population failure distributions have been utilized; e.g., the normal, lognormal, weibull, exponential extreme value. The exponential (similar to the weibull with $\beta = 1$) is often used for modeling because of its ease of use and applicability. The exponential is appropriate for failures caused by random latent defects or a component of many constituents.

The failure rate of devices is expected to vary over the lifetime of the population. This behavior is modeled by the classic "bathtub curve"; which includes an infant mortality region, an intrinsic or useful life region and a wearout region.

Infant mortalities are a result of latent defects or poor manufacturing practices, which result in early failures and a sharply declining failure rate. The device manufacturer should eliminate this region by design or screens, i.e., accelerated stresses that are part of the manufacturing flow.

The wearout region is caused by an accumulation of stress during the operation of the device, resulting in an increasing failure rate. This region is eliminated by the user choosing a device of sufficient reliability for the application.

The useful life region is a function of the intrinsic capability of the device including the design, construction materials, manufacturing, and screening flow. This region is characterized by a relatively constant failure rate; thus, the exponential is an appropriate distribution: $f(t) = \tau e^{(-\tau t)}$ and $h(t) = \tau$; where τ is the constant hazard rate.

The reliability performance of a microcircuit population is evaluated by stressing a sample. The stress is performed at conditions which should accelerate the failure rate during the stress, relative to normal operating conditions. Because a sample is used, the estimate (τ) of the population hazard rate (τ) is derived by statistics. The χ^2 (chi-squared) distribution is used to determine the τ confidence interval.

$$\tau = x / \{2 \times \Sigma ntA\}$$

where χ is the tabular value of the χ^2 for the desired confidence (α), with 2r + 2 degrees of freedom (r = the number of failures in the sample).

n = the number of devices on stress.
t = the duration of the stress for each passing device.
A = the acceleration factor.

The failure mechanisms that contribute to the failure rate vary with temperature. The mortality function is the probability distribution that represents the aggregate of these mechanisms; thus, the mortality rate will vary with temperature. Analogous to modeling the rate of a chemical reaction, the Arrhenius equation is used to model the shift in the mortality distribution. The apparent activation energy, associated with various failure mechanisms, quantifies the temperature dependence of the distribution's shift.

The acceleration factor, A, is calculated by the Arrhenius equation and the apparent activation energy:

$A = \exp\{[Ea/k][(1/Tn) - (1/Tj)]\}$ where,

Ea = the apparent activation energy.

k = Boltzman's constant (8.62×10^5)

Tn = normalized junction temperature °K.

Tj = stress junction temperature in °K.

Models for infant mortality and wearout have been derived, but are not pertinent to useful life failure rate prediction.

EXAMPLE

A sample of 77 devices is submitted to dynamic burn-in at an ambient oven temperature of 150°C for 2000 hours, with 1 failure at 1000 hours. What is the 90% confidence interval estimation of the failure rate at 55°C ambient operating.

$\tau 150 = X / \{2 \times \Sigma nt\}$

where X = 7.779 for α = .90 and degrees of freedom = 4 [(2 x1) + 2]

Σnt = (76 x 2000) + (1 x 1000) = 153,000

thus

$\tau 150$ = 7.779 / (2 x 153,000) = 25,422 FITs

$\tau 55 = \tau 150 / A$

Notes: The typical Ea for an MOS device in dynamic burn-in is .4. Ambient temperatures were given and the equation requires junction temperatures. For this die and package, assume the junction temperature rise is 5°C; therefore,

$A = \exp\{[.4/8.62 \times 10^5] \times \{[1/(55+273+5)] - [1/(150+273+5)]\}\}$

= 22

$\tau 55$ = 25,422 / 22 = 1156 FITs

The estimation of a failure rate based on a single small sample is limited by the statistics of the sample size. In order to have true representations of the population failure rate, data must be combined from several samples. Therefore, typical failure rates are given for device families or technologies, not individual device types.

Single Transistor 5V Flash Technology, with Sector Erase

A 1.0μm Flash technology has been developed, for full device operation with one external 5V power supply. The single transistor Flash cell has been used to obtain a high density with the smallest possible die size, which minimizes cost.

The use of a 5V power supply enlarges the range of applications and reduces cost, by eliminating the need for an additional power supply.

The use of sector erase is particularly suited to applications where a boot program must remain unchanged while the program memory or remaining data is updated. One chip providing both functions will reduce the number of chips on the board. Otherwise, a standard design would use an E^2PROM or battery backed-up RAM, for updatable memory, and a PROM or EPROM to store the boot program.

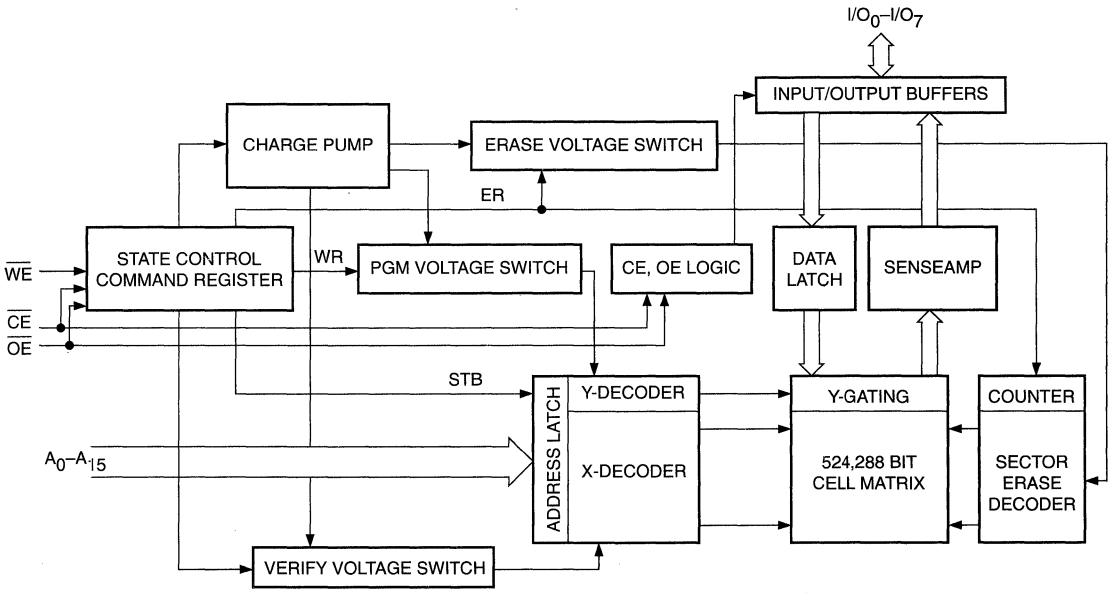
The advantages of one 5V power supply, one chip for boot and updatable memory, and device price will significantly reduce the cost of an application.

The 5V functionality is achieved by means of 2 charge pumps:

a. one providing 10 mA at 7V during programming and 5 mA at 13V during erase,

b. one providing 100 μA at 13V, during programming to pump up the Word Lines and during erase to control the sector decoder.

Figure 1. Block Diagram



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The design of a 5V to 13V converter with high output current implies not only a careful sizing of the capacitors and diode mounted transistors, but requires noise reduction features, such as separate ground lines, stepped clocks and pump output regulation (Figure 1, Block diagram).

The array consists of 8 blocks, one for each I/O pin. To ground the cell source during read and program, pass gates are regularly distributed along each word line. To bring the cell source to a high voltage during erase, each source is tied, through an erase decoder, to the erase voltage internal supply. The sector size is 2K bytes, consisting of 16 rows in each block.

The addition in the array of the pass gates and erase gates allows the erase of single sectors. These gates decrease the leakage on each bit line, since only 16 cells on one bit line have their source grounded at one time. This provides extra protection against the risk of "over-erase," e. g., disturb of the accessed cell by unselected depleted cells (Figure 2, array structure).

The sectors can either be erased one by one at random, or sequentially. One by one, an erase pulse is sent selectively to the chosen sector. The sector data is then verified and other erase pulses are sent, if necessary. Sequentially, each erase pulse increments the sector pointer, so that all sectors erase within the same subroutine. A reset command initializes the sector pointer. The sequential erase is faster for a program memory update, with boot sectors unchanged. The random sector erase is faster for a data memory update, with other data sectors unchanged.

Preliminary reliability evaluations verify the usual floating gate data retention of greater than 100 years. Endurance is specified at 1% AOQL for 1000 cycles, which is more than adequate for program memory and many data memory applications. The technology is intrinsically capable of high endurance; however, the potential additional screening requirements are not compatible with making a low cost device.

The circuitry and technology have been developed for a high density, reliable, cost effective 5V only Flash memory.

A 512K bit, CAT28F512V5, has been designed with this technology, and is now in pre-production. A 1 Megabit, CAT28F010V5, is in development.

Figure 2. Array Structure

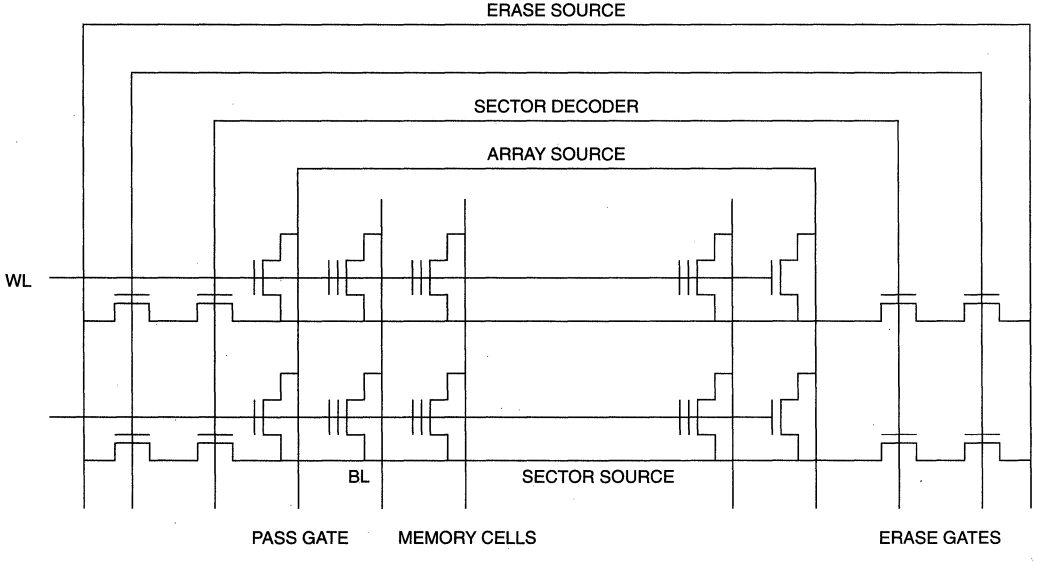

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Table 1. Device Characteristics (Typical)

Access Time	120 ns
I_{CC} Standby	10 µA
I_{CC} Read (8.3 MHz)	30 mA
I_{CC} Program	50 mA
I_{CC} Erase	20 mA
Program Time	10 µs/byte
Erase Time	100 ms/sector

Table 2. Process Characteristics

Erase Mechanism	Tunneling
Program Mechanism	Hot Electron Injection
Tunnel Oxide	11 nm
Gate Oxide	25 nm
Polysilicon Layers	2
Metal Layer	1
Metal Thickness	1.0 µm
Metal Width	1.4 µm
Metal Spacing	1.2 µm
Cell Size	16.8 μm^2

Features and Performance of Reprogrammable Nonvolatile Floating Gate Memories

INTRODUCTION

Over the past 15 years, various floating gate devices have been increasingly used for reprogrammable nonvolatile memory (NVM) applications. The UV-EPROM, developed as an engineering prototype tool, gradually replaced the original IC memory for program storage, the ROM. The UV-EPROM technology evolved into the E^2PROM technology, and the two have recently merged to create the flash E^2PROM and EPROM technology.

The floating gate MOS transistor allows the use of a multitude of design approaches to satisfy user needs. The major device categories are NVRAM, serial E^2PROM, parallel E^2PROM, flash, UV-EPROM and the OTP-EPROM. This paper will compare the features and performance of these categories.

APPLICATIONS

Comparisons must start with the application perspective. Reprogrammable nonvolatile memories are required where information may be changed during operation and must be retained during power-off. The two major types of information are data and program, each type contains several classifications.

Data memory includes information from recorders or sensors that is required for historical purposes or to maintain continuity of operation after power loss.

Program memory can be classified as configuration, traceability, boot program or main program. Configuration contains look-up tables or other settings to control the features and set-up of different equipment and formats within the system. Traceability includes calibration and maintenance settings and history, as well as self-test vectors. The boot program is the series of instructions necessary to start the system. The main program is the algorithm or operating system, containing the instructions to operate the system.

Within each classification of memory, the actual application requirements may vary. Intrinsically, floating gate memories have different performance characteristics and limitations. These must be carefully matched with the application. Some of the most important system considerations are: how many times must the memory be reprogrammed, what is required to change the memory, what voltages must the system supply, how much memory is required and how much does the memory function cost?

These system considerations can be directly compared with NVM features and performance. How many times the memory must be reprogrammed is related to device endurance, i.e., the minimum number of program/erase cycles at a given failure rate (or cumulative percent fail). What is required to change the memory relates ease of erasing and reprogramming the device, i.e., the level, timing, and sequence of waveforms. What voltages the system must supply for device operation relates to tradeoffs in cost and performance issues of the circuit board.

How much memory is required varies by memory classification and available device density. How much the memory function costs depends on what categories and densities of memory and support devices are required.

DEVICE FEATURES AND PERFORMANCE

Important device parameters include speed, write method, power supply requirements, endurance, data retention, density, package pin count and types of usable packages. Speed involves both read and write time impact on system performance. The erasing and programming method, e.g., pulse or algorithmic, affects the total time to change the system memory. Some devices require the system to be interactive with the device during writing, while other devices allow alternate system operations to be performed in parallel.

The endurance capability, typically the number of program/erase cycles to meet a 1% AOQL guarantee, is normally much greater than the system update frequency requirement. Data retention of floating gate

devices is essentially infinite compared to alternates such as batteries or SNOS. The power supply voltage and power dissipation relate to circuit board design and the types of other components required, e.g., a 3 volt device may be more suitable for portable applications.

The number of transistors per memory cell relates directly to density and die size, thus cost. The die function and size also determine what package types and pin counts are suitable.

CONCLUSION

Selection of a device for an NVM application is a complicated task. A number of floating gate reprogrammable nonvolatile memory devices exist, with a wide variety of features and performance, which further complicates the selection. This paper has summarized the status of existing devices, comparing critical features and performance to simplify the choice of the most appropriate device for a given application.

Table 1. Application Comparisons

	Application	Update Frequency	Ease of Write	Density Range	Cost/ Bit	Cost/ Device
NVRAM	Data	Store or Power Down	Very Easy	256 bit to 1K	High	High
Serial	Configuration	Power Down	Easy	256 bit to 16K	Medium	Low
Parallel	Data, Boot Program, Main Program, Configuration, Traceability	1–5/day 1–2/year 1–2/year Power Down 2–6/year	Easy	4K to 1M	Medium	High
Flash	Main Program, Boot Program, Data	1–2/year 1-2/year 1–4/month	Moderate	64K to 2M	Low	Medium

Table 2. Performance Comparisons

	Read Speed	NV Write Speed	NV Write Method	Endurance	Power Supply Required	Typical Power Dissipation
NVRAM	200ns to 100 KHz	10ms /device	Store Device	10,000	5V	100mw to 200mw
Serial	250 KHz to 2 MHz	5–10ms /address	Pulse: Address	100,000	2, 3, 5V	15mw
Parallel	35ns to 250ns	1–10ms /byte,page	Pulse: Byte, Page	10,000 100,000	3, 5V	100mw to 500mw
Flash	150ns to 250ns	10–100 µs /byte	Algorithmic Chip, Sector	100,000	5V or 5V & 12V	150mw to 500mw

Table 3. Technology Comparisons

	Endurance	Data Retention	Density Range	Transistors Per Cell	Package & Pins	Package Types[1]
NVRAM	10,000	>100 years	256 bit to 1K	9–13	8–18	SMT,TH,MOD
Serial	100,000	>100 years	256 bit to 16K	2	8–14	SMT,TH,MOD
Parallel	10,000 100,000	>100 years	4K to 1M	2–6	24–44	SMT,TH,MOD
Flash	100,000	>100 years	64K to 2M	1	28–44	SMT,TH,MOD

Notes
1. SMT = Surface Mount Technology, TH = Through Hole, MOD = Module or Hybrid

CATALYST SEMICONDUCTOR

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Catalyst Die Products

INTRODUCTION TO UNENCAPSULATED DIE

This document provides the user with guidelines for processes, testing, and application issues associated with purchasing unencapsulated die or wafers. Product electrical specifications, functional descriptions, and bonding diagrams are not included. This information is available in the appropriate sections of the Catalyst Data Book or directly from Catalyst.

The guide provides recommendations for die attach and wire bonding methods. Typicals for die thickness, top glassivation composition and thickness, and metalization composition and thickness are included. The Catalyst production flow is outlined herein showing the steps taken for each die or wafer shipment. In addition, application information covering some common issues encountered when using die is provided.

Properly packaged die and wafers will perform according to the parametric, AC, and DC parameters listed in the device data sheet. Procedures to demonstrate conformance to these specifications should be established contractually with Catalyst on an individual basis.

STANDARD DIE SALES GUIDELINES

Reliability Expectations:

1. Endurance/Data Retention: 5% AOQL.
2. Life Test: Same as packaged units; see reliability reports.

Guarantees(1):

1. 1% AOQL for Visual per Standard Commercial Procedure for plated and inspected die.
2. Packing/Shipping per "Packaging" Section, in accordance with Catayst shipping specification 17001.

Correlated Yields:

1. Expect initial yields while doing correlation to be:
   A. ≈70% for high density devices (≥ 64K bits).
   B. ≈90% for low density devices (≤ 16K bits).
2. After correlation, yields should be:
   A. ≈90% for high density devices (≥ 64K bits).
   B. ≈95% for low density devices (≤ 16K bits).

Notes:
1) 1% AOQL for visual per MIL-STD-883, Method 2010, Condition B for plated and inspected die is available. Please contact Catalyst for price adder.

Test Modes:

Catalyst uses control fuses for various built-in test modes and other functions within some devices. Exposure to UV light or misapplications of high voltages can erase or reprogram the fuses, causing loss of functionality. Control fuses are used for redundancy repair to improve manufacturing yield and chip functions to reduce test time. Catalyst strongly recommends the use of control fuses.

STANDARD DIE PACKAGING

All die shipped by Catalyst will be packaged per the following:

1. The die will be placed in a "waffle pack" with a cavity of proper size to restrain the die without causing damage and without allowing the die to change orientation.
2. A lint-free paper insert is placed over the "waffle pack". The waffle pack lid is placed on top and then secured with plastic locking clips.
3. A set of waffle packs (as required) are stacked.
4. A label with lot number, quantity, part number, and packing date is placed on the waffle pack.
5. Die do not require cleaning prior to assembly.

STANDARD WAFER PACKAGING

All wafers shipped by Catalyst will be packaged per the following:

1. Wafers will be separated by lint-free paper.
2. Wafers will be packed in an appropriately sized shipping container to minimize movement.
3. A label with lot number, quantity, part number, and packing date is placed on the shipping container.
4. Catalyst procedure allows for shipping a Broken Wafer, if it is broken in not more than 3 parts.

GENERAL DIE or WAFER SPECIFICATIONS

1. Thickness: 350 to 430 µm (14 to 17 mils).

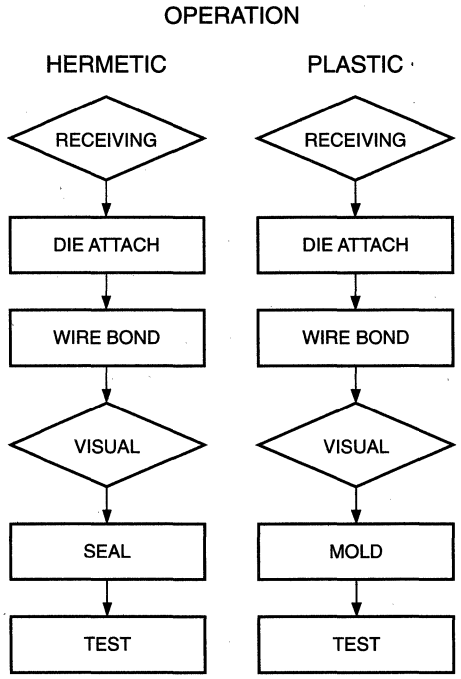
   Other thicknesses down to 280 µm (11 mils) can be accomplished. Please contact Catalyst for additional information.

2. X-Y Dimensions: Per each device (contact Catalyst). Wafer diameter: 125 or 150 mm (5 or 6 inches).

3. Top Glassivation: Varies according to device and manufacturing location. Typically 1 µm of SiON (oxynitride).

4. Metalization: Varies according to device and manufacturing location. Typically 1 µm of Al/Si (99/1) or Al/Si/Cu (98.5/1/.5).

SUGGESTED ASSEMBLY FLOW AND CONDITIONS



CONDITIONS

DOCUMENTATION CHECK. OPTIONAL

VISUAL - 1% AOQL (SAMPLE)
MECHANICAL/FUNCTIONAL - 2.5% AOQL

HERMETIC: SILVER-GLASS WITH VENDOR RECOMMENDED CURE PROFILE.
PLASTIC: EPOXY WITH VENDOR RECOMMENDED CURE PROFILE.

HERMETIC: 99%/1% AL/SI 1.25 MIL WIRE ULTRASONIC WEDGE BOND.
PLASTIC: GOLD 1.3 MIL WIRE, 200°C THERMASONIC BALL BOND.

MIL-STD-883, METHOD 2010, CONDITION B OR COMMERCIAL STANDARD

HERMETIC: GLASS FRIT, PEAK TEMP < 430°C
SOLDER SEAL, PEAK TEMP < 370°C
PLASTIC: LOW STRESS MOISTURE RESISTANT MOLDING COMPOUND.

TIMING, PARAMETRIC, FUNCTIONAL

For additional questions, please contact your local Catalyst Sales Representative.

Note:
(1) Final electrical screen and test yield will vary with device type data sheet performance limits (i.e. access time, temperature range, V_{CC} range and use of redundancy).
(2) For some devices, test yields may be improved by the use of redundancy repair. Information on how to use redundancy repair is available from Catalyst.

CATALYST SEMICONDUCTOR

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Product Selector Table

Serial E²PROMs

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24C01P	128 X 8	PDIP	8	1Kb	4.5-5.5	400kHz	C	
24C01PI	128 X 8	PDIP	8	1Kb	4.5-5.5	400kHz	I	
24C01P-2.7	128 X 8	PDIP	8	1Kb	2.7-6.0	100kHz	C	
24C01PI-2.7	128 X 8	PDIP	8	1Kb	2.7-6.0	100kHz	I	
24C01P-2.5	128 X 8	PDIP	8	1Kb	2.5-6.0	100kHz	C	
24C01PI-2.5	128 X 8	PDIP	8	1Kb	2.5-6.0	100kHz	I	
24C01P-1.8	128 X 8	PDIP	8	1Kb	1.8-6.0	100kHz	C	
24C01PI-1.8	128 X 8	PDIP	8	1Kb	1.8-6.0	100kHz	I	
24C01J	128 X 8	SOIC	8	1Kb	4.5-5.5	400kHz	C	
24C01JI	128 X 8	SOIC	8	1Kb	4.5-5.5	400kHz	I	
24C01J-2.7	128 X 8	SOIC	8	1Kb	2.7-6.0	100kHz	C	
24C01JI-2.7	128 X 8	SOIC	8	1Kb	2.7-6.0	100kHz	I	
24C01J-2.5	128 X 8	SOIC	8	1Kb	2.5-6.0	100kHz	C	
24C01JI-2.5	128 X 8	SOIC	8	1Kb	2.5-6.0	100kHz	I	
24C01J-1.8	128 X 8	SOIC	8	1Kb	1.8-6.0	100kHz	C	
24C01JI-1.8	128 X 8	SOIC	8	1Kb	1.8-6.0	100kHz	I	
24C01J14	128 X 8	SOIC	14	1Kb	4.5-5.5	400kHz	C	
24C01J14I	128 X 8	SOIC	14	1Kb	4.5-5.5	400kHz	I	
24C01J14-2.7	128 X 8	SOIC	14	1Kb	2.7-6.0	100kHz	C	
24C01J14I-2.7	128 X 8	SOIC	14	1Kb	2.7-6.0	100kHz	I	
24C01J14-2.5	128 X 8	SOIC	14	1Kb	2.5-6.0	100kHz	C	
24C01J14I-2.5	128 X 8	SOIC	14	1Kb	2.5-6.0	100kHz	I	
24C01J14-1.8	128 X 8	SOIC	14	1Kb	1.8-6.0	100kHz	C	
24C01J14I-1.8	128 X 8	SOIC	14	1Kb	1.8-6.0	100kHz	I	
24WC01P	128 X 8	PDIP	8	1Kb	4.5-5.5	400kHz	C	Write Protect
24WC01PI	128 X 8	PDIP	8	1Kb	4.5-5.5	400kHz	I	Write Protect
24WC01P-2.7	128 X 8	PDIP	8	1Kb	3.0-6.0	100kHz	C	Write Protect
24WC01PI-2.7	128 X 8	PDIP	8	1Kb	3.0-6.0	100kHz	I	Write Protect
24WC01P-2.5	128 X 8	PDIP	8	1Kb	2.5-6.0	100kHz	C	Write Protect
24WC01PI-2.5	128 X 8	PDIP	8	1Kb	2.5-6.0	100kHz	I	Write Protect
24WC01P-1.8	128 X 8	PDIP	8	1Kb	1.8-6.0	100kHz	C	Write Protect
24WC01PI-1.8	128 X 8	PDIP	8	1Kb	1.8-6.0	100kHz	I	Write Protect
24WC01J	128 X 8	SOIC	8	1Kb	4.5-5.5	400kHz	C	Write Protect
24WC01JI	128 X 8	SOIC	8	1Kb	4.5-5.5	400kHz	I	Write Protect
24WC01J-2.7	128 X 8	SOIC	8	1Kb	2.7-6.0	100kHz	C	Write Protect
24WC01JI-2.7	128 X 8	SOIC	8	1Kb	2.7-6.0	100kHz	I	Write Protect
24WC01J-2.5	128 X 8	SOIC	8	1Kb	2.5-6.0	100kHz	C	Write Protect
24WC01JI-2.5	128 X 8	SOIC	8	1Kb	2.5-6.0	100kHz	I	Write Protect
24WC01J-1.8	128 X 8	SOIC	8	1Kb	1.8-6.0	100kHz	C	Write Protect

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC01JI-1.8	128 X 8	SOIC	8	1Kb	1.8-6.0	100kHz	I	Write Protect
24WC01J14	128 X 8	SOIC	14	1Kb	4.5-5.5	400kHz	C	Write Protect
24WC01J14I	128 X 8	SOIC	14	1Kb	4.5-5.5	400kHz	I	Write Protect
24WC01J14-2.7	128 X 8	SOIC	14	1Kb	2.7-6.0	100kHz	C	Write Protect
24WC01J14I-2.7	128 X 8	SOIC	14	1Kb	2.7-6.0	100kHz	I	Write Protect
24WC01J14-2.5	128 X 8	SOIC	14	1Kb	2.5-6.0	100kHz	C	Write Protect
24WC01J14I-2.5	128 X 8	SOIC	14	1Kb	2.5-6.0	100kHz	I	Write Protect
24WC01J14-1.8	128 X 8	SOIC	14	1Kb	1.8-6.0	100kHz	C	Write Protect
24WC01J14I-1.8	128 X 8	SOIC	14	1Kb	1.8-6.0	100kHz	I	Write Protect
24C02P	256 X 8	PDIP	8	2Kb	4.5-5.5	400kHz	C	
24C02PI	256 X 8	PDIP	8	2Kb	4.5-5.5	400kHz	I	
24C02P-2.7	256 X 8	PDIP	8	2Kb	2.7-6.0	100kHz	C	
24C02PI-2.7	256 X 8	PDIP	8	2Kb	2.7-6.0	100kHz	I	
24C02P-2.5	256 X 8	PDIP	8	2Kb	2.5-6.0	100kHz	C	
24C02PI-2.5	256 X 8	PDIP	8	2Kb	2.5-6.0	100kHz	I	
24C02P-1.8	256 X 8	PDIP	8	2Kb	1.8-6.0	100kHz	C	
24C02PI-1.8	256 X 8	PDIP	8	2Kb	1.8-6.0	100kHz	I	
24C02J	256 X 8	SOIC	8	2Kb	4.5-5.5	400kHz	C	
24C02JI	256 X 8	SOIC	8	2Kb	4.5-5.5	400kHz	I	
24C02J-2.7	256 X 8	SOIC	8	2Kb	2.7-6.0	100kHz	C	
24C02JI-2.7	256 X 8	SOIC	8	2Kb	2.7-6.0	100kHz	I	
24C02J-2.5	256 X 8	SOIC	8	2Kb	2.5-6.0	100kHz	C	
24C02JI-2.5	256 X 8	SOIC	8	2Kb	2.5-6.0	100kHz	I	
24C02J-1.8	256 X 8	SOIC	8	2Kb	1.8-6.0	100kHz	C	
24C02JI-1.8	256 X 8	SOIC	8	2Kb	1.8-6.0	100kHz	I	
24C02J14	256 X 8	SOIC	14	2Kb	4.5-5.5	400kHz	C	
24C02J14I	256 X 8	SOIC	14	2Kb	4.5-5.5	400kHz	I	
24C02J14-2.7	256 X 8	SOIC	14	2Kb	2.7-6.0	100kHz	C	
24C02J14I-2.7	256 X 8	SOIC	14	2Kb	2.7-6.0	100kHz	I	
24C02J14-2.5	256 X 8	SOIC	14	2Kb	2.5-6.0	100kHz	C	
24C02J14I-2.5	256 X 8	SOIC	14	2Kb	2.5-6.0	100kHz	I	
24C02J14-1.8	256 X 8	SOIC	14	2Kb	1.8-6.0	100kHz	C	
24C02J14I-1.8	256 X 8	SOIC	14	2Kb	1.8-6.0	100kHz	I	
24WC02P	256 X 8	PDIP	8	2Kb	4.5-5.5	400kHz	C	Write Protect
24WC02PI	256 X 8	PDIP	8	2Kb	4.5-5.5	400kHz	I	Write Protect
24WC02P-2.7	256 X 8	PDIP	8	2Kb	2.7-6.0	100kHz	C	Write Protect
24WC02PI-2.7	256 X 8	PDIP	8	2Kb	2.7-6.0	100kHz	I	Write Protect
24WC02P-2.5	256 X 8	PDIP	8	2Kb	2.5-6.0	100kHz	C	Write Protect
24WC02PI-2.5	256 X 8	PDIP	8	2Kb	2.5-6.0	100kHz	I	Write Protect
24WC02P-1.8	256 X 8	PDIP	8	2Kb	1.8-6.0	100kHz	C	Write Protect
24WC02PI-1.8	256 X 8	PDIP	8	2Kb	1.8-6.0	100kHz	I	Write Protect
24WC02J	256 X 8	SOIC	8	2Kb	4.5-5.5	400kHz	C	Write Protect
24WC02JI	256 X 8	SOIC	8	2Kb	4.5-5.5	400kHz	I	Write Protect
24WC02J-2.7	256 X 8	SOIC	8	2Kb	2.7-6.0	100kHz	C	Write Protect
24WC02JI-2.7	256 X 8	SOIC	8	2Kb	2.7-6.0	100kHz	I	Write Protect
24WC02J-2.5	256 X 8	SOIC	8	2Kb	2.5-6.0	100kHz	C	Write Protect
24WC02JI-2.5	256 X 8	SOIC	8	2Kb	2.5-6.0	100kHz	I	Write Protect
24WC02J-1.8	256 X 8	SOIC	8	2Kb	1.8-6.0	100kHz	C	Write Protect
24WC02JI-1.8	256 X 8	SOIC	8	2Kb	1.8-6.0	100kHz	I	Write Protect
24WC02J14	256 X 8	SOIC	14	2Kb	4.5-5.5	400kHz	C	Write Protect
24WC02J14I	256 X 8	SOIC	14	2Kb	4.5-5.5	400kHz	I	Write Protect
24WC02J14-2.7	256 X 8	SOIC	14	2Kb	2.7-6.0	100kHz	C	Write Protect
24WC02J14I-2.7	256 X 8	SOIC	14	2Kb	2.7-6.0	100kHz	I	Write Protect

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC02J14-2.5	256 X 8	SOIC	14	2Kb	2.5-6.0	100kHz	C	Write Protect
24WC02J14I-2.5	256 X 8	SOIC	14	2Kb	2.5-6.0	100kHz	I	Write Protect
24WC02J14-1.8	256 X 8	SOIC	14	2Kb	1.8-6.0	100kHz	C	Write Protect
24WC02J14I-1.8	256 X 8	SOIC	14	2Kb	1.8-6.0	100kHz	I	Write Protect
24C04P	512 X 8	PDIP	8	4Kb	4.5-5.5	400kHz	C	
24C04PI	512 X 8	PDIP	8	4Kb	4.5-5.5	400kHz	I	
24C04P-2.7	512 X 8	PDIP	8	4Kb	2.7-6.0	100kHz	C	
24C04PI-2.7	512 X 8	PDIP	8	4Kb	2.7-6.0	100kHz	I	
24C04P-2.5	512 X 8	PDIP	8	4Kb	2.5-6.0	100kHz	C	
24C04PI-2.5	512 X 8	PDIP	8	4Kb	2.5-6.0	100kHz	I	
24C04P-1.8	512 X 8	PDIP	8	4Kb	1.8-6.0	100kHz	C	
24C04PI-1.8	512 X 8	PDIP	8	4Kb	1.8-6.0	100kHz	I	
24C04J	512 X 8	SOIC	8	4Kb	4.5-5.5	400kHz	C	
24C04JI	512 X 8	SOIC	8	4Kb	4.5-5.5	400kHz	I	
24C04J-2.7	512 X 8	SOIC	8	4Kb	2.7-6.0	100kHz	C	
24C04JI-2.7	512 X 8	SOIC	8	4Kb	2.7-6.0	100kHz	I	
24C04J-2.5	512 X 8	SOIC	8	4Kb	2.5-6.0	100kHz	C	
24C04JI-2.5	512 X 8	SOIC	8	4Kb	2.5-6.0	100kHz	I	
24C04J-1.8	512 X 8	SOIC	8	4Kb	1.8-6.0	100kHz	C	
24C04JI-1.8	512 X 8	SOIC	8	4Kb	1.8-6.0	100kHz	I	
24C04J14	512 X 8	SOIC	14	4Kb	4.5-5.5	400kHz	C	
24C04J14I	512 X 8	SOIC	14	4Kb	4.5-5.5	400kHz	I	
24C04J14-2.7	512 X 8	SOIC	14	4Kb	2.7-6.0	100kHz	C	
24C04J14I-2.7	512 X 8	SOIC	14	4Kb	2.7-6.0	100kHz	I	
24C04J14-2.5	512 X 8	SOIC	14	4Kb	2.5-6.0	100kHz	C	
24C04J14I-2.5	512 X 8	SOIC	14	4Kb	2.5-6.0	100kHz	I	
24C04J14-1.8	512 X 8	SOIC	14	4Kb	1.8-6.0	100kHz	C	
24C04J14I-1.8	512 X 8	SOIC	14	4Kb	1.8-6.0	100kHz	I	
24WC04P	512 X 8	PDIP	8	4Kb	4.5-5.5	400kHz	C	Write Protect
24WC04PI	512 X 8	PDIP	8	4Kb	4.5-5.5	400kHz	I	Write Protect
24WC04P-2.7	512 X 8	PDIP	8	4Kb	2.7-6.0	100kHz	C	Write Protect
24WC04PI-2.7	512 X 8	PDIP	8	4Kb	2.7-6.0	100kHz	I	Write Protect
24WC04P-2.5	512 X 8	PDIP	8	4Kb	2.5-6.0	100kHz	C	Write Protect
24WC04PI-2.5	512 X 8	PDIP	8	4Kb	2.5-6.0	100kHz	I	Write Protect
24WC04P-1.8	512 X 8	PDIP	8	4Kb	1.8-6.0	100kHz	C	Write Protect
24WC04PI-1.8	512 X 8	PDIP	8	4Kb	1.8-6.0	100kHz	I	Write Protect
24WC04J	512 X 8	SOIC	8	4Kb	4.5-5.5	400kHz	C	Write Protect
24WC04JI	512 X 8	SOIC	8	4Kb	4.5-5.5	400kHz	I	Write Protect
24WC04J-2.7	512 X 8	SOIC	8	4Kb	2.7-6.0	100kHz	C	Write Protect
24WC04JI-2.7	512 X 8	SOIC	8	4Kb	2.7-6.0	100kHz	I	Write Protect
24WC04J-2.5	512 X 8	SOIC	8	4Kb	2.5-6.0	100kHz	C	Write Protect
24WC04JI-2.5	512 X 8	SOIC	8	4Kb	2.5-6.0	100kHz	I	Write Protect
24WC04J-1.8	512 X 8	SOIC	8	4Kb	1.8-6.0	100kHz	C	Write Protect
24WC04JI-1.8	512 X 8	SOIC	8	4Kb	1.8-6.0	100kHz	I	Write Protect

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC04J14	512 X 8	SOIC	14	4Kb	4.5-5.5	400kHz	C	Write Protect
24WC04J14I	512 X 8	SOIC	14	4Kb	4.5-5.5	400kHz	I	Write Protect
24WC04J14-2.7	512 X 8	SOIC	14	4Kb	2.7-6.0	100kHz	C	Write Protect
24WC04J14I-2.7	512 X 8	SOIC	14	4Kb	2.7-6.0	100kHz	I	Write Protect
24WC04J14-2.5	512 X 8	SOIC	14	4Kb	2.5-6.0	100kHz	C	Write Protect
24WC04J14I-2.5	512 X 8	SOIC	14	4Kb	2.5-6.0	100kHz	I	Write Protect
24WC04J14-1.8	512 X 8	SOIC	14	4Kb	1.8-6.0	100kHz	C	Write Protect
24WC04J14I-1.8	512 X 8	SOIC	14	4Kb	1.8-6.0	100kHz	I	Write Protect
24C08P	1024 X 8	PDIP	8	8Kb	4.5-5.5	400kHz	C	
24C08PI	1024 X 8	PDIP	8	8Kb	4.5-5.5	400kHz	I	
24C08P-2.7	1024 X 8	PDIP	8	8Kb	2.7-6.0	100kHz	C	
24C08PI-2.7	1024 X 8	PDIP	8	8Kb	2.7-6.0	100kHz	I	
24C08P-2.5	1024 X 8	PDIP	8	8Kb	2.5-6.0	100kHz	C	
24C08PI-2.5	1024 X 8	PDIP	8	8Kb	2.5-6.0	100kHz	I	
24C08P-1.8	1024 X 8	PDIP	8	8Kb	1.8-6.0	100kHz	C	
24C08PI-1.8	1024 X 8	PDIP	8	8Kb	1.8-6.0	100kHz	I	
24C08J	1024 X 8	SOIC	8	8Kb	4.5-5.5	400kHz	C	
24C08JI	1024 X 8	SOIC	8	8Kb	4.5-5.5	400kHz	I	
24C08J-2.7	1024 X 8	SOIC	8	8Kb	2.7-6.0	100kHz	C	
24C08JI-2.7	1024 X 8	SOIC	8	8Kb	2.7-6.0	100kHz	I	
24C08J-2.5	1024 X 8	SOIC	8	8Kb	2.5-6.0	100kHz	C	
24C08JI-2.5	1024 X 8	SOIC	8	8Kb	2.5-6.0	100kHz	I	
24C08J-1.8	1024 X 8	SOIC	8	8Kb	1.8-6.0	100kHz	C	
24C08JI-1.8	1024 X 8	SOIC	8	8Kb	1.8-6.0	100kHz	I	
24C08J14	1024 X 8	SOIC	14	8Kb	4.5-5.5	400kHz	C	
24C08J14I	1024 X 8	SOIC	14	8Kb	4.5-5.5	400kHz	I	
24C08J14-2.7	1024 X 8	SOIC	14	8Kb	2.7-6.0	100kHz	C	
24C08J14I-2.7	1024 X 8	SOIC	14	8Kb	2.7-6.0	100kHz	I	
24C08J14-2.5	1024 X 8	SOIC	14	8Kb	2.5-6.0	100kHz	C	
24C08J14I-2.5	1024 X 8	SOIC	14	8Kb	2.5-6.0	100kHz	I	
24C08J14-1.8	1024 X 8	SOIC	14	8Kb	1.8-6.0	100kHz	C	
24C08J14I-1.8	1024 X 8	SOIC	14	8Kb	1.8-6.0	100kHz	I	
24WC08P	1024 X 8	PDIP	8	8Kb	4.5-5.5	400kHz	C	Write Protect
24WC08PI	1024 X 8	PDIP	8	8Kb	4.5-5.5	400kHz	I	Write Protect
24WC08P-2.7	1024 X 8	PDIP	8	8Kb	2.7-6.0	100kHz	C	Write Protect
24WC08PI-2.7	1024 X 8	PDIP	8	8Kb	2.7-6.0	100kHz	I	Write Protect
24WC08P-2.5	1024 X 8	PDIP	8	8Kb	2.5-6.0	100kHz	C	Write Protect
24WC08PI-2.5	1024 X 8	PDIP	8	8Kb	2.5-6.0	100kHz	I	Write Protect
24WC08P-1.8	1024 X 8	PDIP	8	8Kb	1.8-6.0	100kHz	C	Write Protect
24WC08PI-1.8	1024 X 8	PDIP	8	8Kb	1.8-6.0	100kHz	I	Write Protect
24WC08J	1024 X 8	SOIC	8	8Kb	4.5-5.5	400kHz	C	Write Protect
24WC08JI	1024 X 8	SOIC	8	8Kb	4.5-5.5	400kHz	I	Write Protect
24WC08J-2.7	1024 X 8	SOIC	8	8Kb	2.7-6.0	100kHz	C	Write Protect
24WC08JI-2.7	1024 X 8	SOIC	8	8Kb	2.7-6.0	100kHz	I	Write Protect
24WC08J-2.5	1024 X 8	SOIC	8	8Kb	2.5-6.0	100kHz	C	Write Protect
24WC08JI-2.5	1024 X 8	SOIC	8	8Kb	2.5-6.0	100kHz	I	Write Protect
24WC08J-1.8	1024 X 8	SOIC	8	8Kb	1.8-6.0	100kHz	C	Write Protect
24WC08JI-1.8	1024 X 8	SOIC	8	8Kb	1.8-6.0	100kHz	I	Write Protect
24WC08J14	1024 X 8	SOIC	14	8Kb	4.5-5.5	400kHz	C	Write Protect
24WC08J14I	1024 X 8	SOIC	14	8Kb	4.5-5.5	400kHz	I	Write Protect
24WC08J14-2.7	1024 X 8	SOIC	14	8Kb	2.7-6.0	100kHz	C	Write Protect
24WC08J14I-2.7	1024 X 8	SOIC	14	8Kb	2.7-6.0	100kHz	I	Write Protect
24WC08J14-2.5	1024 X 8	SOIC	14	8Kb	2.5-6.0	100kHz	C	Write Protect

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC08J14I-2.5	1024 X 8	SOIC	14	8Kb	2.5-6.0	100kHz	I	Write Protect
24WC08J14-1.8	1024 X 8	SOIC	14	8Kb	1.8-6.0	100kHz	C	Write Protect
24WC08J14I-1.8	1024 X 8	SOIC	14	8Kb	1.8-6.0	100kHz	I	Write Protect
24C16P	2048 X 8	PDIP	8	16Kb	4.5-5.5	400kHz	C	
24C16PI	2048 X 8	PDIP	8	16Kb	4.5-5.5	400kHz	I	
24C16P-2.7	2048 X 8	PDIP	8	16Kb	2.7-6.0	100kHz	C	
24C16PI-2.7	2048 X 8	PDIP	8	16Kb	2.7-6.0	100kHz	I	
24C16P-2.5	2048 X 8	PDIP	8	16Kb	2.5-6.0	100kHz	C	
24C16PI-2.5	2048 X 8	PDIP	8	16Kb	2.5-6.0	100kHz	I	
24C16P-1.8	2048 X 8	PDIP	8	16Kb	1.8-6.0	100kHz	C	
24C16PI-1.8	2048 X 8	PDIP	8	16Kb	1.8-6.0	100kHz	I	
24C16J	2048 X 8	SOIC	8	16Kb	4.5-5.5	400kHz	C	
24C16JI	2048 X 8	SOIC	8	16Kb	4.5-5.5	400kHz	I	
24C16J-2.7	2048 X 8	SOIC	8	16Kb	2.7-6.0	100kHz	C	
24C16JI-2.7	2048 X 8	SOIC	8	16Kb	2.7-6.0	100kHz	I	
24C16J-2.5	2048 X 8	SOIC	8	16Kb	2.5-6.0	100kHz	C	
24C16JI-2.5	2048 X 8	SOIC	8	16Kb	2.5-6.0	100kHz	I	
24C16J-1.8	2048 X 8	SOIC	8	16Kb	1.8-6.0	100kHz	C	
24C16JI-1.8	2048 X 8	SOIC	8	16Kb	1.8-6.0	100kHz	I	
24C16J14	2048 X 8	SOIC	14	16Kb	4.5-5.5	400kHz	C	
24C16J14I	2048 X 8	SOIC	14	16Kb	4.5-5.5	400kHz	I	
24C16J14-2.7	2048 X 8	SOIC	14	16Kb	2.7-6.0	100kHz	C	
24C16J14I-2.7	2048 X 8	SOIC	14	16Kb	2.7-6.0	100kHz	I	
24C16J14-2.5	2048 X 8	SOIC	14	16Kb	2.5-6.0	100kHz	C	
24C16J14I-2.5	2048 X 8	SOIC	14	16Kb	2.5-6.0	100kHz	I	
24C16J14-1.8	2048 X 8	SOIC	14	16Kb	1.8-6.0	100kHz	C	
24C16J14I-1.8	2048 X 8	SOIC	14	16Kb	1.8-6.0	100kHz	I	
24WC16P	2048 X 8	PDIP	8	16Kb	4.5-5.5	400kHz	C	Write Protect
24WC16PI	2048 X 8	PDIP	8	16Kb	4.5-5.5	400kHz	I	Write Protect
24WC16P-2.7	2048 X 8	PDIP	8	16Kb	2.7-6.0	100kHz	C	Write Protect
24WC16PI-2.7	2048 X 8	PDIP	8	16Kb	2.7-6.0	100kHz	I	Write Protect
24WC16P-2.5	2048 X 8	PDIP	8	16Kb	2.5-6.0	100kHz	C	Write Protect
24WC16PI-2.5	2048 X 8	PDIP	8	16Kb	2.5-6.0	100kHz	I	Write Protect
24WC16P-1.8	2048 X 8	PDIP	8	16Kb	1.8-6.0	100kHz	C	Write Protect
24WC16PI-1.8	2048 X 8	PDIP	8	16Kb	1.8-6.0	100kHz	I	Write Protect
24WC16J	2048 X 8	SOIC	8	16Kb	4.5-5.5	400kHz	C	Write Protect
24WC16JI	2048 X 8	SOIC	8	16Kb	4.5-5.5	400kHz	I	Write Protect
24WC16J-2.7	2048 X 8	SOIC	8	16Kb	2.7-6.0	100kHz	C	Write Protect
24WC16JI-2.7	2048 X 8	SOIC	8	16Kb	2.7-6.0	100kHz	I	Write Protect
24WC16J-2.5	2048 X 8	SOIC	8	16Kb	2.5-6.0	100kHz	C	Write Protect
24WC16JI-2.5	2048 X 8	SOIC	8	16Kb	2.5-6.0	100kHz	I	Write Protect
24WC16J-1.8	2048 X 8	SOIC	8	16Kb	1.8-6.0	100kHz	C	Write Protect
24WC16JI-1.8	2048 X 8	SOIC	8	16Kb	1.8-6.0	100kHz	I	Write Protect
24WC16J14	2048 X 8	SOIC	14	16Kb	4.5-5.5	400kHz	C	Write Protect

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC16J14I	2048 X 8	SOIC	14	16Kb	4.5-5.5	400kHz	I	Write Protect
24WC16J14-2.7	2048 X 8	SOIC	14	16Kb	2.7-6.0	100kHz	C	Write Protect
24WC16J14I-2.7	2048 X 8	SOIC	14	16Kb	2.7-6.0	100kHz	I	Write Protect
24WC16J14-2.5	2048 X 8	SOIC	14	16Kb	2.5-6.0	100kHz	C	Write Protect
24WC16J14I-2.5	2048 X 8	SOIC	14	16Kb	2.5-6.0	100kHz	I	Write Protect
24WC16J14-1.8	2048 X 8	SOIC	14	16Kb	1.8-6.0	100kHz	C	Write Protect
24WC16J14I-1.8	2048 X 8	SOIC	14	16Kb	1.8-6.0	100kHz	I	Write Protect
24C32P	4096 X 8	PDIP	8	32Kb	4.5-5.5	400kHz	C	
24C32PI	4096 X 8	PDIP	8	32Kb	4.5-5.5	400kHz	I	
24C32P-2.7	4096 X 8	PDIP	8	32Kb	2.7-6.0	100kHz	C	
24C32PI-2.7	4096 X 8	PDIP	8	32Kb	2.7-6.0	100kHz	I	
24C32P-2.5	4096 X 8	PDIP	8	32Kb	2.5-6.0	100kHz	C	
24C32PI-2.5	4096 X 8	PDIP	8	32Kb	2.5-6.0	100kHz	I	
24C32P-1.8	4096 X 8	PDIP	8	32Kb	1.8-6.0	100kHz	C	
24C32PI-1.8	4096 X 8	PDIP	8	32Kb	1.8-6.0	100kHz	I	
24C32J	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	C	
24C32JI	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	I	
24C32J-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	C	
24C32JI-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	I	
24C32J-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	C	
24C32JI-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	I	
24C32J-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	C	
24C32JI-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	I	
24C32K	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	C	
24C32KI	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	I	
24C32K-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	C	
24C32KI-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	I	
24C32K-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	C	
24C32KI-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	I	
24C32K-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	C	
24C32KI-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	I	
24C32J14	4096 X 8	SOIC	14	32Kb	4.5-5.5	400kHz	C	
24C32J14I	4096 X 8	SOIC	14	32Kb	4.5-5.5	400kHz	I	
24C32J14-2.7	4096 X 8	SOIC	14	32Kb	2.7-6.0	100kHz	C	
24C32J14I-2.7	4096 X 8	SOIC	14	32Kb	2.7-6.0	100kHz	I	
24C32J14-2.5	4096 X 8	SOIC	14	32Kb	2.5-6.0	100kHz	C	
24C32J14I-2.5	4096 X 8	SOIC	14	32Kb	2.5-6.0	100kHz	I	
24C32J14-1.8	4096 X 8	SOIC	14	32Kb	1.8-6.0	100kHz	C	
24C32J14I-1.8	4096 X 8	SOIC	14	32Kb	1.8-6.0	100kHz	I	
24WC32P	4096 X 8	PDIP	8	32Kb	4,5-5.5	400kHz	C	Write Protect
24WC32PI	4096 X 8	PDIP	8	32Kb	4.5-5.5	400kHz	I	Write Protect
24WC32P-2.7	4096 X 8	PDIP	8	32Kb	2.7-6.0	100kHz	C	Write Protect
24WC32PI-2.7	4096 X 8	PDIP	8	32Kb	2.7-6.0	100kHz	I	Write Protect
24WC32P-2.5	4096 X 8	PDIP	8	32Kb	2.5-6.0	100kHz	C	Write Protect
24WC32PI-2.5	4096 X 8	PDIP	8	32Kb	2.5-6.0	100kHz	I	Write Protect
24WC32P-1.8	4096 X 8	PDIP	8	32Kb	1.8-6.0	100kHz	C	Write Protect
24WC32PI-1.8	4096 X 8	PDIP	8	32Kb	1.8-6.0	100kHz	I	Write Protect
24WC32J	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	C	Write Protect
24WC32JI	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	I	Write Protect
24WC32J-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	C	Write Protect
24WC32JI-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	I	Write Protect
24WC32J-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	C	Write Protect
24WC32JI-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	I	Write Protect

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24WC32J-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	C	Write Protect
24WC32JI-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	I	Write Protect
24WC32K	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	C	Write Protect
24WC32KI	4096 X 8	SOIC	8	32Kb	4.5-5.5	400kHz	I	Write Protect
24WC32K-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	C	Write Protect
24WC32KI-2.7	4096 X 8	SOIC	8	32Kb	2.7-6.0	100kHz	I	Write Protect
24WC32K-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	C	Write Protect
24WC32KI-2.5	4096 X 8	SOIC	8	32Kb	2.5-6.0	100kHz	I	Write Protect
24WC32K-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	C	Write Protect
24WC32KI-1.8	4096 X 8	SOIC	8	32Kb	1.8-6.0	100kHz	I	Write Protect
24WC32J14	4096 X 8	SOIC	14	32Kb	4.5-5.5	400kHz	C	Write Protect
24WC32J14I	4096 X 8	SOIC	14	32Kb	4.5-5.5	400kHz	I	Write Protect
24WC32J14-2.7	4096 X 8	SOIC	14	32Kb	2.7-6.0	100kHz	C	Write Protect
24WC32J14I-2.7	4096 X 8	SOIC	14	32Kb	2.7-6.0	100kHz	I	Write Protect
24WC32J14-2.5	4096 X 8	SOIC	14	32Kb	2.5-6.0	100kHz	C	Write Protect
24WC32J14I-2.5	4096 X 8	SOIC	14	32Kb	2.5-6.0	100kHz	I	Write Protect
24WC32J14-1.8	4096 X 8	SOIC	14	32Kb	1.8-6.0	100kHz	C	Write Protect
24WC32J14I-1.8	4096 X 8	SOIC	14	32Kb	1.8-6.0	100kHz	I	Write Protect
24C64P	8192 X 8	PDIP	8	64Kb	4.5-5.5	400kHz	C	
24C64PI	8192 X 8	PDIP	8	64Kb	4.5-5.5	400kHz	I	
24C64P-2.7	8192 X 8	PDIP	8	64Kb	2.7-6.0	100kHz	C	
24C64PI-2.7	8192 X 8	PDIP	8	64Kb	2.7-6.0	100kHz	I	
24C64P-2.5	8192 X 8	PDIP	8	64Kb	2.5-6.0	100kHz	C	
24C64PI-2.5	8192 X 8	PDIP	8	64Kb	2.5-6.0	100kHz	I	
24C64P-1.8	8192 X 8	PDIP	8	64Kb	1.8-6.0	100kHz	C	
24C64PI-1.8	8192 X 8	PDIP	8	64Kb	1.8-6.0	100kHz	I	
24C64J	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	C	
24C64JI	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	I	
24C64J-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	C	
24C64JI-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	I	
24C64J-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	C	
24C64JI-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	I	
24C64J-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	C	
24C64JI-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	I	
24C64K	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	C	
24C64KI	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	I	
24C64K-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	C	
24C64KI-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	I	
24C64K-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	C	
24C64KI-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	I	
24C64K-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	C	
24C64KI-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	I	
24C64J14	8192 X 8	SOIC	14	64Kb	4.5-5.5	400kHz	C	
24C64J14I	8192 X 8	SOIC	14	64Kb	4.5-5.5	400kHz	I	

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs (cont.)

I²C Bus (Data Book Section 2)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
24C64J14-2.7	8192 X 8	SOIC	14	64Kb	2.7-6.0	100kHz	C	
24C64J14I-2.7	8192 X 8	SOIC	14	64Kb	2.7-6.0	100kHz	I	
24C64J14-2.5	8192 X 8	SOIC	14	64Kb	2.5-6.0	100kHz	C	
24C64J14I-2.5	8192 X 8	SOIC	14	64Kb	2.5-6.0	100kHz	I	
24C64J14-1.8	8192 X 8	SOIC	14	64Kb	1.8-6.0	100kHz	C	
24C64J14I-1.8	8192 X 8	SOIC	14	64Kb	1.8-6.0	100kHz	I	
24WC64P	8192 X 8	PDIP	8	64Kb	4.5-5.5	400kHz	C	Write Protect
24WC64PI	8192 X 8	PDIP	8	64Kb	4.5-5.5	400kHz	I	Write Protect
24WC64P-2.7	8192 X 8	PDIP	8	64Kb	2.7-6.0	100kHz	C	Write Protect
24WC64PI-2.7	8192 X 8	PDIP	8	64Kb	2.7-6.0	100kHz	I	Write Protect
24WC64P-2.5	8192 X 8	PDIP	8	64Kb	2.5-6.0	100kHz	C	Write Protect
24WC64PI-2.5	8192 X 8	PDIP	8	64Kb	2.5-6.0	100kHz	I	Write Protect
24WC64P-1.8	8192 X 8	PDIP	8	64Kb	1.8-6.0	100kHz	C	Write Protect
24WC64PI-1.8	8192 X 8	PDIP	8	64Kb	1.8-6.0	100kHz	I	Write Protect
24WC64J	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	C	Write Protect
24WC64JI	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	I	Write Protect
24WC64J-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	C	Write Protect
24WC64JI-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	I	Write Protect
24WC64J-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	C	Write Protect
24WC64JI-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	I	Write Protect
24WC64J-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	C	Write Protect
24WC64JI-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	I	Write Protect
24WC64K	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	C	Write Protect
24WC64KI	8192 X 8	SOIC	8	64Kb	4.5-5.5	400kHz	I	Write Protect
24WC64K-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	C	Write Protect
24WC64KI-2.7	8192 X 8	SOIC	8	64Kb	2.7-6.0	100kHz	I	Write Protect
24WC64K-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	C	Write Protect
24WC64KI-2.5	8192 X 8	SOIC	8	64Kb	2.5-6.0	100kHz	I	Write Protect
24WC64K-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	C	Write Protect
24WC64KI-1.8	8192 X 8	SOIC	8	64Kb	1.8-6.0	100kHz	I	Write Protect
24WC64J14	8192 X 8	SOIC	14	64Kb	4.5-5.5	400kHz	C	Write Protect
24WC64J14I	8192 X 8	SOIC	14	64Kb	4.5-5.5	400kHz	I	Write Protect
24WC64J14-2.7	8192 X 8	SOIC	14	64Kb	2.7-6.0	100kHz	C	Write Protect
24WC64J14I-2.7	8192 X 8	SOIC	14	64Kb	2.7-6.0	100kHz	I	Write Protect
24WC64J14-2.5	8192 X 8	SOIC	14	64Kb	2.5-6.0	100kHz	C	Write Protect
24WC64J14I-2.5	8192 X 8	SOIC	14	64Kb	2.5-6.0	100kHz	I	Write Protect
24WC64J14-1.8	8192 X 8	SOIC	14	64Kb	1.8-6.0	100kHz	C	Write Protect
24WC64J14I-1.8	8192 X 8	SOIC	14	64Kb	1.8-6.0	100kHz	I	Write Protect

Serial E²PROMs

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C46P	64X16 / 128X 8	PDIP	8	1Kb	4.5-5.5	1MHZ	C	
93C46PI	64X16 / 128X 8	PDIP	8	1Kb	4.5-5.5	1MHZ	I	
93C46J	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	C	
93C46JI	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	I	
93C46K	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	C	
93C46KI	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	I	
93C46S	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	C	
93C46SI	64X16 / 128X 8	SOIC	8	1Kb	4.5-5.5	1MHZ	I	
93C46AP	64X16	PDIP	8	1Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C46API	64X16	PDIP	8	1Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C46AJ	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C46AJI	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C46AK	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C46AKI	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C46AS	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C46ASI	64X16	SOIC	8	1Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C46P-2.7	64X16 / 128X 8	PDIP	8	1Kb	2.7-6.0	1MHZ	C	
93C46PI-2.7	64X16 / 128X 8	PDIP	8	1Kb	2.7-6.0	1MHZ	I	
93C46J-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	C	
93C46JI-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	I	
93C46K-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	C	
93C46KI-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	I	
93C46S-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	C	
93C46SI-2.7	64X16 / 128X 8	SOIC	8	1Kb	2.7-6.0	1MHZ	I	
93C46AP-2.7	64X16	PDIP	8	1Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C46API-2.7	64X16	PDIP	8	1Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C46AJ-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C46AJI-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C46AK-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C46AKI-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C46AS-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C46ASI-2.7	64X16	SOIC	8	1Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C46P-2.5	64X16 / 128X 8	PDIP	8	1Kb	2.5-6.0	1MHZ	C	
93C46PI-2.5	64X16 / 128X 8	PDIP	8	1Kb	2.5-6.0	1MHZ	I	
93C46J-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	C	
93C46JI-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	I	
93C46K-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	C	
93C46KI-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	I	
93C46S-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	C	
93C46SI-2.5	64X16 / 128X 8	SOIC	8	1Kb	2.5-6.0	1MHZ	I	
93C46AP-2.5	64X16	PDIP	8	1Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C46API-2.5	64X16	PDIP	8	1Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C46AJ-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C46AJI-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C46AK-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	C	No ORG Pin

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

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Serial E²PROMs (cont.)

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C46AKI-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C46AS-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C46ASI-2.5	64X16	SOIC	8	1Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C46P-1.8	64X16 / 128X 8	PDIP	8	1Kb	1.8-6.0	1MHZ	C	
93C46PI-1.8	64X16 / 128X 8	PDIP	8	1Kb	1.8-6.0	1MHZ	I	
93C46J-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	C	
93C46JI-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	I	
93C46K-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	C	
93C46KI-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	I	
93C46S-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	C	
93C46SI-1.8	64X16 / 128X 8	SOIC	8	1Kb	1.8-6.0	1MHZ	I	
93C46AP-1.8	64X16	PDIP	8	1Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C46API-1.8	64X16	PDIP	8	1Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C46AJ-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C46AJI-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C46AK-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C46AKI-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C46AS-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C46ASI-1.8	64X16	SOIC	8	1Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C56P	128X16 / 256X 8	PDIP	8	2Kb	4.5-5.5	1MHZ	C	
93C56PI	128X16 / 256X 8	PDIP	8	2Kb	4.5-5.5	1MHZ	I	
93C56J	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C56JI	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C56K	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C56KI	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C56S	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C56SI	128X16 / 256X 8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C56AP	128X16	PDIP	8	2Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C56API	128X16	PDIP	8	2Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C56AJ	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C56AJI	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C56AK	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C56AKI	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C56AS	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C56ASI	128X16	SOIC	8	2Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C56P-2.7	128X16 / 256X 8	PDIP	8	2Kb	2.7-6.0	1MHZ	C	
93C56PI-2.7	128X16 / 256X 8	PDIP	8	2Kb	2.7-6.0	1MHZ	I	
93C56J-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C56JI-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
93C56K-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C56KI-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
93C56S-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C56SI-2.7	128X16 / 256X 8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
93C56AP-2.7	128X16	PDIP	8	2Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C56API-2.7	128X16	PDIP	8	2Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C56AJ-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C56AJI-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C56AK-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C56AKI-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C56AS-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C56ASI-2.7	128X16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C56P-2.5	128X16 / 256X 8	PDIP	8	2Kb	2.5-6.0	1MHZ	C	
93C56PI-2.5	128X16 / 256X 8	PDIP	8	2Kb	2.5-6.0	1MHZ	I	
93C56J-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	

Serial E²PROMs (cont.)

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C56JI-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C56K-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
93C56KI-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C56S-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
93C56SI-2.5	128X16 / 256X 8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C56AP-2.5	128X16	PDIP	8	2Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C56API-2.5	128X16	PDIP	8	2Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C56AJ-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C56AJI-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C56AK-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C56AKI-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C56AS-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C56ASI-2.5	128X16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C56P-1.8	128X16 / 256X 8	PDIP	8	2Kb	1.8-6.0	1MHZ	C	
93C56PI-1.8	128X16 / 256X 8	PDIP	8	2Kb	1.8-6.0	1MHZ	I	
93C56J-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C56JI-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C56K-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C56KI-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C56S-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C56SI-1.8	128X16 / 256X 8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C56AP-1.8	128X16	PDIP	8	2Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C56API-1.8	128X16	PDIP	8	2Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C56AJ-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C56AJI-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C56AK-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C56AKI-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C56AS-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C56ASI-1.8	128X16	SOIC	8	2Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C57P	128X16 / 256X8	PDIP	8	2Kb	4.5-5.5	1MHZ	C	
93C57PI	128X16 / 256X8	PDIP	8	2Kb	4.5-5.5	1MHZ	I	
93C57J	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C57JI	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C57K	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C57KI	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C57S	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	C	
93C57SI	128X16 / 256X8	SOIC	8	2Kb	4.5-5.5	1MHZ	I	
93C57P-2.7	128X16 / 256X8	PDIP	8	2Kb	2.7-6.0	1MHZ	C	
93C57PI-2.7	128X16 / 256X8	PDIP	8	2Kb	2.7-6.0	1MHZ	I	
93C57J-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C57JI-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
93C57K-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C57KI-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
93C57S-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
93C57SI-2.7	128X16 / 256X8	SOIC	8	2Kb	2.7-6.0	1MHZ	I	

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

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Serial E²PROMs (cont.)

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C57P-2.5	128X16 / 256X8	PDIP	8	2Kb	2.5-6.0	1MHZ	C	
93C57PI-2.5	128X16 / 256X8	PDIP	8	2Kb	2.5-6.0	1MHZ	I	
93C57J-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
93C57JI-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C57K-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
93C57KI-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C57S-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
93C57SI-2.5	128X16 / 256X8	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
93C57P-1.8	128X16 / 256X8	PDIP	8	2Kb	1.8-6.0	1MHZ	C	
93C57PI-1.8	128X16 / 256X8	PDIP	8	2Kb	1.8-6.0	1MHZ	I	
93C57J-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C57JI-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C57K-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C57KI-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C57S-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	C	
93C57SI-1.8	128X16 / 256X8	SOIC	8	2Kb	1.8-6.0	1MHZ	I	
93C66P	256X16 / 512X 8	PDIP	8	4Kb	4.5-5.5	1MHZ	C	
93C66PI	256X16 / 512X 8	PDIP	8	4Kb	4.5-5.5	1MHZ	I	
93C66J	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	C	
93C66JI	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	I	
93C66K	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	C	
93C66KI	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	I	
93C66S	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	C	
93C66SI	256X16 / 512X 8	SOIC	8	4Kb	4.5-5.5	1MHZ	I	
93C66AP	256X16	PDIP	8	4Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C66API	256X16	PDIP	8	4Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C66AJ	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C66AJI	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C66AK	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C66AKI	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C66AS	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C66ASI	256X16	SOIC	8	4Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C66P-2.7	256X16 / 512X 8	PDIP	8	4Kb	2.7-6.0	1MHZ	C	
93C66PI-2.7	256X16 / 512X 8	PDIP	8	4Kb	2.7-6.0	1MHZ	I	
93C66J-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	C	
93C66JI-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	I	
93C66K-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	C	
93C66KI-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	I	
93C66S-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	C	
93C66SI-2.7	256X16 / 512X 8	SOIC	8	4Kb	2.7-6.0	1MHZ	I	
93C66AP-2.7	256X16	PDIP	8	4Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C66API-2.7	256X16	PDIP	8	4Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C66AJ-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C66AJI-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C66AK-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C66AKI-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C66AS-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C66ASI-2.7	256X16	SOIC	8	4Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C66P-2.5	256X16 / 512X 8	PDIP	8	4Kb	2.5-6.0	1MHZ	C	
93C66PI-2.5	256X16 / 512X 8	PDIP	8	4Kb	2.5-6.0	1MHZ	I	
93C66J-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	C	
93C66JI-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	I	
93C66K-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	C	
93C66KI-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	I	

Serial E²PROMs (cont.)

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C66S-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	C	
93C66SI-2.5	256X16 / 512X 8	SOIC	8	4Kb	2.5-6.0	1MHZ	I	
93C66AP-2.5	256X16	PDIP	8	4Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C66API-2.5	256X16	PDIP	8	4Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C66AJ-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C66AJI-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C66AK-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C66AKI-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C66AS-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C66ASI-2.5	256X16	SOIC	8	4Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C66P-1.8	256X16 / 512X 8	PDIP	8	4Kb	1.8-6.0	1MHZ	C	
93C66PI-1.8	256X16 / 512X 8	PDIP	8	4Kb	1.8-6.0	1MHZ	I	
93C66J-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	C	
93C66JI-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	I	
93C66K-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	C	
93C66KI-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	I	
93C66S-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	C	
93C66SI-1.8	256X16 / 512X 8	SOIC	8	4Kb	1.8-6.0	1MHZ	I	
93C66AP-1.8	256X16	PDIP	8	4Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C66API-1.8	256X16	PDIP	8	4Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C66AJ-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C66AJI-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C66AK-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C66AKI-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C66AS-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C66ASI-1.8	256X16	SOIC	8	4Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C86P	1024X16 / 2048X 8	PDIP	8	16Kb	4.5-5.5	1MHZ	C	
93C86PI	1024X16 / 2048X 8	PDIP	8	16Kb	4.5-5.5	1MHZ	I	
93C86J	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	C	
93C86JI	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	I	
93C86K	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	C	
93C86KI	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	I	
93C86S	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	C	
93C86SI	1024X16 / 2048X 8	SOIC	8	16Kb	4.5-5.5	1MHZ	I	
93C86AP	1024X16	PDIP	8	16Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C86API	1024X16	PDIP	8	16Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C86AJ	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C86AJI	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C86AK	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C86AKI	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C86AS	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	C	No ORG Pin
93C86ASI	1024X16	SOIC	8	16Kb	4.5-5.5	1MHZ	I	No ORG Pin
93C86P-2.7	1024X16 / 2048X 8	PDIP	8	16Kb	2.7-6.0	1MHZ	C	
93C86PI-2.7	1024X16 / 2048X 8	PDIP	8	16Kb	2.7-6.0	1MHZ	I	
93C86J-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	C	

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs (cont.)

Microwire Bus (Data Book Section 3)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
93C86JI-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	I	
93C86K-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	C	
93C86KI-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	I	
93C86S-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	C	
93C86SI-2.7	1024X16 / 2048X 8	SOIC	8	16Kb	2.7-6.0	1MHZ	I	
93C86AP-2.7	1024X16	PDIP	8	16Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C86API-2.7	1024X16	PDIP	8	16Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C86AJ-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C86AJI-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C86AK-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C86AKI-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C86AS-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	C	No ORG Pin
93C86ASI-2.7	1024X16	SOIC	8	16Kb	2.7-6.0	1MHZ	I	No ORG Pin
93C86P-2.5	1024X16 / 2048X 8	PDIP	8	16Kb	2.5-6.0	1MHZ	C	
93C86PI-2.5	1024X16 / 2048X 8	PDIP	8	16Kb	2.5-6.0	1MHZ	I	
93C86J-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	C	
93C86JI-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	I	
93C86K-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	C	
93C86KI-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	I	
93C86S-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	C	
93C86SI-2.5	1024X16 / 2048X 8	SOIC	8	16Kb	2.5-6.0	1MHZ	I	
93C86AP-2.5	1024X16	PDIP	8	16Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C86API-2.5	1024X16	PDIP	8	16Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C86AJ-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C86AJI-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C86AK-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C86AKI-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C86AS-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	C	No ORG Pin
93C86ASI-2.5	1024X16	SOIC	8	16Kb	2.5-6.0	1MHZ	I	No ORG Pin
93C86P-1.8	1024X16 / 2048X 8	PDIP	8	16Kb	1.8-6.0	1MHZ	C	
93C86PI-1.8	1024X16 / 2048X 8	PDIP	8	16Kb	1.8-6.0	1MHZ	I	
93C86J-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	C	
93C86JI-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	I	
93C86K-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	C	
93C86KI-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	I	
93C86S-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	C	
93C86SI-1.8	1024X16 / 2048X 8	SOIC	8	16Kb	1.8-6.0	1MHZ	I	
93C86AP-1.8	1024X16	PDIP	8	16Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C86API-1.8	1024X16	PDIP	8	16Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C86AJ-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C86AJI-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C86AK-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C86AKI-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	I	No ORG Pin
93C86AS-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	C	No ORG Pin
93C86ASI-1.8	1024X16	SOIC	8	16Kb	1.8-6.0	1MHZ	I	No ORG Pin

Serial E²PROMs

SPI Bus (Data Book Section 4)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
64LC10P	64 X 16	PDIP	8	1Kb	2.7-6.0	1MHZ	C	
64LC10PI	64 X 16	PDIP	8	1Kb	2.7-6.0	1MHZ	I	
64LC10P-2.5	64 X 16	PDIP	8	1Kb	2.5-6.0	1MHZ	C	
64LC10PI-2.5	64 X 16	PDIP	8	1Kb	2.5-6.0	1MHZ	I	
64LC10J	64 X 16	SOIC	8	1Kb	2.7-6.0	1MHZ	C	
64LC10JI	64 X 16	SOIC	8	1Kb	2.7-6.0	1MHZ	I	
64LC10J-2.5	64 X 16	SOIC	8	1Kb	2.5-6.0	1MHZ	C	
64LC10JI-2.5	64 X 16	SOIC	8	1Kb	2.5-6.0	1MHZ	I	
64LC10S	64 X 16	SOIC	8	1Kb	2.7-6.0	1MHZ	C	
64LC10SI	64 X 16	SOIC	8	1Kb	2.7-6.0	1MHZ	I	
64LC10S-2.5	64 X 16	SOIC	8	1Kb	2.5-6.0	1MHZ	C	
64LC10SI-2.5	64 X 16	SOIC	8	1Kb	2.5-6.0	1MHZ	I	
64LC20P	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
64LC20PI	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
64LC20P-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
64LC20PI-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
64LC20J	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
64LC20JI	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
64LC20J-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
64LC20JI-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
64LC20S	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	C	
64LC20SI	128 X 16	SOIC	8	2Kb	2.7-6.0	1MHZ	I	
64LC20S-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	C	
64LC20SI-2.5	128 X 16	SOIC	8	2Kb	2.5-6.0	1MHZ	I	
64LC40P	256 X 16	PDIP	8	4Kb	2.7-6.0	1MHZ	C	
64LC40PI	256 X 16	PDIP	8	4Kb	2.7-6.0	1MHZ	I	
64LC40P-2.5	256 X 16	PDIP	8	4Kb	2.5-6.0	1MHZ	C	
64LC40PI-2.5	256 X 16	PDIP	8	4Kb	2.5-6.0	1MHZ	I	
64LC40J	256 X 16	SOIC	8	4Kb	2.7-6.0	1MHZ	C	
64LC40JI	256 X 16	SOIC	8	4Kb	2.7-6.0	1MHZ	I	
64LC40J-2.5	256 X 16	SOIC	8	4Kb	2.5-6.0	1MHZ	C	
64LC40JI-2.5	256 X 16	SOIC	8	4Kb	2.5-6.0	1MHZ	I	
64LC40S	256 X 16	SOIC	8	4Kb	2.7-6.0	1MHZ	C	
64LC40SI	256 X 16	SOIC	8	4Kb	2.7-6.0	1MHZ	I	
64LC40S-2.5	256 X 16	SOIC	8	4Kb	2.5-6.0	1MHZ	C	
64LC40SI-2.5	256 X 16	SOIC	8	4Kb	2.5-6.0	1MHZ	I	

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Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Serial E²PROMs

Secure Access (Data Book Section 5)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Clock Freq.	Temp. Range	Special Features
35C704P	256 X 16/512 X 8	PDIP	8	4Kb	4.5-5.5	3MHz	C	
35C704PI	256 X 16/512 X 8	PDIP	8	4Kb	4.5-5.5	3MHz	I	
35C704J	256 X 16/512 X 8	SOIC	16	4Kb	4.5-5.5	3MHz	C	
35C704JI	256 X 16/512 X 8	SOIC	16	4Kb	4.5-5.5	3MHz	I	
33C704P	256 X 16/512 X 8	PDIP	8	4Kb	2.7-3.3	1MHz	C	
33C704PI	256 X 16/512 X 8	PDIP	8	4Kb	2.7-3.3	1MHz	I	
33C704J	256 X 16/512 X 8	SOIC	16	4Kb	2.7-3.3	1MHz	C	
33C704JI	256 X 16/512 X 8	SOIC	16	4Kb	2.7-3.3	1MHz	I	
35C804AP	256 X 16/512 X 8	PDIP	8	4Kb	4.5-5.5	4.9MHz	C	
35C804API	256 X 16/512 X 8	PDIP	8	4Kb	4.5-5.5	4.9MHz	I	
35C804AJ	256 X 16/512 X 8	SOIC	16	4Kb	4.5-5.5	4.9MHz	C	
35C804AJI	256 X 16/512 X 8	SOIC	16	4Kb	4.5-5.5	4.9MHz	I	
33C804AP	256 X 16/512 X 8	PDIP	8	4Kb	2.7-3.3	4.9MHz	C	
33C804API	256 X 16/512 X 8	PDIP	8	4Kb	2.7-3.3	4.9MHz	I	
33C804AJ	256 X 16/512 X 8	SOIC	16	4Kb	2.7-3.3	4.9MHz	C	
33C804AJI	256 X 16/512 X 8	SOIC	16	4Kb	2.7-3.3	4.9MHz	I	

NVRAMs

(Data Book Section 6)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
22C10P-20	64 X 4	PDIP	18	256b	4.5-5.5	200		C	
22C10PI-20	64 X 4	PDIP	18	256b	4.5-5.5	200		I	
22C10J-20	64 X 4	SOIC	16	256b	4.5-5.5	200		C	
22C10JI-20	64 X 4	SOIC	16	256b	4.5-5.5	200		I	
22C10P-30	64 X 4	PDIP	18	256b	4.5-5.5	300		C	
22C10PI-30	64 X 4	PDIP	18	256b	4.5-5.5	300		I	
22C10J-30	64 X 4	SOIC	16	256b	4.5-5.5	300		C	
22C10JI-30	64 X 4	SOIC	16	256b	4.5-5.5	300		I	
24C44P	16 X 16	PDIP	8	256b	4.5-5.5	1MHz		C	
24C44PI	16 X 16	PDIP	8	256b	4.5-5.5	1MHz		I	
24C44S	16 X 16	SOIC	8	256b	4.5-5.5	1MHz		C	
24C44SI	16 X 16	SOIC	8	256b	4.5-5.5	1MHz		I	

Flash Memories

(Data Book Section 7)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28F512P-90	64K X 8	PDIP	32	512Kb		90		C	
28F512PI-90	64K X 8	PDIP	32	512Kb		90		I	
28F512P-12	64K X 8	PDIP	32	512Kb		120		C	
28F512PI-12	64K X 8	PDIP	32	512Kb		120		I	
28F512P-15	64K X 8	PDIP	32	512Kb		150		C	
28F512PI-15	64K X 8	PDIP	32	512Kb		150		I	
28F512N-90	64K X 8	PLCC	32	512Kb		90		C	
28F512NI-90	64K X 8	PLCC	32	512Kb		90		I	
28F512N-12	64K X 8	PLCC	32	512Kb		120		C	
28F512NI-12	64K X 8	PLCC	32	512Kb		120		I	
28F512N-15	64K X 8	PLCC	32	512Kb		150		C	
28F512NI-15	64K X 8	PLCC	32	512Kb		150		I	
28F512T-90	64K X 8	TSOP	32	512Kb		90		C	
28F512TI-90	64K X 8	TSOP	32	512Kb		90		I	
28F512T-12	64K X 8	TSOP	32	512Kb		120		C	
28F512TI-12	64K X 8	TSOP	32	512Kb		120		I	
28F512T-15	64K X 8	TSOP	32	512Kb		150		C	
28F512TI-15	64K X 8	TSOP	32	512Kb		150		I	
28F512T14-90	64K X 8	TSOP	32	512Kb		90		C	
28F512T14I-90	64K X 8	TSOP	32	512Kb		90		I	
28F512T14-12	64K X 8	TSOP	32	512Kb		120		C	
28F512T14I-12	64K X 8	TSOP	32	512Kb		120		I	
28F512T14-15	64K X 8	TSOP	32	512Kb		150		C	
28F512T14I-15	64K X 8	TSOP	32	512Kb		150		I	
28F512TR-90	64K X 8	TSOP	32	512Kb		90		C	Reverse Pin-out
28F512TRI-90	64K X 8	TSOP	32	512Kb		90		I	Reverse Pin-out
28F512TR-12	64K X 8	TSOP	32	512Kb		120		C	Reverse Pin-out
28F512TRI-12	64K X 8	TSOP	32	512Kb		120		I	Reverse Pin-out
28F512TR-15	64K X 8	TSOP	32	512Kb		150		C	Reverse Pin-out
28F512TRI-15	64K X 8	TSOP	32	512Kb		150		I	Reverse Pin-out
28F010P-90	128K X 8	PDIP	32	1Mb		90		C	
28F010PI-90	128K X 8	PDIP	32	1Mb		90		I	
28F010P-12	128K X 8	PDIP	32	1Mb		120		C	
28F010PI-12	128K X 8	PDIP	32	1Mb		120		I	
28F010P-15	128K X 8	PDIP	32	1Mb		150		C	
28F010PI-15	128K X 8	PDIP	32	1Mb		150		I	
28F010N-90	128K X 8	PLCC	32	1Mb		90		C	
28F010NI-90	128K X 8	PLCC	32	1Mb		90		I	
28F010N-12	128K X 8	PLCC	32	1Mb		120		C	
28F010NI-12	128K X 8	PLCC	32	1Mb		120		I	
28F010N-15	128K X 8	PLCC	32	1Mb		150		C	
28F010NI-15	128K X 8	PLCC	32	1Mb		150		I	
28F010T-90	128K X 8	TSOP	32	1Mb		90		C	
28F010TI-90	128K X 8	TSOP	32	1Mb		90		I	
28F010T-12	128K X 8	TSOP	32	1Mb		120		C	
28F010TI-12	128K X 8	TSOP	32	1Mb		120		I	
28F010T-15	128K X 8	TSOP	32	1Mb		150		C	

Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Flash Memories (cont.)

(Data Book Section 7)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28F010TI-15	128K X 8	TSOP	32	1Mb		150		I	
28F010T14-90	128K X 8	TSOP	32	1Mb		90		C	
28F010T14I-90	128K X 8	TSOP	32	1Mb		90		I	
28F010T14-12	128K X 8	TSOP	32	1Mb		120		C	
28F010T14I-12	128K X 8	TSOP	32	1Mb		120		I	
28F010T14-15	128K X 8	TSOP	32	1Mb		150		C	
28F010T14I-15	128K X 8	TSOP	32	1Mb		150		I	
28F010TR-90	128K X 8	TSOP	32	1Mb		90		C	Reverse Pin-out
28F010TRI-90	128K X 8	TSOP	32	1Mb		90		I	Reverse Pin-out
28F010TR-12	128K X 8	TSOP	32	1Mb		120		C	Reverse Pin-out
28F010TRI-12	128K X 8	TSOP	32	1Mb		120		I	Reverse Pin-out
28F010TR-15	128K X 8	TSOP	32	1Mb		150		C	Reverse Pin-out
28F010TRI-15	128K X 8	TSOP	32	1Mb		150		I	Reverse Pin-out
28F020P-12	256K X 8	PDIP	32	2Mb		120		C	
28F020PI-12	256K X 8	PDIP	32	2Mb		120		I	
28F020P-15	256K X 8	PDIP	32	2Mb		150		C	
28F020PI-15	256K X 8	PDIP	32	2Mb		150		I	
28F020P-20	256K X 8	PDIP	32	2Mb		200		C	
28F020PI-20	256K X 8	PDIP	32	2Mb		200		I	
28F020N-12	256K X 8	PLCC	32	2Mb		120		C	
28F020NI-12	256K X 8	PLCC	32	2Mb		120		I	
28F020N-15	256K X 8	PLCC	32	2Mb		150		C	
28F020NI-15	256K X 8	PLCC	32	2Mb		150		I	
28F020N-20	256K X 8	PLCC	32	2Mb		200		C	
28F020NI-20	256K X 8	PLCC	32	2Mb		200		I	
28F020T-12	256K X 8	TSOP	32	2Mb		120		C	
28F020TI-12	256K X 8	TSOP	32	2Mb		120		I	
28F020T-15	256K X 8	TSOP	32	2Mb		150		C	
28F020TI-15	256K X 8	TSOP	32	2Mb		150		I	
28F020T-20	256K X 8	TSOP	32	2Mb		200		C	
28F020TI-20	256K X 8	TSOP	32	2Mb		200		I	
28F020TR-12	256K X 8	TSOP	32	2Mb		120		C	Reverse Pin-out
28F020TRI-12	256K X 8	TSOP	32	2Mb		120		I	Reverse Pin-out
28F020TR-15	256K X 8	TSOP	32	2Mb		150		C	Reverse Pin-out
28F020TRI-15	256K X 8	TSOP	32	2Mb		150		I	Reverse Pin-out
28F020TR-20	256K X 8	TSOP	32	2Mb		200		C	Reverse Pin-out
28F020TRI-20	256K X 8	TSOP	32	2Mb		200		I	Reverse Pin-out
28F102P-90	64K X 16	PDIP	40	1Mb		90		C	
28F102PI-90	64K X 16	PDIP	40	1Mb		90		I	
28F102P-12	64K X 16	PDIP	40	1Mb		120		C	
28F102PI-12	64K X 16	PDIP	40	1Mb		120		I	
28F102P-15	64K X 16	PDIP	40	1Mb		150		C	
28F102PI-15	64K X 16	PDIP	40	1Mb		150		I	
28F102N-90	64K X 16	PLCC	44	1Mb		90		C	
28F102NI-90	64K X 16	PLCC	44	1Mb		90		I	
28F102N-12	64K X 16	PLCC	44	1Mb		120		C	
28F102NI-12	64K X 16	PLCC	44	1Mb		120		I	
28F102N-15	64K X 16	PLCC	44	1Mb		150		C	
28F102NI-15	64K X 16	PLCC	44	1Mb		150		I	
28F102T-90	64K X 16	TSOP	40	1Mb		90		C	
28F102TI-90	64K X 16	TSOP	40	1Mb		90		I	
28F102T-12	64K X 16	TSOP	40	1Mb		120		C	

Flash Memories (cont.)

(Data Book Section 7)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28F102TI-12	64K X 16	TSOP	40	1Mb		120		I	
28F102T-15	64K X 16	TSOP	40	1Mb		150		C	
28F102TI-15	64K X 16	TSOP	40	1Mb		150		I	
28F102TR-90	64K X 16	TSOP	40	1Mb		90			Reverse Pin-out
28F102TRI-90	64K X 16	TSOP	40	1Mb		90			Reverse Pin-out
28F102TR-12	64K X 16	TSOP	40	1Mb		120			Reverse Pin-out
28F102TRI-12	64K X 16	TSOP	40	1Mb		120			Reverse Pin-out
28F102TR-15	64K X 16	TSOP	40	1Mb		150			Reverse Pin-out
28F102TRI-15	64K X 16	TSOP	40	1Mb		150			Reverse Pin-out
28F202P-12	128K X 16	PDIP	40	2Mb		120		C	
28F202PI-12	128K X 16	PDIP	40	2Mb		120		I	
28F202P-15	128K X 16	PDIP	40	2Mb		150		C	
28F202PI-15	128K X 16	PDIP	40	2Mb		150		I	
28F202P-20	128K X 16	PDIP	40	2Mb		200		C	
28F202PI-20	128K X 16	PDIP	40	2Mb		200		I	
28F202N-12	128K X 16	PLCC	44	2Mb		120		C	
28F202NI-12	128K X 16	PLCC	44	2Mb		120		I	
28F202N-15	128K X 16	PLCC	44	2Mb		150		C	
28F202NI-15	128K X 16	PLCC	44	2Mb		150		I	
28F202N-20	128K X 16	PLCC	44	2Mb		200		C	
28F202NI-20	128K X 16	PLCC	44	2Mb		200		I	
28F202T-12	128K X 16	TSOP	40	2Mb		120		C	
28F202TI-12	128K X 16	TSOP	40	2Mb		120		I	
28F202T-15	128K X 16	TSOP	40	2Mb		150		C	
28F202TI-15	128K X 16	TSOP	40	2Mb		150		I	
28F202T-20	128K X 16	TSOP	40	2Mb		200		C	
28F202TI-20	128K X 16	TSOP	40	2Mb		200		I	
28F202TR-12	128K X 16	TSOP	40	2Mb		120			Reverse Pin-out
28F202TRI-12	128K X 16	TSOP	40	2Mb		120			Reverse Pin-out
28F202TR-15	128K X 16	TSOP	40	2Mb		150			Reverse Pin-out
28F202TRI-15	128K X 16	TSOP	40	2Mb		150			Reverse Pin-out
28F202TR-20	128K X 16	TSOP	40	2Mb		200			Reverse Pin-out
28F202TRI-20	128K X 16	TSOP	40	2Mb		200			Reverse Pin-out
28F001	128K X 8	Contact Catalyst for Product Information				90,120,150			Boot Block Flash
28F002	256K X 8	Contact Catalyst for Product Information				120,150,200			Boot Block Flash

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Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Parallel E²PROMs

(Data Book Section 8)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28C16AP-20	2K X 8	PDIP	24	16Kb	4.5-5.5	200		C	
28C16API-20	2K X 8	PDIP	24	16Kb	4.5-5.5	200		I	
28C16AP-25	2K X 8	PDIP	24	16Kb	4.5-5.5	250		C	
28C16API-25	2K X 8	PDIP	24	16Kb	4.5-5.5	250		I	
28C16AN-20	2K X 8	PLCC	32	16Kb	4.5-5.5	200		C	
28C16ANI-20	2K X 8	PLCC	32	16Kb	4.5-5.5	200		I	
28C16AN-25	2K X 8	PLCC	32	16Kb	4.5-5.5	250		C	
28C16ANI-25	2K X 8	PLCC	32	16Kb	4.5-5.5	250		I	
28C16AJ-20	2K X 8	SOIC	24	16Kb	4.5-5.5	200		C	
28C16AJI-20	2K X 8	SOIC	24	16Kb	4.5-5.5	200		I	
28C16AJ-25	2K X 8	SOIC	24	16Kb	4.5-5.5	250		C	
28C16AJI-25	2K X 8	SOIC	24	16Kb	4.5-5.5	250		I	
28C16AK-20	2K X 8	SOIC	24	16Kb	4.5-5.5	200		C	
28C16AKI-20	2K X 8	SOIC	24	16Kb	4.5-5.5	200		I	
28C16AK-25	2K X 8	SOIC	24	16Kb	4.5-5.5	250		C	
28C16AKI-25	2K X 8	SOIC	24	16Kb	4.5-5.5	250		I	
28C17AP-20	2K X 8	PDIP	28	16Kb	4.5-5.5	200		C	
28C17API-20	2K X 8	PDIP	28	16Kb	4.5-5.5	200		I	
28C17AP-25	2K X 8	PDIP	28	16Kb	4.5-5.5	250		C	
28C17API-25	2K X 8	PDIP	28	16Kb	4.5-5.5	250		I	
28C17AN-20	2K X 8	PLCC	32	16Kb	4.5-5.5	200		C	
28C17ANI-20	2K X 8	PLCC	32	16Kb	4.5-5.5	200		I	
28C17AN-25	2K X 8	PLCC	32	16Kb	4.5-5.5	250		C	
28C17ANI-25	2K X 8	PLCC	32	16Kb	4.5-5.5	250		I	
28C17AJ-20	2K X 8	SOIC	28	16Kb	4.5-5.5	200		C	
28C17AJI-20	2K X 8	SOIC	28	16Kb	4.5-5.5	200		I	
28C17AJ-25	2K X 8	SOIC	28	16Kb	4.5-5.5	250		C	
28C17AJI-25	2K X 8	SOIC	28	16Kb	4.5-5.5	250		I	
28C17AK-20	2K X 8	SOIC	28	16Kb	4.5-5.5	200		C	
28C17AKI-20	2K X 8	SOIC	28	16Kb	4.5-5.5	200		I	
28C17AK-25	2K X 8	SOIC	28	16Kb	4.5-5.5	250		C	
28C17AKI-25	2K X 8	SOIC	28	16Kb	4.5-5.5	250		I	
28C256P-15	32K X 8	PDIP	28	256Kb	4.5-5.5	150		C	
28C256PI-15	32K X 8	PDIP	28	256Kb	4.5-5.5	150		I	
28C256P-20	32K X 8	PDIP	28	256Kb	4.5-5.5	200		C	
28C256PI-20	32K X 8	PDIP	28	256Kb	4.5-5.5	200		I	
28C256P-25	32K X 8	PDIP	28	256Kb	4.5-5.5	250		C	
28C256PI-25	32K X 8	PDIP	28	256Kb	4.5-5.5	250		I	
28C256N-15	32K X 8	PLCC	32	256Kb	4.5-5.5	150		C	
28C256NI-15	32K X 8	PLCC	32	256Kb	4.5-5.5	150		I	
28C256N-20	32K X 8	PLCC	32	256Kb	4.5-5.5	200		C	
28C256NI-20	32K X 8	PLCC	32	256Kb	4.5-5.5	200		I	
28C256N-25	32K X 8	PLCC	32	256Kb	4.5-5.5	250		C	
28C256NI-25	32K X 8	PLCC	32	256Kb	4.5-5.5	250		I	
28C256T13-15	32K X 8	TSOP	28	256Kb	4.5-5.5	150		C	

Parallel E²PROMs (cont.)

(Data Book Section 8)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28C256TI13-15	32K X 8	TSOP	28	256Kb	4.5-5.5	150		I	
28C256T13-20	32K X 8	TSOP	28	256Kb	4.5-5.5	200		C	
28C256TI13-20	32K X 8	TSOP	28	256Kb	4.5-5.5	200		I	
28C256T13-25	32K X 8	TSOP	28	256Kb	4.5-5.5	250		C	
28C256TI13-25	32K X 8	TSOP	28	256Kb	4.5-5.5	250		I	
28C256T14-15	32K X 8	TSOP	32	256Kb	4.5-5.5	150		C	
28C256TI14-15	32K X 8	TSOP	32	256Kb	4.5-5.5	150		I	
28C256T14-20	32K X 8	TSOP	32	256Kb	4.5-5.5	200		C	
28C256TI14-20	32K X 8	TSOP	32	256Kb	4.5-5.5	200		I	
28C256T14-25	32K X 8	TSOP	32	256Kb	4.5-5.5	250		C	
28C256TI14-25	32K X 8	TSOP	32	256Kb	4.5-5.5	250		I	
28C64BP-12	8K X 8	PDIP	28	64Kb	4.5-5.5	120		C	
28C64BPI-12	8K X 8	PDIP	28	64Kb	4.5-5.5	120		I	
28C64BP-15	8K X 8	PDIP	28	64Kb	4.5-5.5	150		C	
28C64BPI-15	8K X 8	PDIP	28	64Kb	4.5-5.5	150		I	
28C64BP-20	8K X 8	PDIP	28	64Kb	4.5-5.5	200		C	
28C64BPI-20	8K X 8	PDIP	28	64Kb	4.5-5.5	200		I	
28C64BN-12	8K X 8	PLCC	32	64Kb	4.5-5.5	120		C	
28C64BNI-12	8K X 8	PLCC	32	64Kb	4.5-5.5	120		I	
28C64BN-15	8K X 8	PLCC	32	64Kb	4.5-5.5	150		C	
28C64BNI-15	8K X 8	PLCC	32	64Kb	4.5-5.5	150		I	
28C64BN-20	8K X 8	PLCC	32	64Kb	4.5-5.5	200		C	
28C64BNI-20	8K X 8	PLCC	32	64Kb	4.5-5.5	200		I	
28C64BT-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		C	
28C64BTI-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		I	
28C64BT-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		C	
28C64BTI-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		I	
28C64BT-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		C	
28C64BTI-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		I	
28C64BT13-12	8K X 8	TSOP	28	64Kb	4.5-5.5	120		C	
28C64BT13I-12	8K X 8	TSOP	28	64Kb	4.5-5.5	120		I	
28C64BT13-15	8K X 8	TSOP	28	64Kb	4.5-5.5	150		C	
28C64BT13I-15	8K X 8	TSOP	28	64Kb	4.5-5.5	150		I	
28C64BT13-20	8K X 8	TSOP	28	64Kb	4.5-5.5	200		C	
28C64BT13I-20	8K X 8	TSOP	28	64Kb	4.5-5.5	200		I	
28C64BT14-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		C	
28C64BT14I-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		I	
28C64BT14-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		C	
28C64BT14I-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		I	
28C64BT14-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		C	
28C64BT14I-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		I	
28C64BJ-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		C	
28C64BJI-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		I	
28C64BJ-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		C	
28C64BJI-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		I	
28C64BJ-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		C	
28C64BJI-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		I	
28C64BK-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		C	
28C64BKI-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		I	
28C64BK-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		C	
28C64BKI-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		I	
28C64BK-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		C	
28C64BKI-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		I	

Parallel E²PROMs (cont.)

(Data Book Section 8)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28C65BP-12	8K X 8	PDIP	28	64Kb	4.5-5.5	120		C	
28C65BPI-12	8K X 8	PDIP	28	64Kb	4.5-5.5	120		I	
28C65BP-15	8K X 8	PDIP	28	64Kb	4.5-5.5	150		C	
28C65BPI-15	8K X 8	PDIP	28	64Kb	4.5-5.5	150		I	
28C65BP-20	8K X 8	PDIP	28	64Kb	4.5-5.5	200		C	
28C65BPI-20	8K X 8	PDIP	28	64Kb	4.5-5.5	200		I	
28C65BN-12	8K X 8	PLCC	32	64Kb	4.5-5.5	120		C	
28C65BNI-12	8K X 8	PLCC	32	64Kb	4.5-5.5	120		I	
28C65BN-15	8K X 8	PLCC	32	64Kb	4.5-5.5	150		C	
28C65BNI-15	8K X 8	PLCC	32	64Kb	4.5-5.5	150		I	
28C65BN-20	8K X 8	PLCC	32	64Kb	4.5-5.5	200		C	
28C65BNI-20	8K X 8	PLCC	32	64Kb	4.5-5.5	200		I	
28C65BT-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		C	
28C65BTI-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		I	
28C65BT-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		C	
28C65BTI-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		I	
28C65BT-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		C	
28C65BTI-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		I	
28C65BT13-12	8K X 8	TSOP	28	64Kb	4.5-5.5	120		C	
28C65BT13I-12	8K X 8	TSOP	28	64Kb	4.5-5.5	120		I	
28C65BT13-15	8K X 8	TSOP	28	64Kb	4.5-5.5	150		C	
28C65BT13I-15	8K X 8	TSOP	28	64Kb	4.5-5.5	150		I	
28C65BT13-20	8K X 8	TSOP	28	64Kb	4.5-5.5	200		C	
28C65BT13I-20	8K X 8	TSOP	28	64Kb	4.5-5.5	200		I	
28C65BT14-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		C	
28C65BT14I-12	8K X 8	TSOP	32	64Kb	4.5-5.5	120		I	
28C65BT14-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		C	
28C65BT14I-15	8K X 8	TSOP	32	64Kb	4.5-5.5	150		I	
28C65BT14-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		C	
28C65BT14I-20	8K X 8	TSOP	32	64Kb	4.5-5.5	200		I	
28C65BJ-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		C	
28C65BJI-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		I	
28C65BJ-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		C	
28C65BJI-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		I	
28C65BJ-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		C	
28C65BJI-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		I	
28C65BK-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		C	
28C65BKI-12	8K X 8	SOIC	28	64Kb	4.5-5.5	120		I	
28C65BK-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		C	
28C65BKI-15	8K X 8	SOIC	28	64Kb	4.5-5.5	150		I	
28C65BK-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		C	
28C65BKI-20	8K X 8	SOIC	28	64Kb	4.5-5.5	200		I	
28LV256P-25	32K X 8	PDIP	28	256Kb	3.0-3.6	250		C	
28LV256PI-25	32K X 8	PDIP	28	256Kb	3.0-3.6	250		I	
28LV256P-30	32K X 8	PDIP	28	256Kb	3.0-3.6	300		C	
28LV256PI-30	32K X 8	PDIP	28	256Kb	3.0-3.6	300		I	
28LV256P-35	32K X 8	PDIP	28	256Kb	3.0-3.6	350		C	
28LV256PI-35	32K X 8	PDIP	28	256Kb	3.0-3.6	350		I	
28LV256N-25	32K X 8	PLCC	32	256Kb	3.0-3.6	250		C	
28LV256NI-25	32K X 8	PLCC	32	256Kb	3.0-3.6	250		I	
28LV256N-30	32K X 8	PLCC	32	256Kb	3.0-3.6	300		C	
28LV256NI-30	32K X 8	PLCC	32	256Kb	3.0-3.6	300		I	
28LV256N-35	32K X 8	PLCC	32	256Kb	3.0-3.6	350		C	
28LV256NI-35	32K X 8	PLCC	32	256Kb	3.0-3.6	350		I	

Parallel E²PROMs (cont.)

(Data Book Section 8)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28LV256T13-25	32K X 8	TSOP	28	256Kb	3.0-3.6	250		C	
28LV256T13I-25	32K X 8	TSOP	28	256Kb	3.0-3.6	250		I	
28LV256T13-30	32K X 8	TSOP	28	256Kb	3.0-3.6	300		C	
28LV256T13I-30	32K X 8	TSOP	28	256Kb	3.0-3.6	300		I	
28LV256T13-35	32K X 8	TSOP	28	256Kb	3.0-3.6	350		C	
28LV256T13I-35	32K X 8	TSOP	28	256Kb	3.0-3.6	350		I	
28LV256T14-25	32K X 8	TSOP	32	256Kb	3.0-3.6	250		C	
28LV256T14I-25	32K X 8	TSOP	32	256Kb	3.0-3.6	250		I	
28LV256T14-30	32K X 8	TSOP	32	256Kb	3.0-3.6	300		C	
28LV256T14I-30	32K X 8	TSOP	32	256Kb	3.0-3.6	300		I	
28LV256T14-35	32K X 8	TSOP	32	256Kb	3.0-3.6	350		C	
28LV256T14I-35	32K X 8	TSOP	32	256Kb	3.0-3.6	350		I	
28LV64P-25	8K X 8	PDIP	28	64Kb	3.0-3.6	250		C	
28LV64PI-25	8K X 8	PDIP	28	64Kb	3.0-3.6	250		I	
28LV64P-30	8K X 8	PDIP	28	64Kb	3.0-3.6	300		C	
28LV64PI-30	8K X 8	PDIP	28	64Kb	3.0-3.6	300		I	
28LV64P-35	8K X 8	PDIP	28	64Kb	3.0-3.6	350		C	
28LV64PI-35	8K X 8	PDIP	28	64Kb	3.0-3.6	350		I	
28LV64N-25	8K X 8	PLCC	32	64Kb	3.0-3.6	250		C	
28LV64NI-25	8K X 8	PLCC	32	64Kb	3.0-3.6	250		I	
28LV64N-30	8K X 8	PLCC	32	64Kb	3.0-3.6	300		C	
28LV64NI-30	8K X 8	PLCC	32	64Kb	3.0-3.6	300		I	
28LV64N-35	8K X 8	PLCC	32	64Kb	3.0-3.6	350		C	
28LV64NI-35	8K X 8	PLCC	32	64Kb	3.0-3.6	350		I	
28LV64T-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		C	
28LV64TI-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		I	
28LV64T-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		C	
28LV64TI-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		I	
28LV64T-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		C	
28LV64TI-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		I	
28LV64T13-25	8K X 8	TSOP	28	64Kb	3.0-3.6	250		C	
28LV64T13I-25	8K X 8	TSOP	28	64Kb	3.0-3.6	250		I	
28LV64T13-30	8K X 8	TSOP	28	64Kb	3.0-3.6	300		C	
28LV64T13I-30	8K X 8	TSOP	28	64Kb	3.0-3.6	300		I	
28LV64T13-35	8K X 8	TSOP	28	64Kb	3.0-3.6	350		C	
28LV64T13I-35	8K X 8	TSOP	28	64Kb	3.0-3.6	350		I	
28LV64T14-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		C	
28LV64T14I-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		I	
28LV64T14-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		C	
28LV64T14I-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		I	
28LV64T14-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		C	
28LV64T14I-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		I	
28LV64J-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		C	
28LV64JI-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		I	
28LV64J-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		C	
28LV64JI-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		I	
28LV64J-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		C	
28LV64JI-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		I	
28LV64K-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		C	
28LV64KI-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		I	
28LV64K-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		C	
28LV64KI-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		I	
28LV64K-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		C	
28LV64KI-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		I	

Parallel E²PROMs (cont.)

(Data Book Section 8)

Part Number	Org.	Pkg	Lead Count	Dnsty	Oprtg Vltg	Access Time	Clock Freq.	Temp. Range	Special Features
28LV65P-25	8K X 8	PDIP	28	64Kb	3.0-3.6	250		C	
28LV65PI-25	8K X 8	PDIP	28	64Kb	3.0-3.6	250		I	
28LV65P-30	8K X 8	PDIP	28	64Kb	3.0-3.6	300		C	
28LV65PI-30	8K X 8	PDIP	28	64Kb	3.0-3.6	300		I	
28LV65P-35	8K X 8	PDIP	28	64Kb	3.0-3.6	350		C	
28LV65PI-35	8K X 8	PDIP	28	64Kb	3.0-3.6	350		I	
28LV65N-25	8K X 8	PLCC	32	64Kb	3.0-3.6	250		C	
28LV65NI-25	8K X 8	PLCC	32	64Kb	3.0-3.6	250		I	
28LV65N-30	8K X 8	PLCC	32	64Kb	3.0-3.6	300		C	
28LV65NI-30	8K X 8	PLCC	32	64Kb	3.0-3.6	300		I	
28LV65N-35	8K X 8	PLCC	32	64Kb	3.0-3.6	350		C	
28LV65NI-35	8K X 8	PLCC	32	64Kb	3.0-3.6	350		I	
28LV65T-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		C	
28LV65TI-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		I	
28LV65T-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		C	
28LV65TI-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		I	
28LV65T-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		C	
28LV65TI-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		I	
28LV65T13-25	8K X 8	TSOP	28	64Kb	3.0-3.6	250		C	
28LV65TI13-25	8K X 8	TSOP	28	64Kb	3.0-3.6	250		I	
28LV65T13-30	8K X 8	TSOP	28	64Kb	3.0-3.6	300		C	
28LV65TI13-30	8K X 8	TSOP	28	64Kb	3.0-3.6	300		I	
28LV65T13-35	8K X 8	TSOP	28	64Kb	3.0-3.6	350		C	
28LV65TI13-35	8K X 8	TSOP	28	64Kb	3.0-3.6	350		I	
28LV65T14-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		C	
28LV65TI14-25	8K X 8	TSOP	32	64Kb	3.0-3.6	250		I	
28LV65T14-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		C	
28LV65TI14-30	8K X 8	TSOP	32	64Kb	3.0-3.6	300		I	
28LV65T14-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		C	
28LV65TI14-35	8K X 8	TSOP	32	64Kb	3.0-3.6	350		I	
28LV65J-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		C	
28LV65JI-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		I	
28LV65J-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		C	
28LV65JI-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		I	
28LV65J-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		C	
28LV65JI-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		I	
28LV65K-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		C	
28LV65KI-25	8K X 8	SOIC	28	64Kb	3.0-3.6	250		I	
28LV65K-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		C	
28LV65KI-30	8K X 8	SOIC	28	64Kb	3.0-3.6	300		I	
28LV65K-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		C	
28LV65KI-35	8K X 8	SOIC	28	64Kb	3.0-3.6	350		I	

Mixed Signal Products

(Data Book Section 9)

Part Number	Resolution (bits)	Pkg	Lead Count	Settling Time (ns)	DACs/ Pkg	Data Latch	NV Mem.	Temp. Range	Special Features
104AC	12	CDIP	24	40	1	NO	NO	C	1/2 LSB
104ACI	12	CDIP	24	40	1	NO	NO	I	1/2 LSB
104BC	12	CDIP	24	40	1	NO	NO	C	1 LSB
104BCI	12	CDIP	24	40	1	NO	NO	I	1 LSB
105AC	12	CDIP	24	40	1	YES	NO	C	1/2 LSB
105ACI	12	CDIP	24	40	1	YES	NO	I	1/2 LSB
105BC	12	CDIP	24	40	1	YES	NO	C	1 LSB
105BCI	12	CDIP	24	40	1	YES	NO	I	1 LSB
504P	8	PDIP	14	104	4	YES	YES	C	1LSB
504PI	8	PDIP	14	104	4	YES	YES	I	1LSB
504J	8	SOIC	14	104	4	YES	YES	C	1LSB
504JI	8	SOIC	14	104	4	YES	YES	I	1LSB
505P	8	PDIP	20	104	4	YES	YES	C	1LSB
505PI	8	PDIP	20	104	4	YES	YES	I	1LSB
505J	8	SOIC	20	104	4	YES	YES	C	1LSB
505JI	8	SOIC	20	104	4	YES	YES	I	1LSB
506AC	12	CDIP	24	25	1	YES	NO	C	1/2 LSB
506BC	12	CDIP	24	25	1	YES	NO	C	1LSB

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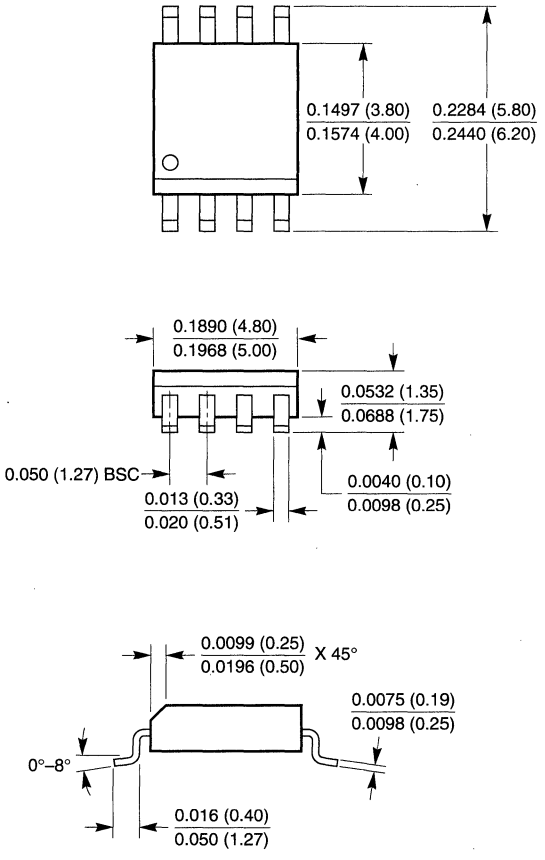
Key:

C = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

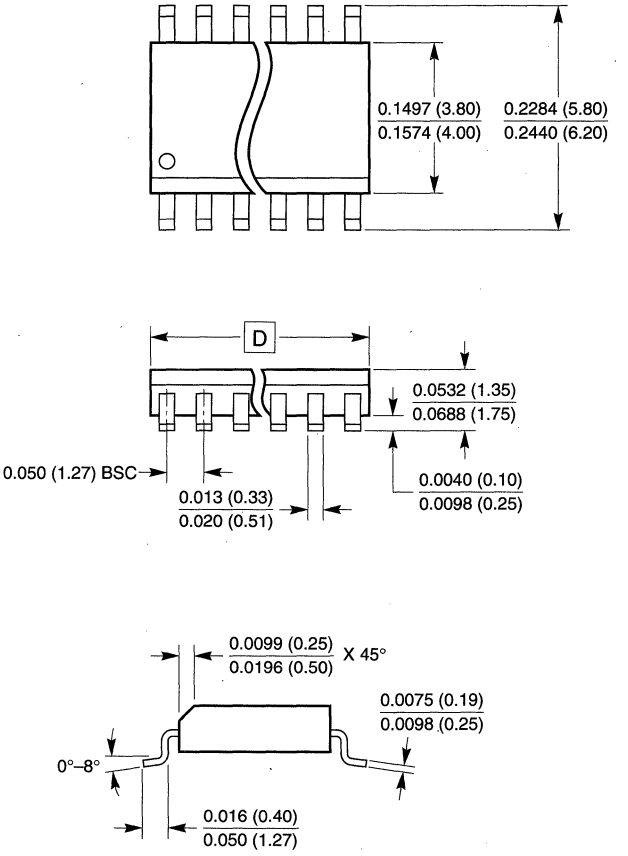
Packaging Information

8-LEAD 150 MIL WIDE SOIC (S)



Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

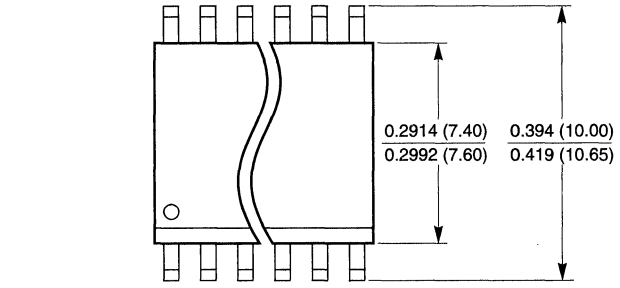
8 AND 14-LEAD 150 MIL WIDE SOIC (J)

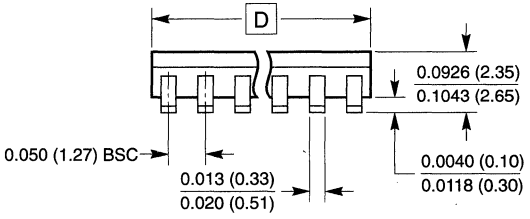


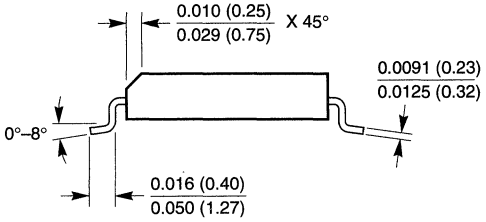
Dimension D		
Pkg	**Min**	**Max**
8L	0.1890(4.80)	0.1968(5.00)
14L	0.3367(8.55)	0.3444(8.75)

Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

16–28-LEAD 300 MIL WIDE SOIC (J)



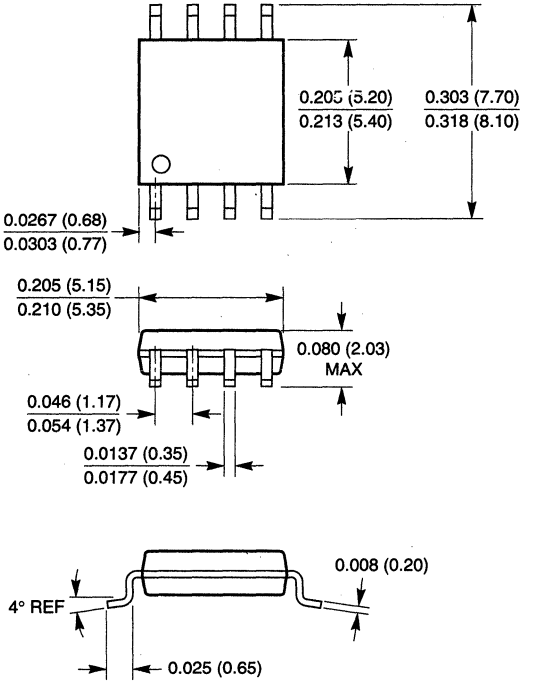




Dimension D		
Pkg	**Min**	**Max**
16L	0.3977 (10.10)	0.4133 (10.50)
18L	0.4469 (11.35)	0.4625 (11.75)
20L	0.4961 (12.60)	0.5118 (13.00)
24L	0.5985 (15.20)	0.6141 (15.60)
28L	0.6969 (17.70)	0.7125 (18.10)

Notes:
1. Complies with JEDEC publication 95 MS-013 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

8-LEAD 210 MIL WIDE SOIC (K)



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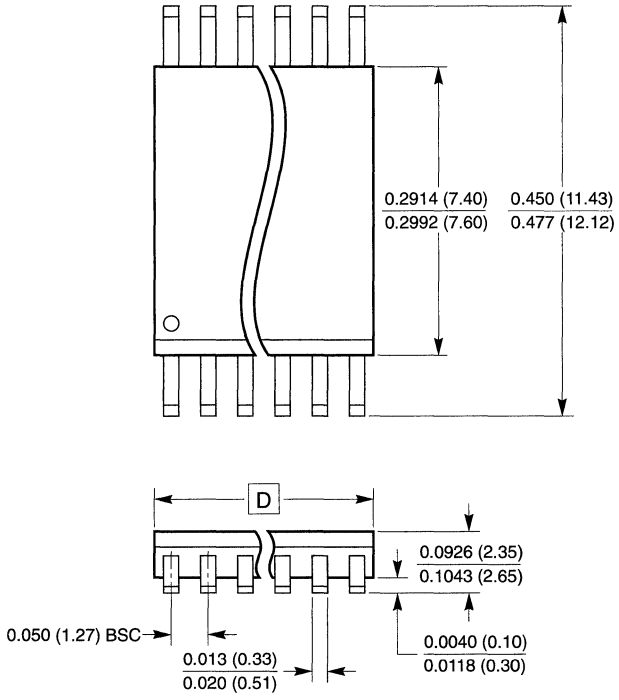
Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

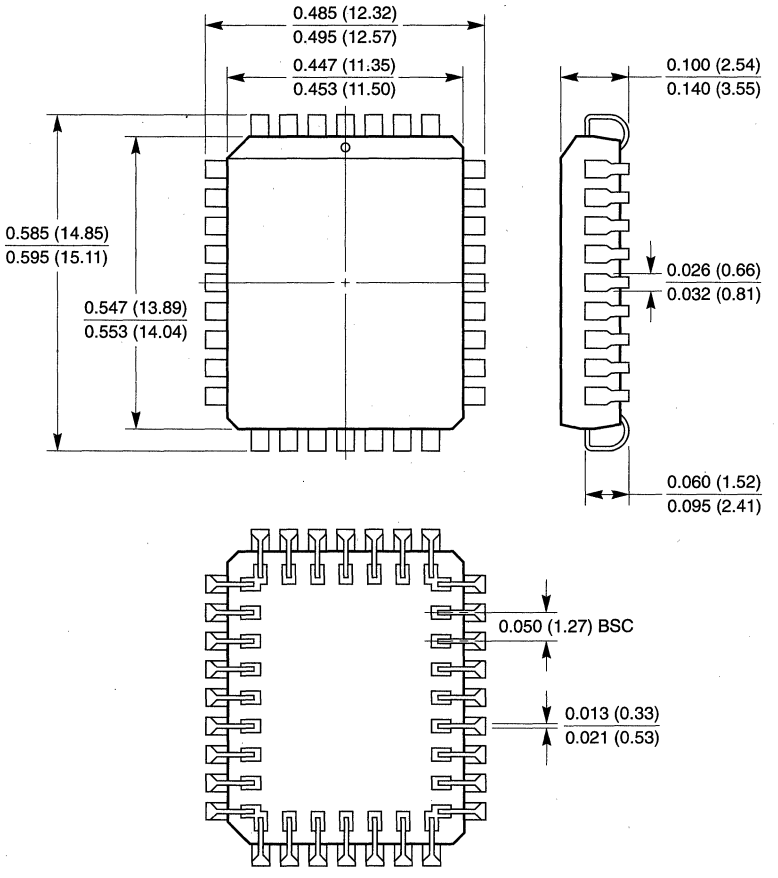
24–28-LEAD 300 MIL WIDE EXTENDED FOOTPRINT SOIC (K)



Dimension D		
Pkg	**Min**	**Max**
24L	0.5985 (15.20)	0.6141 (15.60)
28L	0.6969 (17.70)	0.7125 (18.10)

Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

32-LEAD PLASTIC LEADED CHIP CARRIER (N)



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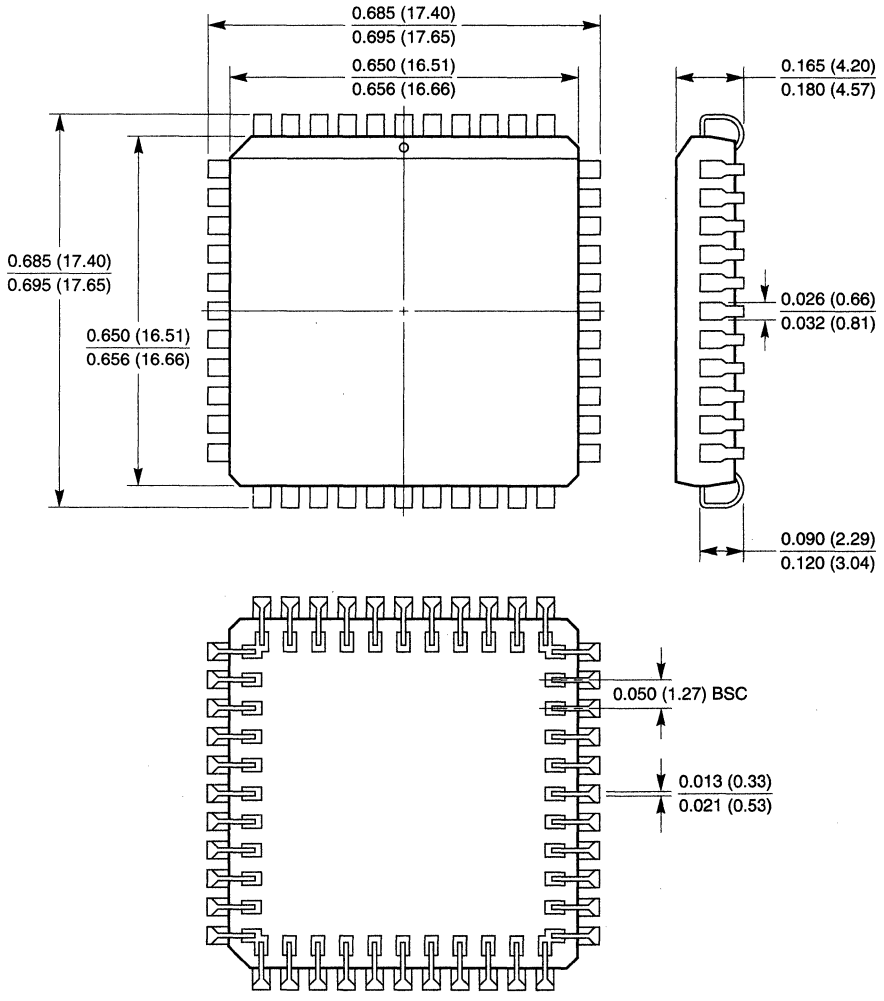
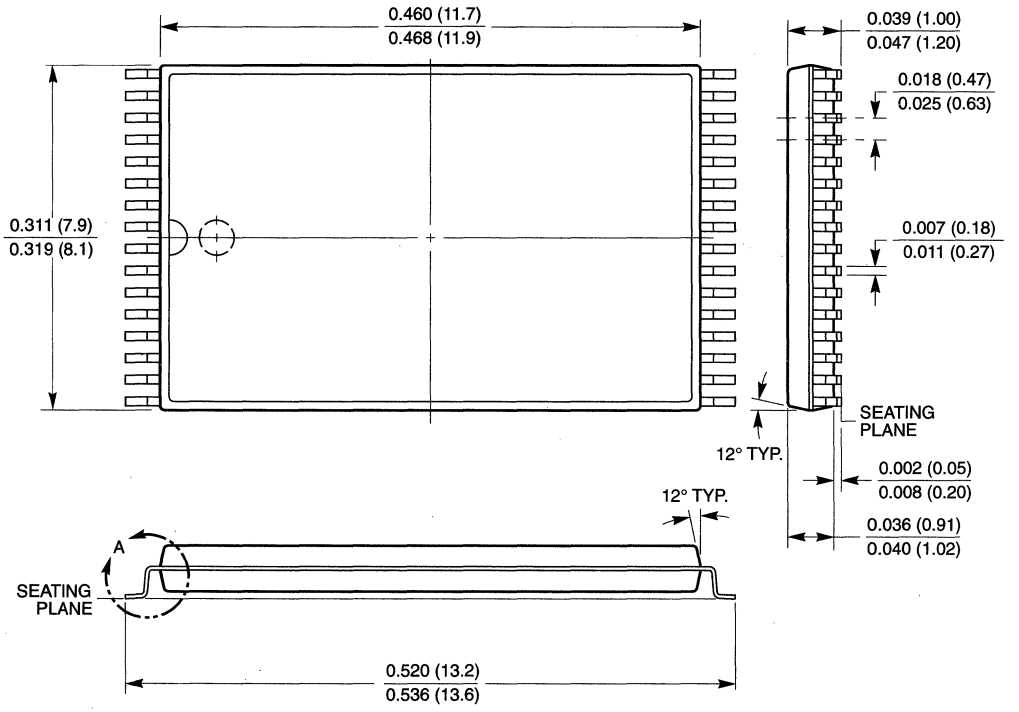
Notes:
1. Complies with JEDEC Publication 95 MO-052 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

44-LEAD PLASTIC LEADED CHIP CARRIER (N)

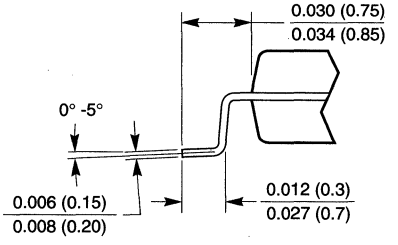


Notes:
1. Complies with JEDEC Publication 95 MO-047 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

28-LEAD 8MM X 13.4 MM TSOP (T13)



DETAIL "A"



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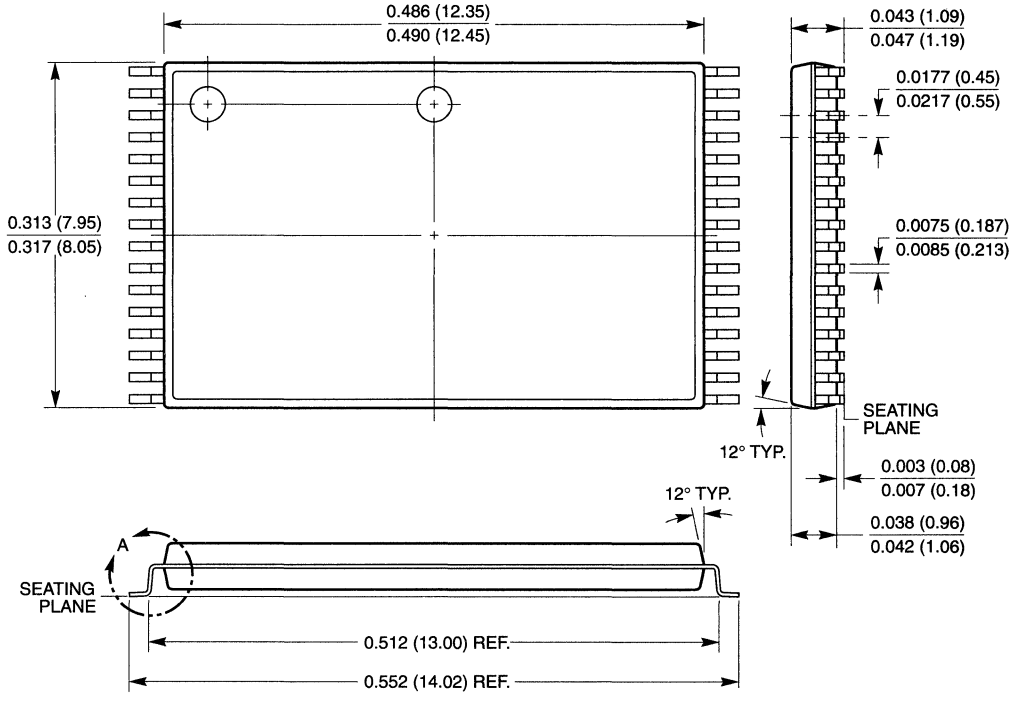
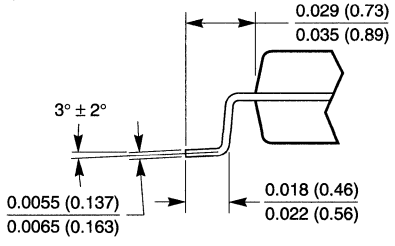
Notes:
1. All linear dimensions are in inches and parenthetically in millimeters.

32-LEAD 8MM X 14MM TSOP (T14)

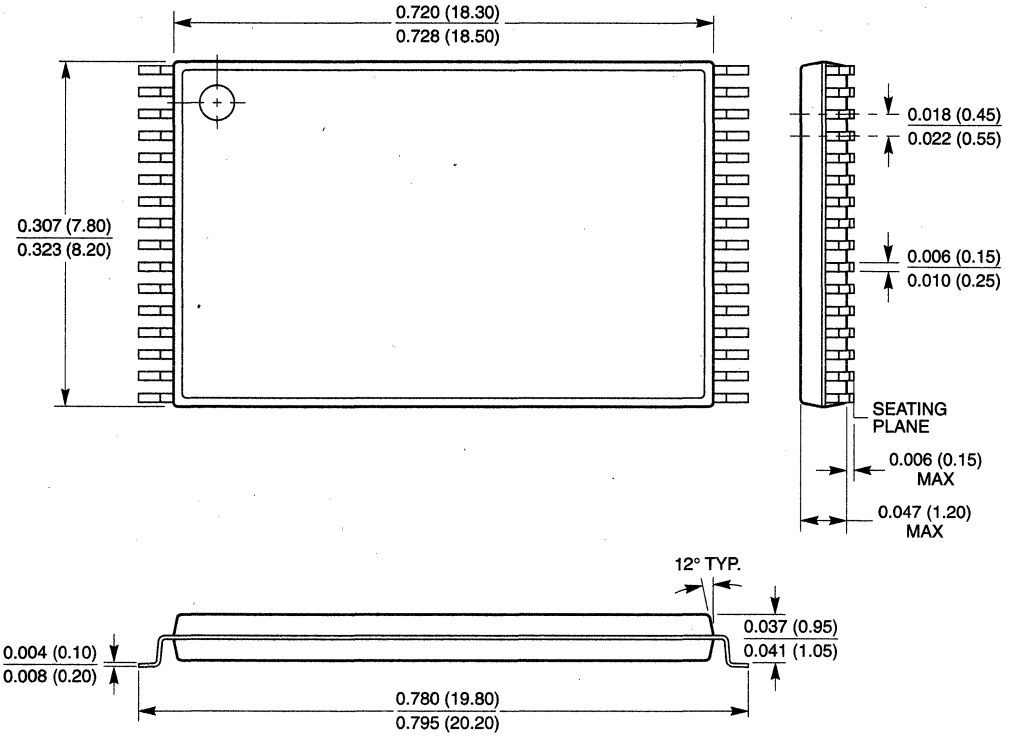


DETAIL "A"



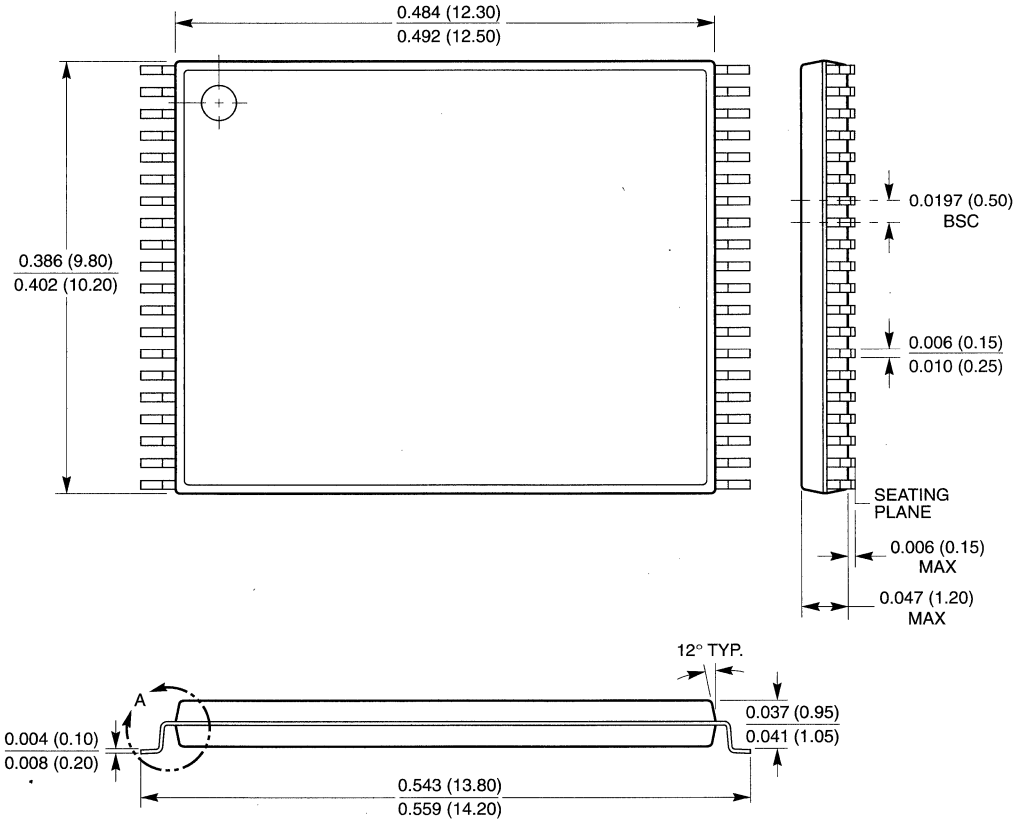
Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

32-LEAD 8MM X 20MM TSOP (T, TR)

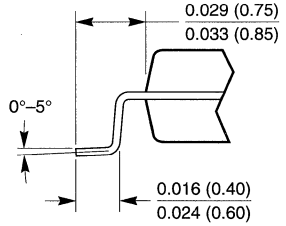


Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

40-LEAD 10MM X 14MM TSOP (T14)

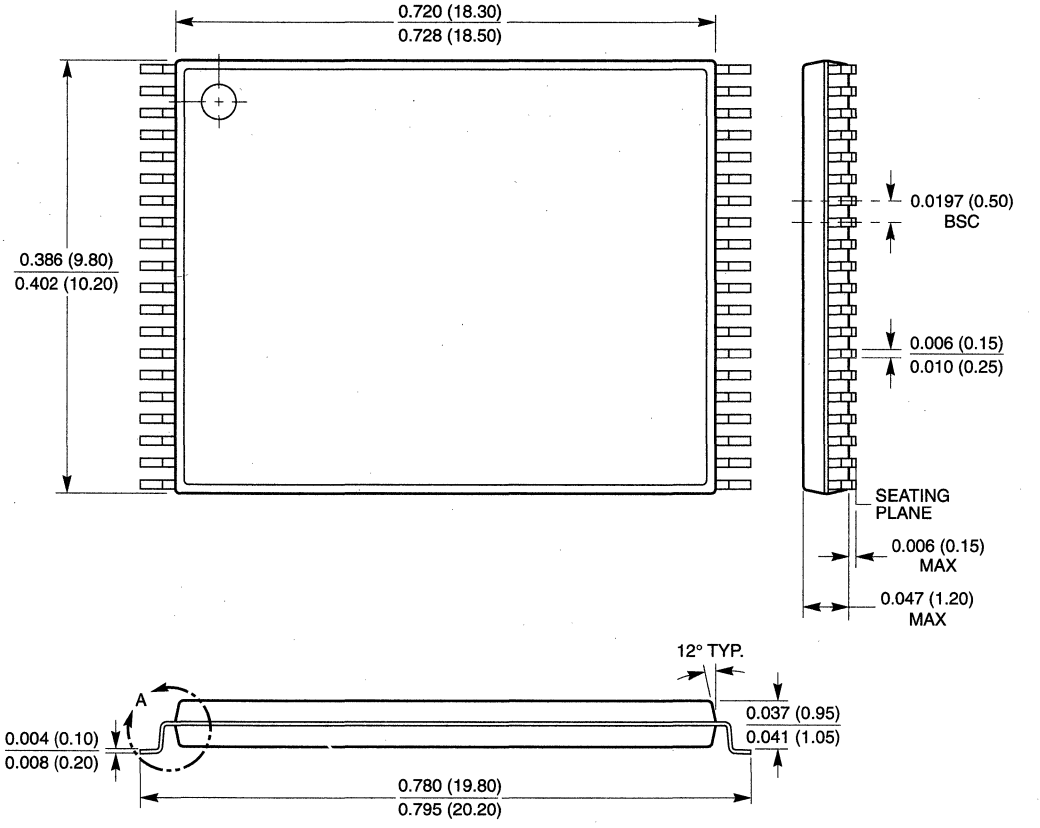


DETAIL "A"

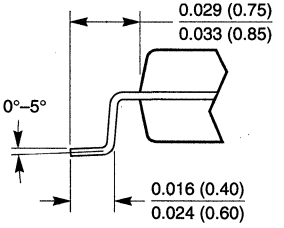


Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

40-LEAD 10MM X 20MM TSOP (T)

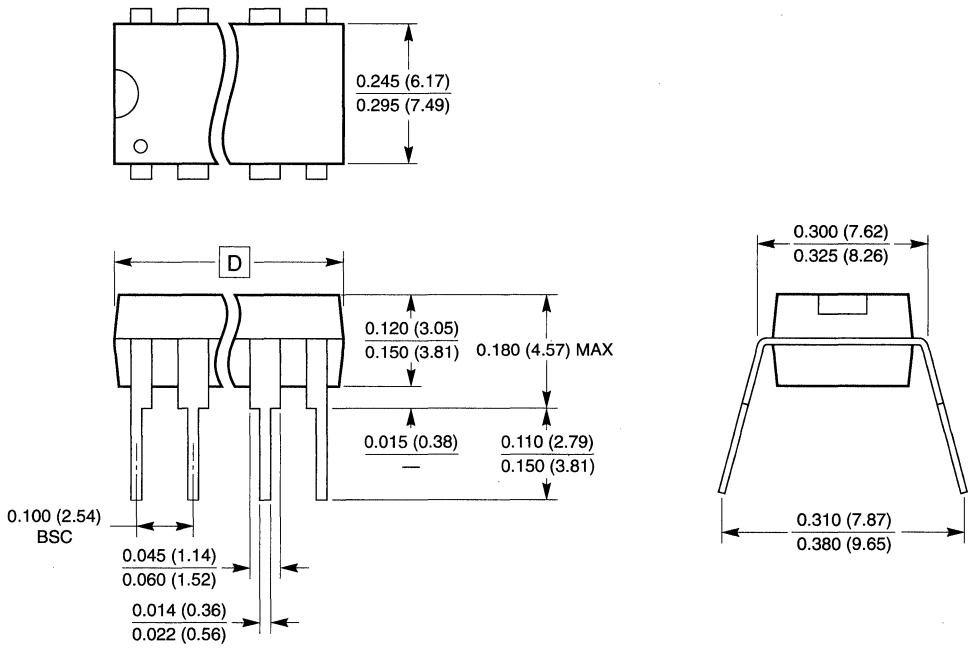


DETAIL "A"



Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

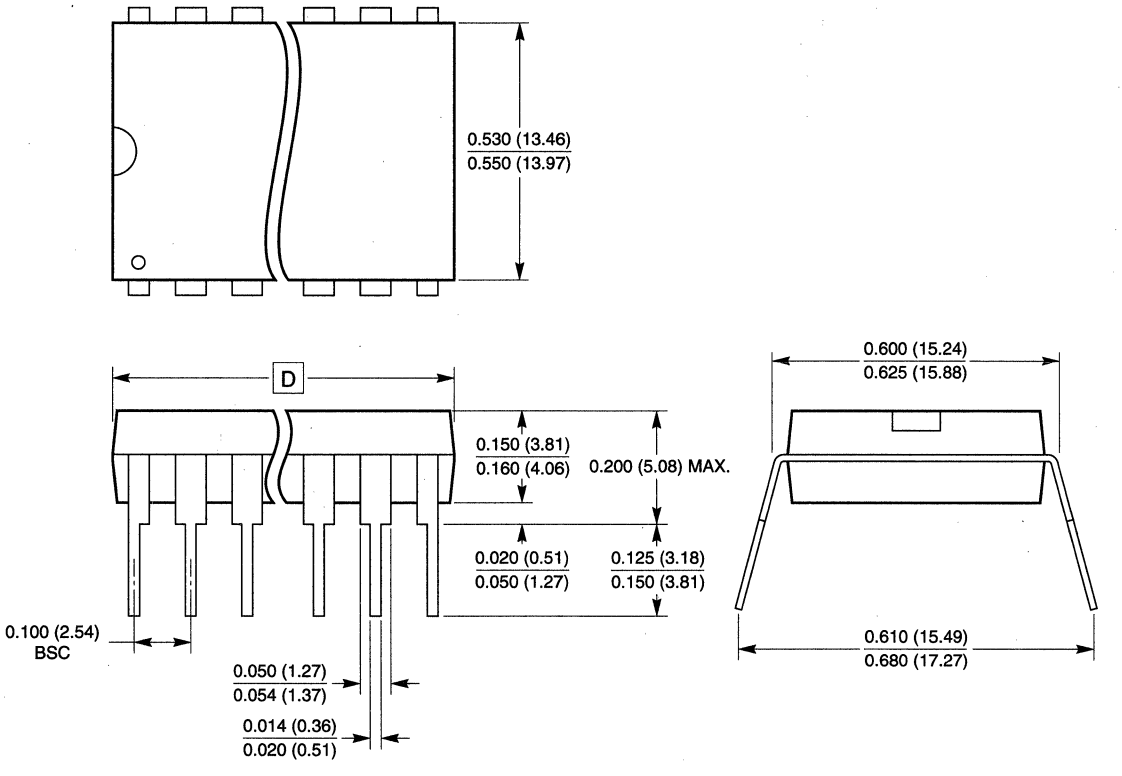
8–22-LEAD 300 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	**Min**	**Max**
8L	0.355 (9.02)	0.385 (9.70)
14L	0.645 (16.38)	0.685 (17.40)
16L	0.745 (21.45)	0.785 (19.94)
18L	0.845 (21.46)	0.885 (22.48)
20L	0.945 (24.00)	0.985 (25.02)
22L	1.045 (26.54)	1.085 (27.56)

Notes:
1. Complies with JEDEC Publication 95 MS001 dimensions; however, some of the dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

24–40-LEAD 600 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	**Min**	**Max**
24L	1.240 (31.50)	1.270 (32.25)
28L	1.420 (36.06)	1.470 (37.33)
32L	1.640 (41.65)	1.670 (42.41)
40L	2.040 (51.81)	2.070 (52.57)

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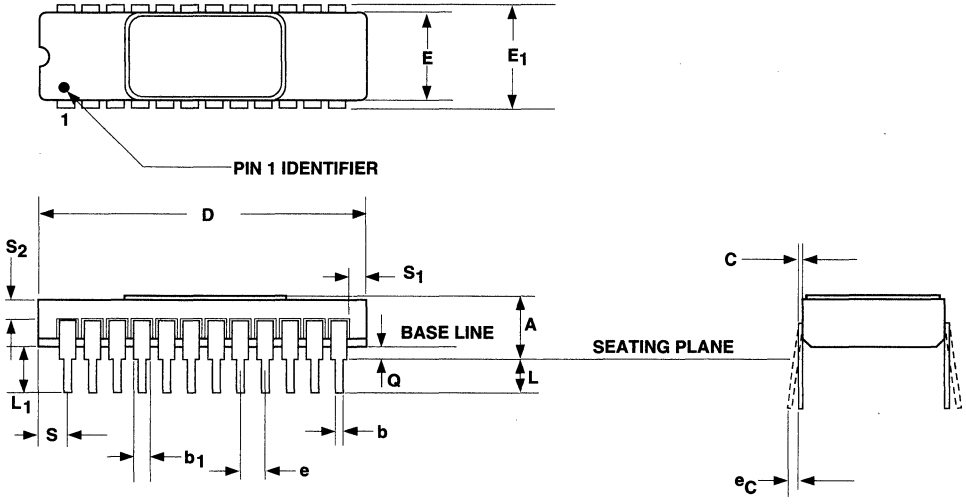
Notes:
1. Complies with JEDEC Publication 95 MO-015 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

24 LEAD 300 MIL WIDE CERDIP (C)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.100	0.200	2.54	5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
e_c	0.125	0.200	3.18	0.508	
L	0.125	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S	0.030	0.065	0.76	1.65	5
S_1	0.005		0.13		5
S_2	0.005			0.13	5

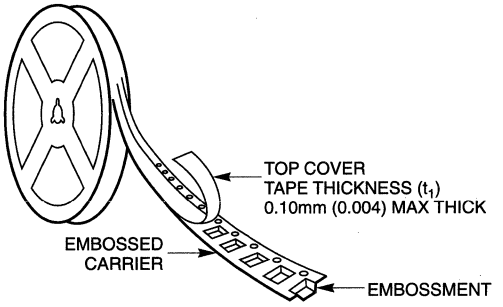
Notes:
(1) Index area; a notch or a lead one identification mark is located adjacent to lead one
(2) The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
(3) Dimension Q shall be measured from the seating plane to the base plane.
(4) This dimension allows for off-center lid, meniscus and glass overrun.
(5) Applies to all four corners.
(6) All leads - increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
(7) Twenty-two-spaces.

TAPE AND REEL

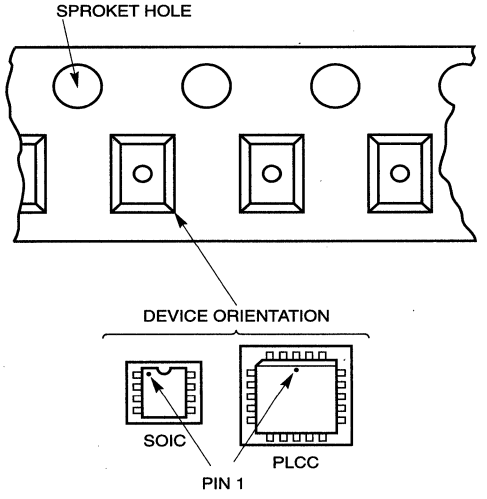
Catalyst surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The tape is wound on 178mm (7 inch) or 330mm (13 inch) reels and individually packaged for shipment.

The following tables and diagrams provide general tape and reel specification data and indicate the tape sizes for various package types. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

Direction of Feed



Device Orientation



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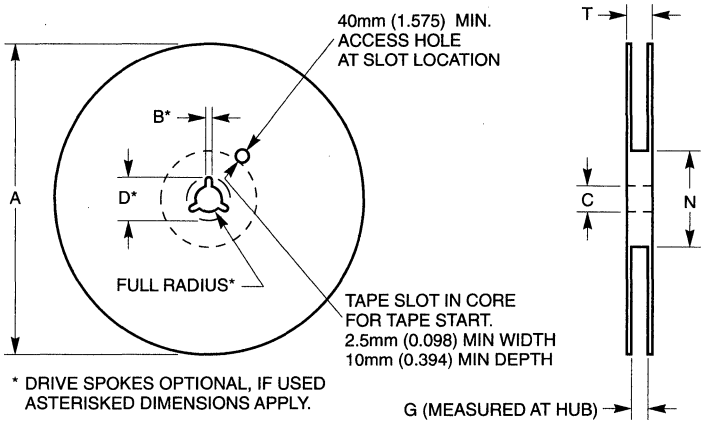
Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

TAPE AND REEL

Reel Dimensions[1]



Tape Size	A				B	C	D*	N	G	T
	Max.	Qty/Reel	Max.	Qty/Reel	Min.		Min.	Min.		Max.
12mm	178 (7.00)	500	330 (13.00)	2000	1.5 (0.059)	12.80 (0.504) / 13.20 (0.520)	20.2 (0.795)	50 (1.969)	12.4 (0.488) / 14.4 (0.558)	18.4 (0.724)
16mm	178 (7.00)	500		2000					16.4 (0.646) / 18.4 (0.724)	22.4 (0.882)
24mm	N/A			500					24.4 (0.961) / 26.4 (1.039)	30.4 (1.197)
				1000						

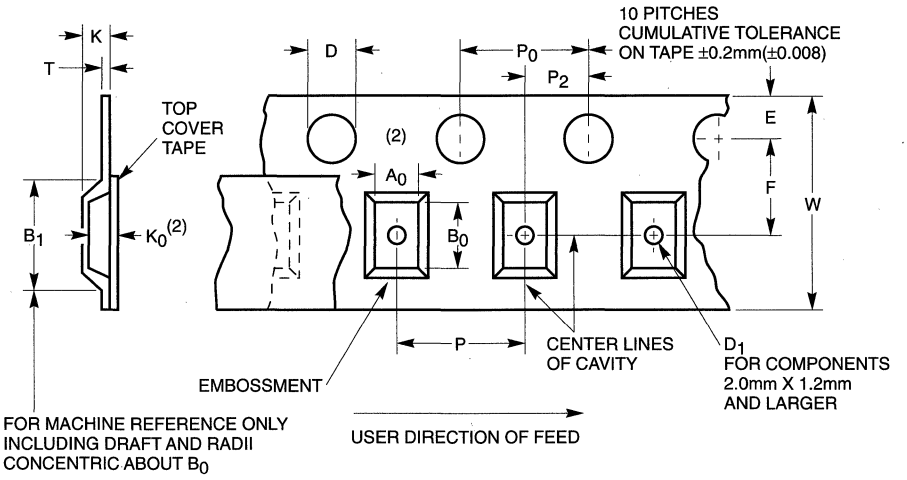
Component/Tape Size Cross-Reference

Component	Package Type	Tape Size (W)	Part Pitch (P)
8-Lead SOIC	J, S	12mm	8mm
8-Lead SOIC	K	16mm	12mm
14-Lead SOIC	J14	16mm	8mm
16-Lead SOIC	J	16mm	12mm
20-Lead SOIC	J	24mm	12mm
24-Lead SOIC	J, K	24mm	12mm
28-Lead SOIC	J, K	24mm	16mm
32-Lead PLCC	N	24mm	16mm
28-Lead TSOP	T14, T13	32mm	16mm
32-Lead TSOP	T	24mm	12mm

Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

TAPE AND REEL

Embossed Carrier Dimensions (12, 16, 24mm Tape Only)



Embossed Tape—Constant Dimensions(1)

Tape Size	D	E	P_0	T Max.	D_1 Min.	A_0 B_0 K_0(2)
12, 16, 24mm	1.5 (0.059) 1.6 (0.063)	1.65 (0.065) 1.85 (0.073)	3.9 (0.153) 4.1 (0.161)	0.400 (0.016)	1.5 (0.059)	

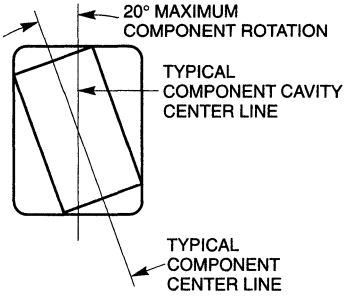
Embossed Tape—Variable Dimensions(1)

Tape Size	B_1 Max.	F	K Max.	P_2	R Min.	W	P
12mm	8.2 (0.323)	5.45 (0.215) 5.55 (0.219)	4.5 (0.177)	1.95 (0.077) 2.05 (0.081)	30 (1.181)	11.7 (0.460) 12.3 (0.484)	7.9 (0.275) 8.1 (0.355)
16mm	12.1 (0.476)	7.4 (0.291) 7.6 (0.299)	6.5 (0.256)	1.9 (0.075) 2.1 (0.083)	40 (1.575)	15.7 (0.618) 16.3 (0.642)	11.9 (0.468) 12.1 (0.476)
24mm	20.1 (0.791)	11.4 (0.449) 11.6 (0.457)			50 (1.969)	23.7 (0.933) 24.3 (0.957)	11.9 (0.468) 12.1 (0.476) 15.9 (0.623) 16.1 (0.634)

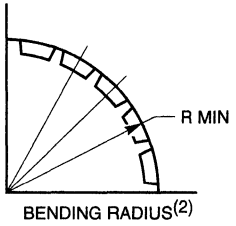
Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.
(2) A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape, and 0.05 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation.

TAPE AND REEL

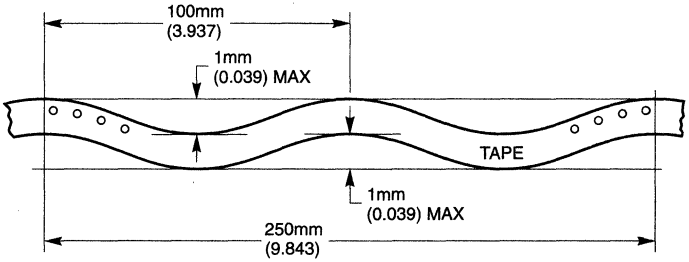
Component Rotation



Bending Radius



Tape Camber (Top View)



ALLOWABLE CAMBER TO BE 1mm/100mm NONACCUMULATIVE OVER 250mm

Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.
(2) Tape and components shall pass around radius "R" without damage.

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Sales Offices

Corporate Headquarters

Catalyst Semiconductor, Inc.
1250 Borregas Avenue
Sunnyvale, California 94089
Phone: 408-752-9600
FAX: 408-752-9800

U.S. Sales Offices

Western U.S.
Catalyst Semiconductor, Inc.
1250 Borregas Avenue
Sunnyvale, California 94089
Phone: 408-752-9600
FAX: 408-752-9800

Central U.S.
Catalyst Semiconductor, Inc.
3800 No. Wilke Road
Suite 372
Arlington Heights, IL 60004
Phone: 708-342-0274
FAX: 708-342-0276

Eastern U.S.
Catalyst Semiconductor, Inc.
50 Nashua Road
Suite 112
Londonberry Square,
Londonberry, NH 03063
Phone: 603-437-2896
FAX: 603-437-6096

International Sales Offices

Japan
Nippon Catalyst K.K.
4th Fl, Shin Nakano
FK Bldg., 6-16-12 Honcho
Nakano-ku, Tokyo 164
JAPAN
Phone: 81.3.5340.3781
FAX: 81.3.5340.3780

Far East
Catalyst Semiconductor, Inc.
9F, No 400, Sec 1
Kee-Lung Road
Taipei, TAIWAN
Phone: 866.2.345.6192
FAX: 866.2.729.9388

CATALYST SEMICONDUCTOR

Catalyst Semiconductor, Inc.
1250 Borregas Avenue
Sunnyvale, California 94089
Phone: 408-752-9600
FAX: 408-752-9800

Until June 1996, Catalyst can be reached at:

Catalyst Semiconductor, Inc.
2231 Calle de Luna
Santa Clara, California 95054
Phone: 408-748-7700
FAX: 408-980-8223

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