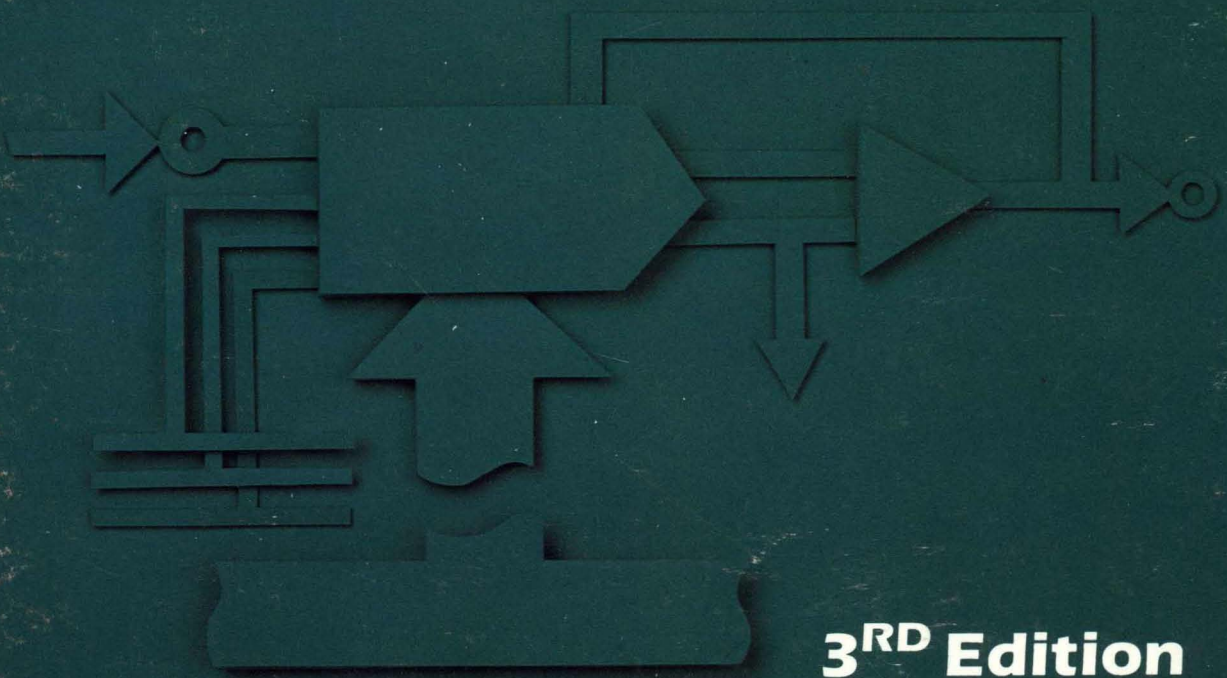
ANALOG DEVICES

CMOS DAC Application Guide



3RD Edition

ANALOG DEVICES

CMOS DAC Application Guide 3RD Edition

CMOS DAC APPLICATION GUIDE

3RD Edition

by

Phil Burton

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October, 1984

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CHAPTER 1

INTRODUCTION TO CMOS DACs

1.1 INTRODUCTION

This text is about CMOS D/A converters—particularly those based on an R-2R resistive ladder network. Since its introduction in 1973 this type of CMOS D/A converter has gained enormous popularity; the aim of this booklet is to explain the basic properties of the circuit and to show how it can best be applied. The emphasis is on the *applications* of CMOS D/A converters rather than the internal design of the circuit although, as always, it is necessary to understand something of the internal workings in order to get the most out of it.

1.2 A BASIC DAC

Most CMOS DACs are based on the circuit shown in Figure 1.1. An external reference is applied to the V_{REF} pin and the R-2R ladder divides the input current I into binary-weighted currents as shown. These currents are then steered by current steering switches to the OUT1 node or to the OUT2 node. The digital input to the D/A converter determines the position of the switch. A logic "1" causes the switch to steer the current to OUT1, a logic "0" causes the switch to steer the current to OUT2. Note that OUT2 is at ground. Feedback around the op

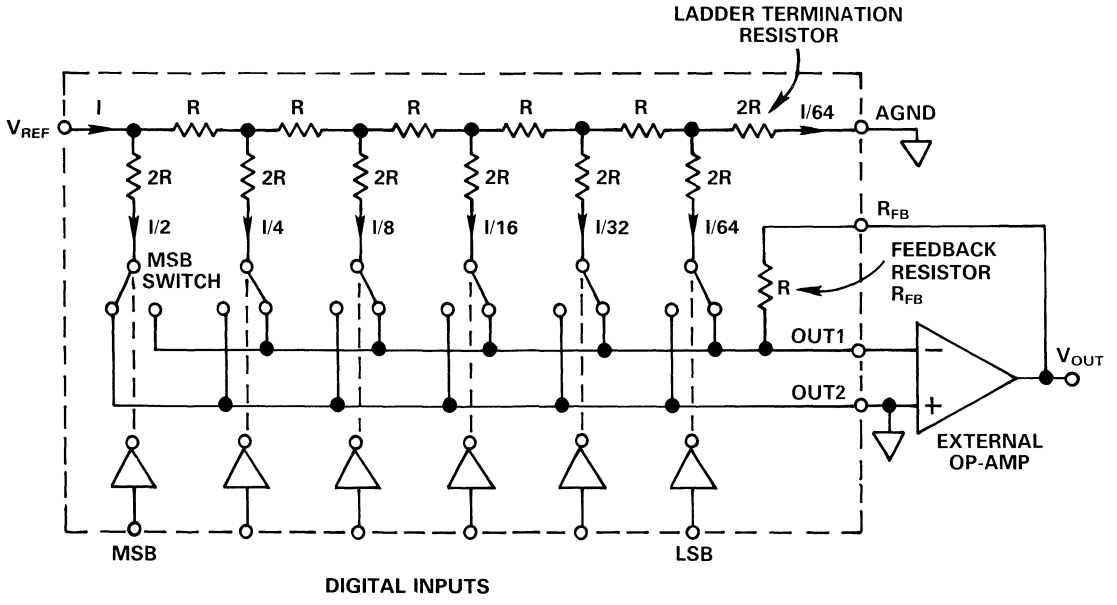


Figure 1.1 Simplified 6-Bit Current-Steering DAC

amp forces OUT1 to also be at ground potential. Thus both switch states look alike to the network. All "0's" at the input causes all the switchable currents to flow to OUT2, all "1's" causes all the switchable currents to flow to OUT1. In the six-bit DAC shown a digital input of "100000" causes I/2 to flow to OUT1 and the remainder of the current to OUT2, thus half the input current is available at OUT1 and 100000 corresponds to half scale. For all 1's the output current is full scale less 1LSB, i.e., $I.(1\text{-}2^{-n})$.

At this stage it is important to point out that the D/A converter will only function as described if the OUT1 and OUT2 nodes are both at the same potential, and furthermore are at ground (AGND). (Chapter 4 discusses some applications where this restriction does not apply.) The standard method of holding OUT1 and OUT2 at ground potential is to use an external op amp connected as a current to voltage converter as shown in Figure 1.1. The feedback resistor R_{FB} is made equal to R and the maximum output voltage is $-I\cdot(1\text{-}2^{-n})\cdot R_{FB}$ where n is the number of bits.

For the six-bit converter of Figure 1.1 the maximum output voltage is $-(63/64)\cdot I\cdot R_{FB}$. Since the remaining one bit worth of current (i.e., I/64), does not exist in the binary system, it is diverted into the ladder termination resistor. The minus sign in the transfer function arises from the inversion introduced by the op amp as a current-to-voltage converter. In a CMOS DAC the resistive ladder is made of thin-film resistors. The feedback resistor R_{FB} is included on the integrated circuit so that $R_{FB} = R$ as nearly as practically possible. This makes the maximum output voltage equal to $-V_{REF}\cdot(1\text{-}2^{-n})$. The current steering switches are fabricated as NMOS switches whose on-resistance is low enough to be negligible compared with the R/2R ladder resistors in the circuit. In a typical CMOS D/A converter the voltage drop across the switches is about 10mV for a reference voltage V_{REF} of +10V. Note that the input resistance at the V_{REF} terminal is constant and equal to R; this is known as the input (or characteristic) resistance of the DAC and is generally denoted by R_{DAC}.

1.3 MULTIPLYING PROPERTIES

So far, it has been assumed that the reference voltage V_{REF} is fixed. In fact V_{REF} can be any voltage that does not overstress the resistors. It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converter" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REF} terminal.

$$V_{OUT} = -D\cdot V_{REF}$$

D is the fractional binary value of the digital word applied to the converter. One popular use of the CMOS multiplying D/A converter is as an audio attenuator. The audio signal is applied to the V_{REF} node, the digital input determines the attenuation, and the output voltage is the product of the two. Other types of D/A converter are often termed "multiplying converters" but upon close examination their multiplying capability may be restricted to a limited range of input voltage (V_{REF}). CMOS D/A converters can operate with values of V_{REF} up to $\pm 25V$ (check the data sheet for individual part ratings) even though the supply voltage to the circuit may be only +5 volts. Furthermore, since most of the significant voltage drops in a CMOS D/A converter are across high quality thin-film resistors, the device inherently has low noise and low distortion.

1.4 CODES AND TERMINOLOGY

The terminology used in describing CMOS D/A converters does not conform to any particular standard and as a result the various nodes on the circuit are not always labelled the same way. For the purposes of standardization this text will use the designated pin names V_{REF}, OUT1, OUT2, R_{FB} and AGND as described for the circuit of Figure 1.1. In later applications the actual use of these terminals may not be reflected by their name (for example OUT1 can be used as a reference terminal) but the text will strive to differentiate between the designated pin name and the function for which it is used. Also it is often necessary to connect nodes together on the chip in order to reduce pin count and bring them out as a single pin (AGND and OUT2 are often joined): this connection will be clear in most applications, but for further reference Appendix A1 gives the internal connection for all Analog Devices CMOS Multiplying DACs.

The R-2R ladder which forms the basis of CMOS D/A converters has an inherent binary nature. There are several forms of binary code in use and it is useful to examine the relationship between these codes. Key codes in the various number systems for an eight bit number are shown in Table 1.1. The simple binary and 2's complement coding schemes will be known to anyone conversant with contemporary computer practice. Offset binary coding arises as a result of some very simple applications schemes for CMOS DACs which will be covered later. Note

	Negative Numbers					Positive Numbers		
Decimal Value	−128	−127	−64	−1	0	+1	+64	+127
Analog Output V_{OUT}	$(-V_{REF})$	$-V_{REF}\left(\frac{127}{128}\right)$	$-V_{REF}\left(\frac{64}{128}\right)$	$-V_{REF}\left(\frac{1}{128}\right)$	0V	$+V_{REF}\left(\frac{1}{128}\right)$	$+V_{REF}\left(\frac{64}{128}\right)$	$+V_{REF}\left(\frac{127}{128}\right)$
2's Complement	1000 0000	1000 0001	1100 0000	1111 1111	0000 0000	0000 0001	0100 0000	0111 1111
Offset Binary	0000 0000	0000 0001	0100 0000	0111 1111	1000 0000	1000 0001	1100 0000	1111 1111
Sign-Magnitude	Not Available	1111 1111	1100 0000	1000 0001	1000 0000 or 0000 0000	0000 0001	0100 0000	0111 1111

Table 1.1 Analog Output vs. Digital Input for Popular Binary Coding Systems

that offset binary and 2's complement coding are identical save for an inversion of the sign bit. Sign-magnitude coding is also in quite general use in computers; it gives rise to applications circuits slightly different from those for 2's complement coding. The column headings for Table 1.1 also give the analog output voltage which would result from a typical applications circuit.

In a simple binary application the DAC delivers an output which is expressed as a fraction of V_{REF}. Consequently the maximum output voltage is given by:

$$V_{OUT\,max} = -(1\text{-}2^{-n}).V_{REF}$$

This corresponds to all data bits being set to a "1", and is always one bit weight less than $-V_{REF}$. For example if $V_{REF} = -10V$ for the circuit of Figure 1.1 then one bit weight = $10/2^6 = 10/64 = 156mV$ approx. and the maximum output voltage (10 − 0.156) = 9.844 volts.

1.5 WHOLE NUMBERS, FRACTIONS, AND JUSTIFICATION

Converters are normalized to full scale; the MSB has a weight of 2^{-1}, the next has a weight of 2^{-2} and so on all the way to the nth bit, or LSB, which has a weight of 2^{-n}. The largest possible number, all 1's, is 1LSB short of full scale—unity—which is independent of the number of bits. Thus, for converters, the binary code 1 0 1 0 1 is interpreted as the left-justified fractional binary expression, 0.10101_2; (0.5 + 0.125 + 0.03125) = 0.65625.

Computers tend to use whole-number coding; the LSB has a weight of 1(viz., 2^0), the next has a weight of 2(viz., 2^1), the next a weight of 4(viz. 2^2), and so on all the way to the MSB, with a weight of $2^{(n-1)}$. The largest possible number, all 1's, is 1LSB short of full scale, which is 2^n (a function of the number of bits). Thus the binary code, 1 0 1 0 1, is interpreted by the computer as the right-justified whole number, 10101, equal to $2^4 + 2^2 + 2^0$ – i.e., 21. The DAC, on the other hand, interprets the number as $2^{-1} + 2^{-3} + 2^{-5}$ to produce an output of 21/32, or 0.65625 of full scale.

The two systems are equivalent, as they must be; the former is easier to use when considering individual bits; the latter is easier for computing the decimal value of a binary word.

As a result of this duality, two bit-numbering systems have come into use for converters, one left-justified, the other right-justified:

MSB(Bit 1) Bit 2..Bit 3.....(Bit n)
MSB Bit(n-1) Bit(n-2).....Bit(n-3)....Bit 0

Converters that interface with computer buses use the right-justified bus notation for pin-labelling, DB0 for the LSB to DB(n-1) for the MSB. Many other types (e.g., AD7530, AD7523) use the left-justified notation: MSB, Bit 2, etc... Bit n.

CHAPTER 2

INSIDE CMOS DACs

2.1 INTRODUCTION

CMOS DACs are fabricated with a CMOS plus thin-film resistor process. The thin-film is used for the R-2R ladder and CMOS provides the N-channel current steering switches and the interface logic. Thin-film resistors are preferred to diffused resistors for a number of reasons:

a) They match one another better and track better with temperature so that more-accurate D/A converters can be made.

b) Thin-film resistors do not have any parasitic diodes to the substrate or surrounding circuit (diffused resistors do); therefore voltages on the resistors can safely exceed the supply voltages without forward biasing any junctions. Furthermore since there are no diodes and the resistors are insulated from the silicon no leakage takes place from the resistors.

c) Thin-film resistors can be laser trimmed to adjust their final in-circuit value. This allows more accurate converters to be made than would otherwise be possible.

d) Diffused resistors exhibit a voltage dependent resistance. This makes them unsuitable for variable reference circuits, and causes harmonic distortion in attenuator type applications.

Different manufacturers use different processes for the CMOS used in D/A converters. Some adapt a fairly standard metal gate process; Analog Devices uses polysilicon gate processes. The polysilicon gate technique is preferred because it gives two levels of interconnect (compared with the single level of metal gate) and therefore produces denser and smaller circuits. Also it makes it possible to design circuits which are virtually free from the latch-up problems (see Section 2-5) that plague many CMOS devices.

2.2 THE BASIC DESIGN OF CMOS DACs

The NMOS switches used in the D/A converter have a finite on resistance. If all the switches shown in Figure 2.1 were made the same physical size (i.e., equal on-resistance), then the voltage dropped across each

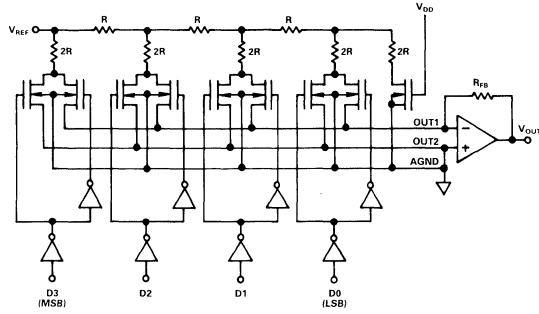


Figure 2.1 Simple CMOS D/A Converter

switch would be proportional to the current in each 2R leg of the R-2R ladder. For example, if V_{REF} = 10V, R = 10 kilohms and the switch on-resistance is 20 ohms then the voltage across the MSB (most significant bit) switch would be 10mV, the voltage across the next most significant switch would be 5mV and so on. This results in each 2R leg of the R-2R ladder having a different voltage at its "lower end". As a result, the D/A converter linearity would be adversely affected. To prevent this from happening the NMOS switches are "scaled" so that the nominal on-resistance of the MSB switch is 20 ohms, the next-significant one is 40 ohms, the next is 80 ohms, etc. all the way down the ladder. For a ten-bit device the least significant bit switch has a nominal

on-resistance of roughly 2 kilohms. All switches therefore have voltage drops of about 10mV for a 10V reference, and each 2R resistor has the same voltage at its "lower end"—thus DAC linearity is unaffected. The resistance of the switches varies with temperature but since the switches are scaled, the voltages across the switches will always match and the D/A converter linearity will be maintained.

The voltage across each switch is chosen to be roughly 10mV (proportional to the reference) because diodes exist from the switch to the P-well containing the switches—see Figure 2.2. With a negative reference voltage the voltage across the switch is negative and the diode is therefore slightly forward biased. However the voltage is designed to be small enough that this does not result in any significant current flowing from the P-well to the R-2R ladder (see section on leakage current).

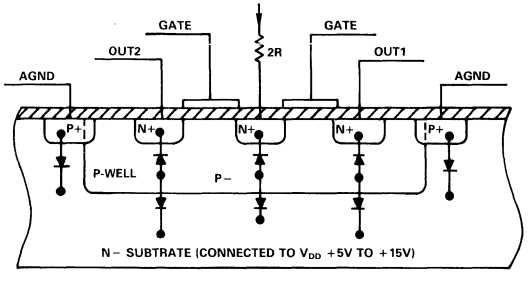


Figure 2.2 Simplified Cross Section through N-Channel DAC Switch Showing Diodes

The P-well containing the N-MOS switches is usually connected to Analog Ground (AGND). If there are sufficient pins available in the package AGND and OUT2 are brought out separately for improved applications flexibility. However, in many cases the number of pins available for analog connections to the DAC are severely limited and OUT2 is often connected internally to AGND and brought out on a single pin. The P-well for the N-MOS switches behaves as an extra gate to the NMOS switches and variations in the P-well voltage can change the on-resistance of the switches, which in turn can cause variations in the output of the D/A converter.

It is, therefore, important to minimize any noise at this node. Some converters use just a single P-well for all N-channel devices, others use separate P-wells for the D/A switches and the supporting interface logic. In this latter case the P-well for the interface logic is connected to digital ground—DGND.

There are three options for connecting the ladder termination resistor:

1) It can be brought out as a separate pin—this is not normally done because a pin is not available.
2) It can be connected internally to AGND (or DGND).
3) It can be connected internally to OUT2.

In designs prior to 1980, the ladder termination resistor is connected to AGND but in more recent circuits the resistor is connected to OUT2 as this is advantageous in some applications. See Appendix 1 for the connections used in various CMOS DACs.

The thin-film resistors used in the R-2R ladder all have the same physical shape: to improve matching 2R is realized by connecting two resistors of value R in series. The resistors are usually designed for a nominal value of 10 or 11 kilohm with a typical manufacturing tolerance of −5, +10 kilohms. Matching between resistors on a given die is of the order of 0.1% which is sufficient for a 10-bit converter. Higher-resolution converters require better matching between resistors; it is achieved by means of laser trimming. A very narrow laser beam is used to evaporate portions of the resistors in order to make them match better. Laser trimming for monolithic CMOS DACs is carried out at the wafer stage, because it is easier and more cost-effective to do the trim prior to separating the wafer into individual dice than to trim after assembly (as is done with hybrids). The trimming process is usually termed L.W.T. for Laser Wafer Trimming.

The switches used in the D/A converter constitute a small extra resistor in series with the 2R leg. Figure 2.3 shows an approximate equivalent circuit for a DAC with all inputs at logic "1"; all the input current is steered to OUT1 with the exception of the ladder

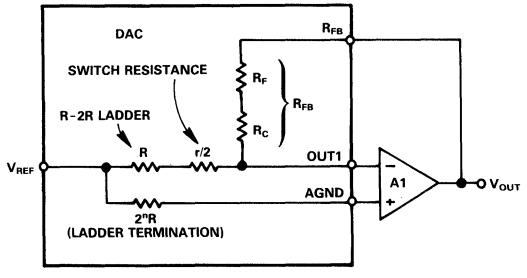


Figure 2.3 Approximate dc Equivalent Circuit of DAC at Full Scale

termination current (which will be neglected here). "r/2" represents the effective on-resistance for all the switches, where r is the on-resistance for the most significant switch. For the circuit to have the correct full-scale value, the equivalent feedback resistor RFB should be equal (R + r/2). To ensure that the performance is held over temperature R_F should equal R and have the same temperature coefficient as the resistors in the R-2R ladder, and RC should equal r/2 and have the same temperature coefficient as the DAC switches. It is a simple matter to achieve this requirement for R_F because the feedback resistor is normally made the same value as the other resistors but the requirement for RC = r/2 is more difficult to achieve. It can be realized by a permanently on switch twice the physical size of the MSB switch; however this significantly increases the die size and cost and also more than doubles the output capacitance which in turn increases the settling time of the DAC. An alternative procedure is to insert a special resistor of value r/2 in series with the feedback resistor R_F. The RC resistor is fabricated from a material whose temperature coefficient matches that of DAC switch. Using either of these methods the "gain error temperature coefficient" of the DAC can be made less than 5ppm/°C.

2.3 CMOS DAC PARAMETERS

2.3.1 Output Leakage Current (ILKG)

Ideally, with all digital inputs at "0", no current should flow out of the OUT1 terminal. In practice the small current that flows is known as the output leakage current. Similarly with all digital inputs at a logic "1", i.e., full scale, no current should flow out of the OUT2 terminal (provided that the ladder termination resistor is not connected to OUT2) but again a leakage current does flow in practice. The leakage current at each terminal comes from two sources, leakage across the source-drain of the "off switch" (ILKGSD), and substrate to P-well leakage (ILKGSS). This is shown in Figure 2.4. Both leakage currents are temperature dependent, roughly doubling for every 10°C temperature rise. ILKGSS will always flow from the substrate out of the OUT1 and OUT2 terminals but the direction and magnitude of ILKGSD will be determined by the reference voltage (analog input). A positive reference voltage gives an ILKGSD which flows out of OUT1 and adds to the effect of ILKGSS; a negative reference voltage gives an ILKGSD which flows into OUT1 and subtracts from the substrate leakage. If the reference voltage is ac, ILKGSD will be ac, setting a lower limit to feedthrough voltage (see 2.3.6). The worst case leakage current arises at the highest operating temperature with a positive reference voltage. For this reason a CMOS D/A converter should always be specified with a positive reference voltage (+10V is normally used). ILKGSS and ILKGSD are usually approximately equal although their relationship depends upon the geometry of the D/A converter under consideration and the various processing steps used in fabrication. In an applications circuit the effect of the leakage currents is to introduce a shift in the D/A transfer function, shown in Figure 2.5, which usually becomes significant at temperatures above 100°C.

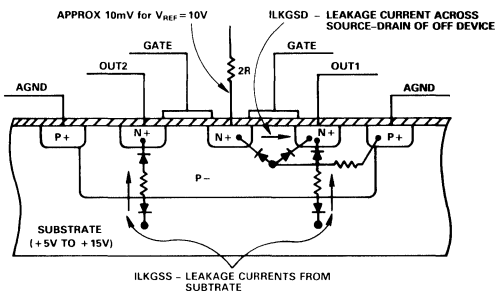
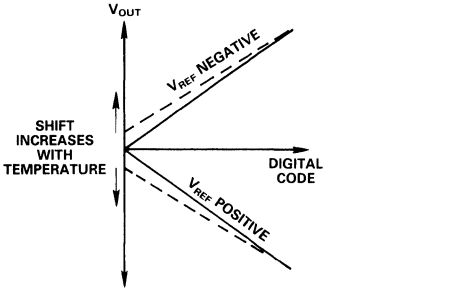
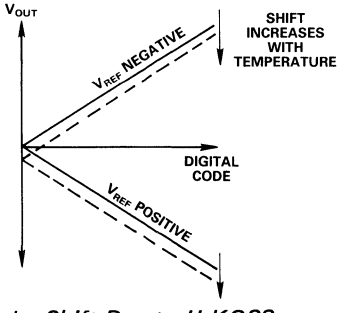


Figure 2.4 Cross-Section through DAC Switch Pair Showing Leakge Paths to OUT1 and OUT2



a. Shift Due to ILKGSD



b. Shift Due to ILKGSS

Figure 2.5 Effect of Leakage Currents on DAC Transfer Function

2.3.2 Gain Error

For an ideal D/A converter the maximum output voltage is given by:

$$V_{max} = -V_{REF} \cdot (1\text{-}2^{-n})$$

In practice the feedback resistor R_{FB} is usually not exactly equal to the ladder resistance R and as a result V_{max} deviates from its correct value. The amount of this deviation is known as gain error and is usually expressed as a percentage or in LSB equivalent units.

$$\text{Gain Error \%} = \frac{V_{max\,actual} - V_{max\,theoretical}}{V_{max\,theoretical}} \times 100$$

The gain error for laser trimmed DACs is usually less than that for non-trimmed devices because laser trim is used to adjust the gain error. As pointed out in the previous section the N-channel DAC switches have a temperature sensitive on-resistance which is compensated for by a matching device in series with the feedback resistor. This reduces the variation of gain error with temperature but does not eliminate it. Gain error temperature coefficient is usually defined as:

$$\text{Gain Error T.C. (ppm/°C)} = \frac{\text{Gain Error at } T_{max} - \text{Gain Error at } T_{min}}{(T_{max} - T_{min})}$$

T_{max} and T_{min} are the two temperatures at which measurements are performed for a given temperature range.

It is very difficult to distinguish between gain error shifts due to temperature coefficient mismatch between the feedback resistor and the DAC, and apparent gain error shifts due to variation in leakage current. As a result the specified gain error for a D/A converter is usually taken to include any effects due to leakage currents. A gain error temperature coefficient of 5ppm/°C results in a 0.5mV shift in full scale output for V_{REF} = 10V and a 10°C temperature change.

2.3.3 Power Supply Rejection Ratio

Gain error is also affected by variations in the supply voltage because a change in V_{DD} changes the gate drive to the DAC switches, causing a variation in switch resistance which in turn results in a small change in the output voltage. Power supply rejection ratio is normally quoted in terms of % change in output per % change in V_{DD} for full scale output of the DAC.

$$\text{Power Supply Rejection Ratio} = \frac{(V_{OUT2} - V_{OUT1}) \cdot V_{DD1}}{(V_{DD2} - V_{DD1}) \cdot V_{OUT1}}$$

V_{OUT1} is the full scale output voltage for $V_{DD} = V_{DD1}$.

V_{OUT2} is the full scale output voltage for $V_{DD} = V_{DD2}$.

A power supply rejection ratio of 0.01%/% results in a full scale output voltage change of 5mV for V_{REF} = 10V and a 5% change in supply voltage.

2.3.4 Output Capacitance

The output capacitance of a CMOS D/A converter may be measured using the circuit of Figure 2.6. The frequency is varied to find the −3dB point and the

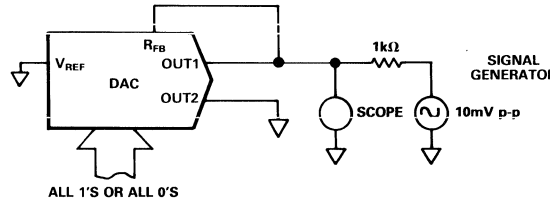


Figure 2.6 Circuit for Measuring Output Capacitance of DAC

capacitance may then be calculated. The output capacitance, which results from the relatively large N-channel devices used for the DAC switches, changes with the digital fraction applied to the D/A converter. The capacitance is a maximum when all the switches to the pin being tested are on and is a minimum when all the switches are off. The output capacitance of a CMOS DAC has a major influence on the settling time of the overall circuit.

2.3.5 Settling Time and Propagation Delays of CMOS DACs

Settling time is defined as the time required for the output of the D/A converter to settle to within 1/2LSB of its final value for a given digital input stimulus—usually zero to full scale. However this apparently straightforward definition hides a multitude of problems. The output current settling time of a CMOS DAC to two equivalent time constants (86%) is measured using an oscilloscope as shown in Figure 2.7 and then this is extrapolated to give a settling time to 1/2LSB assuming single pole exponential response. This provides a basis for comparing different CMOS DACs but is of little practical use because most applications use an output op amp to realize the voltage output. Since the response of the

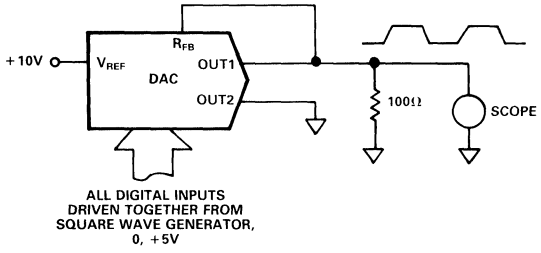


Figure 2.7 Test Circuit for Current Settling Time

output op amp plays a major part in the overall settling time there have been some attempts to quote output voltage settling time using a specified op amp. However, this approach has its own difficulty because different applications use different op amps.

Another factor which complicates the picture is that the definition of settling time given above encompasses both digital propagation delays and analog time constants. Recognizing this, the dependency on the type of op amp used, and the inherent errors in measuring and extrapolating time constants, a useful specification "Propagation Delay" is sometimes employed. Propagation Delay, primarily a measure of the internal digital delays of the DAC, is the time measured from the digital input changing to the output current reaching 90% of the final value. Knowing this, the output capacitance of the DAC (which interacts with the DAC resistance to further delay the response) and the response time of the output op amp, the user is better able to predict the final performance of the circuit.

2.3.6 Multiplying Feedthrough Error

When the D/A converter is operating with an ac signal as its reference some of the input signal may appear on the output even with all 0's presented to the DAC inputs. This is known as Multiplying Feedthrough Error; it arises as a result of stray capacitance, particularly DAC switch capacitance and inter-pin capacitance. Excessive multiplying feedthrough error is usually the result of poor circuit board layout (see Section 5.3.2). Some CMOS DACs have been designed to give very low feedthrough error (notably the AD7111 audio attenuator DAC).

2.3.7 Digital-to-Analog Glitch Impulse

A digital input change results in a change of voltage applied to some of the DAC switch gates. This voltage change is coupled across the stray capacitance shown in Figure 2.8 and appears as an impulse on either the OUT1 or OUT2 line. Digital glitch impulse is usually specified as the area of the resulting spike in either pA-s or nV-s with a specified output amplifier. It is measured with the reference input V_{REF} connected to analog ground and for a zero to full scale output transition. The glitch impulse is proportional to the D/A converter supply voltage and sometimes can be reduced by operating the converter at a lower supply voltage. Excessive digital-to-analog glitch impulse in an applications circuit can often be traced to poor circuit layout or residual solder flux—see Section 5.3.2.

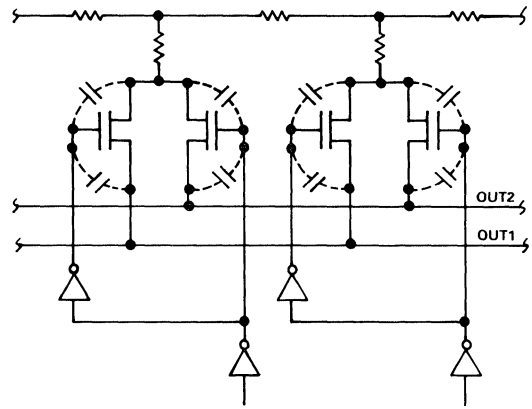


Figure 2.8 Capacitive Coupling from Gate Drive to OUT1 and OUT2

2.3.8 Distortion and Noise

When used as digitally controlled attenuators CMOS DACs exhibit very low distortion—in fact the distortion is primarily determined by the output op amp rather than the DAC itself. CMOS DACs have low distortion because the converter functions as a resistive attenuator using thin-film resistors which have low noise and very low voltage coefficient. The active devices in the DAC, i.e., the DAC switches, have only a very small fraction of the V_{REF} voltage across them; therefore any distortion introduced by the switches is proportionally reduced. The distortion introduced by a CMOS DAC (including the output op amp) is typically −90dB, and the output voltage noise density is about $70nV/\sqrt{Hz}$. It is common to quote the distortion and noise of CMOS D/A converters with a specified op amp. The audio attenuator DACs produced by Analog Devices have been specifically designed for use in applications requiring low noise and distortion.

2.3.9 Supply Voltage (V_{DD})

It is not practical to production test DAC performance for all possible values of supply voltage and as

a result DACs are usually specified and tested at a single value of V_{DD}. DACs can be operated at other supply voltages but this may adversely affect their linearity. Appendix 1 gives the specified operating voltages (i.e., the voltages at which the DACs are tested) for Analog Devices DACs and also their permissible operating range of V_{DD}. Analog Devices (or any other manufacturer) does not guarantee DAC performance at any voltage, other than that for which it is specified. As a general rule, the higher the supply voltage, the better the DAC performance (don't exceed maximum ratings) but there are exceptions to this—see for example Section 2.3.7 above. If the application requires the DAC to operate at a value of V_{DD} other than that for which it is specified, consult the local Analog Devices office for advice. It is often useful to test all DACs at incoming inspection to ensure that they meet their required performance at the application supply voltage.

2.4 EQUIVALENT CIRCUIT OF A CMOS DAC[2]

Figure 2.9 shows an equivalent circuit for a CMOS DAC. C_O is the output capacitance of the DAC switches, and R_S is the output resistance seen between OUT1 and OUT2 with V_{REF} at ground. Both C_O and R_S are code dependent. Full Scale (i.e., 111....111) gives a value for R_S of about 0.75R, and zero gives an almost infinite output resistance. C_O the capacitance from OUT1 to ground, varies approximately linearly with digital fraction from its minimum value at "all zeros" to its maximum value at "all ones".

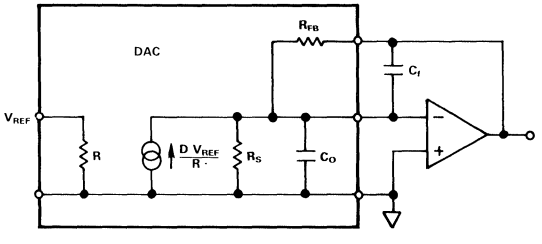


Figure 2.9 Equivalent Circuit of DAC

2.4.1 Feedback Capacitor Selection

The output capacitance of the DAC, C_O, introduces a pole into the open loop response which can cause ringing or instability in the closed loop applications circuit. To compensate for this an external feedback capacitor C_f is usually connected in parallel with R_{FB} as shown in Figure 2.9. Too small a value of C_f can produce ringing at the output, while too large a value can adversely affect the settling time. C_f is best chosen according to the equation

$$C_f = 2 \cdot \sqrt{\frac{C_O}{2\pi \cdot R_{FB}} \cdot \frac{1}{GBW}}$$

where GBW is the small signal unity gain-bandwidth product of the op amp in use. For a typical output capacitance of 100pF, an R_{FB} of 11 kilohm and GBW $= 2.10^6$, C_f = 53pF. Since C_O varies with code (typically 50pF to 200pF), it is not possible to fix a precise value for C_f; and for most DACs a value of 39pF or 47pF is adequate.

2.4.2 Noise Gain of CMOS DACs

The output resistance of a CMOS DAC at OUT1 varies with code. Consequently the feedback circuit of a CMOS DAC exhibits a code-dependent gain for op amp offset voltage. This variable gain is sometimes referred to as the "noise-gain" of the circuit and is shown in Figure 2.10 for an 8-bit DAC. The noise-gain introduces differential linearity errors (i.e., an error between adjacent codes) which, if the amplifier

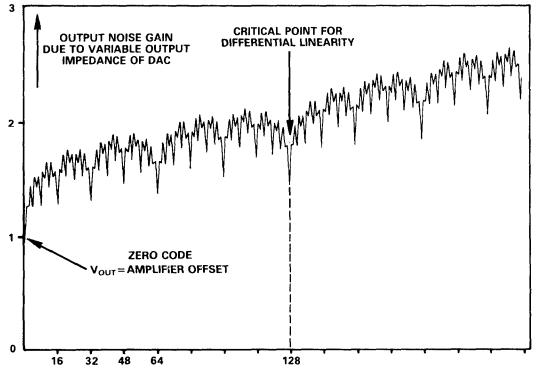


Figure 2.10 DAC Noise Gain vs. Code for 8-Bit DAC

input offset voltage is too large, can result in the DAC becoming non-monotonic. To minimize errors due to the variability of the noise-gain, amplifiers with low offset voltage and low bias currents are used. JFET input amplifiers with laser trimmed offset, such as AD542, AD544, and AD547, are commonly used as DAC output amplifiers—see Section 3.2.

2.5 LATCH-UP IN CMOS

Most CMOS devices contain parasitic SCRs (Silicon Controlled Rectifier)— see Figure 2.11. In normal operation these SCRs are unimportant; however, if an output or input of a CMOS circuit is taken more negative than the most negative supply voltage, the

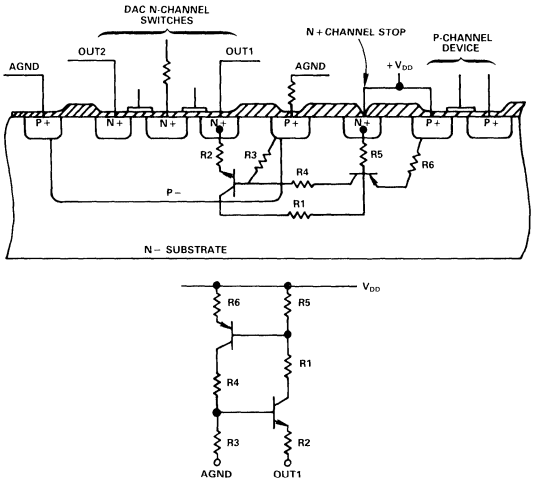


Figure 2.11 Cross Section through CMOS DAC Showing Parasitic NPN and PNP Devices Forming SCR

SCR can be turned on and will remain on until the device is destroyed or the power supply switched off. Negative transient inputs to CMOS devices can occur during power-up as a result of excessive voltage drops in ground lines, or due to transmission line effects in high speed logic systems. In particular some amplifiers exhibit low impedance at their inputs during power-up or power-down sequencing, and as a result the OUT1 or OUT2 lines can go negative. The traditional solution to this problem has been to clamp the OUT1 and OUT2 lines to ground using external Schottky diodes; however, all modern CMOS DACs from Analog Devices use a design technique which reduces the gain of the internal SCR to such a low level that SCR action cannot take place without excessive misuse. Consequently, external Schottky diodes are not required for these DACs. See Appendix 1 for a list of DACs requiring Schottky diodes.

2.6 PROTECTING CMOS AGAINST MISUSE

The digital inputs of Analog Devices' CMOS DACs are diode protected against static electricity using diodes as shown in Figure 2.12. In operation, however, if the digital input goes outside either V_{DD} or GND, the diode turns on and excessive current can flow. If the current exceeds 35mA, metal lines on the chip may fuse open. Close attention should be given to ground management, as substantial negative transients at digital inputs can arise if the ground system is inadequate. In general, "power should be

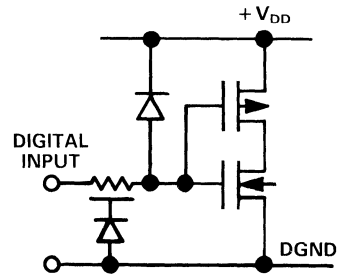


Figure 2.12 Digital Input Circuit Showing Protection Diodes

OFF" when CMOS devices are plugged into working circuits.

2.6.1 Electrostatic Discharge (ESD)[25], [26]

CMOS devices present a very high impedance at their inputs and outputs when not in use. If a high voltage, such as static electricity, is applied to an input or output terminal (usually inadvertently) it is possible, despite the input protection diode, for this voltage to rupture the gate-oxide of some of the MOS devices and destroy the circuit. To prevent such accidents happening, the following five steps should be observed during transportation, storage and system assembly:

1. Keep unused CMOS devices in the black conductive foam or conductive tubes in which they were shipped.
2. Ground the operator who is inserting the devices to the system power ground or bench with a conductive plastic wrist strap.
3. The bench work surface should be made of conductive material and should be connected to ground.
4. Before removing CMOS devices from their foam or tubes, ground the foam to discharge any static that may have built up.
5. After the circuit has been inserted into a circuit board, keep the board grounded or protected whenever it is carried around. Be··are of nylon or similar non-conductive plastic circuit board carriers.

ESD is one of the most common causes of circuit failure during the manufacturing process. It can affect MOS and bipolar devices. For further information see References 25 and 26.

CHAPTER 3

BASIC APPLICATIONS CIRCUITS FOR CMOS DACs OPERATED IN THE CONVENTIONAL CURRENT-STEERING MODE

3.1 UNIPOLAR (CURRENT-STEERING)

Figure 3.1 shows the conventional unipolar D/A converter connection for CMOS DACs. Resistors R1 and R2 are used to trim out any gain error. Resistor R2 places the error band in a region which permits correction within the range of adjustment of R1. For the higher resolution applications (10 bits and up) R1 and R2 should be precision resistors with matched temperature coefficients, as their temperature coefficients can become significant in terms of overall circuit performance. If possible, R1 should be a fixed resistor, rather than a potentiometer, and its value is selected at the time of system calibration. The appropriate value of R2 may be calculated according to the equation.

$$R2 = \frac{(\text{Max DAC Gain Error in \%}) \cdot (RDAC_{max})}{100}$$

$RDAC_{max}$ is the specified maximum input resistance of the DAC. At the reference terminal the maximum range of resistance for R1, when R1 is a potentiometer, may be calculated according to the equation

$$R1 = 2 \cdot R2$$

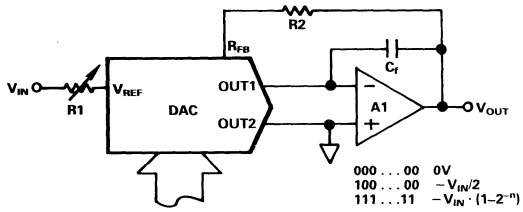


Figure 3.1 Unipolar D/A Converter (Current Steering)

Some CMOS DACs guarantee a maximum gain error of ± 1LSB which may eliminate the requirement for gain error adjustment. Capacitor C_f is for phase compensation and is usually 39pF (see Section 2.4.1). If the op amp is stable when configured with the DAC, C_f may be omitted in applications where settling time or overshoot is unimportant. Input bias current compensation resistors, normally connected to the positive input of the op amp, should not be used, as bias currents can give rise to a voltage offset which in turn results in errors due to the noise gain of the DAC, (see 2.4.2).

The advantages of this particular circuit are its simplicity and low component count. The input impedance presented to V_{REF} is constant, and V_{IN} can exceed the supply voltage (V_{DD}) to the DAC. The main disadvantage of the circuit is that it requires a reference voltage opposite in polarity to the output voltage; as a result single supply operation is not possible.

3.2 OP AMPS FOR CURENT-STEERING MODE DACs[5]

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable "noise gain", (see Section 2-4-2) of the circuit. A change in noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error. If the product of the amplifier input offset voltage and the incremental change in noise gain between adjacent codes exceeds

– 1LSB, a "perfect" D/A converter will nevertheless be non-monotonic. The worst-case incremental changes in noise gain occur on the steps from (Mid-range – 1LSB) to Mid-range and from Mid-range to (Mid-range + 1LSB)—see Figure 2-10. It should be noted that in audio circuits even a small amount of offset can cause an audible "thump" at the output when the DAC changes code.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor R_{FB}. Most op amps have input bias currents low enough to prevent any significant errors (100nA gives an error of about 0.5mV) but the user is cautioned to note that the input bias currents of some JFET amplifiers do reach significant levels at high temperature.

FET-input amplifiers, with low input offset voltage specifications, such as AD542, exhibit negligible offset error due to bias current and are therefore normally used as DAC output amplifiers. For wide temperature range or precision circuits, superbeta input amplifiers such as AD517 work well. They do not have as good a slew rate as the JFET amplifiers, but their open-loop gain is higher and the input offset and bias currents are much lower over the operating temperature range. As a rule of thumb, the maximum input offset voltage for an op amp should be less than 0.1LSB bit weight. For example, a 12-bit DAC with 0 to 10V output range has an LSB bit weight of approximately 2.4mV, which dictates a maximum input offset voltage of less than 240μV. Amplifiers with higher specified offsets can be used if the offset is nulled in-circuit using the external offset trim facilities of the op amp. However, the need to maintain low offset over temperature, the additional cost of an offset trim potentiometer, and the labor to do the calibration is usually much greater than buying the appropriate op amp in the first place. Figure 3.2 shows a method of nulling offset for op amps which do not have external correction terminals. The trimmer is adjusted until OUT1 (not V_{OUT}) is at zero volts and therefore the same potential as OUT2.

The overall settling time of the circuit is a complex function determined by circuit capacitance, gain-bandwidth product of the output amplifier (GBW) and the amplifiers slew rate. For a simple guideline, it is useful to note that the small signal settling time observes the following relationship:

$$\text{Small signal settling time} \propto \sqrt{\frac{R_{FB}(C_O + C_f)}{2 \times GBW}}$$

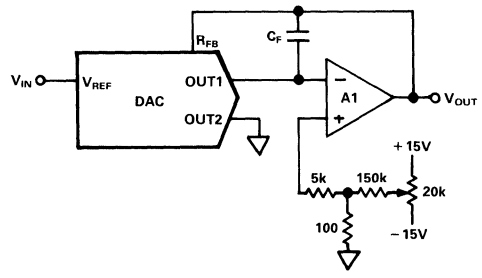


Figure 3.2 Alternative Method of Nulling Op Amp Offset

For optimal settling time in the current-steering mode, DAC output capacitance must be as low as possible and the unity gain-bandwidth product as high as possible.

Finite op amp gain also affects the DAC static accuracy. For example, in the simple D/A converter circuit shown in Figure 3.1.

$$V_{OUT} = -D \cdot V_{IN} \left[\frac{1}{1 + \frac{1}{A}[\text{Noise Gain}]} \right]$$

Thus, the gain-dependent error is approximately

$$D \cdot V_{IN} \cdot \frac{1}{A} \cdot [\text{Noise Gain}]$$

where D is the fractional binary code A is the open loop gain of the amplifier and the "Noise Gain" is the variable gain due to variable output resistance of the DAC. For a 12 bit converter, the value of noise gain at full scale is about 2.0 (See Section 2.4.2).

The error due to finite open loop gain of the amplifier should not be greater than 0.1 LSB. This translates into gains of 5,000, 20,000 and 80,000 for 8-, 10- and 12-bit converters respectively. Fortunately most op amps meet this requirement easily although some of the lower cost (e.g., LM324) or very high speed op amps (e.g., LH0032) do not have adequate gain particularly for 12-bit applications.

3.3 BIPOLAR OUTPUT (OFFSET BINARY AND 2's COMPLEMENT CODING)

The circuit of Figure 3.1 can be modified to give bipolar output by biasing the overall gain negative and doubling the DAC gain as shown in the circuit of Figure 3.3. A code of all 0's corresponds to negative full scale (i.e., $-V_{IN}$) all 1's code gives full scale i.e., $V_{IN}(1\text{-}2^{-(n-1)})$. If an inverter is inserted in the MSB line (shown dotted) then the circuit responds to 2's complement coding.

R1, R2 and R3, should be precision metal film or

wire-wound resistors with matching temperature coefficients. Potentiometers may be used for R1 and R3; however the temperature coefficients of potentiometers vary with position and are unlikely to match R2. In practice, R1 and R3 are best made up

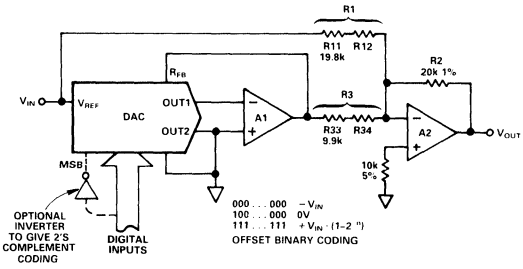


Figure 3.3 Bipolar Ouput D/A Converter

of two resistors in series as shown. R11 and R33 are slightly less than the correct values for R1 and R3 and then R12 and R34 are small value resistors selected at calibration to make up the appropriate value. The circuit is calibrated as follows: first, negative full scale is applied to the digital inputs (all 0's at the DAC), and R12 is selected to give $-V_{IN}$ at the output. Then positive full scale is applied (all 1's at the DAC) and R34 is selected to give $V_{IN}(1\text{-}2^{-(n-1)})$ at the output. A calibration check is then made for zero volts out (1,000...000 at the DAC). The value of R33 + R34 must compensate not only for tolerance errors in R2, but also for gain error in the D/A converter. The value of R33 is therefore given by:

$$R33 = \frac{R2}{2}\ \frac{(1\text{–Max \% Gain Error–R2\% Tolerance})}{100}$$

The main advantages of this circuit are simplicity, constant reference input impedance, and that V_{IN} can exceed the DAC supply voltage.

The main disadvantages are the two-point calibration procedures required and that one bit of resolution is effectively lost in providing the sign—i.e., the 12-bit resolution spans from negative full scale to positive full scale, resulting in 11-bit resolution for each half-scale.

3.4 BIOPOLAR OUTPUT (SIGN + MAGNITUDE CODING)

Figure 3.4 shows a CMOS DAC connected for sign plus magnitude coding. It is similar to the circuit of Figure 3.1 except that the VREF input is switched between $+V_{IN}$ and $-V_{IN}$, depending on the sign bit. Amplifier A2 buffers the V_{REF} input so that variations in the on-resistance of the CMOS switch do not affect calibration. $+V_{IN}$ and $-V_{IN}$ are often available together within a system; but where they are not both present, one can be generated from the other by a simple inverter circuit. The advantage of Figure 3.4 circuit is that it has only a single point calibration for gain error (unlike the circuit of Figure 3.3 which has a two point calibration).

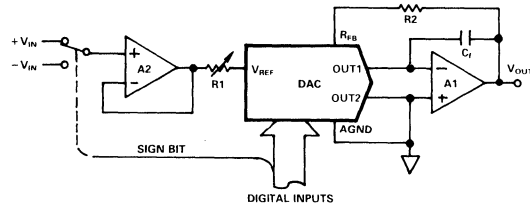


Figure 3.4 Sign Plus Magnitude D/A Converter

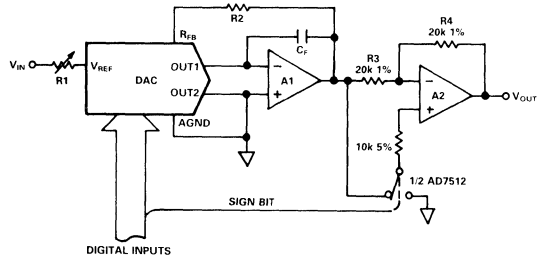


Figure 3.5 Alternative Sign Plus Magnitude D/A Converter

Figure 3.5 shows an alternative circuit for sign plus magnitude coding. This circuit does not require positive and negative reference voltages, but it does require an additional output op amp. Two point calibration is made by first adjusting R3 until the output has equal magnitude for positive and negative full scale and then R1 is adjusted to give the correct full scale. In any system using more than one DAC the circuit of Figure 3.4 is to be preferred since the input buffer op amp A2 minimizes loading on the reference source and the circuit requires fewer components. The input resistance of CMOS DACs (typically 10 kilohms) is quite low—where many DACs are used, they can easily overload the reference source.

3.5 SINGLE SUPPLY DAC WITH OFFSET SCALE

One solution to the design of D/A converters with an offset scale is shown in Figure 3.6. The DAC is operated in the conventional current-steering mode but with OUT2 (and hence OUT1) biased positive by an

amount V_{BIAS}. For this circuit to operate correctly, the ladder termination resistor must be connected to OUT2. The output voltage is given by:

$$V_{OUT} = \left\{D \cdot \frac{R_{FB}}{RDAC} \cdot (V_{BIAS} - V_{IN})\right\} + V_{BIAS}$$

Thus from D = 0 to D = $1-2^{-n}$ the output voltage varies from $V_{OUT} = V_{BIAS}$ to approximately $2V_{BIAS} - V_{IN}$.

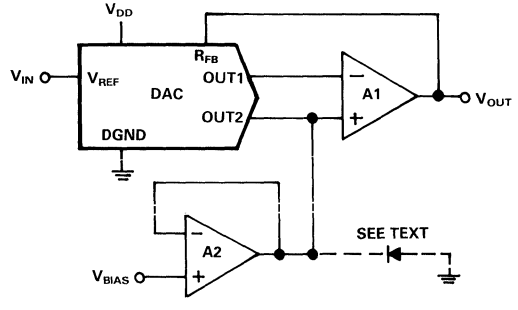


Figure 3.6 Single Supply D/A Converter with Scale Offset from Zero (Current-Steering)

This circuit is useful in that it operates from a single supply voltage with V_{BIAS} positive. It also maintains the full multiplying capability of the DAC. V_{IN} can go outside the supply rails without damaging the circuit. V_{BIAS} should be a low impedance source capable of sinking (or sourcing) all possible variations in current at the OUT2 terminal without any problems. Other schemes for operating CMOS DACs from a single supply voltage are discussed in Chapter 4. If this circuit is used with dual power supplies, positive and negative, it is possible that on power-up the op amp supplying V_{BIAS} may exhibit a transient negative voltage at its output, possibly creating heavy currents which might damage the circuit. To protect against this, include a diode as shown dotted in Figure 3.6. Practical circuits using this method are given in Figures 6.2.4. and 6.5.9.

3.6 CHANGING THE GAIN OF CMOS DACs[4]

Sometimes the DAC output voltage range is required to be greater than V_{IN}. For example, a DAC may be required to operate with a system reference of −5V, but deliver a 0 to +10V output (i.e., gain of −2). The gain could be achieved in an external amplifier stage. It can also be achieved in a single stage. However, in situations such as this, it is important to study the effect of the temperature coefficients of the thin-film resistors that are used to make up the DAC.

At first sight, the gain of a CMOS DAC could be increased by adding a resistor, R2, in series with the feedback resistor, or it could be reduced by adding a resistor R1 in series with V_{REF} as shown in Figure 3.7. This is the method used to trim out gain error as described in Section 3-1. However, for significant changes in gain, R1 or R2 will be large relative to the DAC resistors and the temperature coefficients of R1 and R2 are unlikely to match the resistor temperature coefficient of the DAC (typically—300ppm/°C). As a result, the circuit displays a very large gain temperature coefficient. To overcome this problem, the circuit of Figure 3.8 is recommended where gains greater than 1 are required. R1, R2 and R3 should all have similar temperature coefficients but they need not match the temperature coefficient of the DAC. Gain is best adjusted by varying the attenuator ratio, as adjustment sensitivity is almost unaffected by R3.

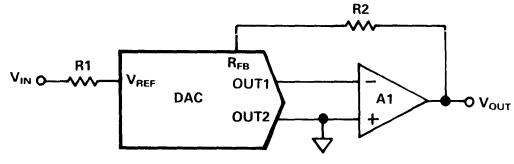


Figure 3.7 Wrong Method of Changing Gain of Current-Steering D/A Converter

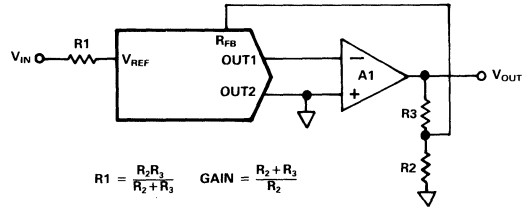


Figure 3.8 Correct Method of Increasing Gain of Current-Steering D/A Converter

3.7 VOLTAGE REFERENCES

Most references are specified with a given temperature coefficient in terms of ppm/°C. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1LSB over the temperature range 0-50°C dictates that the maximum *system* drift with temperature should be less than 78ppm/°C. A 12-bit system for the same temperature range requires a maximum drift of 5ppm/°C and if the temperature range is increased to −55°C to +125°C then the maximum tolerable system drift is 1.4ppm/°C. These figures apply for a total change of 1LSB from the minimum

to maximum temperature. In practice, the maximum permissible drift with temperature is often stated for temperature variations about an ambient temperature of 25°C and the maximum change with temperature may then be relaxed accordingly.

The lowest cost reference circuits are temperature compensated zeners, and bandgap references which synthesize a reference voltage based on the bandgap voltage of silicon (1.23V). Bandgap references such as AD589 are low cost but their output voltage usually has to be buffered to the appropriate level. It is important to consider the offset voltage drift of the op amp when using a buffer amplifier. A drift trimmed op amp, such as AD547, which has been manufactured, trimmed and tested for low drift and offset should be used for the buffer op amp. Alternatively, use a buffered bandgap reference such as the AD584. It is trimmed at the wafer stage to deliver 2.5V, 5V, 7.5V or 10V outputs.

Temperature compensated zeners offer an alternative method of generating a reference voltage. Generally, the reference zener is constructed as a sub-surface zener so that it has lower noise and better stability than the conventional surface zener. The typical temperature drift of a zener is 30 to 50ppm/°C with selections down to 10ppm/°C. Zener references can be further improved, either by incorporating them with an on-chip heater, which keeps the reference temperature constant or by utilizing them in a trimmed hybrid circuit which corrects for second order errors and allows drifts down to 1ppm/°C to be achieved. The on-chip heater method of stabilizing the reference voltage is used in the LM399 family. It is an effective way of protecting against temperature drift but consumes about 20mA of current. The output voltage of the LM399 is nominally 6.95 volts and usually requires an output buffer amp. The AD2710 series of references also use buried zener references but their temperature stability of 1ppm/°C is achieved by the use of active circuitry and active laser trimming. They deliver 10 volt outputs without the requirement for an external buffer amplifier.

For high resolution applications (14 bits and above), the user is cautioned to study the output noise characteristics of the circuit reference since reference noise can contribute significant errors. Buried zener type references usually have lower noise than bandgap references.

CHAPTER 4

SINGLE SUPPLY OPERATION FOR CMOS DACs USING THE VOLTAGE-SWITCHING MODE

4.1 SINGLE SUPPLY UNIPOLAR DAC

CMOS DACs are traditionally used in a current-steering mode. The current in the R-2R ladder is steered either to OUT2 or to OUT1, both of which are at ground potential. D/A converters can also be realized by connecting the DAC, as shown in Figure 4.1. This mode of operation is known as voltage-switching. It is particularly useful where single supply operation is required for CMOS DACs. Figure 4.2 shows a CMOS D/A converter operated in the voltage-switching mode. The reference voltage V_{IN} is applied to OUT1, OUT2 is connected to AGND, and the output voltage is available at the V_{REF} terminal. This book indicates the voltage-switching mode

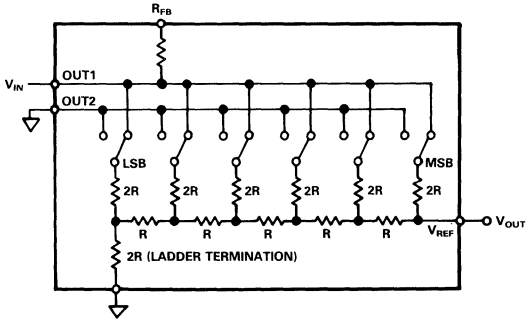


Figure 4.1 Voltage-Switching DAC Using R-2R Ladder

of operation by drawing the DAC symbol as a simple rectangle as shown in Figure 4.2. There are several points to note about this mode of operation:

a) A positive reference voltage gives a positive output voltage—hence, single supply operation is possible.

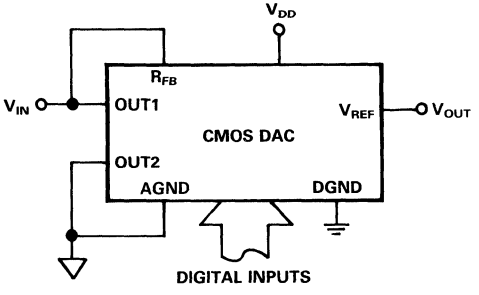


Figure 4.2 Single Supply D/A Converter Using Voltage-Switching Mode

b) The output is a voltage (not a current) at a constant impedance equal to the ladder resistance.

c) The reference voltage input (V_{IN}) no longer sees a constant input impedance, but one which varies with code. Hence, buffering the V_{IN} source is an absolute necessity.

d) V_{IN} is limited to low voltages (about 2.5V max. for $V_{DD} = +15V$) because the switches in the DAC no longer have the same source-drain voltages. As a result their on-resistance differs. This degrades the integral linearity of the DAC.

e) Output spikes due to digital to analog glitch impulses (2.3.7) in the DAC are reduced. Both switched nodes OUT1 and OUT2, are connected to low impedance points V_{IN} and AGND, and parasitic capacitances are charged from these two points.

f) The circuit has no significant gain error drift as long as the current load at the DAC output is small (i.e., use output buffer amplifier).

g) The feedback resistor R_{FB} is not required in the circuit. To minimize stray capacitance effects, tie R_{FB} to OUT1, or use it as a bias resistor for the reference circuit.

In the voltage-switching mode, the full-range multiplying capability of the CMOS DAC is lost. V_{IN} must not go more than 0.3 volts negative with respect to OUT2 or an internal diode will turn on and a heavy current may flow which will damage the device. Furthermore, the maximum permissible value of V_{IN} without substantial degradation of accuracy is determined by several factors. Figures 4.3 and 4.4 show the effect of variation of V_{DD} and V_{IN} for the AD7240, a 12-bit D/A converter designed and specified for use in the voltage-switching mode. In general, a 12-bit DAC requires a greater difference between V_{DD} and V_{IN} (max) than an 8-bit DAC does in order to preserve linearity.

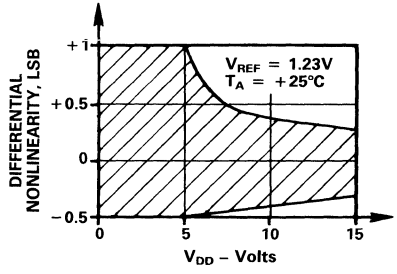


Figure 4.3 Differential Nonlinearity vs. V_{DD} (Shaded Area Shows Typical Range of DNL vs. Supply Voltage)

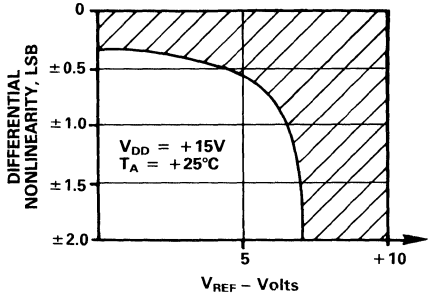


Figure 4.4 Differential Nonlinearity vs. Reference Voltage (Shaded Area Shows Range of Values of DNL That Typical Occur for K and J Grades)

4.2 SINGLE SUPPLY DAC WITH OFFSET SCALE (VOLTAGE-SWITCHING)

In some applications (for example in 4-20mA circuits) a DAC is required to have zero code input correspond to an output value other than zero, i.e., a zero code point offset from ground. This can be achieved by the voltage-switching circuit of Figure 4.5. OUT2 is driven by the lower offset voltage, and OUT1 is driven by the full scale output voltage. If the ladder termination resistor is connected to AGND, then the output voltage for digital input code D is given by:

$$V_{OUT} = D\cdot(V1-V2) + (1-2^{-n})\cdot V2$$

when D = 0, $V_{OUT} = V2\cdot(1-2^{-n})$

when D = $1-2^{-n}$, $V_{OUT} = V1$

If the ladder termination resistor is connected to OUT2, the output voltage is given by:

$$V_{OUT} = D\cdot(V1-V2) + V2$$

when D = 0, $V_{OUT} = V2$

when D = $1-2^{-n}$, $V_{OUT} = V1\cdot(1-2^{-n}) + 2^{-n}\cdot V2$

Thus the end points are V2 and approximately V1. Note that the connection of the ladder termination resistor has a slight dc effect on the transfer function. Practical realizations of the circuit of Figure 4.5 require that DGND and OUT2 be available as separate pins on the D/A converter. The outputs of amplifiers A1 and A2 should never go negative with respect to OUT2 or parasitic transistor action may damage the DAC. Usually A1 and A2 are operated on the same single supply (V_{DD}) as the DAC.

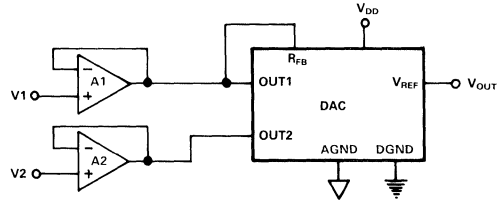


Figure 4.5 Single Supply D/A Converter with Scale Offset from Zero (Voltage-Switching)

4.3 OP AMPS FOR VOLTAGE-SWITCHING DAC CIRCUITS

The output op amp for a voltage-switching DAC circuit buffers the output of the DAC and usually provides some gain, since the input reference voltage, V_{IN}, is usually smaller than the required output voltage span. The output voltage for the circuit of Figure 4.6 is given by:

$$V_{OUT} = D \cdot V_{IN} \cdot G \cdot \frac{1}{1+\frac{G}{A}}$$

$$\text{where } G = \frac{R1+R2}{R1}$$

the nominal gain of the output buffer amplifier. The error due to finite op amp gain A is approximately given by:

$$\text{Absolute Full Scale Error} \approx \frac{-G^2}{A}$$

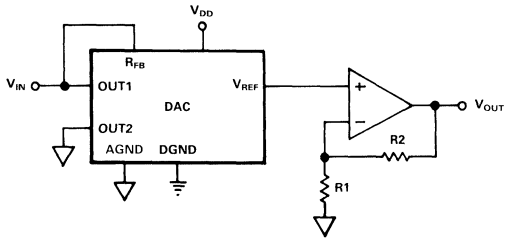


Figure 4.6 Voltage-Switching D/A Converter

Such errors are primarily gain errors which may be corrected by minor gain adjustment. In many voltage-switching circuits, it is convenient to operate with V_{IN} = 1.23V (a low-cost bandgap reference such as AD589) and G = 8.13 for a 0 to 10V output range from the DAC. The input bias current and the input offset voltage of the op amp produce an offset at the voltage output. However, unlike the current-steering circuit, these two parameters are not code dependent and do not affect DAC linearity because the voltage-switching DAC has a constant output impedance.

The common-mode rejection of the op amp is important in voltage-switching circuits, since it produces a code dependent error at the voltage output of the circuit. Unfortunately, most manufacturers do not specify common-mode performance very well because it is a difficult parameter to define and measure. Most op amps have adequate common-mode rejection for use at 8- and 10-bit resolution but for 12 bits the required performance can outstrip that of some popular op amps. For example, a common-mode rejection ratio of 85dB at 1V input is often quoted as an op amp's performance; it results in an error of 0.23LSB for 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew-rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

4.4 OP AMP INPUT STAGES FOR SINGLE SUPPLY

Most single-supply circuits include ground as part of the analog signal range, which in turn requires that the op amps common-mode input range should include its "negative supply". This restricts the available op amps to those that use either PNP transistors, PMOS devices or N-channel JFET's for the input differential pair.

The choice of single supply op amps currently available is quite small. Typical devices are the LM324 PNP input bipolar quad op amp, the CA3130 PMOS input BIMOS op amp family and the TL091 NFET family. The input stage determines most of the op amp's input characteristics. Bipolar inputs have the lowest untrimmed input offset voltage; PMOS inputs have the highest input impedance but also the highest offset voltage while JFETs usually provide the lowest noise.

The output stage of an op amp determines the maximum output voltage swing. CMOS outputs such as those used in the CA3130 can swing to both supply rails unloaded, although their output resistance is fairly high. The output swing available from bipolar output stages such as that used on the LM324 is typically from the negative supply rail (ground) to within 1.5V of the positive supply rail. The current sink capability of the LM324's output stage when V_{OUT} is close to ground is limited but it can be improved by connecting a shunt resistor from V_{OUT} to ground (see Figure 4.7). A more recent bipolar op amp design, the LM10 allows the output to swing to within 15mV of either supply rail. Figure 4.8 shows the performance of the LM10, TL091, LM324 and CA3130 under various load conditions, when operated on a single +5V supply. Be aware of the fact that at low supply voltages op amp settling time and slew rate are seriously impaired.

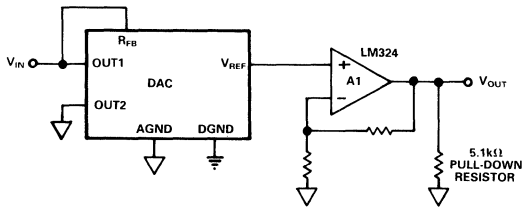


Figure 4.7 Method of Improving LM324 Output Drive Near Ground

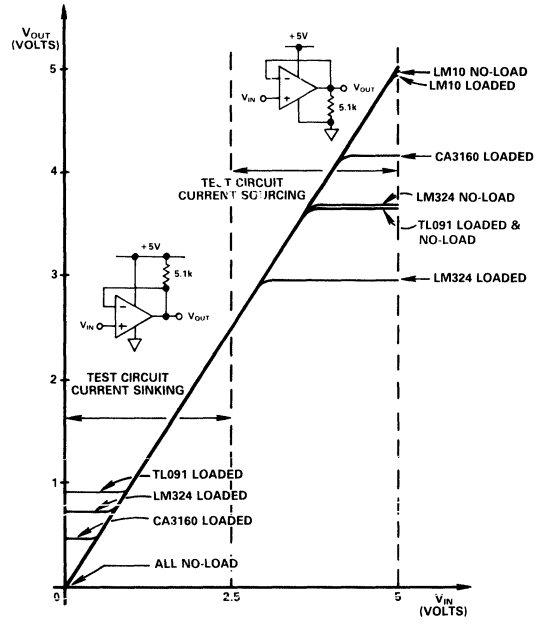


Figure 4.8 Single-Supply Op Amp Performance $V_{CC}+5V$

CHAPTER 5

THE LOGIC INTERFACE

5.1 LEVEL SHIFTERS

Most CMOS DACs include a TTL to CMOS level shifter at each digital input to translate the external TTL input logic levels to the internal CMOS logic levels used in the DAC. There are two basic types of level shifter. One gives TTL compatibility only when the supply voltage V_{DD} is +5V—for other values of V_{DD} it is CMOS compatible but not TTL compatible. A second type gives CMOS and TTL compatibility for all permissible supply voltages. Appendix 1 summarizes these features for Analog Devices' DACs.

The supply current (I_{DD}) drawn by a DAC is chiefly determined by the input logic levels. Figure 5.1 shows the variation in I_{DD} as a single digital input is swept from 0V to +5V. The voltage at which the current peak occurs varies from DAC to DAC but it is clear that to minimize I_{DD} the input logic levels should be as close to the 0 and +5 volt supply rails as is practical. Pull-up resistors at the digital inputs can often help to reduce DAC power consumption.

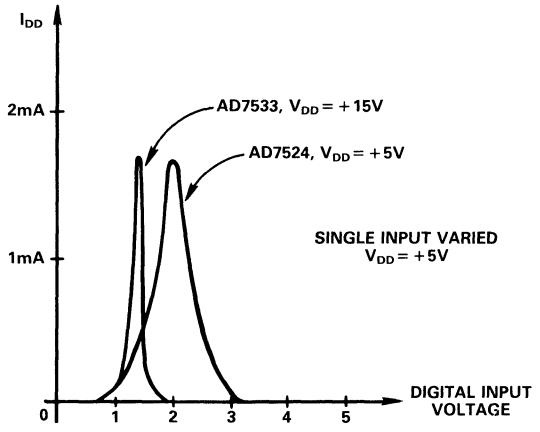


Figure 5.1 Typical I_{DD} vs. Digital Input Voltage

5.2 MICROPROCESSOR COMPATIBLE DACs

A "Microprocessor Compatible DAC" includes one or more sets of registers to hold the digital value to be applied to the DAC. The simplest microprocessor compatible DACs incorporate a single register which is loaded in parallel from the data bus under the control of the $\overline{CS}$ (chip select) and $\overline{WR}$ (write) pins. This scheme is used for the AD7524, AD7528 and AD7545 shown in Figures 5.2, 5.3 and 5.4 respectively. When $\overline{CS}$ and $\overline{WR}$ are both low, the DAC register is transparent and information on the data bus passes directly to the DAC inputs. *If the data bus changes during this time, the inputs to the DAC will change and "noise glitches" may appear on the output.* The data from the bus is latched when $\overline{CS}$ or $\overline{WR}$ goes high. The AD7528 contains two DACs and only

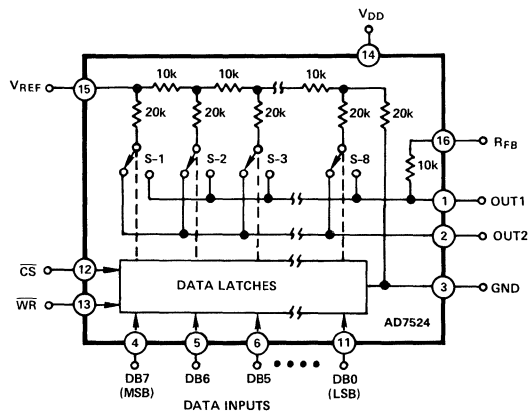


Figure 5.2 AD7524 8-Bit DAC – 16-Pin DIP

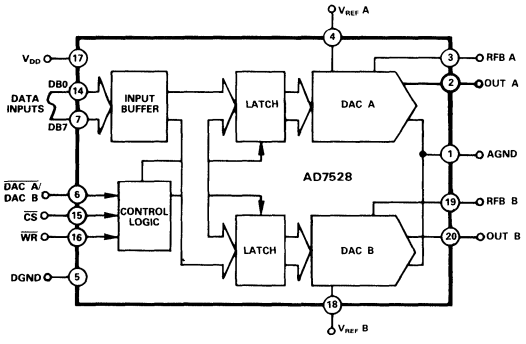


Figure 5.3 AD7528 – Dual 8-Bit DAC – 20-Pin DIP

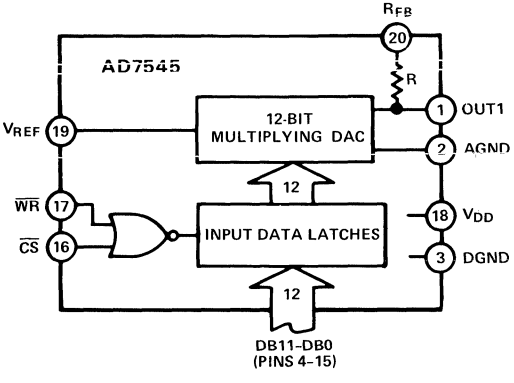


Figure 5.4 AD7545 12-Bit DAC – 20-Pin DIP

the latches associated with the addressed latch are transparent when $\overline{CS}$ and $\overline{WR}$ are low.

In many applications the system bus width is insufficient to load the full data word to the DAC in a single byte; and the data word is therefore transmitted to the DAC in two or more bytes. Additional registers are used on-chip to reassemble the bytes into the full parallel word before it is presented to the DAC. The AD7542, AD7543 and AD7548 shown in Figures 5.5 through 5.7 all incorporate a two register arrangement known as double buffering. The AD7548 (12-bits) is designed to be loaded in 8-bit bytes and is therefore suitable for most 8-bit bus systems including those of the 8088 and 68008 16-bit microprocessors. The AD7542 is loaded by three 4-bit nibbles and can connect directly to the 4-bit expansion port of MCS48 series of microprocessors. The AD7543 is loaded serially. Since multiple byte input to a DAC requires fewer digital input pins than a full parallel input the "free" pins on the dual-in-line package are used to provide features such as additional chip select pins, internal register reset, etc. The list below sum-

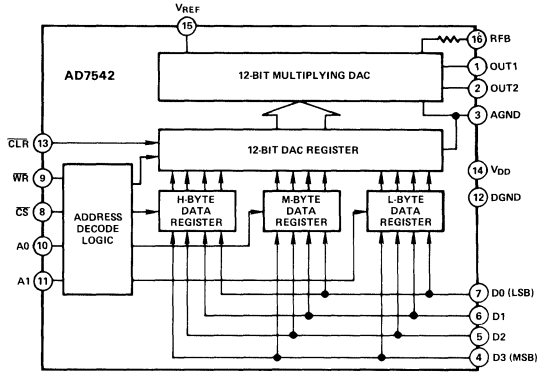


Figure 5.5 AD7542 12-Bit DAC – 16-Pin DIP

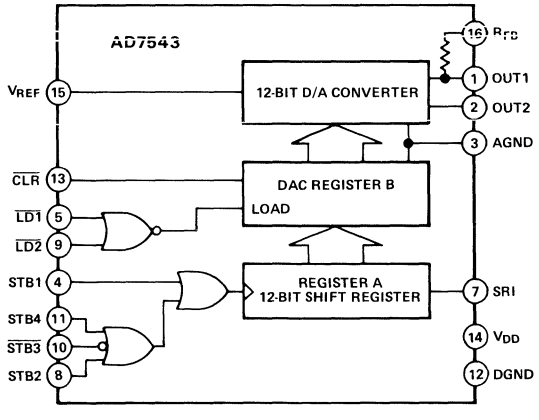


Figure 5.6 AD7543 12-Bit DAC – 16-Pin DIP

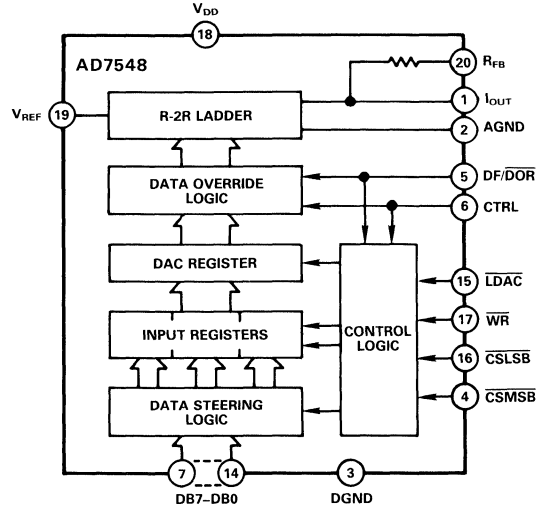


Figure 5.7 AD7548 12-Bit DAC – 20-Pin DIP

marizes various logic features available in the AD7XXX line of microprocessor compatible DACS.

DAC register reset (AD7542, AD7543) sets the contents of the register equal to zero. This is useful in power-up situations requiring the DAC have zero output at switch-on.

Additional chip select pins having a chip-select function found on the AD7542 and AD7543 simplify address decoding.

Pin selectable input format is available on the AD7548. Data to the DAC may be either left-hand justified (8+4) or right-hand justified (4+8). Pin straps are used to appropriately steer the input bytes to the DAC register.

Data override (AD7548) is used to force the digital input word to the DAC to a given code regardless of the contents of the DAC registers. The AD7548 can be forced to zero and full scale. This feature is useful for power-up situations, but more importantly for assisting system calibration because the DAC outputs can be set to known states without having to rely on the host processor to deliver the appropriate codes via special calibration routines.

5.3 PRACTICAL INTERFACE DESIGN

5.3.1 Data and Address Bus Connections

A TTL logic transition can couple a 30mV noise spike from a single pin across an empty integrated circuit package. It is, therefore, important to design digital-to-analog interface circuits which minimize the amount of noise injected from the high speed digital system into the precision analog circuits. It is good practice to disable all logic signals to the DAC when it is not being addressed. Figure 5.8 shows the general principles involved. The data bus, $\overline{CS}$ and $\overline{WR}$ are held to "1" until the DAC address appears on the address bus. The data inputs are then enabled and $\overline{CS}$ and $\overline{WR}$ go low at the appropriate time to strobe the data into the DAC. The introduction of the additional gates between the DAC and the microprocessor changes the relative timing of the microprocessor signals and any practical design must take account of this. Programmable logic arrays such as PAL 16L8A are a useful way to reduce the delays and the number of I.C. packages required to buffer the data bus.

Three state buffers should not be used without pull-up resistors in place of the data bus gates. This is because a high impedance indeterminate state at the buffer outputs will significantly increase the power

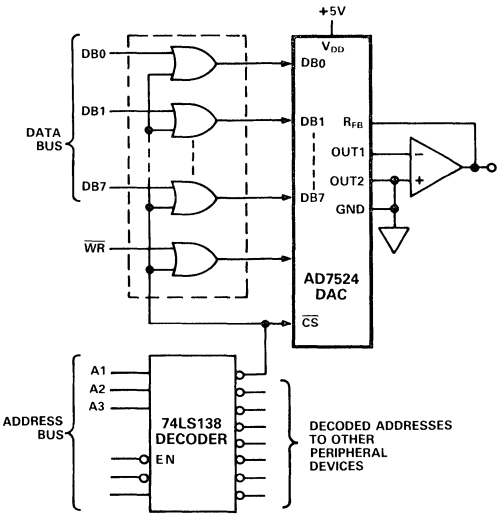


Figure 5.8 General Method of Interfacing DACs to μP Buses

supply current to the DAC (see Section 5.1), and may cause malfunction. The $\overline{CS}$ and $\overline{WR}$ signals should only go low when the DAC is addressed—if possible, do not directly connect the microprocessor write signal to the $\overline{WR}$ pin of the DAC because this signal is continuously active and will therefore create noise at the output of the DAC. Section 6.9 gives some practical circuits for connecting CMOS DACs to microprocessors.

5.3.2 Power Supply, Ground Connections and Circuit Board Layout

CMOS DACs have several important features which directly affect the design of power supply connections, circuit board layout, and other interconnection paths. These include:

a) OUT1 and OUT2 must be at the same potential. For this reason signal paths from OUT1 and OUT2 to the op amp should not be used to carry other currents (for example ground currents in the OUT2 line).

b) Noise on AGND produces noise at the DAC output (see Section 2.2) consequently AGND should be a "quiet" connection.

c) Power supply noise produces noise at the DAC output (see Section 2.3.3 on power supply rejection). DAC power supplies should be decoupled and have a separate connection to the power supply line. DACs operating with V_{DD} = +5V should preferably have a completely separate +5V regulator.

d) If separate DGND and AGND connections are used, caution must be exercised to prevent excessive voltage differences between the two from occuring during power-up or when plugging-in or removing boards. Normally a pair of IN914 diodes connected in inverse parallel between DGND and AGND can be used to prevent this from happening.

Figure 5.9 shows a typical circuit board layout for the AD7545 12-bit D/A converter with an AD542 output amplifier. The board layout has been spread out a little to show both sides of the board more clearly. Dotted lines are for the underside of the board and full lines for the component side. The connection from the positive input of the op amp (pin 3) is routed first to the AGND (and OUT2) of the DAC (pin 2) and then to the AGND bus line. AGND is also used to form an unclosed guard ring around the OUT1 to the op amp negative input. This guard ring prevents unwanted leakage currents from reaching the OUT1 connection. By leaving the ring incomplete the OUT2 to op amp connection is unaffected. All the ground and supply lines run parallel to one another as shown and should be as broad as is practically possible. In addition to the heavy DGND line, a second finer DGND line threads between pins 18 and 19 as shown to screen the analog section from the digital section of the circuit.

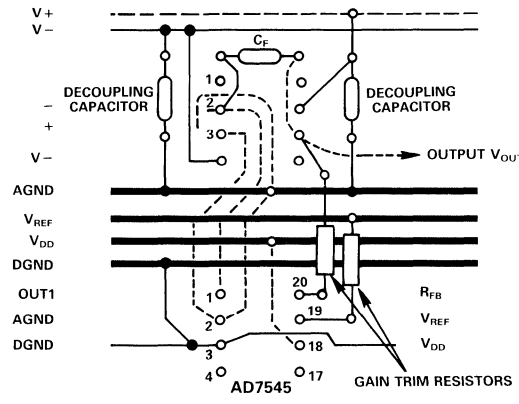


Figure 5.9 Typical Circuit Board Layout for CMOS DAC (AD7545) and Output of Op Amp – Component Side

This screen ties down any stray capacitances and helps minimize digital-analog feedthrough and glitches.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using D/A converters does not allow such a film to form.

CHAPTER 6

APPLICATIONS

6.1 BASIC APPLICATIONS CIRCUITS

6.1.1 DAC as a Multiplier and Attenuator

It was pointed out in Section 1.3 that, in the current-steering mode, the CMOS DAC multiplies the digital input value by the analog input voltage at V_{REF} for any value of V_{REF} up to ±25 volts. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion must consider the CMOS DAC as a candidate. CMOS DACs are widely used as audio frequency attenuators. The audio signal is applied to the V_{REF} input and the attenuation code is applied to the DAC; the output voltage is the product of the two—an attenuated version of the input.

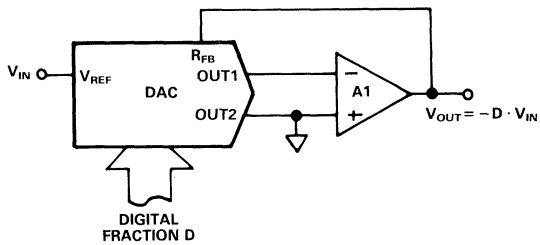


Figure 6.1.1 CMOS DAC as Multiplier or Attenuator

Conventional DACs provide a limited range of attenuation which is linear with code: an 8-bit DAC has a maximum attenuation range of 256:1 or 48dB, a 12-bit DAC gives 4096:1 or 72dB. To simplify the application of CMOS DACs as audio attenuators with logarithmic gain adjustment, three special purpose LOGDACs are available which are coded to give attenuation in equal decibel steps. See Section 6.8.

6.1.2 DAC as a Divider or Programmable Gain Element

If a CMOS DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor, as shown in Figure 6.1.2, then the output voltage is inversely proportional to the digital input fraction D. For $D = 1-2^{-n}$ the output voltage is

$$V_{OUT} = -\frac{V_{IN}}{D} = -\frac{V_{IN}}{(1-2^{-n})}$$

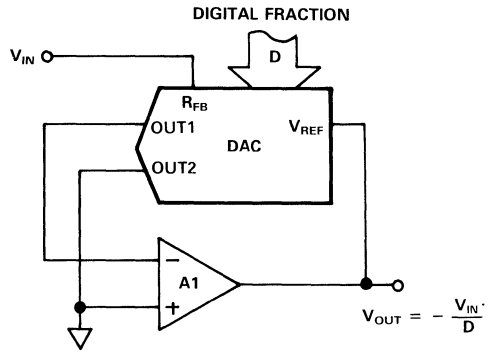


Figure 6.1.2 CMOS DAC as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an eight bit DAC driven with the binary code 10H (00010000), i.e., 16 decimal, in the circuit of Figure 6.1.2 should cause the output voltage to be sixteen times V_{IN}. However, if the DAC has a linearity specification of ± 1/2LSB then D can in fact have the weight anywhere in the range 15.5/256 to 16.5/256,

so that the possible output voltage will be in the range $15.5V_{IN}$ to $16.5V_{IN}$—an error of ±3% even though the DAC itself has a maximum error of 0.2%. The possible error in gain due to an E% linearity error in the DAC is approximately given by:

$$\text{Divider Gain Error} = \pm\frac{E}{D}\ \%$$

It can be seen that a programmable gain circuit with a gain of 16 specified to a maximum error of 1% requires a DAC with 0.06% absolute accuracy—i.e., an 11-bit DAC with ±3/4LSB linearity (AD7545KN would suffice).

DAC leakage current is also a potential error source in the divider circuit. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction D of the current into the V_{REF} terminal is routed to the OUT1 terminal, the output voltage has to change as follows:

$$\text{Output Error Voltage Due to DAC Leakage} = \frac{\text{Ilkg}\cdot R}{D}$$

where R is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10nA, R = 10 kilohm and a gain (i.e., 1/D) of 16 the error voltage is 1.6mV. DAC leakage currents are normally less than 10nA up to 70°C.

6.1.3 Programmable Integrator Circuit

The circuit of Figure 6.1.3 shows a DAC connected as a programmable integrator. The output voltage is given by:

$$V_{OUT} = -\frac{1}{CR}\cdot D\int V_{IN}\ dt.$$

The integrator time constant is shortest when the DAC is at full scale and longest when the DAC is set to near zero code. The feedback resistor R_{FB} is not used in the integrator circuit and it is recommended that R_{FB} be tied to OUT1. The time constant of the integrator is proportional to C and R, the resistance of the DAC. It is normal to include a variable resistor R1 in series with the DAC to allow the full scale time constant to be trimmed to the appropriate value.

The temperature coefficients of the DAC, trim resistor and capacitor are unlikely to match so that the integrator time constant will vary somewhat with temperature. The dependance on the DAC resistance and its temperature coefficient can be removed by using the circuit of Figure 6.1.4 but the temperature coefficients of C and R1 remain critical for applications with wide temperature variations. Programmable integrators form the basis of a number of medium frequency function generators and graphics circuits—see Section 6.6.

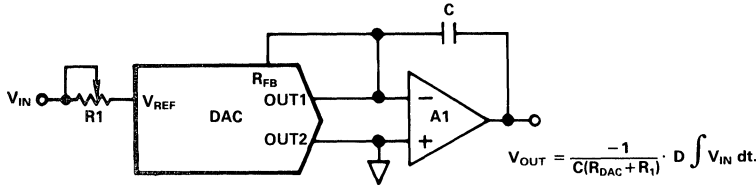


Figure 6.1.3 Programmable Integrator (Inverting)

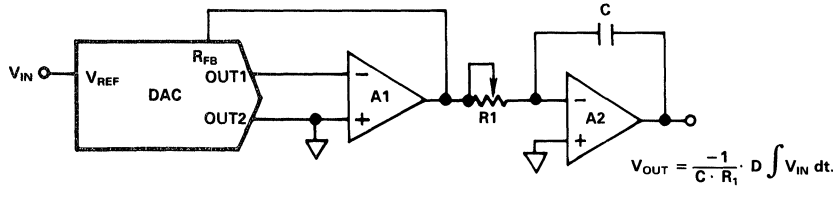
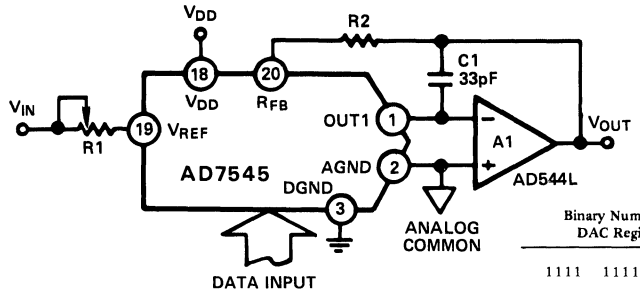


Figure 6.1.4 Programmable Integrator (Noninverting)

6.2 D/A CONVERTERS AND PROGRAMMABLE POWER SUPPLIES

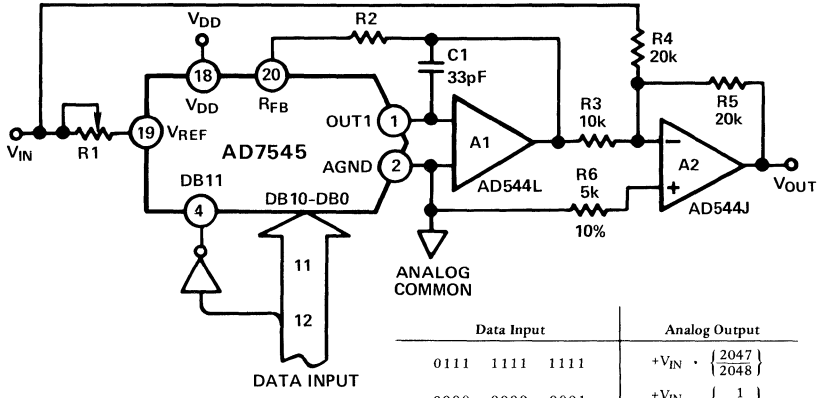
Figures 6.2.1, 6.2.2 and 6.2.3 show conventional circuits for using CMOS DACs. This type of circuit has been discussed at length in the text.



TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

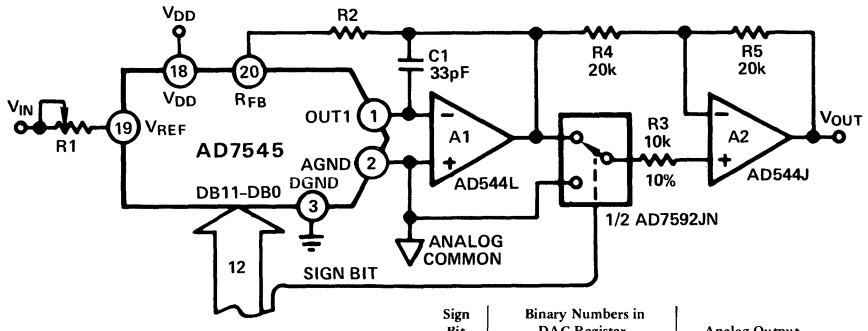
Binary Number in DAC Register	Analog Output
1111 1111 1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000 0000 0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000 0000 0000	0 Volts

Figure 6.2.1 Low Cost 12-Bit Unipolar D/A Converter



Data Input	Analog Output
0111 1111 1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000 0000 0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000 0000 0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Figure 6.2.2 12-Bit Bipolar D/A Converter (2's Complement)



Sign Bit	Binary Numbers in DAC Register	Analog Output
0	1111 1111 1111	$+V_{IN} \cdot \{\frac{4095}{4096}\}$
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	$-V_{IN} \cdot \{\frac{4095}{4096}\}$

Note: Sign bit of "0" connects R3 to GND.

Figure 6.2.3 12-Bit Plus Sign/D/A Converter

6.2.1 D/A Converter with Minimal Leakage Current

Figure 6.2.4 shows the AD7545 operated in the single-supply current-steering mode described in section 3.6. This type of circuit will operate correctly only when the ladder termination resistor is connected to OUT2/AGND as is the case for the AD7545. The P-well for the DAC switches is connected to DGND so that the P-well to N-channel switch diode (see Figure 2.2) is reverse biased by V_{IN}. This reverse bias minimizes leakage currents flowing from the P-well to the switches; it also drives the off-switch hard off due to the body-effect of the P-well (i.e., the well behaves like a second gate), which in turn reduces off-switch leakage. If V_{IN} is in the range 0 to +5V, the DAC linearity does not suffer unduly from the reverse bias of the P-well and 12-bit linearity is maintained up to quite high temperatures, with exceptionally low leakage currents. Certain aspects of this circuit design are the subject of a patent application.

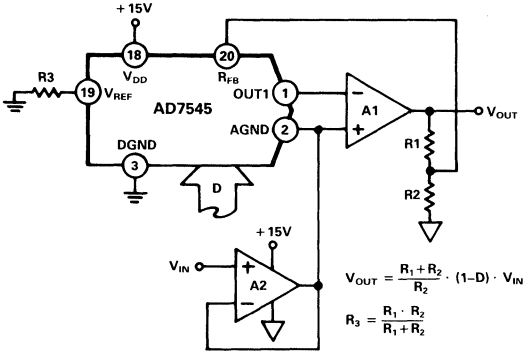


Figure 6.2.4 12-Bit D/A Converter for High Temperature Operation

6.2.2 Dual 8-Bit DAC—Single +5V Supply

Figure 6.2.5 gives the circuit for a low cost dual 8-bit DAC operating from a single +5V. This circuit is an effective way to provide a personal computer with two analog output channels to drive chart recorders, X-Y plotters etc. Care should be taken to minimize logic noise on the +5V and DGND lines to the D/A converter. A simple filter comprising R3, C1 and the ferrite bead cut down any noise. The circuit operates the two DACs in the voltage-switching mode with a +0.6V reference derived from an AD589 1.23V bandgap reference. The output voltage covers the range 0 to 2.54 volts in 10mV steps. If possible, gate the digital inputs as recommended in 5.3.1 (i.e., the DAC inputs are only active when the DAC is addressed). This helps minimize digital feedthrough spikes.

6.2.3 Low Cost 14-Bit Resolution D/A Converter

If the DAC can be calibrated to a voltmeter, then the circuit of Figure 6.2.6 may be used. The two eight-bit DACs are connected so that the reference voltage of DAC A is roughly 1/64 the reference voltage of DAC B. Resistor R2 should be less than one fifth the value of the DAC resistance. This minimizes the effect of changes in RDAC from one device to another.

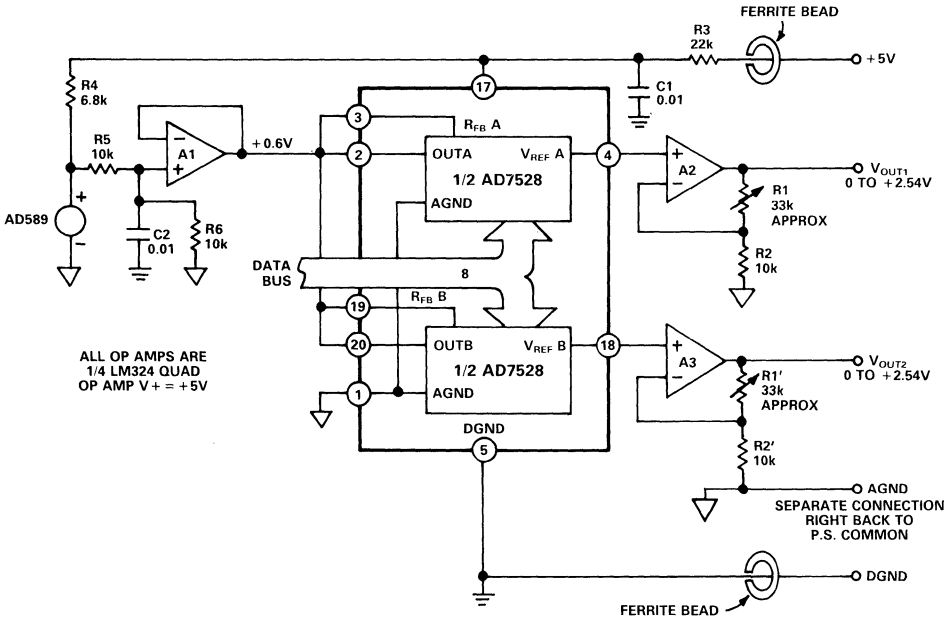


Figure 6.2.5 Dual DAC – Single 5V Supply

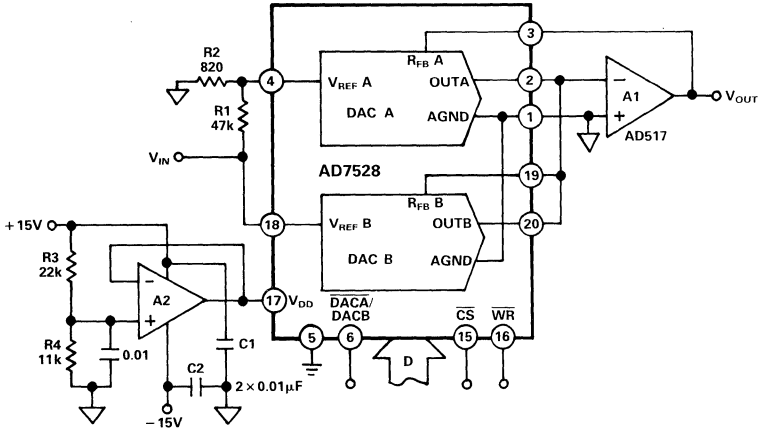


Figure 6.2.6 Low Cost 14-Bit Resolution D/A Converter

DAC B is used to provide a "coarse" setting of the output voltage and DAC A gives a fine adjustment upwards from DAC B setting. The total range covered by DAC A is equal to 4LSBs of the DAC B range. Clearly, DAC A and DAC B must be adjusted within a closed loop and this procedure is not always practical. Section 6.3.2 describes the application of this circuit to trim out the gain-error of a DAC.

In order to obtain satisfactory performance from this circuit, it is necessary to ensure that power lines and V_{IN} are noise free and stable. This is done by deriving the +5V for V_{DD} from the +15V via an op amp. The circuit operates satisfactorily over a wide temperature range, but it requires recalibration if the operating temperature changes because R1 and R2 temperature coefficients will not match those of the DAC. The input offset of amplifier A1 should be nulled to minimize DAC linearity errors due to amplifier input offset.

6.2.4 A 16-Bit D/A Converter[17]

Figure 6.2.7 shows the block diagram of the AD7546 16-bit resolution D/A converter (U.S. Patent No. 4338591). It consists of a 12-bit DAC, operated in the voltage-switching mode, and a tapped divider of 16 equal resistors to provide the voltages to OUT1 and OUT2 of the DAC. The 16 resistors divide the reference voltage into 16 equal segments and the voltage across a particular segment is applied to the DAC.

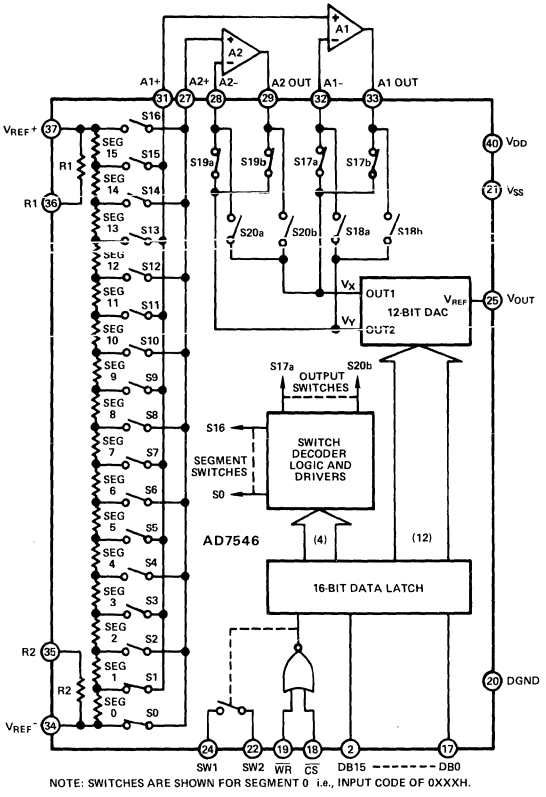


Figure 6.2.7 16-Bit D/A Converter

Since the segment voltage is only one sixteenth of the reference voltage, the potential difference between OUT1 and OUT2 is relatively small and nonlinearity errors due to unequal voltages across the NMOS DAC switches are minimized. A significant feature of the AD7546 is that it allows low cost FET input op amps to be used for the segment buffers and achieves a full 16-bit settling in 10μs. For the same resolution, an extended R-2R ladder would require op amps with excellent input offset and leakage current specifications; and it would have a much longer settling time because of the added switch capacitance at the OUT1 mode.

Since the AD7546 uses its DAC in the voltage-switching mode, it can readily be operated with a single supply. For further information on the AD7546 refer to the data sheet available from Analog Devices.

6.2.5 Simple Programmable Power Supply[6]

The circuit in Figure 6.2.8 shows a simple programmable power supply with programmable current limit. DAC A is used as a programmable voltage source and DAC B sets the current limits. R_{FB} A is not connected directly to the output but via a buffer amplifier, as shown, to eliminate any loading on the output which might cause a false value of I_{OUT}. The dual amplifier feedback of A1 and A3 oscillates with some amplifiers. The differential voltage across RS2 is amplified by A4 and fed to the feedback resistor of DAC B. The current in R_{FB} B is compared to a programmable current of opposite polarity flowing to DAC B. The net difference is applied to A2 which is connected as a "soft" comparator (Gain approx. 100). When over-current exists, the output of amplifier A1 is pulled to ground via RS1 and D1, RS1 limits the short circuit current. The output of amplifier A4 provides a useful indication of the current flowing. Figure 6.2.9 shows a similar circuit for bipolar operation,—i.e., 0 to ± 10V.

Section 6.3.5 shows how CMOS DACs can be used with the popular 723 voltage regulator to create a number of different power supply circuits.

6.3 CMOS DAC AS A CALIBRATION TRIMMER

CMOS DACs can be used to replace trim resistors in most circuits provided the designer makes allowance for this at an early stage. This approach is particularly suitable in self-calibrating type instruments; not only does it improve the instruments' performance but it also eliminates the requirement for trim resistors. This reduces production cost and test time. For example, the instrumentation amplifier shown in Figure 6.3.1 is particularly expensive to use in its basic form because it requires precisely matched resistors and two trim resistors. Additionally the calibration procedure is time consuming and can be a production line bottleneck. However, by replacing the trim-resistors with CMOS DACs the overall production cost and set-up time can be significantly reduced.

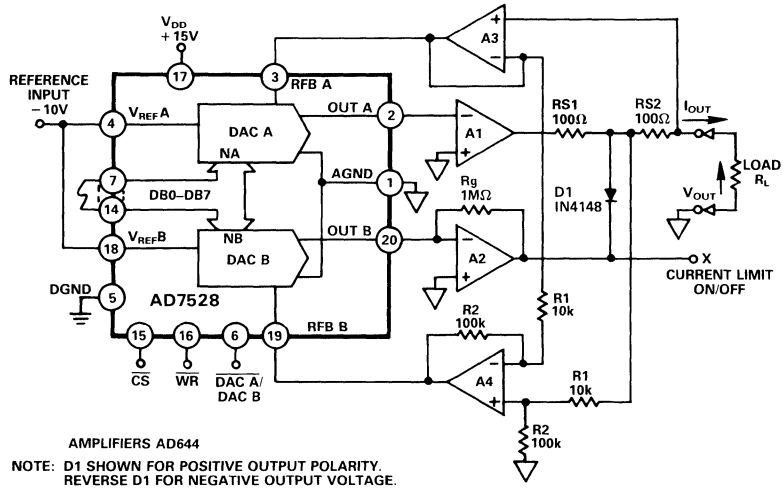


Figure 6.2.8 Programmable Voltage/Current Source V_{OUT} = 0 to +10V, I_{OUT} = 0 to +10mA

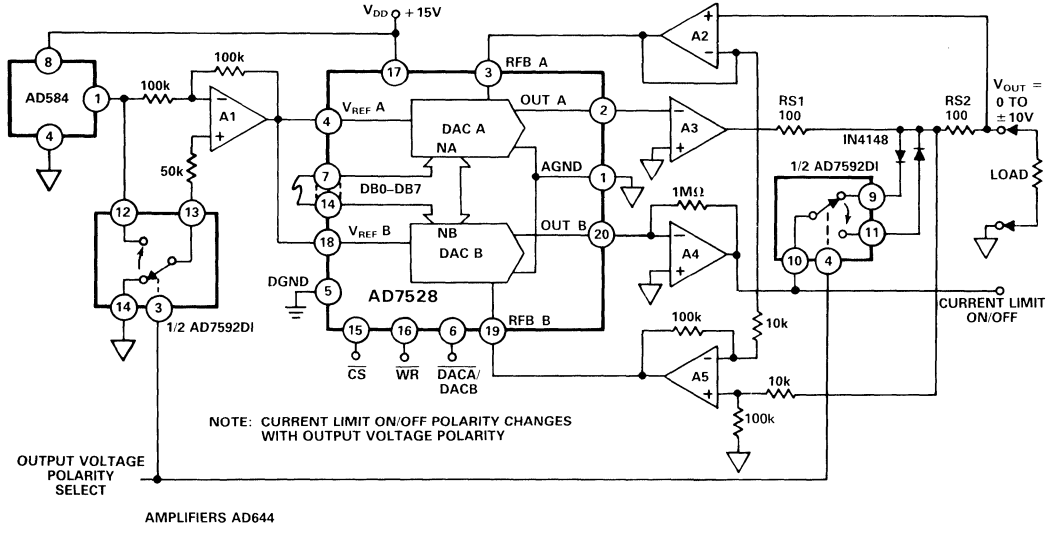
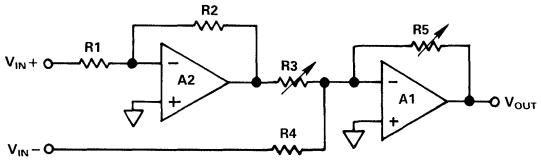


Figure 6.2.9 Programmable Voltage/Current Source with Bipolar Output



$$V_{OUT} = \frac{R_5}{R_3} \cdot \frac{R_2}{R_1} (V_{IN}+) - \frac{R_5}{R_4} (V_{IN}-)$$

Figure 6.3.1 Instrumentation Amplifier

6.3.1 Simple Potentiometer Connection

Figure 6.3.2 shows the simplest practical potentiometer connection and its equivalent circuit. The equivalent trim resistor has a maximum value equal to R3 and a minimum value approximately equal to:

$$\frac{R3}{1 + \frac{R3}{RDAC}}$$

The output voltage V_{OUT} is given by:

$$V_{OUT} = \frac{V1 \cdot R2}{R2 + \left\{\frac{RDAC \cdot R3}{RDAC + D \cdot R3}\right\}}$$

The feedback resistor of the DAC can often be used for R3, and since R3 = RDAC, the relationship simplifies to:

$$V_{OUT} = \frac{V1}{1 + \frac{RDAC}{R2} \cdot \left\{\frac{1}{1 + D}\right\}}$$

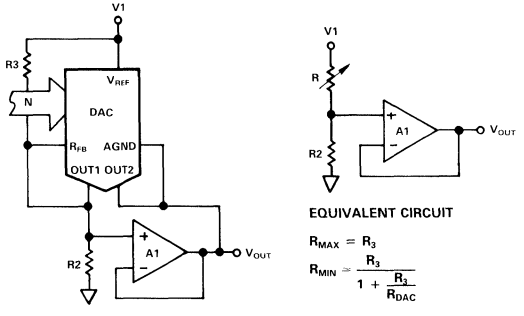


Figure 6.3.2 Simple Potentiometer Circuit

This type of circuit works provided the following constraints are observed:

i) The ladder termination resistor is connected to AGND or OUT2 (see Appendix A1).

ii) V_{DD} is at least 4V more positive than the maximum value of V_{OUT}. This is necessary to preserve DAC linearity.

iii) V1 is positive. Negative values of V1 will turn on internal diodes causing device destruction.

DAC types AD7528, AD7545, AD7240 and AD7548 are particularly suitable for this kind of application. If the AD7528 and AD7545 are operated with a V_{DD} other than +5V, their digital inputs are not TTL compatible. Note how the amplifier is used to bootstrap the potential at OUT2 to be equal to that at OUT1.

The specified resistance of the DAC generally covers quite a wide range; this results in some restriction on the application. Figure 6.3.3 shows an improvement which reduces the effect of variation in RDAC and also allows the trim to cover a narrower range with better resolution. For the equivalent circuit, the maximum value of the trim resistor is equal to R3 and the minimum value of the trim resistor is equal to R3 in parallel with (R1 + RDAC).

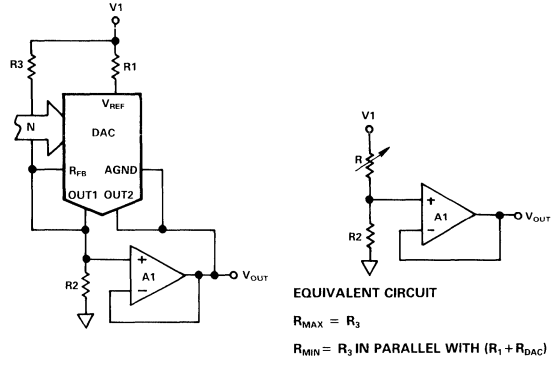


Figure 6.3.3 Potentiometer Circuit with Reduced Range and Improved Resolution

6.3.2 Dual DAC Trims Gain Error

Most CMOS DACs have a specified gain error of the order of 5% which is usually trimmed out by the use of an external trim resistor as described in Section 3.1. An alternative way of doing this is to use the AD7528 dual DAC to build a 14- bit DAC as described in Section 6.2.3. This 14-bit DAC then supplies the reference voltage to the main DAC in use. Figure 6.3.4 shows such a scheme for AD7545, although it could be used with any DAC. The AD7528 DAC combination covers a voltage range which can correct for any gain error in the AD7545. The input offset voltage of amplifier A1 must be nulled because DAC B operates with a very low value of V_{REF} and any input offset voltage may cause differential linearity errors in DAC B. To calibrate the circuit, full scale (all 1's) is applied to the AD7545 and the various codes are loaded to the AD7528 until the

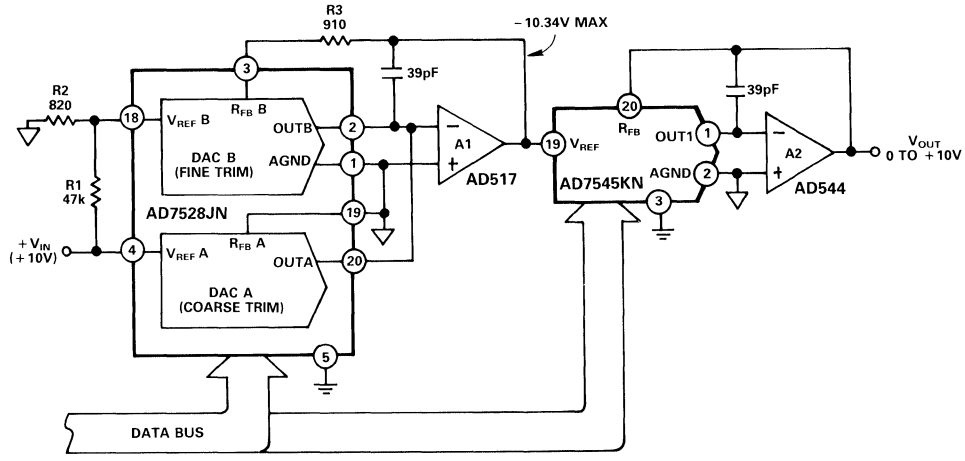


Figure 6.3.4 DAC Gain Error Trim Using AD7528 Dual DAC as Coarse/Fine Trim

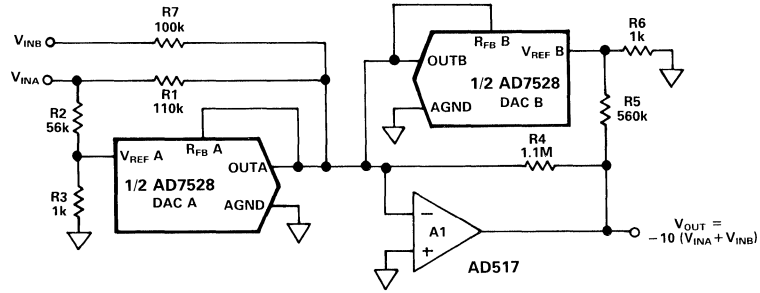


Figure 6.3.5 Precision Summing Amplifier

output voltage is correct. Once the system has been calibrated, the DAC output is determined by the AD7545; no further interaction with the AD7528 is required until the next recalibration.

6.3.3 Precision Gain Summing Amplifier

Precision gain amplifiers require the use of a trim resistor to set the appropriate gain at calibration time or entail the use of high cost precision resistors. The circuit of Figure 6.3.5 provides an alternative solution by using a dual DAC as shown. DAC A is adjusted to provide matching between the two inputs and DAC B is used to adjust the gain over a narrow range. The resistors R2, R3 and RDAC give rise to a small current in DAC A which is steered either to AGND or the amplifier summing junction. Similarly R5 and R6 feed back a small fraction of the output signal through DAC B. R3 and R6 should be about one fifth the maximum value of RDAC in order to make the circuit insensitive to different values of RDAC. For 5% resistance values, the circuit shown delivers 0.1% worst case channel to channel mismatch and 0.1% worst case gain error. Amplifier A1 should have very low input offset voltage because the two DACs operate with a low reference voltage.

6.3.4 Instrumentation Amplifier

Figure 6.3.1 shows a classic two amplifier instrumentation amplifier. It is useful in applications which have a high common-mode voltage at the inputs. Resistors R3 and R5 must be carefully trimmed to achieve good common-mode rejection and the correct gain. In a self-calibrating system, R3 and R5 are replaced by the AD7528 dual DAC circuit as shown in Figure 6.3.6. DAC A is then set by tying both inputs to the common voltage and adjusting the code to DAC A until the output is zero. DAC B code is adjusted to give the correct output for a known input voltage difference. The circuit shown will handle common-mode voltages up to 30V with a gain of 10 accurate to 0.1%.

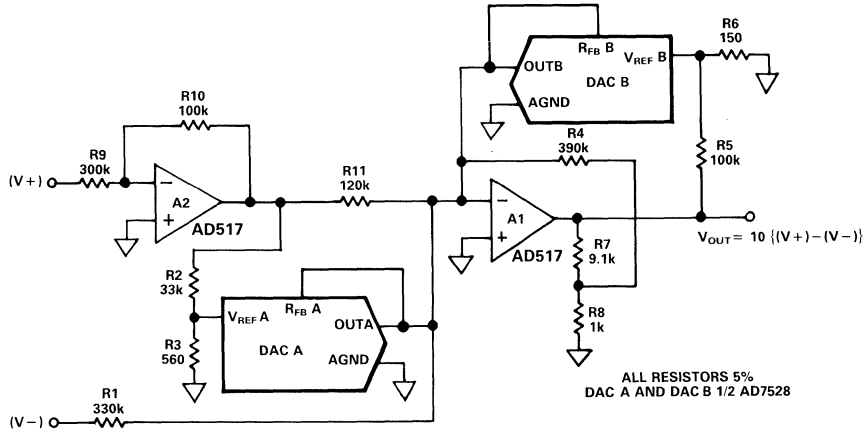


Figure 6.3.6 Instrumentation Amplifier with Digital Calibration for Common-Mode Rejection and Gain

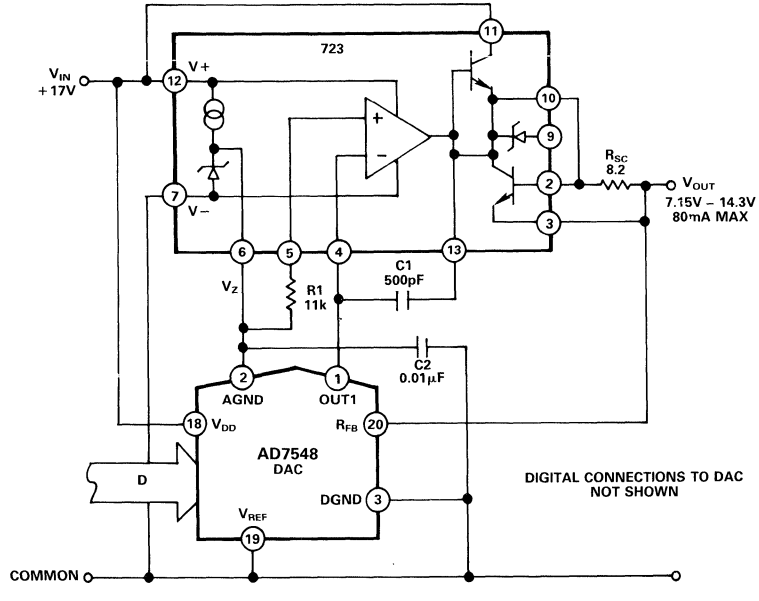


Figure 6.3.7 Simple 2 IC Programmable Power Supply

6.3.5 Programmable Power Supply Using 723 Voltage Regulator

Applications circuits for the 723 voltage regulator generally require a trim resistor to set the output voltage. For many of these circuits the trim resistor can be replaced by a CMOS DAC to form a digitally programmable power supply which can be programmed directly from an 8-bit bus. The circuit given here operates from a single supply and in its simplest form consists of just the 723 and a CMOS DAC with no additional active components.

Figure 6.3.7 shows a basic circuit which has an output programmable from 7.15 to 14.3 volts. The internal 7.15 reference voltage (V_{REF}) of the 723 drives the noninverting input of the 723 amplifier directly and fixes the AGND voltage of the DAC at 7.15 volts. The feedback resistor (R_{FB}) of the DAC and the DAC itself form a potential divider chain across the output and the 723 regulates to force the negative input of its amplifier to V_Z. The DAC is, therefore, operated with OUT1 and AGND at the same voltage (V_Z)—a necessary condition to ensure DAC

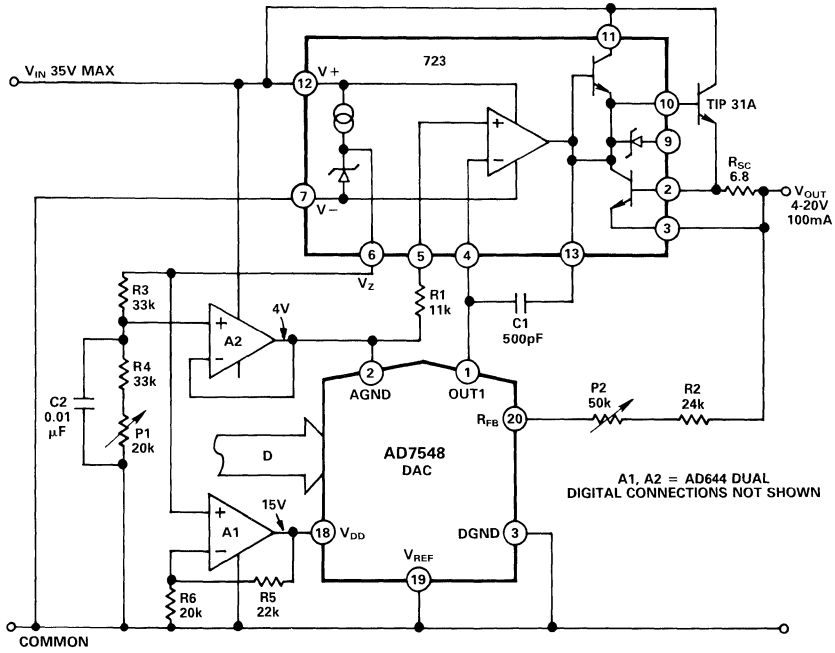


Figure 6.3.8 Inproved Programmable Power Supply

linearity. The input resistance of the DAC at the OUT1 node is equal to RDAC/D where D is the fractional binary input to the DAC and RDAC is the DAC input resistance. It is easily shown that:

$$V_{OUT} = V_Z(1 + D \cdot R_{FB}/RDAC)$$

and since R_{FB} usually matches RDAC to better than 0.5% this reduces to $V_{OUT} = V_Z(1 + D)$—a convenient transfer equation. The AD7548 is used because its inputs are TTL compatible and it interfaces directly to most microprocessor bus systems. Other DACs can be used in place of the AD7548 but the user should ensure that the AGND and DGND terminals are separately available and that logic inputs to the DAC are TTL compatible.

The maximum output current is determined by the power dissipation of the 723: the value of R_{SC} shown limits the current to the recommended value of 80mA for a plastic encapsulated device operated at an ambient temperature of 25°C without a heat-sink. Output current can be increased by heat sinking the 723 and/or using an external transistor as shown in Figure 6.3.8. The supply voltage to the AD7548 must be at least 5V greater than V_Z for the DAC to operate correctly and it should not exceed 17V. Resistor R1 minimizes errors due to different source impedances at the 723 amplifier inputs.

An alternative output voltage range of 3.6 to 7.15 volts can be achieved by connecting the potential divider chain between V_Z and ground, with the center tap going to the positive input of the amplifier: AGND, the output voltage V_{OUT} and the negative input of the amplifier are tied together. In this case the transfer equation is $V_{OUT} = V_Z/(1 + D)$.

In practice V_Z varies from one device to another and it is desirable to include provision for calibrating the power supply. Figure 6.3.8 shows a circuit which achieves this and incorporates a number of other improvements. It operates with any input voltage up to 35V and the output is programmable in the range 4.096 to 20.48 volts (i.e., 16mV/bit for 10-bit resolution). Output current is set to limit at 100mA. Other output currents can be accommodated by using different values of Rsc ($R_{SC} = 0.675/I_{SC}$ for $T_A = 25°C$) and by ensuring that the external transistor can handle the necessary power dissipation. Amplifier A1 buffers V_Z and provides the +15V supply to the DAC. Amplifier A2 generates an adjustable 4V reference voltage which drives the positive input of the 723 amplifier. A variable resistor P2 in series with R_{FB} sets full scale output. To calibrate the circuit D = 0 is applied to the DAC using the data override facility of the DAC and P1 adjusted for 4.096 volts out: then all 1's are applied to the DAC using the override and P2 adjusted for maximum output which

is (20.480 – 0.004) = 20.476 volts. The 723 amplifier has insufficient gain, and excessive input bias currents and offset voltage for the AD7548 to realize its full 12-bit monotonic range. In practice the circuit gives adequate performance for 10-bit resolution i.e. 16mV/bit.

6.4 PROGRAMMABLE CURRENT SOURCES

6.4.1 Basic Current Source Circuits

Programmable current sources form an important part of the analog circuit designers tool kit. They can be used as part of a larger circuit or can exist in their own right. Most of the circuits presented here are self explanatory—they establish a reference current programmed by a DAC, and then mirror the current until it flows in the right direction from the appropriate source. For eight-bit applications, the reference current can often be created by the DAC itself as shown in Figure 6.4.1. A fixed reference voltage is applied to the V_{REF} terminal of the DAC and the reference current created is the current flowing through the DAC itself. However, the D/A converter resistors exhibit an absolute temperature coefficient of the order of −300ppm/°C. For higher resolution or wide-temperature range applications, a more stable reference current is required. This can be achieved

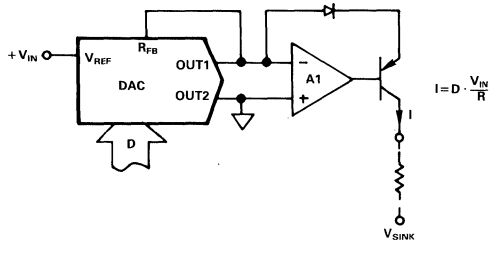


Figure 6.4.1 Simple Programmable Current Source to V_{SINK}

by establishing a precision voltage with the DAC, which in turn causes a reference current to flow through a precision resistor as shown, for example, in Figure 6.4.4.

In the circuits of Figures 6.4.2 and 6.4.3, the parallel combination of R1 and R_{FB} provides a sense resistor which feeds back a current through R_{FB} proportional to I.

$$I = D \cdot \frac{V_{IN}}{R1} \cdot \left\{ 1 + \frac{R1}{RDAC} \right\}_{\text{if } RDAC = R_{FB}}$$

If R1 is made small compared with R_{FB} then the output current will be relatively insensitive to different

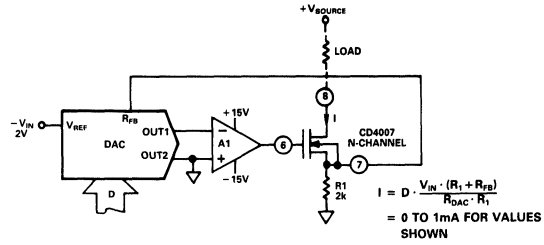


Figure 6.4.2 Programmable Current Sink from $+V_{SOURCE}$

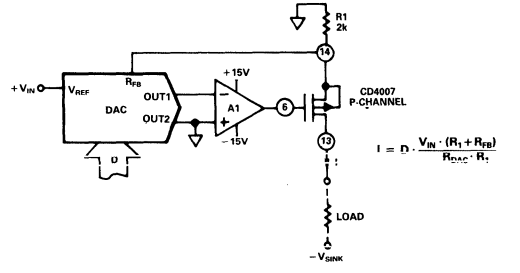


Figure 6.4.3 Programmable Current Source to $-V_{SINK}$

values of DAC resistance or the DAC resistance temperature coefficient.

The circuit of Figure 6.4.4 offers an even greater degree of insensitivity to DAC resistance. The DAC is operated as a programmable voltage source which sets a current through R1. This current is mirrored by Q1 and the same current creates a voltage drop across R3. Amplifier A2 and Q2 set up a proportional current I so that the voltages dropped across R3 and R4 are equal. In order to program right down to near zero levels of current, the input voltages of amplifier A2 must be capable of operating very close to V_{DD} and the output of A2 also must be able to swing near to V_{DD}. To achieve this, it is necessary to connect the positive supply point of the op amp to a voltage about 2.5V more positive than V_{DD}. Diodes D1 through D4 provide for this requirement.

The circuit of Figure 6.4.4 is insensitive to variations in V_{DD} because both R3 and R4 draw their current from the same node, and the output impedance of Q1 is very large due to the gain of amplifier A1. Resistor R2 protects Q1 from overload. Figure 6.4.5 shows a simple modification to the circuit for single supply operation. A further variation on the circuit of Figure 6.4.4 is shown in Figure 6.4.6. This provides a current source programmable in the range 0 to 1mA. NFET input op amps are used to reduce the effect of input bias currents and the bipolar transistors have

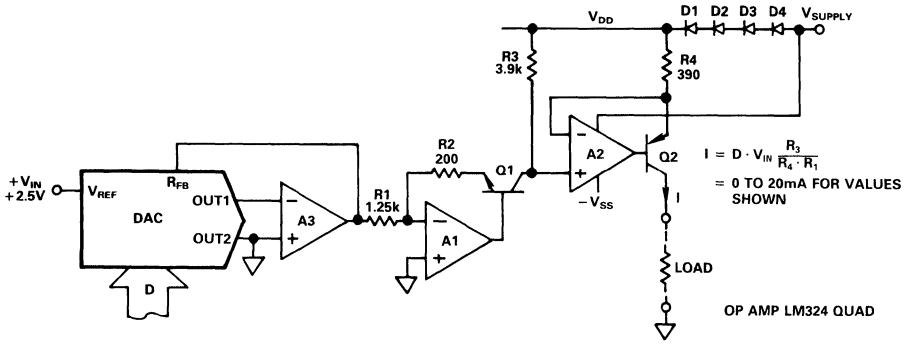


Figure 6.4.4 Programmable Current Source to AGND or $-V_{SINK}$

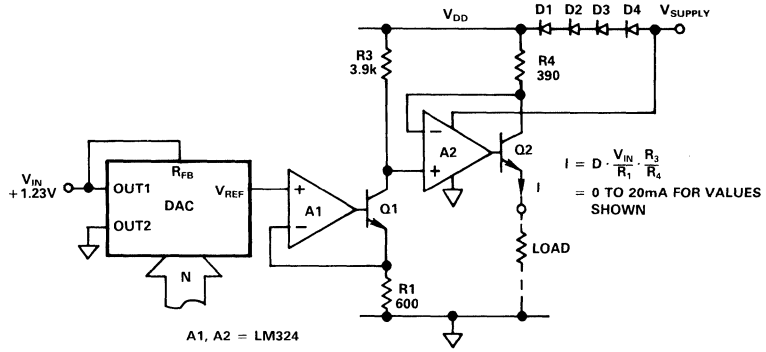


Figure 6.4.5 Single Supply Current Source to AGND

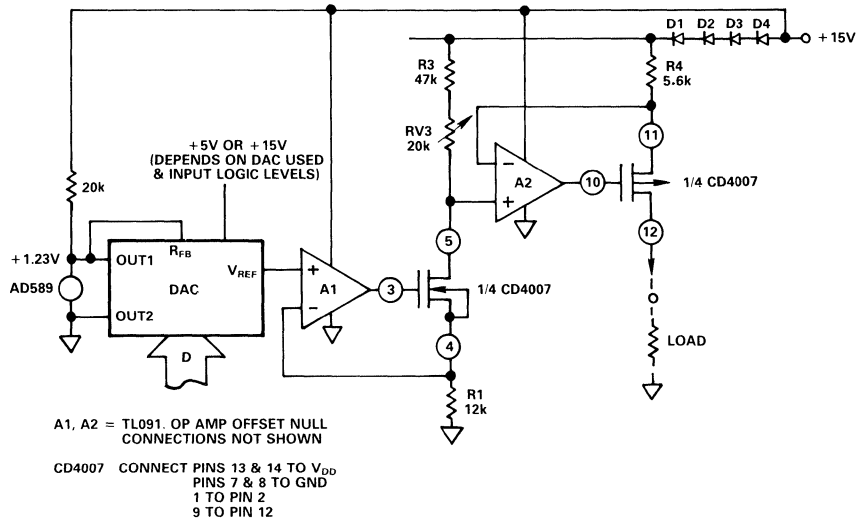


Figure 6.4.6 0 to 1mA Programmable Current Source – Single Supply

been replaced by MOS devices available on the CD4007 transistor array. It is important to null the input offset voltage of the amplifiers because the LSB bit weight of the DAC is only 5mV which is comparable to the typical input offset voltage of the TL091. The pin connections given for the CD4007 should be used to ensure correct operation of the device.

6.4.2 4-20mA Loop Circuits

Circuits of this class are used widely in the process control industry, particularly in the U.S.A. Analog values are transmitted from one point to another in a process plant as a current rather than a voltage to provide a greater degree of noise immunity. The effective 4mA offset on the scale can be used to power the remote receiver.

4-20mA loop circuits can be derived from any of the constant current-circuits described above. If the DAC is operated in the current-steering mode, the offset can be created by adding an offset current to the current from the OUT1 terminal of the DAC. If the DAC is operated in the voltage-switching mode, then the offset can be added by biasing OUT2 positive as described in Section 4.2.

Figure 6.4.7 shows the circuit of Figure 6.4.4 modified for 4-20mA loop applications. An additional current equal to $V_{IN}/4R$ is added to the summing junction of A1 via R8.

Figure 6.4.8 gives a simple 4-20mA loop circuit with the DAC operated in the voltage-switching mode. AGND is biased at approximately 300mV and OUT1 at 1.5V. The current in R1 is, therefore, $V_{OUT2}/R1$ for all zeroes code at the DAC and one bit less than $V_{OUT1}/R1$ for all ones applied to the DAC. The AD7545 and the op amps are operated from the +5V reference to improve system noise rejection. Since the DAC is CMOS, it draws very little supply current. Resistors R2, R3 and R6 improve the amplifiers' source capability (see Section 4.4.2) and R4 and R5 are used to set zero (4mA) and full-scale (20mA) respectively.

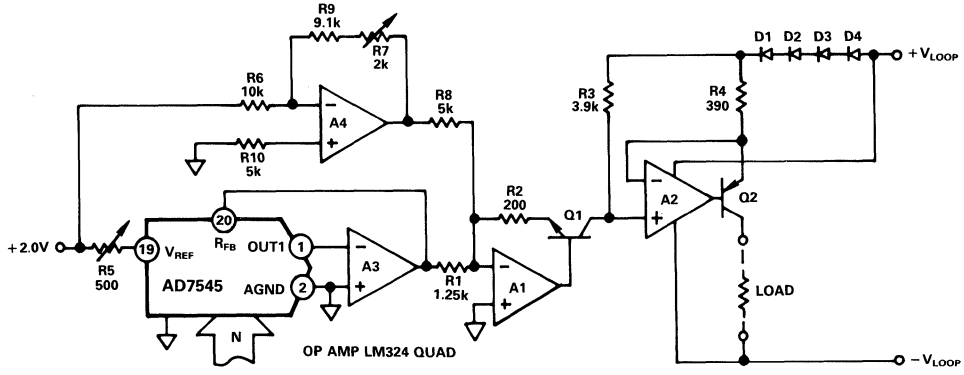


Figure 6.4.7 4-20mA Loop Circuit, Current-Steering Mode

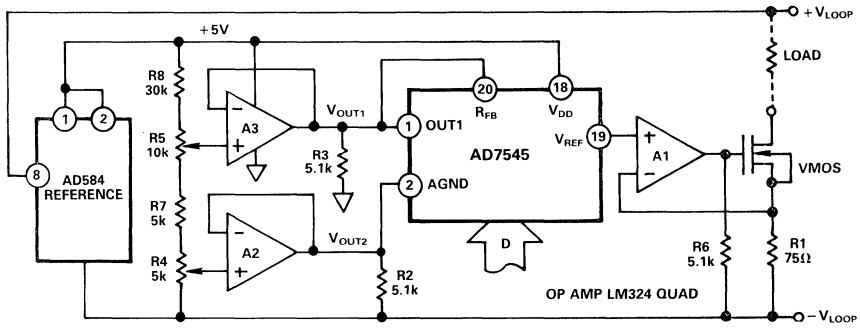


Figure 6.4.8 4-20mA Loop Circuit, Voltage-Switching DAC

6.5 LOW FREQUENCY FUNCTION GENERATION

6.5.1 Function Generation via DACs

Low frequency function generation is achieved by driving a DAC with a series of digital words representing the instantaneous values of the function to be synthesized. There is no limit to the lowest frequency that can be generated. The upper limit is determined by the settling time of the D/A converter circuit, the required resolution, permissible quantization noise etc.

Generally this method of function generation is used up to about 500Hz, although it can be extended up to about 20kHz if the DAC circuit is complemented with the appropriate filters, sample/hold etc. Digital audio systems use 14- and 16-bit D/A converters to reconstitute the analog audio signal.

Figure 6.5.1 shows the basic principle of a low frequency function generator. Since many functions are symmetric, it is normal to synthesize half a waveform and then invert it for the second half. For sinusoids, only the first quarter of the waveform need be synthesized and the remaining section can be derived using the relationships:

$$0 \leq \theta < 90 \quad y = \sin\theta$$
$$90 \leq \theta < 180 \quad y = \sin(180 - \theta)$$
$$180 \leq \theta < 270 \quad y = -\sin\theta$$
$$270 \leq \theta < 360 \quad y = -\sin(360 - \theta)$$

Figure 6.5.2 shows a block diagram of a sine-wave generator where the first quarter segment of the waveform is stored in ROM. The exclusive −OR is used to compute (180-θ) and (360-θ) and a sign magnitude coded DAC circuit is used to generate the appropriate polarity signal. In this type of function

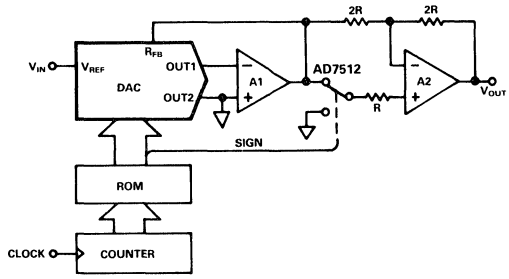


Figure 6.5.1 Basic DAC Based Low Frequency Function Generator

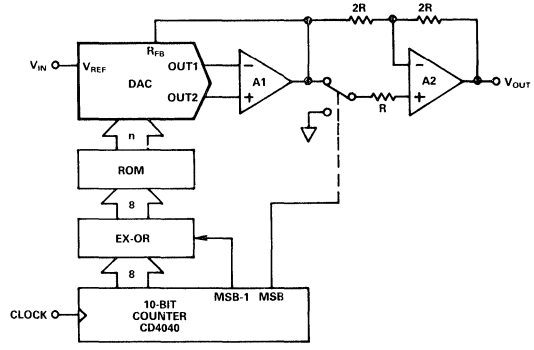


Figure 6.5.2 Block Diagram of Sinusoid Generator

generator, the amplitude of the output signal is easily controlled by varying V_{REF}.

Figure 6.5.3 shows a simple triangle waveform generator. The input clock frequency is applied to the CD4040 counter whose output drives the AD7524 DAC through exclusive −OR gates. The exclusive −OR inverts the binary code fed to the

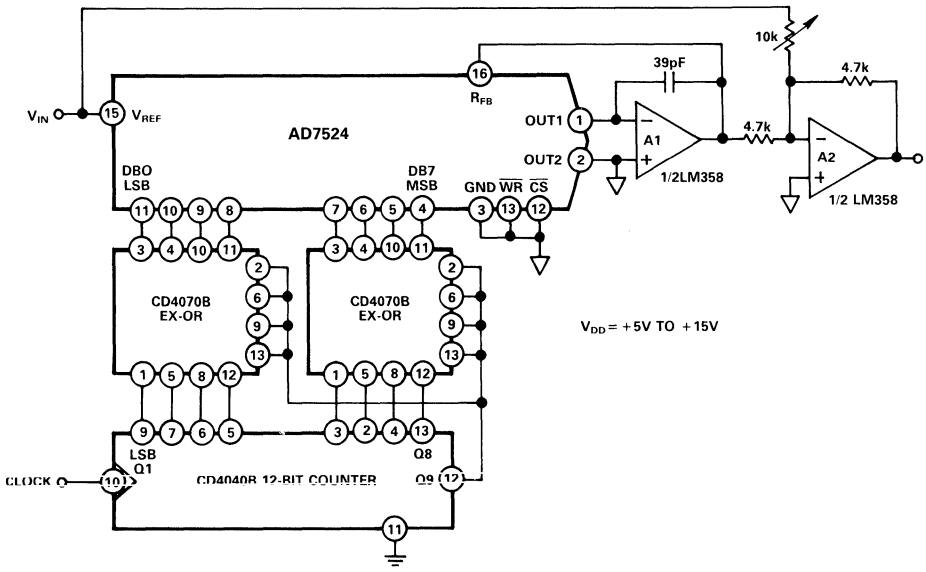


Figure 6.5.3 Simple Triangle Wave Generator

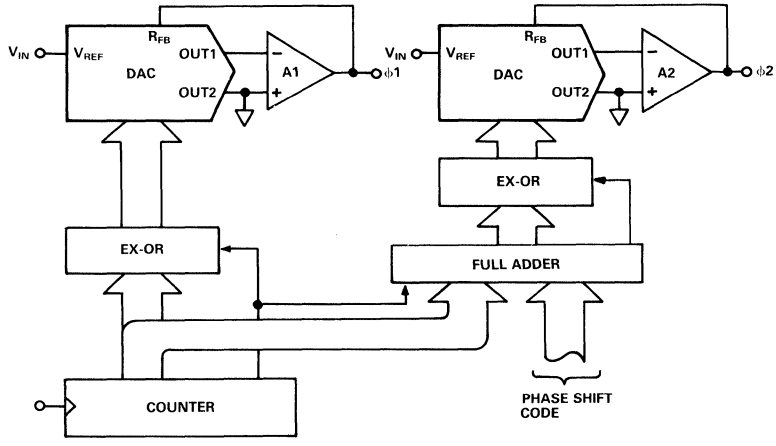


Figure 6.5.4 Two-Phase Triangle Wave Generator with Precision Phase Shift

DAC each half cycle. Consequently the binary number presented to the ROM counts up from 00000000 to 11111111 and then counts down from 11111111 to 00000000, thereby generating a well defined triangle waveform. Output amplitude is determined by V_{REF}, and the frequency is determined by the input clock frequency. Amplifier A2 shifts the dc level of the triangle to make it symmetrical about zero. Multi-phase waveforms can be generated by using an adder to add an offset to the binary code. Changing the offset code changes the phase between the waveforms and a very precise phase relationship between the waveforms can be achieved. Figure 6.5.4 shows the block diagram for a two phase waveform generator with adjustable phase relationship.

6.5.2 Triangle to Sine Conversion

There are various methods for converting a triangle waveform into other waveforms. A sinusoid can be approximated using the logarithmic relationship between V_{BE} and I_C of a bipolar transistor to smooth

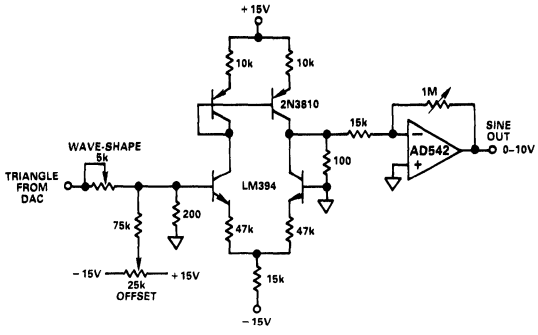


Figure 6.5.5 Triangle to Sine Wave Converter

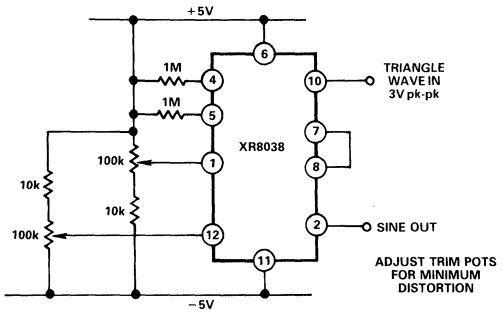


Figure 6.5.6 Monolithic Triangle to Sine Wave Generator

the triangular waveform. Figure 6.5.5 shows such a circuit described in References 7 and 8. A number of monolithic function generator circuits using this principle are also available (e.g., XR8038) and these can be used to convert a triangle wave into a sinusoid.[9] Figure 6.5.6 shows a sine wave generator which can be driven from the triangle-wave generator of Figure 6.5.3. An alternative method of obtaining a sine wave is to approximate it using the quadratic approximation.[10]

$$\sin\theta = 1.828.\theta + 0.828.\theta^2 \text{ for } 0 \leq \theta \leq \frac{\pi}{2}$$

Figure 6.5.7 shows a circuit to achieve this. DAC A and DAC B are driven from an up-down counter as shown. They form a pair of triangle wave generators as previously described. The reference voltage of DAC A is fixed, thus it delivers a simple triangle wave, i.e,. V_{OUT} A is proportional to D. This triangle wave is used as the reference voltage for DAC B so that DAC B behaves as a squaring circuit since both V_{REF} B and the digital inputs are determined by the digital value in the counter. DAC B output is, therefore, proportional to D^2. Amplifier A3 sums V_{OUT} A and V_{OUT} B in the proportion 1.828 : 0.828 and amplifier A4 delivers alternatively positive and negative half cycles. The circuit of Figure 6.5.7 can be used to synthesize sinusoids up to 2.5kHz with a distortion of −35dB. The values of R_A and R_B are critical to proper circuit operation and have a significant effect on wave-shape and distortion levels. Note how the circuit's oscillation rate is determined purely by the input clock frequency, consequently frequency changes are easily made. For amplitude modulation, the modulation voltage is applied to the V_{REF} terminal of DAC A. For more information on this circuit see Reference 10.

6.5.3 Interpolation Methods of Function Generation

Interpolation schemes are often used in vector scan C.R.T. systems where graphics are generated by drawing a series of straight lines on a long persistence C.R.T. Interpolation can also be used to generate any waveform by approximating the wave as a series of chords. The maximum fidelity and frequency of the output signal is determined by the number of chords used.

A simple interpolation scheme is shown in Figure 6.5.8. Two DACs are driven with triangular reference waveforms: the triangles are 180° out of phase. The DACs are alternately fed with the data word corresponding to the end value of the chord in question. In the example shown DAC P receives the first point Y1. Its triangle reference input ramps from zero to its maximum value at which point the output voltage corresponds to Y1. Y2 is now loaded to DAC Q and its reference voltage ramps from zero to maximum while Y1 reference is ramps down to zero. At the end of this period, the output voltage will be equal to Y2, since V_{REF} P = 0. DAC P is now loaded with value Y3 and the ramps are reversed. This process continues as long as required. Note that the digital fraction to each DAC is updated when its V_{REF} = 0, and therefore output glitches are minimized. For an X-Y graphics display two such systems are required, one per axis. Reference 11 gives a much more complete discussion of interpolation schemes.

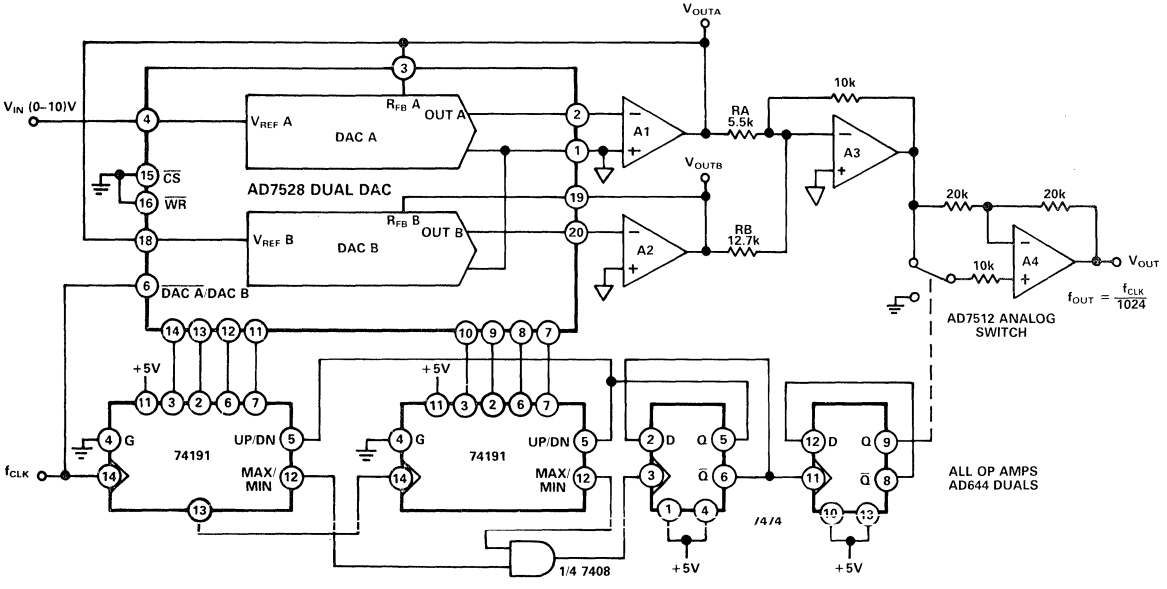


Figure 6.5.7 0-2.5kHz Low Frequency Sine Wave Generator Using Quadratic Approximation Method

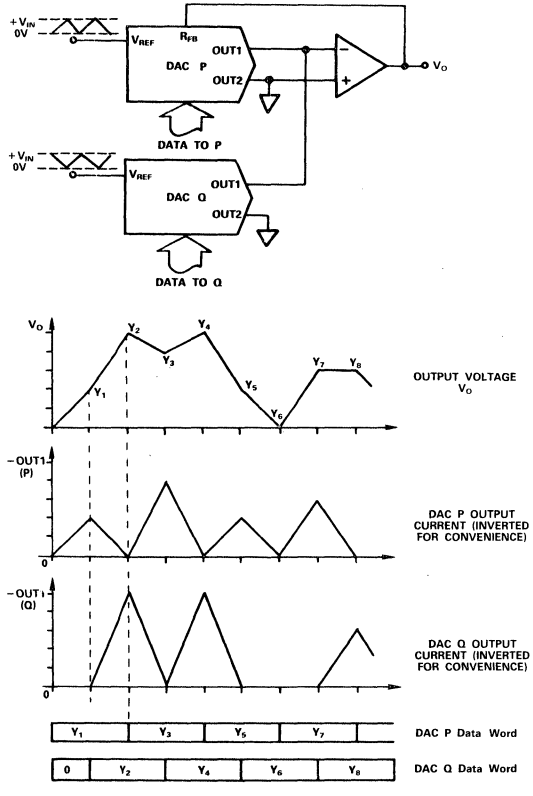


Figure 6.5.8 Simplified Interpolation Scheme for Function Generation

Figure 6.5.9 shows a simple stroke writing X-Y plotter drive for personal computers which demonstrates the interpolation system in use. The whole system operates from a single +5V supply. DAC 3 is used to generate the two triangle waveforms by operating it in the single supply current-steering mode with OUT1 and AGND biased at about +0.5V and with a nominal V_{REF} of 1.2V. Each triangle has exactly the same maximum and minimum values: R1 is used to compensate for amplifier offset mismatch and ensure that the maximum values of the triangle are the same (about 500mV). Resistor R2, which sets the gain of one of the curent to voltage converters, is used to trim the two minimum values to be the same (about 100mV). The triangle is generated by the microcomputer which alternately counts up and down between OOH and FFH and loads each value to DAC 3 as it does so. The peak triangle value of approximately 500mV is determined by the maximum voltage that can be applied to DAC 1 and DAC 2 before linearity is degraded. The minimum value of 100mV is determined by the current sink capability of output amplifiers A3 and A4 which have to sink current from DAC 1 and DAC 2, and must do this without any loss of linearity due to amplifier output impedance. Resistors R7 and R8 provide additional current sinking capability at the outputs of amplifiers A3 and A4 to assist the amplifier outputs to go down to +100mV. The outputs of each dual DAC are summed and amplified by the output amplifiers A1 and A2. Trim

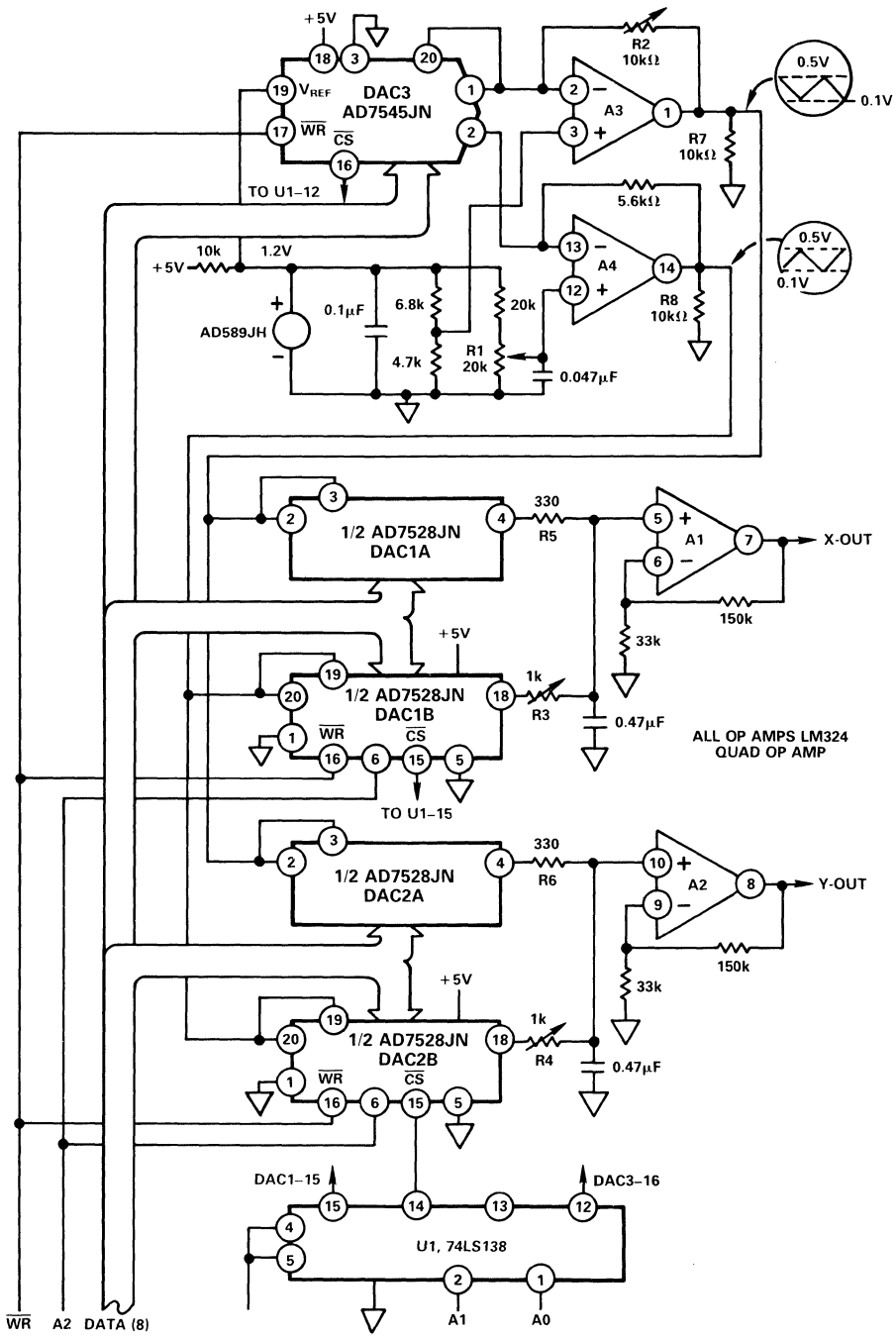


Figure 6.5.9 X-Y Plotter Interface Using +5V Supplies Only

resistors R3 and R4 can be used to match the output impedances of the DAC pairs. While the circuit in schematic form may look formidable, it in fact only uses five DIP packed I.C.'s and a bandgap reference type AD589JH. Note that the AD7545 is a 12-bit wide DAC but, in this application, the four LSBs are strapped low. Where possible, the +5V used by the circuit should be generated separately to reduce noise. Furthermore, the data, address and WR signals from the microprocessor should be gated as suggested in section 5.3.1 so that they only become active when the circuit is addressed.

6.6 MEDIUM FREQUENCY FUNCTION GENERATORS AND OSCILLATORS

6.6.1 Triangle/Square Wave Generator[28]

Figure 6.6.1 shows a basic triangle/square wave generator. A ramp is generated by the digitally controlled integrator : when the upper comparator trip point is reached, the opposite polarity reference is applied which causes the integrator to ramp in the opposite direction until it reaches the lower trigger point. The frequency of oscillation is determined by the fraction applied to the DAC, R, C and the value of the two trigger points. R is made up of R5 plus the DAC resistance: consequently, the oscillator frequency will change with DAC resistance. The circuit of Figure 6.6.2 overcomes this limitation by driving a constant current into the DAC. Amplifiers A3 and A4 form a constant current source which can be positive or negative depending upon the output of window comparator A2. The high frequency performance of this circuit is limited by the slew rate and settling time of amplifiers A2, A3 and A4, and for this reason should be high performance FET amplifiers such as AD544.

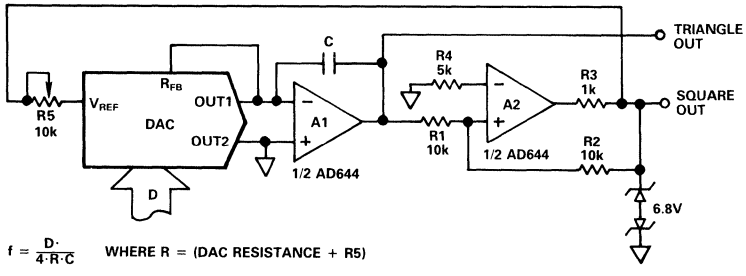


Figure 6.6.1 Programmable Triangle/Square Wave Generator

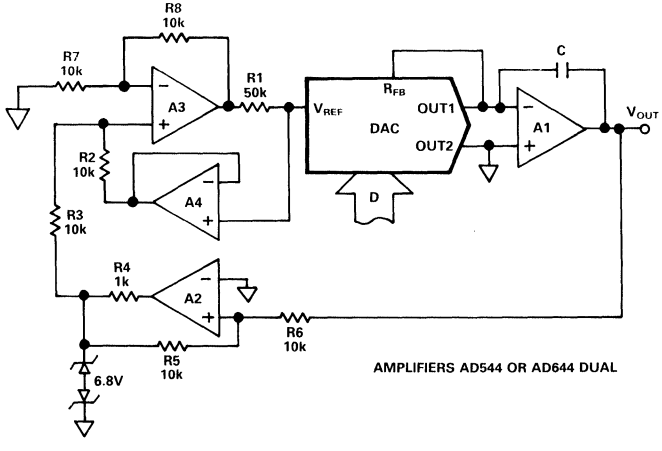


Figure 6.6.2 Improved Triangle Wave Generator

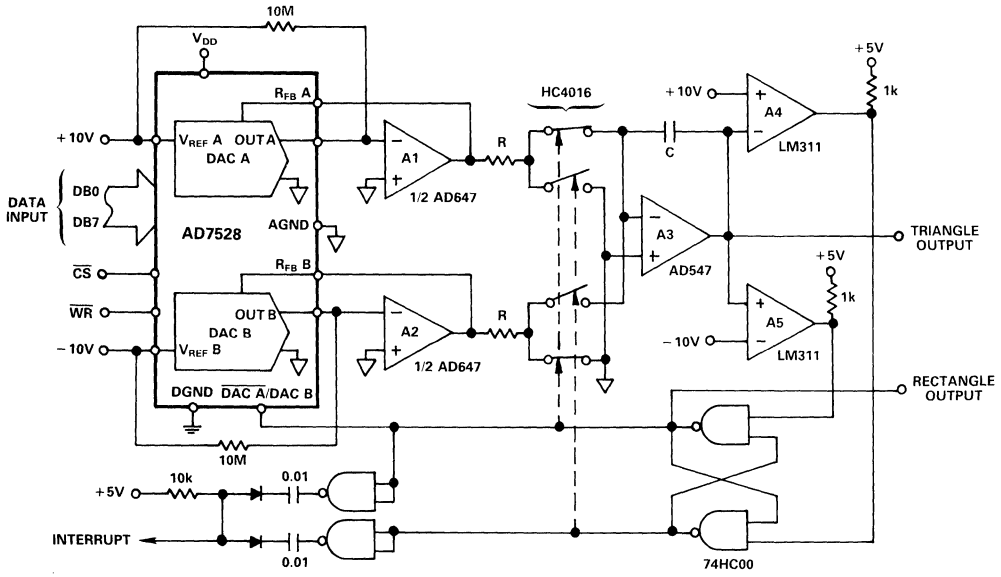


Figure 6.6.3 Triangle/Rectangle Generator with Individual Control of UP/DN Ramps and Mark/Space Ratio

6.6.2 Triangle/Rectangle Wave Generator with Programmable Waveform[10]

The circuit of Figure 6.6.3 overcomes the limitation imposed by amplifier slew rate as discussed above. It can be used to generate frequencies up to about 50kHz. Two DACs are used: DAC A controls the positive ramp and DAC B controls the negative ramp. DAC B is loaded while DAC A is driving the output positive, and vice versa. The flip-flop output automatically connects the "unused" DAC to the data bus for updating if necessary. The flip-flop provides a convenient interrupt to the processor at the start of each ramp. This type of triangle wave generator is useful in microprocessor controlled graphics systems. SW1 and SW2 are high speed CMOS switches such as HC4016. Spikes due to parasitic capacitance around the switches are minimized because the switched nodes are always at the same voltage (earth or virtual earth) and, therefore, a minimum amount of charging and discharging takes place. Each ramp period (i.e., half triangle) has a duration given by:

$$\text{Ramp period} = \frac{256RC}{D}$$

and ramps as short as 10μs (i.e., period frequency of 50kHz) can readily be generated by this method. The 10 megohm resistors provide 1/4LSB bias to each output so that in the event of all zeros being applied to either DAC, the circuit continues to oscillate.

6.6.3 State Variable Sine Wave Oscillators[10], [12]

A conventional state-variable sinusoidal oscillator is shown in Figure 6.6.4. The two integrators have been replaced by programmable integrators which may be conveniently constructed from an AD7528 dual 8-bit DAC. The frequency of oscillation is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\cdot\sqrt{\frac{1}{C1\cdot R1\cdot C2\cdot R2}}$$

where R1 and R2 are the effective resistances of DACs 1 & 2 respectively.

Since both DACs of the AD7528 are constructed on the same die, their resistance matches extremely well (typically 0.5%) and if C1 = C2 and R5 = R6, the frequency of oscillation is given by:

$$f = \frac{D}{2\pi\cdot R\cdot C}$$

where R is the resistance of the DAC. The circuit can be calibrated for a particular frequency/code ratio by adjusting R5. With the values shown, the output frequency varies from 0 to 15kHz in steps of approximately 60Hz/bit, with an amplitude of about 10V p-p. Total harmonic distortion measures −53dB at 1kHz and −43dB at 14kHz.

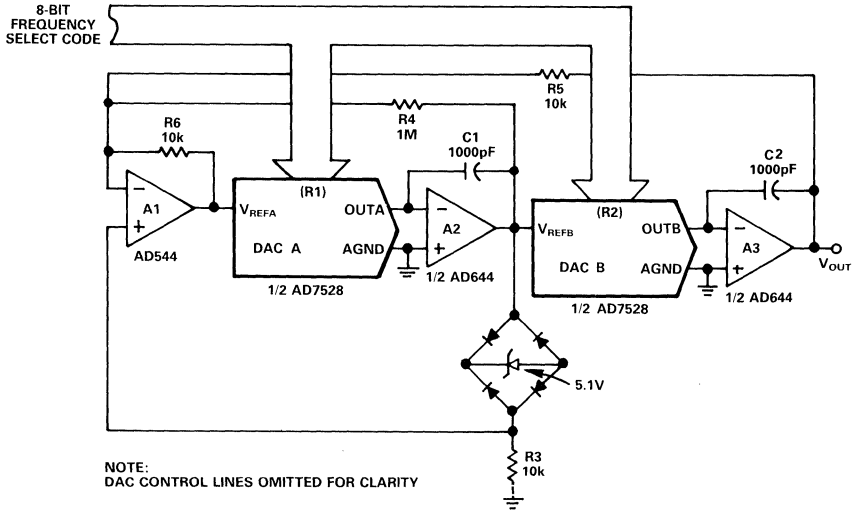


Figure 6.6.4 0-15kHz State-Variable Sine Oscillator

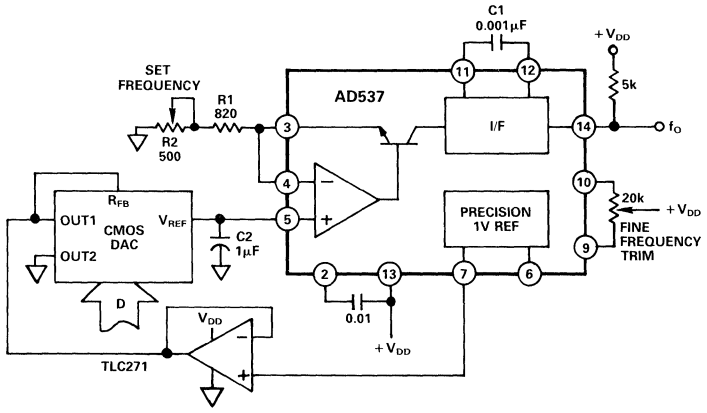


Figure 6.6.5 0-100kHz Programmable Oscillator for Single +5V to +15V Supplies

6.6.4 Digitally Programmable Oscillators and Frequency Modulators

D/A converters are often used to provide the control input to a voltage (or current) controlled oscillator. This technique is not limited to medium frequency applications and can be extended to quite high frequencies—for example, control of varactor diodes.

Figure 6.6.5 shows an AD537 Voltage/Frequency converter controlled by a CMOS DAC connected in the voltage-switching mode. This particular circuit is attractive because it operates from a single positive supply in the range +5V to +15V and exhibits excellent stability and independence from supply variations. The internal bandgap reference of the AD537, available on pin 7 of the device, is used to supply the 1 Volt reference to the DAC. The internal op amp of the AD537 is used to buffer the output of the CMOS DAC. Capacitor C2 in conjunction with the constant output resistance of the DAC forms a simple low pass filter which reduces the AD537 sensitivity to stray noise. The circuit, as shown, covers the range 0 to 100kHz: if C1 is changed to 0.01µF, the frequency range will be 0 to 10kHz. Any CMOS DAC can be used, but if a supply voltage other than +5V is applied and TTL compatible inputs are required then the user should select a DAC which has internal TTL to CMOS level shifters—see Appendix 1. Suitable DACs are AD7524 and AD7545 for +5V only operation and AD7240 or AD7548 for +10V to +15V operation.

The popular 555 timer/oscillator can also be controlled by a CMOS DAC. In its simplest form, the

DAC output voltage is applied to the control voltage pin of the 555. However, this gives a limited range of frequencies and Figure 6.6.6 shows one method of achieving wider control by using the DAC to program a constant current source for the capacitor charging circuit. The voltage-switching DAC supplies a voltage which determines the current in the constant current circuit. This current is mirrored by transistor pair Q1, Q2 to supply the charging current for the 555's timing capacitor. The accuracy of this circuit is limited by the performance of the current mirror and the response time of the comparator in the 555 timer. To improve the linearity of the relationship between digital fraction and oscillator frequency, the circuit of Figure 6.6.7 is recommended. A resistor is inserted between pins 6 and 7 of the 555 timer to increase the capacitor discharge time. Consequently, the comparator response time becomes

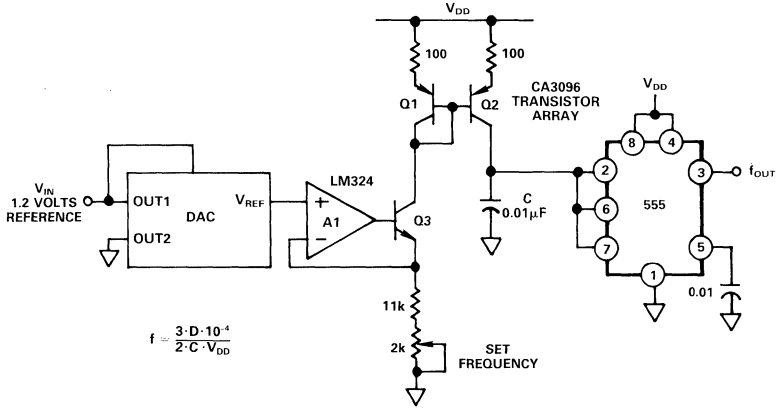


Figure 6.6.6 Single Programmable Oscillator Using 555 Timer

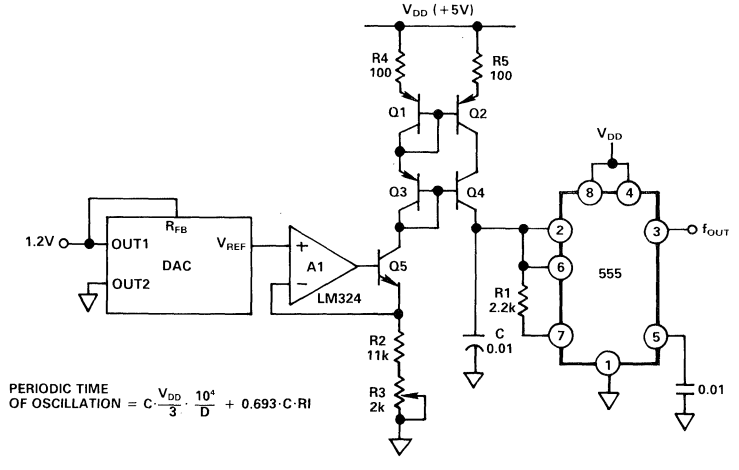


Figure 6.6.7 Programmable Oscillator with Improved Linearity

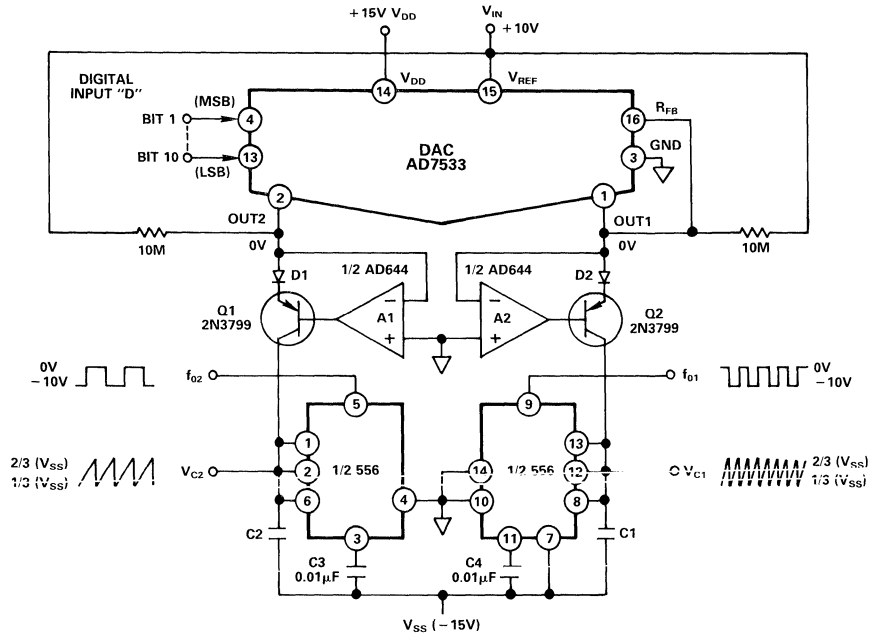


Figure 6.6.8 Programmable Oscillator with Complementary Output Frequencies

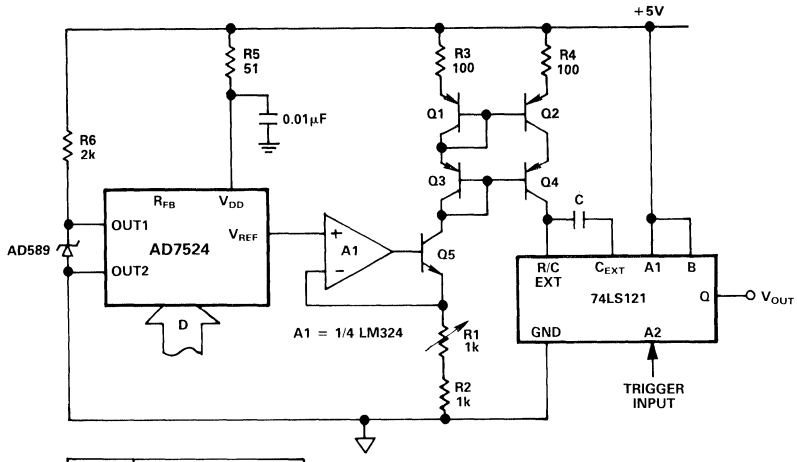
insignificant in the overall transfer function. The resistor does, however, introduce an additional term into the transfer equation of the circuit. The circuit shown covers the range from 20Hz to 5kHz with an accuracy of ± 10Hz.

Figure 6.6.8 shows a novel method of driving a dual 556 timer from one DAC[13]. OUT1 and OUT2 are driven into current mirror circuits consisting of A2, Q2 and A1, Q1. These current mirrors provide the capacitor charging current for the 556 timers which are operated with VCC at ground and their ground at $-V_{SS}$ (−15V). Since the sum of the currents from OUT1 and OUT2 is always a constant, the sum of the frequencies from the two oscillators must also be constant. Thus, as one frequency is increased, the other is decreased.

In all of the applications described above, the oscillator frequency is determined by the code to the DAC and the reference voltage. Frequency modulation from a digital data source is achieved by using the appropriate digital words. Frequency modulation from an analog source is done by adding the analog signal to the reference voltage. Where the DAC is operated in the voltage-switching mode, it is important to ensure that the composite input voltage of reference voltage plus modulation can never go negative, even under overload conditions. If there is any possibility of this happening, OUT1 should be connected to ground by a reverse biased Schottky diode (type HP-5082-2811) to prevent internal diodes from being turned on and damaging the DAC.

6.6.5 Programmable One-Shots and Pulse Generators[14]

The principles described above for controlling oscillators are equally applicable to pulse generators and one shots. In the circuit of Figure 6.6.9 a programmable current programs the pulse width of a 74121 type one shot. Full scale on the DAC produces the shortest pulse and small binary numbers give the longest available pulse. For a given capacitor the useful range of pulses is about 50:1 for an eight bit DAC. With small binary codes the pulse is long and any linearity error of the DAC represents a significant error in pulse width: therefore the circuit has poor accuracy in this region. Calibrate the circuit with the DAC at about half scale: this gives a pulse width long enough to be accurately measured and a binary code large enough to make any DAC linearity error relatively insignificant. For greater accuracy or a wider range of pulse widths use a higher resolution DAC (e.g. AD7545 12 bit DAC).



CμF	APPROX. RANGE OF PULSE WIDTHS
0.001	3μs TO 1ms
0.01	30μs TO 10ms
0.1	300μs TO 100ms

Q1, Q2 and Q3, Q4 CAN BE ANY SMALL DUAL PNP TRANSISTORS OR PART OF TRANSISTOR ARRAY, e.g., CA3096.

Q5 CAN BE ANY SMALL SIGNAL NPN DEVICE, e.g., PART OF CA3096.

Figure 6.6.9 One-Shot with Programmable Pulse Width

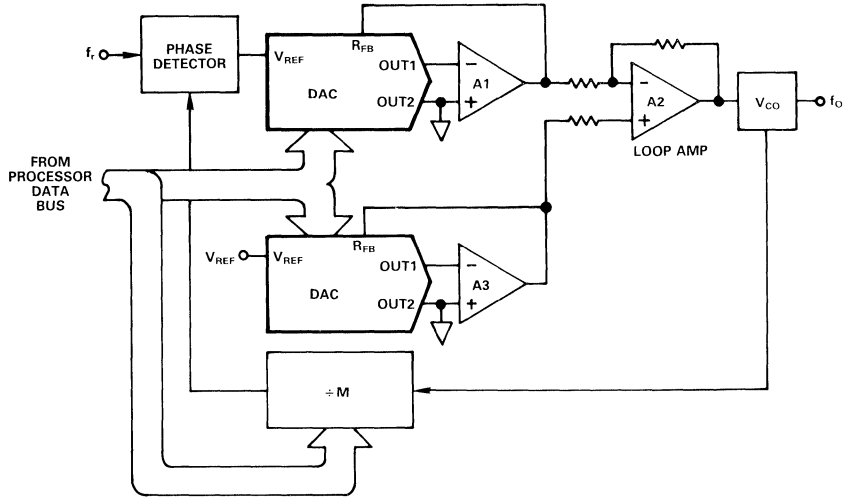


Figure 6.6.10 Phase-Lock Loop Stabilization Using Dual DAC

6.6.6 Phased Locked Loop Stabilization[15]

Phase locked loops allow a high frequency waveform to be synthezised and locked to a lower frequency oscillator. A reference frequency fr is applied to a phase sensitive detector, amplifier and voltage controlled oscillator. The output frequency is a multiple M of fr (i.e., f_o = M·fr) and this is divided by a digital counter for feedback to the phase sensitive detector as shown in Figure 6.6.10. For a given design, large changes in M, 2:1 or greater, during operation can cause severe problems in maintaining transient response, loop bandwith and overall stability. One solution is to compensate for these changes by using a multiplying DAC as a programmable gain (attenuator) element. When M is changed, under computer control, the loop gain is also modified by changing the digital word in the DAC. Since a phase-locked loop is an ac coupled system, it is necessary to cancel out the dc gain of the CMOS DAC attenuator circuit by a second DAC which subtracts the dc offset. Both

DACs should match and track one another so as to reduce any dc error drift—an AD7528 dual DAC is ideal for this task. Figure 6.6.10 shows a block diagram of a phase locked loop system using the dual DAC method of loop gain compensation. This scheme has several advantages over others which generally rely on transconductance amplifiers. Such amplifiers use current mirrors requiring precision resistors and many offset adjustments which cause major delays and expense on the production line. The DAC approach eliminates these problems by inherently possessing the needed accuracy. For more information on this method, the reader is referred to Reference 15.

6.7. DIGITALLY CONTROLLED FILTERS

6.7.1 Simple Low Pass Filters[24]

Multiplying D/A converters can be used to construct active filters with complete control of gain, centre frequency and Q-Factor. The advantage of multiplying DAC filters over other types is that they have very low noise and distortion. The resolution of the filter characteristics is determined by the resolution of the D/A converters.

Figures 6.7.1, 6.7.2 and 6.7.3 show three different methods of realizing simple first order low-pass filters. These illustrate the principle considerations for active filter design with multiplying DACs. Figure 6.7.1 shows the simplest form of a low-pass filter. The cut-off radial frequency is given by:

$$\omega = \frac{R1}{(R1 + R2)} \cdot \frac{D}{(C \cdot RDAC)}$$

Where D is the fractional binary number applied to the DAC.

Note that ω is determined by the value of RDAC which varies from device to device. This problem is avoided in the circuit of Figure 6.7.2 by using the DAC as a programmable gain element. It will be seen that the cut-off frequency is independent of RDAC. If it is required to have a proportional adjustment of a filter time constant rather than its cut-off frequency, the circuit of Figure 6.7.2 can be re-arranged with the DAC connected in the divider configuration as shown in Figure 6.7.3. The time constant of the circuit is given by:

$$\tau = \frac{R2 \cdot R4 \cdot D \cdot C}{R3}$$

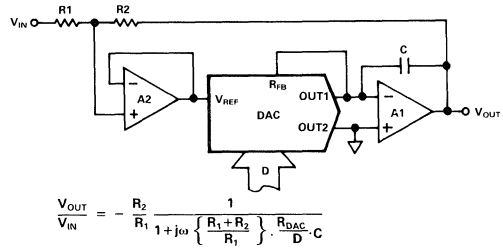


Figure 6.7.1 Simple Low Pass Filter

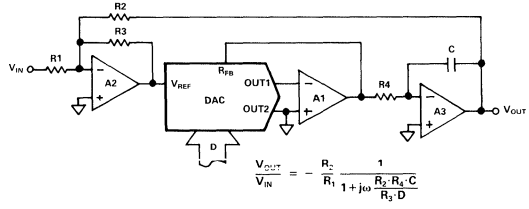


Figure 6.7.2 Low Pass Filter Independent of Value of DAC Resistance R_{DAC}

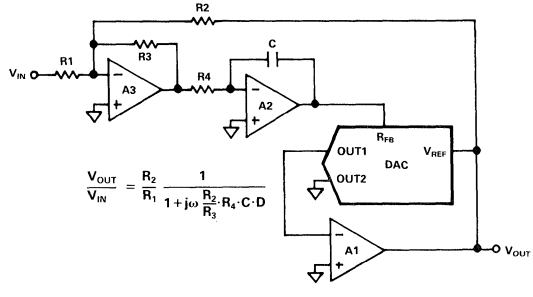


Figure 6.7.3 Low Pass Filter with Digitally Programmable Time Constant

Note that the divider follows the integrator in order to permit the divider to have high gain (at short time constants) without causing the circuit to limit.

6.7.2 State Variable Filters[16]

Most programmable filter circuits using multiplying DACs are based on the state variable technique. They can give high-pass, low-pass and band-pass from the same circuit. A complete analysis of state-variable filter design is beyond the scope of this text, but the following text will serve as an introduction.

Figure 6.7.4 shows one form of a second-order state-variable filter which is particularly suitable for use

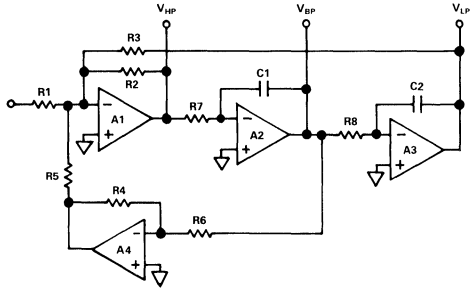


Figure 6.7.4 Second Order State Variable Filter with High Pass, Low Pass and Band Pass Outputs

with multiplying DACs because each amplifier operates with its summing node at virtual earth. Therefore, any one of the resistors could, if required, be replaced by a multiplying DAC operated in the current-switching mode. The transfer functions to the three outputs are as follows:

$$\text{High Pass } V_{HP} = \left\{ \frac{-\frac{R2}{R1} \cdot S^2}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\text{Low Pass } V_{LP} = \left\{ \frac{-\frac{R2}{R1} \cdot \omega_1 \cdot \omega_2}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \cdot \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\text{Band Pass } V_{BP} = \left\{ \frac{\omega_1 \cdot \frac{R2}{R1} \cdot S}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \cdot \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

where $\omega_1 = \frac{1}{C1 \cdot R7}$, $\omega_2 = \frac{1}{C2 \cdot R8}$

and S is the Laplace Operator

The high-pass and low-pass outputs can be considered simultaneously. If R2 = R3 = R5 and R4 = 2R6 and $\omega_1 = \omega_2 = \omega_0$ then the two equations become:

$$V_{HP} = \frac{-\frac{R2}{R1} \cdot S^2}{(S + \omega_0)^2}$$

$$V_{LP} = \frac{-\frac{R2}{R1} \cdot \omega_0^2}{(S + \omega_0)^2}$$

The pass-band gain is set by the ratio R2/R1 and the cut off frequency is determined by (R7·C1) = (R8·C2). Figure 6.7.5 shows a practical realization of this circuit using multiplying DACs. C1 is made equal to C2 and the AD7528 dual 8-bit DAC is used for DAC 1 and DAC 2 which control ω_1 and ω_2 respectively. If the fractional binary value D is applied to both DAC 1 and DAC 2, the transfer function for the two outputs is:

$$V_{HP} = \frac{-R2}{R1} \cdot \frac{S^2}{(S + \omega_0 \cdot D)^2}$$

$$V_{LP} = \frac{-R2}{R1} \cdot \frac{D^2 \cdot \omega_0^2}{(S + \omega_0 \cdot D)^2}$$

Note that the pass-band gain for both outputs is independent of the value of D, and that the cut-off frequency is directly proportional to D. The gain of the filter can be made variable by replacing R1 with another multiplying DAC, in which case the pass-band gain becomes (−D·R2)/RDAC where D is the fractional binary value applied to the DAC replacing R1. Figure 6.7.6 gives the measured frequency response for the high and low-pass outputs of the circuit of Figure 6.7.5.

If R2 = R3 = R5, the band-pass transfer function becomes:

$$V_{BP} = \left\{ \frac{\omega_1 \cdot \frac{R2}{R1} \cdot S}{S^2 + \frac{R4}{R6} \cdot \omega_1 \cdot S + \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\omega_0 = \sqrt{\omega_1 \cdot \omega_2} = \omega_1, \omega_2 \text{ if } C1 \cdot R7 = C2 \cdot R8$$

$$\text{Q factor} = \frac{R6}{R4}$$

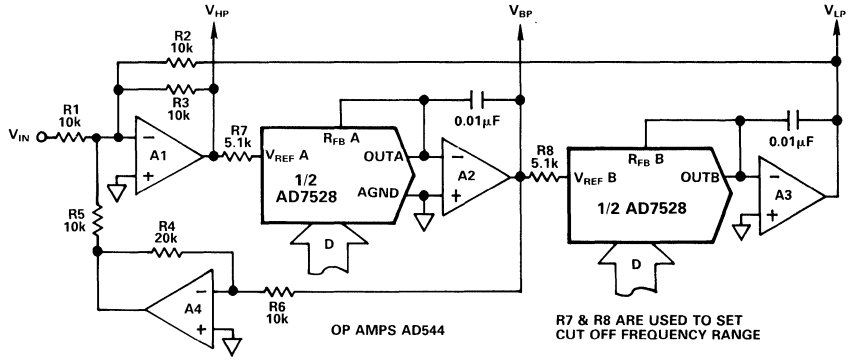


Figure 6.7.5 Practical State Variable Filter with Digital Control of Cut Off Frequencies

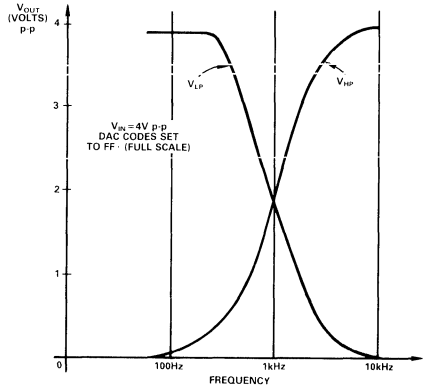


Figure 6.7.6 High and Low Pass Frequency Response for Figure 6.7.5 Circuit

Thus if R1, R6, R7 and R8 are replaced with multiplying DACs, it is possible to construct the state variable filter, shown in Figure 6.7.7 which has control of:

a) Pass band gain – vary D1
b) Q-factor – vary D6 (and D1 for constant gain)
c) Centre frequency – vary D7 and D8 simultaneously.

Changing the Q-factor, via D6 changes the pass-band gain. To hold the pass-band gain constant, DACs 1 and 6 should be changed in proportion to each other. Figure 6.7.8 shows the effect of changing only D6 for the circuit of Figure 6.7.7 with all other DACs set to full scale.

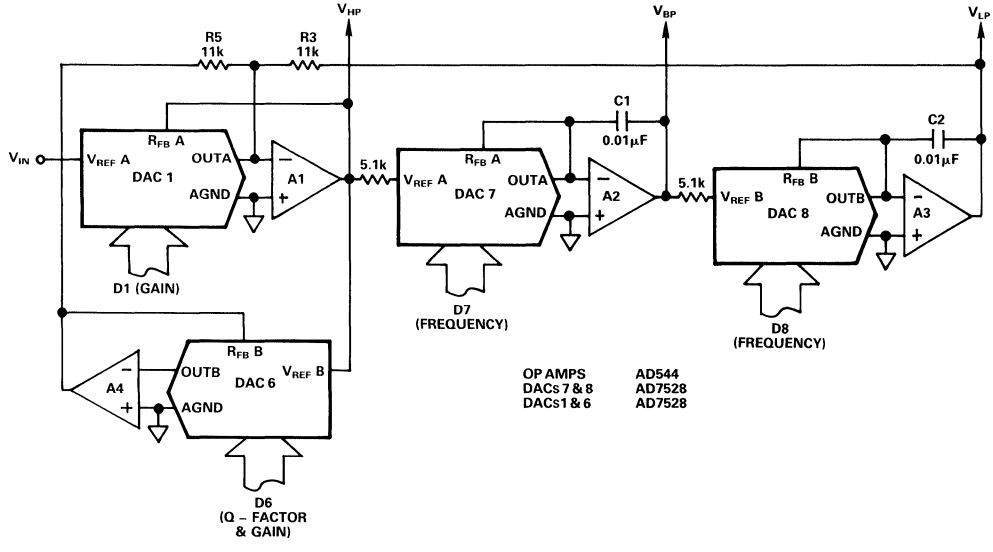


Figure 6.7.7 State Variable Filter with Digital Control of Gain, Frequency, Q-Factor

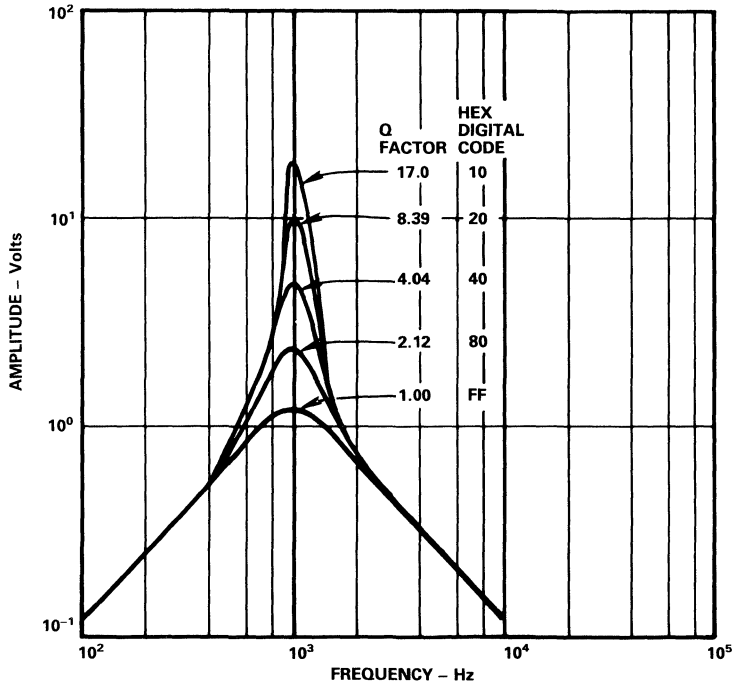


Figure 6.7.8 Effect of Changing D6 in Figure 6.7.7

6.8 AUDIO APPLICATIONS OF CMOS DACs

6.8.1 Audio Attenuators (Volume Control)

It was pointed out in Section 2.3.8 that CMOS DACs are particularly suited to audio applications because they create very little distortion or noise. They make excellent audio attenuators but conventional binary coded DACs deliver linear attenuation rather than the exponential relationship of the human ear. To overcome this, three CMOS DACs are now available which deliver a logarithmic relationship between digital fraction and output signal level. These "LOGDACs" are:

1) AD7111 0 to 88.5dB in 0.375dB steps
2) AD7118 0 to 88.5dB in 1.5 dB steps
3) AD7115 0 to 20dB in 0.1dB steps

Figure 6.8.1 shows the AD7111 connected as an audio attenuator and Figure 6.8.2 shows the AD7115 coupled with a second attenuator to provide precision attenuation accurate to ±0.05dB in the range 0 to 80dB. JFET input amplifiers such as AD542/544 are excellent low noise audio amplifiers in their own right and coupled with a LOGDAC make a formidable team.

6.8.2 Audio Balance and Panners[28]

Eight-bit binary coded DACs such as AD7528JN can give up to 30dB attenuation range to an accuracy of ± 1dB. This is insufficient for use as volume controls but is adequate for stereo balance applications as shown in Figure 6.8.3. The two channels are

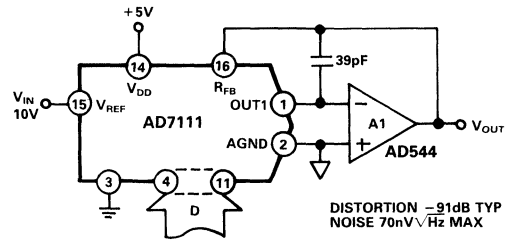
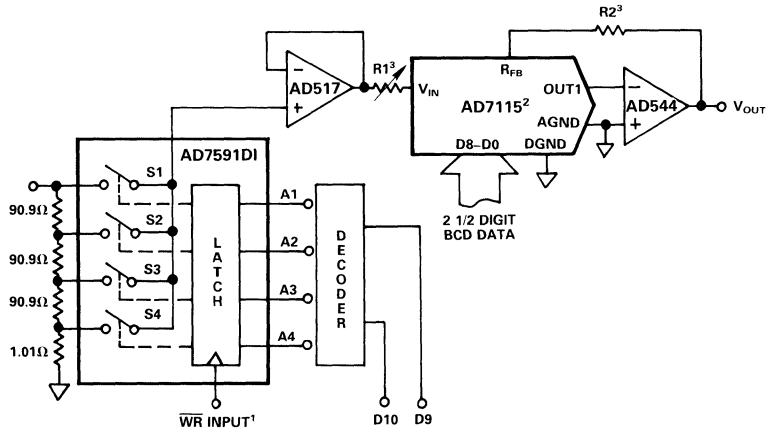


Figure 6.8.1 0.375dB Step Attenuator to −88.5dB



[1]THIS AD7591DI PIN SHOULD BE TIED LOW IF THE DATA LATCH FACILITY IS NOT REQUIRED.
[2]CONTROL INPUTS OMITTED FOR CLARITY.
[3]R1 AND R2 MAY BE OMITTED IF GAIN ERROR TRIM IS NOT REQUIRED.

Figure 6.8.2 0.1dB Step Attenuator to −80dB

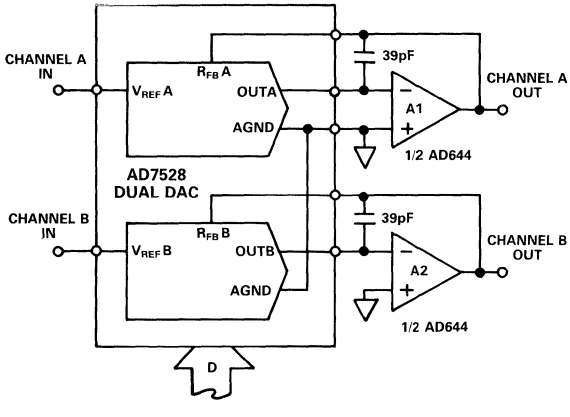


Figure 6.8.3 Dual 8-Bit DAC as Stereo Balance Control

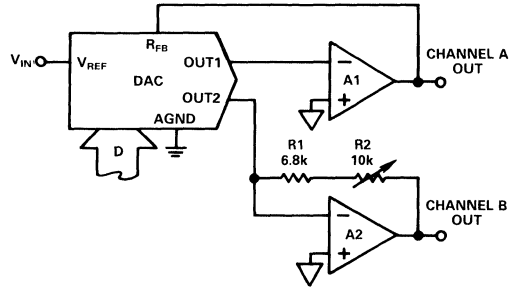


Figure 6.8.4 Digitally Programmed Audio Panner

applied to DACs A and B and the appropriate attenuation levels determined by the digital values loaded to each DAC. If OUTA and OUTB are fed into a single op amp, the circuit functions as a digitally controlled mixer.

Figure 6.8.4 illustrates a simple audio panner used to steer a single signal between two output channels. Since the currents at OUT1 and OUT2 are complementary, the proportion of the signal in each of the output channels is determined by the code applied to the DAC. This circuit works best when the ladder termination resistor is not tied to OUT2 (e.g., AD7533) so that both channels have a "mute" position.

6.9 MICROPROCESSOR INTERFACES

6.9.1 AD7545 to 8-Bit Data Bus Systems

The circuit of Figure 6.9.1 shows the general principles for connecting the AD7545 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 16-bit word. The DAC is connected to this 16-bit bus: the connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, being active only when the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer

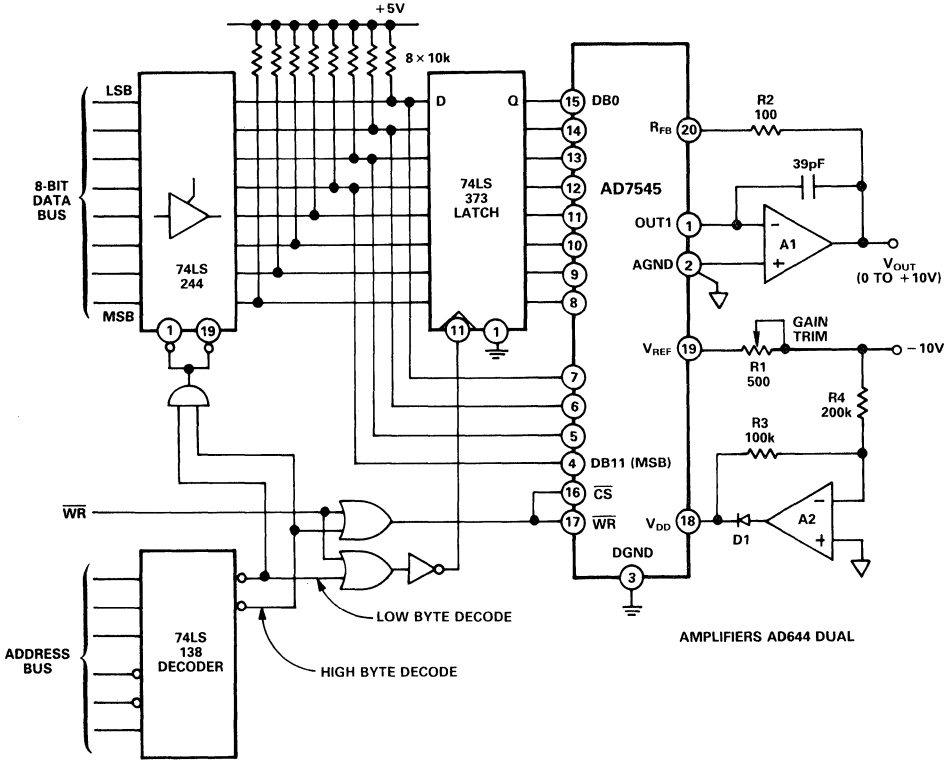


Figure 6.9.1 AD7545 to 8-Bit Data Bus Interface

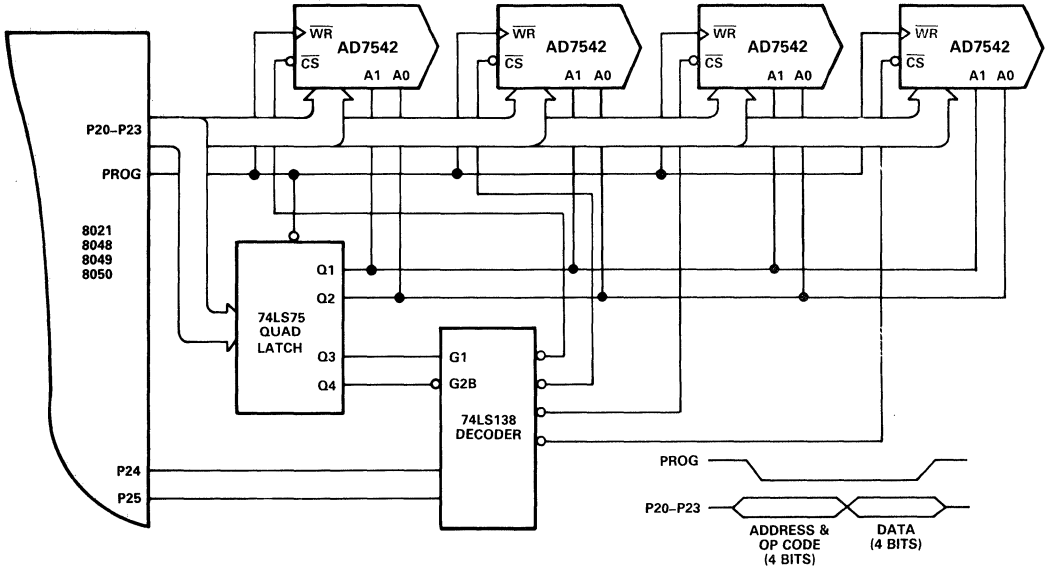


Figure 6.9.2 MCS48 Microcontroller to AD7542 Interface

ensure that the inputs to the DAC do not float at an ill defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when more than two DACs exist on the same circuit board. In other applications, the AD7548 is preferred because it incorporates the octal latch on-chip. To reduce noise injection from the logic circuits, the +5V supply for the DAC is derived from the −10V reference via A2. Diode D1 prevents excessive current being drawn from the DAC in the event of A2 output going negative during power-up or for any other reason (e.g., power supply failure). For further information on reducing extraneous noise and general microprocessor interface techniques, the reader is referred to Chapter 5.

6.9.2 MCS48 Microcontroller to AD7542 Interface[29], [30]

The four-bit input data bus for the AD7542 makes it ideal for connecting to the four-bit expander port of the MCS48 family of microcontrollers as shown in Figure 6.9.2. P20 through P23 provide the four-bit data bus which carries both the DAC register address and the data as shown in the timing diagram. When PROG goes low, the register address and the op code are latched into the 7475 quad latch. The two least significant bits give the register address and the two most significant bits define the op code which is primarily intended for the 8243 expander. In this particular case, the AD7542 is only required to respond to the "WRITE" command. The "WRITE" op code is used to enable the 74LS138 decoder inputs G1 and G2B as shown. Data is latched into the AD7542 when PROG goes high: the particular DAC being selected with the address from bits P24 and P25, via the decoder.

The instruction set for the MCS48 family includes some special instructions which make it particularly easy and effective to communciate with the DACs via the four-bit expander port as shown. Although the MCS51 family of microcontrollers does not have the same four-bit expander port capability, it is a simple matter to emulate these facilities using an MCS51 device: The INTEL Microcontroller User's Handbook gives further details.

6.9.3 AD7542 to 8-Bit Data Bus Systems[23]

The AD7542 uses 4-bit "nibbles" to input data in conjunction with two address lines which determine whether the data is the low, middle or high 4- bits of the 12-bit word required for the DAC. Software difficulties arise when, as is usually the case, the data is stored as a conventional 16-bit value in two registers or consecutive memory bytes. If the four data inputs are connected to the four least significant bits of the data bus, then the lower and higher nibbles can be loaded to the DAC by a straightforward write instruction. But to load the middle nibble, the data must be shifted down four places before being written to the DAC. The circuit shown in Figure 6.9.3 eliminates the need for this shift by selecting the relevant four-bits of the 8-bit bus according to the sense of the address select lines. It allows the LOW byte of data to be loaded to the first two addresses with the lower and middle nibbles going to their respective registers. The addition of the 74LS157 data selector between the DAC and the data bus also serves to isolate the digital inputs to the DAC from the data bus except when the DAC is being addressed and thus reduces crosstalk between the bus and the analog output signal. The OR gates on the address and $\overline{WR}$ lines serve a similar function.

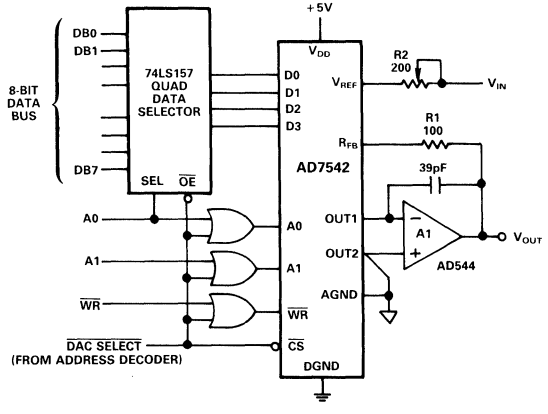


Figure 6.9.3 AD7542 to 8-Bit Data Bus Systems

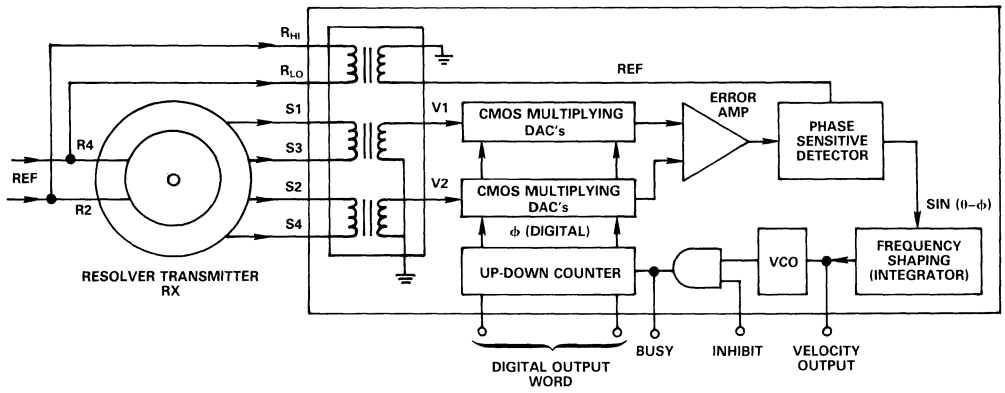


Figure 6.10.1 A Tracking Resolver-to-Digital Converter

6.10 MISCELLANEOUS SYSTEMS APPLICATIONS

6.10.1 Resolver-to-Digital Converter[18]

Resolvers and synchros indicate angular position. A rotor is excited with a reference voltage V sin ωt (usually 60 or 400Hz) and the stator has two windings at 90° to each other, so that the output of one stator winding is V sin ωt·sin θ and the other V sin ωt·cos θ. These two outputs are applied to the V_{REF} inputs of CMOS D/A converters whose digital input words are proportional to the sine and cosine of some angle θ as shown in Figure 6.10.1.

The output of the cosine multiplier is given by

$$V \sin \omega t \cdot \sin \theta \cos \phi$$

and the output of the sine multiplier is given by

$$V \sin \omega \cdot \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give the error signal which is:

$$V \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$
$$= V \sin \omega t (\sin \theta - \phi)$$

This error signal is demodulated by the phase sensitive detector which utilizes the system reference voltage and a dc error signal proportional to sin $(\theta - \phi)$ is produced. The dc error signal is fed back via an integrator and V.C.O. to drive the up-down counter until the error signal is nulled. The contents of the up-down counter give a binary representation of the angular position. In this application, it is the ability of the CMOS DAC to multiply an analog value by a digital word that makes the system feasible. For more information on resolver (and synchro) to digital conversion, the reader is referred to reference 18 from which this section is extracted.

6.10.2 Co-Ordinate Conversion

The circuit described here (taken from Reference 19) takes analog co-ordinates in the X-Y cartesian system and adds an angle of rotation to produce new co-ordinates. The basic principles of co-ordinate conversion as described here are used in some resolver to digital converters. A servo loop, such as that described above, is used to determine that angle of rotation which causes the inputs to match a set of reference co-ordinates. As shown in the schematic (Figure 6.10.2), the analog voltage pair (x_{in}, y_{in}) represents the vector $r \angle \theta$ where $r^2 = x^2 + y^2$ and tangent θ = y/x. The two inputs x_{in}, y_{in}—together with $-x_{in}$, $-y_{in}$ obtained from inverting amplifiers A1 and A2—are applied to the CD4052 dual analog multiplexer, which is controlled by the two most significant bits of the binary-coded rotation angle Φ. Each dual multiplexer output signal passes through a unity-gain amplifier, A3 or A4, and then through a tandem of inverting amplifiers (A5, A7, or A6, A8) to the final output.

Each tandem of inverting amplifiers is coupled with an AD7533 multiplying digital to analog converter to make a four-quadrant multiplier: A5 and A7 are coupled with DAC 1 and A6 and A8 are coupled with DAC 2. The digital input to both converters is provided by the remaining bits of Φ. The analog input to DAC 1 is the average of the signals from A4 and A8, and the analog input to DAC 2 is the average of the signals from A3 and A7. The output currents from the cross-fed D/A converters feed the summing junctions of A5 through A8, where they add to the inputs that have been selected by the multiplexer, thus producing the output voltages x_{out}, y_{out}.

All resistances in the circuit are 30 kilohms so it is convenient to use dual in-line packages, like

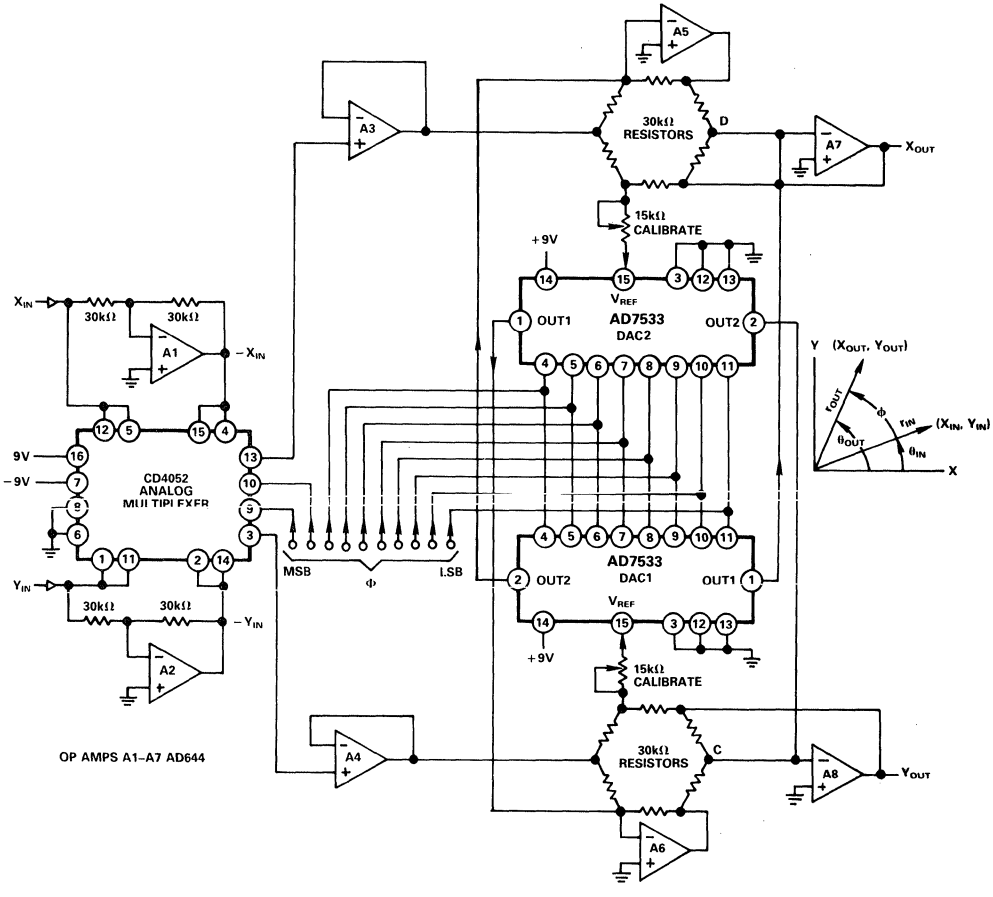


Figure 6.10.2 Co-Ordinate Rotator

Beckman's 698-3, with eight resistors per DIP. Another DIP, Bourn's 7102, could replace the two 15-k trimmers needed to raise the effective input impedance of each AD7533 to $15(2)^{1/2}$ kilohms, the value required in this design.

Regardless of the value of Φ

$$x^2_{out} + y^2_{out} = x^2_{in} = y^2_{in}.$$

In other words, the output vector's magnitude is always equal to that of the input vector. However, the relationship between the input and output vectors is given by $\theta_{out} = \theta_{in} + \Phi'$, where tan $(\Phi'/2)$ is equal to $(2^{1/2} - 1)$. $(\Phi - 45°)/45°$ and Φ is between 0° and 90°. The difference between Φ and Φ– 45° vanishes for Φ = 0°, 45° and 90° and is always less than 1° for other values of Φ in the first quadrant. Note that the error and its variation with angle recur in the other three quadrants. The 45° offset in Φ is due to the bipolar operation of the AD7533 converter. The offset may be corrected by simply adding 45° to the digital equivalent number at the Φ input lines. The remaining error will be small enough to go unnoticed on most graphical displays. To calibrate the vector rotator, x_{in} is set to some constant voltage and set $y_{in} = 0$. Then the trimmers are adjusted to make $x_{out} + y_{out} = 0$ when $\Phi = 0°$ and $x_{out} - y_{out} = 0$ when $\Phi = 90°$.

With the addition of a clock and a counter to make $\Phi = \omega t$, the vector rotator becomes a sine-cosine generator. For example, for a 5-volt-root-mean-square output, x_{in} and y_{in} is set to 5V dc; then $x_{out} = 5(2)^{1/2} \cos \omega t$ and $y_{out} = 5(2)^{1/2} \sin \omega t$.

Because of the functional error in the angle as given by the formula for tan $(\Phi'/2)$, either output will contain third and fifth harmonics each having a magnitude 0.8% that of the fundamental. Total harmonic distortion, therefore, is 1.1%.

This circuit has been used in the design of a low cost electronic compass—see Reference 20.

6.10.3 Using CMOS DACs in an AGC System[22]

In an automatic gain control system, an input signal is attenuated (or amplified) so that its average output level remains constant (Figure 6.10.3). The D/A converter is used here as a variable gain (attenuation) element that adjusts the output signal relative to the input level.

A feedback loop consisting of a detector, comparator, and up-down counter continuously adjusts the contents of the counter, and hence the gain, so that the signal level at the output of the detector remains constant and equal to V_{REF}. The negative feedback action of the loop ensures that the average output voltage of the automatic gain-control system remains constant.

Whenever the input signal level is outside the dynamic range of the programmable gain (attenuation) element of the gain-control system, there should be a stable, well-defined input/output relationship. However, if a simple up-down counter is used, an out-of-range signal causes it to count up continuously—once the counter reaches full scale (all 1's) it increments to the next value (all 0's), which is the zero end of the scale, and this produces a saw-tooth amplitude-modulated output that is determined by the count rate of the automatic gain-control system. To prevent this, the up-down counter should have end-stop logic.

The component values for the circuit depend on the bandwidth of the input signal and the response time of the automatic gain-control loop. The values shown apply for signals in the frequency range of 100Hz to 10kHz. Resistor R2 determines the I/O relationship when overranging occurs (all 0's in the counter), and R3 D2 and R4 D3 limit the outputs of comparators A3 and A4 to positive signals only.

Amplifier A2 and its associated components form the detector, R5 limits the maximum current available from A2 to charge C2, R6 and C2 provide an output voltage droop that is less than the required regulation accuracy of the system, and D1 is the detector diode. The AD584 voltage reference—in conjunction with R7, R8 and R9—determines the upper and lower limits of the output signal level when the automatic gain control is regulated.

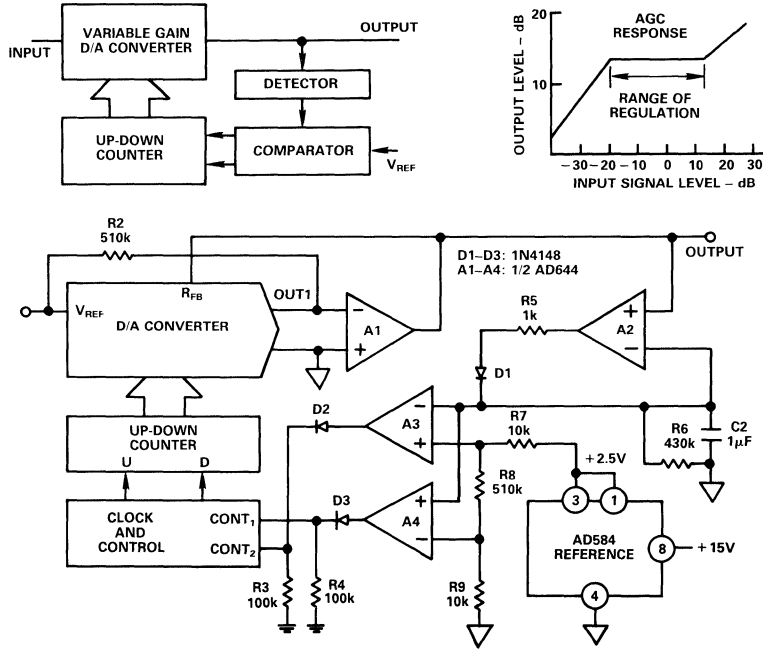


Figure 6.10.3 AGC System

APPENDIX KEY FEATURES AND CONNECTIONS FOR ANALOG DEVICES CMOS DACs

	No. of Pins	DGND	Logic P-Well	DAC Switch P-Well	AGND	OUT2	OUT1
LOGDACs(TM)[2]							
AD7111 (0.375dB Steps)	16	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7115 (0.1dB Steps)	18	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7118 (1.5dB Steps)	14	Pin 8 (DGND)	Pin 8 (DGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 14
8-BIT DAC[2]							
AD7524	16	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
AD7528 Dual 8-Bit DAC	20	Pin 5 (DGND)	Pin 5 (DGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pins 2 & 20
AD7226 Quad 8-Bit DAC	20	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
10-BIT DACs[2]							
AD7522	28	Pin 28 (DGND)	Pin 28 (DGND)	Pin 8 (AGND)	Pin 8 (AGND)	Pin 7	Pin 5
AD7533	16	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
12-BIT DACs[2]							
AD7240	18	Pin 3 (DGND)	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7541A	18	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
AD7542	16	Pin 12 (DGND)	Pin 12 (DGND)	Pin 3 (AGND)	Pin 3 (AGND)	Pin 2	Pin 1
AD7543	16	Pin 12 (DGND)	Pin 12 (DGND)	Pin 3 (AGND)	Pin 3 (AGND)	Pin 2	Pin 1
AD7545	20	Pin 3 (DGND)	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7548	20	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
16-BIT DACs							
AD7546	40	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5

NOTES
[1]Operating a DAC at a voltage other than that for which it is specified may impair its performance – consult factory.
[2]All DACs are specfied in the current steering mode of operation except where stated otherwise.
[3]AD7522 and AD7524 purchased after 1982 do not require protection Schottky diodes.
[4]Not a conventional CMOS multiplying DAC – consult data sheet.
[5]Not a conventional CMOS multiplying DAC – see Section 6.2.4.

This Appendix is not a product specification and is for design guidance only. Consult product data sheet for full information.

Ladder Termination Connections	RDAC Min/Max kΩ	Protection Schottky Required	Specified Operating Voltage(s)	Operating Voltage Range[1]	Operating Voltage Range for TTL Compatibility	Description of Logic Structure and Other Comments
AGND (Pin 2)	9/15	No	+5	+5	+5	8-Bit Latched Data
AGND (Pin 2)	7/18	No	+5	+5	+5	2 1/2 Digit Latched BCD
AGND (Pin 1)	9/17	No	+5 & +15	+5 to +15	+5	6-Bit, No Latches
GND (Pin 3)	5/20	Note 3	+5 & +15	+5 to +15	+5	8-Bit, with Data Latches Can Be Made Transparent
AGND (Pin 1)	8/15	No	+5 & +15	+5 to +15	+5	Data Latches for Each DAC
Note 4	Note 4	Note 4	+15	11.4 to 16.5	11.4 to +16.5	Includes Output Amplifiers and Data Latches
Pin 2	5/20	Note 3	V_{DD} = +15 V_{CC} = +5	+12 to +15	+12 to +15 V_{CC} = +5	Double Buffered
GND (Pin 3)	5/20	No	+15	+7 to +15	+7 to +15	No Latches
						Specified in Voltage Switching Mode
AGND (Pin 2)	7/15	No	+15	+7 to +15	+7 to +15	No Latches
GND (Pin 3)	7/18	No	+15	+7 to +15	+7 to +15	No Latches
AGND (Pin 3)	8/25	No	+5	+5	+5	3 × 4-Bit Nibble Load
AGND (Pin 3)	8/25	No	+5	+5	+5	12-Bit Serial-In
AGND (Pin 2)	7/25	No	+5 & +15	+5 to +15	+5	12-Bit Parallel in with Data Latches
AGND (Pin 2)	7/20	No	+5, +12 & +15	+5 to +15	+5 to +15	8-Bit + 4-Bit (i.e., Two Byte) Load Double Buffered
Note 5	Note 5	Note 5	+15	+15	+15	16-Bit Parallel in with Data Latches

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