

Am2971/Am2971A

Programmable Event Generator (PEG)TM



PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Generates arbitrarily defined output sequences on 12 parallel outputs
- Timing resolution down to 10 ns
- Internal frequency-multiplying Phase-Locked Loop (PLL)
- Crystal-controlled on-chip oscillator (Am2971A only)
- Programmable trigger polarity and STOP function

GENERAL DESCRIPTION

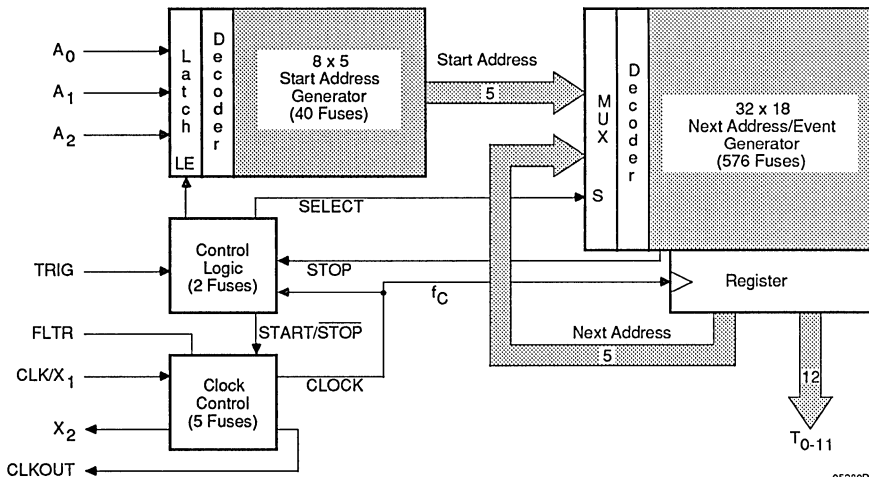
The PEG is a versatile source of 12 simultaneous timing sequences. It can act as a digital substitute for multiple tapped delay lines or as a general-purpose user-programmable waveform generator.

Timing is derived from an external TTL source or an on-chip crystal oscillator (Am2971A only), combined with an on-chip programmable frequency-multiplying PLL and

clock divider. This achieves excellent timing resolution, down to 10 ns, from low-cost stable frequency sources of 10 MHz or less. The PEG uses platinum-silicide fuse technology and is programmed similar to any other AMD PROM.

The two PEG versions available are the Am2971 and Am2971A (see Table 7 for a comparison).

BLOCK DIAGRAM



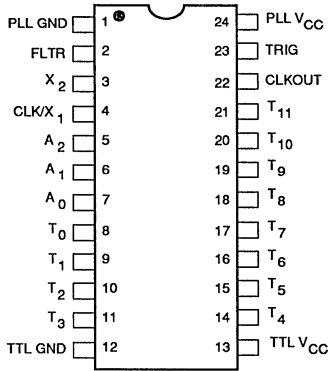
05280D-1A

Am2971/Am2971A

Advanced Micro Devices

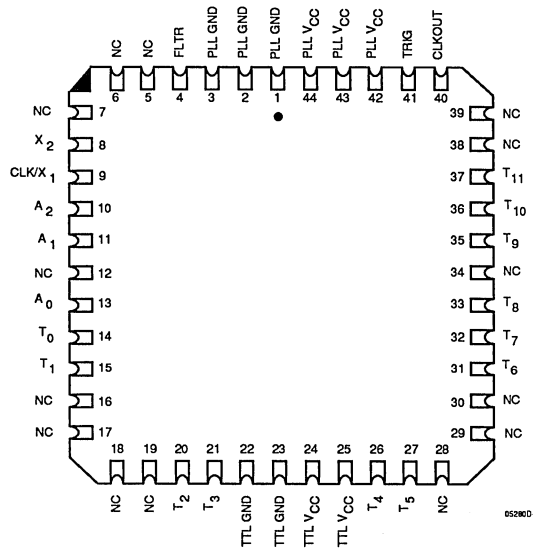
CONNECTION DIAGRAMS

DIP*



05280D-2A

LCC**

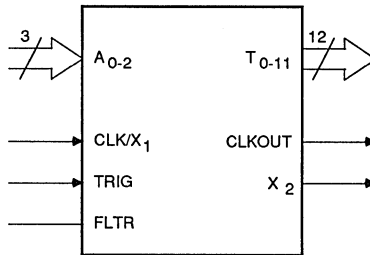


05280D-3A

* Also available in Flatpack; pinout is identical to DIP.

** Top View, JEDEC type-C package (NC = No Connection)

LOGIC SYMBOL



05280D-4A

Approximate Gate Count: 100

Die Size: 0.173" x 0.257"

Thermal Characteristics

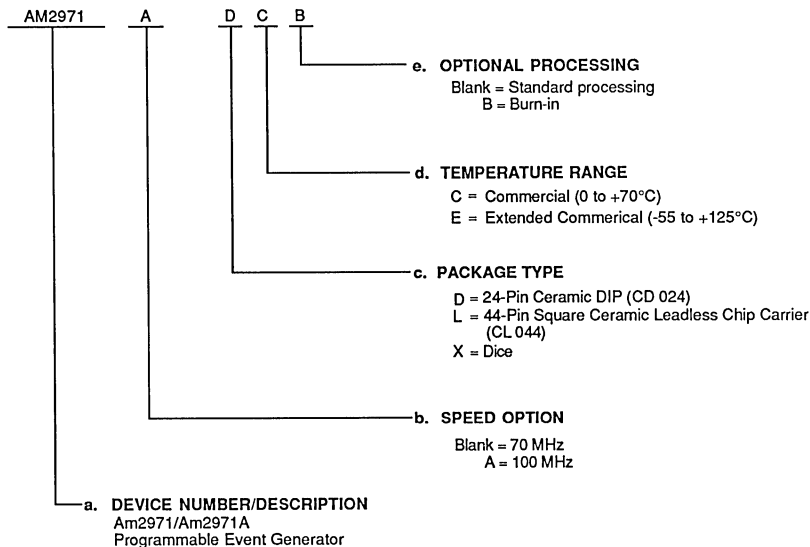
	24-Pin Ceramic DIP	24-Pin Ceramic Flatpack	44-Pin Ceramic LCC	Unit
θ_{JC} Max.	11	8	15	°C/W
θ_{JA} Max.	49	99	75	°C/W

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2971	DC, DCB, LC, LCB, XC
AM2971A	DC, DCB, DE, LC, LCB, LE, XC

Valid Combinations

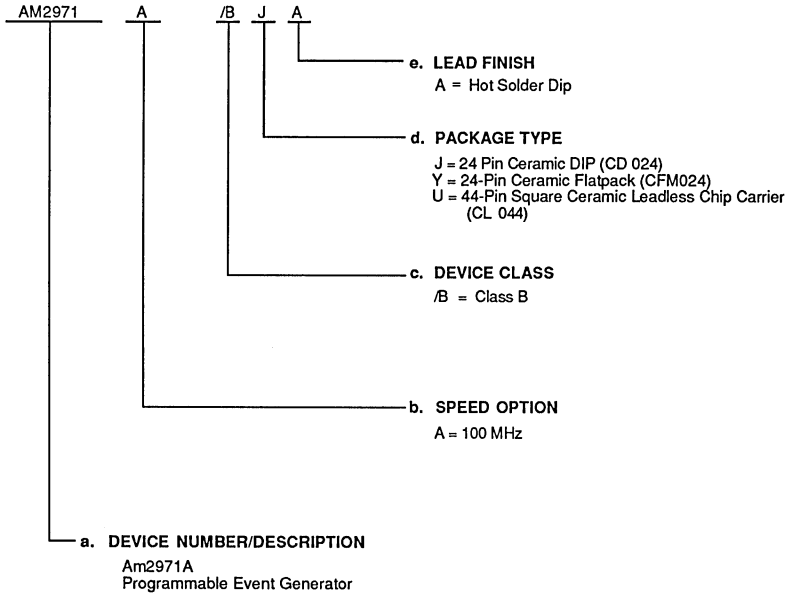
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defence applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM2971A	/BJA, /BYA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_0 – A_2 Addresses (Inputs)

These three bits access the Start Address Generator which contains eight user-programmed start locations. Each cycle starts at the location pointed to by the Start Address Generator word selected by the A_0 – A_2 inputs. In the Program Mode, these inputs are unused and may be allowed to float.

CLK/ X_1 and X_2 Clock/Crystal (Input/Output)

A TTL-level clock may be applied to the CLK/ X_1 input, with the X_2 output left floating, or an AT-cut parallel resonant crystal may be connected between these two pins (Am2971A only).

CLKOUT Output Clock (Output)

CLKOUT is a clock output pin which may be used for system reference. The output frequency for CLKOUT (f_o) is fuse-programmable to be either 0.5, 1, or 2 times the input frequency. This output is not valid in the Bypass Mode. In the Program Mode a high-voltage pulse is applied to CLKOUT to blow selected fuses.

FLTR Filter

This pin is used to connect a 0.47- μ F filter capacitor between the Phase-Locked Loop and ground when an external crystal is used or the PLL is selected. When clocking the PEG with an external TTL source greater than 10 MHz in the Bypass Mode, this pin should be tied LOW. See Figure 8 for proper device decoupling with the PLL Bypassed.

T_0 – T_{11} Timing Outputs (Outputs; Active HIGH)

These are the twelve timing outputs which follow a user-programmed timing pattern. They are registered for glitch-free operation. In the Program and Verify Modes, T_0 – T_{10} function as address inputs to access each individual fuse. T_0 – T_5 serve as Row Address inputs, and T_6 – T_{10} serve as Column Address inputs (see Table 6). After power-up, these outputs are all LOW. T_{11} functions as data input in the Program Mode and as data output in the Verify Mode.

TRIG Trigger (Input)

The timing cycle of the PEG can be started by either the rising or falling edge of the start (TRIG) pulse; the polarity is defined as a fuse option (fuse #621) in the TRIGGER POLARITY block. The trailing edge of the start (TRIG) pulse stops the timing sequence if the STOP TRIG fuse (fuse #622) is left unprogrammed (0).

Power, Ground TTL/PLL Power Pair

There are two sets of V_{cc} and ground pins. One power pair is used by the PLL (Phase-Locked Loop) and the internal ECL circuitry. The other power pair is used by the remainder of the chip (TTL). Surface-mount packages have additional supply connections. All power and grounds must be connected regardless of mode of operation.

FUNCTIONAL DESCRIPTION

The leading edge of the trigger pulse (polarity is fuse-programmable) causes the continuously running internal clock to step through the on-chip PROM addresses, starting at one of eight fuse-programmed locations selected by the A_0 – A_2 inputs.

Each addressed PROM location generates a fuse-programmed 12-bit pattern on the T_0 – T_{11} outputs, and internally generates the fuse-programmable next PROM address as well as a fuse-programmable STOP bit, if desired. Since there is no program counter, there is an almost infinite number of ways of programming the PEG for any desired output pattern. The user will most likely choose an ascending address sequence, but this is only one of many arbitrary choices.

The address sequence can loop but cannot execute conditional jumps.

The sequence of operations stops either as a result of the trailing edge of the trigger pulse (if so enabled by a fuse) or by the programmable STOP bit. A new sequence can only be started after the previous sequence has stopped.

The internal clock frequency, f_c (see Operational Description for an explanation of all internal and external signal frequencies), is derived from and is proportional to the frequency on the X_1 input, which is either an external TTL signal or the resonant frequency of a crystal connected between X_1 and X_2 . Controlled by programmable fuses, the frequency on X_1 is either used directly or is first multiplied by a factor of 1.25, 2.5, 5, or 10 to generate the internal clock frequency. A clock

output is available; its frequency (fuse-programmable) is either half, double, or equal to the frequency on X_1 . This output is not valid in the Bypass Mode.

Operational Description

Frequency Definitions

To avoid confusion, the definitions of the various frequencies associated with the PEG are given below:

- f_i = This is the user's Input Frequency into the CLK/ X_1 pin.
- f_o = This is the PEG's Output Frequency at the CLKOUT pin. A CLKOUT signal is valid only when the PLL is used.
- f_c = This is the Internal Clock Frequency, which is gated into the event generator state machine. When a timing sequence has been stopped, there is no f_c .
- f_A = This is the Internal Altered Input Frequency, which is equivalent to f_c in value. This frequency is always generated, but it is not gated to the state machine (thus becoming f_c) unless a sequence is started.
- f_{PLL} = This is the Phase-Locked Loop Frequency ($f_i \times 5$ or $f_i \times 10$).

TRIG-to-Output Delay

Operation of the PEG is initiated by a transition (of programmed polarity) on the TRIG input. This transition starts a series of internal events which lead to the clocking of the T_0-T_{11} output registers and to programmed changes on these outputs.

There are two possible conditions:

If the TRIG transition is synchronous with the frequency on X_1 (i.e., X_1 is a TTL clock signal and TRIG is synchronized with it), then the TRIG-to-output delay can be well-controlled, but the designer must analyze the timing and programming relationship carefully, as described below.

In the more normal case where TRIG is asynchronous to the frequency on X_1 , the TRIG-to-output delay can be described very simply, but it has an unavoidable uncertainty of one internal clock period.

Trigger Asynchronous

Start Delay

The delay from the active trigger edge to the first possible change of output pattern on T_0-T_{11} is the sum of:

- 1) Propagation delays in the trigger circuit plus output driver,
- 2) Up to one clock period of f_A due to the asynchronous relationship between TRIG and f_A , and
- 3) One clock period of f_A (used internally to prevent metastable operation).

Stop Delay

A timing sequence can be stopped either by the trailing edge of the start (TRIG) pulse (if so enabled by leaving fuse #622 unprogrammed) or by a programmed STOP bit in the Next Address/Event Generator fuse block.

The timing sequence stops when it detects either or both of these conditions. If stopped by a programmed STOP bit, the outputs remain at the level that is programmed in the same address location as the STOP bit. If stopped from the TRIG input, there is a delay equivalent to the starting delay.

Trigger Synchronous

Detailed Analysis of the Start and Stop Timing Sequences

The operation of the TRIG function can best be described by a synchronous state machine which uses f_A as the clock. All transitions occur on the rising clock edge. Figure 1 is the state diagram, Figure 2 the equivalent timing diagram. The state diagram uses the terms "active" and "inactive" edges of TRIG, since the actual polarity of TRIG is user-programmable.

State A is the idle state, after a reset or after operation has stopped for more than two periods of f_A . In state A, Select and f_C are HIGH (i.e., the Next Address/Event Generator PROM is addressed from the Start Address Generator PROM), but the output registers are not clocked; they retain their previous value.

When TRIG goes active, the next rising edge of f_A forces the state machine into state B and causes f_C to be equal to f_A . The output registers are still not clocked.

The next rising edge of f_A forces the state machine into state C, clocks the output from the Next Address/Event Generator PROM into the output register and forces Select LOW. Subsequent cycles use the registered "next address" output as an address to the Next Address/Event Generator PROM. State C lasts until a STOP condition is encountered.

When a STOP condition is encountered, the next rising edge of f_C forces the state machine into state D. If TRIG goes active while the state machine is in state D, the next rising edge of f_A will cause it to go to state B; otherwise it will go to state A.

The shortest possible sequence is A-B-C-D-A, staying one f_A period in states B, C, D.

The fastest possible retrigger goes C-D-B-C, staying one f_A period in states D and B, at frequencies below 50 MHz. At frequencies greater than 50 MHz, the PEG will stay two clock periods in state D.

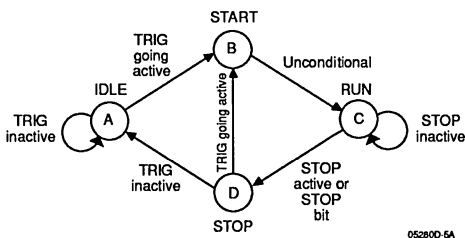


Figure 1. State Machine Diagram

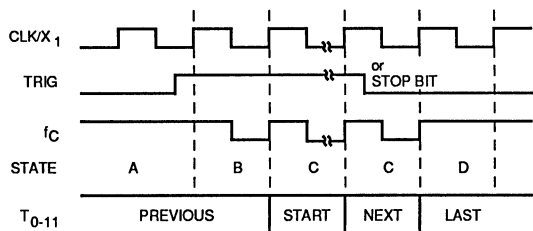


Figure 2. State Machine Timing (Bypass Mode)

Start and Stop Timing Synchronous With f_1

The following paragraphs describe in detail the timing relationship and requirements between TRIG and the output changes on T_{0-11} , provided that TRIG is synchronous with f_1 .

Bypass Mode ($f_c = f_1$)

TRIG must change from inactive to active for a specified setup time before the rising edge on X_1 and must stay active at least until 5 ns after the next subsequent rising edge on X_1 . If the inactive-going edge of TRIG is programmed as a STOP condition, the shortest legitimate TRIG pulse will cause the state machine to cycle from state A to B to C to D, clocking the output register twice (first with the code accessed by the start address, then with the code accessed by the "next address" bits). If TRIG lasts additional X_1 clock periods, the state machine will spend this additional time in state C and the PEG will step through more codes.

PLL x5 or x10 Mode

When the f_{PLL} output is used as f_A , either 5 or 10 internal clock cycles occur for every f_1 clock cycle. Since f_A is phase-

synchronized to the rising edge of X_1 , the timing analysis is very similar to the previous one, with f_A substituted for periods on X_1 . The setup times associated with f_1 also apply to f_A , since f_A is in phase with f_1 . If the TRIG setup time with respect to X_1 exceeds one f_{PLL} period, then the state machine may trigger on the earlier internal clock. Because of the spread of guaranteed device parameters, an uncertainty is introduced. Thus, using the "STOP-from-TRIG" feature to generate a predetermined number of output sequences could result in an incorrect number of transitions (either more or less).

+2 or +4 Mode

In this mode the rising transitions of f_A are no longer uniquely related to the rising transitions of f_1 or f_{PLL} , since the +2 counter can be in either of two starting states and the +4 counter can be in any one of four possible starting states.

The START and STOP sequences, therefore, have an additional unpredictable delay of either a 0 or 1/2 period of f_A (if +2 is chosen), or either a 0, 1/4, 1/2, or 3/4 period of f_A (if +4 is chosen).

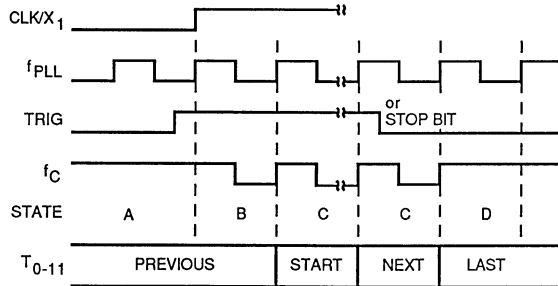


Figure 3. PLL Mode

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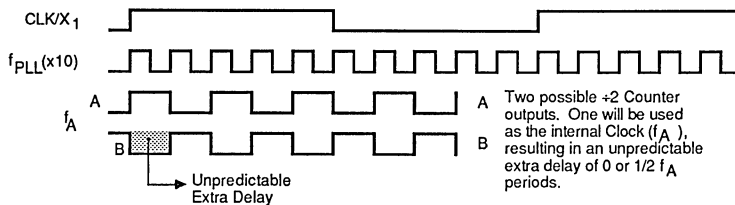


Figure 4. +2 Mode

05280D-8A

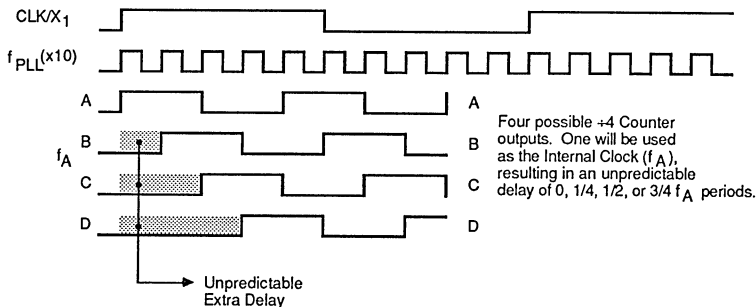


Figure 5. +4 Mode

05280D-9A

Output Skew and Jitter

The twelve timing waveform outputs (T_0-T_{11}) are synchronized internally in an output register in order to minimize output skew.

The guaranteed maximum value for the remaining skew is specified by parameters 6–10 in the Switching Characteristics Table (depending upon the PEG version used and the number and type of transitions).

See Switching Characteristics for tighter skew specifications of certain outputs. More closely matched outputs should be used for more critical timing.

Any oscillator, and especially a Phase-Locked Loop, exhibits a certain amount of jitter — random phase modulation of the internal clock. Such jitter affects all outputs together (synchronously).

Jitter is typically less than ± 1.0 ns for the ceramic DIP and Flatpack, and less than ± 0.5 ns for the LCC package.

Output Event Resolution

Each of the twelve timing waveform outputs (T_0-T_{11}) can be programmed to change on any rising edge of the internal clock frequency (f_c), with the following restrictions:

The maximum operating frequency of the Am2971 is 85 MHz if the PLL is bypassed, all outputs in use. Thus, an output resolution of 24 ns is established for transitions of the same output, and 12 ns between transitions of different outputs. When the PLL is selected, the maximum f_i is 70 MHz, thus establishing an output resolution of 30 ns for transitions of the same output, and 15 ns between transitions of different outputs.

The Am2971A has a maximum operating frequency of 100 MHz with a TTL source, all outputs in use. An output resolution of 10 ns for transitions of the same output or between transitions of different outputs is obtainable when a maximum of nine outputs (any nine) are switched simultaneously. If more than nine outputs are used, resolution within the same output is 20 ns, and 10 ns between outputs. If a crystal is used to clock the Am2971A, all outputs may be used, but only six outputs (any six) can be programmed to switch simultaneously. The output resolution with six outputs switching can be 10 ns within or between outputs. At internal frequencies less than 85 MHz, there are no programming restrictions (all outputs can switch simultaneously).

**TABLE 1. OUTPUT RESOLUTION
(BETWEEN SUCCESSIVE TRANSITIONS OF THE SAME OUTPUT)**

Number of outputs switching simultaneously			12, 11, 10	9, 8, 7	6, 5, 4, 3, 2, 1
TTL Clock Source	Am2971A	PLL	20 ns	10 ns	10 ns
		Bypass			
	Am2971	PLL	30 ns	30 ns	30 ns
		Bypass	24 ns	24 ns	24 ns
Crystal Clock Source	Am2971A	Not Allowed	Not Allowed	10 ns	
	Am2971			Not Allowed	

Oscillator

The Am2971A contains an inverting linear amplifier which can be used as a crystal oscillator. Various types of crystals are available, and the manufacturers' literature should be consulted to determine the appropriate type. The on-chip oscillator is not available on the Am2971.

Crystal frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32 pF), or to specify the load when ordering a special crystal.

The circuit of a typical 1st-harmonic oscillator is shown in Figure 6. The crystal load is comprised of the two 68-pF

capacitors effectively in series. This 34 pF approximates the standard 32-pF crystal load. If a closer match is required, one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer.

A typical crystal specification for use in this circuit is:

Frequency Range: 2–20 MHz
Resonance: AT, Parallel Resonant Mode
Load: 32 pF
Stability: to match system requirements

In order to eliminate stray pick-up, it is good practice to ground the case of the crystal and to keep all connections as short as possible.

At fundamental frequencies below 6 MHz, the crystal might accidentally operate in 3rd-harmonic mode. To prevent this, a resistor should be added in series with the X₂ pin as shown in the circuit diagram (Figure 6).

The resistor value should equal the impedance of C:

$$R = XC = \frac{1}{2\pi f C} = \frac{2342 \Omega}{f(\text{MHz})} \quad \text{Example: } R = 390 \Omega \text{ for } 6 \text{ MHz}$$

Design Considerations

- 1) Oscillator external connections must be less than 1" long — wirewrap is not recommended.
- 2) V_{CC} and GND connections to power plane should be less than 1/2" long.
- 3) Effective supply decoupling over a broad frequency range is mandatory (Reference Figures 7 and 8).

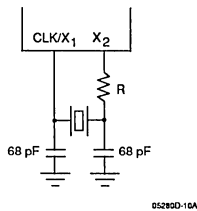


Figure 6. Am2971A Crystal Oscillator Circuit

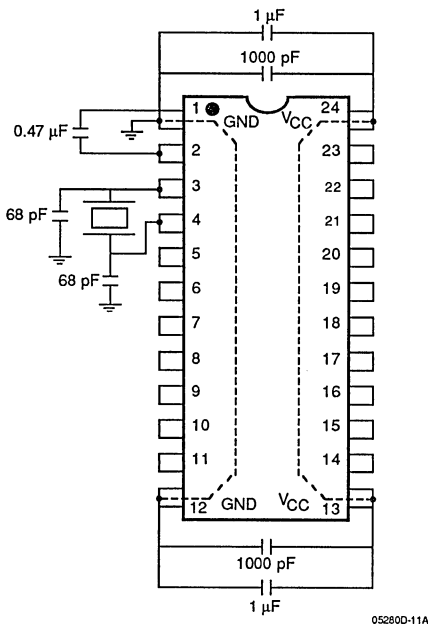


Figure 7. Am2971A Recommended Layout and Decoupling (Crystal Input)

Bypass Mode Decoupling

When using the PEG with a direct TTL source above 10 MHz with the PLL bypassed, the decoupling shown in Figure 8 is mandatory.

The decoupling of the FLTR (filter) pin is necessary at frequencies higher than 10 MHz because the PLL will attempt to lock onto the incoming clock signal at CLK/X₁. This can cause anomalies in device operation and increase device jitter. Grounding the FLTR pin will isolate the PLL from the incoming clock and permit proper operation of the PEG.

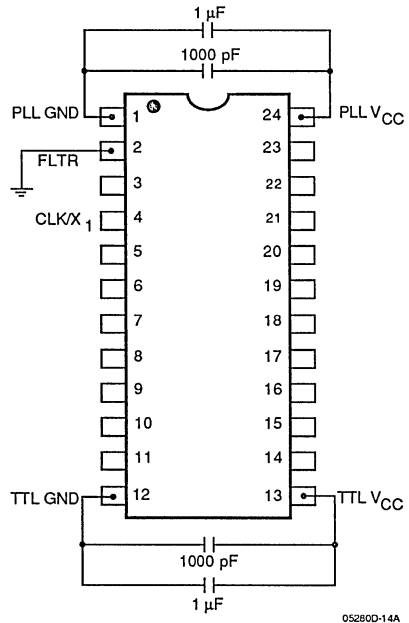


Figure 8. PEG Decoupling With PLL Bypassed

PROGRAMMING

JEDEC Fuse Map

Table 6 shows the JEDEC fuse map and describes the fuse-addressing mechanism. For programming purposes the fuses are addressed by using T₀–T₁₀ as inputs.

Each of the 622 fuses is addressed individually and programmed (output HIGH) or left unprogrammed (output LOW) by the equivalent level on T₁₁.

The fuses are addressed by a row/column matrix:

Input signals on pins T₀–T₅ define the row (T₀ = LSB, T₅ = MSB).

Input signals on pins T₆–T₁₀ define the column (T₆ = LSB, T₁₀ = MSB).

(Table 6 uses decimal notation for rows and columns. Note that there is no direct relationship between the row and column addresses and the fuse number. The fuse number is only used to refer to a particular fuse.)

In the Next Address/Event Block, each row describes the fuses used in one event. The bits accessed by columns 0 to 4 represent the Next Address column (address 0 accesses the LSB of the next address), the bits accessed by columns 5 through 16 represent the 12 output levels (column address 5 accesses the bit that uses T_o as an output), and column address 17 accesses the STOP bit.

In the Start Address Block, the eight starting addresses are programmed by row addresses 32–39 (row address 32 programs the 5-bit word that defines the starting address selected by a 0 on the A_0 – A_2 inputs, row address 39 programs the word that defines the starting address selected by a 7 on the A_0 – A_2 inputs).

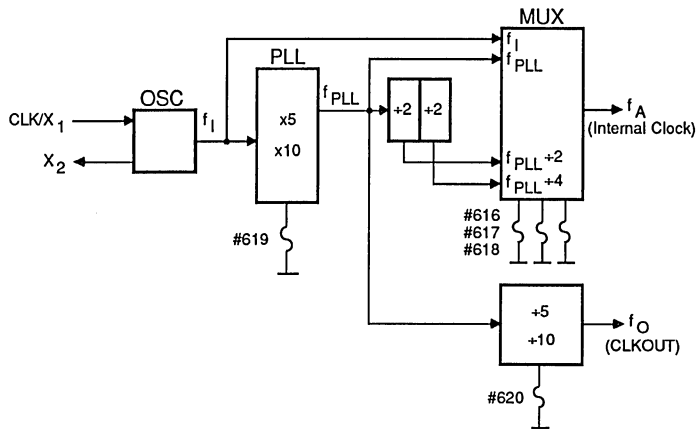
The Control Fuses (Reference Tables 2 and 6, and Figure 9) are accessed by row address 40 and column addresses 23–29. The functions of these fuses are described below:

- Fuse #616:** 0 = Divide-by-2 divider is not selected
1 = Divide-by-2 divider is selected (#617 must be zero)
- Fuse #617:** 0 = Divide-by-4 divider is not selected
1 = Divide-by-4 divider is selected (#616 must be zero)
- Fuse #618:** 0 = f_A is generated from PLL output
1 = $f_A = f_i$
- Fuse #619:** 0 = PLL multiplies by 10
1 = PLL multiplies by 5
- Fuse #620:** 0 = $f_o = f_{PLL}$ divided by 10
1 = $f_o = f_{PLL}$ divided by 5
- Fuse #621:** 0 = Start on rising edge of TRIG
1 = Start on falling edge of TRIG
- Fuse #622:** 0 = Stop on trailing edge of TRIG (polarity defined by #621)
1 = No stop on trailing edge of TRIG

TABLE 2. CLOCK LOGIC CONTROL FUSES

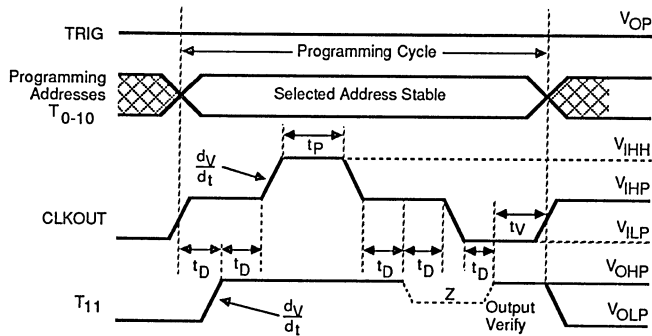
Fuse Pattern					Internal Clock f_A (f_i)	CLKOUT f_o
#616	#617	#618	#619	#620		
0	0	0	0	0	10	$X f_i$
1	0	0	0	0	5	$X f_i$
0	1	0	0	0	2.5	$X f_i$
0	0	0	0	1	10	$X f_i$
1	0	0	0	1	5	$X f_i$
0	1	0	0	1	2.5	$X f_i$
0	0	0	1	0	5	$X f_i$
1	0	0	1	0	2.5	$X f_i$
0	1	0	1	0	1.25	$X f_i$
0	0	0	1	1	5	$X f_i$
1	0	0	1	1	2.5	$X f_i$
0	1	0	1	1	1.25	$X f_i$
X	X	1	0	0	1	$X f_i$
X	X	1	0	1	1	$X f_i$
X	X	1	1	0	1	$X f_i$
X	X	1	1	1	1	$X f_i$
1	1	X	X	X	Illegal code	

Note: f_i is the frequency on the X_i input.



05280D-12A

Figure 9. Clock Logic Control Fuse Locations



05280D-13A

Figure 10. Programming and Verify Mode Timing

Programming Procedure

The following section describes the hardware requirements for programming the PEG.

This information is supplied for the designer of programming equipment. Normally the user of a PEG will utilize commercially available programming equipment and therefore has no need to study these pages (programming equipment information can be found in Table 3).

The PEG, like all AMD bipolar PROMs and PALs®, is programmed by selectively blowing platinum-silicide fuse links, one link at a time.

The table of programming parameters specifies not only the required voltage levels, but also the delays between the various actions (rise times for T_{11} and CLKOUT), and the length of the programming pulse t_p .

During the program and verify operation, TRIG must be pulled to V_{op} (15 V) which disables the T_0 - T_{11} and CLKOUT outputs.

The fuse to be programmed (or verified) is selected by applying Row and Column addresses (see Figure 10) to T_0 - T_{10} . (T_0 is the LSB of the Row address, T_6 is the LSB of the Column address.) The selected fuse is programmed (blown, changed from 0 to 1) by a logic HIGH on T_{11} and a V_{IH} pulse (12 V, 40–100 μ s) on CLKOUT. It is common practice to verify each fuse-programming operation by three-stating the signal driving T_{11} and then applying a LOW level to CLKOUT. A blown link is indicated by a HIGH output on T_{11} .

Most links will open within the specified programming time. Occasionally a link might be stronger and require an additional programming pulse of longer duration (4 to 10 ms).

After the link has been verified, programming proceeds to the next link. After all links have been programmed, the entire array should be verified. An unprogrammed fuse (0) is indicated by a LOW on T_{11} ; a programmed fuse (1) by a HIGH on T_{11} .

All unprogrammed (unblown) fuses are 0.

An unprogrammed fuse in the Next Event/Address Block generates a LOW on the outputs and a 0 as the next address. (The user can take advantage of this fact to "repair" a program error. For example: If address 31 had been left unprogrammed, any erroneously programmed location (0-3) can be moved to address 31 by programming the additional "1"s in the Next-Address field of the preceding word.)

Table 3 is a list of recommended suppliers for Am2971/A programming support. Each supplier is required to complete qualification by AMD to ensure high programming yields. An asterisk indicates a certified supplier (qualification complete). Consult your AMD Sales Representative to determine the current status of vendors noted as TBD or for other available models.

TABLE 3. PROGRAMMING EQUIPMENT INFORMATION

Supplier and Location	Programmer Model(s)	Personality Modules	Socket Adaptors	Development Software
*Digelec, Inc. Ocean, NJ 201-493-2420	u803B	FAM 12	DA 42	—
	860	—	—	—
Stag Microsystems Santa Clara, CA 800-227-8836 800-222-7824	ZM 2200	—	—	—
Varix, Inc. Dallas, TX 214-437-0777	SP 0300	—	—	—
	GP 1140			
*AMD, Inc. Sunnyvale, CA 800-538-8450	Data I/O Model 29/B	UniPak™ 2/2B	AmPEGASUS™	AmPEGPDS
Inlab, Inc. Broomfield, CO 800-237-6759	Inlab 28	—	—	A.C.E.
Kontron, Inc. Mountain View, CA 415-965-7020	EPP80	UPM/B	—	—
Minato, KK Tokyo, Japan	TBD	TBD	TBD	—
Data I/O, Inc. Redmond, WA 206-881-6444	UniSite™ 40	—	—	—

* Certified supplier (qualification complete).

TABLE 4. PROGRAMMING PROCEDURE

Step	Item	Description
1	Determine location of fuses which are to be blown	
2	Set TRIG = V_{OP}	This disables T_0-T_{11} as outputs and prepares the chip for programming.
3	Set CLKOUT = V_{IHP}	This will three-state T_{11} and cause it to float up to V_{IHP} .
4	Set $T_{11} = V_{IHP}$ after t_d	This prepares T_{11} to accept the programming current which will be gated through CLKOUT.
5	Set CLKOUT = V_{IHH} after t_d for a programming time, t_{PF}	This gates the programming current to T_{11} .
6	Set CLKOUT = V_{IHP}	This removes the programming current from CLKOUT.
7	Remove applied voltage from T_{11}	This sets up T_{11} as output for Program Verification.

TABLE 5. PROGRAMMING VERIFICATION PROCEDURE

Step	Item	Description
1	Set TRIG = V_{OP} after t_d	TRIG remains at V_{OP} during the entire programming/verify cycle.
2	Set CLKOUT = V_{ILP} after t_d	This enables T_{11} as an output.
3a	Verify $T_{11} = V_{OHP}$ (Note 1)	This condition occurs if programming has been successful.
3b	Verify $T_{11} = V_{OLP}$ (Note 2)	This condition occurs if programming has been unsuccessful.

- Notes:
1. If verify indicates programming has been successful, proceed to the next fuse and program using the programming steps of the previous table.
 2. If verify indicates programming has been unsuccessful, return to the same fuse and re-attempt programming using the programming time t_{PS} .

PROGRAMMING PARAMETERS ($T_A, T_C = +25^\circ\text{C}$)

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit	
V_{IHH}	Control Pin Extra HIGH Level	11	12	13	V	
V_{OP}	Program Voltage at 15–200 mA	14	15	16	V	
V_{IHP}	Input HIGH Level During Programming and Verify	2.4	5	5.5	V	
V_{ILP}	Input LOW Level During Programming and Verify	0	0.3	0.5	V	
V_{CCP}	V_{CC} During Programming @ $I_{CC} = 250$ mA	COM'L	5	5.2	5.5	V
		MIL/E-COM'L	5	5.2	5.5	
dV_{T11}/dt	Rate of Output Voltage Change (T_{11} , Rising Edge)	20		250	V/ μs	
dV_{CLKOUT}/dt	Rate of Fuse Enable Voltage Change (CLKOUT Rising Edge)	100		1000	V/ μs	
t_p	Programming Time First Attempt, t_{PF}	40	50	100	μs	
	Programming Time Subsequent Attempts, t_{PS}	4	5	10	ms	
t_D	Delays Between Various Level Changes	100	200	1000	ns	
t_V	Period During which Timing Output, T_n is Valid for Program Verification			500	ns	
V_{OHP}	Output HIGH Level During Programming and Verify	2.5	5	5.5	V	
V_{OLP}	Output LOW Level During Programming and Verify	0	0.3	0.4	V	

Notes: 1. Parameters are not tested, but are guaranteed by design.

TABLE 7. PEG COMPARISON

Parameter Description	Am2971	Am2971A
Max. Operating Frequency	70 MHz	100 MHz
Max. 12-Output Skews:		
LOW-to-HIGH	3.5 ns	2.5 ns
HIGH-to-LOW	5.0 ns	2.5 ns
Opposite	8.5 ns	6.5 ns
Max. Matched Output Skews: *		Down to:
LOW-to-HIGH	5.0 ns	1.0 ns
HIGH-to-LOW	5.0 ns	1.0 ns
Opposite	8.5 ns	6.5 ns
I_{CC} , Maximum	310 mA	425 mA
On-Chip Crystal Oscillator	No	Yes
Minimum Output Resolution:		
Between Outputs	15 ns	10 ns
Same Output	30 ns	10 ns

* See AC Switching Characteristics.

Peg Support

AmPEGASUS

AMD's PEG Adaptor Socket and Universal Software (AmPEGASUS) is a passive programmer adaptor socket made for use in conjunction with Data I/O Corporation's Model 29/29A/29B Universal Programmer equipped with a UniPak 2/2A/2B adaptor. This passive unit makes use of the generic 2K x 8 PROM socket by reassigning the PROM configuration into a PEG pin configuration and programming algorithm. The socket draws its power from the Model 29 and contains protective circuitry to provide additional safeguards for the Unipak. Additional information can be obtained from the AmPEGASUS User's Manual, PID # 09241A.

AmPEGCPS

AMD's PEG Custom Programming Service (AmPEGCPS) provides fully tested, pre-programmed PEGs as defined and requested by customers for customer-specific applications. PEG devices programmed by this service are produced after receipt of a customer-validated Verification Approval/Production Release Form available from any AMD Sales Representative.

AmPEGPDS

AMD's PEG Programming Development Software (AmPEGPDS) is a software tool designed to aid the user in creating a fuse map in the JEDEC standard for programming a PEG device. The main purpose of the software is to create and translate the input specification into a format that can be accepted by the programmer. The input specification is created by the designer using AmPEGPDS as an editor. AmPEGPDS is available on a standard 5-1/4" floppy disk, included in both of the PEG Application Kits described as follows.

PEG Application Kits

The **PEG Starter Kit** includes:

- Am2971/A PEG Data Sheet
- AmPEGPDS
- AmPEGPDS Software User's Manual
- Two PEG Unprogrammed Samples
(customer to specify Am2971
or Am2971A)
- Applications Articles
- Am2971 Product Description

The PEG Starter Kit is available free of charge from any AMD Sales Representative.

The **PEG Design Kit** includes the **PEG Starter Kit** plus:

- AmPEGASUS Programming Adaptor
Socket (customer to specify DIP or LCC)
- AmPEGASUS Translation Software
- AmPEGASUS User's Manual

Consult your AMD Sales Representative for pricing information on the PEG Design Kit.

PEG Updates

"PEG Updates" is a newsletter distributed by AMD to PEG customers who complete and return the response card in the PEG Product Description, PID # 08697A. This newsletter publishes changes/upgrades to the PEG Programming Development Software (implemented as data is collected from the many systems now being designed with PEGs) to keep customers up-to-date on changes. Also included are new documentation, application notes and ideas, and advance information about new PEG versions which will become available in the future.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage to Ground Potential Continuous (TLL and PLL V_{CC})	0 to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	0 to + V_{CC} Max.
DC Input Voltage	-0.5 to +5.5 V
DC Input Current	-18 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T_A)	0 to +70°C
TLL and PLL Supply Voltage (V_{CC})	5.0 V \pm 10%
Min.	4.5 V
Max.	5.5 V

Military* (M) or Extended Commercial (E) Devices	
Case Temperature (T_C)	-55 to +125°C
TLL and PLL Supply Voltage (V_{CC})	5.0 V \pm 10%
Min.	4.5 V
Max.	5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C .

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)*		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 8 \text{ mA}$		0.4	V
V_{IH} (Note 2)	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs		2.0		V
V_{IL} (Note 2)	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_{IHc}	Input HIGH Voltage to CLK/ X_1	Guaranteed Input HIGH Voltage for All Inputs		3.0		V
V_{ILc}	Input LOW Voltage to CLK/ X_1	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_I (Note 2)	Input Clamp Voltage	$V_{CC} = \text{Min.}$	$I_{IN} = -18 \text{ mA}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Min.}$ $V_{IN} = 3.0 \text{ V}$	CLK/ X_1		700	μA
		$V_{CC} = \text{Max.}$ $V_{IN} = 2.7 \text{ V}$	A_0 - A_2 and TRIG		20	
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$ $V_{IN} = 0.5 \text{ V}$	CLK/ X_1		-500	μA
		$V_{CC} = \text{Max.}$ $V_{IN} = 0.5 \text{ V}$	A_0 - A_2 and TRIG		-250	
I_I	Input Current	$V_{CC} = \text{Min.}$ $V_{IN} = 4.0 \text{ V}$	CLK/ X_1		1.2	mA
		$V_{CC} = \text{Max.}$ $V_{IN} = 5.5 \text{ V}$	A_0 - A_2		100	μA
		$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.5 \text{ V}$	TRIG		100	

DC CHARACTERISTICS (Cont'd.)

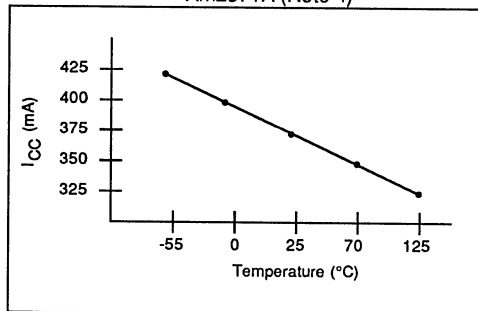
Parameter Symbol	Parameter Description	Test Conditions (Note 1)*		Min.	Max.	Unit
I_{sc} (Note 3)	Output Short-Circuit Current	$V_{cc} = \text{Max.}$ $V_{out} = 0 \text{ V}$	$T_o - T_{11}, \text{ CLKOUT}$	-15	-100	mA
I_{cc} (Note 4)	Power Supply Current (Am2971)	$V_{cc} = \text{Max.}$			310	mA
		$V_{cc} = 5.0 \text{ V}$	$T_A = 25^\circ\text{C}$		240	
	Power Supply Current (Am2971A)	$V_{cc} = \text{Max.}$			425	
		$V_{cc} = 5.0 \text{ V}$	$T_c = 25^\circ\text{C}$		370	

*Key: C = COM'L Devices
M/E = MIL or E-COM'L Devices

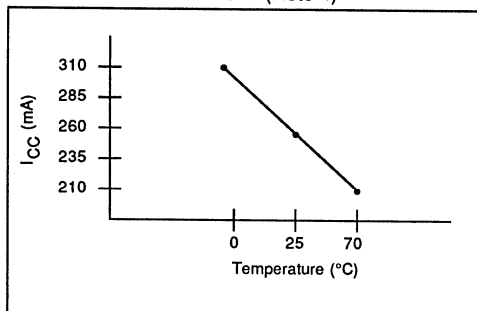
- Notes:
1. For conditions shown as Min. or Max., use appropriate value specified under Operating Range for the applicable device type.
 2. Does not apply to CLK/X₁ and X₂.
 3. No more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
 4. I_{cc} varies with temperature and oscillation frequency. Worst-case I_{cc} is at minimum temperature. Typical I_{cc} ($V_{cc} = 5.0 \text{ V}$, $T_A, T_c = +25^\circ\text{C}$) represents nominal units and is not tested. See the following graphs.

Typical Power Supply Current (Nominal Unit)

Am2971A (Note 4)



Am2971 (Note 4)



052800-15A

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Clock Control Logic: PLL Bypassed

No.	Parameter Symbol	Parameter Description	Test Conditions*	Am2971		Am2971A		Unit	
				Min.	Max.	Min.	Max.		
1	f_i	Direct TTL Clock Source, Input Frequency at CLK/X ₁ with PLL Multiplier set to "x1" (Fuse #618 = 0)	(Notes 1,4)	C	0	85	0	100	MHz
				M/E	-	-	0	100	
		Crystal Clock Source (Note 6). Input Frequency at CLK/X ₁ and X ₂ with PLL Multiplier set to "x1" (Fuse #618 = 1)		C	-	-	0	100	
				M/E	-	-	0	100	
2	t_{RCO}	Rise Time of Clock Out (CLKOUT) Signal	(Note 1)	C		14		10	ns
				M/E				10	
3	t_{FCO}	Fall Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10		10	ns
				M/E				10	
4	t_{RTO}	Rise Time of T _n Outputs	(Note 1)	C		10		8	ns
				M/E				8	
5	t_{FTO}	Fall Time of T _n Outputs	(Note 1)	C		9		8	ns
				M/E				8	
6	t_{SKEWLH}	Skew Time between T _n Outputs. All Outputs Switching ↑	C _L = 50 pF (Note 5)	C		3.5		2.5	ns
				M/E				2.5	
6a	t_{SKEWHL}	Skew Time between T _n Outputs. All Outputs Switching ↓	C _L = 50 pF (Note 5)	C		5		2.5	ns
				M/E				2.5	
7	t_{SKEW8}	Skew Time between Matched T _n Outputs. Eight Outputs Switching ↑ or ↓ (T _{0-3, 5, 6, 10, 11})	C _L = 50 pF (Note 5)	C		5		2	ns
				M/E				2	
8	t_{SKEW6}	Skew Time between Matched T _n Outputs. Six Outputs Switching ↑ or ↓ (T _{1-3, 5, 10, 11})	C _L = 50 pF (Note 5)	C		5		1.5	ns
				M/E				1.5	
9	t_{SKEW4}	Skew Time between Matched T _n Outputs. Four Outputs Switching ↑ or ↓ (T _{2, 3, 10, 11})	C _L = 50 pF (Note 5)	C		5		1	ns
				M/E				1.5	
10	t_{SKEW}	Skew Time between T _n Outputs. All Outputs Switching Mixed Transition	C _L = 50 pF (Note 5)	C		8.5		6.5	ns
				M/E				6.5	
11	$t_{SET TCA}$	TRIG Active to CLK/X ₁ ↑ Setup Time to Start an Output (T _n) Sequence		C	11		8		ns
				M/E			8		
12	$t_{SET TCI}$	TRIG Inactive to CLK/X ₁ ↑ Setup Time to Terminate an Output (T _n) Sequence		C	4		4		ns
				M/E			4		

SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Bypassed (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*	Am2971		Am2971A		Unit	
				Min.	Max.	Min.	Max.		
13	t_{PDCTO}	Propagation Delay from an Input Clock Edge (CLK/X _n) ↑ to an Active T _n Output		C		23	10	22	ns
				M/E			10	22	
14	t_{SETAT}	A ₀₋₂ Inputs to TRIG ↑ Setup Time	(Note 2)	C	1	1			ns
				M/E			2		
15	t_{HOLDAT}	A ₀₋₂ Inputs to TRIG ↑ Hold Time	(Note 2)	C	11	8			ns
				M/E			8		
16	t_{RCVRY} (Min.)	Chip Recovery/Reset Time between New (TRIG Active) Timing Sequences when Halting via STOP Bits	(Note 1)	C		2f _i		2f _i	ns
				M/E				2f _i	
		C			2f _i		2f _i		
		M/E					2f _i		
17	$t_{PD TTA}$	Propagation Delay from TRIG Active to Start of First T _n Output Signals	(Note 3)	C		34 + 1/f _i	18 + 1/f _i	30 + 1/f _i	ns
				M/E			18 + 1/f _i	30 + 1/f _i	
18	$t_{PD TTI}$	Propagation Delay from TRIG Inactive to Completion of Last T _n Output Signals	(Note 3)	C		27 + 1/f _i	14 + 1/f _i	26 + 1/f _i	ns
				M/E			14 + 1/f _i	26 + 1/f _i	
19	$t_{PWH T}$	TRIG Input Pulse Width in HIGH State	(Note 3)	C	16		13		ns
				M/E			13		
20	$t_{PWL T}$	TRIG Input Pulse Width in LOW State	(Note 3)	C	16		13		ns
				M/E			13		
21	$t_{PRD TO}$	T _n Output Period/Timing Resolution between T _n Outputs	(Note 3)	C	1/f _i		1/f _i		ns
				M/E	1/f _i		1/f _i		

*Key: C = COM'L Devices
M/E = MIL or E-COM'L Devices

SWITCHING CHARACTERISTICS (Cont'd.)

Clock Control Logic: PLL Selected

No.	Parameter Symbol	Parameter Description	Test Conditions*	Am2971		Am2971A		Unit	
				Min.	Max.	Min.	Max.		
1	f_i	Direct TTL Clock Source. Input Frequency at CLK/X ₁ with PLL Multiplier set to "x10" (Fuse #619 = "0")	(Notes 1,4)	C	1	7	1	10	MHz
				M/E			1	10	
		Direct TTL Clock Source. Input Frequency at CLK/X ₁ with PLL Multiplier set to "x5" (Fuse #619 = "1")		C	2	14	2	20	
				M/E			2	20	
		Crystal Clock Source (Note 6). Input Frequency at CLK/X ₁ and X ₂ with PLL Multiplier set to "x10" (Fuse #619 = "0")		C			1	10	
				M/E			1	10	
Crystal Clock Source (Note 6). Input Frequency at CLK/X ₁ and X ₂ with PLL Multiplier set to "x5" (Fuse #619 = "1")	C			2	20				
	M/E			2	20				
2	t_{RCO}	Rise Time of Clock Out (CLKOUT) Signal	(Note 1)	C		14	10	ns	
				M/E			10		
3	t_{FCO}	Fall Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10	10	ns	
				M/E			10		
4	t_{FTO}	Rise Time of T _n Outputs	(Note 1)	C		10	8	ns	
				M/E			8		
5	t_{FTO}	Fall Time of T _n Outputs	(Note 1)	C		9	8	ns	
				M/E			8		
6	t_{SKEWLH}	Skew Time between T _n Outputs. All Outputs Switching ↑	C _L = 50 pF (Note 5)	C		3.5	2.5	ns	
				M/E			2.5		
6a	t_{SKEWLH}	Skew Time between T _n Outputs. All Outputs Switching ↓	C _L = 50 pF (Note 5)	C		5.0	2.5	ns	
				M/E			2.5		
7	t_{SKEW8}	Skew Time between Matched T _n Outputs. Eight Outputs Switching ↑ or ↓ (T _{0-3,5,6,10,11})	C _L = 50 pF (Note 5)	C		5.0	2.0	ns	
				M/E			2.0		
8	t_{SKEW6}	Skew Time between Matched T _n Outputs. Six Outputs Switching ↑ or ↓ (T _{1-3,5,10,11})	C _L = 50 pF (Note 5)	C		5.0	1.5	ns	
				M/E			1.5		
9	t_{SKEW4}	Skew Time between Matched T _n Outputs. Four Outputs Switching ↑ or ↓ (T _{2,3,10,11})	C _L = 50 pF (Note 5)	C		5.0	1.0	ns	
				M/E			1.5		
10	t_{SKEW}	Skew Time between T _n Outputs. All Outputs Switching Mixed Transition	C _L = 50 pF (Note 5)	C		8.5	6.5	ns	
				M/E			6.5		

SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Selected (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*	Am2971		Am2971A		Unit	
				Min.	Max.	Min.	Max.		
11	$t_{SET TCA}$	TRIG Active to CLK/ X_1 (\uparrow) Setup Time to Start an Output (T_n) Sequence		C	11		8	ns	
				M/E			8		
12	$t_{SET TCI}$	TRIG Inactive to CLK/ X_1 (\uparrow) Setup Time to Terminate an Output (T_n) Sequence		C	6		4	ns	
				M/E			4		
13a	$t_{PD CTO}$	Propagation Delay from an Input Clock Edge (CLK/ X_1) (\uparrow) to an Active T_n Output when "1" has been Selected (Fuses #616 and 617 = "0")		C		25	10	20	ns
				M/E			10	26	
13b	$t_{PD CTO}$	Propagation Delay from an Input Clock Edge (CLK/ X_1) (\uparrow) to an Active T_n Output when "2" has been Selected (Fuse #616 = "1" and Fuse #617 = "0")	(Note 3)	C		$25 + 1/2f_c$	$10 + 1/2f_c$	$20 + 1/2f_c$	ns
				M/E			$10 + 1/2f_c$	$26 + 1/2f_c$	
13c	$t_{PD CTO}$	Propagation Delay from an Input Clock Edge (CLK/ X_1) (\uparrow) to an Active T_n Output when "4" has been Selected (Fuse #616 = "0" and Fuse #617 = "1")	(Note 3)	C		$25 + 3/4f_c$	$10 + 3/4f_c$	$20 + 3/4f_c$	ns
				M/E			$10 + 3/4f_c$	$26 + 3/4f_c$	
14	$t_{SET AT}$	A_{0-2} Inputs to TRIG (\uparrow) Setup Time	(Note 2)	C	1		1.0	ns	
				M/E			2.0		
15	$t_{HOLD AT}$	A_{0-2} Inputs to TRIG (\uparrow) Hold Time	(Note 2)	C	11		8	ns	
				M/E			8		
16	t_{RCVRY} (Min.)	Chip Recovery/Reset Time between New (TRIG Active) Timing Sequence when Halting via STOP Bits	(Note 1)	C		$2f_c$		$2f_c$	ns
				M/E				$2f_c$	
				C		$2f_c$		$2f_c$	
				M/E				$2f_c$	
17a	$t_{PD TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "1" has been Selected (Fuses #616 and 617 = "0")	(Note 3)	C		$36 + 1/f_c$	$18 + 1/f_c$	$28 + 1/f_c$	ns
				M/E			$18 + 1/f_c$	$34 + 1/f_c$	
17b	$t_{PD TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "2" has been Selected (Fuse #616 = "1" and Fuse #617 = "0")	(Note 3)	C		$36 + 1/f_c$	$18 + 1/2f_c$	$28 + 1/2f_c$	ns
				M/E			$18 + 1/2f_c$	$34 + 1/2f_c$	

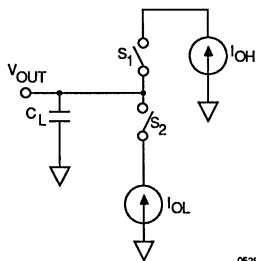
SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Selected (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971		Am2971A		Unit
					Min.	Max.	Min.	Max.	
17c	$t_{PD\ TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "4" has been Selected (Fuse #616 = "0" and Fuse #617 = "1")	(Note 3)	C		$36 + \frac{3}{4}f_c$	$18 + \frac{3}{4}f_c$	$28 + \frac{3}{4}f_c$	ns
				M/E			$18 + \frac{3}{4}f_c$	$34 + \frac{3}{4}f_c$	
18	$t_{PD\ TTI}$	Propagation Delay from TRIG Inactive to Completion of the Last T_n Output Signals	(Note 3)	C		$29 + \frac{1}{f_c}$	$14 + \frac{1}{f_c}$	$24 + \frac{1}{f_c}$	ns
				M/E			$14 + \frac{1}{f_c}$	$30 + \frac{1}{f_c}$	
19	$t_{PWH\ T}$	TRIG Input Pulse Width in HIGH State when "1" has been Selected (Fuses #616 and 617 = "0")	(Note 3)	C	16		13		ns
				M/E			13		
20	$t_{PWL\ T}$	TRIG Input Pulse Width in LOW State	(Note 3)	C	16		13		ns
				M/E			13		
21	$t_{PRD\ TO}$	T_n Output Period/Timing Resolution between T_n Outputs	(Note 3)	C	$\frac{1}{f_c}$		$\frac{1}{f_c}$		ns
				M/E			$\frac{1}{f_c}$		
22	$t_{PD\ CTC}^*$	Propagation Delay from an Input Clock Edge (CLK/X _i) (↑) to an Output Clock Edge (CLKOUT) (↑) (Fuses #616 and 617 = "0")	(Note 1)	C		19	10	19	ns
				M/E			10	21	

*Key: C = COM'L Devices
M/E = MIL or E-COM'L Devices

- Notes:
1. Not production tested due to automatic test equipment limitation; guaranteed by characterization.
 2. Only A_2 is tested.
 3. Not tested; calculated from other parameters.
 4. f_i input clock duty cycle should be $50\% \pm 10\%$.
 5. Not tested. Skew times shown in each case are guaranteed by characterization for specific outputs listed with any number of outputs switching.
 6. The maximum operating frequency of the Am2971 is 85 MHz if the PLL is bypassed, all outputs in use. If the PLL is selected, the maximum operating frequency is 70 MHz, all outputs in use. The Am2971A has a maximum operating frequency of 100 MHz with a TTL source, all outputs in use, but only nine outputs (any nine) may be programmed to switch simultaneously. If a crystal is used to clock the Am2971A, all outputs may be used, but only six outputs (any six) can be programmed to switch simultaneously.

SWITCHING TEST CIRCUIT

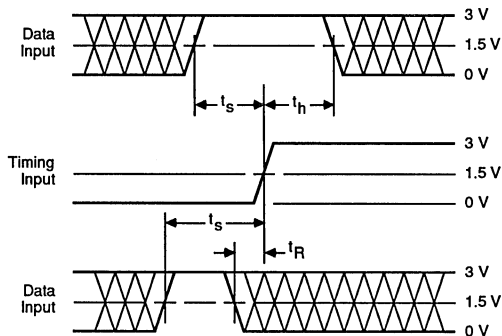


05280D-16A

A. Outputs

- Notes:
1. $C_L = 50$ pF. The load capacitance includes scope probe, wiring, and stray capacitance without the device in the test fixture.
 2. S_1 and S_2 are open during all DC and functional testing.
 3. During AC testing, switches are set as follows:
 - 1) For $V_{OUT} > 1.5$ V, S_1 is closed and S_2 open
 - 2) For $V_{OUT} < 1.5$ V, S_1 is open and S_2 closed

SWITCHING TEST WAVEFORMS

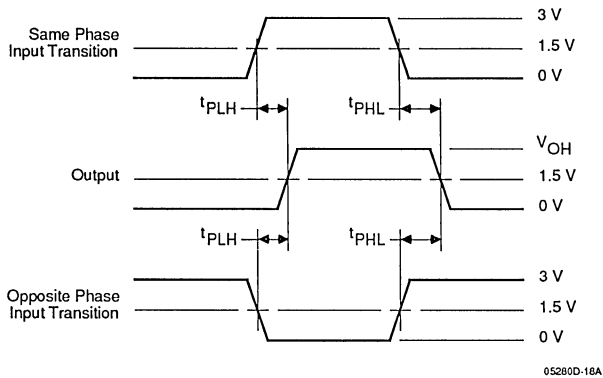


05280D-17A

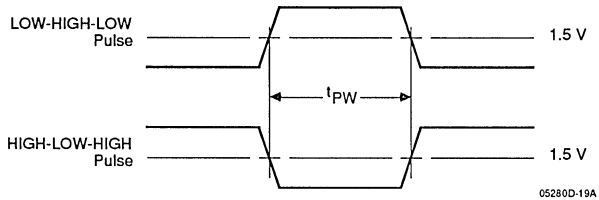
- Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
 2. Cross-hatched area is don't care condition.

A. Setup, Hold, and Release Times

SWITCHING TEST WAVEFORMS (Cont'd.)



B. Propagation Delay



C. Pulse Width

General Test Notes

Automatic tester hardware and handler hardware add additional round-trip AC delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

Function testing is done with input LOW less than V_{IL} and input HIGH greater than V_{IH} . A single trip point at the





approximate threshold voltage is used to determine output logic level.

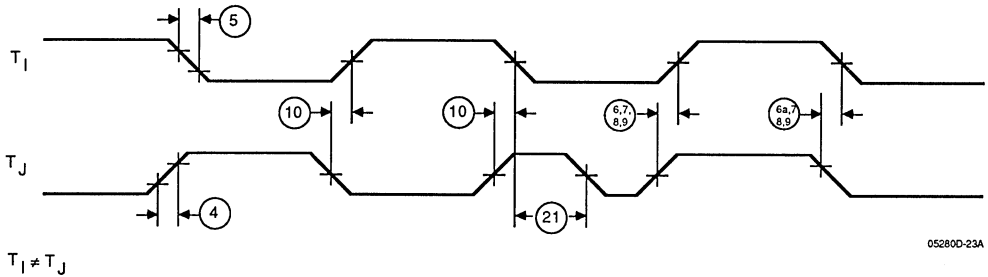
Some Setup and Hold tests are not performed due to tester accuracy limitation. They are guaranteed by correlation.

AC loads specified in this data sheet are used for bench testing. Programmable loads, which simulate data sheet loads, are used during automatic production testing.

SWITCHING WAVEFORMS

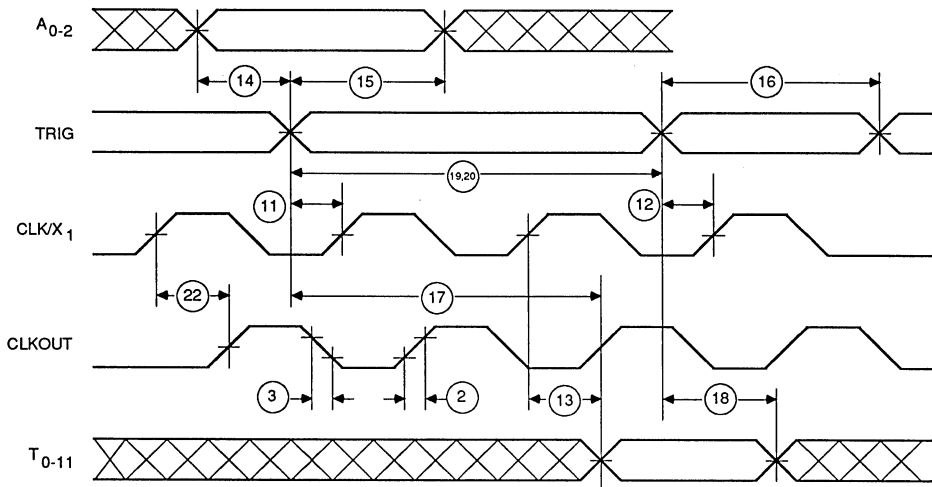
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN



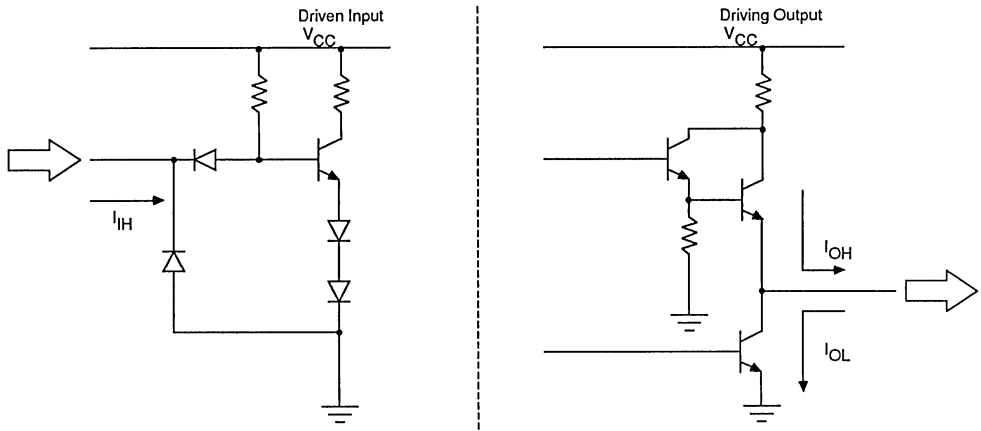
052800-23A

Rise Time/Fall Time/Skews

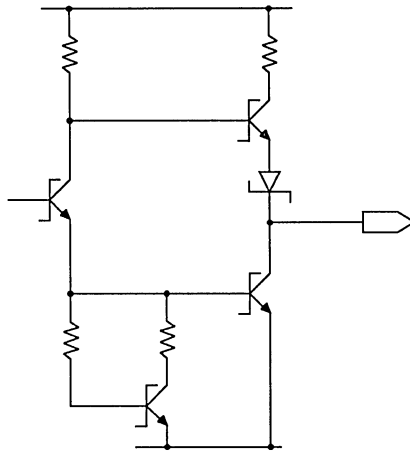


05280D-22A

INPUT/OUTPUT CIRCUIT DIAGRAMS



05280D-20A

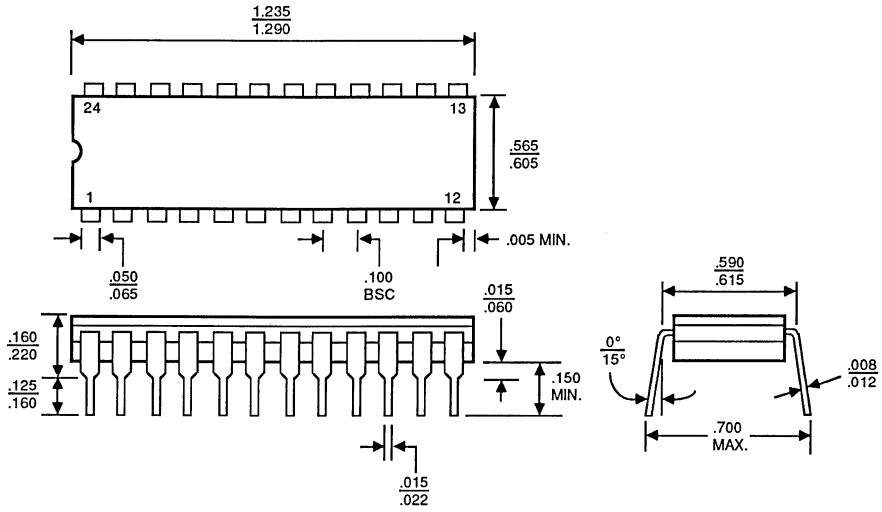


05280D-21A

Output Configuration for CLKOUT

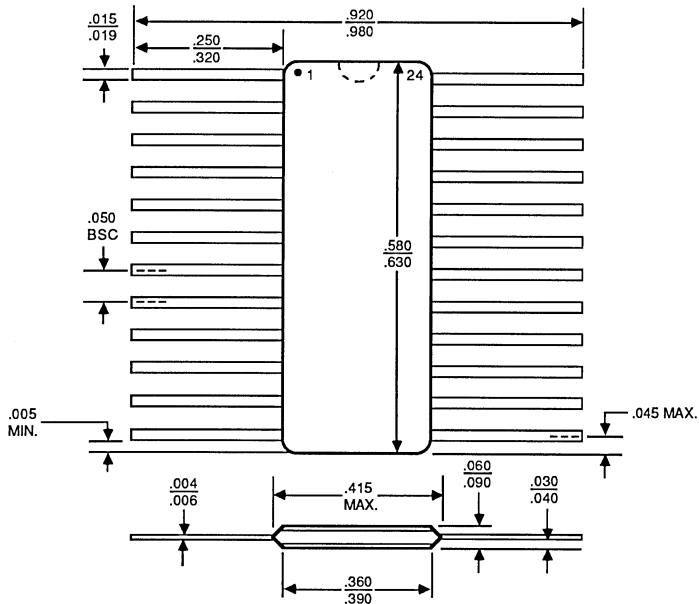
PHYSICAL DIMENSIONS*

CD 024



PID# 07156B

CFM024

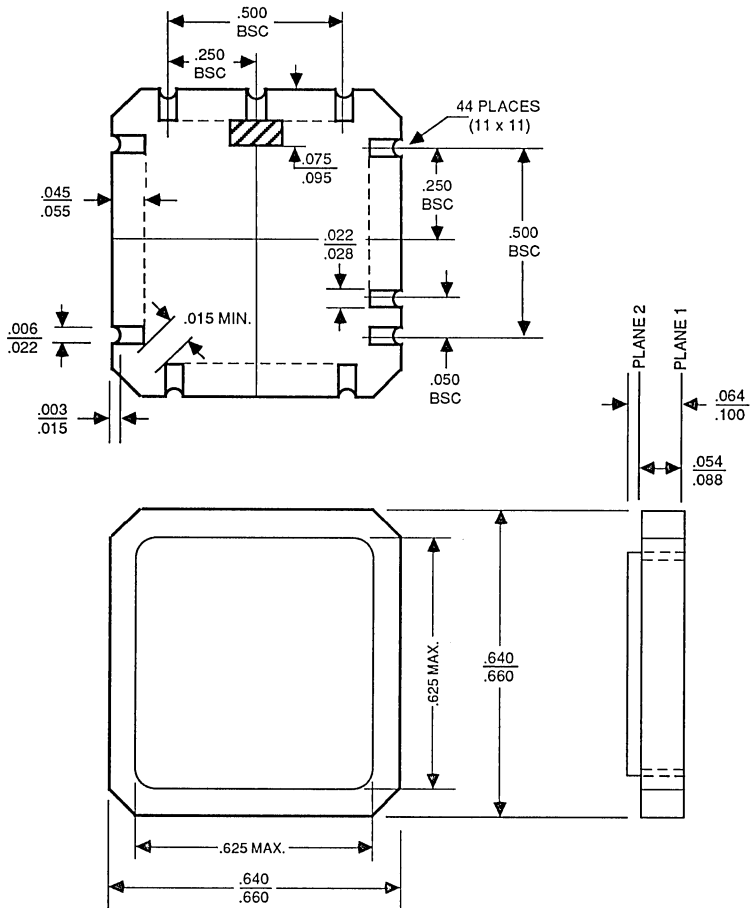


PID# 07371C

* For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

CL 044



PID #06825E

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