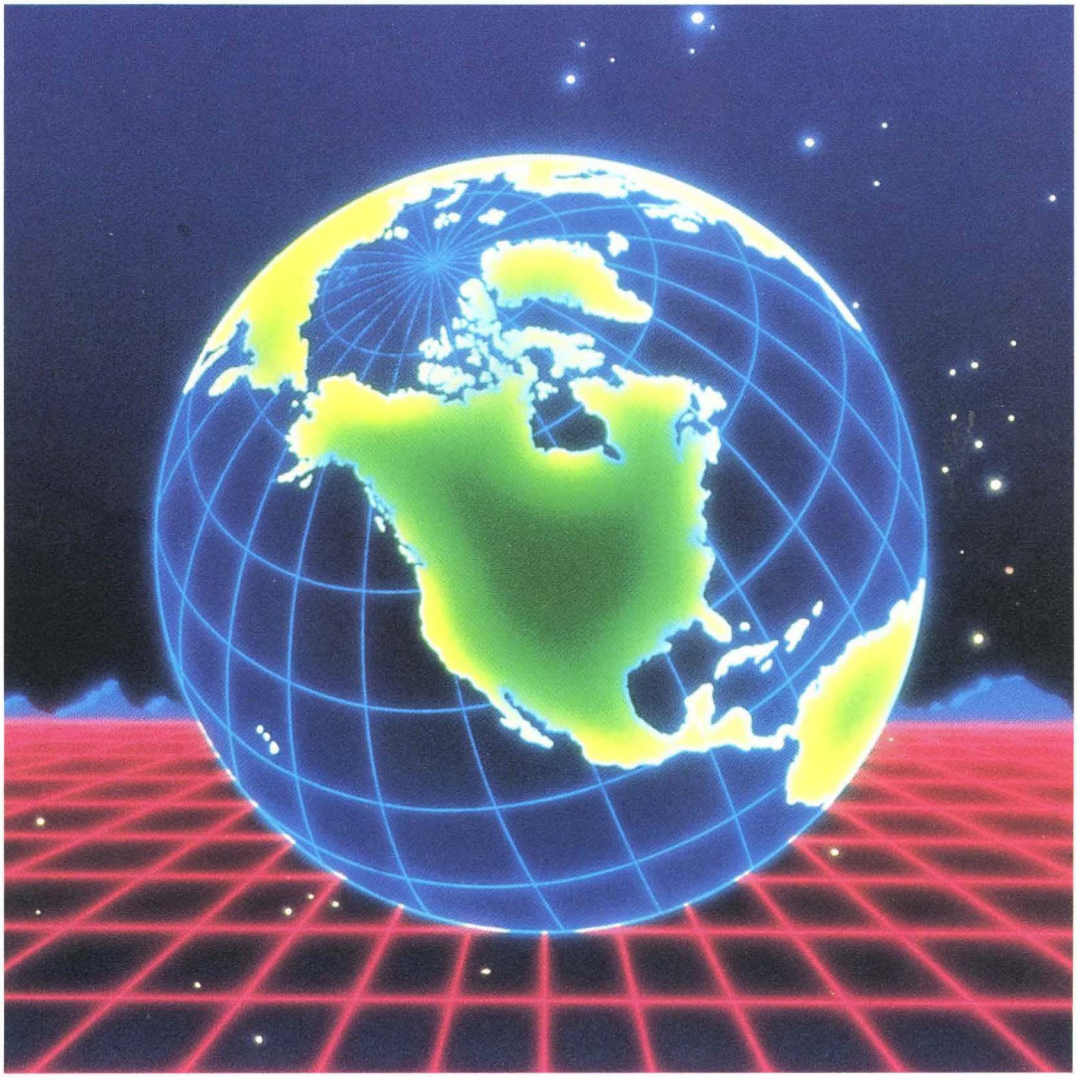
Telecommunication Products

Data Book 1992/1993

Advanced
Micro
Devices



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Telecommunication Products Data Book

1992/1993

ADVANCED MICRO DEVICES 

TELECOMMUNICATION PRODUCTS
DATA BOOK 1992/1993
TABLE OF CONTENTS

INTRODUCTION TO TELECOMMUNICATION PRODUCTS

Advanced Micro Devices supplies system solutions for your telecommunications applications. AMD provides customers with the most advanced integrated circuits, together with the software and development tools necessary for keeping pace with the ongoing revolution in telecommunications. AMD telecommunication products support applications ranging from switches for the analog telephone network to terminals for the Integrated Services Digital Network (ISDN).

Analog Subscriber Solutions

AMD has established a leadership position in the telephone switching equipment marketplace with the Subscriber Line Interface Circuit (SLIC) and Subscriber Line Audio-Processing Circuit (SLAC™ and DSLAC™) products. These components are used in telephone Central Office Exchanges and PBXs around the world and are used in some of the most sophisticated Central Office Exchanges available today.

AMD's many evaluation boards, software packages, kits, and extensive documentation allow quick evaluation of the SLIC/SLAC and DSLAC circuit's performance and features, and fast time-to-market for linecard applications.

ISDN Solutions

ISDN is the standard for the conversion of the world telephone network to an integrated, public digital network for both voice and data. ISDN technology is being implemented and tested in many parts of the world, and its use will accelerate as the speed and cost advantages of digital communications become readily apparent. The ISDN network will provide a multitude of new services through simultaneous transmission and reception of voice, data, and video over a common network.

AMD's Am79C30A Digital Subscriber Controller™ ISDN circuit provides maximum functional integration consistent with international standards. It is the world's first ISDN terminal circuit that can be used to build ISDN telephones and terminals that conform to CCITT power specifications. This circuit, combined with EPROM, SRAM, a microcontroller, and a power controller, are all that is needed for a basic CCITT power-compliant telephone or terminal. AMD's ISDN development boards and support software guide the user through each step of the ISDN product development process, significantly reducing time-to-market.

AMD's Complete Offering

The telecommunication function is just one of the areas where AMD can aid design efforts. AMD is also a leading supplier of programmable logic devices, high-performance memories, the CISC and RISC processors, and related peripherals.

AMD has developed more solutions than anyone else for getting applications to market faster with programmable logic. AMD offers the broadest, best-supplied line of programmable logic devices in the industry.

AMD's total system solution for managing high-performance dynamic memories offers flexibility, integration, and performance with the industries fastest 32- and 16-bit error detection and correction circuits and the most flexible DRAM controllers and drivers. AMD is a pioneer in the field of specialty memory devices with an extensive line of bipolar and CMOS FIFOs. AMD also supplies a broad range of EPROM and SRAM products.

AMD's Embedded Processor Division supplies 8- and 16-bit microcontrollers as well as bit block and field programmable controllers. This group also manufacturers the high-performance Am29000™ Family of 32-bit RISC processors. AMD also offers a line of iAPX microprocessors and related peripherals from the 8088 to the high-performance Am386™ microprocessor.

Chapter 1

SLIC Products

CHAPTER 1
SLIC Products

INTRODUCTION TO SLIC PRODUCTS

AMD's Subscriber Line Interface Circuit (SLIC) products perform the telephone line interface functions required by most types of telephone switching and transmission equipment. In addition to supporting the BORSCHT functions (Battery Feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid and Test), the AMD SLIC Family offers such features as current limiting, on-hook transmission, polarity reversal, tip-open mode for ground start signaling, ground- key detection, and ground-key filtering.

SLICs optimize linecard costs by minimizing the number of components needed per line, by minimizing the board space requirements, and by supporting automated manufacturing techniques not supported by alternative technologies.

SLIC Types

AMD's SLIC products are designed to address a number of different applications including:

- Central Office Switches,
- Private Branch Exchanges (PBXs) and Key Systems,
- Digital Loop Carriers (DLCs), Multiplexers, Channel Banks, and Fiber-In-The-Loop (FITL) equipment.

SLICs intended primarily for Central Office applications are offered and comply with the most stringent standards set by the CCITT, Bellcore, and/or British Telecom. Central Office SLICs also incorporate a self-adjusting switching regulator to reduce power consumption to a minimum and enhance system reliability. Constant current feed SLICs, constant voltage feed SLICs, and versions of each SLIC that supports metering are offered in a variety of configurations and package types.

AMD also offers SLICs optimized for other switching applications such as PBXs. These SLICs are specified and tested to meet the requirements of both the EIA/TIA-464-A and ETSI TE10–02 PBX standards. They have a wider battery operating range than the Central Office SLICs and will operate with either 24- or 48-V batteries. Also, the switching regulator function is either not offered or is optional, saving the cost of a few external components in applications where power control into short loops is unnecessary.

Both Central Office and PBX SLICs support on-hook transmission and offer extended temperature performance, making either type ideal for Digital Loop Carrier and Multiplexer applications. SLICs from both Central Office and PBX families are offered that comply with Bellcore's TR-TSY-000057 Specification for DLCs, and TR-909 for FITL.

Performance grades are offered for all AMD SLICs that support the various idle channel noise and longitudinal balance specifications worldwide.

SLIC Functions

The signal transmission functions of all AMD SLICs include both two-to-four wire and four-to-two wire conversion. The two-wire termination impedance is programmed with a single external impedance. The companion AMD SLAC or DSLAC IC (Single- or Dual-Channel Subscriber Line Audio-Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the DSLAC device is not used, most codec/filters provide an uncommitted op amp for this purpose.

The SLIC's battery feed architecture makes the DC feed characteristics programmable by external resistors. Furthermore, these characteristics are independent of battery variations. AMD's PBX SLICs can operate from below 24 V to above 48 V, while the Central Office SLICs are optimized for 48-V operation.

A polarity reversal function is provided on most SLICs which transposes the voltage applied to the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode is also provided, limiting loop current and cutting power dissipation while allowing the full complement of supervisory functions to be utilized.

The supervisory functions of off-hook detection and ring-trip detection are read through a single, TTL-compatible output. To eliminate noise-induced errors, the off-hook signal may be filtered before being detected. Off-hook detection has a threshold that is set by the value of an external resistor. Additional supervisory controls put the A lead into an open circuit (high impedance) state suitable for application in ground-start systems. Similarly, both the A and B leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Two relay drivers support ring and test relay functions, or can be used for other functions such as a message-waiting lamp.

The SLIC's user-programmable states are controlled by a TTL-compatible code. The control inputs are designed to easily interface to popular single-chip microcontrollers, such as the industry standard 8051, or to latched outputs from a SLAC or DSLAC device.

PRODUCT SELECTOR GUIDE

The following selector chart shows the most commonly used AMD SLIC types offered at the time of publication. SLIC part numbers are shown at the top of the chart and are referenced to the principal SLIC characteristics and features on the left. Use this selection chart to identify a SLIC that meets the general needs of a specific application, then turn to the appropriate data sheet for detailed information. If there is no SLIC that meets these specific requirements, contact the local AMD sales office or the AMD Communication Products Division for information on new SLIC product offerings or other assistance.

Bond-Out Options

Some of the Central Office SLICs are offered in a number of different bond-out options. These SLICs are the Am7953n, Am7957n, Am79M53n, and Am79M57n, where the n is a number indicating the bond-out option used. Generally, the bond-out options are as follows.

n = 0 indicates that both E0 and E1 functions are present, with one relay driver and no ground-key filter.

n = 1 indicates that both E0 and E1 functions are present, with a ground-key filter and one relay driver.

n = 2 indicates that the E1 function only is present, with two relay drivers.

n = 3 indicates that the E0 function only is present, with two relay drivers.

n = 4 indicates that both E0 and E1 functions are present, with two relay drivers (32-pin PLCC package).

n = 5 indicates that both E0 and E1 functions are present, with a ground-key filter pin and one relay driver (32-pin PLCC package).

All these SLIC versions are potentially available, but not all are presently in production. Versions that are in volume production are indicated in the chart. If a specific bond-out configuration is not indicated to be in production, please contact AMD's Communication Products Division or the local AMD Sales Office.

Performance Grades

Each of the devices shown on the selector chart is offered in standard, –1, and –2 performance grades. Enhanced performance is specified in the following areas:

- Analog output DC offset
- Longitudinal balance
- Gain flatness and tracking
- Idle channel noise
- Power supply rejection ratio
- Power dissipation

The –2 performance grade has the same performance as the –1 grade except where noted. See the individual product's data sheet for more information. The –2 performance grade SLICs have also been characterized for extended temperature performance. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Selector Chart

Possible SLIC Products

	Am7953n				Am7957n			Am7958	Am79M53n		Am79M57n		Am79HM53	Am7942	Am7943
	n=				n=				n=		n=				
	0	1	4	5	1	3	4		1	5	0	4			
Functions															
Constant Current Feed	•	•	•	•					•	•			•	•	•
Constant Resistance Feed					•	•	•	•			•	•			
2.2-V Metering									•	•	•	•			
5-V Metering													•		
Switching Regulator	•	•	•	•	•	•	•	•	•	•	•	•	•	Option	
$\overline{\text{DET}}$ Enable Bit, E0	•	•	•	•	•	•	•	•	•	•	•	•	•		JC only
GND Key Select Bit, E1	•	•	•	•	•		•	•	•	•	•	•	•	•	JC only
GND Key Filter Pin		•		•	•				•	•				•	
Ring Relay Driver	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Test Relay Driver			•			•	•	JC only				•	JC only	JC only	
Packaging															
28-pin DIP	•	•			•	•		•	•		•		•	•	
22-pin DIP															•
32-pin PLCC			•	•			•	•		•		•	•	•	•

SLIC FAMILY FUNCTIONAL DESCRIPTION

The internal operation of the AMD Family of Subscriber Line Interface Circuits is summarized in the Block Diagram in each of the SLIC Family data sheets. The following sections describe in detail the operation of each block in these diagrams.

Two-Wire Interface

The function of the two-wire interface is to provide DC current and to send voice signals to a telephone apparatus connected to the central office with a two-wire line. The two-wire interface also receives the returning voice signals from the telephone transmitter.

The two-wire interface (see Figure 1) consists of two current mode line-driver amplifiers, line-voltage sensing circuits with AC/DC pass separation, and a loop-current sensing circuit.

The current mode amplifiers driving the AX(TIPX) and BX(RINGX) pins are controlled by two input signals, I_{LI} and I_{MI}. I_{LI} controls the longitudinal (common mode) current, and I_{MI} controls the metallic (transverse) current.

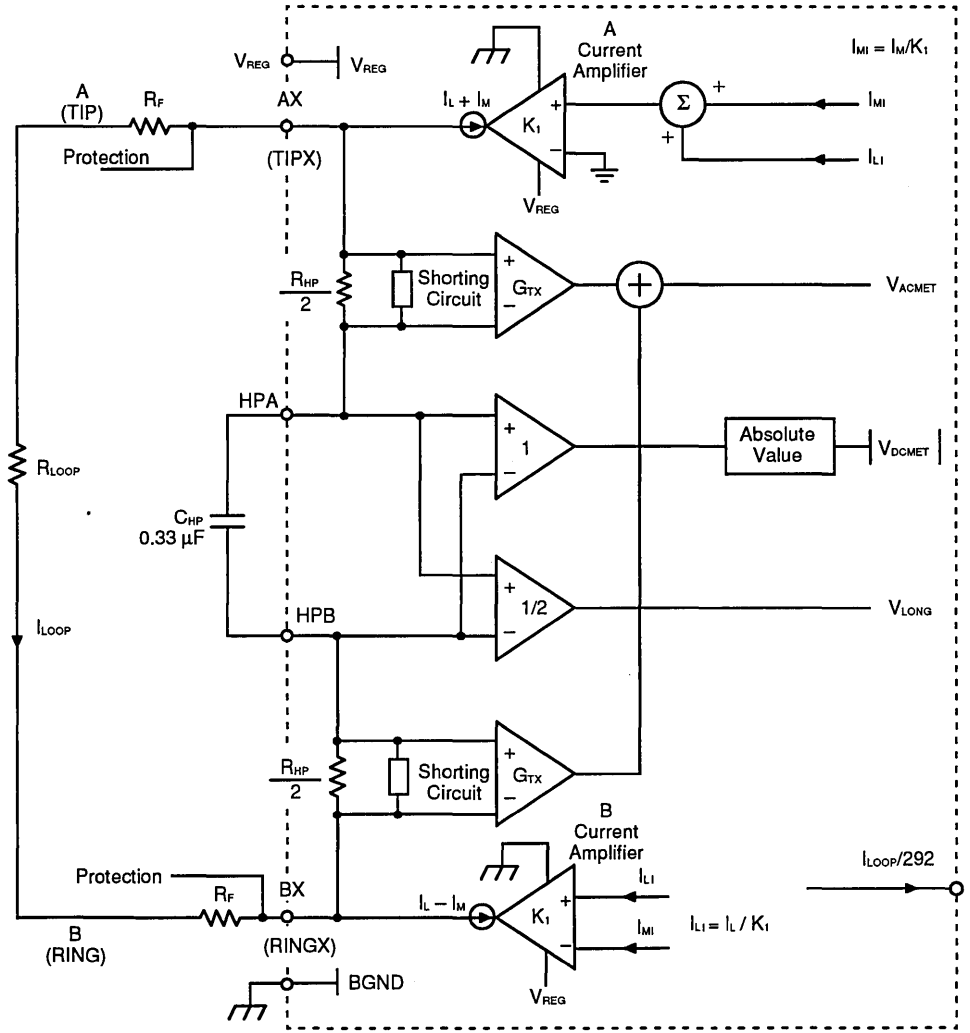

Figure 1. Two-Wire Interface

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The two-wire currents are:

$I_{AX} = K_I(I_{LI} + I_{MI})$ and $I_{BX} = K_I(I_{LI} - I_{MI})$

Where: K_I is the internal current mode amplifier gain.

I_{MI} is equal to the current into the Receive Summing Node (RSN), which is the terminating point for the external networks controlling two-wire impedance, receive gain, battery feed, and metering gain (in metering versions). These networks are described in detail later. I_{LI} controls the longitudinal line voltage to obtain the optimum common mode DC operating point for the current mode amplifiers.

The voltage sense signal (V_{ACMET}) that goes to the signal transmission block is the AC metallic component of the AX and BX voltages.

Two voltage sense signals ($|V_{DCMET}|$ and V_{LONG}) go to the power feed controller block. V_{DCMET} is the DC metallic component of the AX and BX voltages. V_{LONG} is the longitudinal component of the AX and BX voltages.

An external capacitor (C_{HP}), connected between HPA and HPB, separates the AC and DC components of the metallic voltage. Since the time constant would be too long during polarity reversal or pulse dialing, the two-wire interface has a shorting circuit that decreases the time constant during these events.

The loop-current sensing circuit produces a current (I_D) that is proportional to the magnitude of the loop current and is output to the R_D pin. An external resistor and filter capacitor connected from R_D to V_{EE} converts this current to a filtered voltage for use by the off-hook detector.

Signal Transmission

Figures 2a and 2b provide more detail of the SLIC transmission path. This path is split between the signal transmission block and the two-wire interface block.

The AC line voltage is sensed by differential amplifiers between the AX and HPA leads, and between the HPB and BX leads. The outputs of these amplifiers are equal to the AC metallic components of the line voltages. These voltages are summed and buffered by the op amp G_{TX}. For non-metering versions, G_{TX} is set to a gain of 1.0. For metering SLICs, G_{TX} is set to a gain of either 0.51 (2.2 VRMS metering versions) or 0.282 (5.1 VRMS versions) to avoid overload during metering signal transmission. Longitudinal voltages are rejected by the differential amplifiers and do not affect V_{TX}.

The balance return signal on V_{TX} exhibits 180° phase shift with respect to V_{RX}. This allows the SLIC's two-wire AC input impedance to be programmed by means of an external impedance that is connected between RSN and V_{TX} (see Figures 2a and 2b). This impedance may be a complex R-C network and should be K_I times the desired two-wire input impedance minus K_I times the fuse resistors. This means resistors become K_I times larger and capacitors become K_I times smaller. Note that any external stray capacitance between V_{TX} and RSN must be included in Z_T when precise computations for output impedance, gain, trans-hybrid loss, or return loss are being made.

$$Z_T = K_I G_{TX} (Z_{2WIN} - 2R_F)$$

Where: Z_{2WIN} = desired two-wire impedance

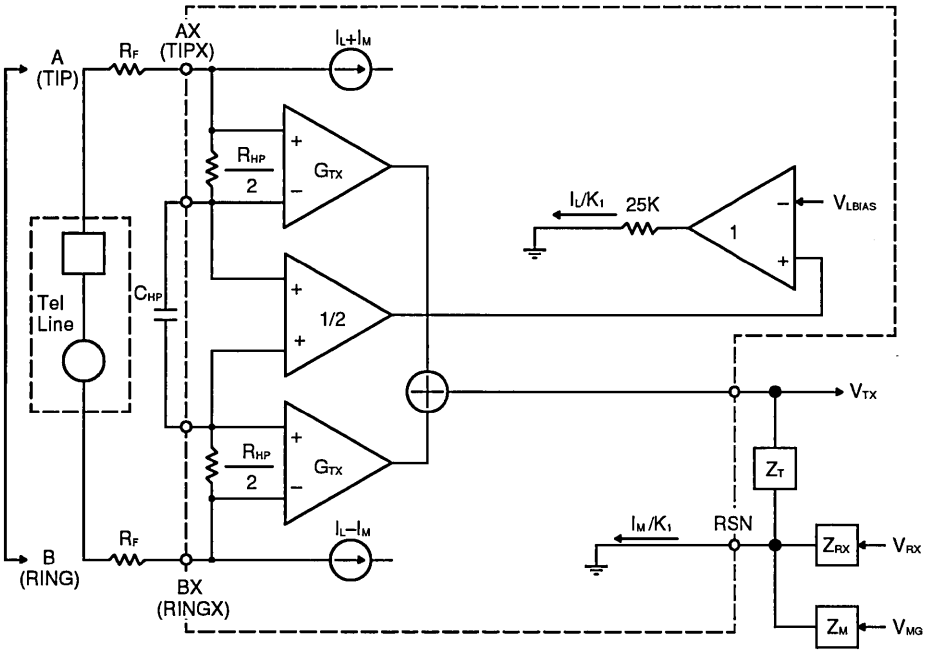
The four-wire output is found on the V_{TX} terminal, and the four-wire input terminal is V_{RX} (see Figure 2b). Both these ports are referenced to analog ground (AGND).

Because the fuse resistors are outside the feedback loops, they influence the effective gains. These gains are as follows:

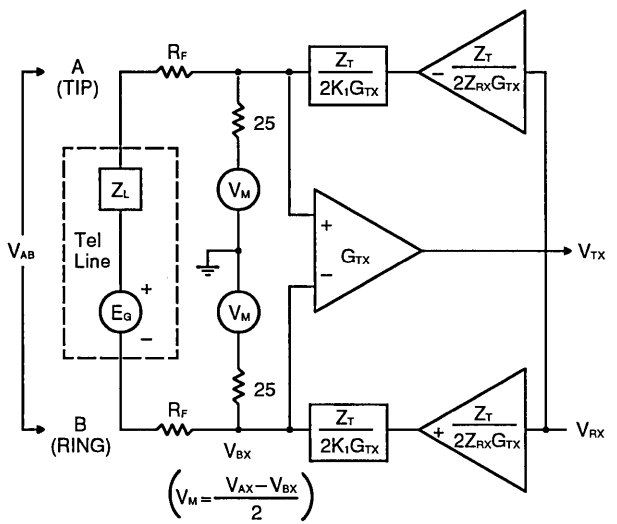
$$G_{42L} = \frac{V_{AB}}{V_{RX}} [E_G = 0] = -\frac{Z_L}{Z_{RX}} \frac{K_I Z_T}{Z_T + K_I G_{TX} (Z_L + 2R_F)}$$

$$G_{24} = \frac{V_{TX}}{V_{AB}} [V_{RX} = 0] = \frac{\frac{Z_T}{K_I}}{2R_F + \frac{Z_T}{K_I G_{TX}}}$$

$$G_{44L} = \frac{V_{TX}}{V_{RX}} [E_G = 0] = -\frac{Z_T}{Z_{RX}} \frac{(Z_L + 2R_F)}{Z_L + 2R_F + \frac{Z_T}{K_I G_{TX}}}$$



2a. Detailed Model



2b. Simplified Model (AC Only for Conceptual Purposes)

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Figure 2. SLIC Transmission Model

The dynamic performances of K_I (the current amplifier gain) and G_{TX} (the transmit voltage amplifier gain) are modeled by the following S-domain transfer functions:

$$K_I(S) = |K_I| \cdot \frac{1}{1 + 1.15 \cdot 10^{-6} \cdot [36 + Z_{AB}(S)] \cdot S}$$

$$G_{TX}(S) = \frac{|G_{TX}|}{1 + \frac{1}{424 \cdot 10^3 C_{HP} S}} \cdot \frac{1}{1 + 4.5 \cdot 10^{-7} S}$$

Where: $|K_I|$ = Current amplifier DC gain
Z_{AB} = Load between the AX and BX pins
$|G_{TX}|$ = Two- to four-wire transmit path midband gain

These functions are useful for the prediction of system return loss and echo cancellation performance. The value of K_I is typically 1000 for the Am795XX/ Am79M5XX versions. K_I is 200 for the Am7942, Am7943, and Am7958. G_{TX} is 1.0 for non-metering SLICs, 0.51 for metering versions, (Am79M53X/M57X) and .282 for the Am79HM53. C_{HP} sets the low frequency limit of the voice band response. A C_{HP} value of 0.33 µF should optimize voice-band and DC-loop performance in many applications.

The transmission circuit also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage (VL_{BIAS}) which comes from the power feed controller. Longitudinally, the SLIC typically appears as 25-ohm resistors from AX and BX to VL_{BIAS}. The longitudinal feedback does not affect metallic signals.

In metering versions of the SLIC, metering signals are injected by adding an additional current into summing point RSN through an external impedance, Z_M.

Power Feed Controller

The power feed controller has three sections: (1) the battery feed circuit; (2) the polarity reversal circuit; and (3) the bias circuit. These are shown in Figures 3a and 3b. The detailed model is shown in Figure 3a and the simplified model in Figure 3b.

The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. The polarity reversal circuit gives the SLIC the capability to reverse the loop current for pay telephone coin return and other applications. The bias circuit provides a reference voltage, which is offset from the subscriber line voltage. The reference voltage controls the switched mode regulator (described later), which minimizes SLIC power consumption by providing the minimum supply voltage needed by the line drivers for proper operation.

V_{DCMET} is the DC component of the voltage between AX and BX. When C_{HP} is 0.33 µF, the low pass filter formed by R_{HP} and C_{HP} attenuates frequencies above 1.2 Hz. The loop current is equal to K_I times the current into the Receive Summing Node (RSN), which is equal to the voltage on R_{DC} divided by $R_{DC1} + R_{DC2}$. The values of the programming resistors, R_{DC1} and R_{DC2}, should be kept somewhat equal in order to minimize the size of C_{DC}.

In constant current feed versions, the battery feed circuit produces a voltage at the R_{DC} pin whose magnitude is equal to 2.5 V, and whose sign depends on the feed polarity desired (minus for normal polarity and plus for reverse polarity). The net result is that the SLIC appears to have a constant current feed with the feed current given by the following equation:

$$I_{FEED} = \frac{2.5K_I}{R_{DC2} + R_{DC2}}$$

For example, if K_I is 1000 and a loop current of 40 mA is desired:

$$R_{DC1} + R_{DC2} = \frac{2.5 \cdot 1000}{40} = 62.5K$$

In this example, values of R_{DC1} and R_{DC2} of 31.25K could be used.

For resistance feed versions, the battery feed produces a voltage at the R_{DC} pin whose magnitude is equal to $(50 - |V_{DCMET}|)/20$, and whose sign depends on the feed polarity desired (minus for normal polarity and plus for reverse polarity). The net result is that the SLIC appears to have an apparent open circuit voltage of 50 V and a feed resistance, R_{FEED}, equal to $20(R_{DC1} + R_{DC2})/K_I$; thus, the feed resistance is programmable, but the apparent open circuit voltage is not. Including the fuse resistors R_F, the total feed resistance is then:

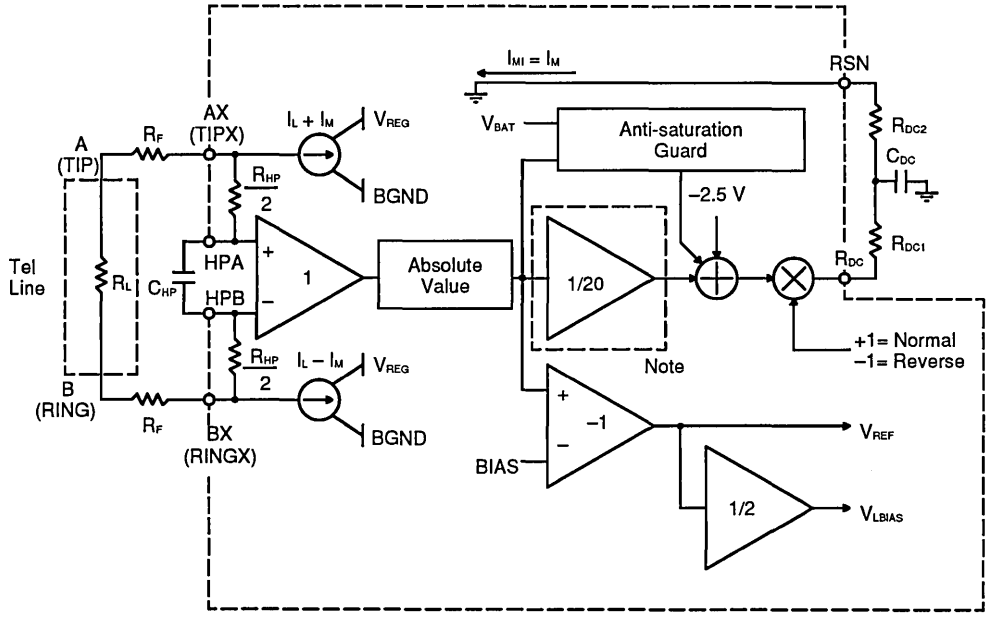
$$R_{FEED} = 2R_F + \frac{20(R_{DC1} + R_{DC2})}{K_I}$$

For example, if K_I = 1000, and a feed resistance of 840 ohms is desired using 20-ohm fuse resistors:

$$R_{DC1} + R_{DC2} = \frac{1000(840 - 2 \cdot 20)}{20} = 40K$$

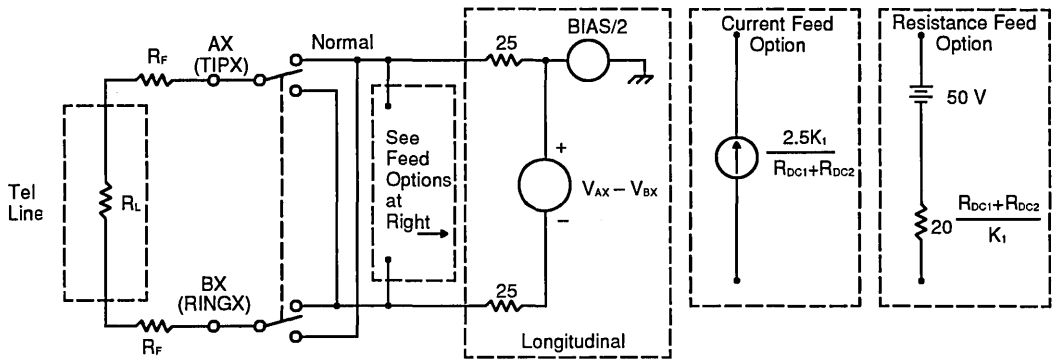
In this example, values of R_{DC1} and R_{DC2} of 20K could be used.

All versions of the SLIC have an anti-saturation guard that prevents the output amplifiers from saturating under high line voltage conditions which, in turn, prevents clipping. When the V_{AX} to V_{BX} voltage reaches a threshold of approximately 30 V (exact voltage depends on SLIC version), the SLIC goes into the Anti-sat 1 region of operation.



Note: The 1/20 operational amplifier is only present in constant resistance feed versions of the SLIC.

3a. Detailed Model



3b. Simplified Model

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Figure 3. SLIC Power Feed Controller

In this region, the feed synthesis loop gain is greatly increased, thereby reducing the output resistance to a much lower value. The output voltage then rises at a slower rate with increasing loop resistance, thereby keeping the amplifier out of saturation. All transmission specifications are met in the Anti-sat 1 region. If the line voltage increases further to greater than approximately 15 V (exact voltage depends on SLIC version) below V_{BAT}, the SLIC goes into the Anti-sat 2 region where the loop gain is again increased and the output resistance further decreased. In this region, the voltage rises very slowly, with increasing loop resistance, and the DC feed of the SLIC looks almost like a constant voltage source. The transmission specifications in the Anti-sat 2 region will be somewhat degraded. Load lines and equations describing all regions of operation are provided in each device data sheet.

To obtain polarity reversal, the input decoder and control circuit send a signal that reverses the sign of the voltage on the R_{DC} pin. During reversal, sense resistors R_{HP} are drastically reduced in value to reduce the time constant formed by R_{HP} and C_{HP}. This allows the polarity reversal time to be controlled only by C_{DC} and the parallel combination of R_{DC1} and R_{DC2}. A typical polarity transition time is 1.5 ms. In the previous example for a resistance feed version SLIC, R_{DC1} and R_{DC2} were computed to be 20K. The value of C_{DC} should then be 0.15 µF.

The V_{REF} output of this block is fed to the switching regulator (see next section) which adjusts V_{REG}, the voltage supplying the line output amplifiers, until it is equal to twice V_{LBIAS}. Additional BIAS is added to provide enough "headroom" for the amplifiers to always operate in the linear region. In summary, the equations for these voltages are:

$$V_{REG} = V_{REF} = -(|V_{DCMET}| + BIAS)$$

$$V_{LBIAS} = V_{REF}/2$$

Switching Regulator

The switching regulator supplies the operating voltage, V_{REG}, to the two-wire interface (see Figure 4). This circuit adjusts V_{REG} to the minimum voltage necessary to power the output amplifiers. In this manner, the power consumption is held to a minimum. This is particularly important for short loops where there is a potential for high loop currents.

A 256- to 282-kHz clock is required at input CHCLK to operate the switching regulator. The switch control tells the switch to disconnect the L pin from V_{BAT} at the beginning of each CHCLK cycle, and connect it for a time that depends upon the difference between V_{REF} and V_{REG}. During this time, the current through the inductor decreases. A comparator senses when V_{REG} falls below V_{REF} and the inductor is again switched to V_{BAT}. The result is that the average value of V_{REG} is always held equal to the value of V_{REF}. The filter capacitor, C_{FIL}, between V_{REG} and BGND smooths out the ripple caused by the inductor switching action.

The regulator is a high-gain feedback circuit, and therefore requires the stabilization network formed by R_{CH}, C_{CH1}, and C_{CH2} between V_{REG} and CHS.

The design and layout of the external switching regulator circuitry are very important. Fast switching currents can occur in the catch diode, D_1, and in the V_{BAT} filter capacitor, C_{BAT}. These must be low inductance components with short leads. Capacitor C_{FIL} must have low effective series resistance at high frequencies. A stable, voltage insensitive capacitor, such as a metallized polyester type, should be used.

The connections from the diode to the L pin, from C_{BAT} to the V_{BAT} pin, and from the diode to C_{BAT} must all be short, low-inductance connections. The L pin is subject to very fast voltage transients as the switch turns on and off, so all of the connections to this pin must be isolated from sensitive signals by means of traces connected to BGND. All of the external components in the regulator circuit except C_{CH1} must have voltage ratings in excess of 70 V. C_{CH1} can have a voltage rating of 10 V or more. In addition, the diode must have a reverse recovery time of less than 4 ns. All of the SLICs in a system should be synchronized to a common clock to prevent intermodulation products and crosstalk in the voice band.

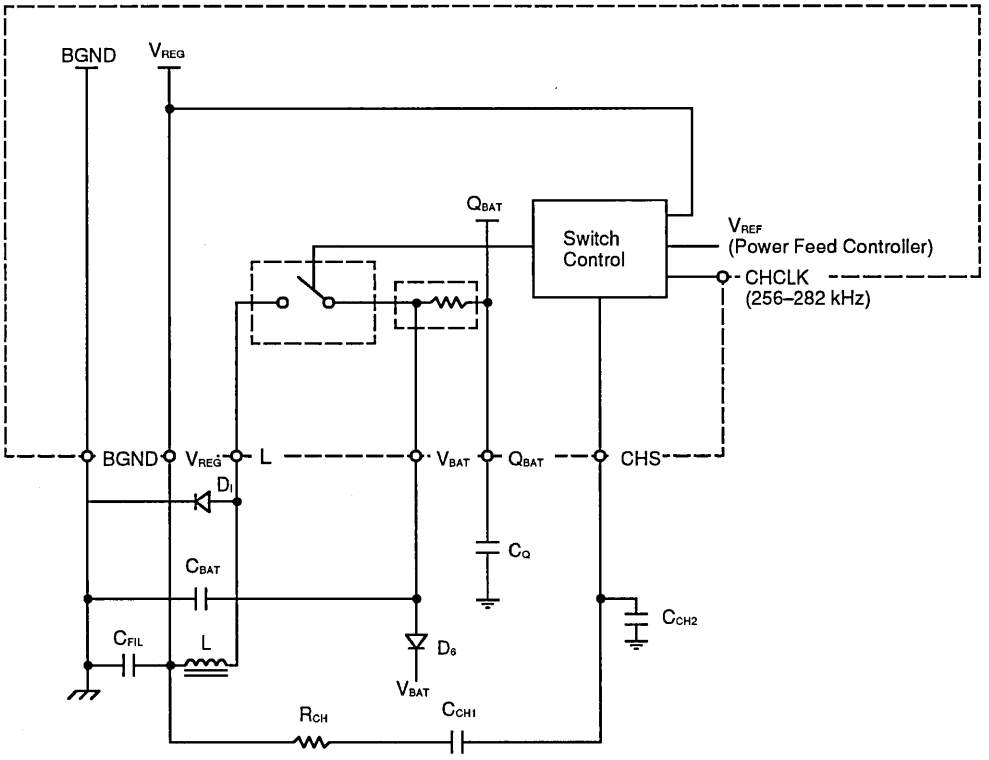

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Figure 4. SLIC Switching Regulator

Input Decoder and Control

The input decoder and control block provide a means for a microprocessor or SLAC IC to control such system functions as line activate/disable, ringing, and polarity reversal.

The input decoder and control block has TTL-compatible inputs, and sets the operating states of the SLIC. C_1, C_2, and C_3 inputs are common to all versions and can select seven operating states. C_4 is a dedicated input used as a test relay command in versions with a test relay driver. E_0 and E_1 control the function of the $\overline{DET}$ output. Table 1 summarizes the SLIC control logic.

Off-Hook Detector

The first and most important loop monitoring function is off-hook detection. The block diagram of this detector is shown in Figure 5.

The two-wire interface produces a current equal in magnitude to the loop current divided by 292, and sends it out on the R_D pin. An external resistor and capacitor (R_d and C_d) connects the R_D pin to V_{EE} (–5 V). The value of the voltage across resistor R_d is the current leaving the R_D pin times the value of R_d. The off-hook detector outputs a logic Low to the $\overline{DET}$ pin when this voltage rises above a threshold of 1.25 V.

The value of R_d required for a desired off-hook line current threshold is then:

$$R_d = \frac{365}{I_{THRESH}}$$

The value of C_d for a typical on-hook to off-hook time constant of 0.5 ms should satisfy the relation:

$$R_d C_d = 0.5 \text{ ms}$$

Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	E0 = 1 E1 = 0	E0 = 1 E1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

Open Circuit: When the SLIC is in the Open Circuit state, both the AX(TIPX) and BX(RINGX) power amplifiers are switched off and present high impedance to the line. The Open Circuit state has the lowest power dissipation. Loop detectors are inoperative in this state. This function is useful for allowing line-powered relays to collapse, denying power to out-of-service lines, as well as allowing clearing of line faults.

Ringing: When the SLIC is in the Ringing state, the ring relay driver (RINGOUT) is activated, and the Ring Trip Detector is readable at $\overline{DET}$. Also, the AX(TIPX) and BX(RINGX) are both open circuit. While the SLIC is in the ringing state, signal transmission is inhibited.

Active: In states where normal, Active operation is indicated, the standard battery convention applies; AX(TIPX) is near ground and sources current. BX(RINGX) is near V_{BAT} and sinks current. During active mode operation, all signal transmission and loop supervision functions operate, and the off-hook detector or ground-key detector is gated to $\overline{DET}$.

Disable: The Disable operating state is the SLIC's low-power mode in which the battery feed circuit limits the DC loop current to typically 0.5 (value depends on SLIC version) times the active-mode short circuit current limit. In this state, the off-hook detector works normally.

Tip Open: When the SLIC is in the Tip Open state, the AX(TIPX) power amplifier is switched off so that it presents a high impedance to the line. This mode is provided to facilitate ground start signaling.

Active Polarity Reversal: When the SLIC is in Active Polarity Reversal state, the normal battery feed convention is reversed, with BX(RINGX) approaching ground and sourcing current, while AX(TIPX) approaches battery and sinks current. While AX(TIPX) and BX(RINGX) are in transition, the off-hook function is meaningless because the loop current must pass through zero.

Disable Polarity Reversal: This state is similar to the Disable state, except that the feed is reversed.

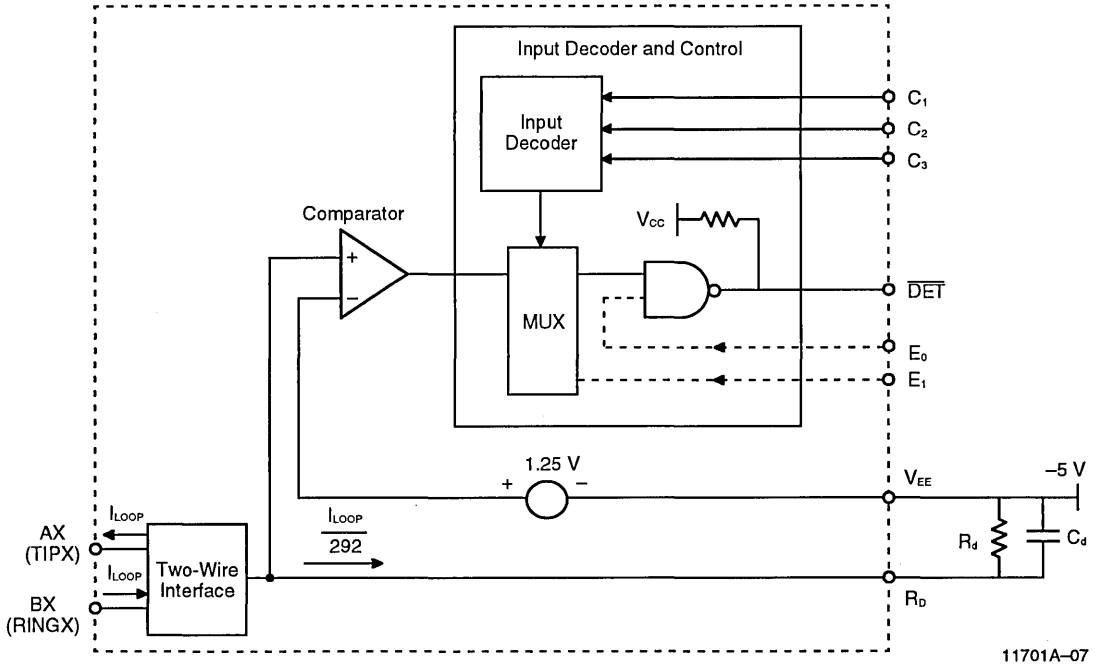

Figure 5. Signaling Off-Hook Detection

Ringing Circuit

A generalized ringing circuit is shown in Figure 6. In common applications, the circuit can be simplified as shown later. During ringing, the ring relay driver is activated and the AX(TIPX) and BX(RINGX) leads are placed in the open circuit state. The ring feed source is connected by the ring relay to the line, through ring feed resistors R_1 and R_2.

The bridging resistors R_{B1}, R_{B2}, R_3, and R_4, and filter capacitors C_{RT1} and C_{RT2}, produce a DC voltage sign reversal between DA and DB when an off-hook occurs.

If R_{LMAX} is the maximum line resistance that is to be detected as an off-hook, the bridging resistors should be chosen such that:

$$\frac{R_{B1}}{R_3} = \frac{R_{B2}}{R_4} = \frac{(R_{LMAX} + R_{FEED})}{R_{LMAX}}$$

Where: $R_{FEED} = R_1 + R_2$

The capacitors reduce the effective amplitude of the ringing signal by a factor of $1/|1+j2\pi f_r t|$.

$$\text{where: } t = \frac{R_3 R_{B1} C_{RT1}}{R_3 + R_{B1}} + \frac{R_4 R_{B2} C_{RT2}}{R_4 + R_{B2}}$$

For $f_r = 20$ Hz ringing, C_{RT} should be chosen to give a value of $t = 50$ ms. This will reduce the ringing by a factor 6.4 and allow detection within 2 ringing cycles.

For balanced ringing, the ringing voltage splits between the ground and battery sides. The resistors should be balanced, (i.e., $R_1 = R_2$, $R_{B1} = R_{B2}$, and $R_3 = R_4$). A single capacitor of half the value between DA and DB can replace the capacitors C_{RT1} and C_{RT2}.

For unbalanced ringing on the ground side, use equal networks with $R_1 = R_2$, $R_{B1} = R_{B2}$, $R_3 = R_4$, and $C_{RT1} = C_{RT2}$.

For unbalanced ringing on the battery side, the following simplification can be made. The positive side of the ringing supply is grounded and R_1 is replaced by a short circuit. In this case, the R_4, R_{B2}, and C_{RT2} network can be combined with other channels into a ringer threshold, because the voltage on the DA pin is independent of line conditions.

Ground-Key Detector

The Ground-Key Detector (for ground-key versions, see Figure 7) compares the longitudinal control current (I_L) to an internally generated threshold current, I_{LT}. The current flowing in the earth loop will be proportional to the longitudinal control current. When the current in the earth loop exceeds the threshold value and E_1 is High, the ground-key signal forces the $\overline{DET}$ output Low.

Ring Relay Driver

A ring relay driver is provided in all versions. The normal functioning driver is an internal transistor, with the collector sourced to BGND and the emitter as the driver output. Some versions may have the collector brought out to a separate pin.

Test Relay Driver

A test relay driver is provided only on dual relay driver versions, and has specifications identical to the ring relay driver. In these versions, the test relay driver is activated by logic 0 at input pin C_4.

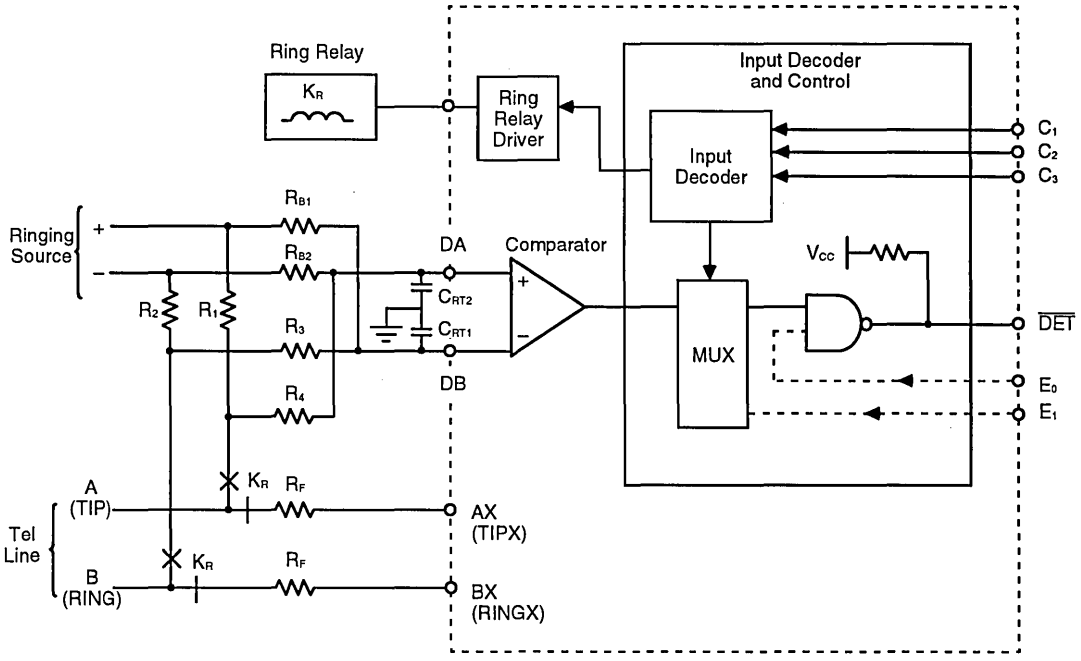

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Figure 6. Ringing Circuit

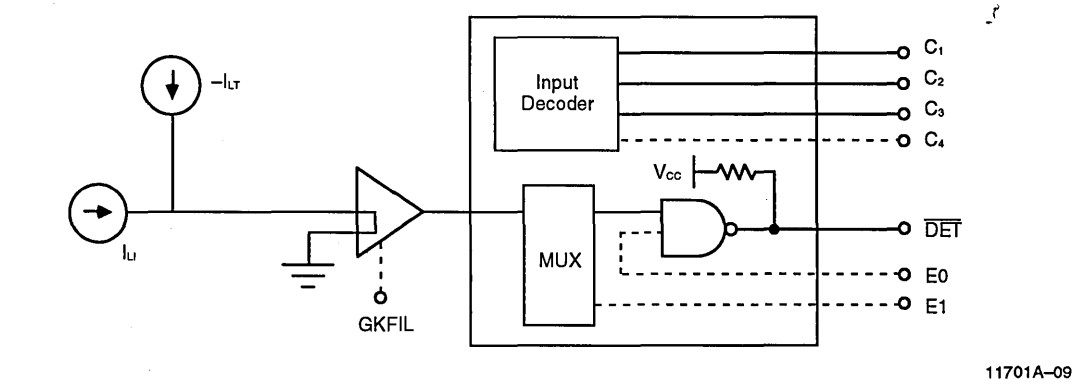

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Figure 7. Ground-Key Detector

PBX SLICs

PBX SLIC

General Description

AMD's PBX SLICs are the Am7942 and Am7943(A). Both are compliant to EIA/TIA-464-A and ETSI-TE10-02 PBX standards, and will operate over a wide range of battery voltages.

The Am7942 incorporates a switching regulator function, similar to that offered on the Central Office SLICs, and is ideal for large PBXs intended for campus environments or other applications where loop length is expected to vary a great deal. In applications such as this, the switching regulator automatically adjusts the voltage applied to the SLIC's amplifiers to the minimum required to achieve the specified loop current, thus minimizing the system's power consumption. In cases where power consumption is not an issue, such as many 24-V battery applications, the switcher can be bypassed, eliminating the need for a few external components and lowering system cost. The Am7942 is tested under both 24- and 48-V battery conditions.

The Am7943(A) also incorporates power management circuitry, but in this case, power is dissipated in an external resistor. This approach, while not minimizing system power dissipation, lowers system cost by eliminating some external component requirements, and maintains device reliability, even at higher battery voltages.

Two versions of the Am7943(A) are offered: the standard Am7943 and the Am7943A. The primary difference between the two versions is the way the devices are tested. The standard version is tested with a 24-V battery and a 600-ohm load to ensure compliance to most PBX requirements. Polarity reversal and other functions not typically required by PBXs are not offered on the standard version. The "A" version of the Am7943 is specified and tested for compliance to Bellcore's TR-TSY-000057 standard required by Digital Loop Carriers (DLCs) and other types of switching equipment. The Am7943A is tested with a 48-V battery and a 900-ohm load.

Both the Am7942 and Am7943 support on-hook transmission and offer extended temperature performance, making either type suitable for Digital Loop Carriers and other applications.

The signal transmission functions of all AMD SLICs include both two-to-four-wire and four-to-two-wire conversion. The two-wire termination impedance is programmable with a single external impedance. The companion AMD SLAC or DSLAC IC (Single-Channel or Dual-Channel Subscriber Line Audio-Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the DSLAC IC is not used, most codec/filters provide an uncommitted op amp for this purpose.

The SLIC's battery feed architecture makes their DC feed characteristics programmable with external resistors. Furthermore, these characteristics are independent of battery variations.

A polarity reversal function is provided on all SLICs which transposes the normal voltage sense of the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode is also provided, limiting loop current and cutting power dissipation while allowing the full complement of supervisory functions to be utilized.

The supervisory functions of off-hook detection and ring trip detection are read through a single, TTL-compatible output. To eliminate noise-induced errors, the off-hook detector signal may be filtered. Off-hook detection has a threshold that is set by the value of an external resistor. Additional supervisory controls put the A lead into an open circuit or high-impedance state suitable for application in ground start systems. Similarly, both the A and B leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Relay drivers support ring and/or test relay functions, or can be used for other functions such as activating a message waiting lamp.

The SLIC's user-programmable states are controlled by a TTL-compatible code. The control inputs are designed to easily interface to popular single-chip microcontrollers, such as the industry standard 8051, or to latched outputs from a SLAC or DSLAC device.

PRELIMINARY

Am7942

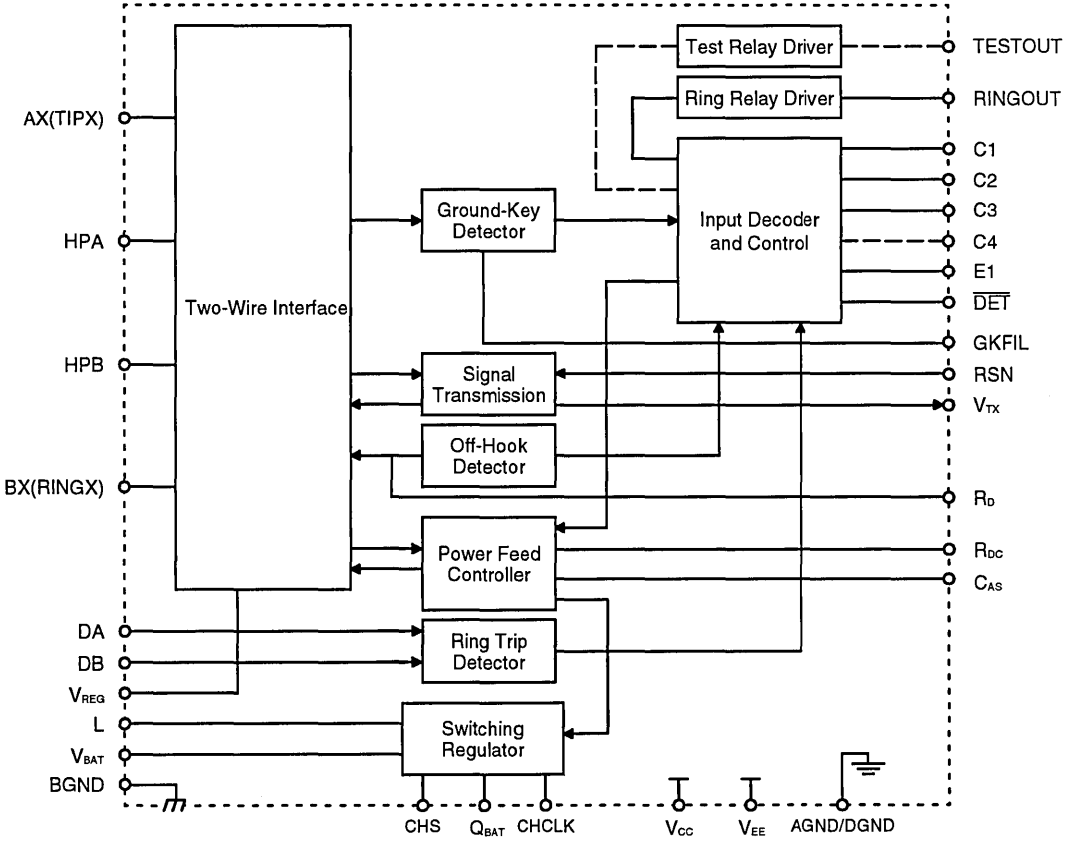
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Receive current gain = 200
- Programmable loop detect threshold
- Low standby power
- Performs polarity reversal
- Ground-key detector
- Pin for external ground-key noise filter capacitor
- Test relay driver option (PLCC only)
- Tip open state for ground start lines
- –19 V to –63 V battery operation
- Meets EIA/TIA–464–A
- On-chip switching regulator for low-power dissipation
- Can be used without switching regulator with 24-V battery
- Two-wire impedance set by single external impedance

BLOCK DIAGRAM



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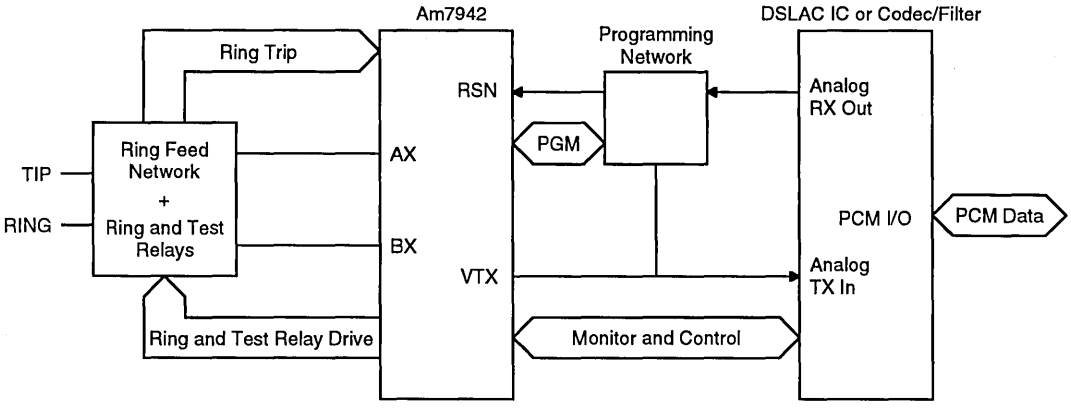
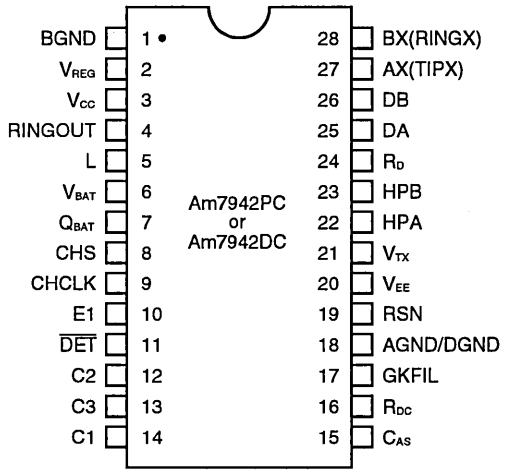
Publication #: 15474 Rev: B Amendment: /0
Issue Date: June 1992

SYSTEM BLOCK DIAGRAM

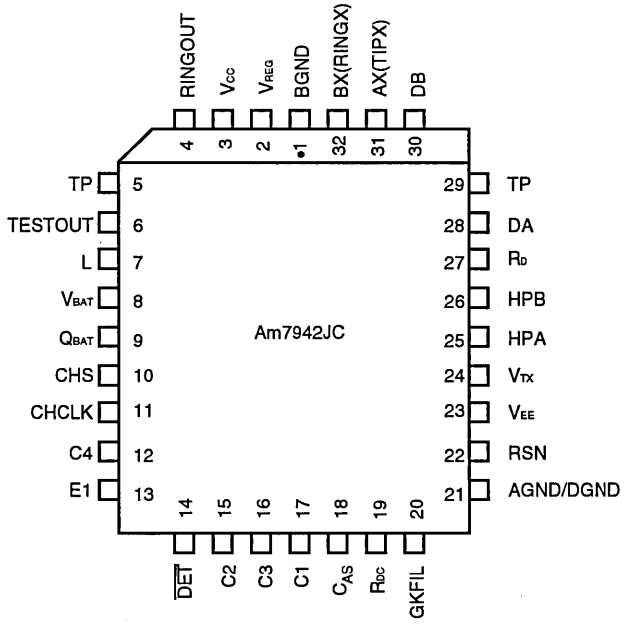


CONNECTION DIAGRAMS

28-Pin Plastic DIP
or
28-Pin Ceramic DIP



32-Pin PLCC

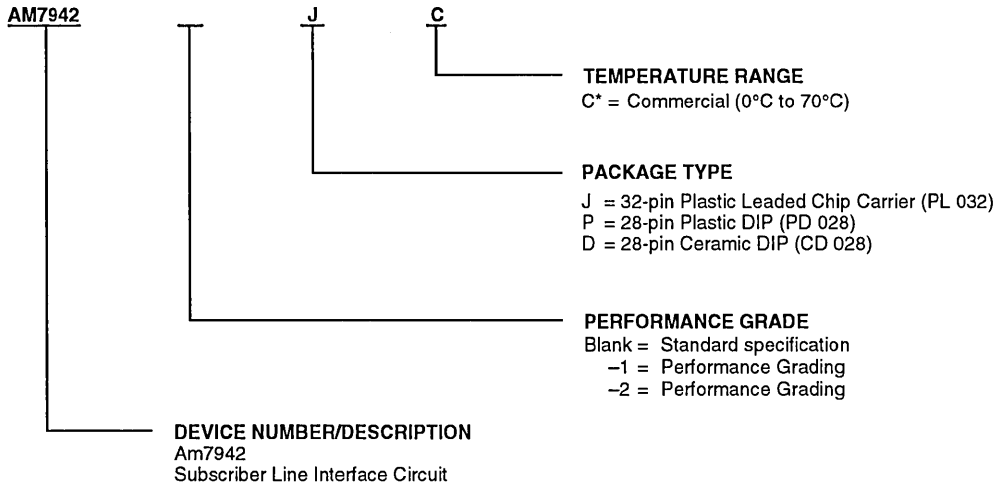


Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7942	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND/DGND
Ground

Analog and Digital ground.

AX(TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX(RINGX)
(Output)

Output of B(RING) power amplifier.

C3–C1 Decoder
(Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

CHCLK
Chopper Clock (Input)—(see Note 1)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (nominal).

CHS
Chopper Stabilization (Input)—(see Note 1)

Connection for external chopper stabilizing components.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15K pull-up resistor.

E1
Ground-Key Enable (Input)

E1 = High connects the ground-key detector to $\overline{\text{DET}}$.
E1 = Low connects the off-hook or ring trip detector to $\overline{\text{DET}}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L
Switching Regulator Power Transistor
(Output)—(see Note 1)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}
Quiet Battery—(see Note 1)

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

TESTOUT
Test Relay Driver (Output)—(see Note 3)

Open collector driver with emitter internally connected to BGND.

C4
Test Relay Driver Command (Input)—(see Note 3)

TTL compatible. A logic Low enables the driver.

GKFIL
(see Notes 2 and 3)

Connection for external ground-key, noise-filter capacitor.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)—(see Note 1)

Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

C_{AS}

Reference Filter Capacitor

A capacitor should be connected to this pin to filter internal anti-saturation reference voltage.

Notes: 1. All pins, except CHCLK, connect to V_{BAT} when using SLIC without a switching regulator. CHCLK is connected to AGND/DGND.

2. To prevent noise pickup by the detection circuits when using ground-key mode (E1 = logical 1), a 3300-pF minimum bypass capacitor is recommended between the GKFIL pin and ground.

3. Not available on standard 28-pin DIP package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –19 V to –63 V*

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

*Can be used without switching regulator components in this range of battery voltages provided maximum power dissipation specifications are not exceeded.

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS (see Note 1)

Description	Test Conditions	Notes	P.G.*	Preliminary Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance		5		3		ohm	
Analog (V_{TX}) Output Offset			 –1 –2	–35 –35 –30		+35 +35 +30	mV
Analog (RSN) Input Impedance	300 Hz to 3.4 kHz				1	20	ohm
Longitudinal Impedance at AX or BX						35	ohm
Overload Level	four-wire two-wire	2		–2.5		+2.5	Vpk
Transmission Performance, two-wire impedance (see Test Circuit D)							
Two-Wire Return Loss	300 Hz to 3400 Hz	5, 10		26			dB
Longitudinal Balance (two-wire and four-wire, see Test Circuit C); R_L = 600 ohms							
Longitudinal to Metallic L-T, L-4	200 Hz to 1 kHz Normal Polarity		 –1 –2	52 63 63			dB
	200 Hz to 1 kHz Reverse Polarity		 –1 –2	52 54 54			dB
	1 kHz to 3.4 kHz Normal Polarity		 –1 –2	52 58 58			dB
	1 kHz to 3.4 kHz Reverse Polarity		 –1 –2	52 54 54			dB
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz Reverse Polarity		 –1 –2	40 40 42			dB
Longitudinal Current Capability per Wire	Active State		all		28		mA
	Disable State		all		18		RMS
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B) Battery = –48 V, R_{LDC} = R_{LAC} = 600 ohms; Battery = –24 V, R_{LDC} = 300 ohms, R_{LAC} = 600 ohms							
Gain Accuracy	0 dBm, 1 kHz		 –1 –2	–0.15 –0.15 –0.10		+0.15 +0.15 +0.10	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz		 –1 –2	–0.15 –0.15 –0.10		+0.15 +0.15 +0.10	dB
Gain Tracking	+7 dBm to –55 dBm Reference: –0 dBm	5		–0.10		+0.10	dB

*P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Balance Return Signal (four-wire to four-wire, see Test Circuit B) **Battery = –48 V, R_{LDC} = R_{LAC} = 600 ohms; Battery = –24 V, R_{LDC} = 300 ohms, R_{LAC} = 600 ohms**							
Gain Accuracy	0 dBm, 1 kHz		–1 –2	–0.15 –0.15 –0.10		+0.15 +0.15 +0.10	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	3		–0.10		+0.10	dB
Gain Tracking	+3 dBm to –55 dBm Reference: 0 dBm	5		–0.10		+0.10	dB
Group Delay	f = 1 kHz	5, 12			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B) **Battery = –48 V, R_{LDC} = R_{LAC} = 600 ohms**							
Harmonic Distortion 300 Hz to 3400 Hz	0 dBm +7 dBm				–64 –55	–50 –40	dB
Idle Channel Noise **Battery = –48 V, R_{LDC} = R_{LAC} = 600 ohms; Battery = –24 V, R_{LDC} = 300 ohms, R_{LAC} = 600 ohms**							
C-Message Weighted Noise	two-wire four-wire	5			+7 +7	+10 +10	dBrnC
Psophometric Weighted Noise	two-wire four-wire				–83 –83	–80 –80	dBmp
Single Frequency Out-of-Band Noise (see Test Circuit E)							
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics*	5 4, 5, 8 4, 5			–76 –76 –63		dBm
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics*	5 4, 5, 8 4, 5			–70 –85 –57		dBm
Line Characteristics (see Figures 1a, 1b, 1c)							
Short Loops, Active Mode	Battery = –24 V, R_{LDC} = 300 ohms Battery = –43 V, R_{LDC} = 600 ohms Battery = –48 V, R_{LDC} = 600 ohms	5, 9 5		32.4	35.0	37.6	mA
Long Loops, Active Mode	Battery = –24 V, R_{LDC} = 640 ohms Battery = –43 V, R_{LDC} = 1300 ohms Battery = –48 V, R_{LDC} = 1900 ohms	5, 9 5		20.0 23.0 18.0			mA
Disable Mode	Battery = –24 V, R_{LDC} = 600 ohms Battery = –48 V, R_{LDC} = 600 ohms	5, 9		15.5	17.5	19.5	mA
Loop Current	Tip Open, R_L = 0 Disconnect, R_L = 0					1.0	mA
ILLIM (ITip & IRing)	Tip and Ring Shorted to Ground				70	105	mA

*Applies only when switching regulator is used.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Power Dissipation Battery, Normal Loop Polarity							
On-Hook Open Circuit	Battery = –24 V, w/o Switching Reg.	9			30	75	mW
	Battery = –48 V, with Switching Reg.				35	100	
On-Hook Disable Mode	Battery = –24 V, w/o Switching Reg.	9		100	175		
	Battery = –48 V, with Switching Reg.				135	225	
On-Hook Active Mode	Battery = –24 V, w/o Switching Reg.	9			135	225	
	Battery = –48 V, with Switching Reg.				180	300	
Off-Hook Disable Mode	Battery = –24 V, w/o Switching Reg.	9			500	800	
R_L = 50 ohms	Battery = –48 V, with Switching Reg.				400	750	
Off-Hook Active Mode	Battery = –24 V, w/o Switching Reg.	9			800	1100	
R_L = 50 ohms	Battery = –48 V, with Switching Reg.				800	1000	
Supply Currents, Battery = –24 V or –48 V							
V_{CC} On-Hook Supply Current	Open Circuit Mode	9			3.0	4.5	mA
	Disable Mode				6.0	10.0	
	Active Mode				7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode	9			1.0	2.3	
	Disable Mode				2.2	3.5	
	Active Mode				2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode	9			0.4	1.0	
	Disable Mode				3.0	5.0	
	Active Mode				4.0	6.0	
Power Supply Rejection Ratio (Vripple = 50 mV RMS)							
V_{CC}	50 Hz to 3400 Hz	6		25	45		dB
	3.4 kHz to 50 kHz			22	35		
V_{EE}	50 Hz to 3400 Hz	6		20	40		
	3.4 kHz to 50 kHz			10	25		
V_{BAT}	50 Hz to 3400 Hz	6		27	45		
	3.4 kHz to 50 kHz			20	40		
Effective Int. Resistance	C_{AS} to GND	5		85	170	255	Kohm
Off-Hook Detector							
Current Threshold	$I_{DET} = 365/R_D$			–20		+20	%
Ground-Key Detector Thresholds, Active Mode							
Ground-Key Resistance Threshold	Battery = –24 V, B(Ring) to GND	9		1.0	2.2	4.5	Kohm
	Battery = –48 V, B(Ring) to GND			2.0	5.0	10.0	
Ground-Key Current Threshold	B(Ring) to GND	7			9		mA
	Midpoint to GND				9		
Effective Int. Resistance	GKFIL to AGND/DGND	5		18	36	54	Kohm
Ring Trip Detector Input							
Bias Current				–5	–0.05		µA
Offset Voltage	Source Resistance = 0 to 2 Mohm	11		–50	0	+50	mV

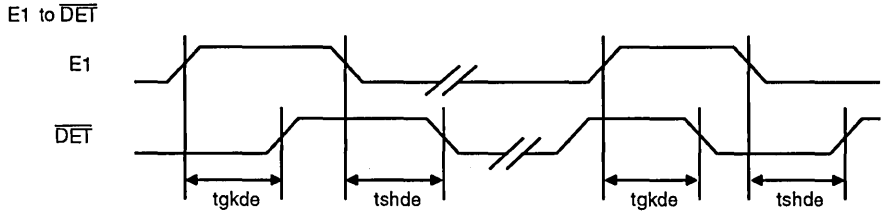
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Preliminary Min	Typ	Max	Unit
Logic Inputs (C1, C2, C3, C4, E0, E1, and CHCLK)							
Input High Voltage				2.0			V
Input Low Voltage						0.8	V
Input High Current				–75		40	µA
Input Low Current				–0.4			mA
Logic Output ($\overline{DET}$)							
Output Low Voltage	I_{OUT} = 0.8 mA					0.4	V
Output High Voltage	I_{OUT} = –0.1 mA			2.4			V

SWITCHING CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E1 High to $\overline{DET}$ High	Ground-Key Detect Mode	–	–	3.8	µs
	E1 High to $\overline{DET}$ Low	R_L Open, R_G Connected (see Test Circuit H)	–	–	1.1	
tshde	E1 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.2	µs
	E1 Low to $\overline{DET}$ High	R_L = 600 ohms, R_G Open (see Test Circuit G)	–	–	3.8	

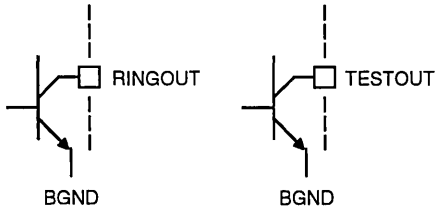
SWITCHING WAVEFORMS



Note: All delays measured at 1.4-V levels.

15474A–005

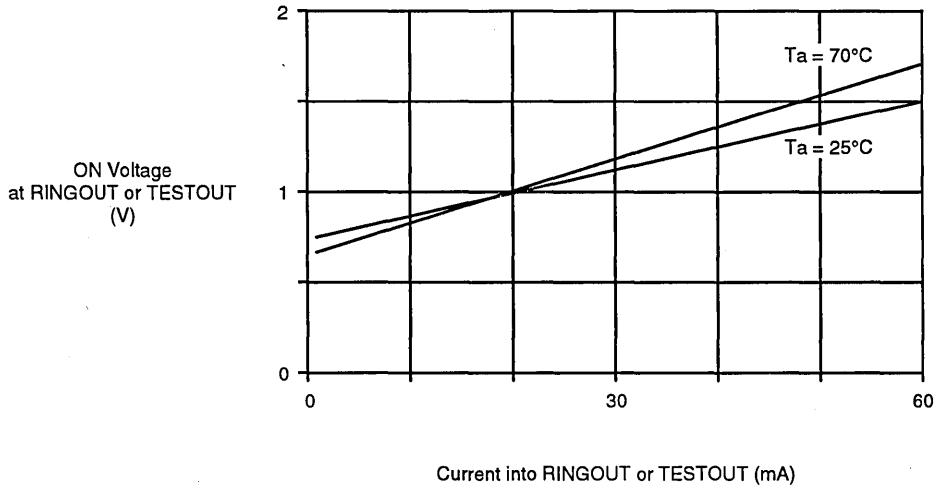
RELAY DRIVER SPECIFICATIONS



15474A–006

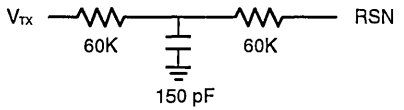
Description	Test Conditions	Note	Preliminary Min	Typ	Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)						
On Voltage	25 mA Sink				+1.5	V
Off Leakage	V_{OH} = +15 V				100	µA

RELAY DRIVER CHARACTERISTICS (typical)



Notes:

1. Unless otherwise noted, test conditions are: Battery = −48 V, V_{CC} = +5 V, V_{EE} = −5 V, R_L = 600 ohms, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 7.14K, C_{DC} = 0.47 µF, R_d = 35.4K, C_{CAS} = 0.47 µF, no fuse resistors, R_T = 120K, and R_{RX} = 60K. Switching regulator components: L = 1 mH, C_{FIL} = 0.47 µF (see Application Circuit).
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes the two-wire AC load impedance matches the programmed impedance.
4. For frequencies below 12 kHz, these tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms. For frequencies greater than 12 kHz, a longitudinal impedance of 90 ohms and a metallic impedance of 135 ohms is used. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
8. Fundamental and harmonics from 256-kHz switch regulator chopper are not included.
9. For −24-V battery, switching regulator is disabled. L, CHS, and V_{REG} pins connected to V_{BAT} pin; CHCLK pin connected to AGND/DGND.
10. Assumes the following Z_T network:



11. Tested with 0 ohm source impedance. Two Mohms are specified for system design purposes only.
12. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC device.

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F^*)$	Z_T is connected between the V_{TX} and RSN pins.The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42_L} \cdot \frac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN. Z_T is defined above, and $G42_L$ is the desired receive gain.
$R_{DC1} + R_{DC2} = 500/I_{LOOP}$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to −5 V, and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_C}$	C_{CAS} is the regulator filter capacitor, and f_C is the desired filter cut-off frequency.

*R_{FUSE} = 20 ohm–50 ohm, user selectable.

$R_{DC1} + R_{DC2} = R_{DC} = 14.28K$

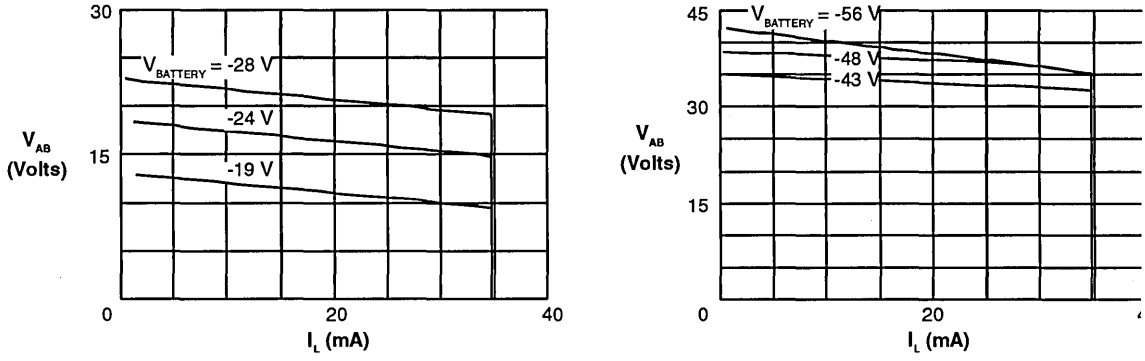


Figure 1a. Load Line (Typical)

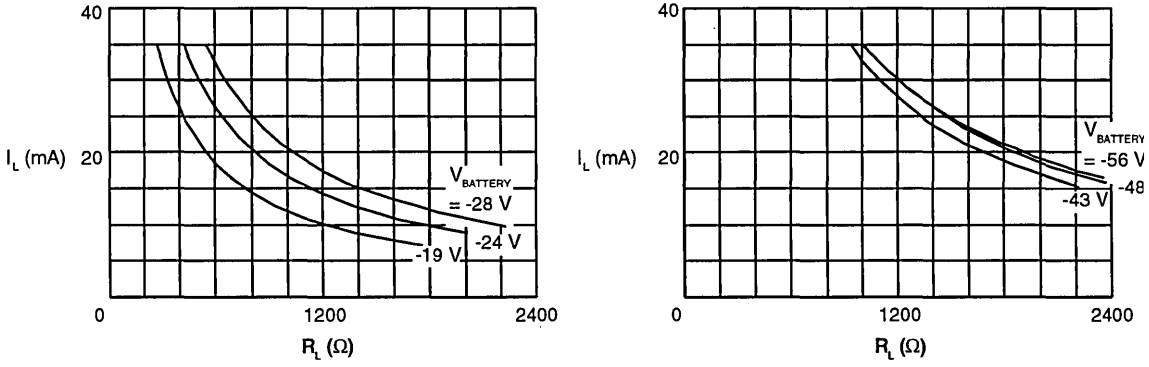
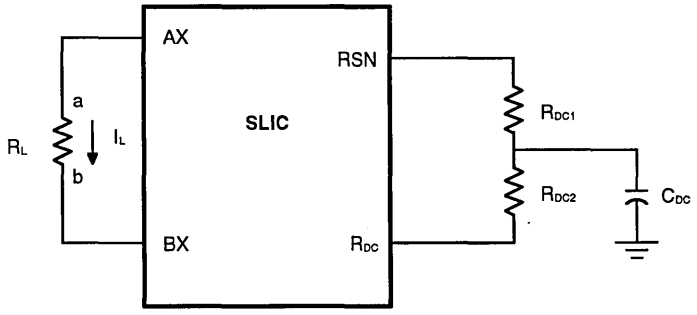


Figure 1b. Feed Characteristics (Typical)

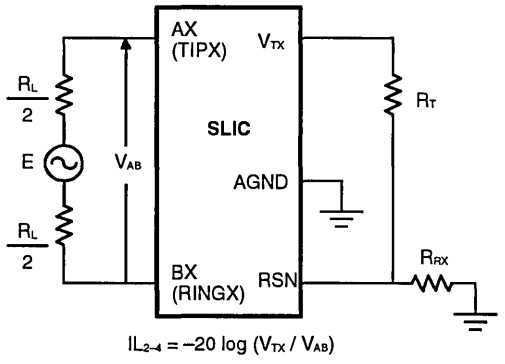


Feed Current programmed by R_{DC1} and R_{DC2}.

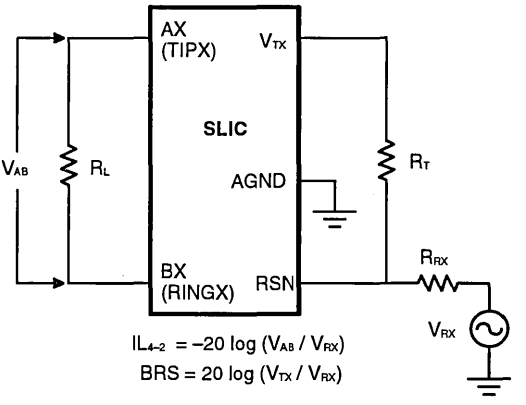
15474A-009

Figure 1c. Feed Programming

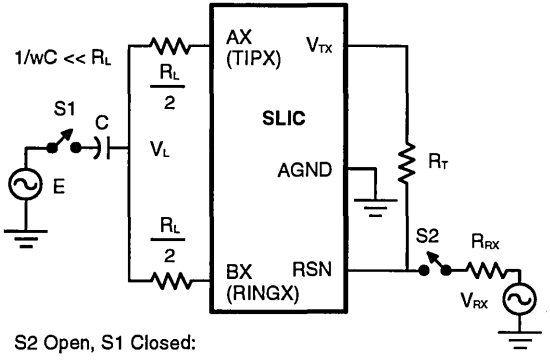
TEST CIRCUITS



A. Two-to-Four Wire Insertion Loss



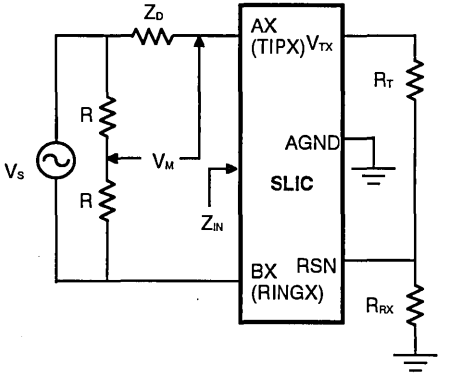
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 log (V_{AB}/E)
L-4 Long. Rej. = 20 log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 log (V_L/V_{RX})

C. Longitudinal Balance



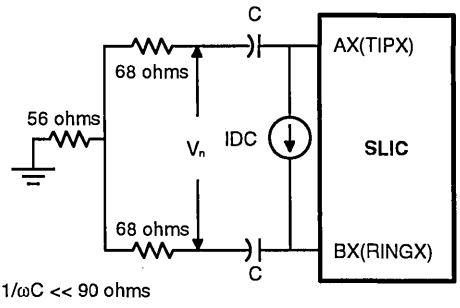
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = –20 log (2 V_M/V_S)

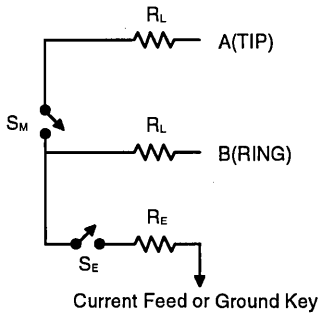
D. Two-Wire Return Loss Test Circuit

15474A–010

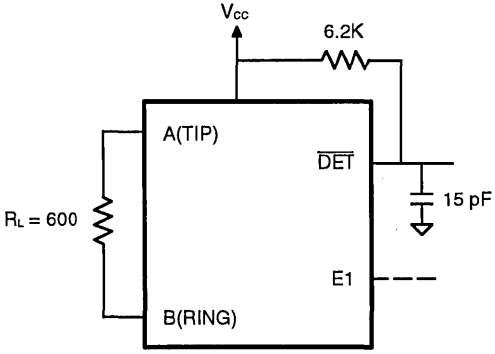
TEST CIRCUITS (continued)



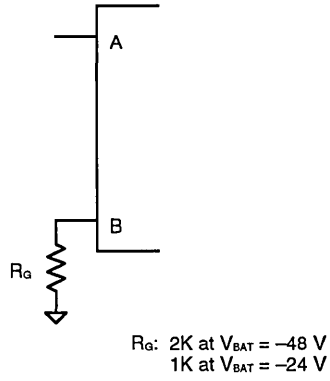
E. Single-Frequency Noise



F. Ground-Key Detection Center Point Test



G. Loop Detector Switching



H. Ground-Key Switching

15474A–010

ADVANCE INFORMATION

Am7943(A)

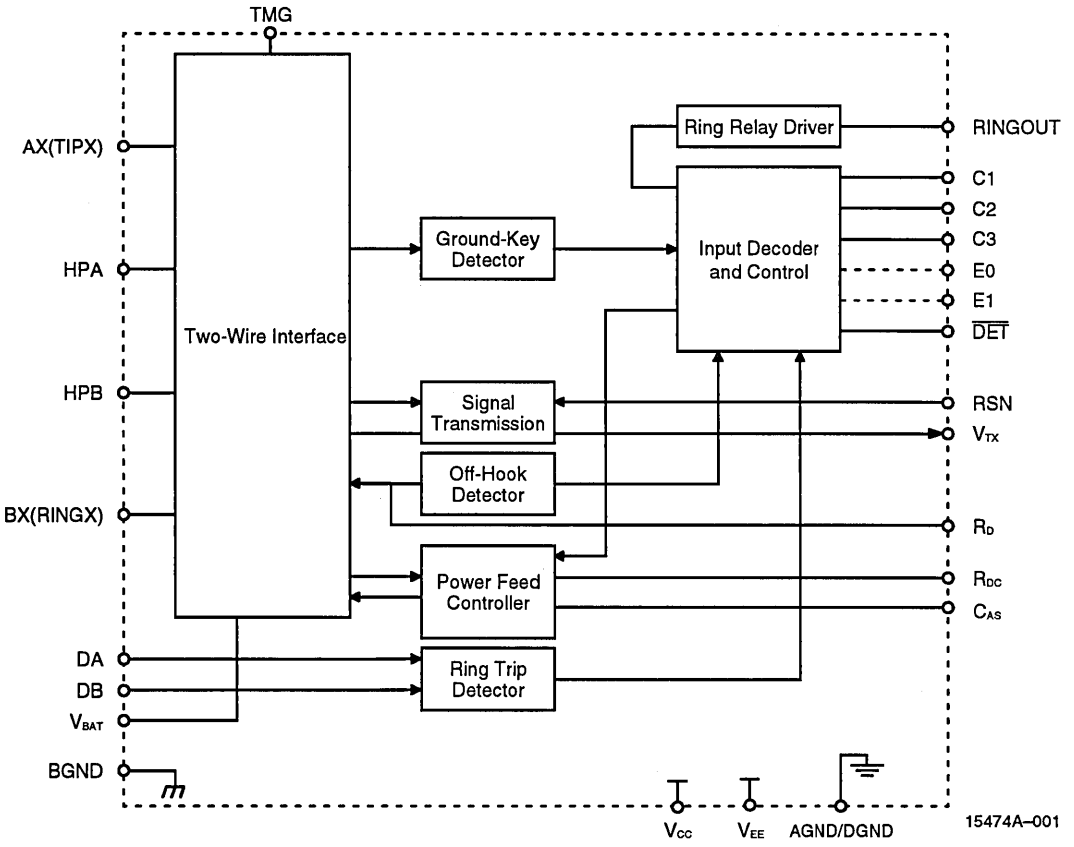
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Current gain = 200
- Programmable loop detect threshold
- Low standby power
- Performs polarity reversal (A version)
- Ground-key detector
- 0°C to +70°C ambient temperature range
- Tip open state for ground start lines
- –19 V to –56.5 V battery operation
- Two-wire impedance set by single external impedance
- On-hook transmission
- On-chip ring relay driver and relay snubber circuit
- A version satisfies TR-TSY-000057 requirements
- Standard version satisfies EIA/TIA-464-A

BLOCK DIAGRAM

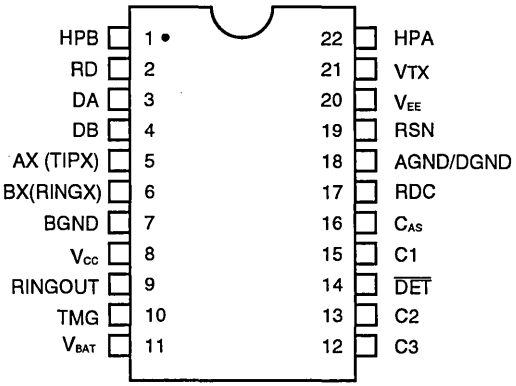


This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication #: 16853 Rev: A Amendment: /0
Issue Date: June 1992

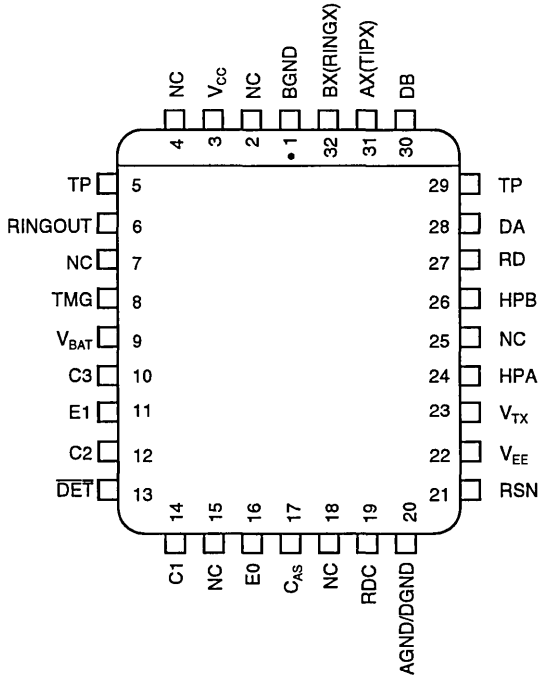
CONNECTION DIAGRAMS

22-Pin Plastic DIP
or
22-Pin Ceramic DIP



16853A-01

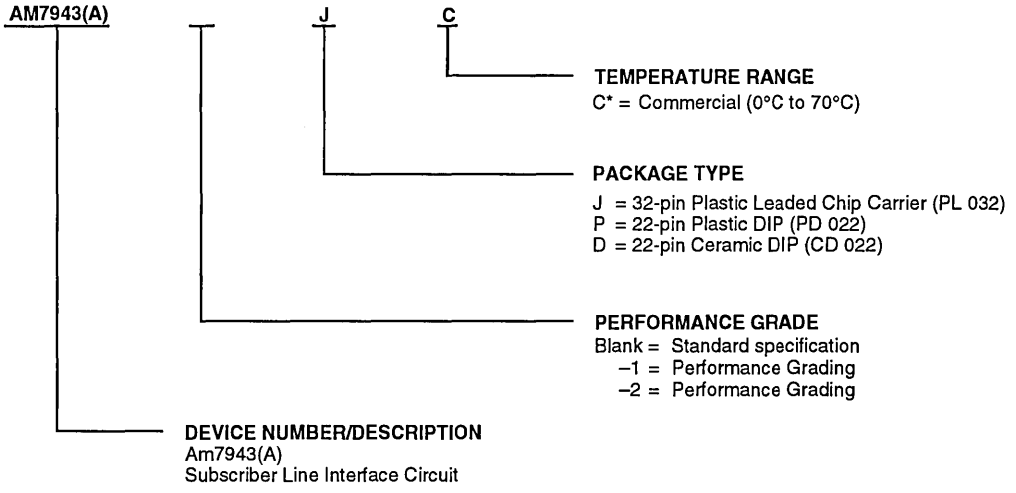
32-Pin PLCC



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. NC = No connect.

ORDERING INFORMATION
Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7943(A)	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND/DGND
Ground

Analog and Digital ground.

AX(TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX(RINGX)
(Output)

Output of B(RING) power amplifier.

C3–C1 Decoder
(Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0, E1). The output is open-collector with a built-in 15K pull-up resistor.

E0
Ground-Key Enable (Input)

A logic High enables $\overline{DET}$. Low disables $\overline{DET}$ (PLCC only).

E1
Ground-Key Enable (Input)

E1 = Low connects the ground-key or ring-trip detector to $\overline{DET}$; E1 = High connects the off-hook or ring-trip detector to $\overline{DET}$ (PLCC only).

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

RD

Threshold modification and filter point for the off-hook detector.

RDC

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{TX}
Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

C_{AS}
Reference Filter Capacitor

A capacitor should be connected to this pin to filter internal anti-saturation reference voltage.

TMG
Thermal Management

A resistor connected from this pin to V_{BAT} reduces the on-chip power dissipation in the normal polarity, active state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

AGND/DGND with respect to
BGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT ..... BGND to +10 V

Current through Relay Driver
or internal driver catch diodes ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

C3–C1, E0, E1 to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation (see note) ... T_A = 70°C

In 22-pin ceramic DIP package ..... 1.5 W
In 22-pin plastic DIP package ..... 1.25 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never reach this temperature, and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) ..... 0°C to +70°C

Supply Voltage (V_{CC}) ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –19 V to –56.5 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the device specifications are guaranteed.

ELECTRICAL CHARACTERISTICS (see Note 1, page 1-45)

The Am7943 (non-A) device is tested under the following conditions unless otherwise noted. Battery = –24 V, RL = 600 ohms. The Am7943(A) device is tested under the following conditions unless otherwise noted. Battery = –48 V, RL = 900 ohms. All specifications apply to both the Am7943 and Am7943(A) unless noted.

Description	Test Conditions	Notes	P.G.*	Advance Information Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance					3		ohm
Analog (V_{TX}) Output Offset				–30		+30	mV
Analog (RSN) Input Impedance	300 Hz to 3.4 kHz				1	20	ohm
Longitudinal Impedance at AX or BX						35	ohm
Overload Level	four-wire active state	2		–2.5		+2.5	Vpk
	two-wire active state						
	On-hook, R_{LAC} = 900 ohm Active or Disable State	2		0.95			Vrms
Transmission Performance							
Two-Wire Return Loss (see Test Circuit D)	200 Hz to 3400 Hz	4, 8		26			dB
Longitudinal Balance (two-wire and four-wire, see Test Circuit C); RL = 600 ohms at V_{BAT} = 24 V, RL = 740 ohms at V_{BAT} = 48 V							
Longitudinal to Metallic L-T, L-4	200 Hz to 1 kHz Normal Polarity		–1	54			dB
			–2	63			
				63			
	1 kHz to 3.4 kHz Normal Polarity		–1	54			dB
			–2	58			
				58			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz Normal Polarity			42			dB
Longitudinal Current	Active State			27	35		mA RMS
	Disable State			27	35		
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)							
Gain Accuracy	0 dBm, 1 kHz			–0.15		+0.15	dB
Gain Accuracy, Disable Mode	–10 dBm, On-hook, R_{LAC} = 900 ohms			–1.0		+1.0	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz			–0.10		+0.10	dB
Gain Tracking	+7 dBm to –55 dBm Reference: 0 dBm	4		–0.10		+0.10	dB

*P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Balance Return Signal (four-wire to four-wire, see Test Circuit B)							
Gain Accuracy	0 dBm, 1 kHz			–0.15		+0.15	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	3		–0.10		+0.10	dB
Gain Tracking	+3 dBm to –55 dBm Reference: 0 dBm	4		–0.10		+0.10	dB
Group Delay	f = 1 kHz	4, 9			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Harmonic Distortion 300 Hz to 3400 Hz	two-wire level = 0 dBm				–64	–50	dB
	two-wire level = +7 dBm				–55	–40	
Idle Channel Noise							
C-Message Weighted Noise	two-wire	4		+7		+10	dBrnc
	four-wire			+7		+10	
Psophometric Weighted Noise	two-wire			–83		–80	dBmp
	four-wire			–83		–80	
Line Characteristics, Active Mode (see Figures 1a and 1b)							
Short Loops, Active Mode	Battery = –43 V, R_{LDC} = 600 ohms	4		25	27	29	mA
	Battery = –48 V, R_{LDC} = 600 ohms						
	Battery = –24 V, R_{LDC} = 300 ohms						
Long Loops, Active Mode	Battery = –43 V, R_{LDC} = 1.3 K			23			mA
	Battery = –48 V, R_{LDC} = 1.9 K			18			
Disable Mode	Battery = –48 V, R_{LDC} = 600 ohms			17	19	21	mA
	Battery = –24 V, R_{LDC} = 300 ohms						
Standby Mode	$IL = \frac{\lvert V_{BAT} \rvert - 3\,V}{RL + 1800}$, $T_A = 25°C$			.7IL	IL	1.3IL	mA
Loop Current	Tip open, RL = 0					1	mA
	Disconnect, RL = 0					1	
ILLIM (Itip + Iring)	Tip and Ring Shorted to Ground				100	130	mA
Open Circuit Voltage	Battery = –48 V, Active and Disable			41.3	42.3		V
	Battery = –24 V, Active and Disable			16	17.3		V

*Applies only when switching regulator is used.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Power Dissipation, Normal Loop Polarity, Battery = −48 V							
On-Hook, Open Circuit					25	70	mW
On-Hook, Disable Mode					120	210	
On-Hook, Active Mode					160	280	
On-Hook, Standby Mode					35	85	
Off-Hook, Disable Mode	RL = 300 Ω, RTMG = ∞						
	Battery = −48 V				900	1050	
	Battery = −24 V				470	560	
	RL = 300 Ω, RTMG = 1700				250	600	
Off-Hook, Active Mode	RL = 300 Ω, RTMG = ∞						W
	Battery = −48 V				1.25	1.45	
	Battery = −24 V				.6	.75	
	RL = 300 Ω, RTMG = 1700				.65	.85	
Off-Hook, Standby Mode	RL = 300 Ω, T_A = 25°C				.88	1.20	
Supply Currents							
V_{CC} On-Hook Supply Current	Open Circuit Mode				1.5	2	mA
	Disable Mode				4	7.5	
	Standby Mode				2	2.5	
	Active Mode				5	8.5	
V_{EE} On-Hook Supply Current	Open Circuit Mode				0.7	2	
	Disable Mode				2	3.5	
	Standby Mode				0.7	2	
	Active Mode				2.5	5	
V_{BAT} On-Hook Supply Current	Open Circuit Mode				0.3	1	
	Disable Mode				2.5	4.7	
	Standby Mode				0.8	1.5	
	Active Mode				3.5	5.7	
Power Supply Rejection Ratio (Vripple = 50 mV RMS), Active Normal Mode							
V_{CC}	50 Hz to 3400 Hz	5		35	45		dB
V_{EE}	50 Hz to 3400 Hz	5		30	45		
V_{BAT}	50 Hz to 3400 Hz	5		35	45		
Effective Int. Resistance	C_{AS} Pin to Ground	4		85	170	255	Kohm
RFI Rejection	100 Hz to 30 MHz (See Figure E)	4				1	mVRMS
Off-Hook Detector							
Current Threshold	I_{DET} = 365/RD			−10		+10	%
Ground-Key Detector Thresholds, Active Mode							
Resistance Threshold	B(Ring) to GND			2.0	5.0	10.0	Kohm
Ground-Key Current Threshold	B(Ring) to GND	6			9		mA
	Midpoint to GND				9		
Ring Trip Detector Input							
Bias Current				−0.5	−0.05		µA
Offset Voltage	Source Resistance = 2 Mohm	7		−50	0	+50	mV

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Logic Inputs (C1, C2, C3, E0, and E1							
Input High Voltage				2.0			V
Input Low Voltage						0.8	V
Input High Current	All inputs except C3			–75		40	µA
Input High Current	Input C3			–75		150	µA
Input Low Current				–0.4			mA
Logic Output ($\overline{DET}$)							
Output Low Voltage	I_{OUT} = 0.8 mA					0.4	V
Output High Voltage	I_{OUT} = –0.1 mA			2.4			V

Table 1. SLIC Decoding

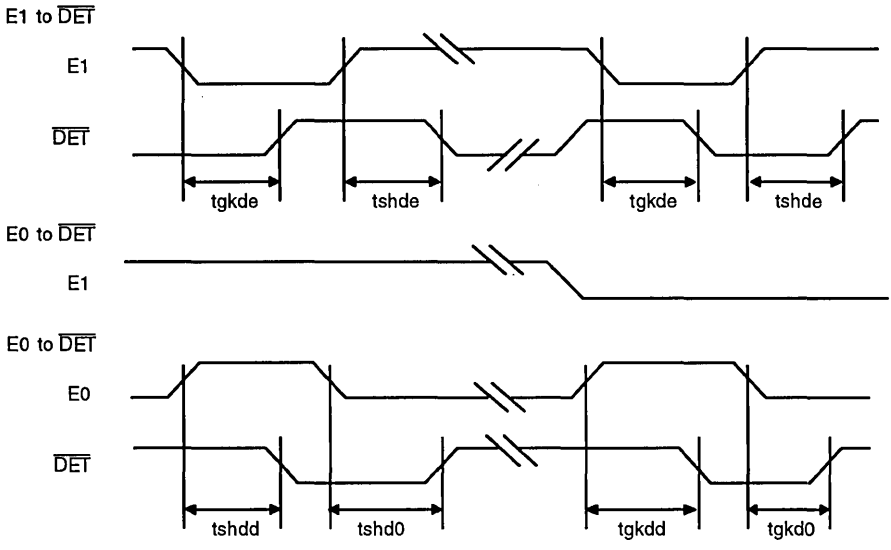
State	C3	C2	C1	Two-Wire Status	$\overline{DET}$ Output E1 = 1	$\overline{DET}$ Output E1 = 0
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	Ground Key
5	1	0	1	Standby	Loop Det.	Ground Key
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

Note: E0 and E1 are internally pulled High and, in the 22-pin DIP package option, are not pinned-out.

SWITCHING CHARACTERISTICS (32-Pin PLCC Only)

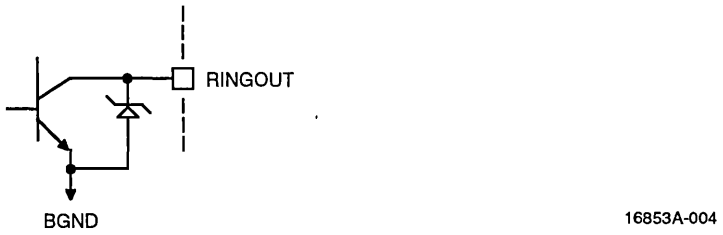
Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect Mode RL Open, RG Connected (see Test Circuit H)	–	–	3.8	µs
	E1 Low to $\overline{DET}$ Low (E0 = 1)		–	–	1.1	
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switch Hook Detect Mode R_L = 600 ohms, RG Open (see Test Circuit G)	–	–	1.2	µs
	E1 High to $\overline{DET}$ High (E0 = 1)		–	–	3.8	
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)				1.1	
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)				3.8	
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)				1.1	
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)				3.8	

SWITCHING WAVEFORMS



Note: All delays measured at 1.4-V levels.

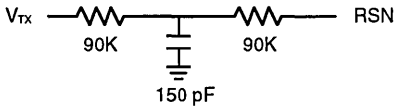
RELAY DRIVER SPECIFICATIONS



Description	Test Conditions	Note	Advance Information Min	Typ	Max	Unit
Relay Driver Output (RINGOUT)						
On Voltage	30 mA Sink			+0.3	+0.6	V
Off Leakage	V_{OH} = +5 V				100	µA
Zener Breakover	100 µA		6	7.2		V
Zener On Voltage	30 mA			10		V

Notes:

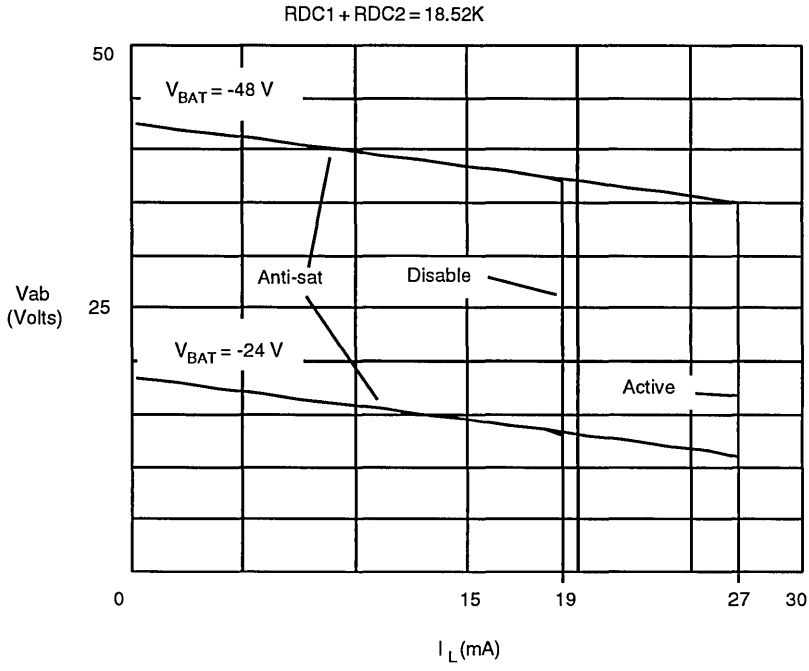
1. Unless otherwise noted, test conditions are: V_{CC} = +5 V, V_{EE} = –5 V, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 9.26 Kohms, C_{DC} = 0.33 µF, RD = 35.4K, C_{AS} = 0.33 µF, and no fuse resistors. For the Am7943 (non-A): Battery = –24 V, RL = 600 ohms, and R_{MG} = ∞. For the Am7943A: Battery = –48 V, RL = 900 ohms, and R_{MG} = 1700 ohms.
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
6. Midpoint is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
7. Tested with 0 ohm source impedance. Two Mohm is specified for system design only.
8. Assumes the following Z_T network:



9. Group delay can be considerably reduced by using a ZT network such as that shown in Note 8 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC device.

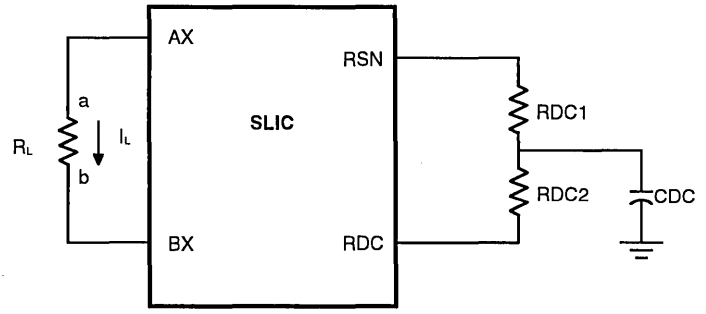
Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \bullet \frac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN. Z_T is defined above, and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 500/I_{LOOP}$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
RD = 365/I_T, CD = 0.5 ms/RD	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and fc is the desired filter cut-off frequency.
$R_{MG} \geq \frac{V_{BAT} - 6\ V}{I_{LOOP}}$	R_{MG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC.



In anti-sat region: $V_L = V_{BAT} - 5.7 - \frac{R_{DC}}{70} \cdot I_L$.

Figure 1a. Load Line (Typical)

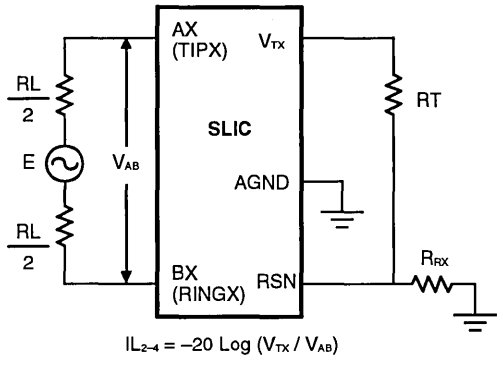


Feed Current programmed by R_{DC1} and R_{DC2}.

15474A–009

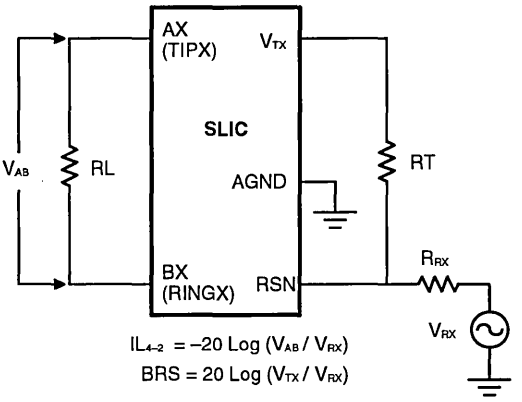
Figure 1b. Feed Programming

TEST CIRCUITS



$IL_{2-4} = -20 \text{ Log } (V_{TX} / V_{AB})$

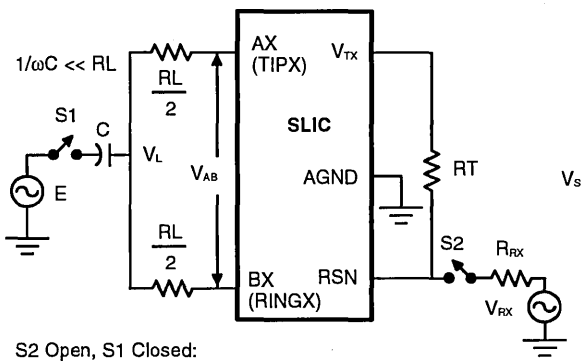
A. Two-to-Four Wire Insertion Loss



$IL_{4-2} = -20 \text{ Log } (V_{AB} / V_{RX})$

$BRS = 20 \text{ Log } (V_{TX} / V_{RX})$

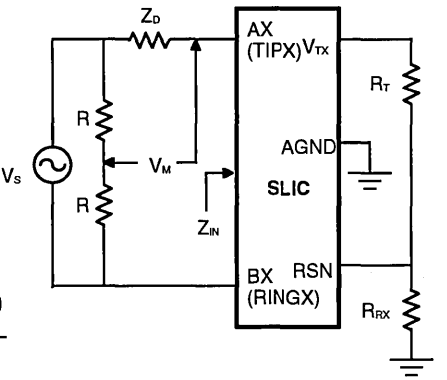
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 Log (V_{AB}/E)
L-T Long. Rej. = 20 Log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 Log (V_L/V_{RX})

C. Longitudinal Balance (IEEE 455-1984)



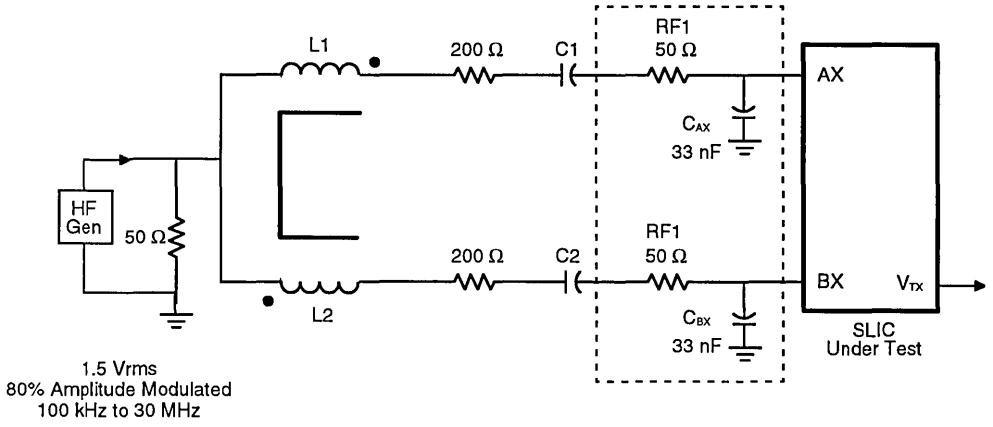
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = $-20 \text{ Log } (2 V_M / V_S)$

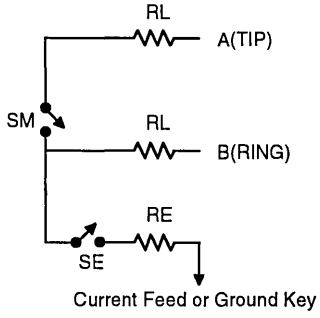
D. Two-Wire Return Loss Test Circuit

15474A-010

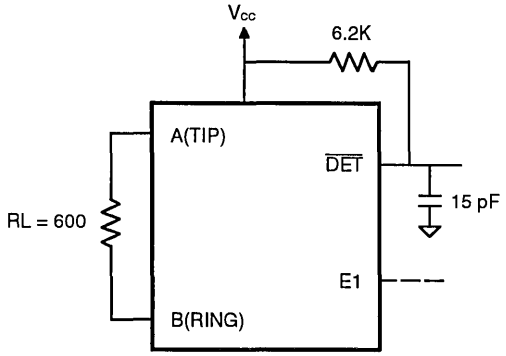
TEST CIRCUITS (continued)



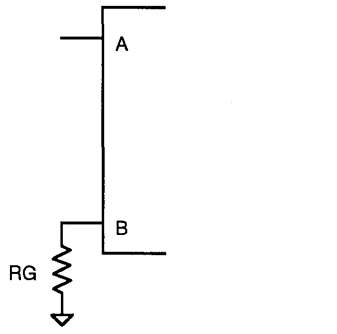
E. RFI Test Circuit



F. Ground-Key Detection Center Point Test



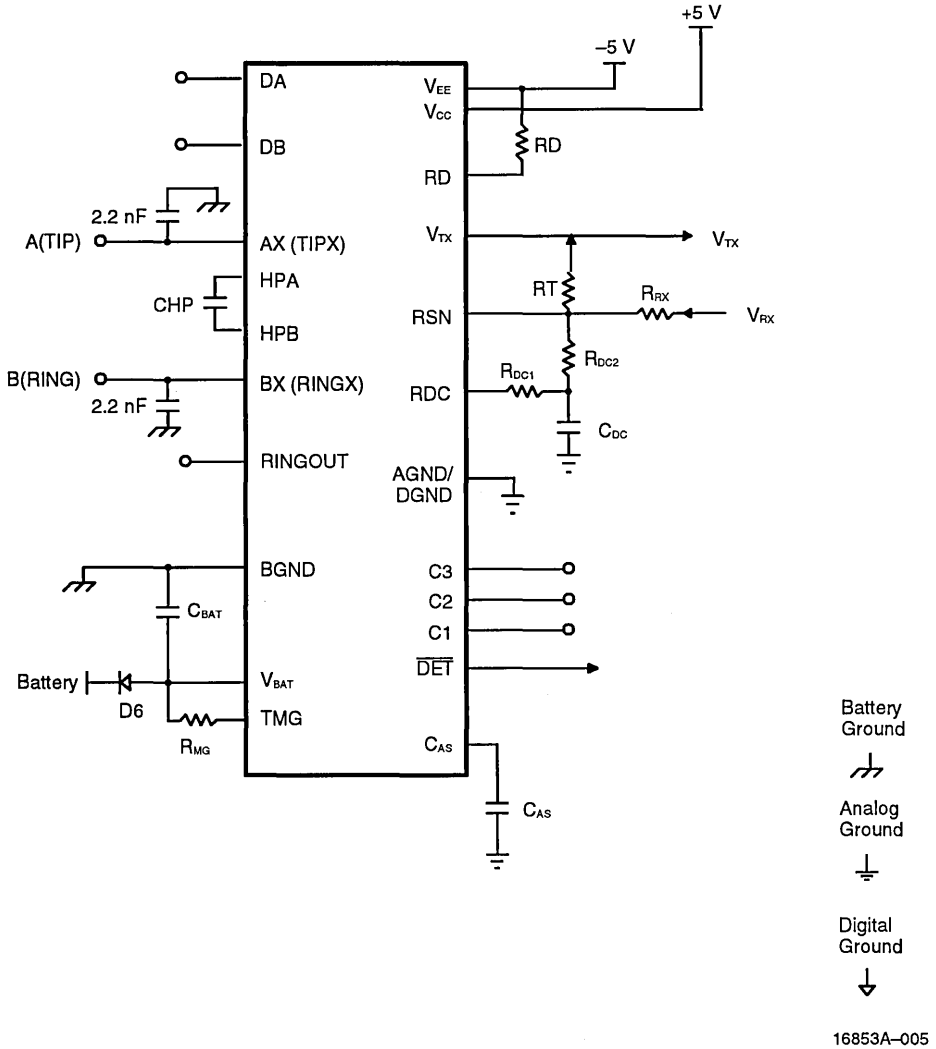
G. Loop Detector Switching



H. Ground-Key Switching

15474A–010

TEST CIRCUITS (continued)



I. Am7943 Test Circuit

PBX SLICs

Application Notes

The AMD PBX SLIC Family offers a high degree of versatility for applications in many PBX, DLC, and other types of line circuits. In this section, typical single-channel and multiple-channel applications are described.

Figure 1 shows a detailed schematic of a single line of a basic system using one SLIC and one-half of an Am79C02 DSLAC IC.

In the receive path, the DSLAC IC processes digital PCM voice data into analog signals and inputs them to the SLIC RSN pin through resistor RRX. In the transmit path, the analog output at the SLIC V_{TX} pin is processed by the DSLAC IC and output in serial-digital format to the PCM interface. RRX sets the receive gain, and R_T is used to synthesize the AC two-wire output impedance. Both RT and RRX can be complex to achieve optimized parameters over the voice band.

In the control path, when the line goes off-hook, the SLIC pulls its collector $\overline{DET}$ output down and enables the DSLAC IC serial control data I/O pins, D_{IN} and D_{OUT} (see Figure 1). The microprocessor also recognizes the off-hook, and typically will send a response such as an active state or ring relay release command back to the SLIC, via the DSLAC IC D_{IN} pin and the C3–C1 data bus. The C4 line is also addressed in the same manner, to enable or disable the test relay driver. The E1 pin is addressed directly by the microprocessor as shown.

SLIC monitor and control functions which can be performed using a microprocessor and the circuitry shown in Figure 2 include:

- During the disable state, inform the processor when an off-hook has occurred and send a power-up command to the SLIC.
- Detect an off-hook during ringing and send a command to the SLIC to release the ring relay.
- Detect an on-hook condition during the active state and send a command to the SLIC to enter the disable state.
- Send a line polarity reverse command to the SLIC.
- Command the SLIC into the ground-key sense mode.
- Command the SLIC to energize the ring relay, K_R.
- Command the SLIC to energize the test relay, K_T.

For more detailed information on designing with the AMD SLIC Family, please refer to *The Subscriber Line Interface Circuit Family Application Note*, order #07030.

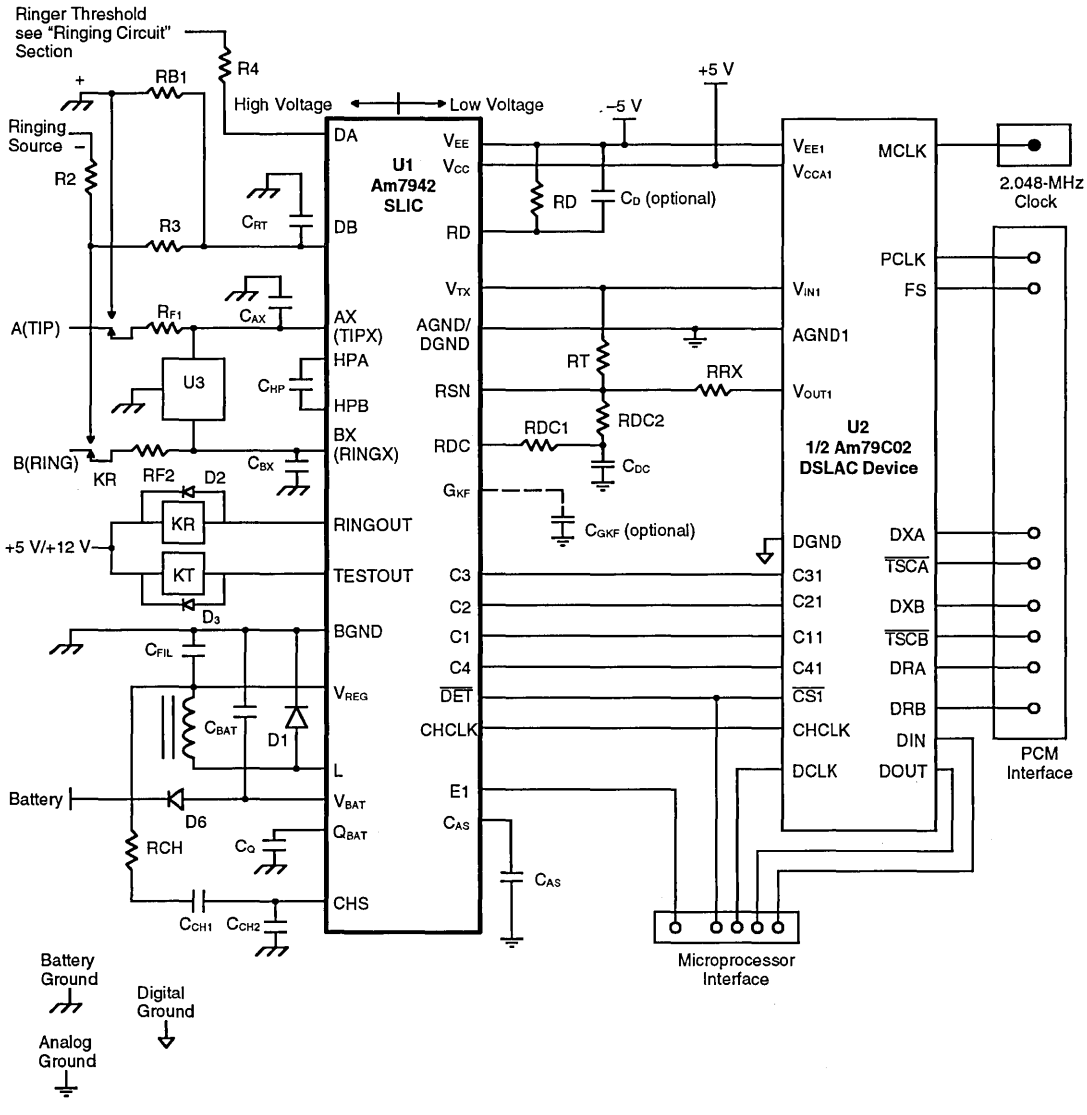
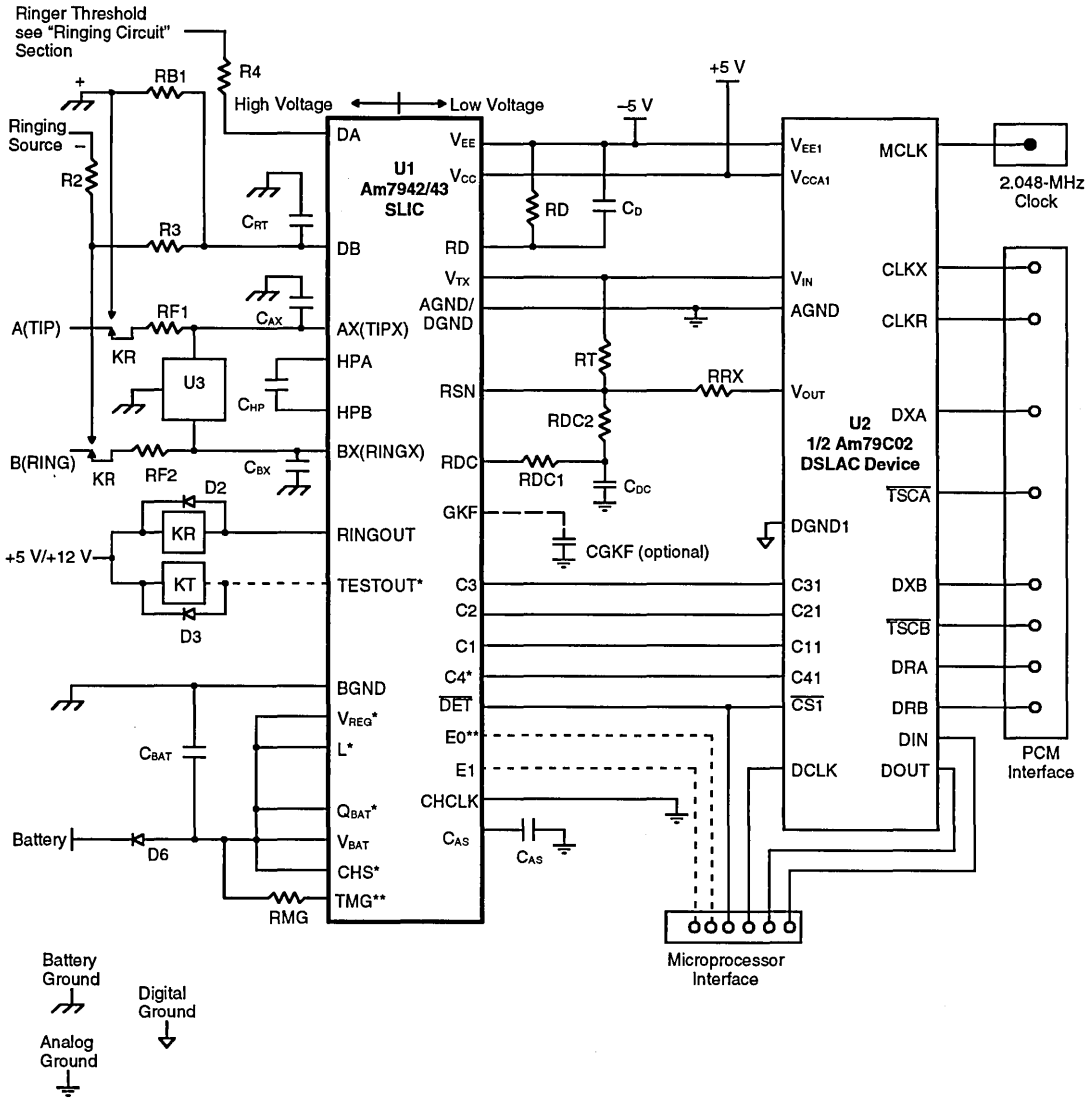


Figure 1. Single Channel of a Dual Channel Subscriber Line Circuit with Switcher Components



*Pin not available on the Am7943.
**Pin not available on the Am7942.

Figure 2. Single Channel of a Dual Channel Subscriber Line Circuit (24-V Battery, Without Switcher Components)

Table 1. Parts List — Single Channel Subscriber Line System

U1	Am7942 or Am7943 SLIC
U2	Am79C02 DSLAC device
K_R, K_T	Relay, 2-C contacts, 1500-V rating
L	Inductor, 1 mH, 5%**
D1	Diode, 100 V, 100 mA, 4 ns**
U3	Dual transient suppressor, Texas Instruments TISP108A or equivalent
D2, D3, D6	Diode 100 V, 100 mA, 10 ns
RF_1, RF_2	Resistor, fuse, 20 ohms to 50 ohms
R2	Resistor, 800 ohms, 3%, 3 W (Ring feed resistor)*
R_{B1}	Resistor, 1 Mohm, 1%, 1/4 W
R3	Resistor, 825K, 1%, 1/4 W
R4	Resistor, 452K, 1%, 1/4 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W**
RD	Resistor, 35.4K, 1%, 1/4 W (sets off-hook threshold)*
RT	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX}	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{DC1}, R_{DC2}	Resistor, 7.14K, 1%, 1/4 W (sets loop current)*
RMG	Resistor 1700 ohms, 5% 2 W (Am7943)
C_{RT1}	Capacitor, 0.1 µF, 20%, 100 V
C_{DC}	Capacitor 0.47 µF, 20%, 10 V
C_{HP}	Capacitor, 0.33 µF, 20%, 100 V
C_{AS}	Capacitor, 0.15 µF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2200 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.47 µF, 10%, 100 V, metalized polyester**
C_{BAT}	Capacitor, 0.47 µF, 20%, 100 V
C_Q	Capacitor, 0.33 µF, 20%, 100 V**
C_{CH1}	Capacitor, 0.015 µF, 10%, 50 V, X7R ceramic**
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic**
C_D	Capacitor, 0.01 µF, 20%, 10 V (sets off-hook filtering)*
C_{GKF}	Capacitor, 3300 pF, 10%, X7R ceramic

Note: *The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.
**The parts marked by a double asterisk (**) are not needed for 24-V battery operation without a switcher.

Central Office SLICs

CENTRAL OFFICE SLIC PRODUCTS

General Description

AMD's Central Office SLIC (Subscriber Line Interface Circuit) products perform the telephone line interface functions required by most types of telephone switching and transmission equipment. The full range of signal transmission, battery feed, and loop supervision functions are supported.

The Am7953X and Am7957X Central Office SLICs are compatible with CCITT recommendations, while North American LSSGR recommendations are accommodated by the new Am7958. A number of SLICs in this family also support the metering function required by many European countries (see Central Office Metering SLICs section). The Central Office SLICs feature an internal, self-adjusting switching regulator to reduce power consumption to a minimum and enhance system reliability. Central Office SLICs also support on-hook transmission and offer extended temperature performance, making either type ideal for Digital Loop Carrier and Multiplexer applications.

The signal transmission functions of all AMD SLICs include both two-to-four-wire and four-to-two-wire conversion. The two-wire termination impedance is programmable with a single external impedance. The companion AMD SLAC or DSLAC IC (Single-Channel or Dual-Channel Subscriber Line Audio-Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the DSLAC IC is not used, most codec/filters provide an uncommitted op amp for this purpose.

The SLIC's battery feed architecture makes their DC feed characteristics programmable with external resistors. Furthermore, these characteristics are independent of battery variations. AMD's Central Office SLICs are optimized for either 48- or 63-V operation.

A polarity reversal function is provided on all SLICs and transposes the normal voltage sense of the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode is also provided, limiting loop current and cutting power dissipation while allowing the full complement of supervisory functions to be utilized.

The supervisory functions of off-hook detection and ring trip detection are read through a single, TTL-compatible output. To eliminate noise-induced errors, the off-hook detector signal may be filtered. Off-hook detection has a threshold that is set by the value of an external resistor. Additional supervisory controls put the A lead into an open circuit or high-impedance state suitable for application in ground start systems. Similarly, both the A and B leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Two relay drivers support ring and test relay functions, or can be used for other functions.

The SLIC's user-programmable states are controlled by a TTL-compatible code. The control inputs are designed to easily interface to popular single-chip microcontrollers, such as the industry standard 8051, or to latched outputs from a SLAC or DSLAC device.

PRELIMINARY

Am79530/Am79531/ Am79534/Am79535

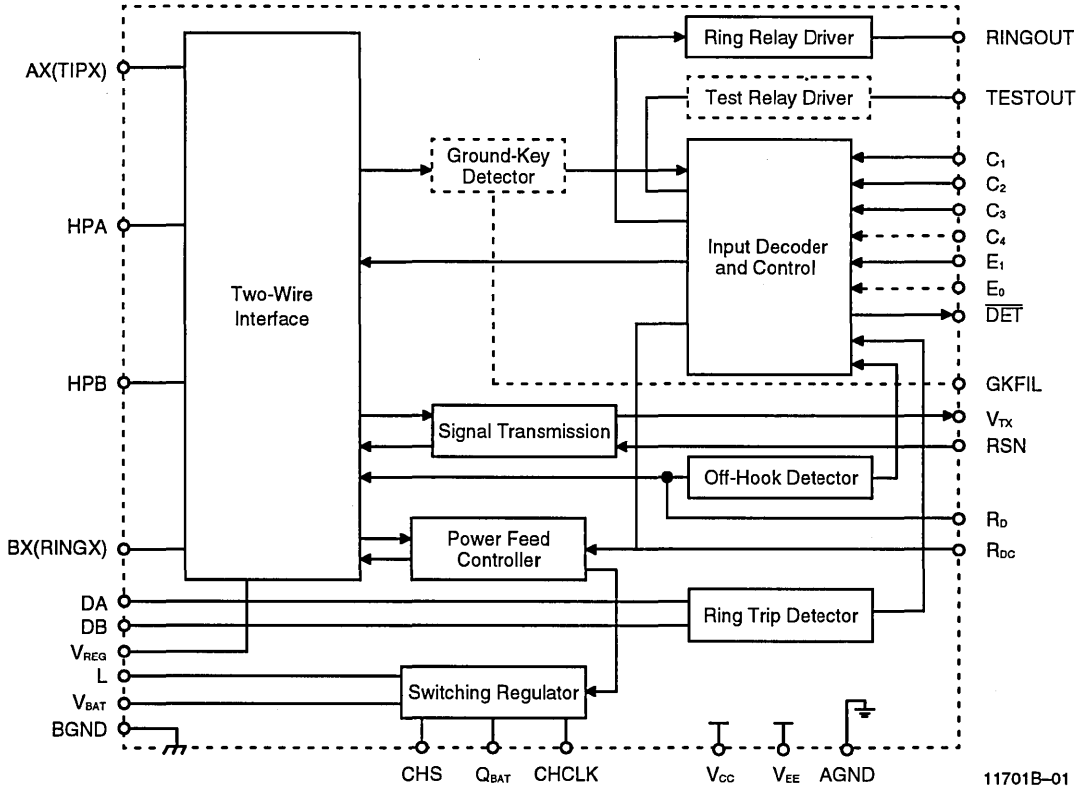
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Line-feed characteristics independent of battery variations
- Programmable loop detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise filter capacitor available
- Ground-key detect
- Low standby power
- Two-wire impedance set by single external impedance
- Polarity reversal feature
- Tip open state for ground start lines
- Test relay driver optional

BLOCK DIAGRAM

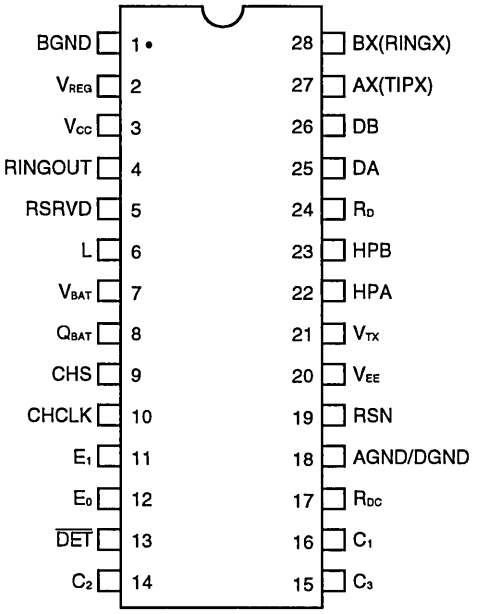


Notes: Am79530—E_0 and E_1 inputs; ring relay sourced internally to BGND; no test relay driver.
Am79531—E_0 and E_1 inputs; ring relay sourced internally to BGND; no test relay driver; ground-key filter pin.
Am79534—E_0 and E_1 inputs; ring and test relay drivers sourced internally to BGND.
Am79535—E_0 and E_1 inputs; ring relay driver sourced internally to BGND; ground-key filter pin.
Current gain (K_1) = 1000 for all parts.

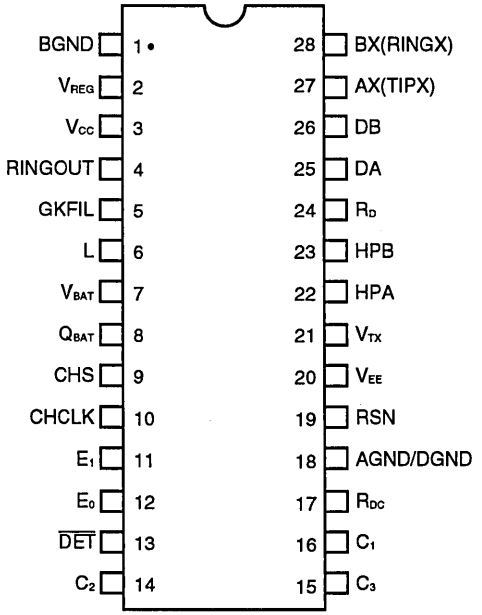
Publication #: 16854 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View

Am79530



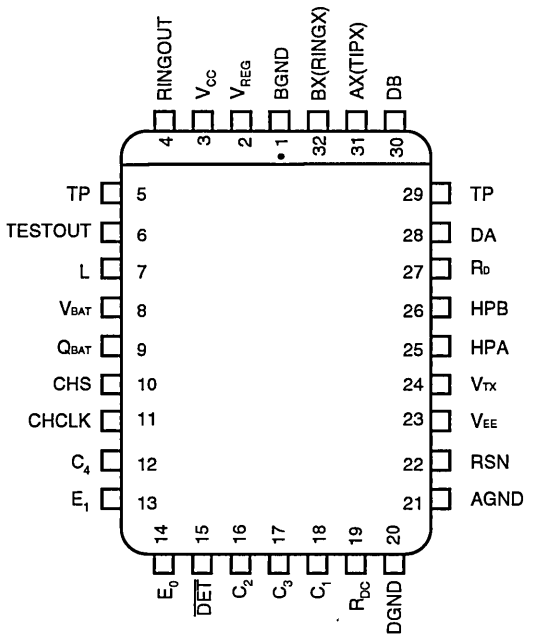
Am79531



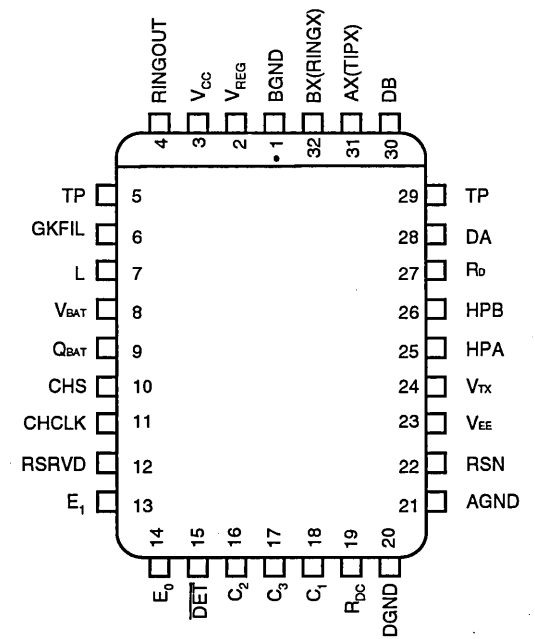
Note: Pin 1 is marked for orientation.

CONNECTION DIAGRAMS (continued)

Am79534



Am79535

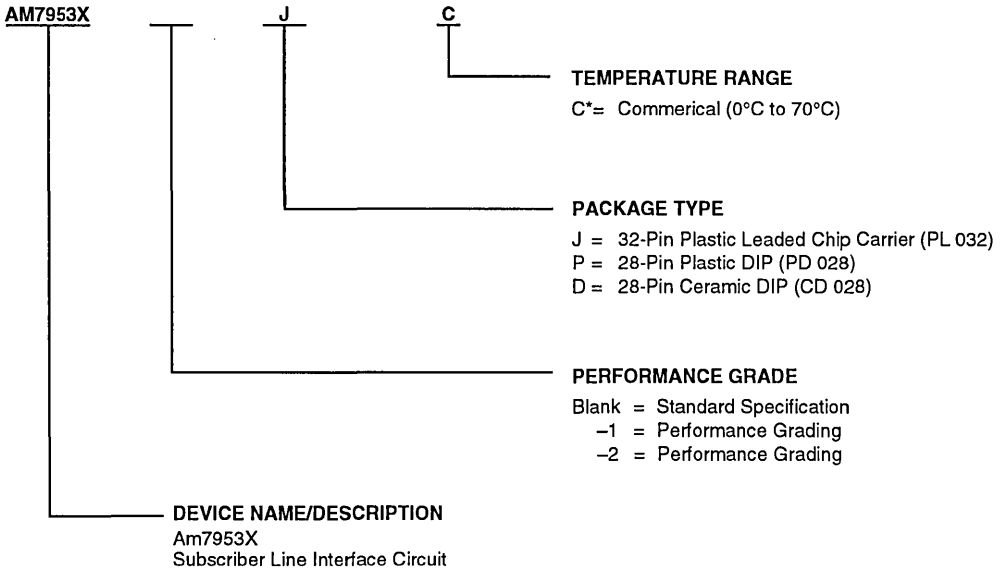


Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7953X	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND

Ground (Am79534 and Am79535)

Analog (Quiet) ground.

DGND

Ground (Am79534 and Am79535)

Digital ground.

AGND/DGND

Ground (Am79530, Am79531)

Analog and digital ground are connected internally to a single pin.

AX(TIPX)

(Output)

Output of A(TIP) power amplifier.

BGND

Ground

Battery (power) ground.

BX(RINGX)

(Output)

Output of B(RING) power amplifier.

C_3–C_1

Decoder (Inputs)

TTL compatible. C_3 is MSB and C_1 is LSB.

C_4

Test Relay Driver Command (Input) (Am79534)

TTL compatible. A logic Low enables the driver.

CHCLK

Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (Nominal).

CHS

Chopper Stabilization (Input)

Connection for external stabilization components.

DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$

Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C_3–C_1, E_0, E_1). The output is open-collector with a built-in 15K pull-up resistor.

E_0

Read Enable (Input)
(Am79530, Am79531, and Am79534)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E_1

Ground Key Enable (Input)

When E_0 is High, E_1 = High connects the ground-key detector to $\overline{DET}$, and E_1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

GKFIL

Ground-Key Filter Capacitor Connection
(Am79531 and Am79535)

An external capacitor for filtering out high-frequency noise from the ground-key loop can be connected to this pin. An internal 36K –20%, +40% resistor is provided to form an RC filter with the external capacitor.

In versions which have a GKFIL pin, 3.3 nF minimum capacitance must be connected from the GKFIL pin to ground.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L

Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}

Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT

Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

TESTOUT

Test Relay Driver (Output) (Am79534)

Sourcing from BGND with internal diode to Q_{BAT}.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

V_{BAT}

Connected to office battery supply through an external protection diode.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers and connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –40 V to –63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS over operating range

Am79530/Am79531/Am79534/Am79535 (see Note 1)

Description	Test Conditions	Preliminary P.G.*	Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance (Note 5)				3		ohm
Analog (V_{TX}) Output Offset			−35		+35	mV
		−1	−30		+30	
Analog (RSN) Input Impedance (Note 5)	300 Hz to 3.4 kHz			1	20	ohm
Longitudinal Impedance at AX or BX					35	
Overload Level	four-wire		−3.1		+3.1	Vpk
Z_{2WIN} = 600 to 900 ohms (Note 2)	two-wire					
Transmission Performance, two-wire impedance						
Two-Wire Return Loss	300 Hz to 500 Hz		26			dB
(See Test Circuit D)	500 Hz to 2500 Hz		26			
(Notes 5, 10)	2500 Hz to 3400 Hz		20			
Longitudinal Balance (two-wire and four-wire, see Test Circuit C)						
R_L = 600 ohms	300 Hz to 3400 Hz		48			dB
Longitudinal to Metallic L-T, L-4		−1	52			
Longitudinal to Metallic L-T and	200 Hz to 1000 Hz	−2**	63	70		
L-4 for trimmed version (consult factory)	1000 Hz to 3400 Hz		58	70		
	200 Hz to 3400 Hz (Reverse polarity)		54			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		40			dB
	300 Hz to 800 Hz	−1	42			
Longitudinal Current Capability	Active State			25		mA
per Wire (Note 5)	Disable State			18		RMS
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)						
Gain Accuracy	0 dBm, 1 kHz		−0.15		+0.15	dB
		−1	−0.1		+0.1	
Variation with Frequency (Note 5)	300 Hz to 3400 Hz Relative to 1 kHz		−0.1		+0.1	dB
Gain Tracking (Note 5)	+7 dBm to −55 dBm Reference: 0 dBm		−0.1		+0.1	dB
Balance Return Signal (four-wire to four-wire, see Test Circuit B)						
Gain Accuracy (Note 3)	0 dBm, 1 kHz		−0.15		+0.15	dB
		−1	−0.1		+0.1	
Variation with Frequency (Notes 3, 5)	300 Hz to 3400 Hz Relative to 1 kHz		−0.1		+0.1	dB
Gain Tracking (Note 5)	+3 dBm to −55 dBm Reference: 0 dBm		−0.1		+0.1	dB
Group Delay (Notes 5, 12)	F = 1 kHz			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)						
Total Harmonic Distortion	0 dBm, 300 Hz–3.4 kHz			−64	−50	dB
	+9 dBm, 300 Hz–3.4 kHz			−55	−40	

*P.G. = Performance Grade
**All other performance parameters equivalent to −1 grade.
Normal Polarity only.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Idle Channel Noise						
C-Message Weighted Noise (Notes 5, 7)	two-wire			+7	+15	dBrnC
		–1		+7	+12	
	four-wire			+7	+15	dBrnC
		–1		+7	+12	
Psophometric Weighted Noise (Note 7)	two-wire			–83	–75	dBmp
		–1		–83	–78	
	four-wire			–83	–75	dBmp
		–1		–83	–78	
Single Frequency Out-of-Band Noise (see Test Circuit E)						
Metallic	4 kHz to 9 kHz			–76		dBm
(Notes 4, 5, 9)	9 kHz to 1 MHz			–76		
(Notes 4, 5)	256 kHz and harmonics			–57		
Longitudinal	1 kHz to 15 kHz			–70		dBm
(Notes 4, 5, 9)	Above 15 kHz			–85		
(Notes 4, 5)	256 kHz and harmonics			–57		
DC Feed Currents (see Figures 1a, 1b, 1c) Battery = –48 V						
Active Mode Loop Current Accuracy	I_{LOOP} (nominal) = 40 mA		–7.5		+7.5	%
Disable Mode	R_L = 600 ohms		18	20	22	mA
Tip Open Mode	R_L = 600 ohms				1.0	
Open Circuit Mode	R_L = 0 ohms				1.0	
Fault Current Limit, I_{LLIM} (I_{AX} + I_{BX})	AX and BX shorted to ground				130	mA
Power Dissipation Battery = –48 V, Normal Polarity						
On-Hook Open Circuit				35	120	mW
		–1		35	80	
On-Hook Disable Mode				135	250	
		–1		135	200	
On-Hook Active Mode				200	400	
		–1		200	300	
Off-Hook Disable Mode	R_L = 600 ohms			500	750	
Off-Hook Active Mode	R_L = 600 ohms			650	1000	
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3.0	4.5	mA
	Disable Mode			6.0	10.0	
	Active Mode			7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.2	3.5	
	Active Mode			2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.0	5.0	
	Active Mode			4.0	6.0	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Vripple = 50 mV RMS)						
V_{CC} (Notes 6, 7)	50 Hz to 3400 Hz		25	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		22	35		dB
		–1	25	35		
V_{EE} (Notes 6, 7)	50 Hz to 3400 Hz		20	40		dB
		–1	25	40		
	3.4 kHz to 50 kHz		10	25		dB
		–1	10	25		
V_{BAT} (Notes 6, 7)	50 Hz to 3400 Hz		27	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		20	40		dB
		–1	25	40		
Off-Hook Detector						
Current Threshold Accuracy	I_{DET} = 365/R_D Nominal		–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V (see Test Circuit F)						
Ground-Key Resistance Threshold	B(Ring) to GND		2.0	5.0	10.0	Kohm
Ground-Key Current Threshold (Note 8)	B(Ring) to GND			9		mA
	Midpoint to GND			9		
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage (Note 11)	Source Resistance 0 to 2 Mohm		–50	0	+50	mV
Logic Inputs (C_1, C_2, C_3, C_4, E_0, E_1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4			mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

SWITCHING CHARACTERISTICS
Am79530/Am79531/Am79534/Am79535

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E_1 High to $\overline{DET}$ High (E_0 = 1)	Ground-Key Detect Mode R_L Open, R_G Connected (see Test Circuit H)			3.8	µs
	E_1 High to $\overline{DET}$ Low (E_0 = 1)				1.1	
tshde	E_1 Low to $\overline{DET}$ Low (E_0 = 1)				1.2	µs
	E_1 Low to $\overline{DET}$ High (E_0 = 1)				3.8	
tshdd	E_0 High to $\overline{DET}$ Low (E_1 = 0)	Switch Hook Detect Mode R_L = 600 ohms, R_G Open (see Test Circuit G)			1.1	µs
tshd0	E_0 Low to $\overline{DET}$ High (E_1 = 0)				3.8	
tgkdd	E_0 High to $\overline{DET}$ Low (E_1 = 1)				1.1	µs
tgkd0	E_0 Low to $\overline{DET}$ High (E_1 = 1)				3.8	

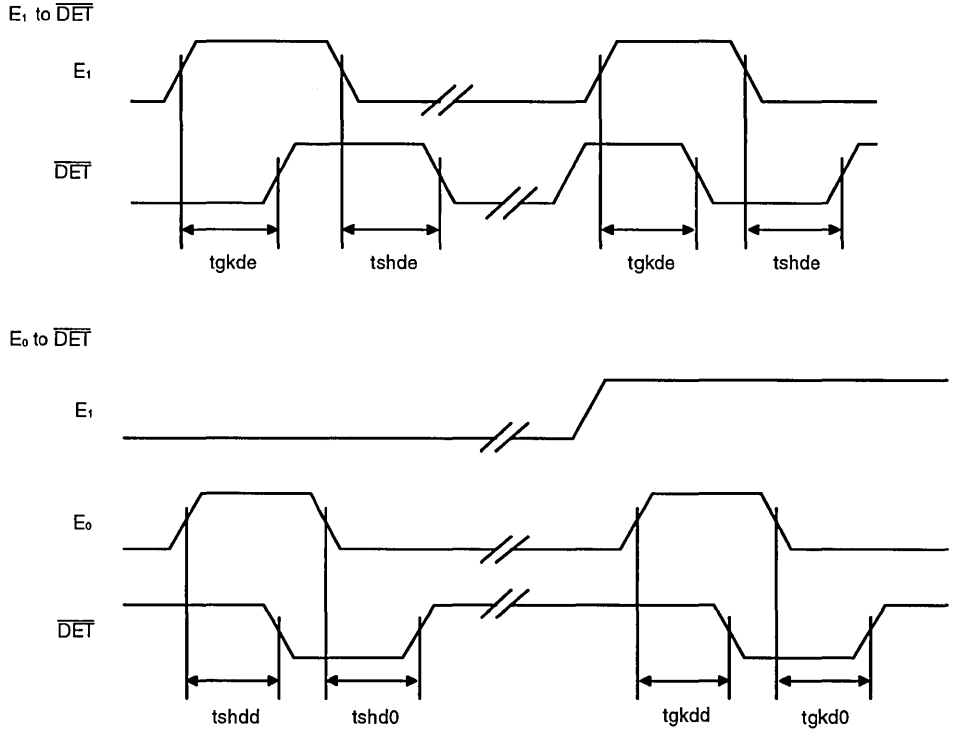
Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	E_0 = 1* E_1 = 0	E_0 = 1* E_1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

For the Am79530, Am79531, Am79534, and Am79535, a logic Low on E_0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING WAVEFORMS

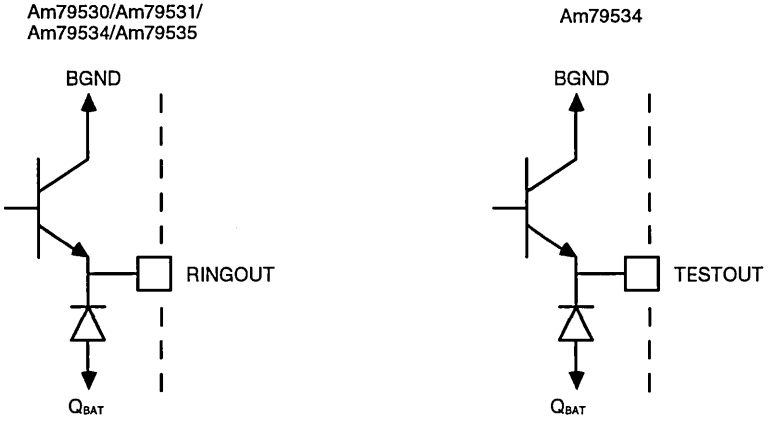
Am79530/Am79531/Am79534/Am79535



11701B–002

Note: All delays measured at 1.4-V level.

Relay Driver Specifications



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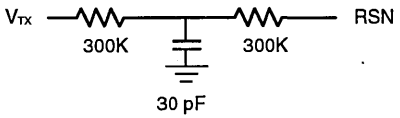
Description	Test Conditions	Min	Typ	Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)					
On Voltage	50 mA Source	BGND –2	BGND – 0.95		V
Off Leakage			0.5	100	µA
Clamp Voltage	50 mA Sink	Q_{BAT} –2			V

Notes:

1. Unless otherwise noted, test conditions are: Battery = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.22 µF, $R_{DC1} = R_{DC2}$ = 31.25K, C_{DC} = 0.1 µF, R_d = 51.1K, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600K resistive, receive input summing impedance (Z_{RX}) = 300K resistive. (See Table 2 for component formulas.)
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 11 V.
8. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from 256-kHz switch-regulator chopper are not included.
10. Assumes the following Z_T network:

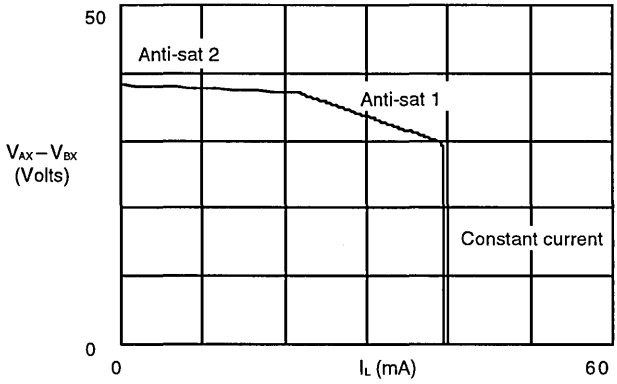


11. Tested with 0 ohm source impedance. Two Mohms is specified for system design purposes only.
12. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins.The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{1000\,Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 2500/I_{FEED}$ $C_{DC} = (1.5\text{ ms})(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\text{ ms}/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.

$V_{BAT} = -47.3$ V
$R_{DC1} + R_{DC2} = R_{DC} = 62.5$K



Constant current region: $I_L = \frac{2500}{R_{DC}}$

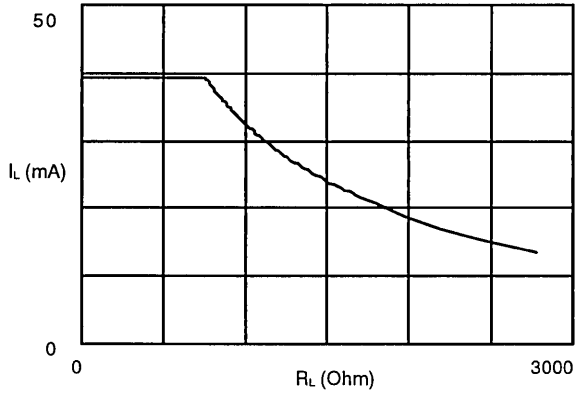
Anti-sat 1 region: $V_{AX-BX} = 45.78 - \frac{R_{DC}}{152.6} I_L$

Anti-sat 2 region: $V_{AX-BX} = 1.067 | V_{BAT} | - 12.22 - \left(0.0128 + \frac{R_{DC}}{1523}\right) I_L$

See Figure 1c.

11701B–004

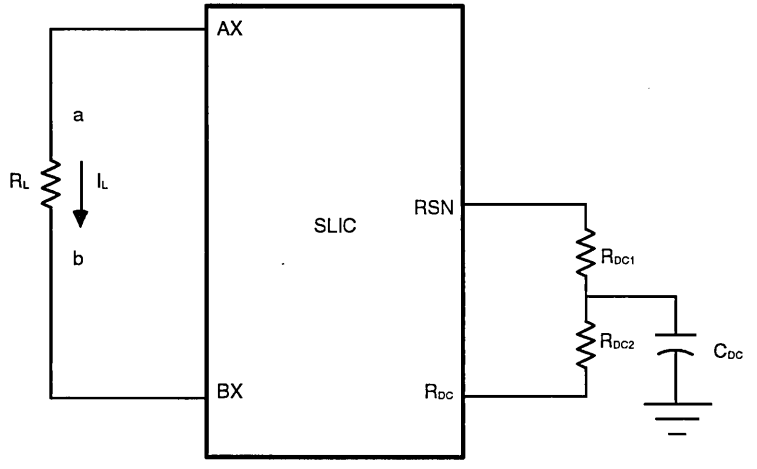
Figure 1a. Load Line (Typical)



Load Current versus Load Resistance—Am79530/Am79531/Am79534/Am79535
V_{BAT} = –47.3 V
R_{DC} = 62.5K
See Figure 1c.

11701B–005

Figure 1b. Feed Characteristics (Typical)

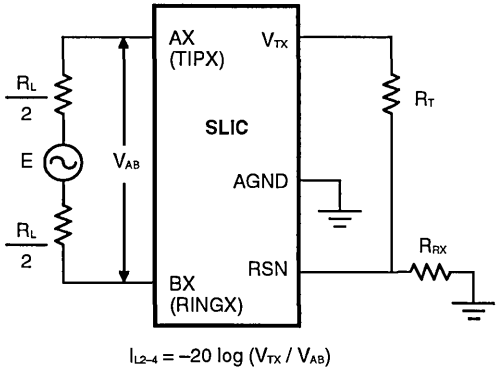


Current programmed by R_{DC1} and R_{DC2}.

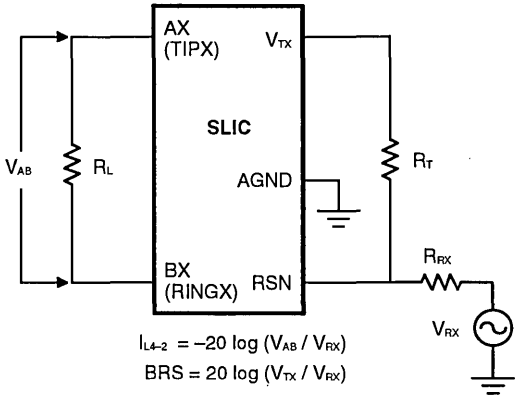
11701B–006

Figure 1c. Feed Programming

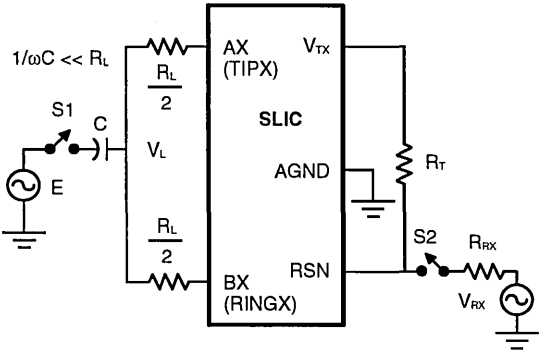
TEST CIRCUITS



A. Two-to-Four Wire Insertion Loss



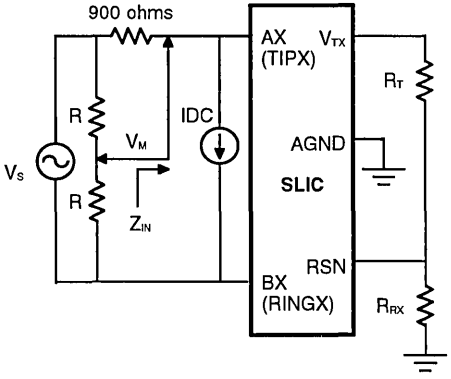
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 log (V_{AB} / E)
L-4 Long. Rej. = 20 log (V_{TX} / E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance



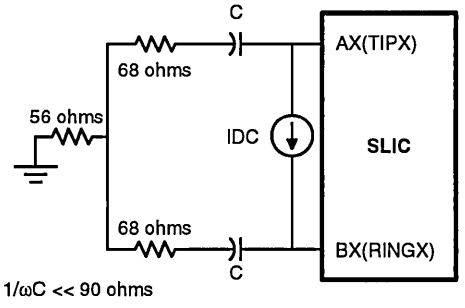
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = –20 log (2 V_M / V_S)

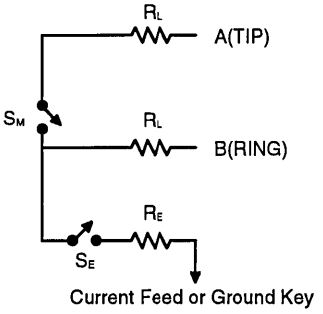
D. Two-Wire Return Loss Test Circuit

15772A–017a

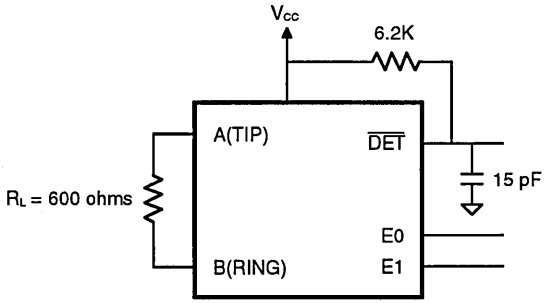
TEST CIRCUITS (continued)



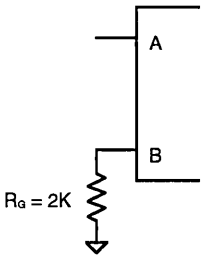
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching

15772A-017b

PRELIMINARY

Am79571/Am79573/Am79574

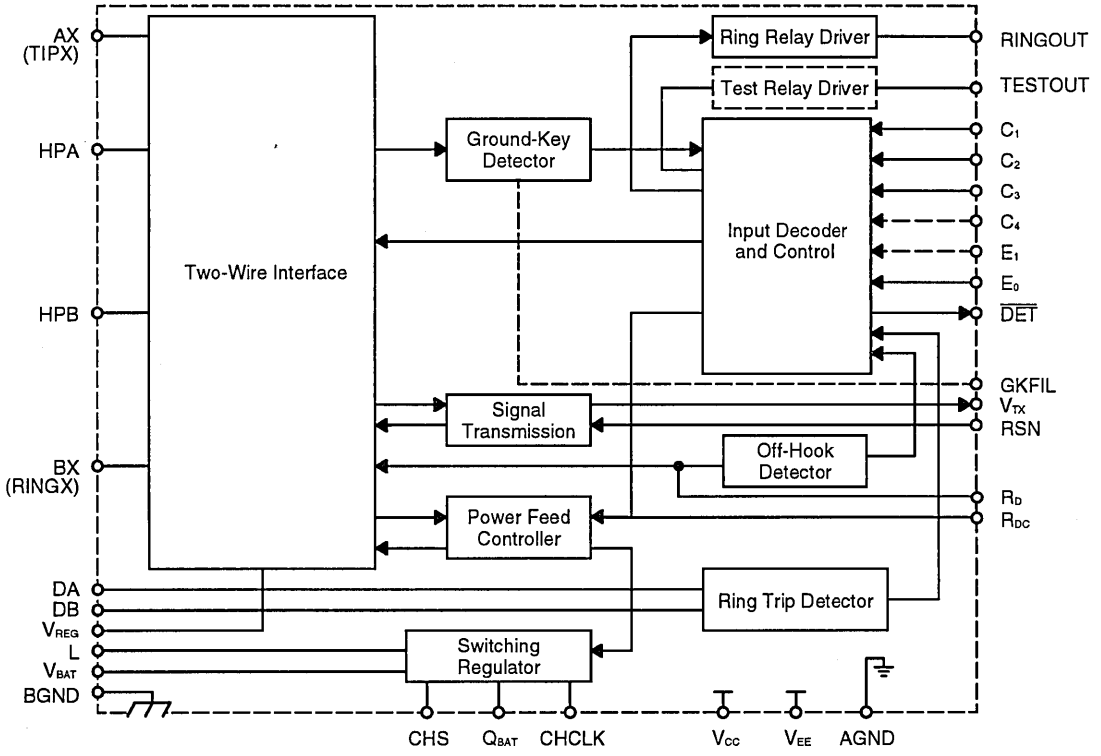
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant resistance feed
- Line-feed characteristics independent of battery variations
- Programmable loop detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise filter capacitor available
- Ground-key detect option available
- Low standby power
- Two-wire impedance set by single external impedance
- Polarity reversal feature
- Tip open state for ground start lines
- Test relay driver optional

BLOCK DIAGRAM



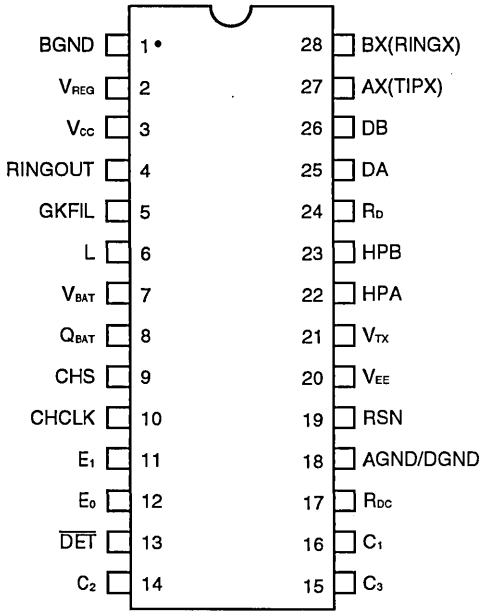
11701B–007

Notes: Am79571—E_0 and E_1 inputs; ring relay sourced internally to BGND; no test relay driver; ground-key filter pin.
Am79573—E_0 input and no E_1 input; ring and test relay drivers sourced internally to BGND.
Am79574—E_0 and E_1 inputs; ring and test relay drivers sourced internally to BGND.
Output amplifier current gain (K_1) = 1000 for all three parts.

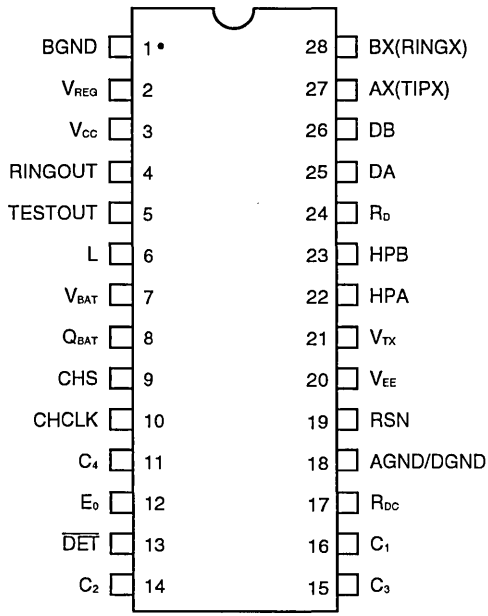
Publication #: 16855 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View

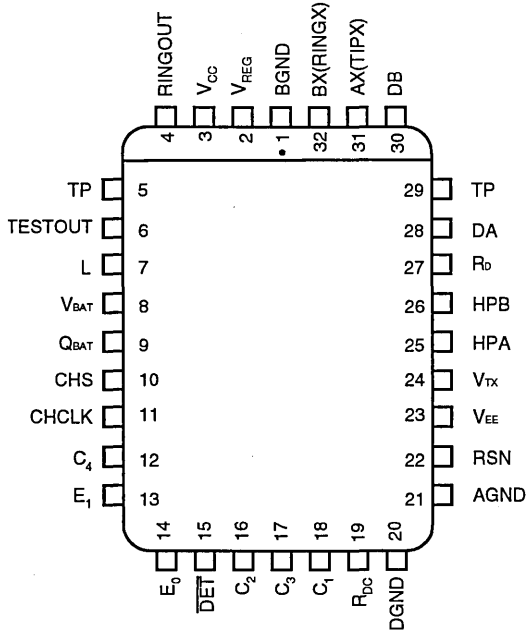
Am79571



Am79573



Am79574



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

PIN DESCRIPTION

AGND

Ground (Am79574)

Analog (Quiet) ground.

DGND

Ground (Am79574)

Digital ground.

AGND/DGND

Ground (Am79571 and Am79573)

Analog and digital ground are connected internally to a single pin.

AX(TIPX)

(Output)

Output of A(TIP) power amplifier.

BGND

Ground

Battery (power) ground.

BX(RINGX)

(Output)

Output of B(RING) power amplifier.

C_3–C_1

Decoder (Inputs)

TTL compatible. C_3 is MSB and C_1 is LSB.

C_4

Test Relay Driver Command (Input)
(Am79573 and Am79574)

TTL compatible. A logic Low enables the driver.

CHCLK

Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (Nominal).

CHS

Chopper Stabilization (Input)

Connection for external stabilization components.

DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$

Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C_3–C_1, E_0, E_1). The output is open-collector with a built-in 15K pull-up resistor.

E_0

Read Enable (Input)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E_1

Ground-Key Enable (Input)
(Am79571 and Am79574)

When E_0 is High, E_1 = High connects the ground-key detector to $\overline{DET}$, and E_1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

GKFIL

Ground-Key Filter Capacitor Connection
(Am79571)

An external filter capacitor for filtering out high frequency noise from the ground-key loop can be connected to this pin. An internal 36K –20%, +40% resistor is provided to form an RC filter with the external capacitor.

In versions which have a GKFIL pin, 3.3-nF minimum capacitance must be connected from the GKFIL pin to ground.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L

Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}

Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC-feed resistance programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT

Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

TESTOUT

Test Relay Driver (Output)
(Am79573 and Am79574)

Sourcing from BGND with internal diode to Q_{BAT}.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

V_{BAT}

Connected to office battery supply through an external protection diode.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

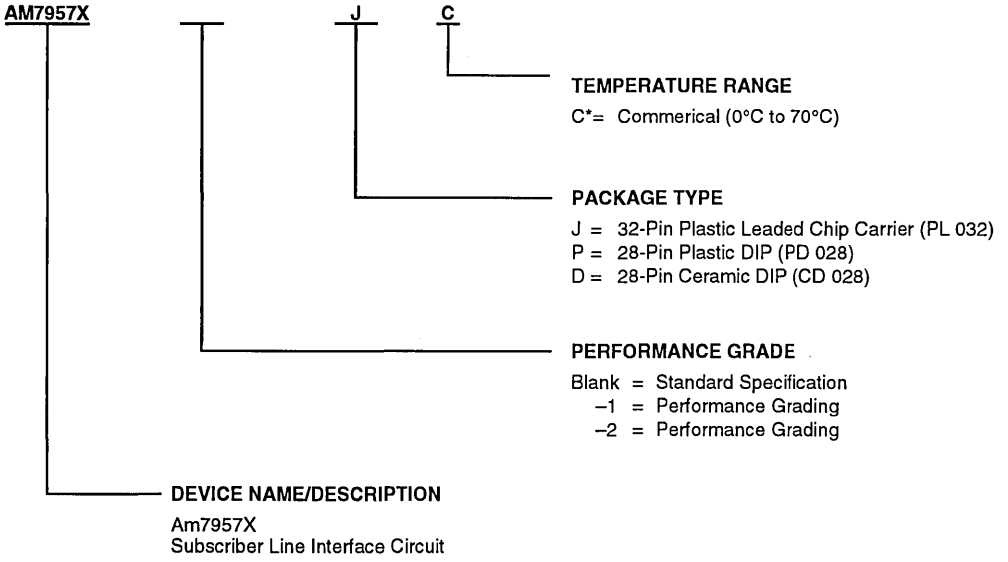
Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7957X	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –40 V to –63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS over operating range
Am79571/Am79573/Am79574 (see Note 1)

Description	Test Conditions	Preliminary P.G.*	Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance (Note 5)				3		ohm
Analog (V_{TX}) Output Offset			−35		+35	mV
		−1	−30		+30	
Analog (RSN) Input Impedance (Note 5)	300 Hz to 3.4 kHz			1	20	ohm
Longitudinal Impedance at AX or BX (Note 5)					35	
Overload Level	four-wire		−3.1		+3.1	Vpk
Z_{2WIN} = 600 to 900 ohms (Note 2)	two-wire					
Transmission Performance, two-wire impedance						
Two-Wire Return Loss	300 Hz to 500 Hz		26			dB
(See Test Circuit D)	500 Hz to 2500 Hz		26			
(Notes 5, 11)	2500 Hz to 3400 Hz		20			
Longitudinal Balance (two-wire and four-wire, see Test Circuit C)						
R_L = 600 ohms	300 Hz to 3400 Hz		48			dB
Longitudinal to Metallic L-T, L-4		−1	52			
Longitudinal to Metallic L-T and	200 Hz to 1000 Hz	−2**	63	70		
L-4 for trimmed version (consult factory)	1000 Hz to 3400 Hz		58	70		
	200 Hz to 3400 Hz (Reverse Polarity)		54			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		40			dB
	300 Hz to 800 Hz	−1	42			
Longitudinal Current Capability	Active State			25		mA
per Wire (Note 5)	Disable State			18		RMS
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)						
Gain Accuracy	0 dBm, 1 kHz		−0.15		+0.15	dB
		−1	−0.1		+0.1	
Variation with Frequency (Note 5)	300 Hz to 3400 Hz Relative to 1 kHz		−0.1		+0.1	dB
Gain Tracking (Note 5)	+7 dBm to −55 dBm Reference: 0 dBm		−0.1		+0.1	dB
Balance Return Signal (four-wire to four-wire, see Test Circuit B)						
Gain Accuracy (Note 3)	0 dBm, 1 kHz		−0.15		+0.15	dB
		−1	−0.1		+0.1	
Variation with Frequency (Notes 3, 5)	300 Hz to 3400 Hz Relative to 1 kHz		−0.1		+0.1	dB
Gain Tracking (Note 5)	+3 dBm to −55 dBm Reference: 0 dBm		−0.1		+0.1	dB
Group Delay (Notes 5, 13)	F = 1 kHz			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)						
Total Harmonic Distortion	0 dBm, 300 Hz–3.4 kHz			−64	−50	dB
	+9 dBm, 300 Hz–3.4 kHz			−55	−40	

*P.G. = Performance Grade
**All other performance parameters equivalent to −1 grade.
Normal Polarity only.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Idle Channel Noise						
C-Message Weighted Noise (Notes 5, 7)	two-wire			+7	+15	dBrnC
		–1		+7	+12	
	four-wire			+7	+15	dBrnC
		–1		+7	+12	
Psophometric Weighted Noise (Note 7)	two-wire			–83	–75	dBmp
		–1		–83	–78	
	four-wire			–83	–75	dBmp
		–1		–83	–78	
Single Frequency Out-of-Band Noise (see Test Circuit E)						
Metallic	4 kHz to 9 kHz			–76		dBm
(Notes 4, 5, 9)	9 kHz to 1 MHz			–76		
(Notes 4, 5)	256 kHz and harmonics			–57		
Longitudinal	1 kHz to 15 kHz			–70		dBm
(Notes 4, 5, 9)	Above 15 kHz			–85		
(Notes 4, 5)	256 kHz and harmonics			–57		
Line Characteristics (see Figures 1a, 1b, 1c) Battery = –48 V, R_L = 600 and 900 ohms, R_{FEED} = 800 ohms						
Apparent Battery Voltage	Active Mode		47	50	53	V
Loop Current Accuracy	Active Mode		–7.5		+7.5	%
Loop Current—Tip Open	R_L = 600 ohms				1.0	mA
Loop Current—Open Circuit	R_L = 0 ohms				1.0	
Loop Current Limit Accuracy (Note 10)	Disable Mode Active Mode		–20		+20	%
Fault Current Limit, I_{LLIM} (I_{AX} + I_{BX})	AX and BX shorted to ground				130	mA
Power Dissipation Battery = –48 V, Normal Polarity						
On-Hook Open Circuit				35	120	mW
		–1		35	80	
On-Hook Disable Mode				135	250	
		–1		135	200	
On-Hook Active Mode				200	400	
		–1		200	300	
Off-Hook Disable Mode	R_L = 600 ohms			500	750	
Off-Hook Active Mode	R_L = 600 ohms			650	1000	
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3.0	4.5	mA
	Disable Mode			6.0	10.0	
	Active Mode			8.0	13.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.3	3.7	
	Active Mode			3.0	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.2	5.5	
	Active Mode			4.5	7.0	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Vripple = 50 mV RMS)						
V_{CC} (Notes 6, 7)	50 Hz to 3400 Hz		25	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		22	35		dB
		–1	25	40		
V_{EE} (Notes 6, 7)	50 Hz to 3400 Hz		20	40		dB
		–1	25	40		
	3.4 kHz to 50 kHz		10	25		dB
		–1	10	25		
V_{BAT} (Notes 6, 7)	50 Hz to 3400 Hz		27	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		20	40		dB
		–1	25	40		
Off-Hook Detector						
Current Threshold Accuracy	I_{DET} = 365/R_D Nominal		–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V (see Test Circuit F)						
Ground-Key Resistance Threshold	B(Ring) to GND		2.0	5.0	10.0	Kohm
Ground-Key Current Threshold (Note 8)	B(Ring) to GND			9		mA
	Midpoint to GND			9		
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage (Note 12)	Source Resistance 0 to 2 Mohm		–50	0	+50	mV
Logic Inputs (C_1, C_2, C_3, C_4, E_0, E_1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4			mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

SWITCHING CHARACTERISTICS
Am79571/Am79573/Am79574

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde*	E_1 High to $\overline{DET}$ High (E_0 = 1)	Ground-Key Detect Mode R_L Open, R_G Connected (see Test Circuit H)			3.8	µs
	E_1 High to $\overline{DET}$ Low (E_0 = 1)				1.1	
tshde*	E_1 Low to $\overline{DET}$ Low (E_0 = 1)				1.2	µs
	E_1 Low to $\overline{DET}$ High (E_0 = 1)				3.8	
tshdd	E_0 High to $\overline{DET}$ Low (E_1 = 0)	Switch Hook Detect Mode R_L = 600 ohms, R_G Open (see Test Circuit G)			1.1	µs
tshd0	E_0 Low to $\overline{DET}$ High (E_1 = 0)				3.8	
tgkdd*	E_0 High to $\overline{DET}$ Low (E_1 = 1)				1.1	µs
tgkd0*	E_0 Low to $\overline{DET}$ High (E_1 = 1)				3.8	

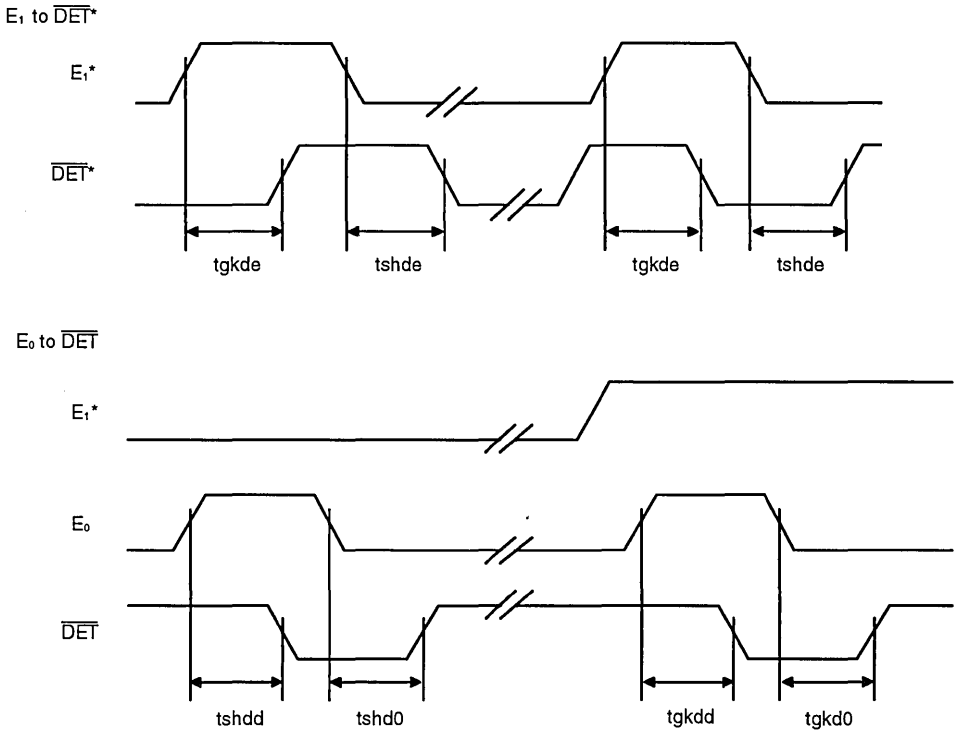
* This parameter is not applicable to the Am79573. E_1 is internally connected to a logical 0.

Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	E_0 = 1* E_1 = 0**	E_0 = 1* E_1 = 1**
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

*A logic Low on E_0 disables the $\overline{DET}$ output into the open-collector state.
**For the Am79573, E_1 is internally connected to a logical 0.

SWITCHING WAVEFORMS
Am79571/Am79573/Am79574

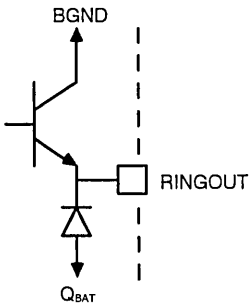


*This waveform is not applicable to the Am79573. E_1 is internally connected to a logical 0.
Note: All delays measured at 1.4-V level.

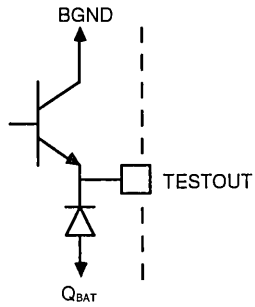
11701B–008

Relay Driver Specifications

Am79571/Am79573/Am79574



Am79573/Am79574



11701A-18

Description	Test Conditions	Min	Typ	Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)					
On Voltage	50 mA Source	BGND –2	BGND –0.95		V
Off Leakage			0.5	100	µA
Clamp Voltage	50 mA Sink	Q_{BAT} –2			V

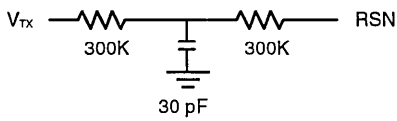
Notes:

1. Unless otherwise noted, test conditions are: Battery = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.22 µF, R_{DC1} = R_{DC2} = 20K, C_{DC} = 0.1 µF, R_d = 51.1K, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600K resistive, receive input summing impedance (Z_{RX}) = 300K resistive. (See Table 2 for component formulas.)
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 14 V.
8. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from 256-kHz switch-regulator chopper are not included.
10. Loop-current limit is calculated using the following equations:

$$\text{In Disable Mode: } I_{LIMIT} = 0.5\,\frac{V_{apparent}}{R_{FEED}}$$

$$\text{In Active Mode: } I_{LIMIT} = 0.8\,\frac{V_{apparent}}{R_{FEED}}$$

11. Assumes the following Z_T network:

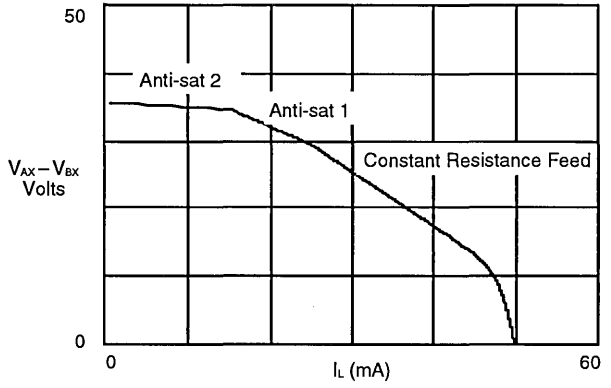


12. Tested with 0 ohms source impedance. Two Mohms is specified for system design purposes only.
13. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 11 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{1000\ Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 50(R_{FEED} - 2R_F)$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.

$V_{BAT} = -47.3$ V
$R_{DC1} + R_{DC2} = R_{DC} = 40K$



Constant resistance region: $V_{AX-BX} = 50 - \frac{R_{DC}}{50} I_L$

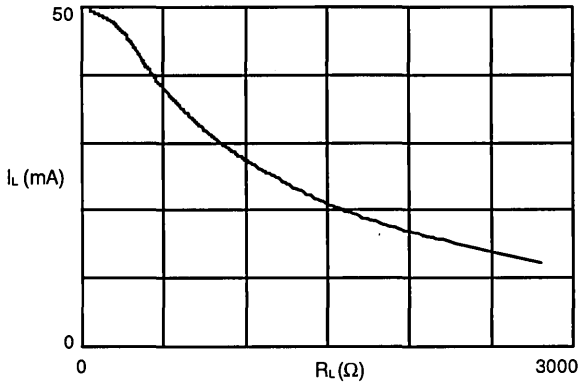
Anti-sat 1 region: $V_{AX-BX} = 42.72 - \frac{R_{DC}}{76.66} I_L$

Anti-sat 2 region: $V_{AX-BX} = |V_{BAT}| - 11.86 - \left(.01 + \frac{R_{DC}}{836}\right) I_L$

See Figure 1c.

11701B–009

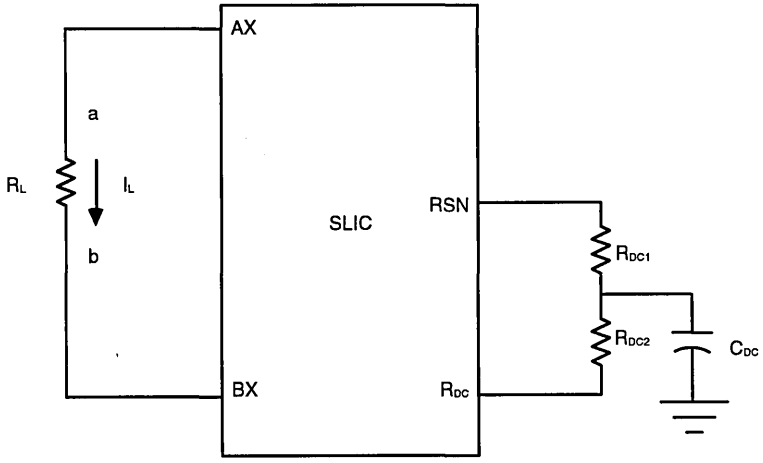
Figure 1a. Load Line (Typical)



Load Current versus Load Resistance—Am79571/Am79573/Am79574
V_{BAT} = –47.3 V
R_{DC} = 40K
See Figure 1c.

11701B–010

Figure 1b. Feed Characteristics (Typical)

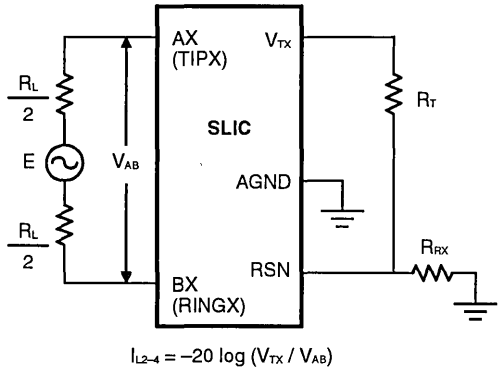


Feed resistance programmed by R_{DC1} and R_{DC2}.

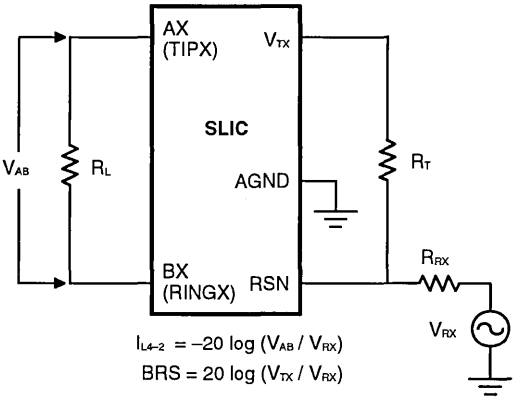
11701B–011

Figure 1c. Feed Programming

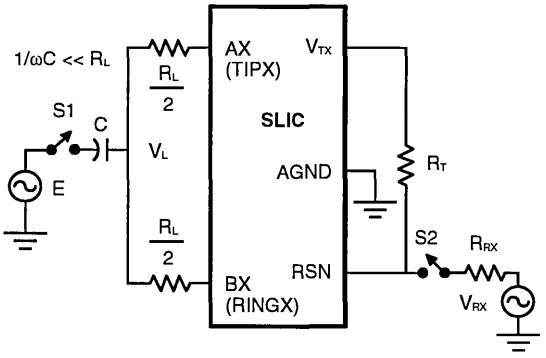
TEST CIRCUITS



A. Two-to-Four Wire Insertion Loss



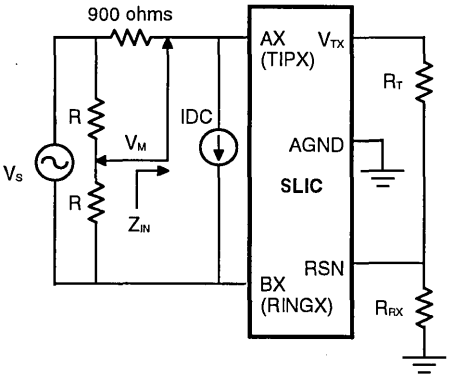
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 log (V_{AB}/E)
L-4 Long. Rej. = 20 log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 log (V_L/V_{RX})

C. Longitudinal Balance



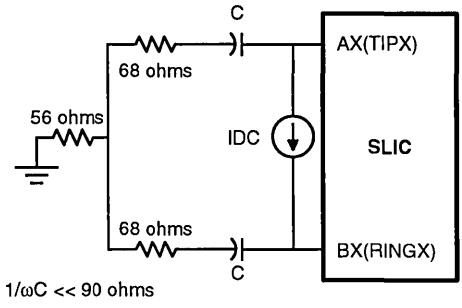
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = –20 log (2 V_M/V_S)

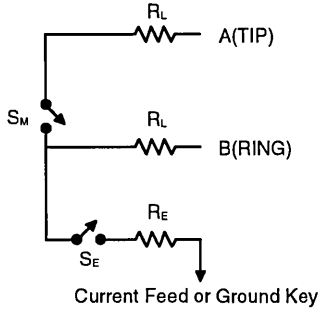
D. Two-Wire Return Loss Test Circuit

15772A–017a

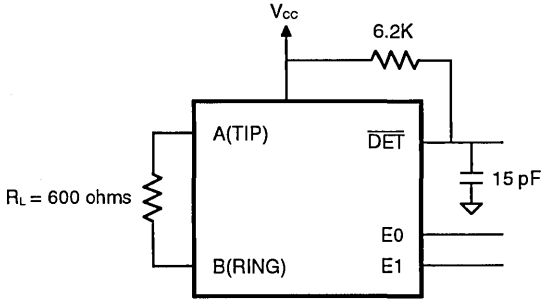
TEST CIRCUITS (continued)



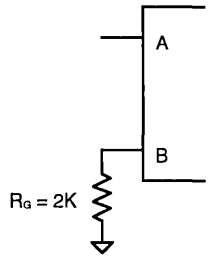
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching

15772A-017b

PRELIMINARY

Am7958

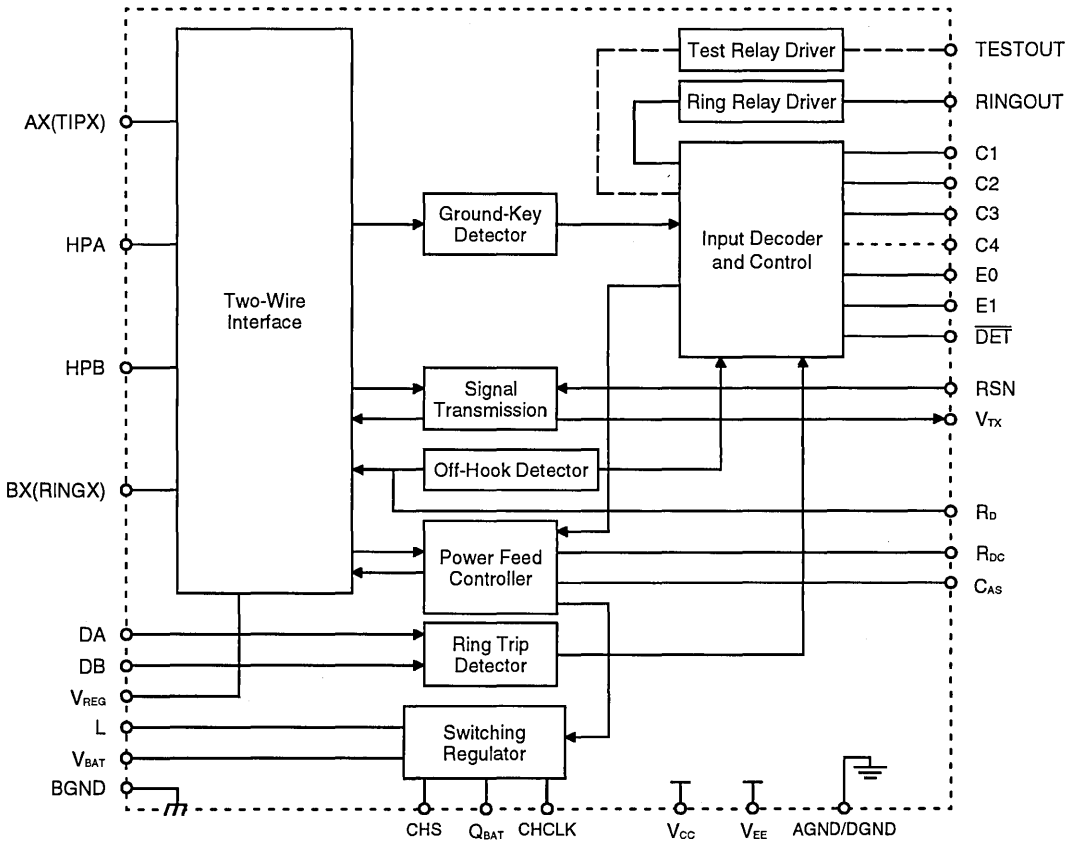
Subscriber Line Interface Circuit (SLIC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Meets LSSGR DC feed requirements
- Programmable constant resistance feed
- Receive Current gain = 200
- Programmable loop detect threshold
- Ground-key detector
- Low standby power
- Performs polarity reversal
- Tip open state for ground start lines
- On-chip switching regulator for low-power dissipation
- Two-wire impedance set by single external impedance
- Test relay driver (PLCC only)

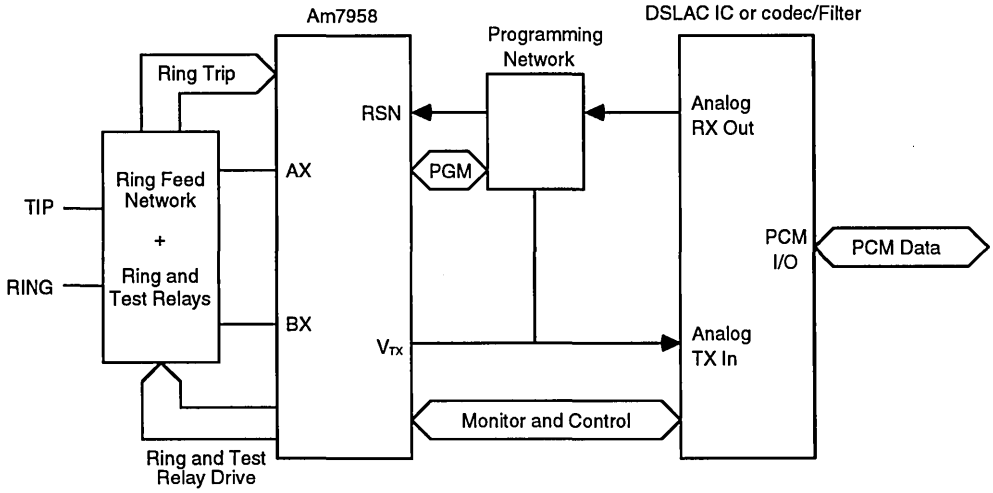
BLOCK DIAGRAM



15772A-001

Publication #: 15772 Rev. B Amendment /0
Issue Date: June 1992

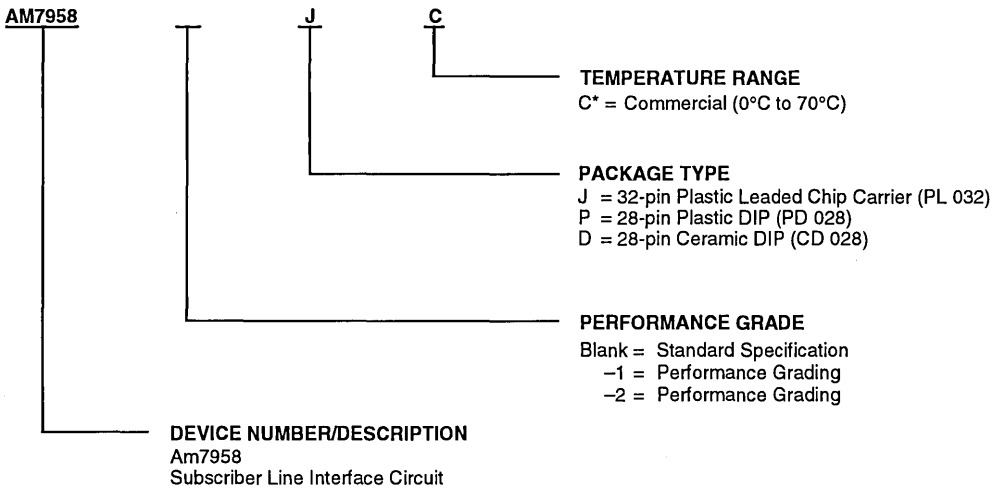
SYSTEM BLOCK DIAGRAM



15772A–002

ORDERING INFORMATION
Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7958	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

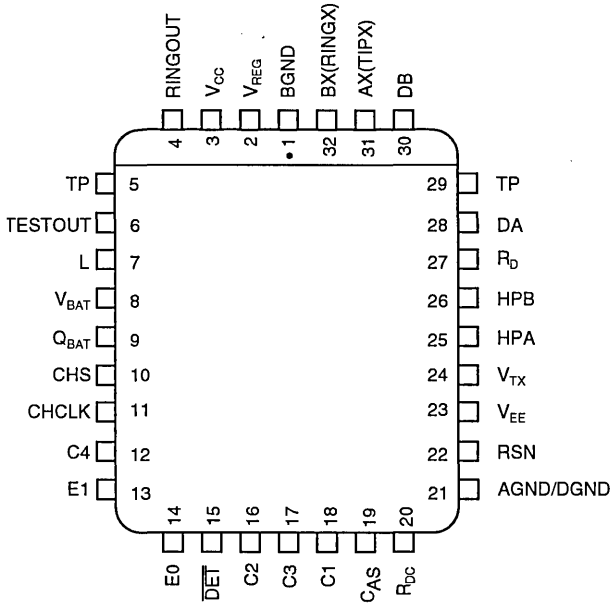
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

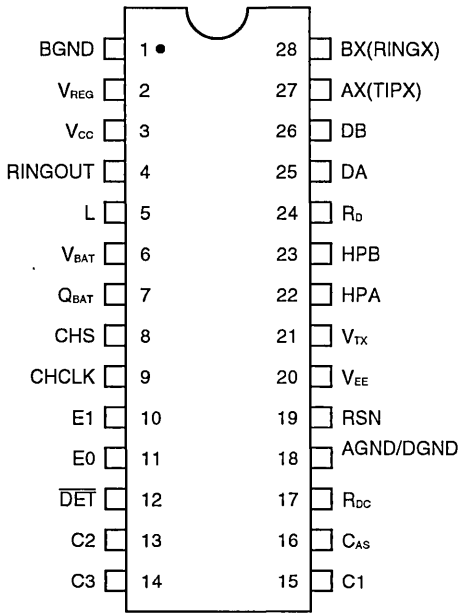
*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

CONNECTION DIAGRAMS

32-Pin Plastic Leaded Chip Carrier (PL 032)



28-Pin Plastic DIP (PD 028)
or
28-Pin Ceramic DIP (CD 028)



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

PIN DESCRIPTION

AGND/DGND
Ground—(see Note 1)

Analog and Digital ground.

AX(TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX(RINGX)
(Output)

Output of B(RING) power amplifier.

C3–C1 Decoder
(Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

CHCLK
Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 250–282 kHz.

CHS
Chopper Stabilization (Input)

Connection for external chopper stabilizing components.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0, E1). The output is open-collector with a built-in 15K pull-up resistor.

E0
Read Enable (Input)

A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$.

E1
Ground-Key Enable (Input)

When E0 is High, E1 = High connects the ground-key detector to $\overline{\text{DET}}$, and E1 = Low connects the off-hook or ring trip detector to $\overline{\text{DET}}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L
Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 50 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}
Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

TESTOUT
Test Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

C4
Test Relay Driver Command (Input)

TTL compatible. A logic Low enables the driver.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

C_{AS}

Reference Filter Capacitor

A capacitor should be connected to this pin to filter internal anti-saturation reference voltage.

Note 1: Analog and digital ground are connected internally to a single pin.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −55°C to +150°C

V_{CC} with respect to AGND/DGND .. −0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to −7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to −70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to −3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... −70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... −70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... −90 V to +10 V
250 ns (F = 0.1 Hz) ..... −120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND ..... −0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C

In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... −4.75 V to −5.25 V

V_{BAT} ..... −40 V to −63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... −100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"−2" performance grade SLICs are functional from −40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (−40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS (see Note 1)

Description	Test Conditions	Preliminary					Unit
		Notes	P.G.*	Min	Typ	Max	
Analog (V_{TX}) Output Impedance		5			3		ohm
Analog (V_{TX}) Output Offset			 –1 –2	–35 –35 –30		+35 +35 +30	mV
Analog (RSN) Input Impedance	300 Hz to 3.4 kHz	5			1	20	ohm
Longitudinal Impedance at AX or BX		5			25	35	ohm
Overload Level	four-wire two-wire	2		–2.5		+2.5	Vpk
Transmission Performance, two-wire impedance (see Test Circuit D)							
Two-Wire Return Loss	300 Hz to 3400 Hz	5, 10		26			dB
Longitudinal Balance (two-wire and four-wire, see Test Circuit C); R_L = 740 ohms							
Longitudinal to Metallic L-T, L-4	200 Hz to 1 kHz Normal Polarity		 –1 –2	54 63 63			dB
	200 Hz to 1 kHz Reverse Polarity			54			dB
	1 kHz to 3.4 kHz Normal Polarity		 –1 –2	54 58 58			dB
	1 kHz to 3.4 kHz			54			dB
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		 –1 –2	40 40 42			dB
Longitudinal Current Capability per Wire	Active State				28		mA
	Disable State				18		RMS
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)							
Gain Accuracy	0 dBm, 1 kHz		 –1 –2	–0.15 –0.15 –0.10		+0.15 +0.15 +0.10	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	5		–0.10		+0.10	dB
Gain Tracking	+7 dBm to –55 dBm Reference: 0 dBm	5		–0.10		+0.10	dB

*P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary Notes	P.G.*	Min	Typ	Max	Unit
Balance Return Signal (four-wire to four-wire, see Test Circuit B)							
Gain Accuracy	0 dBm, 1 kHz		 –1 –2	–0.15 –0.15 –0.10		+0.15 +0.15 +0.10	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	3, 5		–0.10		+0.10	dB
Gain Tracking	+3 dBm to –55 dBm Reference: 0 dBm	5		–0.10		+0.10	dB
Group Delay	f = 1 kHz	5, 12			8		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Distortion Level 300 Hz to 3400 Hz	0 dBm +7.15 dBm				–64 –55	–50 –40	dB
Idle Channel Noise							
C-Message Weighted Noise	two-wire	5			+7	+10	dBrnC
	four-wire				+7	+10	
Single Frequency Out-of-Band Noise (see Test Circuit E)							
Metallic	4 kHz to 9 kHz	4, 5, 8			–76		dBm
	9 kHz to 1 MHz	4, 5, 8			–76		
	256 kHz and harmonics	4, 5			–64		
Longitudinal	1 kHz to 15 kHz	5			–70		dBm
	Above 15 kHz	4, 5			–85		
	256 kHz and harmonics	4, 5			–57		
D.C. Feed Characteristics Without Fuse Resistors (See Figures 1a, 1b, 1c), Battery = –48 V							
Apparent Battery, Active Mode	R_L=600 and 900 ohm			47	50	53	V
Loop Current Accuracy, Active Mode	R_L=600 and 900 ohm			–7.5		+7.5	%
Loop Current, Active Mode	R_L= 2000 ohm			20			mA
Loop Current, Tip open Tip open	 R_L= 600 ohm R_L= 0					 1.0 1.0	mA
Loop Current Limit Accuracy–Active and Disable Mode	R_L= 0	9		–20		+20	%
I_{LLIM} (I_{tip} + I_{ring})	Tip and Ring shorted to ground, normal polarity				95	115	mA
Power Dissipation Battery; Battery = –48 V; Normal Loop Polarity Rfuse = 2x50 ohm							
On-Hook Open Circuit					35	100	mW
On-Hook Disable Mode					135	225	
On-Hook Active Mode					180	300	
Off–Hook Disable Mode R_L = 50 ohms					450	700	
Off-Hook Active Mode R_L = 50 ohms					975	1150	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary Notes	P.G.*	Min	Typ	Max	Unit
Supply Currents							
V_{CC} On-Hook Supply Current	Open Circuit Mode				3.0	4.5	mA
	Disable Mode				6.0	10.0	
	Active Mode				7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode				1.0	2.3	
	Disable Mode				2.2	3.5	
	Active Mode				2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode				0.4	1.0	
	Disable Mode				3.0	5.0	
	Active Mode				4.0	6.0	
Power Supply Rejection Ratio (Vripple = 50 mV RMS)							
V_{CC}	50 Hz to 3400 Hz	6		25	45		dB
	3.4 kHz to 50 kHz	6		22	35		
V_{EE}	50 Hz to 3400 Hz	6		20	40		
	3.4 kHz to 50 kHz	6		10	25		
V_{BAT}	50 Hz to 3400 Hz	6		27	45		
	3.4 kHz to 50 kHz	6		20	40		
Effective Internal Resistance	C_{AS} pm to GND	5		85	170	255	Kohm
Off-Hook Detector							
Current Threshold	$I_{DET} = 365/R_D$			–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V							
Ground-Key Resistance Threshold	B(Ring) to GND			2.0	5.0	12.0	Kohm
Ground-Key Current Threshold	B(Ring) to GND	7			9		mA
	Midpoint to GND				9		
Ring Trip Detector Input							
Bias Current				–5	–0.05		µA
Offset Voltage	Source Resistance = 0 to 2 Mohm	11		–50	0	+50	mV
Logic Inputs (C1, C2, C3, C4, E0, E1, and CHCLK)							
Input High Voltage				2.0			V
Input Low Voltage						0.8	V
Input High Current				–75		40	µA
Input Low Current				–0.4			mA
Logic Output ($\overline{DET}$)							
Output Low Voltage	I_{OUT} = 0.8 mA					0.4	V
Output High Voltage	I_{OUT} = –0.1 mA			2.4			V

SWITCHING CHARACTERISTICS

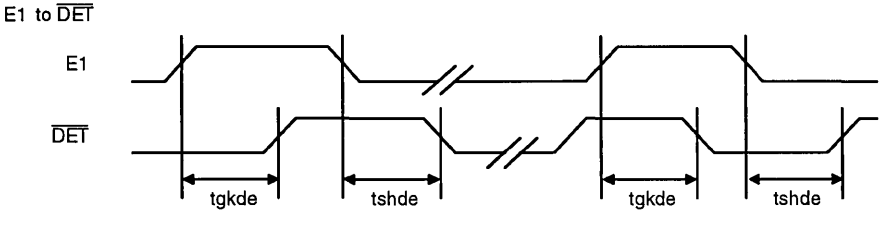
Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E1 High to $\overline{DET}$ High	Ground-Key Detect Mode	–	–	3.8	µs
	E1 High to $\overline{DET}$ Low	E0 = 0 (see Test Circuit H)	–	–	1.1	
tshde	E1 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.2	µs
	E1 Low to $\overline{DET}$ High	E0 = 1 (see Test Circuit G)	–	–	3.8	
tshdd	E0 High to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.1	µs
tshd0	E0 Low to $\overline{DET}$ High	E1 = 0 (see Test Circuit G)	–	–	3.8	
tgkdd	E0 High to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.1	µs
tgkd0	E0 Low to $\overline{DET}$ High	E1 = 1 (see Test Circuit G)	–	–	3.8	

Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C3	C2	C1	Two-Wire Status	E0 = 1*, E1 = 0	E0 = 1*, E1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

*A logic Low on E0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING WAVEFORMS



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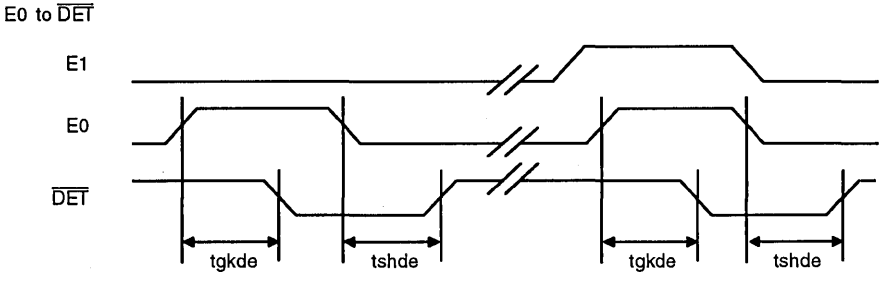
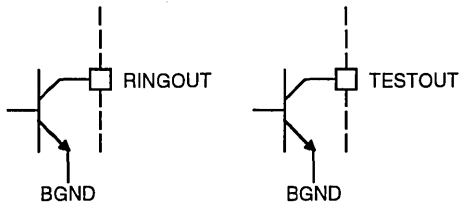


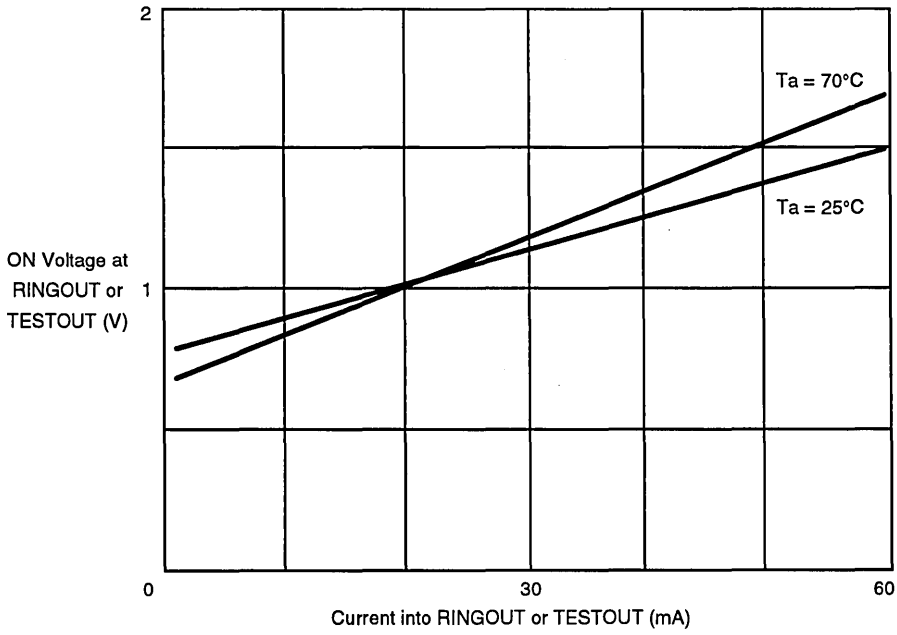
15772A–013

RELAY DRIVER SPECIFICATIONS



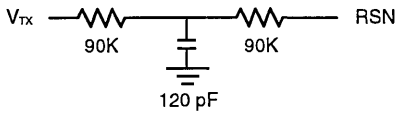
Description	Test Conditions	Note	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)						
On Voltage	25 mA Sink				+1.5	V
Off Leakage	V_{OFF} = + 15 V				100	µA

Relay Driver Characteristics (Typical)



Notes:

1. Unless otherwise noted, test conditions are: Battery = –48 V battery applied to V_{BAT} pin through a surge protection diode, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 900 ohms, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 2K, C_{DC} = 1.0 µF, R_d = 51.1K, C_{AS} = 0.47 µF, no fuse resistors. RT = 180K, R_{RX} = 90 V.
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes the two-wire AC load impedance matches the programmed impedance.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
8. Fundamental and harmonics from switch regulator chopper are not included.
9. Loop current limit is calculated using the following equations:
   In Disable Mode: $I_{LIMIT} = 90/(R_{DC1} + R_{DC2})$
   In Active Mode: $I_{LIMIT} = 230/(R_{DC1} + R_{DC2})$
10. Assumes the following Z_T network:



11. Tested with 0 ohms source impedance. Two Mohms is specified for system design purposes only.
12. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN, Z_T is defined above, and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 10(R_{FEED} - 2R_F)$ $C_{DC} = (1.0\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and f_c is the desired filter cut-off frequency.
R_{FUSE}	20 ohm–50 ohm user selectable

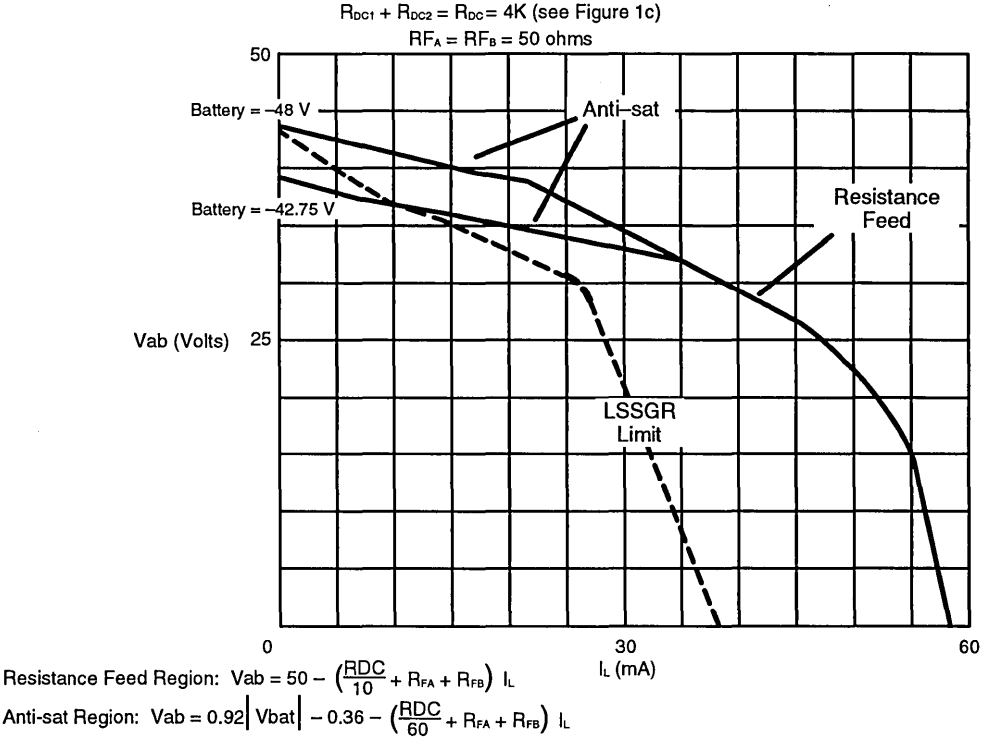


Figure 1a. Vab versus I_L (Typical)

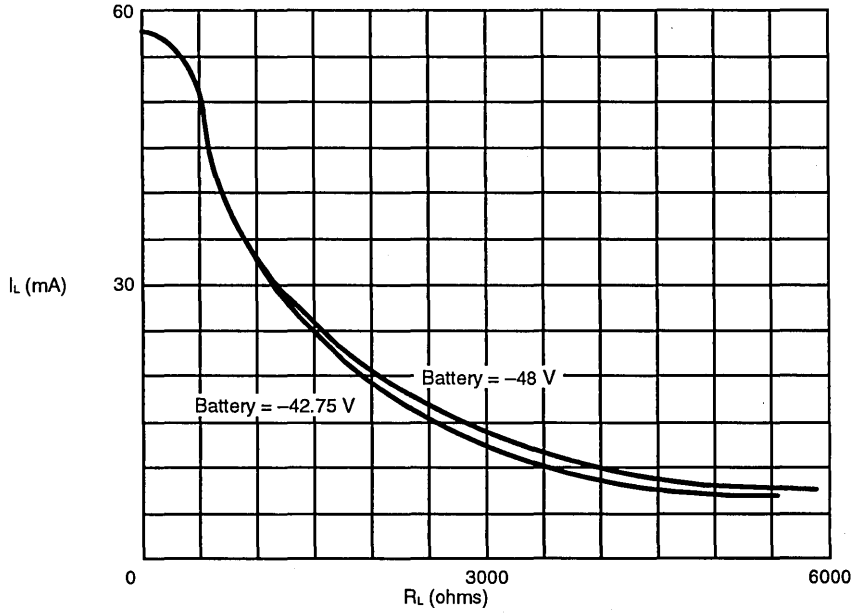
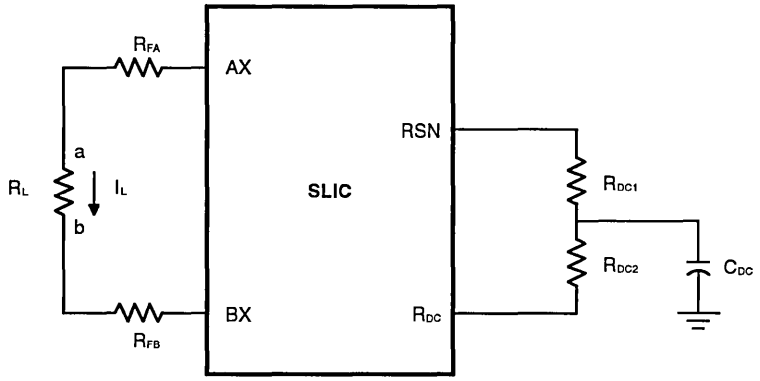


Figure 1b. I_L versus R_L

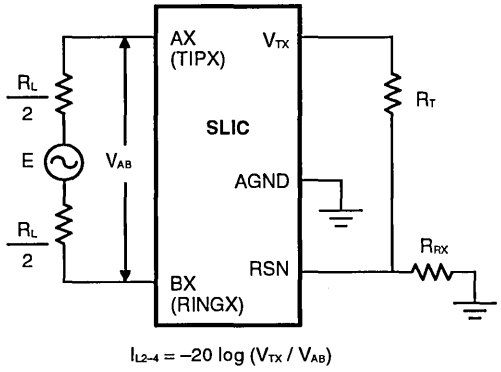


Feed Resistance programmed by R_{DC1} and R_{DC2}.

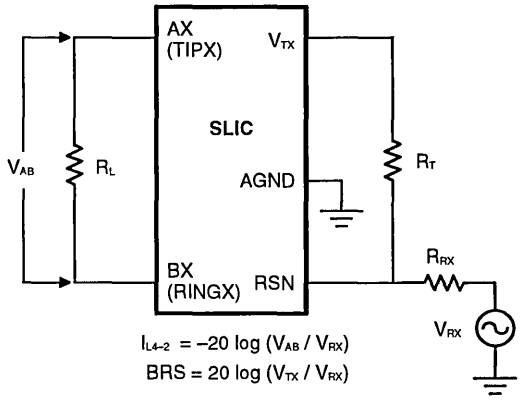
15772A–016

Figure 1c. Feed Programming

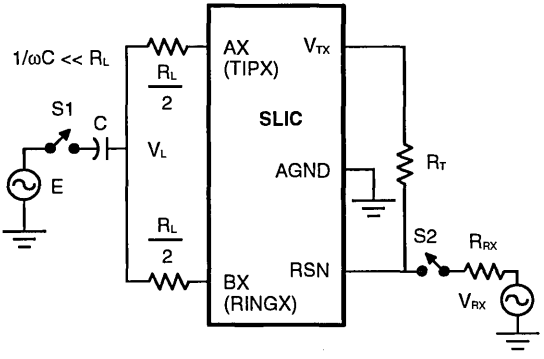
TEST CIRCUITS



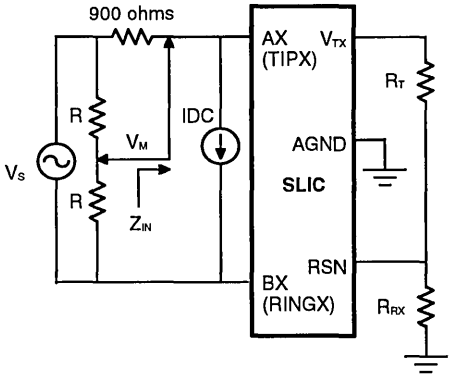
A. Two-to-Four Wire Insertion Loss



B. Four-to-Two Wire Insertion Loss and Balance Return Signal



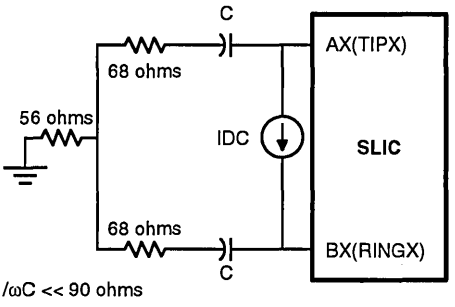
C. Longitudinal Balance



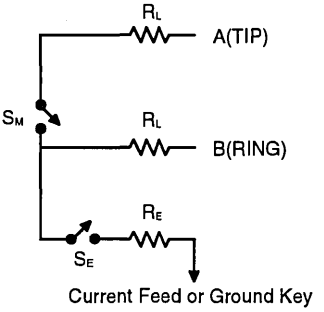
D. Two-Wire Return Loss Test Circuit

15772A–017a

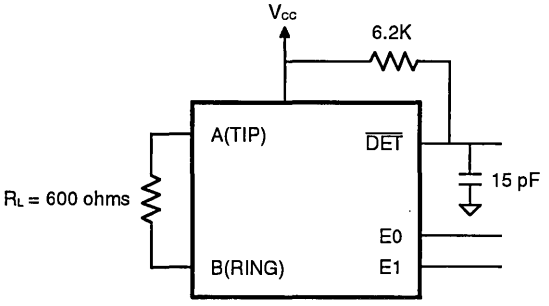
TEST CIRCUITS (continued)



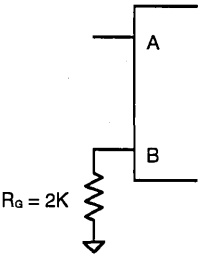
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching

15772A-017b

CENTRAL OFFICE SLICs

Application Notes

The AMD SLIC Family offers a high degree of versatility for applications in many types of Central Office and PBX line circuits. In this section, typical single-channel and multiple-channel applications are described.

Figure 1 shows a detailed schematic of a basic single-line system using one SLIC and one-half of an Am79C02 DSLAC IC.

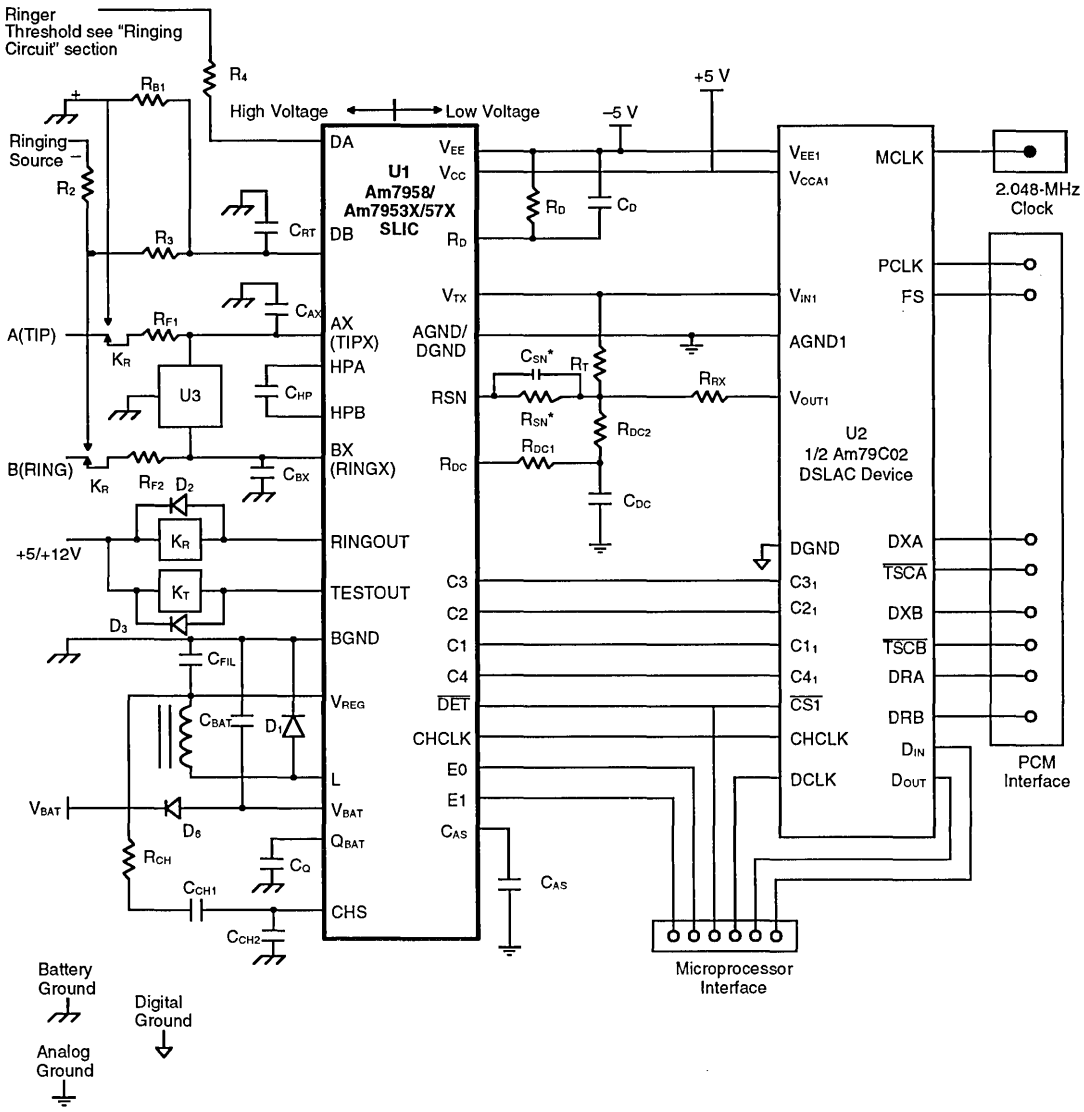
In the receive path, the DSLAC IC processes digital PCM voice data into analog signals and inputs them to the SLIC RSN pin through resistor R_{RX}. In the transmit path, the analog output at the SLIC V_{TX} pin is processed by the DSLAC IC and output in serial-digital format to the PCM interface. R_{RX} sets the receive gain, and R_T is used to synthesize the AC two-wire output impedance. Both R_T and R_{RX} can be complex, to achieve optimized parameters over the voice band.

In the control path, when the line goes off-hook, the SLIC pulls its collector $\overline{DET}$ output down and enables the DSLAC IC serial control data I/O pins, D_{IN} and D_{OUT} (see Figure 1). The microprocessor also recognizes the off-hook, and typically will send a response such as an active state or ring relay release command back to the SLIC, via the DSLAC IC D_{IN} pin and the C3–C1 data bus.

The C4 line is also addressed in the same manner, to enable or disable the test relay driver. The E0 and E1 pins are addressed directly by the microprocessor as shown.

SLIC monitor and control functions which can be performed using a microprocessor and the circuitry shown in Figure 1 include:

- During the disable state, inform the processor when an off-hook has occurred and send a power up command to the SLIC.
- Detect an off-hook during ringing and send a command to the SLIC to release the ring relay.
- Detect an on-hook condition during the active state and send a command to the SLIC to enter the disable state.
- Send a line polarity reverse command to the SLIC.
- Command the SLIC into the ground-key sense mode.
- Command the SLIC to energize the ring relay, K_R.
- Command the SLIC to energize the test relay, K_T.



*Am7958 only. Replace with short circuit for Am7953X/57X.

15772B-018

Figure 1. Single Channel of a Dual Channel Subscriber Line Circuit

Table 1. Parts List — 1/2 of a Dual Channel Subscriber Line System (see Figure 1 for Circuit)

U1	Am7958 SLIC
U2	Am79C02 DSLAC Device
K_R, K_T	Relay, 2C contacts, 1500-V rating
L	Inductor, 1 mH, 5%
D_1	Diode, 100 V, 100 mA, 4 ns
U_3	Dual transient suppressor, Texas Instruments TISP1082
D_6, D_2, D_3	Diode 100 V, 100 mA, 10 ns
RF_1, RF_2	Resistor, fuse, 50 *ohms
R_2	Resistor, 800 ohms, 3%, 3 W (Ring Feed Resistor)*
RB_1	Resistor, 1 meg, 1%, 1/4 W
R_3	Resistor, 8.25 K, 1%, 1/4 W
R_4	Resistor, 452 K, 1 %, 1/4 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W**
R_D	Resistor, 51.1K, 1%, 1/4 W (sets off-hook threshold)*
R_{DC1}, R_{DC2} (Am7958)	Resistor, 2K, 1%, 1/4 W (sets loop current)*
R_{DC1}, R_{DC2} (Am7953X)	Resistor, 31.25K, 1%, 1/4 W*
R_{DC1}, R_{DC2} (Am7957X)	Resistor, 20K, 1%, 1/4 W*
R_T (Am7958)	Resistor, 160K, 1%, 1/4 W (sets two-wire impedance)*
R_T (Am7953X/57X)	Resistor, 560K, 1%, 1/4 W*
R_{SN} (Am7958)	Resistor, 300K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX}	Resistor, 115K, 1%, 1/4 W (sets receive gain)*
R_{RX} (Am7953X/57X)	Resistor, 560K, 1%, 1/4 W
C_{SN} (Am7958)	Capacitor, 39 nF, 10%, 10 V
C_{RT}	Capacitor, 0.047 µF, 20%, 100 V
C_{DC} (Am7953X/57X)	Capacitor 0.15 µF, 10%, 10 V
C_{DC} (Am7958)	Capacitor 1.0 µF, 20%, 10 V
C_{HP}	Capacitor, 0.33 µF, 20%, 100 V
C_{AS}	Capacitor, 0.15 µF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2200 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.15 µF, 10%, 100 V, Metallized Polyester
C_{BAT}	Capacitor, 0.47 µF, 20%, 100 V
C_Q	Capacitor, 0.33 µF, 20%, 100 V
C_{CH1}	Capacitor, 0.015 µF, 10%, 50 V, X7R ceramic
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic
C_D	Capacitor, 0.01 µF, 20%, 10 V (sets off-hook filtering)*

Note:The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.

Central Office Metering SLICs

CENTRAL OFFICE METERING SLIC PRODUCTS

General Description

AMD's Central Office Metering SLIC (Subscriber Line Interface Circuit) products perform the telephone line interface functions required by most types of telephone switching and transmission equipment that must support the metering function. The full range of signal transmission, battery feed, and loop supervision functions are also supported.

The Am79M53X and Am79M57X Central Office Metering SLIC Family is compatible with CCITT recommendations and supports 2.2-V metering at 12 and 16 kHz. The new Am79HM53 is designed to support higher level metering requirements such as the 5.1-V metering in required in Germany. All of the Central Office Metering SLICs feature an internal, self-adjusting switching regulator to reduce power consumption to a minimum and enhance system reliability. They also support on-hook transmission and offer extended temperature performance, making either type ideal for Digital Loop Carriers and other applications that require metering.

The signal transmission functions of all AMD SLICs include both two-to-four-wire and four-to-two-wire conversion. The two-wire termination impedance is programmable with a single external impedance. The companion AMD SLAC or DSLAC IC (Single-Channel or Dual-Channel Subscriber Line Audio-Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the DSLAC IC is not used, most codec/filters provide an uncommitted op amp for this purpose.

The SLIC's battery feed architecture makes their DC feed characteristics programmable with external resistors. Furthermore, these characteristics are independent of battery variations. AMD's Central Office Metering SLICs are optimized for either 48- or 63-V operation.

A polarity reversal function is provided on all SLICs and transposes the normal voltage sense of the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode is also provided, limiting loop current and cutting power dissipation while allowing the full complement of supervisory functions to be utilized.

The supervisory functions of off-hook detection and ring trip detection are read through a single, TTL-compatible output. To eliminate noise-induced errors, the off-hook detector signal may be filtered. Off-hook detection has a threshold that is set by the value of an external resistor. Additional supervisory controls put the A lead into an open circuit or high-impedance state suitable for application in ground start systems. Similarly, both the A and B leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Two relay drivers support ring and test relay functions, or can be used for other functions such as activating a message waiting lamp.

The SLIC's user-programmable states are controlled by a TTL-compatible code. The control inputs are designed to easily interface to popular single-chip microcontrollers, such as the industry standard 8051, or to latched outputs from a SLAC or DSLAC device.

PRELIMINARY

Am79M531/Am79M535

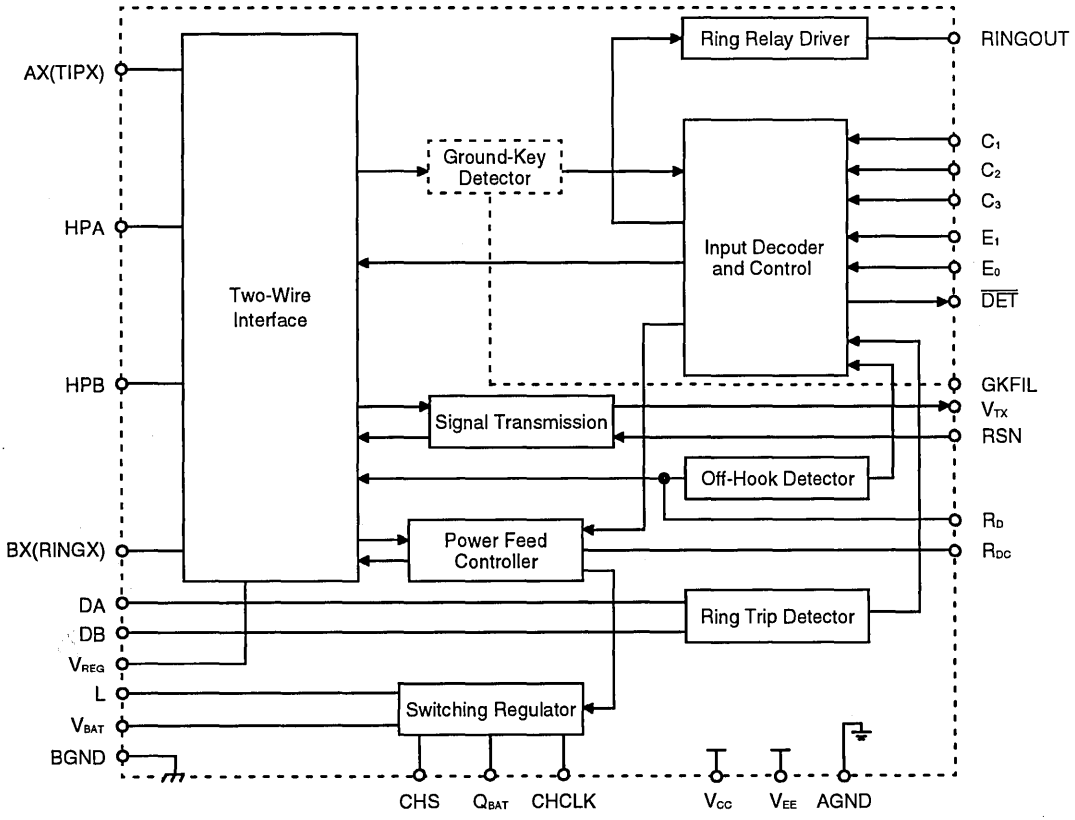
Metering Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Line-feed characteristics independent of battery variations
- Programmable loop detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise filter capacitor available
- Ground-key detect
- Low standby power
- Two-wire impedance set by single external impedance
- Performs polarity reversal
- Tip open state for ground start lines
- Supports 2.2-V RMS metering (12 and 16 kHz)

BLOCK DIAGRAM



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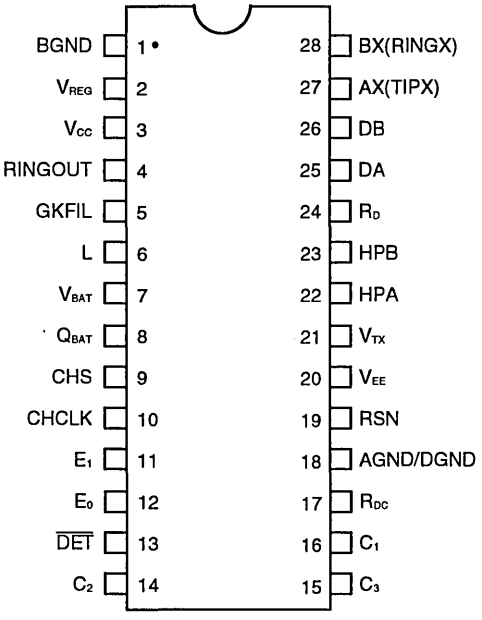
Notes: Am79M531—E_0 and E_1 inputs; ring relay driver sourced internally to BGND; no test relay driver; ground-key filter pin.
Am79M535—E_0 and E_1 inputs; ring relay driver sourced internally to BGND; ground-key filter pin.
Current gain (K_I) = 1000 for all parts.

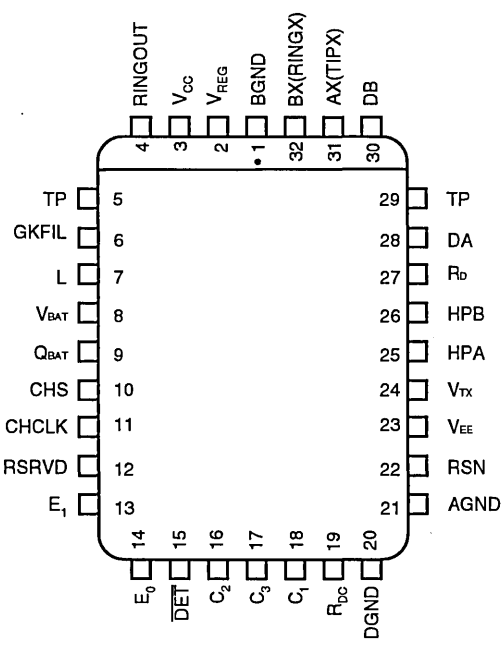
Publication #: 16856 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View

Am79M531



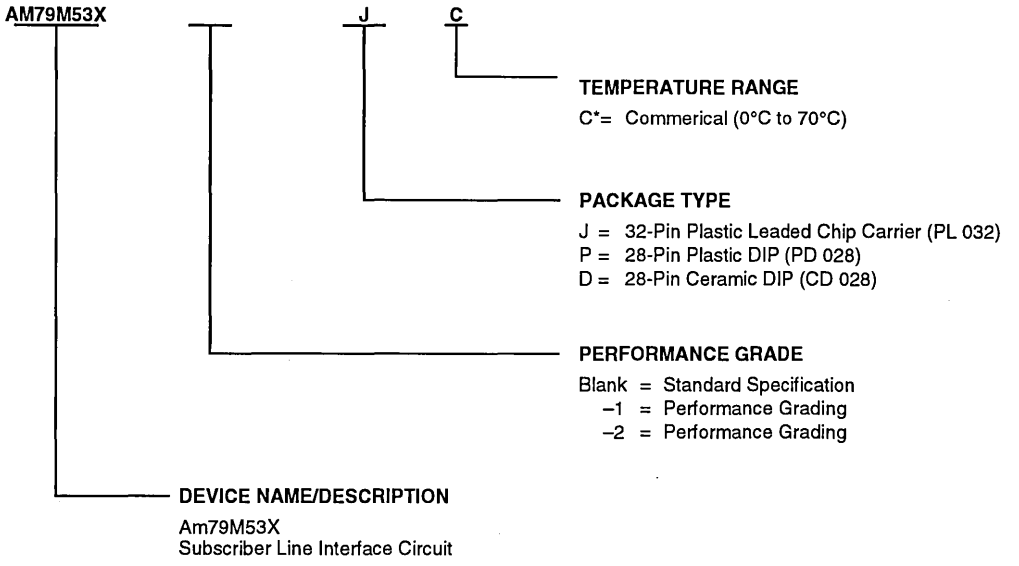
Am79M535



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79M53X	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND
Ground (Am79M535)

Analog (Quiet) ground.

DGND
Ground (Am79M535)

Digital ground.

AGND/DGND
Ground (Am79M531)

Analog and digital ground are connected internally to a single pin.

AX(TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX(RINGX)
(Output)

Output of B(RING) power amplifier.

C_3–C_1
Decoder (Inputs)

TTL compatible. C_3 is MSB and C_1 is LSB.

CHCLK
Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (nominal).

CHS
Chopper Stabilization (Input)

Connection for external stabilization components.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$
Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C_3–C_1, E_0, E_1). The output is open-collector with a built-in 15K pull-up resistor.

E_0
Read Enable (Input)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E_1
Ground-Key Enable (Input)

When E_0 is High, E_1 = High connects the ground-key detector to $\overline{DET}$, and E_1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

GKFIL
Ground-Key Filter Capacitor Connection

An external capacitor for filtering out high-frequency noise from the ground-key loop can be connected to this pin. An internal 36K –20%, +40% resistor is provided to form an RC filter with the external capacitor.

In versions which have a GKFIL pin, a 3.3 nF minimum capacitance must be connected from the GKFIL pin to ground.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L
Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}
Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT} (Am79M531).

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

V_{BAT}

Connected to office battery supply through an external protection diode.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is 0.510 times the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −55°C to +150°C

V_{CC} with respect to AGND/DGND .. −0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to −7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to −70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to −3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... −70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... −70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... −90 V to +10 V
250 ns (F = 0.1 Hz) ..... −120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Driver ..... 60 mA

Voltage on Ring Trip Input
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C3–C1, E0, E1, CHCLK to
AGND/DGND ..... −0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... −4.75 V to −5.25 V

V_{BAT} ..... −40 V to −63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... −100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"−2" performance grade SLICs are functional from −40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (−40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS over operating range

Am79M531/Am79M535 (see Note 1)

Description	Test Conditions	Preliminary P.G.*	Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance (Note 5)				3		ohm
Analog (V_{TX}) Output Offset			−35		+35	mV
		−1	−30		+30	
Analog (RSN) Input Impedance (Note 5)	300 Hz to 3.4 kHz			1	20	ohm
Longitudinal Impedance at AX or BX (Note 5)					35	
Overload Level	four-wire		−3.1		+3.1	Vpk
Z_{2WIN} = 600 to 900 ohms (Note 2)	two-wire		−6.0		+6.0	
Transmission Performance, two-wire impedance						
Two-Wire Return Loss	300 Hz to 500 Hz		26			dB
(See Test Circuit D)	500 Hz to 2500 Hz		26			
(Notes 5, 13)	2500 Hz to 3400 Hz		20			
Longitudinal Balance (two-wire and four-wire, see Test Circuit C)						
R_L = 600 ohms, Longitudinal to Metallic	300 Hz to 3400 Hz		48			dB
L-T, L-4 (normalized to unity gain)		−1	52			
Longitudinal to Metallic L-T and L-4 (normalized to unity gain) (for trimmed version consult factory)	200 Hz to 1000 Hz	−2**	63	70		
	1000 Hz to 3400 Hz		58	70		
	200 Hz to 3400 HZ (Reverse Polarity)		54			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		40			dB
	300 Hz to 800 Hz	−1	42			
Longitudinal Current Capability	Active State			25		mA
per Wire (Note 5)	Disable State			18		RMS
Insertion Loss (see Test Circuits A and B)						
Two-Wire to Four-Wire	V_{AB} = 0 dBm, 1 kHz		5.70	5.85	6.00	dB
		−1	5.75		5.95	
Four-Wire to Two-Wire	V_{RX} = 0 dBm, 1 kHz		−0.15		+0.15	dB
		−1	−0.1		+0.1	
Insertion Loss versus Frequency (see Test Circuits A and B)						
Two-Wire to Four-Wire or	300 Hz to 3400 Hz		−0.1		+0.1	dB
Four-Wire to Two-Wire	Relative to 1 kHz					
Gain Tracking (see Test Circuits A and B)						
Two-Wire to Four-Wire or	+7 dBm to −55 dBm		−0.1		+0.1	dB
Four-Wire to Two-Wire (Note 5)	Reference: 0 dBm					
Balance Return Signal (four-wire to four-wire, see Test Circuit B)						
Gain Accuracy (Note 3)	0 dBm, 1 kHz		−6.00	−5.85	−5.70	dB
		−1	−5.95		−5.75	
Variation with Frequency (Notes 3, 5)	300 Hz to 3400 Hz		−0.1		+0.1	dB
	Relative to 1 kHz					
Gain Tracking (Note 5)	+3 dBm to −55 dBm		−0.1		+0.1	dB
	Reference: 0 dBm					
Group Delay (Notes 5, 14)	F = 1 kHz			5.3		µs

*P.G. = Performance Grade
**All other performance parameters equivalent to −1 grade.
Normal Polarity only.

ELECTRICAL CHARACTERISTICS (continued)

Description		Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Total Harmonic Distortion		0 dBm, 300 Hz to 3.4 kHz +9 dBm, 300 Hz to 3.4 kHz			–64 –55	–50 –40	dB
Total Harmonic Distortion With Metering (Notes 5, 10)						–35	dB
Idle Channel Noise							
C-Message Weighted Noise (Notes 5, 7)		two-wire	 –1		+7 +7	+15 +12	dBrnC
		four-wire	 –1		+3 +3	+10 +7	dBrnC
Psophometric Weighted Noise (Note 7)		two-wire	 –1		–83 –83	–75 –78	dBmp
		four-wire	 –1		–87 –87	–80 –83	dBmp
Psophometric Idle Channel Noise with Metering (Notes 5, 11)		two-wire				–46	dBmp
		four–wire				–52	
Single Frequency Out-of-Band Noise (see Test Circuit E)							
Metallic	Notes 4, 5, 9	4 kHz to 9 kHz			–76		dBm
	(Notes 4, 5, 9)	9 kHz to 1 MHz			–76		
	(Notes 4, 5)	256 kHz and harmonics			–57		
Longitudinal	(Notes 4, 5, 9)	1 kHz to 15 kHz			–70		dBm
	(Notes 4, 5, 9)	Above 15 kHz			–85		
	(Notes 4, 5)	256 kHz and harmonics			–57		
DC Feed Currents (see Figures 1a, 1b, 1c) Battery = –48 V							
Active Mode Loop Current Accuracy		I_{LOOP} (nominal) = 40 mA		–7.5		+7.5	%
Disable Mode		R_L = 600 ohms		18	20	22	mA
Tip Open Mode		R_L = 600 ohms				1.0	
Open Circuit Mode		R_L = 0 ohms				1.0	
Fault Current Limit, I_{LIM} (I_{AX} + I_{BX})		AX and BX shorted to ground				130	mA
Power Dissipation Battery = –48 V, Normal Polarity							
On-Hook Open Circuit			 –1		35 35	120 80	mW
On-Hook Disable Mode			 –1		135 135	250 200	
On-Hook Active Mode			 –1		200 200	400 300	
Off-Hook Disable Mode		R_L = 600 ohms			500	750	
Off-Hook Active Mode		R_L = 600 ohms			650	1000	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3.0	4.5	mA
	Disable Mode			6.0	10.0	
	Active Mode			7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.2	3.5	
	Active Mode			2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.0	5.0	
	Active Mode			4.0	6.0	
Power Supply Rejection Ratio (Vripple = 50 mV RMS)						
V_{CC} (Notes 6, 7)	50 Hz to 3400 Hz		25	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		22	35		dB
		–1	25	35		
V_{EE} (Notes 6, 7)	50 Hz to 3400 Hz		20	40		dB
		–1	25	40		
	3.4 kHz to 50 kHz		10	25		dB
		–1	10	25		
V_{BAT} (Notes 6, 7)	50 Hz to 3400 Hz		27	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		20	40		dB
		–1	25	40		
Off-Hook Detector						
Current Threshold Accuracy	I_{DET} = 365/R_D Nominal		–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V (see Test Circuit F)						
Ground-Key Resistance Threshold	B(Ring) to GND		2.0	5.0	10.0	Kohm
Ground-Key Current Threshold (Note 8)	B(Ring) to GND			9		mA
	Midpoint to GND			9		
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage (Note 12)	Source Resistance 0 to 2 Mohms		–50	0	+50	mV
Logic Inputs (C_1, C_2, C_3, C_4, E_0, E_1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4			mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

SWITCHING CHARACTERISTICS
Am79M531

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E_1 High to $\overline{DET}$ High (E_0 = 1)	Ground-Key Detect Mode R_L Open, R_G Connected (see Test Circuit G)			3.8	µs
	E_1 High to $\overline{DET}$ Low (E_0 = 1)				1.1	
tshde	E_1 Low to $\overline{DET}$ Low (E_0 = 1)	Switch Hook Detect Mode R_L = 600 ohms, R_G Open (see Test Circuit H)			1.2	µs
	E_1 Low to $\overline{DET}$ High (E_0 = 1)				3.8	
tshdd	E_0 High to $\overline{DET}$ Low (E_1 = 0)				1.1	µs
tshd0	E_0 Low to $\overline{DET}$ High (E_1 = 0)				3.8	
tgkdd	E_0 High to $\overline{DET}$ Low (E_1 = 1)				1.1	µs
tgkd0	E_0 Low to $\overline{DET}$ High (E_1 = 1)				3.8	

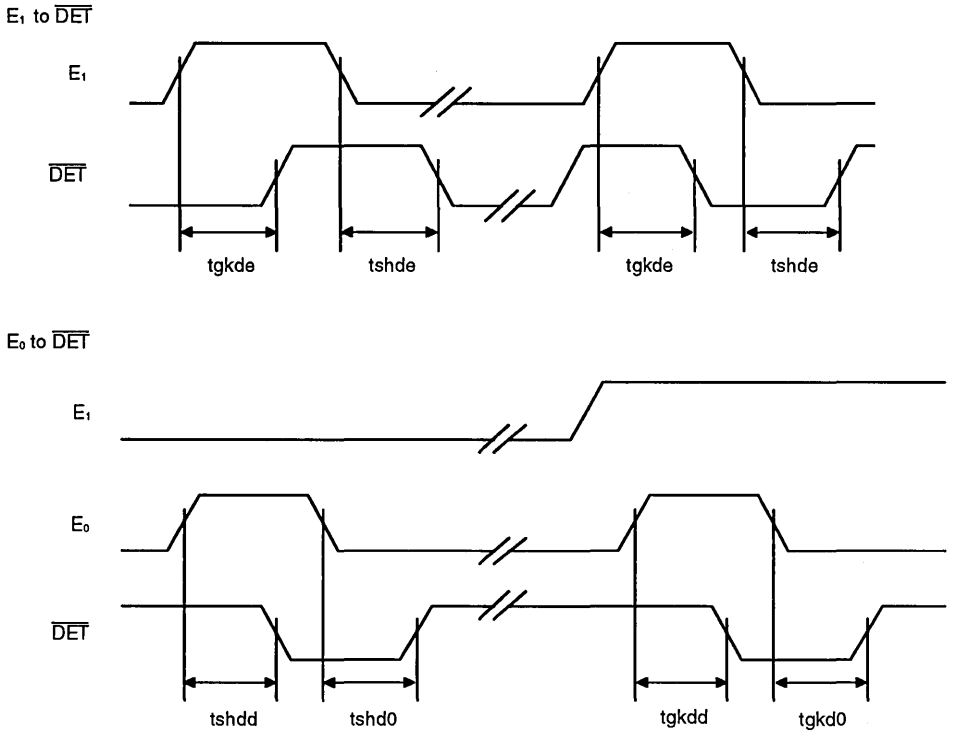
Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	E_0 = 1* E_1 = 0	E_0 = 1 E_1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

*A logic Low on E_0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING WAVEFORMS

Am79M531/Am79M535

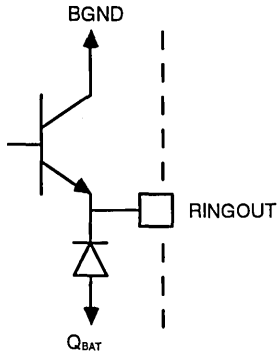


Note: All delays measured at 1.4-V level.

11701B–013

Relay Driver Specifications

Am79M531/Am79M535



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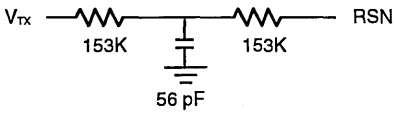
Description	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Relay Driver Outputs (RINGOUT)					
On Voltage	50 mA Source	BGND –2	BGND – 0.95		V
Off Leakage			0.5	100	µA
Clamp Voltage	50 mA Sink	Q_{BAT} –2			V

Notes:

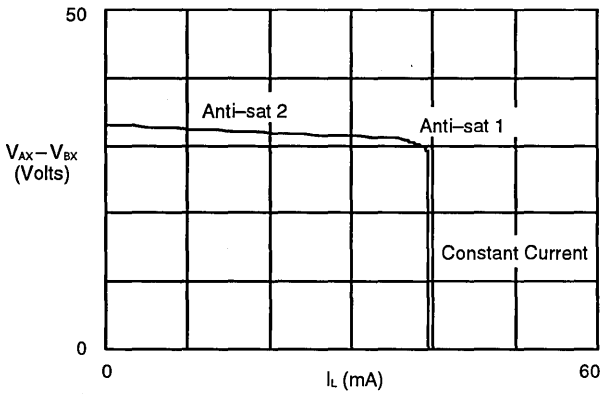
1. Unless otherwise noted, test conditions are: Battery = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.22 µF, R_{DC1} = R_{DC2} = 31.25K, C_{DC} = 0.1 µF, R_d = 51.1K, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 306K resistive, receive input summing impedance (Z_{RX}) = 300K resistive. (See Table 2 for component formulas.)
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 17 V.
8. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from 256-kHz switch-regulator chopper are not included.
10. Total harmonic distortion with metering as specified with a metering signal of 2.2 VRMS at the two-wire output, and a transmit signal of +3 dBm or receive signal of –4 dBm. The transmit or receive signals are single-frequency inputs, and the distortion is measured as the highest in-band harmonic at the two-wire or the four-wire output relative to the input signal.
11. Noise with metering is measured by applying a 2.2-VRMS metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire and four-wire outputs over a 200-ms time interval.
12. Tested with 0 ohms source impedance. Two Mohms is specified for system design purposes only.
13. Assumes the following Z_T network:



14. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 13 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 510(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{1000\ Z_T}{Z_T + 510\ (Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 2500/I_{FEED}$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$Z_M = \frac{V_{MG}}{V_{M2W}} \cdot \frac{K_1(\omega)\ Z_L \cdot Z_T}{Z_T + 0.51 \cdot K_1(\omega)\ (2R_F + Z_L)}$	Z_M is connected from V_{MG} (metering source) to the RSN pin, V_{M2W} is the desired magnitude of the metering signal at the two-wire output (usually 2.2 VRMS) and $K_1(\omega)$ is defined below. $K_1(\omega) = \frac{1000}{1 + j\omega\ (11.5 \cdot 10^{-9} + CX/2)(36 + Z_L + 2R_F)}$ where: CX = The values of the identical capacitors from AX and BX to ground $\omega = 2\pi \times$ metering frequency



$V_{BAT} = -47.3$ V
$R_{DC1} + R_{DC2} = R_{DC} = 62.5K$

Constant current region: $I_L = \frac{2500}{R_{DC}}$

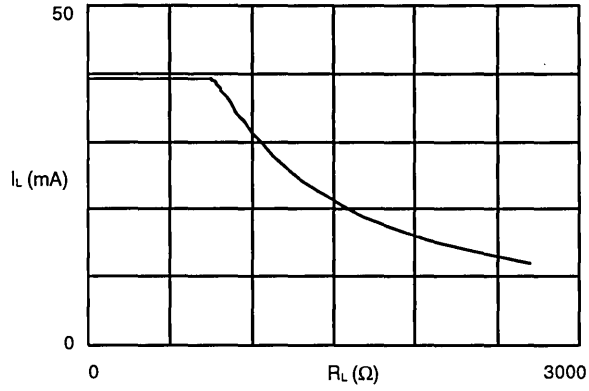
Anti-sat 1 region: $V_{AX-BX} = 45.78 - \frac{R_{DC}}{152.6} I_L$

Anti-sat 2 region: $V_{AX-BX} = 1.075 \mid V_{BAT} \mid -17.86 - \left(0.013 + \frac{R_{DC}}{1512}\right) I_L$

See Figure 1c.

11701B–014

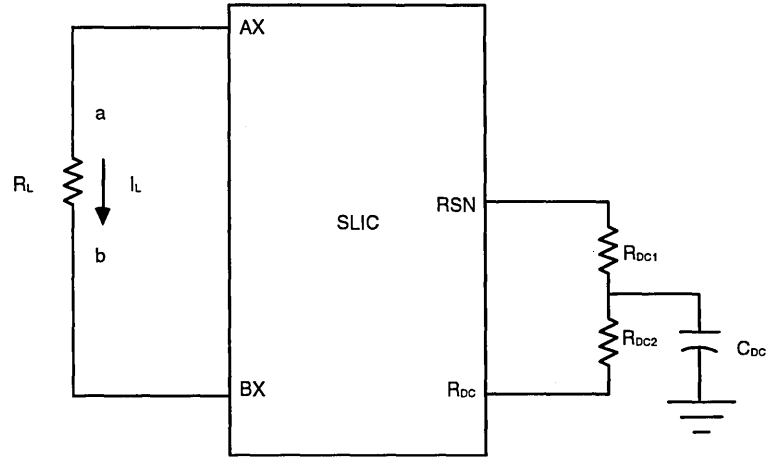
Figure 1a. Load Line (Typical)



Load Current versus Load Resistance – Am79M531/Am79M535
V_{BAT} = –47.3 V
R_{DC} = 62.5K
See Figure 1c.

11701B–015

Figure 1b. Feed Characteristics (Typical)

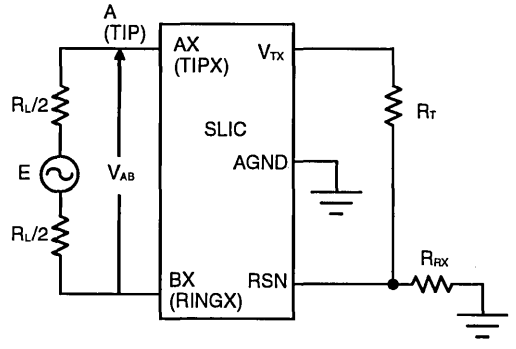


Current programmed by R_{DC1} and R_{DC}.

11701B–016

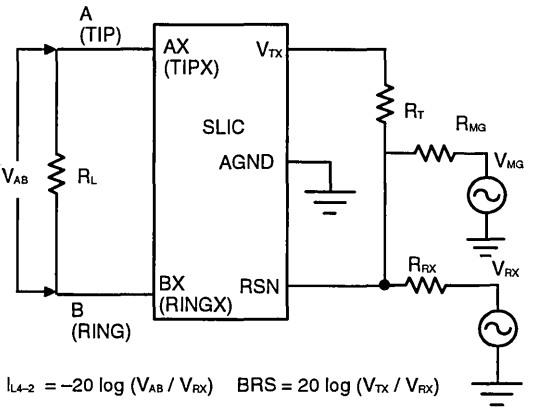
Figure 1c. Feed Programming

TEST CIRCUITS



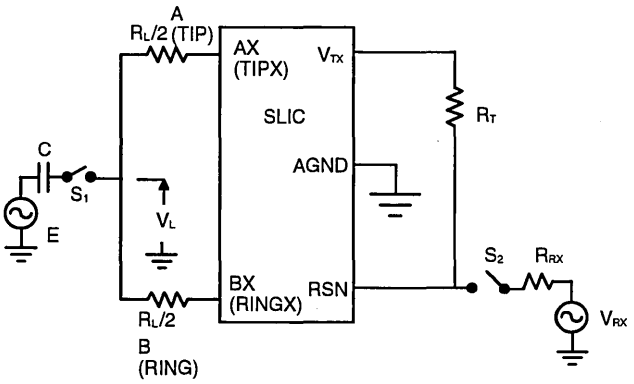
$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$

A. Two-to-Four Wire Insertion Loss



$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$ $BRS = 20 \log (V_{TX} / V_{RX})$

B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S_1 closed, S_2 open and $1/\omega C << R_L$:

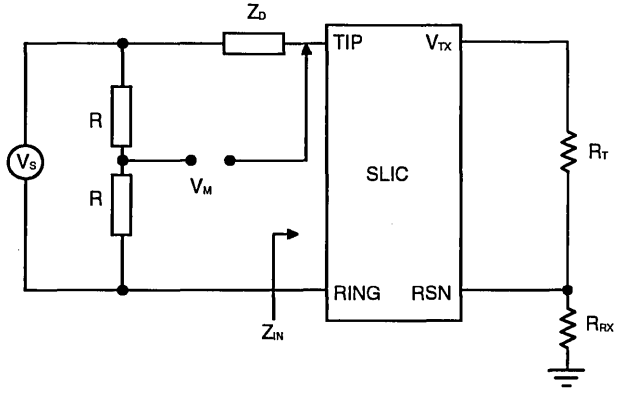
L-T Long. Bal. $= -20 \log \left(\frac{V_{AB}}{E}\right)$

L-4 Long. Rej. $= -20 \log \left(\frac{V_{TX}}{G_{TX} \cdot E}\right)$

S_2 closed, S_1 open:

4-L Long. Sig. Gen. $= -20 \log \left(\frac{V_L}{V_{RX}}\right)$

C. Longitudinal Balance (IEEE)



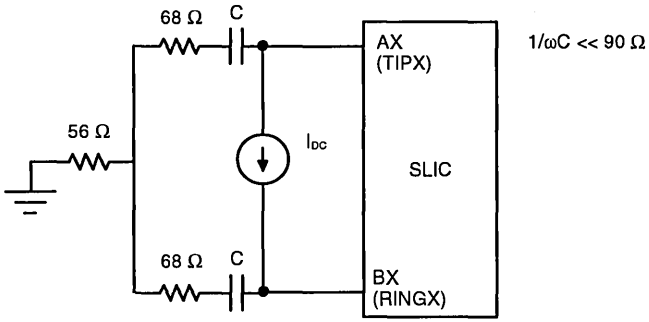
Z_D: The desired impedance; for example, the characteristic impedance of the line.

$R_L = 20 \log \left(\frac{2V_M}{V_S}\right)$

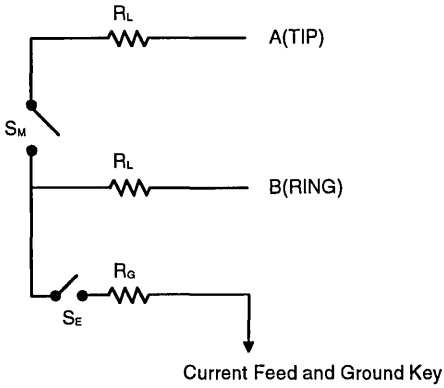
11701B–022

D. Two-Wire Return Loss Test Circuit

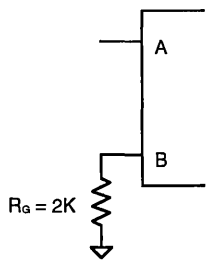
TEST CIRCUITS (continued)



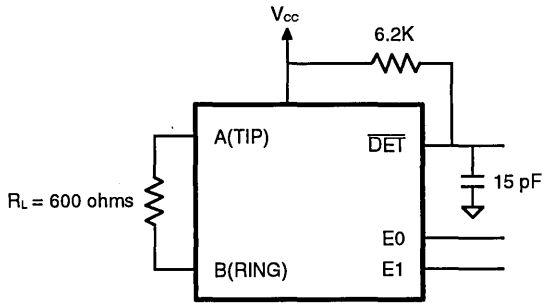
E. Single-Frequency Noise



F. Ground-Key Detection



G. Ground-Key Switching



15772A-017b

H. Loop Detector Switching

PRELIMINARY

Advanced Micro Devices

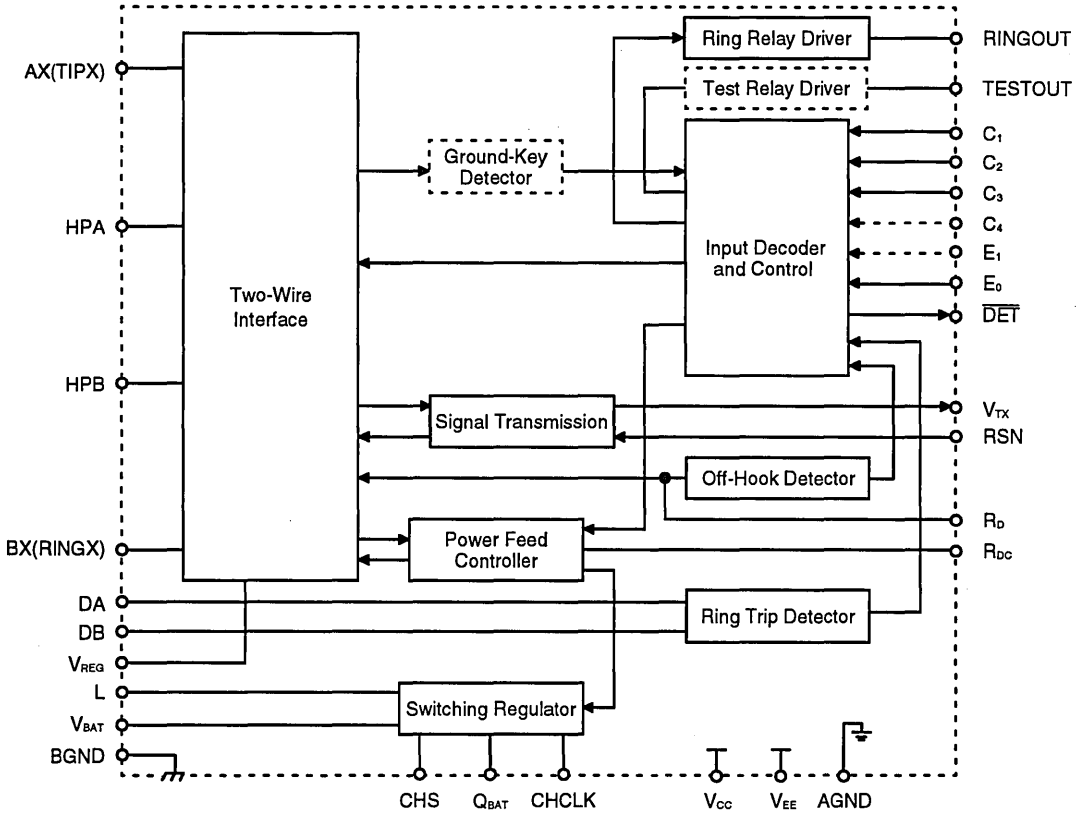
Am79M570/Am79M574

Metering Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Programmable constant resistance feed
- Programmable loop detect threshold
- Ground-key detect
- Low standby power
- Performs polarity reversal
- Line-feed characteristics independent of battery variations
- Test relay driver optional
- Supports 2.2-V RMS metering (12 and 16 kHz)
- On-chip switching regulator for low-power dissipation
- Two-wire impedance set by single external impedance
- Tip open state for ground start lines

BLOCK DIAGRAM



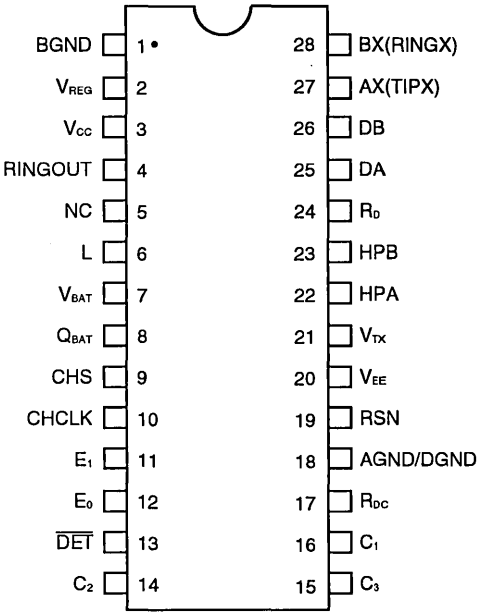
11701B-017

Notes: Am79M570—E_0 and E_1 inputs; ring relay driver sourced internally to BGND.
Am79M574—E_0 and E_1 inputs; ring and test relay drivers sourced internally to BGND.
Current gain (K_I) = 1000 for both parts.

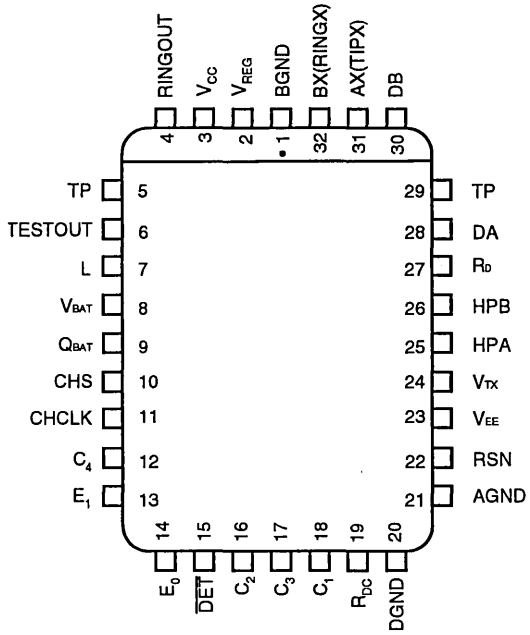
Publication #: 16857 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View

Am79M570



Am79M574

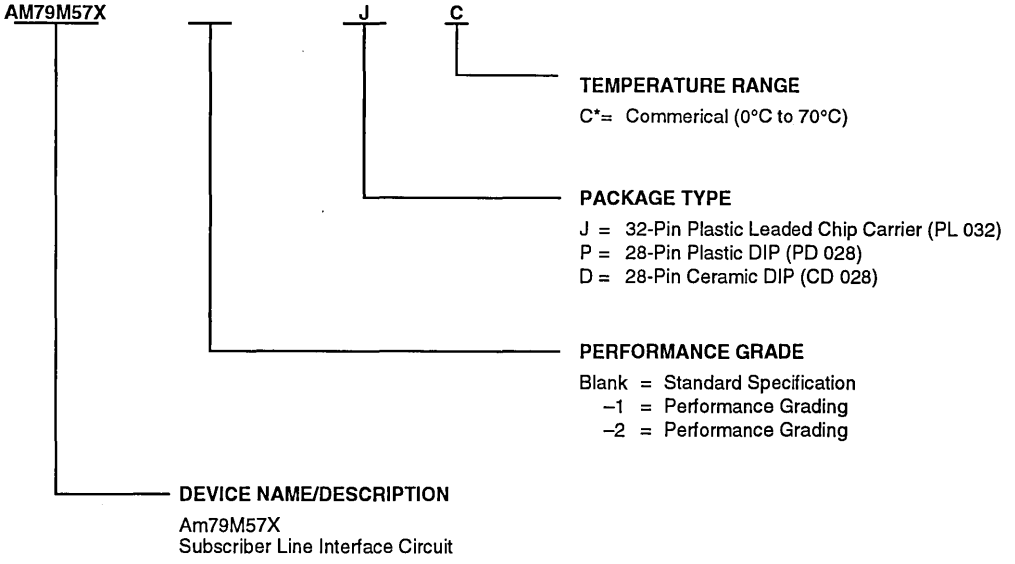


Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).
3. NC = No connect.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79M57X	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND

Ground (Am79M574)

Analog (Quiet) ground.

DGND

Ground (Am79M574)

Digital ground.

AGND/DGND

Ground (Am79M570)

Analog and digital ground are connected internally to a single pin.

AX(TIPX)

(Output)

Output of A(TIP) power amplifier.

BGND

Ground

Battery (power) ground.

BX(RINGX)

(Output)

Output of B(RING) power amplifier.

C_3–C_1

Decoder (Inputs)

TTL compatible. C_3 is MSB and C_1 is LSB.

C_4

Test Relay Driver Command (Input) (Am79M574)

TTL compatible. A logic Low enables the driver.

CHCLK

Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (nominal).

CHS

Chopper Stabilization (Input)

Connection for external stabilization components.

DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$

Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C_3–C_1, E_0, E_1). The output is open-collector with a built-in 15K pull-up resistor.

E_0

Read Enable (Input)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E_1

Ground-Key Enable (Input)

When E_0 is High, E_1 = High connects the ground-key detector to $\overline{DET}$, and E_1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L

Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}

Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed resistance programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT

Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

TESTOUT

Test Relay Driver (Output)
(Am79M574)

Sourcing from BGND with internal diode to Q_{BAT}.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, 2-wire impedance, and feed resistance all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

V_{BAT}

Connected to office battery supply through an external protection diode.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is 0.510 times the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E0, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –40 V to –63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS over operating range
(see Note 1)

Description	Test Conditions	Preliminary P.G.*	Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance				3		ohm
Analog (V_{TX}) Output Offset			–35		+35	mV
		–1	–30		+30	
Analog (RSN) Input Impedance (Note 5)	300 Hz to 3.4 kHz			1	20	ohm
Longitudinal Impedance at AX or BX					35	
Overload Level	four-wire		–3.1		+3.1	Vpk
Z_{2WIN} = 600 to 900 ohms (Note 2)	two-wire		–6.0		+6.0	
Transmission Performance, two-wire impedance						
Two-Wire Return Loss	300 Hz to 500 Hz		26			dB
(See Test Circuit D)	500 Hz to 2500 Hz		26			
(Notes 5, 14)	2500 Hz to 3400 Hz		20			
Longitudinal Balance (two-wire and four-wire, see Test Circuit C)						
R_L = 600 ohms, Longitudinal to Metallic	300 Hz to 3400 Hz		48			dB
L-T, L-4 (normalized to unity gain)		–1	52			
Longitudinal to Metallic L-T and	200 Hz to 1000 Hz	–2**	63	70		
L-4 (normalized to unity gain)	1000 Hz to 3400 Hz		58	70		
(for trimmed version consult factory)	200 Hz to 3400 Hz (Reverse Polarity		54			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		40			dB
	300 Hz to 800 Hz	–1	42			
Longitudinal Current Capability	Active State			25		mA
per Wire (Note 5)	Disable State			18		RMS
Insertion Loss (see Test Circuits A and B)						
Two-Wire to Four-Wire	V_{AB} = 0 dBm, 1 kHz		5.70	5.85	6.00	dB
		–1	5.75		5.95	
Four-Wire to Two-Wire	V_{RX} = 0 dBm, 1 kHz		–0.15		+0.15	dB
		–1	–0.1		+0.1	
Insertion Loss versus Frequency (see Test Circuits A and B)						
Two-Wire to Four-Wire or	300 Hz to 3400 Hz		–0.1		+0.1	dB
Four-Wire to Two-Wire	Relative to 1 kHz					
Gain Tracking (see Test Circuits A and B)						
Two-Wire to Four-Wire or	+7 dBm to –55 dBm		–0.1		+0.1	dB
Four-Wire to Two-Wire (Note 5)	Reference: 0 dBm					
Balance Return Signal (four-wire to four-wire, see Test Circuit B)						
Gain Accuracy (Note 3)	0 dBm, 1 kHz		–6.00	–5.85	–5.70	dB
		–1	–5.95		–5.75	
Variation with Frequency (Notes 3, 5)	300 Hz to 3400 Hz		–0.1		+0.1	dB
	Relative to 1 kHz					
Gain Tracking (Note 5)	+3 dBm to –55 dBm		–0.1		+0.1	dB
	Reference: 0 dBm					
Group Delay (Notes 5, 15)	F = 1 kHz			5.3		µs

*P.G. = Performance Grade
**All other performance parameters equivalent to –1 grade.
Normal Polarity only.

ELECTRICAL CHARACTERISTICS (continued)

Description		Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Total Harmonic Distortion		0 dBm, 300 Hz–3.4 kHz +9 dBm, 300 Hz–3.4 kHz			–64 –55	–50 –40	dB
Total Harmonic Distortion With /Metering		See Notes 5 and 11				–35	dB
Idle Channel Noise							
C-Message Weighted Noise (Notes 5, 7)		two-wire	–1		+7 +7	+15 +12	dBrnC
		four-wire	–1		+3 +3	+10 +7	dBrnC
Psophometric Weighted Noise (Note 7)		two-wire	–1		–83 –83	–75 –78	dBmp
		four-wire	–1		–87 –87	–80 –83	dBmp
Psophometric Idle Channel Noise with Metering (Notes 5 and 12)		two-wire four-wire				–46 –52	dBmp
Single Frequency Out-of-Band Noise (see Test Circuit E)							
Metallic	(Notes 4, 5, 9)	4 kHz to 9 kHz			–76		dBm
	(Notes 4, 5, 9)	9 kHz to 1 MHz			–76		
	(Notes 4, 5)	256 kHz and harmonics			–57		
Longitudinal	(Notes 4, 5, 9)	1 kHz to 15 kHz			–70		dBm
	(Notes 4, 5, 9)	Above 15 kHz			–85		
	(Notes 4, 5)	256 kHz and harmonics			–57		
Line Characteristics (see Figures 1a, 1b, 1c) Battery = –48 V, R_L = 600 and 900 ohms, R_{FEED} = 800 ohms							
Apparent Battery Voltage		Active Mode		47	50	53	V
Loop Current Accuracy		Active Mode		–7.5		+7.5	%
Loop Current—Tip Open		R_L = 600 ohms				1.0	
Loop Current—Open Circuit		R_L = 0 ohms				1.0	
Loop Current Limit Accuracy (Note 10)		Disable Mode Active Mode		–20		+20	%
Fault Current Limit, I_{LLIM} (I_{AX} + I_{BX})		AX and BX shorted to ground				130	mA
Power Dissipation Battery = –48 V, Normal Polarity							
On-Hook Open Circuit			–1		35 35	120 80	mW
On-Hook Disable Mode			–1		135 135	250 200	
On-Hook Active Mode			–1		200 200	400 300	
Off-Hook Disable Mode		R_L = 600 ohms			500	750	
Off-Hook Active Mode		R_L = 600 ohms			650	1000	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3.0	4.5	mA
	Disable Mode			6.0	10.0	
	Active Mode			7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.2	3.5	
	Active Mode			2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.0	5.0	
	Active Mode			4.0	6.0	
Power Supply Rejection Ratio (Vripple = 50 mV RMS)						
V_{CC} (Notes 6, 7)	50 Hz to 3400 Hz		25	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		22	35		dB
		–1	25	35		
V_{EE} (Notes 6, 7)	50 Hz to 3400 Hz		20	40		dB
		–1	25	40		
	3.4 kHz to 50 kHz		10	25		dB
		–1	10	25		
V_{BAT} (Notes 6, 7)	50 Hz to 3400 Hz		27	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		20	40		dB
		–1	25	40		
Off-Hook Detector						
Current Threshold Accuracy	I_{DET} = 365/R_D Nominal		–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V (see Test Circuit F)						
Ground-Key Resistance Threshold	B(Ring) to GND		2.0	5.0	10.0	Kohm
Ground-Key Current Threshold (Note 8)	B(Ring) to GND			9		mA
	Midpoint to GND			9		
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage (Note 13)	Source Resistance 0 to 2 Mohms		–50	0	+50	mV
Logic Inputs (C_1, C_2, C_3, C_4, E_0, E_1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4			mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

SWITCHING CHARACTERISTICS
Am79M570/Am79M574

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E_1 High to $\overline{DET}$ High ($E_0 = 1$) E_1 High to $\overline{DET}$ Low ($E_0 = 1$)	Ground-Key Detect Mode R_L Open, R_G Connected (see Test Circuit G)			3.8 1.1	µs
tshde	E_1 Low to $\overline{DET}$ Low ($E_0 = 1$) E_1 Low to $\overline{DET}$ High ($E_0 = 1$)				1.2 3.8	µs
tshdd	E_0 High to $\overline{DET}$ Low ($E_1 = 0$)	Switch Hook Detect Mode R_L = 600 ohms, R_G Open (see Test Circuit H)			1.1	µs
tshd0	E_0 Low to $\overline{DET}$ High ($E_1 = 0$)				3.8	
tgkdd	E_0 High to $\overline{DET}$ Low ($E_1 = 1$)				1.1	µs
tgkd0	E_0 Low to $\overline{DET}$ High ($E_1 = 1$)				3.8	

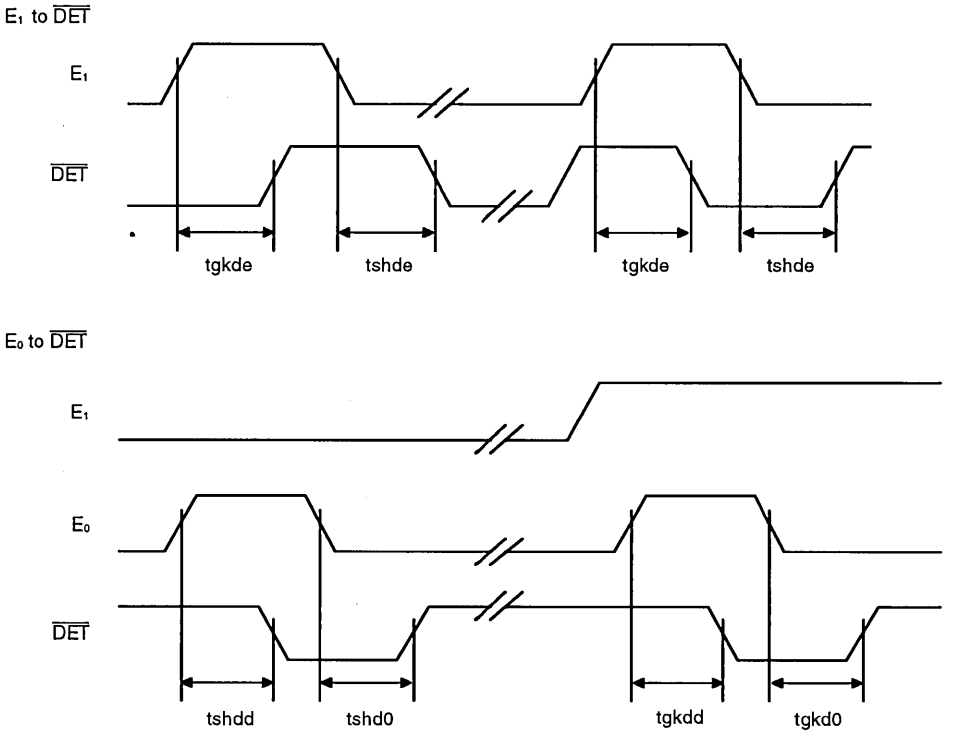
Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	$E_0 = 1$* $E_1 = 0$	$E_0 = 1$* $E_1 = 1$
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

*For the Am79M570 and Am79M574 logic Low on E_0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING WAVEFORMS

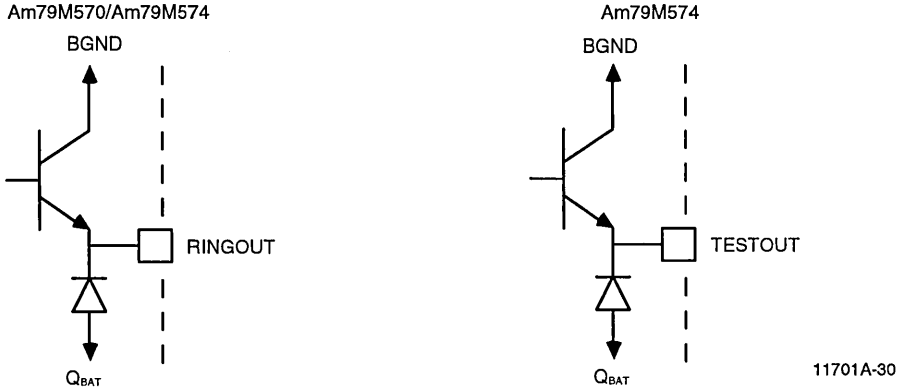
Am79M570/Am79M574



Note: All delays measured at 1.4-V level.

11701B–018

Relay Driver Specifications



Description	Test Conditions	Min	Typ	Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)					
On Voltage	50 mA Source	BGND –2	BGND – 0.95		V
Off Leakage			0.5	100	µA
Clamp Voltage	50 mA Sink	Q_{BAT} –2			V

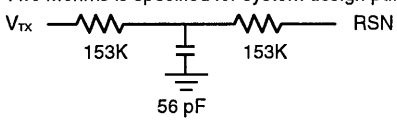
Notes:

1. Unless otherwise noted, test conditions are: Battery = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.22 µF, R_{DC1} = R_{DC2} = 20K, C_{DC} = 0.1 µF, R_d = 51.1K, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 306K resistive, receive input summing impedance (Z_{RX}) = 300K resistive. (See Table 2 for component formulas.)
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 17 V.
8. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from 256-kHz switch-regulator chopper are not included.
10. Loop-current limit which depends upon the programmed apparent open circuit voltage and the feed resistance is calculated as follows:

$$\text{In Disable mode: } I_{LIMIT} = 0.5 \frac{V_{apparent}}{R_{FEED}}$$

$$\text{In Active mode: } I_{LIMIT} = 0.8 \frac{V_{apparent}}{R_{FEED}}$$

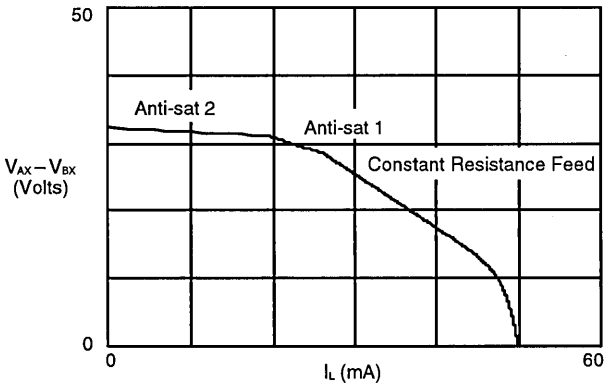
11. Total harmonic distortion with metering as specified with a metering signal of 2.2 VRMS at the two-wire output, and a transmit signal of +3 dBm or receive signal of –4 dBm. The transmit or receive signals are single-frequency inputs, and the distortion is measured as the highest in band harmonic at the two-wire or the four-wire output relative to the input signal.
12. Noise with metering is measured by applying a 2.2-VRMS metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire and four-wire outputs over a 200-ms time interval.
13. Tested with 0 ohms source impedance. Two Mohms is specified for system design purposes only.
14. Assumes the following Z_T network:



15. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 14. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 510(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{1000\ Z_T}{Z_T + 510\ (Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 50(R_{FEED} - 2R_F)$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$Z_M = \frac{V_{MG}}{V_{M2W}} \cdot \frac{K_1(\omega)\ Z_L \cdot Z_T}{Z_T + 0.51 \cdot K_1(\omega)\ (2R_F + Z_L)}$	Z_M is connected from V_{MG} (metering source) to the RSN pin, V_{M2W} is the desired magnitude of the metering signal at the two-wire output (usually 2.2 VRMS) and $K_1(\omega)$ is defined below. $K_1(\omega) = \frac{1000}{1 + j\omega\ (11.5 \cdot 10^{-9} + CX/2)\ (36 + Z_L + 2R_F)}$ where: CX = The values of the identical capacitors from AX and BX to ground $\omega = 2\pi \times$ metering frequency



$V_{BAT} = -47.3$ V
$R_{DC1} + R_{DC2} = R_{DC} = 40K$

Constant resistance feed region: $V_{AX-BX} = 50 - \frac{R_{DC}}{50} I_L$

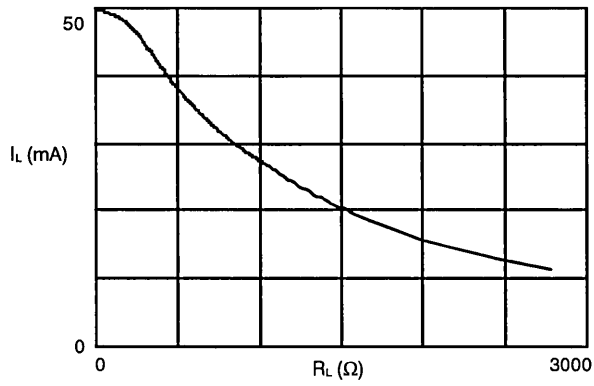
Anti-sat 1 region: $V_{AX-BX} = 39 - \frac{R_{DC}}{102.5} I_L$

Anti-sat 2 region: $V_{AX-BX} = 1.003 \mid V_{BAT} \mid - 15.3 - \left(.01 + \frac{R_{DC}}{834}\right) I_L$

See Figure 1c.

11701B–019

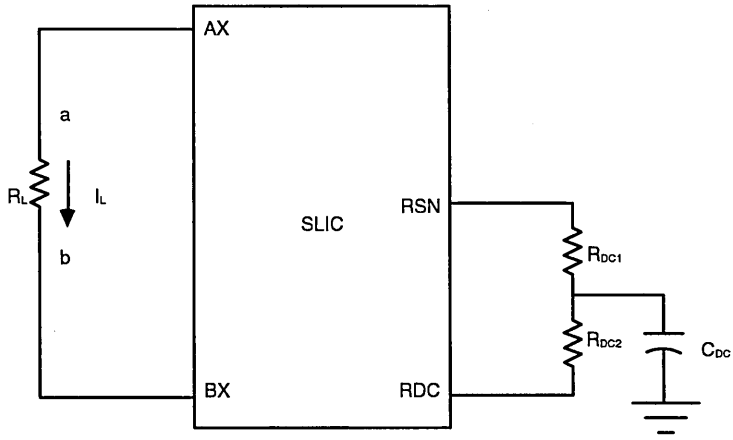
Figure 1a. Load Line (Typical)



Load Current vs Load Resistance
V_{BAT} = −47.3 V
R_{DC} = 40K
See Figure 1c.

11701B–020

Figure 1b. Feed Characteristics (Typical)

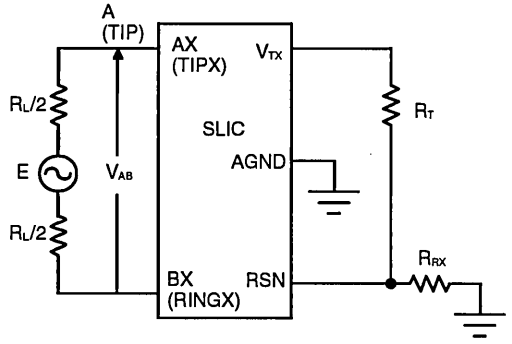


Feed resistance programmed by R_{DC1} and R_{DC2}.

11701B–021

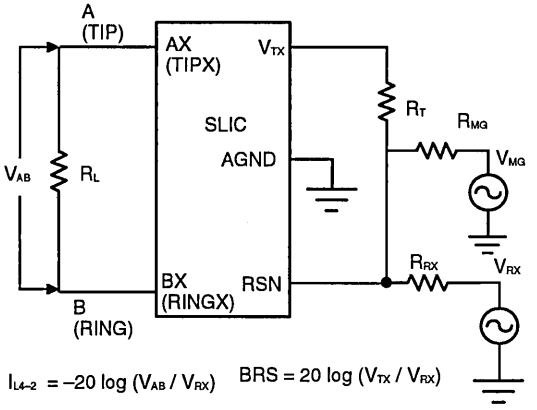
Figure 1c. Feed Programming

TEST CIRCUITS



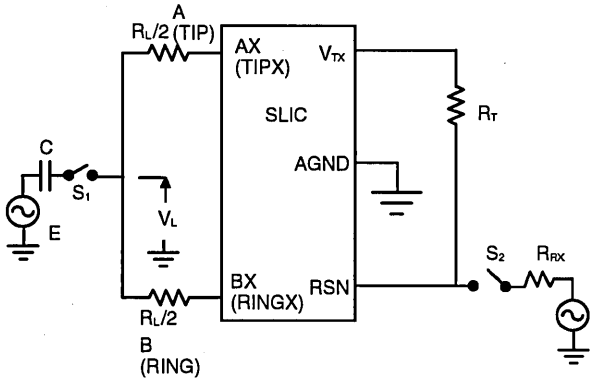
$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$

A. Two-to-Four Wire Insertion Loss



$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$ $BRS = 20 \log (V_{TX} / V_{RX})$

B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S_1 closed, S_2 open and $1/\omega C << R_L$:

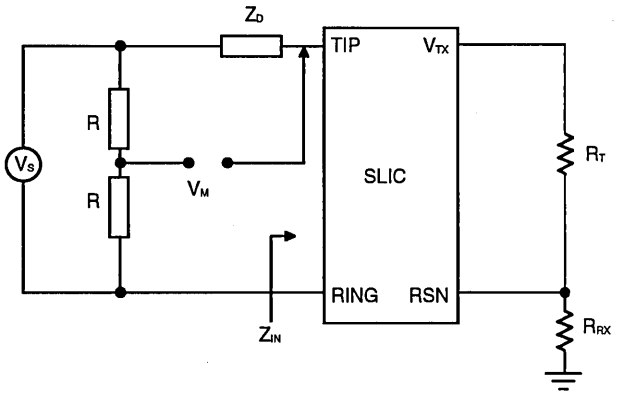
L-T Long. Bal. $= -20 \log \left(\frac{V_{AB}}{E}\right)$

L-4 Long. Rej. $= -20 \log \left(\frac{V_{TX}}{G_{TX} \cdot E}\right)$

S_2 closed, S_1 open:

4-L Long. Sig. Gen. $= -20 \log \left(\frac{V_L}{V_{RX}}\right)$

C. Longitudinal Balance (IEEE)



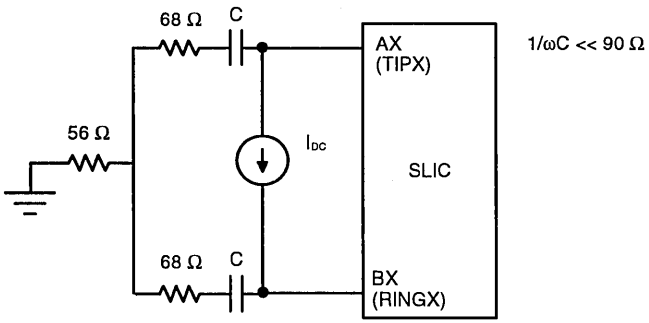
Z_D: The desired impedance; for example, the characteristic impedance of the line.

$R_L = 20 \log \left(\frac{2V_M}{V_S}\right)$

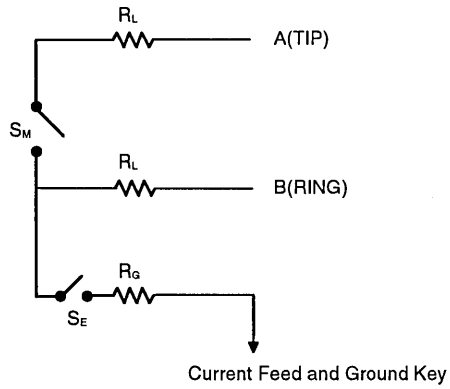
11701B–022

D. Two-Wire Return Loss Test Circuit

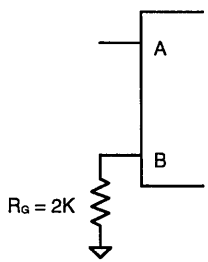
TEST CIRCUITS (continued)



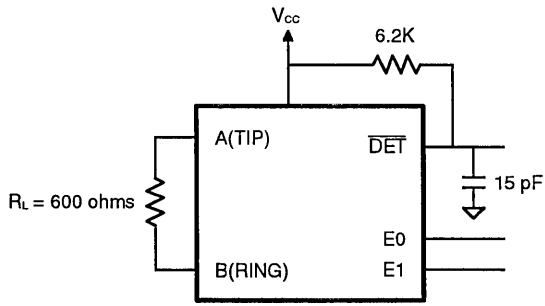
E. Single-Frequency Noise



F. Ground-Key Detection



G. Ground-Key Switching



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H. Loop Detector Switching

ADVANCE INFORMATION

Am79HM53

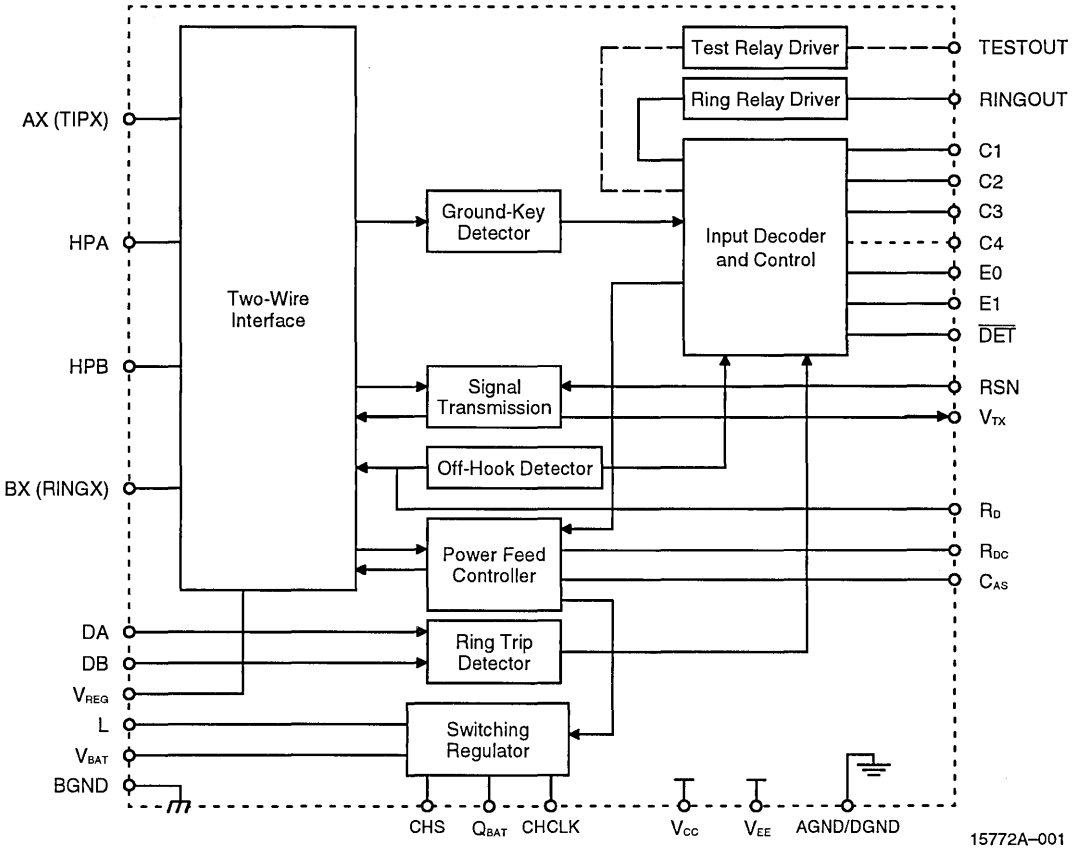
High-Level Metering Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Programmable loop detect threshold
- Ground-key detect
- Low standby power
- Performs polarity reversal
- Various ring and test relay driver combinations available
- Supports up to 5.1-V RMS metering (12 and 16 kHz)
- Line feed characteristics independent of battery variations
- On-chip switching regulator for low power dissipation
- Two-wire impedance set by single external impedance
- Tip open state for ground start lines
- Current gain = 200

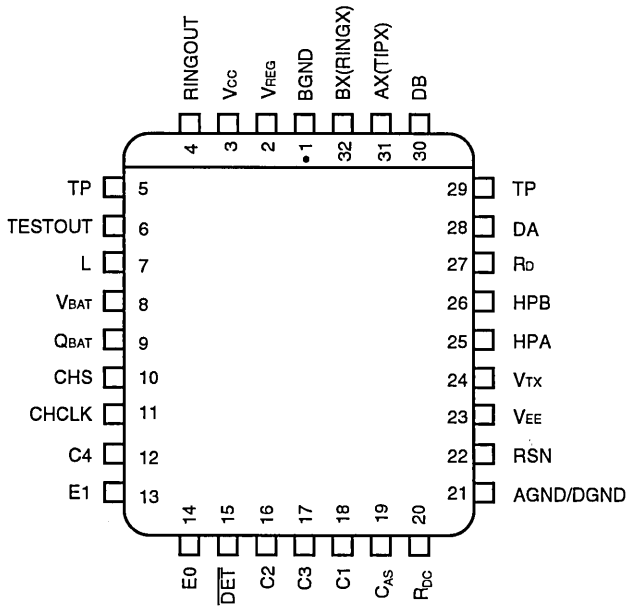
BLOCK DIAGRAM



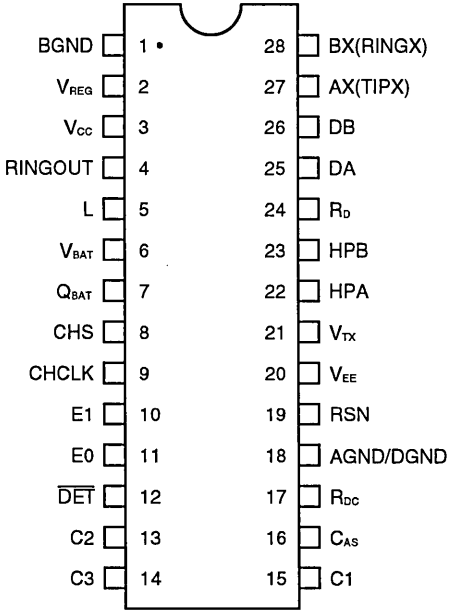
Publication #: 16814 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS

32-Pin Plastic Leaded Chip Carrier (PL 032)



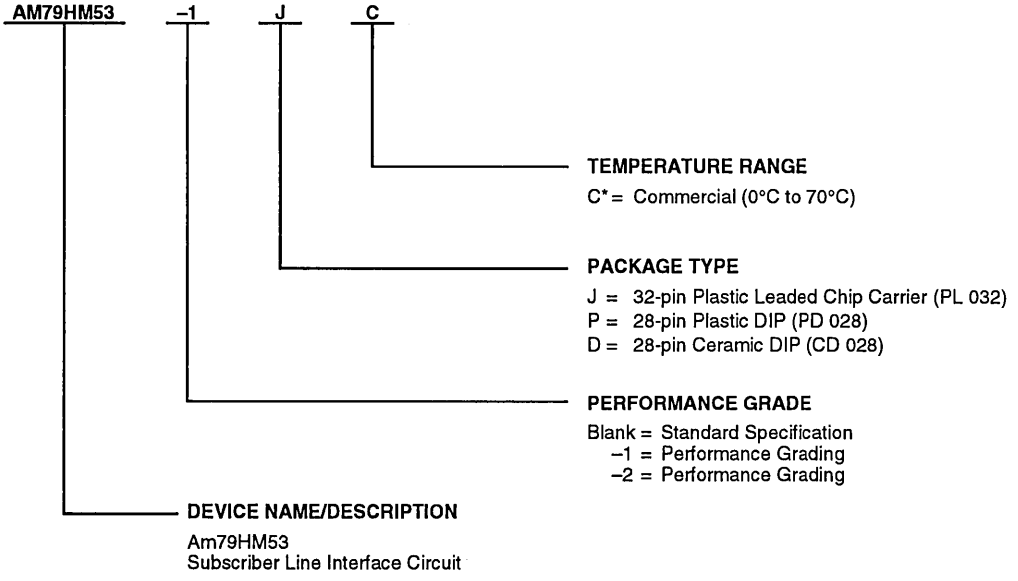
28-Pin Plastic DIP (PD 028) or 28-Pin Ceramic DIP (CD 028)



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

ORDERING INFORMATION
Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79HM53	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND/DGND
Ground

Analog and Digital ground.

AX (TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX (RINGX)
(Output)

Output of B(RING) power amplifier.

C3–C1
Decoder (Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

C4
Test Relay Driver Command (Input)

TTL compatible. A logic Low enables the driver.

CHCLK
Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (Nominal).

CHS
Chopper Stabilization (Input)

Connection for external chopper stabilizing components.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0, E1). The output is open-collector with a built-in, pull-up resistor.

E0
Read Enable (Input)

A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$.

E1
Ground-Key Enable (Input)

When E0 is High, E1 = High connects the ground-key detector to $\overline{\text{DET}}$, and E1 = Low connects the off-hook or ring trip detector to $\overline{\text{DET}}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L
Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 70 V of pulse waveform and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}
Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed current all connect to this node.

TESTOUT
Test Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}
Regulated Voltage (Input)

Provides negative power supply for power amplifiers. It also provides a connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}
Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

C_{AS}
Reference Filter Capacitor

A capacitor should be connected between this pin and AGND to filter internal reference voltages.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E0, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –54V to –63 V*

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

*Can be used without switching regulator components in this range of battery voltages provided maximum power dissipation specifications are not exceeded.

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS (see Note 1)

Description	Test Conditions	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Analog (V_{TX}) Output Impedance		5		3		ohm
Analog (V_{TX}) Output Offset			−35		+35	mV
Analog (RSN) Input Impedance	300 Hz to 3400 Hz	5		1	20	ohm
Longitudinal Impedance at AX or BX		5			35	ohm
Overload Level	four-wire	2	−3.2		+3.2	Vpk
Z_{2WIN} = 600–900 ohms	two-wire		−11.4		+11.4	
Transmission Performance, two-wire impedance (see Test Circuit D)						
Two-Wire Return Loss	300 Hz to 500 Hz	5, 11	26			dB
	500 Hz to 2500 Hz		26			
	2500 Hz to 3400 Hz		20			
Longitudinal Balance (Two-wire and Four-wire; see Test Circuit C)						
Longitudinal to Metallic L-T, L-4 (normalized to unify gain)	300 Hz to 3400 Hz		52	63		dB
Longitudinal Signal Generation 4–L	300 Hz to 800 Hz		40	56		dB
Longitudinal Current Capability	Active State	5		25		mA
per Wire	Disable State	5		18		RMS
Insertion Loss (see Test Circuits A and B)						
Two-wire to Four-wire	V_{AB} = 0 dBm, 1 kHz		10.85	11	11.15	dB
Four-wire to Two-wire	V_{AB} = 0 dBm, 1 kHz		−0.15		+0.15	dB
Insertion Loss vs Frequency (see Test Circuits A and B)						
Two-wire to Four-wire or Four-wire to Two-wire	300 Hz to 3400 Hz Relative to 1 kHz		−0.1		+0.1	dB
Gain Tracking (see Test Circuits A and B)						
Two-wire to Four-wire or Four-wire to Two-wire	+7 dBm to −55 dBm Reference: 0 dBm	5	−0.1		+0.1	dB
Balance Return Signal (Four-wire to Four-wire; see Test Circuit B)						
Gain Accuracy	0 dBm, 1 kHz	3	−10.85	−11	−11.15	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	3, 5	−0.1		+0.1	dB
Gain Tracking	+3 dBm to −55 dBm Reference: 0 dBm	5	−0.1		+0.1	dB
Group Delay	f = 1 kHz	5, 13		5.3		µs
Total Harmonic Distortion (Two-wire to Four-wire or Four-wire to Two-wire; see Test Circuits A and B)						
Without Metering	0 dBm, 300 Hz to 3400 Hz	9		−64	−50	dB
With Metering	0 dBm, 300 Hz to 3400 Hz	9, 5			−35	dB
Idle Channel Noise without Metering						
Psophometric Weighted Noise	two-wire				−80	dBmp
	four-wire				−87	
Psophometric Idle Channel	two-wire	5, 9,			−60	dBmp
Noise with Metering	four-wire	10			−70	

ELECTRICAL CHARACTERISTICS (continued)

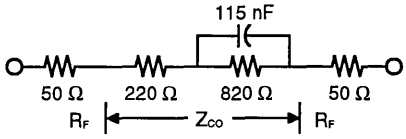
Description	Test Conditions	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Single Frequency Out-Of-Band Noise (see Test Circuit E)						
Metallic	4 kHz to 9 kHz	4, 5, 8		–76		dBm
	9 kHz to 1 MHz	4, 5, 8		–76		
	256 kHz and Harmonics	4, 5		–65		
Longitudinal	1 kHz to 15 kHz	4, 5, 8		–70		dBm
	Above 15 kHz	4, 5, 8		–85		
	256 kHz and Harmonics	4, 5		–57		
DC Feed Characteristics with 2×50 ohm Fuse Resistors (see Figures 1a, 1b, and 1c); Battery = –60 V						
Active Mode Loop Current Accuracy	I_{LOOP} (nominal) = 30 mA		–7.5		+7.5	%
Loop Current	R_L = 1800 ohms Battery = –54 V		19			mA
Disable Mode	R_L = 600 ohms		13.5	15	16.5	mA
Tip Open Mode	R_L = 600 ohms				1.0	mA
Disconnect Mode	R_L = 0 ohms				1.0	mA
Power Dissipation						
On-Hook Open Circuit Mode				50	120	mW
On-Hook Disable Mode				150	250	mW
On-Hook Active Mode				210	350	mW
Off-Hook Disable Mode	R_L = 600 ohms			620	850	mW
Off-Hook Active Mode	R_L = 600 ohms			1000	1200	mW
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3	4.5	mA
	Disable Mode			6	10	
	Active Mode			7.5	12	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.2	3.5	
	Active Mode			2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.0	5.0	
	Active Mode			4.0	6.0	
Power Supply Rejection Ratio (V_{RIPPLE} = 50-mV RMS)						
V_{CC}	200 Hz to 3400 Hz	6	20	40		dB
	3.4 kHz to 50 kHz		20	35		
V_{EE}	200 Hz to 3400 Hz	6	20	35		dB
	3.4 kHz to 50 kHz		10	25		
V_{BAT}	200 Hz to 3400 Hz	6	27	40		dB
	3.4 kHz to 50 kHz		20	40		
Effective Internal Resistance	C_{AS} pin to ground	5	85	170	255	Kohm
Off-Hook Detector						
Current Threshold Accuracy	$I_{DET} = 365/R_D$ (7.14 mA)		–20		+20	%

ELECTRICAL CHARACTERISTICS (continued)

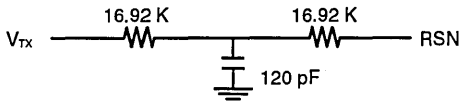
Description	Test Conditions	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Ground-Key Detector Thresholds (see Test Circuit F); Active Mode; Battery = –60 V						
Ground-Key Resistance Threshold	B(Ring) to ground		2.0	6	12.0	Kohm
Ground-Key Current Threshold	B(Ring) to ground and Midpoint to ground	7		9		mA
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage	Source Resistance = 0 to 2 Mohm	12	–50	0	+50	mV
Logic Inputs (C1, C2, C3, C4, E0, E1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4	–0.2		mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

Notes:

1. Unless otherwise noted, test conditions are: Battery = –60-V battery applied to V_{BAT} pin through a surge protection diode, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 8.33K, C_{DC} = 0.39 µF, R_d = 51.1K, no fuse resistors, two-wire AC output impedance programming impedance (Z_T) = 33.84K resistive, receive input summing impedance (Z_{RX}) = 59.9K resistive (see Table 2 for component formulas).
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the impedance programmed by Z_T.
4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.
5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
8. Fundamental and harmonics from 256-kHz switch regulator chopper are not included.
9. Total harmonic distortion and noise with 16-kHz metering is specified with the two-wire output (AX, BX) loaded with the impedance shown below with a 5.1-V RMS metering signal across Z_{CO} and a transmit signal of +0 dBm or receive signal of 0 dBm (600 ohms). The transmit or receive signals are single-frequency inputs, and the distortion is measured as the highest in-band harmonic at the two-wire or the four-wire output relative to the input signal.

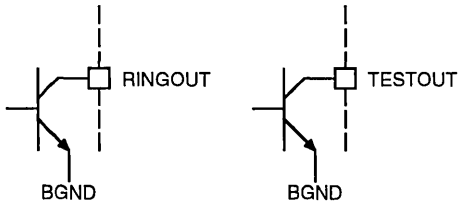


10. Noise with metering is measured by applying a 5.1-V RMS metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire and four-wire outputs over a 200-ms time interval.
11. Measured using the following Z_T network:



12. Tested with 0 ohms source impedance. Two Mohms is specified for system design purposes only.
13. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 11 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC devices.

RELAY DRIVER SPECIFICATIONS



Description	Test Conditions	Notes	Preliminary			Unit
			Min	Typ	Max	
Relay Driver Outputs (RINGOUT, TESTOUT)						
On Voltage	25-mA Sink				+1.5	V
On Voltage	50-mA Sink				+2.0	V
Off Leakage	V_{OH} = + 15 V		0.1		100	µA

RELAY DRIVER CHARACTERISTICS (Typical)

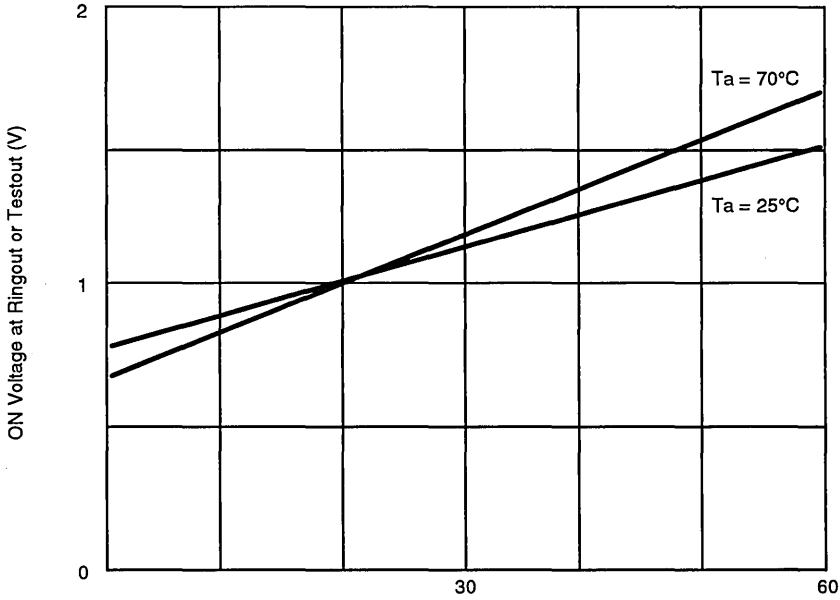


Table 1. SLIC Decoding

State	C3	C2	C1	Two-Wire Status	$\overline{DET}$ Output	
					E0 = 1*, E1 = 0	E0 = 1*, E1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

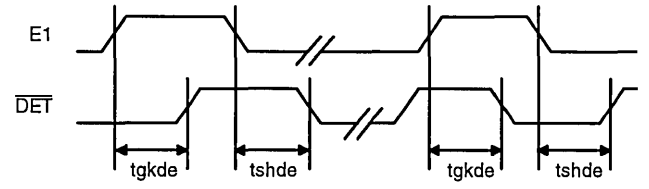
*A logic Low on E0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E1 High to $\overline{DET}$ High	Ground-Key Detect Mode	–	–	3.8	µs
	E1 High to $\overline{DET}$ Low	E0 = 1 (see Test Circuit H)	–	–	1.1	
tshde	E1 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.2	µs
	E1 Low to $\overline{DET}$ High	E0 = 1 (see Test Circuit G)	–	–	3.8	
tshdd	E0 High to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.1	µs
tshd0	E0 Low to $\overline{DET}$ High	E1 = 0 (see Test Circuit G)	–	–	3.8	
tgkdd	E0 High to $\overline{DET}$ Low	Switch Hook Detect Mode	–	–	1.1	µs
tgkd0	E0 Low to $\overline{DET}$ High	E1 = 1 (see Test Circuit G)	–	–	3.8	

SWITCHING WAVEFORMS

E1 to $\overline{DET}$



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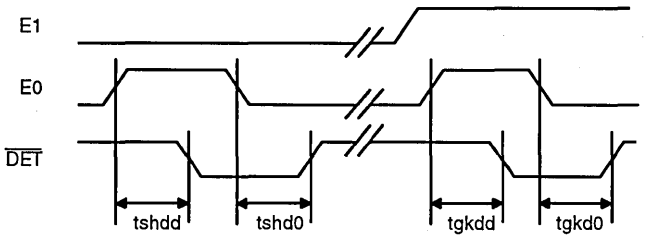
E0 to $\overline{DET}$



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Note: All delays measured at 1.4-V level.

Table 2. User-Programmable Components

$Z_T = 56.4\ (Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{200\ Z_T}{Z_T + 56.4\ (Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin, Z_T is defined above, and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 10(R_{FEED} - 2R_F)$ $C_{DC} = (1.5\ ms)\ \frac{R_{DC1} + R_{DC2}}{R_{DC1}\ R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$Z_M = \frac{V_{MG}}{V_{M2W}} \cdot \frac{K1\ (\omega)\ Z_L \cdot Z_T}{Z_T + 0.282 \cdot K1\ (\omega)\ (2R_F + Z_L)}$	Z_M is connected from V_{MG} (metering source) to the RSN pin, V_{M2W} is the desired magnitude of the metering signal at the two-wire output, and K1 (ω) is defined below.

$$K1\ (\omega) = \frac{200}{1 + j\omega\ (11.5 \cdot 10^{-9} + CX/2)\ (36 + Z_L + 2R_F)}$$

CX = The values of the identical capacitors from AX and BX to ground; $\omega = 2\pi \times$ metering frequency

$C_{AS} = 1/10^5 \pi fc$	C_{AS} is the regulator filter capacitor and fc is the desired filter cut-off frequency.

FEED CHARACTERISTICS (typical)

$R_{DC1} + R_{DC2} = R_{DC} = 16.67K$ (see Figure 1c); $R_{FA} = R_{FB} = 50$ ohms

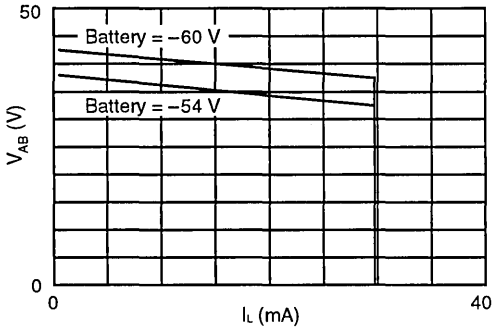


Figure 1a. V_{AB} vs I_L

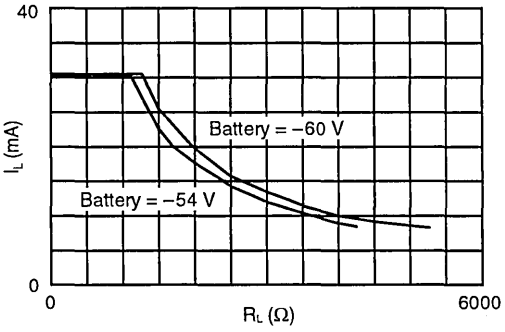
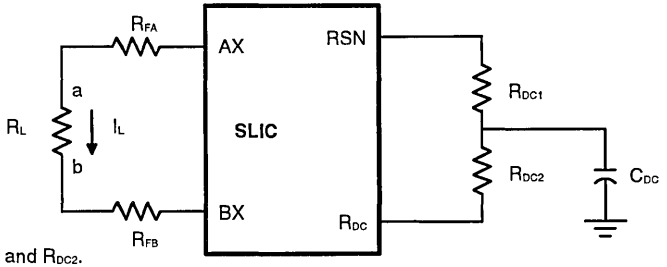


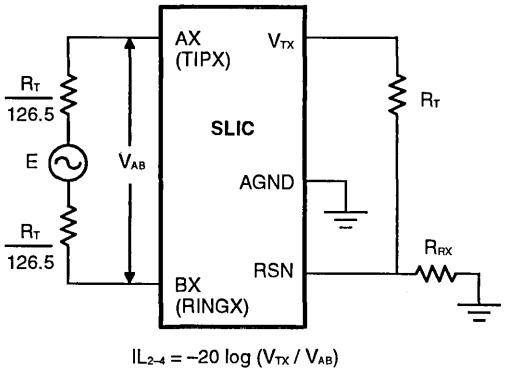
Figure 1b. I_L vs R_L



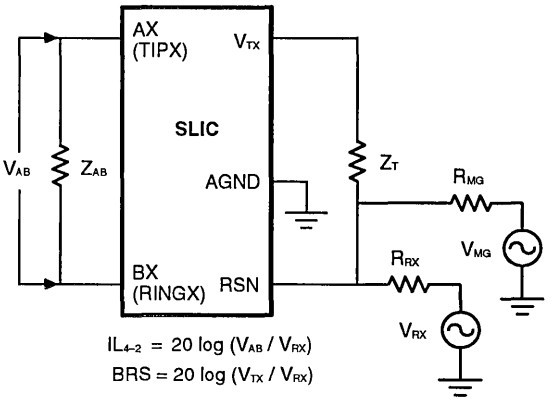
Current programmed by R_{DC1} and R_{DC2}.

Figure 1c. Feed Programming

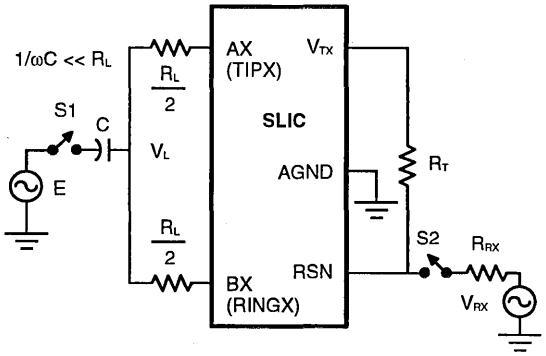
TEST CIRCUITS



A. Two-to-Four Wire Insertion Loss



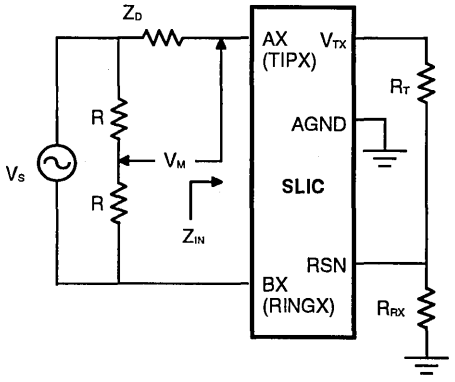
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 log (V_{AB}/E)
L-T Long. Rej. = 20 log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 log (V_L/V_{RX})

C. Longitudinal Balance (IEEE)

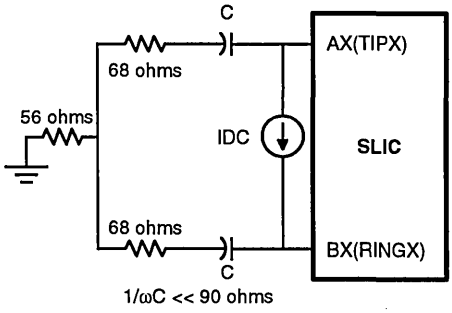


Z_D: The desired impedance (e.g., the characteristic impedance of the line).

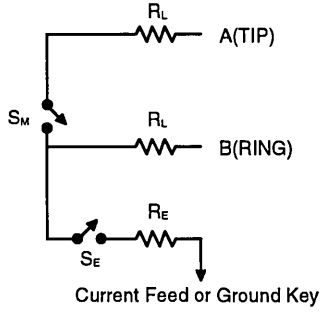
Return Loss = 20 log ($2V_M$/V_S)

D. Two-Wire Return Loss Test Circuit

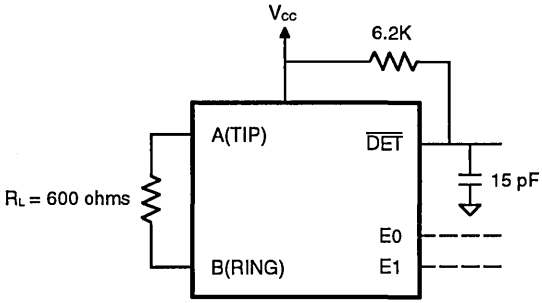
TEST CIRCUITS (continued)



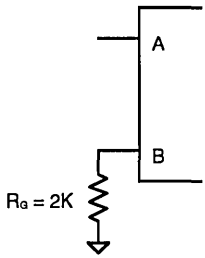
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching

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METERING SLIC PRODUCTS

Application Notes

The AMD Metering SLIC Family offers a high degree of versatility for applications in many types of line circuits. In this section, typical single-channel and multiple-channel applications are described.

Figure 1 shows a detailed schematic of a basic single-line system using one Am79M5XX series SLIC and one Am7901 or Am7905 SLAC IC or one-half of an Am79C02 DSLAC IC. The dashed connection lines in the schematic show the wiring of the various relay, $\overline{DET}$ enabling, and ground-key options available. The TESTOUT, C4, E0, or E1 pins may or may not be present, depending on the version used.

In the receive path, the SLAC IC processes digital PCM voice data into analog signals and inputs them to the SLIC RSN pin through resistor R_{RX}. In the transmit path, the analog output at the SLIC V_{TX} pin is processed by the SLAC IC and output in serial-digital format to the PCM interface. R_{RX} sets the receive gain, and R_T is used to synthesize the AC two-wire output impedance. Both R_T and R_{RX} can be complex, to achieve optimized parameters over the voice band.

The Metering Filter block represents an external 12- or 16-kHz low pass or notch filter to reduce the metering level in the transmit path, before it can overload the SLAC IC input. A suggested metering filter circuit, shown in Figure 2 is a notch filter centered at 12 or 16 kHz. This filter has enough attenuation at the metering frequency and does not require an additional cancellation circuit.

In the control path, when the line goes off-hook, the SLIC pulls its collector $\overline{DET}$ output down and enables the SLAC IC serial control data I/O pins, D_{IN} and D_{OUT} (see Figure 1). The microprocessor also recognizes the off-hook, and typically will send a response such as power up or ring relay disable back to the SLIC, via the SLAC IC D_{IN} pin and the C3–C1 data bus. The C4 line is addressed in the same manner, to enable or disable the test relay driver. The E0 and E1 pins are addressed directly by the microprocessor as shown.

SLIC monitor and control functions which can be performed using a microprocessor and the circuitry shown in Figure 1 include:

- During the disable state, inform the processor when an off-hook has occurred and send a power up command to the SLIC.
- Detect an off-hook during ringing and send a command to the SLIC to release the ring relay.
- Detect an on-hook condition during the power up and send a command to the SLIC to enter the disable state.
- Send a line polarity reverse command to the SLIC.
- Command the SLIC into the ground-key sense mode in versions with a ground-key sense enable pin, E1.
- Command the SLIC to energize the ring relay, KD.
- Command the SLIC to energize the test relay in versions with a test relay driver.

A block diagram describing a typical eight-line system is shown in Figure 4. In this application, the processor, through the linecard controller, writes or reads control data via pins D_{IN} and D_{OUT} by first pulling all of the SLIC E0 pins Low, which places all SLIC $\overline{DET}$ outputs in the open state. The microprocessor then takes control of the $\overline{DET}/\overline{CS}$ bus and enables the desired SLAC IC control I/O for reading and writing. In this manner, the microprocessor can control and monitor any one of the eight-line circuits independently.

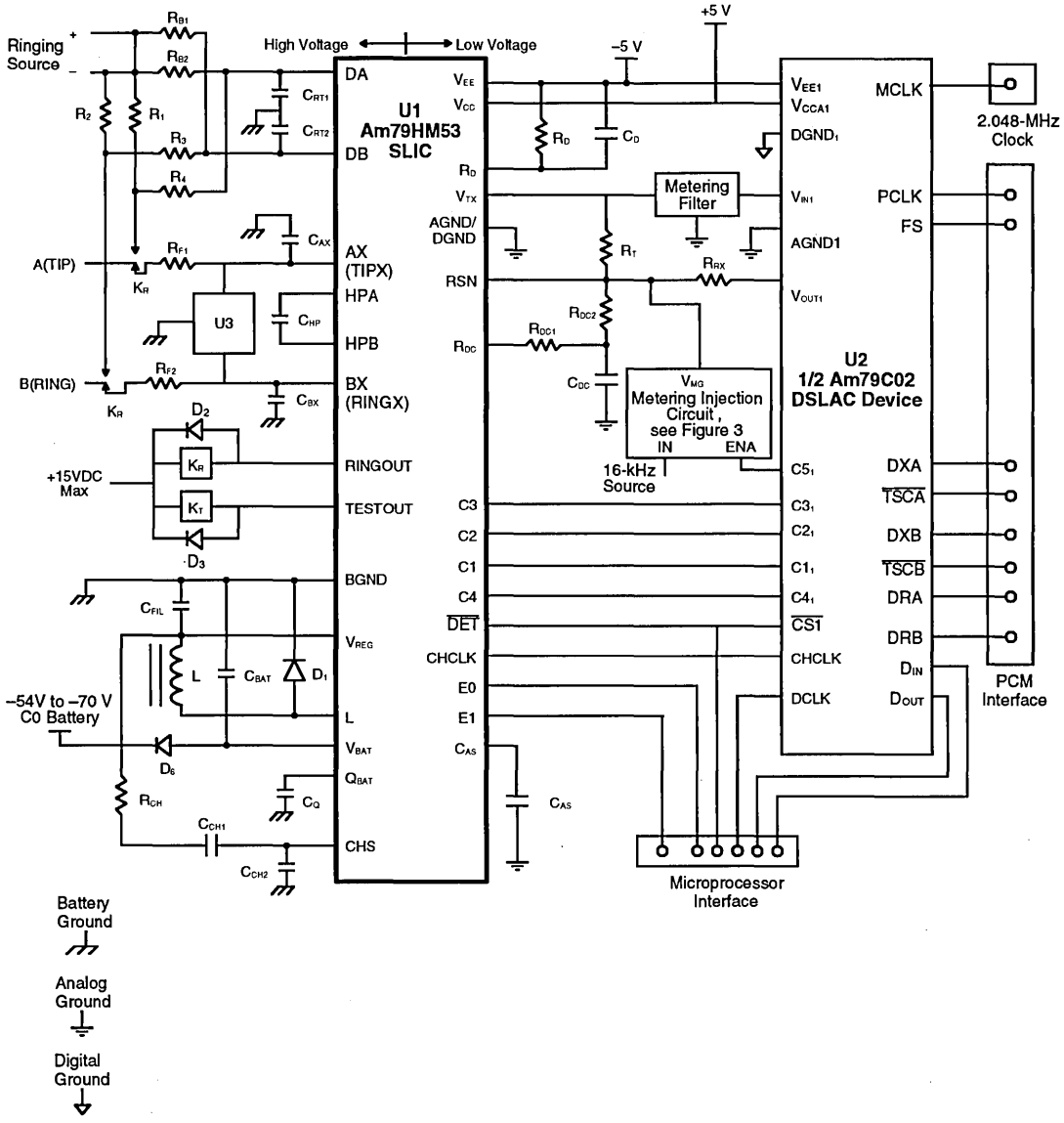


Figure 1. Single Channel of a Dual Channel Metering Subscriber Line Circuit

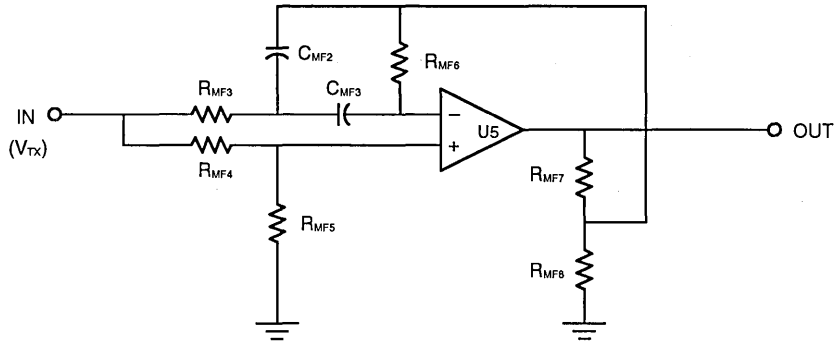


Figure 2. 16-kHz Metering Notch Filter

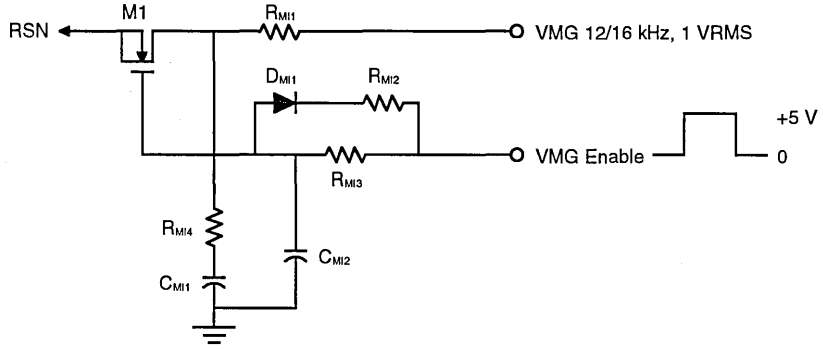
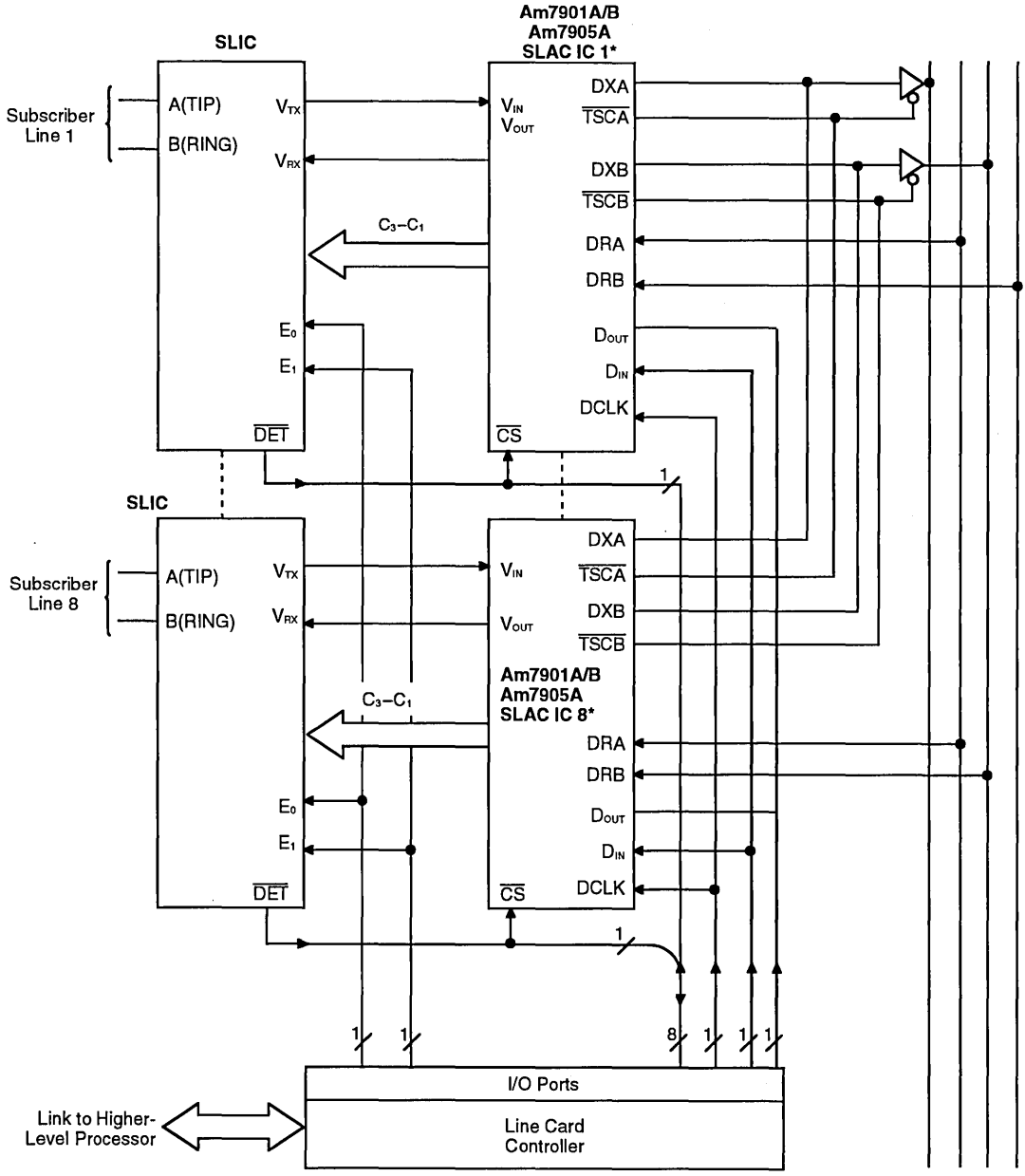


Figure 3. Metering Injection Circuit



*1/2 of an Am79C02 DSLAC IC per line can be used.
Note: Am7905A combines D_{IN} and D_{OUT} into a single pin called D_{IO}.

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Figure 4. AMD Subscriber Line System Eight-Channel Line Card

Table 1. Parts List — 1/2 of a Dual Channel Metering Subscriber Line System (See Figure 1 for Circuit)

U1	Am79MXXX or Am79HM53 SLIC
U2	Am79C02 DSLAC Device
K_R, K_T	Relay, 60-V coil, 2C contacts, 1500-V rating
L	Inductor, 1 mH, 5%
D_1	Diode, 100 V, 100 mA, 4 ns
U_3	Dual transient suppressor, Texas Instruments TISP1082A
D_6, D_2, D_3	Diode 100 V, 100 mA, 10 ns
RF_1, RF_2 (Am79HM53)	Resistor, fuse, 50 ohms
RF_1, RF_2 (Am79M53X/57X)	Resistor, fuse, 20 ohms
R_1, R_2	Resistor, 400 ohms, 3%, 3 W (Ring Feed resistors)*
RB_1, RB_2	Resistor, 249K, 1%, 1/4 W
R_3, R_4	Resistor, 205K, 1%, 1/2 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W
R_D	Resistor, 51.1K, 1%, 1/4 W (sets off-hook threshold)*
R_T (Am79M53X/57X)	Resistor, 286K, 1%, 1/4 W (sets two-wire impedance)*
R_T (Am79HM53)	Resistor, 30.1K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX} (Am79M53X/57X)	Resistor, 560K, 1%, 1/4 W (sets receive gain)*
R_{RX} (Am79HM53)	Resistor, 140K, 1%, 1/4 W (sets receive gain)*
R_{DC1}, R_{DC2} (Am79M53X)	Resistor, 31.25K, 1%, 1/4 W (sets 40 mA loop current)*
R_{DC1}, R_{DC2} (Am79M57X)	Resistor, 20K, 1%, 1/4 W (sets 40 mA loop current)*
R_{DC1}, R_{DC2} (Am79HM53)	Resistor, 8.33K, 1%, 1/4 W (sets 30 mA loop current)*
C_{RT1}, C_{RT2}	Capacitor, 0.43 µF, 20%, 100 V (replace C_{RT1} and C_{RT2} by a single 0.43 µF capacitor for balanced ringing)
C_{DC} (Am79M53X/M57X)	Capacitor 0.1 µF, 20%, 10 V
C_{DC} (Am79HM53)	Capacitor 0.39 µF, 20%, 10 V
C_{HP}	Capacitor, 0.33 µF, 20%, 100 V
C_{AS}	Capacitor, 0.47 µF, 20%, 100 V
C_{AX}, C_{BX} (Am79M53X/57X)	Capacitor, 2.2 pF, 20%, 100 V
C_{AX}, C_{BX} (Am79HM53)	Capacitor, 39 nF, 10%, 100 V
C_{FIL}	Capacitor, 0.47 µF, 10%, 100 V, Metallized Polyester
C_{BAT}	Capacitor, 0.47 µF, 20%, 100 V
C_Q	Capacitor, 0.33 µF, 20%, 100 V
C_{CH1}	Capacitor, 0.015 µF, 10%, 50 V, X7R ceramic
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic
C_D	Capacitor, 0.01 µF, 20%, 10 V (sets off-hook filtering)*

Note:The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.

Table 2. Parts List for Am79M53X/Am79M57X Metering Notch Filter

	FNOTCH		
	12 kHz	16 kHz	
R_{MF3} Resistor	5.07K	4.0K	1%, 1/4 W*
R_{MF4} Resistor	5.39K	5.58K	1%, 1/4 W*
R_{MF5} Resistor	22.0K	22.0K	1%, 1/4 W*
R_{MF6} Resistor	37.9K	27.9K	1%, 1/4 W*
R_{MF7} Resistor	2.17K	2.25K	1%, 1/4 W*
R_{MF8} Resistor	8.84K	8.84K	1%, 1/4 W*
C_{MF2} Capacitor	1.0 nF	1.0 nF	5%, 10 V*
C_{MF3} Capacitor	1.0 nF	1.0 nF	5%, 10 V*

Table 3. Parts List for 16 kHz Metering Notch Filter for Am79HM53 (See Figure 2 for Circuit)

U5	Operational amplifier, μA 741 or equivalent
R_{MF3}	Resistor, 7.32K, 1%, 1/4 W*
R_{MF4}	Resistor, 8.91K, 1%, 1/4 W*
R_{MF5}	Resistor, 22.0K, 1%, 1/4 W*
R_{MF6}	Resistor, 22.1K, 1%, 1/4 W*
R_{MF7}	Resistor, 35.1K, 1%, 1/4 W*
R_{MF8}	Resistor, 8.8K, 1%, 1/4 W*
C_{MF2}, C_{MF3}	Capacitor, 1 nf, 5%, COG, 10 V*

Table 4. Parts List for Metering Injection Circuit (See Figure 3 for Circuit)

R_{MI1} (5.1 V metering)	Resistor, 3.62K, 1%, 1/4 W*
R_{MI1} (2.2 V metering)	Resistor, 8.33K, 1%, 1/4 W*
R_{MI2}	Resistor, 200K, 1%, 1/4 W*
R_{MI3}	Resistor, 300K, 1%, 1/4 W*
R_{MI4}	Resistor, 300 Ω, 1%, 1/4 W*
C_{MI1}	Capacitor, 220 nF, 10%, 10 V*
C_{MI2} (16 kHz metering)	Capacitor, 39 nF, 10%, 10 V*
C_{MI2} (12 kHZ metering)	Capacitor, 51 nF, 10%, 10 V*
M1	N Channel MOS transistor, 3N169 or equivalent
D_{MI1}	Diode, 100 V, 100 mA, 10 ns

Note: The parts marked by an asterisk (*) are user programmable. The values shown can be altered to suit the application.

SLIC Extended Temperature and Packaging Considerations

SLIC Extended Temperature Supplement

AMD's SLIC products have been characterized over the –40° to +85°C. extended temperature range to establish their suitability for applications such as Remote Concentrators, Digital Loop Carriers, Fiber-In-The-Loop and other applications that may be subjected to temperature extremes. The –2 performance grade SLICs were found to be fully functional over this extended temperature range and are recommended for such applications.

Characterization has indicated that a few specifications of the SLICs tested for operation between 0° and 70°C. may vary beyond data sheet limits. This document identifies those specifications and their expected limits in the temperature ranges beyond 0°C to 70°C. It also addresses other issues associated with extended temperature operation such as recommended conditions for use of SLICs packaged in plastic and system design guidelines.

Note that the specifications in this supplement have been determined through characterization to apply to AMD's standard commercial grade product. If specifications over the –40° to +85°C range or another extended temperature range must be guaranteed, and tested at the temperature extremes, the customer is asked to contact an AMD representative for more information.

SLIC Family Extended Temperature Information

SLIC Electrical Characteristics	Test Conditions	Commerical Specification 0°C to +70°C	Extended Specification –40°C to +85°C	Unit
Analog (V_{TX}) Output Offset		+/– 30	+/– 35	mV
Longitudinal Balance (Two-wire and Four-wire, see Test Circuit C)				
Longitudinal to Metallic L-T, L-4, RL = 740 ohm	200 Hz to 1000 Hz, Normal Polarity	63 min	58 min	dB
Insertion Loss (Two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)				
Gain Accuracy	0 dBm, 1 kHz	+/– 0.1	+/– 0.15	dB
Variation with frequency	300 to 3400 Hz relative to 1 kHz	+/– 0.1	+/– 0.15	dB
Gain Tracking	+7 dBm to –55 dBm reference: 0 dBm	+/– 0.1	+/– 0.15	dB
Balance Return Signal (Four-wire to Four-wire, see Test Circuit B)				
Gain Accuracy	0 dBm, 1 kHz	+/– 0.1	+/– 0.15	dB
Variation with frequency	300 to 3400 Hz relative to 1 kHz	+/– 0.1	+/– 0.15	dB
Gain Tracking	+7 dBm to –55 dBm reference: 0 dBm	+/– 0.1	+/– 0.15	dB

SLIC Switching Characteristics

Symbol	Parameter	Test Conditions	Commerical Specification 0°C to +70°C	Extended Specification –40°C to +85°C	Unit
tgkde	E1 High to $\overline{DET}$ High	Ground-Key Detect Mode	3.8 Max	4.0 Max	µs
	E1 High to $\overline{DET}$ Low	E0 = 1 (see Test Circuit G)	1.1 Max	1.6 Max	
tshde	E1 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	1.2 Max	1.7 Max	µs
	E1 Low to $\overline{DET}$ High	E0 = 1 (see Test Circuit H)	3.8 Max	4.0 Max	
tshdd	E0 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	1.1 Max	1.6 Max	µs
tshd0	E0 Low to $\overline{DET}$ High	E1 = 0 (see Test Circuit H)	3.8 Max	4.0 Max	
tgkdd	E0 Low to $\overline{DET}$ Low	Switch Hook Detect Mode	1.1 Max	1.6 Max	µs
tgkd0	E0 Low to $\overline{DET}$ High	E1 = 1 (see Test Circuit H)	3.8 Max	4.0 Max	

Note: The above specifications apply to the –2 SLIC performance grade for all AMD SLIC types.

Publication #: 16193 Rev. A Amendment /0
Issue Date: May 1992

SLIC Packaging Considerations

Due to the effect of temperature on semiconductor reliability and the high voltage nature of the SLIC's function, power dissipation levels, package types, and the temperature of the die resulting from those two factors should be considered when designing with the SLIC. Thermal shutdown circuitry is incorporated into the SLIC that will suspend the chip's operation at a junction temperature of ~165°C. Operation for short periods at a junction temperature of up to 145°C should not be a problem. However, over extended periods, the SLIC's die temperature should be kept under 130°C.

Since thermal resistance characteristics of different package types vary, some packages may be inappropriate for a particular application depending upon the ambient temperature range required and the power dissipated by the SLIC. The following analysis is provided to help identify appropriate packages for use based upon the maximum power dissipation expected in both commercial and extended temperature applications.

The table below is based upon a maximum allowable junction temperature of 145°C. 145°C is used as the design guideline in this analysis rather than 130°C because the worst case power dissipation is determined under short circuit current conditions which are expected to be temporary. Normal operation of a SLIC circuit will include a load of at least several hundred ohms which will substantially reduce the SLIC's power dissipation compared to worst case. If the above recommendations are followed, the SLIC's junction temperature under normal operating conditions should be below 130°C.

The letters following the power dissipation numbers on the chart refer to the graphs on the following pages. The horizontal lines on the graph for a particular SLIC refer to the maximum power dissipation recommended for the packages offered as shown above. The curves indicates the maximum SLIC power dissipation expected for different values of RDC. After RDC is selected for your application, the charts should allow you to easily determine which package types are acceptable.

The worst case power dissipation of a current feed SLIC may be determined by the short circuit current limit set by the value of RDC. The charts indicate the worst case power dissipation expected for AMD's current feed SLICs relative to the value chosen for RDC, assuming two fuse resistors between 0 ohm and 100 ohm (2 x 50 ohm) and a TIP to RING short circuit. The lower curve in each chart represents the power dissipation with 50 ohm fuse resistors and the upper curve with 0 ohm fuse resistors. Also shown on the charts are the recommended maximum power dissipation levels for various packages. Plastic packaging should be appropriate for most current feed SLICs even over the extended temperature range since the short circuit current limit is typically set for 30 mA or less.

In the special case of the Am7943 SLIC due to its power management circuitry, worst case power dissipation occurs with a TIP to RING short circuit only when the external power management resistor is not used. When the recommended resistor is used (1700 ohm), the conditions for worst case power dissipation will vary depending on the value of the loop resistance as well as RDC. Power dissipation curves for the Am7943 are shown versus RDC for several different values of loop resistance.

The worst case power dissipation of a voltage feed SLIC may also be determined by the value of RDC, in this case the programmed feed resistance, making the same fuse resistor assumptions as above and a TIP to RING short circuit. The charts below indicate this worst case power dissipation relative to the value chosen for RDC for the three different types of voltage feed SLICs: the Am7957X Family, the Am79M57X Family, and the Am7958.

For example, the Am7958 is designed to meet all LSSGR requirements for North American Central Office applications, including a long loop battery feed requirement of 20 mA into 1900 ohm.

In order to accomplish this in a typical application, assuming 50 ohm fuse resistors, RDC would be set at ~4Kohm. The Am7958 power dissipation chart indicates that an RDC of 4 Kohm implies a maximum power dissipation of 1.13 W. Since 1.13 W is at the line indicating that plastic DIP is acceptable for the commercial temperature range but above the line for extended temperature, plastic DIP should be an acceptable package for commercial range applications but ceramic DIP would be recommended for extended temperature.

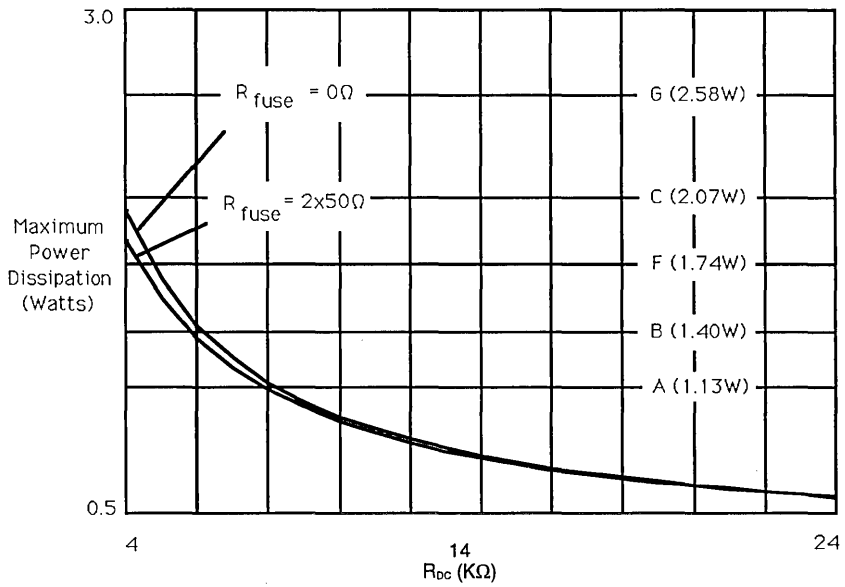
Package Type	Theta J/A	Maximum SLIC power Dissipation for +85°C ambient	Maximum SLIC power dissipation for +70°C ambient
28-Pin Plastic DIP	53° C/W	1.13 W (A)	1.4 W (B)
32-Pin PLCC	43° C/W	1.4 W (B)	1.74 W (F)
28-Pin Ceramic DIP	29° C/W	2.07 W (C)	2.58 W (G)
22-Pin Plastic DIP	60° C/W est	1 W (D)	1.25 W (H)
22-Pin Ceramic DIP	50° C/W est	1.2 W (E)	1.5 W (I)

Key for Charts
Maximum Power Dissipation

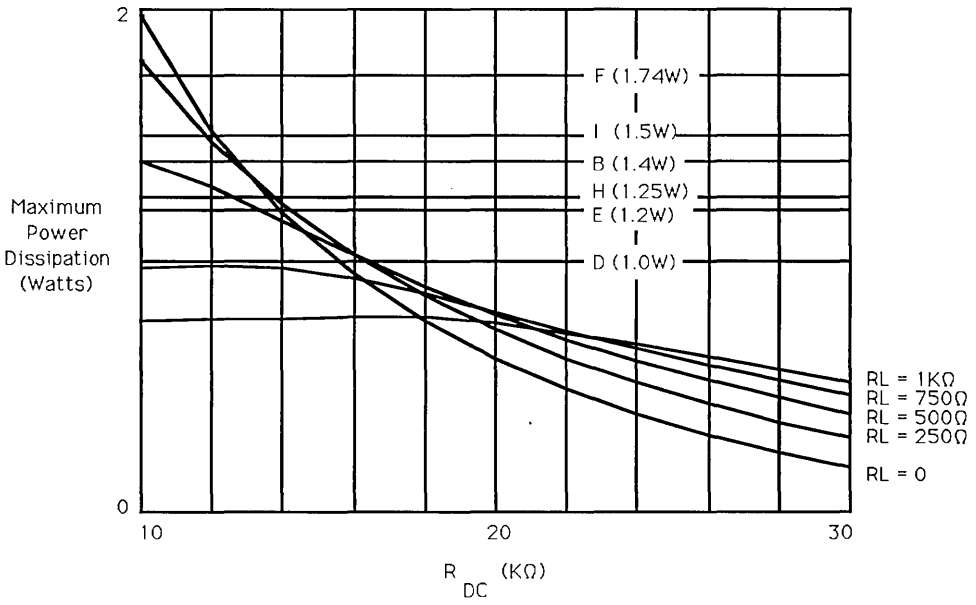
Symbol on Chart	Package Type	Temp Range
A	28-Pin Plastic DIP	Extended
B	32-Pin PLCC	Extended
	28-Pin Plastic DIP	Commerical
C	28-Pin Ceramic DIP	Extended
D	22-Pin Plastic DIP	Extended
E	22-Pin Ceramic DIP	Extended
F	32-Pin PLCC	Commercial
G	28-Pin Ceramic DIP	Commercial
H	22-Pin Plastic DIP	Commercial
I	22-Pin Ceramic DIP	Commercial

Note: The worst case power dissipation analysis does not apply to fault conditions where TIP and RING are shorted to Battery or Ground.

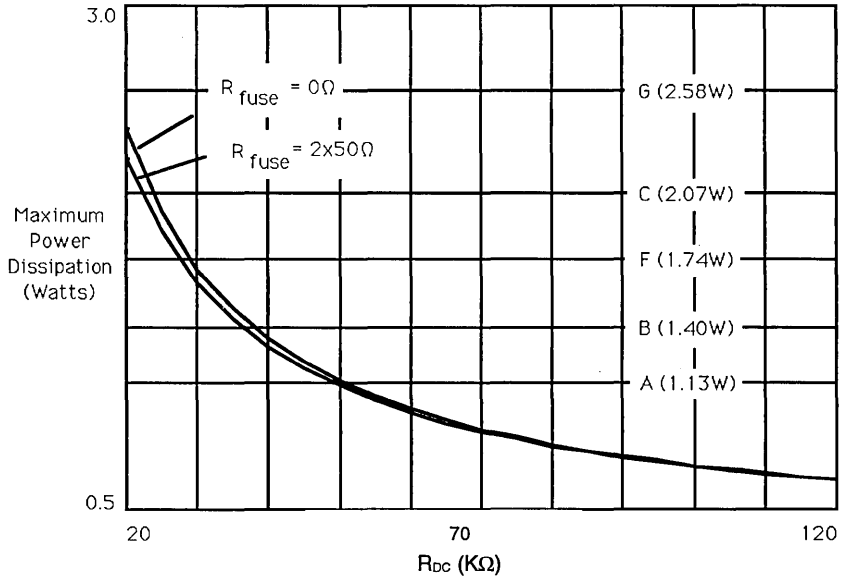
Am7942



Am7943



Am7953



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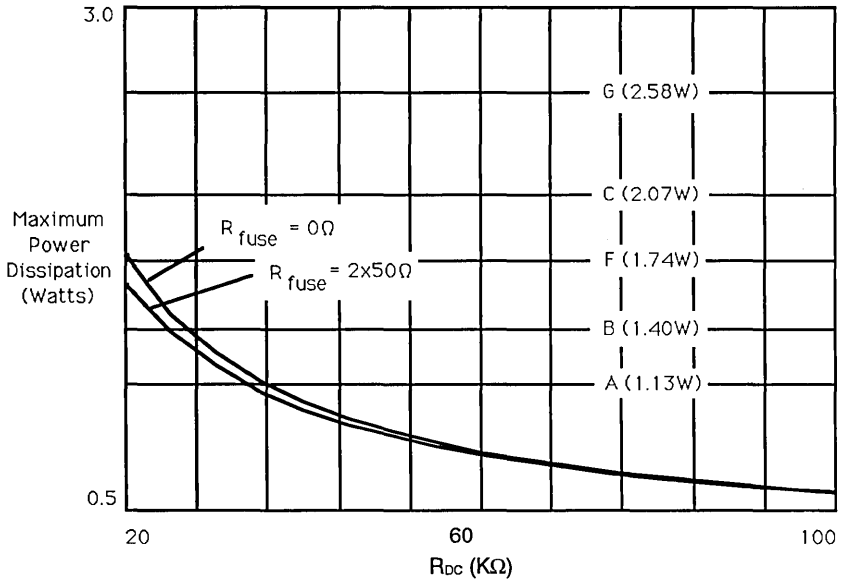
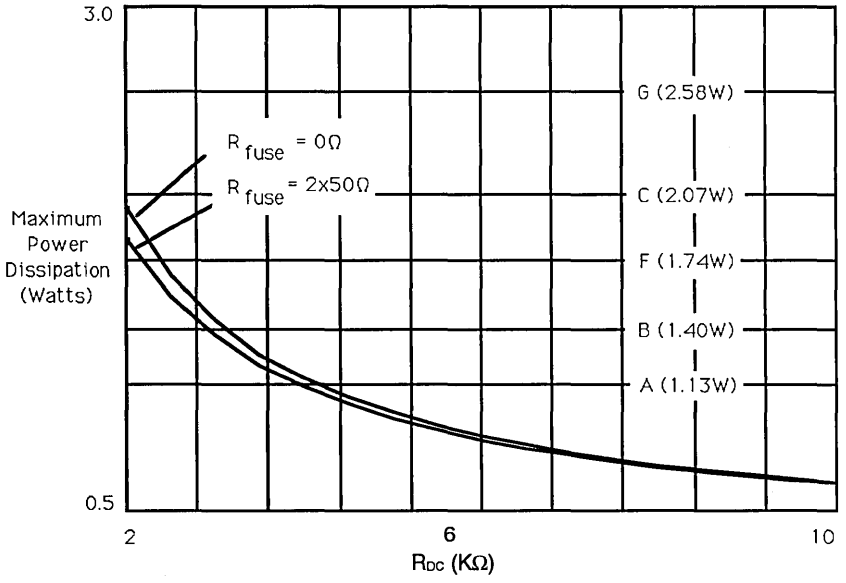
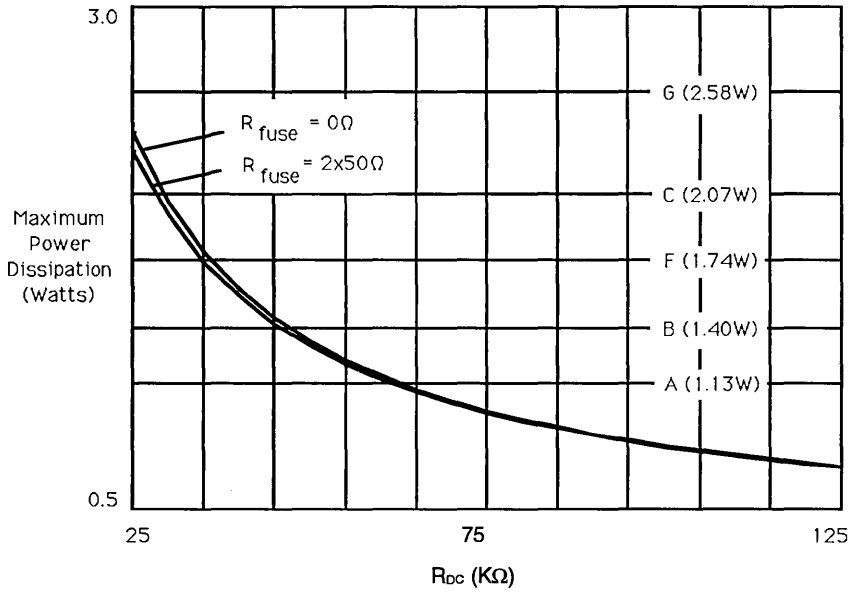


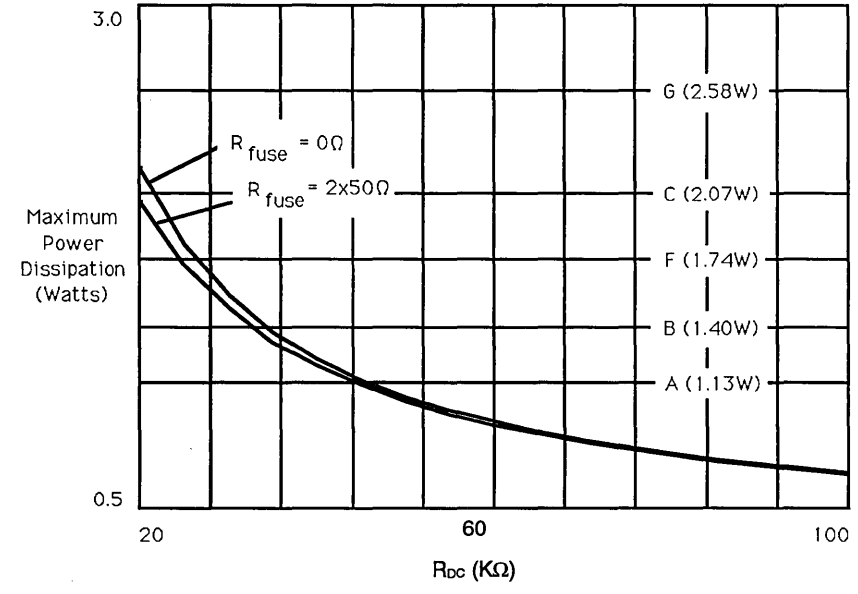
Am7958



Am79M53



Am79M57



Chapter 2

SLAC/DSLAC Products

CHAPTER 2
SLAC/DSLAC Products

INTRODUCTION TO SLAC/DSLAC PRODUCTS

AMD's Subscriber Line Audio-Processing Circuit (SLAC device) products are a family of programmable codec/filter ICs. They handle the analog-to-digital conversion, filtering, compression, digital-to-analog conversion, and expansion functions required to interface the analog voice signal from a telephone to the digital "PCM Highway." In addition, the SLAC Family devices incorporate a number of programmable digital filters that allow a linecard's analog characteristics to be adapted through software to address virtually any set of line conditions. This gives the linecard designer the flexibility to create a single hardware design that can satisfy the requirements of multiple markets, or multiple requirements within a market. This, in turn, streamlines manufacturing, helps control inventory and administrative costs, and reduces the time required to address new markets.

The SLAC Family consists of two product types, the SLAC devices and the Dual SLAC (DSLAC) devices. The NMOS Am7901 and Am7905 SLAC ICs support a single transmit and receive channel on a linecard, while the CMOS Am79C02, Am79C03, and Am79C04 DSLAC ICs are newer dual-channel devices.

The entire family complies with the most stringent telecommunication standards, such as those set by the CCITT, Bellcore, and British Telecom.

The SLAC Family's programmability resides in digital filters based on Digital Signal Processing (DSP) technology. The digital nature of the filters results in high reliability, no drift in filter response over time or temperature, and superior transmission performance. The following filters are provided for each channel supported by the SLAC or DSLAC devices.

- The Z and B filters configure feedback paths to accurately cancel the two-wire and four-wire echoes respectively. This permits optimal two-wire impedance matching and trans-hybrid balance to be achieved.
- The GX and GR filters allow for programmable gain and loss in the transmit and receive paths.
- The X and R filters provide for attenuation distortion correction, or may be used for line equalization.

The DSLAC device features adaptive trans-hybrid balance in addition to the functions provided by the SLAC device. This function automatically optimizes the four-wire return loss of the linecard by adapting to actual conditions in the field. A more detailed explanation of adaptive balance follows this section.

On the network side, most of the SLAC Family devices interface directly with the PCM highway and have programmable time slot assignments, eliminating the need for a special interface chip. The Am79C04 DSLAC features the IOM 2 interface which multiplexes control and PCM data over a single serial bus. This interface minimizes the amount of busing required on the linecard and is also used by many ISDN linecard devices.

Several test modes are provided by the SLAC Family to support linecard diagnostics including analog loopback, digital loopback, cut-off receive path, and high-pass disable.

Adaptive Balance

The fundamental problem addressed by the echo control in telephone subscriber linecards is a mismatch in the impedance characteristics of the two-wire loop and the balancing network. Because of this mismatch, some energy from the receive signal is returned to the transmitted signal and becomes an undesirable echo. Conventional echo removal uses an echo cancellation circuit in the transmit path with the balancing network fixed to a compromise network (representing the average impedance characteristics of a nation's subscriber local loops).

Instead of an echo cancellation circuit, the AMD DSLAC device uses an advanced adaptive filtering technology to remove the echo energy from the transmitted signal. The DSLAC device adaptive B filter is used to cancel the near-end echo produced at the four-to-two wire hybrid junction via coefficients found dynamically. The adaptive filter performs an estimate of the echo path impulse response and creates the echo replica, which is then subtracted so echo control is attainable. Thus, the echo cancellation is maintained under various and/or changing local loop conditions.

By turning on the adaptation for approximately one second and then turning it off, an adapt and freeze on the B filter is implemented. This operation develops the B-filter coefficients needed to optimize trans-hybrid balance. Adapt and freeze mode is intended for use in applications such as voice mail systems or PBX, where the loop condition and subscriber terminal equipment are not changed very often. It can also be used in central office applications on a per line basis during the installation/maintenance phase or on a per call basis if a training signal at the beginning of a call is considered acceptable.

The other type of adaptive balance incorporates both adapt and freeze and dynamic adaptive balance that continuously adjusts for changes in subscriber line conditions due to such factors as temperature variation, stress, or aging. Continuous adaptation mode is intended for applications where local loop conditions and customer premise equipment are changed frequently and a highly balanced echo return loss needs to be maintained. In this mode, the adaptive B filter will be turned on from the beginning of a call and will stay on until the call ends.

Final

Am7901B/C

Subscriber Line Audio-Processing Circuit (SLAC) WORLD-CHIP

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

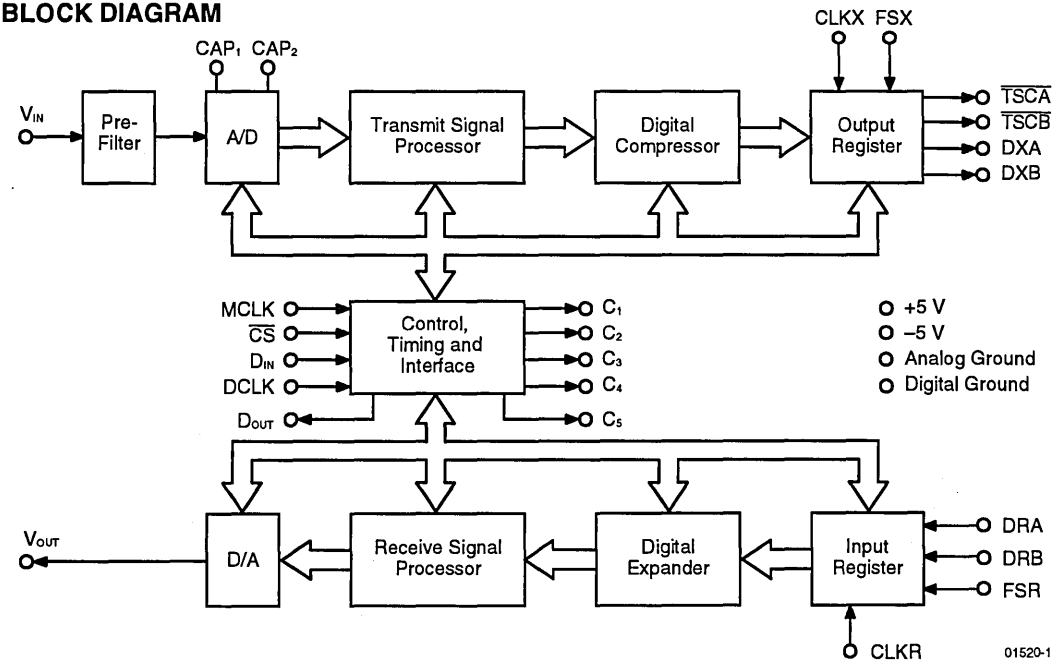
- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only two external components (non-precision)
- Dual PCM ports
- 4.096-MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable A-law, μ-law (Am7901B) or linear, A-law (Am7901C)

GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC™) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T® and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter, and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law (Am7901C). Either one of two output ports may be selected for PCM data transmission.

BLOCK DIAGRAM



Publication #: 01520 Rev. E Amendment /0
Issue Date: August 1990

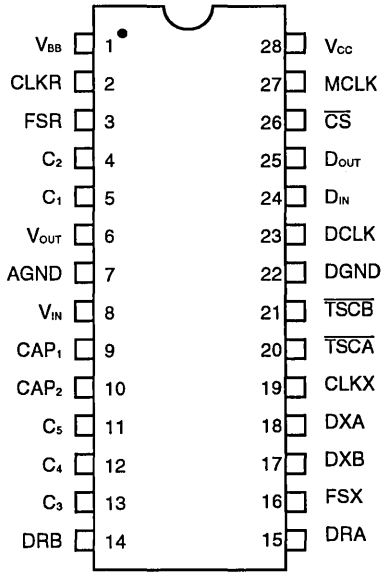
GENERAL DESCRIPTION (continued)

The receive section contains a digital signal processor and a D/A converter. Either 8 bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law codes (Am7901C) are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

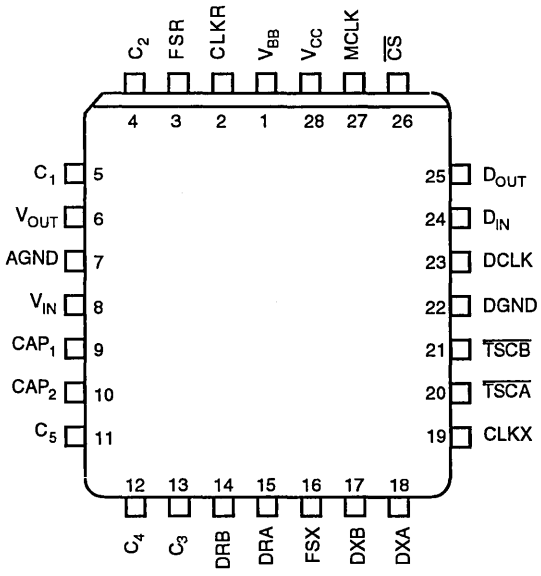
The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of commands.

CONNECTION DIAGRAM
Top View

DIPs

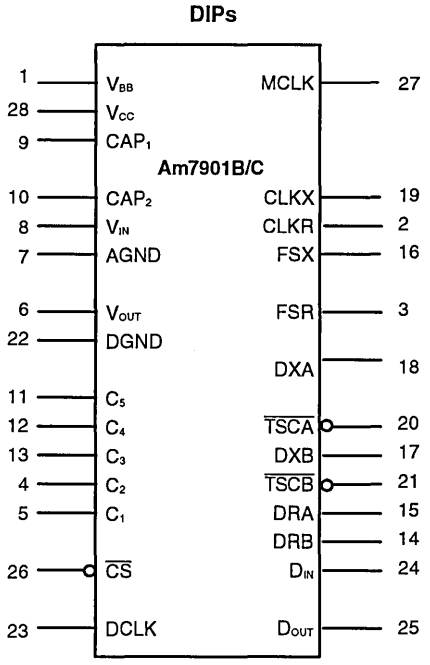


PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



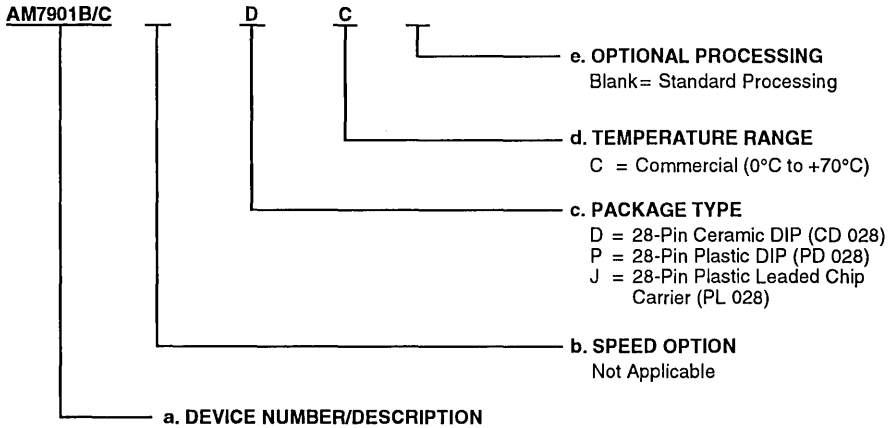
01520-2

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7901B	DC, PC, JC
AM7901C	DC, PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTIONS

AGND
Analog ground.

C_5–C_1
Latched Outputs

The serial interface may be used to write data to a register whose outputs are brought out to C_5–C_1. These 5 lines are TTL-compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line. C_5 is used as an output in the Auto-zero Speedup Mode.

CAP_2, CAP_1
An external series resistor and capacitor are connected to these pins. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1K ohm ±5% and 2000 pF ±20%.

CLKX, CLKR
PCM Clocks

The PCM Clocks determine the rate at which PCM data is serially shifted into or out of the PCM ports. The maximum clock frequency is 4.096 MHz and the minimum clock frequency is 128 kHz. CLKX determines the rate at which PCM data is transmitted. CLKR determines the rate at which PCM data is received.

$\overline{CS}$
Chip Select

The Chip Select input enables the device to either input or output control data. A level of –5 V on this input places the device in the Auto-zero Speedup Mode.

DCLK
Data Clock

The Data Clock shifts control data either into or out of the SLAC. The maximum clock rate is 2.048 MHz. A level of –5 V on this pin forces the device into the Reset state.

D_{IN}
Data Input

Control data is serially written via the Data Input port. The input rate is determined by the Data Clock.

D_{OUT}
Data Output

Control data is serially read via the Data Output port. The output rate is determined by the Data Clock. D_{OUT} is high-impedance when control data output is completed and $\overline{CS}$ is High.

DGND
Digital ground.

DRA, DRB
PCM Inputs

The receive-PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For μ-law and A-law, 8 bits are received and for linear code, 16 bits are received. The data is received in 8- or 16-bit bursts every 125 μs at the CLKR rate.

DXA, DXB
PCM Outputs

The transmit-PCM data is serially fed out to either the DXA or the DXB port. The port selection is under user program control. For μ-law and A-law, 8 bits are transmitted and for linear code, 16 bits are transmitted. The output is available every 125 μs and the data is shifted out in 8 or 16-bit bursts at the CLKX rate. DXA and DXB are high-impedance between bursts and also in the standby mode.

FSX, FSR
Frame Sync

The Frame Sync pulse is an 8-kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the Frame Sync pulse. FSX is the transmit-PCM Frame Sync and FSR is the receive-PCM Frame Sync. The FSX pulse must not be longer than 8 clock periods when companded code is used, and 16 clock periods when linear code is used.

MCLK
Master Clock

The Master Clock must be a 2.048 ±100 ppm clock input. MCLK is used by the digital signal processors. Loss of MCLK must be treated like a loss of power.

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control

The Time Slot Control outputs are open-drain outputs and are normally High. $\overline{TSCA}$ is Low when PCM data is present on the DXA output and $\overline{TSCB}$ is Low when PCM data is present on the DXB output.

V_{BB}
–5-V power supply.

V_{CC}
+5-V power supply.

V_{IN}
Analog Input

The analog input is applied to the transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.

V_{OUT}
Analog Output

The received-PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.

FUNCTIONAL DESCRIPTION

Device Operation

General

The Am7901B/C performs the codec and filtering functions associated with the four-wire section of the subscriber line circuitry in a digital switch. When used with the Am795XX Subscriber Line Interface Circuit (SLIC), the pair provide a complete solution to the BORSCHT (Battery feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid, and Test) functions (see Figure 1).

The SLAC contains A/D and D/A converters. A microprocessor-compatible interface is provided to program the device into a variety of modes. These operating modes include companded or linear-code operation, dynamic time-slot assignment, and PCM-port selection.

The SLAC samples the analog signal at the V_{IN} pin and digitally processes it to produce either a linear or companded PCM code at the DXA or DXB output (see Figure 2). Conversely, it receives either a linear or companded PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} pin. The processing is accomplished at the frame rate (8 kHz), and the digital output/input is available for transmission/reception every 125 µs.

Transmit Signal Processor

In the transmit path (see Figure 3), the analog signal is converted, filtered, compressed, and made available for output.

The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal-to-noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512-kHz sampling rate.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The B, X, and GX blocks shown in Figure 3 are user-programmable filter sections and their coefficients are stored in the Coefficient RAM. These filters may be transparent when not required in a system. The digital compressor may be bypassed when linear-code operation is desired.

The decimator reduces the high input sample rate. The X filter is a 4-tap Finite Impulse Response (FIR) section and is part of the frequency response correction network. The GX filter allows the user to program up to 12-dB gain in the transmit path with an accuracy of ±0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB. The B filter has 8 taps and operates on samples input from the Receive Signal Processor in order to provide trans-hybrid balancing in the loop. The low-pass filter limits the output bandwidth to meet the transmission requirements. The high-pass filter rejects 15-Hz and 50/60-Hz frequencies and may be disabled for testing.

Transmit PCM Interface

The Transmit PCM Interface receives either a16-bit linear code (for linear operation) or an 8-bit compressed code (for µ-law and A-law operation) from the digital compressor. This code is loaded into the output register. The Transmit PCM Interface logic (see Figure 4) controls the transmission of data onto the PCM highway through the output port-selection circuitry and the Time Slot Control block.

The Frame Sync (FSX) pulse identifies the beginning of a Transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers. The Time Slot register is normally 5-bits wide and allows up to thirty-two 8-bit channels or sixteen 16-bit channels (using CLKX = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give thirty-two 16-bit channels or sixty-four 8-bit channels (using CLKX = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 64 is selected. This feature allows any combination of channel assignments and clock frequencies (over a range of 128 kHz to 4.096 MHz) in a system. For µ-law and A-law operation, 8 bits/channel are output and for linear code operation, 16 bits/channel are output. The data is transmitted Most Significant Bit (MSB) first. The Clock Slot register is 3 bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKX periods to eliminate any clock skew in the system (see Figure 5).

In the Am7901B/C, the PCM data may be user-programmed to be output onto one of two ports, DXA or DXB. Correspondingly, either $\overline{TSCA}$ or $\overline{TSCB}$ is also Low.

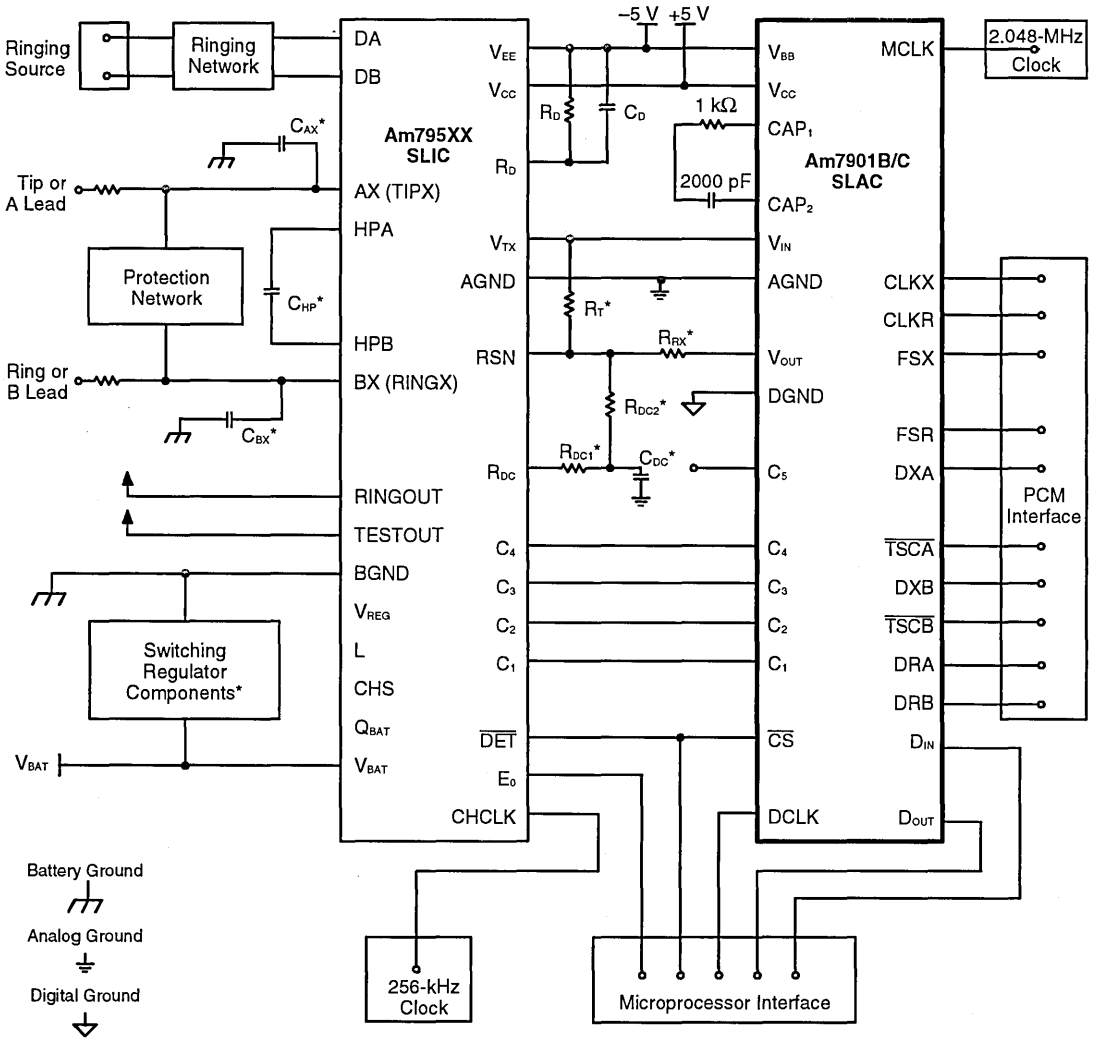
Receive PCM Interface

The Receive PCM Interface logic (see Figure 6) controls the reception of data from the PCM highway and transfers it for expansion (µ-law or A-law) to the Receive Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FSR) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it. The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is normally 5-bits wide and allows up to thirty-two 8-bit channels (using CLKR = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give thirty-two 16-bit channels or sixty-four 8-bit channels (using CLKR = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 63 is selected. This feature allows any combination of clock frequencies (over a range of 128 kHz to

4.096 MHz) and channel assignments in a system. For μ-law and A-law operation, 8 bits/channel are input and for linear code, 16 bits/channel are input. The MSB of the code must be received first. The Clock Slot register is 3-bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKR periods to eliminate any clock skews in the system (see Figure 7).

In the Am7901B/C, the PCM data may be user-programmed to be input from one of two ports, DRA or DRB.



*Component values are user-programmable. Refer to SLIC product specification.

Figure 1. Single-Channel Subscriber Line System

01520-3

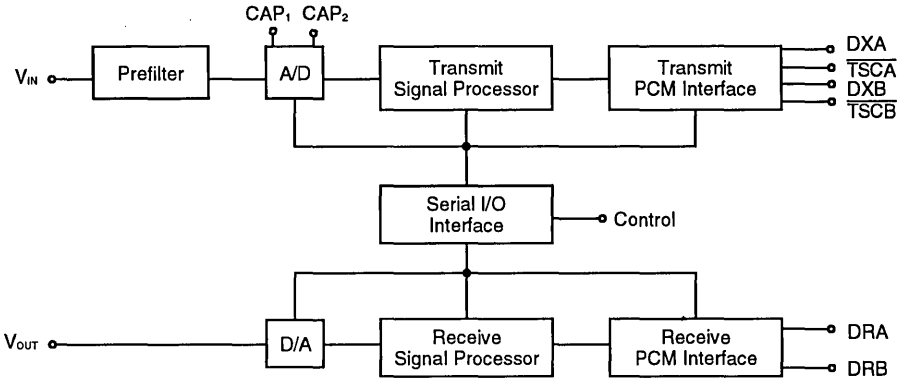
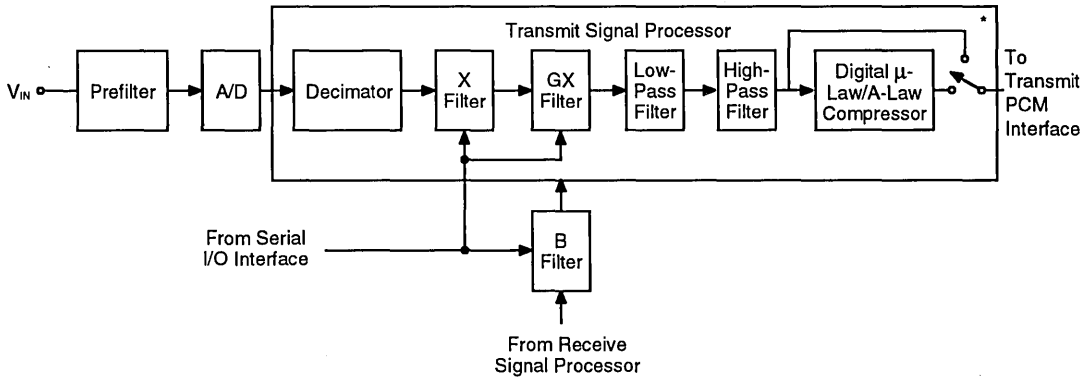


Figure 2. SLAC Block Diagram 01520-4



* Am7901C linear mode only.

Figure 3. Transmit Signal Processor 01520-5

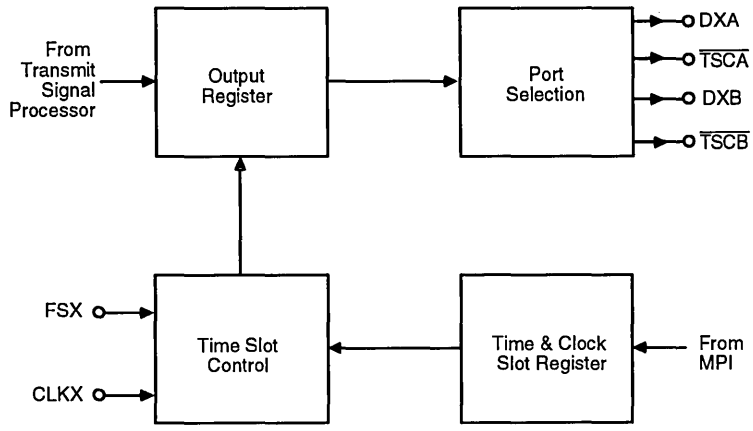


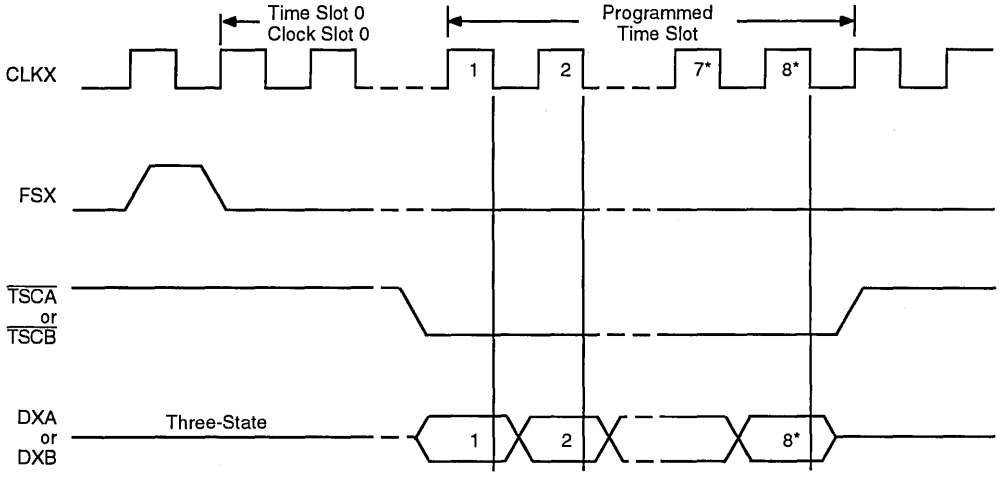
Figure 4. Transmit PCM Interface 01520-6

Receive Signal Processor

In the receive path (see Figure 8), the digital signal is expanded, filtered, converted to analog, and output onto the V_{OUT} pin.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The Z, R and GR are user-programmable filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The low-pass filter band-limits the signal. The GR filter allows the user to program a loss of up to 12 dB with an accuracy of ±0.051 dB. The R filter is a 4-tap FIR section and is part of the frequency response correction network. The Z filter provides feedback from the Transmit Signal Processor to the Receive Signal Processor and is used to modify the effective input impedance to the system. The interpolator provides the higher sample rate to the D/A converter.



*For linear code, the 7th and 8th clock cycles correspond to the 15th and 16th clock cycles.

Figure 5. Transmit PCM Timing Diagram

01520-7

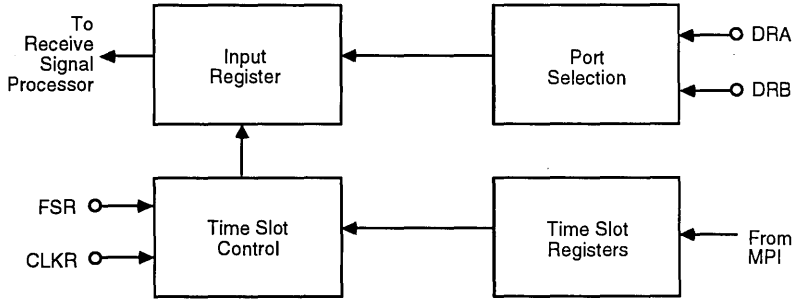
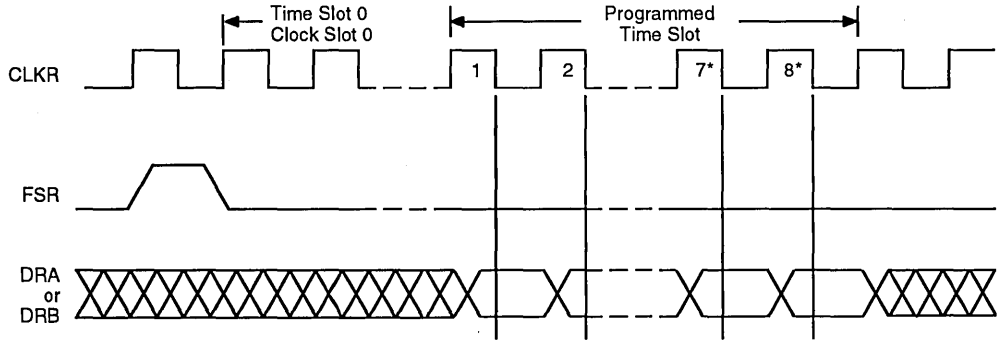


Figure 6. Receive PCM Interface

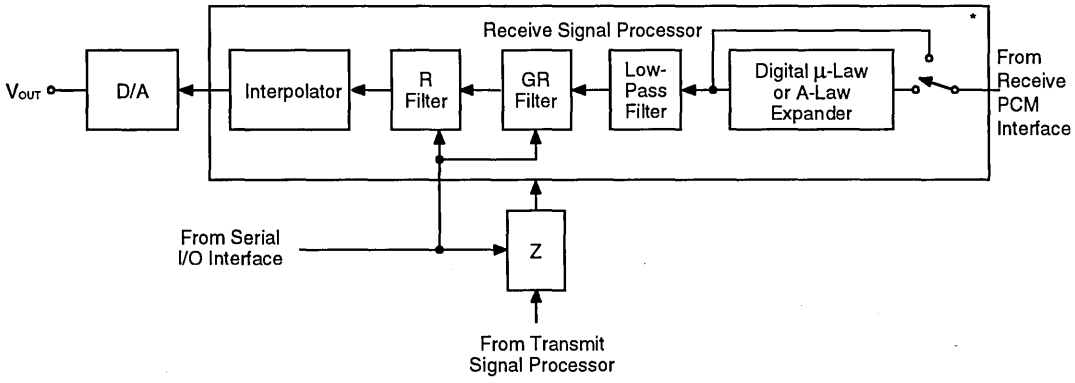
01520-9



*For linear code, the 7th and 8th clock cycles correspond to the 15th and 16th clock cycles.

01520-10

Figure 7. Receive PCM Timing Diagram



* For Am7901B, the expander cannot be bypassed.

01520-8

Figure 8. Receive Signal Processor

Serial I/O Interface

A microprocessor may be used to program the SLAC and control its operation using the Serial I/O Interface (see Figure 9). Additionally, data programmed previously may be read out for verification. The control word format is shown in Table 1. Commands are provided to:

- Set active/inactive modes
- Set up test functions
- Set up operating functions
- Program filter coefficients
- Assign time slots and port selection
- Write to the SLIC latch
- Enable/Disable each user-programmable filter

The interface consists of 4 pins, $\overline{CS}$, DCLK, D_{IN} and D_{OUT}. The device is accessed by $\overline{CS}$ and data is serially loaded-in on D_{IN} or read-out on D_{OUT} under control of DCLK. Either commands or data words may be written to the SLAC, but only data words can be read out. All words are 8-bits wide and are written or read MSB first (see Figure 10).

For both reception or transmission of words, exactly 8 Data Clock cycles must be received after $\overline{CS}$ goes Low. $\overline{CS}$ must stay High (off period) for a minimum time pe-

riod before it can go Low again. During this off-period, the logic decodes and executes the command. All reading of data must be preceded by an input command requesting the data. Once control data transmission has begun, no new input commands will be accepted until control data transmission is completed.

A Serial I/O cycle is defined by transitions of $\overline{CS}$ and DCLK. Upon proper application of power supplies and MCLK, the device expects the first word to be a command. A number of commands require additional data words to be input or output. The SLAC will not accept new commands until all this data has been transferred.

There are two possible operations of DCLK and $\overline{CS}$ for the SLAC to function correctly. If the $\overline{CS}$ is held in the High state between accesses, the DCLK may free run with no change to the internal control data. Using this method, the same DCLK may be run to a number of SLACs and individual $\overline{CS}$ lines will select the appropriate device to access. If the DCLK is held in the Low state between accesses, the $\overline{CS}$ line may make multiple transitions between accesses for a particular SLAC. This allows running one $\overline{CS}$ line to all SLACs and selecting a particular device through enabling or disabling its DCLK.

It should be noted that the DCLK can stay in the Low state indefinitely with no loss of internal control information. However, it should not be held in the High state for more than 20 µs to ensure proper operation as indicated by the Switching Characteristics Table.

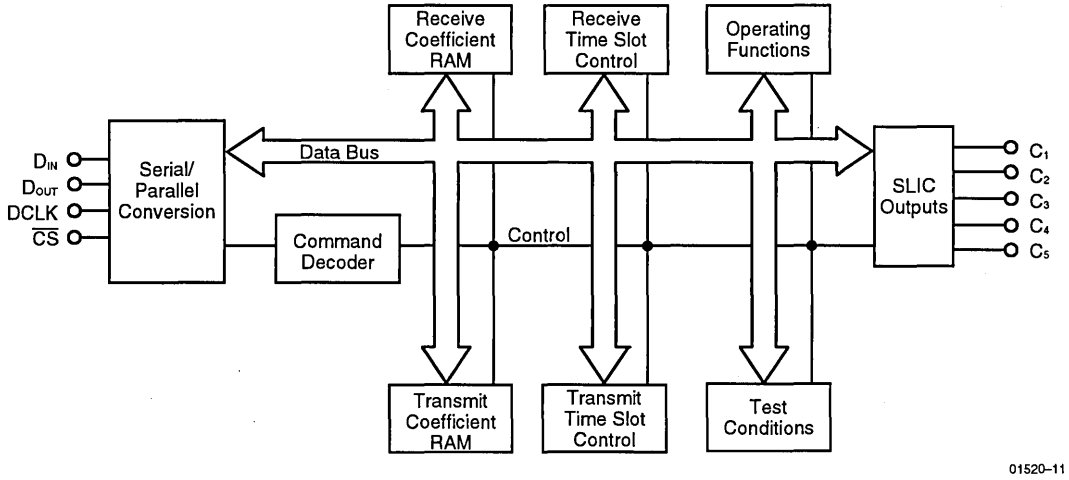


Figure 9. Serial I/O Interface

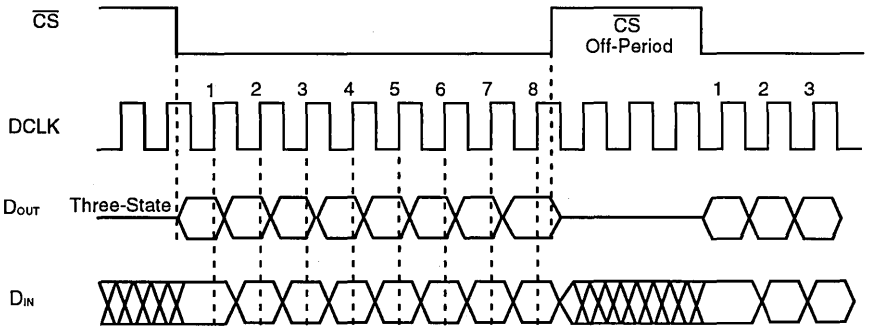


Figure 10. Serial I/O Interface Timing Diagram

Table 1. Control Word Summary

The Serial I/O Interface consists of Data Input, Data Output, Data Clock and $\overline{CS}$ Input. Data is read in (read out) on the Serial Data Input (output). The Serial Input consists of 8-bit (byte) command words which may be followed with additional bytes of input data or may be followed by the SLAC outputting bytes of data. All words are input with MSB (D_7) first and LSB (D_0) last. All outputs are output with the MSB (D_7) first and the LSB (D_0) last. Words are written or read one at a time, with $\overline{CS}$ going High for at least the minimum off-period (see under Switching Characteristics) before the next read or write operation. The first 3 bits of the command word indicate the type of command and the last 5 bits contain either data or further information about the command. The classes of command are:

D_7	D_6	D_5	
0	0	0	Inactivate/No Operation
0	0	1	Transmit Time Slot Selection
0	1	0	Receive Time Slot Selection
0	1	1	Clock Slot and Gain Selection Read Slot, Gain and PCM Mode
1	0	0	Set Basic and Operating Functions and PCM Modes
1	0	1	Read/Write Coefficients, Set Test Modes, Select μ-law/A-law/linear
1	1	0	Data for SLIC Interface
1	1	1	Activate/No Operation

MSB	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LSB	
	0	0	0	0	0	0	0	0	Inactivate	
	0	0	1	T	T	T	T	T	Transmit Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	0	T	T	T	T	T	Receive Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	1	0	0	C	C	C	Transmit Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	0	1	C	C	C	Receive Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	1	0	0	1	0	Transmit Gain Selection (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	0	1	0	Receive Gain Selection (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	0	1	Read Transmit Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	0	0	0	1	Read Transmit Gain (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	1	0	1	Read Receive Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	1	0	0	1	Read Receive Gain (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	1	1	Read PCM Mode	Followed by 1 Byte of Data
	1	0	0	0	B	X	R	Z	Enable Filters	
	1	0	0	1	D_R	D_X	R_{EX}	T_{EX}	PCM-Mode Selection	
	1	0	1	0	0	0	0	0	Write B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	0	0	Write X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	0	0	Write R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	0	0	Write Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	0	0	1	1	Read B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	1	1	Read X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	1	1	Read R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	1	1	Read Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	1	0	0	0	0	Reset to normal conditions	
	1	0	1	1	0	0	0	1	Add –6 dB to receive gain	
	1	0	1	1	0	0	1	0	Cutoff receive path	
	1	0	1	1	0	1	1	1	Test mode–analog loop-back	
	1	0	1	1	0	1	0	0	Test mode–digital loop-back	
	1	0	1	1	0	0	1	1	Disable High-Pass Filter (set to 1) and freeze auto zero circuit	
	1	0	1	1	1	0	0	B	Choose PCM Code	
	1	1	0	C	C	C	C	C	Outputs to SLIC	
	1	1	1	1	1	1	1	1	Activate	

Am7901B/C Detailed Serial Command Definitions

Inactivate (Standby Mode)

MSB							LSB
0	0	0	0	0	0	0	0

In the inactive mode, none of the programmed information is changed and the analog output is set to zero volts through a moderate series impedance. The Serial I/O remains active, the SLIC control outputs remain valid, and the PCM outputs are high impedance.

Activate (Operational Mode)

MSB							LSB
1	1	1	1	1	1	1	1

Valid PCM data is not transmitted until after the second FSX pulse is received following the execution of the Activate command.

Transmit Time Slot Selection

MSB							LSB
0	0	1	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Transmit Clock Slot Selection

MSB							LSB
0	1	1	0	0	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Transmit Time and Clock Slots

Command

MSB							LSB
0	1	1	1	0	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The transmit time and clock slots are read out time slot first, followed by clock slot.

Receive Time Slot Selection

MSB							LSB
0	1	0	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Receive Clock Slot Selection

MSB							LSB
0	1	1	0	1	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Receive Time and Clock Slots

Command

MSB							LSB
0	1	1	1	1	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The receive time and clock slots are read out time slot first, followed by clock slot.

Write GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	1	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Read GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	0	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Write GR Filter Coefficients

Command

MSB							LSB
0	1	1	1	1	0	1	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Read GR Filter Coefficients

Command

MSB							LSB
0	1	1	1	1	0	0	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Write PCM Mode Selection

MSB							LSB
1	0	0	1	D_R	D_X	R_{EX}	T_{EX}

Receive Port: $D_R = 0$: PCM data is input on DRA.
$D_R = 1$: PCM data is input on DRB.

Transmit Port: $D_X = 0$: PCM data is output on DXA.
$D_X = 1$: PCM data is output on DXB.

Receive Expanded Mode: $R_{EX} = 0$: Reset Receive Expanded Mode.
$R_{EX} = 1$: Set Receive Expanded Mode.

Transmit Expanded Mode: $T_{EX} = 0$: Reset Transmit Expanded Mode.
$T_{EX} = 1$: Set Transmit Expanded Mode.

Read PCM Mode Selection

Command

MSB							LSB
0	1	1	1	0	1	1	1

Output Data

1	1	1	1	D_R	D_X	R_{EX}	T_{EX}

Enable Filters

MSB							LSB
1	0	0	0	EB	EX	ER	EZ

B Filter: EB = 0: B filter disabled.
EB = 1: B filter enabled.

X Filter: EX = 0: X filter disabled.
EX = 1: X filter enabled.

R Filter: ER = 0: R filter disabled.
ER = 1: R filter enabled.

Z Filter: EZ = 0: Z filter disabled.
EZ = 1: Z filter enabled.

Write Test Mode Selection

MSB							LSB
1	0	1	1	0	T_3	T_2	T_1

T3	T2	T1	Function
0	0	0	Reset to normal conditions as follows. Receive gain is set to the value stored in the GR register. Analog and digital loopback modes are reset. The high-pass filter is enabled and the auto-zero circuit is operational. The receive path is not cutoff.
0	0	1	Add –6 dB to receive gain.
0	1	0	Cutoff receive path.
0	1	1	Disable high-pass filter (set to 1) and freeze auto-zero circuit.
1	0	0	Activate digital loopback.
1	1	1	Activate analog loopback.

Select PCM Coding

MSB							LSB
1	0	1	1	1	0	0	B

Bit B selects the type of PCM code to be used.

For the Am7901B: B = 0: A-law.
B = 1: μ-law.

For the Am7901C: B = 0: Linear.
B = 1: A-law.

Write SLIC Output Registers

MSB							LSB
1	1	0	C_5	C_4	C_3	C_2	C_1

Write B Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	0	0	0

Input Data

C_{30} m_{30}	C_{20} m_{20}	Byte 1
C_{10} m_{10}	C_{31} m_{31}	Byte 2
C_{21} m_{21}	C_{11} m_{11}	Byte 3
C_{32} m_{32}	C_{22} m_{22}	Byte 4
C_{12} m_{12}	C_{33} m_{33}	Byte 5
C_{23} m_{23}	C_{13} m_{13}	Byte 6
C_{34} m_{34}	C_{24} m_{24}	Byte 7
C_{14} m_{14}	C_{35} m_{35}	Byte 8
C_{25} m_{25}	C_{15} m_{15}	Byte 9
C_{36} m_{36}	C_{26} m_{26}	Byte 10
C_{16} m_{16}	C_{37} m_{37}	Byte 11
C_{27} m_{27}	C_{17} m_{17}	Byte 12

Read B Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	0	1	1

Output Data

C_{30} m_{30}	C_{20} m_{20}	Byte 1
C_{27} m_{27}	C_{17} m_{17}	Byte 12

Write X Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	1	0	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2
C_{41} m_{41}	C_{31} m_{31}	Byte 3
C_{21} m_{21}	C_{11} m_{11}	Byte 4
C_{42} m_{42}	C_{32} m_{32}	Byte 5
C_{22} m_{22}	C_{12} m_{12}	Byte 6
C_{43} m_{43}	C_{33} m_{33}	Byte 7
C_{23} m_{23}	C_{13} m_{13}	Byte 8

Read X Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	1	1	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 8

Write R Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	0	0	0

Input Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 2
C_{42} m_{42}	C_{32} m_{32}	Byte 3
C_{22} m_{22}	C_{12} m_{12}	Byte 4
C_{41} m_{41}	C_{31} m_{31}	Byte 5
C_{21} m_{21}	C_{11} m_{11}	Byte 6
C_{40} m_{40}	C_{30} m_{30}	Byte 7
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Read R Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	0	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Read Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Write Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	0	0

Input Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 2
C_{42} m_{42}	C_{32} m_{32}	Byte 3
C_{22} m_{22}	C_{12} m_{12}	Byte 4
C_{41} m_{41}	C_{31} m_{31}	Byte 5
C_{21} m_{21}	C_{11} m_{11}	Byte 6
C_{40} m_{40}	C_{30} m_{30}	Byte 7
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Digital Filters

The SLAC uses digital signal processing to implement the various filters (see Figure 11).

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance

Six of the digital filters in the signal processing sections are user-programmable. These allow the user to independently modify the gain in both the transmit and receive paths, provide trans-hybrid balancing in the system, and adjust the two-wire line termination impedance. This programming capability feature allows the user to optimize the performance of the SLAC for his system.

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the SLAC is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \quad (1)$$

where the number of taps in the filter = n + 1.

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + \ldots + B_N 2^{-MN}, \quad (2)$$

where:

the number of shifts = $M_i \leq M_{i+1}$

sign = $B_i = \pm 1$

N = Number of CSD coefficients.

The value of h_i in (2) represents a decimal number which is broken down into a sum of successive values of:

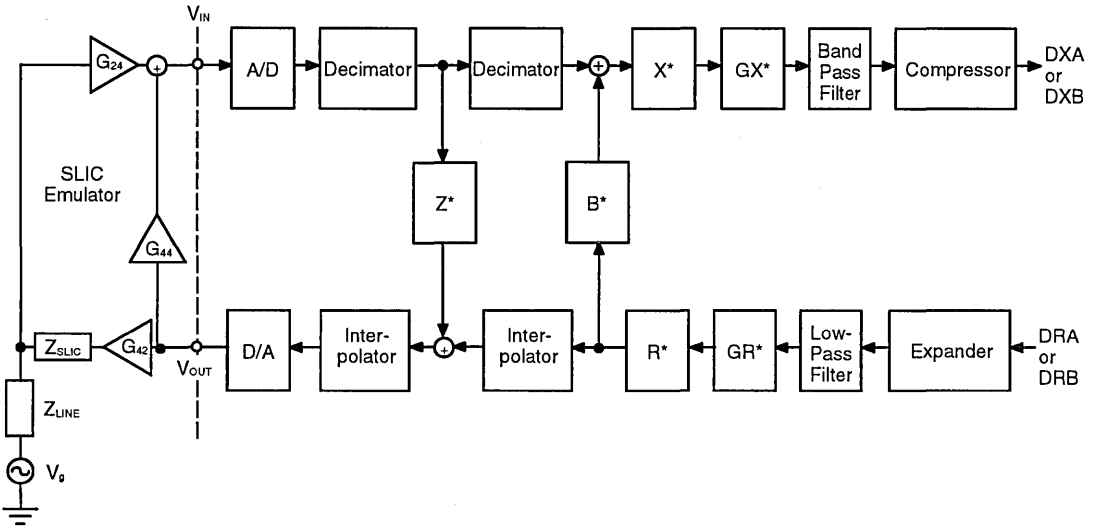
± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 ... 1/128....

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 2 can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is



*User-Programmable Filters

Figure 11. SLAC Signal Processing Flow

01520–13

shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take; for example, if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4.

Detailed Description of SLAC Coefficients

The CSD coding scheme in the SLAC uses a value called m_i, where m_1 represents the distance shifted right of the decimal point for the first binary 1, m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 2 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + B_3 2^{-M3} + B_4 2^{-M4} \quad (3)$$

$$h_i = C_1 2^{-m1} + C_1 C_2 2^{-(m1+m2)} + C_1 C_2 C_3 2^{-(m1+m2+m3)} + C_1 C_2 C_3 C_4 2^{-(m1+m2+m3+m4)} \quad (4)$$

$$h_i = C_1 2^{-m1} \cdot [1 + C_2 2^{-m2} \cdot \{1 + C_3 2^{-m3} \cdot (1 + C_4 2^{-m4})\}] \quad (5)$$

where:

$M_1 = m_1$	and	$B_1 = C_1$
$M_2 = m_1 + m_2$		$B_2 = C_1 \cdot C_2$
$M_3 = m_1 + m_2 + m_3$		$B_3 = C_1 \cdot C_2 \cdot C_3$
$M_4 = m_1 + m_2 + m_3 + m_4$		$B_4 = C_1 \cdot C_2 \cdot C_3 \cdot C_4$

In the SLAC, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is three bits. Each CSD coefficient is broken down as follows:

- C_{xy} is the sign bit (0 = positive, 1 = negative).
- m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:
  - 000: illegal
  - 001: 6 shifts
  - 010: 5 shifts
  - 011: 4 shifts
  - 100: 3 shifts
  - 101: 2 shifts
  - 110: 1 shift
  - 111: 0 shifts
- y is the coefficient number (the i in h_i).
- x is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, and Z filters, and 3 for the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters:

$$h_{iGX} = 1 + h_i \quad (6)$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Two-Wire Impedance Matching

A feedback path is provided from the transmit to the receive section via the Z filter. This filter may be programmed to modify the effective termination impedance (Z_{SLIC}) of a SLIC or a transformer hybrid to a desired value. The desired impedance may be complex. This feature allows the user to terminate each SLIC in a Subscriber Line System with a fixed resistor and digitally modify their impedance using the Z filter.

The X and R filters are the Transmit and Receive attenuation distortion correction filters. These filter sections are programmed to compensate the attenuation distortion caused by the Z filter.

Trans-Hybrid Balance

In a traditional line card system, a balance network is used with the SLIC to achieve trans-hybrid balancing. If the balance network perfectly matches the subscriber's line, infinite trans-hybrid balancing is achieved. But in general, the matching in traditional systems is poor and trans-hybrid balancing is not very good. Some systems have up to 2 or 3 compromise networks per line that must be selected semi-automatically or manually to provide the balance.

In the SLAC, a feedback path is provided from the receive to the transmit section via the B filter. This filter may be programmed to cancel the received signal from the transmit signal path and achieve a significantly improved level of trans-hybrid balance.

Gain Adjustment

Signal levels in the transmit and receive paths may be modified by programming the GX and GR filters. The GX filter allows the user to add up to 12 dB of gain with an accuracy of 0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB in the transmit path. The GR filter allows the user to add up to 12 dB of loss with an accuracy of ±0.051 dB in the receive path.

Test Features

The SLAC simplifies system testing by providing both digital and analog loop-back paths. Under program control, either the DRA or DRB input is looped to the DXA or

DXB output (digital loop-back) through a path from the output of the interpolator in the receive path to the input of the decimator in the transmit path, or the V_{IN} input is looped to the V_{OUT} output (analog loop-back) through the Z filter. To allow testing of the subscriber loop cabling for leakage, the transmit high pass filter may be disabled and auto-zero operation interrupted. The receive analog output may be programmed to cut off. This receive cut-off command may be used to stop oscillations in the four-wire side of the telephone network.

The SLAC contains an auto-zero circuit in the A/D converter which takes several seconds to settle following a change in the offset voltage at V_{IN}. To facilitate component testing of the SLAC, there is a test mode available to accelerate settling of the auto-zero circuit. This test mode is activated by holding the CS input at -5 V for at least 64 ms with the offset voltage applied to V_{IN} (and no signal). The auto-zero will settle in this time. In a component test environment, this procedure should be followed after programming the filters. The C_5 output is also used in this mode. The output level on C_5 may be modified.

Note: The digital loopback (DLB) path processes an internal data word 2-bits shorter than in normal mode. Therefore, DLB signal processing performance is not equivalent to normal mode signal processing and does not meet the specified Transmission specifications. DLB is recommended for use with 0-dB programmed gain/attenuation and PCM signal levels above –25 dBm0.

Stand-By Mode

The SLAC is forced into the stand-by mode either by a hardware reset applied to the DCLK input or by reception of the Inactivate command. In this mode, power is switched off from all circuitry that can be turned off. No transmission or reception of PCM data takes place. However, the circuits which contain programmed information retain their data. The Serial I/O Interface remains active to receive new commands.

Power-On Clear

Before any other commands are written to the SLAC, 13 Inactivate commands should be sent to the serial port of the SLAC in case the SLAC powers up in the middle of a read sequence. Alternatively, a hardware reset operation can be carried out by applying –5 V to the DCLK pin. A loss of MCLK should be treated like a loss of power.

Stand-Alone Mode

In the stand-alone mode, the serial interface is not used. The DCLK and D_{IN} pins may be used to control the device. Applying –5 V to the DCLK pin resets the device and the D_{IN} pin can subsequently be used to power-up or power-down the SLAC.

DCLK	D_{IN}	
0	X	Normal Mode
1	X	Normal Mode
–5 V	0	Reset and Power-Down
–5 V	1	Reset and Power-Up

Reset State

The Reset State of the device is:

a. Both Transmit and Receive Time and Clock Slots are set to 0.

b. A-law is selected.

c. B, X, R, Z filters are disabled.

d. Both Transmit (GX) and Receive (RX) gains are set to unity.

e. SLIC outputs are set High.

f. Normal conditions are selected.

g. DXA/DRA ports are selected.

μ-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number *n*	Decision Value x_n (1)	Character Signal (5) Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		8159	(128)	(8159)	- - - - - - - - - - -		
8	16×256		127	7903	1 0 0 0 0 0 0 0	8031	127
			⋮	⋮	⋮ (2)	⋮	⋮
			113	4319	1 0 0 0 1 1 1 1	4191	112
7	16×128	4063	112	4063	⋮ (2)	⋮	⋮
			⋮	⋮	1 0 0 1 1 1 1 1	2079	96
			97	2143	⋮ (2)	⋮	⋮
6	16×64	2015	96	2015	1 0 1 0 1 1 1 1	1023	80
			⋮	⋮	⋮ (2)	⋮	⋮
			81	1055	1 0 1 1 1 1 1 1	495	64
5	16×32	991	80	991	⋮ (2)	⋮	⋮
			⋮	⋮	1 1 0 0 1 1 1 1	231	48
			65	511	⋮ (2)	⋮	⋮
4	16×16	479	64	479	1 1 0 1 1 1 1 1	99	32
			⋮	⋮	⋮ (2)	⋮	⋮
			49	239	1 1 1 0 1 1 1 1	33	16
3	16×8	223	48	223	⋮ (2)	⋮	⋮
			⋮	⋮	1 1 1 1 1 1 1 0	2	1
			33	103	1 1 1 1 1 1 1 1	0	0
2	16×4	95	32	95			
			⋮	⋮			
			17	35			
1	15×2	31	16	31			
			⋮	⋮			
			2	3			
	1×1		1	1			
			0	0			

Notes:
1. 8159 normalized value units correspond to $T_{MAX} = 3.17$ dBm0.
2. The character signal corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
3. The value at the decoder is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, \ldots, 127$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

A-Law, Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal Before Inversion of the Even Bits Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		4096	(128)	(4096)	- - - - - - - -		
7	16×128		127 ⋮ 113	3968 ⋮ 2176	1 1 1 1 1 1 1 1 ⋮ (2) 1 1 1 1 0 0 0 0	4032 ⋮ 2112	128 ⋮ 113
6	16×64	2048	112 ⋮ 97	2048 ⋮ 1086	⋮ (2) 1 1 1 0 0 0 0 0	⋮ 1056	⋮ 97
5	16×32	1024	96 ⋮ 81	1024 ⋮ 544	⋮ (2) 1 1 0 1 0 0 0 0	⋮ 528	⋮ 81
4	16×16	512	80 ⋮ 65	512 ⋮ 272	⋮ (2) 1 1 0 0 0 0 0 0	⋮ 264	⋮ 65
3	16×8	256	64 ⋮ 49	256 ⋮ 136	⋮ (2) 1 0 1 1 0 0 0 0	⋮ 132	⋮ 49
2	16×4	128	48 ⋮ 33	128 ⋮ 68	⋮ (2) 1 0 1 0 0 0 0 0	⋮ 66	⋮ 33
1 ↓	32×2	64	32 ⋮ 1	64 ⋮ 2	⋮ (2) 1 0 0 0 0 0 0 0	⋮ 1	⋮ 1
			0	0			

Notes:
1. 4096 normalized value units correspond to $T_{MAX}=3.14$ dBm0.
2. The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and $n+1$ (see column 4) is $(128+n)$ expressed as a binary number.
3. The value at the decoder output is $y_n=\frac{x_{n-1}+x_n}{2}$ for $n=1, \ldots, 127, 128$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –60 to 125°C
Ambient Temperature under Bias ..... 0 to 70°C
V_{CC} with respect to DGND ..... –0.4 to +6.0 V
V_{BB} with respect to DGND ..... +0.4 to –6.0 V
V_{IN} with respect to AGND ..... V_{BB} to V_{CC}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) ..... 0 to 70°C
V_{CC} ..... +5.0 V ±5%
V_{BB} ..... –5.0 V ±5%
DGND ..... 0 V
AGND ..... DGND ±100 mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (Note 1) unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Z_{IN}	Analog Input Impedance	$-3.2\ V < V_{IN} < 3.2\ V$	20			kΩ
Z_{OUT}	Analog Output Impedance	$-3.2\ V < V_{OUT} < 3.2\ V$			20	Ω
V_{IOS}	Offset Voltage Allowed on V_{IN}				±40	mV
V_{OOS}	Analog Output Offset Voltage				±30	mV
V_{IR}	Analog Input Voltage Range				±3.2 V	V
V_{OR}	Analog Output Voltage Range	$R_L \geq 10\ k\Omega$, $C_L \leq 50\ pF$			±3.2 V	V
I_{OUT}	Analog Output Current		350			µA
V_{IL}	Input Low Voltage (All Digital Inputs Except DCLK in Stand Alone Mode and $\overline{CS}$ in Auto Zero Speedup Mode)		–0.5		0.8	V
V_{IH}	Input High Voltage (All Digital Inputs)		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (All Digital Outputs)	$I_{OL} = 2\ mA$			0.45	V
V_{OH}	Output High Voltage (All Outputs Except TSC)	$I_{OH} = 400\ \mu A$	2.4			V
I_{OL}	Output Leakage Current				±10	µA
I_{IL}	Input Leakage Current				±1	µA
I_{IL} (V_{IN})	Input Leakage Current on V_{IN} Pin				±0.2	µA
I_{CC} (S)	V_{CC} Supply Current (Standby)	$V_{CC} = 5.25\ V$, $V_{BB} = -4.75\ V$			15	mA
I_{BB} (S)	V_{BB} Supply Current (Standby)				10	mA
I_{CC} (A)	V_{CC} Supply Current (Active)				60	mA
I_{BB} (A)	V_{BB} Supply Current (Active)				20	mA
PSRR	V_{CC} Power Supply Rejection Ratio	200 mV p-p @ 1.02 kHz on the appropriate supply, $V_{CC} = +5\ V$, $V_{BB} = -5\ V$	35			dB
PSRR	V_{BB} Power Supply Rejection Ratio		30			dB
C_I	Input Capacitance (Digital)			5		pF
C_O	Output Capacitance (Digital)			8		pF

Note: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages. Min and max specifications are over the temperature and supply voltage ranges shown in the above table entitled "Operating Ranges."

TRANSMISSION CHARACTERISTICS

(All specifications are guaranteed with 0 dB ≤ GX ≤ +12 dB, −12 dB ≤ GR ≤ 0 dB and A-law or μ-law companded PCM, unless otherwise specified.)

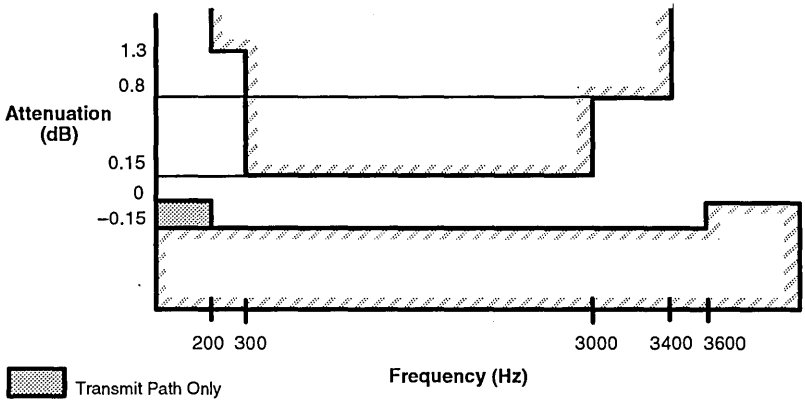
When GR = 0 dB, a 1020 Hz sine wave signal with level of 0 dBm0 at the digital input will correspond to an rms voltage of 1.6 V for A-law and 1.588 V for μ-law at the analog output. When GX = 0 dB, a 1020-Hz sine wave signal with rms voltage of 1.569 V for A-law and 1.557 V for μ-law at the analog input will correspond to a level of 0 dBm0 at the digital output.

Description	Test Conditions	Min	Typ	Max	Units
Attenuation Distortion	1020 Hz at −10 dBm0		(see Fig. 12)		dB
Gain (either path) a. deviation from ideal value b. deviation from initial value	1020 Hz at −10 dBm0	 −0.2 −0.2		 +0.2 +0.2	 dB dB
Group Delay Distortion (either path)	−10 dBm0 signal		(see Fig. 14)		
Harmonic Distortion	(Note 1)			−40	dB
Intermodulation Distortion	a. (Note 2) b. (Note 3)			−35 −49	dB dBm0
Crosstalk a. Go-to-Return Path b. Return-to-Go path	 300–3400 Hz, 0 dBm0 300–3400 Hz, 0 dBm0		 −90 −90	 −70 −70	 dB dB
Gain Tracking (either path)			(see Fig. 15, 17)		dB
Signal to Total Distortion (either path)			(see Fig. 16, 18, 19)		dB
μ-Law Companded PCM					
Idle Channel Noise (weighted, transmit)				19	dBrnc0
Idle Channel Noise (weighted, receive)				15	dBrnc0
A-Law Companded PCM					
Idle Channel Noise (weighted, transmit)				−68	dBm0p
Idle Channel Noise (weighted, receive)				−78	dBm0p

Notes: 1. Applied signal is a 0-dBm0 sine wave within 300 to 3400 Hz. The signal measured is any frequency in the range 300 to 3400 Hz.

2. Two different frequencies, f_1 and f_2, in the range 300–3400 Hz and of equal levels in the range −4 to −21 dBm0 are applied. $2f_1–f_2$ products are measured relative to the level of either f_1 or f_2.

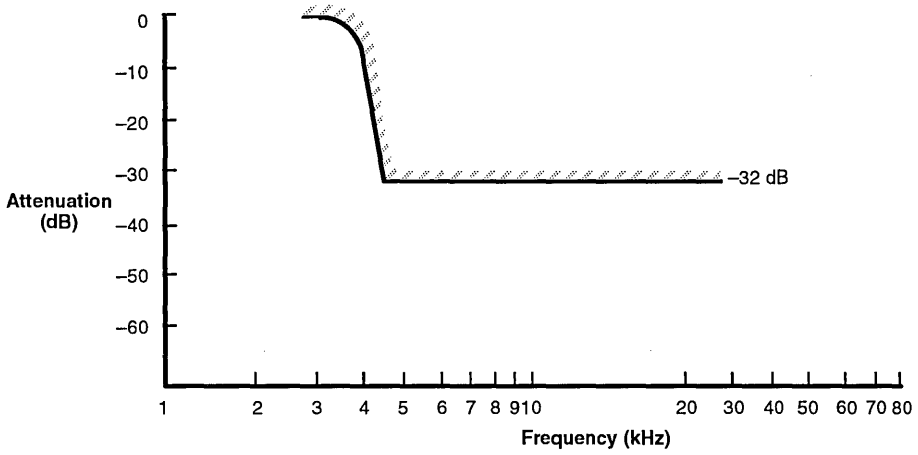
3. Any intermodulation product due to a signal in the range 300–3400 Hz with input level −9 dBm0 and a 50-Hz signal with input level −23 dBm0.



Note: Measured per CCITT Rec. G.714 Paragraph 7.

01520–14

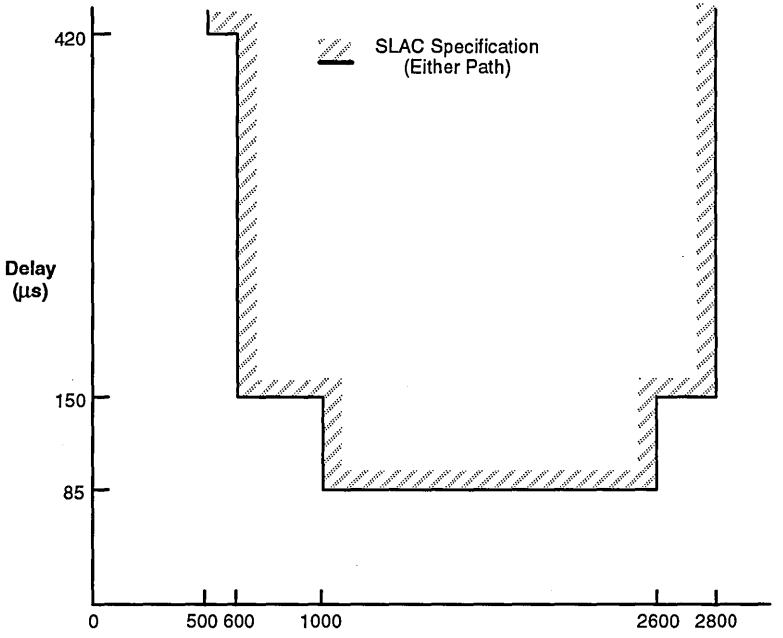
Figure 12. Attenuation Distortion Transmit or Receive Path



Notes: 1. The frequency is 1020 Hz.
2. Input signal level is 0 dBm0.

Figure 13. Out of Band Signals (End-to-End)

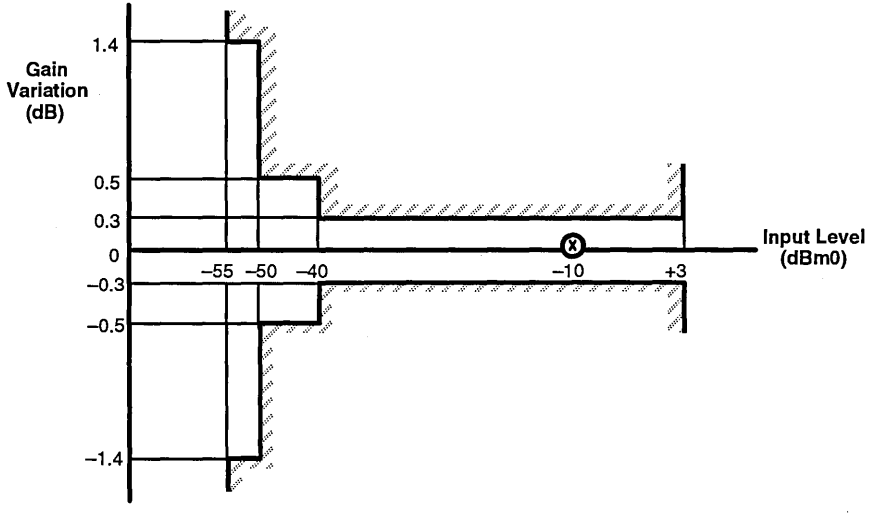
01520–15



Note: Minimum value of group delay is taken as reference.

01520-16

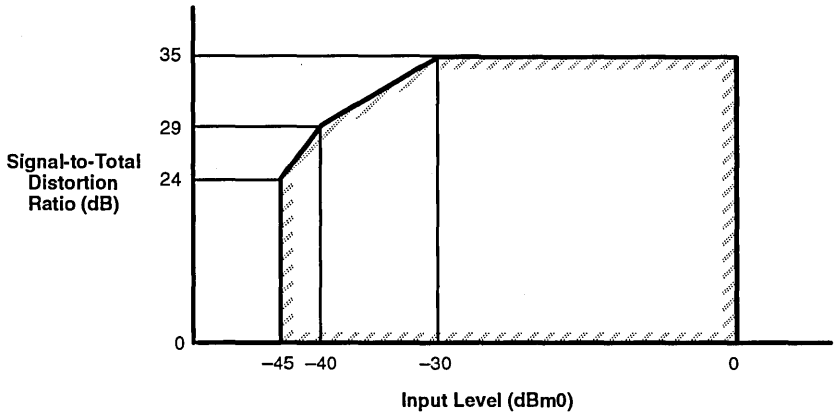
Figure 14. Group Delay Distortion (Either Path)



Note: Measured per CCITT Rec. G.714 Paragraph 15.

01520-17

Figure 15. Gain Tracking with Tone (Method 2) Transmit or Receive Path

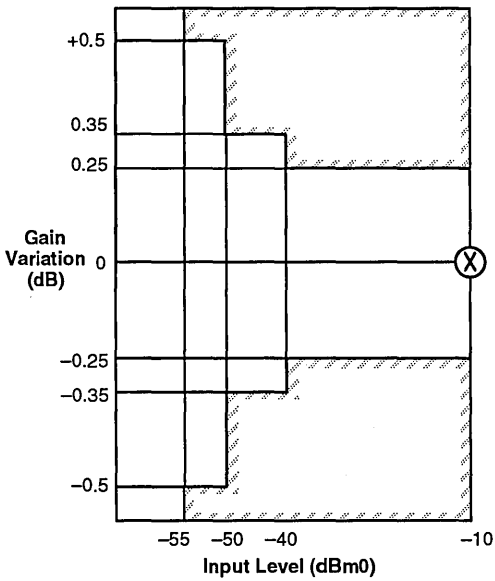


Note: Measured per CCITT Rec. G.714 Paragraph 14.

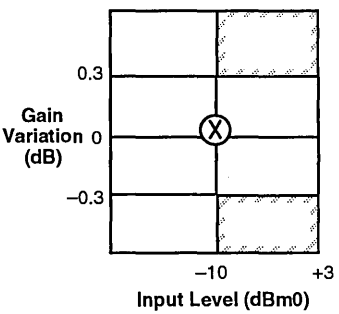
01520–18

Figure 16. Signal-to-Total Distortion With Tone (Method 2) Transmit or Receive Path

a. Noise Test Signal



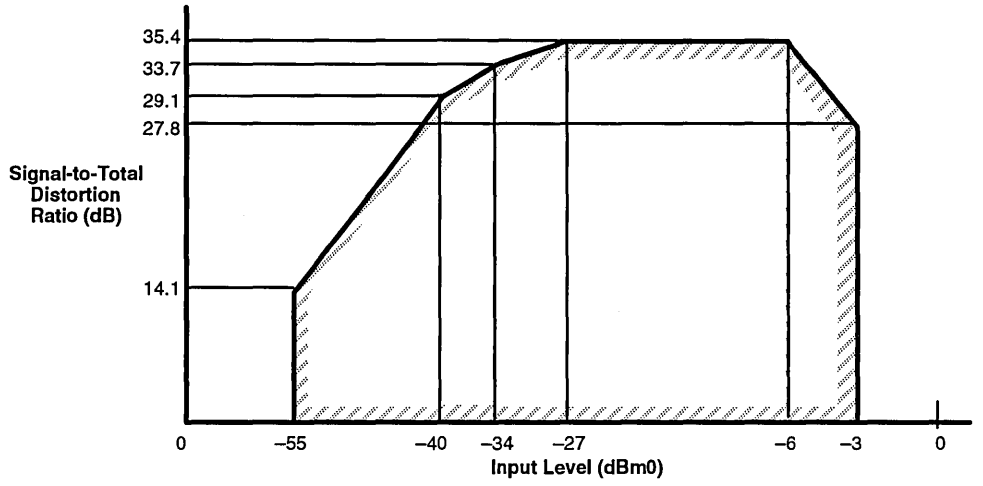
b. Sinusoidal Test Signal



Note: Measured per CCITT Rec. G.714 Paragraph 15.

01520-19

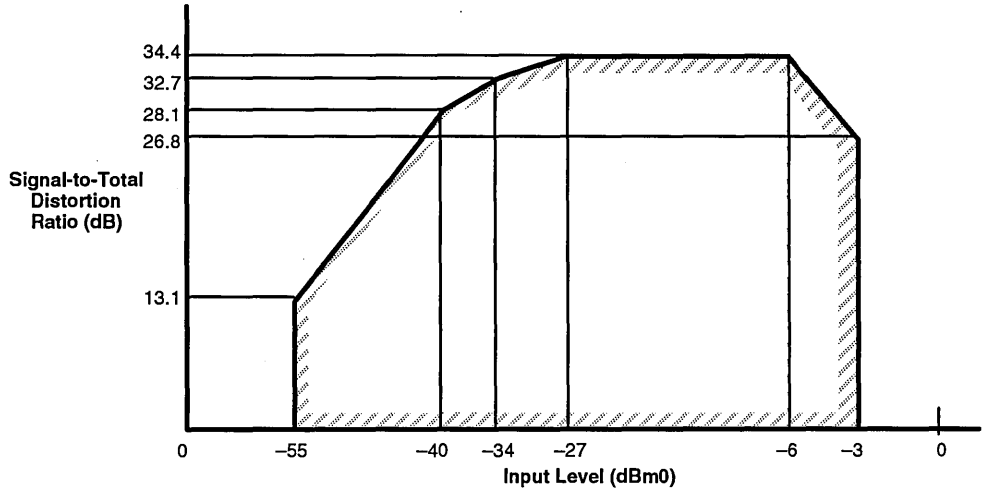
Figure 17. Gain Tracking with Noise (Method 1) Transmit or Receive Path



Note: Measured per CCITT Rec. G.714 Paragraph 14.

01520-20

Figure 18. Signal-to-Total Distortion With Noise (Receive Path—Method 1)



Note: Measured per CCITT Rec. G.714 Paragraph 1.

01520-21

Figure 19. Signal-to-Total Distortion With Noise (Transmit Path—Method 1)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

$T_A = 0$ to 70°C, $V_{CC} = +5$ V ±5%, $V_{BB} = -5$ V ±5% (see Notes 1, 6 & 7)

No.	Parameter	Description	Min	Typ	Max	Units
Serial Interface Input Mode						
1	t_{DCH}	Data Clock High Pulse Width (Note 2)	0.220		20	µs
2	t_{DCL}	Data Clock Low Pulse Width (Note 2)	0.220			µs
3	t_{DCR}	Rise Time of Clock	5		50	ns
4	t_{DCF}	Fall Time of Clock	5		50	ns
5	t_{ICSS}	Chip Select Setup Time	175			ns
6	t_{ICSH}	Chip Select Hold Time	50			ns
7	t_{ICSL}	Chip Select Pulse Width (Notes 3 & 8)		8 t_{DCY}		ns
8	t_{ICSO}	Chip Select Off Time after byte written to or before byte read from B, Z, X, R, GX or GR in Active mode: Otherwise:	 32 t_{MCY} 7 t_{MCY}			
9	t_{IDS}	Input Data Setup Time	50			ns
10	t_{IDH}	Input Data Hold Time	30			ns
11	t_{OLH}	Output Latch Propagation Delay	0.75		2.1	µs
Serial Interface Output Mode						
12	t_{OCSS}	Chip Select Setup Time	150			ns
13	t_{OCSH}	Chip Select Hold Time	50			ns
14	t_{OCSL}	Chip Select Pulse Width (Notes 3 & 8)		8 t_{DCY}		ns
15	t_{OCSO}	Chip Select Off Time after byte written to or before byte read from B, Z, X, R, GX or GR in Active mode: Otherwise:	 32 t_{MCY} 7 t_{MCY}			
16	t_{ODD}	Output Data Turn on Delay			100	ns
17	t_{ODH}	Output Data Hold Time	30			ns
18	t_{ODOF}	Output Turn off Delay			100	ns
19	t_{ODC}	Output Data Valid	30		150	ns
PCM Interface						
20	t_{PCY}	PCM Clock Period (Note 4)	0.244		7.8	µs
21	t_{PCH}	PCM Clock High Pulse Width (Note 4)	110			ns
22	t_{PCL}	PCM Clock Low Pulse Width (Note 4)	110			ns
23	t_{PCF}	Fall Time of Clock	5		15	ns
24	t_{PCR}	Rise Time of Clock	5		15	ns
25	t_{FSS}	Frame Sync Setup Time	50		(t_{PCY} − 30)	ns
26	t_{FSH}	Frame Sync Hold Time (Companded Mode)	30		(8 t_{PCY} − 50)	ns
		Frame Sync Hold Time (Linear Mode)	30		(16 t_{PCY} − 50)	ns
27	t_{TSD}	Delay to TSC Valid (Note 5)	(N t_{PCY} + 30)		(N t_{PCY} + 150)	ns
28	t_{TSQ}	Delay to TSC Off (High Impedance)	30			ns
29	t_{DXD}	PCM Data Output Delay	95		185	ns
30	t_{DXH}	PCM Data Output Hold Time	30		100	ns
31	t_{DXZ}	PCM Data Output Delay to High Z	45		90	ns
32	t_{DRS}	PCM Data Input Setup Time	50			ns
33	t_{DRH}	PCM Data Input Hold Time	30			ns

SWITCHING CHARACTERISTICS (continued)

Master Clock

34	t_{MCY}	Master Clock Period	488.23	488.28	488.33	ns
35	t_{MCH}	Master Clock High Pulse Width	220			ns
36	t_{MCL}	Master Clock Low Pulse Width	238			ns
37	t_{MCR}	Rise Time of Clock	5		15	ns
38	t_{MCF}	Fall Time of Clock	5		15	ns

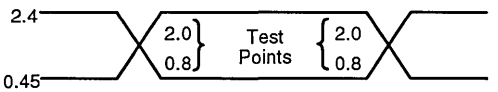
Notes: 1. Min and Max values are valid on all digital outputs except C_5–C_1 with a 150-pF load. C_5–C_1 outputs are valid with a 30-pF load.

2. The Data Clock may be stopped in the Low state indefinitely without loss of information. Data will not be clocked in or out while the clock is in the Low state.
3. Chip Select Pulse Width is nominally 8 Data Clock Cycles with a minimum value of 7 Data Clock Cycles + t_{ICSH} + t_{ICSS} and a maximum value of 9 Data Clock Cycles − t_{ICSH} − t_{ICSS}.
4. The maximum allowed PCM clock frequency is 4.096 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz.
5. $\overline{TSC}$ is delayed from FS by a typical value of N t_{PCY}, where N is the value stored in the Time/Clock Slot register.
6. The Frame Sync pulses (FSX, FSR) repeat at an 8-kHz rate.
7. FSR, FSX, CLKR, CLKX, and MCLK all must be synchronized and exactly 256 cycles of MCLK must be guaranteed between Frame Syncs. All five clocks must not be interrupted to assure proper operation.
8. t_{DCY} is 1 Data Clock Cycle.

SWITCHING WAVEFORMS

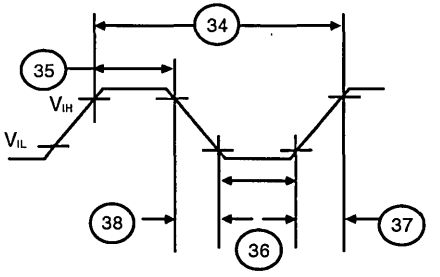
Timing Diagrams

Input and Output Waveforms For AC Tests



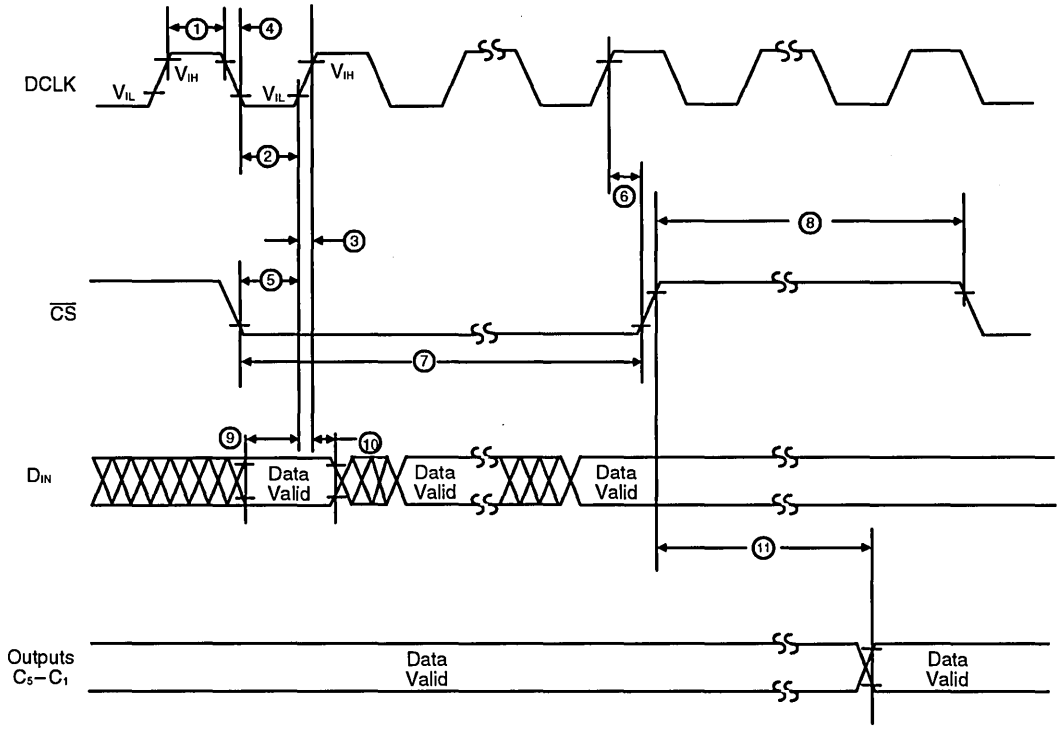
01520–22

Master Clock Timing



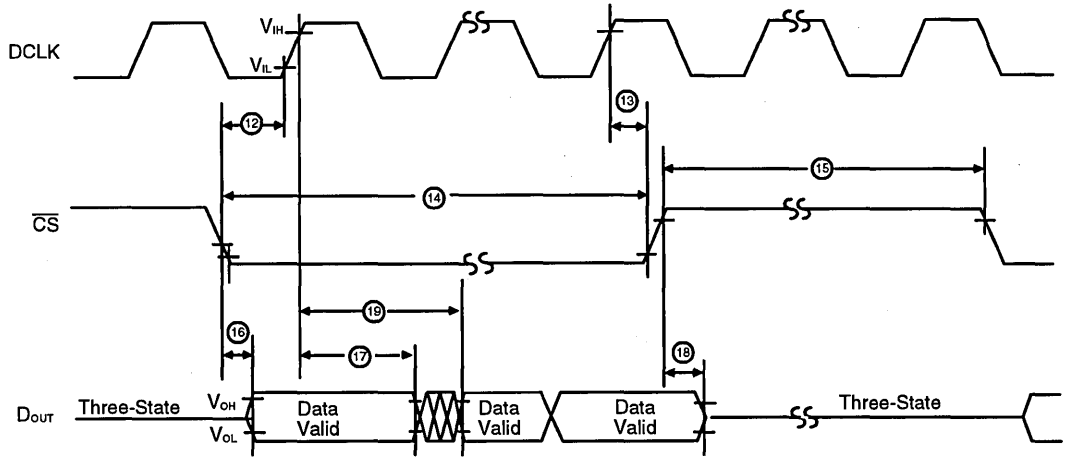
01520–23

Serial Interface (Input Mode)



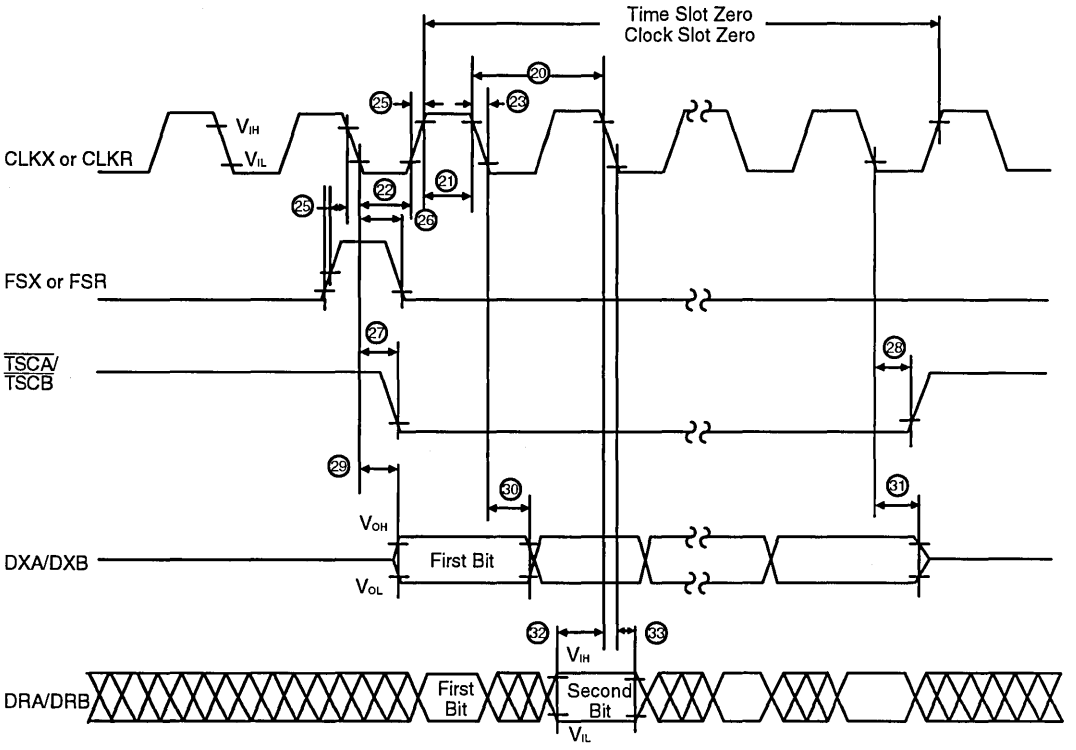
01520-24

Serial Interface (Output Mode)



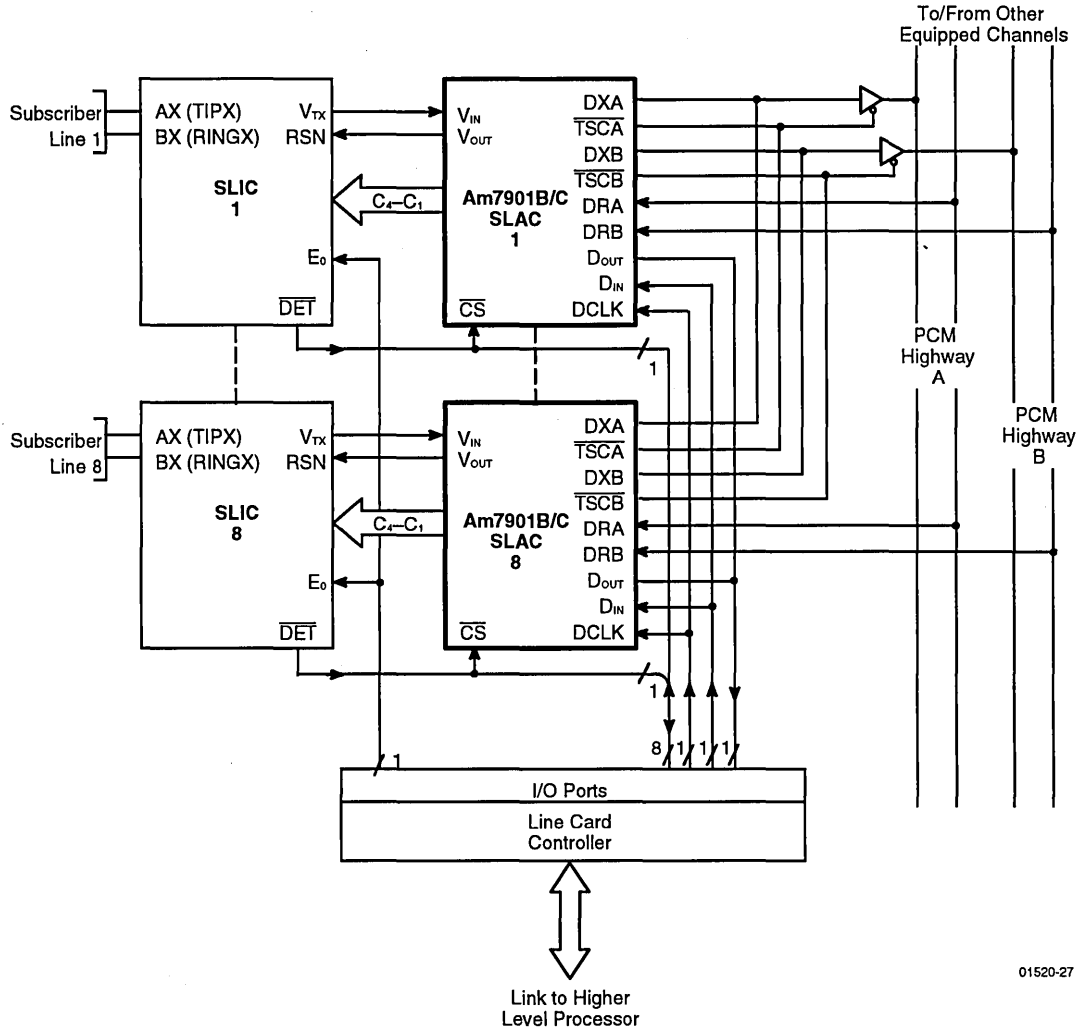
01520-25

PCM Highway Timing



01520-26

AMD 8-Channel Subscriber Line Card



Final

Am7905A

Subscriber Line Audio-Processing Circuit (SLAC) WORLD-CHIP

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

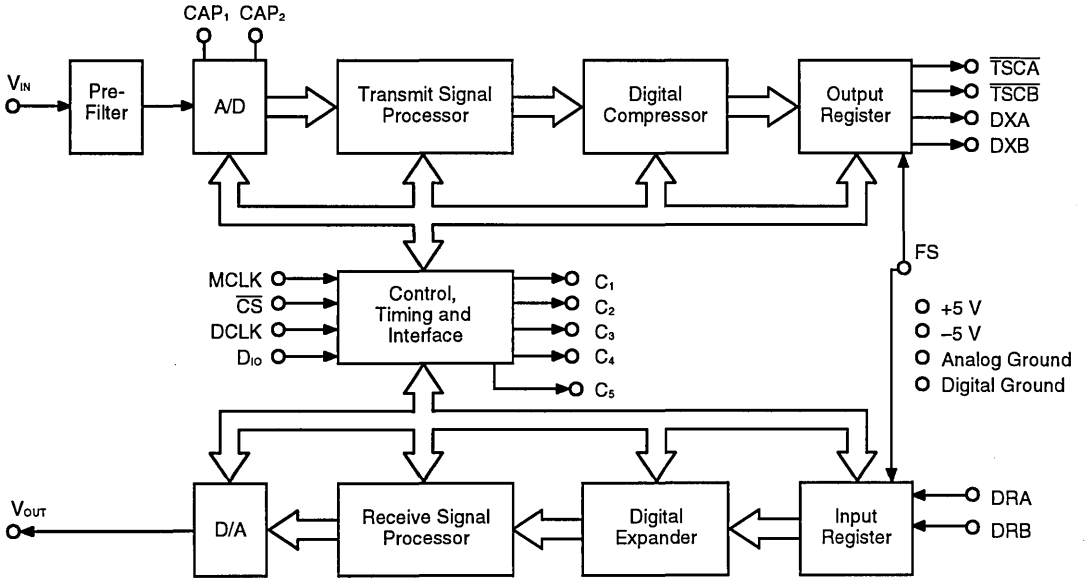
- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only two external components (non-precision)
- Dual PCM ports
- 4.096-MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable μ-law or A-law
- 24-pin DIPs

GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC™) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T® and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes. Either one of two output ports may be selected for PCM data transmission.

BLOCK DIAGRAM



07004B-01

GENERAL DESCRIPTION (continued)

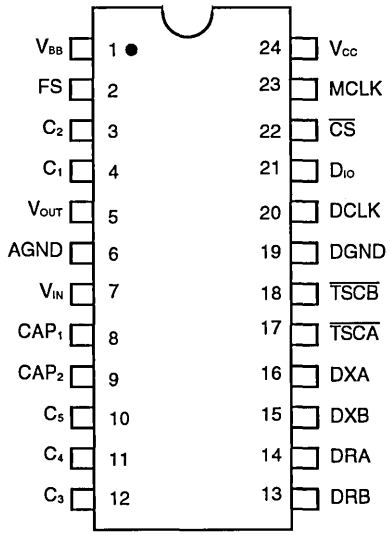
The receive section contains a digital signal processor and a D/A converter. Either 8-bit μ-law or A-law codes are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of commands.

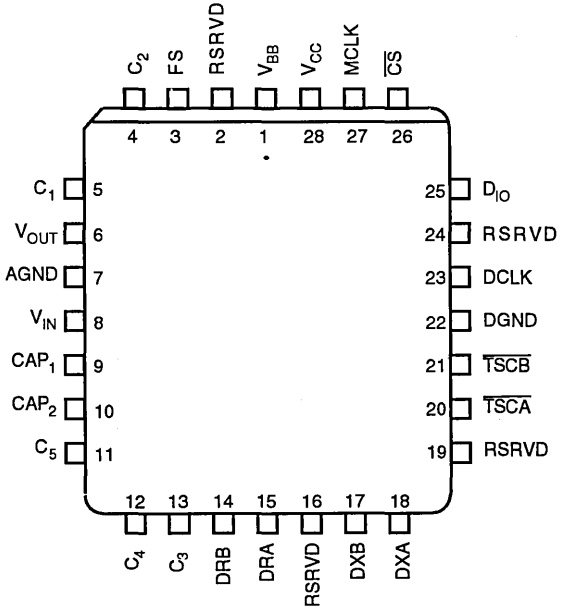
CONNECTION DIAGRAMS

Top View

24-Pin DIP

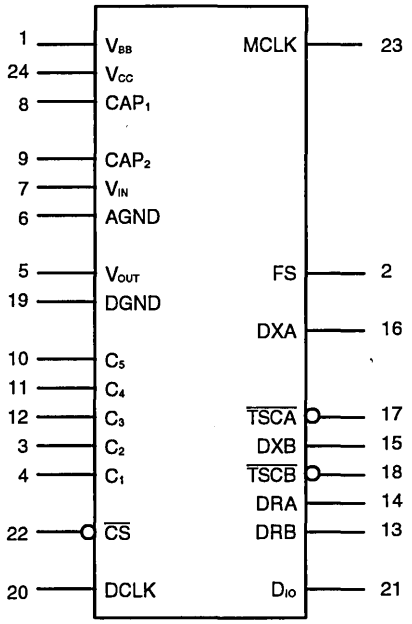


28-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



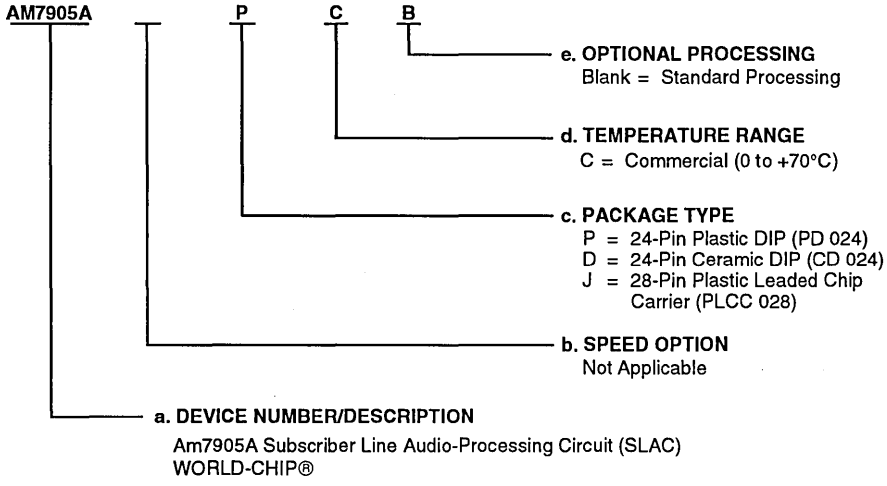
07004B-2

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7905A	PC, DC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTIONS

AGND
Analog ground.

C_5–C_1
Latched Outputs

The serial interface may be used to write data to a register whose outputs are brought out to C_5–C_1. These 5 lines are TTL-compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line. C_5 is used as an output in the Auto-zero Speedup Mode.

CAP_2, CAP_1
An external series resistor and capacitor are connected to these pins. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1K ohm ±5% and 2000 pF ±20%.

$\overline{CS}$
Chip Select

The Chip Select input enables the device to either input or output control data. A level of –5 V on this input places the device in the Auto-zero Speedup Mode.

DCLK
Data Clock

The Data Clock input shifts control data either into or out of the SLAC. The maximum clock rate is 2.048 MHz. A level of –5 V on this input forces the device into the Reset state.

D_{IO}
Data Input/Output

Control data is serially written and read via the Data Input/Output port. The input and output rate is determined by the Data Clock.

DGND
Digital ground.

DRA, DRB
PCM Inputs

The receive-PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For both μ-law and A-law, 8 bits are received. The data is received in 2.048- or 4.096-MHz bursts.

DXA, DXB
PCM Outputs

The transmit-PCM data is serially fed out to either the DXA or the DXB port. The port selection is under user program control. For both μ-law and A-law, 8 bits are transmitted. The output is available every 125 μs and the data is shifted out in 2.048-MHz or 4.096-MHz bursts. DXA and DXB are high impedance between bursts and also in the standby mode.

FS
Frame Sync

The Frame Sync pulse input is an 8-kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the Frame Sync pulse. The FS pulse must not be longer than 8-clock periods.

MCLK
Master Clock

The Master Clock is a 2.048- or 4.096-MHz ±100 ppm clock input. MCLK is used by the digital signal processors and by the PCM interface. Loss of MCLK should be treated like a loss of power.

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control

The Time Slot Control outputs are open-drain outputs and are normally High. $\overline{TSCA}$ is Low when PCM data is present on the DXA output and $\overline{TSCB}$ is Low when PCM data is present on the DXB output.

V_{BB}
–5-V power supply.

V_{CC}
+5-V power supply.

V_{IN}
Analog Input

The analog input is applied to the transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.

V_{OUT}
Analog Output

The received-PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.

FUNCTIONAL DESCRIPTION

Device Operation

General

The Am7905A performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. When used with the Am795XX Subscriber Line Interface Circuit (SLIC), the pair provide a complete solution to the BORSCHT (Battery feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid, and Test) functions (see Figure 1).

The SLAC contains auto-zeroed A/D and D/A converters. A microprocessor-compatible interface is provided to program the device into a variety of modes. These operating modes include companded operation, dynamic time-slot assignment, and PCM-port selection.

The SLAC samples the analog signal at the V_{IN} pin and digitally processes it to produce either a companded μ-law or A-law PCM code at the DXA or DXB output (see Figure 2). Conversely, it receives either a companded μ-law or A-law PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} pin. The processing is accomplished at the frame rate (8 kHz), and the digital output/input is available for transmission/reception every 125 μs.

Transmit Signal Processor

In the transmit path (see Figure 3), the analog signal is converted, filtered, compressed, and made available for output.

The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal-to-noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512-kHz sampling rate.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The B, X, and GX blocks shown in Figure 3 are user-programmable filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The decimator reduces the high input sample rate. The X filter is a 4-tap Finite Impulse Response (FIR) section and is part of the frequency response correction network. The GX filter allows the user to program up to 12-dB gain in the transmit path with an accuracy of ±0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB. The B filter has 8 taps and operates on sampled input from the Receive Signal Processor in order to provide trans-hybrid balancing in the loop. The low-pass filter limits the output bandwidth to meet the transmission requirements. The high-pass filter rejects 15-Hz and 50/60-Hz frequencies, and may be disabled for testing.

Transmit PCM Interface

The Transmit PCM interface receives either 8-bit compressed μ-law or A-law code from the digital compressor. This code is loaded into the output register. The Transmit PCM interface logic (see Figure 4) controls the transmission of data onto the PCM highway through the output port-selection circuitry and the Time Slot Control block.

The Frame Sync (FS) pulse identifies the beginning of a Transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers. The Time Slot register is normally 5 bits wide and allows up to thirty-two 8-bit channels (using MCLK = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give sixty-four 8-bit channels (using MCLK = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 64 is selected. This only applies if MCLK is 4.096 MHz. This feature allows clock frequencies of 2.048 or 4.096 MHz in a system. For μ-law and A-law operation, 8 bits/channel are output. The data is transmitted Most Significant Bit (MSB) first. The Clock Slot register is 3 bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 MCLK periods to eliminate any clock skew in the system (see Figure 5).

In the Am7905A, the PCM data may be user-programmed to be output onto one of two ports, DXA or DXB. Correspondingly, either $\overline{TSCA}$ or $\overline{TSCB}$ is also Low.

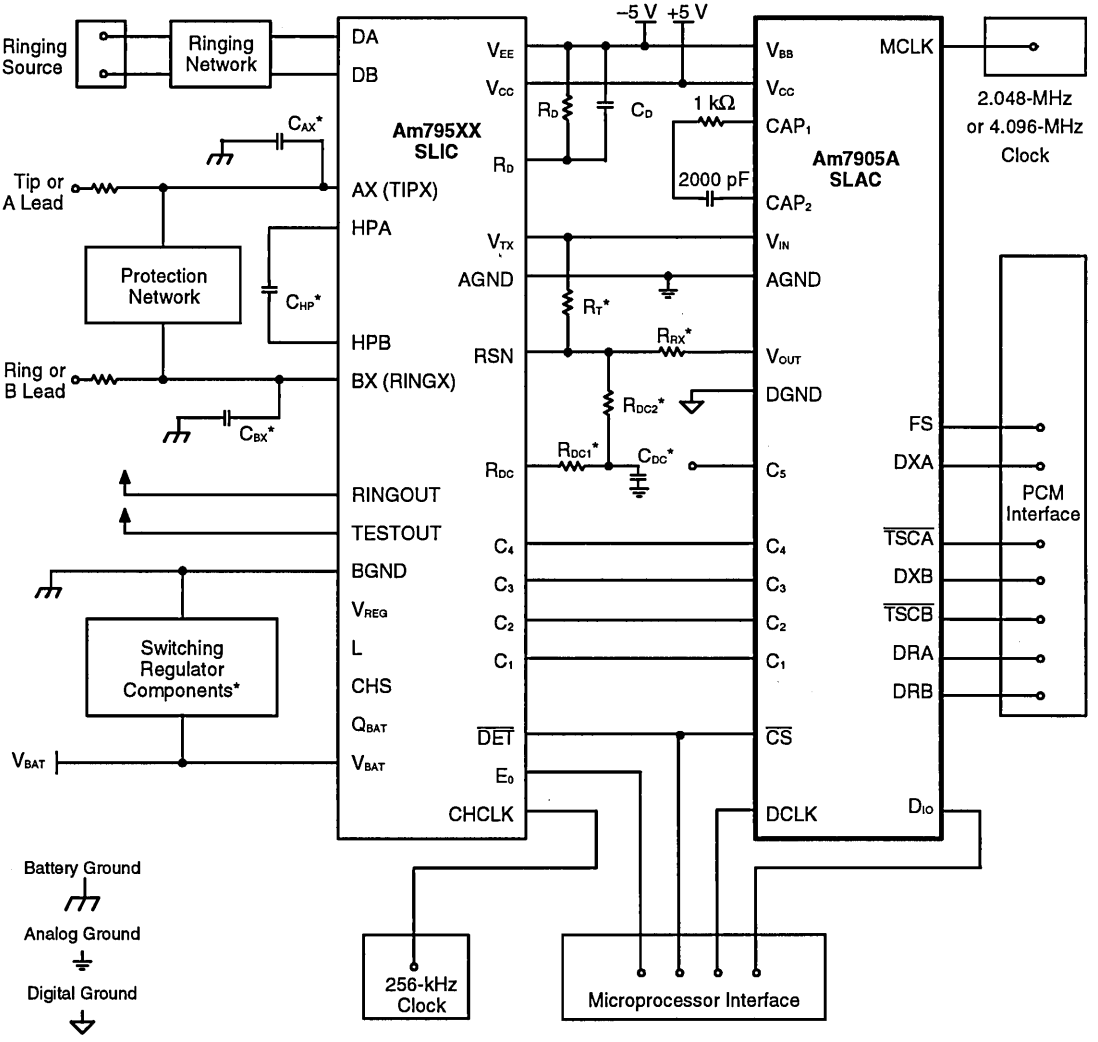
Receive PCM Interface

The Receive PCM interface logic (see Figure 6) controls the reception of data from the PCM highway and transfers it for expansion (μ-law or A-law) to the Receive Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FS) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it. The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is normally 5-bits wide and allows up to thirty-two 8-bit channels (using MCLK = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give sixty-four 8-bit channels (using MCLK = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 63 is selected. This only applies if MCLK is 4.096 MHz. This feature allows clock frequencies of 2.048 MHz or 4.096 MHz in a system. The MSB of the code must be

received first. The Clock Slot register is 3-bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 MCLK periods to eliminate any clock skews in the system (see Figure 7).

In the Am7905A, the PCM data may be user-programmed to be input from one of two ports, DRA or DRB.



* Component values are user-programmable. Refer to SLIC product specifications.

07004B-03

Figure 1. Single-Channel Subscriber Line System

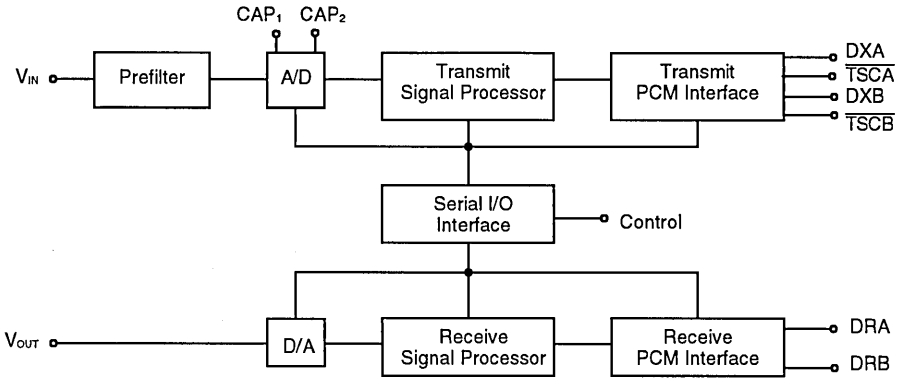
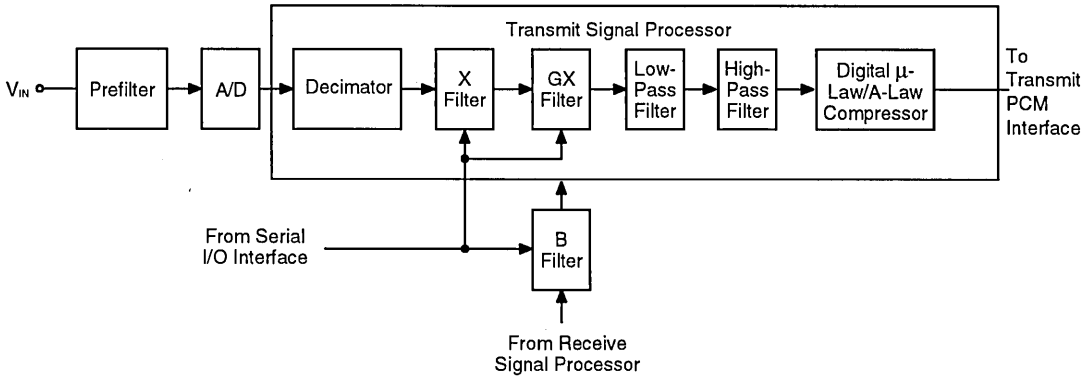


Figure 2. SLAC Block Diagram

07004B-04



07004B-05

Figure 3. Transmit Signal Processor

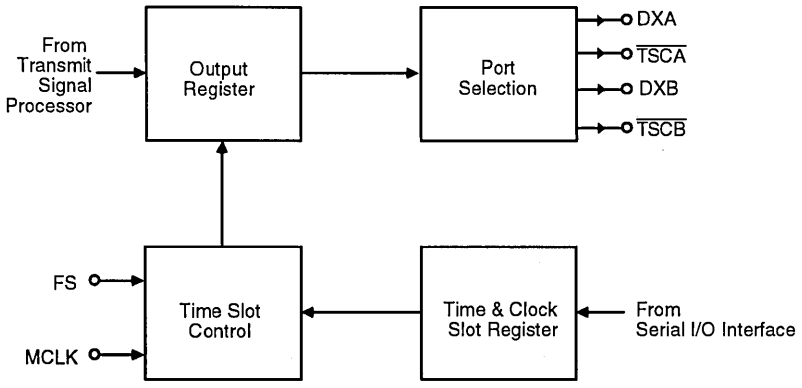


Figure 4. Transmit PCM Interface

07004B-06

Receive Signal Processor

In the receive path (see Figure 8), the digital signal is expanded, filtered, converted to analog, and output onto the V_{OUT} pin.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The Z, R and GR are user-programmable filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The low-pass filter band-limits the signal. The GR filter allows the user to program a loss of up to 12 dB with an accuracy of ±0.051 dB. The R filter is a 4-tap FIR section and is part of the frequency response correction network. The Z filter provides feedback from the Transmit Signal Processor to the Receive Signal Processor and is used to modify the effective input impedance to the system. The interpolator provides the higher sample rate to the D/A converter.

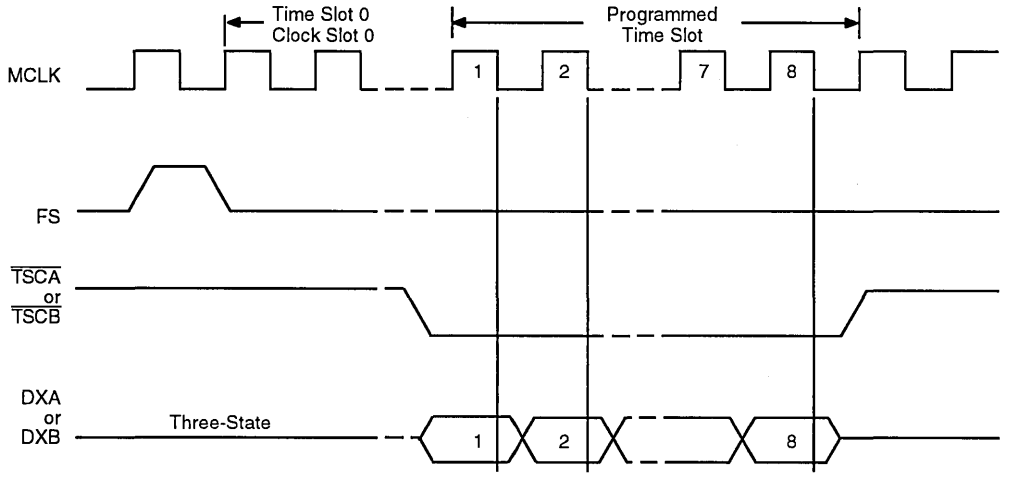
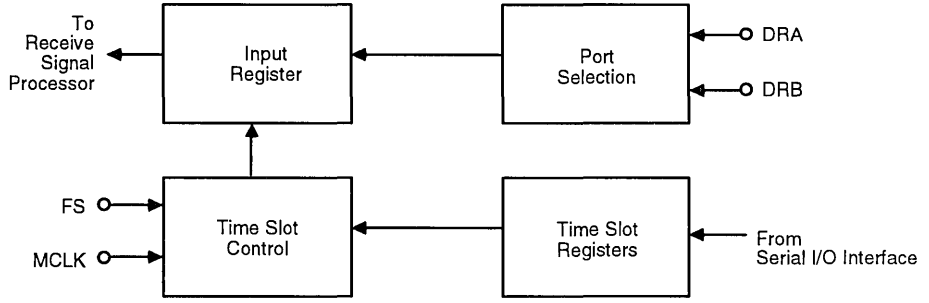


Figure 5. Transmit PCM Timing Diagram

07004B-07



07004B-09

Figure 6. Receive PCM Interface

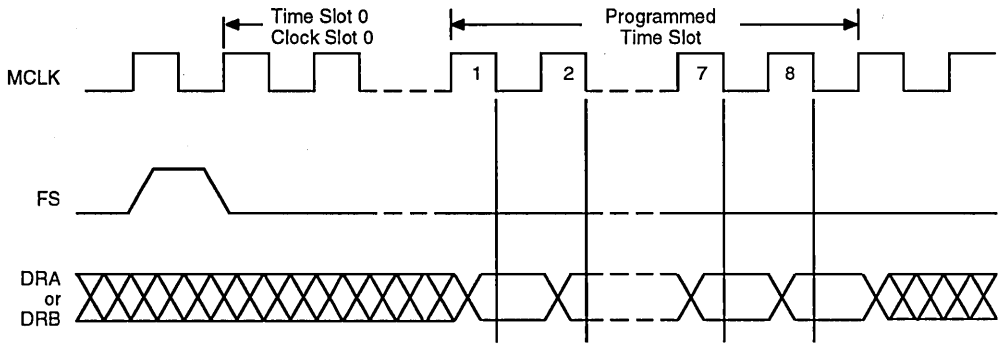
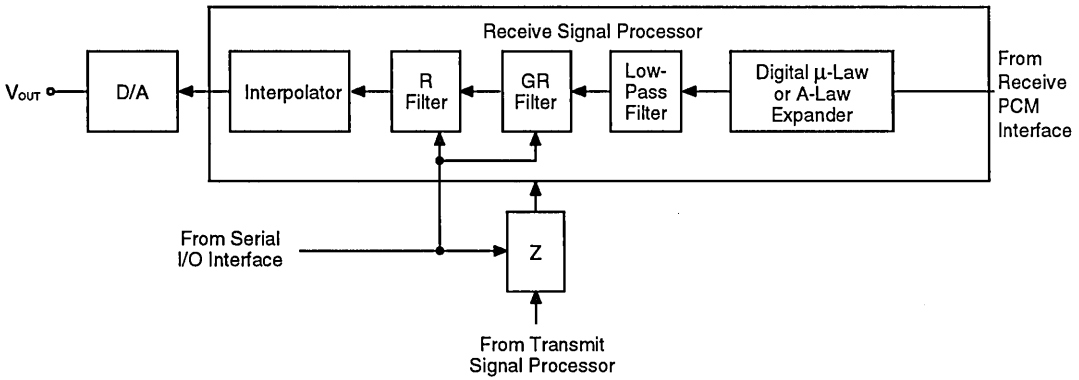


Figure 7. Receive PCM Timing Diagram

07004B-010



07004B-08

Figure 8. Receive Signal Processor

Serial I/O Interface

A microprocessor may be used to program the SLAC and control its operation using the Serial I/O Interface (see Figure 9). Additionally, data programmed previously may be read out for verification. The control word format is shown in Table 1. Commands are provided to:

- Set active/inactive modes
- Set up test functions
- Set up operating functions
- Program filter coefficients
- Assign time slots and port selection
- Write to the SLIC latch
- Enable/Disable each user-programmable filter

The interface consists of 3 pins, $\overline{CS}$, DCLK, and D_{IO}. The device is accessed by $\overline{CS}$ and data is serially loaded-in or read-out on D_{IO} under control of DCLK. Either commands or data words may be written to the SLAC, but only data words can be read out. All words are 8-bits wide and are written or read MSB first (see Figure 10).

For both reception or transmission of words, exactly 8 Data Clock cycles must be received after $\overline{CS}$ goes Low. $\overline{CS}$ must stay High (off period) for a minimum time period before it can go Low again (see Note 4 under Switching Characteristics). During this off-period, the logic decodes and executes the command. All reading of data by the SLAC must be preceded by an input command requesting the data. Once control data transmission has begun, no new input commands will be accepted until control data transmission is completed.

A Serial I/O cycle is defined by transitions of $\overline{CS}$ and DCLK. Upon proper application of power supplies and MCLK, the device expects the first word to be a command. A number of commands require additional data words to be input or output. The SLAC will not accept new commands until all this data has been transferred.

There are two possible operations of DCLK and $\overline{CS}$ for the SLAC to function correctly. If the $\overline{CS}$ is held in the High state between accesses, the DCLK may free run with no change to the internal control data. Using this method, the same DCLK may be run to a number of SLACs and individual $\overline{CS}$ lines will select the appropriate device to access. If the DCLK is held in the Low state between accesses, the $\overline{CS}$ line may make multiple transitions between accesses for a particular SLAC. This allows running one $\overline{CS}$ line to all SLACs and selecting a particular device through enabling or disabling its DCLK.

It should be noted that the DCLK can stay in the Low state indefinitely with no loss of internal control information. However, it should not be held in the High state for more than 20 µs to ensure proper operation as indicated by the Switching Characteristics Table.

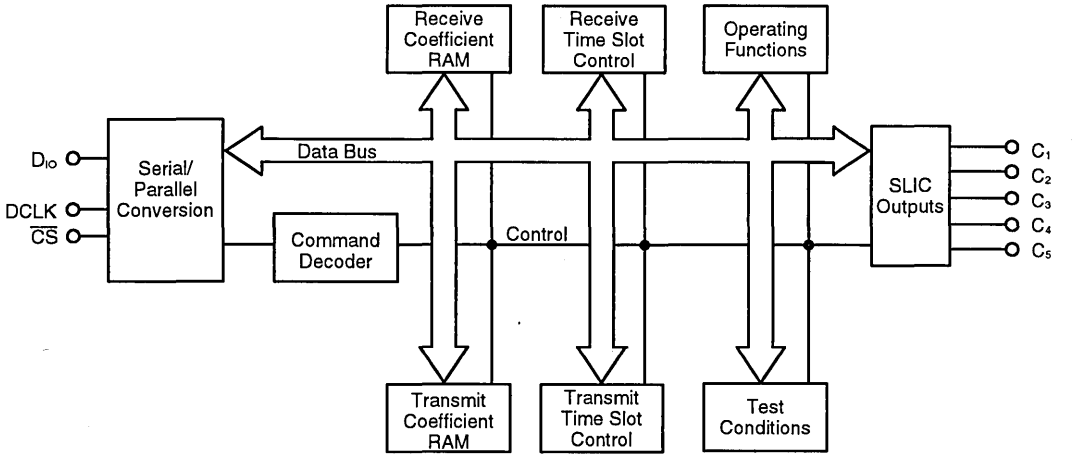


Figure 9. Serial I/O Interface

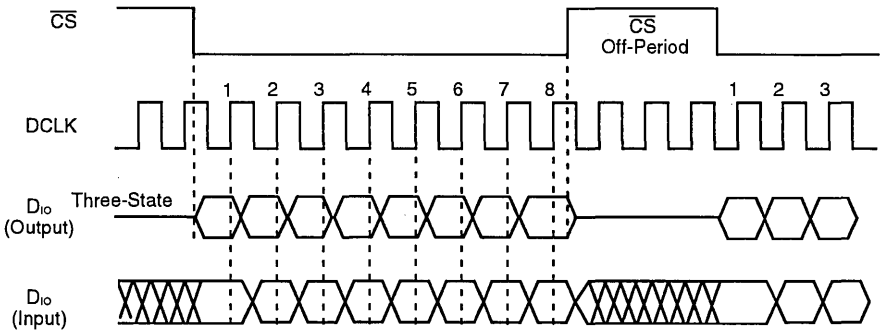


Figure 10. Serial I/O Interface Timing Diagram

Table 1. Command Summary

The Serial I/O Interface consists of Data Input/Output, Data Clock and $\overline{CS}$ Input. Data is read in (read out) on the Serial Data Input (output). The Serial Input consists of 8-bit (byte) command words which may be followed with additional bytes of input data or may be followed by the SLAC outputting bytes of data. All words are input with MSB (D_7) first and LSB (D_0) last. All outputs are output with the MSB (D_7) first and the LSB (D_0) last. Words are written or read one at a time, with $\overline{CS}$ going High for at least the minimum off-period (see Switching Characteristics) before the next read or write operation. The first 3 bits of the command word indicate the type of command and the last 5 bits contain either data or further information about the command. The classes of command are:

D_7	D_6	D_5	
0	0	0	Inactivate/No Operation
0	0	1	Transmit Time Slot Selection
0	1	0	Receive Time Slot Selection
0	1	1	Clock Slot and Gain Selection Read Slot, Gain and PCM Mode
1	0	0	Set Basic and Operating Functions and PCM Modes
1	0	1	Read/Write Coefficients, Set Test Modes, Select μ-law/A-law
1	1	0	Data for SLIC Interface
1	1	1	Activate/No Operation

MSB	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LSB	
	0	0	0	0	0	0	0	0	Inactivate	
	0	0	1	T	T	T	T	T	Transmit Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	0	T	T	T	T	T	Receive Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	1	0	0	C	C	C	Transmit Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	0	1	C	C	C	Receive Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	1	0	0	1	0	Transmit Gain Selection (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	0	1	0	Receive Gain Selection (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	0	1	Read Transmit Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	0	0	0	1	Read Transmit Gain (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	1	0	1	Read Receive Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	1	0	0	1	Read Receive Gain (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	1	1	Read PCM Mode	Followed by 1 Byte of Data
	1	0	0	0	B	X	R	Z	Enable Filters	
	1	0	0	1	D_R	D_X	R_{EX}	T_{EX}	PCM-Mode Selection	
	1	0	1	0	0	0	0	0	Write B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	0	0	Write X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	0	0	Write R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	0	0	Write Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	0	0	1	1	Read B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	1	1	Read X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	1	1	Read R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	1	1	Read Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	1	0	0	0	0	Reset to normal conditions	
	1	0	1	1	0	0	0	1	Add –6 dB to receive gain	
	1	0	1	1	0	0	1	0	Cutoff receive path	
	1	0	1	1	0	1	1	1	Test mode–analog loop-back	
	1	0	1	1	0	1	0	0	Test mode–digital loop-back	
	1	0	1	1	0	0	1	1	Disable High-Pass Filter (set to 1) and freeze auto-zero circuit	
	1	0	1	1	1	0	0	0	Choose A-law	
	1	0	1	1	1	0	0	1	Choose μ-law	
	1	0	1	1	1	1	1	0	Set device to operate with MCLK = 2.048 MHz	
	1	0	1	1	1	1	1	1	Set device to operate with MCLK = 4.096 MHz	
	1	1	0	C	C	C	C	C	Outputs to SLIC	
	1	1	1	1	1	1	1	1	Activate	

Am7905A Detailed Serial Command Definitions

Inactivate (Standby Mode)

MSB							LSB
0	0	0	0	0	0	0	0

In the inactive mode, none of the programmed information is changed and the analog output is set to 0 V through a moderate series impedance. The Serial I/O remains active, the SLIC control outputs remain valid, and the PCM outputs are high impedance.

Activate (Operational Mode)

MSB							LSB
1	1	1	1	1	1	1	1

Valid PCM data is not transmitted until after the second FS pulse is received following the execution of the Activate command.

Transmit Time Slot Selection

MSB							LSB
0	0	1	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Transmit Clock Slot Selection

MSB							LSB
0	1	1	0	0	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Transmit Time and Clock Slots

Command

MSB							LSB
0	1	1	1	0	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The transmit time and clock slots are read out time slot first, followed by clock slot.

Receive Time Slot Selection

MSB							LSB
0	1	0	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Receive Clock Slot Selection

MSB							LSB
0	1	1	0	1	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Receive Time and Clock Slots

Command

MSB							LSB
0	1	1	1	1	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The receive time and clock slots are read out time slot first, followed by clock slot.

Write GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	1	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Read GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	0	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Write GR Filter Coefficients

Command

MSB							LSB
0	1	1	1	1	0	1	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Read GR Filter Coefficients

Command

MSB							LSB
0	1	1	1	1	0	0	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Write PCM Mode Selection

MSB							LSB
1	0	0	1	D_R	D_X	R_{EX}	T_{EX}

Receive Port: $D_R = 0$: PCM data is input on DRA.
$D_R = 1$: PCM data is input on DRB.

Transmit Port: $D_X = 0$: PCM data is output on DXA.
$D_X = 1$: PCM data is output on DXB.

Receive Expanded Mode: $R_{EX} = 0$: Reset Receive Expanded Mode.
$R_{EX} = 1$: Set Receive Expanded Mode.

Transmit Expanded Mode: $T_{EX} = 0$: Reset Transmit Expanded Mode.
$T_{EX} = 1$: Set Transmit Expanded Mode.

Read PCM Mode Selection

Command

MSB							LSB
0	1	1	1	0	1	1	1

Output Data

1	1	1	1	D_R	D_X	R_{EX}	T_{EX}

Enable Filters

MSB							LSB
1	0	0	0	EB	EX	ER	EZ

B Filter: EB = 0: B filter disabled.
EB = 1: B filter enabled.

X Filter: EX = 0: X filter disabled.
EX = 1: X filter enabled.

R Filter: ER = 0: R filter disabled.
ER = 1: R filter enabled.

Z Filter: EZ = 0: Z filter disabled.
EZ = 1: Z filter enabled.

Write Test Mode Selection

MSB							LSB
1	0	1	1	0	T_3	T_2	T_1

T3	T2	T1	Function
0	0	0	Reset to normal conditions as follows. Receive gain is set to the value stored in the GR register. Analog and digital loopback modes are reset. The high-pass filter is enabled and the auto-zero circuit is operational. The receive path is not cutoff.
0	0	1	Add –6 dB to receive gain.
0	1	0	Cutoff receive path.
0	1	1	Disable high-pass filter (set to 1) and freeze auto-zero circuit.
1	0	0	Activate digital loopback.
1	1	1	Activate analog loopback.

Select PCM Coding

MSB							LSB
1	0	1	1	1	0	0	B

Bit B selects the type of PCM code to be used.

For the Am7905A: B = 0: A-Law.

B = 1: μ-Law.

Write SLIC Output Registers

MSB							LSB
1	1	0	C_5	C_4	C_3	C_2	C_1

Write B Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	0	0	0

Input Data

C_{30} m_{30}	C_{20} m_{20}	Byte 1
C_{10} m_{10}	C_{31} m_{31}	Byte 2
C_{21} m_{21}	C_{11} m_{11}	Byte 3
C_{32} m_{32}	C_{22} m_{22}	Byte 4
C_{12} m_{12}	C_{33} m_{33}	Byte 5
C_{23} m_{23}	C_{13} m_{13}	Byte 6
C_{34} m_{34}	C_{24} m_{24}	Byte 7
C_{14} m_{14}	C_{35} m_{35}	Byte 8
C_{25} m_{25}	C_{15} m_{15}	Byte 9
C_{36} m_{36}	C_{26} m_{26}	Byte 10
C_{16} m_{16}	C_{37} m_{37}	Byte 11
C_{27} m_{27}	C_{17} m_{17}	Byte 12

Read B Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	0	1	1

Output Data

C_{30} m_{30}	C_{20} m_{20}	Byte 1
C_{27} m_{27}	C_{17} m_{17}	Byte 12

Write X Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	1	0	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2
C_{41} m_{41}	C_{31} m_{31}	Byte 3
C_{21} m_{21}	C_{11} m_{11}	Byte 4
C_{42} m_{42}	C_{32} m_{32}	Byte 5
C_{22} m_{22}	C_{12} m_{12}	Byte 6
C_{43} m_{43}	C_{33} m_{33}	Byte 7
C_{23} m_{23}	C_{13} m_{13}	Byte 8

Read X Filter Coefficients

Command

MSB							LSB
1	0	1	0	0	1	1	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 8

Write R Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	0	0	0

Input Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 2
C_{42} m_{42}	C_{32} m_{32}	Byte 3
C_{22} m_{22}	C_{12} m_{12}	Byte 4
C_{41} m_{41}	C_{31} m_{31}	Byte 5
C_{21} m_{21}	C_{11} m_{11}	Byte 6
C_{40} m_{40}	C_{30} m_{30}	Byte 7
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Read R Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	0	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Write Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	0	0

Input Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 2
C_{42} m_{42}	C_{32} m_{32}	Byte 3
C_{22} m_{22}	C_{12} m_{12}	Byte 4
C_{41} m_{41}	C_{31} m_{31}	Byte 5
C_{21} m_{21}	C_{11} m_{11}	Byte 6
C_{40} m_{40}	C_{30} m_{30}	Byte 7
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Read Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Select MCLK Frequency

MSB							LSB
1	0	1	1	1	1	1	C

Bit C selects the MCLK frequency to be used.

C = 0: MCLK = 2.048 MHz
C = 1: MCLK = 4.096 MHz

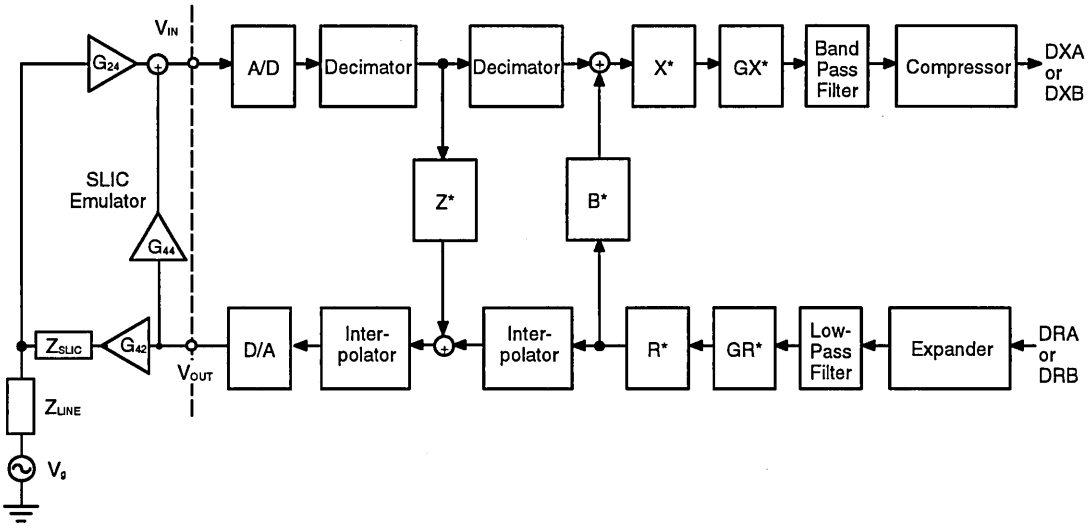


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Figure 11. SLAC Signal Processing Flow

Digital Filters

The SLAC uses digital signal processing to implement the various filters (see Figure 11).

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance

Six of the digital filters in the signal processing sections are user-programmable. These allow the user to independently modify the gain in both the transmit and receive paths, provide trans-hybrid balancing in the system, and adjust the two-wire line termination impedance. This programming capability feature allows the user to optimize the performance of the SLAC for his system.

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the SLAC is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \quad (1)$$

where the number of taps in the filter = n + 1.

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_I = B_1 2^{-M1} + B_2 2^{-M2} + \ldots + B_N 2^{-MN}, \quad (2)$$

where:

the number of shifts = $M_I \leq M_{I+1}$

sign = $B_I = \pm 1$

N = Number of CSD coefficients.

The value of h_i in (2) represents a decimal number which is broken down into a sum of successive values of:

± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 ... 1/128....

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 2 can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the

rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take; for example, if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4.

Detailed Description of SLAC Coefficients

The CSD coding scheme in the SLAC uses a value called m_i, where m_1 represents the distance shifted right of the decimal point for the first binary 1, m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 2 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + B_3 2^{-M3} + B_4 2^{-M4} \quad (3)$$

$$h_i = C_1 2^{-m1} + C_1 C_2 2^{-(m1+m2)} + C_1 C_2 C_3 2^{-(m1+m2+m3)} + C_1 C_2 C_3 C_4 2^{-(m1+m2+m3+m4)} \quad (4)$$

$$h_i = C_1 2^{-m1} \cdot [1 + C_2 2^{-m2} \cdot \{1 + C_3 2^{-m3} \cdot (1 + C_4 2^{-m4})\}] \quad (5)$$

where:

$M_1 = m_1$	and	$B_1 = C_1$
$M_2 = m_1 + m_2$		$B_2 = C_1 \cdot C_2$
$M_3 = m_1 + m_2 + m_3$		$B_3 = C_1 \cdot C_2 \cdot C_3$
$M_4 = m_1 + m_2 + m_3 + m_4$		$B_4 = C_1 \cdot C_2 \cdot C_3 \cdot C_4$

In the SLAC, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is 3 bits. Each CSD coefficient is broken down as follows:

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000:	illegal
001:	6 shifts
010:	5 shifts
011:	4 shifts
100:	3 shifts
101:	2 shifts
110:	1 shift
111:	0 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, and Z filter, and 3 for the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters:

$$h_{iGX} = 1 + h_i \quad (6)$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Two-Wire Impedance Matching

A feedback path is provided from the transmit to the receive section via the Z filter. This filter may be programmed to modify the effective termination impedance (Z_{SLIC}) of a SLIC or a transformer hybrid to a desired value. The desired impedance may be complex. This feature allows the user to terminate each SLIC in a Subscriber Line System with a fixed resistor and digitally modify their impedance using the Z filter.

The X and R filters are the Transmit and Receive attenuation distortion correction filters. These filter sections are programmed to compensate the attenuation distortion caused by the Z filter.

Trans-Hybrid Balance

In a traditional line card system, a balance network is used with the SLIC to achieve trans-hybrid balancing. If the balance network perfectly matches the subscriber's line, infinite trans-hybrid balancing is achieved. But in general, the matching in traditional systems is poor and trans-hybrid balancing is not very good. Some systems have up to 2 or 3 compromise networks per line that must be selected semi-automatically or manually to provide the balance.

In the SLAC, a feedback path is provided from the receive to the transmit section via the B filter. This filter may be programmed to cancel the received signal from the transmit signal path and achieve a significantly improved level of trans-hybrid balance.

Gain Adjustment

Signal levels in the transmit and receive paths may be modified by programming the GX and GR filters. The GX

filter allows the user to add up to 12 dB of gain (with an accuracy of 0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB) in the transmit path. The GR filter allows the user to add up to 12 dB of loss (with an accuracy of ±0.051 dB) in the receive path.

Test Features

The SLAC simplifies system testing by providing both digital and analog loop-back paths. Under program control, either the DRA or DRB input is looped to the DXA or DXB output (digital loop-back) through a path from the output of the interpolator in the receive path to the input of the decimator in the transmit path. The V_{IN} input is looped to the V_{OUT} output (analog loop-back) through the Z filter. To allow testing of the subscriber loop cabling for leakage, the transmit high pass filter may be disabled and auto zero operation interrupted. The receive analog output may be programmed to open-circuit or cut off the receive path. This receive cut-off command may be used to stop oscillations in the four-wire side of the telephone network.

The SLAC contains an auto-zero circuit in the A/D converter which takes several seconds to settle following a change in the offset voltage at V_{IN}. To facilitate component testing of the SLAC, there is a test mode available to accelerate settling of the auto-zero circuit. This test mode is activated by holding the CS input at –5 V for at least 64 ms with the offset voltage applied to V_{IN} (and no signal). The auto-zero will settle in this time. In a component test environment, this procedure should be followed after programming the filters.

Note: The digital loopback (DLB) path processes an internal data word 2-bits shorter than in normal mode. Therefore, DLB signal processing performance is not equivalent to normal mode signal processing and does not meet the specified transmission specifications. DLB is recommended for use with 0 dB programmed gain/attenuation and PCM signal levels above –25 dBm0.

Standby Mode

The SLAC is forced into the standby mode either by a hardware reset applied to the DCLK input or by reception of the Inactivate command. In this mode, power is switched off from all circuitry that can be turned off. No transmission or reception of PCM data takes place. However, the circuits which contain programmed information retain their data. The Serial I/O Interface remains active to receive new commands.

Power-On Clear

Before any other commands are written to the SLAC, 13 Inactivate commands should be sent to the serial port of the SLAC in case the SLAC powers up in the middle of a read sequence. Alternatively, a hardware reset operation can be carried out by applying –5 V to the DCLK pin. A loss of MCLK should be treated like a loss of power.

Stand-Alone Mode

In the stand-alone mode, the serial interface is not used. The DCLK and D_{IO} pins may be used to control the device. Applying –5 V to the DCLK pin resets the device and the D_{IO} pin can subsequently be used to power-up or power-down the SLAC.

DCLK	D_{IO}	
0	X	Normal Mode
1	X	Normal Mode
–5 V	0	Reset and Power-Down
–5 V	1	Reset and Power-Up

Reset State

The Reset State of the device is:

a. Both Transmit and Receive, Time and Clock Slots are set to 0.

b. A-law is selected.

c. B, X, R, Z filters are disabled.

d. Both Transmit (GX) and Receive (RX) gains are set to unity.

e. SLIC outputs (C_5–C_1) are set High.

f. Normal conditions are selected.

g. DXA/DRA ports are selected.

h. Device operates with 2.048-MHz clock only.

μ-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number *n*	Decision Value x_n (1)	Character Signal (5) Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		8159	(128)	(8159)			
8	16×256		127 ⋮ 113	7903 ⋮ 4319	1 0 0 0 0 0 0 0 ⋮ (2)	8031 ⋮	127 ⋮
7	16×128	4063	112 ⋮ 97	4063 ⋮ 2143	1 0 0 0 1 1 1 1 ⋮ (2)	4191 ⋮	112 ⋮
6	16×64	2015	96 ⋮ 81	2015 ⋮ 1055	1 0 0 1 1 1 1 1 ⋮ (2)	2079 ⋮	96 ⋮
5	16×32	991	80 ⋮ 65	991 ⋮ 511	1 0 1 0 1 1 1 1 ⋮ (2)	1023 ⋮	80 ⋮
4	16×16	479	64 ⋮ 49	479 ⋮ 239	1 0 1 1 1 1 1 1 ⋮ (2)	495 ⋮	64 ⋮
3	16×8	223	48 ⋮ 33	223 ⋮ 103	1 1 0 0 1 1 1 1 ⋮ (2)	231 ⋮	48 ⋮
2	16×4	95	32 ⋮ 17	95 ⋮ 35	1 1 0 1 1 1 1 1 ⋮ (2)	99 ⋮	32 ⋮
1	15×2	31	16 ⋮ 2	31 ⋮ 3	1 1 1 0 1 1 1 1 ⋮ (2)	33 ⋮	16 ⋮
	1×1		1	1	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1	2 0	1 0
			0	0			

Notes:
1. 8159 normalized value units correspond to $T_{MAX} = 3.17$ dBm0.
2. The character signal corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
3. The value at the decoder is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, \ldots, 127$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

A-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal Before Inversion of the Even Bits Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		4096	(128)	(4096)	- - - - - - - - - -		
			127	3968	1 1 1 1 1 1 1 1	4032	128
7	16×128		⋮	⋮	⋮ (2)	⋮	⋮
			113	2176	1 1 1 1 0 0 0 0	2112	113
		2048	112	2048	⋮ (2)	⋮	⋮
6	16×64		⋮	⋮	1 1 1 0 0 0 0 0	1056	97
			97	1086	⋮ (2)	⋮	⋮
		1024	96	1024	1 1 0 1 0 0 0 0	528	81
5	16×32		⋮	⋮	⋮ (2)	⋮	⋮
			81	544	1 1 0 0 0 0 0 0	264	65
		512	80	512	⋮ (2)	⋮	⋮
4	16×16		⋮	⋮	1 0 1 1 0 0 0 0	132	49
			65	272	⋮ (2)	⋮	⋮
		256	64	256	1 0 1 0 0 0 0 0	66	33
3	16×8		⋮	⋮	⋮ (2)	⋮	⋮
			49	136	1 0 0 0 0 0 0 0	1	1
		128	48	128	⋮ (2)		
2	16×4		⋮	⋮			
			33	68			
		64	32	64			
1	32×2		⋮	⋮			
↓			1	2			
			0	0			

Notes:
1. 4096 normalized value units correspond to $T_{MAX} = 3.14$ dBm0.
2. The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (128 + n) expressed as a binary number.
3. The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for $n = 1, \ldots, 127, 128$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –60 to 125°C
Ambient Temperature under Bias ..... 0 to 70°C
V_{CC} with respect to DGND ..... –0.4 to +6.0 V
V_{BB} with respect to DGND ..... +0.4 to –6.0 V
V_{IN} with respect to AGND ..... V_{BB} to V_{CC}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) ..... 0 to 70°C
V_{CC} ..... +5.0 V ±5%
V_{BB} ..... –5.0 V ±5%
DGND ..... 0 V
AGND ..... DGND ±100 mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (Note 1) unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Z_{IN}	Analog Input Impedance	–3.2 V < V_{IN} < 3.2 V	20			kΩ
Z_{OUT}	Analog Output Impedance	–3.2 V < V_{OUT} < 3.2 V			20	Ω
V_{IOS}	Offset Voltage Allowed on V_{IN}				±40	mV
V_{OOS}	Analog Output Offset Voltage				±30	mV
V_{IR}	Analog Input Voltage Range				±3.2	V
V_{OR}	Analog Output Voltage Range	$R_L \geq 10$ kΩ, $C_L \leq 50$ pF			±3.2	V
I_{OUT}	Analog Output Current		350			µA
V_{IL}	Input Low Voltage (All Digital Inputs Except DCLK in Stand Alone Mode and $\overline{CS}$ in Auto-zero Speedup Mode)		–0.5		0.8	V
V_{IH}	Input High Voltage (All Digital Inputs)		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (All Digital Outputs)	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage (All Outputs Except TSC)	I_{OH} = 400 µA	2.4			V
I_{OL}	Output Leakage Current				±10	µA
I_{IL}	Input Leakage Current				±1	µA
I_{IL} (V_{IN})	Input Leakage Current on V_{IN} Pin				±0.2	µA
I_{CC} (S)	V_{CC} Supply Current (Standby)	V_{CC} = 5.25 V V_{BB} = –4.75 V			15	mA
I_{BB} (S)	V_{BB} Supply Current (Standby)				10	mA
I_{CC} (A)	V_{CC} Supply Current (Active)				60	mA
I_{BB} (A)	V_{BB} Supply Current (Active)				20	mA
PSRR	V_{CC} Power Supply Rejection Ratio	200 mV p-p @ 1.02 kHz on the appropriate supply, V_{CC} = +5 V, V_{BB} = –5 V	35			dB
PSRR	V_{BB} Power Supply Rejection Ratio		30			dB
C_I	Input Capacitance (Digital)			5		pF
C_O	Output Capacitance (Digital)			8		pF

Note: 1. Typical values are for T_A = 25°C and nominal supply voltages. Min and max specifications are over the temperature and supply voltage ranges shown in the above table entitled "Operating Ranges."

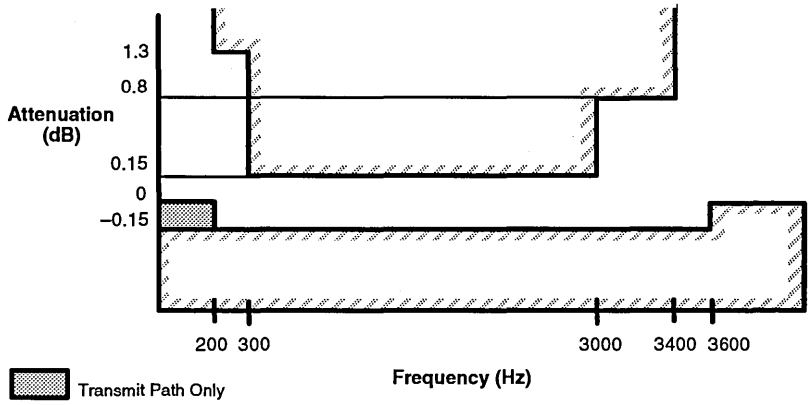
TRANSMISSION CHARACTERISTICS

All specifications are guaranteed with 0 dB ≤ GX ≤ +12 dB, −12 dB ≤ GR ≤ 0 dB and A-law or μ-law companded PCM, unless otherwise specified.

When GR = 0 dB, a 1020-Hz sine wave signal with level of 0 dBm0 at the digital input will correspond to an rms voltage of 1.6 V for A-law and 1.588 V for μ-law at the analog output. When GX = 0 dB, a 1020-Hz sine wave signal with rms voltage of 1.569 V for A-law and 1.557 V for μ-law at the analog input will correspond to a level of 0 dBm0 at the digital output.

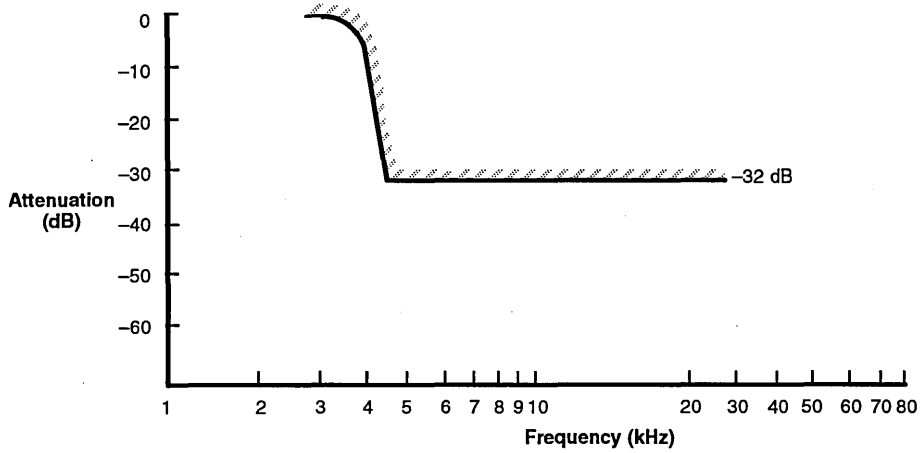
Description	Test Conditions	Min	Typ	Max	Units
Attenuation Distortion	1020 Hz @ −10 dBm0		(see Fig. 12)		
Gain (either path) a. Deviation from ideal value b. Deviation from initial value	1020 Hz @ −10 dBm0	 −0.2 −0.2		 +0.2 +0.2	 dB dB
Group Delay Distortion (either path)	−10 dBm0 signal		(see Fig. 14)		
Harmonic Distortion	(Note 1)			−40	dB
Intermodulation Distortion	a. (Note 2) b. (Note 3)			−35 −49	dB dBm0
Crosstalk a. Go-to-Return Path b. Return-to-Go path	 300–3400 Hz, 0 dBm0 300–3400 Hz, 0 dBm0		 −90 −90	 −70 −70	 dB dB
Gain Tracking (either path)			(see Fig. 15 & 17)		dB
Signal to Total Distortion (either path)			(see Fig. 16, 18, & 19)		dB
μ-Law Companded PCM					
Idle Channel Noise (weighted, transmit)				19	dBrnc0
Idle Channel Noise (weighted, receive)				15	dBrnc0
A-Law Companded PCM					
Idle Channel Noise (weighted, transmit)				−68	dBm0p
Idle Channel Noise (weighted, receive)				−78	dBm0p

Notes:
1. Applied signal is a 0-dBm0 sine wave within 300 to 3400 Hz. The signal measured is any frequency in the range 300 to 3400 Hz.
2. Two different frequencies, f_2 and f_1, in the range 300–3400 Hz and of equal levels in the range −4 to −21 dBm0 are applied. $2f_1–f_2$ products are measured relative to the level of either f_1 or f_2.
3. Any intermodulation product due to a signal in the range 300–3400 Hz with input level −9 dBm0 and a 50-Hz signal with input level −23 dBm0.



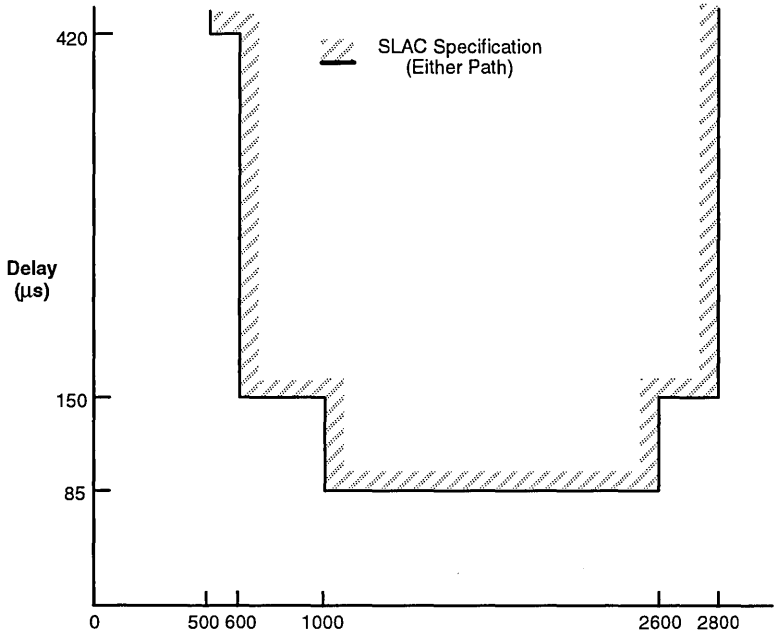
Note: Measured per CCITT Rec. G.714 Paragraph 7.

Figure 12. Attenuation Distortion Transmit or Receive Path 07004B-014



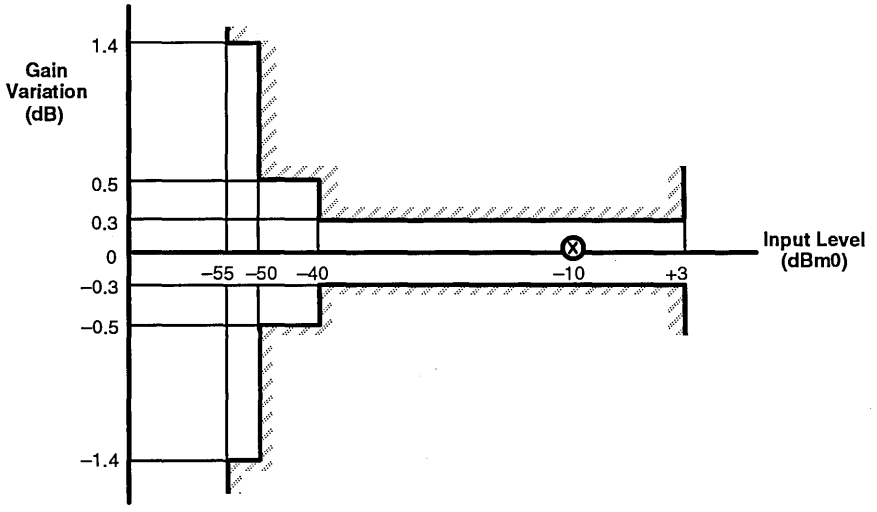
Notes: 1. The frequency is 1020 Hz.
2. Input signal level is 0 dBm0.

Figure 13. Out-of-Band Signals (End-to-End) 07004B-015



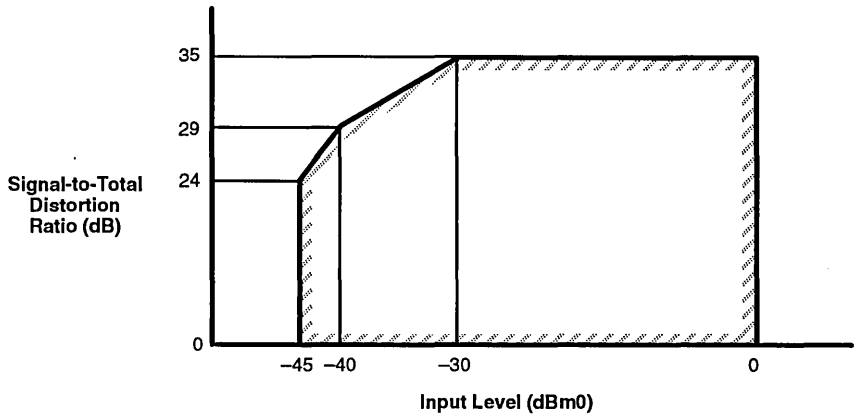
Note: Minimum value of group delay is taken as reference.

Figure 14. Group Delay Distortion (Either Path) 07004-016



Note: Measured per CCITT Rec. G.714 Paragraph 15.

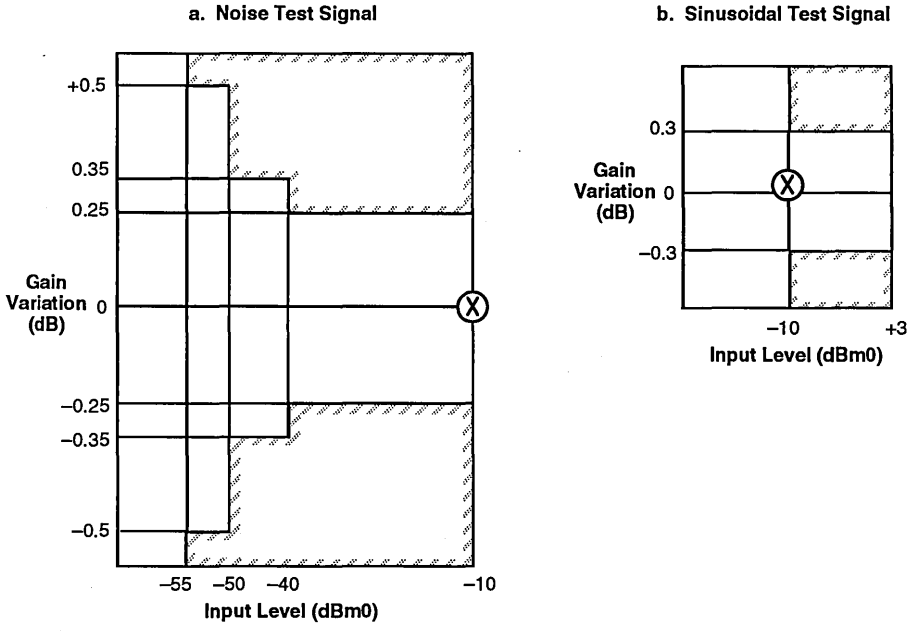
Figure 15. Gain Tracking with Tone (Method 2) Transmit or Receive Path 07004B-017



Note: Measured per CCITT Rec. G.714 Paragraph 14.

07004B-019

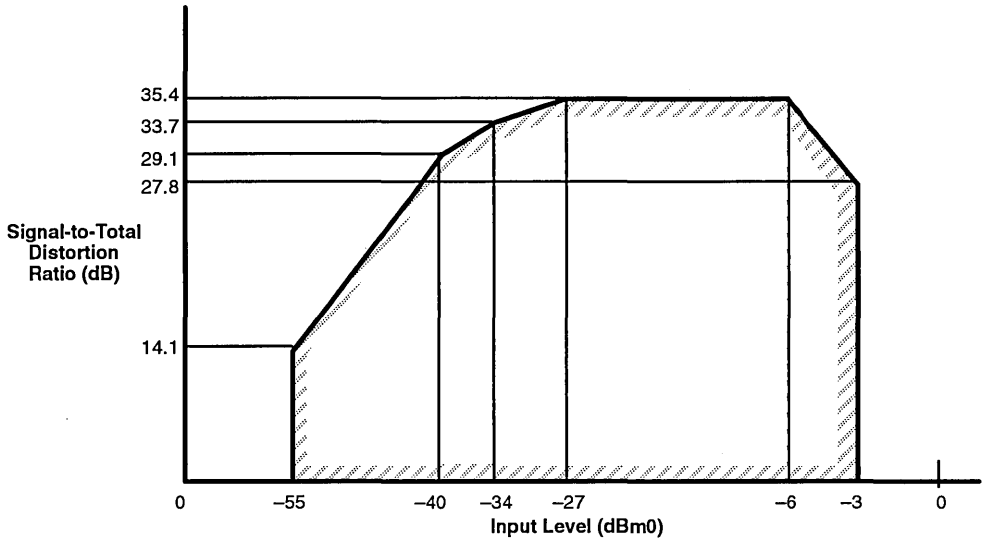
Figure 16. Signal-to-Total Distortion With Tone (Method 2) Transmit or Receive Path



Note: Measured per CCITT Rec. G.714 Paragraph 15.

07004B-018

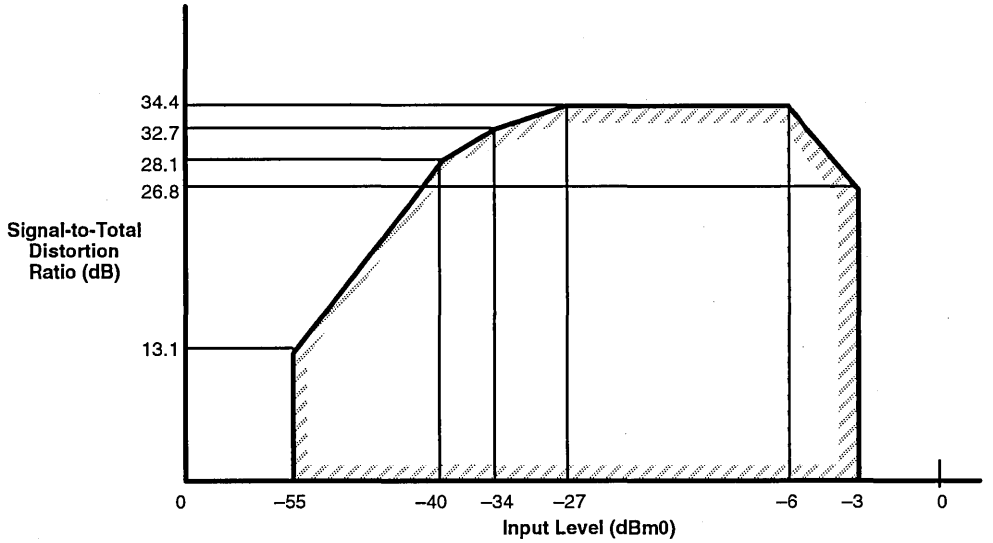
Figure 17. Gain Tracking with Noise (Method 1) Transmit or Receive Path



Note: Measured per CCITT Rec. G.714 Paragraph 14.

Figure 18. Signal-to-Total Distortion With Noise (Receive Path—Method 1)

07004B-020



Note: Measured per CCITT Rec. G.714 Paragraph 14.

Figure 19. Signal-to-Total Distortion With Noise (Transmit Path—Method 1)

07004B-021

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

$T_A = 0$ to 70°C, $V_{CC} = +5$ V ±5%, $V_{BB} = -5$ V ±5% (see Notes 1, 5 & 6)

No.	Parameter	Description	Min	Typ	Max	Units
Serial Interface Input Mode						
1	t_{DCH}	Data Clock High Pulse Width (Note 2)	0.220		20	µs
2	t_{DCL}	Data Clock Low Pulse Width (Note 2)	0.220			µs
3	t_{DCR}	Rise Time of Clock	5		50	ns
4	t_{DCF}	Fall Time of Clock	5		50	ns
5	t_{ICSS}	Chip Select Setup Time	175			ns
6	t_{ICSH}	Chip Select Hold Time	50			ns
7	t_{ICSL}	Chip Select Pulse Width (Notes 3 & 7)		8 t_{DCY}		ns
8	t_{ICSO}	Chip Select Off Time after byte written to or before byte read from B, Z, X, R, GX, or GR in Active mode. MCLK = 2.048 MHz MCLK = 4.096 MHz Otherwise: MCLK = 2.048 MHz MCLK = 4.096 MHz	 32 t_{MCY} 64 t_{MCY} 7 t_{MCY} 14 t_{MCY}			
9	t_{IDS}	Input Data Setup Time	50			ns
10	t_{IDH}	Input Data Hold Time	30			ns
11	t_{OLH}	Output Latch Propagation Delay	0.75		2.1	µs
Serial Interface Output Mode						
12	t_{OCSS}	Chip Select Setup Time	150			ns
13	t_{OCSH}	Chip Select Hold Time	50			ns
14	t_{OCSL}	Chip Select Pulse Width (Notes 3 & 7)		8 t_{DCY}		ns
15	t_{OCSO}	Chip Select Off Time After Byte written to or before byte read from B, Z, X, R, GX, or GR in Active mode. MCLK = 2.048 MHz MCLK = 4.096 MHz Otherwise: MCLK = 2.048 MHz MCLK = 4.096 MHz	 32 t_{MCY} 64 t_{MCY} 7 t_{MCY} 14 t_{MCY}			
16	t_{ODD}	Output Data Turn on Delay			100	ns
17	t_{ODH}	Output Data Hold Time	30			ns
18	t_{ODOF}	Output Turn off Delay			100	ns
19	t_{ODC}	Output Data Valid	30		150	ns
PCM Interface						
25	t_{FSS}	Frame Sync Setup Time	50		(t_{MCY} − 30)	ns
26	t_{FSH}	Frame Sync Hold Time (Companded Mode)	30		(8 t_{MCY} − 50)	ns
27	t_{TSD}	Delay to $\overline{TSC}$ Valid (Note 4)	(N t_{MCY} + 30)		(N t_{MCY} + 150)	ns
28	t_{TSO}	Delay to $\overline{TSC}$ Off (High Impedance)	30			ns
29	t_{DXD}	PCM Data Output Delay	95		185	ns
30	t_{DXH}	PCM Data Output Hold Time	30		100	ns
31	t_{DXZ}	PCM Data Output Delay to High Z	45		90	ns
32	t_{DRS}	PCM Data Input Setup Time	50			ns
33	t_{DRH}	PCM Data Input Hold Time	30			ns

SWITCHING CHARACTERISTICS (continued)

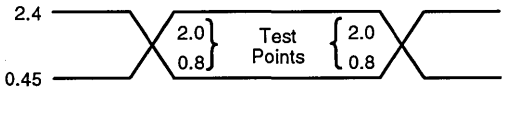
Master Clock (2.048 MHz)						
34	t_{MCY}	Master Clock Period	488.23	488.28	488.33	ns
35	t_{MCH}	Master Clock High Pulse Width	220			ns
36	t_{MCL}	Master Clock Low Pulse Width	238			ns
37	t_{MCR}	Rise Time of Clock	5		15	ns
38	t_{MCF}	Fall Time of Clock	5		15	ns
Master Clock (4.096 MHz)						
39	t_{MCY}	Master Clock Period	244.11	244.14	244.17	ns
40	t_{MCH}	Master Clock High Pulse Width	110			ns
41	t_{MCL}	Master Clock Low Pulse Width	115			ns
42	t_{MCR}	Rise Time of Clock	5		15	ns
43	t_{MCF}	Fall Time of Clock	5		15	ns

Notes: 1. Min and Max values are valid on all digital outputs except C_5–C_1 with a 150-pF load. C_5–C_1 outputs are valid with a 30-pF load.

2. The Data Clock may be stopped in the Low state indefinitely without loss of information. Data will not be clocked in or out while the clock is in the Low state.
3. Chip Select Pulse Width is nominally 8 Data Clock Cycles with a minimum value of 7 Data Clock Cycles + t_{ICSH} + t_{ICSS} and a maximum value of 9 Data Clock Cycles − t_{ICSH} − t_{ICSS}.
4. $\overline{TSC}$ is delayed from FS by a typical value of N t_{MCY}, where N is the value stored in the Time/Clock Slot register.
5. The Frame Sync pulses repeat an 8-kHz rate.
6. FS and MCLK must be synchronized and exactly 256 cycles of MCLK must be guaranteed between Frame Syncs.
7. t_{DCY} is 1 Data Clock Cycle.

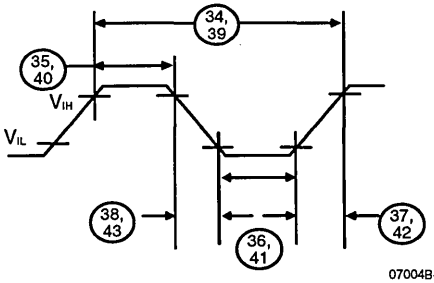
SWITCHING WAVEFORMS

Input and Output Waveforms For AC Tests



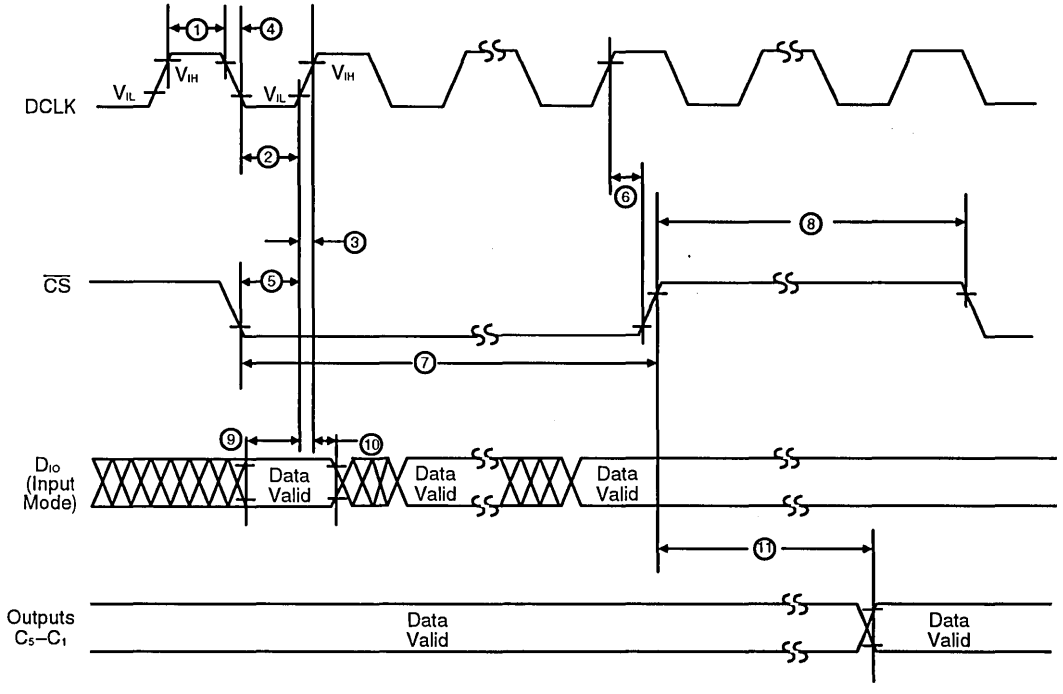
07004B-022

Master Clock Timing



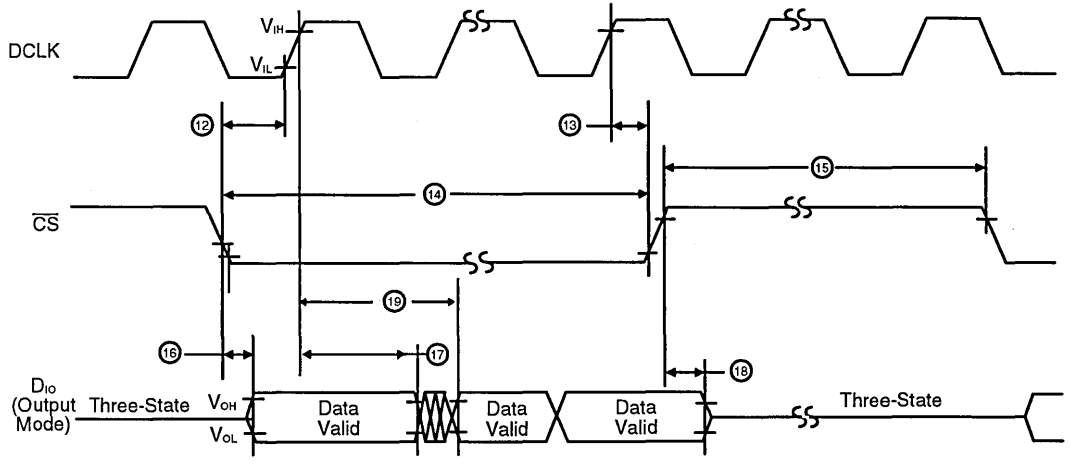
07004B-023

Serial Interface (Input Mode)



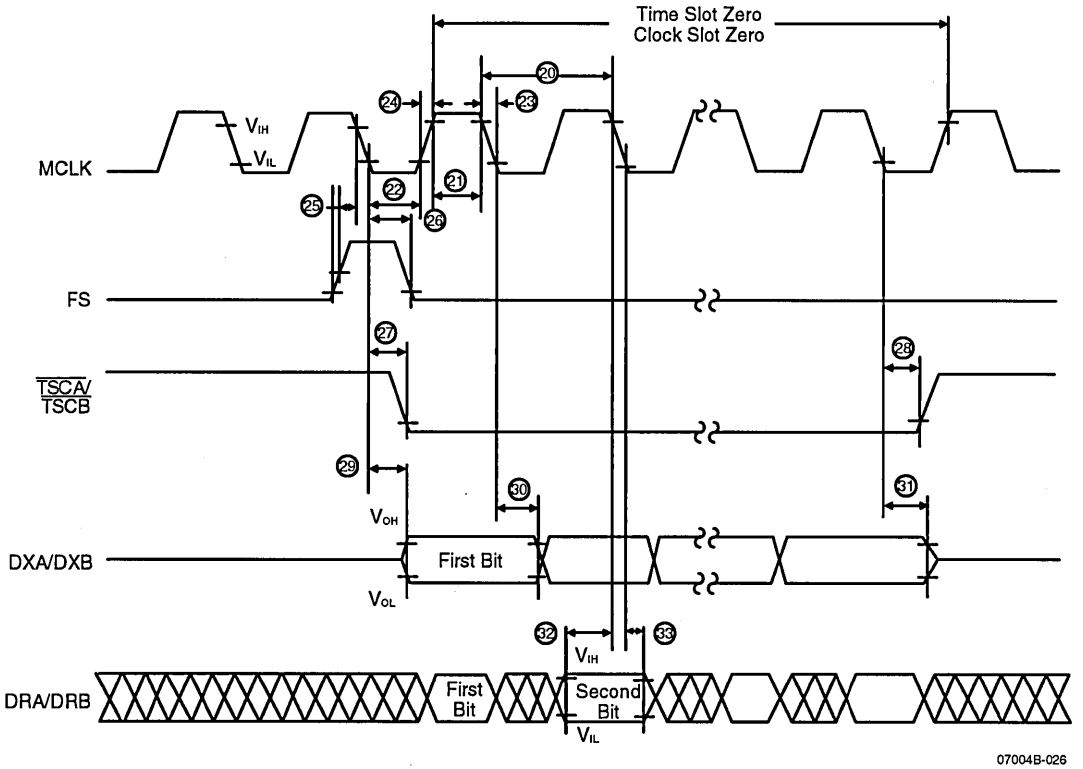
07004B-024

Serial Interface (Output Mode)

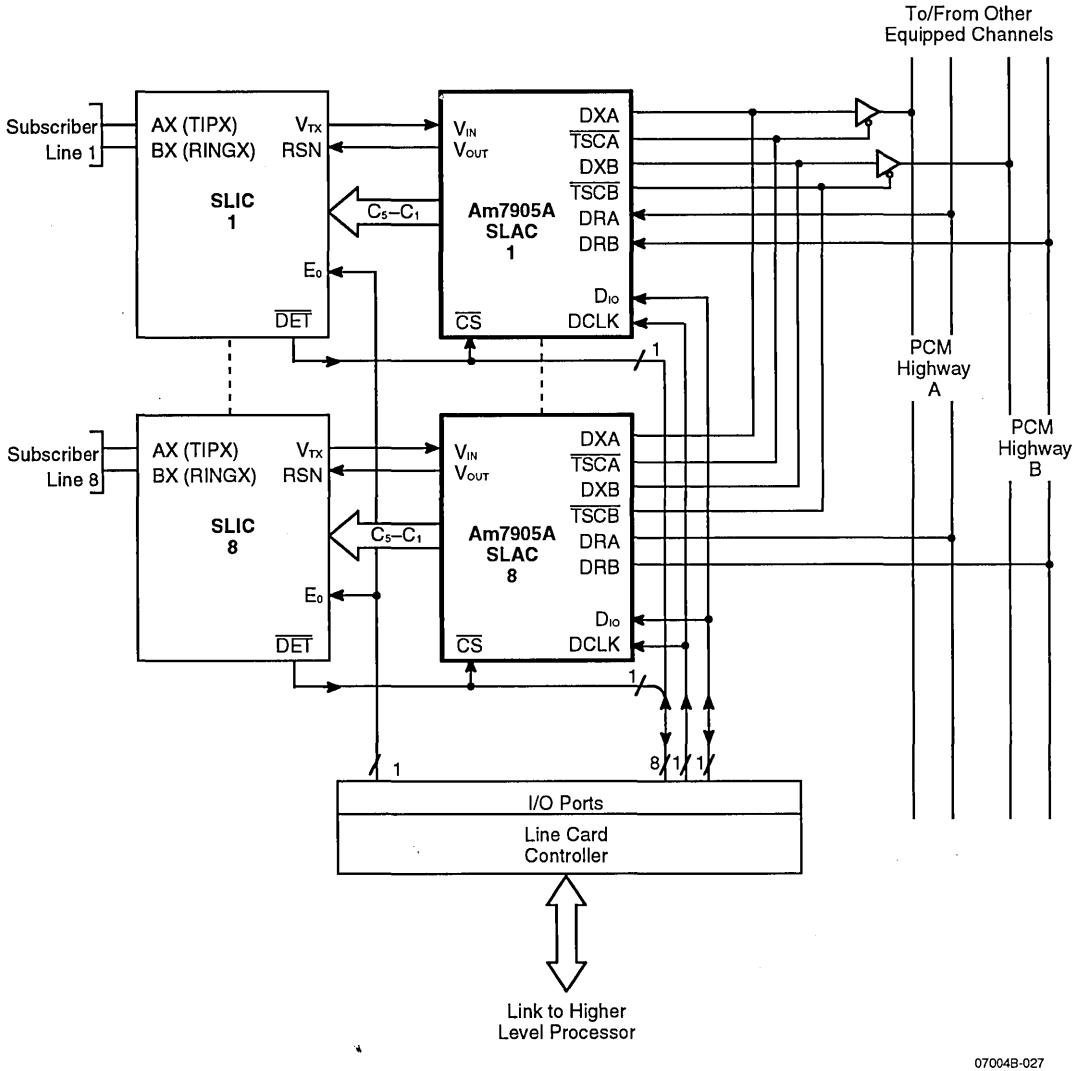


07004B-025

PCM Highway Timing



8-Channel Subscriber Line Card



PRELIMINARY

Am79C02/3(A)

Dual Subscriber Line Audio-Processing Circuit (DSLAC™ Device)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

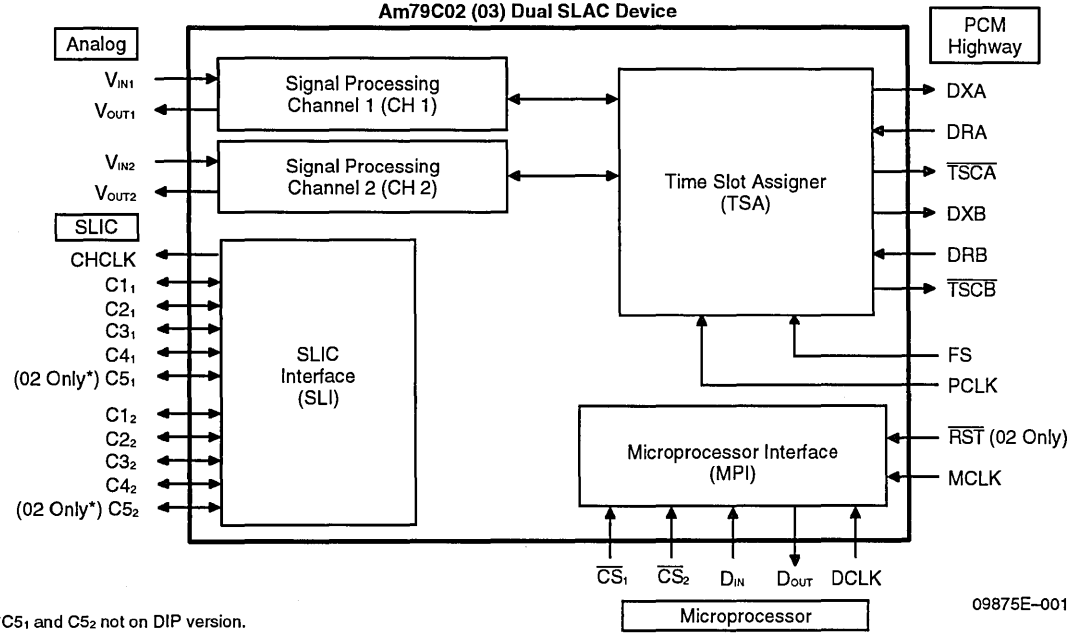
- **Software programmable:**
  - –SLIC impedance
  - –Trans-hybrid balance
  - –Transmit and Receive gains
  - –Equalization
  - –Digital I/O pins
  - –Time Slot Assigner
  - –PCM transmit clock edge options
- **Adaptive trans-hybrid balance filter (Am79C02/3A only)**
- **A-law or μ-law coding**
- **Dual PCM ports**
  - –Up to 8.192 MHz (128 channels per port) through the PCM Interface
- **2.048- or 4.096-MHz master clock**
- **Direct transformer drive**
- **Built-in test modes**
- **Low-power CMOS**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12-dB gain range**

GENERAL DESCRIPTION

The Am79C02/3(A) Dual Subscriber Line Audio-Processing Circuit (DSLAC device) integrates the key functions of an analog linecard into one programmable, high-performance dual Codec-filter device. The DSLAC device is based on the proven design of the reliable Am7901A Subscriber Line Audio-Processing Circuit (SLAC™ device). The advanced architecture of the DSLAC device implements two independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the four-wire-to-PCM section of a linecard.

Advanced CMOS technology makes the Am79C02/3(A) DSLAC device an economical device that has both the functionality and the low-power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC device provides a complete, software-configurable solution to the BORSCHT function.

BLOCK DIAGRAM



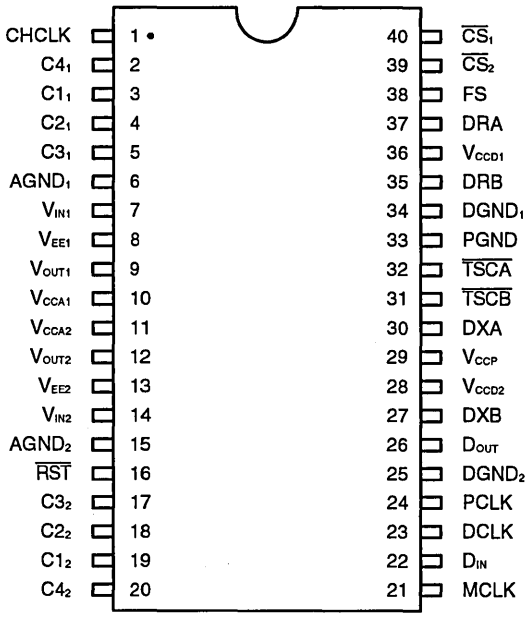
09875E–001

*$C5_1$ and $C5_2$ not on DIP version.

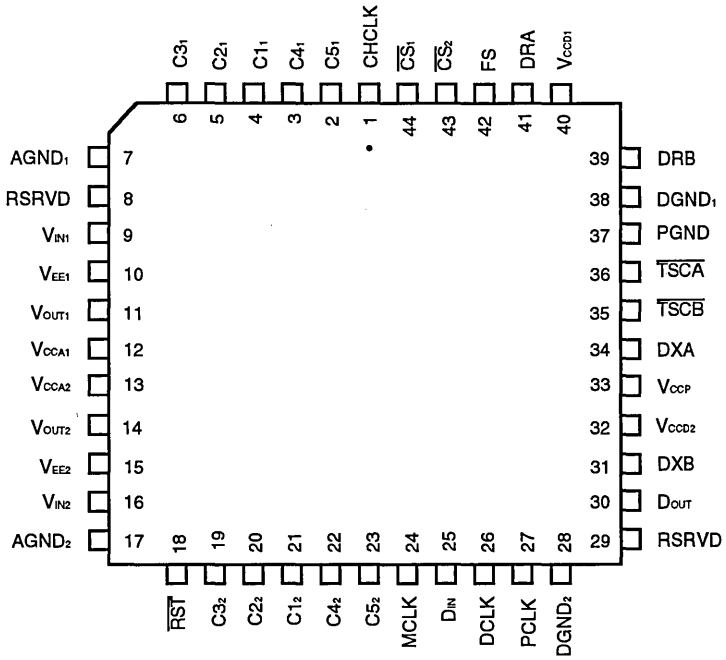
Publication #: 09875 Rev. F Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View (Am79C02 only)

40-Pin DIP



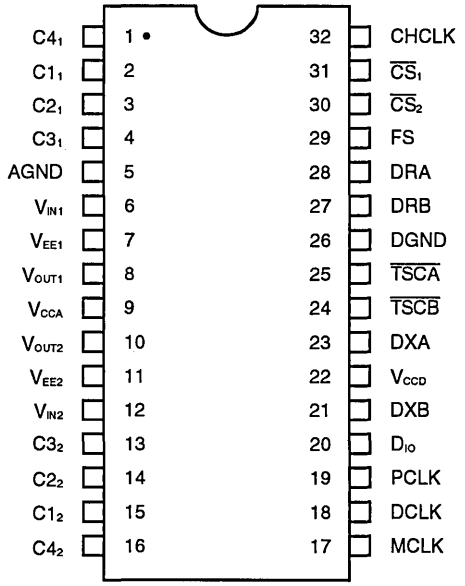
44-Pin PLCC



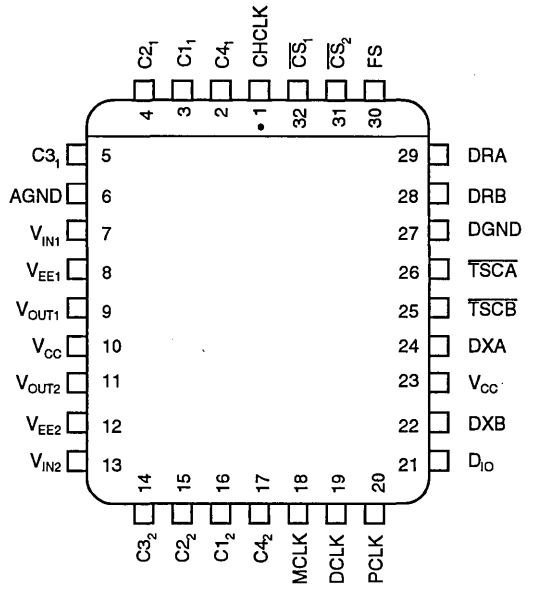
Note: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

CONNECTION DIAGRAMS
Top View (Am79C03 only)

32-Pin DIP



32-Pin PLCC

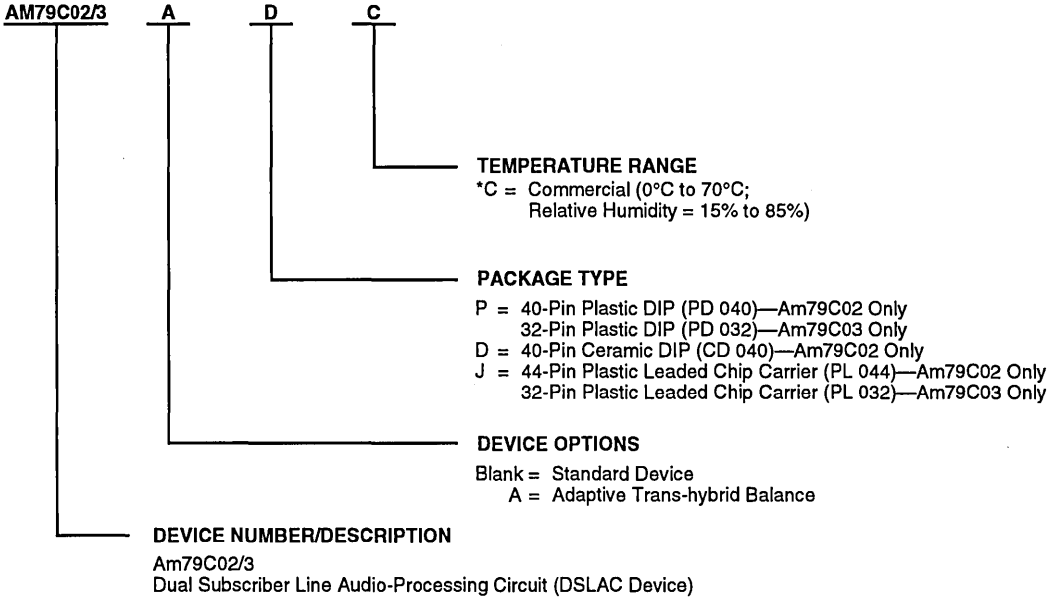


Note: Pin 1 is marked for orientation purposes.

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C02	ADC, AJC, APC
	DC, JC, PC
AM79C03	APC, PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the DSLAC Extended Temperature Supplement (page 2-153) for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

$C1_1$–$C5_1$, $C1_2$–$C5_2$
SLIC Inputs/Outputs (Inputs/Outputs)

The five SLIC control lines per channel are TTL compatible and bi-directional. They can be used to monitor or control the operation of a SLIC or any other device associated with the subscriber line. Lines $C1_1$–$C5_1$ are associated with Channel 1, and lines $C1_2$–$C5_2$ are associated with Channel 2. The $C5_1$ and $C5_2$ lines are only available on the 44-pin PLCC version of the Am79C02(A).

CHCLK
SLIC Clock (Output)

This output provides a 256-kHz, 50%-duty cycle, TTL-compatible clock for use by two SLICs. The CHCLK frequency is synchronous to MCLK but the phase relationship to MCLK is random. CHCLK is capable of driving two TTL inputs.

$\overline{CS_1}$, $\overline{CS_2}$
Chip Selects (Inputs, Active Low)

The Chip Select inputs enable the device to read or write control data. $\overline{CS_1}$ is for the Channel 1 microprocessor interface. $\overline{CS_2}$ is for the Channel 2 microprocessor interface.

DCLK
Data Clock (Input)

The Data Clock input shifts data either into or out of the Microprocessor Interface of the DSLAC device. The maximum clock rate is 4.096 MHz.

D_{IN}
Data Input (Input)

Control data is serially written into the DSLAC device via the D_{IN} pin with the most significant bit first. The Data Clock determines the data rate. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor. (Not available on the Am79C03.)

D_{OUT}
Data Output (Output)

Control data is serially read out of the DSLAC device via the D_{OUT} pin with the most significant bit first. The Data Clock determines the data rate. D_{OUT} is high impedance except when data is being transmitted from the DSLAC device under control of $\overline{CS_1}$ or $\overline{CS_2}$. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor. (Not available on the Am79C03.)

D_{IO}
Data Input/Output

Control data is serially written into and read out of the Am79C03(A) DSLAC device via the D_{IO} pin with the most significant bit first. The Data Clock determines the data rate. D_{IO} is high impedance except when data is being transmitted from the DSLAC device under control of $\overline{CS_1}$ or $\overline{CS_2}$. D_{IO} replaces D_{IN} and D_{OUT} found on the Am79C02(A).

DRA, DRB
PCM Inputs (Inputs)

The Receive PCM data for Channels 1 and 2 is serially received on either the DRA or the DRB port with port selection under user program control. Eight bits are received with the most significant bit first. Data for each channel is received in 8-bit bursts every 125 µs at the PCLK rate.

DXA, DXB
PCM Outputs (Outputs)

The Transmit PCM data from Channels 1 and 2 is sent serially through either the DXA or DXB port with port selection under user program control. Eight bits are transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the Inactive mode.

FS
Frame Sync (Input)

The Frame Sync pulse is an 8-kHz signal that identifies the beginning of a frame. The DSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.

MCLK
Master Clock (Input)

The Master Clock must be a 2.048-MHz or 4.096-MHz clock input for use by the digital signal processor. MCLK may be asynchronous to PCLK.

PCLK
PCM Clock (Input)

The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz. The PCLK clock may be asynchronous to MCLK.

$\overline{RST}$
Reset (Input, Active Low)

A TTL Low signal on this input resets the DSLAC device to its default state. (Not available on the Am79C03.)

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control (Outputs, Open Drain, Active Low)

The Time Slot Control outputs are open drain (requiring pull-up resistors) and are normally inactive (high impedance). $\overline{TSCA}$ is active (Low) when PCM data is present on the DXA output and $\overline{TSCB}$ is active (Low) when PCM data is present on the DXB output.

V_{IN1}, V_{IN2}

Analog Inputs (Inputs)

The analog input is applied to the transmit path of the DSLAC device. The signal is sampled, digitally processed and encoded for the PCM output. V_{IN1} is the input for Channel 1 and V_{IN2} is the input for Channel 2.

V_{OUT1}, V_{OUT2}

Analog Outputs (Outputs)

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is the output from Channel 1 and V_{OUT2} is the output for Channel 2. These outputs can directly drive a transformer SLIC.

For Am79C02:

$AGND_1$	Analog Ground (Channel 1)
$AGND_2$	Analog Ground (Channel 2)
$DGND_1$	Digital Ground 1
$DGND_2$	Digital Ground 2
PGND	PCM I/O Ground
V_{CCA1}	+5-V Analog Power Supply (Channel 1)
V_{CCA2}	+5-V Analog Power Supply (Channel 2)
V_{CCD1}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{CCD2}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{CCP}	+5-V PCM I/O Power Supply. Internally connected to substrate on the IC.
V_{EE1}	–5-V Power Supply (Channel 1)
V_{EE2}	–5-V Power Supply (Channel 2)

For Am79C03:

AGND	Analog Ground
DGND	Digital Ground
V_{CCA}	+5-V Analog Power Supply
V_{CCD}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{EE1}	–5-V Power Supply (Channel 1)
V_{EE2}	–5-V Power Supply (Channel 2)

The many separate power supply inputs are intended to provide for good power supply decoupling techniques. Note that all of the +5-V inputs should be connected to the same source, all of the ground inputs should be connected to the same source, and both of the –5-V inputs should be connected to the same source.

FUNCTIONAL DESCRIPTION

The DSLAC device performs the Codec/filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

Independent channels allow the DSLAC device to function as two SLAC devices. All of the digital filtering is performed in digital signal processors operating from either a 2.048-MHz or 4.096-MHz external clock. The A/D, D/A, and signal processing is separate for each channel and each channel has its own chip select ($\overline{CS_1}$ and $\overline{CS_2}$) to allow separate programming.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the AmSLAC2™ software. The PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read or written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The output hold time and the transmit clock edge can be selected for compatibility with other devices which can be connected to the PCM highway.

Two pin configurations of the DSLAC device are offered with the PCM interface described above. The Am79C02(A), the original version of the DSLAC device, is available in both 40-pin DIP and 44-pin PLCC packages. The PLCC version has one extra SLIC I/O line per channel. The Am79C03(A) is a reduced pin-count version obtained by consolidating a number of ground and power supply buses on-chip, and eliminating the hardware reset function. The Am79C03(A) is available in both 32-pin plastic DIP and 32-pin PLCC packages. The "A" version of both devices (e.g., Am79C02A) offers an adaptive trans-hybrid balance feature described in the Adaptive B-Filter Overview.

The following documentation describes the operation of a single channel of the DSLAC device. The description is valid for either Channel 1 or 2. V_{IN} in this data sheet refers to either V_{IN1} or V_{IN2}, V_{OUT} refers to either V_{OUT1} or V_{OUT2}, and $\overline{CS}$ refers to either $\overline{CS_1}$ or $\overline{CS_2}$.

Operational Modes

Active Mode

Each channel of the DSLAC device can operate in either the active (operational) or inactive (standby) mode. In the active mode, the DSLAC device is able to transmit and receive PCM and analog information. This is the normal operating mode when a telephone call is in progress. The Activate command, Microprocessor Interface (MPI) Command #5, puts the device into this state. Bringing the DSLAC device into the active mode is only possible through the MPI.

Inactive Mode

The Am79C02(A) DSLAC device is forced into the inactive (standby) mode at power-up, by a hardware or software reset, or is programmed into this mode by the inactivate command (Command #1). The Am79C03 DSLAC device is forced into the standby mode at power-up or by a software reset. No transmission or reception of PCM data takes place, but the circuits which contain programmed information retain their data. Power is switched off from all non-essential circuitry, though the MPI remains active to receive new commands. The analog output is tied to ground through an approximately 3-Kohm resistor.

Reset State

An active Low, hardware Reset pin ($\overline{RST}$) is available on the Am79C02 which resets the device to the following default state. (For the Am79C03, when power is first applied, an internal power-on reset puts the device into the following default state.)

1. A-law is selected.
2. B, X, R, and Z filters are disabled and AISN gain is zero.
3. Digital (GX and GR) gain blocks are disabled, resulting in unity gain, and analog (AX and AR) gains are set to unity.
4. SLIC input/output direction is set to the input mode.
5. Normal conditions are selected (see Command #4).
6. The B-filter adaptive mode is turned off.
7. Both channels are placed in the Inactive (standby) mode.
8. Transmit time, receive time, and clock slots are set to zero.
9. DXA/DRA ports are selected for Channel 1.
10. DXB/DRB ports are selected for Channel 2.
11. MCLK is selected to be 4.096 MHz.
12. The transmit outputs are selected to change on the negative edge of PCLK.
13. PCM Delay is inserted.

Reset states 1 to 7 are identical to those of the software reset (Command #2), but the hardware (or power-on) reset applies to both channels simultaneously. When power is initially applied to the DSLAC device or when $\overline{RST}$ is asserted (Am79C02 only), the following sequence of actions is necessary to ensure correct operation of the DSLAC device.

1. Select MCLK frequency (Command #6).
2. Software reset (Command #2).
3. Program filter coefficients and all other required parameters.

Upon initial application of power, a minimum of 1 ms is needed before $\overline{CS_1}$ or $\overline{CS_2}$ may go Low and an MPI command initiated. If the power supply (V_{CCD1} or V_{CCD2}) falls below approximately 2.0 V, the device is software-reset and will require complete reprogramming with the above sequence. Bit 7 of the SLIC Direction Register will read back as a logical 1 to indicate a power interruption has been detected. This bit is cleared when a software reset command is sent to the DSLAC device. The $\overline{RST}$ pin may be tied to +5 V if it is not needed in the system (Am79C02 only).

Signal Processing

Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the DSLAC device for the system. Figure 1 shows DSLAC device signal processing and indicates the programmable blocks.

The advantages of digital filters are:

–high reliability;
–no drift with time or temperature;
–unit-to-unit repeatability; and,
–superior transmission performance.

Two-Wire Impedance Matching

Two feedback paths on the DSLAC device modify the effective two-wire input impedance of the SLIC by providing programmable feedback from V_{IN} to V_{OUT}. The Analog Impedance Scaling Network (AISN) provides a programmable analog gain of –0.9375 to +0.9375 from V_{IN} to V_{OUT}. The Z filter is a programmable digital filter, also connecting V_{IN} to V_{OUT}.

Distortion Correction and Equalization

The DSLAC device contains programmable filters in the receive (R) and transmit (X) directions. These may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter.

Trans-Hybrid Balancing

The DSLAC device's programmable B filter is used to adjust trans-hybrid balance. The filter has a single-pole IIR section (B-IIR) and an eight-tap FIR section (B-FIR), both operating at 16 kHz. The DSLAC device has an optional adaptive mode for the B filter which may be used to achieve optimum performance. The Echo Path Gain (EPG) and Error Level Threshold (ELT) registers contain values which determine the adaptive mode performance.

Gain Adjustment

The DSLAC device transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB, located immediately before the A/D converter. Gain block GX is a digital gain that is programmable to any gain from 0 dB to +12 dB with a worst case step size of 0.1 dB for gain settings below +10 dB, and a worst case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB.

The DSLAC device receive path has two programmable loss blocks. Loss block GR is a digital loss that is programmable from 0 dB to 12 dB with a worst case step size of 0.1 dB. Loss block AR is an analog loss of 0 dB or 6.02 dB, located immediately after the D/A converter. This provides a net loss in the range of 0 dB to 18 dB.

Transmit Signal Processing

In the transmit path, the analog input signal is A/D converted, filtered, companded (A- or μ-law), and made available for output to the PCM highway. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The B, X, and GX blocks are user-programmable digital filter sections with

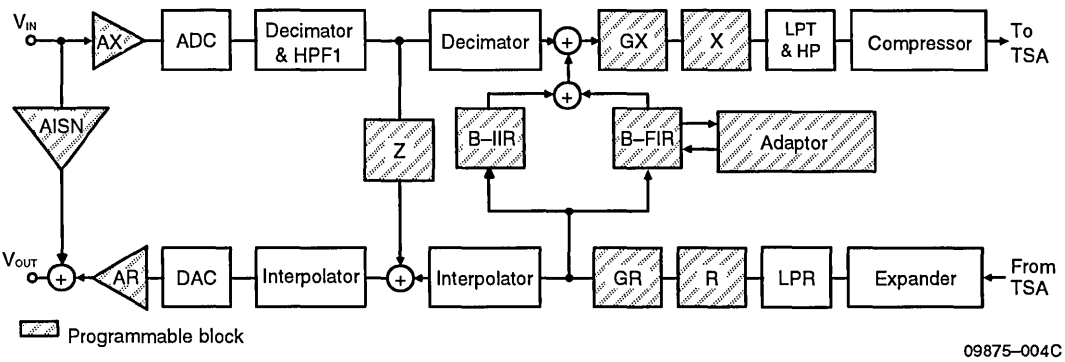


Figure 1. DSLAC Device Signal Processing

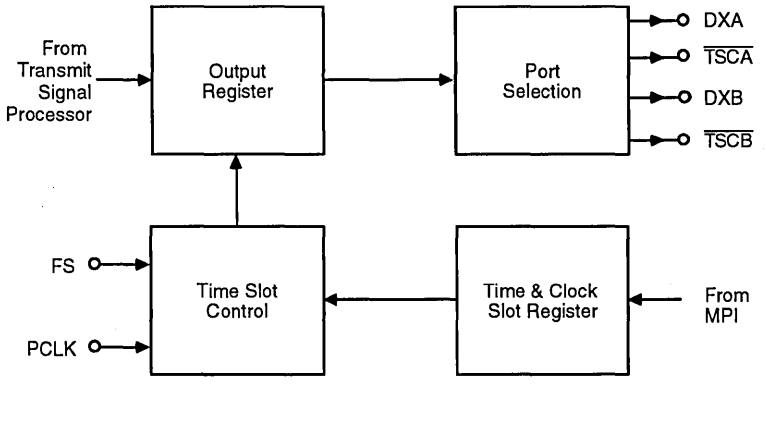


Figure 2. Transmit PCM Interface

coefficients stored in the coefficient RAM. AX is an analog amplifier which can be programmed for 0-dB or 6.02-dB gain. The filters may be made transparent when not required in a system.

The decimator reduces the high input sampling rate to 16 kHz for input to the B, GX, and X filters. The X filter is a 6-tap FIR section which is part of the frequency response correction network. The B filter operates on samples from the receive signal path in order to provide trans-hybrid balancing in the loop. The high-pass filter rejects low frequencies such as 50 or 60 Hz and may be disabled.

Transmit PCM Interface

The transmit PCM interface receives an 8-bit compressed code from the digital A-/μ-law compressor. The transmit PCM interface logic (Figure 2) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block.

The frame sync (FS) pulse identifies the beginning of a transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers.

The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skew in the system. The data is transmitted in bytes with the most significant bit first.

The PCM data may be user-programmed for output onto either the DXA or DXB port. Correspondingly, either $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is Low during transmission.

The DXA/DXB and $\overline{\text{TSCA}}$/$\overline{\text{TSCB}}$ outputs can be programmed to change either on the negative or positive edge of PCLK. In the first case, an extra delay (PCM

delay) in the timing of the DXA and DXB signals may be programmed to allow timing compatibility with other devices on the PCM highway.

Receive Signal Processing

In the receive path, the digital signal is expanded, filtered, converted to analog, and passed to the V_{OUT} pin. The signal processor contains an ALU, RAM, ROM, and Control logic to implement the filter sections. The Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM while AR is an analog amplifier which can be programmed for a 0-dB or 6.02-dB loss. The filters may be made transparent when not required in a system.

The low-pass filter band limits the signal. The R filter is a 6-tap FIR section operating at a 16-kHz sampling rate and is part of the frequency response correction network. The analog impedance scaling network (AISN) is a user-programmable gain block providing feedback from V_{IN} to V_{OUT} to emulate different Z_{SLIC} impedances from a single external Z_{SLIC} impedance. The Z filter provides feedback from the transmit signal path to the receive path and is used to modify the effective input impedance to the system. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface

The receive PCM interface logic (Figure 3) controls the reception of data bytes from the PCM highway, transfers the data to the A-/μ-law expansion logic, and then passes the data to the receive path of the signal processor. The frame sync (FS) pulse identifies the beginning of a receive frame, and all channels (time slots) are referenced to it.

The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skews in the system. The PCM data may be user-programmed for input from either the DRA or DRB port.

Analog Impedance Scaling Network (AISN)

The AISN is incorporated in the DSLAC device to scale the value of the external Z_{SLIC} impedance. Scaling this external impedance with the AISN (along with the Z filter) allows matching of many different line conditions using a single impedance value. Linecards may be designed for many different specifications without any hardware changes.

The AISN is a programmable gain that is connected across the DSLAC device input from V_{IN} to V_{OUT}. The gain can be varied from –0.9375 to +0.9375 in 31 steps of 0.0625. The AISN gain is given by the following equation:

$$h_{AISN} = 0.0625\,[(A \cdot 2^4 + B \cdot 2^3 + C \cdot 2^2 + D \cdot 2^1 + E \cdot 2^0) - 16]$$

where A, B, C, D, and E = 1 or 0.

The AISN gain is used to alter the input impedance of the DSLAC device and SLIC as shown in Figure 4.

The input impedance into the DSLAC device from the SLIC is given by:

$$Z_{IN} = \frac{1 - G_{44}\, h_{AISN}}{1 - G_{440}\, h_{AISN}}\, Z_{SL},$$

where G_{440} (defined as $G_{24}\, G_{42} + G_{44}$) is the echo gain into an open circuit and G_{44} is the echo gain into a short circuit.

There are two special cases to the formula for h_{AISN}: 1) value of ABCDE = 00000 will specify a gain of 0 (or cutoff), and 2) a value of ABCDE = 10000 is a special case where the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN} with a gain of 0 dB. This allows a digital-to-digital loopback mode wherein a digital PCM input signal is completely processed through the receive section all the way to the V_{OUT} pin. The signal is then connected internally to V_{IN} where it is processed through the transmit section and output as digital PCM data.

Speech Coding

The A/D and D/A conversion follows either the A-law or the μ-law as they are defined in CCITT Rec. G.711. A-law or μ-law operation is programmed using MPI Command #19. Alternate bit inversion is performed as part of the A-law coding.

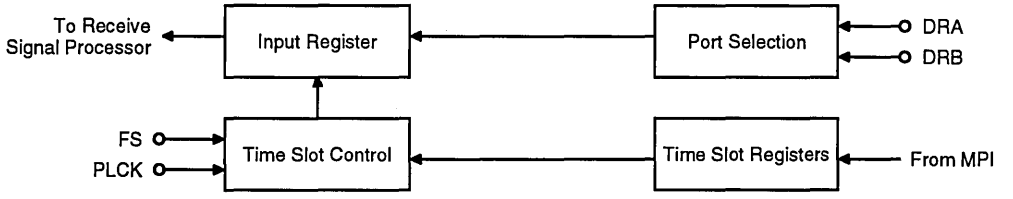


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Figure 3. Receive PCM Interface

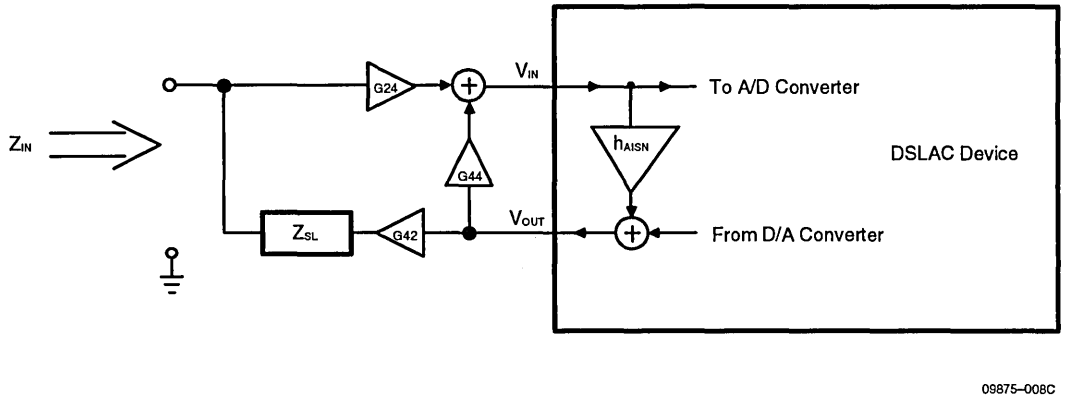


Figure 4. Input Impedance Modification Due to AISN

Command Description and Formats

Microprocessor Interface Description

A microprocessor may be used to program the DSLAC device and control its operation using the Microprocessor Interface (MPI). Data programmed previously may be read out for verification. For each channel, commands are provided to assign values to the following parameters.

–Transmit time slot
–Receive time slot
–Transmit clock slot
–Receive clock slot
–Transmit gain
–Receive loss
–B-filter coefficients
–X-filter coefficients
–R-filter coefficients
–Z-filter coefficients
–Adaptive B filter parameters
–AISN coefficient
–Read/Write SLIC Input/Output
–Select A-law or μ-law code
–Select Transmit PCM Port A or B
–Select Transmit PCM clock edge
–Select Transmit PCM delay
–Select Receive PCM Port A or B
–Enable/disable B filter
–Enable/disable Z filter
–Enable/disable X filter
–Enable/disable R filter
–Enable/disable GX filter
–Enable/disable GR filter
–Enable/disable AX amplifier
–Enable/disable AR amplifier
–Enable/disable adaptive B filter
–Select test modes
–Select active or inactive (standby) mode

The following description of the MPI is valid for either Channel 1 or 2. Whenever $\overline{CS}$ is specified, it refers to either $\overline{CS}_1$ or $\overline{CS}_2$. If desired, both channels may be programmed simultaneously with identical information by activating $\overline{CS}_1$ and $\overline{CS}_2$ at the same time.

The MPI consists of serial data input (D_{IN} or D_{IO} on Am79C03), output (D_{OUT} or D_{IO} on Am79C03), data clock (DCLK), and a separate chip select ($\overline{CS}_1$ and $\overline{CS}_2$) input for each channel (Figure 5). The serial input consists of 8-bit command words which may be followed with additional bytes of input data or may be followed by the DSLAC device sending out bytes of data. All data input and output is MSB (D_7) first and LSB (D_0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least the minimum off-period before the next byte is read or written.

All commands requiring additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All commands followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The DSLAC device will not accept any input commands until all the data has been shifted out. Unused bits in the data bytes are read out as zeros.

A command sequence to one channel must be finished before a command can be sent to the other channel.

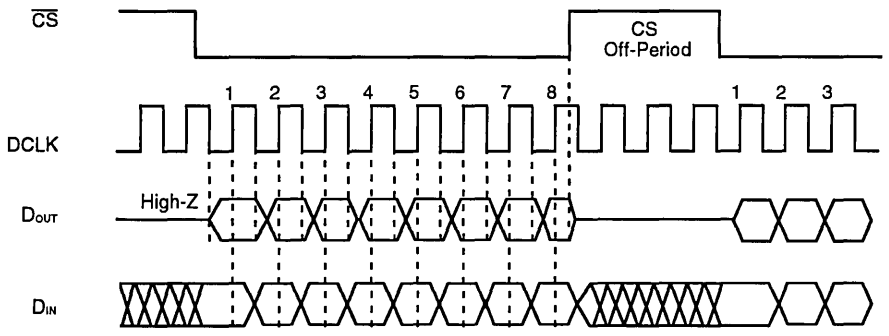


Figure 5. Microprocessor Interface Timing Diagram

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK may be run to a number of DSLAC devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi-byte read or write command sequence, DCLK can also stay in the High state indefinitely; however, each low-going transition of the $\overline{CS}$ line will still advance the byte counter. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ lines remain at a High level.

Summary of MPI Commands**

C#	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
1.	00	0	0	0	0	0	0	0	0	Inactivate (Standby mode)
2.	02	0	0	0	0	0	0	1	0	Reset
3.	06	0	0	0	0	0	1	1	0	No Operation
4.	08	0	0	0	0	1	0	0	0	Reset to Normal Conditions
5.	0E	0	0	0	0	1	1	1	0	Activate
6.	1*	0	0	0	1	0	0	*	0	MCLK Selection
7.	40	0	1	0	0	0	0	0	0	Write TX Time Slot & PCM Highway
8.	41	0	1	0	0	0	0	0	1	Read TX Time Slot & PCM Highway
9.	42	0	1	0	0	0	0	1	0	Write RX Time Slot & PCM Highway
10.	43	0	1	0	0	0	0	1	1	Read RX Time Slot & PCM Highway
11.	44	0	1	0	0	0	1	0	0	Write RX & TX Clock Slot and TX Clock Edge
12.	45	0	1	0	0	0	1	0	1	Read RX & TX Clock Slot and TX Clock Edge
13.	50	0	1	0	1	0	0	0	0	Write AISN, PCM delay, Analog Gains
14.	51	0	1	0	1	0	0	0	1	Read AISN, PCM delay, Analog Gains
15.	52	0	1	0	1	0	0	1	0	Write SLIC Input/Output Register
16.	53	0	1	0	1	0	0	1	1	Read SLIC Input/Output Register
17.	54	0	1	0	1	0	1	0	0	Write SLIC Input/Output Direction
18.	55	0	1	0	1	0	1	0	1	Read SLIC I/O Direction, Power Interruption Bit, and Channel Status Bit
19.	60	0	1	1	0	0	0	0	0	Write Operating Functions
20.	61	0	1	1	0	0	0	0	1	Read Operating Functions
21.	70	0	1	1	1	0	0	0	0	Write Operating Conditions
22.	71	0	1	1	1	0	0	0	1	Read Operating Conditions
23.	73	0	1	1	1	0	0	1	1	Read Revision Code Number
24.	80	1	0	0	0	0	0	0	0	Write GX-Filter Coefficients
25.	81	1	0	0	0	0	0	0	1	Read GX-Filter Coefficients
26.	82	1	0	0	0	0	0	1	0	Write GR-Filter Coefficients
27.	83	1	0	0	0	0	0	1	1	Read GR-Filter Coefficients
28.	84	1	0	0	0	0	1	0	0	Write Z-Filter Coefficients
29.	85	1	0	0	0	0	1	0	1	Read Z-Filter Coefficients
30.	86	1	0	0	0	0	1	1	0	Write B-Filter Coefficients
31.	87	1	0	0	0	0	1	1	1	Read B-Filter Coefficients
32.	88	1	0	0	0	1	0	0	0	Write X-Filter Coefficients
33.	89	1	0	0	0	1	0	0	1	Read X-Filter Coefficients
34.	8A	1	0	0	0	1	0	1	0	Write R-Filter Coefficients
35.	8B	1	0	0	0	1	0	1	1	Read R-Filter Coefficients
36.	8C	1	0	0	0	1	1	0	0	Write Echo Path Gain
37.	8D	1	0	0	0	1	1	0	1	Read Echo Path Gain
38.	8E	1	0	0	0	1	1	1	0	Write Error Level Threshold
39.	8F	1	0	0	0	1	1	1	1	Read Error Level Threshold

*Code changes with function.
**All codes not listed are reserved by AMD and should not be used.

THE COMMAND STRUCTURE

This section describes in detail each of the MPI commands. Each of the commands is shown along with the format of any additional data bytes that follow. For details on the filter coefficients of the form $C_{xy}m_{xy}$, please refer to the Description of Coefficients section.

1. Inactivate (Standby Mode)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

During the inactive mode (of one or both channels):
a) All of the programmed information is retained.
b) The Microprocessor Interface (MPI) remains active.
c) The PCM outputs are in high impedance and the PCM inputs are disabled.
d) The analog output is tied to zero volts through an internal resistor (~3 Kohm).

2. Reset

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	1	0

The reset state of the device is:
a) A-law is selected.
b) B, X, R, and Z filters are disabled and AISN gain is zero.
c) Digital (GX and GR) gain blocks are disabled resulting in unity gain, and analog (AX and AR) gains are set to unity.
d) All SLIC I/O lines are configured as inputs.
e) Normal conditions are selected (see Command #4).
f) The B-filter Adaptive mode is reset.
g) The channel is placed in the inactive (standby) mode.

3. No Operation

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	1	1	0

4. Reset to Normal Conditions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	1	0	0	0

Reset to Normal Conditions performs the following operations:
a) Does not insert 6 dB loss in receive path.
b) Receive & transmit paths are not cutoff.
c) High pass filter is enabled.
d) Test modes are turned off.

5. Activate (Operational Mode)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	1	1	1	0

This command places the device in the active mode. No valid PCM data is transmitted until after the second FS pulse is received following the execution of the Activate command.

6. MCLK Selection

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	0	A	0

MCLK may be selected to operate from a 2.048-MHz or 4.096-MHz external clock. MCLK selection on either channel affects both channels.
A = 0: 2.048 MHz
A = 1: 4.096 MHz

7. Write Transmit Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	0	0
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B

TS: Time slot number 0 to 127

The Transmit section of both channels must not be set to the same time slot on the same output port simultaneously.

8. Read Transmit Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	0	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

9. Write Receive Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	1	0
Input data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B

TS: Time slot number 0 to 127

10. Read Receive Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	1	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

11. Write Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	1	0	0
Input data:	—	XE	RCS	RCS	RCS	TCS	TCS	TCS

TCS: Transmit Clock Slot number 0 to 7
RCS: Receive Clock Slot number 0 to 7

XE = 0 Transmit changes on negative edge of PCLK
XE = 1 Transmit changes on positive edge of PCLK

Note: XE = 1 should not be programmed unless the PCM delay is removed, (i.e., PCD = 1). XE must be written on Channel 1, but affects both channels. If XE = 1, the maximum PCM clock rate becomes 4.096 MHz.

12. Read Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	1	0	1
Output data:	—	XE	RCS	RCS	RCS	TCS	TCS	TCS

13. Write AISN, PCM Delay, and Analog Gains

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	0	0
Input data:	PCD	AX	AR	A	B	C	D	E

PCM Delay: PCD = 0 Delay inserted (SLAC device compatible)
PCD = 1 Delay removed (high speed)

Transmit Analog Gain: AX = 0 0-dB gain
AX = 1 6.02-dB gain

Receive Analog Loss: AR = 0 0-dB loss
AR = 1 6.02-dB loss

AISN coefficient: A, B, C, D, E

The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$$h_{AISN} = 0.0625\,[(A \cdot 2^4 + B \cdot 2^3 + C \cdot 2^2 + D \cdot 2^1 + E \cdot 2^0) - 16]$$

where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = 10000 implements a special digital loopback mode, and a value of ABCDE = 00000 indicates a gain of 0 (cutoff).

14. Read AISN, PCM Delay, and Analog Gains

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	0	1
Output data:	PCD	AX	AR	A	B	C	D	E

15. Write SLIC Output Register

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	1	0
Input data:	—	—	—	C5	C4	C3	C2	C1

C1 through C5 are set to 1 or 0. The data will appear latched on the C1 through C5 SLIC I/O pins, provided they were set in the output mode (see Command #17). The data sent to any of the pins set to the input mode will be latched, but will not appear at the pins.

16. Read SLIC Pins

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	1	1
Output data:	—	—	—	C5	C4	C3	C2	C1

The logic state of pins C1 through C5 is read regardless of the direction programmed into the Input/Output register.

17. Write SLIC Input/Output Direction

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	1	0	0
Input data:	—	—	—	A	B	C	D	E

Pins C1 through C5 are set to input or output modes individually. The input mode is set when the appropriate data bit is a 0, and the output mode is set when the data bit is a 1. All unused SLIC I/O pins should be programmed as outputs to reduce power consumption.

Data bit A sets pins $C5_1$ or $C5_2$.
Data bit B sets pins $C4_1$ or $C4_2$.
Data bit C sets pins $C3_1$ or $C3_2$.
Data bit D sets pins $C2_1$ or $C2_2$.
Data bit E sets pins $C1_1$ or $C1_2$.

18. Read SLIC Input/Output Direction, Channel Status Bit, and Power Interrupt Bit

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	1	0	1
Output data:	PI	CS	—	A	B	C	D	E

PI = 0 There has not been a power interruption since the last software reset command.

PI = 1 A power interruption has been previously detected requiring the DSLAC device to be completely reprogrammed. This bit is cleared by issuing a software reset command.

CS = 0 Channel is inactive (standby mode).

CS = 1 Channel is active.

19. Write Operating Functions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	0	0	0	0	0
Input data:	ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Adaptive B-Filter: ABF = 0 B-filter non-adaptive mode
ABF = 1 B-filter adaptive mode

A-law/μ-law: A/μ = 0 A-law coding
A/μ = 1 μ-law coding

GR Filter: EGR = 0 GR filter disabled
EGR = 1 GR filter enabled

GX Filter: EGX = 0 GX filter disabled
EGX = 1 GX filter enabled

X Filter: EX = 0 X filter disabled
EX = 1 X filter enabled

R Filter: ER = 0 R filter disabled
ER = 1 R filter enabled

Z Filter: EZ = 0 Z filter disabled
EZ = 1 Z filter enabled

B Filter: EB = 0 B filter disabled
EB = 1 B filter enabled

Note: The enable adaptive B-filter command is only effective when used with the enable B-filter command.

20. Read Operating Functions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	0	0	0	0	1
Output data:	ABF	A/U	EGR	EGX	EX	ER	EZ	EB

21. Write Operating Conditions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	0	0
Input data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

Cut off Transmit Path: CTP = 0 Transmit path connected
CTP = 1 Transmit path cut off
Cut off Receive Path: CRP = 0 Receive path connected
CRP = 1 Receive path cut off
High-Pass Filter: HPF = 0 High-pass filter enabled
HPF = 1 High-pass filter disabled
Receive Path Gain: RG = 0 6-dB loss not inserted
RG = 1 6-dB loss inserted
Analog Loopback: ALB = 0 Analog loopback disabled
ALB = 1 Analog loopback enabled
TSA Loopback: TLB = 0 TSA loopback disabled
TLB = 1 TSA loopback enabled

22. Read Operating Conditions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	0	1
Output data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

23. Read Revision Code Number

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	1	1
Output data:	#	#	#	#	#	#	#	#

This command returns an 8-bit number describing the revision number of the DSLAC device. It can be read on either channel.

24. Write GX-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	0	0
Input data byte 1:	C40 m40				C30 m30			
Input data byte 2:	C20 m20				C10 m10			

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + \left(C_{10} \cdot 2^{-m10} \{1 + C_{20} \cdot 2^{-m20} [1 + C_{30} \cdot 2^{-m30} (1 + C_{40} \cdot 2^{-m40})]\}\right).$$

25. Read GX-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	0	1
Output data byte 1:	C40 m40				C30 m30			
Output data byte 2:	C20 m20				C10 m10			

26. Write GR-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	1	0
Input data byte 1:	C40 m40				C30 m30			
Input data byte 2:	C20 m20				C10 m10			

The coefficient for the GR filter is defined as:

$$H_{GR} = C_{10} \cdot 2^{-m10}\{1 + C_{20} \cdot 2^{-m20}[1 + C_{30} \cdot 2^{-m30}(1 + C_{40} \cdot 2^{-m40})]\}.$$

27. Read GR-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	1	1
Output data byte 1:	C40 m40				C30 m30			
Output data byte 2:	C20 m20				C10 m10			

28. Write Z Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	0	0
Input data byte 1:	C45		m45		C35		m35	
Input data byte 2:	C25		m25		C15		m15	
Input data byte 3:	C40		m40		C30		m30	
Input data byte 4:	C20		m20		C10		m10	
Input data byte 5:	C41		m41		C31		m31	
Input data byte 6:	C21		m21		C11		m11	
Input data byte 7:	C42		m42		C32		m32	
Input data byte 8:	C22		m22		C12		m12	
Input data byte 9:	C43		m43		C33		m33	
Input data byte 10:	C23		m23		C13		m13	
Input data byte 11:	C44		m44		C34		m34	
Input data byte 12:	C24		m24		C14		m14	
Input data byte 13:	C46		m46		C36		m36	
Input data byte 14:	C26		m26		C16		m16	

The Z-transform equation for the Z filter is defined as:

$$H_Z(z) = Z_0 + Z_1 z^{-1} + Z_2 z^{-2} + Z_3 z^{-3} + Z_4 z^{-4} + \frac{Z_5}{1 - Z_6 z^{-1}}$$

The coefficients are defined as:

$$Z_I = C_{1I} \cdot 2^{-m1I}\{1 + C_{2I} \cdot 2^{-m2I}[1 + C_{3I} \cdot 2^{-m3I}(1 + C_{4I} \cdot 2^{-m4I})]\}$$

for i = 0,1,2,3,4,5,6.

29. Read Z-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	0	1
Output data byte 1:	C45		m45		C35		m35	
Output data byte 2:	C25		m25		C15		m15	
Output data byte 3:	C40		m40		C30		m30	
Output data byte 4:	C20		m20		C10		m10	
Output data byte 5:	C41		m41		C31		m31	
Output data byte 6:	C21		m21		C11		m11	
Output data byte 7:	C42		m42		C32		m32	
Output data byte 8:	C22		m22		C12		m12	
Output data byte 9:	C43		m43		C33		m33	
Output data byte 10:	C23		m23		C13		m13	
Output data byte 11:	C44		m44		C34		m34	
Output data byte 12:	C24		m24		C14		m14	
Output data byte 13:	C46		m46		C36		m36	
Output data byte 14:	C26		m26		C16		m16	

30. Write B-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	1	0
Input data byte 1:	C30		m30		C20		m20	
Input data byte 2:	C10		m10		C31		m31	
Input data byte 3:	C21		m21		C11		m11	
Input data byte 4:	C32		m32		C22		m22	
Input data byte 5:	C12		m12		C33		m33	
Input data byte 6:	C23		m23		C13		m13	
Input data byte 7:	C34		m34		C24		m24	
Input data byte 8:	C14		m14		C35		m35	
Input data byte 9:	C25		m25		C15		m15	
Input data byte 10:	C36		m36		C26		m26	
Input data byte 11:	C16		m16		C37		m37	
Input data byte 12:	C27		m27		C17		m17	
Input data byte 13:	C48		m48		C38		m38	
Input data byte 14:	C28		m28		C18		m18	

The z-transform equation for the B filter is defined as:

$$H_B(z) = B_0 + B_1z^{-1} + B_2z^{-2} + B_3z^{-3} + B_4z^{-4} + B_5z^{-5} + B_6z^{-6} + \frac{B_7z^{-7}}{1 - B_8z^{-1}}$$

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

$$B_I = C_{1I} \cdot 2^{-m1I}[1 + C_{2I} \cdot 2^{-m2I}(1 + C_{3I} \cdot 2^{-m3I})].$$

The feedback coefficient of the IIR B section is defined as:

$$B_8 = C_{18} \cdot 2^{-m18}\ \{1 + C_{28} \cdot 2^{-m28}[1 + C_{38} \cdot 2^{-m38}(1 + C_{48} \cdot 2^{-m48})]\}.$$

Warning: Not all B-filter coefficients are "legal" to initiate adaptive balance. One legal coefficient is set as: 2A F2 AF 2A F2 AF 2A F2 AF 2A F2 AF 0A 80, which corresponds to all FIR coefficients (B_0 through B_7) equal to zero, and the IIR denominator coefficient (B_8) equal to 1/2. Other legal coefficients that may reduce the time to convergence of the algorithm may be obtained by reading back the registers after adaptive balance has been run (see Command #31).

31. Read B-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	1	1
Output data byte 1:	C30	m30			C20	m20		
Output data byte 2:	C10	m10			C31	m31		
Output data byte 3:	C21	m21			C11	m11		
Output data byte 4:	C32	m32			C22	m22		
Output data byte 5:	C12	m12			C33	m33		
Output data byte 6:	C23	m23			C13	m13		
Output data byte 7:	C34	m34			C24	m24		
Output data byte 8:	C14	m14			C35	m35		
Output data byte 9:	C25	m25			C15	m15		
Output data byte 10:	C36	m36			C26	m26		
Output data byte 11:	C16	m16			C37	m37		
Output data byte 12:	C27	m27			C17	m17		
Output data byte 13:	C48	m48			C38	m38		
Output data byte 14:	C28	m28			C18	m18		

32. Write X-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	0	0
Input data byte 1:	C40	m40			C30	m30		
Input data byte 2:	C20	m20			C10	m10		
Input data byte 3:	C41	m41			C31	m31		
Input data byte 4:	C21	m21			C11	m11		
Input data byte 5:	C42	m42			C32	m32		
Input data byte 6:	C22	m22			C12	m12		
Input data byte 7:	C43	m43			C33	m33		
Input data byte 8:	C23	m23			C13	m13		
Input data byte 9:	C44	m44			C34	m34		
Input data byte 10:	C24	m24			C14	m14		
Input data byte 11:	C45	m45			C35	m35		
Input data byte 12:	C25	m25			C15	m15		

The z-transform equation for the X filter is defined as:

$$H_X(z) = X_0 + X_1 z^{-1} + X_2 z^{-2} + X_3 z^{-3} + X_4 z^{-4} + X_5 z^{-5}.$$

The coefficients for the X filter are defined as:

$$X_I = C_{1I} \cdot 2^{-m1I}\{1 + C_{2I} \cdot 2^{-m2I}[1 + C_{3I} \cdot 2^{-m3I}(1 + C_{4I} \cdot 2^{-m4I})]\}.$$

33. Read X-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	0	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	
Output data byte 3:	C41		m41		C31		m31	
Output data byte 4:	C21		m21		C11		m11	
Output data byte 5:	C42		m42		C32		m32	
Output data byte 6:	C22		m22		C12		m12	
Output data byte 7:	C43		m43		C33		m33	
Output data byte 8:	C23		m23		C13		m13	
Output data byte 9:	C44		m44		C34		m34	
Output data byte 10:	C24		m24		C14		m14	
Output data byte 11:	C45		m45		C35		m35	
Output data byte 12:	C25		m25		C15		m15	

34. Write R-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	1	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	
Input data byte 3:	C41		m41		C31		m31	
Input data byte 4:	C21		m21		C11		m11	
Input data byte 5:	C42		m42		C32		m32	
Input data byte 6:	C22		m22		C12		m12	
Input data byte 7:	C43		m43		C33		m33	
Input data byte 8:	C23		m23		C13		m13	
Input data byte 9:	C44		m44		C34		m34	
Input data byte 10:	C24		m24		C14		m14	
Input data byte 11:	C45		m45		C35		m35	
Input data byte 12:	C25		m25		C15		m15	

The z-transform equation for the R filter is defined as:

$$H_R(z) = R_0 + R_1z^{-1} + R_2z^{-2} + R_3z^{-3} + R_4z^{-4} + R_5z^{-5}.$$

The coefficients for the R filter are defined as:

$$R_i = C_{1i} \cdot 2^{-m1i}\{1 + C_{2i} \cdot 2^{-m2i}[1 + C_{3i} \cdot 2^{-m3i}(1 + C_{4i} \cdot 2^{-m4i})]\}.$$

35. Read R-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	1	1
Output data byte 1:	C40			m40	C30			m30
Output data byte 2:	C20			m20	C10			m10
Output data byte 3:	C41			m41	C31			m31
Output data byte 4:	C21			m21	C11			m11
Output data byte 5:	C42			m42	C32			m32
Output data byte 6:	C22			m22	C12			m12
Output data byte 7:	C43			m43	C33			m33
Output data byte 8:	C23			m23	C13			m13
Output data byte 9:	C44			m44	C34			m34
Output data byte 10:	C24			m24	C14			m14
Output data byte 11:	C45			m45	C35			m35
Output data byte 12:	C25			m25	C15			m15

36. Write Echo Path Gain

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	0	0
Input data byte 1:	C80			m80	C70			m70
Input data byte 2:	C60			m60	C50			m50
Input data byte 3:	C40			m40	C30			m30
Input data byte 4:	C20			m20	C10			m10

The equation for the Echo Path Gain is defined as:

$$EPG = 8 \cdot C_{10} \cdot 2^{-m10} \left(1 + C_{50} \cdot 2^{-m50}\{1 + C_{60} \cdot 2^{-m60}[1 + C_{70} \cdot 2^{-m70}(1 + C_{80} \cdot 2^{-m80})]\}\right),$$

C_{20}, M_{20}, C_{30}, M_{30}, C_{40}, and M_{40} must be zero.

37. Read Echo Path Gain

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	0	1
Output data byte 1:	C80			m80	C70			m70
Output data byte 2:	C60			m60	C50			m50
Output data byte 3:	C40			m40	C30			m30
Output data byte 4:	C20			m20	C10			m10

38. Write Error Level Threshold

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	1	0
Input data byte 1:	C20 m20				C10 m10			

The equation for the Error Level Threshold is defined as:

$$ELT = C_{10} \cdot 2^{-m10}(1 + C_{20} \cdot 2^{-m20}).$$

39. Read Error Level Threshold

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	1	1
Output data byte 1:	C20 m20				C10 m10			

Programmable Filters

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the DSLAC device is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1z^{-1} + h_2z^{-2} + \ldots + h_nz^{-n} \qquad \text{Eq. (1)}$$

where the number of taps in the filter = n + 1.

The transfer function for the IIR part of the Z and B filters is:

$$HI(z) = \frac{1}{1 - h_{(n+1)}z^{-1}} \qquad \text{Eq. (2)}$$

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \ldots + B_N 2^{-M_N}, \qquad \text{Eq. (3)}$$

where:

the number of shifts = $M_i \leq M_{i+1}$

sign = $B_i = \pm 1$

N = Number of CSD coefficients.

The value of h_i in Eq. (3) represents a decimal number which is broken down into a sum of successive values of:

± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 ... 1/128....

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Eq. (3) can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take (e.g., if N = 3 the maximum and minimum values are ± 3, and if N = 4 the values are between ± 4).

Detailed Description of DSLAC Device Coefficients

The CSD coding scheme in the DSLAC device uses a value called m_i, where m_1 represents the distance shifted right of the decimal point for the first binary 1. m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Eq. (3) is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + B_3 2^{-M3} + B_4 2^{-M4} \qquad \text{Eq. (4)}$$

$$h_i = C_1 2^{-m1} + C_1C_2 2^{-(m1+m2)} + C_1C_2C_3 2^{-(m1+m2+m3)} + C_1C_2C_3C_4 2^{-(m1+m2+m3+m4)} \qquad \text{Eq. (5)}$$

$$h_i = C_1 2^{-m1} \cdot \{1 + C_2 2^{-m2} \cdot [1 + C_3 2^{-m3} \cdot (1 + C_4 2^{-m4})]\} \qquad \text{Eq. (6)}$$

where:

$M_1 = m_1$ and $B_1 = C_1$

$M_2 = m_1 + m_2$ $B_2 = C_1 \cdot C_2$

$M_3 = m_1 + m_2 + m_3$ $B_3 = C_1 \cdot C_2 \cdot C_3$

$M_4 = m_1 + m_2 + m_3 + m_4$ $B_4 = C_1 \cdot C_2 \cdot C_3 \cdot C_4$

In the DSLAC device, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is 3 bits. Each CSD coefficient is broken down as follows.

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000:	0 shifts
001:	1 shifts
010:	2 shifts
011:	3 shifts
100:	4 shifts
101:	5 shifts
110:	6 shifts
111:	7 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, Z, and the IIR part of the B filter, and 3 for the FIR part of the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters.

$$h_{IGX} = 1 + h_I \qquad \text{Eq. (7)}$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Adaptive B-Filter Overview

The DSLAC device B filter is designed to work with pre-programmed coefficients or with coefficients determined by an adaptive algorithm. **(Note that the adaptive trans-hybrid balance feature is only guaranteed on the A version of the Am79C02/3).** The adaptive algorithm can be operated in a mode where it continuously adapts or where it adapts for a short period and then holds its value.

Operation with pre-programmed coefficients requires only the use of MPI Command #30 to feed in the coefficients. The adaptive mode uses some pre-programmed coefficients and generates new ones using an algorithm By a series of iterations, the algorithm minimizes the receive signal that is echoed in the transmit signal (due to mismatches in the SLIC, hybrid, and line). Adaptation only applies to the FIR part of the filter. Pre-programmed coefficients used to initiate the adaptive algorithm must be "legal" (shown under Command #30 on page 2-88). Other legal coefficients may be obtained by using this coefficient, running adaptive balance, and then reading back the registers (refer to #30 in command structure).

In the continuous adaptation mode, the algorithm is switched on (via MPI Command #19) after a call is connected and remains on until the call ends. In this way, the B filter is continually being optimized to the received signal.

In the adapt and freeze mode, the algorithm is used only when a line is brought into service and the DSLAC device is activated. The algorithm is switched on and is allowed to converge with the received signal, which is a band-limited white noise signal generated in the exchange for this purpose. The noise signal need only be injected for less than a second to yield converged coefficients. The adaptive mode is then switched off (via Command #19).

The converged coefficients may be read out of the DSLAC device (using MPI Command #31) and stored for future reference. The DSLAC device is now optimized for general input signals.

Adaptive Filter Programming

The purpose of the B filter is to cancel the received signal that leaks across the hybrid into the transmit path. The B-filter transfer function must match (as closely as possible) the transfer function of the echo path.

There are two programmable registers associated with the adaptive B filtering. The Echo Path Gain (EPG) is a programmable value that predicts the amount of the receive signal leaking across the hybrid to the transmit path. The EPG is used as part of an algorithm which stops the adaptive filter from iterating in the presence of signals from the subscriber line (near-end talker).

The Error Level Threshold (ELT) is a programmable value that determines the trans-hybrid loss the adaptive filter will attempt to meet. The adaptive algorithm will continue to iterate until it meets the loss requirement specified by the ELT. Both the EPG and ELT values are generated by the AmSLAC2 software program. Please refer to the AmSLAC2 Technical Manual.

User Test Modes

The DSLAC device supports testing by providing both digital and analog loopback paths as shown in Figure 6. In the TSA Loopback Mode, the DR input is connected to the DX output in the Time Slot Assigner circuitry. The TSA Loopback Mode is programmed via Command #21.

A different type of digital loopback is provided when the AISN register is programmed with a value of 10000. In this case, the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN}. This allows the D/A and A/D converters to be included in the digital loopback test. This mode is programmed via Command #13. Note that the signal connected internally from V_{OUT} to V_{IN} is also present on the V_{OUT} pin.

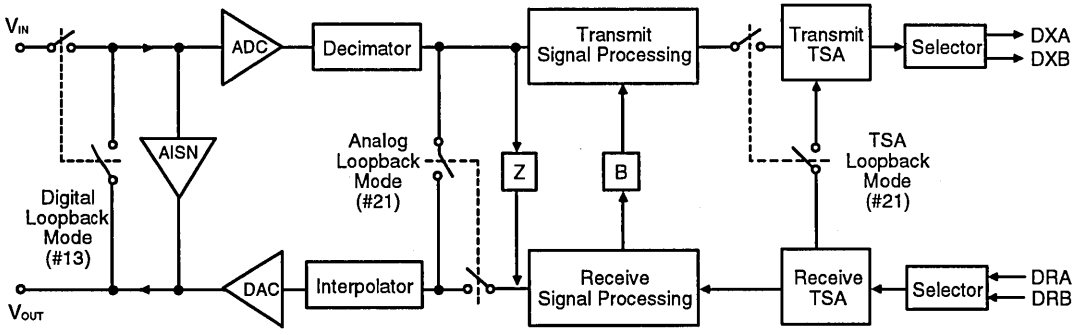
The V_{IN} input can be connected to the V_{OUT} output through the Z filter for analog loopback. The response of the line to low frequencies can be tested by disabling the high-pass filter. Additionally, the receive and transmit paths may be cut off.

APPLICATIONS

The DSLAC device performs a programmable codec/filter function for two telephone lines. It interfaces to the telephone lines through either a transformer or an electronic SLIC such as the Am795XX series devices. The DSLAC device provides latched digital I/O to control and monitor two SLICs and has a 256-kHz clock output to operate the switched mode regulator in an Am795XX. When several line conditions must be matched, the physical SLIC can be constant, and its characteristics (such as apparent impedance, attenuation, and hybrid balance) can be altered by programming each DSLAC channel's coefficients to suit the line. For a transformer-based SLIC, the DSLAC device can drive the transformer without a buffer.

Connection to a dual PCM highway backplane is implemented by means of a simple buffer chip. Several DSLAC devices can be bussed together into one bus interface buffer. An intelligent bus interface chip is not required because each DSLAC device provides its own buffer control. The DSLAC device can be controlled through the Microprocessor Interface, either by a microprocessor on the linecard or by a central processor.

Figures 7 and 8 illustrate typical Am79C02 DSLAC device applications. Figure 7 shows the basic system architecture. Figure 8 illustrates the significant details of the interface to an Am795XX-based SLIC and to a transformer-based SLIC.



09875-010C

Figure 6. Test Mode Operation

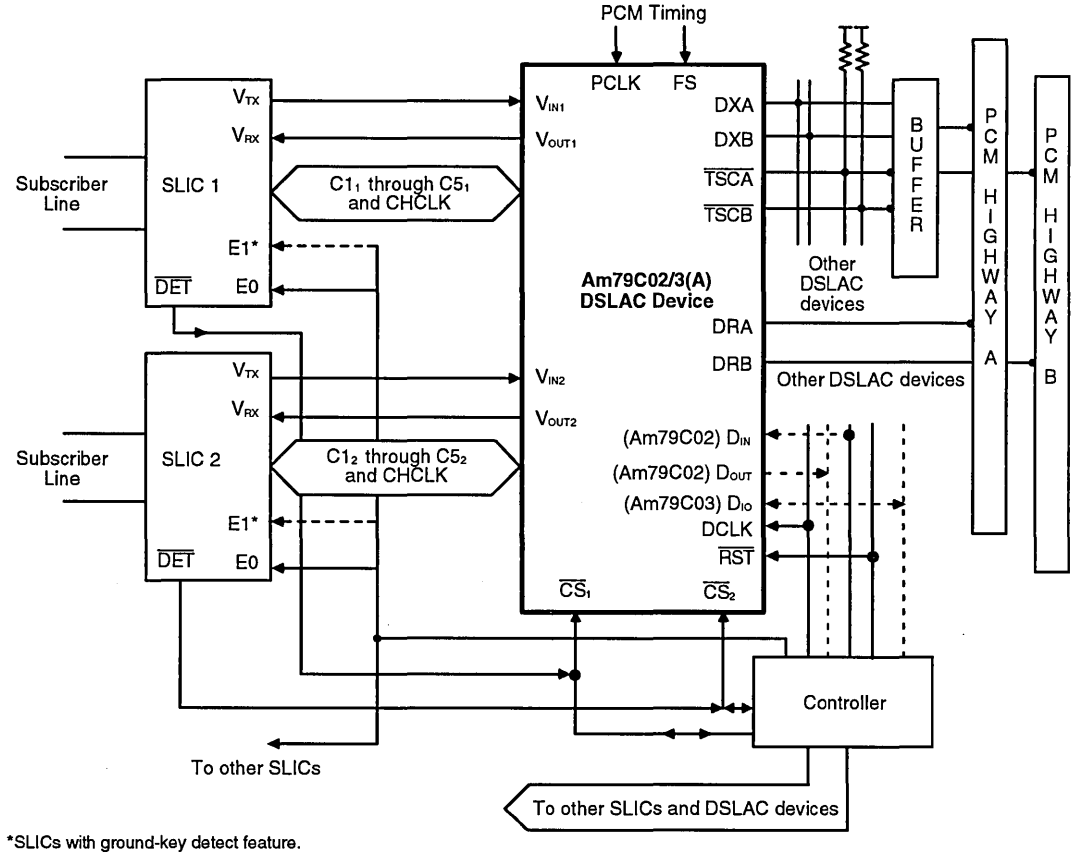


Figure 7. Basic System Architecture

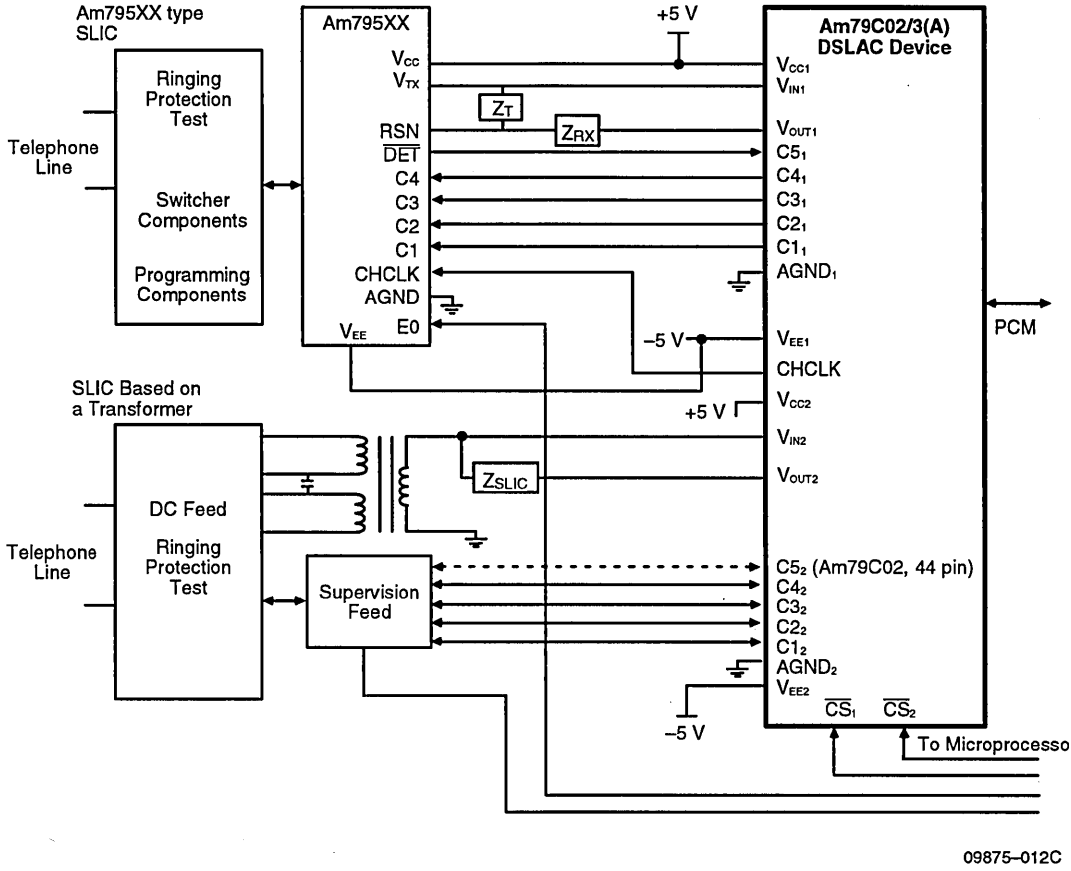


Figure 8. Typical SLIC Connections

Controlling the SLIC

SLIC Chopper Clock

The CHCLK output pin on the DSLAC device drives the CHCLK inputs for Am795XX series SLICs. The CHCLK output is a 256-kHz TTL-compatible signal that can drive two SLICs. It is only active when one or both channels are activated; otherwise it is held High internally.

SLIC Input/Output

The DSLAC device has five TTL-compatible I/O pins (C1 to C5) for each channel. On the 40-pin and 32-pin DSLAC devices, only C1 through C4 are available. On the 44-pin version, C5 (one for each channel) is also available and can be used for another function (for example, to control metering signal injection). The outputs are programmed using Command #15 and the status is read back using Command #16. The direction of the pins (input or output) is specified by programming the SLIC I/O direction register (Command #17).

Calculating Filter Coefficients with AmSLAC2 Software

AmSLAC2 software is a program which models the DSLAC device, the line conditions, the SLIC, and the other linecard components to obtain optimal coefficients for the programmable filters of the DSLAC device and some of the resulting transmission performance plots.

The following parameters relating to the desired line conditions and the components/circuits used in the linecard design are to be provided as input to the program:

1. **Line Impedance.** The line impedance or the balance impedance of the line which is usually specified by the local PTT.
2. **Desired Impedance.** This is the desired terminating impedance at the exchange. This impedance is also specified by the local PTT.
3. **SLIC Impedance.** This is the actual terminating impedance at the exchange.

4. **GR-Filter Attenuation**. This is the desired attenuation for the GR filter.
5. **GX-Filter Gain**. This is the desired gain of the GX filter.
6. **Receive Buffer Transfer Function**. It is quite common to use an amplifier and/or filter between the SLIC and the SLAC device in the design of the linecard. The transfer function of this amplifier/filter is called the Receive Buffer Transfer Function.
7. **Transmit Buffer Transfer Function**. Same as the Receive Buffer Transfer Function but for the Transmit path.
8. **Fuse Resistance and Coupling**. This is the value of the Fuse Resistance and the Coupling capacitor used in the linecard.
9. **Two-Wire Return Loss Template**. The Two-Wire Return Loss Template is usually specified by the local PTT.
10. **Four-Wire Return Loss Template**. The Four-Wire Return Loss Template is usually specified by the local PTT.

The output from the AmSLAC2 program includes the coefficients of the GR, GX, Z, R, X, B, and EPG filters as well as predicted transmission performance plots of (1) two-wire return loss, (2) receive and transmit path frequency response, and (3) four-wire return loss.

The software supports the use of the AMD Am795XX series SLICs or a transformer SLIC, or allows entry of the transfer functions describing the behavior of any type of SLIC (hybrid).

Systems for Customer Evaluation

The DSLAC Low Noise Evaluation Board is designed to demonstrate the high performance capabilities of the DSLAC device. The board is used to evaluate the DSLAC device available in a 40-pin DIP package.

The SLAC/DSLAC Computer Interface Board provides a user-friendly, computer-driven interface to control up to two DSLAC Low Noise Evaluation Boards or SLAC Low Noise Boards. The Computer Interface Board allows an IBM-compatible PC to control a SLAC device, DSLAC device, and a SLIC via its serial port. The board is designed to operate with the DSLAC.IF software program which runs on the PC. A block dia-gram of a typical lab setup is shown in Figure 9.

The Computer Interface Board can also interface to a Hewlett-Packard 3779 series PMA or a Wandel and Goltermann (W&G) PCM-4. These PCM Channel Measurement Sets are used to measure the quality of signal transmission through the DSLAC device.

An RS-232C serial port on the SLAC/DSLAC Computer Interface Board is designed to plug directly into a serial port on the back of a PC. The DSLACIF software program which controls the Computer Interface Board will operate on an IBM PC or compatible computer containing at least one serial port and having at least 512 Kb of memory. The program is capable of running from a floppy disk (360 Kb) or from a hard disk. The DSLACIF software program is completely menu driven and features extensive on-line help.

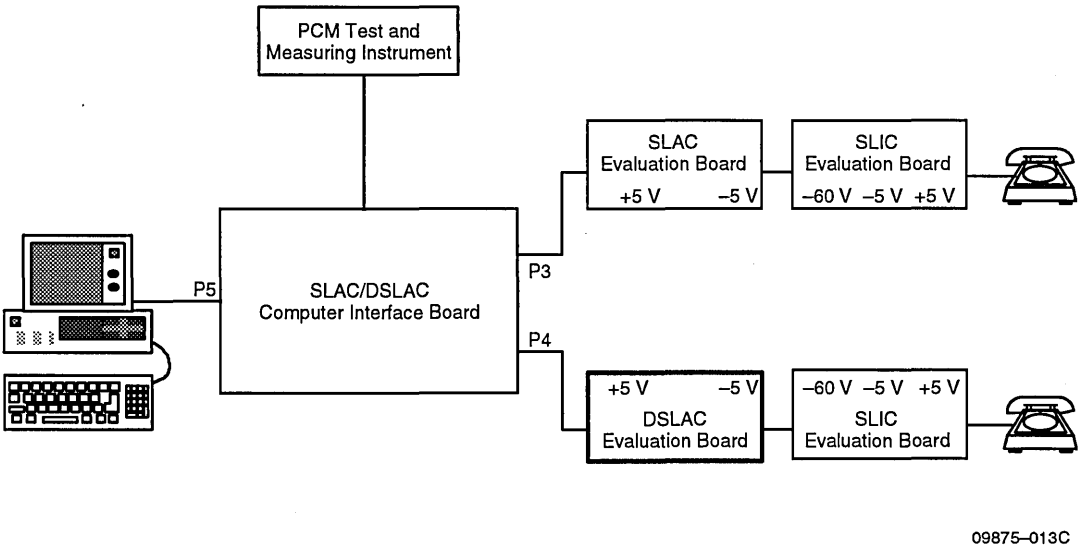


Figure 9. Evaluation System Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... $-60°C \le T_A \le +125°C$
Ambient Operating Temperature . $-40°C \le T_A \le +85°C$
Ambient relative humidity
(noncondensing) ..... 5% to 100%
V_{CCA} with respect to AGND ..... −0.4 V to +7.0 V
V_{CCD} with respect to DGND ..... −0.4 V to +7.0 V
V_{CCP} with respect to PGND ..... −0.4 V to +7.0 V
V_{EE} with respect to AGND ..... +0.4 V to − 7.0 V
V_{IN} with respect to V_{CCA}
(V_{EE} = −5 V) ..... +0.4 V to −10.0 V
V_{IN} with respect to V_{EE}
(V_{CCA} = +5 V) ..... −0.4 V to +10.0 V
Total combined C1–C5 current per channel
Source from V_{CC} ..... 32 mA
Sink into DGND ..... 24 mA
Latch-up immunity (any pin) ..... ±30 mA
Any other pin with respect to $DGND_1$ .. −0.4 V to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Analog Supply V_{CCA1}, V_{CCA2} (V_{CCA}) ..... +5.0 V ±5%
Digital Supply V_{CCD1}, V_{CCD2}, V_{CCP} (V_{CCD}) .. +5.0 V ±5%
Analog Supply V_{EE1}, V_{EE2} ..... −5.0 V ±5%
$DGND_1$, $DGND_2$, PGND (DGND) ..... 0 V
$AGND_1$, $AGND_2$ (AGND) ..... ±50 mV
Ambient Temperature ..... $0°C \le T_A \le +70°C$
Ambient Relative Humidity ..... 15% to 85%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise noted

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in Operating Ranges.

		Preliminary			
Symbol	**Parameter Descriptions**	**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input Low Voltage	−0.5		0.8	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
I_{IL}	Input Leakage Current			±10	µA
V_{OL}	Output Low Voltage				
	C1–C5 (I_{OL} = 6 mA) (Note 2)			0.4	V
	C1–C5 (I_{OL} = 15 mA) (Note 2)			1.0	V
	$\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} = 14 mA)			0.4	V
	Other Digital Outputs (I_{OL} = 2 mA)			0.4	V
V_{OH}	Output High Voltage				
	C1–C5 (I_{OH} = 4 mA) (Note 2)	V_{CC} − 0.4			V
	C1–C5 (I_{OH} = 10 mA) (Note 2)	V_{CC} − 1.0			V
	Other Digital Outputs (I_{OH} = 400 µA)	2.4			V
I_{OL}	Output Leakage Current (H_i = Z State)			±10	µA
V_{IR}	Analog Input Voltage Range (AX = 0 dB)			±3.12	V
	(AX = 6.02 dB)			±1.56	V
V_{IOS}	Offset Voltage Allowed on V_{IN}			±160	mV
I_{IL} (V_{IL})	Input Leakage Current on V_{IN}			±10	µA
Z_{OUT}	V_{OUT} Output Impedance		1	10	ohms
I_{OUT}	V_{OUT} Output Current (f < 3400 Hz) (Note 1)			±6.3	mA

DC CHARACTERISTICS over COMMERCIAL operating range (continued)

Symbol	Parameter Descriptions		Preliminary Min	Typ	Max	Unit
V_{OR}	V_{OUT} Voltage Range	(AR = 0 dB) (AX = 6.02 dB)			±3.12 ±1.56	V V
V_{OOS}	V_{OUT} Offset Voltage (AISN off)				±40	mV
V_{OOSA}	V_{OUT} Offset Voltage (AISN on) (Note 3)				±80	mV
LIN_{AISN}	Linearity of AISN Circuitry (Input = 0 dBm0)				±1/4	LSB
PD	Power Dissipation (MCLK, PCLK = 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		180 120 10	240 160 19	mW mW mW
PD	Power Dissipation (MCLK, PCLK > 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		190 130 10	270 175 19	mW mW mW
I_{CC}	Total +5-V Current	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		24.0 18.0 2.5		mA mA mA
I_{EE}	Total –5-V Current	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		10.0 5.0 0.05		mA mA mA
C_I	Input Capacitance (Digital)			15		pF
C_O	Output Capacitance (Digital)			15		pF
PSRR	Power Supply Rejection Ratio (1.02 kHz, 100 mV_{RMS}, either supply or path, GX = GR = 0 dB)		40			dB

Notes:
1. When the DSLAC device is in the inactive mode, the analog output will present a 0-V output level through an ~3K resistor.
2. The C1–C5 outputs are resistive for less than a 1-V drop. Total current must not exceed absolute maximum ratings.
3. If there is an external DC path from V_{OUT} to V_{IN} with a gain of G_{DC} and the AISN has a gain of h_{AISN}, then the output offset will be multiplied by $1/[1-(h_{AISN} \cdot G_{DC})]$.
4. Power Dissipation in the inactive mode is measured with all digital inputs at $V_{ih} = V_{CC}$ and $V_{il} = V_{SS}$ and with no load connected to V_{OUT1} or V_{OUT2}.

Transmission Characteristics

When the gain in the receive path is set at 0 dB, a 1014-Hz PCM sine-wave input with level 0 dBm0 will correspond to a nominal RMS voltage of 1.55 V for μ-law and 1.56 V for A-law at the analog output. When the gain in the transmit path is set at 0 dB, a 1014-Hz sine-wave signal with a nominal RMS voltage of 1.55 V for μ-law and 1.56 V for A-law will correspond to a level of 0 dBm0 at the digital output.

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the AX + GX gain from 0 to 12 dB and the AR + GR loss from 0 to 12 dB. Performance specification for settings of the AX + GX gain from 12 to 18 dB and the AR + GR loss from 12 to 18 dB will be determined as the device is characterized.

These performance specifications are valid for the commercial temperature range device only. See the DSLAC Extended Temperature Supplement for information on performance over the industrial temperature range (–40°C to +85°C).

Gain Stability

For a 0 dBm0 1014-Hz sine-wave signal, the gains in the transmit and receive paths (with B = 0, Z = 0 & X = R = 1) will not deviate from their ideal value by more than ±0.2 dB at 25°C.

Over the full temperature range (specified in the Operating Ranges), the gains in the transmit and receive paths will not deviate from their ideal values by more than ±0.25 dB.

The variation of the digital to digital loop gain (when the analog input and output ports are connected together) or the analog to analog loop gain (when the digital input and output ports are connected together) will be within ±0.2 dB at 25°C.

Over the full temperature range (specified in the Operating Ranges), the variation of the digital to digital or the analog to analog loop gain will be within ±0.25 dB.

The above specifications apply with reference to temperature and supply voltage variations within the specifications of the Operating Ranges.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown. The reference frequency is 1014 Hz and the signal level is 0 dBm0. The deviation is less than ±0.125 dB for 300 Hz < f < 3000 Hz.

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 11. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

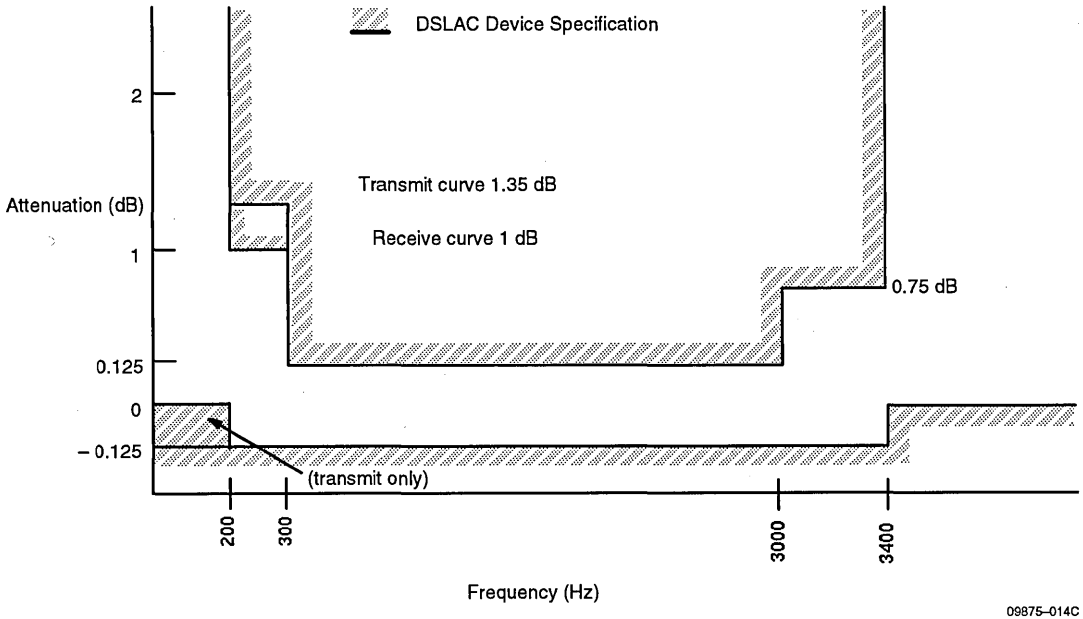


Figure 10. Attenuation Distortion (Single Ended)

Group Delay

The Group Delay specification is defined as the sum of the minimum values of the group delays for the transmit and the receive paths when the transmit and receive time slots are identical and the B, X, R, and Z filters are disabled. For PCLK frequencies greater than 1.53 MHz, the group delay is less than 630 µs. For PCLK frequencies less than 1.03 MHz, the group delay is less than 695 µs. (At PCLK frequencies between these two values, the group delay may vary from one cycle to the next.)

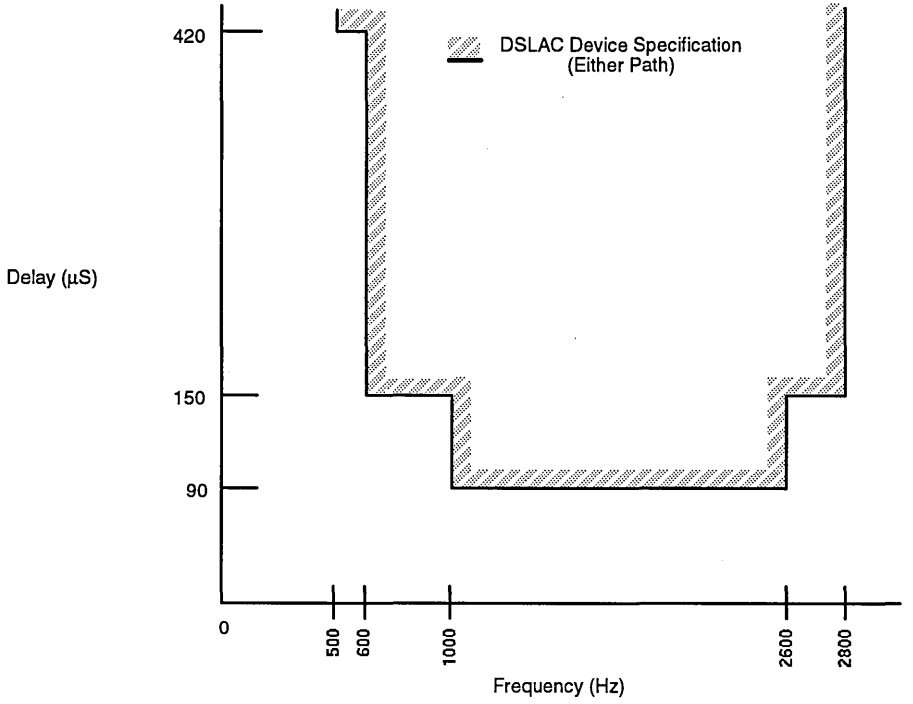


Figure 11. Group Delay Distortion

09875-015C

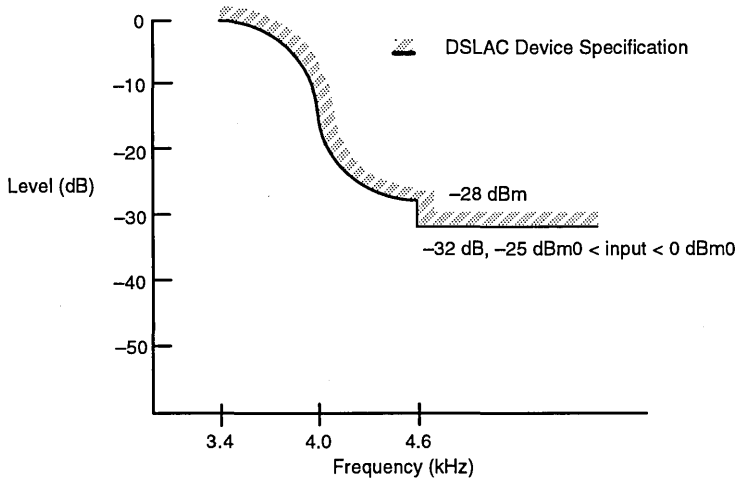
Discrimination Against Out-of-Band Input Signals

When an out-of-band sine-wave signal with frequency f and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output, caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine-wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are:

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz <f< 45 Hz	–25 dBm0 < A≤ 0 dBm0	18 dB
45 Hz <f< 65 Hz	–25 dBm0 < A≤ 0 dBm0	25 dB
65 Hz <f< 100 Hz	–25 dBm0 < A≤ 0 dBm0	10 dB
3400 Hz <f< 4600 Hz	–25 dBm0 < A≤ 0 dBm0	see Figure 12
4600 Hz <f< 100 kHz	–25 dBm0 < A≤ 0 dBm0	32 dB

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (dB)} = 14 - 14 \sin \frac{\pi(4000 - f)}{1200}$$



09875–016C

Figure 12. Discrimination Against Out-of-Band Signals

Discrimination Against 12- and 16-kHz Metering Signals

If the DSLAC device is used in a metering application where 12- or 16-kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of those tones may also appear at the V_{IN} input terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12-kHz tone, the frequency components below 4 kHz will be reduced from the input by at least 48 dB, and for 16-kHz tones, the components are reduced by more than 70 dB.

To avoid degradation of in-band transmission performance, the input levels of these out-of-band tones must be limited. The maximum allowable level at 12 kHz is 100 mV rms, and is 500 mV rms at 16 kHz. An external notch filter at the V_{IN} input to the DSLAC device, incorporated along with the metering injection design, is effective in reducing these tone levels.

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine-wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine-wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 13. The amplitude of the Spurious Out-of-Band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14 \sin \frac{\pi (f - 4000)}{1200} \quad \text{dBm0}$$

Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 Hz to 3400 Hz, other than that due to an applied 0-dBm0 sine-wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3400 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Intermodulation Distortion

Two sine-wave signals of different frequencies f_1 and f_2 (not harmonically related) in the range 300 Hz to 3400 Hz and of equal levels in the range –4 dBm0 to –21 dBm0 do not produce any $2 \cdot f_1 - f_2$ products having a level greater than –42 dB relative to the level of the two input signals.

A sine-wave signal in the frequency band 300 Hz to 3400 Hz with input level –9 dBm0 and a 50-Hz signal with input level –23 dBm0, will not give any intermodulation products exceeding a level of –56 dBm0. These specifications are valid for either transmission path.

Idle Channel Noise

When the signal at the analog input is zero and the digital output (DXA or DXB) is connected to the digital input (DRA or DRB), the maximum levels of the noise measured at the analog output are:

Weighted noise:	–68 dBm0p
Unweighted noise (300–3400 Hz):	–55 dBm0

When the signal at the analog input is zero, the maximum level of the noise measured at the digital output does not exceed –68 dBm0p (A-law) or 19 dBrnc0 (μ-law). When PCM code words representing digital zero are applied to the digital input, the maximum level of the noise measured at the analog output does not exceed –78 dBm0p (A-law) or 12 dBrnc0 (μ-law). No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.

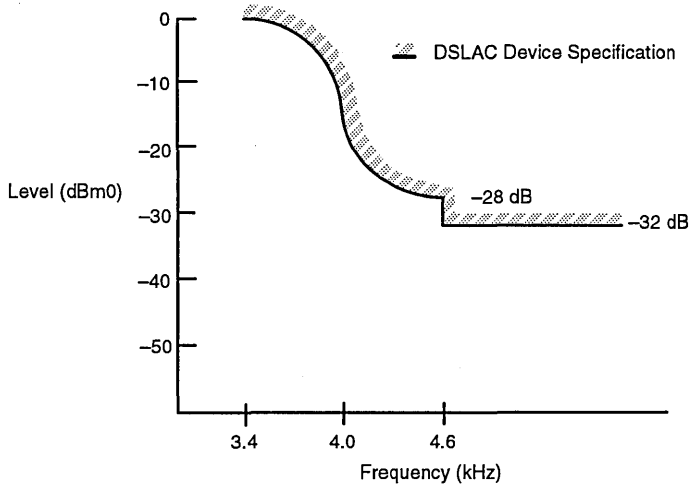


Figure 13. Spurious Out-of-Band Signals

Crosstalk

Transmit to Receive crosstalk within a channel. The crosstalk level at the analog output due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input, is less than –75 dBm0.

Receive to Transmit crosstalk within a channel. The crosstalk level at the digital output due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input, is less than –75 dBm0.

Transmit to Transmit crosstalk between channels. With a 0-dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz applied to the analog input of one channel, the level at the digital output of the other channel does not exceed –76 dBm0.

Transmit to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input of the other channel, will be less than –78 dBm0.

Receive to Transmit crosstalk between channels. The crosstalk level at the digital output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –76 dBm0.

Receive to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –78 dBm0.

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 14 for either transmission path when the input signal is a noise signal (for example, CCITT Rec. O.131).

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 15 for either transmission path when the input is a sine-wave signal of frequency 1014 Hz.

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion ratio will exceed the limits shown in Figure 16 for the receive path when the input signal is a noise signal (for example, CCITT Rec. O.131). The transmit path specification is 1 dB less than that shown for the receive path.

The signal-to-total distortion will exceed the limits shown in Figure 17 for either transmission path when the input is a sine-wave signal of frequency 1014 Hz.

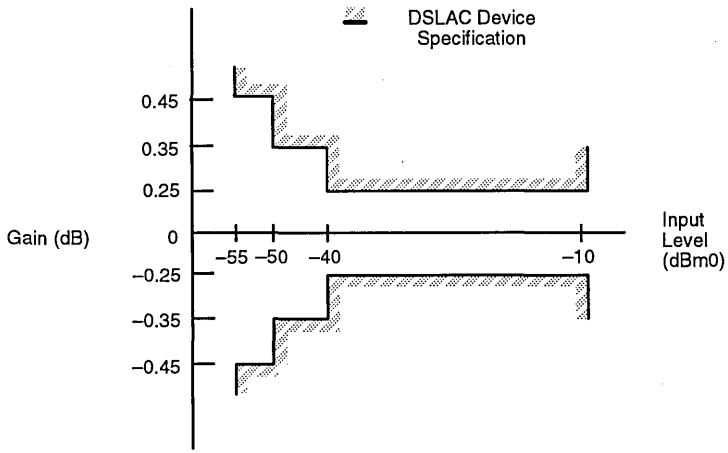


Figure 14. Gain Tracking with Noise Input

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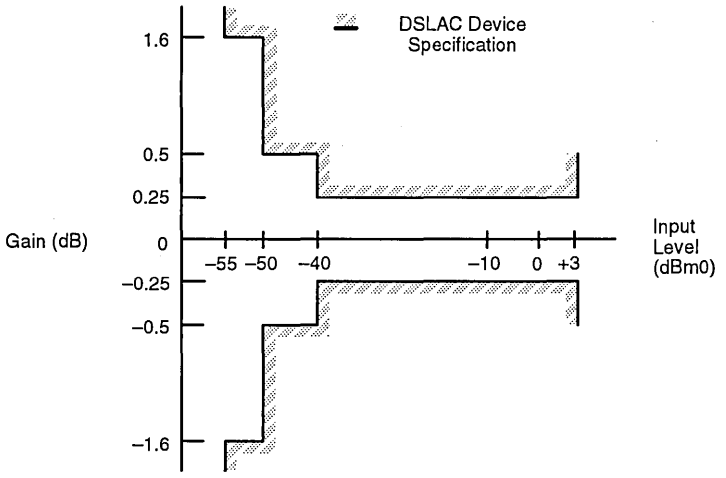

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Figure 15. Gain Tracking with Tone Input

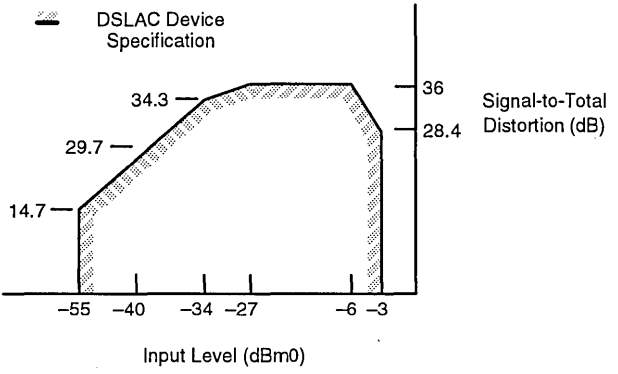

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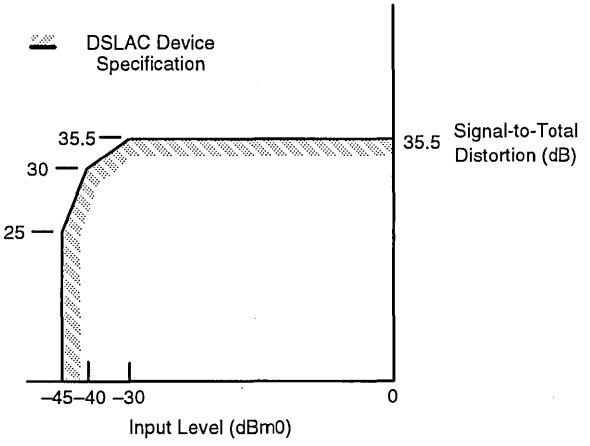
Figure 16. Total Distortion with Noise Input (Receive Path)



09875-021C

Figure 17. Total Distortion with Tone Input (Both Paths)

Overload Compression

Figure 18 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are: (1) 1 dB < GX ≤ 12 dB; (2) –12 dB ≤ GR < –1 dB; (3) PCM output connected to PCM input; and (4) measurement analog-to-analog.

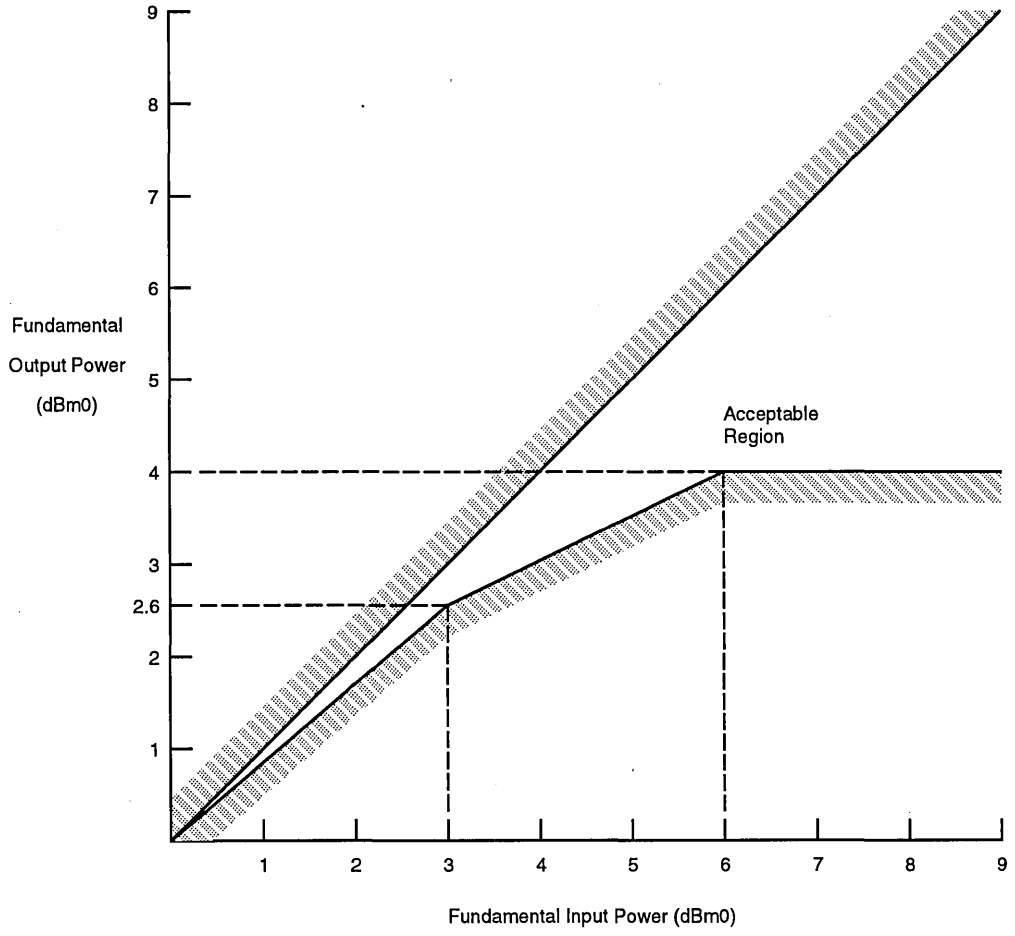


Figure 18. A/A Overload Compression

SWITCHING CHARACTERISTICS over operating range (unless otherwise noted)

Microprocessor Interface

Min and Max values are valid for all digital outputs with a 150-pF load, except C1 to C5 with a 30 pF load. Pull-up resistors of 360 ohms are attached to $\overline{TSCA}$ and $\overline{TSCB}$.

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
1	t_{DCY}	Data Clock Period	244			ns
2	t_{DCH}	Data Clock High Pulse Width (Note 1)	97			ns
3	t_{DCL}	Data Clock Low Pulse Width (Note 1)	97			ns
4	t_{DCR}	Rise Time of Clock			25	ns
5	t_{DCF}	Fall Time of Clock			25	ns
6	t_{ICSS}	Chip Select Setup Time, Input Mode	70		$t_{DCY}-10$	ns
7	t_{ICSH}	Chip Select Hold Time, Input Mode	0		$t_{DCH}-20$	ns
8	t_{ICSL}	Chip Select Pulse Width, Input Mode		$8t_{DCY}$		ns
9	t_{ICSO}	Chip Select Off Time, Input Mode (Note 7)		5		µs
10	t_{IDS}	Input Data Setup Time	30			ns
11	t_{IDH}	Input Data Hold Time	30			ns
12	t_{OLH}	SLIC Output Latch Valid	20		1000	ns
13	t_{OCSS}	Chip Select Setup Time, Output Mode	70		$t_{DCY}-10$	ns
14	t_{OCSH}	Chip Select Hold Time, Output Mode	0		$t_{DCH}-20$	ns
15	t_{OCSL}	Chip Select Pulse Width, Output Mode		$8t_{DCY}$		ns
16	t_{OCSO}	Chip Select Off Time, Output Mode (Note 7)		5		µs
17	t_{ODD}	Output Data Turn On Delay (Note 5)			50	ns
18	t_{ODH}	Output Data Hold Time	0			ns
19	t_{ODOF}	Output Data Turn Off Delay			50	ns
20	t_{ODC}	Output Data Valid	0		50	ns

PCM Interface

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
21	t_{PCY}	PCM Clock Period (Note 2)	0.122		7.8125	µs
22	t_{PCH}	PCM Clock High Pulse Width	48		3890	ns
23	t_{PCL}	PCM Clock Low Pulse Width	48		3890	ns
24	t_{PCF}	Fall Time of Clock			15	ns
25	t_{PCR}	Rise Time of Clock			15	ns
26	t_{FSS}	FS Setup Time	25		$t_{PCY}-50$	ns
27	t_{FSH}	FS Hold Time	50			ns
28	t_{TSD}	Delay to $\overline{TSC}$ Valid (with Programmable Delay) (Note 3)	5 30		80 150	ns ns
29	t_{TSO}	Delay to $\overline{TSC}$ Off (with Programmable Delay) (Note 6)	5 30		80 150	ns ns
30	t_{DXD}	PCM Data Output Delay (with Programmable Delay) (Note 4)	3 30		80 150	ns ns
31	t_{DXH}	PCM Data Output Hold Time (with Programmable Delay) (Note 4)	5 30		80 150	ns ns
32	t_{DXZ}	PCM Data Output Delay to High-Z (with Programmable Delay) (Note 4)	5 30		80 150	ns ns
33	t_{DRS}	PCM Data Input Setup Time	25		70	ns
34	t_{DRH}	PCM Data Input Hold Time	5		150	ns

Master Clock

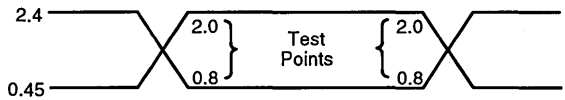
For 2.048 MHz ±100 ppm or 4.096 MHz ±100 ppm operation:

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
35	t_{MCY}	Master Clock Period (2.048 MHz)	488.23	488.28	488.33	ns
		Master Clock Period (4.096 MHz)	244.11	244.14	244.17	ns
36	t_{MCR}	Rise Time of Clock		15		ns
37	t_{MCF}	Fall Time of Clock			15	ns
38	t_{MCH}	MCLK High Pulse Width (2.048 MHz)	200			ns
		MCLK High Pulse Width (4.096 MHz)	80			ns
39	t_{MCL}	MCLK Low Pulse Width (2.048 MHz)	200			ns
		MCLK Low Pulse Width (4.096 MHz)	80			ns

Notes
1. DCLK may be stopped in the High or Low state indefinitely without loss of information. If DCLK is stopped in the High state, $\overline{CS}$ can subsequently make any number of transitions without activating the Microprocessor Interface logic.
2. The PCM clock frequency must be an integer multiple of the frame sync frequency with a long term accuracy of 100 ppm. The maximum allowed PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz. A PCLK of 1.544 MHz may easily be used for standard U.S. transmission systems.
3. $\overline{TSC}$ is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time/clock-slot register.
4. There is a special conflict detection circuitry which will prevent high-power dissipation from occurring when the DXA or DXB pins of two DSLAC devices are tied together and one DSLAC device starts to transmit before the other has gone into a high-impedance state.
5. The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.
6. t_{TSO} is defined as the time at which the output achieves the open circuit condition.
7. The DSLAC device requires 40 cycles of the 8-MHz internal clock (5 µs) between SIO operations. If the MPI is being accessed while the MCLK input is not active, a Chip Select Off time of 20 µs is required.

SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



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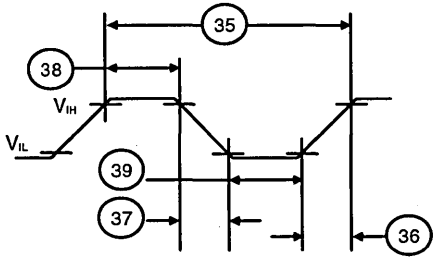
Master Clock Timing



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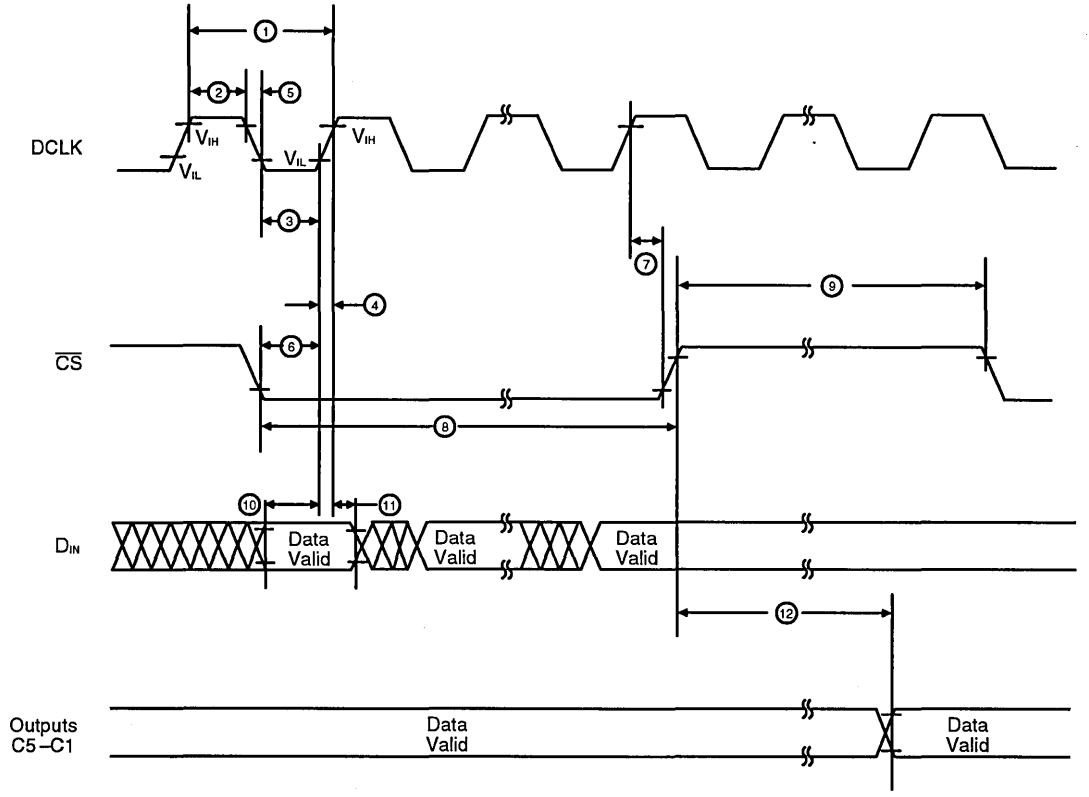
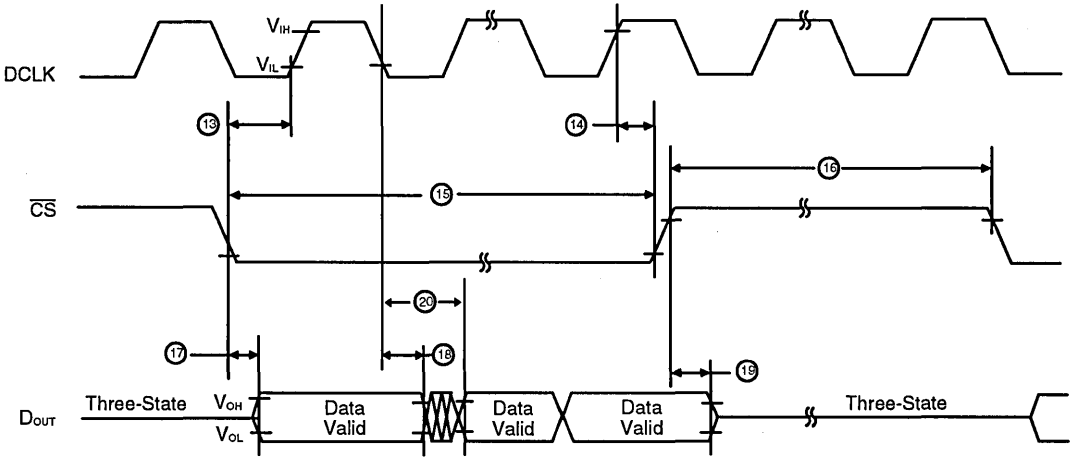
Microprocessor Interface (Input Mode)



09875–025C

Microprocessor Interface (Output Mode)



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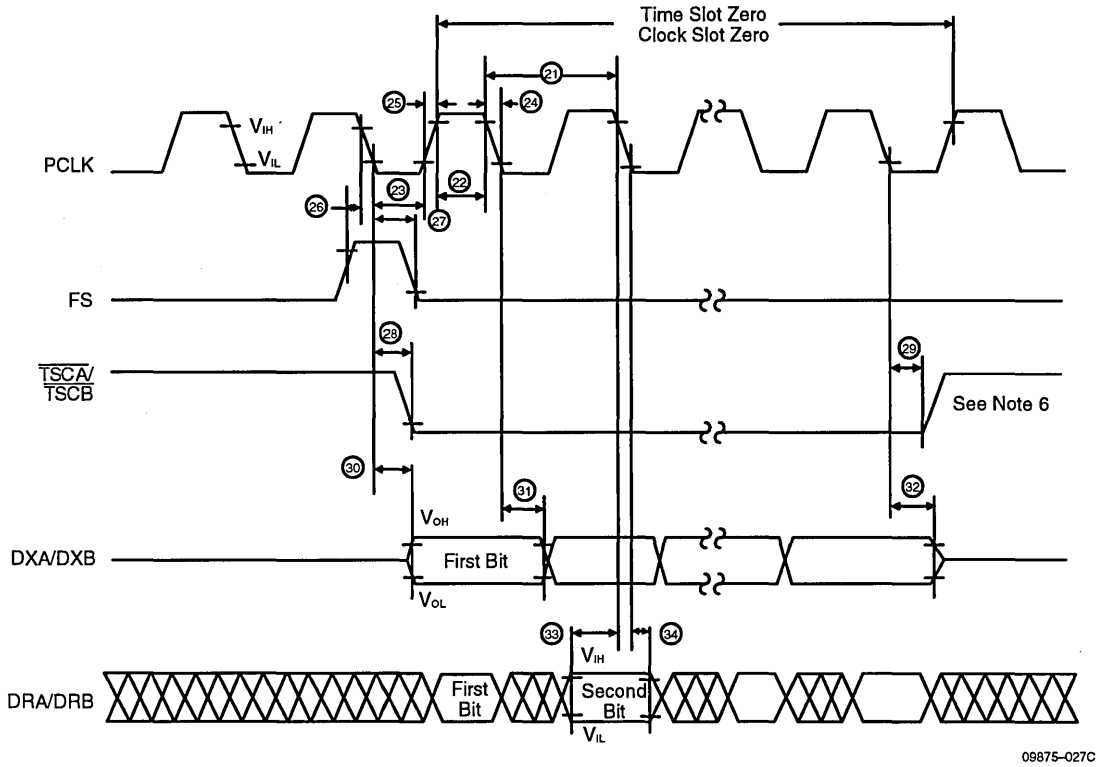
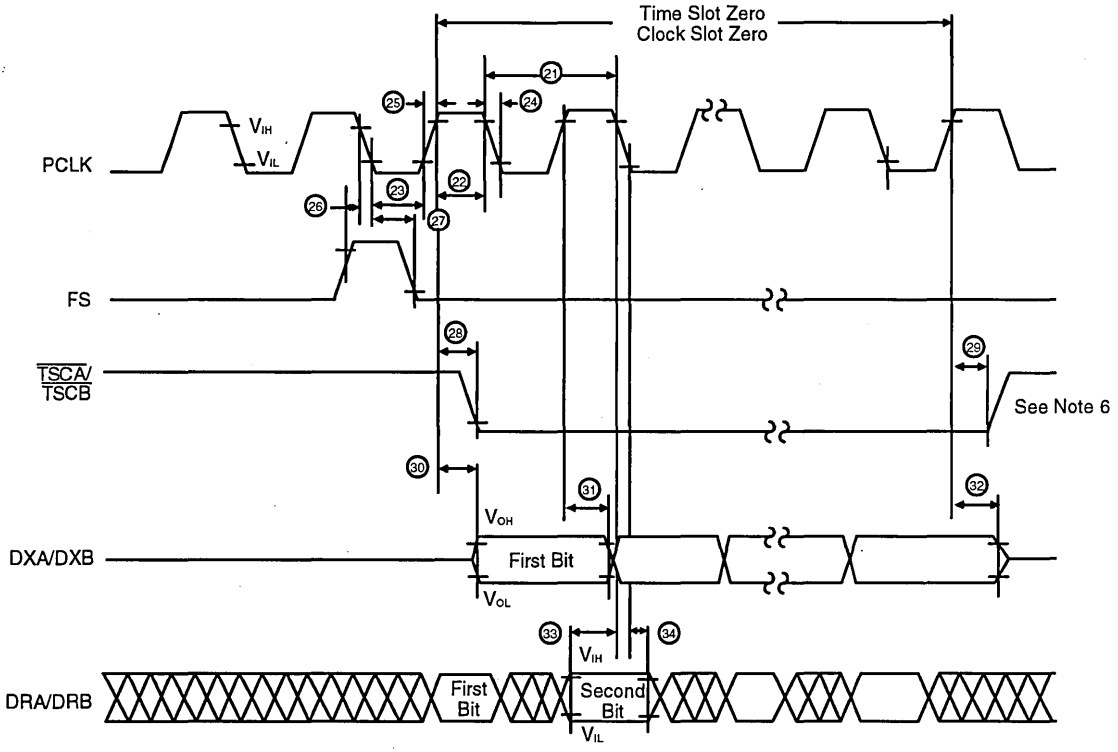
PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)



09875-027C

PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



Note: In this mode, the PCM transmit timing is compatible with other CODEC IC's.

09875–027C

PRELIMINARY

Am79C04(A)

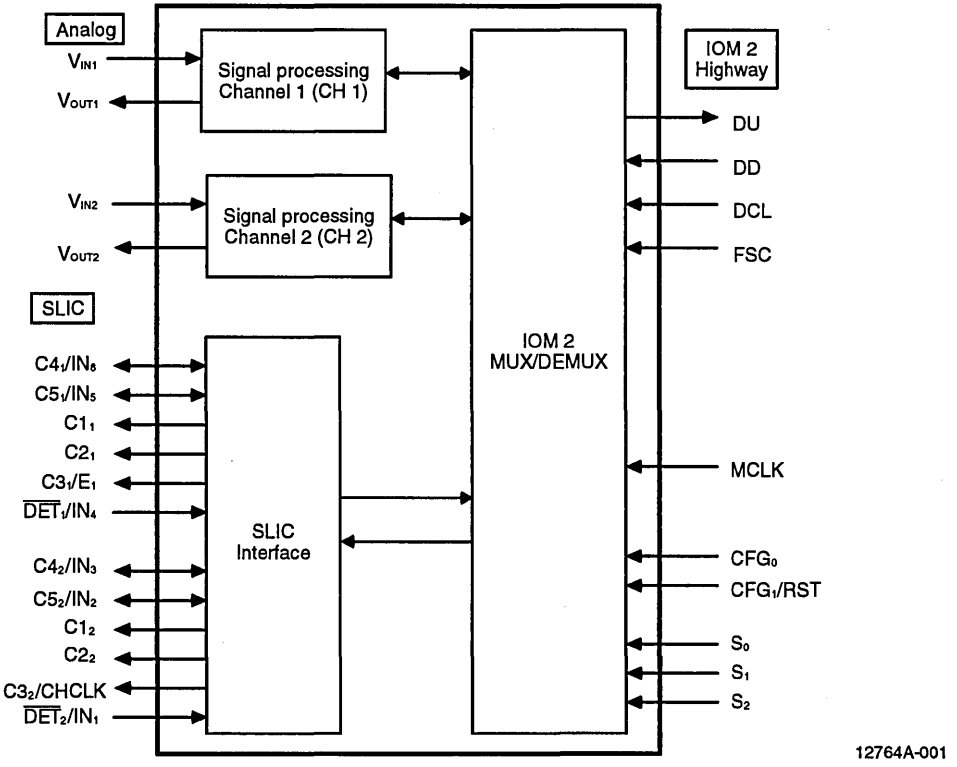
Dual Subscriber Line Audio-Processing Circuit (DSLAC™ Device)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **IOM 2 Interface**
  - —Control and PCM on one bus
  - —Data rate up to 4.096-MHz independent of master clock
- **Two independent channels**
- **Software programmable**
  - —SLIC impedance
  - —Trans-hybrid balance
  - —Transmit and receive gains
  - —Equalization
  - —Digital I/O pins with input debouncing
- **A-law or μ-law coding**
- **Adaptive trans-hybrid balance function (Am79C04/A only)**
- **2.048- or 4.096-MHz master clock**
- **Simple interface to Am795XX series SLICs**
- **Direct transformer drive**
- **Built-in test modes**
- **Low-power CMOS**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12-dB gain range**

BLOCK DIAGRAM



12764A-001

Publication #: 12764 Rev. C Amendment /0
Issue Date: June 1992

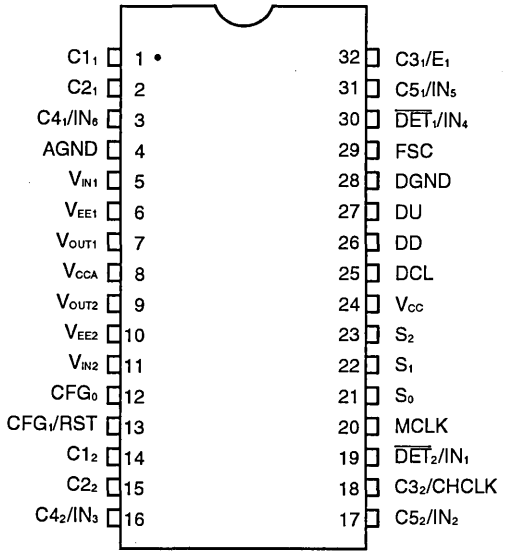
GENERAL DESCRIPTION

The DSLAC IC is designed to be used in telecommunication linecards for both PBX and central office telephone exchanges. It converts the analog signal from the subscriber to digital PCM-encoded signals for transmission on the IOM 2 highway and converts a PCM-encoded signal received from an IOM 2 highway to an analog signal to be sent to the subscribers. The advanced architecture of the DSLAC device implements two independent channels and employs digital filters to allow software control of transmission parameters.

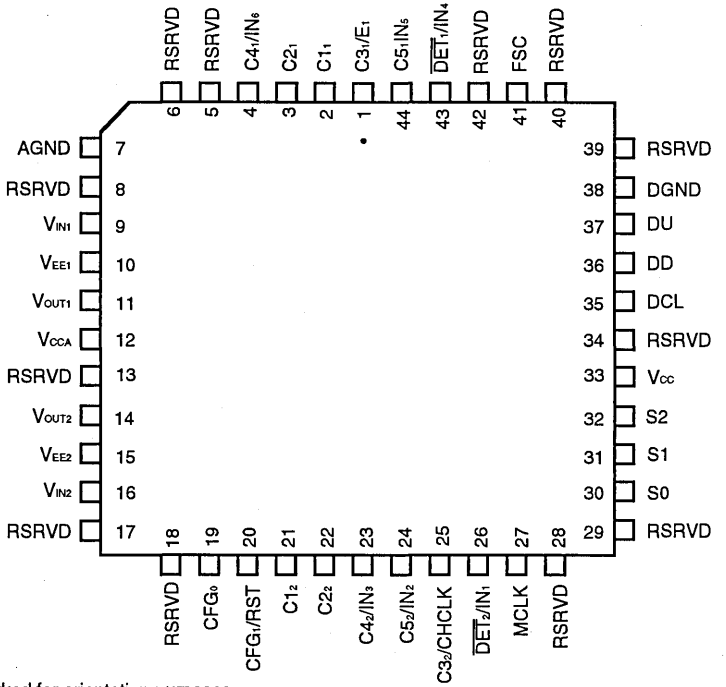
Advanced CMOS technology gives the economical DSLAC device both the functions and the low-power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC device provides a complete dual-channel, software-configurable solution to the BORSCHT (Battery feed, Overvoltage protection, Ringing, Supervision, coding, Hybrid and Test) function.

CONNECTION DIAGRAMS
Top View

32-Pin DIP



44-Pin PLCC

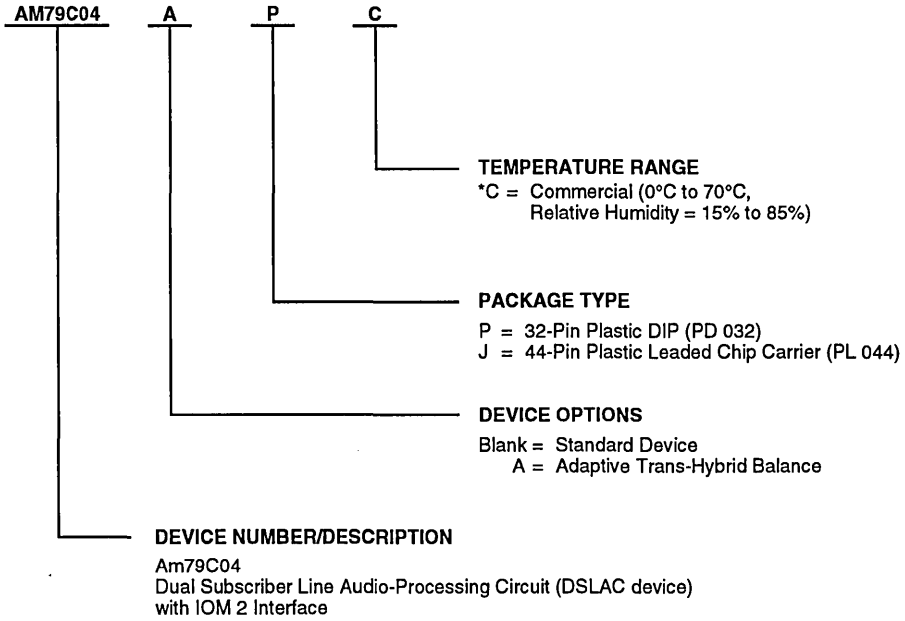


Note: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C04	AJC, APC, JC, PC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

* The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the DSLAC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND

Analog Ground

$C1_1$, $C2_1$, $C3_1/E_1$, $C1_2$, $C2_2$, $C3_2$/CHCLK

SLIC Outputs

These latched outputs are TTL compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line. $C1_1$, $C2_1$, and $C3_1/E_1$ are associated with Channel 1 and $C1_2$, $C2_2$, and $C3_2$/CHCLK are associated with Channel 2. The outputs are set to a Low level when the device is powered up. The C/I (Command/Indicate) channel is then used to write data to these pins.

In the Multiplexed mode, the $C3_2$/CHCLK output provides a 256-kHz or 273-kHz, 50% duty-cycle clock for use by two SLICs. The CHCLK frequency is synchronous to MCLK, but the phase relationship to MCLK is random. It is capable of driving two TTL inputs. As CHCLK, this output is only active when one or both channels are in the active state; otherwise it is held High. In the Multiplexed mode, the $C3_1/E_1$ output is used to control the $\overline{DET}$ output from an Am795XX series SLIC. A High level allows the SLIC to output its ground-key detect status while a Low level allows the SLIC to output the status of its off-hook detector. $C3_1/E_1$ can be programmed to go to a High level for approximately 16 µs every 1 to 15 ms to demultiplex the $\overline{DET}$ inputs.

$C5_1/IN_5$, $C5_2/IN_2$, $C4_1/IN_6$, $C4_2/IN_3$

SLIC Inputs/Outputs

Each pin may be programmed to be an input or output. $C4_1/IN_6$ and $C5_1/IN_5$ are associated with Channel 1 and $C4_2/IN_3$ and $C5_2/IN_2$ are associated with Channel 2. All pins are set to the Input mode when the device is powered up. If these pins are programmed to be outputs, they are written via the C/I channel. These lines are TTL compatible with latched outputs and may be used to control the operation of a SLIC or any other device associated with the subscriber line. If the pins are programmed to be inputs, $C4_1/IN_6$ will appear as C/I upstream bit 6, $C5_1/IN_5$ will appear as C/I upstream bit 5, $C4_2/IN_3$ will appear as C/I upstream bit 3, and $C5_2/IN_2$ will appear as C/I upstream bit 2. The Monitor Channel may be used to read the data on these pins.

CFG_1/RST, CFG_0

Configuration Number Assignment

These inputs allow a configuration number assignment from 0 to 5 by connecting them to either –5 V, ground, or +5 V. A voltage of greater than +2 V applied to the CFG_1/RST input causes the device to perform a hardware reset. For proper operation, CFG_0 should be hardwired to one of the DSLAC device's power supplies.

DCL

IOM 2 Clock

The IOM 2 clock determines the rate at which IOM 2 data is serially shifted into or out of the IOM 2 ports. This rate is twice the desired bit rate. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 512 kHz. The IOM 2 clock may be asynchronous to MCLK.

DD

IOM 2 Downstream Input

Downstream data is received serially on the DD port every 125 µs at half the DCL rate.

$\overline{DET_1}/IN_4$, $\overline{DET_2}/IN_1$

Loop Status Detector Inputs

In the Multiplexed mode, the $\overline{DET_1}/IN_4$ and $\overline{DET_2}/IN_1$ inputs are intended to monitor outputs from a Subscriber Line Interface Circuit (SLIC), providing off-hook and ground-key sensing on the same signal. When the E_1 output is Low, the IOM 2 DSLAC device interprets $\overline{DET_1}/IN_4$ or $\overline{DET_2}/IN_1$ as off-hook detector inputs. When E_1 is High, the DSLAC device interprets these pins as ground-key detector inputs. These pins may also be used in a non-Multiplexed mode, whereby the $\overline{DET_1}/IN_4$ input is routed to the C/I upstream bit 4 and the $\overline{DET_2}/IN_1$ input is routed to the C/I upstream bit 1. These inputs are TTL compatible.

DGND

Digital Ground

DU

IOM 2 Upstream Output

Upstream data is output serially on the DU pin every 125 µs at half the DCL rate. DU is high impedance between bursts. This pin is an open-drain output.

FSC

Frame Sync

The Frame Sync pulse is an 8-kHz signal which identifies the beginning of a frame. The IOM 2 DSLAC device references individual time slots with respect to the Frame Sync pulse. FSC is synchronized to DCL.

MCLK

Master Clock

The Master Clock is a 2.048- or 4.096-MHz clock input for use by the digital signal processor. DCL may be asynchronous to MCLK.

S_2–S_0

Time Slot Number Assignment

These inputs are used for a time slot number assignment from 0 to 7. They direct the DSLAC device to input and output PCM and programming information on one of eight time slots.

V_{CC}

Digital Power Supply

+5-V digital power supply.

V_{CCA}

Analog Power Supply

+5-V analog power supply must be connected to the +5-V digital power supply.

V_{EE1}

–5-V power supply—Channel 1.

V_{EE2}

–5-V power supply—Channel 2.

V_{IN1},V_{IN2}

Analog Inputs

The analog input is applied to the transmit path of the IOM 2 DSLAC device. The signal is sampled, digitally processed, and encoded for the IOM 2 PCM output. V_{IN1} is for Channel 1 and V_{IN2} is for Channel 2.

V_{OUT1},V_{OUT2}

Analog Outputs

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is for Channel 1 and V_{OUT2} is for Channel 2. These outputs may be used to drive a transformer SLIC directly.

FUNCTIONAL DESCRIPTION

The DSLAC device performs the Codec/filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. The PCM codes are 8-bit and are programmed to be either A-law or μ-law companded. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive trans-hybrid balancing is a feature of the Am79C04A. All programmable digital filter coefficients can be calculated using AmSLAC2™ software.

The independent channels allow the DSLAC device to function as two SLAC™ devices. All of the digital filtering is performed in digital signal processors operating from either a 2.048-MHz or 4.096-MHz external clock. The A/D, D/A, and signal processing are separate for each channel. The IOM 2 DSLAC device is available in a 32-pin DIP or a 44-pin PLCC.

This section describes the operation of the IOM 2 interface portion of the Am79C04 DSLAC device. The operational and signal processing features of the Am79C04 DSLAC device are identical to the Am79C02. A full description of these features can be found in the Am79C02 data sheet.

Operational Modes

See the Am79C02/3(A) Data Sheet.

Signal Processing

See the Am79C02/3(A) Data Sheet.

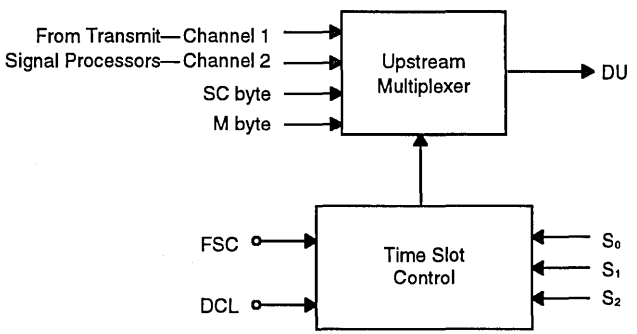
IOM 2 Interface

The IOM 2 Interface allows communication of both control and voice data between the IOM 2 highway and subscriber line circuits over a single pair of pins on the DSLAC device.

Upstream IOM 2 Interface

The upstream IOM 2 Interface logic (Figure 1) receives an 8-bit compressed voice code from each subscriber channel signal processor. Also input to the multiplexer are a Status and Control (SC) byte containing subscriber line status information and a Monitor (M) byte containing processor status information. These four inputs are formed into a 4-byte time slot by the upstream multiplexer and sent upstream via the DU pin on the DSLAC device. The frame sync (FSC) pulse identifies the beginning of a frame and all time slots are referenced to it.

The time slot is determined by the code appearing on the Time Slot Assignment pins, S_2–S_0. This allows up to eight 4-byte time slots (using a DCL of 4.096 MHz) in each frame. This feature allows any clock frequency between 512 kHz and 4.096 MHz (1 to 8 time slots) in a system. Frequencies between 4.096 MHz and 8.192 MHz are allowed, but only the first eight time slots are used.



12764A-002

Figure 1. Transmit (Upstream) IOM 2 Interface

Downstream IOM 2 Interface

The downstream IOM 2 Interface logic (Figure 2) demultiplexes a time slot (determined by the code on pins S_2–S_0) from the downstream data on input DD of the DSLAC device. The time slot contains voice data destined for each of the subscriber line signal processors. Also obtained from the time slot are an SC byte used for SLIC I/O programming and an M byte used for signal processor programming.

As in the upstream interface, one to eight 4-byte time slots are allowed in each frame (using a DCL frequency of 512 kHz to 4.096 MHz).

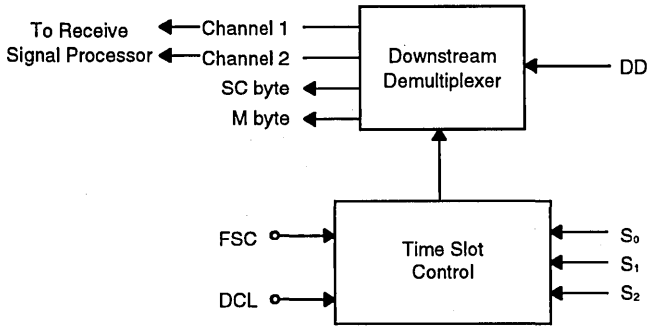
IOM 2 FORMAT AND COMMAND STRUCTURE

IOM 2 Format

A complete IOM 2 frame is sent upstream on the DU pin and received downstream on the DD pin every 125 µs. Each frame consists of up to eight 4-byte time slots. The overall structure of the IOM 2 frame is shown in Figures 3 and 4. Figure 3 shows the pattern when only a single IOM 2 time slot is used with a 256 kb/s bit rate. In this case the same 32-bit time slot is sent for every frame. Figure 4 shows the pattern when the maximum capacity of eight IOM 2 time slots is used. In this case, a bit rate of 2048 kb/s is needed. Any number of time slots between 1 and 8 can be used, provided the bit rate is adjusted such that a complete frame of time slots can occur every 125 µs. Note that the DCL clock input must be set at a frequency of twice the desired bit rate.

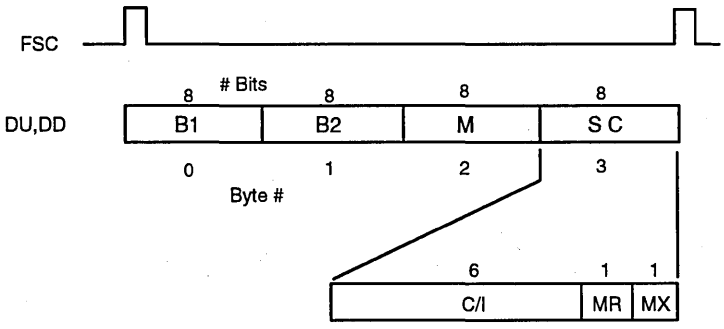
An individual 4-byte IOM 2 time slot contains the following:

- Two bytes, B1 and B2, containing voice data for two separate channels. One IOM 2 time slot can serve two analog subscriber lines.
- One Monitor (M) byte for reading and writing control data and DSP coefficients.
- One Signaling and Control (SC) byte containing a 6-bit Command/Indicate (C/I) field for control information and a 2-bit field with Monitor Receive and Monitor Transmit (MR and MX) bits for handshaking functions. All principal signaling information is carried on the C/I channel.



12764A-003

Figure 2. Receive (Downstream) IOM 2 Interface



12764A-004

Figure 3. IOM 2 Time Slot Structure (256 kb/s)

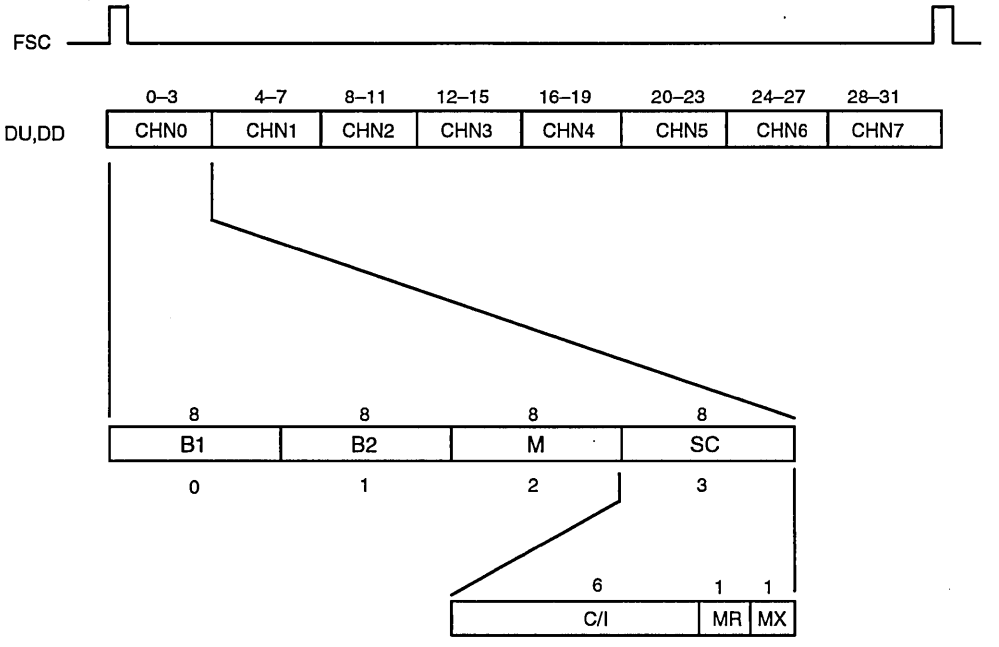


Figure 4. Multiplexed IOM 2 Time Slot Structure (2048 kb/s)

Programming the DSLAC device is accomplished by using the Signaling and Control (SC) and Monitor (M) bytes of the downstream IOM 2 channel. Additionally, data programmed previously may be read out for verification via the upstream IOM 2 channel M and SC bytes. For each subscriber channel, commands are provided to assign values to the following parameters:

Transmit gain

Receive loss

B-filter coefficients

X-filter coefficients

R-filter coefficients

Z-filter coefficients

Adaptive B-filter parameters

AISN coefficient

Switch-hook/ground-key sampling interval

Debounce time for SLIC input port

Read/Write SLIC input/output

Enable/disable GX filter

Enable/disable GR filter

Enable/disable B filter

Enable/disable X filter

Enable/disable R filter

Enable/disable Z filter

Enable/disable adaptive B filter

Enable/disable AX amplifier

Enable/disable AR amplifier

Selection of A-law or μ-law code

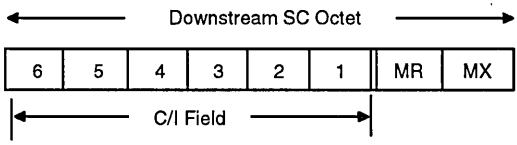
Selection of test modes

Selection of active or standby mode

The SC Channel Command Structure

Downstream C/I Channel

C/I bit 6, the first bit received of the SC octet, is the address bit and selects whether the data in C/I bits 5 through 1 is intended for Channel 1 or Channel 2. C/I bits 5 through 1 are directed to C_5 through C_1, provided these SLIC I/O bits are programmed to be outputs. Any data directed to a SLIC line programmed to be an input would be ignored.



Downstream Bit Definitions of C/I field:

Bit 6—Address bit. A0 selects Channel 1. A1 selects Channel 2

Bit 5—Data to C5 (if configured to be an output)

Bit 4—Data to C4 (if configured to be an output)

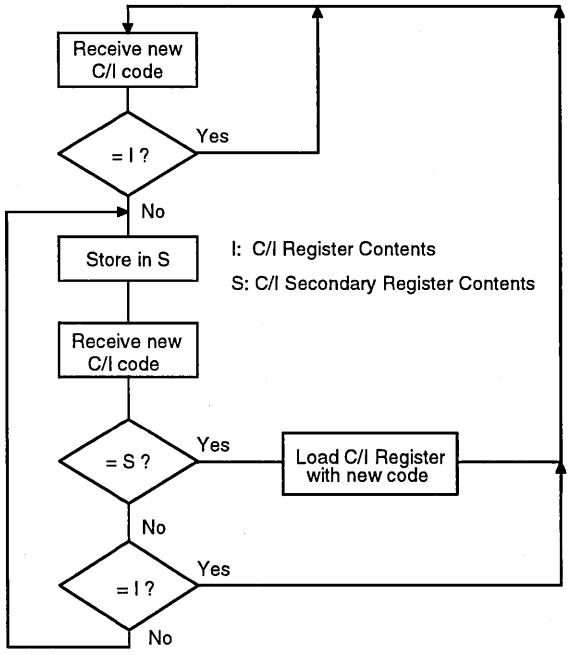
Bit 3—Data to C3 (in non-Multiplexed mode)

Bit 2—Data to C2

Bit 1—Data to C1

Figure 5 shows a flow chart describing the maximum security protocol. Whenever the received pattern of C/I bits 6 through 1 is different from the pattern currently in the C/I input register, the new pattern is loaded into a secondary C/I register. When the next pattern is received (in the following cycle), the following rules apply:

1. If the channel is addressed in the following frame and the received pattern corresponds to the pattern in the secondary register, then the new pattern is loaded into the C/I register.
2. If the channel is not addressed in the following frame, the newly received pattern is loaded into the secondary C/I and the content of the C/I register is unchanged.
3. If the channel is addressed in the following frame but the received pattern is different from the pattern in the secondary register and different from the pattern currently in the C/I register, the newly received pattern is loaded into the secondary C/I register.
4. If the channel is addressed in the following frame but the received pattern is the same as the pattern currently in the C/I register, the C/I register is unchanged. The result is the C/I field (6–1) must be the same for two consecutive frames before it is latched internally.

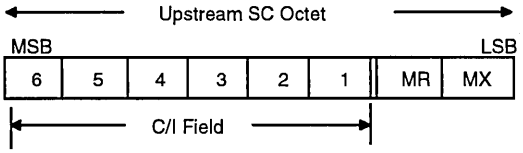


12764A–006

Figure 5. Security Procedure for C/I Downstream Byte

Upstream C/I Channel

There are three upstream C/I bits for each of the two analog lines. C/I bits 4, 5, and 6 are used for Channel 1, while C/I bits 1, 2, and 3 are used for Channel 2. Since the upstream receiving device will also be applying a last look security protocol to the complete 6-bit C/I field, and since changes to the C/I pattern will not be synchronized between two independent source devices, each new 3-bit pattern must be present in at least three consecutive 125-µs frames to ensure transfer.



Upstream Bit Definitions of C/I field:

Bit 6—$C4_1/IN_6$, if $C4_1/IN_6$ is programmed to be an input, High otherwise

***Bit 5**—Ground-key detect, Channel 1 (Multiplexed mode), or $C5_1/IN_5$ (non-Multiplexed mode if pin is programmed to be an input), or logic 1 (if pin is programmed to be an output)

***Bit 4**—Switch-hook detect, Channel 1 (Multiplexed mode), or $\overline{DET}_1/IN_4$ (non-Multiplexed mode)

Bit 3—$C4_2/IN_3$, if $C4_2/IN_3$ is programmed to be an input, High otherwise

***Bit 2**—Ground-key detect, Channel 2 (Multiplexed mode), or $C5_2/IN_2$ (non-Multiplexed mode if pin is programmed to be an input), or logic 1 (if pin is programmed to be an output)

***Bit 1**—Switch-hook detect, Channel 2 (Multiplexed mode), or $\overline{DET}_2/IN_1$ (non-Multiplexed mode)

*The data sent from the DSLAC device on bits 5, 4, 2, and 1 reflect the output from the corresponding debounce circuit, if enabled.

The Monitor Channel

Monitor Channel Protocol

The Monitor Channel is used to load internal device registers, to read the status of the device and the contents of the internal registers, and to provide supplementary signaling. Information is transferred on the Monitor Channel using the MR and MX bits of the fourth (SC) octet to provide a reliable method of handshaking.*

Monitor byte information is transferred via the IOM 2 Interface between read/write registers in the DSLAC device and upstream devices using the following procedure (refer to Figures 6 through 9). Note that the active state of the MX and MR bits is Low.

1. The MX bit remains in the inactive state for two or more consecutive frames to indicate an idle state or an end of transmission on the Monitor channel.
2. A start-of-message is initiated by the sender by a transition of the MX bit from the inactive state to the active state together with the first byte transmitted in the monitor data octet of the same frame. The transmission may start only if the MR bit received by the transmitter has previously been in the inactive state for at least two frames. The receiver acknowledges start-of-messages by a transition of its MR bit to the active state and confirms receipt of the first byte by holding the MR bit in the active state for a second frame.
3. The transition of the MX bit from the active to the inactive state indicates the transmission of a new byte. The transition of the MX bit from the inactive state to the active state in the following frame indicates a repeat of the new data byte.
4. The transition of the MX bit from the active to the inactive state, followed by a repeat of the inactive state for at least one or more frames, indicates end-of-message and that the content of the monitor data field is invalid.
5. The transition of the MR bit from the active to the inactive state acknowledges receipt of the first transmission of a new byte. The transition of the MR bit from the inactive to the active state in the following frame confirms the new byte has been correctly received.
6. The transition of the MR bit from the active to the inactive state, followed by a repeat of the inactive state for at least one more frame, acknowledges the receipt of end-of-message or, if received before end-of-message has been transmitted, requests to abort the message and repeat.
7. The active state of the MX bit, accompanied by further transmissions of the current data byte, may continue indefinitely (subject to a time out) for the purpose of flow control.
8. The active state of the MR bit may continue indefinitely (subject to a time out) for the purpose of flow control.

Each data byte is repeated until the transmission of a new byte, an end-of-message, or an abort.

*The IOM 2 DSLAC device will acknowledge receipt of a Monitor byte only if it is identical to the Monitor byte of the previous Frame. [This is the same security protocol used for the C/I bits (6–1).]

The circled numbers in Figures 6 through 9 refer to the sequence numbers listed previously:

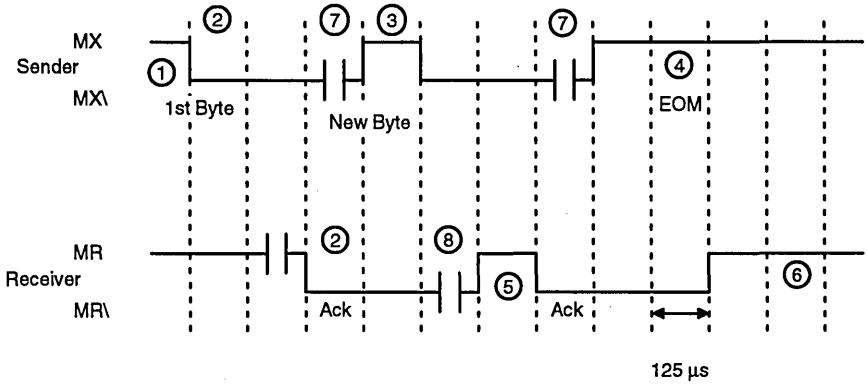


Figure 6. General Case of Multiple Byte Message Transfer

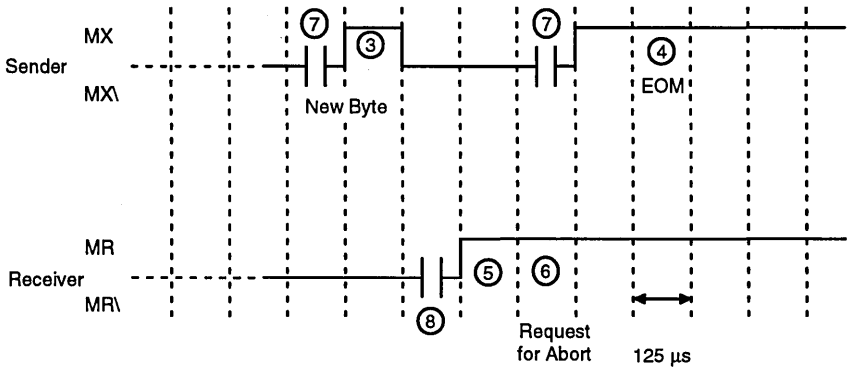


Figure 7. Abort Request on Multiple Byte Message Transfer

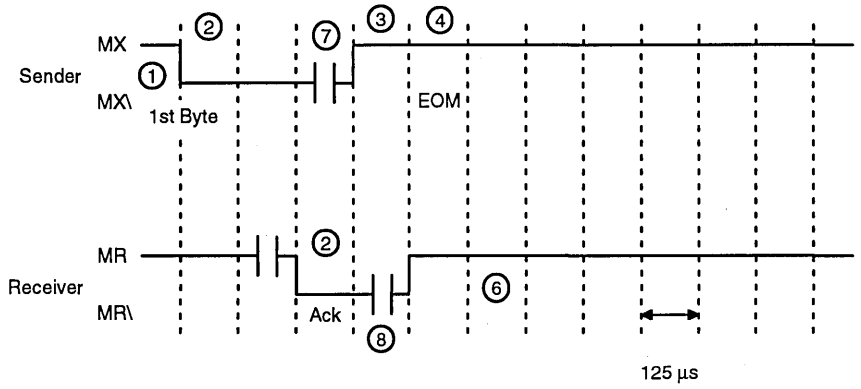


Figure 8. Single Byte Message Transfer

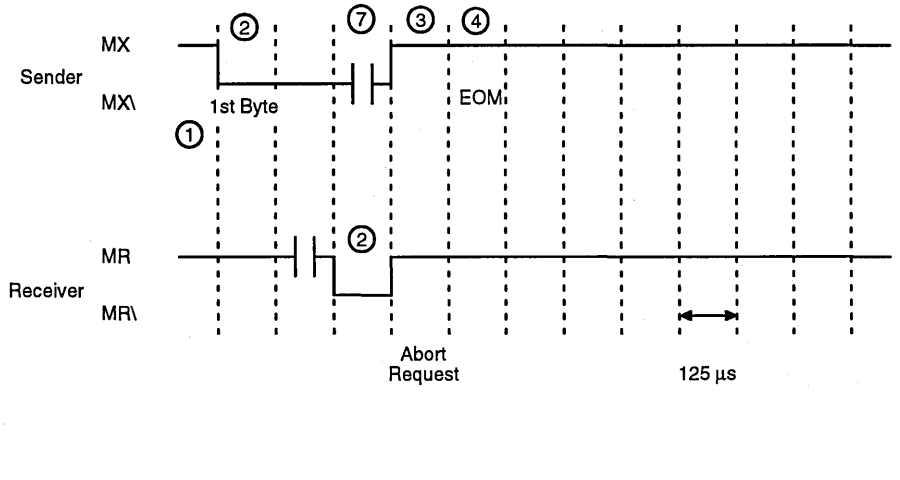
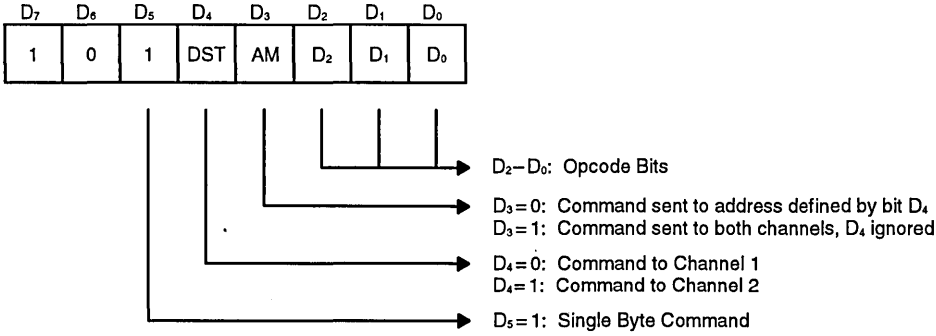


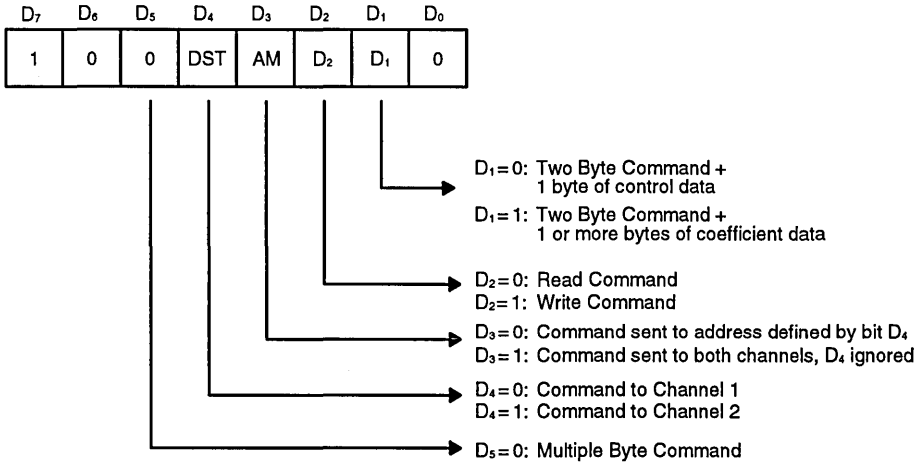
Figure 9. Abort Request on Single Byte Message Transfer

Monitor Channel Command Structure

The Monitor byte is the third byte in the 4-byte frame sent and received every 125 µs over the DU or DD pins. A Monitor command consists of one or more command bytes which may be followed with additional bytes of input data or may be followed by the DSLAC device sending out bytes of data over the DU pin. The first byte sent in a monitor channel message contains address, command, and read/write information conforming to the format in the diagrams below. Commands #25 through #40 are used to program the internal filters of the DSLAC device. Please refer to the Am79C02/3(A) DSLAC Preliminary Data Sheet for a complete description of the filter transfer functions and the coefficient structure.



12764A–011



12764A–012

Summary of Monitor Channel Commands

#	Byte 1	Byte 2	
1	101AB000		Inactivate (Standby mode)
2	101AB001		Reset
3	101AB010		No Operation
4	101AB011		Reset to Normal Conditions
5	101AB100		Activate
6	101AB110		MCLK = 2.048 MHz
7	101AB111		MCLK = 4.096 MHz
8	100A0000	00000000	Read Channel ID Information
9	100AB100	00000001	Write AISN & Analog Gains
10	100A0000	00000001	Read AISN & Analog Gains
11	100AB100	00000011	Write SLIC Input/Output Direction
12	100A0000	00000011	Read SLIC Input/Output Direction and Power Status
13	100A0000	00000100	Read SLIC Input/Output Registers
14	100AB100	00000101	Write Operating Functions
15	100A0000	00000101	Read Operating Functions
16	100AB100	00000110	AMD Internal Use Only
17	100A0000	00000110	AMD Internal Use Only
18	100AB100	00000111	Write Operating Conditions
19	100A0000	00000111	Read Operating Conditions
20	100A0000	00001000	Read Revision Code Number
21	100AB100	00001001	Write Ground-Key Sampling Interval
22	100A0000	00001001	Read Ground-Key Sampling Interval
23	100AB100	00001010	Write SLIC Upstream Input Debounce Time
24	100A0000	00001010	Read SLIC Upstream Input Debounce Time
25	100AB110	00000000	Write GX-Filter Coefficients
26	100A0010	00000000	Read GX-Filter Coefficients
27	100AB110	00000001	Write GR-Filter Coefficients
28	100A0010	00000001	Read GR-Filter Coefficients
29	100AB110	00000010	Write Z-Filter Coefficients
30	100A0010	00000010	Read Z-Filter Coefficients
31	100AB110	00000011	Write B-Filter Coefficients
32	100A0010	00000011	Read B-Filter Coefficients
33	100AB110	00000100	Write X-Filter Coefficients
34	100A0010	00000100	Read X-Filter Coefficients
35	100AB110	00000101	Write R-Filter Coefficients
36	100A0010	00000101	Read R-Filter Coefficients
37	100AB110	00000110	Write Echo Path Gain
38	100A0010	00000110	Read Echo Path Gain
39	100AB110	00000111	Write Error Level Threshold
40	100A0010	00000111	Read Error Level Threshold

A is referred to as DST in the following section.

A: 0 = Destination is Channel 1
1 = Destination is Channel 2

B is referred to as AM in the following section.

B: 0 = Command to channel defined by A bit
1 = Command to both channels, A bit ignored

DETAILED MONITOR COMMAND DEFINITIONS

Inactivate (Standby mode)

	MSB							LSB
Format:	1	0	1	DST	AM	0	0	0

Bit Name	Description
	During Inactive mode (of one or both channels), none of the programmed information is changed and the analog output is set to 0 V.

Reset

	MSB							LSB
Format:	1	0	1	DST	AM	0	0	1

Bit Name	Description
	The Reset state of the device is: a. A-law is selected. b. B, X, R, and Z filters are disabled and AISN gain is zero. c. Transmit (GX and AX) and Receive (GR and AR) gains are set to unity. d. SLIC Input/Output is set to the Read mode. e. Normal conditions are selected (see Command 4). f. The Adaptive mode and Error Level Threshold are reset. g. The SLIC interface is set to the non-Multiplexed mode. h. Both channels are placed in the Inactive (Standby) mode.

Reset to Normal Conditions

	MSB							LSB
Format:	1	0	1	DST	AM	0	1	1

Bit Name	Description
	Normal conditions are: a. 6 dB loss in receive path not inserted. b. Receive path not cut off. c. High-pass filter enabled. d. Test modes are turned off.

Activate (Operational Mode)

	MSB							LSB
Format:	1	0	1	DST	AM	1	0	0

Bit Name	Description
	Valid IOM 2 data is not transmitted until after the second FSC pulse is received following the execution of the Activate command.

Set MCLK to 2.048 MHz

	MSB							LSB
Format:	1	0	1	DST	AM	1	1	0

Set MCLK to 4.096 MHz

	MSB							LSB
Format:	1	0	1	DST	AM	1	1	1

Read Channel Identification Information

Command

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	0	0

Output Data

	1	0	0	SRC	0	C	C	C
	T	T	L	L	L	L	L	L

Bit Name	Description
SRC	Source 0 = Source is Channel 1. 1 = Source is Channel 2.
C	Configuration This field reflects the state of the configuration inputs.
T	Device Type These 2 bits always have a value of 10.
L	Design Level This 6-bit field is used to differentiate between different implementations of the same device type. The IOM 2 DSLAC device is assigned the number 000100.

Write AISN and Analog Gains

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	0	0	1

Input Data

—	AX	AR	A	B	C	D	E

Bit Name	Description
AX	Transmit Analog Gain AX = 0 0 dB gain AX = 1 6 dB gain
AR	Receive Analog Loss AR = 0 0 dB loss AR = 1 6 dB loss
A, B, C, D, E	AISN coefficients The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in increments of 0.0625. The gain coefficient is encoded and decoded using the following equation: $h_{AISN} = 0.0625\ ((A2^4 + B2^3 + C2^2 + D2^1 + E2^0) - 16)$ where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = 10000 implements a special digital loop-back mode and a value of ABCDE = 00000 indicates a gain of 0 (cut off).

Read AISN and Analog Gains

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	0	1

Output Data

—	AX	AR	A	B	C	D	E

Write SLIC Input/Output Direction

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	0	1	1

Input Data

	—	—	—	A	B	—	—	—

Bit Name	Description
	Pins $C5_1/IN_5$, $C5_2/IN_2$, $C4_1/IN_6$, and $C4_2/IN_3$ are set to Input or Output modes individually. The Input mode is set when the appropriate data bit is set to 0, and the Output mode is set when the data bit is set to 1. Data bit A sets pins $C5_1/IN_5$ or $C5_2/IN_2$ Data bit B set pins $C4_1/IN_6$, or $C4_2/IN_3$

Read SLIC Input/Output Direction and Power Status

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	1	1

Output Data

	PI	CS	—	A	B	—	—	—

Bit Name	Description
PI	Power Interrupt Bit PI = 0 There has not been a power interruption since the last software reset command. PI = 1 A power interruption has been previously detected requiring the DSLAC device to be completely reprogrammed. This bit is cleared by issuing a software reset command. THE DSLAC DEVICE CANNOT BE ACTIVATED UNTIL THIS BIT IS CLEAR.
CS	Channel Status Bit CS = 0 The status of the channel is inactive (Standby mode). CS = 1 The status of the channel is active (Operational mode).

Read SLIC Input/Output Registers

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	1	0	0

Output Data

—	—	DET	C5	C4	C3	C2	C1

Bit Name	Description
C5	Refers to $C5_1$ or $C5_2$ if they are used as outputs. Refers to IN_5 or IN_2 if they are used as inputs.
C4	Refers to $C4_1$ or $C4_2$ if they are used as outputs. Refers to IN_6 or IN_3 if they are used as inputs.

Write Operating Functions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	1	0	1

Input Data

ABF	A/U	EGR	EGX	EX	ER	EZ	EB

Bit Name	Description
ABF	Adaptive B Filter ABF = 0 non-Adaptive mode ABF = 1 Adaptive mode
A/U	A-law/μ-law A/U = 0 A-law coding A/U = 1 μ-law coding
EGR	GR Filter EGR = 0 GR filter disabled EGR = 1 GR filter enabled
EGX	GX Filter EGX = 0 GX filter disabled EGX = 1 GX filter enabled
EX	X Filter EX = 0 X filter disabled EX = 1 X filter enabled

Write Operating Functions—(continued)

Bit Name	Description
ER	R Filter
	ER = 0 R filter disabled
	ER = 1 R filter enabled
EZ	Z Filter
	EZ = 0 Z filter disabled
	EZ = 1 Z filter enabled
EB	B Filter
	EB = 0 B filter disabled
	EB = 1 B filter enabled

Read Operating Functions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	1	0	1

Output Data

ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Write Operating Conditions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	1	1	1

Input Data

—	CRP	HPF	RG	ALB	DLB	—	—

Bit Name	Description
CRP	Cutoff Receive Path
	CRP = 0 Receive path connected
	CRP = 1 Receive path cutoff
HPF	High-Pass Filter
	HPF = 0 High-pass filter enabled
	HPF = 1 High-pass filter disabled
RG	Receive Path Gain
	RG = 0 6 dB loss not inserted
	RG = 1 6 dB loss inserted

Write Operating Conditions—(continued)

Bit Name	Description
ALB	Analog Loop-Back ALB = 0 Analog loop-back disabled ALB = 1 Analog loop-back enabled
DLB	Digital Loop-Back DLB = 0 Digital loop-back disabled DLB = 1 Digital loop-back enabled

Note: Analog and Digital loop-backs must not be programmed at the same time.

Read Operating Conditions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	1	1	1

Output Data

—	CRP	HPF	RG	ALB	DLB	—	—

Read Revision Code Number

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	1	0	0	0

Input Data

#	#	#	#	#	#	#	#

Bit Name	Description
DST	Don't care

Write Ground-Key Sampling Interval

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	0	0
0	0	0	0	1	0	0	1

Input Data

—	—	CHF*	MUX	Gk3	Gk2	Gk1	Gk0

Bit Name	Description
MUX	Multiplexed mode MUX = 0 non-Multiplexed mode MUX = 1 Multiplexed mode The device may be configured to operate in the Multiplexed mode (MUX) where the off-hook status and the ground-key status are multiplexed onto the same line. Note that there is only one Ground-Key Sampling Interval register and one MUX bit per IOM 2 DSLAC device (not per channel). Thus, the DST and the AM fields are not decoded and a command to either channel will write into the Ground-Key register and the MUX bit.
Gk3–Gk0	Sampling Interval 1 to 15 ms in 1 ms steps. If the Gk3–Gk0 field is set to 0000 there is no debounce performed. If, additionally, the MUX bit is set to a 0 or if the Gk3–Gk0 field is set to 0000, the $C3_I/E_1$ output is controlled by writing a 0 or a 1 into the output latch via the C/I downstream byte.

Read Ground-Key Sampling Interval

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	0	0
0	0	0	0	1	0	0	1

Output Data

—	—	CHF*	MUX	Gk3	Gk2	Gk1	Gk0

*CHF— Chopper Clock Frequency (this bit sets the chopper clock frequency when the IOM 2 DSLAC device is operating in multiplexed mode).
CHF = 0 256 kHz (default)
CHF = 1 273 kHz

Write SLIC Detect Inputs Debounce Time

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	0	0
0	0	0	0	1	0	1	0

Input Data

—	—	—	—	Db3	Db2	Db1	Db0

Bit Name	Description
Db3–Db0	Debounce Interval Sets the debounce time from 0 to 15 ms in steps of 1 ms. This command sets the debounce interval for the input signals at $\overline{DET}_1$ and $\overline{DET}_2$. Note that there is only one Detect Input Debounce register per IOM 2 DSLAC device (not per channel). Thus, the DST and the AM fields are unused and a command to either channel will write into the Debounce register. If the Db3–Db0 field is set to 0000, there is no debounce performed.

Read SLIC Upstream Inputs Debounce Time

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	0	0
0	0	0	0	1	0	1	0

Output Data

—	—	—	—	Db3	Db2	Db1	Db0

Write GX-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	0	0

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Read GX-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	0	0

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Write GR-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	0	1

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Read GR-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	0	1

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Write Z-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	1	0

Input Data

C_{45}	m_{45}	C_{35}	m_{35}	Byte 1
C_{25}	m_{25}	C_{15}	m_{15}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4
C_{41}	m_{41}	C_{31}	m_{31}	Byte 5
C_{21}	m_{21}	C_{11}	m_{11}	Byte 6
C_{42}	m_{42}	C_{32}	m_{32}	Byte 7
C_{22}	m_{22}	C_{12}	m_{12}	Byte 8
C_{43}	m_{43}	C_{33}	m_{33}	Byte 9
C_{23}	m_{23}	C_{13}	m_{13}	Byte 10
C_{44}	m_{44}	C_{34}	m_{34}	Byte 11
C_{24}	m_{24}	C_{14}	m_{14}	Byte 12
C_{46}	m_{46}	C_{36}	m_{36}	Byte 13
C_{26}	m_{26}	C_{16}	m_{16}	Byte 14

Read Z-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	1	0

Output Data

C_{45}	m_{45}	C_{35}	m_{35}	Byte 1
C_{25}	m_{25}	C_{15}	m_{15}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4
C_{41}	m_{41}	C_{31}	m_{31}	Byte 5
C_{21}	m_{21}	C_{11}	m_{11}	Byte 6
C_{42}	m_{42}	C_{32}	m_{32}	Byte 7
C_{22}	m_{22}	C_{12}	m_{12}	Byte 8
C_{43}	m_{43}	C_{33}	m_{33}	Byte 9
C_{23}	m_{23}	C_{13}	m_{13}	Byte 10
C_{44}	m_{44}	C_{34}	m_{34}	Byte 11
C_{24}	m_{24}	C_{14}	m_{14}	Byte 12
C_{46}	m_{46}	C_{36}	m_{36}	Byte 13
C_{26}	m_{26}	C_{16}	m_{16}	Byte 14

Write B-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	1	1

Input Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{10}	m_{10}	C_{31}	m_{31}	Byte 2
C_{21}	m_{21}	C_{11}	m_{11}	Byte 3
C_{32}	m_{32}	C_{22}	m_{22}	Byte 4
C_{12}	m_{12}	C_{33}	m_{33}	Byte 5
C_{23}	m_{23}	C_{13}	m_{13}	Byte 6
C_{34}	m_{34}	C_{24}	m_{24}	Byte 7
C_{14}	m_{14}	C_{35}	m_{35}	Byte 8
C_{25}	m_{25}	C_{15}	m_{15}	Byte 9
C_{36}	m_{36}	C_{26}	m_{26}	Byte 10
C_{16}	m_{16}	C_{37}	m_{37}	Byte 11
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12
C_{48}	m_{48}	C_{38}	m_{38}	Byte 13
C_{28}	m_{28}	C_{18}	m_{18}	Byte 14

Read B-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	1	1

Output Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{10}	m_{10}	C_{31}	m_{31}	Byte 2
C_{21}	m_{21}	C_{11}	m_{11}	Byte 3
C_{32}	m_{32}	C_{22}	m_{22}	Byte 4
C_{12}	m_{12}	C_{33}	m_{33}	Byte 5
C_{23}	m_{23}	C_{13}	m_{13}	Byte 6
C_{34}	m_{34}	C_{24}	m_{24}	Byte 7
C_{14}	m_{14}	C_{35}	m_{35}	Byte 8
C_{25}	m_{25}	C_{15}	m_{15}	Byte 9
C_{36}	m_{36}	C_{26}	m_{26}	Byte 10
C_{16}	m_{16}	C_{37}	m_{37}	Byte 11
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12
C_{48}	m_{48}	C_{38}	m_{38}	Byte 13
C_{28}	m_{28}	C_{18}	m_{18}	Byte 14

Write X-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	0	0

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Read X-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	0	0

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Write R-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	0	1

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Read R-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	0	1

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Write Echo Path Gain

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	1	0

Input Data

C_{80}	m_{80}	C_{70}	m_{70}	Byte 1
C_{60}	m_{60}	C_{50}	m_{50}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4

Read Echo Path Gain

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	1	0

Output Data

C_{80}	m_{80}	C_{70}	m_{70}	Byte 1
C_{60}	m_{60}	C_{50}	m_{50}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4

Write Error Level Threshold

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	1	1

Input Data

C_{20}	m_{10}	C_{20}	m_{10}	Byte 1

Read Error Level Threshold

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	1	1

Output Data

C_{20}	m_{20}	C_{10}	m_{10}	Byte 1

SLIC INTERFACE

General Description

Each channel of the DSLAC device has I/O pins for interfacing with a SLIC or other line circuit device. The I/O pins on port 1 are labeled $C5_1/IN_5$, $C4_1/IN_6$, $C3_1/E_1$, $C2_1$, and $C1_1$. The I/O pins on port 2 are labeled $C5_2/IN_2$, $C4_2/IN_3$, $C3_2$/CHCLK, $C2_2$, and $C1_2$. One input-only pin for each channel ($\overline{DET}_1/IN_4$ for Channel 1 and $\overline{DET}_2/IN_1$ for Channel 2) is also available. When used with an Am795XX series SLIC, C_4, C_2, and C_1 can be used as outputs to set the Operating mode of the SLIC while C_5 would typically be used to control a test relay driver on the SLIC. $C3_1/E_1$ is used (in the Multiplexed mode) to control the function of the SLIC line monitor output, $\overline{DET}$. C_5 and C_4 of each channel can be programmed to be an input or an output via a Monitor channel command.

Data can be sent to any of the I/O pins configured as outputs via the six C/I bits of the downstream SC byte. All of the I/O pins configured as inputs may be read via a Monitor channel command. Additionally, three input signals from each channel are taken to form the six C/I bits of the upstream SC byte.

Ground-Key/Switch-Hook Detector Multiplexing

The $\overline{DET}$ input for each channel can be programmed to operate in the Multiplexed mode to interface with the Am795XX series SLIC devices. In this mode, the interpretation of the signal on the $\overline{DET}$ input is controlled by the $C3_1/E_1$ output. When E_1 is Low, $\overline{DET}$ is interpreted as switch-hook detect. When E_1 is High, $\overline{DET}$ is interpreted as ground-key detect. Input debouncing may be selected for both the switch-hook and ground-key functions. Note that in the Multiplexed mode, the ground- key detect status and not the $C5_1/IN_5$ and the $C5_2/IN_2$ inputs are part of the upstream SC byte.

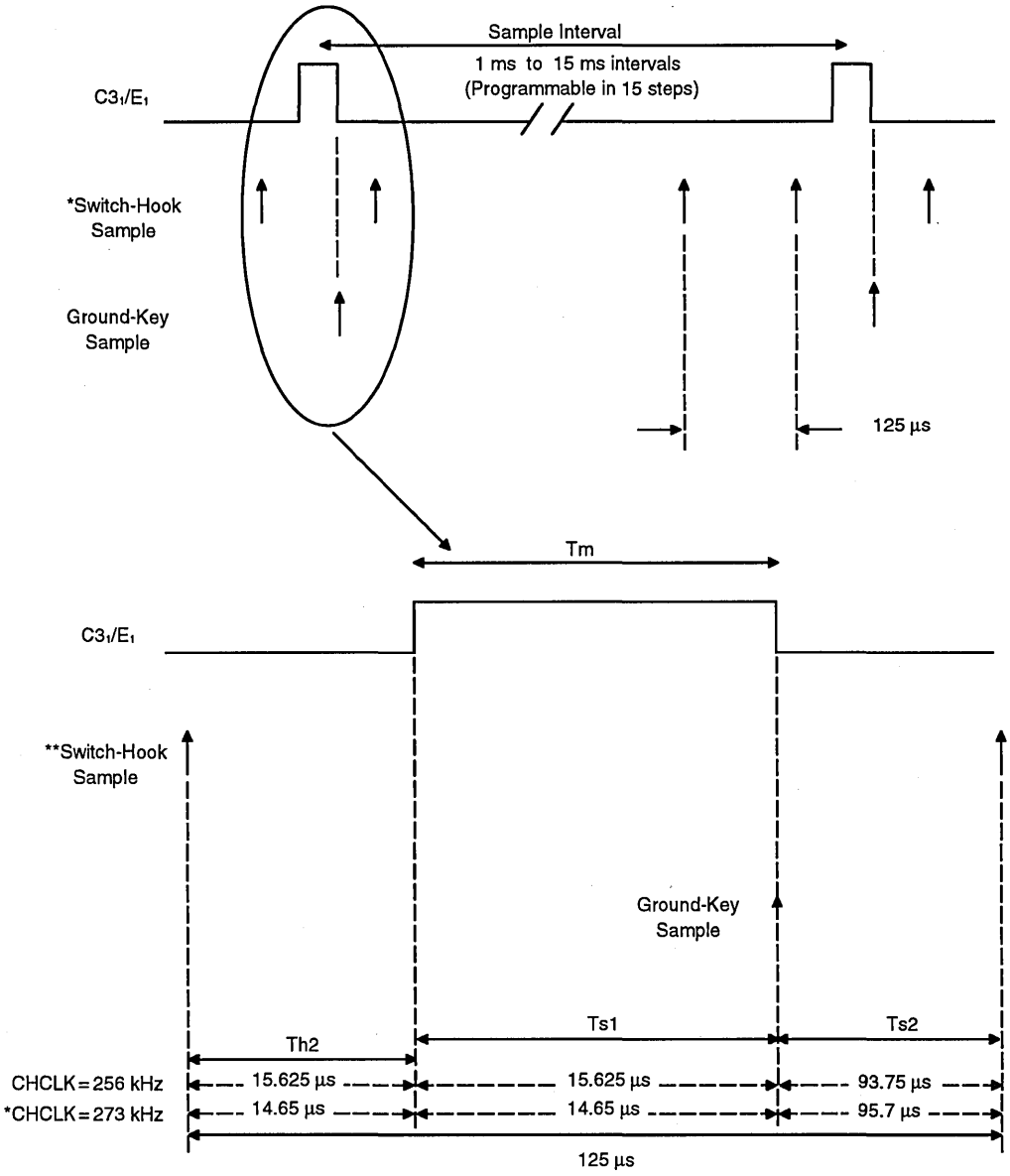
The state of E_1 can be controlled directly via a Monitor channel command or by the internal ground-key (Gk) timer which allows it to go High for approximately 16 µs every 1 to 15 ms. In this way, the DSLAC device can automatically de-multiplex the switch-hook and ground-key detector. Figure 10 shows the details of ground-key/switch-hook multiplexer timing.

Input Debouncing for Switch-Hook and Ground-Key Detect Inputs

There are two input debounce circuits associated with each channel of the DSLAC device. The first is used to debounce the $\overline{DET}$ input. The circuitry requires the signal on the $\overline{DET}$ input to be stable for two of the debounce intervals defined by the state of the Db timer (1 to 15 ms set by monitor command #23) in order for the upstream C/I byte to reflect the change.

A second debounce circuit per channel is available which would typically be used for the ground-key input. The input to this debounce circuit can come from $C5_1/IN_5$ and $C5_2/IN_2$ (in the non-Multiplexed mode), or the $\overline{DET}_1$ and $\overline{DET}_2$ inputs (in the Multiplexed mode). This circuit operates as a duty-cycle detector and consists of an up/down counter which can range between 0 and 6. The counter is clocked by the Gk timer which is set by monitor command #21 to a value between 1 to 15 ms. When the sampled value of the ground-key input is High, the counter is incremented. When the sampled value is a Low, the counter is decremented. If the counter increments to its maximum value of 6, it sets a latch whose output is the corresponding upstream C/I bit. If the counter decrements to its minimum value of 0, the latch is cleared. The following truth table shows the functioning of the ground key debounce circuit at every Gk clock.

Ground-Key Input	Current State	Next State	Action On C/I Bit Latch
0	State 0	State 0	Force Low
0	State 1	State 0	Force Low
0	State 2	State 1	No change
0	State 3	State 2	No change
0	State 4	State 3	No change
0	State 5	State 4	No change
0	State 6	State 5	No change
1	State 0	State 1	No change
1	State 1	State 2	No change
1	State 2	State 3	No change
1	State 3	State 4	No change
1	State 4	State 5	No change
1	State 5	State 6	Force High
1	State 6	State 6	Force High



*Programmed through CHF bit in Ground-Key Sampling Internal Register.
**Switch-hook samples occur at the beginning of selected time slot.

12764A–013

Figure 10. Switch-Hook/Ground-Key Multiplex Timing

The following table describes the various operating modes depending on the state of the MUX bit and the Ground Key (Gk) and the Debounce (Db) timers. A diagram of the SLIC I/O architecture is shown in Figure 11.

MUX	Gk3–Gk0	Db3–Db0	Operating Mode
0	0000	0000	1. **Non-Multiplexed mode.** The $\overline{DET_1}$ input is sampled every cycle and appears on C/I bit 4. The $\overline{DET_2}$ input is sampled every cycle and appears on C/I bit 1. Since the Db3–Db0 field is set to all 0s, there is no input debouncing. The $C5_1/IN_5$ input is sampled every frame and appears on C/I bit 5. The $C5_2/IN_2$ input is sampled every frame and appears on C/I bit 2. Since the Gk3–Gk0 field is set to all 0s, there is no input debouncing on C/I bit 5 or C/I bit 2.
0	1–15	1–15	2. **Same as 1**, except the $\overline{DET}$ inputs must be stable for two of the clock cycles defined by the state of the Db timer (1 to 15 ms) for the upstream C/I byte to reflect the change. The $C5_1/IN_5$ and the $C5_2/IN_2$ inputs are passed through the ground-key debounce circuit at a clock rate defined by the state of the Gk timer (1 to 15 ms).
1	1–15	0–15	3. **Multiplexed mode.** The $C3_1/E_1$ output will pulse High for one frame at a rate set by the Gk timer (1 to 15 ms). Thus, the state of the ground-key detector will be sampled at the Gk rate and passed to the ground-key debounce circuit. The ground-key status bits, C/I bit 2 and C/I bit 5, will reflect the output of the debounce circuit. If the Db3–Db0 field is set to 0000, C/I bit 1 and C/I bit 4 will be updated every frame except when the ground-key is being sampled. Otherwise, the switch-hook detect is sampled at the Db-clock rate and C/I bit 1 and C/I bit 4 will be updated when the sampled value has been stable for 2 Db-clock cycles.
1	0000	0–15	4. **Same as 3**, except the $C3_1/E_1$ pin is controlled by the downstream C/I channel and not by the Gk timer. Thus, the multiplexer can be manually set to interpret the $\overline{DET}$ input as either switch-hook status or ground-key status. When the E_1 signal is Low (selecting switch-hook status), C/I bits 5 and 2 (the ground-key detect bits) will not change states. Conversely, when the E_1 signal is High, C/I bits 4 and 1 will not change states.

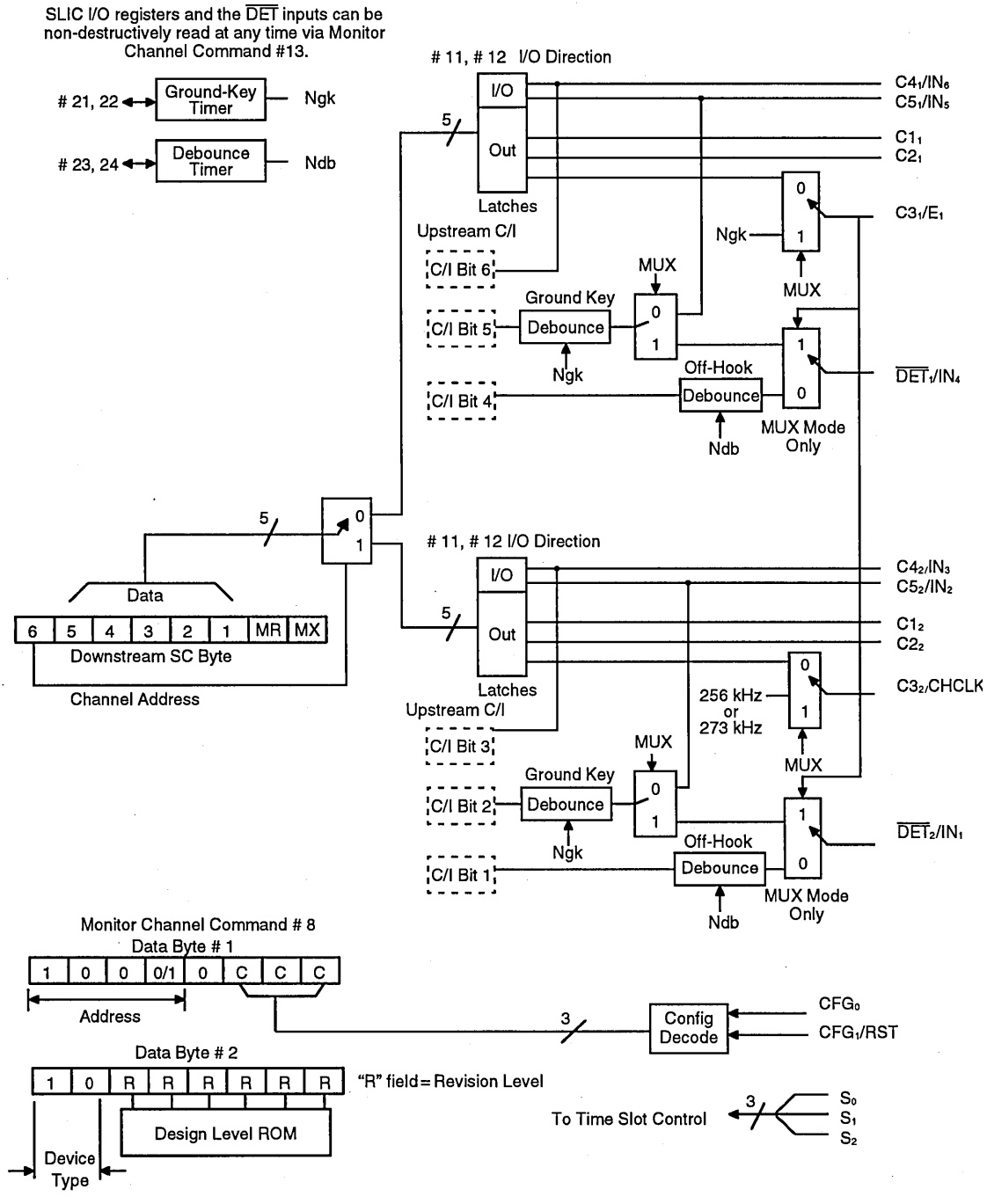


Figure 11. SLIC I/O Architecture

CONFIGURATION INPUTS

A method of identifying the configuration of the line circuit in which the DSLAC device is used is provided by strapping configuration inputs CFG_0 and CFG_1/RST. There are six possible configuration states which can be set via these two inputs. This data is sent upstream over the Monitor channel using command #8. The CFG_0 and CFG_1/RST inputs are decoded in the following table. A possible circuit for the CFG_1/RST pin is shown in Figure 12.

CFG_1	CFG_0	Configuration Number
+5 V	X	Hardware Reset
GND	–5 V	000
GND	GND	001
GND	+5 V	010
–5 V	–5 V	011
–5 V	GND	100
–5 V	+5 V	101

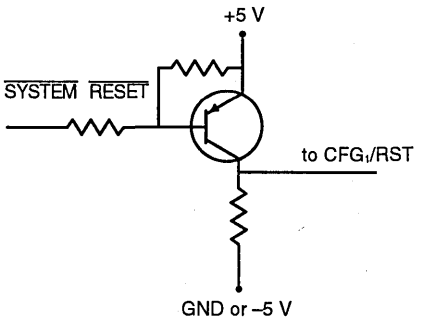


Figure 12. Circuit Schematic for the CFG_1, RST Input

TIME SLOT ASSIGNMENT INPUTS

In the time slot control block (shown in Figure 13), the Frame Sync (FSC) pulse identifies the beginning of a Transmit frame and all IOM 2 time slots are referenced to it. The time slot number is read from the external time slot identification pins, S_2–S_0. The table below shows the decoding on the time slot assignment inputs.

S_2	S_1	S_0	Time Slot Number	Byte number
0	0	0	0	0–3
0	0	1	1	4–7
0	1	0	2	8–11
0	1	1	3	12–15
1	0	0	4	16–19
1	0	1	5	20–23
1	1	0	6	24–27
1	1	1	7	28–31

The time slot number information is sent to the Transmit multiplexer where the code is shifted out during the appropriate time slot. From one to eight IOM 2 time slots per frame are allowed. The bit rate must be at least 256K times the number of IOM 2 time slots to be compatible with the number of time slots used. For example, since the DCL clock is twice the bit rate, DCL is at least 512 kHz for one time slot and 4.096 MHz for the full eight time slots.

The DSLAC device is capable of operation at a bit rate up to 4096 kb/s (DCL = 8.192 MHz). If the clock frequency exceeds the minimum for the given number of time slots on the IOM 2 line, there will be some time slots or surplus bits at the end of each frame which are ignored.

The receive side uses the same time slot control block information to de-multiplex the incoming IOM 2 data stream and load each byte into the input register. The input register feeds these bytes into the A-/μ-law expander for further signal processing.

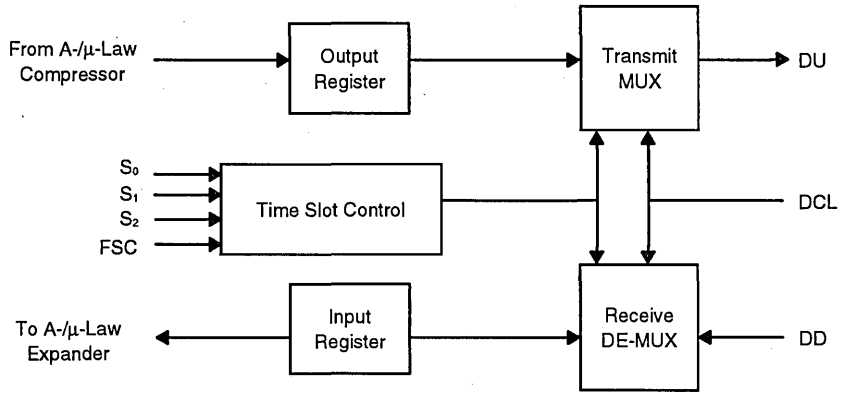


Figure 13. Time Slot Control and IOM 2 Interface

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... $-60°C \le T_A \le +125°C$
Ambient Temperature, under Bias ..... $-40°C \le T_A \le 85°C$
Ambient Relative Humidity (non-condensing) ..... 5 to 100%
V_{CCA} with respect to AGND ..... −0.4 V to +7.0 V
V_{CC} with respect to DGND ..... −0.4 V to +7.0 V
V_{EE1} with respect to AGND ..... +0.4 V to −7.0 V
V_{EE2} with respect to AGND ..... +0.4 V to −7.0 V
V_{IN} with respect to V_{CCA} (V_{EE} = −5 V) ..... +0.4 V to −10.0 V
V_{IN} with respect to V_{EE} (V_{CCA} = +5 V) ..... −0.4 V to +10.0 V
Any other pin with respect to DGND ... −0.4 V to V_{CC}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Analog Supply V_{CCA} ..... +5.0 V ±5%
Digital Supply V_{CC} ..... +5.0 V ±5%
Analog Supply V_{EE1}, V_{EE2} ..... −5.0 V ±5%
DGND ..... 0 V
AGND ..... DGND ±50 mV
Ambient Temperature ..... $0°C \le T_A \le +70°C$
Ambient Relative Humidity ..... 15% to 85%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DISTINCTIVE CHARACTERISTICS

Symbol	Parameter		Preliminary Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
I_{IL}	Input Leakage Current				±10	µA
V_{OL}	Output Low Voltage (I_{OL} = −2 mA)				0.4	V
V_{OH}	Output High Voltage (I_{OH} = 400 µA)		2.4			V
I_{OL}	Output Leakage Current (Hi-Z state)				±10	µA
V_{IR}	Analog Input Voltage Range (AX = 0 dB) (AX = 6.02 dB)				±3.24 ±1.62	V V
V_{IOS}	Offset Voltage allowed on V_{IN}				±160	mV
I_{IL} (V_{IN})	Input Leakage Current on V_{IN}				±10	µA
Z_{OUT}	V_{OUT} Output Impedance			1	10	ohms
I_{OUT}	V_{OUT} Output Current (f < 3400 Hz) (Note 1)				±6.3	mA
V_{OR}	V_{OUT} Voltage Range (AR = 0 dB) (AR = 6.02 dB)				±3.24 ±1.62	V V
V_{OOS}	V_{OUT} Offset Voltage (AISN off)				±40	mV
V_{OOSA}	V_{OUT} Offset Voltage (AISN on)				±80	mV
LIN_{AISN}	Linearity of AISN Circuitry (Input = 0 dBm0)				±1/4	LSB
PD	Power Dissipation (Note 2) (MCLK, PCLK = 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		180 120 10	240 160 19	mW mW mW
PD	Power Dissipation (Note 2) (MCLK, PCLK > 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		190 130 10	270 175 19	mW mW mW
I_{CC}	Total +5-V Current (Note 2)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		24.0 18.0 2.5		mA mA mA
I_{EE}	Total −5-V Current (Note 2)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		10.0 5.0 0.05		mA mA mA
C_I	Input Capacitance (Digital)			15		pF
C_O	Output Capacitance (Digital)			15		pF
C_{DU}	Output Load Capacitance (DU pin only)				150	pF

Notes: 1. When the DSLAC device is in the Power Down mode, the analog output will present a 0-V output level through a ≈3K resistor.

2. V_{OUT1} and V_{OUT2} have no load.

3. Power Dissipation in the inactive mode is measured with all digital inputs at $V_{ih} = V_{CC}$ and $V_{il} = V_{SS}$ and with no load connected to V_{OUT1} or V_{OUT2}.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V ±5%, AGND = DGND = 0 V, V_{EE} = –5 V ±5%. C_{DU} = 150 pF (Note 2)

IOM 2 Interface

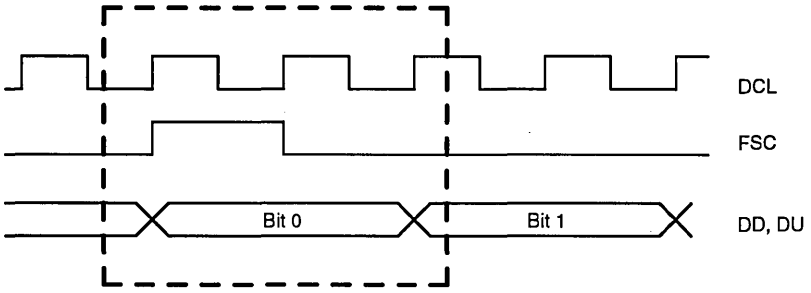
Symbol	Signal	Parameter	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t_r, t_f	DCL[1]	Rise/Fall Time (Note 1)			60	ns
t_{DCL}	DCL	Period	110			ns
t_{wH}, t_{wL}	DCL	Pulse Width	53			ns
t_r, t_f	FSC	Rise/Fall Time			60	ns
t_{sF}	FSC	Setup Time	70			ns
t_{hF}	FSC	Hold Time	50			ns
t_{wFH}	FSC	High Pulse Width	130			ns
t_{dDC}	DU[2]	Delay from DCL edge			100	ns
t_{dDF}	DU	Delay from FSC edge			150	ns
t_{sD}	DD	Data Setup	t_{WH} + 20			ns
t_{hD}	DD	Hold Setup	50			ns

MCLK, for 2.048 MHz + 100 ppm or 4.096 MHz + 100 ppm

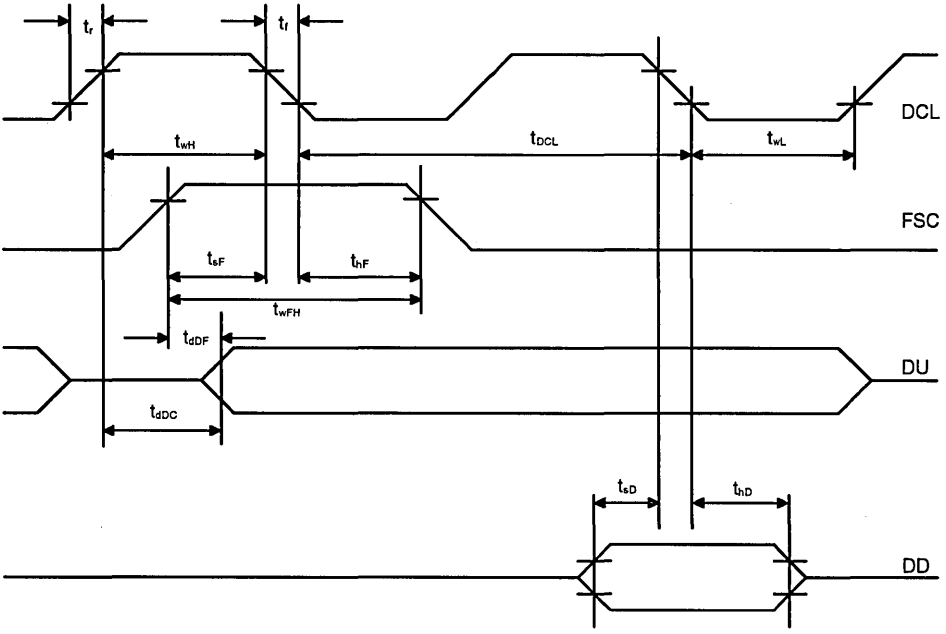
Symbol	Signal	Parameter	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t_{MCR}, t_{MCF}	MCLK	Rise/Fall Time			10	ns
t_{MCY}	MCLK	Period, 2.048 MHz Peroid, 4.096 MHz	488.23 244.11	488.28 244.14	488.33 244.17	ns ns
t_{MCH}, t_{MCL}	MCLK	High/Low Pulse Width	80			ns

Notes: 1. The IOM 2 clock may be stopped in the High or Low state without loss of information.
2. The drive capacity of the IOM 2 Interface allows eight DSLAC devices per linecard (16 subscriber lines) without using external buffers.

IOM 2 Switching Characteristics



Detail A



Detail A

12764A-017

DSLAC EXTENDED TEMPERATURE SUPPLEMENT

The DSLAC device has been characterized over the –40°C to +85°C temperature range to establish its suitability for applications such as Remote Concentrators, Digital Loop Carriers, and other applications that may be subjected to temperature extremes. All versions of the DSLAC device are fully functional over this extended temperature range and are recommended for such applications.

Characterization indicates that certain parameters of a small percentage of DSLAC devices tested for operation between 0°C and 70°C may vary beyond data sheet limits in the extended temperature ranges. This document identifies those parameters and their expected limits in the temperature ranges beyond 0°C to 70°C.

The specifications in this supplement have been determined through characterization to apply to AMD's standard commercial grade product. If specifications over the –40°C to +85°C range or another extended temperature range must be guaranteed and tested at the temperature extremes, the customer is asked to contact an AMD representative for more information.

DSLAC Family Extended Temperature Information

DSLAC Electrical Specifications		Commercial Specification 0°C to +70°C	Extended Specification –40°C to +85°C	Unit
Absolute Gain (See Note)		+/– 0.2	+/– 0.35	dB
Receiver Gain Tracking (Noise)	–10 dBm0 to –40 dBm0	+/– 0.25	+/– 0.4	dB
Receiver Gain Tracking (Noise)	–40 dBm0 to –50 dBm0	+/– 0.35	+/– 0.55	dB
Receiver Gain Tracking (Noise)	–50 dBm0 to –55 dBm0	+/– 0.45	+/– 0.55	dB
Transmitter Gain Tracking (Noise)	–10 dBm0 to –40 dBm0	+/– 0.25	+/– 0.3	dB
Transmitter Gain Tracking (Noise)	–40 dBm0 to –50 dBm0	+/– 0.35	+/– 0.4	dB
Receiver Signal/Distortion (Noise)	–27 dBm0	36	35	dB
Receiver Signal/Distortion (Noise)	–34 dBm0	34.3	33.3	dB

Note: Absolute Gain stability is specified as +/– 0.2 dB at 25°C, but +/– 0.25 dB over the commercial temperature range (0°C to +70°C). This should be relaxed to +/– 0.35 dB over the extended temperature range (–40°C to +85°C).

Chapter 3

ISDN Products

CHAPTER 3
ISDN Products

INTRODUCTION TO ISDN PRODUCTS

The Am79C30A DSC device combines an S/T-interface transceiver, a D-channel data link controller, and an audio codec/filter into a single low-power CMOS device. It is the most highly integrated ISDN terminal device currently available that provides voice and data capability on a single chip.

The Am79C30A is the world's first ISDN terminal circuit that can be used to build ISDN telephones and terminals that conform to CCITT power specifications. This circuit, combined with EPROM, SRAM, a microcontroller, and a power controller, are all that is needed for a basic CCITT power-compliant telephone or terminal.

The Digital Subscriber Controller™ circuit interfaces directly to a telephone handset and drives the four-wire S/T Interface. The data-link controller supports the LAPD protocol defined for the 16 kb/s D Channel, and allows full compliance to the CCITT's recommendations for ISDN.

The Am79C30A supports both the active and low-power restricted conditions specified by the CCITT, and will allow incoming and outgoing calls to be made (including ringing) with only 380 mW available for the complete system.

FIFOs of 32 bytes for receive and 16 bytes for transmit further reduce the power requirements of the DSC circuit by allowing it to be used in conjunction with low-power, low-performance microprocessors. Clock frequencies automatically increase whenever the FIFO threshold is reached or when a new packet is received while a previous packet is still in the FIFO. This allows the microprocessor to run with a very slow clock when no D-channel activity is present.

Data may be transmitted on the D Channel (using LAPD) and/or either B Channel. Access to the B Channel is provided via the microprocessor port or a serial port. The serial port will interface directly to the Data Protocol Controller to provide packet handling for B-channel data. The circuit also supports the industry standard IOM-2 interchip interface in its peripheral port for simplified design with other ISDN circuits.

The Am79C30A is a highly programmable device; the audio processor has programmable filters allowing the designer to compensate for the characteristics of low-cost telephone handsets. A programmable second tone ringer provides increased volume levels and features such as incoming call alert while a voice conversation is in progress. Programmable gain on the microphone amplifier is provided at the analog input adjustable in 6-dB increments from 0 dB to +24 dB, eliminating the need for an external amplifier with electret microphones. Mute capability is also available allowing the microphone path to be enabled and disabled. The DSC device allows the EAR and Loud Speaker (LS) outputs to be simultaneously enabled, allowing the use of an external speaker together with a conventional handset for loud hearing applications. A digital loopback mode is available internally connecting the EAR output to the analog input, extending the user test capabilities.

PRELIMINARY

Am79C30A

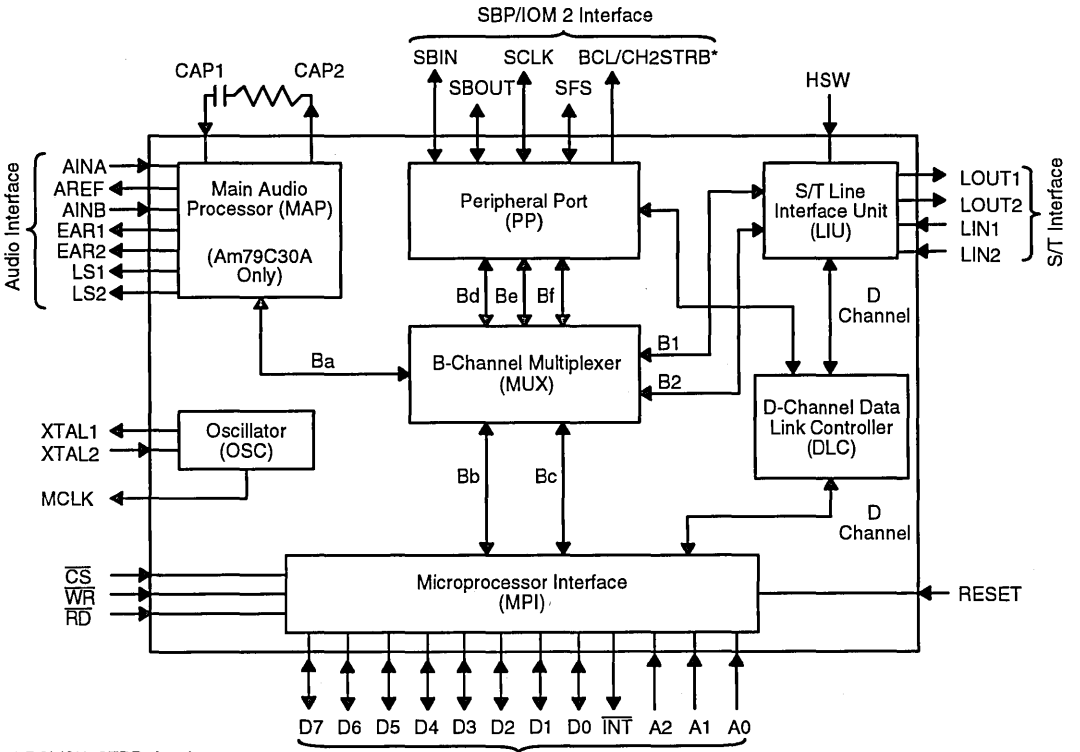
Digital Subscriber Controller™ (DSC™) Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Combines CCITT I.430 S/T-Interface Transceiver, D-Channel LAPD Processor, Audio Processor (DSC device only), and IOM 2 Interface in a single chip**
- **Special operating modes allow realization of CCITT I.430 power-compliant terminal equipment**
- **S- or T-Interface Transceiver**
  - —Level 1 Physical Layer Controller
  - —Supports point-to-point, short and extended passive bus configurations
  - —Provides multiframe support
- **Certified protocol software support available**
- **CMOS technology, TTL compatible**
- **D-channel processing capability**
  - —Flag generation/detection
  - —CRC generation/checking
  - —Zero insertion/deletion
  - —Four 2-byte address detectors
  - —32-byte receive and 16-byte transmit FIFOs

BLOCK DIAGRAM



* BCL/CH2STRB signal present only for PLCC package.

09893F-001

Publication #: 09893 Rev. F Amendment /0
Issue Date: June 1992

DISTINCTIVE CHARACTERISTICS (continued)

- **Audio processing capability (DSC circuit only)**
  - —Dual audio inputs
  - —Earpiece and loudspeaker drivers
  - —Codec/filter with A/μ selection
  - —Programmable gain and equalization filters
  - —Programmable sidetone level
  - —Programmable DTMF, single tone, progress tone, and ringer tone generation
  - —Programmable on-chip microphone amplifier
- **Pin and software compatible with the Am79C32A ISDN Data Controller (IDC™) Circuit. The Am79C32A is used in data-only applications**

GENERAL DESCRIPTION

The Am79C30A Digital Subscriber Controller (DSC) Circuit and Am79C32A ISDN Data Controller (IDC) Circuit, shown in the Block Diagram, allow the realization of highly-integrated Terminal Equipment for the ISDN. The Am79C30A/32A is fully compatible with the CCITT-I-series recommendations for the S and T reference points, ensuring that the user of the device may design TEs which conform to the international standards.

The Am79C30A/32A provides a 192-kb/s full duplex digital path over four wires between the TE located on the subscriber's premises and the NT or PABX linecard. All physical Layer functions and procedures are implemented in accordance with CCITT Recommendation I.430, including framing, synchronization, maintenance, and multiple terminal contention. Both point-to-point and point-to-multipoint configurations are supported.

The Am79C30A/32A processes the ISDN basic rate bit stream, which consists of B1 (64 kb/s), B2 (64 kb/s), and D (16 kb/s) Channels. The B Channels are routed to and from different sections of the Am79C30A/32A under software control. The D Channel is partially processed by the DSC/IDC circuit and is passed to the microprocessor for further processing.

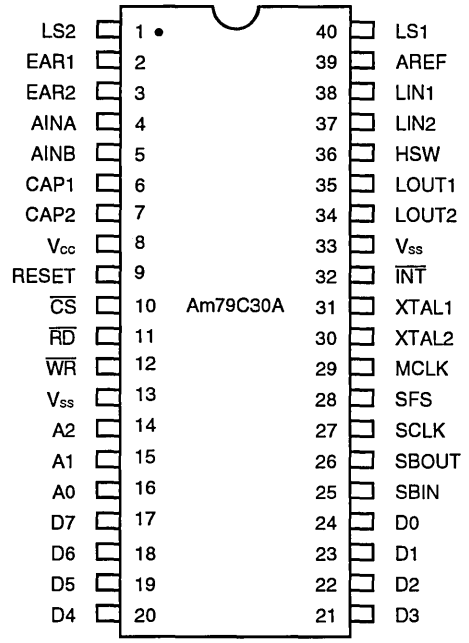
The Main Audio Processor (MAP) uses Digital Signal Processing (DSP) to implement a high performance codec/filter function. The MAP interface supports a loudspeaker, an earpiece, and two separate audio inputs. Programmable on-chip gain is provided to simplify use of low output level microphones. The user may alter frequency response and gain of the MAP receive and transmit paths. Tone generators are included to implement ringing, call progress, and DTMF signals.

A Peripheral Port (PP) is provided to allow the B Channels to be routed off-chip for processing by other peripherals. This port is configurable as either an industry-standard IOM 2 port, or as a serial bus port (SBP).

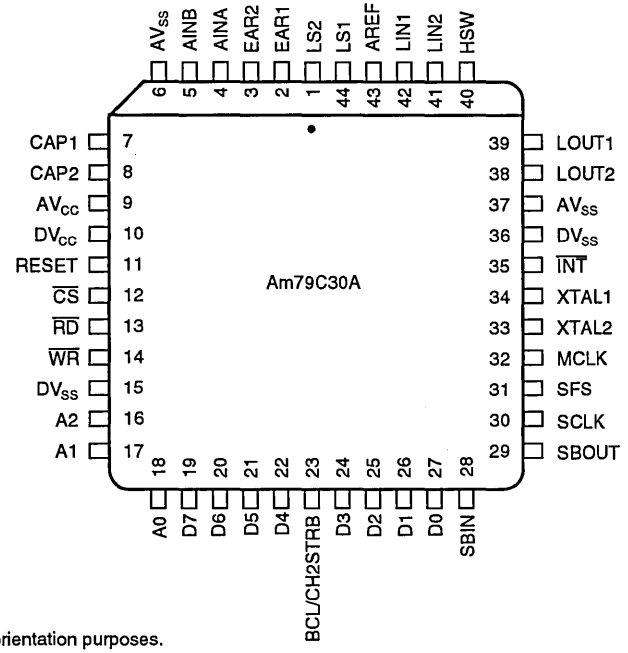
The TE design process is simplified by the availability of certified protocol software packages, which provide complete system solutions through OSI Layer 3.

CONNECTION DIAGRAMS
Top View

40-Pin DIP



44-Pin PLCC

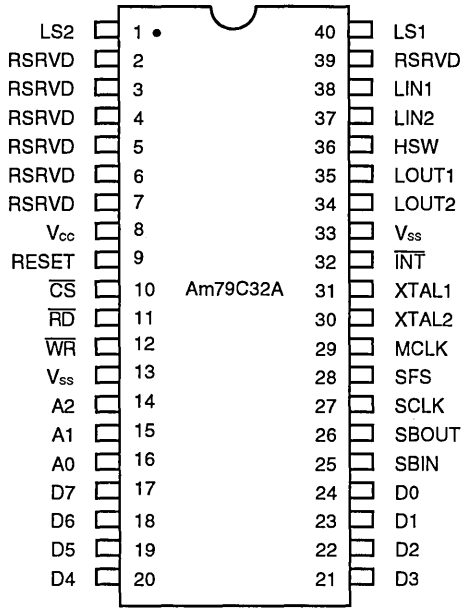


Note: Pin 1 is marked for orientation purposes.

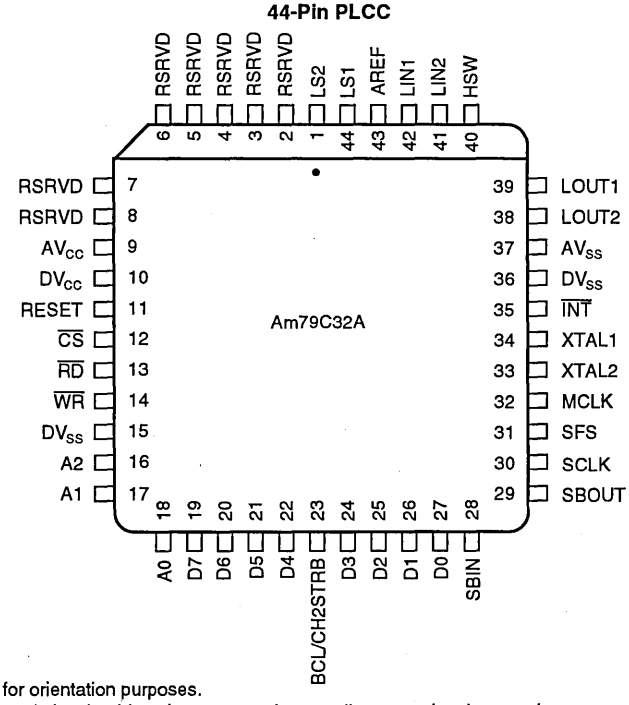
CONNECTION DIAGRAMS (continued)

Top View

40-Pin DIP



44-Pin PLCC

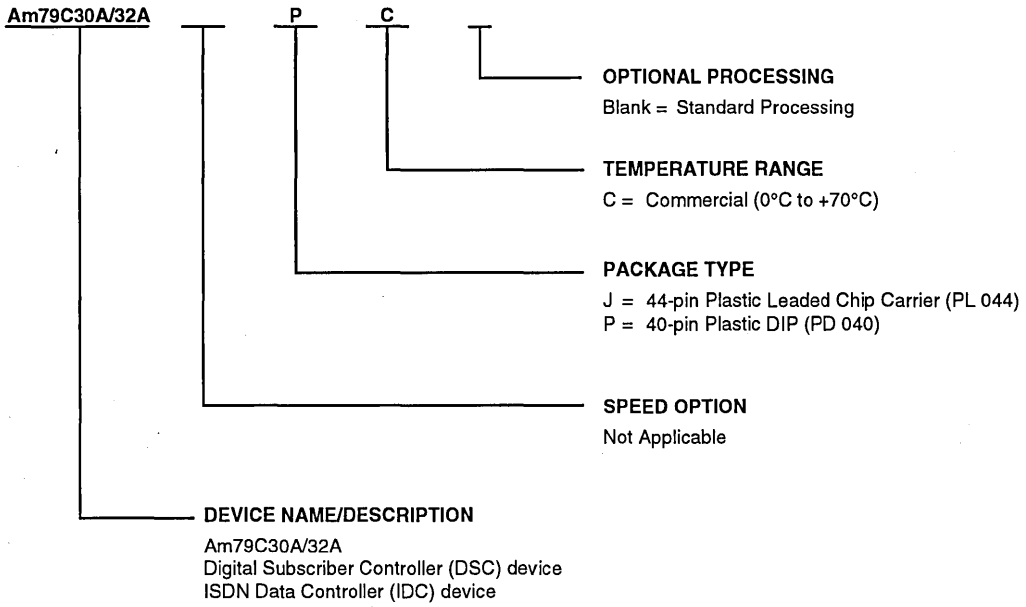


Notes: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C30A	PC, JC
AM79C32A	PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

PIN DESCRIPTION*

Line Interface Unit (LIU)

HSW
Hook-Switch (Input)

The HSW signal indicates if the hook-switch is on or off hook. This signal may be generated with a mechanical switch wired to ground with a pull-up resistor to V_{CC}. Any change in the HSW state causes an interrupt.

LIN1, LIN2
Subscriber Line Input (Differential Inputs)

The LIN1 and LIN2 inputs interface to the subscriber (S reference point) via an isolation transformer. LIN2 is the positive input; LIN1 is the negative input. These pins are not TTL compatible.

LOUT1, LOUT2
Subscriber Line Output (Differential Outputs)

The LOUT1 and LOUT2 line driver output signals interface to the subscriber line at the S reference point via an isolation transformer and resistors. LOUT2 is the positive S-interface driver (sources current during a High mark), and LOUT1 is the negative S-interface driver (sources current during Low mark). For multipoint applications, all TEs must maintain the same polarity on the S Interface. These pins are not TTL compatible.

Main Audio Processor (MAP)

All MAP pins are analog, and therefore are not TTL compatible.

AINA, AINB
Analog (Inputs)

These analog inputs allow for two separate analog (audio) inputs to the transmit path of the codec/filter. Input signals on either of these pins must be referenced to AREF.

AREF
Analog Reference (Output)

This is a nominal 2.4-V reference voltage output for biasing the analog inputs. When the MAP is disabled, this pin is high-impedance.

CAP1, CAP2
Capacitor/Resistor (CAP1, Input; CAP2, Output)

An external resistor and capacitor are connected in series between these pins. These components are needed for the integrator in the Analog-to-Digital Converter (ADC).

EAR1, EAR2
Earpiece Interface (Differential Outputs)

EAR1 and EAR2 are the outputs from the receive path of the codec/filter. These differential outputs can directly drive a minimum load of 540 ohms.

LS1, LS2
Loudspeaker Interface (Differential Outputs)

LS1 and LS2 are push-pull outputs which can directly drive a minimum load of 40 ohms.

Microprocessor Interface (MPI)

A2–A0
Address Line (Inputs)

A2, A1, and A0 signals select source and destination registers for read and write operations on the data bus.

$\overline{CS}$
Chip Select (Input)

$\overline{CS}$ must be Low to read or write to the Am79C30A/32A. Data transfer occurs over the bidirectional data lines (D7–D0).

D7–D0
Data Bus (Bidirectional with High Impedance State)

The eight bidirectional data bus lines are used to exchange information with the microprocessor. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). A High on the data bus line corresponds to a logic 1, and Low corresponds to a logic 0. These lines act as inputs when both $\overline{WR}$ and $\overline{CS}$ are active and as outputs when both $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive or both $\overline{RD}$ and $\overline{WR}$ are inactive, the D7–D0 pins are in a high-impedance state.

$\overline{INT}$
Interrupt (Output)

An active Low output on the $\overline{INT}$ pin informs the external microprocessor that the Am79C30A/32A needs interrupt service. $\overline{INT}$ is updated once every 125 µs. The $\overline{INT}$ pin remains active until the Interrupt Register (IR) is read or the Am79C30A/32A is reset.

RESET
Reset (Input)

Reset is an active High signal which causes the Am79C30A/32A to immediately terminate its present activity and initialize to the reset condition. When reset returns Low, the Am79C30A/32A enters the Idle Mode. The MCLK output remains active while RESET is held High.

* All signal levels are TTL compatible unless otherwise stated.

$\overline{RD}$
Read (Input)

The active Low read signal is conditioned by $\overline{CS}$ and indicates that internal information is to be transferred onto the data bus. A number of internal registers are user accessible. The contents of the accessed register are transferred onto the data bus after the High to Low transition of the $\overline{RD}$ input.

$\overline{WR}$
Write (Input)

The active Low write signal is conditioned by $\overline{CS}$ and indicates that external information on the data bus is to be transferred to an internal register. The contents of the data bus are loaded on the Low to High transition of the $\overline{WR}$ input.

Oscillator (OSC)

MCLK
Master Clock (Output)

The MCLK output is available for use as the system clock for the microprocessor. MCLK is derived from the 12.288-MHz crystal via a programmable divider in the Am79C30A/32A which provides the following MCLK output frequencies: 12.288, 6.144, 4.096, 3.072, 1.536, 0.768, and 0.384 MHz.

XTAL1, XTAL2
External Crystal (Output, Input)

XTAL1 and XTAL2 are connected to an external parallel resonant crystal for the on-chip oscillator. XTAL2 can also be connected to an external source instead of a crystal, in which case XTAL1 should be left disconnected. The frequency must be 12.288 MHz, ± 80 ppm.

Peripheral Port (PP)

SBIN
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP Mode, SBIN operates as an input for serial data. When the Peripheral Port is programmed to IOM 2 Mode, SBIN functions as the data input except in the special case of IOM 2 Slave Mode, when it becomes an open-drain output during sub-frame 0 or when deactivated.

SBOUT
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP Mode, SBOUT operates as an output for serial data. When the Peripheral Port is programmed to IOM 2 Mode, SBOUT functions as the data output except in the special case of IOM 2 Slave Mode when it becomes an input during sub-frame 0.

SCLK
Serial Data Clock (Input/Output)

When the PP is programmed to SBP Mode, SCLK outputs a 192-kHz data clock, which may be inverted under software control. When the PP is programmed to IOM 2 Master Mode, SCLK outputs a 1.536-MHz 2X data clock. In IOM 2 Slave Mode, SCLK functions as the clock input. The SCLK pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM 2 Master Mode.

SFS
Serial Frame Sync (Input/Output)

In SBP Mode, SFS outputs an 8-kHz frame synchronization signal. SFS is an output in IOM 2 Master Mode, and an input in IOM 2 Slave Mode. As an output, SFS is active for 8-bit periods. The SFS pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM 2 Master Mode. For SBP Mode, the active signal state is Low during Idle and 8 kHz in Active Data Only and Active Voice and Data Modes.

BCL/CH2STRB
Bit Clock/SBP Channel 2 Strobe
(Output, Three-state) (present only in PLCC package)

In SBP Mode, this pin provides a strobe during the 8-bit times of the second 64-kb/s data channel. In IOM 2 Master Mode, this pin provides a 768-kHz bit clock to aid in the connection of non-IOM 2 devices to the port. In IOM 2 Slave Mode, this pin is high-impedance.

Power Supply Pins

PLCC Packages

AV_{CC}	+5-V analog power supply, ±5% (PLCC only)
AV_{SS}	Analog ground (PLCC only)
DV_{SS}	Digital ground (PLCC only)
DV_{CC}	+5-V digital power supply, ±5% (PLCC only)

DIP Packages

V_{CC}	+5-V power supply, ±5% (DIP only)
V_{SS}	Ground (DIP only)

Note: For best performance, decoupling capacitors should be installed between V_{CC} and V_{SS} as close to the chip as possible. Do not use separate supplies for analog and digital power and ground connections.

OPERATIONAL DESCRIPTION

Overview of Power Modes

The minimization of power consumption is a key factor in the design of Terminal Equipment for the ISDN, and the DSC/IDC circuit employs two basic approaches to power management:

1. The power consumption of the DSC/IDC circuit itself is managed by using four basic power modes which allow unused functional blocks to be disabled. The INIT register may be programmed to select Active Voice and Data, Active Data Only, Idle, or Power-Down Mode, depending upon which DSC/IDC device resources are required at the time.
2. The power consumption of the controlling microprocessor system may be controlled by driving the processor clock with the DSC/IDC circuit MCLK output. A wide range of MCLK operating frequencies may be selected, and a special Clock Speed-up function is provided which increases the speed of MCLK upon the occurrence of a key event, without processor intervention. Control of MCLK frequency and Clock Speed-up is accomplished by programming the INIT and INIT2 registers, as described later.

Active Voice and Data Mode

In Active Voice and Data Mode all functional blocks of the DSC/IDC circuit are available. Device registers may be accessed through the MPI, the LIU and DLC are available, the OSC is running, the Peripheral Port is available, MUX connections may be made, the Secondary Tone Ringer may be activated, and the MAP is operational (DSC circuit only).

Active Data Only Mode

Active Data Only Mode is similar to Active Voice and Data Mode, except that the MAP (DSC circuit only) is disabled to reduce system power consumption. This increases the amount of power available for the Secondary Tone Ringer or microprocessor system during the phases of call setup and teardown, or during a data-only telephone call.

Idle Mode

Idle Mode is the RESET default mode of DSC/IDC circuit operation, and represents an operational state in which power consumption is reduced, yet the microprocessor system is operational to program DSC/IDC circuit registers or perform other required background tasks. Idle Mode may also be entered by appropriate programming of the INIT register.

In Idle Mode, the MCLK output is available to drive the microprocessor system, the MPI is available for programming of DSC/IDC registers, and the LIU is available to initiate or respond to S/T interface activity. The HSW hookswitch interrupt is also available in Idle Mode.

Idle Mode reduces DSC/IDC circuit power consumption by disabling the MUX, DLC, and MAP functional blocks. The Peripheral Port is also disabled, except that an IOM 2 activation request interrupt is possible, and the SFS and SCLK outputs may still be activated. The SFS and SCLK outputs are high-impedance upon RESET, but become active after any MUX connection is programmed. The DLC read-only registers are cleared when the DSC/IDC circuit enters the Idle Mode.

Power-Down Mode

Power-Down Mode consumes the least power of all the DSC/IDC power options, and differs from Idle Mode in that all clocks, including the XTAL oscillator, are stopped. Most functional blocks are disabled, except for those required to recognize key external events that will force the DSC/IDC circuit to return to Idle Mode.

The Power-Down Mode is not available unless the Power-Down Enable bit is set in the INIT2 register; see the INIT2 register description for further details.

Entering the Power-Down Mode

The Power-Down Mode is entered by appropriate programming of the INIT and INIT2 registers. Selection of the Power-Down Mode causes the DSC/IDC circuit to begin an internal countdown of at least 250 MCLK cycles after which the MCLK and XTAL1 outputs are both stopped and held High, and the XTAL2 input will be disregarded. The purpose of this countdown cycle is to allow the microprocessor time for housekeeping operations before its clock is stopped. If an interrupt causes the DSC $\overline{INT}$ pin to go Low during the countdown, the Power-Down Mode bits in the INIT register will be reset and the countdown will be canceled.

If the LIU is enabled and in any state other than F3 at the end of the countdown, MCLK is stopped but the oscillator continues to run. This allows the LIU to identify the incoming signal and either (1) generate an interrupt and force the DSC/IDC circuit to Idle Mode when activation is complete, or (2) move to the F3 state and stop the oscillator once the line goes idle.

Exiting the Power-Down Mode

The DSC/IDC circuit will exit the Power-Down Mode and enter the Idle Mode if any of the following events occur:

- The DSC/IDC circuit receives a hardware reset via the RESET pin.
- The $\overline{CS}$ and $\overline{WR}$ pins are both pulled Low at the same time, as would occur during a normal write operation from the microprocessor to the DSC circuit. No data will be transferred by this operation.
- The HSW hookswitch pin changes state, and the hookswitch interrupt is enabled.

- The LIU receiver is enabled, detects an incoming signal on the S/T Interface, and achieves activation as indicated by a transition to state F7. Both the $\overline{INT}$ pin and the F7 transition interrupt must be enabled for Power-Down Mode to be exited. If the LIU is enabled, it may restart the oscillator so that it can identify the activity on the interface. If the activity is determined to be noise, the LIU will stop the oscillator and continue to monitor the line without an interrupt or returning to Idle Mode.
- The IOM 2 Interface is enabled as a clock master and the SBIN input pin goes Low. This indicates that a slave device wants to activate the IOM 2 Interface and communicate with the DSC circuit. Both the $\overline{INT}$ pin and the IOM 2 timing request interrupts must be enabled for Power-Down Mode to be exited.
- The IOM 2 Interface is enabled as a clock slave and the SCLK input pin goes High. This indicates that the master device is activating the IOM 2 Interface and the DSC circuit must wake up in order to monitor the data. Both the $\overline{INT}$ pin and the IOM 2 timing request interrupts must be enabled for Power-Down Mode to be exited.

If the DSC/IDC circuit is awakened by any condition other than RESET, the MCLK output will be restored to its previously programmed frequency, and will not generate any shortened or spurious output cycles. If the DSC/IDC circuit is revived by RESET, MCLK will default to its normal 6.144-MHz rate. The DSC/IDC circuit provides a minimum of two MCLK cycles prior to activating the interrupt pin when exiting Power-Down Mode.

MCLK Frequency Control

The MCLK frequency selection bits in the INIT register are unchanged from Revision D. However, additional MCLK frequencies are available by programming bits in the INIT2 register. No shortened or spurious clock pulses that might disrupt the external microprocessor will result when the MCLK frequency is changed.

In order to reduce the probability of errant software disrupting system operation, the INIT2 register requires two consecutive writes before the value will be entered into the register. Note that there will be no MCLK countdown as is the case for entering Power-Down Mode if INIT2 is programmed to cause MCLK to STOP, and there will be no shortened or spurious MCLK pulses.

MCLK Clock Speed-up Function

A programmable automatic MCLK speed-up option is provided that will force a hardware reset of INIT2 Bits 3–0, which will cause the MCLK frequency to be restored to the value programmed in the INIT register. There are two events that will trigger the clock speed-up function:

1. The DLC receive FIFO threshold has been reached; or,
2. a second packet begins to be received while data from a prior packet is still in the receive FIFO.

The second packet case requires provision of an interrupt; see the DLC register section for further information. The clock speed-up function allows the user to program a very slow MCLK frequency using INIT2 when D-channel activity is minimal. If a burst of activity is seen on the D Channel which exceeds the programmed threshold of the receive FIFO or threatens to overrun the receive FIFO status buffers, MCLK will instantly toggle back to the higher frequency programmed in the INIT register. This eliminates the latency incurred if an interrupt has to be serviced to change the clock speed, and allows the overall system power to be reduced during typical voice connections. Note that automatic clock speed-up will not function unless at least one of the associated interrupts are enabled so the processor can be informed that the clock speed has been altered.

Global Register Functions

INIT Register (INIT) default = 00H; Address = Indirect 21 Hex, Read/Write

Bit 7 6 5 4 3 2 1 0	Function
X X X X X X 0 0	Idle Mode
X X X X X X 0 1	Active Voice and Data Mode
X X X X X X 1 0	Active Data Only Mode
X X X X X X 1 1	Power-Down Mode
X X X X X 0 X X	$\overline{INT}$ output enabled
X X X X X 1 X X	$\overline{INT}$ output disabled
X X 0 0 0 X X X	MCLK frequency = 6.144 MHz
X X 0 0 1 X X X	MCLK frequency = 12.288 MHz
X X 0 1 0 X X X	MCLK frequency = 3.072 MHz
X X 0 1 1 X X X	MCLK frequency = 6.144 MHz
X X 1 0 0 X X X	MCLK frequency = 4.096 MHz
X X 1 0 1 X X X	MCLK frequency = 6.144 MHz
X X 1 1 0 X X X	MCLK frequency = 6.144 MHz
X X 1 1 1 X X X	MCLK frequency = 6.144 MHz
X 0 X X X X X X	DLC receiver abort disabled
X 1 X X X X X X	DLC receiver abort enabled
0 X X X X X X X	DLC transmitter abort disabled
1 X X X X X X X	DLC transmitter abort enabled

INIT2 Register (INIT2) default = 00H; Address = Indirect 20 Hex, Read/Write

A special write procedure must be followed in order to modify the contents of the INIT2 Register, since the INIT2 register includes control bits which could result in the stopping of the microprocessor clock. This procedure greatly reduces the probability of errant software disabling the system, and is described as follows:

1. Write the INIT2 address to the Command Register.
2. Write to the Data Register (INIT2 is not yet updated).
3. Write the INIT2 address to the Command Register.
4. Write to the Data Register (INIT2 is updated).

The writes must take place without any intervening indirect accesses to the DSC/IDC circuit.

Bit 7 6 5 4 3 2 1 0	Function
0 0 X X X X X X	Reserved, must be written to 0 READ's are undefined
0 0 0 X X X X X	Power-Down disabled; writing 11 to the INIT register will put the DSC/IDC circuit into Idle Mode
0 0 1 X X X X X	Power-Down enabled; writing 11 to the INIT register will put the DSC/IDC circuit into Power-Down Mode
0 0 X 0 X X X X	Multiframe Interrupt Filter disabled
0 0 X 1 X X X X	Multiframe Interrupt Filter enabled (see LIU section for detailed description)
0 0 X X 0 X X X	Clock speed-up option disabled
0 0 X X 1 X X X	Clock speed-up option enabled; if set, this register bit will be cleared when the DLC FIFO receive threshold or second packet received interrupt is triggered
0 0 X X X 0 0 0	MCLK frequency determined by INIT register
0 0 X X X 0 0 1	MCLK frequency is 1.536 MHz
0 0 X X X 0 1 0	MCLK frequency is 768 kHz
0 0 X X X 0 1 1	MCLK frequency is 384 kHz
0 0 X X X 1 0 0	MCLK stopped in High state
0 0 X X X 1 0 1	Reserved
0 0 X X X 1 1 0	Reserved
0 0 X X X 1 1 1	Reserved

RESET Operation

The Am79C30A/32A can be reset by driving the RESET pin High. When power is first supplied to the DSC/IDC circuit, a reset must be performed. This initializes the DSC/IDC circuit to its default condition as defined in the following table.

Pin Name	State following RESET
D7–D0	High Impedance
MCLK	6.144 MHz
$\overline{INT}$	Logical 1
SBOUT	High Impedance
SFS	High Impedance
SCLK	High Impedance
LS1, LS2	High Impedance
EAR1	High Impedance
EAR2	High Impedance
AREF	High Impedance
LOUT1	High Impedance
LOUT2	High Impedance

Receive and Transmit Abort Commands

The microprocessor has the option via INIT register bits 6 and 7 to abort the receive and transmit D-channel packets. When the microprocessor sets one of these bits, the Am79C30A/32A aborts the respective operation. The frame abort sequence is defined in greater detail later. (See Data Link Controller section.)

Interrupt Handling

The Am79C30A/32A generates either no interrupt or only one interrupt every 125 µs. Once asserted, $\overline{INT}$ remains active until the microprocessor responds by interrogating the Am79C30A/32A's Interrupt Register (IR) (see Table 1). Reading the IR in response to an activated $\overline{INT}$ pin deactivates the $\overline{INT}$ pin, and clears the IR.

If an event causing an interrupt occurs while the IR is being read by the microprocessor, the effect of the event is held until the microprocessor has completed its read cycle. A reset clears all conditions causing interrupts.

Bits 0,1, and 4 of the IR, if set, advise the microprocessor that the respective buffer is ready for reading or writing. If Bit 0 is set due to an empty buffer, the D-Channel Transmit Buffer must be serviced within 375 µs. If Bit1 is set and the D-Channel Receive Buffer is full, the buffer must be serviced within 425 µs. This is to prevent erroneous data transfers causing transmitter underrun and receiver overrun errors. If Bit 4 is set then the Bb or Bc buffers must be accessed within 122.4 µs. This is to prevent erroneous data transfers. Only one interrupt is used to signal accessibility for both B Channels of the S Interface. Since the data transfer must occur synchronously to the S Interface, any data access to either Bb or Bc or both must be made within the 122.4 µs limit.

Note that even though only a single interrupt is issued, either or both S-interface B Channels must be serviced. IR bits 2, 3, 5, 6, and 7, if set, indicate that a bit has

been set in the associated status or error register. All of the interrupts generated by the Am79C30A/32A can be individually disabled. In the case of IR Bit 7, the interrupt can also be masked by setting PPIER Bit 7 to 0.

DMR1, DMR2, DMR3, LMR2, MCR4, and MF control the mask conditions which affect the $\overline{INT}$ pin. The $\overline{INT}$ pin is activated only by interrupts which are not disabled.

The Interrupt Register reflects the status of enabled interrupts. The $\overline{INT}$ pin can be disabled by setting INIT register bit 2 to a logical 1.

The Am79C30A/32A has facilities that allow the microprocessor to read the status registers (status update is inhibited during status read) or the IR at any time during functional operation.

Table 1. Format of the Interrupt Register (IR), Read Only

Bit	Interrupt Generated/Action Required		Interrupt Mask
0	D-channel transmit threshold interrupt/load D-Channel Transmit Buffer		DMR1 bit 0
1	D-channel receive threshold interrupt/read D-Channel Receive Buffer		DMR1 bit 1
2	D-channel status interrupt/read DSR1		
	Source	Cause	
	DSR1 bit 0	Valid Address (VA) or End of Address (EOA)	DMR3 bit 0
	DSR1 bit 1	When a closing flag is received or a receive error occurs	DMR1 bit 3
	DSR1 bit 6	When a closing flag is transmitted	DMR3 bit 1
3	D-channel error interrupt/read DER and DSR2 bit 2		
	Source	Cause	
	DER bit 0	Current received packet has been aborted	DMR2 bit 0
	DER bit 1	Non-integer number of bytes received	DMR2 bit 1
	DER bit 2	Collision abort detected	DMR2 bit 2
	DER bit 3	FCS error	DMR2 bit 3
	DER bit 4	Overflow error	DMR2 bit 4
	DER bit 5	Underflow error	DMR2 bit 5
	DER bit 6	Overrun error	DMR2 bit 6
	DER bit 7	Underrun error	DMR2 bit 7
	DSR2 bit 2	Receive packet lost	DMR3 bit 6
4	Bb or Bc byte available or buffer empty interrupt/read or write Bb or Bc buffers		MCR4 bit 3
5	LIU status interrupt/read LSR		
	Source	Cause	
	LSR bit 3	Change of state to F3	LMR2 bit 3
	LSR bit 4	Change of state from/to F7	LMR2 bit 6
	LSR bit 5	Change of state from/to F8	LMR2 bit 4
	LSR bit 7	HSW change of state	LMR2 bit 5
6	D-channel status interrupt/read DSR2		
	Source	Cause	
	DSR2 bit 0	Last byte of received packet	DMR3 bit 2
	DSR2 bit 1	Receive byte available	DMR3 bit 3
	DSR2 bit 3	Last byte transmitted	DMR3 bit 4
	DSR2 bit 4	Transmit buffer available	DMR3 bit 5
	DSR2 bit 7	Start of second packet	EFCR bit 1
7	Multiframe or PP interrupt/read MFSB and PPSR		
	Source	Cause	
	MFSB bit 5	S-data available	MF bit 1
	MFSB bit 6	Q-bit buffer empty	MF bit 2
	MFSB bit 7	Multiframe change of state (in/out of sync)	MF bit 3
	PPSR bit 0	Monitor receive, data available	PPIER bit 0
	PPSR bit 1	Monitor transmit, buffer available	PPIER bit 1
	PPSR bit 2	Monitor EOM received	PPIER bit 2
	PPSR bit 3	Monitor abort received	PPIER bit 3
	PPSR bit 4	C/I channel 0, data change	PPIER bit 4
	PPSR bit 5	C/I channel 1, data change	PPIER bit 5
	PPSR bit 6	IOM 2 timing request	PPIER bit 6

FUNCTIONAL DESCRIPTION

Microprocessor Interface (MPI)

The Am79C30A/32A can be connected to any general purpose 8-bit microprocessor via the MPI. The MCLK from the Am79C30A/32A can be used as the clock for the microprocessor. The MPI is an interrupt driven interface containing all the circuitry necessary for access to the internal programmable registers, status registers, coefficient RAM, and transmit/receive buffers.

MPI External Interface

The MPI has the following external connections:

Name	Direction	Function
D7–D0	Bidirectional	Data Bus
A2–A0	Inputs	Address Line
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
RESET	Input	Initialization
$\overline{INT}$	Output	Interrupt

Direct Registers

Access to the Direct Registers of the Am79C30A/32A is controlled by the state of the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A2, A1, and A0 input pins, as defined below by Table 2.

Indirect Registers

To read from or write to any of the Indirect Registers, an indirect address command is first written to the Command Register (CR). One or more data bytes may then be transferred to or from the selected register through the Data Register (DR).

Registers within certain groups can be quickly accessed by using internal circuitry which automatically increments the indirect value. In Table 3, the "bytes transferred numbers" are the number of bytes which are read or written to the DR after the CR has been loaded. Whenever the CR is loaded, any previous commands are automatically terminated.

Table 2. Direct Register Access Guide

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A2	A1	A0	Register(s) Accessed	Mode
0	1	0	0	0	0	Command Register (CR)	W
0	0	1	0	0	0	Interrupt Register (IR)	R
0	1	0	0	0	1	Data Register (DR)	W
0	0	1	0	0	1	Data Register (DR)	R
0	0	1	0	1	0	D-Channel Status Register 1 (DSR1)	R
0	0	1	0	1	1	D-Channel Error Register (DER) (2-byte FIFO)	R
0	1	0	1	0	0	D-Channel Transmit Buffer (DCTB) (8- or 16-byte FIFO)	W
0	0	1	1	0	0	D-Channel Receive Buffer (DCRB) (8- or 32-byte FIFO)	R
0	1	0	1	0	1	Bb-Channel Transmit Buffer (BBTB)	W
0	0	1	1	0	1	Bb-Channel Receive Buffer (BBRB)	R
0	1	0	1	1	0	Bc-Channel Transmit Buffer (BCTB)	W
0	0	1	1	1	0	Bc-Channel Receive Buffer (BCRB)	R
0	0	1	1	1	1	D-Channel Status Register 2 (DSR2)	R
1	X	X	X	X	X	No access (X = logical 0 or 1)	—

Note: The $\overline{RD}$ and $\overline{WR}$ signals must never both be Low under normal operating conditions.

Table 3. Indirect Register Access Guide

Operation Block	Register	Register Number	Indirect Name	Mode	Address	Byte Sequence
INIT		1	INIT	R/W	21H	One byte transferred
INIT		2	INIT2	R/W	20H	One byte transferred
LIU	LIU Status Register	1	LSR	R	A1H	One byte transferred
LIU	LIU Priority Register	2	LPR	R/W	A2H	One byte transferred
LIU	LIU Mode Register 1	3	LMR1	R/W	A3H	One byte transferred
LIU	LIU Mode Register 2	4	LMR2	R/W	A4H	One byte transferred
LIU	—	5	Perform 2–4	—	A5H	LPR, LMR1, LMR2
LIU	Multiframe Register	6	MF	R/W	A6H	One byte transferred
LIU	Multiframe S-Bit/Status Register	7	MFSB	R	A7H	One byte transferred
LIU	Multiframe Q-Bit Buffer	8	MFQB	W	A8H	One byte transferred
MUX		1	MCR1	R/W	41H	One byte transferred
MUX		2	MCR2	R/W	42H	One byte transferred
MUX		3	MCR3	R/W	43H	One byte transferred
MUX		4	MCR4	R/W	44H	One byte transferred
MUX		5	Perform 1–4	—	45H	MCR1, 2, 3, 4
MAP	X Filter Coefficient Register	1	X Coeff.	R/W	61H	h0 LSB, h0 MSB...h7 MSB
MAP	R Filter Coefficient Register	2	R Coeff.	R/W	62H	h0 LSB, h0 MSB...h7 MSB
MAP	GX Gain Coefficient Register	3	GX Coeff.	R/W	63H	LSB, MSB
MAP	GR Gain Coefficient Register	4	GR Coeff.	R/W	64H	LSB, MSB
MAP	GER Gain Coefficient Register	5	GER Coeff.	R/W	65H	LSB, MSB
MAP	Sidetone Gain Coefficient Register	6	STG Coeff.	R/W	66H	LSB, MSB
MAP	Frequency Tone Generator Register 1, 2	7	FTGR1,FTGR2	R/W	67H	FTGR1, 2
MAP	Amplitude Tone Generator Register 1, 2	8	ATGR1,ATGR2	R/W	68H	ATGR1, 2
MAP	MAP Mode Register 1	9	MMR1	R/W	69H	One byte transferred
MAP	MAP Mode Register 2	10	MMR2	R/W	6AH	One byte transferred
MAP	—	11	Perform 1–10	—	6BH	46 bytes loaded 1–10
MAP	MAP Mode Register 3	12	MMR3	R/W	6CH	One byte transferred
MAP	Secondary Tone Ringer Amplitude	13	STRA	R/W	6DH	One byte transferred
MAP	Secondary Tone Ringer Frequency	14	STRF	R/W	6EH	One byte transferred
DLC	First Received Byte Address Registers 1, 2, 3	1	FRAR1, 2, 3	R/W	81H	FRAR1, 2, 3
DLC	Second Received Byte Address Registers 1, 2, 3	2	SRAR1, 2, 3	R/W	82H	SRAR1, 2, 3
DLC	Transmit Address Register	3	TAR	R/W	83H	LSB, MSB
DLC	D-Channel Receive Byte Limit Register	4	DRLR	R/W	84H	LSB, MSB
DLC	D-Channel Transmit Byte Count Register	5	DTCR	R/W	85H	LSB, MSB
DLC	D-Channel Mode Register 1	6	DMR1	R/W	86H	One byte transferred
DLC	D-Channel Mode Register 2	7	DMR2	R/W	87H	One byte transferred

Table 3. Indirect Register Access Guide (continued)

Operation Block	Register	Register Number	Indirect Name	Mode	Address	Byte Sequence
DLC	—	8	Perform 1–7	—	88H	4 bytes loaded 1–7
DLC	D-Channel Receive Byte Count Register	9	DRCR	R	89H	LSB, MSB
DLC	Random Number Generator Register	10	RNGR1 (LSB)	R/W	8AH	One byte transferred
DLC	Random Number Generator Register	11	RNGR2 (MSB)	R/W	8BH	One byte transferred
DLC	First Received Byte Address Register 4	12	FRAR4	R/W	8CH	One byte transferred
DLC	Second Received Byte Address Register 4	13	SRAR4	R/W	8DH	One byte transferred
DLC	D-Channel Mode Register 3	14	DMR3	R/W	8EH	One byte transferred
DLC	D-Channel Mode Register 4	15	DMR4	R/W	8FH	One byte transferred
DLC	—	16	Perform 12–15	—	90H	FRAR4, SRAR4, DMR3, DMR4
DLC	Address Status Register	17	ASR	R	91H	One byte transferred
DLC	Extended FIFO Control Register	18	EFCR	R/W	92H	One byte transferred
PP	Peripheral Port Control Register 1	1	PPCR1	R/W	C0H	One byte transferred
PP	Peripheral Port Status Register	2	PPSR	R	C1H	One byte transferred
PP	Peripheral Port Interrupt Enable Register	3	PPIER	R/W	C2H	One byte transferred
PP	Monitor Transmit Data Register	4	MTDR	W	C3H	One byte transferred
PP	Monitor Receive Data Register	5	MRDR	R	C3H	One byte transferred
PP	C/I Transmit Data Register 0	6	CITDR0	W	C4H	One byte transferred
PP	C/I Receive Data Register 0	7	CIRDR0	R	C4H	One byte transferred
PP	C/I Transmit Data Register 1	8	CITDR1	W	C5H	One byte transferred
PP	C/I Receive Data Register 1	9	CIRDR1	R	C5H	One byte transferred
PP	Peripheral Port Control Register 2	10	PPCR2	R/W	C8H	One byte transferred

Line Interface Unit (LIU)

The LIU connects to the four-wire S Interface through a pair of isolation transformers, one for the transmit and one for the receive direction, as shown in Figure 1.

The receiver section of the LIU consists of a differential receiver, circuitry for bit timing recovery, circuitry for detecting High and Low marks, and a frame recovery circuit for frame synchronization. The receiver converts the received pseudo-ternary coded signals to binary before delivering them to the other blocks of the Am79C30A/32A. It also performs collision detection (E- and D-bit comparison) per the CCITT recommendations so several TEs can be connected to the same S Interface.

The transmitter consists of a binary to pseudo-ternary encoder and a differential line driver which meets the CCITT recommendations for the S Interface.

The Am79C30A/32A can establish multiframe synchronization, receive S Bits, and transmit Q bits synchronized to the received frame.

External Interface

The LIU can be connected to both point-to-point and point-to-multipoint configurations at the CCITT S reference point. The point-to-point configuration consists of one TE connected to the NT or PABX linecard. The point-to-multipoint configuration can have multiple TEs connected to one NT.

Line Code

Pseudo-ternary coding is used for both transmitting and receiving over the S Interface. In this type of coding, a binary 1 is represented by a space (zero voltage), and a binary 0 is represented by a High mark or a Low mark. Two consecutive binary 0s are represented by alternate

marks to reduce DC offset on the line. A mark followed, either immediately or separated by spaces, by a mark of the same polarity, is defined as a code violation. Code violations are used to identify the boundaries of the frame.

Frame Structures

In both transmit and receive directions, the bits are grouped into frames of 48 bits each. The frame structure is identical for both point-to-point and point-to-multipoint configurations. Each frame transmitted at 4 kHz consists of several groups of bits.

Multiframing

If multiframing is enabled, the Am79C30A/32A recognizes and establishes multiframe synchronization based on the monitoring of the F_A (Q-bit control) and M (M-bit control) Bits. The Am79C30A/32A also receives and compiles S Bits, and transmits Q Bits synchronized to the received frame.

Establishment of Multiframe Synchronization

When the enable multiframe synchronization bit (Bit 0 of the Multiframe Register) is set and the LIU is in state F7, the LIU monitors the F_A (Q-bit control) and M (M-bit control) Bits. When three consecutive multiframes with the M Bits and F_A Bits set as defined in Table 4 are received, the multiframe synchronized bit (Bit 7 of the Multiframe Register) and multiframe change of state bit (Bit 7 of the Multiframe S Bit/Status Buffer) are set. Note that S-bit data is received, compiled and transferred to the user after attaining synchronization at the start of the next multiframe.

S-Bit Reception

The default operation of the DSC/IDC circuit is that the LIU will receive and pass multiframe data to the user in 5-bit increments four times per multiframe, regardless of the value of the data. After multiframe synchronization has been requested and established, the microprocessor can read the Multiframe S Bit/Status Buffer (MFSB) once the S-bit available bit (MFSB Bit 5) is set. The S-data available bit is set to a logical 1 when the Am79C30A/32A has received five S Bits (one S Bit per S-interface frame) synchronized to the setting of the FA-bit to a logical 1 and transferred them into the MFSB. Once the S-bit available bit is set, the MFSB must be accessed within 1.25 ms or succeeding S data will be lost.

Subsequent to the original definition of the DSC/IDC circuit, the CCITT has defined a structure for the 20 multiframe bits, which specifies five 4-bit channels. Furthermore, the idle code for these channels has been defined as 0000. An enhanced mode of multiframe reception has been included, which may be enabled by setting INIT2 Bit 4 to a 1. This enhanced mode reduces processor overhead by generating an interrupt only upon the reception of a non-zero S-channel word. INIT2 Bit 4 will be automatically cleared by hardware when the five received data bits in the MFSB are not all 0s, as long as MF Bit 1 (interrupt enable) is set. This allows subsequent valid all-zero words to be received. Furthermore, when the first five S Bits of the multiframe are loaded into the MFSB, Bit 4 of the MF register will be set, which allows identification of the position of received words within the multiframe.

HSW

The hookswitch circuitry on the DSC circuit provides the attached microprocessor with a way of converting an external mechanical hookswitch into a software status condition capable of generating an interrupt. Debounce and glitch rejection are provided internal to the DSC circuit. The logic rejects glitches less than 162 ns and provides debounce of 16 ms. HSW status reporting is disabled after RESET. It is enabled by any of the following: taking the device out of Idle Mode, a write to a MUX Control register (MCR3–MCR1), or unmasking the HSW interrupt.

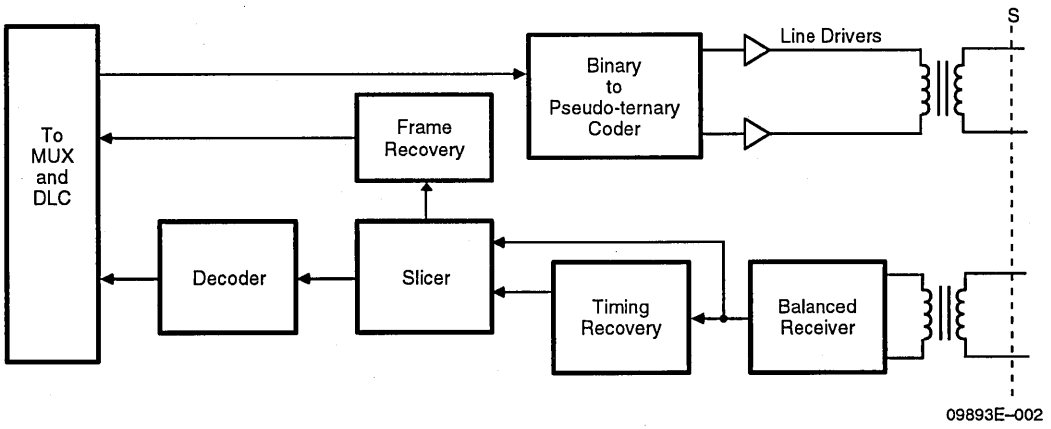


Figure 1. LIU Block Diagram

Table 4. Multiframing Structures

Frame Number	NT-to-TE Q Control Bit FA	NT-to-TE M Bit (M)	NT-to-TE S Bit (S)	TE-to-NT F_A Bit (Q Bit)
1	1	1	SC11	Q1
2	0	0	SC21	0
3	0	0	SC31	0
4	0	0	SC41	0
5	0	0	SC51	0
6	1	0	SC12	Q2
7	0	0	SC22	0
8	0	0	SC32	0
9	0	0	SC42	0
10	0	0	SC52	0
11	1	0	SC13	Q3
12	0	0	SC23	0
13	0	0	SC33	0
14	0	0	SC43	0
15	0	0	SC53	0
16	1	0	SC14	Q4
17	0	0	SC24	0
18	0	0	SC34	0
19	0	0	SC44	0
20	0	0	SC54	0
1	1	1	SC11	Q1
2	0	0	SC21	0
etc.				

Transmission of Q-bits

The microprocessor can load the Multiframe Q-bit Buffer (MFQB) once the Q-bit buffer empty bit (Bit 6 of the Multiframe S Bit/Status Buffer) is set. The Q-bit buffer empty bit is set to a logical 1 at reset or when data that has been written to the Multiframe Q-bit Buffer is transferred to the LIU. The Q-bit buffer empty bit is cleared to a logical 0 when the Multiframe S-bit/Status Buffer is read. After multiframing has been requested and established the Am79C30A/32A transfers the data written into the Q-bit Register to the LIU, synchronized to the multiframe, irrespective of the receipt of valid Q-control bits. If the microprocessor does not reload the Q-bit Register for retransmission, the Q-bit pattern is repeated in the next multiframe.

If multiframing is enabled but multiframe synchronization is not established, the LIU transmits the value loaded in MFQB Bit 4 in all Q Bits. The default value of MFQB Bit 4 is a logical 0 which satisfies the CCITT recommendations. When synchronization is achieved, the contents of MFQB Bits 3 to 0 are transmitted according to Table 4.

Loss of Multiframe Synchronization

The Am79C30A/32A continuously monitors the F_A (Q-bit control) and the M Bits to assure multiframe synchronization. Once multiframe synchronization is established, multiframe synchronization is lost if three consecutive invalid multiframes are received, or the LIU exits state F7, or multiframing is disabled. When loss of multiframe synchronization occurs, Bit 7 of the Multiframe Register is set to a logical 0, and Bit 7 of the Multiframe S Bit/Status Buffer is set to a logical 1. The Am79C30A/32A also terminates the reception of S Bits and transmission of Q Bits until multiframing synchronization is re-established.

LIU Registers

The LIU contains the following registers:

Registers	No./Registers	Mnemonic
LIU Status Register	1	LSR
LIU Priority Register	1	LPR
LIU Mode Registers	2	LMR1, LMR2
Multiframe Register	1	MF
Multiframe S-Bit/Status Register	1	MFSB
Multiframe Q-Bit Buffer	1	MFQB

LIU Status Register (LSR), Read Only; Address = Indirect A1H

The LSR has the following format:

Bit	Logical 1	Generates Interrupt
2,1,0	Binary values 000 through 110 represent the LIU activation circuitry's current state (F2 through F8, respectively) Bit 2 is MSB	No
3	Change of state to F3	If LMR2 bit 3 = 1
4	Change of state from/to F7	If LMR2 bit 6 = 1
5	Change of state from/to F8	If LMR2 bit 4 = 1
6	HSW state	No
7	HSW change of state	If LMR2 bit 5 = 1

When the microprocessor reads the LSR, Bits 3, 4, 5, and 7 are cleared. The other bits retain the current status of the LIU. Bits 0 to 2 are defined such that state F2 (see CCITT I.430 state matrix tables) is coded as 0, F3 as 1, F4 as 2, and so on, where Bit 0 is the LSB. The LIU interrupts the microprocessor via Bit 4 of the LSR when activation has been achieved (that is, when the LIU moves to state F7 upon receipt of INFO 4). During reset the LSR is 0.

Even though the LIU Status Register (LSR) is read-only, no default value upon power-up is given due to the uncertain state of Bit 6 (Hookswitch State). Following RESET, The LIU State is F2 and the HSW bit reflects the HSW pin, producing a power-up value of either 00H or 40H.

LIU D-Channel Priority Register (LPR), Read/Write

The LPR contains the priority level for D-channel access. Its default value after reset is 0.

The D-channel access procedure of the Am79C30A/32A uses the priority level programmed in the LPR. The priority mechanism defined by the CCITT I-series recommendations is fully implemented if the LPR is programmed via the microprocessor to conform to the priority class of the Layer-2 frame to be transmitted. The LPR has 16 possible programmable priority levels. The priority levels are numbered 0–15. Priority Level 0 corresponds to counting eight 1s in the echo channel, priority Level 1 corresponds to counting ten 1s in the echo channel, priority Level 2 corresponds to counting twelve 1s, etc. The DSC circuit automatically handles transitions between the programmed priority level n and the associated odd value n+1. The priority is incremented following a successfully transmitted packet, and decremented when the higher count has been satisfied.

The LPR has the following format:

Bits	Description
3,2,1,0	D-channel access priority level Bit 0 is LSB
7,6,5,4	Reserved, reads logical 0

LIU Mode Register (LMR1), Read/Write; Address = Indirect A3H

LMR1 is defined as follows:

Bit	Logical 1	Logical 0 (default value)
0	Enable B1 transmit	Disable B1 transmit
1	Enable B2 transmit	Disable B2 transmit
2	Disable F transmit	Enable F transmit
3	Disable F_A transmit	Enable F_A transmit
4	Activation request	No activation request
5	Go from F8 to F3	No transition
6	Enable receiver/transmitter	Disable receiver/transmitter
7	Reserved; must be set to logical 0	Reserved; must be set to logical 0

The F and F_A Bits in LMR1 (Bits 2 and 3) should be enabled during the activation procedure so the Am79C30A/32A can respond with INFO 3.

LMR1 Bit 4 is used to transfer the signals PH-AR and Expiry of Timer from the microprocessor to the LIU (see CCITT I.430 state diagram—activation request). PH-AR is defined as Bit 4 being a logical 1 and Expiry of Timer is defined as the transition of Bit 4 from a logical 1 to a logical 0. This bit must not be set until the LIU, as reflected in the LSR, is in state F3, F6 or F7 and the receiver has been enabled for a minimum of 250 µs.

LMR1 Bit 6 is primarily used to disable the receiver when the terminal does not require access to the S Interface signals. This bit is cleared by reset and must be written to logical 1 in order to receive activation from the S Interface, or to request activation.

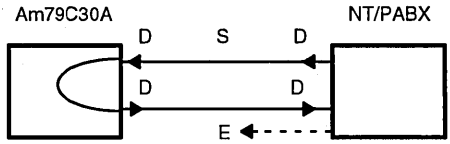
LIU Mode Register 2 (LMR2), Read/Write; Address = Indirect A4H

LMR2 is used to select the following operations:

Bit	Logical 1	Logical 0 (Default Value)
0	D-channel loopback at Am79C30A/32A enable	D-channel loopback at Am79C30A/32A disable
1	D-channel loopback at LIU enable	D-channel loopback at LIU disable
2	D-channel back-off disable	D-channel back-off enable
3	F3 change of state interrupt enable	F3 change of state interrupt disable
4	F8 change of state interrupt enable	F8 change of state interrupt disable
5	HSW interrupt enable	HSW interrupt disable
6	F7 change of state interrupt enable	F7 change of state interrupt disable
7	Reserved; must be set to logical 0	Reserved; must be set to logical 0

The three D-channel loopback controls defined in LMR2 Bits 0, 1, and 2 are explained below:

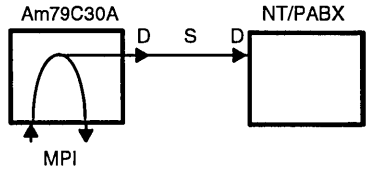
Bit 0, D-channel loopback at Am79C30A/32A enable:



This remote loopback is provided for maintenance purposes from the NT's perspective. The NT transmits D-channel bits to the Am79C30A/32A where they are internally looped (with the Data Link Controller) and transmitted back to the NT. The incoming D-channel data can be accessed by the microprocessor; however, the microprocessor cannot send data on the outgoing D Channel.

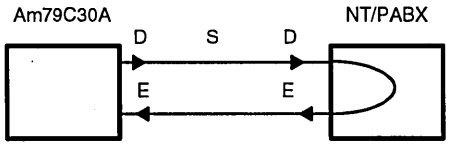
Any difference between the transmitted D-channel bits and the received E-channel bits to/from the Am79C30A/32A (normally detected as an error which halts the transmission) is ignored, thereby allowing the transmission to continue.

Bit 1, D-channel loopback at LIU enable:



This local loopback is provided for local testing. Data on the incoming D Channel is ignored. The data from the microprocessor is processed by the DLC and then looped back to the microprocessor in addition to being output to the S Interface.

Bit 2, D-channel back-off disable:



This loopback is provided for maintenance purposes from the TE's perspective. The Am79C30A/32A transmits D-channel bits to the NT where they are looped and transmitted back to the Am79C30A/32A in the E Channel. The operation is normal except differences between the D and E Channels do not halt the transmission.

Multiframe Register (MF), Read/Write; Address = Indirect A6H

Bit	Logical 1	Logical 0 (Default Value)
0	Enable multiframe synchronization	Disable multiframe synchronization
1	Enable S-data available interrupt	Disable interrupt
2	Enable Q-bit buffer empty interrupt	Disable interrupt
3	Enable Multiframe change of state interrupt	Disable interrupt
4	First subframe	Not first subframe
6,5	Not used, reads logical 0	Not used, reads logical 0
7	Multiframe synchronized (read only)	Multiframe not synchronized (read only)

Multiframe S-bit/Status Buffer (MFSB), Read Only; Address = Indirect A7H

Bit	Description	Generates Interrupt
0	S1	No
1	S2	No
2	S3	No
3	S4	No
4	S5	No
5	S-data available	If MF bit 1 = 1
6	Q-bit buffer empty	If MF bit 2 = 1
7	Multiframe change of state	If MF bit 3 = 1

The MFSB reset default value is 40H.

Multiframe Q-bit Buffer (MFQB), Write Only; Address = Indirect A8H

Bit	Description
0	Q1 (default = 1)
1	Q2 (default = 1)
2	Q3 (default = 1)
3	Q4 (default = 1)
4	Q-bit value when multiframing enabled but synchronization not achieved (default = 0)
5,6,7	Not used

Multiplexer (MUX)

The MUX contains the following registers:

Register	No./Registers	Mnemonic
MUX Control Registers	4	MCR1, MCR2, MCR3, MCR4

The Multiplexer is used to selectively route 64-kb/s full-duplex B Channels between the LIU (Line Interface Unit), MAP (Main Audio Processor), MPI (Microprocessor Interface), and the PP (Peripheral Port).

The logical channels available at the MUX are shown in Figure 2. They are:

1. From/to the LIU Channels B1 and B2
2. From/to the MAP Channel Ba
3. From/to the MPI Channels Bb and Bc
4. From/to the PP Channels Bd, Be, and Bf

For any specific application, the MUX can be programmed by the microprocessor to route any three B-channel ports to any other three B-channel ports. Programmable bidirectional bit reversal is provided for both of the MPI data channels Bb and Bc.

MUX Control Registers 1, 2, and 3 (MCR1, MCR2, and MCR3), Read/Write; Addresses = Indirect 41H, 42H, 43H

The MUX can support three bidirectional paths. The contents of the MUX Control Registers MCR1, MCR2, and MCR3 direct the flow of data between the eight MUX logical B Channels (see Figure 2). These three MCRs are programmed to connect any two B-channel ports together by writing the appropriate channel code into an MCR. These MCRs have the same format, where Bits 7–4 indicate port 1 and Bits 3–0 indicate port 2. In each of these three MCR registers, the following channel codes are used for both ports 1 and 2:

MCR Register Channel Codes

Code	Channel
0000	No connection (default value)
0001	B1 (LIU)
0010	B2 (LIU)
0011	Ba (MAP)
0100	Bb (MPI)
0101	Bc (MPI)
0110	Bd (PP channel 1)
0111	Be (PP channel 2)
1000	Bf (PP channel 3)

For example, to connect B1(LIU) with Bb (MPI) and B2 (LIU) with Ba (MAP), the contents of the MCRs would be:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 1 0 1 0 0	B1 (LIU)<—>Bb (MPI)
MCR2	0 0 1 0 0 0 1 1	B2 (LIU)<—>Ba (MAP)
MCR3	0 0 0 0 0 0 0 0	No connect<->No connect

Therefore, in this example, MCR1 provides a data link from the S Interface and MCR2 sets up a voice connection across the S Interface.

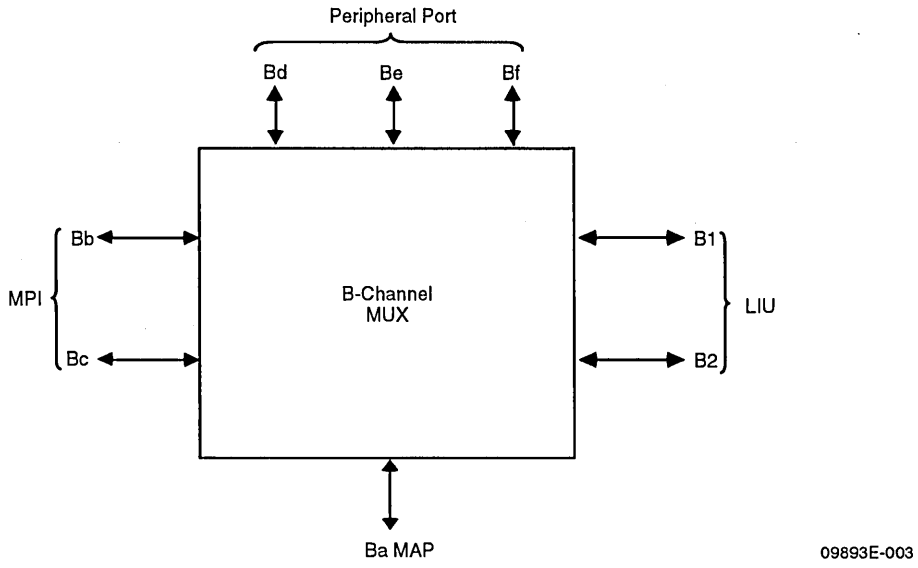


Figure 2. MUX Logical Channels

To loopback a channel, the same channel code is used for port 1 and port 2. For example, to loopback B1, B2, and Ba, the MCRs would be:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 1 0 0 0 1	B1 (LIU) Loopback
MCR2	0 0 1 0 0 0 1 0	B2 (LIU) Loopback
MCR3	0 0 1 1 0 0 1 1	Ba (MAP) Loopback

MCR3 has higher priority than MCR2. MCR2 has higher priority than MCR1.

If multiple connections are made to the same port, the data from the connecting ports in the highest priority MCR will overwrite the data from the connecting port in the lower priority MCR, for example:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 0 0 0 0 0	No connect
MCR2	0 0 0 1 0 1 0 0	B1 (LIU)<—>Bb (MPI)
MCR3	0 1 0 0 0 0 1 1	Bb (MPI)<—>Ba (MAP)

The final data transfers are:

B1 (LIU) receives Bb (MPI),
Ba (MAP) receives Bb (MPI),
Bb (MPI) receives Ba (MAP).

Therefore, the data transfer from B1(LIU) to Bb(MPI) is lost in the arrangement proposed in MCR2.

MUX Control Register 4 (MCR4), Read/Write; Address = Indirect 44H

The MUX Control Register 4 (MCR4) can prevent interrupt generation by masking the output of IR Bit 4. MCR4 has the following format:

Bit	Logical 1	Logical 0 (Default Value)
2,1,0	Reserved, must be set to logical 0	Reserved, must be set to logical 0
3	Enable Bb- or Bc-channel byte available interrupt (IR Bit 4)	Disable interrupt
4	Reverse bit order of Bb (LSB transmitted/received first)	No Bb bit reversal (MSB transmitted/received first)
5	Reverse bit order of Bc (LSB transmitted/received first)	No Bc bit reversal (MSB transmitted/received first)
6	Reserved, must be set to logical 0	Reserved, must be set to logical 0
7	Reserved, must be set to logical 0	Reserved, must be set to logical 0

Main Audio Processor (MAP)

(Am79C30A Only)

Overview

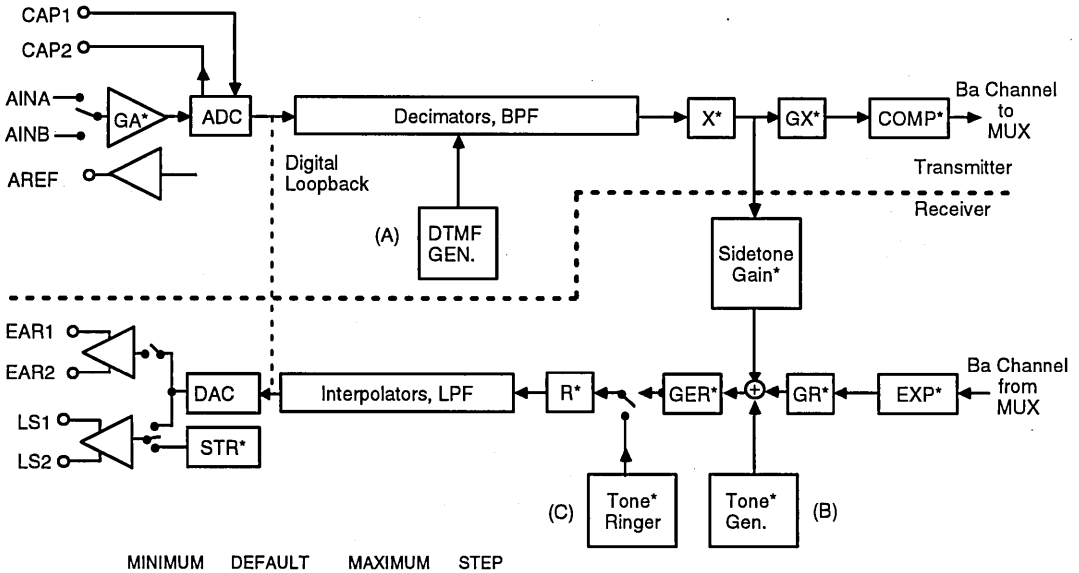
The MAP, as illustrated in Figure 3, implements audio-band analog-to-digital (ADC) and digital-to-analog (DAC) conversions together with a wide variety of audio support functions. Analog interfaces are provided for a handset earpiece, a handset mouthpiece, a microphone, and a loudspeaker. A programmable analog preamplifier is included in front of the A/D converter. The codec and filter functions are implemented using digital signal processing (DSP) techniques to provide operational stability and programmable features. There is one programmable digital gain stage in the transmit path and two in the receive path to allow precise signal level control. Sidetone attenuation is programmable, and programmable equalization filters are present in both the receive and transmit paths in order to modify the frequency response of either or both paths. Tone generation capability is included to allow generation of ringing signals, DTMF tones, and call progress signals. MAP operation is described in detail in the following sections.

Audio Inputs

The audio input port consists of two inputs (AINA and AINB) which are selectable, one at a time, by register programming. Signals applied to these inputs must be AC-coupled.

Earpiece and Loudspeaker Drivers

The earpiece and loudspeaker drivers each consist of amplifiers with differential, low-impedance outputs. The MAP receive path signal may be routed to either of these outputs, or to both outputs simultaneously. Alternatively, the MAP receive path may be routed to the EAR outputs while the Secondary Tone Ringer (STR) is routed to the LS outputs. The EAR drivers can drive loads ≥540 ohms between the EAR1 and EAR2 pins, while the LS drivers can drive loads ≥40 ohms between the LS1 and LS2 pins. The maximum capacitive-loading between EAR1 and EAR2 or between LS1 and LS2 is 100 pF. The EAR outputs are high-impedance when the MAP is disabled. The LS outputs are high impedance when both the MAP and the Secondary Tone Ringer are disabled.



	MINIMUM	DEFAULT	MAXIMUM	STEP
GX	0 dB**	0 dB	12 dB	0.5 dB
GER	−10 dB**	0 dB	18 dB	0.5 dB
GR	−12 dB**	0 dB	0 dB	0.5 dB
STG	−18 dB**	−18 dB	0 dB	0.5 dB
GA	0 dB	0 dB	24 dB	6.0 dB

09893E-004

* Programmable
**These registers can also be programmed for infinite attenuation to break the signal path if desired.

Figure 3. Main Audio Processor Block Diagram

Programmable Analog Preamplifier

A programmable analog preamplifier GA is included in front of the A/D converter, and is adjustable in 6-dB increments from 0 dB to +24 dB. The existing GX gain stage in the transmit path may be used for finer adjustment of transmit gain. This preamplifier eliminates the need for an external operational amplifier when interfacing electret-type handsets to the DSC circuit.

Signal Processing

Transmitter

The transmitter performs a series of operations as described below:

1. An ADC converts the incoming analog signal at a sampling rate of 512 kHz.
2. The Band Pass Filter and a series of decimators reject DC and 50- to 60-Hz line frequencies while reducing the sampling rate to 8 kHz.
3. The X filter is an 8-tap user-programmable filter for tuning the microphone. The default is flat with unity gain.
4. The GX filter is a programmable gain filter that allows the user to program a gain of 0 to +12 dB in 0.5-dB steps. The default value is 0 dB.
5. The μ-law or A-law digital compression algorithm converts the linear output of the GX filter to μ- or A-law code. The default algorithm is μ-law code. The MSB (sign bit) is transferred first to (or from) the MUX.

Receiver

The receiver performs a series of operations described as follows:

1. An expander converts the input A- or μ-law data to digital linear data. The most significant bit is transferred from the MUX first. The default value is μ-law.
2. The GR filter is a programmable gain filter that allows the user to program a gain of –12 to 0 dB in 0.5-dB steps. The default value of GR is 0 dB.
3. The GER and Sidetone Gain (STG) are programmable constant multipliers which allow the user to program a gain of –10 to +18 dB in 0.5-dB steps (default value 0 dB) and –18 to 0 dB in 0.5-dB steps (default value –18 dB) respectively. The GER provides volume control (for the hearing impaired) and should be programmed to 0 dB for normal operation. The sidetone gain path provides feedback from the transmitter.
4. The R filter is provided to correct for speaker attenuation distortion and is a user-programmable filter similar to the X filter in the transmitter.
5. A series of interpolators increases the sampling frequency.
6. A DAC converts the digital signal to the analog audio output signal.

Tone Generators

The MAP contains three tone generators which can be enabled via MAP Mode Register 2 Bits 2, 3, and 4. Only one of the three tone generator bits in the register can be set at a time. If more than one bit is set, all three bits are considered set to zero and tone generation is disabled. The tone generators are:

DTMF Generator

This generator provides tone injection at a sampling rate of 32 kHz into the transmit and sidetone paths (Figure 3, Block A). The DTMF frequencies generated are guaranteed to ±1.2% deviation.

Tone Generation

This generator provides call progress tones to the receive path, where it is added to the incoming speech (Figure 3, Block B).

Tone Ringer

This generator provides tone alert signals output through the receive path to the loudspeaker or earpiece (Figure 3, Block C).

To program the DTMF tone generators, two frequency values and two amplitude values must be written to the two 8-bit Frequency Tone Generator Registers (FTGR1, FTGR2) and the two 8-bit Amplitude Tone Generator Registers (ATGR1, ATGR2), respectively.

The Tone Generator and the Tone Ringer use the frequency programmed in FTGR1. The Tone Generator uses the amplitude programmed in ATGR1 while the Tone Ringer uses the amplitude programmed in ATGR2.

The FTGR codes to obtain DTMF dialing output frequencies are listed in the table below:

FTGR 1 OR 2 (HEX REG VALUE)	FREQ	FTGR 2 or 1 → 9BH	ABH	BFH	D3H
		1209	1336	1477	1633
5AH	697	1	2	3	A
63H	770	4	5	6	B
6EH	852	7	8	9	C
79H	941	*	0	#	D

The output frequency of the DTMF tone generator approximately equals :

$$\text{DTMF Frequency in Hz} = \frac{64000}{\text{integer}\,(8192/i) + 1}$$

where i is the decimal equivalent of value programmed into the FTGR register. This allows the DTMF generator to supply common dual tone call progress signals such as Busy or Dial tones.

Table 5. Tone Ringer and Tone Generator Frequency Coefficients

Frequency (Hz)	Hex Code
2666	AB
2000	81
1600	67
1333	56
1142	4A
1000	41
889	39
800	34
727	2F
667	2B
615	28
571	25
533	23
500	21
471	1F
444	1D
421	1B
400	1A
381	19
364	18
348	17
333	16
320	15

Note: These coefficients do not apply to the DTMF generator.

The ATGR registers allow the user to program a gain of –18 dB to 0 dB in 2-dB steps. Example ATGR codes to obtain amplitude gains are listed in the following table.

0 dB implies a level of +3 dBm0. The gain values are rounded off to the nearest 1 dB.

Amplitude Gain Coefficients

Gain (dB)	Hex Code
–18	37
–16	32
–14	31
–12	27
–10	22
–8	21
–6	20
–4	12
–2	11
0	10

Secondary Tone Ringer

A Secondary Tone Ringer is included, which is able to ring the phone using the LS outputs while a voice conversation is in progress on the EAR outputs. The STR is louder than the Tone Generator, and may be used with or without enabling the MAP in order to provide flexible control of system power consumption. The STR is not available if the INIT register is programmed to Idle or Power-Down Mode. The amplitude and frequency of the STR square-wave output waveform is programmable via the STRA and STRF registers, respectively. If both the LS outputs from the MAP receive path and the STR are simultaneously enabled, priority is given to the STR connection. The STR is available for both the DSC and IDC circuits. A legal value must be programmed in the STRF register before the STR is enabled.

Programmable Gain Coefficients

The GER, GR, GX, and Sidetone gain coefficients are each 16 bits in length. Two consecutive register locations correspond to one gain coefficient. The LSB is transferred first to (or from) the microprocessor. Sample coefficients for the GER filter are listed in Table 6. The gain values are rounded off to the nearest 0.1dB.

Table 6. GER Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB	Gain (dB)	Hex Code MSB	Hex Code LSB
−10.0	AA	AA	4.0	31	DD
−9.5	9B	BB	4.5	44	1F
−9.0	79	AC	5.0	43	1F
−8.5	09	9A	5.5	33	1F
−8.0	41	99	6.0	40	DD
−7.5	31	99	6.5	11	DD
−7.0	9C	DE	7.0	44	0F
−6.5	9D	EF	7.5	41	1F
−6.0	74	9C	8.0	31	1F
−5.5	54	9D	8.5	55	20
−5.0	6A	AE	9.0	10	DD
−4.5	AB	CD	9.5	42	11
−4.0	AB	DF	10.0	41	0F
−3.5	74	29	10.5	11	1F
−3.0	64	AB	11.0	60	0B
−2.5	6A	FF	11.5	00	DD
−2.0	2A	BD	12.0	42	10
−1.5	BE	EF	12.5	40	0F
−1.0	5C	CE	13.0	11	0F
−0.5	75	CD	13.4	22	10
0.0	00	99	14.0	72	00
0.5	55	4C	14.5	42	00
1.0	43	DD	15.0	21	10
1.5	33	DD	15.5	10	0F
2.0	52	EF	15.9	22	00
2.5	77	1B	16.6	11	10
3.0	55	42	16.9	00	0B
3.5	41	DD	17.5	21	00
			18.0	00	0F

Note: The coefficient 0008 provides an attenuation of infinity when GER gain is enabled.

Example coefficients for the GR, GX, and STG filters are listed in the following table. The gain values are rounded off to the nearest 0.1 dB.

GX Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
0.0	08	08
0.5	4C	B2
1.0	3D	AC
1.5	2A	E5
2.0	25	33
2.5	22	22
3.0	21	22
3.5	1F	D3
4.0	12	A2
4.5	12	1B
5.0	11	3B
5.5	0B	C3
6.0	10	F2
6.5	03	BA
7.0	02	CA
7.5	02	1D
8.0	01	5A
8.5	01	22
9.0	01	12
9.5	00	EC
10.0	00	32
10.5	00	21
11.0	00	13
11.5	00	11
12.0	00	0E

GR Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
−12.0	91	F9
−11.5	91	C5
−11.0	91	B6
−10.5	92	12
−10.0	91	A4
−9.5	92	22
−9.0	92	32
−8.5	92	FB
−8.0	92	AA
−7.5	93	27
−7.0	93	B3
−6.5	94	B3
−6.0	9F	91
−5.5	9C	EA
−5.0	9B	F9
−4.5	9A	AC
−4.0	9A	4A
−3.5	A2	22
−3.0	A2	A2
−2.5	A6	8D
−2.0	AA	A3
−1.5	B2	42
−1.0	BB	52
−0.5	CB	B2
0.0	08	08

STG Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
−18.0	8B	7C
−17.5	8B	44
−17.0	8B	35
−16.5	8B	2A
−16.0	8B	24
−15.5	8B	22
−15.0	91	23
−14.5	91	2E
−14.0	91	2A
−13.5	91	32
−13.0	91	3B
−12.5	91	4B
−12.0	91	F9
−11.5	91	C5
−11.0	91	B6
−10.5	92	12
−10.0	91	A4
−9.5	92	22
−9.0	92	32
−8.5	92	FB
−8.0	92	AA
−7.5	93	27
−7.0	93	B3
−6.5	94	B3
−6.0	9F	91
−5.5	9C	EA
−5.0	9B	F9
−4.5	9A	AC
−4.0	9A	4A
−3.5	A2	22
−3.0	A2	A2
−2.5	A6	8D
−2.0	AA	A3
−1.5	B2	42
−1.0	BB	52
−0.5	CB	B2
0.0	08	08

The coefficient 9008 provides an attenuation of infinity when GR, GX, and/or STG are enabled.

Overflow/Underflow Precautions When Using Programmable Gains

Care must be taken so that at *any* point in the signal processing path, the combination of gains and filters and/or tones does not result in a signal that is larger than full scale. Full scale is defined as the digital representation of the maximum analog signal that is allowed into the transmitter or out of the receiver with all filters and gain stages at their default (0 dB) settings (e.g., in A-Law, the transmitter full scale is $\pm 1.25\ V_P$ and the receiver full scale is $\pm 2.5\ V_P$). Likewise, it is desirable that the peak signal be kept as close to full scale as possible at any point in the signal processing path in order to minimize digital truncation effects in the A/D, D/A, and MAP DSP.

Consider the following example: STG is programmed for infinite attenuation, GR is programmed to −6 dB while GER is programmed to +12 dB, and the R filter is

programmed to exhibit a net gain of –6 dB. Assume the analog full scale out of the receiver is ± 2.5 V_P, and a full scale PCM code is possible from the MUX. After GR, the equivalent analog signal will be 2.5 / 2 = ±1.25 V_P. However, after GER the signal will be 1.25 · 4, or ± 5 V_P. Even though the R filter will have a net gain of –6 dB, the signal will be clipped after GER and distorted for PCM codes between full scale and 6 dB below full scale due to the intermediate result at the output of GER.

Be very careful when programming the tone ringers/ generators. For example, if one of the DTMF tones is programmed to 0 dB, a tone is generated that is equivalent to a ± full scale signal in the transmit path. This means no headroom is left for the other DTMF tone. Therefore, the DTMF generator should never be programmed to exceed full scale if signal quality is to be maintained. In the receive path, similar caution should be exercised in order to prevent the combination of Tone Generator, Sidetone, GR, and GER from clipping the signal.

Programmable Filter Coefficients and Equations

The frequency domain transfer function equation for the X and R filters is:

$$h_f = h_0 + h_1z^{-1} + h_2z^{-2} + h_3z^{-3} + h_4z^{-4} + h_5z^{-5} + h_6z^{-6} + h_7z^{-7}$$

where:

$z = \cos(wT) + i \cdot \sin(wT)$

$i = (-1)^{1/2}$

w = frequency of input signal in Hz · 2pi

T = sample period in seconds (0.125 ms)

hj (j = 0,1,...7) = user defined coefficients.

Each hj coefficient is defined by the following equation:

$$hj = A3\{1 + A2[1 + A1(1 + A0)]\}$$

where each hj Coefficient Register pair has the following format:

Byte	7	6 5 4	3	2 1 0
LSB	S1	M1	S0	M0
MSB	S3	M3	S2	M2

and $Ai = -1^{Si} 2^{-Mi}$, (i=0,1,2,3).

The X and R filter coefficients are programmed using a 16-byte transfer with the following format:

Byte	Value
0	h0 LSB
1	h0 MSB
2	h1 LSB
3	h1 MSB
4	h2 LSB
5	h2 MSB
6	h3 LSB
7	h3 MSB
8	h4 LSB
9	h4 MSB
10	h5 LSB
11	h5 MSB
12	h6 LSB
13	h6 MSB
14	h7 LSB
15	h7 MSB

AmMAP™ software, which calculates X and R filter coefficients, is available from Advanced Micro Devices. Contact your local AMD® Sales Office for more information.

Test Facilities

Three capabilities are provided for MAP operation verification:

MAP Analog Loopback

Signals sent in on AINA or AINB may be sent back out to EAR1/EAR2 or LS1/LS2 by looping the MAP path in the MUX. The MUX should be set up for Ba-to-Ba loopback by writing 33H to MCR1, MCR2, or MCR3. No other MUX connections overriding Ba-to-Ba should be programmed. This test allows the MAP analog and digital to be tested using a local signal source.

MAP Digital Loopback 1

This loopback mode connects the interpolator output to the decimator input, in place of the ADC output. This mode allows verification, from the S Interface or microprocessor, that the MAP digital circuitry is functional. Note that the digital patterns received after loopback will not be identical to the transmitted patterns. The D-D gain is approximately 2.5 dB.

MAP Digital Loopback 2

This loopback mode connects the analog D/A output path to the analog A/D input path, internal to the DSC circuit. The EAR and LS outputs and both AIN inputs will be disabled. This mode allows verification, from the S Interface or microprocessor, that the MAP analog and digital circuitry are functional. The digital patterns

received after loopback will not be identical to the transmitted patterns.

The bits in the MAP Mode Register define the enable/disable options for the various MAP configurations as follows:

MAP Registers

The MAP contains the following programmable registers:

MAP Register	# Bytes	Mnemonic
X-Filter Coefficient Register	16	X
R-Filter Coefficient Register	16	R
GX-Gain Coefficient Register	2	GX
GR-Gain Coefficient Register	2	GR
GER-Gain Coefficient Register	2	GER
Sidetone-Gain Coefficient Register	2	STGR
Frequency Tone Generator Register	2	FTGR
Amplitude Tone Generator Register	2	ATGR
MAP Mode Registers (3)	1	MMR
Secondary Tone Ringer Amplitude Reg.	1	STRA
Secondary Tone Ringer Frequency Reg.	1	STRF

Note: It is necessary to complete any transfers to the multi-byte MAP registers. For instance, a total of 16 bytes must be transferred to update the X filter.

Following reset, the MAP registers FTGR, MMR1, MMR2, MMR3, STRA, and STRF all default to 00 hex. All other MAP registers are not affected by reset and must be programmed by the microprocessor before being enabled. When the registers are disabled, or after reset, the MAP will have the following response:

Filter	Default Response
X Filter	Disabled (0 dB, Flat)
R Filter	Disabled (0 dB, Flat)
GX Filter	Disabled (0 dB, Gain)
GR Filter	Disabled (0 dB, Gain)
GER Filter	Disabled (0 dB, Gain)
Sidetone gain	Disabled (–18 dB, Gain)

MAP Mode Register 1 — (MMR1) — Read/Write

Address = Indirect 69H

Bit	Logical 1	Logical 0 (default mode)
0	A-Law	μ-Law
1	GX coefficient loaded from register	GX bypassed; gain = 0 dB
2	GR coefficient loaded from register	GR bypassed; gain = 0 dB
3	GER coefficient loaded from register	GER bypassed; gain = 0 dB
4	X coefficient loaded from register	X bypassed; response = flat
5	R coefficient loaded from register	R bypassed; response = flat
6	Sidetone gain coefficient loaded from register	STG gain = –18 dB*
7	Digital loopback at MAP enabled	Digital loopback at MAP disabled

*To remove the sidetone path completely, it is necessary to enable the STG function by setting MMR1 Bit 6 to 1, and program the STGR coefficient to 9008 (hex).

MAP Mode Register 2 — (MMR2) — Read/Write

Address = Indirect 6AH

Bit	Logical 1	Logical 0 (default mode)
0	AINB selected	AINA selected
1	LS1/LS2 selected	EAR1/EAR2 selected
2	DTMF enabled	DTMF disabled
3	Tone generator enabled	Tone generator disabled
4	Tone ringer enabled	Tone ringer disabled
5	High pass filter disabled	High pass filter enabled
6	ADC auto-zero function disabled	ADC auto-zero function enabled
7	Reserved, must be Logical 0	Reserved, must be Logical 0

Note: For most applications, MMR2 Bits 5 and 6 should always be written to logical 0. This enables the 50–60 Hz rejection filter and the internal offset cancellation circuits to operate normally. They can both be disabled when system or test conditions require the transmission of DC or low frequency signals.

Map Mode Register 3—(MMR3)—Read/Write

Address Indirect 6CH

Bit 7	6	5	4	3	2	1	0	Function
0	X	X	X	X	X	X	X	Bit 7 Reserved, must be written to 0
0	0	0	0	X	X	X	X	0-dB pre-amplifier gain, 1.250-V maximum peak input voltage
0	0	0	1	X	X	X	X	+6-dB pre-amplifier gain, 0.625-V maximum peak input voltage
0	0	1	0	X	X	X	X	+12-dB pre-amplifier gain, 0.312-V maximum peak input voltage
0	0	1	1	X	X	X	X	+18-dB pre-amplifier gain, 0.156-V maximum peak input voltage
0	1	0	0	X	X	X	X	+24-dB pre-amplifier gain, 0.078-V maximum peak input voltage
0	1	0	1	X	X	X	X	Reserved; undefined
0	1	1	0	X	X	X	X	Reserved; undefined
0	1	1	1	X	X	X	X	Reserved; undefined
0	X	X	X	1	X	X	X	MUTE ON, AINA and AINB inputs disabled
0	X	X	X	0	X	X	X	MUTE OFF, AINA or AINB enabled
0	X	X	X	X	1	X	X	Digital Loopback 2 enabled; D/A output looped to A/D input; EAR, LS, and AIN pin disabled
0	X	X	X	X	0	X	X	Digital Loopback 2 disabled
0	X	X	X	X	X	1	X	EAR and LS simultaneously enabled
0	X	X	X	X	X	0	X	EAR or LS enabled by MMR2 Bit 1
0	X	X	X	X	X	X	1	Secondary Tone Ringer enabled
0	X	X	X	X	X	X	0	Secondary Tone Ringer disabled

Secondary Tone Ringer Amplitude Register—(STRA)—Read/Write

Address = Indirect 6DH

Bit 7	6	5	4	3	2	1	0	Peak-to-Peak Output Voltage	Relative Output	Approximate Power into 50 Ohms
0	0	0	0	0	0	0	0	Silent		
0	0	0	1	0	0	0	0	Reserved		
0	0	1	0	0	0	0	0	Reserved		
0	0	1	1	0	0	0	0	Reserved		
0	1	0	0	0	0	0	0	Reserved		
0	1	0	1	0	0	0	0	Reserved		
0	1	1	0	0	0	0	0	0.22 V	–27 dB	0.25 mW
0	1	1	1	0	0	0	0	0.31 V	–24 dB	0.5 mW
1	0	0	0	0	0	0	0	0.44 V	–21 dB	1.0 mW
1	0	0	1	0	0	0	0	0.62 V	–18 dB	2.0 mW
1	0	1	0	0	0	0	0	0.88 V	–15 dB	4 .0 mW
1	0	1	1	0	0	0	0	1.25 V	–12 dB	8 .0 mW
1	1	0	0	0	0	0	0	1.77 V	–9 dB	16.0 mW
1	1	0	1	0	0	0	0	2.50 V	–6 dB	31.25 mW
1	1	1	0	0	0	0	0	3.53 V	–3 dB	62.5 mW
1	1	1	1	0	0	0	0	5.00 V	0 dB	125.0 mW
X	X	X	X	0	0	0	0	Bits 0–3 Reserved; must be written to 0		

Secondary Tone Ringer Frequency Register (STRF), Read/Write; Address = Indirect 6EH

STRF is a Read/Write register controlling the frequency of the secondary tone ringer. Hex codes 7F and 00 are reserved and should not be used. The coefficients are defined in the following table:

Table 7. Frequencies for Secondary Tone Ringer

Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)
3F	Reserved	3B	727.3	D8	369.2	F7	247.4
1F	Reserved	9D	716.4	6C	366.4	FB	246.2
0F	12000.0	4E	705.9	36	363.6	FD	244.9
87	9600.0	27	695.7	1B	360.9	7E	243.7
43	8000.0	13	685.7	8D	358.2	BF	242.4
A1	6857.1	09	676.1	C6	355.6	5F	241.2
D0	6000.0	04	666.7	E3	352.9	2F	240.0
E8	5333.3	82	657.5	F1	350.4	97	238.8
F4	4800.0	41	648.7	78	347.8	CB	237.6
7A	4363.6	A0	640.0	3C	345.3	65	236.5
3D	4000.0	50	631.6	9E	342.9	32	235.3
1E	3692.3	A8	623.4	CF	340.4	99	234.2
8F	3428.6	D4	615.4	E7	338.0	CC	233.0
C7	3200.0	6A	607.6	73	335.7	66	231.9
63	3000.0	B5	600.0	39	333.3	B3	230.8
B1	2823.5	DA	592.6	9C	331.0	59	229.7
58	2666.7	6D	585.4	CE	328.8	AC	228.6
2C	2526.3	B6	578.3	67	326.5	56	227.5
16	2400.0	5B	571.4	33	324.3	2B	226.4
0B	2285.7	AD	564.7	19	322.2	15	225.4
05	2181.8	D6	558.1	8C	320.0	8A	224.3
02	2087.0	6B	551.7	46	317.9	C5	223.3
01	2000.0	35	545.5	A3	315.8	62	222.2
80	1920.0	9A	539.3	D1	313.7	31	221.2
40	1846.2	4D	533.3	68	311.7	18	220.2
20	1777.8	A6	527.5	B4	309.7	0C	219.2
10	1714.3	D3	521.7	5A	307.7	06	218.2
88	1655.2	69	516.1	2D	305.7	83	217.2
C4	1600.0	34	510.6	96	303.8	C1	216.2
E2	1548.4	1A	505.3	4B	301.9	E0	215.3
71	1500.0	0D	500.0	25	300.0	70	214.3
38	1454.6	86	494.9	12	298.1	B8	213.3
1C	1411.8	C3	489.8	89	296.3	5C	212.4
8E	1371.4	E1	484.9	44	294.5	AE	211.5
47	1333.3	F0	480.0	A2	292.7	57	210.5
23	1297.3	F8	475.3	51	290.9	AB	209.6
91	1263.2	7C	470.6	28	289.2	55	208.7
48	1230.8	BE	466.0	94	287.4	AA	207.8
A4	1200.0	DF	461.5	4A	285.7	D5	206.9
D2	1170.7	6F	457.1	A5	284.0	EA	206.0
E9	1142.9	B7	452.8	52	282.4	F5	205.1
74	1116.3	DB	448.6	A9	280.7	FA	204.3
3A	1090.9	ED	444.4	54	279.1	7D	203.4
1D	1066.7	F6	440.4	2A	277.5	3E	202.5
0E	1043.5	7B	436.4	95	275.9	9F	201.7
07	1021.3	BD	432.4	CA	274.3	4F	200.8
03	1000.0	5E	428.6	E5	272.7	A7	200.0
81	979.6	AF	424.8	72	271.2	53	199.2
C0	960.0	D7	421.1	B9	269.7	29	198.4
60	941.2	EB	417.4	DC	268.2	14	197.5
30	923.1	75	413.8	EE	266.7	0A	196.7
98	905.7	BA	410.3	77	265.2	85	195.9
4C	888.9	5D	406.8	BB	263.7	42	195.1
26	872.7	2E	403.4	DD	262.3	21	194.3
93	857.1	17	400.0	6E	260.9	90	193.6
49	842.1	8B	396.7	37	259.5	C8	192.8
24	827.6	45	393.4	9B	258.1	E4	192.0
92	813.6	22	390.2	CD	256.7	F2	191.2
C9	800.0	11	387.1	E6	255.3	F9	190.5
64	786.9	08	384.0	F3	254.0	FC	189.7
B2	774.2	84	381.0	79	252.6	FE	189.0
D9	761.9	C2	378.0	BC	251.3	FF	188.2
EC	750.0	61	375.0	DE	250.0		
76	738.5	B0	372.1	EF	248.7		

Data Link Controller (DLC)

Overview

A 16 kb/s D Channel is time multiplexed within the frame structure of the S Interface. The data carried by the D Channel is encoded using the Link Access Protocol D-channel (LAPD) format shown in Figure 5. The D Channel can be used to carry either end-to-end signaling or Low speed packet data. Further information concerning LAPD protocol can be found in the CCITT recommendations. The LIU controls the multiplexing and demultiplexing of the D-channel data between the S Interface and the DLC.

The DLC performs processing of Level 1 and partial Level-2 LAPD protocol, including flag detection and generation, zero deletion and insertion, Frame Check Sequence (FCS) processing for error detection, and some addressing capability. High level protocol processing is done by the external microprocessor. The microprocessor may process the address field in the LAPD frame depending on the programmed state of the DLC. The status of the DLC is held in the status registers and relevant interrupts are generated under user program control. In addition to transmit and receive data FIFOs, the DLC contains a 16-bit pseudo-random number generator (RNG) used in the CCITT D-channel address allocation procedure.

D-Channel Processing

Random Number Generator (RNG)

The RNG is accessible by the microprocessor and operates in the following manner:

On the Low-to-High transition of the reset signal, the RNG is cleared, then started. The RNG stops when the LSB or MSB of the 16-bit counter is read by the microprocessor, or when the MSB is loaded by the microprocessor. Writing to the MSB of the counter loads this byte but does not start the RNG. The RNG starts when the LSB of the counter is loaded by the microprocessor.

Frame Abort

The DLC aborts an incoming D-channel frame when seven contiguous logical 1s are received. When this occurs, an "End of Receive Packet" interrupt is issued to the processor. DER Bit 0 is set to a logical 1 when the last byte of the aborted packet is read from the D-Channel Receive Buffer. The "Receive Abort" interrupt can be masked by setting DMR2 Bit 0 to a logical 0. With the exception of the "Packet Reception in Progress" bit, no other bits associated with packet reception are updated after a receive packet abort. The receive frame can be aborted at any time by setting INIT Bit 6 to logical 1. Similarly, the transmit frame can be aborted by setting INIT Bit 7 to a logical 1. When the transmit frame is aborted, seven consecutive 1s are transmitted on the S Interface followed by a logical 0, and DSR1 Bit 7 is set to a logical 1. Seven consecutive 1s followed by a 0 will continue to be transmitted as long as INIT Bit 7 is set to 1. DSR1 Bit 7 will be set after each sequence of seven consecutive 1s followed by 0.

Level-2 Frame Structure

The D-channel Level-2 frame structure conforms to one of the formats shown in Figure 5. All frames start and end with the flag sequence consisting of one 0 followed by six 1s followed by one 0. A packet consists of a Level-2 frame minus the flag bytes. The LSB is transmitted first for all bytes except the FCS.

The flag preceding a packet is defined as the opening flag. Therefore, the byte following an opening flag, by definition, cannot be an abort or another flag. A closing flag is defined as a flag that terminates a packet. This flag can be followed by another flag(s), interframe fill consisting of all 1s or flags, or the address field of the next packet. In the latter case, the closing flag of one packet is the opening flag of the next packet. The DLC receiver can recognize interframe fill consisting of logical 1s or flags. The DLC transmitter follows the closing flag with interframe fill consisting of all 1's (mark Idle) if DMR4 Bit 4 is set to a logical 0, or all 0's (flag Idle) if DMR4 Bit 4 is set to a logical 1. CCITT I-series D-channel access protocol specifies use of mark Idle.

When a collision is detected (mismatch of a D and E Bit), a complete frame must be retransmitted. For transfer across the S Interface, the S-interface frame structure is impressed upon the D-channel frame structure (LAPD).

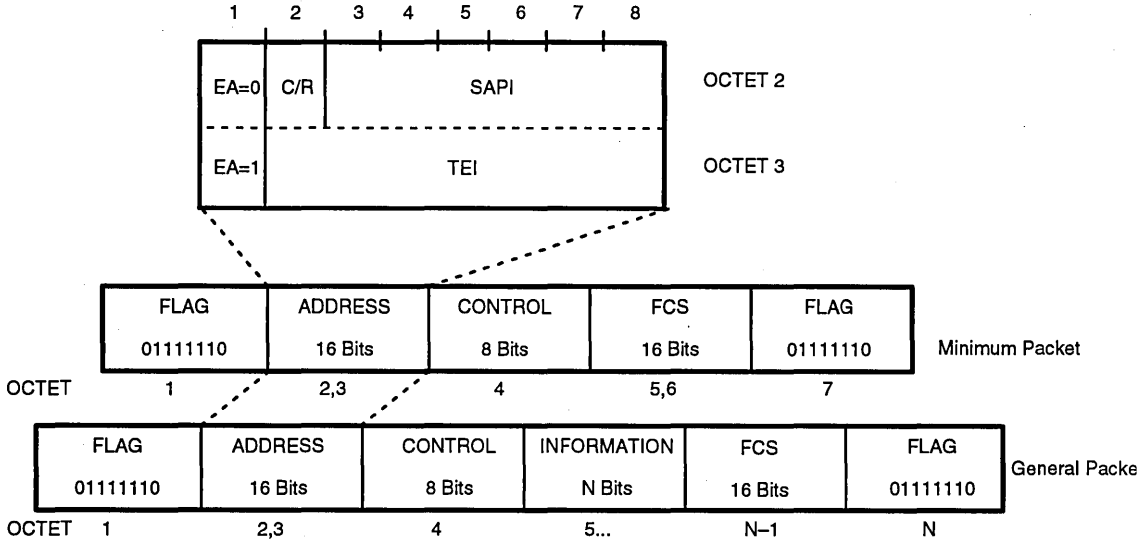
Zero Insertion/Deletion

When transmitting, the DLC examines the frame content between the opening and closing flags. To ensure that a flag sequence is not repeated within the flag boundaries of the frame, a logical 0 bit is automatically inserted after each sequence of five contiguous logical 1s. When receiving, the DLC examines the frame content between the opening and closing flags and automatically discards the first logical 0 which directly follows five contiguous logical 1s.

D-Channel Address Recognition

The address field, shown in Figure 5, allows for three types of addresses:

1. 1-byte address signified by the LSB of the first address byte being set to a logical 1
2. 2-byte address signified by the LSB of the first address byte being set to a logical 0, and the LSB of the second address byte being set to a logical 1
3. More than 2-byte address signified by the LSB of both the first and second address bytes being set to a logical 0



Notes: EA = Address Field Extension Bit
C/R = Command/Response Field Bit
SAPI = Service Access Point Identifier
TEI = Terminal Endpoint Identifier
FCS = Frame Check Sequence

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Figure 5. Level-2 Frame Structure Formats

In the case of the LAPD operating environments, the address is a 2-byte address where the first byte is analogous to the Service Access Point Identifier (SAPI) and the second byte is analogous to the Terminal Endpoint Identifier (TEI) as defined by the CCITT recommendations.

The DLC is able to recognize D-channel addresses of all of the three types outlined above. Note that only the first two bytes of a more than 2-byte address can be checked by the DLC. There are four First Received Byte Address Registers (FRARs) which hold the values used to match against the first byte of the incoming address. Similarly, there are four Second Received Byte Address Registers (SRARs) which hold the values used to match against the second byte of the incoming address.

FRAR4 defaults to FE hex; SRAR4 defaults to FF hex. This default is analogous to the broadcast address defined by the CCITT recommendations. The type of address recognition which is enabled is determined as follows:

DMR4 Bit 7	DMR4 Bit 5	DMR1 Bits 7	6	5	4		Type of address recognition
0	1	X	X	X	1	FRAR1	First received byte-only address
		X	X	1	X	FRAR2	
		X	1	X	X	FRAR3	
		1	X	X	X	FRAR4	
1	1	X	X	X	1	SRAR1	Second received byte-only address
		X	X	1	X	SRAR2	
		X	1	X	X	SRAR3	
		1	X	X	X	SRAR4	
X	0	X	X	X	1	FRAR1 : SRAR1	2-byte address
		X	X	1	X	FRAR2 : SRAR2	
		X	1	X	X	FRAR3 : SRAR3	
		1	X	X	X	FRAR4 : SRAR4	
X	X	0	0	0	0		Address recognition disabled

If DMR4 Bit 6 is set to a logical 0, Bit 1 of the FRARs is ignored when matching the first incoming address byte. If DMR4 Bit 6 is set to a logical 1, all bits of the FRARs are used when matching the first incoming address byte. FRAR Bit 1 is analogous to the C/R Bit defined by the CCITT recommendations. The address recognition mechanism for the four FRAR/SRAR addresses can be individually enabled/disabled via DMR1 bits 4–7.

First Received Byte-Only Address Recognition

If DMR4 Bit 5 is set to a logical 1 and DMR4 Bit 7 is set to a logical 0, only the first byte of the incoming address is compared with the values stored in the enabled FRARs. An interrupt is generated if there is an address match and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

Second Received Byte-Only Address Recognition

If DMR4 Bits 5 and 7 are set to a logical 1, the DLC compares only the value in the second byte of the incoming address with values stored in the enabled SRARs. An interrupt is generated if there is an address match and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

2-Byte Address Recognition

If DMR4 Bit 5 is set to a logical 0, the first byte of the incoming address is compared with the values stored in the enabled FRARs, and the second byte of the incoming address is compared with the value stored in the corresponding SRAR. An interrupt is generated if a match is found for both incoming address bytes with a FRAR/SRAR pair and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

Disabling Address Recognition

If DMR1 Bits 4, 5, 6, and 7 are all set to logical 0, all address recognition is disabled and all addresses are recognized and received. In this case, the Am79C30A/32A receives the first two bytes following the opening flag (the incoming address), and then issues an "End of Address" interrupt if the "End of Address" interrupt is enabled.

DLC Operation

DLC Transmit and Receive FIFOs

The DLC Transmit and Receive FIFOs may be configured to the Normal or Extended mode of operation. Normal mode is fully backwards compatible with the Revision D or prior DSC circuit, and is activated upon RESET or if EFCR Bit 0 is programmed to logical 0. In Normal mode the Transmit and Receive FIFOs are each eight bytes in length.

The Extended mode of FIFO operation may be activated by programming EFCR Bit 0 to a logical 1, increasing the depth of the Transmit and Receive FIFOs to 16 bytes and 32 bytes, respectively. The setting of EFCR Bit 0 to logical 1 also alters the available programmable FIFO threshold values set by DMR4 Bits 2 and 3.

Receiving D-Channel Packets

The receiver controls the flow of D-channel data to the D-Channel Receive Buffer and the termination of a receive packet. Up to two packets can be contained in the D-Channel Receive Buffer.

After receiving an opening flag (a bit sequence of 01111110) and one byte of data which is not an abort or flag on the D Channel, the DLC sets the "Packet Reception in Progress" status bit (Bit 2) in D-Channel Status Register 1 (DSR1). The DLC then receives the first two bytes (the two address bytes). If address recognition is enabled, the Am79C30A/32A issues a "Valid Address" interrupt if a match between the programmed values and the received address is detected. If no match is detected and address recognition is enabled, the DLC ignores the packet. If address recognition is disabled, the Am79C30A/32A receives the first two bytes, issues an "End of Address" interrupt, and receives the packet. Both a "Valid Address" and an "End of Address" interrupt set Interrupt Register Bit 2 to a logical 1 and Bit 0 of the D-Channel Status Register 1 (DSR1) to a logical 1. The "Valid Address/End of Address" interrupt can be disabled via DMR3 Bit 0. There is an internal 3-byte delay which holds the first of the D-channel address bytes until the interrupt has been issued. Note that the incoming address bytes cannot be read however, until the "D-Channel Receive Byte Available" or "D-Channel Receive Threshold" interrupt is set.

After the address is received, the DLC continues to receive D-channel bytes into the D-Channel Receive Buffer FIFO. The DLC issues an interrupt when data is available in the D-Channel Receive Buffer. This interrupt can be disabled by setting DMR3 Bit 3 to a logical 0. The DLC also issues an interrupt when the receive threshold set in DMR4 is reached. This interrupt can be disabled by programming a logical 0 into DMR1 Bit 1. By polling, the microprocessor can then read the D-channel bytes. The 3-byte delay incurred during address recognition is maintained. Therefore, the DLC receives the Frame Check Sequence (FCS) before issuing an interrupt to signal the last byte of the packet has been received and appropriate status bits have been updated. If DMR3 Bit 7 is set, the two FCS bytes at the end of the packet are transferred into the D-Channel Receive Buffer along with the data.

The DLC issues an interrupt when the last byte of the packet is read from the DCRB. This interrupt can be disabled by setting DMR3 Bit 2 to a logical 0.

After the FCS is received, the DLC receiver detects the closing flag (a bit sequence of 01111110) and then terminates the packet by issuing an "End Of Receive Packet" interrupt (Bit 1 of DSR1) and returns to looking for opening flags. The DLC also terminates the packet when an abort, an overflow, or overrun error condition is detected. The "End Of Receive Packet" interrupt can be disabled by setting DMR1 Bit 3 to a logical 0.

The D-Channel Receive Byte Count Register (DRCR) is a 16-bit wide, two-word deep FIFO which is used to record the number of bytes in the incoming D-channel packets. Each count is terminated by an end-of-packet condition. Thus, the DRCR informs the microprocessor of the number of bytes, including the address bytes, which have been received. The counter is updated when the last byte of a packet is placed in the D-Channel Receive Buffer. When the FCS bytes are included in the data transferred to the D-Channel Receive Buffer, the FCS bytes are included in the byte count; if the FCS bytes are not included in the transfer, they are not included in the byte count. The opening flag and closing flag are not included in the byte count.

The D-Channel Error and Address Status Registers are also double buffered. Reading the last byte of a packet causes the DER byte to propagate to the output of the FIFO and updates the D-Channel Status and Interrupt Registers accordingly. Reading the MSB of the DRCR causes the next count and associated ASR byte to propagate to the output of the FIFOs and updates the D-Channel Status and Interrupt Registers accordingly. For this reason it is important to read ASR, DER, and DSR1 prior to reading the DRCR.

When a receive error occurs, an "End-of-Packet" interrupt is generated and the packet is terminated. When the last byte of the associated packet is read from the D-Channel Receive Buffer, the appropriate DER bits are set and an error interrupt is generated. All error interrupts can be individually masked by setting the corresponding bits in DMR2 to a logical 0.

There is one 16-bit D-Channel Receive Byte Limit Register (DRLR). The received byte count is compared with the DRLR. When the byte count of the currently received D-channel packet exceeds the limit value, a receiver overflow is detected, the packet is terminated, and an "End-of-Packet" interrupt is issued. D-Channel Error Register (DER) Bit 4 is set to a logical 1 and an overflow interrupt issued when the last byte of the associated packet is read from the D-Channel Receive Buffer. The "Overflow Error" interrupt can be masked by setting DMR2 Bit 4 to a logical 0.

The minimum packet length is five bytes for a 2-byte address packet (not including flags). If the packet length is less than the above, an interrupt is issued and DER Bit 5 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer. The error interrupt can be masked by setting DMR2 Bit 5 to a logical 0.

If packet reception is in progress and the D-Channel Receive Buffer is full, the microprocessor has a maximum of 425 µs to respond to the D-Channel "Receive Data Available" interrupt. If the microprocessor fails to do so, then an overrun error occurs when the data byte is overwritten. When this happens, the packet is terminated. DER Bit 6 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer. The "Overrun Error" interrupt can be masked by setting DMR2 Bit 6 to logical 0.

Error indication is given if two packets have been received and not serviced by the user and a third packet is received via DSR2 Bit 2. When this error occurs, the third packet is terminated (not received).

Error indication is given for a receiver abort (the reception of seven contiguous 1s) by DER Bit 0.

If the number of bits received between two flags is not an integer multiple of eight (if the received packet does not contain an integral number of bytes), DER Bit 1 is set and an interrupt is generated when the last byte of the associated packet is read from the D-Channel Receive Buffer.

The incoming bit stream (including FCS) is run through the FCS generation and compare block. Upon receipt of the closing flag, the result is checked and must be (MSB first) 0001110100001111. Any other pattern indicates an FCS error, and DER Bit 3 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

The DLC receiver does not assume the packet to be byte-aligned. The architecture supports shared flags between packets, interframe fill consisting of logical 1s (Mark idle), and interframe fill consisting of flags (Flag idle). Mark idle is defined as at least 15 or more contiguous 1s. Flag idle is defined as more than two consecutive flag characters, not including a closing flag. DSR2 Bit 5 is set to a logical 1 while Mark idle is being detected. DSR2 Bit 6 is set to a logical 1 while Flag idle is being detected. The receiver D-channel packet can be aborted at any time during reception by setting INIT Bit 6.

Transmitting D-Channel Packets

The DLC Transmitter is activated as soon as the MSB (the second byte) of the 16-bit D-Channel Transmit Byte Count Register (DTCR) has been loaded by the microprocessor.

Next, the LIU starts counting the number of consecutive 1s on the E Channel until the number of 1s defined by the LIU priority mechanism is detected. After the sequence of 1s, the DLC transmitter will begin packet transmission.

Address bytes for a transmit packet can be handled in two ways: they can be loaded into the transmit buffer or loaded into the Transmit Address Register (TAR).

There is one 16-bit TAR which can be loaded by the microprocessor. The bytes loaded into the TAR are transmitted LSB first followed by MSB. For LAPD operation, the LSB contains the SAPI, and the MSB contains TEI. This 16-bit address (loaded LSB first) is transmitted within the address field of the D-channel packet if enabled by setting DMR1 Bit 2 to a logical 1. If the TAR is enabled, the DTCR should be loaded with the number of bytes to be transmitted excluding the address, flags, and FCS. If the TAR is disabled, the DTCR should be loaded with the number of bytes to be transmitted excluding the flags and FCS, and the microprocessor must load the address to be transmitted as the first two bytes of the D-channel packet data.

The DLC issues an interrupt when a position is available in the D-Channel Transmit Buffer. This interrupt can be disabled by setting DMR3 Bit 5 to a logical 0. The DLC also issues an interrupt to the microprocessor to request D-channel data bytes when the D-Channel Transmit Buffer empties to the threshold specified in the D-Channel FIFO Mode Register. This interrupt can be disabled by setting DMR1 Bit 0 to a logical 0.

If the D-Channel Transmit Buffer is empty, the microprocessor has up to 375 µs to respond to the D-channel transmit buffer interrupt. If the microprocessor fails to load the data bytes in this time frame, an underrun interrupt is generated in DER Bit 7, and packet transmission is terminated with a transmitted abort. The "Underrun" interrupt can be masked by setting DMR2 Bit 7 to a logical 0. Transmission is also terminated when a collision is detected or LIU loss of synchronization occurs.

The D-Channel Transmit Byte Count Register is decremented each time a byte of data is transferred from the D-Channel Transmit Buffer to the DLC. The count represents the number of bytes left to be transferred, excluding the FCS and flags. If the transmit abort bit (INIT Bit 7) is set, the transmit byte count is frozen and indicates the number of bytes left to transfer, not the number of bytes transmitted. The last byte of the packet is determined by the D-Channel Transmit Byte Count decrementing to zero. When this occurs, DSR2 Bit 3 is set to a logical 1.

After the last byte of the packet is transmitted, the DLC adds the FCS and closing flag. Then the DLC issues an interrupt (Bit 6 of DSR1) to signify the end of the packet transmission. This interrupt can be masked by setting DMR3 Bit 1 to a logical 0, and is reset either by reading DSR1 or when the D-Channel Transmit Byte Count Register is loaded for the next packet.

Once the D-Channel Transmit Byte Count has decremented to 0, a second packet may be loaded into the D-Channel Transmit FIFO. If the MSB of the D-Channel Transmit Byte Count Register is loaded prior to the "end-of-transmit packet" interrupt, the second packet is transmitted back-to-back with the previous packet. The "End-of-Transmit Packet" interrupt is not set between the two packets. If the MSB of the D-Channel Transmit Byte Count Register is loaded after the "end-of-packet" interrupt, the second packet is transmitted once the LIU priority mechanism has been re-satisfied.

Collision Detection

The Network Terminator echoes the transmitted D-channel data back to the DLC in the E-channel bits of the S-interface frame. If there is a difference between the data transmitted and the data echoed back, a collision has occurred. The DLC alerts the microprocessor to this event by asserting the interrupt line ($\overline{INT}$) and setting DER Bit 2. If a collision occurs during the transmission of an abort sequence, the interrupt is still issued. The collision detect interrupt can be masked by setting DMR2 Bit 2 to a logical 0.

D-Channel Receive and Transmit Errors

Non-Integer Number of Bytes

A non-integer number of bytes occurs when the number of D-channel bits received between opening and closing flags is not divisible by eight. If a received packet consists of a non-integer number of bytes, the DLC sets Bit 1 in the D-Channel Error Register (DER) to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Frame Check Sequence Error

If a received packet, including its 16-bit Frame Check Sequence, is not received perfectly, the DLC sets DER Bit 3 to a logical 1 when the last byte of the associated packet is read from the Receive Buffer.

Receive Packet Abort

If seven contiguous 1s are received while receiving a packet, the packet will be terminated. DER Bit 0 will be set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Overflow

Overflow occurs when the total number of D-channel bytes within a packet (including, only when enabled, the Frame Check Sequence bytes) exceeds the limit contained in the D-Channel Receive Byte Limit Register. (See Receiving D-Channel Packets section.) When this occurs, the DLC terminates the packet, and sets DER Bit 4 to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Underflow

If a received D-channel (including FCS) packet is less than five bytes for a 2-byte address packet, an underflow error condition occurs, and the DLC sets DER Bit 5 to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Overrun

A D-channel overrun error occurs when the receiver buffer is full, and another byte is received. This can happen if the D-Channel Receive Buffer fills, and is not read within 425 µs. When this error occurs, the DLC sets DER Bit 6 to a logical 1 and terminates the packet.

Underrun

A D-channel underrun error occurs when an empty D-channel buffer is transmitted. This can happen if the D-Channel Transmit Buffer is not loaded within 375 µs of the D-Channel "Transmit Buffer Empty" interrupt being asserted (IR Bit 0). When this error occurs, the DLC sets DER Bit 7 to a logical 1 and terminates the packet.

Receive Packet Lost

"Receive Packet Lost" occurs when two outstanding packets have been received and not serviced (the microprocessor has not read the DRCB register), and a third packet is received. When this error occurs, DSR2 Bit 2 is set to a logical 1 and the incoming packet is terminated (not received).

DLC Registers

The DLC contains the following registers:

Registers	No./Registers	Mnemonic
First Received Byte Address Registers	4	FRAR
Second Received Byte Address Registers	4	SRAR
Transmit Address Register (16-bit)	1	TAR
D-Channel Receive Byte Limit Register (16-bit)	1	DRLR
D-Channel Receive Byte Count Register (16-bit) (2-word FIFO)	1	DRCR
D-Channel Transmit Byte Count Register (16-bit)	1	DTCR
Random Number Generator Registers	2	RNGR
D-Channel Mode Registers	4	DMR
Address Status Register (2-byte FIFO)	1	ASR
Extended FIFO Control Register	1	EFCR
D-Channel Transmit Buffer Register	–	DCTB
D-Channel Receive Buffer Register	–	DCRB

There are three other read-only accessible registers associated with the DLC:

D-Channel Status Registers (DSR1 and DSR2)
D-Channel Error Register (DER) (2-byte FIFO)

Transmit Address Register—(TAR)—Read/Write
Address = Indirect 83H

This register contains the address of the packet to be transmitted if the TAR bit is enabled (DMR1 Bit 2).

First Received Byte Address Register—(FRAR1–FRAR4)—Read/Write
Address = Indirect FRAR1–FRAR3 = 81H, FRAR4 = 8CH

These registers contain the value to match against the first byte of the incoming address. If DMR1 Bits 4–7 are disabled, these registers will be ignored.

Second Received Byte Address Register—(SRAR1–SRAR4)—Read/Write
Address = Indirect SRAR1–SRAR3 = 82H, SRAR4 = 8DH

These registers contain the value to match against the first byte of the incoming address. If DMR1 Bits 4–7 are disabled, these registers will be ignored.

D-Channel Receive Byte Count Register—(DRCR)—Read
Address = Indirect 89H

This register determines the maximum number of bytes in a received packet.

D-Channel Receive Byte Limit Register—(DRLR)—Read/Write
Address = Indirect 84H

This register contains the total number of received bytes.

D-Channel Transmit Byte Count Register—(DTCR)—Read/Write
Address = Indirect 85H

This register contains the total number of transferred bytes.

Random Number Generator Register—(RNGR1, RNGR2)—Read/Write
Address = Indirect RNGR1 = 8AH, RNGR2 = 8BH

These registers control the operation of the Random Number Generator. When read, they display the random number generated by the chip.

D-Channel Transmit Buffer Register—(DCTB)—Write

D-Channel transmit FIFO.

D-Channel Receive Buffer Register—(DCRB)—Read

D-Channel receive FIFO.

D-Channel Mode Register 1—(DMR1)—Read/Write
Address = Indirect 86H

DMR1 controls the enable/disable options for the DLC. It is under sole control of the microprocessor, and does not generate any interrupts. DMR1 is defined below.

Bit	Logical 1	Logical 0
0	Enable "D-channel Transmit Threshold" interrupt (see IR Bit 0)	Disable interrupt (default value)
1	Enable "D-channel Receive Threshold" interrupt (see IR Bit 1)	Disable interrupt (default value)
2	Enable Transmit Address Register	Disable Transmit Address Register (default value)
3	Enable "End of Receive Packet" interrupt (see DSR1 Bit 1)	Disable interrupt (default value)
4	Enable FRAR1/SRAR1	Disable FRAR1/SRAR1 (default value)
5	Enable FRAR2/SRAR2	Disable FRAR2/SRAR2 (default value)
6	Enable FRAR3/SRAR3	Disable FRAR3/SRAR3 (default value)
7	Enable FRAR4/SRAR4	Disable FRAR4/SRAR4

D-Channel Mode Register 2—(DMR2)—Read/Write
Address = Indirect 87H

DMR2 is used to enable/disable the interrupts generated in the DER (see DER definition on page 41). DMR2 is controlled by the microprocessor, and does not generate interrupts. DMR2 is defined below.

Bit	Logical 1	Logical 0 (default value)
0	Enable "Receive Abort" interrupt (see DER Bit 0)	Disable interrupt
1	Enable "Non-integer Number of Bytes Received" interrupt (see DER Bit 1)	Disable interrupt
2	Enable "Collision Abort Detected" interrupt (see DER Bit 2)	Disable interrupt
3	Enable "FCS Error" interrupt (see DER Bit 3)	Disable interrupt
4	Enable "Overflow Error" interrupt (see DER Bit 4)	Disable interrupt
5	Enable "Underflow Error" interrupt (see DER Bit 5)	Disable interrupt
6	Enable "Overrun Error" interrupt (see DER Bit 6)	Disable interrupt
7	Enable "Underrun Error" interrupt (see DER Bit 7)	Disable interrupt

D-Channel Mode Register 3—(DMR3)—Read/Write
Address = Indirect 8EH

Bit	Logical 1	Logical 0
0	Enable "Valid Address/End of Address" interrupt (default value)(see DSR1 Bit 0)	Disable interrupt
1	Enable "End of Valid Transmit Packet" interrupt (default value)(see DSR1 Bit 6)	Disable interrupt
2	Enable "Last Byte of Received Packet" interrupt (see DSR2 Bit 0)	Disable interrupt (default value)
3	Enable "Receive Byte Available" interrupt (see DSR2 Bit 1)	Disable interrupt (default value)
4	Enable "Last Byte Transmitted" interrupt (see DSR2 Bit 3)	Disable interrupt (default value)
5	Enable "Transmit Buffer Available" interrupt (see DSR2 Bit 4)	Disable interrupt (default value)
6	Enable "Received Packet Lost" interrupt (see DSR2 Bit 2)	Disable interrupt (default value)
7	Enable FCS transfer to FIFO	Disable FCS transfer to FIFO (default value)

D-Channel Mode Register 4—(DMR4)—Read/Write
Address = Indirect 8FH

Bit 7 6 5 4 3 2 1 0	Control	Function
X X X X X X 0 0	Receiver Threshold	1 byte (EFCR Bit 0 = 0) 1 byte (EFCR Bit 0 = 1)
X X X X X X 0 1		2 bytes (EFCR Bit 0 = 0) 16 bytes (EFCR Bit 0 = 1)
X X X X X X 1 0		4 bytes (EFCR Bit 0 = 0) 24 bytes (EFCR Bit 0 = 1)
X X X X X X 1 1		8 bytes (EFCR Bit 0 = 0) 30 bytes (EFCR Bit 0 = 1)
X X X X 0 0 X X	Transmitter Threshold	1 byte (EFCR Bit 0 = 0) 1 byte (EFCR Bit 0 = 1)
X X X X 0 1 X X		2 bytes (EFCR Bit 0 = 0) 6 bytes (EFCR Bit 0 = 1)
X X X X 1 0 X X		4 bytes (EFCR Bit 0 = 0) 10 bytes (EFCR Bit 0 = 1)
X X X X 1 1 X X		8 bytes (EFCR Bit 0 = 0) 14 bytes (EFCR Bit 1 = 1)
X X X 0 X X X X X X X 1 X X X X	Interframe Fill	Mark Idle (default value) Flag Idle
X X 0 X X X X X 0 X 1 X X X X X 1 X 1 X X X X X	Address Recognition	2-byte (default value) First Received Byte only Second Received Byte only
X 0 X X X X X X X 1 X X X X X X	C/R Bit Compare	Disable FRAR Bit 1 compare (default value) Enable FRAR Bit 1 compare

Note: The receiver and transmitter thresholds can only be changed when the Am79C30A/32A is in Idle Mode.

Address Status Register—(ASR)—Read Only
Address = Indirect 91H

Bit	Logical 1	Logical 0 (default value)
0	FRAR1/SRAR1 address recognized	No FRAR1/SRAR1 address match
1	FRAR2/SRAR2 address recognized	No FRAR2/SRAR2 address match
2	FRAR3/SRAR3 address recognized	No FRAR3/SRAR3 address match
3	FRAR4/SRAR4 address recognized	No FRAR4/SRAR4 address match
4–7	Reserved	Reserved

D-Channel Status Register 1—(DSR1)—Read Only
DSR1 has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Valid Address (VA) if the address decode logic is enabled or End-of-Address (EOA) if the address decode logic is disabled	No valid address
1	End of receive packet	Not end of packet
2	Packet reception in progress	Packet not being received
3	Loopback in operation at Am79C30A/32A	No loopback in operation at Am79C30A/32A
4	Loopback in operation at LIU	No loopback in operation at LIU
5	D-channel back-off not in operation	D-channel back-off in operation
6	End of valid transmit packet	No end-of-transmit packet or no transmission
7	Current transmit packet has been aborted	No transmit packet abort

The DSR1 bits generate interrupts, and are set/reset under the following conditions (in addition to a hardware reset or Idle Mode):

Bit	Generate Interrupt	Bit Set	Bit Reset
0	Yes, if DMR3 Bit 0 = 1	Two bytes after an opening flag if a VA is decoded or address recognition is disabled	When the microprocessor reads DSR1 or associated DRCR
1	Yes, if DMR1 Bit 3 = 1	When a closing flag is received	When the microprocessor reads DSR1 or associated DRCR
2	No	One byte after the opening flag of any packet, valid or not	When a flag or an abort is received
3	No	When the operation is in progress	When the operation is not in progress
4	No	When the operation is in progress	When the operation is not in progress
5	No	When the operation is in progress	When the operation is not in progress
6	Yes, if DMR3 Bit 1 = 1	When the closing flag is transmitted	When the microprocessor reads DSR1 or when DTCR is loaded
7	No	When seven 1s and a 0 have been transmitted	When the microprocessor reads DSR1 or when DTCR is loaded

D-Channel Status Register 2—(DSR2)—Read Only

DSR2 has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Last byte of received packet	Not last byte of received packet
1	Receive byte available	Receive byte not available
2	Receive packet lost	Receive packet not lost
3	Last byte transmitted	Last byte not transmitted
4	Transmit buffer available	Transmit buffer not available*
5	Mark idle detected (15 or more contiguous 1s)	Mark idle not detected
6	Flag idle detected (more than two contiguous flags)	Flag idle not detected
7	Start of second received packet in FIFO	Second packet not yet in FIFO

*Following RESET, the Transmit Buffer Available (Bit 4) is set, producing a default value of 10H instead of 00H.

The DSR2 bits generate interrupts and are set/reset under the following conditions (in addition to a hardware reset or Idle Mode):

Bit	Generate Interrupt	Bit Set	Bit Reset
0	Yes, if DMR3 Bit 2 = 1	When last byte of a received packet is read from the DCRB	When the microprocessor reads the DSR2
1	Yes, if DMR3 Bit 3 = 1	When DCRB contains one or more bytes of data	When DCRB is empty
2	Yes, if DMR3 Bit 6 = 1	When two outstanding packets are received and not serviced, and a third packet is received	When the microprocessor reads DSR2
3	Yes, if DMR3 bit 4 = 1	When the last byte of a transmit packet is transferred from the DCTB	When the microprocessor reads DSR2
4	Yes, if DMR3 Bit 5 = 1	When the DCTB is available to be loaded with a data byte	When the DCTB is full
5	No	When 15 contiguous one bits have been detected in the incoming D Channel	When the first zero bit is detected on the incoming D Channel
6	No	When more than two contiguous flags are detected on the incoming D Channels not including a closing flag	When a non-flag character is detected on the incoming D Channel
7	Yes, if EFCR Bit 1 = 1	When start of second packet is in the receive FIFO	When second receive packet is not present

D-Channel Error Register—(DER)—Read Only

The DER has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Received Packet Abort	No abort received
1	Non-integer number of bytes have been received	Integer number of bytes received
2	Collision Detected	No error
3	FCS Error	No error
4	Overflow Error	No error
5	Underflow Error	No error
6	Overrun Error	No error
7	Underrun Error	No error

The DER bits generate interrupts, and are set/reset under the following conditions (in addition to a hardware reset):

Bit	Generates Interrupt	Bit Set	Bit Reset
0	Yes, if DMR2 Bit 0 = 1	When seven consecutive 1s are received within a packet (DSR1 Bit 2 = 1)	When the microprocessor reads the DER or associated DRCR
1	Yes, if DMR2 Bit 1 = 1	Upon error condition after closing flag has been received	When the microprocessor reads the DER or associated DRCR
2	Yes, if DMR2 Bit 2 = 1	See section on collision detection	When the microprocessor reads the DER or when DTCR is loaded
3	Yes, if DMR2 Bit 3 = 1	If error occurs	When the microprocessor reads the DER or associated DRCR
4	Yes, if DMR2 Bit 4 = 1	If error occurs	When the microprocessor reads the DER or associated DRCR
5	Yes, if DMR2 Bit 5 = 1	If error occurs	When the microprocessor reads the DER or associated DRCR
6	Yes, if DMR2 Bit 6 = 1	If error occurs	When the microprocessor reads the DER or associated DRCR
7	Yes, if DMR2 Bit 7 = 1	If error occurs	When the microprocessor reads the DER or when DTCR is loaded

DER Bits 0, 1, 3, 4, 5, and 6 are set when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Extended FIFO Control Register—(EFCR)—Read/Write

Address = Indirect 92H

Bit 7	6	5	4	3	2	1	0	Function
0	0	0	0	0	0	X	X	Bits 2–7 reserved, must be written to 0
0	0	0	0	0	0	0	X	"Start of Second Received Packet In FIFO" interrupt disabled
0	0	0	0	0	0	1	X	"Start of Second Received Packet In FIFO" interrupt enabled
0	0	0	0	0	0	X	0	Normal mode of FIFO operation
0	0	0	0	0	0	X	1	Extended mode of FIFO operation

Peripheral Port (PP)

Overview

The purpose of the Peripheral Port is to allow external peripherals to be connected to the DSC/IDC circuit. There are two basic modes of operation, Serial Bus Port Mode, and IOM 2 Terminal Mode. Within IOM 2 Terminal Mode, the DSC/IDC circuit may be configured as either an IOM 2 timing master or slave. The definition of the Peripheral Port pins depends on the operating mode of the port, as described in Table 8.

Serial Bus Port (SBP) Mode

The SBP Mode of operation is backwards compatible with the Revision D DSC circuit serial port, and is entered either following a device RESET or if programmed in PPCR1.

In SBP Mode, the SCLK output provides a 192-kHz 1X data clock of programmable polarity. The SBIN and SBOUT pins support three 8-bit serial data channels, designated Bd, Be, and Bf. The SFS output provides an 8-kHz serial frame sync pulse eight bit periods in width, coincident with the Bd channel. The SBP Mode timing is illustrated in Figure 6.

Following a RESET, the SCLK and SFS outputs will default to a high-impedance state, which will be maintained until any MUX connection is programmed (or until the Peripheral Port is programmed to an IOM 2 Mode). SCLK and SFS will remain in a high-impedance state if the Peripheral Port is explicitly disabled. The SCLK and SFS signals are synchronized to the received S-interface frame. If there is no S-interface frame synchronization, the SCLK and SFS signals will free-run at 192 kHz and 8 kHz respectively.

If the DSC/IDC circuit is programmed to Idle Mode, the SFS output is driven Low but SCLK continues to run. In Power-Down Mode, both the SFS and SCLK outputs are high-impedance.

IOM 2 Terminal Mode Overview

The IOM 2 Interface standard encompasses both a Linecard Mode and a Terminal Mode. The Terminal Mode was defined to provide four functions, as follows:

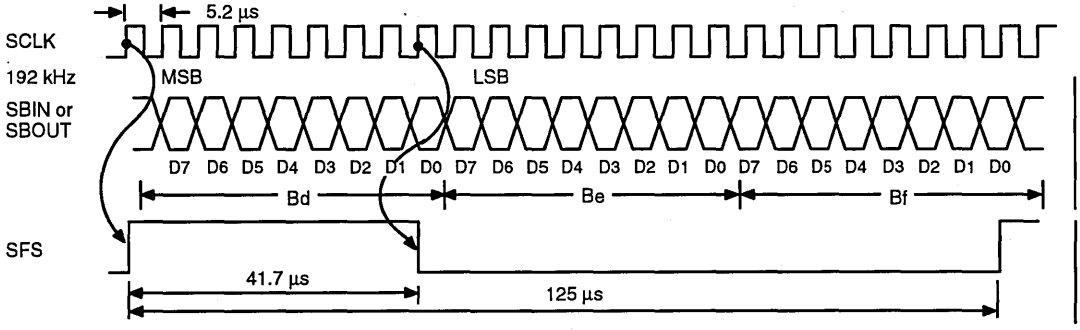
1. Connection of multiple Layer-2 devices to a Layer-1 device (in this case, the Layer-1 device is the S/T Interface LIU). Provision for the connection of non-IOM 2 devices is included.
2. Programming and control of Layer-1 or Layer-2 devices that do not have a microprocessor interface, for example, a U-interface transceiver.

Table 8. Pin Operation versus Peripheral Port Modes

Pin	SBP On	Port Disabled	IOM 2 M Activated	IOM 2 M Deactivated	IOM 2 S* Activated	IOM 2 S* Deactivated
SBIN	IN	Z	IN	IN	IN/OD	OD
SBOUT	OUT	Z	OD	Z	OD/IN	Z
SCLK	OUT	Z	OUT	Low	IN	IN
SFS	OUT	Z	OUT	Low	IN	IN
BCL/CH2STRB	OUT	Z	OUT	Low	Z	Z

IN = Input OUT = Output Z = High Impedance OD = Open Drain Output

*The Am79C30A is a non-Layer 1 component when operated in the slave mode; however, it has a microprocessor interface. As a result, it is required to change the direction of its I/O pins at certain times in order to communicate with both the upstream Layer-1 device and any downstream peripheral devices. In the IOM 2 Slave Mode, the direction of data flow is reversed with respect to the DSC circuit during Sub-frame 0 and during the deactivated state. The rule is that the upstream Layer-1 device only uses Sub-frame 0 and does not reverse its pins. Any non-Layer 1 component that does not contain a microprocessor interface (i.e., program by the DSC circuit over the Monitor Channel in Sub-frame 1) uses Sub-frame 0 to talk to the Layer-1 device and Sub-frame 1 to talk to the DSC circuit. It does not reverse its pins.



Note: SBIN is sampled on the rising edge of SCLK, SBOUT is changed on the falling edge of SCLK. 09893E–007

Figure 6. Serial Bus Port Mode Timing

3. Inter-chip communication between devices on the bus, for instance, data flow between the DSC circuit MAP and an external speech encryption device.
4. Connection of multiple DLCs to the D Channel, including access arbitration. This function is referred to as the TIC Channel and is not applicable to the DSC circuit environment.

A subset of the first three functions is implemented in the Revision E DSC circuit. The fourth, referred to as the TIC Channel, will not be implemented since it is not useful in the DSC circuit environment.

The IOM 2 Terminal Mode bus consists of three IOM 2 subframes, each containing 32 bits. This 12-byte frame is repeated at 8 kHz, resulting in an aggregate data rate of 768 kb/s. The frame structure is illustrated in Figure 7, and contains the following channels:

- Two 64-kb/s data channels, labeled B1 and B2.
- Two device programming channels, labeled Monitor 0 and 1. Each channel has an associated pair of MX and MR handshake bits that control data flow.
- One 16-kb/s D Channel for signaling and data packets.
- Two Command/Indicate channels, labeled C/I_0, and C/I_1, to provide status and command for devices connected via the monitor channels. The Command/Indicate Channel in the first IOM 2 subframe consists of four bits, providing 16 states in each direction. In the second subframe the C/I Channel is 6 bits, providing 64 states in each direction.
- Two 64-kb/s intercommunication channels, labeled IC1 and IC2, to provide additional interdevice communications bandwidth.

All data transmitted on the IOM 2 Interface via the SBOUT pin is transmitted MSB first, with the exception of D-channel data, which is transmitted LSB first. The receiver operates in a compatible way via the SBIN pin.

DSC/IDC Circuit IOM 2 Terminal Mode Implementation

Data Channels

The B1 and B2 Channels are physically the first two 8-bit time slots after the frame sync pulse. When making a MUX connection to these channels, IOM 2 Channels B1 and B2 correspond to MUX Channels Bd and Be, respectively. When in an IOM 2 Mode, a MUX connection to Channel Bf provides access to one of the two intercommunication channels, as selected in PPCR1.

Command/Indicate Channels

The Peripheral Port supports the C/I Channels of the first and second IOM 2 subframes.The Peripheral Port monitors these two channels, and generates an interrupt any time the received data changes and is stable for two frames. The received data is read from C/I Receive Data Register 0 or 1, and C/I transmit data is written to C/I Transmit Data Register 0 or 1.

D Channel

If the Peripheral Port is configured as IOM 2 master, the DLC will transmit and receive D-channel data to and from the S Interface through the LIU. The D-channel data received from the S Interface is also output on the IOM 2 Interface. D-channel data received from the IOM 2 Interface is disregarded.

If the Peripheral Port is configured as IOM 2 slave, the DLC will transmit and receive D-channel data to and from the IOM 2 Interface. The LIU is not used in this situation, so there is no D-channel data flow between the DLC and LIU.

Monitor Channels

Support for the two Monitor Channels is provided on a one-at-a-time basis. A bit in Peripheral Port Control Register 1 selects which one of the two Monitor Channels is utilized at any time.

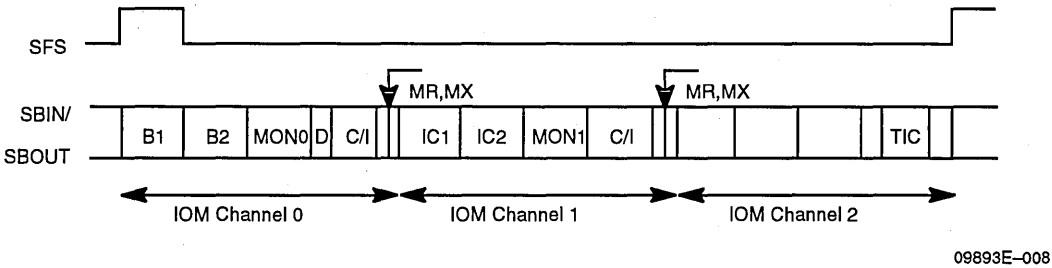


Figure 7. IOM 2 Terminal Mode Frame Structure

Monitor Channel Procedures

The Monitor Channel operates on an event-driven basis; although data transfers on the bus are synchronized to the frame sync, the flow of data is controlled by a handshake procedure using the outgoing MX and incoming MR bits. Thus, the actual data rate is not fixed, but is dependent upon the response speed of transmitter and receiver. Figure 8 illustrates the sequence of events in the monitor handshake procedure.

Idle State

The outgoing MX and incoming MR bits held inactive for two or more frames indicates that the Monitor Channel is Idle in the outgoing direction.

Start of Transmission

The PPCR1 register is programmed to select one of the two monitor channels. Data is then loaded into the monitor Transmit Data Register, causing the first data byte to be presented to the bus as well as an inactive-to-active transition of outgoing MX. The Monitor Channel transmit buffer available interrupt is also generated when data is placed on the bus, indicating that the next data byte may be written to the buffer. Outgoing MX remains active, and the data is repeated until an inactive-to-active transition of the incoming MR is received.

Subsequent Transmission

Following detection of the first inactive-to-active transition of incoming MR, all following bytes to be transmitted will be presented to the bus coincident with an active-to-inactive transition of outgoing MX. The IOM 2 specification defines a general case (Figure 8a) in which the transmitter waits for an inactive-to-active transition of incoming MR, and a maximum speed case (Figure 8c) in which the transmitter achieves a higher transmission rate by anticipating the falling edge of incoming MR.

The DSC/IDC circuit Monitor Channel transmitter implements the maximum speed case as follows: the second byte is placed onto the bus at the start of the frame following the transition of incoming MR (High to Low), and a Monitor Channel transmit buffer available interrupt is generated. Simultaneously, outgoing MX is returned inactive for one frame, then reactivated. Note that two frames of outgoing MX inactive signifies the end of a message. Outgoing MX and the data byte remain valid until incoming MR goes inactive. The next byte is transmitted during the next frame, meaning one frame after incoming MR goes inactive. In this manner, the transmitter is anticipating incoming MR returning active, which it will do one frame time after it is deactivated, unless an abort is signaled from the receiver. After the last byte of data has been transmitted, indicated by the Monitor Transmit Data Register being empty and the end-of-transmission (EOM) bit being set in PPCR1, outgoing MX is deactivated in response to incoming MR going inactive, and left inactive.

First Byte Reception

At the time the receiver sees the first byte, indicated by the inactive-to-active transition of incoming MX, outgoing MR is by definition inactive. Outgoing MR is activated in response to the activation of incoming MX, the data byte on the bus is loaded into the Monitor Receive Data Register, and a Monitor Channel receive data available interrupt is generated. Outgoing MR remains active until the next byte is received or an end-of-message is detected (incoming MX held inactive for two or more frames).

Subsequent Reception

Data is received into the buffer on each falling edge of incoming MX, and a Monitor Channel receive data available interrupt is generated. Note that the data was actually valid at the time incoming MX became inactive, one frame prior to becoming active. Outgoing MR is deactivated at the time data is read, and reactivated one frame later. The reception of data is terminated by reception of an end-of-message indication, which is incoming MX remaining inactive for two or more frames.

End-of-Transmission (EOM)

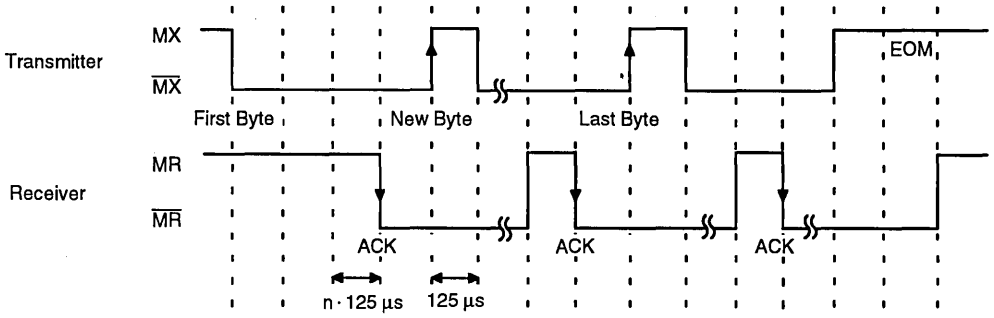
The transmitter sends an EOM in response to the EOM request bit being set in PPCR1. Once the EOM bit is set, the EOM is transmitted as soon as the Monitor Transmit Data Register becomes empty. This is normally done when the last byte of a message has been transmitted. The DSC/IDC circuit transmits an EOM simply by not reactivating MX after deactivating it in response to MR going inactive. The EOM request bit in PPCR1 is automatically cleared when the EOM has been transmitted, indicating that the monitor transmitter is available for a new message.

Abort

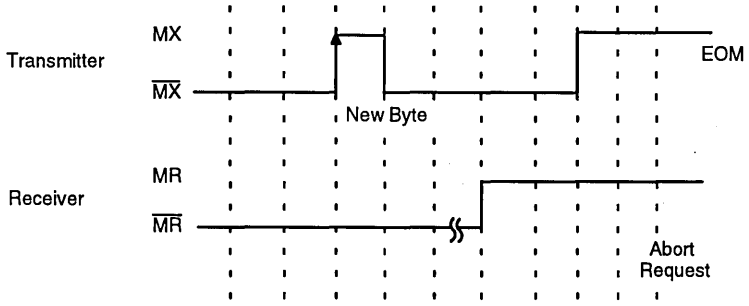
An abort is a signal from the receiver to the transmitter indicating that data has been missed. The receiver sends an abort by holding MR inactive for two or more frames in response to MX going active. An interrupt is generated when an abort is received.

Flow Control

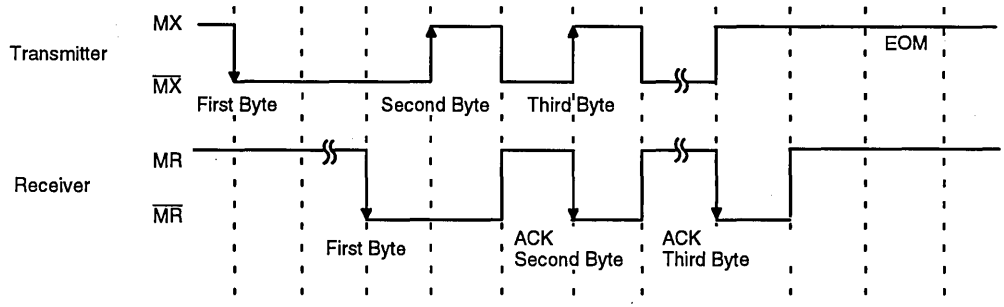
The transmitter is held off until the Monitor Receive Data Register is read, since MR is held active until the receive byte is read. The transmitter will not start the next transmission cycle until MR goes inactive.



a. General Case



b. Abort Request from the Receiver



c. Maximum Speed Case

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Figure 8. Monitor Handshake Timing

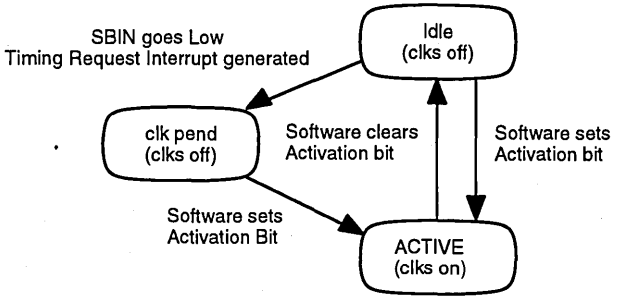
IOM 2 Activation/Deactivation

The IOM 2 Interface includes an activation/deactivation capability (see Figure 9). Activation and deactivation can be initiated from either upstream or downstream components on the bus. When deactivated, the upstream device holds all the clock outputs Low, and the downstream devices force their open drain data outputs to a High-Z state (seen as a High on the system bus due to the external pullup resistor). The activation/deactivation procedure is a combination of software handshakes via the C/I Channel, and hardware indications via the clock and data lines. The IOM 2 specification describes both the hardware and software protocols in detail; the hardware operation supported by the Am79C30A IOM 2 implementation is outlined below.

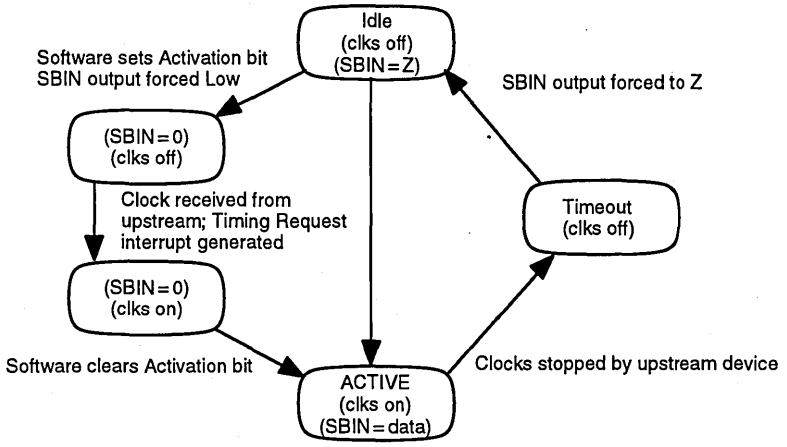
DSC/IDC Circuit as Upstream Device (Clock Master)

Deactivation

Deactivation of the IOM 2 Interface from the Am79C30A operating as an upstream device is initiated and controlled by the microprocessor. A series of software handshakes via the C/I Channel must be performed before the hardware deactivation can take place. The upstream device must issue a deactivation request command on the C/I Channel and wait for a deactivation indication from all downstream units. Once this is received, a deactivation confirmation command must be sent on the C/I Channel by the upstream device. The upstream device will then stop all clocks and hold them Low. On the Am79C30A, the IOM 2 clocks (SCLK, SFS, and BCL/CH2STRB) are stopped and forced Low



Am79C30A as Upstream Device



Am79C30A as Downstream Device

Note: This diagram shows only the portions of the IOM 2 activation/deactivation procedures that are affected by the Am79C30A hardware.The C/I-channel software handshakes are not shown.

09893E-010

Figure 9. IOM 2 Activation/Deactivation

when the microprocessor clears the activation/deactivation bit in the Peripheral Port Control Register Number 1 (PPCR1). When this bit is cleared, the data output pin (SBOUT) is also forced to High-Z (seen as a High on the system bus due to the external pullup resistor), and the Am79C30A begins monitoring the data input pin (SBIN) for the presence of a timing request from any downstream units.

Activation

Activation can be initiated locally by the processor or remotely by one of the downstream units. To activate locally, the processor sets the activation/deactivation bit in PPCR1 (starting the clocks), and then proceeds through the software activation protocol on the C/I Channel. For remote activation, the upstream device receives a request from the downstream device via the data input pin. When the data input pin (SBIN) goes Low, Am79C30A will generate an IOM 2 timing-request interrupt, Bit 6 in the Peripheral Port Status Register (PPSR). The processor must respond to this interrupt, and restart the IOM 2 clocks by setting the activation/deactivation bit in PPCR1. Once the clocks are running, the downstream device can request full activation via the C/I Channel using the IOM 2 software protocol.

DSC/IDC Circuit as a Downstream Device (Clock Slave)

Deactivation

Deactivation is normally initiated by the upstream device as described above. When the deactivation request is received by the downstream device over the C/I Channel, the processor must respond by sending the deactivation indication over the C/I Channel. The upstream device will then send the deactivation confirmation command over the C/I Channel and stop the IOM 2 clocks. The Am79C30A will detect that the clock has stopped (defined as no clock pulse received for 650 ns) and force itself to the deactivated state. In the deactivated state, SBIN, and SBOUT are both forced to a High-Z state, and the SCLK input is monitored for any rising edge that would indicate an activation request from the upstream device.

Activation

Once again, activation can originate from either the upstream or the downstream device. To activate the interface from the downstream device, the processor sets the activation/deactivation bit in the PPCR1 register. This will force the Am79C30A to pull its data output pin (SBIN in this case, since the I/O pin definition is reversed when talking to the upstream device) Low, causing the upstream device to start the IOM 2 clocks. Once the clocks are running, as indicated by SCLK input going High, the Am79C30A will generate an IOM 2 timing request interrupt (Bit 6 in PPSR). The processor must respond to the interrupt by loading the proper C/I command response into C/ITRDO, then clearing the activation/deactivation bit in PPCR1. This will release the data output pin (SBIN) from being held Low and allow the processor to complete the activation procedure by sending the proper commands over the C/I Channel.

When the activation is originated from the upstream device, the Am79C30A will generate an IOM 2 timing request interrupt (Bit 6 in PPSR) when the IOM 2 clocks become active as indicated by the SCLK input pin going High. The Am79C30A will begin normal IOM 2 transmission/reception as soon as SCLK appears; no intervention from the microprocessor is required. However, the processor must respond to the interrupt and perform the normal C/I Channel software handshakes before activation will be complete.

Peripheral Port Registers

The PP contains the following registers:

Registers	# of Registers	Mnemonic
Peripheral Port Control Register	2	PPCR1, PPCR2
Peripheral Port Status Register	1	PPSR
Peripheral Port Interrupt Enable Register	1	PPIER
Monitor Transmit Data Register	1	MTDR
Monitor Receive Data Register	1	MRDR
C/I Transmit Data Register	2	CITDR0, CITDR1
C/I Receive Data Register	2	CIRDR0, CIRDR1

Peripheral Port Control Register 1 (PPCR1) Default = 01 Hex; Address = Indirect C0 Hex, Read/Write

7	6	5	4	3	2	1	0
MONTR ABORT RQST	MONTR ENABL	MONTR CHANL SELECT	MONTR EOM RQST	IC CHANL SELECT	IOM 2 ACTV/ DEACT	PORT MODE SELECT BIT 1	PORT MODE SELECT BIT 0

Bit	Function
7	**Monitor Channel Abort Request**—This bit is automatically cleared during RESET or manually by software as follows: to send an ABORT message, software should set this bit, wait at least two frames, then clear the bit.
6	**Monitor Channel Enable**—This bit only affects IOM 2 operation. When set, the selected Monitor Channel is enabled. When cleared, both monitor channels are disabled. Whenever the Monitor Channel is disabled, the Monitor Transmit and Receive Data Register (MTDR, MRDR) are updated to their default states: MTDR = FFH, MRDR = 00H.
5	**Monitor Channel Select**—This bit only affects IOM 2 operation. When set, Monitor Channel 1 is used (second subframe). When cleared, Monitor Channel 0 is used (first subframe).
4	**Monitor End-of-Message Request**—When set, this bit forces the Monitor Channel transmitter to send an EOM once all data written into the Monitor Transmit Data Register has been transmitted. This tells the receiving device that the message is complete. The bit is cleared by hardware when the EOM is sent by reset or by software.
3	**IC Channel Select**—This bit only affects IOM 2 operation. When set, the IC2 time slot is used (sixth octet after the frame sync). When cleared, the IC1 time slot is used (fifth octet after the frame sync). The unused channel is always placed in a high-impedance state.
2	**IOM 2 Activation/Deactivation Bit**—This bit only affects IOM 2 operation. Note that this bit controls only the starting and stopping of SCLK, BCL/CH2STRB, SFS, and the state of the SBIN/SBOUT pins; this alone does not constitute activation or deactivation of the IOM 2 bus. The activation/deactivation procedure involves the exchange of a series of commands and indications over the C/I Channel. This procedure, including a state diagram, is detailed in the IOM 2 specification. IOM 2 Master Mode—This bit is set by software. When deactivated, the master will turn on SCLK, BCL/CH2STRB, and SFS clocks via software by setting this bit when the SBIN pin is pulled Low, indicating that a downstream device wishes to communicate over the interface. The IOM 2 activation/deactivation bit is cleared by software or reset. When cleared, the clocks are stopped, and SBIN is monitored for the reactivation request from the slave (SBIN held Low). [Reset defaults the Peripheral Port to SBP operation.] IOM 2 Slave Mode—This bit is set by software to initiate an activation request to the master. When set, the SBIN pin is driven Low, and held Low until the activation/deactivation bit is cleared by software. In response to SBIN going Low the master will start SCLK, which generates a timing request interrupt in the DSC circuit. The activation/ deactivation bit is cleared by software in response to this interrupt.

Peripheral Port Control Register 1 (PPCR1)—(continued)

Bit	Function
1–0	**Port Mode Select Field**—These two bits select the configuration of the Peripheral Port as follows:

Bit 1	Bit 0	Function
0	0	Port disabled
0	1	SBP Mode, enabled
1	0	IOM 2 Slave Mode, enabled
1	1	IOM 2 Master Mode, enabled

When the port is disabled, SBOUT, SBIN, and all port-related clocks are placed in a high-impedance state.

When the DSC circuit is reset, this bit field is set to 01, and the port is not enabled until a MUX MCR register is written to. If this bit is cleared prior to such a path being programmed, the port will remain disabled until the bit is set via a software write operation.

Peripheral Port Status Register (PPSR)
Default = Bit 1 = 1, Bits 6-2 and 0 = 0, Bit 7 is indeterminate; Address = Indirect C1 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	IOM-2 TIME RQST	CHNG IN C/I 1 DATA	CHNG IN C/I 0 DATA	MONTR ABORT RECVD	MONTR EOM RECVD	MONTR XMIT BUFFR AVAIL	MONTR RECV DATA AVAIL

The Peripheral Port Status Register presents various status conditions to the user, and is only used in the IOM 2 Mode. Each of these conditions can generate an interrupt to the user. The interrupts are enabled via the Peripheral Port Interrupt Enable Register. The state of the respective interrupt enable bits does not affect the setting of bits in this register. Bits 6, 3, and 2 are cleared when this register is read. Bit 1 is cleared when the Data Register is written, and Bit 0 is cleared when the Data Register is read. In addition, Bits 3, 2, 1, and 0 are cleared when the Monitor Channel is disabled (via Bit 6 of the PPCR1 Register). Because Bit 7 is reserved, the default value of this register is either 02H or 82H.

Bit	Function
6	**IOM 2 Timing Request**—When the DSC circuit is the upstream device (master mode), this bit is set by hardware to indicate that a downstream device has requested the starting of the IOM 2 clocks. The clocks are started by software. This bit does not indicate the receipt of an activation request on the C/I Channel. When the DSC circuit is the downstream component (slave mode), this bit is set in response to SCLK starting (going High) when the bus is deactivated. *Note: The DSC circuit will not exit Power-Down Mode in response to either a timing request or the clocks being started, if this interrupt is masked. It is essential that an interrupt be generated when the DSC circuit leaves Power-Down Mode. Otherwise, power consumption could increase significantly without the processor's knowledge.*
5	**Change in C/I 1 Channel Status**—This bit is set by hardware to indicate that the contents on the receive side of C/I Channel 1 have changed since the C/I Receive Data Register was last read.
4	**Change in C/I 0 Channel Status**—This bit is set by hardware to indicate that the contents on the receive side of C/I Channel 0 have changed since the C/I Receive Data Register was last read.
3	**Monitor Channel Abort Request Received**—This bit is set by hardware to indicate that an abort request has been received on the monitor channel. This indicates that the receiver on the other end of the Monitor Channel has failed to receive the transmitted data correctly, and wishes that the current transmission be discontinued, and the data transmission repeated via software.
2	**Monitor Channel End-of-Message Indication Received**—This bit is set by hardware to indicate that an EOM has been received on the monitor channel. This indicates that the message currently being received has concluded.
1	**Monitor Channel Transmit Buffer Available**—This bit is set by hardware to indicate that a new byte of data can be loaded into the Monitor Transmit Data Register.
0	**Monitor Channel Receive Data Available**—This bit is set by hardware to indicate that a byte of data has been received on the monitor channel and is available in the Monitor Receive Data Register.

Peripheral Port Interrupt Enable Register (PPIER) = 1
Default = Write = 00 Hex, Read = Bit 7 = 1, Bits 6–0 = 0; Address = Indirect C2 Hex, Read/Write

7	6	5	4	3	2	1	0
PP/MF INT EN	ENABL IOM 2 TIME RQST	ENABL CHNG IN C/I1 DATA	ENABL CHNG IN C/I0 DATA	ENABL MONTR ABORT RECVD	ENABL MONTR EOM RECVD	ENABL MONTR XMIT BUFFR AVAIL	ENABL MONTR RECV DATA AVAIL

The Peripheral Port Interrupt Enable Register provides an individual interrupt-enable bit corresponding with each of the status conditions in the Peripheral Port Status Register. When set, the interrupt is enabled. Clearing the bit disables the interrupt. These bits are set and cleared by software.

Bit	Function
7	**PP/MF Interrupt Enable**—When set, this bit enables the Peripheral Port and Multiframing interrupts. When cleared, the PP and MF interrupts are disabled. *Note: To ensure proper interrupt reporting, software must disable PP/MF interrupts when the interrupt routine is entered and enable them when exiting.*

Monitor Transmit Data Register (MTDR) Default = FF Hex; Address = Indirect C3 Hex, Write

7	6	5	4	3	2	1	0
DATA BIT 7 (MSB)	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0 (LSB)

The Monitor Transmit Data Register is the user-visible portion of the Monitor Channel Transmitter Data Buffer. Data is written into this register by the user in response to a monitor transmit buffer available interrupt. It is then transmitted to the receiver on the other side of the IOM 2 bus. The MTDR is emptied when the PP is reset.

Monitor Receive Data Register (MRDR) Default = 00 Hex; Address = Indirect C3 Hex, Read

7	6	5	4	3	2	1	0
DATA BIT 7 (MSB)	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0 (LSB)

The Monitor Receive Data Register is the user-visible portion of the Monitor Channel Receiver Data Buffer. Data is written into this register by the hardware as it is received over the monitor channel. A monitor data available interrupt is generated when the register is loaded. The register is overwritten by hardware only after the register has been read. The default on reset is 00 hex.

C/I Transmit Data Register 0 (C/ITDR0) Default = 0F Hex; Address = Indirect C4 Hex, Write

7	6	5	4	3	2	1	0
RSRVD	RSRVD	RSRVD	RSRVD	C/I0 DATA BIT 3 (MSB)	C/I0 DATA BIT 2	C/I0 DATA BIT 1	C/I0 DATA BIT 0 (LSB)

The C/I Transmit Data Register 0 is the user-visible portion of the C/I Channel 0 transmitter. Data can be written into this register by the user at any time and is transmitted continuously during each subsequent frame until changed. The register is set to its default value, 0F hex (C/I Channel idle), by reset or disabling of the Peripheral Port.

C/I Receive Data Register 0 (C/IRDR0) Default = XF Hex; Address = Indirect C4 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	RSRVD	RSRVD	RSRVD	C/I0 DATA BIT 3 (MSB)	C/I0 DATA BIT 2	C/I0 DATA BIT 1	C/I0 DATA BIT 0 (LSB)

The C/I Receive Data Register 0 contains data valid for two frames from C/I Receive Channel 0. The register is set to its default value of XF hex by a reset or the disabling of the Peripheral Port.

C/I Transmit Data Register 1 (C/I TDR1) Default = 3F Hex; Address = Indirect C5 Hex, Write

7	6	5	4	3	2	1	0
RSRVD	RSRVD	C/I1 DATA BIT 5 (MSB)	C/I1 DATA BIT 4	C/I1 DATA BIT 3	C/I1 DATA BIT 2	C/I1 DATA BIT 1	C/I1 DATA BIT 0 (LSB)

The C/I Transmit Data Register 1 is the user-visible portion of the C/I Channel 1 transmitter. Data can be written into this register by the user at any time. It is transmitted continuously during each subsequent frame until changed. The register is set to its default value, 3F hex (C/I Channel idle), by reset or disabling of the Peripheral Port.

C/I Receive Data Register 1 (C/IRDR1)
Default = Bits 7 and 6 are Indeterminate, Bits 5–0 = 1; Address = Indirect C5 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	RSRVD	C/I1 DATA BIT 5 (MSB)	C/I1 DATA BIT 4	C/I1 DATA BIT 3	C/I1 DATA BIT 2	C/I1 DATA BIT 1	C/I1 DATA BIT 0 (LSB)

The C/I Receive Data Register 1 contains the data (valid for two frames) from C/I Receive Channel 1. The register is set to its default value by a reset or the disabling of the Peripheral Port.

Peripheral Port Control Register 2 (PPCR2)
Default = Bits 7, 6, and 0 = 0, Bit 5 = 1, Bits 4–1 are Indeterminate*; Address = Indirect C8 Hex, Read/Write

7	6	5	4	3	2	1	0
REV CODE BIT 2 (MSB)	REV CODE BIT 1	REV CODE BIT 0 (LSB)	RSRVD	RSRVD	RSRVD	RSRVD	SCLK INVRT ENABL

The Peripheral Port Control Register 2 controls the inversion of the SCLK output in SBP Mode. This provides flexibility in the connection of peripheral devices to the DSC circuit. The hardware revision code is also contained in this register, which allows software to identify the revision of the hardware.

* The default value is revision-level dependent. Revision E will report a hardware revision code of 001.

Bit	Function
7–5	**Hardware Revision Code**—This read-only field reports the hardware revision level. Revision E of the DSC circuit will report a hardware revision code of 001.
0	**SCLK Inversion Enable**—When set, the SCLK output is inverted in SBP Mode. When cleared, the SCLK output is identical to the Revision D DSC circuit. This bit should not be changed while SCLK is enabled.

APPLICATIONS

ISDN Feature Phone

This basic feature phone is the ISDN equivalent to the common analog phone. The keypad can be a simple four-by-four single pole switch matrix or a larger matrix to provide full key system features. The display option illustrated in Figure 10 can be included in any of the applications shown in this section.

ISDN Feature Phone with Parallel and Serial Data Ports Plus Other Peripherals

Access to the CCITT R reference interface is provided via both the serial and parallel ports in Figure 11. This application may easily have voice capability added by using a DSC circuit in place of the IDC circuit. Figure 12 illustrates applications with increased B-channel data processing requirements.

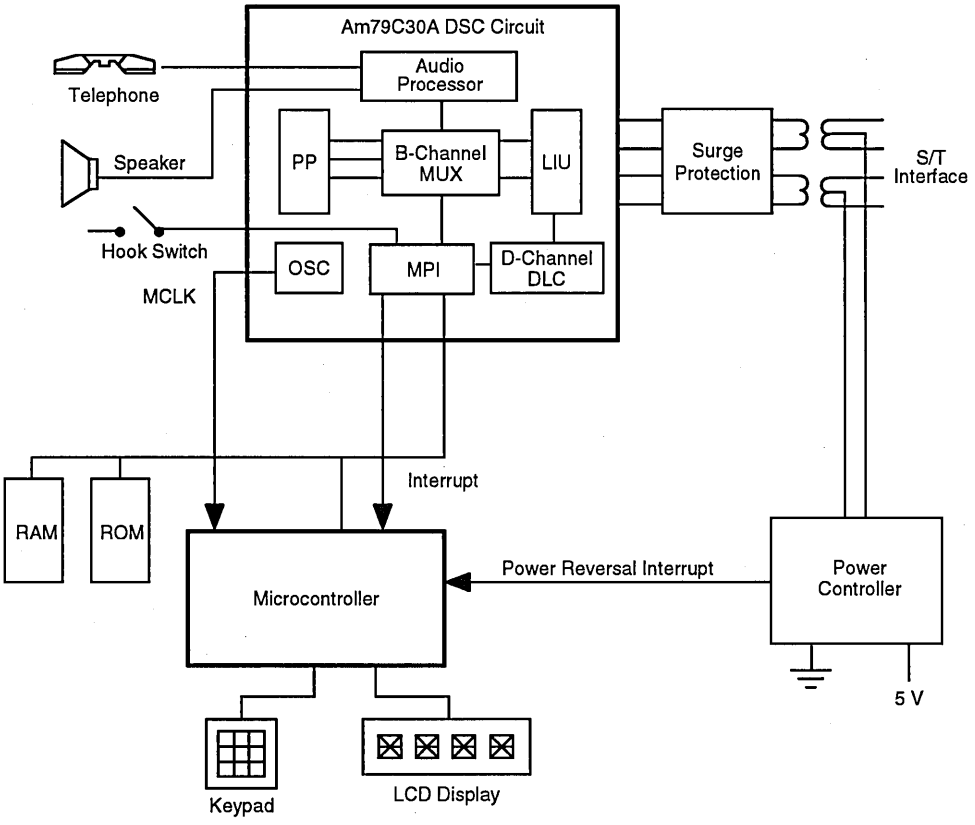


Figure 10. ISDN Telephone

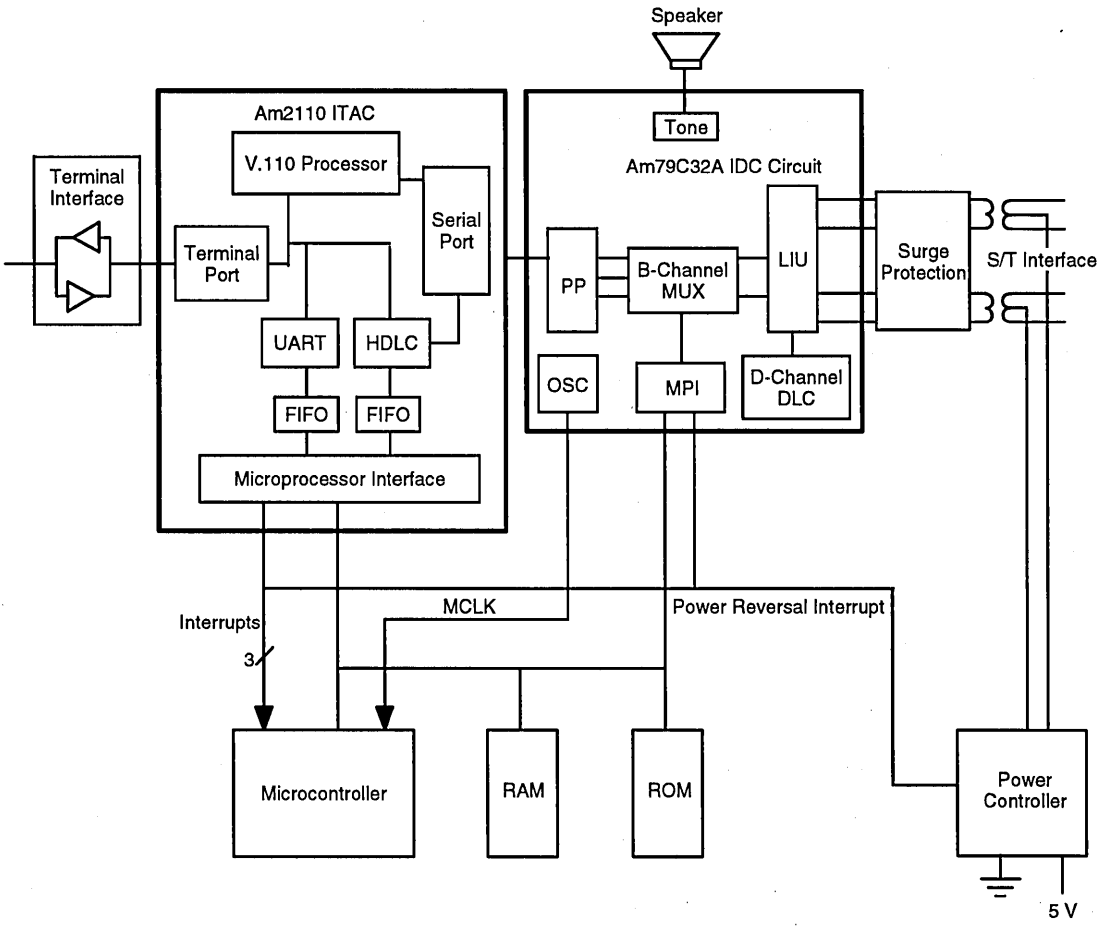
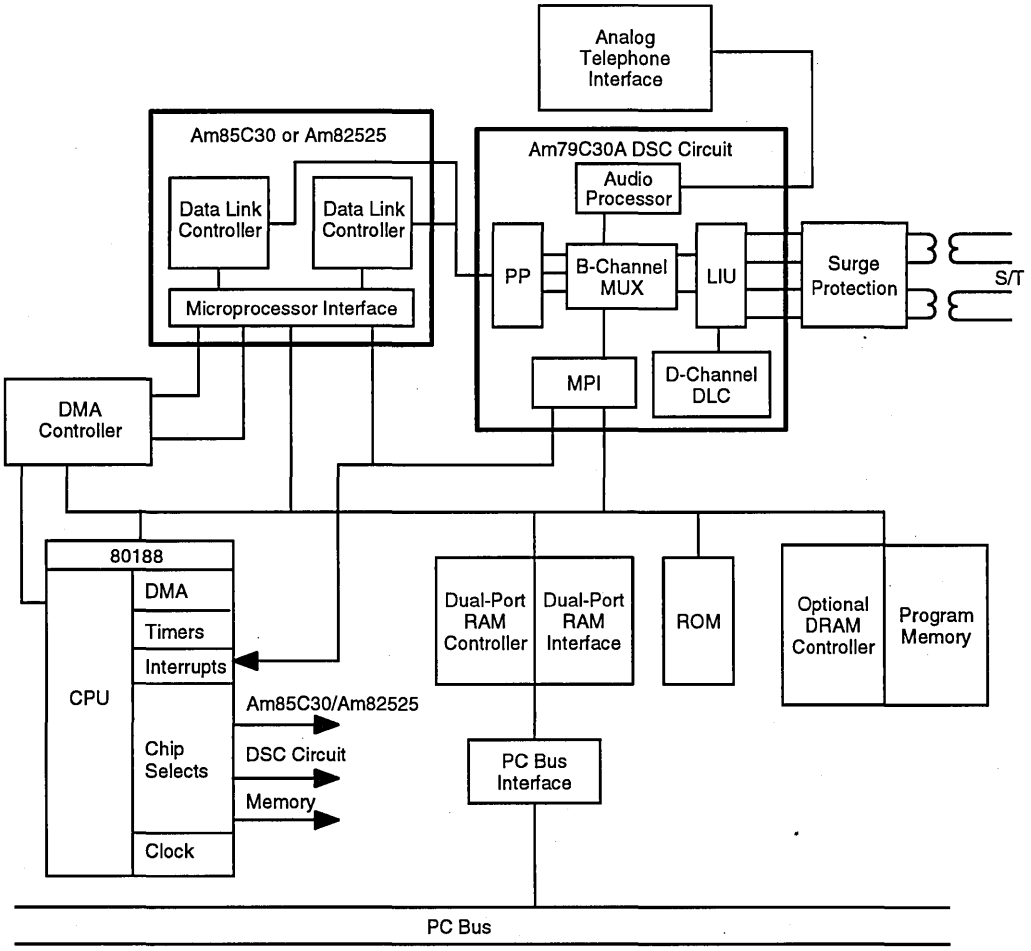


Figure 11. Terminal Adaptor (V.110/V.120) With Voice Upgrade Capability



09893E–015

Figure 12. PC Add-On-Board (1 or 2 Data Channels)

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature ..... −65°C to +150°C
Ambient temperature
with power applied ..... −55°C to +125°C
Supply voltage to ground,
potential continuous ..... 0 V to +7.0 V
Lead temperature (soldering, 10 sec) ..... 300°C
Maximum power dissipation ..... 1.5 W
Voltage from any
pin to V_{SS} ..... V_{SS} − 0.5 V to V_{CC} + 0.5 V
DC input/output current
(except LS1, LS2) ..... 10 mA
DC output current, LS1, LS2 only ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) devices
Operating V_{CC} range with respect
to V_{SS} ..... 4.75 V to 5.25 V
Ambient temperature (T_A) ..... 0°C to +70°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics over Commercial operating ranges (unless otherwise specified)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IH}	Input High Level, except XTAL2		2.0	V_{CC} + 0.25	V
V_{IH2}	Input High Level XTAL2		0.8 V_{CC}	V_{CC} + 0.25	V
V_{IL}	Input Low Level		V_{SS} − 0.25	0.8	V
V_{OL}	Output Low Level, except SBOUT Output Low Level, SBOUT only	I_{OL} = 2 mA I_{OL} = 7 mA		0.4 0.4	V
V_{OH}	Output High Level	I_{OH} = −400 µA = −10 µA	2.4 0.9 V_{CC}		V
I_{OL}	Output Leakage Current	0 < V_{OUT} < V_{CC} Output in High-Z State		±10	µA
I_{IL}	Input Leakage Current Digital Inputs LIN1/LIN2 XTAL2	0 < V_{IN} < V_{CC}		 ±10 ±200 TBD	 µA µA µA
C_I	Input Capacitance Digital Input	Temp = 25°C Freq = 1 MHz		10 (TYP)	pF
C_O	Output Capacitance Digital Input/Output	Temp = 25°C Freq = 1 MHz		15 (TYP)	pF

Table 9. Revision E Power Specifications for CCITT-Restricted Mode Phone Operation

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Typ	Preliminary Max	Unit
$I_{CC}0$	V_{CC} Supply Current (Power-Down Mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; Mode = Power-Down; Clocks & Oscillator Stopped; LIU Receiver Enabled; S Interface Silent (INFO 0)	4	5	mW
$I_{CC}1$	V_{CC} Supply Current (Idle Mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; Mode = Idle; f_{MCLK} = 384 kHz; LIU Receiver Enabled; S Interface Silent (INFO 0)	20	25	mW
$I_{CC}2$	V_{CC} Supply Current (Active; Call Set-Up)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; Mode = Active, Data Only; f_{MCLK} = 3.072 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel Only; S-interface Load = 50 ohms	80	105	mW
$I_{CC}3$	V_{CC} Supply Current (Active; Voice Mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; Mode = Active Voice & Data; f_{MCLK} = 384 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel and one B Channel; S-interface Load = 50 ohms; AINA = –15 dBm0, 1-kHz Sine Wave; EAR1/EAR2 = –15 dBm0, 1-kHz Tone Driving 600 ohms	155	190	mW
$I_{CC}4$	V_{CC} Supply Current (Active; Ringing, No Load*)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; Mode = Active, Data Only; f_{MCLK} = 384 kHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel Only; S-interface Load = 50 ohms; Secondary Tone Ringer Enabled at 0 dB, 400 Hz, No Load	125	150	mW

Note: All power measurements assume PP disabled or in IOM 2 Deactivated Mode.

*Power Consumption with the output loaded will be $I_{CC}4 + \frac{(V_{OUT}, \text{peak})}{R_{LOAD}} (V_{CC})$

For R_{LOAD} = 50 ohms and V_{OUT} = –12 dB (625 mV, peak), the maximum power consumption will be 215 mW.

AC Characteristics

V_{CC} = 5 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; MCLK = 3.072 MHz

MAP Analog Characteristics (Am79C30A Only)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Z_{IN}	Analog Input Impedance AINA or AINB to AREF	–1.25 V < V_{IN} < +1.25 V f_{IN} < 4 kHz	200			Kohm
V_{IOS}	Allowable Offset Voltage at AINA or AINB	with respect to AREF pin	–5		+5	mV
L_{LS}	Allowable Load LS1 to LS2			R_{LOAD} > 40 ohms and C_{LOAD} < 100 pF		
L_{EAR}	Allowable Load EAR1 to EAR2			R_{LOAD} > 540 ohms and C_{LOAD} < 100 pF		
L_{AREF}	Allowable Load AREF to V_{SS} or V_{CC}			R_{LOAD} > 1 Kohm and C_{LOAD} < 100 pF		
V_{AREF}	Analog Reference Voltage		2.25	2.4	2.55	V

MAP Transmission Characteristics (Am79C30A only)

The half channel parameters are specified from AINA or AINB input pins to a B Channel for the transmit path, and from a B Channel to EAR1/EAR2 or LS1/LS2 pins measured differentially for the receive path. The parameters are applicable for both A- or μ-law conversion. (A-law assumes psophometric filtering, and μ-law assumes c-message weighting.) All parameters are specified with the GR, X, R, GX, and GER filters disabled; STG filter is enabled but is programmed for infinite attenuation.

All limits are guaranteed for V_{CC} = 5 V ±5%, T_A = 0°C to 70°C, and programmable filters/gains disabled (0 dB, flat) unless otherwise indicated.

MAP Transmission Characteristics (Am79C30A Only)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
TXG1	Transmit Absolute Gain (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C	−0.30		+0.30	dB
TXG2	Transmit Gain Variation vs Temperature and V_{CC}	0 dBm0; 1020 Hz	−0.25		+0.25	dB
TXG3	Transmit Gain Variation vs Programmed Gain in GX	0 dBm0; 1020 Hz	−0.15		+0.15	dB
TXG4	Transmit Gain Variation vs Programmed Gain in GA	0 dBm0; 1020 Hz	−0.25		+0.25	dB
RXG1E	Receive Absolute Gain at EAR1/EAR2 (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C; R_{LOAD} > 540 ohms	−0.30		+0.30	dB
RXG1L	Receive Absolute Gain at LS1/LS2 (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C; R_{LOAD} > 40 ohms	−0.50		+0.50	dB
RXG2	Receive Gain Variation vs Temperature and V_{CC}	0 dBm0; 1020 Hz	−0.25		+0.25	dB
RXG3	Receive Gain Variation vs Programmed Gain in GR and GER	0 dBm0; 1020 Hz	−0.25		+0.25	dB
TXF	Transmit Frequency Response (Attenuation vs Frequency Relative to −10 dBm0 at 1020 Hz)—see Figure 13	*50 Hz–60 Hz < 300 Hz 0.3 kHz–3.0 kHz 3.0 kHz–3.4 kHz 3.4 kHz–3.6 kHz 3.6 kHz–3.9 kHz 3.9 kHz–4.0 kHz	24.0 −0.25 −0.25 −0.25 −0.25 0.0 9.0		 +0.25 +0.9	dB dB dB dB dB dB dB
RXF	Receive Frequency Response (Attenuation vs Frequency Relative to −10 dBm0 at 1020 Hz)—see Figure 17	< 300 Hz 0.3 kHz–3.0 kHz 3.0 kHz–3.4 kHz 3.4 kHz–3.6 kHz 3.6 kHz–3.9 kHz 3.9 kHz–4.0 kHz	−0.25 −0.25 −0.25 −0.25 0.0 9.0		 +0.25 +0.9	dB dB dB dB dB dB
TXD	Transmit Group Delay Variation vs Frequency at −10 dBm0 Relative to Minimum Delay Frequency—see Figure 14	500 Hz–600 Hz 600 Hz–1000 Hz 1.0 kHz–2.6 kHz 2.6 kHz–2.8 kHz			750 380 130 750	μs μs μs μs
RXD	Receive Group Delay Variation vs Frequency at −10 dBm0 Relative to Minimum Delay Frequency—see Figure 18	500 Hz–600 Hz 600 Hz–1000 Hz 1.0 kHz–2.6 kHz 2.6 kHz–2.8 kHz			750 380 130 750	μs μs μs μs
TXSTD	Transmit Signal/Total Distortion vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0dB)—see Figure 16	0 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 29.0 24.0			dB dB dB
RXSTD	Receive Signal/Total Distortion vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0dB)—see Figure 20	0 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 29.0 24.0			dB dB dB

*Measured with the high pass filter and auto-zero enabled in MMR2.

MAP Transmission Characteristics (Am79C30A Only)—(continued)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
TXGT	Transmit Gain Tracking vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0 dB)—see Figure 15	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.3 −0.6 −1.6		+0.3 +0.6 +1.6	dB dB dB
RXGT	Receive Gain Tracking vs Level; CCITT Method 2, 1020 Hz (Receive Gain = 0 dB)—see Figure 19	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.3 −0.6 −1.6		+0.3 +0.6 +1.6	dB dB dB
TXICN	Transmit Idle Channel Noise AINA or AINB Connected to AREF	GX = 0 dB, GA = 0 dB GX = 6 dB, GA = 0 dB GX = 6 dB, GA = 6 dB GX = 6 dB, GA = 12 dB GX = 6 dB, GA = 18 dB		−82 −79 −76 −73 −70	−78 −75 −72 −69 −66	dBm0 dBm0 dBm0 dBm0 dBm0
RXICN	Receive Idle Channel Noise	GR = 0 dB, GER = 0 dB GR = −12 dB, GER = 0 dB		−90 −80	−85 −75	dBm0 dBm0

*Measured with the high pass filter and auto-zero enabled in MMR2.

Notes: The following test conditions apply to all MAP tests:

1. An external 1-Kohm ±5% resistor and 2200-pF ±10% capacitor are connected in series between the CAP1 and CAP2 pins for all transmit tests.
2. All tests are half-channel with the sidetone path enabled but programmed for infinite attenuation (STG = 9008 hex).
3. Transmit specs are guaranteed for both AINA and AINB inputs with the auto-zero and high-pass filters enabled in MMR2.
4. Transmit specs are tested and guaranteed with the input signal source referenced to AREF; see test circuit below.
5. Receive specs are guaranteed for both EAR1/EAR2 and LS1/LS2 outputs measured differentially. Some degradation in performance may occur if used single ended rather than differential.

Transmitter 0-dB Reference Point:

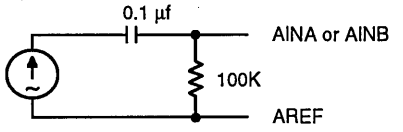
Nominal input voltage at AINA or AINB will produce a 0-dBm, 1-kHz digital code at the transmit output with all transmit gains at 0 dB.

A law = 625 mV rms
μ law = 620 mV rms

Receiver 0-dB Reference Point:

Nominal output voltage between EAR1/EAR2 or LS1/LS2 resulting from a 0-dBm, 1-kHz digital code at the receive input with all receive gains at 0 dB.

A law = 1.25 V rms
μ law = 1.2 V rms



Transmit Test Circuit with Input Source Referenced to AREF

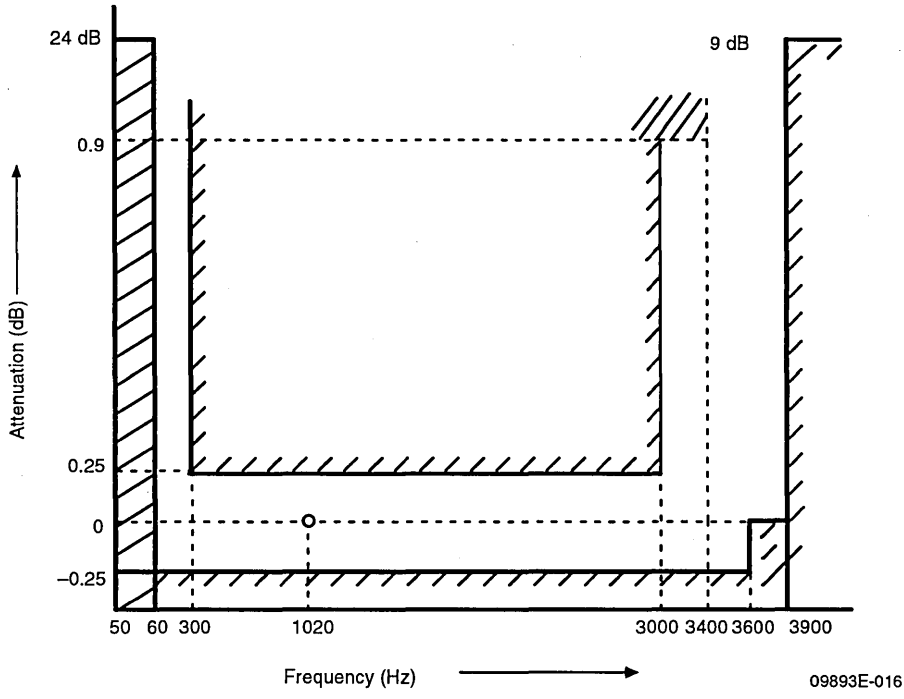


Figure 13. Attenuation/Frequency Distortion (Transmit)

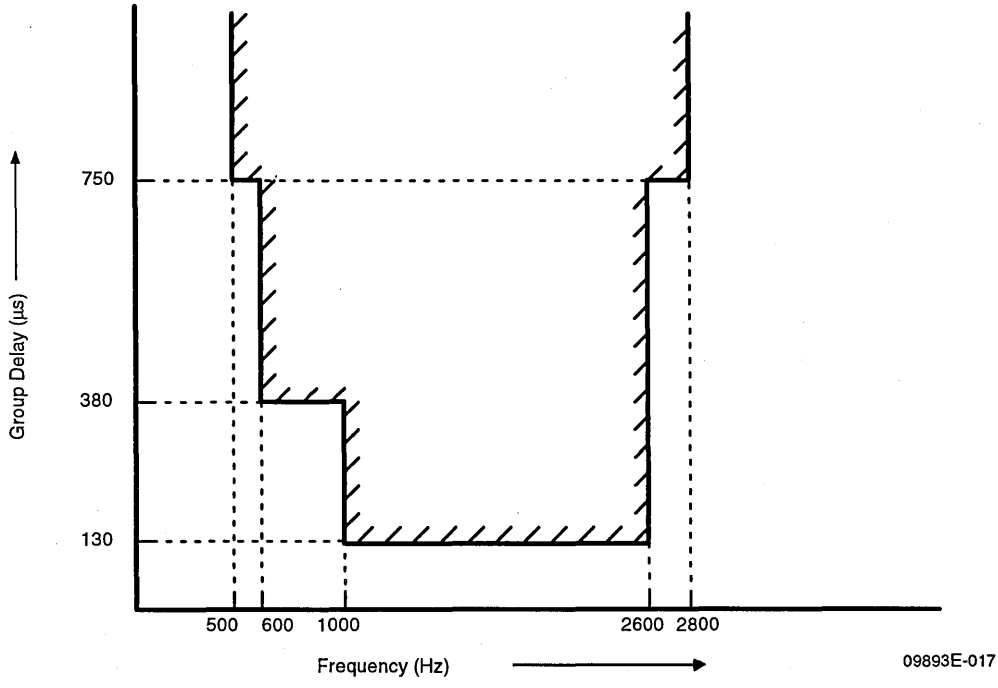


Figure 14. Group Delay Variation with Frequency (Transmit)

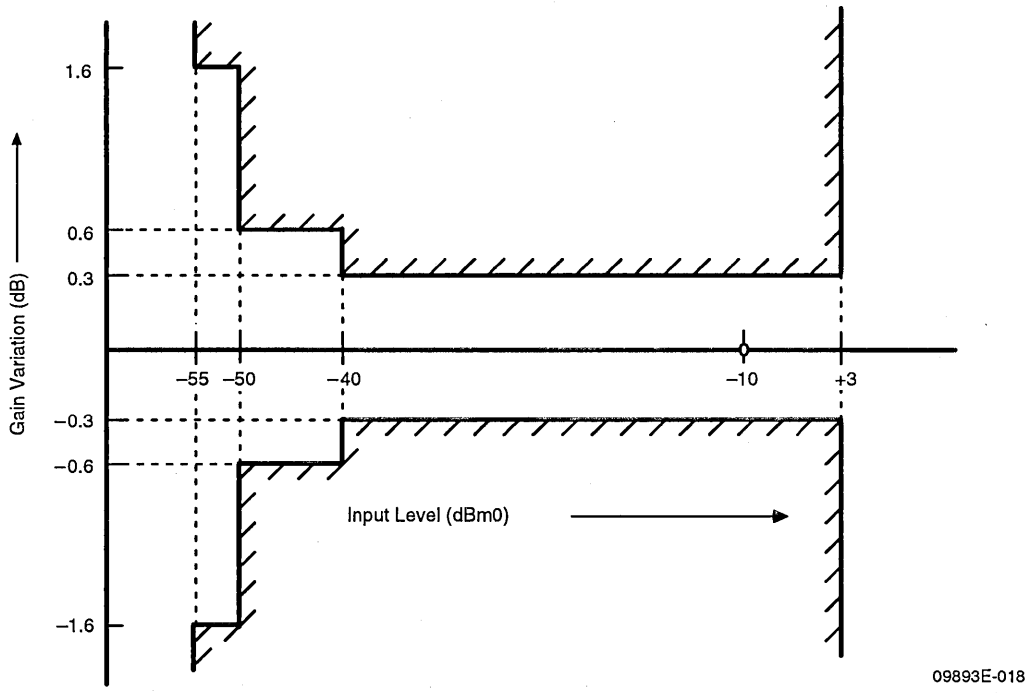


Figure 15. Gain Tracking Error (Transmit) (CCITT Method 2 at 1020 Hz)

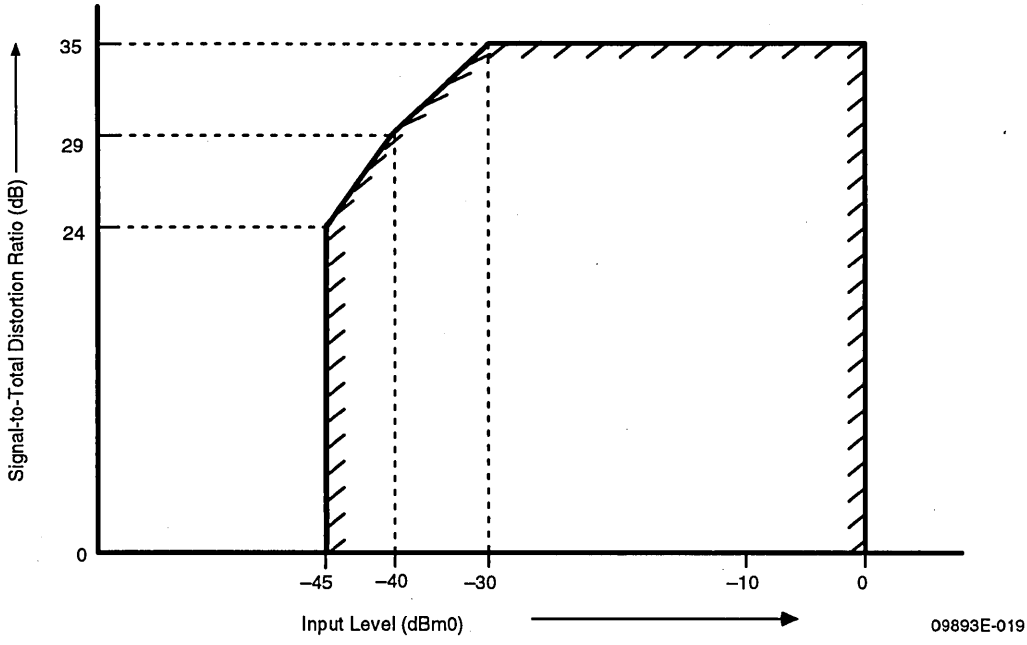


Figure 16. Signal-to-Total Distortion Ratio (Transmit) (CCITT Method 2 at 1020 Hz)

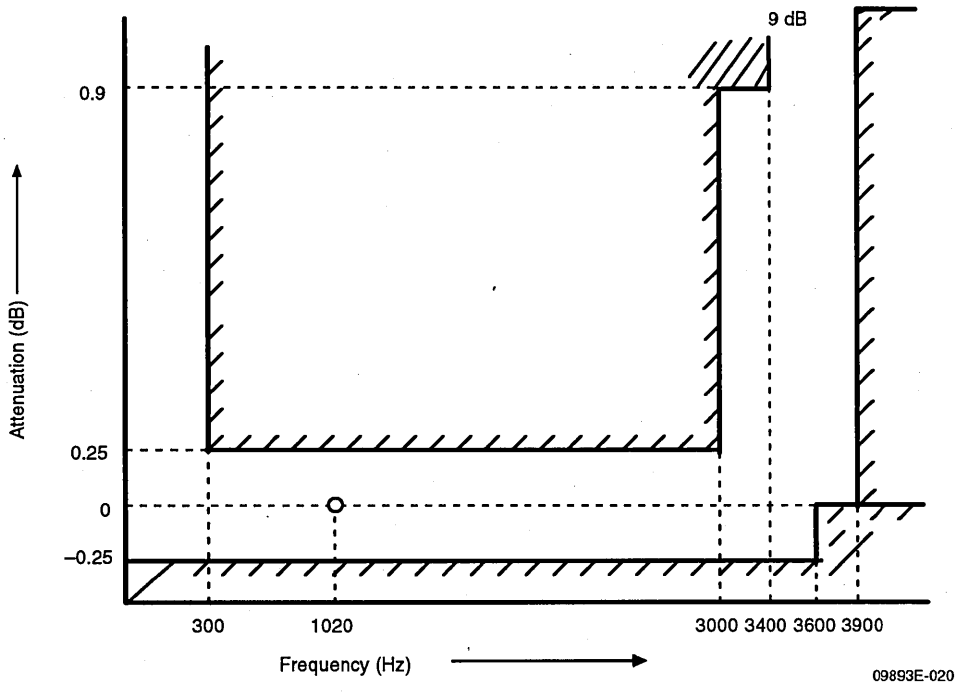


Figure 17. Attenuation/Frequency Distortion (Receive)

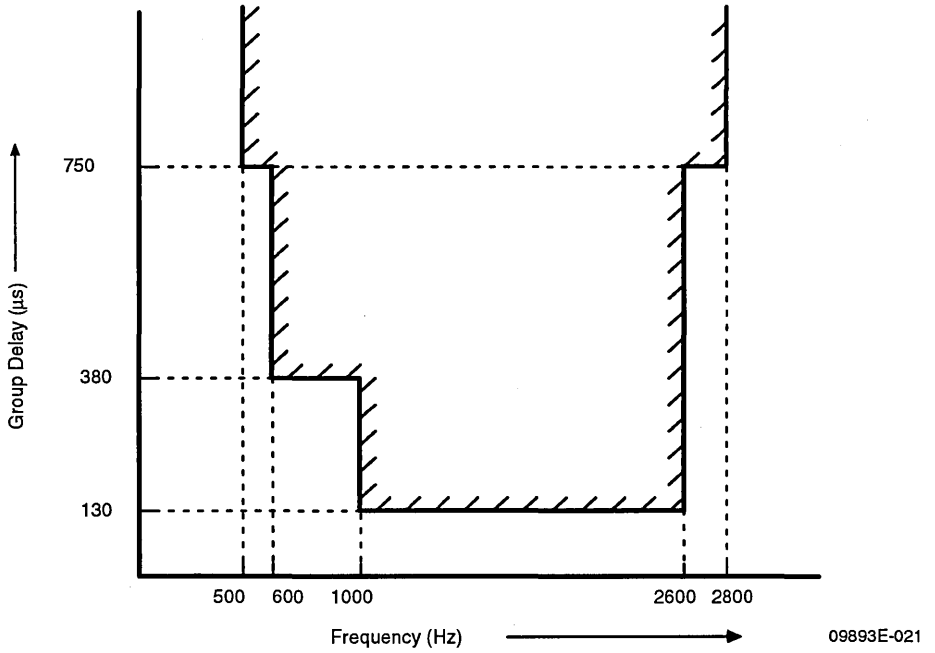


Figure 18. Group Delay Variation with Frequency (Receive)

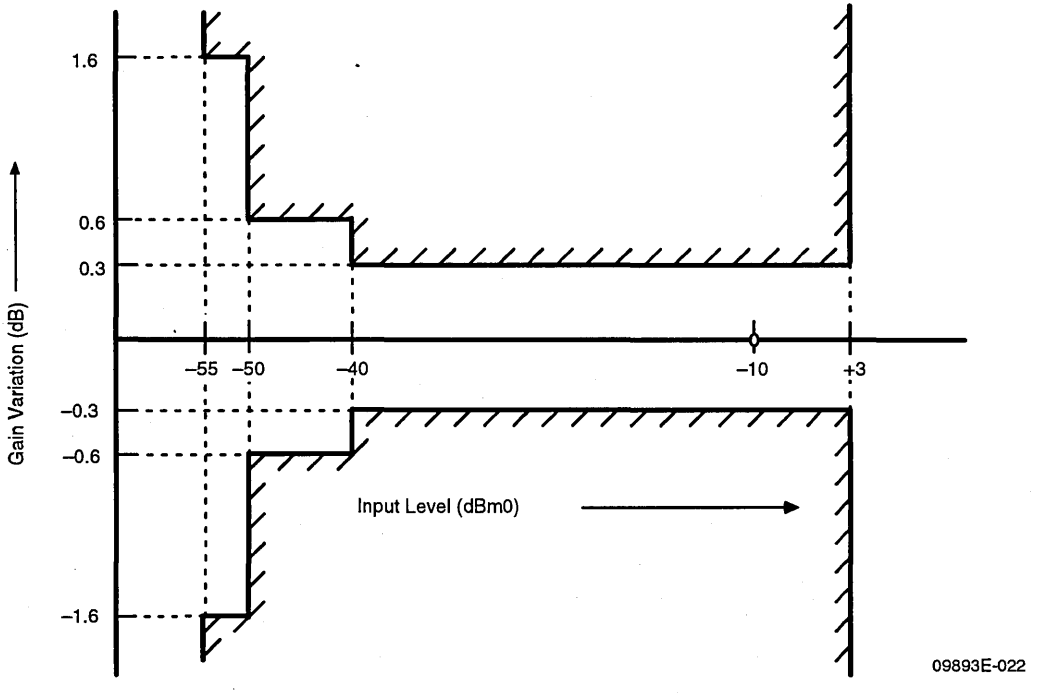


Figure 19. Gain Tracking Error (Receive) (CCITT Method 2 at 1020 Hz)

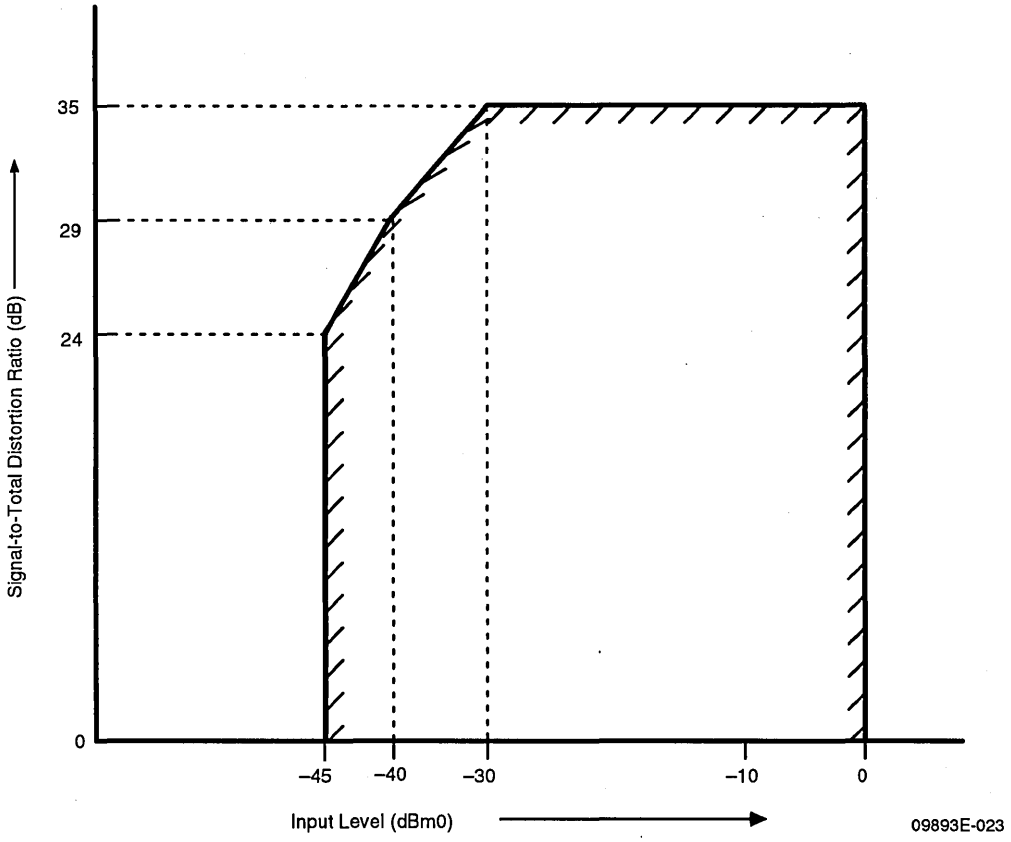


Figure 20. Signal to Total Distortion Ratio (Receive) (CCITT Method 2 at 1020 Hz)

LIU Characteristics

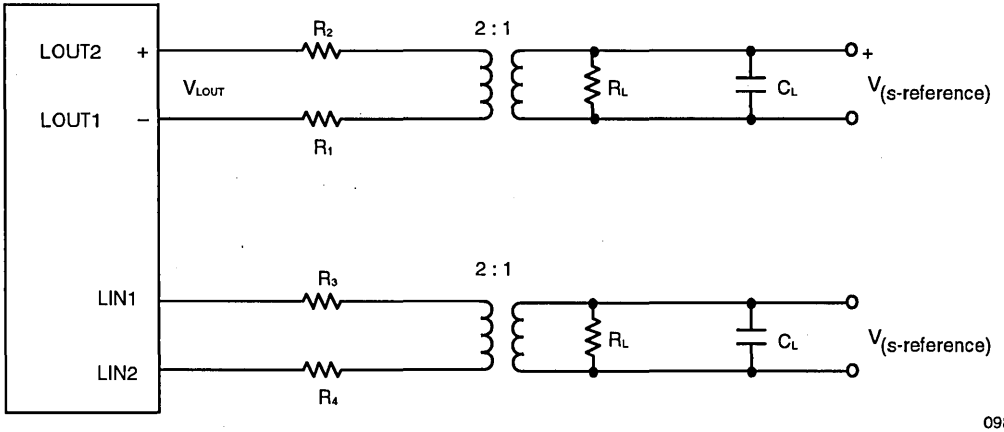
All of the parameters below are measured at the chip terminals and are consistent with 2:1 transformers.

Parameter Symbol	Parameter Descriptions	Preliminary			Unit
		Min	Typ	Max	
V_{LOUT}	Output mark amplitude measured between LOUT2 and LOUT1 (Note 1)	2.210	2.326	2.442	V
V_{LIN}	Receivable input level measured between LIN2 and LIN1, with noise added as specified by CCITT I.430 section 8.6.2.1 (Note 2)	530		1800	mV
Z_{OUT}	Output impedance measured between LOUT2 and LOUT1 spacing condition	20			Kohm
Z_{IN}	Input impedance measured between LIN2 and LIN1	20			Kohm
J	Timing extraction jitter on LOUT	−7		+7	%
PD	Total phase deviation (LOUT with respect to LIN)	−7		+15	%
PU	Pulse unbalanced measured between LOUT2 and LOUT1 (Note 1)	−5		+5	%
PW	Output pulse width measured between LOUT2 and LOUT1 (Note 1)	4.7	5.2	5.7	µs

Note 1. See the equivalent test load circuit and pulse template in Figures 22 and 23.

Note 2. The 530-mV receive input level is equivalent to 9.0 dB of attenuation from a nominal transmit level when measured at the LIN pins. Allowing 0.5-dB loss in the isolation transformer, and 1.0-dB loss in the input isolation resistors, this level will guarantee compliance to the CCITT receiver sensitivity spec of 7.5 dB when measured at the S reference point.

Note 3. Typical receiver performance is 220 mV.



$V_{(S\text{-interface})}$: Transmitter output at the S-interface reference point.
R_L is the termination impedance at the S Interface.
C_L is the effective capacitance at the S Interface.
R_1 and R_2 are the transmitter output series resistors; their value depends upon the characteristics of the pulse transformer (see equations below).
R_3 and R_4 are required for multipoint operation to prevent loading of the line when power is removed from the terminal.

Figure 21. System Interface to LIU

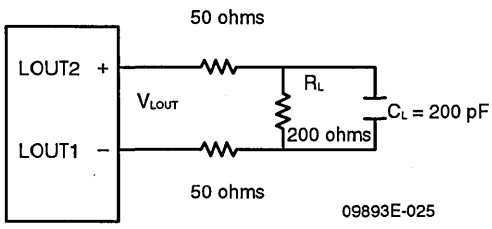


Figure 22. Equivalent Test Load Conditions

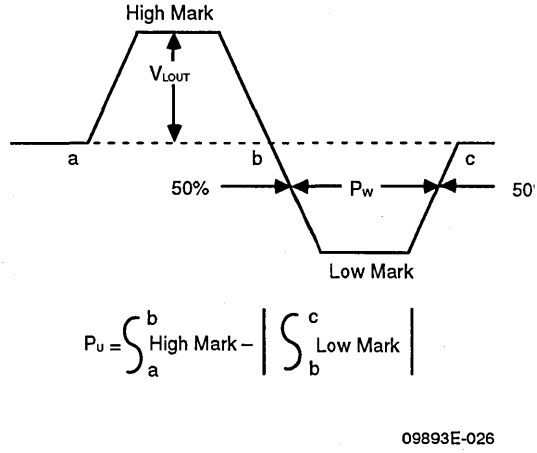
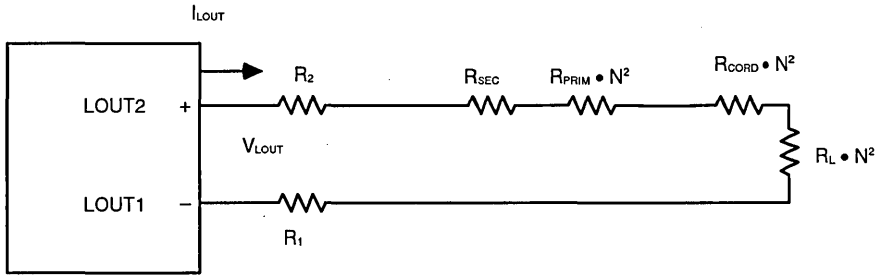


Figure 23. Differential Output Signals Between LOUT2, and LOUT1 (Using the Test Circuit in Figure 23)



R_{SEC} is the DC impedance of the transformer secondary (IC side of transformer).
R_{PRIM} is the DC impedance of the transformer primary (line side of transformer).
R_{CORD} is the DC impedance of the TE connecting cord; typically 4–6 ohms.
N is the transformer turns ratio (N = 2 for Am79C30A/32A).
R_L is the S-interface line impedance (50 ohms).
I_{LOUT} is the desired load current for the CCITT transmission templates (7.5 mA for 50-ohm line).
V_{LOUT} is the nominal output voltage from the DSC/IDC line driver.

09893E-027

Figure 24. Equivalent DC Circuit at LOUT Pins for calculation of R_1 and R_2

Series Resistor Calculations

$$I_{LOUT} = \frac{V_{LOUT}}{R_1 + R_2 + R_{SEC} + (R_{PRIM} \bullet N^2) + (R_L \bullet N^2) + (R_{CORD} \bullet N^2)}$$

$$R_1 + R_2 = \frac{(V_{LOUT})}{(I_{LOUT})} - R_{SEC} - (R_{PRIM} \bullet N^2) - (R_L \bullet N^2) - (R_{CORD} \bullet N^2)$$

Let $R_1 = R_2$

$$R_1 = R_2 = \frac{1}{2}\left\{ \frac{V_{LOUT}}{I_{LOUT}} - R_{SEC} - (R_{PRIM} \bullet N^2) - (R_L \bullet N^2) - (R_{CORD} \bullet N^2) \right\}$$

N = 2
R_L = 50 ohms
V_{LOUT} = 2.326 V
I_{LOUT} = 7.5 mA

$$R_1 = R_2 = 55.067 - 1/2\ \{ R_{SEC} + (4 \bullet R_{PRIM}) + (4 \bullet R_{CORD}) \}$$

This equation should be used to determine the value of R_1 and R_2 for the particular transformer used by each customer.

Microprocessor Read/Write Timing

Microprocessor Read Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{RLRH}	$\overline{RD}$ Pulse Width	200		ns
t_{RHRL}	Read Recovery Time (Notes 1, 2)	200		ns
t_{AVRL}	Address Valid to $\overline{RD}$ Low	20		ns
t_{AHRH}	Address Hold After $\overline{RD}$ High	10		ns
t_{RHCH}	$\overline{RD}$ High to $\overline{CS}$ High (Note 7)	0		ns
t_{RACC}	Read Access Time (Note 3)		80	ns
t_{RHDZ}	$\overline{RD}$ High to Data Hi-Z		50	ns
t_{RDCS}	$\overline{RD}$ Low to $\overline{CS}$ Low (Note 4)		30	ns

Microprocessor Write Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{WLWH}	$\overline{WR}$ Pulse Width	200		ns
t_{WHWL}	Write Recovery Time (Note 1)	200		ns
t_{AVWL}	Address Valid to $\overline{WR}$ Low	20		ns
t_{AHWH}	Addess Hold After $\overline{WR}$ High (Note 8)	10		ns
t_{WHCH}	$\overline{WR}$ High to $\overline{CS}$ High (Note 7)	0		ns
t_{DSWH}	Data Setup to $\overline{WR}$ High	100		ns
t_{DHWH}	Data Hold After $\overline{WR}$ High	10		ns
t_{WRCS}	$\overline{WR}$ Low to $\overline{CS}$ Low (Note 4)		30	ns

Note 1: The read/write recovery time of 200 ns holds in all cases except when a write command register operation is followed by a read data register operation when accessing the MAP coefficient RAM. This operation requires a minimum recovery time of 450 ns.

Note 2: Successive reads of the D-Channel Receive Buffer require a minimum cycle time (t_{RLRH} + t_{RHRL}) of 480 ns.

Note 3: Read access time is measured from the falling edge of $\overline{CS}$ or the falling edge of $\overline{RD}$, whichever occurs last.

Note 4: $\overline{CS}$ may go Low before either $\overline{RD}$ or $\overline{WR}$ goes Low.

Note 5: In minimal systems, $\overline{CS}$ may be tied Low.

Note 6: Read and write indirect register operations cannot be mixed without at least one write command register operation between them.

Note 7: $\overline{CS}$ may go High before either $\overline{RD}$ or $\overline{WR}$ goes High.

Note 8: If $\overline{CS}$ goes High before $\overline{WR}$ goes High, the minimum Address Hold time becomes 12 ns.

Note 9: $\overline{RD}$ and $\overline{WR}$ pulse width, Address setup and hold, and Data setup and hold timing are measured from the points where both $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ are Low simultaneously.

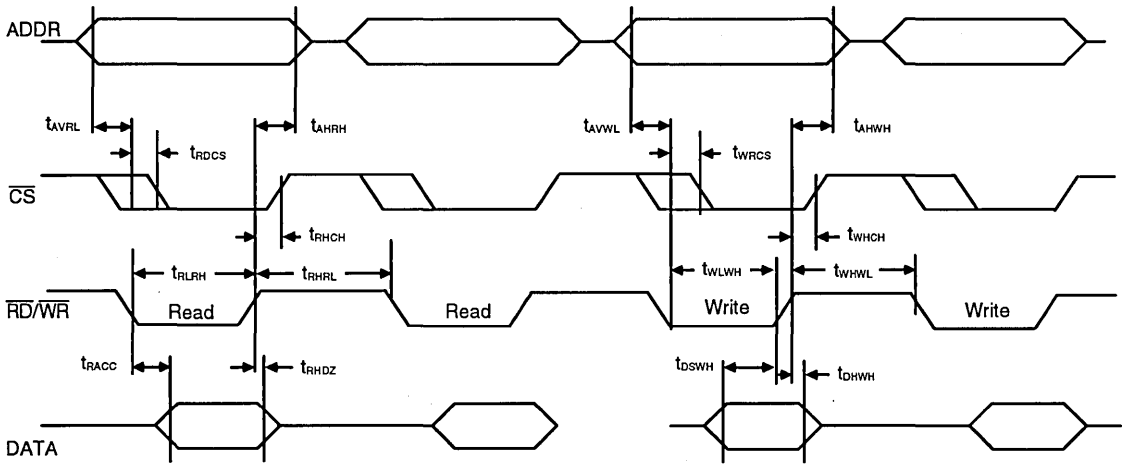


Figure 25. Microprocessor Read/Write Timing

Interrupt Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{INTC}	$\overline{INT}$ Cycle Time	125		µs
t_{REC}	$\overline{INT}$ Recovery Time	500		ns

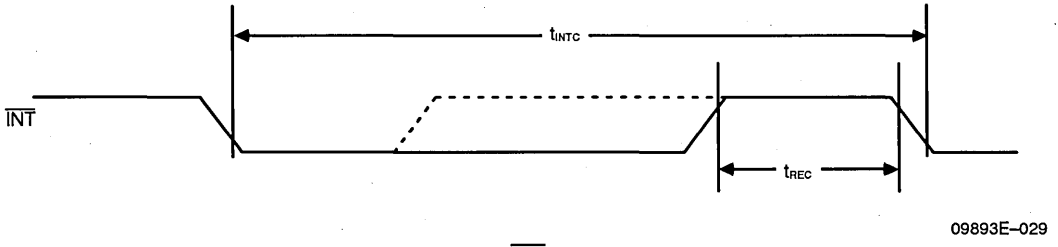


Figure 26. $\overline{INT}$ Timing

Reset and Hookswitch Timing

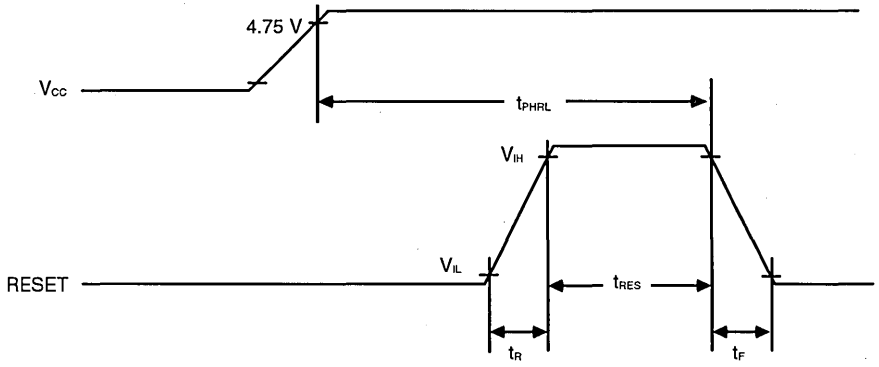
Reset Timing

Parameter Symbol	Parameter Description	Min	Max	Units.
t_{RES}	Reset Pulse Width	1		µs
t_{PHRL}	Power Stable to Reset Low	1		µs
t_F	Reset Transition Fall Time		1	ms
t_R	Reset Transition Rise Time		20	µs

Hookswitch Timing

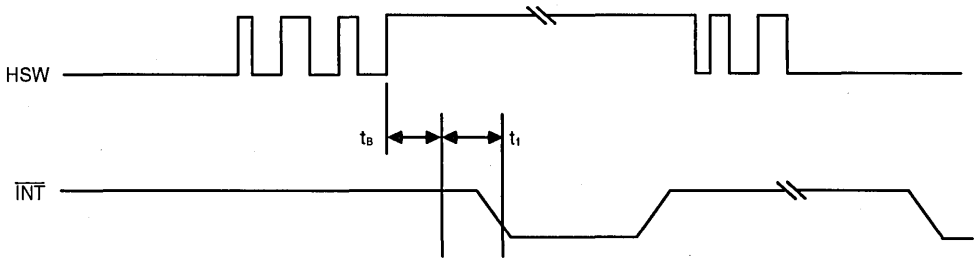
Parameter Symbol	Parameter Description	Min	Max	Units
t_B	Debounce Time	16	16.25	ms
t_I	HSW Detected to $\overline{INT}$ Delay	0	370	µs

Note: Due to clock start-up times, the hookswitch Min and Max Debounce times are approximately 3 ms greater in Power-Down Mode.



09893E-030

Figure 27. Reset Timing



09893E-031

Figure 28. Hookswitch Debounce Timing

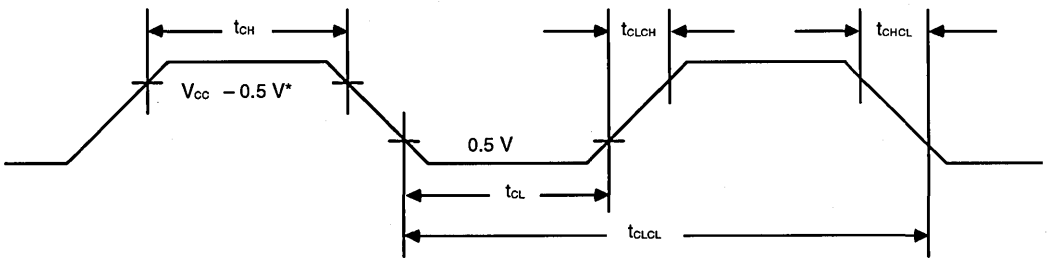
OSC (XTAL2) Timing

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
t_{CLCL}	Oscillator Period		81.374	81.387	ns
t_{CH}	High Time		33		ns
t_{CL}	Low Time		33		ns
t_{CLCH}	Rise Time			10	ns
t_{CHCL}	Fall Time			10	ns

Frequency = 12.288 MHz ±80 ppm.

MCLK Timing

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Units
t_D	XTAL2 $V_{CC}/2$ to MCLK $V_{CC}/2$		MCLK Load < 80pF		60	ns
t_{RISE1}	Rise Time		MCLK Load < 80pF 0.5 V to (V_{CC}–0.5V)		15	ns
t_{RISE2}	Rise Time		MCLK Load < 40pF 1.0 V to 3.5 V		5	ns
t_{FALL1}	Fall Time		MCLK Load < 80pF (V_{CC}–0.5V) to 0.5 V		15	ns
t_{FALL2}	Fall Time		MCLK Load < 40pF 3.5 V to 1.0 V		5	ns
t_{PWH}	High Pulse Width	12.288 MHz	MCLK Load < 80pF	33		ns
		6.144 MHz		73		ns
		4.069 MHz		114		ns
		3.072 MHz		155		ns
		1.536 MHz		317		ns
		768 kHz		643		ns
		384 kHz		1.294		µs
t_{PWL}	Low Pulse Width	12.288 MHz	MCLK Load < 80pF	33		ns
		6.144 MHz		73		ns
		4.096 MHz		114		ns
		3.072 MHz		155		ns
		1.536 MHz		317		ns
		768 kHz		643		ns
		384 kHz		1.294		µs



*Not TTL V_{IH}

09893E–032

Figure 29. External Clock Driver (XTAL2) Timing

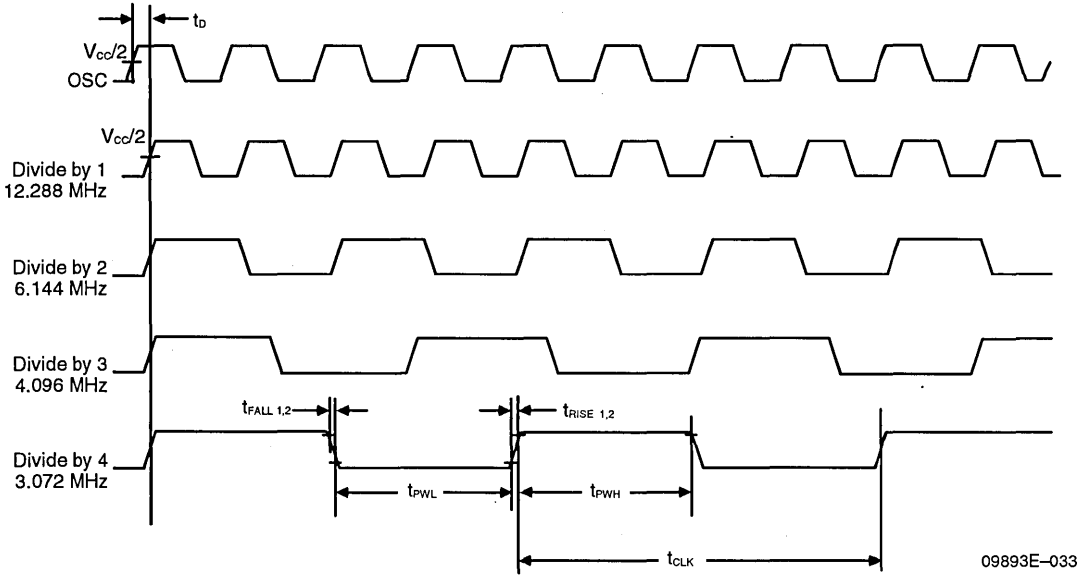
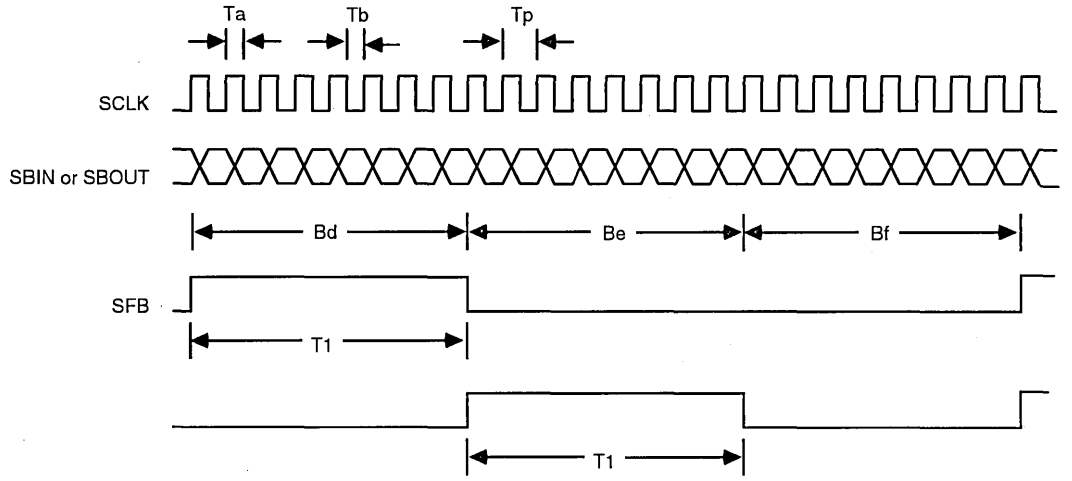


Figure 30. OSC/MCLK Timing

SBP Mode Timing

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Tp*	SCLK		5.025	5.392	µs
Ta	High time		2.594	2.615	µs
Tb*	Low time		2.431	2.777	µs
t_{RISE}	SCLK rise time	SCLK Load < 80pF		20	ns
t_{FALL}	SCLK fall time	SCLK Load < 80pF		20	ns
t_{MCSC}	MCLK to SCLK @6.144 MHz	MCLK Load < 80pF SCLK Load < 80pF		60	ns
t_{CHFS}	SCLK High to frame sync		50	250	ns
t_{CLDO}	SBOUT Data available	SBOUT/SFS Load = 80 pF	50	250	ns
t_{DICH}	SBIN set-up time		200		ns
t_{CHDZ}	SBIN hold time		0		ns

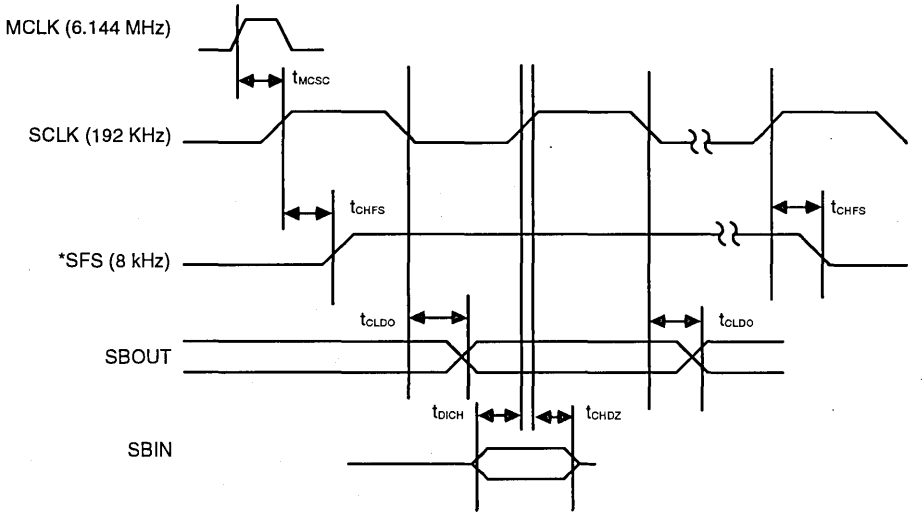
* The frequency of SCLK is f_{XTAL2}/64. Tp and Tb are based on this SCLK frequency, but include a ±163-ns allowance for internal phase lock loop correction.



Notes: 1. For PPCR2(0) = 0, SBIN data is sampled on the rising edge of SCLK, SBOUT data is changed on the falling edge of SCLK.
For PPCR2(0) = 1, SBIN data is sampled on the falling edge of SCLK; SBOUT data is changed on the rising edge of SCLK.
2. T1 width is eight SCLK periods.

09893E–034

Figure 31. SBP Mode Timing



Note 1. CH2STRB timing is identical to SFS timing, but delayed by eight SCLK cycles.
Note 2. This timing diagram reflects SCLK for PPCR2(0)=0. For PPCR2(0)=1, the diagram is identical except that the SCLK waveform should be inverted.

09893E–035

Figure 32. SBP Mode MCLK/SCLK/SFS Timing

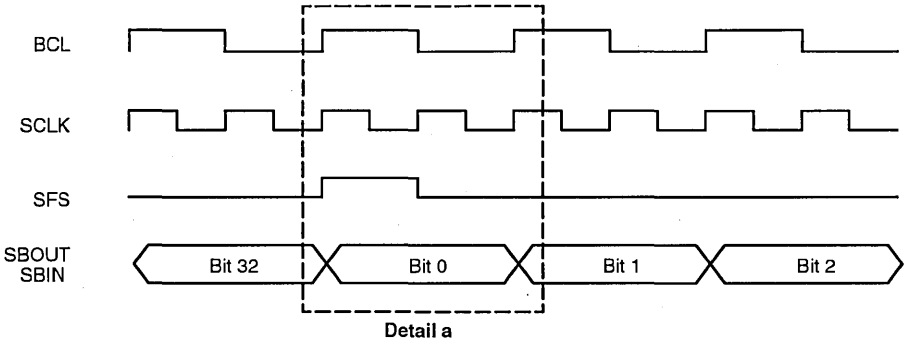
IOM 2 Master Mode Timing

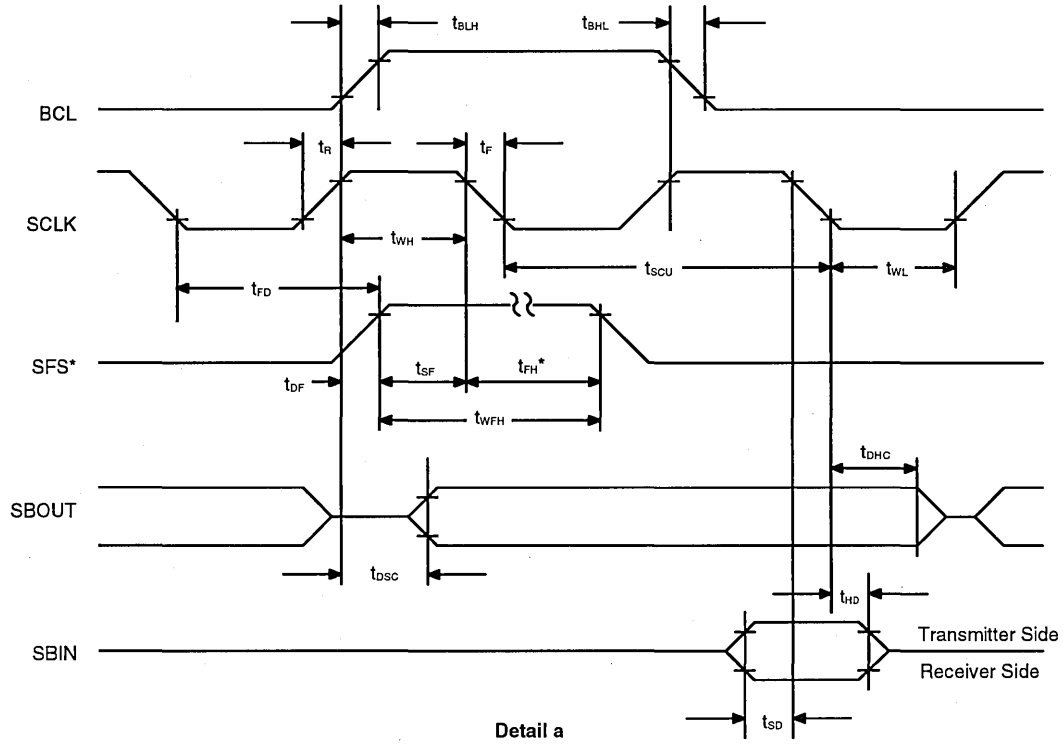
Parameter	Signal	Abbr	Test Condition	Min	Max	Units
Data Clock Rise/Fall	SCLK	t_R, t_F	$C_L = 150$ pF		50	ns
Clock Period	SCLK	t_{SCL}	1.536 MHz ±100 PPM ±163 ns*	487	815	ns
Pulse Width	SCLK	t_{WH}, t_{WL}		260		ns
Frame Sync	SFS	t_R, t_F	$C_L = 150$ pF		50	ns
Frame Sync Setup/Clock	SFS	t_{SF}	$C_L = 150$ pF	50		ns
Frame Sync Delay/Clock	SFS	t_{FD}	$C_L = 150$ pF	0		ns
Frame Sync Hold/Clock	SFS	t_{FH}	$C_L = 150$ pF	50	$t_{WL}+50$	ns
Frame Delay	SFS	t_{DF}	$C_L = 150$ pF	$-t_{WL}$	50	ns
Data Delay/Clock	SBOUT	t_{DSC}	$C_L = 150$ pF		100	ns
Data Hold/Clock	SBOUT	t_{DHC}	$C_L = 150$ pF	70		ns
Data Setup	SBIN	t_{SD}		$t_{WH}+20$		ns
Data Hold	SBIN	t_{HD}		50		ns

IOM 2 Slave Mode Timing

Parameter	Signal	Abbr	Min	Max	Units
Data Clock Rise/Fall	SCLK	t_R, t_F		60	ns
Clock Frequency (1/period)	SCLK	$1/t_{SCLK}$	1.536 MHz ±100 PPM ±163 ns*		Hz
Clock Delay High/Low	BCL	t_{BLH}, t_{BHL}		30	ns
Pulse Width	SCLK	t_{WH}, t_{WL}	240		ns
Frame Sync Rise/Fall	SFS	t_R, t_F		60	ns
Frame Set-up	SFS	t_{SF}	70		ns
Frame Hold/Clock	SFS	t_{FH}	20		ns
Frame Delay/Clock	SFS	t_{FD}	0		ns
Frame Width High	SFS	t_{WFH}	130		ns
Frame Width Low	SFS	t_{WFL}	t_{SCLK}		ns
Data Delay/Clock	SBOUT	t_{DSC}		100**	ns
Data Hold/Clock	SBOUT	t_{DHC}	70		ns
Data Set-up	SBIN	t_{SD}	$t_{WH}+20$		ns
Data Hold	SBIN	t_{HD}	50		ns

*The ±163-ns value can occur once per frame for digital phase lock loop correction.
**$C_L = 150$ pF



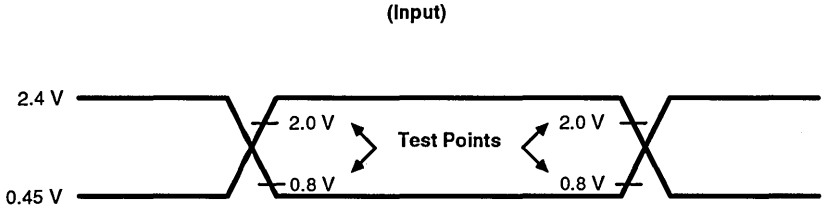


* In Master Mode, SFS is 16 SCLK cycles + set-up time + hold time in length

09893E–036

Figure 33. IOM 2 Timing

Switching Test Conditions



Note: AC testing inputs are driven at 2.4 V for a logical 1, and 0.45 V for a logical 0. Timing measurements are made at 2.0 V and 0.8 V for a logical 1, and a logical 0, respectively.

Figure 34. Switching Test Input/Output Waveform

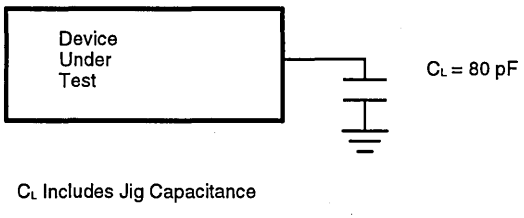


Figure 35. Switching Test Load Circuit

KEY DESIGN HINTS FOR THE DSC/IDC CIRCUIT

Due to the high level of integration of the Am79C30A/32A DSC/IDC circuit, it is easy to overlook important design information when reading the data sheet. The following list of key design hints has been compiled to streamline the design process. A comprehensive series of ISDN application notes and tutorials is available from Advanced Micro Devices; please contact an AMD sales office or factory for current information.

- The AREF pin *must* be used to bias the AINA and AINB inputs. There is a datasheet parameter, Vios, which states that the analog inputs must be biased to within 5 mV of AREF. AREF is *nominally* 2.4 V; normal device-to-device variation will exceed the 5-mV Vios specification. If a voltage other than AREF is used, transmission performance at very low signal levels will be degraded.
- The recommended method of biasing the AINA and AINB inputs is to use a 15–100 Kohm resistor between the input and AREF. The signal source should be AC-coupled to the analog input. Take care that the RC formed by the biasing resistor and blocking capacitor does not distort the input signal.
- The AREF output must not be loaded with a capacitor, since it may cause the internal buffer amplifier to become unstable. For some applications involving significant gain external to the DSC circuit, the AREF output may require a simple RC noise filter. In this case, the AREF output should be isolated from the capacitor by a resistance of greater than 1 Kohm to ensure stability.
- The analog gain selection value (in MMR3) should be written before the MAP is enabled.
- The MAP auto-zero function (MMR2) should be enabled before the MAP is enabled.
- The DSC/IDC circuit should be provided with decoupling capacitors, situated as close as possible to the package power leads. In general, 0.1-µF ceramic capacitors are sufficient, but bulk decoupling capacitors will be required if the LS1 and LS2 loudspeaker outputs are driving a heavy load.
- The DSC/IDC circuit is constructed on a single substrate, and therefore the device power pins must not be from separate supplies. If there is a DC offset between the analog and digital power-supply pins, excessive current may flow through the device substrate.
- The LS1, LS2, EAR1, and EAR2 outputs are intended to be used differentially. Although it is possible to use only a single output, the rejection of power-supply noise and internal digital noise is improved if the outputs are used differentially.
- Be certain to observe the maximum loading specification for the LS and EAR outputs. When used differentially, the EAR outputs must see a minimum of 540 ohms between them. Similarly, the LS outputs must see a minimum of 40 ohms. The maximum capacitive loading in either case is 100 pF.
- The LS and EAR outputs need not be matched to the load. The LS and EAR outputs are voltage drivers, and do not assume the presence of any particular load impedance. If the maximum loading specification is met, the LS and EAR outputs will function satisfactorily. In some cases, an external resistor may be used to center the desired output volume—for instance, while driving a 150-ohms earpiece with the EAR outputs.
- If using an EAR or LS output in a single-ended fashion, AC-couple the pin to the load. If not, the excessive DC current will cause signal distortion.
- When using programmable gains and filters in the MAP, consider the dynamic range effects such as truncation error and clipping. In case of questions in any particular application, please contact the AMD applications staff for assistance.
- All MAP tone generators are referenced with respect to the +3-dBm0 overload voltage—that is, a 0-dB tone yields a +3-dBm0 output. Take care to avoid clipping when adding tones to signals as, for example, when generating DTMF waveforms.
- The RC connected to CAP1/CAP2 must be situated as close as possible to the DSC circuit package to reduce the amount of noise coupled in from other signal traces.
- Observe the XTAL2 frequency accuracy requirement of 12.288 MHz ± 80 ppm. Since crystals from different manufacturers will vary, the DSC circuit oscillator output frequency at the MCLK pin must be measured and, if necessary, the value of the crystal load capacitors should be adjusted as part of the initial design procedure. An application note of oscillator considerations is available from AMD (ISDN System Engineering Application Note, order #12557).
- If driving the XTAL2 pin with the external oscillator, it is necessary to observe the datasheet input voltage and rise/fall time requirements. Note that the XTAL2 levels are not TTL-compatible.
- Take care in board layout of the DSC circuit, as with any sensitive analog device. An application note of DSC circuit board layout hints is available from AMD (ISDN Systems Engineering Application Note, order #12557).
- The sidetone path defaults to –18-dB attenuation. If disabling the sidetone path is desired, the sidetone block must be enabled and programmed for infinite attenuation.
- Consider the LIU transformers, series resistors, and IC LIU output drivers as a functional unit. Transformers that meet CCITT I.430 requirements with other

transceivers are not necessarily appropriate for use with the DSC circuit, and vice versa.

- Interrupts should be masked when reading or writing any indirect or multibyte DSC circuit registers to prevent the possibility of an interrupt occurring and destroying the contents of the Command Register.
- If the MAP and secondary tone ringer are disabled, the EAR, AREF, and LS outputs are high-impedance. If the MAP is enabled, the unselected audio output is high-impedance.
- The MAP should not be enabled until after the LIU has achieved synchronization. This will eliminate the possibility of audible distortion when the internal device timing is re-synchronized to the S Interface.
- To make optimum use of the MAP digital signal processsing chain, use digital gain (GX) for fine adjustment, and analog gain (GA) for coarse adjustment.
- The user must program the Secondary Tone Ringer Frequency Register (STFR) with a legal value *before* enabling the secondary tone ringer.
- In order to exit Power-Down Mode due to LIU activation, *both* the F7 interrupt and the DSC/IDC circuit interrupt pin must be enabled. In order to exit Power-Down Mode due to IOM 2 activation, *both* the IOM 2 Timing Request interrupt and the DSC/IDC circuit interrupt pin must be enabled.
- The MAP auto-zero function must be enabled *prior* to enabling the MAP. For all normal applications, the auto-zero function should always be enabled.
- To ensure proper operation of the filters (X and R) and gains (GX, GR, GER, STGR, and ATGR), these register blocks should not be accessed more frequently than 128-µs intervals. This allows the internal buffers to the map to operate properly since they are updated only once per frame.

Preliminary

Am7938

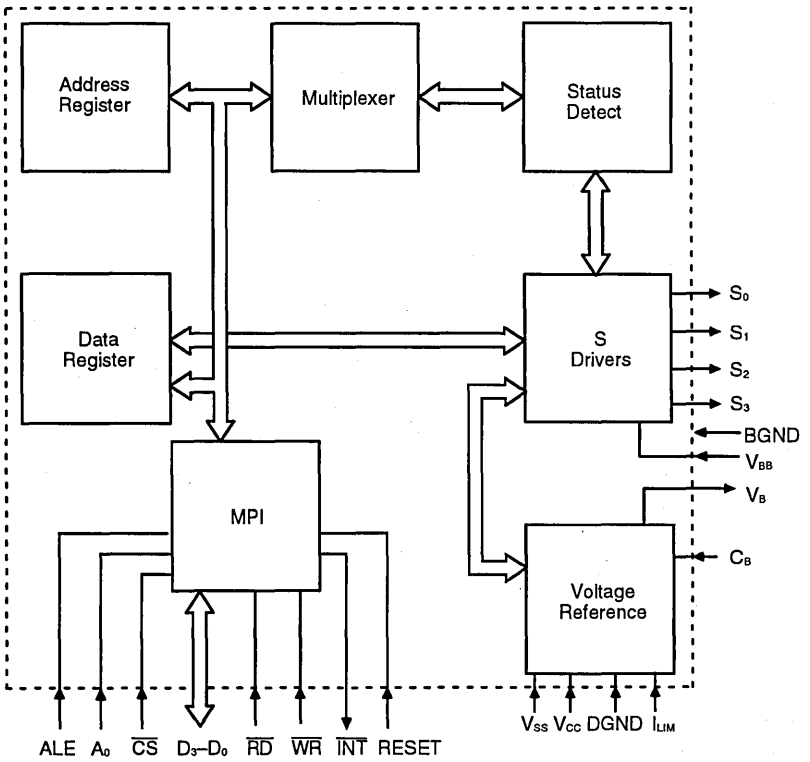
Quad Exchange Power Controller (QEPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Supplies power for up to four-digital telephone lines
- Conforms to the CCITT recommendations for power feed at the S or T reference point
- Applications for intelligent NTs and PABX/ Central Office line cards
- Supports point-to-point and point-to-multi-point configurations
- Built-in battery control circuit for operation at –40 V
- Each of the four lines is individually controlled
- Status detectors for each line driver; open loop, current overload, low output voltage, thermal overload
- Programmable current limiting
- Automatic shutdown of overloaded lines
- Automatic thermal shutdown
- Microprocessor-compatible interface, including interrupt on current overload
- High-voltage bipolar technology allows battery voltages up to –65 V
- Output current up to 150 mA per driver

BLOCK DIAGRAM



09153–001A

Publication #: 09153 Rev. D Amendment /0
Issue Date: April 1990

GENERAL DESCRIPTION

The Am7938 Quad Exchange Power Controller (QEPC) provides a power source for up to four line interfaces. The power source to the Am7938 is a local battery or a centralized regulated power supply. The Am7938 can reside in intelligent NTs or PABX/Central Office line cards. It can operate in point-to-point and point-to-multipoint configurations. Via the Am7938's microprocessor interface, each powered line is individually controlled and monitored. The power to each line can be controlled independently. Therefore, overloads and faults are easy to detect and localize even in a large system. The status conditions detected by the Am7938 on each line that may be read by the microprocessor are: low output voltage, open loop, current overload, thermal overload, and normal line conditions.

Current limit and thermal shutdown circuits protect the Am7938 against overload conditions. However, certain applications may require additional external protection circuitry.

The Am7938 has been developed specifically for CCITT-compatible ISDN configurations. Recognize, however, that due to its versatile design, the Am7938 can be used in numerous other applications.

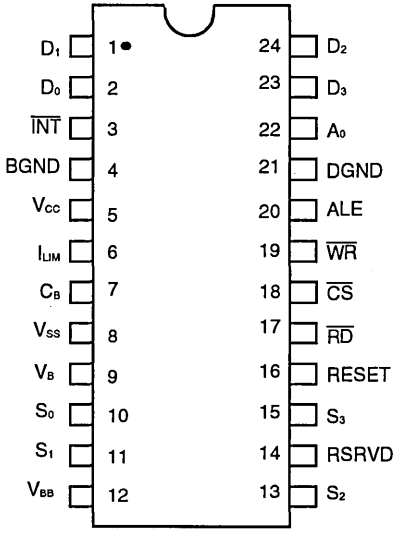
GLOSSARY OF ABBREVIATIONS

A_0	Address Bit
ALE	Address Latch Enable
BGND	Battery Ground (Battery refers to Telephone Line Supply)
C_B	Battery Compensation Capacitor
CCITT	Consultative Committee for International Telegraph and Telephone
CO	Central Office
COD	Current Overload Detector
$\overline{CS}$	Chip Select
D_3–D_0	Data Lines 3–0
DGND	Digital Ground
IAR	Indirect Address Register
I_{LIM}	Current Limit Programming
I_{SLIM}	S-Output Current Limit
$\overline{INT}$	Interrupt
ISDN	Integrated Services Digital Network
LER	Line Enable Register
LVD	Low Voltage Detector
MPI	Microprocessor Interface
NT	Network Terminator
OLD	Open Loop Detector
PABX	Private Automatic Branch Exchange
$\overline{RD}$	Read
R_{LIM}	Current Limit Programming Resistor
RSRVD	Reserved
S	S Reference Point
S_3–S_0	S Driver Lines 3–0
TE	Terminal Equipment
T/I	Thermal/Interrupt Bit
TOR	Thermal Overload Register
U	U Reference Point
V_B	Battery-control Voltage
V_{BB}	Battery Supply
V_{CC}	+5-V Power Supply
V_{SS}	Substrate Voltage
$\overline{WR}$	Write

CONNECTION DIAGRAM

Top View

24-Pin DIP



Notes: 1. Pin 1 is marked for orientation.
2. Reserved (RSRVD) pins should not be connected externally to any signal or supply.

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM7938 **D** **C** **B**

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD 024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am7938
Quad Exchange Power Controller (QEPC)

Valid Combinations	
AM7938	DC, DCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_0
Address Line (Input)

A_0 selects source and destination locations for read and write operations on the data bus. A_0 must be valid on the falling edge of ALE or during $\overline{RD}$ and $\overline{WR}$ if ALE is tied High.

ALE
Address Latch Enable (Input; Active High)

ALE is an input control pulse used to strobe the address on the A_0 line into the address latch. This signal is active High to admit the input address. The address is latched on the High–Low transition of ALE. While ALE is High, the address latch is transparent. For an unmultiplexed microprocessor bus, ALE must be tied High.

BGND
Ground Battery

Regulated output on V_B is referenced to this ground.

C_B
Battery Compensation Capacitor

C_B is intended for users who operate the QEPC with an external Darlington transistor (Figure 2) to allow users a simple way of stabilizing the QEPC/Darlington circuit over a wide range of operating conditions. If the voltage on the S-output drivers oscillates due to some instability of the Darlington, a capacitor should be connected to C_B, with the other side of the capacitor connected to V_B.

$\overline{CS}$
Chip Select (Input; Active Low)

$\overline{CS}$ must be Low to enable the read or write operations of the Am7938. Data transfer occurs over the D_3–D_0 lines. The interaction of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and D_3–D_0 is described below.

D_3–D_0
Data Bus (Input/Output; Three State, Active High)

The four bidirectional data bus lines are to exchange information with a microprocessor. D_0 is the least significant bit and D_3 is the most significant bit. A High on the data bus corresponds to a logical 1. These lines act as inputs when $\overline{WR}$ and $\overline{CS}$ are active and as outputs when $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive, the D_3–D_0 pins are placed in a high-impedance state.

DGND
Ground Digital

Digital ground to logic.

I_{LIM}
Current Limit Programming (Input)

I_{LIM} programs the current limit of the S drivers using an external resistor connected between I_{LIM} and V_{SS}. The I_{LIM} pin is 1.25 V more positive than V_{SS}. The current limit is 5 mA plus 1000 times the current in the external resistor. The programmed current limit applies to each S driver.

$\overline{INT}$
Interrupt (Output; Open-Collector, Active Low)

$\overline{INT}$ augments the Microprocessor Interface by generating an interrupt when a Current Overload Detector (COD) occurs. $\overline{INT}$ is active whenever any bits in the COD register are active. Note that $\overline{INT}$ is not latched; when the COD register is zero, $\overline{INT}$ goes inactive (High). $\overline{INT}$ will also go inactive if the QEPC automatically disables the S-output driver that caused the interrupt (due to Thermal Overload), or if the microprocessor disables that line via the Line Enable Register (LER). COD interrupts can be masked via the Indirect Address Register (IAR); RESET always disables the $\overline{INT}$ pin.

$\overline{RD}$
Read (Input; Active Low)

The active Low read signal is conditioned by $\overline{CS}$ and transfers internal information to the data bus. If A_0 is a logical 0, logic levels of the Indirect Address Register (IAR) and Thermal Shutdown Status bit will be transferred to D_3–D_0. If A_0 is a logical 1, the data addressed by the IAR will be transferred to D_3–D_0.

RESET
Reset (Input; Active High)

RESET initializes the registers in the Am7938, leaving the S drivers switched off.

S_3–S_0
S Drivers (Output)

S_3–S_0 each supply power to one line. The outputs can sink up to 150 mA each. The voltage at the line is connected to V_{BB} through a saturated transistor switch.

V_B
Battery Reference Voltage (Output)

V_B provides an output proportional to the deviation of V_{BB} from an internal –40 V reference with respect to BGND. V_B can be used as a driver for an external PNP Darlington power transistor supplying power from the battery to V_{BB} (see Figure 2).

V_{BB}
Supply Voltage S Driver (Input)

V_{BB} supplies power to the S drivers.

V_{CC}
+5-V Power Supply (Input)

V_{SS}
Substrate Voltage (Input)

V_{SS} is the internal negative supply voltage. V_{SS} must always be connected to the most negative supply voltage. The MPI Registers will not function properly when the battery power is disconnected, that is, when V_{SS} is floating or grounded. The QEPC should also be reset if a drastic transient is applied to V_{SS}.

$\overline{WR}$
Write (Input; Active Low)

The active Low write signal is conditioned by $\overline{CS}$ and transfers information from the data bus to an internal register selected by A_0. If A_0 is a logical 1, D_3–D_0 is written into the Line Enable Register (LER). If A_0 is a logical 0, D_3–D_0 is written into the IAR. LER and IAR are the only two writable registers in the Am7938.

FUNCTIONAL DESCRIPTION

The Am7938 is divided into two sections, the Analog section and the Microprocessor Interface (MPI) section. The analog section provides power and detects the status of the S lines. This status information is available to the microprocessor via the MPI.

Initialization

The Am7938 is initialized when reset by an external signal applied to the RESET pin. In the initialized state the analog drivers are switched off, the Indirect Address Register (IAR) is cleared, and the internally latched address A_0 is cleared.

–40 V Power

The voltage at the S drivers is approximately V_{BB} (less V_{SAT}). A regulated –40V S output can be achieved by using the V_B pin to drive an external Darlington power transistor.

Analog Section

The major functions of the analog section are the four line drivers, which are saturated Darlington transistor switches capable of sinking up to 150 mA each. The power to the drivers is derived from the negative supply voltage (V_{BB}) to the Am7938. The output voltage to each line is slaved to V_{BB}, and the voltage drop in each driver is approximately 1.5 V.

Line driver protection is provided through the integration of current limit and over-temperature shut-off. The current limit is hardware-programmable via an external resistor (R_{LIM}) connected between I_{LIM} and V_{SS}. The I_{LIM} pin is 1.25 V more positive than V_{SS}. The output limit is: $5\ mA + 1000 \cdot 1.25\ V/R_{LIM}$. This $1000\times$gain makes the I_{LIM} pin susceptible to external noise. Care should be taken to connect R_{LIM} as close to the QEPC as possible.

The thermal shut-off is internally set at approximately 175°C. At this temperature all the drivers are unconditionally switched off. However, at approximately 140°C, only the drivers that are in the current-overload condition will be turned off.

Status detectors, associated with each of the line drivers, monitor the load conditions on each line by comparing an electrical parameter (e.g., current and voltage at the line) with a reference level. The output of each detector can be read by the microprocessor. In addition to these status detectors, the temperature of the Am7938 is monitored via integrated temperature detectors. The detectors respond at approximately 140°C and 175°C, as defined above, and the 175°C detector can be monitored by the microprocessor via the MPI. The status detectors provide the following information from each of the lines (all detectors have built-in hysteresis):

Low Output Voltage Detection

The low-output-voltage status bit becomes active when the output transistor is pulled out of saturation.

Open Loop Detection

The open-loop status bit becomes active when the current on the line drops below a minimum value.

Current Overload Detection

The current-overload status bits become active when the current on the line nears the current limit. These bits activate the $\overline{INT}$ output if COD interrupts are enabled via the IAR Register.

Thermal Overload Detection

If the Am7938 device temperature reaches 140°C, then all the line drivers in the current-overload condition will be switched off and the corresponding bits in the Thermal Overload Register will be cleared. If the device temperature increases to 175°C, all the line drivers will be turned off, and all the bits in the Thermal Overload Register will be cleared. The T-bit will also be set, and it can be read along with the Indirect Address Register (IAR) to indicate that all the drivers have been turned off. To initialize any of the bits in the Thermal Overload Register, the microprocessor must first turn off the line drivers via the Line Enable Register (LER) (see MPI definition). The line drivers must not be reactivated until the T-bit in the address register is cleared by the temperature detector in the Am7938.

MPI Section

The MPI allows the user to access the detectors defined in the analog section. The line driver's status bits are grouped by function. Bits 3–0 of the detectors correspond to lines 3–0, respectively. The status groups are:

Low Voltage Detector (LVD)
Open Loop Detector (OLD)
Current Overload Detector (COD)
Thermal Overload Register (TOR)

The data is not latched in these status groups except in the TOR. Thus, the user should filter (multiple samples) the received data to ensure its integrity. There are two other registers in the MPI: the Indirect Address Register (IAR), and Line Enable Register (LER).

The IAR contains 3 bits that address the desired status group or the LER. The IAR is read along with the T-bit defined in the analog section. The microprocessor can read the IAR to check the validity of the address. A 1-µs delay is required between a Write to the LER Register, followed by a Read of that same register. Subsequent reads of the LER do not have this constraint.

The LER is used to enable or disable the individual line drivers. The line drivers will only become active if the corresponding bit in the TOR is inactive. The LER is a read/write register. The MPI contains the interface to the following pins:

D_3–D_0	Bidirectional	Data Bus
A_0	Input	Address Line
ALE	Input	Address Latch Enable
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
$\overline{INT}$	Output	COD Interrupt

The 4-bit bidirectional data bus (D_3–D_0) is used to communicate with the registers. Access to the registers is controlled by $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, and A_0 as shown below. A read or write cycle must be preceded by a valid A_0. A_0 is latched internally in a transparent latch by ALE. The selection of the status group or the LER is determined by the content of the IAR.

The truth table for the MPI control is shown below:

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	
0	1	0	0	Write IAR (T bit is read only)
0	0	1	0	Read IAR and T bit
0	1	0	1	Write LER
0	0	1	1	Read status groups or LER
1	X	X	X	No access

Indirect Address Register (IAR) and T/I Bit

The IAR is 3 bits wide and accessible through the data port, D_2–D_0. The content of the Indirect Address Register (IAR_2–IAR_0) determines the selection of the status groups or the LER. The thermal overload bit T/I is read and written at the same time as IAR and occupies D_3. This register has the following format:

Bit	Symbol	
0	IAR_0	Bit 0 of the IAR
1	IAR_1	Bit 1 of the IAR
2	IAR_2	Bit 2 of the IAR
3	T/I	T bit: (Read only)
		Logical 0: temperature normal (default value)
		Logical 1: temperature above 175°C (all drivers shut off)
		I bit: (Write only)
		Logical 0: $\overline{INT}$ pin disabled
		Logical 1: COD interrupts enabled via $\overline{INT}$ pin

IAR_2–IAR_0 address the status groups and the LER as shown below:

IAR_2	IAR_1	IAR_0	Select
0	0	0	LVD
0	0	1	OLD
0	1	0	COD
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	LER
1	1	1	TOR

The contents and format of the status groups and the LER are as follows:

LVD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 low voltage	S_0 voltage normal
1	S_1 low voltage	S_1 voltage normal
2	S_2 low voltage	S_2 voltage normal
3	S_3 low voltage	S_3 voltage normal

The Low Voltage Detector (LVD) indicates the voltage level on the S lines, even when the lines are disabled. Note however, that the detection threshold is slightly different. The low-voltage condition becomes active (logical 1) if the output reaches the Low Voltage Threshold (V_{LVD}).

OLD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 open loop	S_0 current normal
1	S_1 open loop	S_1 current normal
2	S_2 open loop	S_2 current normal
3	S_3 open loop	S_3 current normal

The Open Loop Detector (OLD) indicates the open-loop condition on the S lines. The open-loop condition becomes active (logical 1) if the current on the line drops below the threshold value ISOC.

COD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 current overload	S_0 current normal
1	S_1 current overload	S_1 current normal
2	S_2 current overload	S_2 current normal
3	S_3 current overload	S_3 current normal

The Current Overload Detector (COD) indicates the current-overload condition on the S lines. The overload condition becomes active (logical 1) if the output current approaches the value programmed by an external resistor between I_{LIM} and V_{SS}.

TOR:

Bit	Logical 1 (default value)	Logical 0
0	S_0 operational	S_0 off
1	S_1 operational	S_1 off
2	S_2 operational	S_2 off
3	S_3 operational	S_3 off

The Thermal Overload Register (TOR) contains the overload status of the S line drivers. If the Am7938 device temperature reaches 140°C, then the S line drivers that are in the current-overload condition will be switched off. The corresponding bits in the TOR will be set to a logical 0 . To initialize any of the bits in the TOR, the microprocessor must first turn off the S line drivers via the LER. However, the TOR bits cannot be deactivated if the 175°C detector is active. The µP may re-enable the S drivers via the LER after the TOR condition is removed. The TOR is a read-only register.

LER:

Bit	Logical 1	Logical 0 (default value)
0	S_0 on	S_0 off
1	S_1 on	S_1 off
2	S_2 on	S_2 off
3	S_3 on	S_3 off

The Line Enable Register (LER) is used to enable or disable the individual S line drivers. The S line will only become active if the corresponding bit in the TOR is set to a logical 1. The LER can be written directly and read indirectly.

APPLICATIONS

The Am7938 major applications are in intelligent NTs, and in PABX and Central Office line cards.The applications show the Am7938 interfaced to the CCITT S interface point; however, the Am7938 can be used to control the power feed for any transformer coupled system, that is, the CCITT U interface point.

The Am7938 Used With a Regulated Supply

Figure 1 shows the Am7938 used with a regulated supply voltage of $V_{BB} = -40\ V - V_{SAT}$. The output voltage from the S drivers (because of the voltage drop across the internal transistors) will be V_{SAT} more positive than V_{BB}. The V_B and C_B pins are unused; V_{SS} is tied to V_{BB}. Other battery voltages can be used. The Am7938 can power up to eight TEs per S line provided the total current per line does not exceed 150 mA.

Recommended Decoupling:

- ≥10 µF from V_{CC} to DGND
- 0.1 µF from V_{CC} to DGND
- 1.0 µF from V_{SS} to DGND
- V_{SS} shorted to V_{BB}
- DGND shorted to BGND

The Am7938 Used With an External Power Transistor

Power to the Am7938 is supplied from the local battery with an external power transistor to dissipate power from the Am7938. The Am7938 allows battery voltages up to –65 V provided the external power transistor can handle the power dissipation (see Figure 2).

Recommended Decoupling:

- ≥10 µF from V_{CC} to DGND
- 0.1 µF from V_{CC} to DGND
- 1.0 µF from V_{SS} to DGND
- 0.1 µF from V_{BB} to DGND
- TBD µF from C_B to V_B
- DGND shorted to BGND

The Am7938 Employing a Relay to Provide Polarity Reversal

The CCITT recommends that polarity reversal be used to resolve the power contention in a point-to-multipoint configuration when local power is lost. In Figure 3, polarity reversal is implemented using the Am7938 and one additional relay. The coil and contacts of the relay are connected so that the relay is activated when local power is available, and is deactivated when local power is lost. Hence, power consumption is minimized when local power is lost.

An alternative solution for power contention resolution is to power only a few lines when local power is lost. In the Am7938, each line is independently controlled via the microprocessor through the LER, hence, the microprocessor can turn off non-priority lines as required.

Four Am7938s Interfaced to a Microprocessor Bus

Figure 4 illustrates four Am7938s interfaced to a microprocessor. Only the lower four data lines from the microprocessor's 8-bit data bus are used. These are connected to the Am7938's D_3–D_0 pins. In a non-multiplexed microprocessor bus system ALE must be tied to a logical 1.

Protection of the QEPC Against Overvoltage

In Central Office (CO) or long-line PABX applications, the QEPC requires additional external protection against lightning and voltages induced from the power lines.

Figure 5 shows how the QEPC and the system is protected via an overvoltage-limiting device and fuse resistors.

The voltage-limiting device limits the voltage on the S line to a safe value, and the fuse resistors break the circuit if a continuous high-power source is connected to the S line. The diode in the battery line prevents the line surges from going below the substrate voltage.

General Information

$\overline{INT}$ should be connected to an edge-triggered input on the controlling microprocessor since $\overline{INT}$ is not latched. In this way, the microprocessor interrupt logic will latch the fact that $\overline{INT}$ went Low. $\overline{INT}$ is an open-collector output so that multiple QEPCs can be wire-ORed to produce a single interrupt for all QEPCs on a line card. It is impossible to read the Current Overload Interrupt mask since the interrupt mask bit is shared with the Thermal Shutdown bit (MSB of the IAR). Therefore, it is prudent to keep a RAM copy of the interrupt mask if this status is required for the application.

The microprocessor should enable one S Output Driver at a time (via the LER) to avoid undue current surges through the QEPC. This is due to the inherently inductive nature of the S Interface Lines. The user should expect the corresponding bits in the COD Register to momentarily become active when the Line has just been enabled. Because of this, it is recommended to mask the COD Interrupt (via the IAR Register) until all desired lines are enabled. In addition, for highly inductive lines, the user should connect a 0.01-µF capacitor from each S Output Driver pin to V_{SS}. Protective diodes should also be connected to S Output Drivers under these conditions (see Figure 5).

The COD Interrupt Service Routine should not blindly assume that the S Interface Line corresponding to the COD bit is shorted and immediately disable that line. A short circuit condition can be determined by the presence of a COD and a Low Voltage Detector (LVD) on the same line. This fact should be considered if the line

normally operates near the programmed current limit (set by R_{LIM}). Also, a momentary COD Interrupt may be generated by an additional load if the line was already operating near the programmed current limit. The COD Interrupt Service Routine should read the COD Register again to determine if the COD was a transient spike.

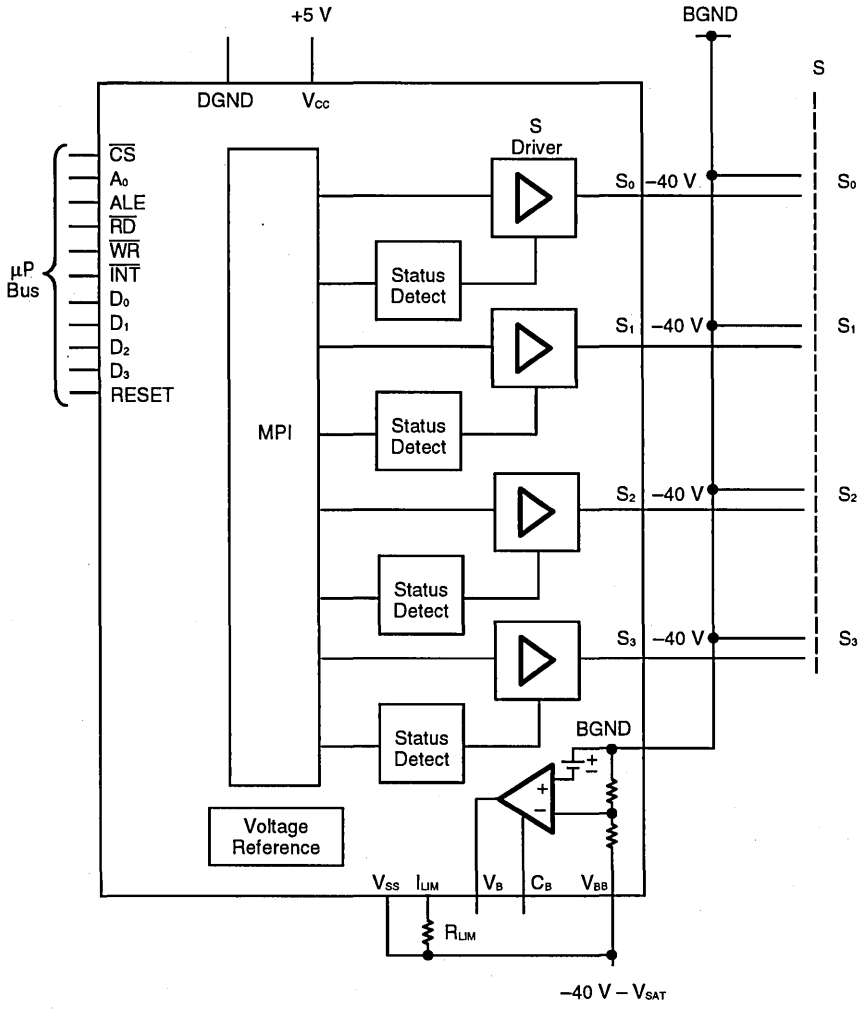


Figure 1. The Am7938 Used With a Regulated Supply
(other battery/S_{out} voltages can be used)

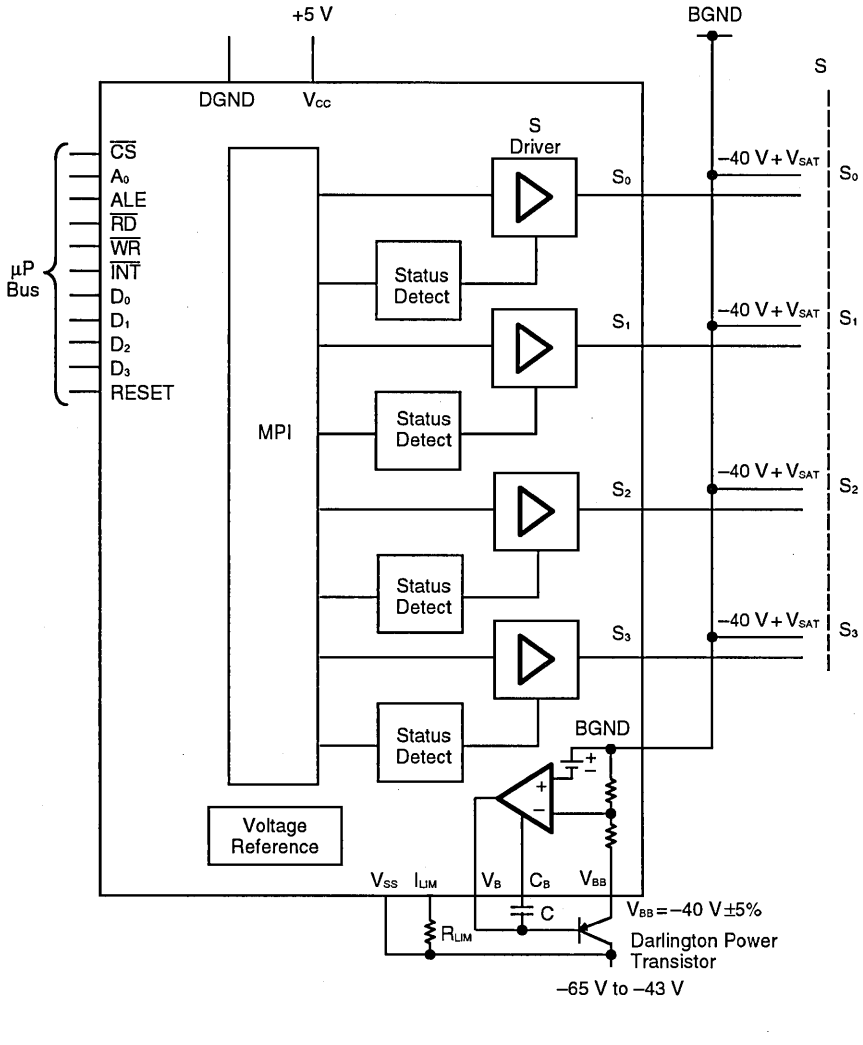


Figure 2. The Am7938 Used With an External Power Transistor

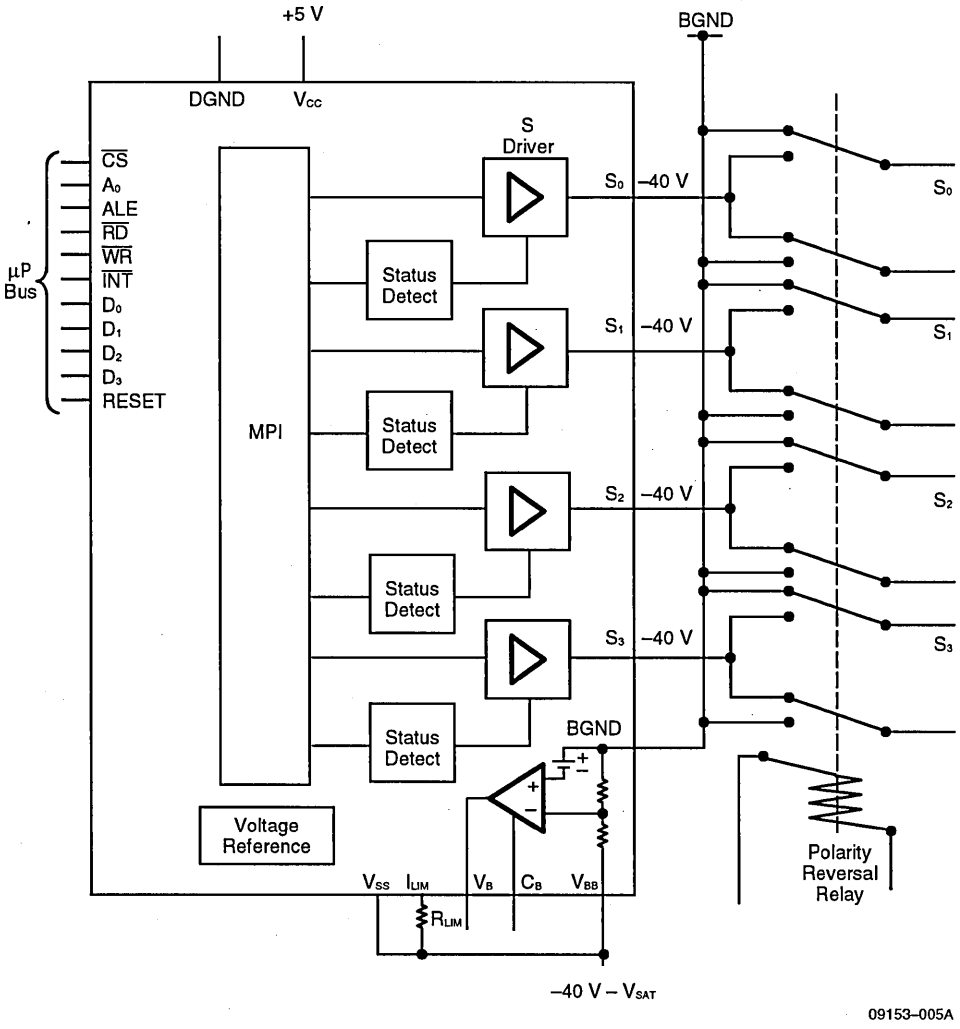


Figure 3. The Am7938 Employing a Relay to Provide Polarity Reversal

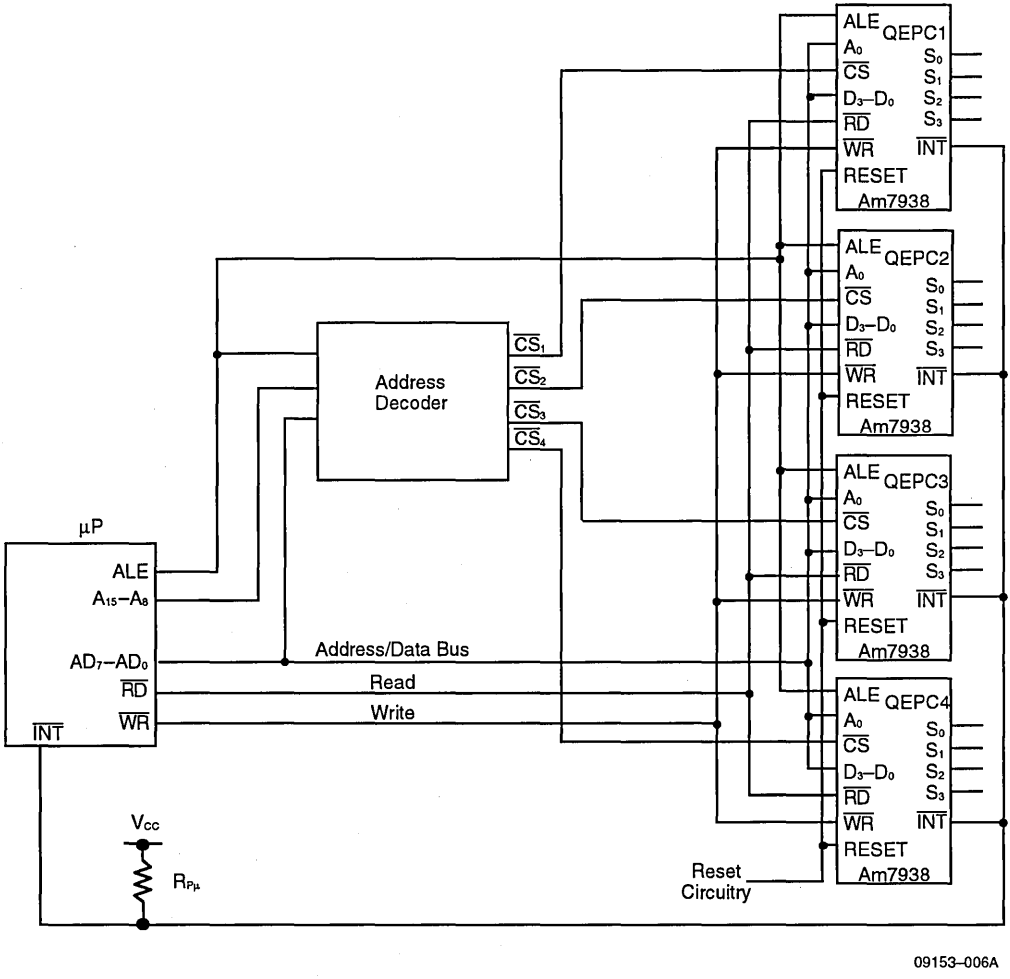


Figure 4. Four Am7938s Interfaced to a Microprocessor Bus

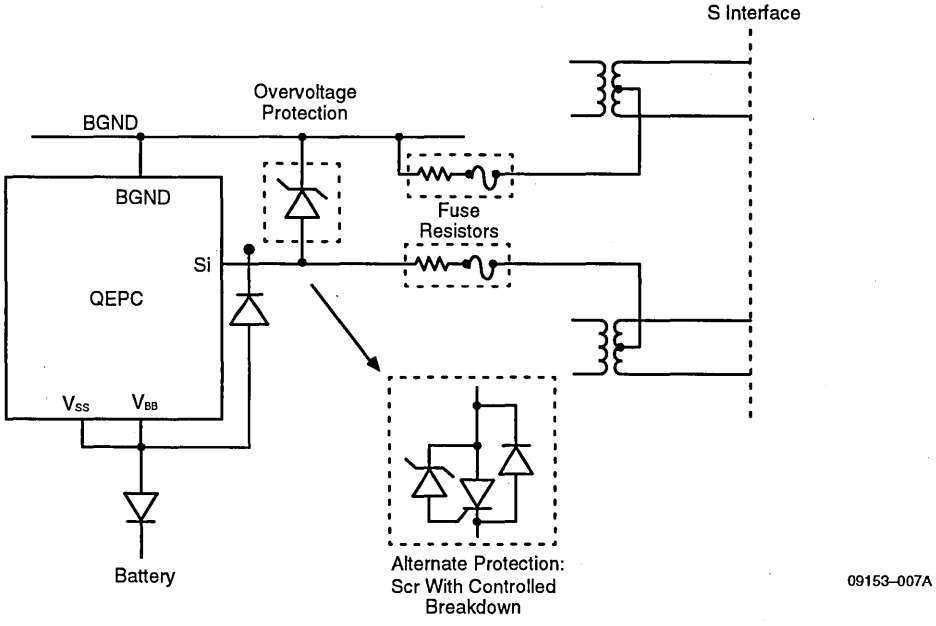
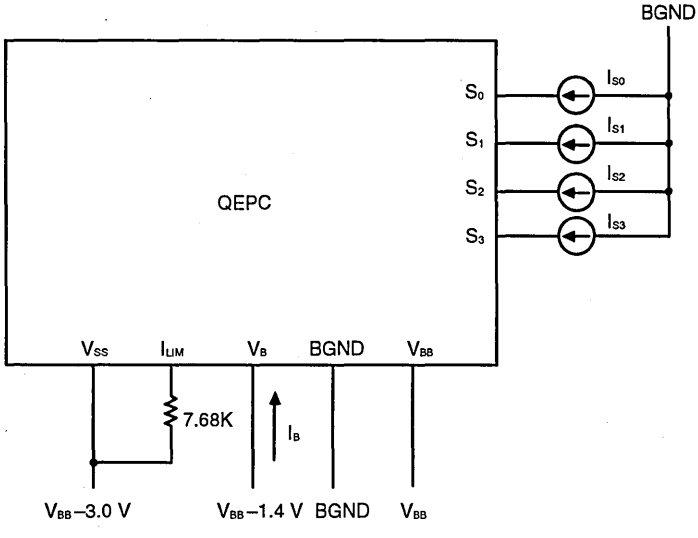


Figure 5. Protection of the QEPC Against Overvoltage



I_{Si} = Current at S Output Driver i, where i = 0–3

Figure 6. Current Into V_B

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –60°C to +150°C
Voltage from Digital Input
to DGND ..... –0.4 V to V_{CC}
Voltage from V_{CC}
to DGND ..... –0.4 V to 7 V
Voltage from V_{SS}
to DGND ..... –70 V to +0.4 V
Voltage from V_{BB}
to DGND ..... (V_{SS} –0.4 V) to +0.4 V
..... and (V_{CC} –70 V) to +0.4 V

100-ns Pulse Voltage from Si
to DGND (Notes 1 and 3) ..... –90 V to + 2 V
Voltage from BGND
to DGND ..... V_{SS} to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Ambient Temperature(T_A) ..... 0°C to +70°C
DGND ..... 0 V
BGND Voltage ..... –2 V to + 0.5 V
V_{CC} Voltage ..... +5 V ± 5%
V_{BB} Voltage ..... –65 V to –38 V
V_{SS} Voltage, V_B Unused ..... V_{BB}
V_{SS} Voltage, V_B Used ..... –65 V to –43 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Notes:
1. Si stands for S_0, S_1, S_2, or S_3 outputs.

2. Operation at smaller V_{BB} magnitudes is possible, but parameters are not guaranteed. V_{BB} must be at least –15 V with respect to BGND.

3. The test condition is specified with a diode in series with V_{SS} as shown in Figure 5.

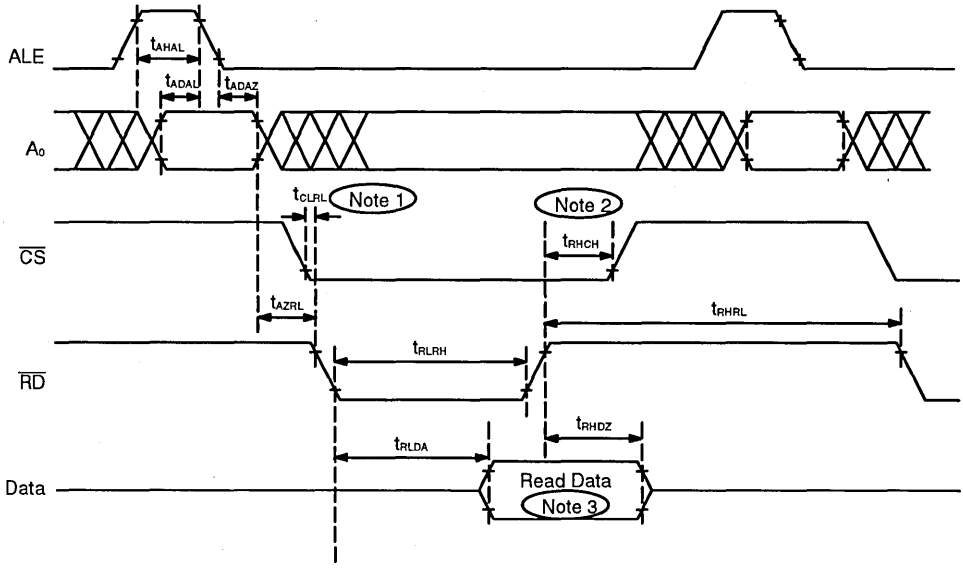
DC CHARACTERISTICS over commercial operating range

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic Input High Level		2.0			V
V_{IL}	Logic Input Low Level				0.8	V
I_{OH}	Logic Output High Current	(V_{OH} = 2.4 V)	400			µA
I_{OL}	Logic Output Low Current	(V_{OL} = 0.4 V)	2.0			mA
I_{IH}	Logic Input High Current	(V_{IH} = 2.0 V)			10	µA
I_{IL}	Logic Input Low Current	(V_{IL} = 0.8 V)			60	µA
I_{OZH}	Output Hi-Z Current High	(2.4 V < V_{OZ} < V_{CC})			10	µA
I_{OZL}	Output Hi-Z Current Low	(0 V < V_{OZ} < 0.4 V)			10	µA
I_{CC}	V_{CC} Supply Current			17	TBD	mA
C_L	Logic Input/Output Capacitance			10		pF
V_{SAT}	Saturation Voltage	(V_{Si} – V_{BB}), I_{Si} = 150 mA			2.0	V
I_B	Current Into V_B (see Figure 6)	V_{BB} = –42 V			80	µA
		V_{BB} = –38 V	1200			µA
I_{SS}	V_{SS} Supply Current	V_{SS} = –65 V, V_{BB} = –40 V		1.5	TBD	mA
I_{BB}	V_{BB} Supply Current, V_{BB} = –42 V	(Outputs Disabled)		2.6	TBD	mA
I_{SLIM}	Limit Current	R_{LIM} = 8.62K	TBD	150	TBD	mA
		R_{LIM} = 27.8K	TBD	50	TBD	mA
V_{LVD}	Low Voltage Detector	Si off		1.7	TBD	V
	Relative to V_{BB}	Si on		3	TBD	V
I_{SOL}	Current Overload Detector(I_{SLIM})		TBD	85	TBD	%
I_{SOC}	Current at Open Circuit Detector		TBD	5	TBD	mA
I_{SZ}	S_i Current to Ground, S_i Disabled	S_i is i-th output		50	TBD	µA
H_{LVD}	Low Voltage Detector Hysteresis			60		mV
H_{OLD}	Open Loop Detector Hysteresis			1		mA
H_{COD}	Current Overload Detector Hysteresis			2.6		mA
H_{140}	Thermal Detector (140°C) Hysteresis			15		°C
H_{175}	Thermal Detector (175°C) Hysteresis			15		°C

SWITCHING CHARACTERISTICS over operating range

Parameter Number	Parameter Symbol	Parameter Description	Min	Max	Unit
Microprocessor Read/Write Timing					
1	t_{RLRH}	$\overline{RD}$, $\overline{CS}$ Pulse Width	220		ns
2	t_{RHRL}	$\overline{RD}$ Recovery Time	200		ns
3	t_{RLDA}	$\overline{RD}$, $\overline{CS}$ Low to Data Available		220	ns
4	t_{RHDZ}	$\overline{RD}$ or $\overline{CS}$ High to Data Hi Z		110	ns
5	t_{AHAL}	ALE Pulse Width	60		ns
6	t_{ADAL}	Address Setup Time	30		ns
7	t_{ADAZ}	Address Hold Time	30		ns
8	t_{AZRL}	Address Hi Z to $\overline{RD}$ Low	0		ns
9	t_{WLWH}	$\overline{WR}$ or $\overline{CS}$ Pulse Width	200		ns
10	t_{WHWL}	Write Recovery Time	200		ns
11	t_{DAWH}	Data Setup Time	100		ns
12	t_{WHDZ}	Data Hold Time	30		ns
Reset Timing					
13	t_{RES}	Reset Pulse Width	200		ns
14	t_{PHRL}	Power Stable to Reset Low	1		µs
15	t_{ACC}	Reset Recovery Time to Access	700		ns
Si Timing			**Typ**		
16	t_{EN}	Si Output Enable Time (from LER)	1		µs
17	t_{DIS}	Si Output Disable Time (from LER or RESET)	2		µs

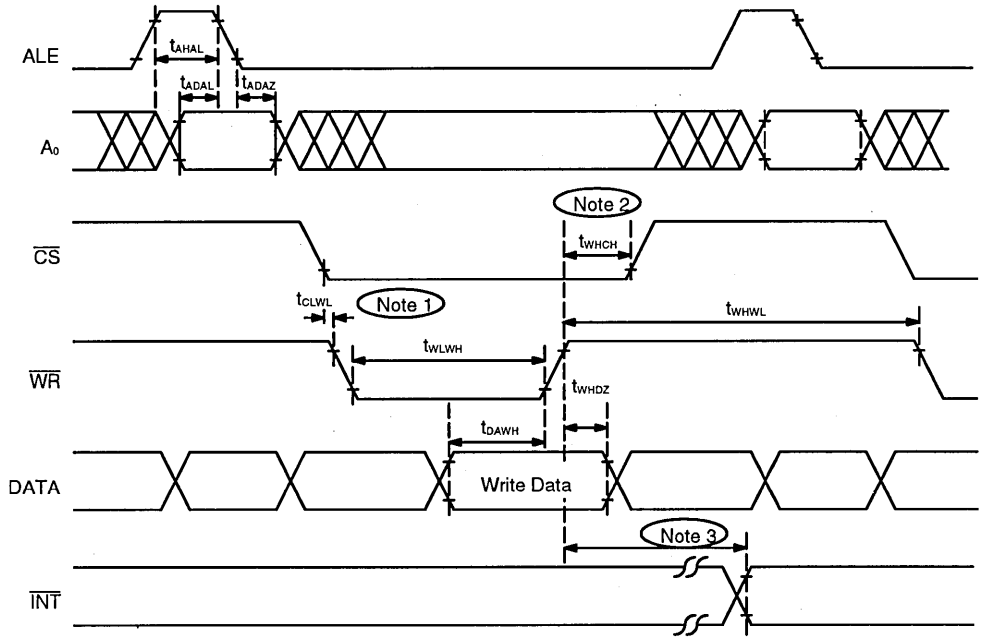
Note: All switching characteristics tests are performed with a 100-pF test load, and TTL-compatible voltage levels.



Notes:

1. If t_{CLRL} is negative, t_{RHRL}, t_{RLRH}, t_{AZRL}, and t_{RLDA} are measured from $\overline{CS}$ rathar than $\overline{RD}$.
2. If t_{RHCH} is negative, t_{RHRL}, t_{RLRH}, and t_{RHDZ} are measured from $\overline{CS}$ rather than $\overline{RD}$.
3. When a read from the LER immediately follows a write to the LER, a minimum of 1 µs is required between these operations. This is to allow the internal buffers in the Am7938 to settle. Subsequent reads from the status group or the LER do not have this restriction.

Figure 7. Microprocessor Read Timing



Notes: 1. If t_{CLWL} is negative, t_{WHWL} and t_{WLWH} are measured from $\overline{CS}$ rather than $\overline{WR}$.
2. If t_{WHCH} is negative, t_{WHWL}, t_{WLWH}, t_{DAWH}, and t_{WHDZ} are measured from $\overline{CS}$ rather than $\overline{WR}$.
3. The propagation delay from the writing of the T/I bit to the effect on the $\overline{INT}$ pin is approximately 1.3 µs for both mask and enable operations.

Figure 8. Microprocessor Write Timing

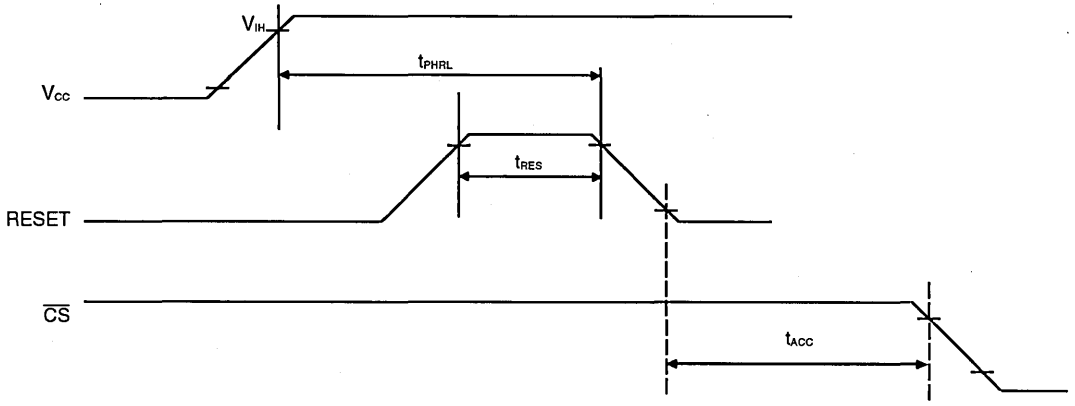


Figure 9. Reset Timing

09153–010A

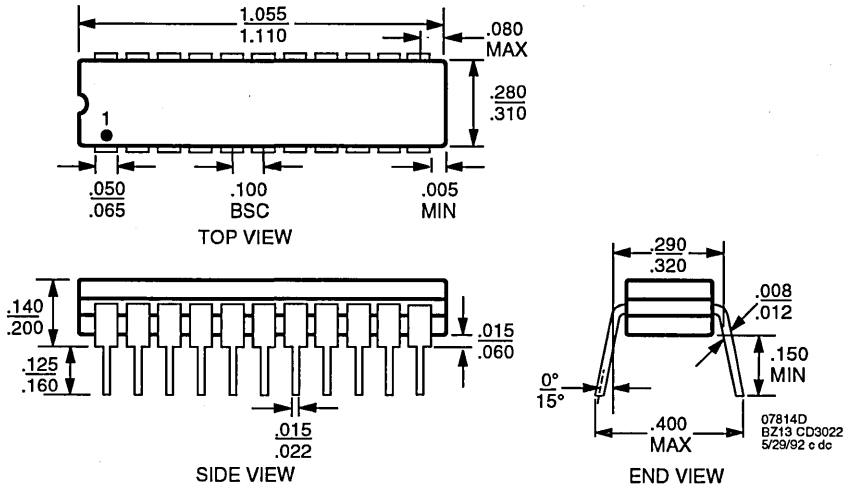
Chapter 4

Physical Dimensions

PHYSICAL DIMENSIONS

Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

CD022



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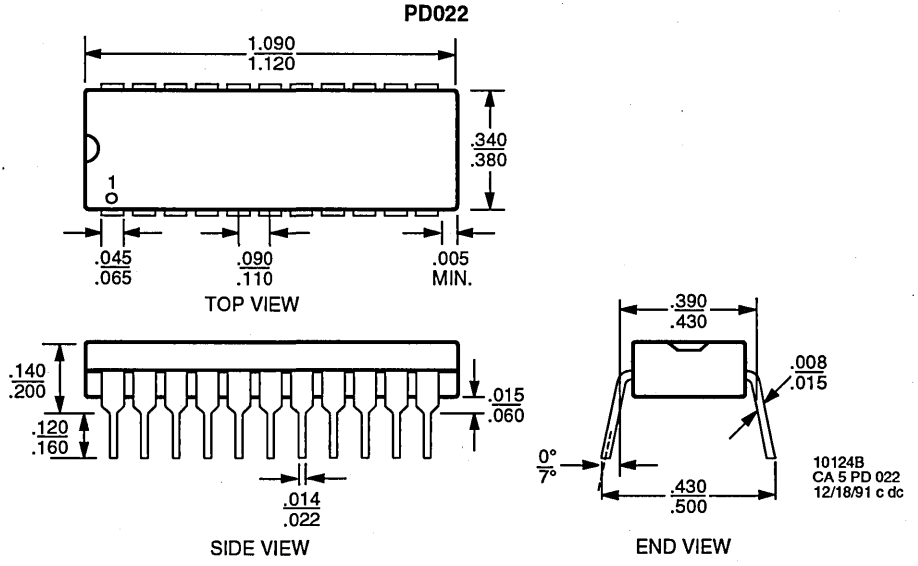

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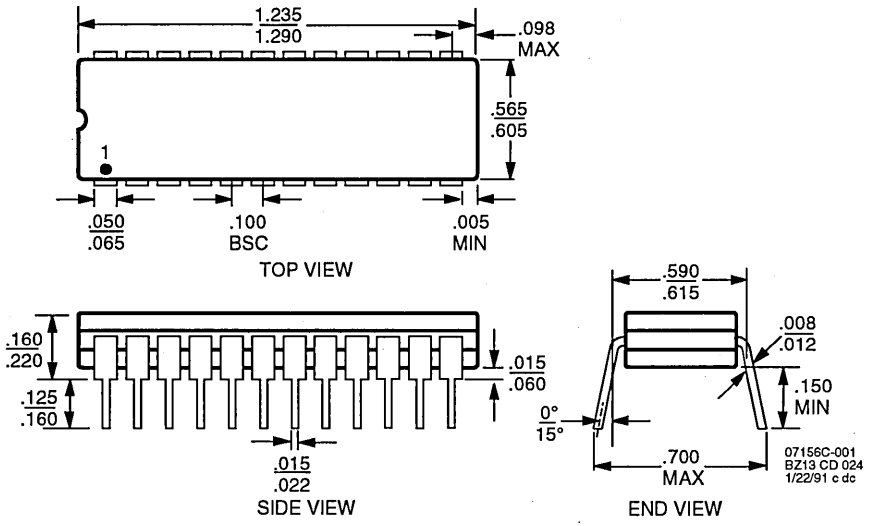
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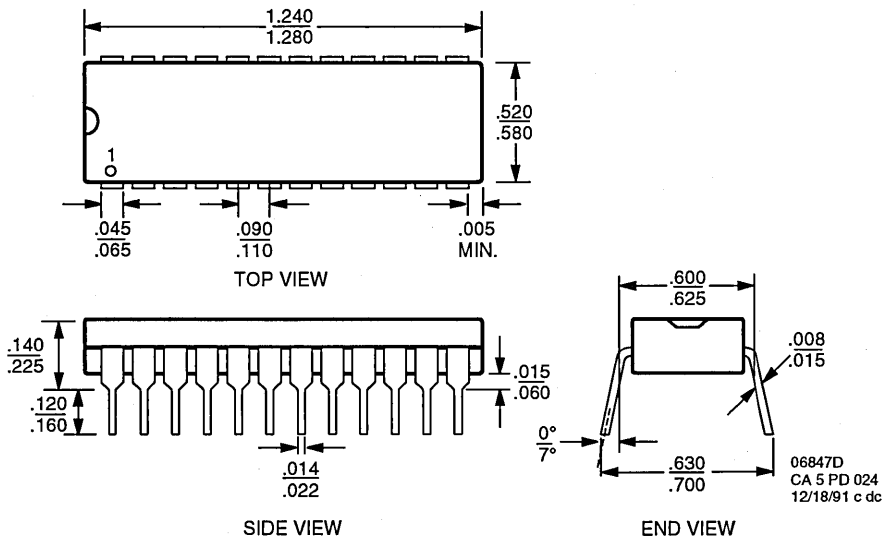
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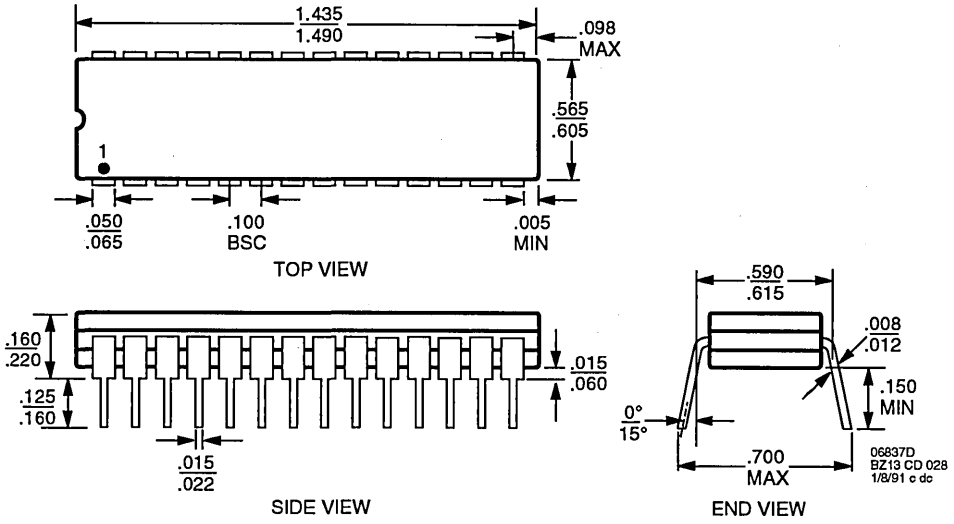
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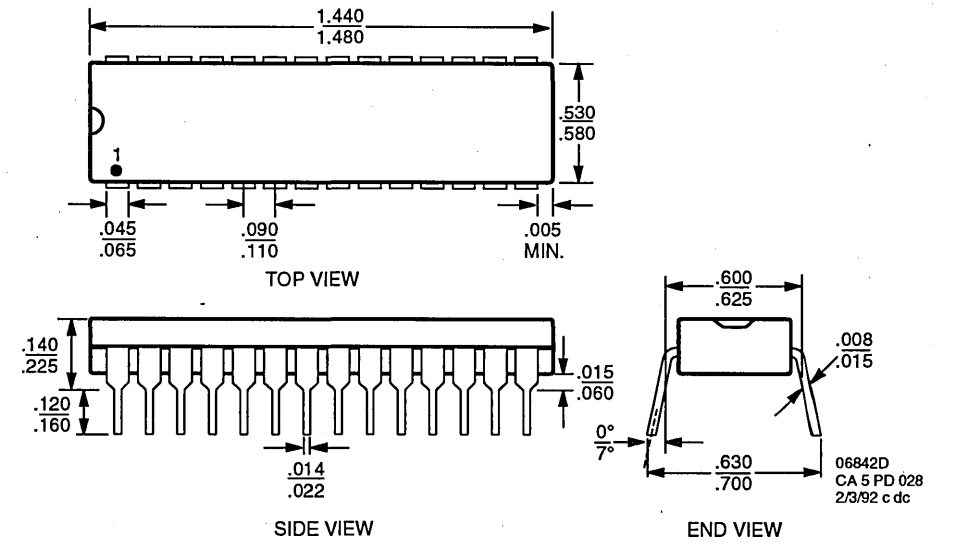
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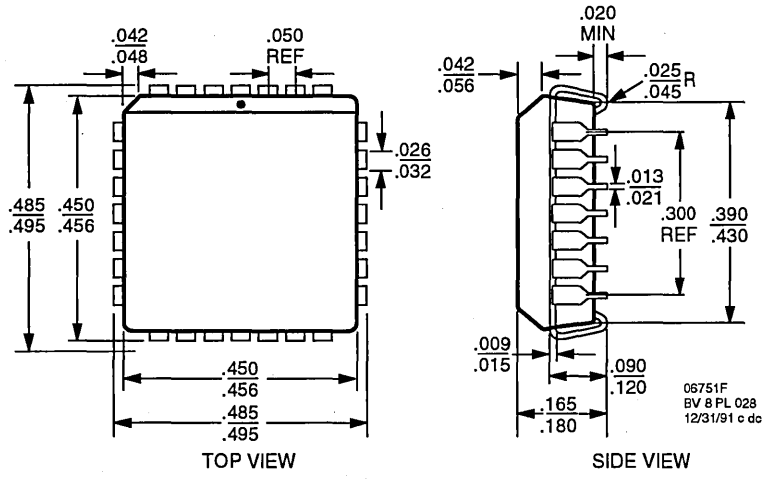
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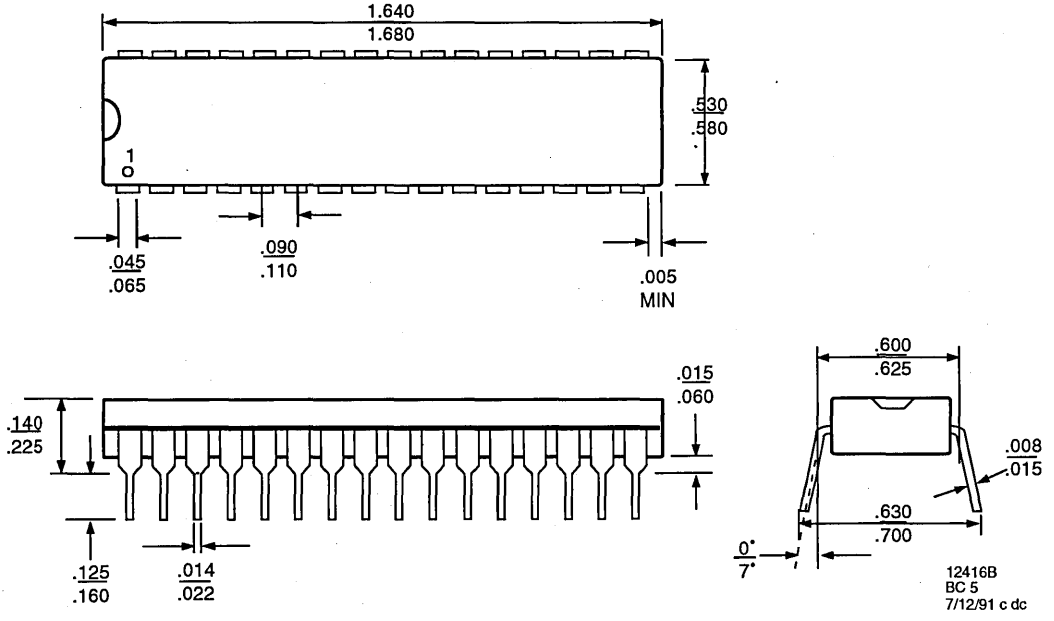
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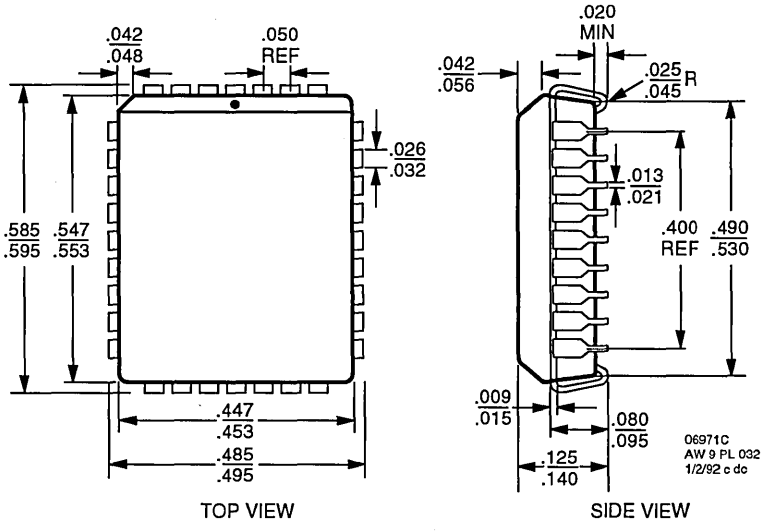
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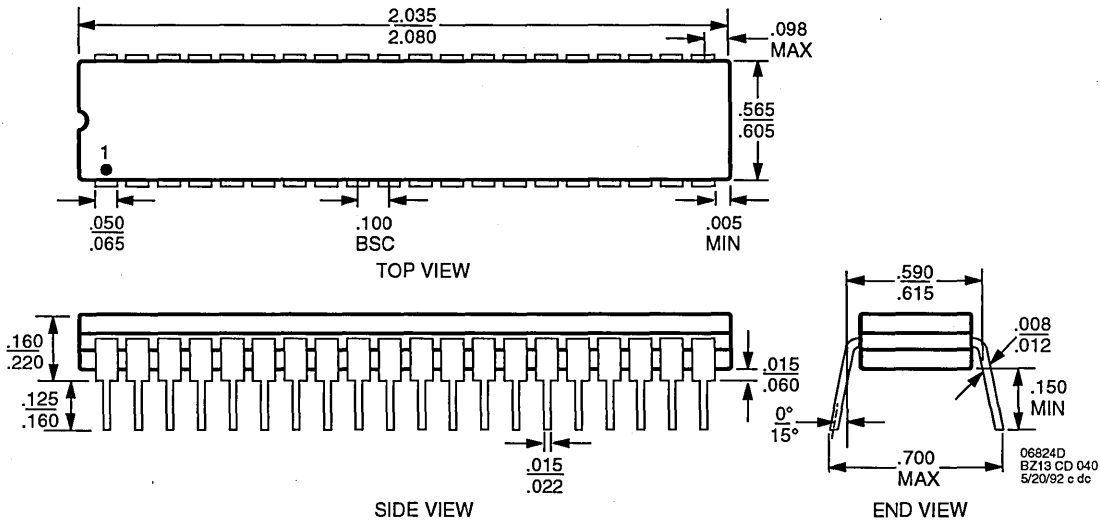
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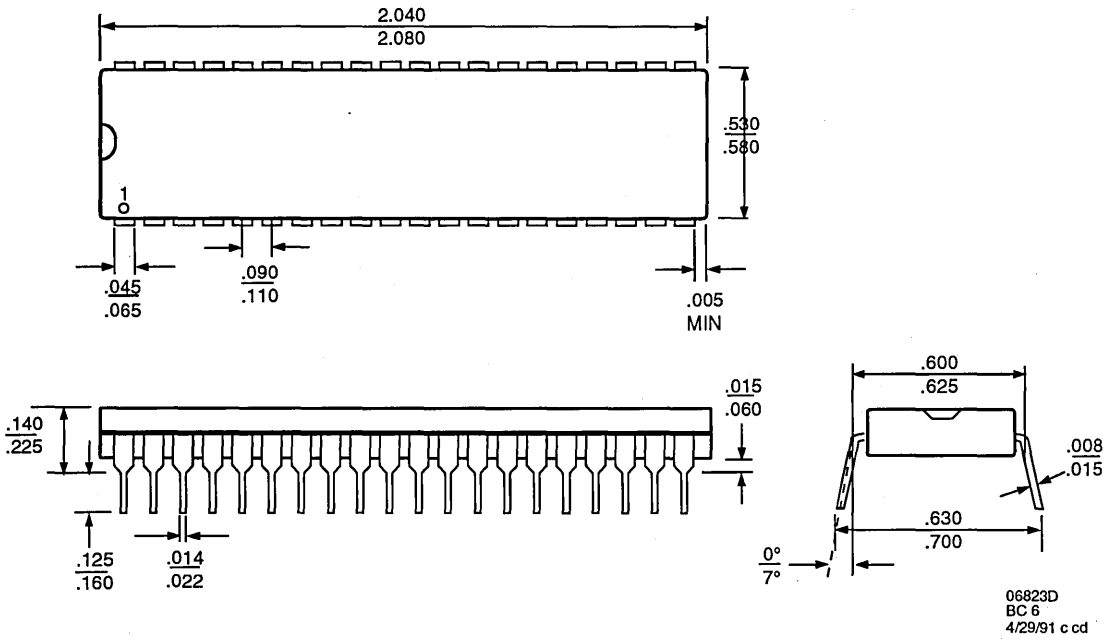
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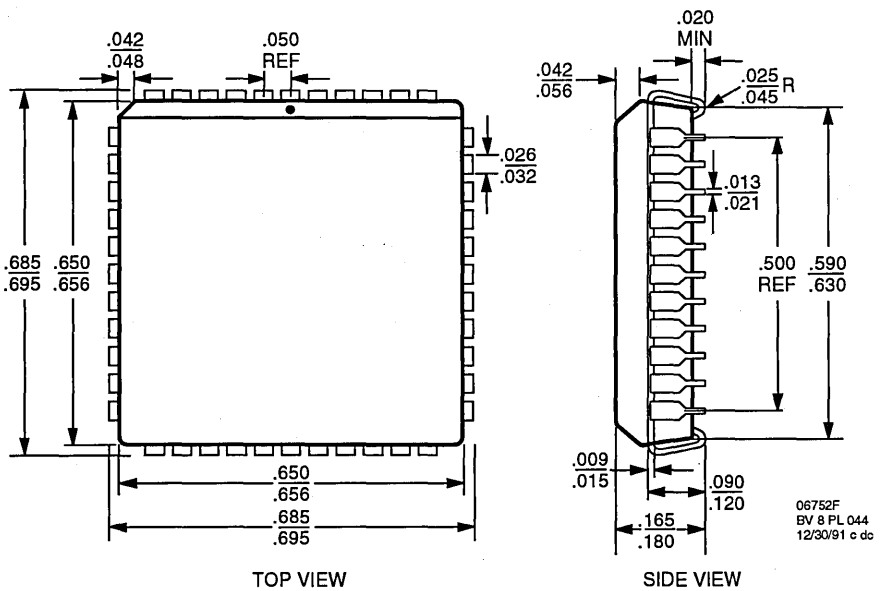
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