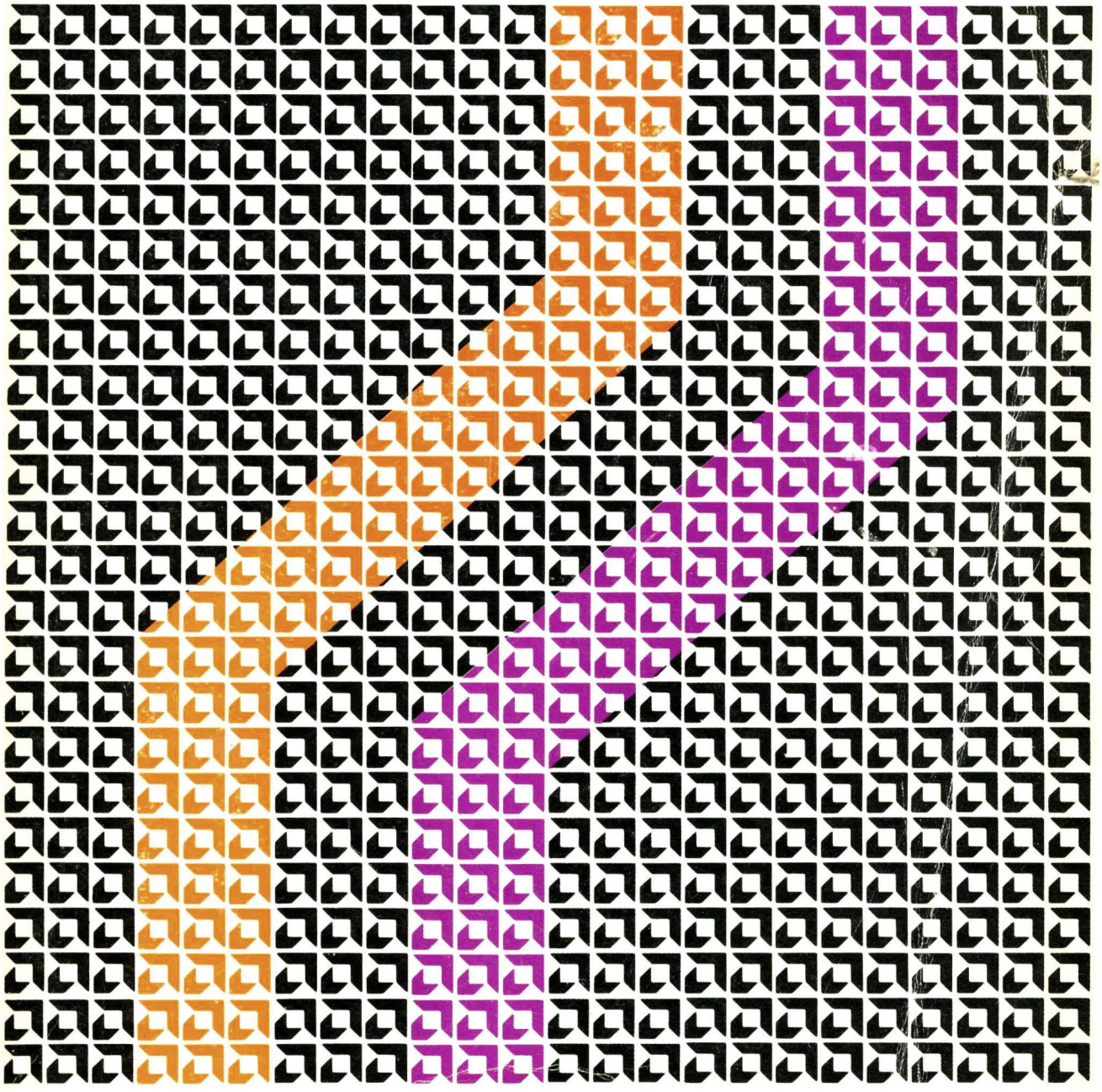
Advanced Micro Devices, Inc.

Linear And Interface Data Book



Advanced Micro Devices, Inc.

Linear And Interface Data Book

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SELECTION GUIDE

OPERATIONAL AMPLIFIERS

UNCOMPENSATED

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LM748	7-84	General Purpose, 500nA I_B, 5mV Vos
LM101A	7-5	Improved General Purpose, 75nA I_B, 2mV Vos
AM1501	7-90	Dual Improved General Purpose, 75nA I_B, 2mV Vos
LH2101A	7-99	Dual Improved General Purpose, 75nA I_B, 2mV Vos
725	7-59	Instrumentation, 100nA I_B, 1mV Vos, 0.5μV/°C TCVIO
SSS725	7-28	Improved Instrumentation, 70nA I_B, 0.1mV Vos, 0.1μV/°C TCVIO
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LM108A	7-18	Low Input Current and Offset Voltage Precision, 2nA I_B, 0.5mV Vos, 0.2nA IOS, 5μV/°C TCVIO
715	7-55	High Speed, 15V/μsec slew rate, 750nA I_B, 5mV Vos

INTERNALLY COMPENSATED

741	7-64	General Purpose, 500nA I_B, 5mV Vos
741A,E	7-64	Improved General Purpose, 80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/VPSRR
SSS741	7-64	High Performance, 50nA I_B, 2mV Vos
747	7-71	Dual General Purpose, 500nA I_B, 5mV Vos
747A,E	7-71	Dual Improved General Purpose, 80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/VPSRR
SSS747	7-71	Dual High Performance, 50nA I_B, 2mV Vos
AM1558	7-95	Dual General Purpose, 500nA I_B, 5mV Vos
LM124 LM124A	7-36	Quad General Purpose, 150nA I_B, 5mV Vos, Single or Dual Supply, 3 to 30V, 1mW/op amp at +5V
LM148	7-41	Quad 741, 500nA I_B, 5mV Vos
LM149	7-41	Quad Decompensated, 500nA I_B, 5mV Vos $A_{V(min.)} = 5$
LM107	7-14	Improved General Purpose, 75nA I_B, 2mV Vos
LM112	7-26	Low Input Current Precision, 2nA I_B, 2mV Vos
LM216	7-51	Very Low Input Current Precision, 150pA I_B, 10mV Vos
LM216A	7-51	Very Low Input Current Precision, 50pA I_B, 3mV Vos
LM118	7-30	High Speed, 50V/μsec slew rate, 4mV Vos, 250nA I_B
LF155	7-43	FET Input General Purpose, 5mV Vos, 20pA I_{OS}, 100pA I_B
LF155A	7-43	FET Input General Purpose, 2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B
LF156	7-43	FET Input Wideband, 5mV Vos, 20pA I_{OS}, 100pA I_B, 7.5V/μsec SR
LF156A	7-43	FET Input Wideband, 2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B, 10V/μsec SR
LF157	7-43	FET Input Wideband Decompensated, 5mV Vos, 20pA I_{OS}, 100pA I_B, 30V/μsec SR ($A_V = 5$)
LF157A	7-43	FET Input Wideband Decompensated, 2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B, 40V/μsec SR ($A_V = 5$)

VOLTAGE FOLLOWERS

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LM102	7-10	Low Input Current, High Speed, 10nA I_B, 5mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin
LM110	7-22	Improved Low Input Current, High Speed, 3nA I_B, 4mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin

VOLTAGE COMPARATORS

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LM111	2-5	General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
LH2111	2-38	Dual General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
AM1500	2-34	Dual General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
LM106	2-1	High Speed, 20μA I_B, 2mV Vos, 40ns Response Time, 24V and 100mA Output
LM119	2-12	Dual General Purpose, 500nA I_B, 4mV Vos, 80ns Response Time, 35V and 25mA Output, +5 or +15V Supply
LM139 LM139A	2-16	Quad General Purpose, 100nA I_B, 2mV Vos, Single or Dual Supply 2 to 36V, 1mW/comp. at +5V
AM685	2-22	Very Fast ECL Output, 10μA I_B, 2mV Vos, 6.5ns Response Time
AM686	2-30	Very Fast TTL Output, 10μA I_B, 2mV Vos, 12ns Response Time
AM687	2-32	Dual Very Fast ECL Output, 10μA I_B, 2mV Vos, 6.5ns Response Time
LF111	2-9	FET Input General Purpose, 50pA I_B, 4mV Vos, 250 Response Time, 50V and 50mA Output

VOLTAGE REGULATORS

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723	9-5	General Purpose, 2-37V Output, 0.15% load reg., 50V input, 150mA Output
LM105	9-1	General Purpose, 4.5-40V Output, 0.05% load reg., 50V input, 12mA Output

DATA CONVERSION PRODUCTS

	Page No.	
AM1508	3-7	8-Bit Multiplying D-to-A Converter, Accuracy 0.19%, Settling Time 300nsec typ.
SSS1508A	3-7	8-Bit Multiplying D-to-A Converter, Accuracy 0.1%, Settling Time 135nsec
DAC-08	3-1	

SELECTION GUIDE (Cont.)

LINE DRIVERS

DUAL DIFFERENTIAL	Page No.		Use With
75109	4-118	Open collector differential outputs, typical current 6mA, inhibit controls	75107B 75108B
75110	4-118	12mA output current version of Am75109	75107B 75108B
8830	4-129	Designed for single 5V supply operation	7820 or 7820A
8831	4-133	Dual differential device which may also be used as a quad single-ended driver. Three-state output.	9615 or 2615
8832	4-133	Similar to 8831 but no V_{CC} clamp diodes	9615 or 2615
9614	4-146	5 volt supply driver with complementary outputs	9615
9621	4-163	200mA transient capability with 130Ω back matching resistor	9620
QUAD DIFFERENTIAL EIA RS-422, FEDERAL STD 1020			
26LS31	4-14	High-speed, low output skew	26LS32 or 26LS33
SINGLE ENDED			
2614	4-33	High-speed quad driver for multichannel, common ground operation	2615
SINGLE ENDED, EIA RS-232-C			
1488	4-7	Quad EIA RS-232C driver (14 pins)	1489/ 1489A
2616	4-44	Quad 16-pin driver for EIA RS-232C, CCITT V.24 and MIL-188C interface	2617
9616	4-151	Triple EIA RS-232C driver (14 pins)	9617

LINE RECEIVERS

DUAL DIFFERENTIAL	Page No.		Use With
3603	4-1	Receiver with differential input to detect signals >25mV. Three-state outputs.	75110
2615	4-38	Receiver for 3 volt single-ended TTL level data.	2614
75107B	4-112	Totem-pole TTL output version of Am363	75109 or 75110
75108B	4-112	Open collector TTL output version of Am363	75109 or 75110
8820	4-124	Designed for ±15V common mode using 5V supply	8830
8820A	4-124	Higher speed, tighter spec 8820	8830
9615	4-38	±15 volt common mode, 5 volt supply receivers with uncommitted collector and active pull-up controls	9614
9620	4-159	±15 volt common mode receiver with direct and attenuated inputs	9621
QUAD DIFFERENTIAL EIA RS-422, FEDERAL STD 1020			
26LS32	4-18	±7 volt common mode, 5 volt supply, three state output	26LS31
26LS33	4-18	±15 volt common mode, 5 volt supply, three-state output	26LS31
SINGLE ENDED, EIA-RS-232-C			
1489	4-10	Quad EIA RS-232C receiver with input threshold hysteresis	1488
1489A	4-10	Higher threshold version of Am1489	1488
2617	4-48	Quad EIA RS-232 receiver specified over military temperature range (same pinout as Am1489A)	2616
9617	4-155	Triple EIA RS-232 receiver with adjustable hysteresis	9616

OCTAL BUFFER/DRIVER

	Page No.	
†74S240	4-107	Inverting octal buffer/driver with three state output
†74S241	4-107	Non-inverting octal buffer/driver with three state output
†74S242	4-107	Inverting buffer/driver with two quad data paths connected input-to-output
†74S243	4-107	Non-inverting buffer/driver with two quad data paths connected input-to-output
†74S244	4-107	Non-inverting octal buffer/driver with three state output and two inverting enables

SELECTION GUIDE (Cont.)

CORE MEMORY

DRIVERS	Page No.	
75325	5-35	Dual high-speed, 600mA, 24V output
SENSE AMPLIFIERS		
7520	5-1	Dual high-speed, ±4mV threshold, complementary outputs
7521	5-1	±7mV version 7520
75234	5-11	Dual high speed, ±4mV threshold, internally compensated
75235	5-11	±7mV version 75234
75238	5-19	Dual high-speed, ±4mV threshold sense amplifiers with test points, internally compensated
75239	5-19	±7mV version 75238
7524	5-27	Dual high-speed, ±4mV threshold, separate outputs
7525	5-27	±7mV version 7524

SPECIAL FUNCTIONS

WIDEBAND AMPLIFIERS	Page No.	
733	8-12	Differential Input and Output, 40-120MHz B. W., 100-400 Voltage Gain
Am592	8-9	Differential Input and Output, 40-120MHz B. W., 100-400 Voltage Gain
TIMERS		
555	8-1	Single, Precision oscillator/timer
556	8-5	Dual version 555

MOS-MICROPROCESSOR INTERFACE CIRCUITS

8080A/9080A	Page No.	
8212	4-94	8-Bit input/output port, with storage
8216	4-102	4-Bit parallel bidirectional bus driver
8224	6-25	Clock generator and driver
8226	4-102	Inverting version 8216
8228	6-30	System controller and bus driver
8238	6-30	System controller and bus driver with extended IOW/MEMW

MOS MEMORY

DRIVERS	Page No.	
0026	6-1	Dual 5MHz Two-Phase MOS clock driver
0056	6-7	0026 with added V_{BB} terminal
SENSE AMPLIFIERS		
3604	6-13	Differential input for signals > 10mV, Three-state outputs
75207	6-19	Totem-pole TTL output 3604
75208	6-19	Open-collector output 3604

QUAD BUS TRANSCEIVERS

Device	Page No.	Output	Function	Hysteresis	Speed (Note 1)	Comments
Am26S10	4-23	100mA-O.C.	Inverting	No	20ns	SN55/75138 pin out
Am26S11	4-23	100mA-O.C.	Non-Inverting to bus; Inverting off bus	No	22ns	Same as Am26S10 except non-inverting to bus
Am26S12	4-28	100mA-O.C.	Inverting	Yes-.6V	32ns	Same pin out as DS78/8838 and 8T38
Am26S12A	4-28	100mA-O.C.	Inverting	Yes-1.05V	32ns	Wider threshold Am26S12
Am2905	4-52	100mA-O.C.	Inverting	No	31ns (note 2)	Has 2-input multiplexer
Am2906	4-59	100mA-O.C.	Inverting	No	31ns (note 2)	Has 2-input multiplexer and parity
Am2907	4-66	100mA-O.C.	Inverting	No	31ns (note 2)	Includes parity
Am2915A	4-73	48mA/3-St.	Inverting	No	31ns (note 2)	Has 2-input multiplexer
Am2916A	4-80	48mA/3-St.	Inverting	No	31ns (note 2)	Has 2-input multiplexer and parity
Am2917A	4-87	48mA/3-St.	Inverting	No	31ns (note 2)	Includes parity
Am3216	4-103	50mA/3-St.	Non-Inverting	No	34ns	Same as 8216 except different A.C. loading spec
Am3226	4-103	50mA/3-St.	Inverting	No	30ns	Same as 8216 except different A.C. loading spec
Am78/8838	4-139	50mA-O.C.	Inverting	No	38ns	Same pin out and function as Am26S12A and 8T38
Am8T26A	4-141	48mA/3-St.	Inverting	No	19ns	V_{OH} MOS compatible
Am8T28 (note 3)	4-141	48mA/3-St.	Non-Inverting	No	25ns	V_{OH} MOS compatible
Am8216	4-102	50mA/3-St.	Non-Inverting	No	34ns	Similar to 8T28
Am8226	4-102	50mA/3-St.	Non-Inverting	No	30ns	Similar to 8T26A

Notes: 1. Typical delay at 25°C for input to bus plus receiver to output.
2. Bus enable to bus plus bus to receiver output. All parts include register or driver plus receiver with latch.
3. To be announced.

SELECTION GUIDE (Cont.)

MONOSTABLES (ONE SHOTS)

Device No.	Description	Dual	Retri-gerable	Reset Table	Initial Accuracy %	Min. Output t_{pw}(ns)	Pulse Width Variation (%) Temp.	V_{CC}	Power Dissipation (mW typ.)	No. Package Leads
Am25LS123	Low-Power Schottky version 26123	X	X	X	±10	116	±2.5	±1.0	60	16
Am2600	t_{pw} = 55ns to ∞, with guaranteed < 1% change over temperature range	X	X	X	±10	45	±0.5	±1.5	95	14
Am2602	t_{pw} = 55ns to ∞, with guaranteed < 1% change over temperature range	X	X	X	±10	45	±0.5	±1.5	175	16
Am26L02	Low-Power version 2602, t_{pw} = 100ns to ∞	X	X	X	±10	110	±0.3	±1.0	50	16
Am26L123	Low-Power version 26123, t_{pw} = 120ns to ∞	X	X	X	±10	120	±0.3	±1.0	60	16
Am26S02	High speed Schottky version 2602, t_{pw} = 28ns to ∞	X	X	X	±5	33	±0.4	±1.5	240	16
Am26123	t_{pw} = 45ns to ∞, with guaranteed < 1% change over temperature range. Output stability latch improves noise immunity	X	X	X	±10	45	±0.5	±0.5	230	16
Am54/74LS123	Same as 25LS123, except no output latch, no Δt_{pw} guarantee	X	X	X	±10	116	±3.0	±1.0	60	16
Am54/74123	Same as 26123, except no output latch, no Δt_{pw} guarantee	X	X	X	±10	45	±2.7	±1.0	230	16
Am54/74221	Schmitt-trigger input	X		X	±7	30	±0.3	±0.3	130	16
Am9600	Same as 2600, except no Δt_{pw} guarantee		X	X	±10	50	±1.5	±1.5	95	14
Am9601	Non-resettable version of 9600, t_{pw} = 55ns to ∞		X		±10	45	±2.7	±1.0	95	14
Am9602	Same as 2602, except t_{pw} = 60ns to ∞, no Δt_{pw} guarantee	X	X	X	±10	50	±1.5	±1.5	175	16
Am96L02	Same as 26L02, except t_{pw} guaranteed <1.6% change over temperature range	X	X	X	±10	110	±0.3	±0.5	50	16

Note: Contact your AMD sales office for full data.

INDUSTRY CROSS REFERENCE

AMD*	Fairchild	Intel	Motorola	National	Signetics	Texas Instruments

Manufacturer Identification Cross Reference

AM	μA, or None	None	M, MC	DM, DS, LM, MH	None	SN

Temperature Range Cross Reference

Commercial	C	C	–	14, 34, 86	3, 86, 88	NE, N	72, 74, 75
Military	M	M	M	15, 35, 96	1, 96, 78	SE, S	52, 54, 55

Package Cross Reference

Hermetic DIP	D	D	C, D	L	D	F, I	J
Molded DIP	P	P	P	P_2	N	A, B	N
Mini-Molded DIP	T	T	–	P_1	N	V	P
Flat Pack	F	F	–	F	F, W	W, Q	H, U, Z, W
TO-5 Type Can	H	H	–	G, R	H	DB, K, T	L
TO-8 Type Can	G	–	–	H	G	–	–

*The original manufacturers part number and package code are used for second source devices.

FAIRCHILD

9614 D M

Device Type | Package Type | Temperature Range

Fairchild	AMD Direct Replacement	AMD Functional Replacement
μA101D	LM101D	
μA101H	LM101H	
μA101AD	LM101AD	
μA101AF	LM101AF	
μA101AH	LM101AH	
μA102H	LM102H	
μA105H	LM105H	
μA107H	LM107H	
μA108AH	LM108AH	
μA108H	LM108H	
μA110H	LM110H	
μA111H	LM111H	
μA139D	LM139D	
μA1458H	AM1458H	
μA1558H	AM1558H	
μA201D	LM201D	
μA201H	LM301H	
μA201AD	LM201AD	
μA201AF	LM201AF	
μA201AH	LM201AH	
μA207H	LM207H	
μA208H	LM208H	
μA208AH	LM208AH	
μA301AD	LM301AD	
μA301AH	LM301AH	
μA301AN	LM301AN	
μA302H	LM302H	
μA305H	LM305H	
μA305AH	LM305AH	
μA307H	LM307H	
μA308H	LM308H	
μA308AH	LM308AH	
μA310H	LM310H	
μA311H	LM311H	

FAIRCHILD (Cont.)

μA 556 D M

Mfg's Ident. | Device Type | Package Type | Temperature Range

Fairchild	AMD Direct Replacement	AMD Functional Replacement
μA311P	LM311N	
μA339D	LM339D	
μA339P	LM339N	
μA555HC	NE555T	
μA555HM	SE555T	
μA555TC	NE555V	
μA556DC	NE556F	
μA556DM	SE556F	
μA556PC	NE556	
μA715DC	715DC	
μA715DM	715DM	
μA715HC	715HC	
μA715HM	715HM	
μA723DC	723DC	
μA723DM	723DM	
μA723HC	723HC	
μA723HM	723HM	
μA725HC	725HC	
μA725HM	725HM	
μA725PC	725CN	
μA733DC	733DC	
μA733DM	733DM	
μA733FM	733FM	
μA733HC	733HC	
μA733HM	733HM	
μA741DC	741DC	
μA741DM	741DM	
μA741FM	741FM	
μA741HC	741HC	
μ741HM	741HM	
μA741ADM	741ADM	
μA741AFM	741AFM	
μA741AHM	741AHM	
μA741EDC	741EDC	

INDUSTRY CROSS REFERENCE

FAIRCHILD (Cont.)

Fairchild	AMD Direct Replacement	AMD Functional Replacement
μA741EHC	741EHC	
μA747DC	747DC	
μA747DM	747DM	
μA747HC	747HC	
μA747HM	747HM	
μA747PC	747PC	
μA747ADM	747ADM	
μA747AHM	747AHM	
μA747EDC	747EDC	
μA747EHC	747EHC	
μA748DC	748DC	
μA748DM	748DM	
μA748FM	748FM	
μA748HC	748HC	
μA748HM	748HM	
μA748PC	748PC	
μA760DC		AM686DC
μA760DM		AM686DM
μA760HC		AM686HC
μA760HM		AM686HM
μA775DM	LM139D	
μA775DC	LM339D	
μA775PC	LM339N	
54123DM	SN54123J	
54123FM	SN54123W	
55107ADM	SN55107BJ	
55107BDM	SN55107BJ	
55107AFM	SN55107BW	
55107BFM	SN55107BW	
55108ADM	SN55108BJ	
55108AFM	SN55108BW	
55108BDM	SN55108BJ	
55108BFM	SN55108BW	
55109DM	SN55109J	
55109FM	SN55109W	
55110DM	SN55110J	
55110FM	SN55110W	
5520DM	SN5520J	
5521DM	SN5521J	
55234DM	SN55234J	
55234FM	SN55234W	
55235DM	SN55235J	
55235FM	SN55235W	
55238DM	SN55238J	
55238FM	SN55238W	
55239DM	SN55239J	
55239FM	SN55239W	
5524DM	SN5524J	
5525DM	SN5525J	
55325DM	SN55325J	
55325FM	SN55325W	
74123DC	SN74123J	
74123PC	SN74123N	
75107ADC	SN75107BJ	
75107APC	SN75107BN	
75107BDC	SN75107BJ	
75107BPC	SN75107BN	
75108ADC	SN75108BJ	
75108APC	SN75108BN	
75108BDC	SN75108BJ	
75108BPC	SN75108BN	
75109DC	SN75109J	
75109PC	SN75109N	
75110DC	SN75110J	

FAIRCHILD (Cont.)

Fairchild	AMD Direct Replacement	AMD Functional Replacement
75110PC	SN75110N	
7520DC	SN7520J	
7520PC	SN7520N	
75207DC	SN75207J	
75207PC	SN75207N	
75208DC	SN75208J	
75208PC	SN75208N	
7521DC	SN7521J	
7521PC	SN7521N	
75234DC	SN75234J	
75234PC	SN75234N	
75235DC	SN75235J	
75235PC	SN75235N	
75238DC	SN75238J	
75238PC	SN75238N	
75239DC	SN75239J	
75239PC	SN75239N	
7524DC	SN7524J	
7524PC	SN7524N	
7525DC	SN7525J	
7525PC	SN7525N	
75325DC	SN75325J	
75325PC	SN75325N	
9600DC	9600DC	
9600DM	9600DM	
9600FM	9600FM	
9600PC	9600PC	
9601DC	9601DC	
9601DM	9601DM	
9601FM	9601FM	
9601PC	9601PC	
9602DC	9602DC	
9602DM	9602DM	
9602FM	9602FM	
9602PC	9602PC	
96L02DC	96L02DC	
96L02DM	96L02DM	
96L02FM	96L02FM	
96L02PC	96L02PC	
96S02DC		AM26S02DC
96S02PC		AM26S02PC
9614DC	9614DC	
9614DM	9614DM	
9614FM	9614FM	
9614PC	9614PC	
9615DC	9615DC	
9615DM	9615DM	
9615FM	9615FM	
9615PC	9615PC	
9616DC	9616DC	
9616DM	9616DM	
9616EDC	9616EDC	
9616EPC	9616EPC	
9616FM	9616FM	
9616PC	9616PC	
9617DC	9617DC	
9617PC	9617PC	
9620DC	9620DC	
9620DM	9620DM	
9620FM	9620FM	
9620PC	9620PC	
9621DC	9621DC	
9621DM	9621DM	
9621FM	9621FM	

INDUSTRY CROSS REFERENCE

FAIRCHILD (Cont.)

Fairchild	AMD Direct Replacement	AMD Functional Replacement
9621PC	9621PC	
9640DC	AM26S10DC	
9640DM	AM26S10DM	
9640PC	AM26S10PC	
9641DC	AM26S11DC	
9641DM	AM26S11DM	
9641PC	AM26S11PC	

INTEL

/ D8228

Temperature Range — Package Type — Device Type

Intel	AMD Direct Replacement	AMD Functional Replacement
D3212	D3212	
MD3212	MD3212	
P3212	P3212	
D3216	D3216	N8T28F
MD3216	MD3216	S8T28F
P3216	P3216	N8T28B
D3226	D3226	N8T26F
MD3226	MD3226	S8T26F
P3226	P3226	N8T26B
D8212	D8212	
MD8212	AM8212DM	
P8212	AM8212PC	
D8216	D8216	N8T28F
MD8216	MD8216	S8T28F
P8216	P8216	N8T28B
D8224	D8224	
MD8224	AM8224DM	
P8224	AM8224PC	
D8226	D8226	N8T26F
MD8226	MD8226	S8T26F
P8226	P8226	N8T26B
D8228	D8228	
MD8228	AM8228DM	
P8228	AM8228PC	
D8238	D8238	
MD8238	AM8238DM	
P8238	AM8238PC	

MOTOROLA

MC 14 88 L

/lfg's dent. — Temperature Range — Device Type — Package Type

Motorola	AMD Direct Replacement	AMD Functional Replacement
MC1408L6	AM1408L6	
MC1408L7	AM1408L7	
MC1408L8	AM1408L8	
MC1455G	NE555T	
MC1455PI	NE555V	
MC1458G	AM1458H	
MC1488L	MC1488L	
MC1488P	AM1488PC	

MOTOROLA (Cont.)

Motorola	AMD Direct Replacement	AMD Functional Replacement
MC1489L	MC1489L	
MC1489P	AM1489PC	
MC1489AL	MC1489AL	
MC1489AP	AM1489APC	
MC1508L8	AM1508L8	
MC1555G	SE555T	
MC1558G	AM1558H	
MC1723CG	723HC	
MC1723CL	723DC	
MC1723G	723HM	
MC1723L	723DM	
MC1733CG	733HC	
MC1733CL	733DC	
MC1733F	733FM	
MC1733G	733HM	
MC1733L	733DM	
MC1741CG	741HC	
MC1741CL	741DC	
MC1741F	741FM	
MC1741G	741HM	
MC1741L	741DM	
MC1747CG	747HC	
MC1747CL	747DC	
MC1747G	747HM	
MC1747L	747DM	
MC1748CG	748HC	
MC1748G	748HM	
MC26S10L	AM26S10DC	
MC26S10P	AM26S10PC	
MC3438L		AM26S12ADC
MC3438P		AM26S12APC
MC3443L		AM26S10DC
MC3443P		AM26S10PC
MC3456L	NE556F	
MC3456P	NE556A	
MC3486L		AM26LS31DC
MC3486P		AM26LS31PC
MC3487L		AM26LS32DC
MC3487P		AM26LS32PC
MC3556L	SE556F	
MC55107L	SN55107BJ	
MC55108L	SN55108BJ	
MC55109L	SN55109J	
MC55110L	SN55110J	
MC5524L	SN5524J	
MC5525L	SN5525J	
MC55325L	SN55325J	
MC75107L	SN75107BJ	
MC75107P	SN75107BN	
MC75108L	SN75108BJ	
MC75108P	SN75108BN	
MC75109L	SN75109J	
MC75109P	SN75109N	
MC75110L	SN75110J	
MC75110P	SN75110N	
MC7524L	SN7524J	
MC7524P	SN7524N	
MC7525L	SN7525J	
MC7525P	SN7525N	
MC75325L	SN75325J	
MC75325P	SN75325N	
MC8T26L	N8T26F	
MC8T26P	N8T26B	
MC8601L	9601DC	

INDUSTRY CROSS REFERENCE

MOTOROLA (Cont.)

Motorola	AMD Direct Replacement	AMD Functional Replacement
MC8601P	9601PC	
MC8602L	9602DC	AM2602DC
MC8602P	9602PC	AM2602PC
MC9601L	9601DM	AM2602DM
MC9602L	9602DM	AM2602DM
MLM101AG	LM101AH	
MLM105G	LM105H	
MLM107G	LM107H	
MLM110G	LM110H	
MLM111F	LM111F	
MLM111G	LM111H	
MLM111L	LM111D	
MLM201AG	LM210AH	
MLM205G	LM205H	
MLM207G	LM207H	
MLM210G	LM210H	
MLM211G	LM211H	
MLM211L	LM211D	
MLM301AG	LM301AH	
MLM301API	LM301AN	
MLM305G	LM305H	
MLM307G	LM307H	
MLM310G	LM310H	
MLM311G	LM311H	
MLM211PI	LM311N	
MLM311L	LM311D	
MMH0026CG	MH0026CH	
MMH0026CL	MMH0026CL	
MMH0026CPI	MH0026CN	
MMH0026G	MH0026H	
MMH0026L	MMH0026L	

NATIONAL

DS 78 20 J

Mfg's Ident. — Temperature Range — Device Type — Package Type

National	AMD Direct Replacement	AMD Functional Replacement
DM54123J	SN54123J	
DM54123W	SN54123W	
DM54L123J		AM26L123DM
DM54L123W		AM26L123FM
DM71LS95J		†SN54LS241J
DM71LS96J		†SN54LS240J
DM71LS97J		†SN54LS244J
DM71LS98J		†SN54LS240J
DM74L123J		AM26L123DC
DM74L123N		AM26L123PC
DM74123J	SN74123J	AM26123DC
DM74123N	SN74123N	AM26123PC
DM81LS95J		†SN74LS240J
DM81LS95N		†SN74LS240N
DM81LS96J		†SN74LS241J
DM81LS96N		†SN74LS241N
DM81LS97J		†SN74LS241J
DM81LS97N		†SN74LS241N
DM81LS98J		†SN74LS240J
DM81LS98N		†SN74LS240N
DM8601J	9601DC	
DM8601N	9601PC	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
DM8602J	9602DC	AM2602DC
DM8602N	9602PC	AM2602PC
DM9601J	9601DM	
DM9601W	9601FM	
DM9602J	9602DM	AM2602DM
DM9602W	9602FM	AM2602FM
DS0026CG	MH0026CJ	
DS0026CH	MH0026CH	
DS0026CJ	MMH0026CL	
DS0026CN	MH0026CN	
DS0026F	DS0026F	
DS0026G	MH0026G	
DS0026H	MH0026H	
DS0026J	MMH0026L	
DS0056CG	DS0056CG	
DS0056CH	DS0056CH	
DS0056CJ	DS0056CJ	
DS0056CN	DS0056CN	
DS0056G	DS0056G	
DS0056H	DS0056H	
DS0056J	DS0056J	
DS1488J	MC1488L	
DS1488N	AM1488PC	
DS1489J	MC1489L	
DS1489N	AM1489L	
DS1489AJ	MC1489AL	
DS1489AN	AM1489APC	
DS1603J	DS1603J	
DS3603J	DS3603J	
DS3603N	DS3603N	
DS3604J	DS3604J	
DS3604N	DS3604N	
DS7820J	DM7820J	
DS7820AJ	DM7820AJ	
DS7830J	DM7830J	
DS7831J	DM7831J	
DS7832J	DM7832J	
DS7835J		S8T26F
DS7838J	DS7838J	AM26S12ADM
DS8820J	DM8820J	
DS8820N	DM8820N	
DS8820AJ	DM8820AJ	
DS8820AN	DM8820AN	
DS8830J	DM8830J	
DS8830N	DM8830N	
DS8831J	DM8831J	
DS8831N	DM8831N	
DS8832J	DM8832J	
DS8832N	DM8832N	
DS8835J		N8T26F
DS8835N		N8T26B
DS8838J	DS8838J	AM26S12ADC
DS8838N	DS8838N	AM26S12APC
DS55107J	SN55107BJ	
DS55108J	SN55108BJ	
DS55109J	SN55109J	
DS55110J	SN55110J	
DS5520J	SN5520J	
DS5521J	SN5521J	
DS5524J	SN5524J	
DS5525J	SN5525J	
DS55325J	SN55325J	
DS75107J	SN75107BJ	
DS75107N	SN75107BN	

INDUSTRY CROSS REFERENCE

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
DS75108J	SN75108BJ	
DS75108N	SN75108BN	
DS75109J	SN75109J	
DS75109N	SN75109N	
DS75110J	SN75110J	
DS75110N	SN75110N	
DS7520J	SN7520J	
DS7520N	SN7520N	
DS75207J	SN75207J	
DS75207N	SN75207N	
DS75208J	SN75208J	
DS75208N	SN75208N	
DS7521J	SN7521J	
DS7521N	SN7521N	
DS7524J	SN7524J	
DS7524N	SN7524N	
DS7525J	SN7525J	
DS7525N	SN7525N	
DS75325J	SN75325J	
DS75325N	SN75325N	
LF111D, J	LF111D	
LF111F	LF111F	
LF111H	LF111H	
LF155H	LF155H	
LF155AH	LF155AH	
LF156H	LF156H	
LF156AH	LF156AH	
LF157H	LF157H	
LF157AH	LF157AH	
LF198H	LF198H	
LF211D, J	LF211D	
LF211F	LF211F	
LF211H	LF211H	
LF255H	LF255H	
LF256H	LF256H	
LF257H	LF257H	
LF298H	LF298H	
LF311D	LF311D	
LF311H	LF311H	
LF355H	LF355H	
LF355N	LF355N	
LF355AH	LF355AH	
LF356H	LF356H	
LF356N	LF356N	
LF356AH	LF356AH	
LF357H	LF357H	
LF357N	LF357N	
LF357AH	LF357AH	
LF398H	LF398H	
LH2101AD, J	LH2101AD	
LH2101AF	LH2101AF	
LH2111D, J	LH2111D	
LH2111F	LH2111F	
LH2201AD, J	LH2201AD	
LH2201AF	LH2201AF	
LH2211D, J	LH2211D	
LH2211F	LH2211F	
LH2301AD, J	LH2301AD	
LH2311D, J	LH2311D	
LM101D, J	LM101D	
LM101F	LM101F	
LM101H	LM101H	
LM101AD, J	LM101AD	
LM101AF	LM101AF	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LM101AH	LM101AH	
LM102D, J	LM102D	
LM102F	LM102F	
LM102H	LM102H	
LM105F	LM105F	
LM105H	LM105H	
LM106F	LM106F	
LM106H	LM106H	
LM107D, J	LM107D	
LM107F	LM107F	
LM107H	LM107H	
LM108D, J	LM108D	
LM108F	LM108F	
LM108H	LM108H	
LM108AD, J	LM108AD	
LM108AF	LM108AF	
LM108AH	LM108AH	
LM110D, J	LM110D	
LM110F	LM110F	
LM110H	LM110H	
LM111D, J	LM111D	
LM111F	LM111F	
LM111H	LM111H	
LM112D, J	LM112D	
LM112F	LM112F	
LM112H	LM112H	
LM118D, J	LM118D	
LM118F	LM118F	
LM118H	LM118H	
LM119D, J	LM119D	
LM119F	LM119F	
LM119H	LM119H	
LM124D, J	LM124D	
LM124F	LM124F	
LM139D, J	LM139D	
LM139AD, J	LM139AD	
LM139F	LM139F	
LM139AF	LM139AF	
LM148D	LM148D	
LM149D	LM149D	
LM201H	LM301H	
LM201AD, J	LM201AD	
LM201AF	LM201AF	
LM201AH	LM201AH	
LM202H	LM202H	
LM205H	LM205H	
LM206H	LM206H	
LM207D, J	LM207D	
LM207F	LM207F	
LM207H	LM207H	
LM208AD, J	LM208AD	
LM208AF	LM208AF	
LM208AH	LM208AH	
LM208D, J	LM208D	
LM208F	LM208F	
LM208H	LM208H	
LM210D, J	LM210D	
LM210H	LM210H	
LM211D, J	LM211D	
LM211F	LM211F	
LM211H	LM211H	
LM212D, J	LM212D	
LM212F	LM212F	
LM212H	LM212H	

INDUSTRY CROSS REFERENCE

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LM216AD, J	LM216AD	
LM216AF	LM216AF	
LM216AH	LM216AH	
LM216D, J	LM216D	
LM216F	LM216F	
LM216H	LM216H	
LM218D, J	LM218D	
LM218F	LM218F	
LM218H	LM218H	
LM219D, J	LM219D	
LM219F	LM219F	
LM219H	LM219H	
LM224D, J	LM224D	
LM239D, J	LM239D	
LM239AD, J	LM239D	
LM248D	LM248D	
LM249D	LM249D	
LM301AD, J	LM301AD	
LM301AF	LM301AF	
LM301AH	LM301AH	
LM301AN	LM301AN	
LM302F	LM302F	
LM302H	LM302H	
LM305F	LM305F	
LM305H	LM305H	
LM305AH	LM305AH	
LM306F	LM306F	
LM306H	LM306H	
LM307D, J	LM307D	
LM307F	LM307F	
LM307H	LM307H	
LM308AD, J	LM308AD	
LM308AF	LM308AF	
LM308AH	LM308AH	
LM308AN	LM308AN	
LM308D, J	LM308D	
LM308F	LM308F	
LM308H	LM308H	
LM308N	LM308N	
LM310D, J	LM310D	
LM310F	LM310F	
LM310H	LM310H	
LM310N	LM310N	
LM311D, J	LM311D	
LM311F	LM311F	
LM311N	LM311N	
LM312D, J	LM312D	
LM312F	LM312F	
LM312H	LM312H	
LM316AD, J	LM316AD	
LM316AF	LM316AF	
LM316AH	LM316AH	
LM316D, J	LM316D	
LM316F	LM316F	
LM316H	LM316H	
LM318D, J	LM318D	
LM318F	LM318F	
LM318H	LM318H	
LM318N	LM318N	
LM319H	LM319H	
LM319D, J	LM319D	
LM319N	LM319N	
LM324D, J	LM324D	
LM324N	LM324N	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LM339D, J	LM339D	
LM339AD, J	LM339AD	
LM339N	LM339N	
LM339AN	LM339AN	
LM348D	LM348D	
LM348N	LM348N	
LM349D	LM349D	
LM349N	LM349N	
LM555CH	NE555T	
LM555CN	NE555V	
LM555H	SE555T	
LM556CJ	NE556F	
LM556CN	NE556A	
LM556J	SE556F	
LM723D, J	723DM	
LM723H	723HM	
LM723CD, J	723DC	
LM723CH	723HC	
LM725H	725HM	
LM725CH	725HC	
LM725CN	725CN	
LM725D, J	725DM	
LM725CD, J	725DC	
LM733D, J	733DM	
LM733H	733HM	
LM733CD, J	733DC	
LM733CH	733HC	
LM741D, J	741DM	
LM741F	741FM	
LM741H	741HM	
LM741CD, J	741DC	
LM741CF	741FC	
LM741CH	741HC	
LM747D, J	747DM	
LM747H	747HM	
LM747F	747FM	
LM747CD, J	747DC	
LM747CP	747PC	
LM747CH	747HC	
LM747CN	747PC	
LM478H	748HM	
LM748CH	748HC	
LM748CN	748PC	
LM1458H	AM1458H	
LM1558H	AM1558H	

SIGNETICS

NE — Temperature Range

555 — Device Type

V — Package Type

Signetics	AMD Direct Replacement	AMD Functional Replacement
DM7820F	DM7820J	
DM7830F	DM7830J	
DM8820A	DM8820N	
DM8820F	DM8820J	
DM8830A	DM8830N	
DM8830F	DM8830J	
LM101F	LM101D	

INDUSTRY CROSS REFERENCE

SIGNETICS (Cont.)

Signetics	AMD Direct Replacement	AMD Functional Replacement
LM101T	LM101H	
LM101AF	LM101AD	
LM101AT	LM101AH	
LM107F	LM107D	
LM107T	LM107H	
LM108F	LM108D	
LM108T	LM108H	
LM108AF	LM108AD	
LM108AT	LM108AH	
LM111F	LM111D	
LM111T	LM111H	
LM119H	LM119H	
LM119D	LM119D	
LM124F	LM124D	
LM139F	LM139D	
LM201T	LM301H	
LM201AF	LM201AD	
LM201AT	LM201AH	
LM201AV	LM201AN	
LM207F	LM207D	
LM207T	LM207H	
LM208F	LM208D	
LM208T	LM208H	
LM208AF	LM208AD	
LM208AT	LM208AH	
LM211F	LM211D	
LM211T	LM211H	
LM219H	LM219H	
LM219D	LM219D	
LM224F	LM224D	
LM239F	LM239D	
LM301AT	LM310AH	
LM301AV	LM301AN	
LM307F	LM307D	
LM307T	LM307H	
LM308F	LM308D	
LM308T	LM308H	
LM308V	LM308N	
LM380AF	LM308AD	
LM308AT	LM308AH	
LM311F	LM311D	
LM311T	LM311H	
LM311V	LM311N	
LM319H	LM319H	
LM319D	LM319D	
LM319A	LM319N	
LM324A	LM324N	
LM324F	LM324D	
LM339A	LM339N	
LM339F	LM339D	
MC1488F	MC1488L	
MC1489F	MC1489L	
MC1489AF	MC1489AL	
NE529K		AM686HC
NE555T	NE555T	
NE555V	NE555V	
NE556A	NE556A	
NE556F	NE556F	
NE592K	AM592HC	
N74123B	SN74123N	
N74123F	SN74123J	
N74221B	SN74221N	
N74221F	SN74221J	
N8T22A	9601PC	

SIGNETICS (Cont.)

Signetics	AMD Direct Replacement	AMD Functional Replacement
N8T22F	9601DC	
N8T26B	N8T26B	
N8T26F	N8T26F	
N8T26AB	N8T26AB	
N8T26AF	N8T26AF	
N8T28B	N8T28B	
N8T28F	N8T28F	
N8T38B		DS8838N
N8T38F		DS8838J
N9602B	9602PC	
N9602F	9602DC	
SE529K		AM686HM
SE555T	SE555T	
SE556F	SE556F	
SE592A	AM592PC	
SE592K	AM592HM	
SN7520N	SN7520N	
SN7521N	SN7521N	
SN7524N	SN7524N	
SN7525N	SN7525N	
S54123F	SN54123J	
S54221F	SN54221J	
S9602F	9602DM	
S8T26F	S8T26F	
S8T26AF	S8T26AF	
S8T28F	S8T28F	
S8T38F		DS7838J
μA723CF	723DC	
μA723CL	723HC	
μA723F	723DM	
μA723L	723HM	
μA733CA	733PC	
μA733CF	733DC	
μA733CK	733HC	
μA733F	733DM	
μA733K	733HM	
μA741CF	741DC	
μA741CT	741HC	
μA741F	741DM	
μA741T	741HM	
μA747CA	747PC	
μA747CF	747DC	
μA747CK	747HC	
μA747F	747DM	
μA747K	747HM	
μ748CT	748HC	
μA748F	748DM	
μA748T	748HM	

TEXAS INSTRUMENTS

SN 75 110 N

Mfg's Ident. | Temperature Range | Device Type | Package Type

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN52101AJ	LM101AD	
SN52101AL	LM101AH	
SN52101AZ	LM101AF	
SN52105L	LM105H	
SN52106FA	LM106F	

INDUSTRY CROSS REFERENCE

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN52106L	LM106H	
SN52107J	LM107D	
LM52107L	LM107H	
SN52107Z	LM107F	
SN52108AFA	LM108AF	
SN52108AJA	LM108AD	
SN52108AL	LM108AH	
SN52108FA	LM108F	
SN52108JA	LM108D	
SN52108L	LM108H	
SN52111FA	LM111F	
SN52111J	LM111D	
SN52111L	LM111H	
SN52118FA	LM118F	
SN52118JA	LM118D	
SN52118L	LM118H	
SN52555L	SE555T	
SN52723J	723DM	
SN52723L	723HM	
SN52733FA	733FM	
SN52733J	733DM	
SN52733L	733HM	
SN52741FA	741FM	
SN52741JA	741DM	
SN52741L	741HM	
SN52747FA	747FM	
SN52747JA	747DM	
SN52747L	747HM	
SN52748FA	748FM	
SN52748JA	748DM	
SN52748L	748HM	
SN54LS123J	†SN54LS123J	†AM25LS123DM
SN54LS123W	†SN54LS123W	†AM25LS123FM
SN54L123J		AM26L123DM
SN54L123W		AM26L123FM
SN54LS240J	†SN54LS240J	
SN54LS241J	†SN54LS241J	
SN54S240J	†SN54S240J	
SN54S241J	†SN54S241J	
SN54123J	SN54123J	AM26123DM
SN54123W	SN54123W	AM26123DM
SN54221J	SN54221J	
SN54221W	SN54221W	
SN55107AJ	SN55107BJ	
SN55107BJ	SN55107BJ	
SN55108AJ	SN55108BJ	
SN55108BJ	SN55108BJ	
SN55109J	SN55109J	
SN55110J	SN55110J	
SN55114J	9614DM	
SN55114W	9614FM	
SN55115J	9615DM	
SN55115W	9615FM	
SN55182J	DM7820AJ	
SN55182W	DM7820AW	
SN55183J	DM7830J	
SN55183W	DM7830W	
SN5520J	SN5520J	
SN5521J	SN5521J	
SN55234J	SN55234J	
SN55234W	SN55234W	
SN55235J	SN55235J	
SN55235W	SN55235W	
SN55238J	SN55238J	

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN55238W	SN55238W	
SN55239J	SN55239J	
SN55239W	SN55239W	
SN5524J	SN5524J	
SN5525J	SN5525J	
SN55325J	SN55325J	
SN55325W	SN55325W	
SN55369J	MMH0026L	
SN72301AJ	LM301AD	
SN72301AL	LM301AH	
SN72305L	LM305H	
SN72306L	LM306H	
SN72307J	LM307D	
SN72307L	LM307H	
SN73208AJA	LM308AD	
SN72308AL	LM308AH	
SN72308JA	LM308D	
SN72308L	LM308H	
SN72311J	LM311D	
SN72311L	LM311H	
SN72318JA	LM318D	
SN72318L	LM318H	
SN72555L	NE555T	
SN72555P	NE555V	
SN72723J	723DC	
SN72723L	723HC	
SN72733J	733DC	
SN72733L	733HC	
SN72741JA	741DC	
SN72741L	741HC	
SN72747JA	747DC	
SN72747L	747HC	
SN72748JA	748DC	
SN72748L	748HC	
SN74LS123J	†SN74LS123J	†AM25LS123DC
SN74LS123N	†SN74LS123N	†AM25LS123PC
SN74L123J		AM26L123DC
SN74L123N		AM26L123PC
SN74LS240J	SN74LS240J	
SN74LS240N	†SN74LS240N	
SN74LS241J	SN74LS241J	
SN74LS241N	†SN74LS241N	
SN74LS424J	D8224	
SN74LS424N	P8224	
SN74S240J	SN74S240J	
SN74S240N	†SN74S240N	
SN74S241J	SN74S241J	
SN74S241N	†SN74S241N	
SN74S412J	D8212	
SN74S412	P8212	
SN74123J	SN74123J	AM26123DC
SN74123N	SN74123N	AM26123PC
SN74221J	SN74221J	
SN74221N	SN74221N	
SN75107AJ	SN74107BJ	
SN75107AN	SN75107BN	
SN75107BJ	SN75107BJ	
SN74107BN	SN75107BN	
SN75108AJ	SN75108BJ	
SN75108AN	SN75108BN	
SN75108BJ	SN75108BJ	
SN75108BN	SN75108BN	
SN75109J	SN75109J	
SN75109N	SN75109N	

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN75110J	SN75110J	
SN75110N	SN75110N	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115N	9615PC	
SN75182J	DM8820AJ	
SN75182N	DM8820AN	
SN75183J	DM8830J	
SN75183N	DM8830N	
SN75188J	MC1488L	
SN75188N	AM1488PC	
SN75189J	MC1489L	
SN75189N	AM1489PC	
SN75189AJ	MC1489AL	
SN75189AN	AM1489APC	
SN7520J	SN7520J	
SN7520N	SN7520N	
SN7521J	SN7521J	
SN7521N	SN7521N	
SN75207J	SN75207J	
SN75207N	SN75207N	
SN75208J	SN75208J	
SN75208N	SN75208N	
SN75234J	SN75234J	
SN75234N	SN75234N	
SN75235J	SN75235J	
SN75235N	SN75235N	
SN75238J	SN75238J	
SN75238N	SN75238N	
SN75239J	SN75239J	
SN75239N	SN75239N	
SN7524J	SN7524J	
SN7524N	SN7524N	
SN7525J	SN7525J	
SN7525N	SN7525N	
SN75325J	SN75325J	
SN75325N	SN75325N	
SN75369J	MMH0026CL	
SN75369P	MH0026CN	

†To be announced.

DICE POLICY

Advanced Micro Devices, interface and linear products are all available in dice form.

ELECTRICAL CHARACTERISTICS

Each die is electrically tested to the commercial or military grade DC parameters to guardbanded limits at 25°C to guarantee operation over the temperature range.

QUALITY ASSURANCE

All dice are 100% visually inspected to the requirements of MIL-STD-883A, Method 2010.2, condition B.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection. All dice are provided without gold backing.

SHIPPING PACKAGES/ORDER INFORMATION

All dice are packaged in containers with individual compartments which prevent damage to the die during shipping.

Minimum order for AMD dice is 10 pcs.

SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, contact AMD for detailed information.

See following pages on ordering information for detail ordering number.

ORDERING INFORMATION

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pak	Dice
Am592	AM592HC	AM592DC	AM592PC	AM592XC	AM592HM	AM592DM		AM592XM
AM685	AM685HL*	AM685DL*		AM685XL*	AM685HM	AM685DM		AM685XM
Am686	AM686HC	AM686DC		AM686XC	AM686HM	AM686DM		AM686XM
Am687		AM687DL*		AM687XL*		AM687DM		AM687XM
Am1500		AM1500DC				AM1500DM	AM1500FM	
						AM1500DL*	AM1500FL*	
Am1501		AM1501DC				AM1501DM	AM1501FM	
						AM1501DL*	AM1501FL*	
Am1508		AM1408L8				AM1508L8		
		AM1408L7						
		AM1408L6						
Am1558	AM1458H				AM1558H			
Am25 Series								
Am25LS123		AM25LS123DC	AM25LS123PC	AM25LS123XC		AM25LS123DM	AM25LS123FM	AM25LS123XM
Am26 Series								
Am2600		AM2600DC	AM2600PC	AM2600XC		AM2600DM	AM2600FM	AM2600XM
Am2602		AM2602DC	AM2602PC	AM2602XC		AM2602DM	AM2602FM	AM2602XM
Am2614		AM2614DC	AM2614PC	AM2614XC		AM2614DM	AM2614FM	AM2614XM
Am2615		AM2615DC	AM2615PC	AM2615XC		AM2615DM	AM2615FM	AM2615XM
Am2616		AM2616DC	AM2616PC	AM2616XC		AM2616DM	AM2616FM	AM2616XM
Am2617		AM2617DC	AM2617PC	AM2617XC		AM2617DM	AM2617FM	AM2617XM
Am26123		AM26123DC	AM26123PC	AM26123XC		AM26123DM	AM26123FM	AM26123XM
Am26LS31		AM26LS31DC	AM26LS31PC	AM26LS31XC		AM26LS31DM	AM26LS31FM	AM26LS31XM
Am26LS32		AM26LS32DC	AM26LS32PC	AM26LS32XC		AM26LS32DM	AM26LS32FM	AM26LS32XM
Am26L02		AM26L02DC	AM26L02PC	AM26L02XC		AM26L02DM	AM26L02FM	AM26L02XM
Am26L123		AM26L123DC	AM26L123PC	AM26L123XC		AM26L123DM	AM26L123FM	AM26L123XM
Am26S02		AM26S02DC	AM26S02PC	AM26S02XC		AM26S02DM	AM26S02FM	AM26S02XM
Am26S10		AM26S10DC	AM26S10PC	AM26S10XC		AM26S10DM	AM26S10FM	AM26S10XM
Am26S11		AM26S11DC	AM26S11PC	AM26S11XC		AM26S11DM	AM26S11FM	AM26S11XM
Am26S12		AM26S12DC	AM26S12PC	AM26S12XC		AM26S12DM	AM26S12FM	AM26S12XM
Am26S12A		AM26S12ADC	AM26S12APC	AM26S12AXC		AM26S12ADM	AM26S12AFM	AM26S12AXM
Am29 Series								
Am2905		AM2905DC	AM2905PC	AM2905XC		AM2905DM	AM2905FM	AM2905XM
Am2906		AM2906DC	AM2906PC	AM2906XC		AM2906DM	AM2906FM	AM2906XM
Am2907		AM2907DC	AM2907PC	AM2907XC		AM2907DM	AM2907FM	AM2907XM
Am2915A		AM2915ADC	AM2915APC	AM2915AXC		AM2915ADM	AM2915AFM	AM2915AXM
Am2916A		AM2916ADC	AM2916APC	AM2916AXC		AM2916ADM	AM2916AFM	AM2916AXM
Am2917A		AM2917ADC	AM2917APC	AM2917AXC		AM2917ADM	AM2917AFM	AM2917AXM
Am32XX Series								
Am3212		D3212	P3212	AM8212XC		MD3212		
Am3216		D3216	P3216	AM8212XC		MD3216		
Am3226		D3226	P3226	AM8226XC		MD3226		
DAC-08		DAC-08EQ				DAC-08AQ		
		DAC-08CQ				DAC-08Q		
DM or DS78/88 Series								
DM78/8820		DM8820J	DM8820N	AM8820X		DM7820J	DM7820W	AM7820X
DM78/8820A		DM8820AJ	DM8820AN	AM8820AX		DM7820AJ	DM7820AW	AM7820AX
DM78/8830		DM8830J	DM8830N	AM8830X		DM7830J	DM7830W	AM7830X
DM78/8831		DM8831J	DM8831N	AM8831X		DM7831J	DM7831W	AM7831X
DM78/8832		DM8832J	DM8832N	AM8832X		DM7832J	DM7832W	AM7832X
DS78/8838		DS8838J	DS8838N			DS7838J	DS7838W	
DS0056 (8 pin)	DS0056CH		DS0056CN	AM0056CX	DS0056H			AM0056X
DS0056 (12 pin)	DS0056CG				DS0056G			
DS0056 (14 pin)	DS0056CJ				DS0056J			
DS16/3603	DS3603J		DS3603N	AM3603X	DS1603J			AM1603X
DS3604	DS3604		DS3604N	AM3604X				
LF155	LF355H		LF355N	LD355	LF155H			LD155
•					LF255			
LF155A	LF355AH			LD355A	LF155AH			LD155A
•								
LF156	LF356H		LF356N	LD356	LF156H			LD156
•					LF256			
LF156A	LF356AH			LD356A	LF156AH			LD156A
•								
LF157	LF357H		LF357N	LD357	LF157H			LD157
•					LF257H			
LF157A	LF357AH			LD357A	LF157AH			LD157A
LH2101A		LH2301AD				LH2101AD	LH2101AF	
•						LH2201AD	LH2201AF	
LH2111		LH2311D				LH2111D	LH2111F	
•						LH2211D	LH2211F	
LM101	LM301H	LM301D	LM301N	LD301	LM101H	LM101D	LM101F	LD101
•			LM201N		LM201H	LM201D	LM201F	
LM101A	LM301AH	LM301AD	LM301AN	LD301A	LM101AH	LM101AD	LM101AF	LD101A
•			LM201AN		LM201AH	LM201AD	LM201AF	
LM102	LM302H	LM302D		LD302	LM102H	LM102D	LM102F	LD102
•					LM202H	LM202D	LM202F	
LM105	LM305H			LD305	LM105H			LD105
•	LM305AH				LM205H			
LM106	LM306H	LM306D		LD306	LM106H		LM106F	LD106
•					LM206H		LM206F	
LM107	LM307H	LM307D		LD307	LM107H	LM107D	LM107F	LD107
•					LM207H	LM207D	LM207F	
LM108	LM308H	LM308D	LM308N	LD308	LM108H	LM108D	LM108F	LD108
•					LM208H	LM208D	LM208F	
LM108A	LM308AH	LM308AD	LM308AN	LD308A	LM108AH	LM108AD	LM108AF	LD108A
•					LM208AH	LM208AD	LM208AF	
LM110	LM310H	LM310D	LM310N	LD310	LM110H	LM110D	LM110F	LD110
•					LM210H	LM210D	LM210F	
LM111	LM311H	LM311D	LM311N	LD311	LM111H	LM111D	LM111F	LD111
•					LM211H	LM211D	LM211F	
LF111	LF311H	LF311D		LFD311	LF111H	LF111D	LF111F	LFD111
•					LF211H	LF211D	LF211F	
LM112	LM312H	LM312D		LD312	LM112H	LM112D	LM112F	LD112
•					LM212H	LM212D	LM212F	

ORDERING INFORMATION (Cont.)

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pak	Dice
LM118	LM318H	LM318D	LM318N	LD318	LM118H	LM118D	LM118F	LD118
•					LM218H	LM218D	LM218F	
LM119	LM319H	LM319D	LM319N	LD319	LM119H	LM119D	LM119F	LD119
•					LM219H	LM219D	LM219F	
LM124		LM324D	LM324N	LD324		LM124D	LM124F	LD124
•						LM224D	LM224F	
LM124A		LM324AD	LM324AN	LD324A		LM124AD	LM124AF	LD124A
•						LM224AD	LM224AF	
LM139		LM339D	LM339	LD339		LM139D	LM139F	LD139
•						LM239D	LM239F	
LM139A		LM339AD	LM339AN	LD339A		LM139AD	LM139AF	LD139A
•						LM239AD	LM239AF	
LM148		LM348D	LM348N	LD348		LM148D		LD148
•						LM248D		
LM149		LM349D	LM349N	LD349		LM149D		LD149
•						LM249D		
LM216	LM316H	LM316D		LD316				
•					LM216H	LM216D	LM216F	LD216
LM216A	LM316AH	LM316AD		LD316A				
•					LM216AH	LM216AD	LM216AF	LD216A
MC1488		MC1488L	AM1488PC	AM1488XC				
MC1489		MC1489L	AM1489PC	AM1489XC				
MC1489A		MC1489AL	AM1489APC	AM1489AXC				
MH0026 (8 pin)	MH0026CH		MH0026CN	AM0026CX	MH0026H			AM0026X
MH0026 (12 pin)	MH0026CG				MH0026G			
MH0026 (14 pin)		MMH0026CL				MMH0026L		
N/SE555			NE555V	AM555XC	SE555T			AM555XM
N/SE556	NE555T		NE556A	AM556XC		SE556F		AM556XM
SN54/74 Series								
SN54/74123		SN74123J	SN74123N	AM74123X		SN54123J	SN54123W	AM54123X
SN54/74221		SN74221J	SN74221N	AM74221X		SN54221J	SN54221W	AM54221X
SN54/74LS123		SN74LS123J	SN74LS123N	AM74LS123X		SN54LS123J	SN54LS123W	AM54LS123X
SN54/74S240		SN74S240J	SN74S240N	AM74S240X		SN54S240J		AM54S240X
SN54/74S241		SN74S241J	SN74S241N	AM74S241X		SN54S241J		AM54S241X
SN54/74S242		SN74S242J	SN74S242N	AM74S242X		SN54S242J		AM54S242X
SN54/74S243		SN74S243J	SN74S243N	AM74S243X		SN54S243J		AM54S243X
SN54/74S244		SN74S244J	SN74S244N	AM74S244X		SN54S244J		AM54S244X
SN55/75 Series								
SN55/75107B		SN75107BJ	SN75107BN	AM75107BX		SN55107BJ		AM55107BX
SN55/75108B		SN75108BJ	SN75108BN	AM75108BX		SN55108BJ		AM55108BX
SN55/75109		SN75109J	SN75109N	AM75109X		SN55109J		AM55109X
SN55/75110		SN75110J	SN75110N	AM75110X		SN55110J		AM55110X
SN55/7520		SN7520J	SN7520N	AM7520X		SN5520J	SN5520W	AM5520X
SN75207		SN75207J	SN75207N	AM75207X				
SN75208		SN75208J	SN75208N	AM75208X				
SN55/7521		SN7521J	SN7521N	AM7521X		SN5521J	SN5521W	AM5521X
SN55/75234		SN75234J	SN75234N	AM75234X		SN55234J	SN55234W	AM55234X
SN55/75235		SN75235J	SN75235N	AM75235X		SN55235J	SN55235W	AM55235X
SN55/75238		SN75238J	SN75238N	AM75238X		SN55238J	SN55238W	AM55238X
SN55/75239		SN75239J	SN75239N	AM75239X		SN55239J	SN55239W	AM55239X
SN55/7524		SN7524J	SN7524N	AM7524X		SN5524J	SN5524W	AM5524X
SN55/7525		SN7525J	SN7525N	AM7525X		SN5525J	SN5525W	AM5525X
SN55/75325		SN75325J	SN75325N	AM75325X		SN55325J	SN55325W	AM55325X
715	715HC	715DC		715XC				
723	723HC	723DC	723PC	723XC	723HM	723DM		723XM
725	725HC	725DC	725CN	725XC	725HM	725DM		725XM
SSS725	SSS725CJ	SSS725CP			SSS725J	SSS725P		
733	733HC	733DC		733XC	733HM	733DM	733FM	733XM
741	741HC	741DC		741XC	741HM	741DM	741FM	741XM
741A	741EHC	741EDC			741AHM	741ADM	741AFM	
SSS741	SSS741CJ				SSS741J			
747	747HC	747DC	747PC	747XC	747HM	747DM	747FM	747XM
747A	747EHC	747EDC			747AHM	747ADM	747AFM	
SSS747	SSS747CK	SSS747CP			SSS747K	SSS747P	SSS747M	
748	748HC	748DC	748PC	748XC	748HM	748DM	748FM	748XM
8XXX Series								
8T26		N8T26F	N8T26B	AM8T26X		S8T26F		AM8T26X
8T26A		N8T26AF	N8T26AB	AM8T26AX		S8T26AF		AM8T26AX
8T28		N8T28F	N8T28B	AM8T28X		S8T28F		AM8T28X
8212		C8212	P8212	AM8212XC		AM8212DM		
8216		C8216	P8216	AM8216XC		AM8216DM		
8224		D8224	AM8224PC	AM8224XC		AM8224DM		
8226		C8226	AM8226PC	AM8226XC		AM8226DM		
8228		C8228	AM8228PC	AM8228XC		AM8228DM		
8238		D8238	AM8238PC	AM8238XC		AM8238DM		
96 Series								
9600		9600DC	9600PC	AM9600XC		9600DM	9600FM	AM9600XM
9601		9601DC	9601PC	AM9601XC		9601DM	9601FM	AM9601XM
9602		9602DC	9602PC	AM9602XC		9602DM	9602FM	AM9602XM
9614		9614DC	9614PC	AM9614XC		9614DM	9614FM	AM9614XM
9615		9615DC	9615PC	AM9615XC		9615DM	9615FM	AM9615XM
9616		9616DC	9616PC	AM9616XC		9616DM		
9617		9617DC	9617PC	AM9617XC		9617DM		AM9617XM
9620		9620DC	9620PC	AM9620XC		9620DM	9620FM	AM9620XM
9621		9621DC	9621PC	AM9621XC		9621DM	9621FM	AM9621XM
96L02		96L02DC	96L02PC	AM96L02XC		96L02DM	96L02FM	AM96L02XM

*Indicates −25°C to +85°C Operating Temperature Range.

For MIL-STD-883A Class B processing order as follows: For all LM100 and LM2100 series devices add/883B suffix.

Example: LM101AH/883B, LH2111D/883B

For other devices add B suffix.

Example: 741HMB, AM687DMB, AM1500DMB

PRODUCT ASSURANCE
MIL-M-38510 • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Three military documents provide the foundation for this program. They are:

MIL-M-38510—General Specification for Microcircuits
MIL-Q-9858—Quality Program Requirements
MIL-STD-883—Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. **All linear, MSI, and interface circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.**

MIL-Q-9858 identifies 28 elements of management, planning and control that are necessary in maintaining a quality program. **Advanced Micro Devices complies with all requirements of MIL-Q-9858.**

MIL-STD-883 contains detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C — Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B — Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C. All other process requirements are the same.

Class A — Used where replacement is extremely difficult and reliability is imperative. Class A screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number.*

All molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted for solid-package parts.

Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels for each class are given for Group A (electrical), Group B (mechanical quality measurements related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user. Tables I, II, III and IV give standard test groupings and quality levels for Class B screened devices. These quality levels are used as a minimum for all tests.

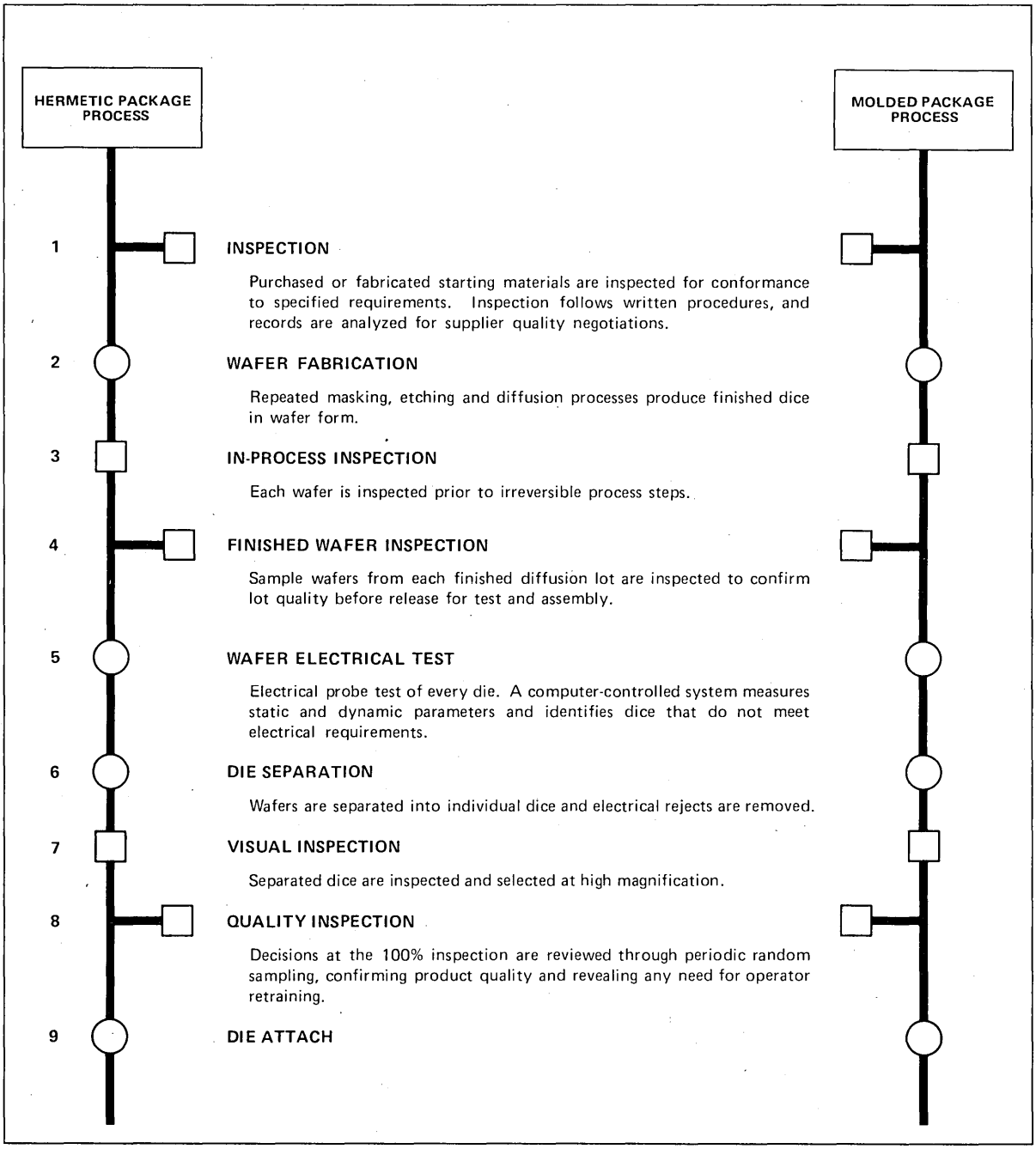
*Exception is linear 100, 200 and 300 series parts which are marked "/883B".

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B levels.

All full-temperature-range (−55°C to +125°C) linear, MSI and interface circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.



10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices—MIL-STD-883, Method 2010, Condition B.
Full temperature devices identified above—MIL-M-38510, Para. 3.7 for workmanship.

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

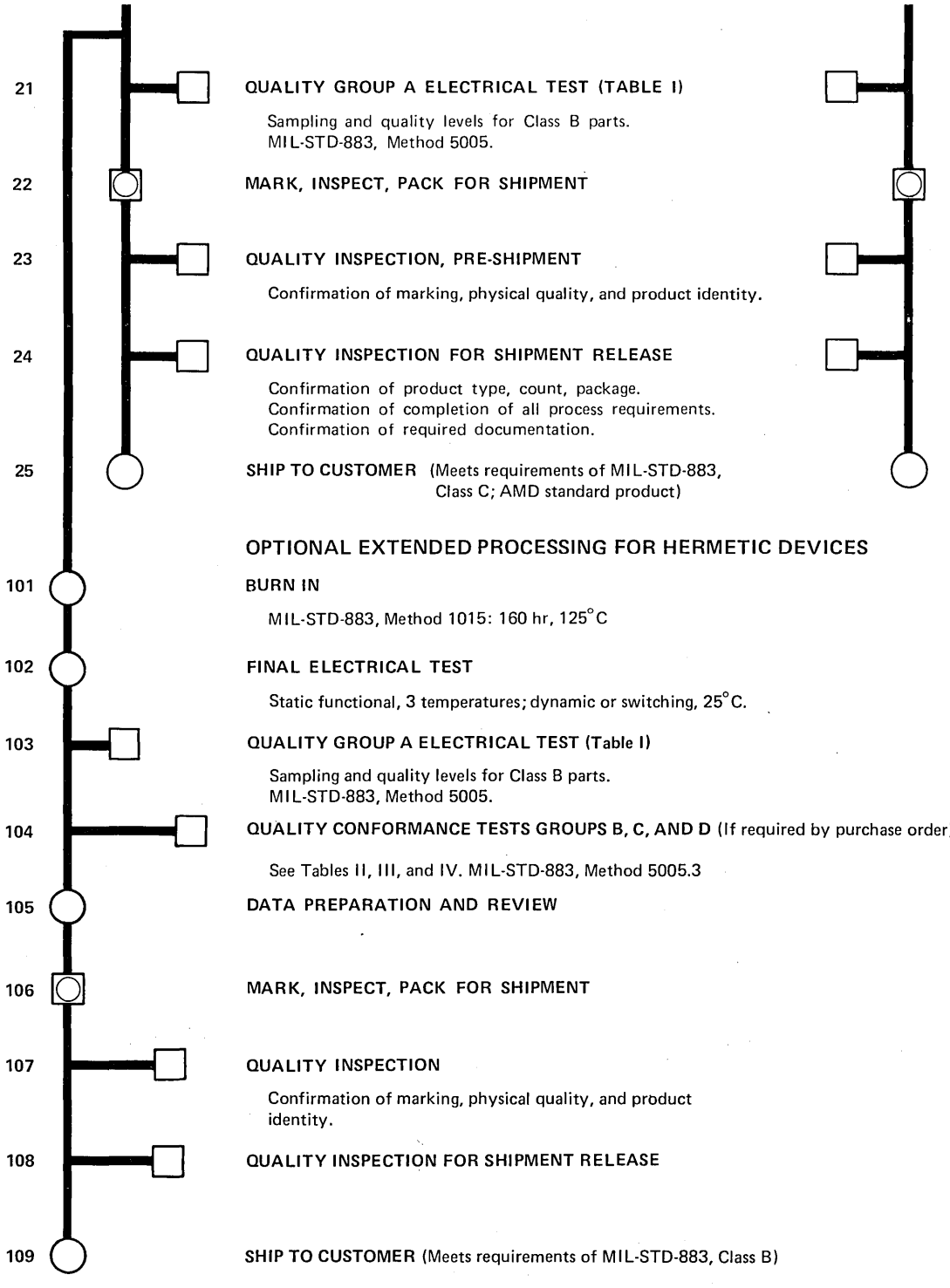
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

Sampling and quality levels for Class B parts.
MIL-STD-883, Method 5005.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER** (Meets requirements of MIL-STD-883, Class C; AMD standard product)

OPTIONAL EXTENDED PROCESSING FOR HERMETIC DEVICES

101 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C

102 **FINAL ELECTRICAL TEST**

Static functional, 3 temperatures; dynamic or switching, 25°C.

103 **QUALITY GROUP A ELECTRICAL TEST (Table I)**

Sampling and quality levels for Class B parts.
MIL-STD-883, Method 5005.

104 **QUALITY CONFORMANCE TESTS GROUPS B, C, AND D** (If required by purchase order)

See Tables II, III, and IV. MIL-STD-883, Method 5005.3

105 **DATA PREPARATION AND REVIEW**

106 **MARK, INSPECT, PACK FOR SHIPMENT**

107 **QUALITY INSPECTION**

Confirmation of marking, physical quality, and product identity.

108 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

109 **SHIP TO CUSTOMER** (Meets requirements of MIL-STD-883, Class B)

Standard AMD parts with this processing are marked with "—B" after part number*.

*Exception is linear 100, 200 and 300 series parts which are marked "/883B"

QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Subgroups and LTPD levels as given in MIL-STD-883A, Method 5005.3, for Class B parts.

Table I. Group A Electrical Tests

Subgroups	LTPD	Initial (Note 1) Sample Size
Subgroup 1 — Static tests at 25°C	5	45
Subgroup 2 — Static tests at maximum rated operating temperature	7	32
Subgroup 3 — Static tests at minimum rated operating temperature	7	32
Subgroup 4 — Dynamic tests at 25°C	5	45
Subgroup 5 — Dynamic tests at maximum rated operating temperature	7	32
Subgroup 6 — Dynamic tests at minimum rated operating temperature	7	32
Subgroup 7 — Functional tests at 25°C	5	45
Subgroup 8 — Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 — Switching tests at 25°C	7	32
Subgroup 10 — Switching tests at minimum rated operating temperature (Note 2)	10	10
Subgroup 11 — Switching tests at minimum rated operating temperature (Note 2)	10	10

Notes: 1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. For qualification only if required on purchase order.

Table II. Group B Tests

Test	Method	Conditions	LTPD	Initial Sample Size
Subgroup 1 Physical dimensions	2016	AMD standard dimensions unless listed by customer	2 devices (no failures)	2
Subgroup 2 a) Resistance to Solvents	2015	Alcohol, mineral spirits, trichloroethane, and Freon solvents	3 devices (no failures)	3
b) Internal visual and mechanical	2014		1 device (no failures)	1
c) Bond strength	2011	Test Condition D	15	15 leads
Subgroup 3 Solderability	2003	Solder temperature 260°C ± 10°C	15	15

Table III. Group C (Die-Related Tests)

Test	Method	Condition	LPTD	Initial Sample Size
Subgroup 1				
a) Operating life test	1005	AMD standard burn-in circuit (1000 hr.)	5	77
b) End point electrical parameters		DC room temperature parameters		ACC = 1
Subgroup 2				
a) Temperature cycling	1010	Test condition C: air to air, –65°C to +150°C, 10 cycles	15	15
b) Constant acceleration	2001	Test condition E: 30kG centrifugal acceleration Y axis followed by one other axis X or Z.		
c) Seal	1014			
1. Fine		Condition A: helium, or condition B: radioactive tracer		
2. Gross		Condition C, step 2: fluorocarbon		
d) Visual examination	Note 3			
e) End point electrical parameters		DC room temperature parameters.		

Note: 3. Visual examination shall be in accordance with method 1010 of MIL-STD-883.

Table IV. Group D (Package Related Tests)

Test	Method	Condition	LPTD	Initial Sample Size
Subgroup 1				
a) Physical dimensions	2016		15	15
Subgroup 2				
a) Lead integrity	2004	Test condition B2 (lead fatigue)	15	15
b) Seal	1014			
1. Fine		Condition A: helium, or condition B: radioactive tracer		
2. Gross		Condition C, step 2: fluorocarbon		
Subgroup 3				
a) Thermal shock	1011	Test condition B: liquid to liquid, –55°C to +125°C	15	15
b) Temperature cycling	1010	Test condition C: air to air, –65°C to +150°C, 100 cycles		
c) Moisture resistance	1004	Omit initial conditioning and vibration		
d) Seal	1014			
1. Fine		Condition A: helium, or condition B: radioactive tracer		
2. Gross		Condition C, step 2: fluorocarbon		
e) Visual examination	Note 4			
f) End point electrical parameters		DC room temperature parameters		
Subgroup 4				
a) Mechanical shock	2002	Test condition B: 5 shock pulses; 6 directions; 1,500 G	15	15
b) Vibration variable frequency	2007	Test condition A: 20 Hz – 2kHz; 20G, X, Y, Z orientation		
c) Constant acceleration	2001	Test condition E: 30kG centrifugal acceleration		
d) Seal	1014			
1. Fine		Condition A: helium, or condition B: radioactive tracer		
2. Gross		Condition C, step 2: fluorocarbon		
e) Visual examination	Note 5			
f) End point electrical parameters		DC room temperature parameters		
Subgroup 5				
a) Salt atmosphere	1009	Test condition A: 24 hr.	15	15
b) Visual examination	Note 6			

Notes: 4. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
5. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
6. Visual examination shall be in accordance with MIL-STD-883, Method 1009 para. 3.3.1.

Comparators — Section II

Application Notes

Am106/206/306

Voltage Comparator/Buffer

Distinctive Characteristics

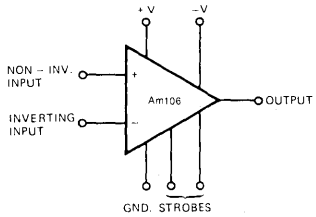
- Functionally, electrically, and pin-for-pin equivalent to the National LM 106/206/306
- Drives RTL, DTL or TTL directly
- Output can switch voltages up to 24 V @ 100 mA
- Fan-out of 10 with DTL or TTL
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Available in metal can and hermetic flat package.

2

FUNCTIONAL DESCRIPTION

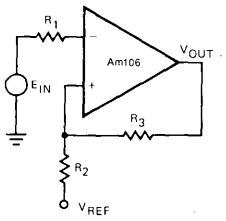
The Am106/206/306 are high-speed voltage comparators/buffers designed to be used in applications where high accuracy and fast response times are required. The device is useful as a pulse-height discriminator, relay or lamp driver or a line receiver.

FUNCTIONAL DIAGRAM



APPLICATION

Level Detector With Hysteresis



Upper and Lower Trip Points:

$$V_{UT} = V_{REF} + \frac{R_2 [V_{0\ MAX} - V_{REF}]}{R_2 + R_3}$$

and

$$V_{LT} = V_{REF} + \frac{R_2 [V_{0\ MIN} - V_{REF}]}{R_2 + R_3}$$

$$\text{Hysteresis} = V_H = V_{UT} - V_{LT}$$

$$= \frac{R_2 [V_{0\ MAX} - V_{0\ MIN}]}{R_2 + R_3}$$

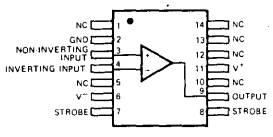
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am306	Metal Can	0°C to +70°C	LM306H
	Dice	0°C to +70°C	LD306
Am206	Metal Can	−25°C to +85°C	LM206H
Am106	Metal Can	−55°C to +125°C	LM106H
	Flat Pak	−55°C to +125°C	LM106F
	Dice	−55°C to +125°C	LD106

CONNECTION DIAGRAMS

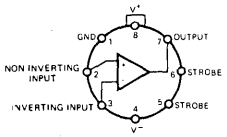
Top Views

Flat Package



Note: Pin 6 connected to bottom of package.

Metal Can



Note: Pin 4 connected to case.

MAXIMUM RATINGS

Positive Supply Voltage	15 V
Negative Supply Voltage	−15 V
Output Voltage	24 V
Output to Negative Supply Voltage	30 V
Differential Input Voltage	±5 V
Input Voltage	±7 V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am106	−55°C to +125°C
Am206	−25°C to +85°C
Am306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am306 Min	Am306 Typ	Am306 Max	Am106 Am206 Min	Am106 Am206 Typ	Am106 Am206 Max	Units
Input Offset Voltage	Note 3		1.6	5.0		0.5	2.0	mV
Input Offset Current	Note 3		1.8	5.0		0.7	3.0	μA
Input Bias Current			16	25		10	20	μA
Voltage Gain			40			40		V/mV
Response Time	Note 4		30	40		30	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 100$ mA		0.8	2.0		1.0	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8 V \leq V_{OUT} \leq 24 V$		0.02	2.0		0.02	1.0	μA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	Note 3			6.5			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		5.0	20		3.0	10	μV/°C
Input Offset Current	$T_A = T_{A(max)}$		0.6	5.0		0.25	3.0	μA
	Note 3, $T_A = T_{A(min)}$		2.4	7.5		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A(max)}$		15	50		5.0	25	nA/°C
	$T_{A(min)} \leq T_A \leq 25°C$		24	100		15	75	nA/°C
Input Bias Current				40			45	μA
Input Voltage Range	$-7 V \geq V^- \geq -12 V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 50$ mA			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} \leq 16$ mA			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = 400$ μA	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8 V \leq V_{OUT} \leq 24 V$			100			100	μA
Strobe Current	$V_{strobe} = 0.4$ V		1.7	3.3		1.7	3.3	mA
Strobe ON Voltage		0.9	1.4		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1.4	2.5		1.4	2.5	V
Positive Supply Current	$V_{IN} = -5$ mV		5.5	10		5.5	10	mA
Negative Supply Current			1.5	3.6		1.5	3.6	mA

Note 1: Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 60°C; derate flat package at 5.4 mW/°C for operation at ambient temperatures above 40°C.

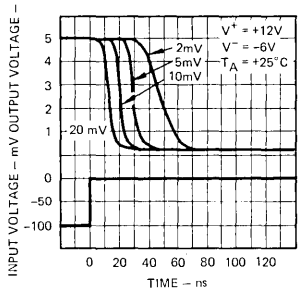
Note 2: These specifications apply for $-3 V \geq V^- \geq -12 V$, $V^+ = 12$ V and $T_A = 25°C$ unless otherwise specified.

Note 3: The offset voltages, offset currents, and bias currents given are the maximum values required to drive the output from the minimum output level up to the maximum output level. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

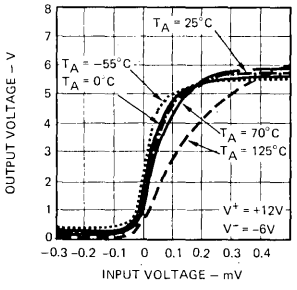
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

PERFORMANCE CURVES

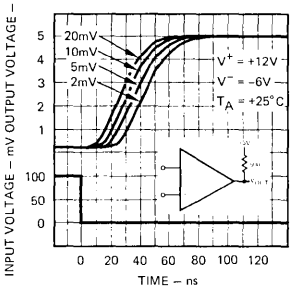
Response Time For Various Input Overdrives



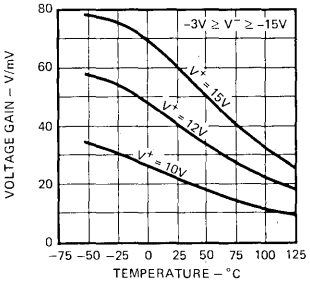
Transfer Function



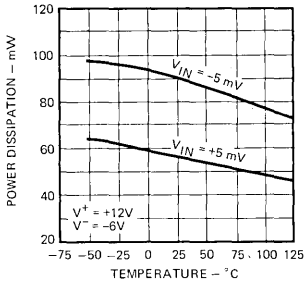
Response Time For Various Input Overdrives



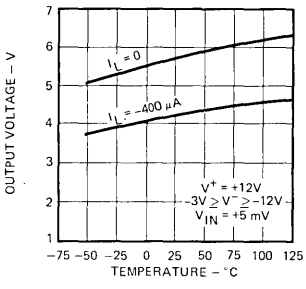
Voltage Gain



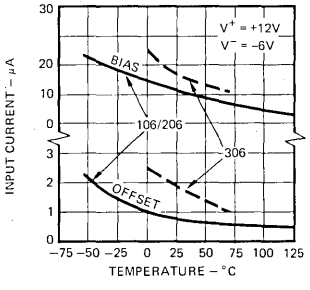
Power Consumption



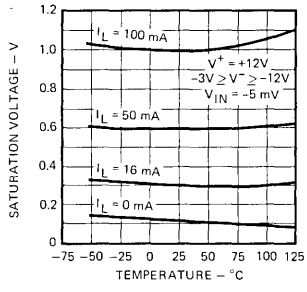
Positive Output Level



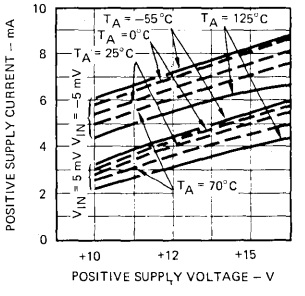
Input Current



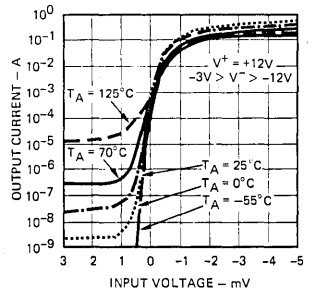
Saturation Voltage



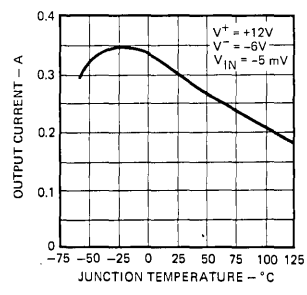
Positive Supply Current



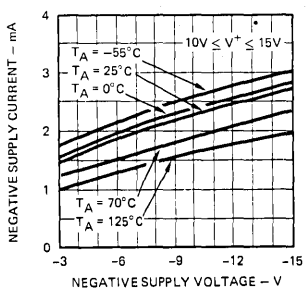
Transconductance



Short Circuit Output Current

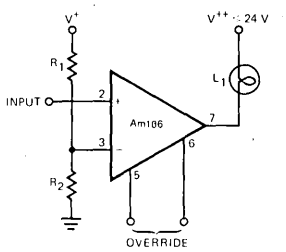


Negative Supply Current

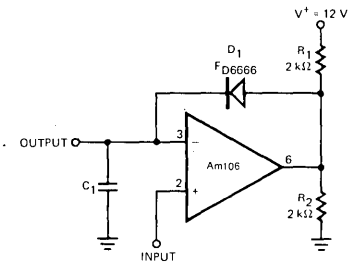


ADDITIONAL APPLICATIONS

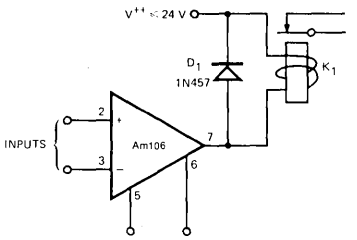
Level Detector and Lamp Driver



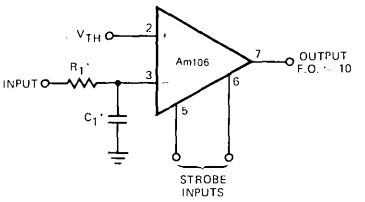
Fast Response Peak Detector



Relay Driver

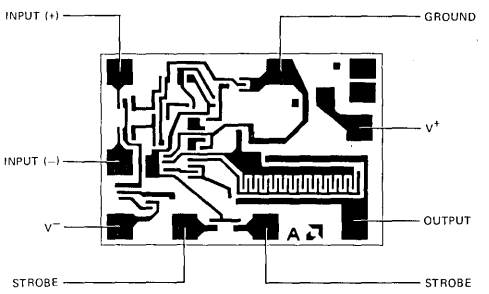


Adjustable Threshold Line Receiver



*Optional for response time control

Metallization and Pad Layout



33 x 46 Mils

Am111/211/311

Precision Voltage Comparator

Distinctive Characteristics

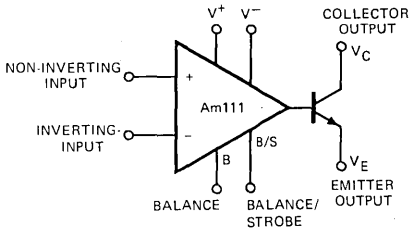
- The Am111/211/311 are functionally, electrically, and pin-for-pin equivalent to the National LM 111/211/311
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4mV max.
- Differential Input Voltage Range – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in Metal Can, Hermetic Dual-In-Line or hermetic Flat Packages

2

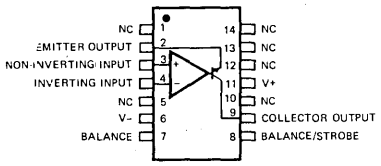
FUNCTIONAL DESCRIPTION

The Am111/211/311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads refered to ground or either supply. Strobing and offset balancing are available and the outputs can be wire ORed.

FUNCTIONAL DIAGRAM

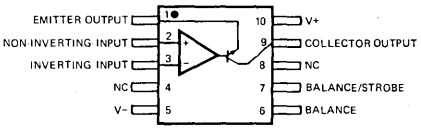


CONNECTION DIAGRAM
Top View
Dual-In-Line
Am111/211/311



Pin 6 is connected to bottom of package.

CONNECTION DIAGRAM
Top View
Flat Package
Am111/211/311

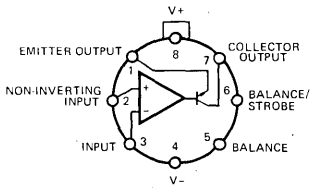


Pin 5 is connected to bottom of package.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am311	TO-99	0°C to 70°C	LM311H
	Hermetic DIP	0°C to 70°C	LM311D
	Dice	0°C to 70°C	LD311
Am211	TO-99	−25°C to +85°C	LM211H
	Hermetic DIP	−25°C to +85°C	LM211D
Am111	TO-99	−55°C to +125°C	LM111H
	Hermetic DIP	−55°C to +125°C	LM111D
	Flat Pak	−55°C to +125°C	LM111F
	Dice	−55°C to +125°C	LD111

CONNECTION DIAGRAM
Top View
Metal Can
Am111/211/311



Pin 4 is connected to case.

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
Am111/211	50V
Am311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, −0V
Voltage from Inputs to V^+	−30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am111	−55°C to +125°C
Am211	−25°C to +85°C
Am311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameters (see definitions)	Test Conditions	Am311 Min.	Am311 Typ.	Am311 Max.	Am111 Am211 Min.	Am111 Am211 Typ.	Am111 Am211 Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500 Ω to +5 V, V_E = 0		200			200		ns
Supply Current								
Positive (Note 5)			3.9	7.5		3.9	6.0	mA
Negative (Note 5)			2.6	5.0		2.6	4.5	mA
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{IN} \leq -5$ mV, I_C = 50 mA					0.75	1.5	Volts
	$V_{IN} \leq -10$ mV, I_C = 50 mA		0.75	1.5				Volts
Output Leakage Current	$V_{IN} \geq +5$ mV, V_C to V_E = 50 V					0.2	10.0	nA
	$V_{IN} \geq +10$ mV, V_C to V_E = 40 V		0.2	50.0				nA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{IN} \leq -6$ mV, I_C = 8 mA					0.23	0.40	Volts
	$V_{IN} \leq -10$ mV, I_C = 8 mA		0.23	0.40				Volts
Output Leakage Current	$V_{IN} \geq +6$ mV, V_C to V_E = 50 V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		Volts
Supply Current								
Positive (Note 5)	T_A = 125°C					2.7	4.5	mA
Negative (Note 5)						1.8	3.5	mA

Notes: 1. For the Am111/211/311, derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4mW/°C for operation at ambient temperatures above 57°C.

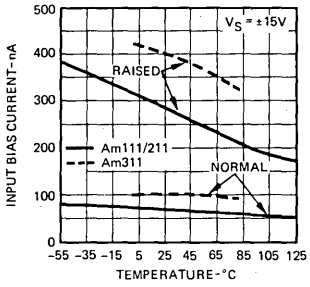
2. Unless otherwise specified, these specifications apply for V^+ = +15V, V− = −15V, V_E = −15V, and R_L at collector output = 7.5kΩ to +15V.

3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

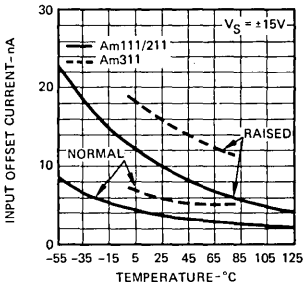
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

PERFORMANCE CURVES

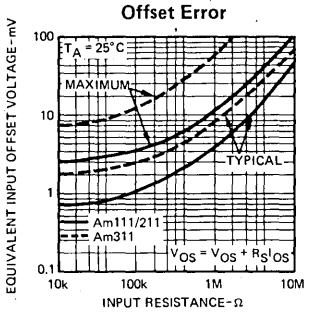
Input Bias Current



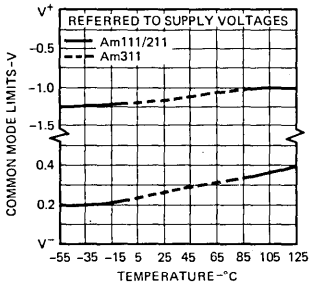
Input Offset Current



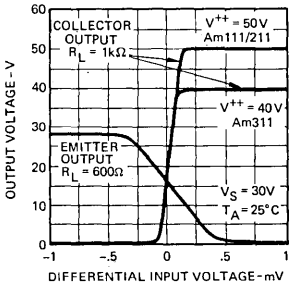
Offset Error



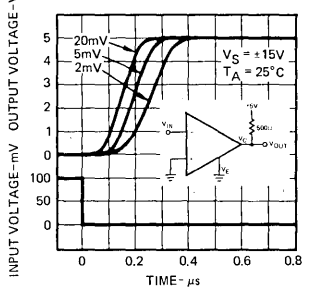
Common-Mode Limits



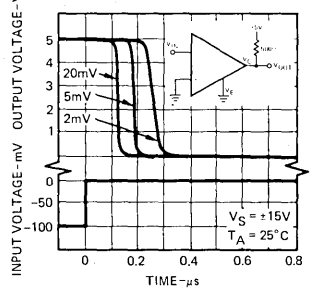
Transfer Function



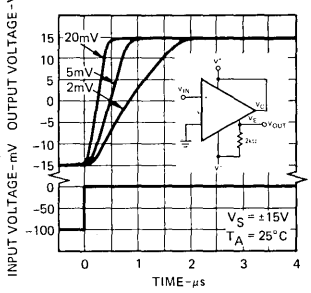
Response Time For Various Input Overdrives



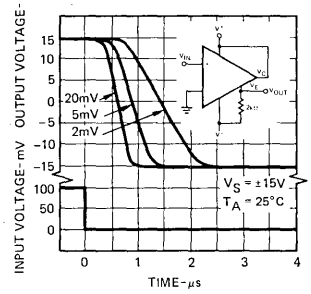
Response Time For Various Input Overdrives



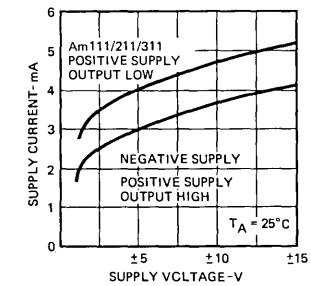
Response Time For Various Input Overdrives



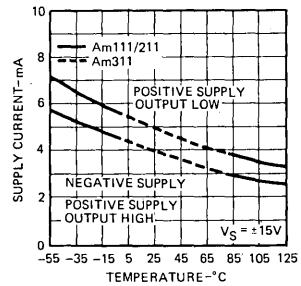
Response Time For Various Input Overdrives



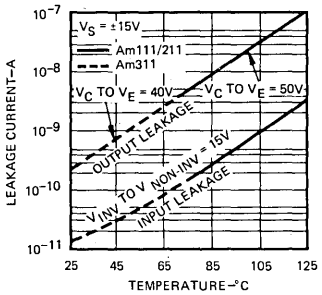
Supply Current



Supply Current

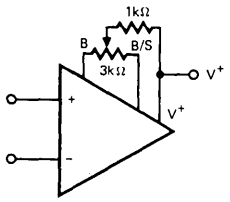


Leakage Current

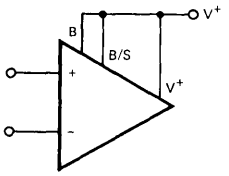


APPLICATIONS

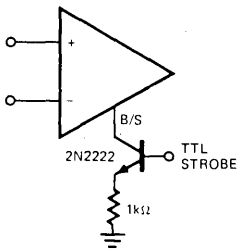
Offset Balancing



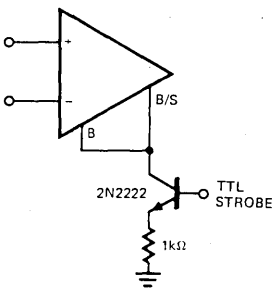
Increasing Input Stage Current*



Strobing



Strobing OFF both Input and Output Stages**



*Increases input bias current and common mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

Metallization and Pad Layout

LF111/LF211/LF311

Voltage Comparators

GENERAL DESCRIPTION

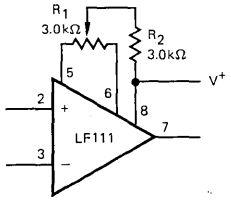
The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

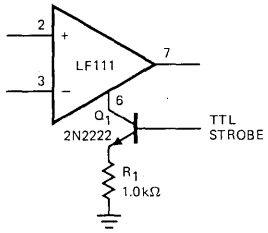
Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents.

TYPICAL APPLICATIONS

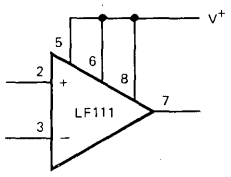
Offset Balancing



Strobing



Increasing Input Stage Current*



*Increases common-mode slew rate by a factor of 3.

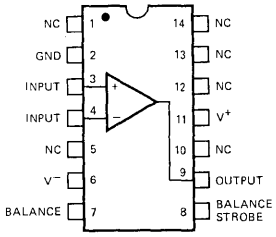
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LF311	Metal Can	0°C to +70°C	LF311H
	Hermetic DIP	0°C to +70°C	LF311D
	Flat Pack	0°C to +70°C	LF311F
	Dice	0°C to +70°C	LFD311
LF211	Metal Can	−25°C to +85°C	LF211H
	Hermetic DIP	−25°C to +85°C	LF211D
	Flat Pack	−25°C to +85°C	LF211F
LF111	Metal Can	−55°C to +125°C	LF111H
	Hermetic DIP	−55°C to +125°C	LF111D
	Flat Pack	−55°C to +125°C	LF111F
	Dice	−55°C to +125°C	LFD111

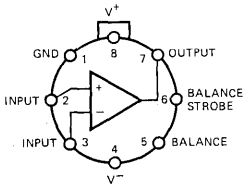
CONNECTION DIAGRAMS

Top Views

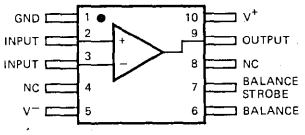
Dual-In-Line



Metal Can



Flat Package



Notes: 1. On Metal Can, pin 4 is connected to case.
2. On DIP and Flat Package, pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500mW	500mW
Output Short Circuit Duration	10 seconds	10 seconds
Operating Temperature Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

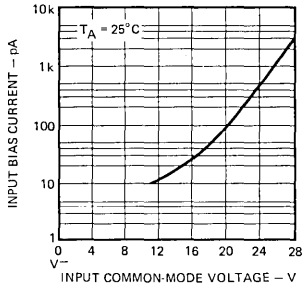
ELECTRICAL CHARACTERISTICS (Note 3)

Parameters	Test Conditions	LF111/LF211 Min.	LF111/LF211 Typ.	LF111/LF211 Max.	LF311 Min.	LF311 Typ.	LF311 Max.	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	4.0		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50		25	150	pA
Voltage Gain	$T_A = 25°C$		200			200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200			200		ns
Saturation Voltage	$V_{IN} \leq -5.0mV$, $I_{OUT} = 50mA$, $T_A = 25°C$		0.75	1.5				Volts
	$V_{IN} \leq -12mV$					0.75	1.5	
Strobe On Current	$T_A = 25°C$		3.0			3.0		mA
Output Leakage Current	$V_{IN} \geq 5.0mV$, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10				nA
	$V_{IN} \geq 12mV$					0.2	10	
Input Offset Voltage (Note 4)				6.0			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0		1.0		nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0		3.0		nA
Input Voltage Range			14			14		Volts
			−13.5			−13.5		
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$, $I_{SINK} \leq 8.0mA$, $V_{IN} \leq -8.0mV$		0.23	0.4				Volts
	$V_{IN} \leq -20mV$					0.23	0.4	
Output Leakage Current	$V_{IN} \geq 8.0mV$, $V_{OUT} = 35V$		0.1	0.5				μA
Positive Supply Current	$T_A = 25°V$		5.1	6.0		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

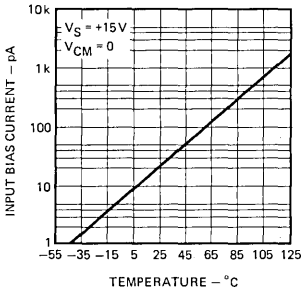
Notes:
1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of +185°C/W when mounted on a 1/16-inch thick epoxy glass board with ten, 0.03-inch wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line packages is +100°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0mV supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5.0mV overdrive.
6. For input voltages greater than 15V above the negative supply the bias and offset currents will increase — see typical performance curves.

TYPICAL PERFORMANCE

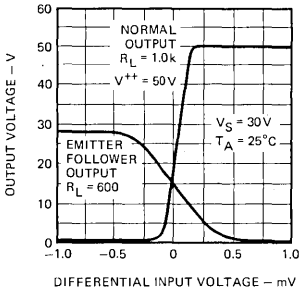
Input Bias Current Versus Common Mode



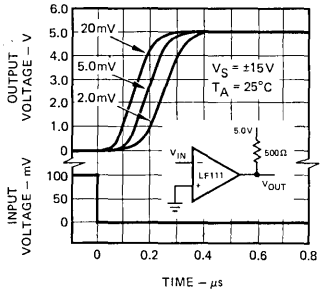
Input Bias Current Versus Temperature



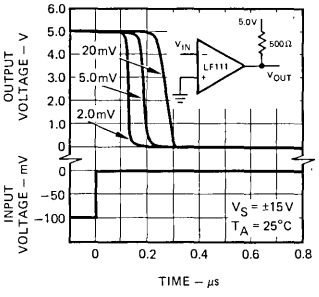
Transfer Function



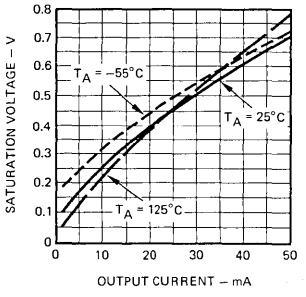
Response Time For Various Input Overdrives



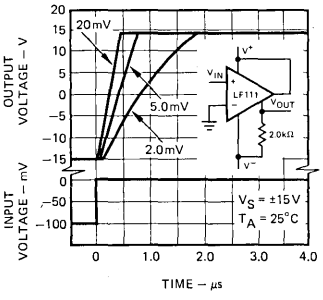
Response Time For Various Input Overdrives



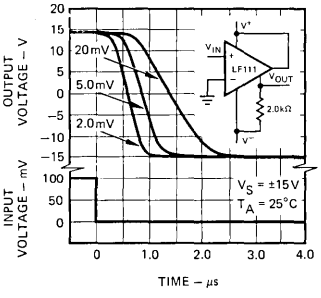
Output Saturation Voltage



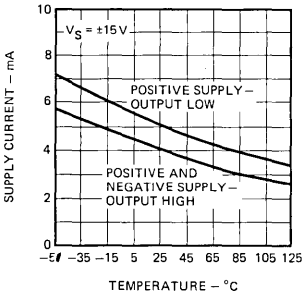
Response Time For Various Input Overdrives



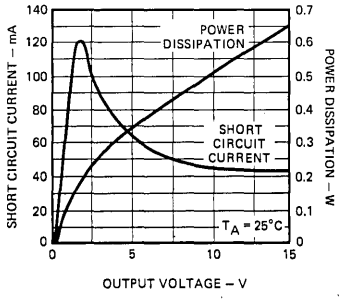
Response Time For Various Input Overdrives



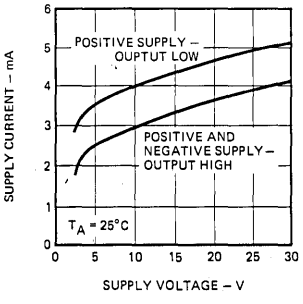
Supply Current



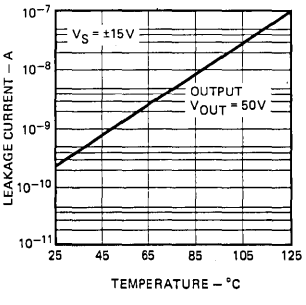
Output Limiting Characteristics



Supply Current



Leakage Current



Am119/219/319

Dual Comparator

Distinctive Characteristics

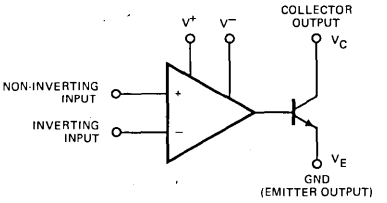
- The Am119/219/319 are functionally, electrically, and pin-for-pin equivalent to the National LM119/219/319.
- Two independent comparators.
- Operates from single 5V supply.
- Output drive – 35V and 25mA.
- Input bias current – 1μA max. (1.2μA for Am319)
- Response time 80ns typical at ±15V.
- Minimum fan out of 2 each side.
- Inputs and outputs isolated from system ground.
- High common mode slew rate.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Available in Metal Can, Hermetic Dual-In-Line, Hermetic Flatpack or Molded DIP packages.

FUNCTIONAL DESCRIPTION

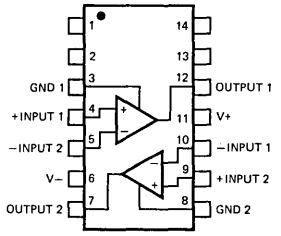
The Am119/219/319 are dual high-speed voltage comparators designed to operate over a wide range of voltage supplies down to a single 5V supply and ground. They have higher gain and lower input bias currents than devices such as the μA710. The uncommitted collector of the output stage facilitates RTL, DTL and TTL interfacing, and driving lamps and relays at currents up to 25mA. The device is specified for operation from power supplies up to ±15V and features faster response than the Am111 at the expense of higher power dissipation.

The Am119 performance is specified over the temperature range –55°C to 125°C, the Am219 performance is specified over the temperature range –25°C to 85°C and the Am319 performance is specified over the temperature range 0°C to 70°C.

FUNCTIONAL DIAGRAM
(One Comparator)

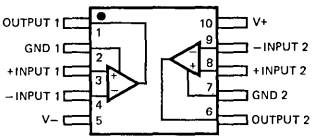


CONNECTION DIAGRAM
Top View
Dual In-Line



Pin 6 connected to bottom of package.

CONNECTION DIAGRAM
Top View
Flat Package

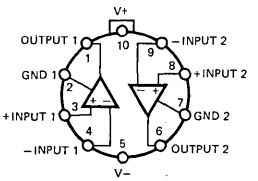


Pin 5 connected to bottom of package.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am319	TO-99	0°C to +70°C	LM319H
	DIP	0°C to +70°C	LM319D
	Molded DIP	0°C to +70°C	LM319N
	Dice	0°C to +70°C	LD319
Am219	TO-99	–25°C to +85°C	LM219H
	DIP	–25°C to +85°C	LM219D
	Flat Pak	–25°C to +85°C	LM219F
Am119	TO-99	–55°C to +125°C	LM119H
	DIP	–55°C to +125°C	LM119D
	Flat Pak	–55°C to +125°C	LM119F
	Dice	–55°C to +125°C	LD119

CONNECTION DIAGRAM
Top View
Metal Can



Pin 5 connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	36V
Voltage from Ground to V^+	18V
Voltage from Ground to V^-	25V
Differential Input Voltage	±5.0V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10s
Operating Temperature Range	
Am119	−55°C to +125°C
Am219	−25°C to +85°C
Am319	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

2

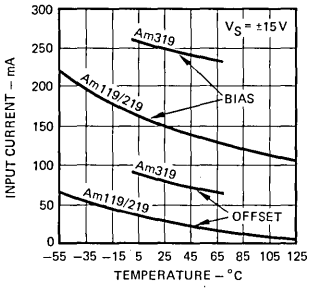
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Noted) (Note 3)

Parameters (See definitions)		Conditions	Am319 Min.	Am319 Typ.	Am319 Max.	Am119/219 Min.	Am119/219 Typ.	Am119/219 Max.	Units
Input Offset Voltage (Note 4)		$R_S \leq 5k$		2.0	8.0		0.7	4.0	mV
Input Offset Current (Note 4)				80	200		30	75	nA
Input Bias Current				250	1000		150	500	nA
Response Time (Note 5)				80			80		ns
Supply Current	Positive	$V^+ = 5.0V, V^- = 0$		4.3			4.3		mA
		$V_S = \pm 15V$		8.0	12.5		8.0	11.5	
	Negative	$V_S = \pm 15V$		3.0	5.0		3.0	4.5	
Voltage Gain			8.0	40		10	40		
Saturation Voltage		$V_{in} \leq -5.0mV, I_C = 25mA$					0.75	1.5	Volts
		$V_{in} \leq -10mV, I_C = 25mA$		0.75	1.5				
Output Leakage Current		$V_{in} \geq +5.0mV, V_C$ to $V_E = 35V$					0.2	2.0	μA
		$V_{in} \geq +10mV, V_C$ to $V_E = 35V$		0.2	10				
The Following Specifications Apply Over The Operating Temperature Ranges									
Input Offset Voltage (Note 4)		$R_S \leq 5k$			10			7.0	mV
Input Offset Current (Note 4)					300			100	nA
Input Bias Current					1200			1000	nA
Saturation Voltage		$V_{in} \leq -8.0mV, I_C = 3.2mA$, $T_A \geq 0°C$					0.23	0.4	Volts
		$V_{in} \leq -8.0mV, I_C = 3.2mA$, $T_A \leq 0°C$						0.6	
		$V_{in} \leq -12mV, I_C = 3.2mA$		0.3	0.4				
Output Leakage Current		$V_{in} \geq +8.0mV, V_C$ to $V_E = 35V$					1.0	10	μA
Input Voltage Range		$V_S = \pm 15V$		±13			±13		Volts
		$V^+ = 5.0V, V^- = 0$	1.0		3.0	1.0		3.0	

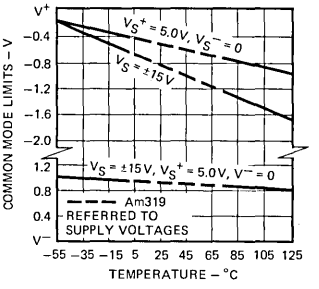
Notes:
1. For supply voltages less than ± 15V the absolute maximum rating is equal to the supply voltage.
2. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line at 9mW/°C for operation at temperatures above 95°C, and the Flat Package at 5.4mW/°C for operation at temperatures above 57°C.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ± 15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within 1 volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified is for a 100mV input step with 5mV overdrive.

TYPICAL PERFORMANCE CURVES

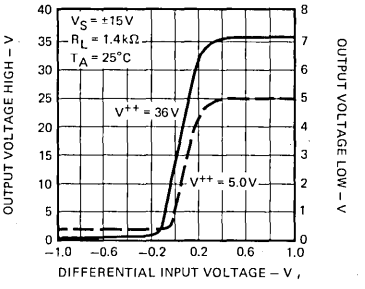
Input Currents



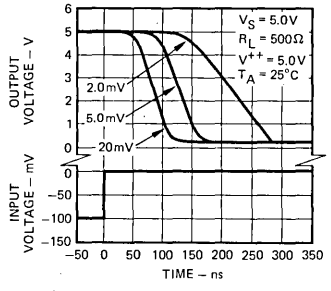
Common Mode Limits



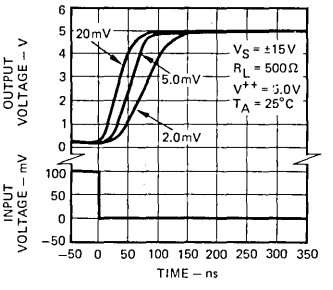
Transfer Function



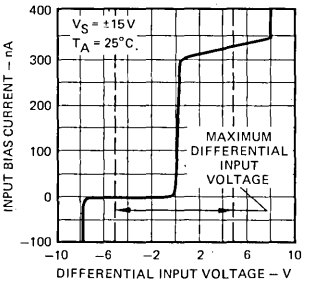
Response Time for Various Input Overdrives



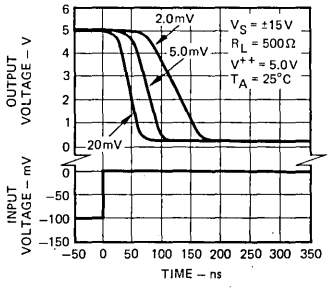
Response Time for Various Input Overdrives



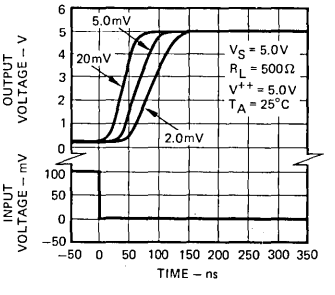
Input Characteristics



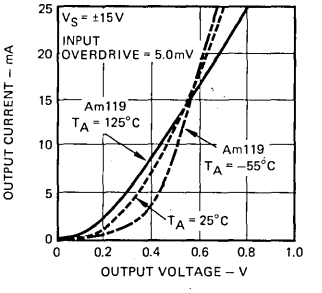
Response Time for Various Input Overdrives



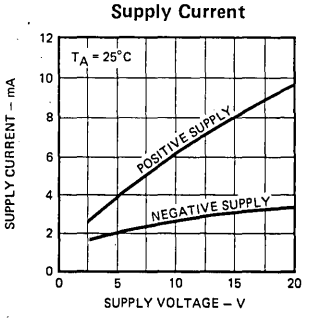
Response Time for Various Input Overdrives



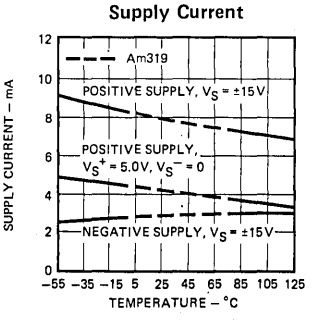
Output Saturation Voltage



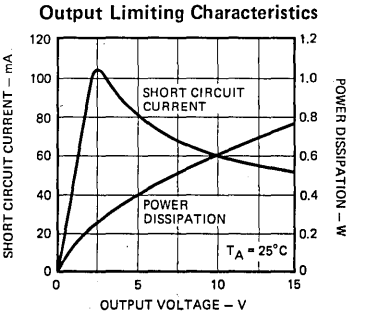
Supply Current



Supply Current

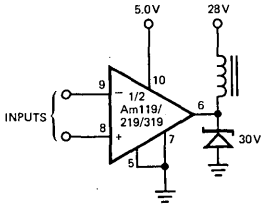


Output Limiting Characteristics

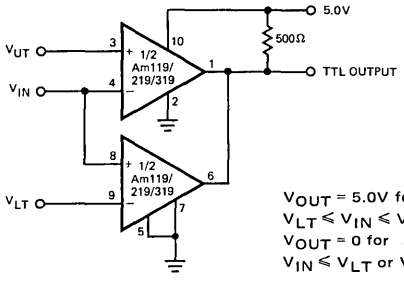


APPLICATIONS

Relay Driver



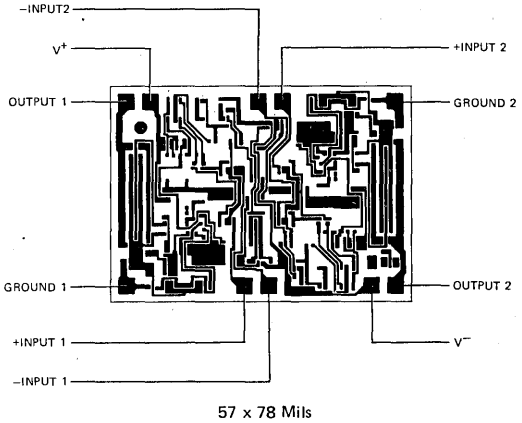
Window Detector



V_{OUT} = 5.0V for
$V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0 for
$V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$

2

Metallization and Pad Layout



57 x 78 Mils

Am139/239/339 • Am139A/239A/339A

Low Offset Voltage Quad Comparators

Distinctive Characteristics

- Four high precision comparators
- Reduced VOS drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Wide single supply voltage range or dual supplies
  $2.0V_{DC}$ to $36V_{DC}$
  $\pm 1.0V_{DC}$ to $\pm 18V_{DC}$
- Very low supply current drain (0.8mA)—independent of supply voltage (1.0mW/comparator) makes these comparators suitable for battery operation.
- Low input bias current – 35nA
- Low input offset current – 3.0nA and offset voltage – 2.0mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage
  1.0mV at 5.0μA
  60mV at 1.0mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

FUNCTIONAL DESCRIPTION

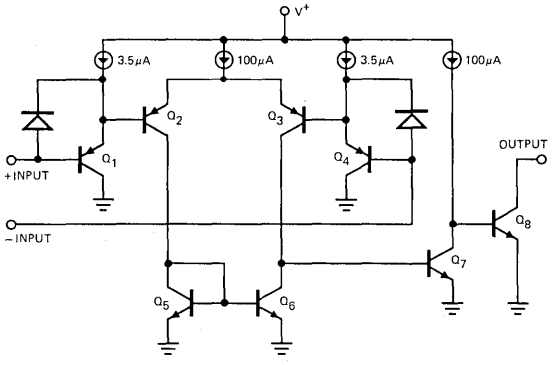
The Am139, Am239, Am339, Am339A, Am239A and Am339A quad comparators are functionally, electrically and pin-for-pin equivalent to the National LM139, LM239, LM339, LM339A, LM239A and LM339A. This series of precision comparators consists of four independent voltage comparators which were specifically designed to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The Am139/A series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the Am139/A will directly interface with MOS logic – where the lower power drain of the Am139/A is a distinct advantage over standard comparators.

ORDERING INFORMATION

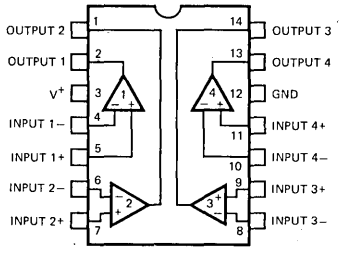
Part Number	Package Type	Temperature Range	Order Number
Am339	DIP	0°C to 70°C	LM339D
	Molded DIP	0°C to 70°C	LM339N
	Dice	0°C to 70°C	LD339
Am239	DIP	–25°C to +85°C	LM239D
Am139	DIP	–55°C to +125°C	LM139D
	Flat Pack	–55°C to +125°C	LM139F
	Dice	–55°C to +125°C	LD139
Am339A	DIP	0°C to 70°C	LM339AD
	Molded DIP	0°C to 70°C	LM339AN
	Dice	0°C to 70°C	LD339A
Am239A	DIP	–25°C to +85°C	LM239AD
Am139A	DIP	–55°C to +125°C	LM139AD
	Flat Pack	–55°C to +125°C	LM139AF
	Dice	–55°C to +125°C	LD139A

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage, V+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Ceramic Dip	900 mW
Plastic Dip	570 mW
Flat Pack	800 mW
Output Short Circuit to GND (Note 2)	Continuous
Input Current (V_{in} −0.3 V_{DC}) (Note 3)	50 mA
Operating Temperature Range	
Am339/A	0°C to +70°C
Am239/A	−25°C to +85°C
Am139/A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

(V^+ = +5.0V_{DC}) (Note 4)

Parameters	Test Conditions	Am239 Am339 Min.	Am239 Am339 Typ.	Am239 Am339 Max.	Am139 Min.	Am139 Typ.	Am139 Max.	Am239A Am339A Min.	Am239A Am339A Typ.	Am239A Am339A Max.	Am139A Min.	Am139A Typ.	Am139A Max.	Units
Input Offset Voltage	T_A = +25°C (Note 9)		±2.0	±5.0		±2.0	±5.0		±1.0	±2.0		±1.0	±2.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = +25°C		25	250		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C		±5.0	±50		±3.0	±25		±5.0	±50		±3.0	±25	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	T_A = +25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L = ∞ on all Comparators T_A = +25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
Voltage Gain	R_L ≥ 15kΩ, T_A = +25°C, V^+ = 15 V_{DC} (To Support Large V_o Swing)		200			200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V_{DC}, V_{R_L} = 5.0V_{DC}, R_L = 5.1kΩ and T_A = +25°C		300			300			300			300		ns
Response Time (Note 7)	V_{R_L} = 5.0 V_{DC} and R_L = 5.1 kΩ T_A = +25°C		1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0, and V_o ≤ +1.5 V_{DC}, T_A = +25°C	6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0, and I_{sink} ≤ 4.0 mA, T_A = +25°C		250	500		250	500		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ ≥ +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 5.0 V_{DC}, T_A = +25°C		0.1			0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			9.0			9.0			4.0			4.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150			±100			±150			±100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400			300			400			300	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0 and I_{sink} ≤ 4.0 mA			700			700			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ ≥ +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 30 V_{DC}			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage (Note 8)	Keep all V_{IN}'s ≥ 0 V_{DC} (or V^- if used)			36			36			V^+			V^+	V_{DC}

Note 1: For high temperature operation, the Am339/A must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am239/A and Am139/A must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate.

2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal outputs states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.

4: These specifications apply for V^+ = +5.0 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the Am239/A all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C and the Am339/A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5 V, but either or both inputs can go to +30 V_{DC} without damage.

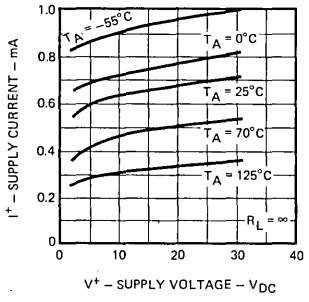
7: The response time specified is for a 100mV input step with 5.0mV overdrive. 300ns can be achieved with larger overdrive signals, see typical performance characteristics section.

8: If the voltage applied to any input exceeds V^+, all four comparator outputs will go to the high voltage level. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).

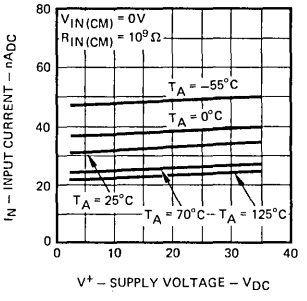
9: At output switch point, $V_O \cong 1.4V_{DC}$, R_S = 0Ω with V^+ from 5.0 V_{DC}; and over the full input common mode range (0 V_{DC} to V^+ -1.5V_{DC}).

TYPICAL PERFORMANCE CHARACTERISTICS

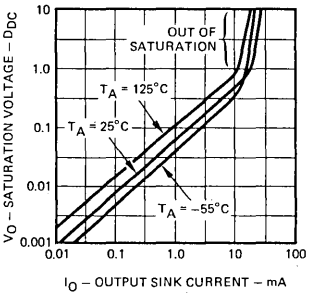
Supply Current



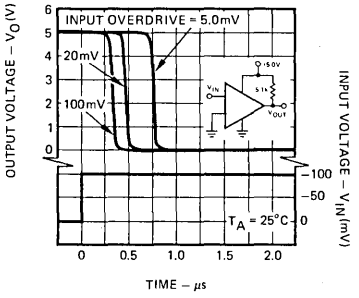
Input Current



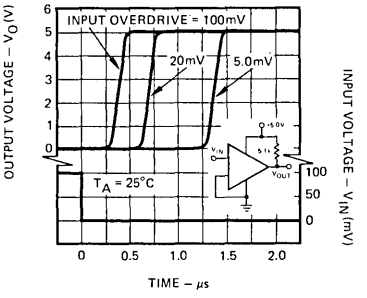
Output Saturation Voltage



Response Time for Various Input Overdrives Negative Transition



Response Time for Various Input Overdrives Positive Transition



APPLICATION HINTS

The Am139/A is a high gain, wide bandwidth device; which like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. The oscillation shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Lowering the input resistors to $<10k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C card attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the Am139/A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30\ V_{DC}$.

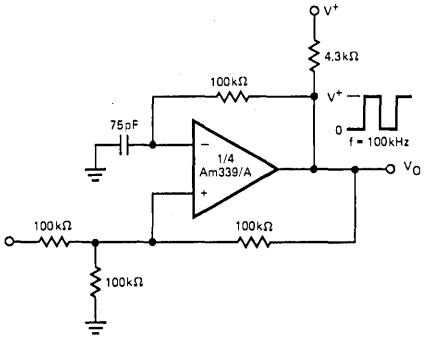
It is not normally necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

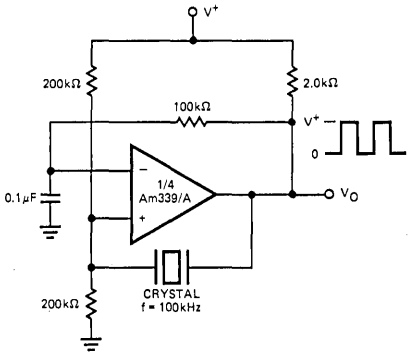
The output of the Am139/A is the uncommitted collector of a grounded-emitter NPN output transistor. Several collectors can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the Am139/A package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp very nearly to ground level for small load currents.

TYPICAL APPLICATIONS

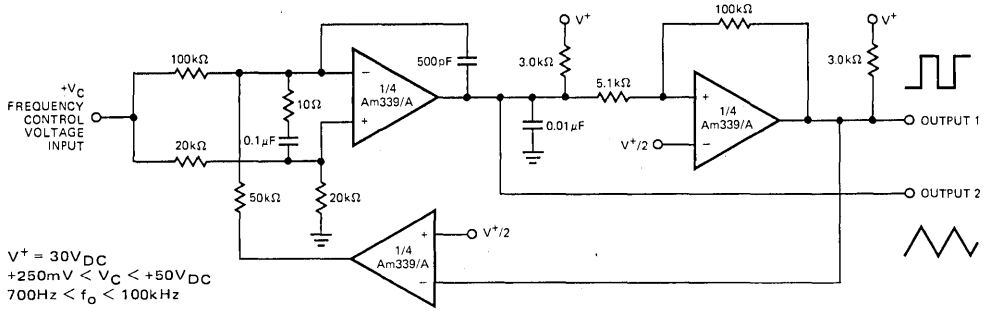
($V^+ = 5.0V_{DC}$)



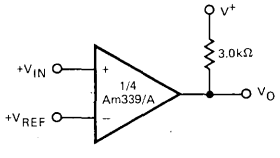
Squarewave Oscillator



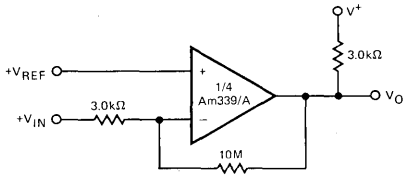
Crystal Controlled Oscillator



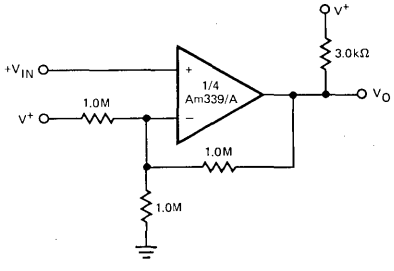
Two-Decade High-Frequency VCO



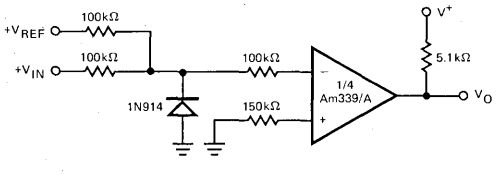
Basic Comparator



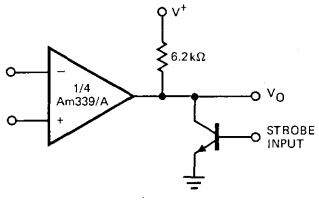
Non-Inverting Comparator with Hysteresis



Inverting Comparator with Hysteresis



Comparing Input Voltages of Opposite Polarity

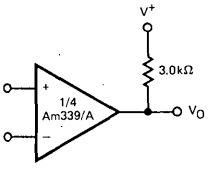


*Or logic gate without pull-up resistor.

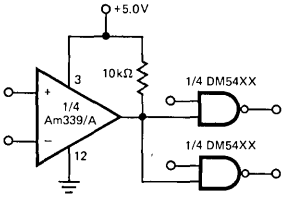
Output Strobing

TYPICAL APPLICATIONS (Cont.)

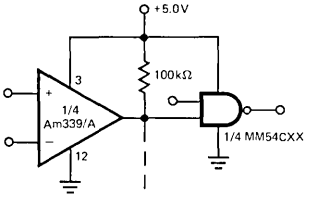
($V^+ = 5.0V_{DC}$)



Basic Comparator

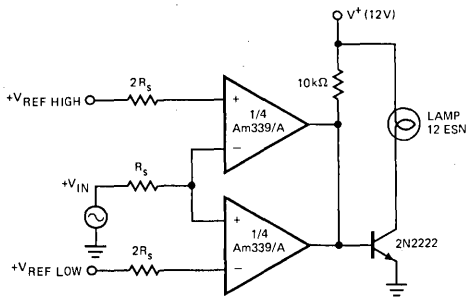


Driving TTL

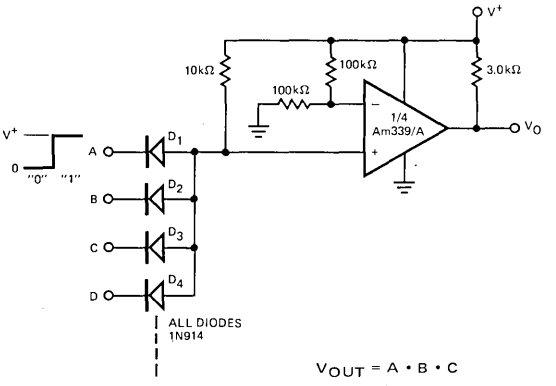


Driving CMOS

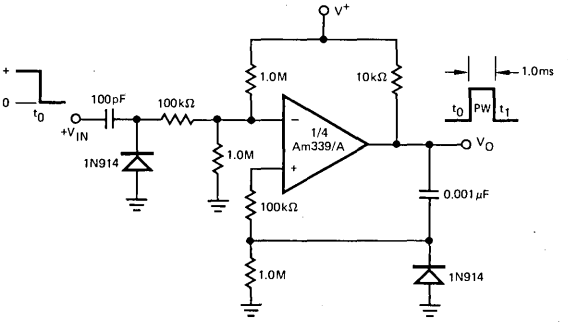
($V^+ = 15V_{DC}$)



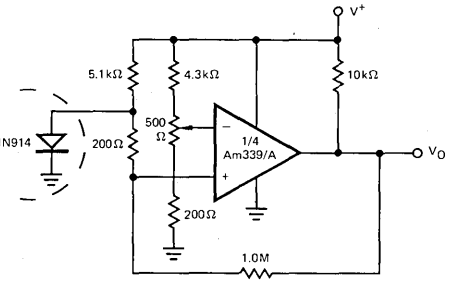
Limit Comparator



Large Fan-In AND Gate



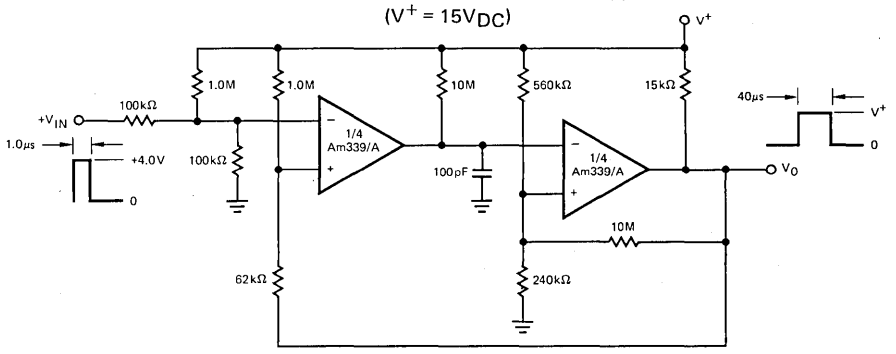
One-Shot Multivibrator



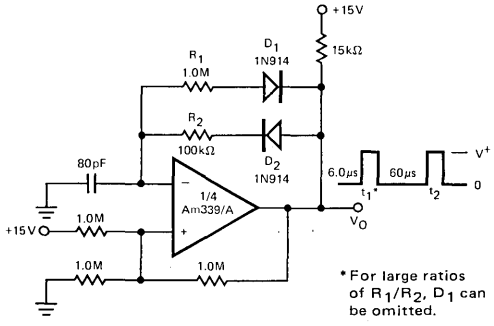
Remote Temperature Sensing

TYPICAL APPLICATIONS (Cont.)

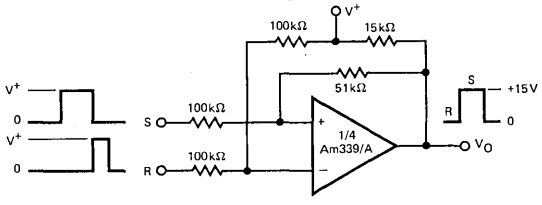
($V^+ = 15V_{DC}$)



One-Shot Multivibrator with Input Lock Out

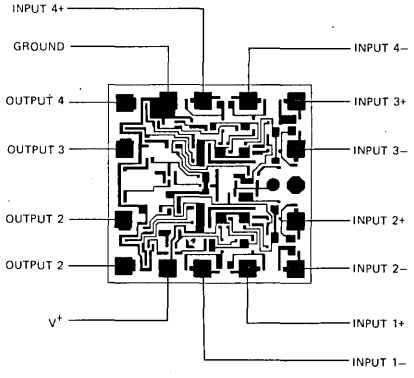


Pulse Generator



Bi-Stable Multivibrator

Metallization and Pad Layout



47 x 48 Mils

Am685

Voltage Comparator

Distinctive Characteristics:

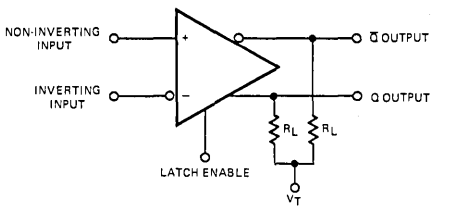
- 6.5ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- 3.0ns Latch setup time
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products
- Available in metal can and hermetic dual-in-line packages

FUNCTIONAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

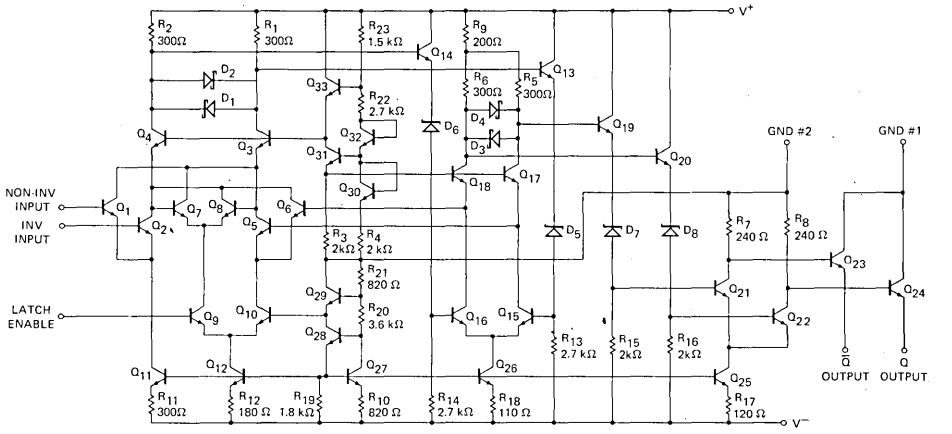
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0 V, or 200–2000Ω connected to –5.2 V.

CIRCUIT DIAGRAM



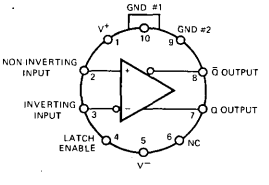
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am685	Metal Can	–30°C to +85°C	Am685HL
	DIP	–30°C to +85°C	Am685DL
Am685	Metal Can	–55°C to +125°C	Am685HM
	DIP	–55°C to +125°C	Am685DM
Am685	Dice	–30°C to +85°C	Am685XL
	Dice	–55°C to +125°C	Am685XM

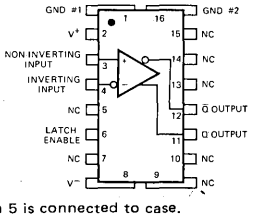
CONNECTION DIAGRAMS

Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case. On DIP, pin 8 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	500 mW

Operating Temperature Range	
Am685-L	−30°C to +85°C
Am685-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd+(E)}$	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd-(E)}$	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
$t_{pw(E)}$	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

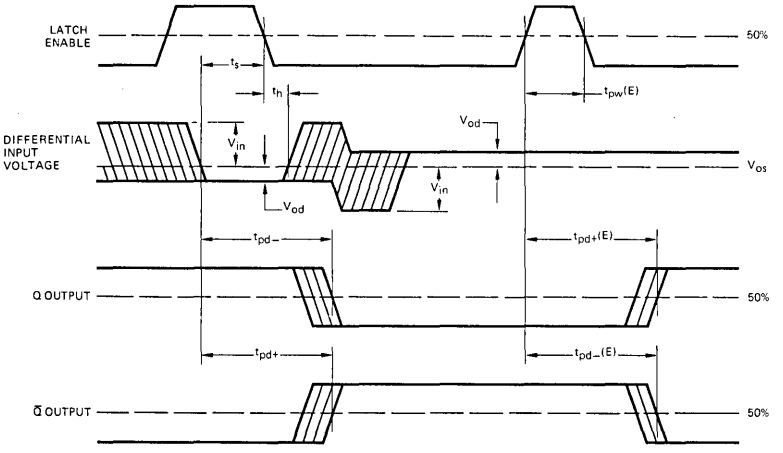
NOTES:

2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3: Unless otherwise specified $V^+ = 6.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

TIMING DIAGRAM



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

Figure 1

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** — The average of the two input currents.

R_{IN} **INPUT RESISTANCE** — The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** — The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I^+ **POSITIVE SUPPLY CURRENT** — The current required from the positive supply to operate the comparator.

I^- **NEGATIVE SUPPLY CURRENT** — The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** — The power dissipated by the comparator with both outputs terminated in 50Ω to -2.0V.

SWITCHING TERMS (refer to Fig. 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ **LATCH ENABLE TO OUTPUT HIGH DELAY** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ **LATCH ENABLE TO OUTPUT LOW DELAY** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **MINIMUM LATCH ENABLE PULSE WIDTH** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

OTHER SYMBOLS

T_A	Ambient temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{in}	Input pulse amplitude
V^+	Positive supply voltage	V_{od}	Input overdrive
V^-	Negative supply voltage	f	Frequency

MEASUREMENT OF PROPAGATION DELAY

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large- and small-signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100mV step with an overdrive of 5mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50% point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.

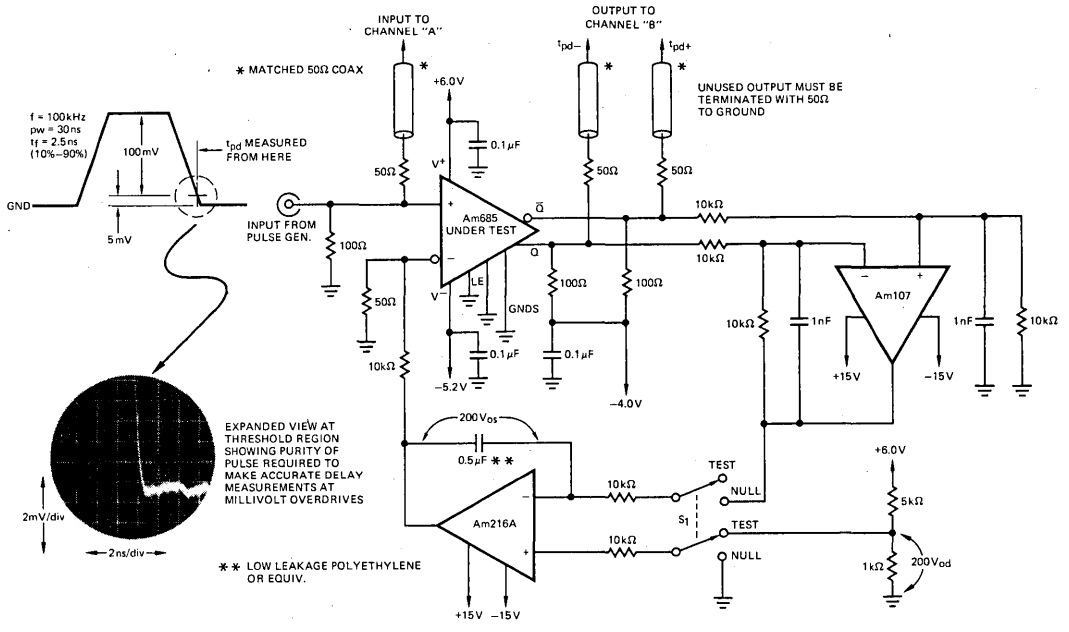


Figure 2

The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50Ω inputs of the sampling scope via equal lengths of 50Ω coaxial cable. For the conditions shown in the figure, t_{pd+} is measured at the $\overline{Q}$ output and t_{pd-} at the Q output. If it is desired to measure the opposite output polarities, the polarities of the input signal and overdrive must be reversed.

THERMAL CONSIDERATIONS

To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

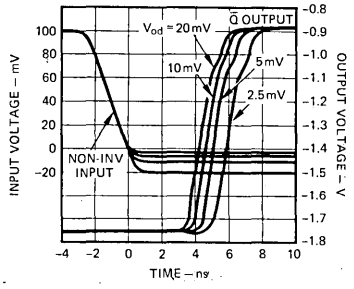
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60dB) at very high frequencies (100MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to -2.0V, but a Thevenin equivalent to V^- can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.

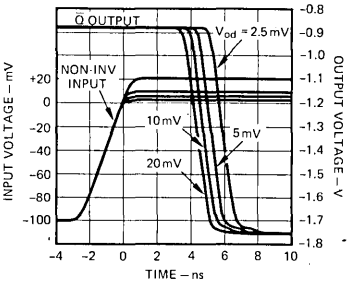
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

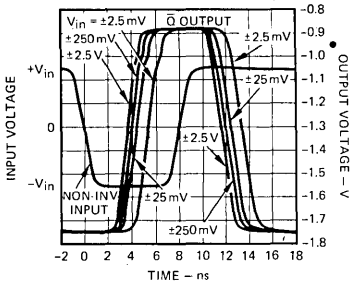
Response for Various Input Overdrives



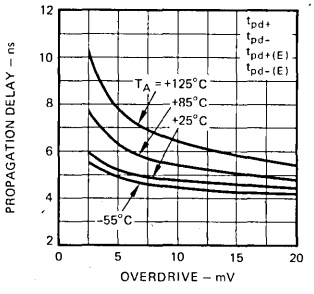
Response for Various Input Overdrives



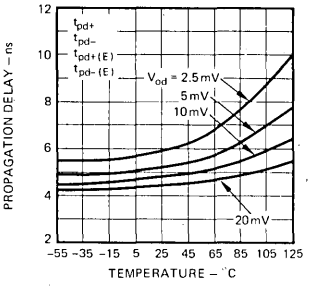
Response for Various Input Signal Levels



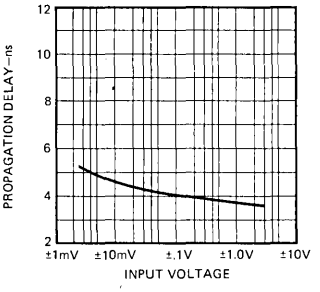
Propagation Delays as a Function of Input Overdrive



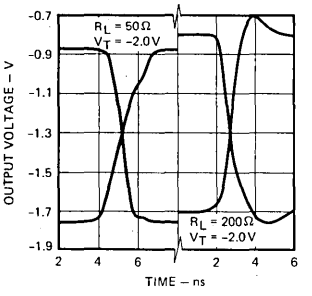
Propagation Delays as a Function of Temperature



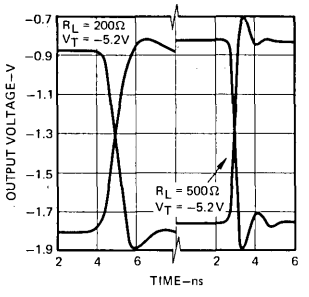
Propagation Delay as a Function of Input Signal Level



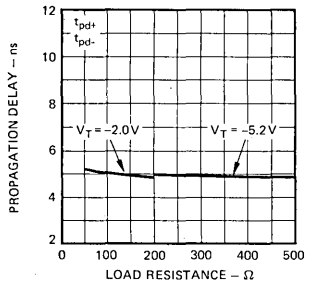
Response for Various Load Resistances



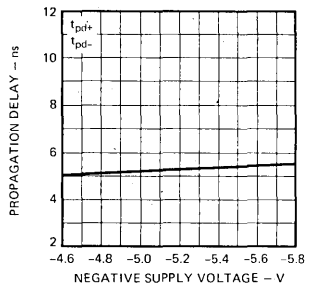
Response for Various Load Resistances



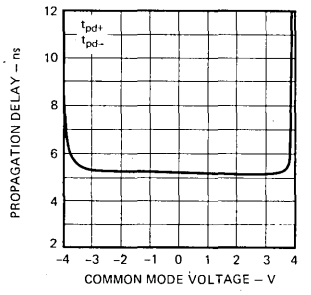
Propagation Delays as a Function of Load Resistance



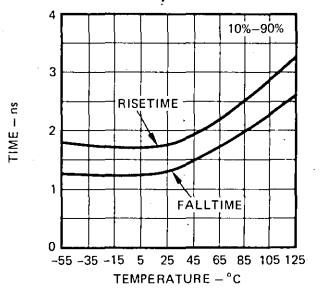
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



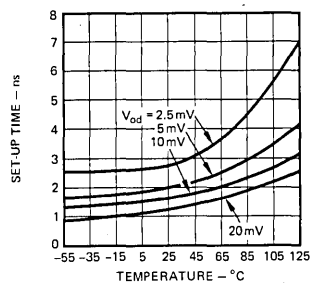
Output Rise and Fall Times as a Function of Temperature



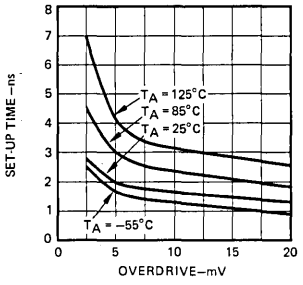
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

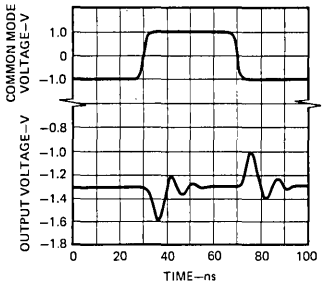
Set-up Time as a Function of Temperature



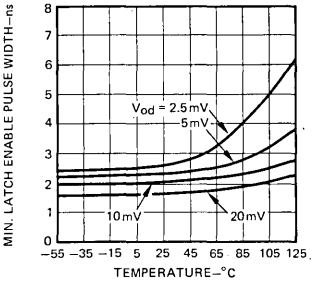
Set-up Time as a Function of Input Overdrive



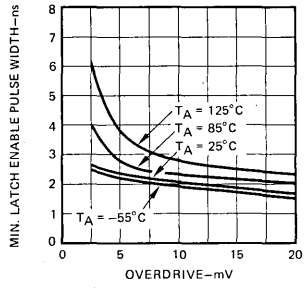
Common Mode Pulse Response



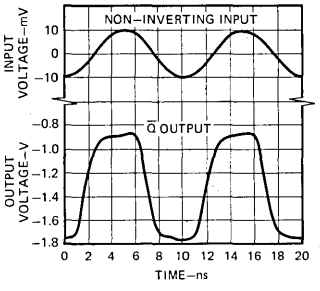
Min. Latch Enable Pulse Width as a Function of Temperature



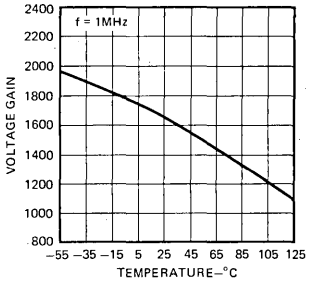
Min. Latch Enable Pulse Width as a Function of Input Overdrive



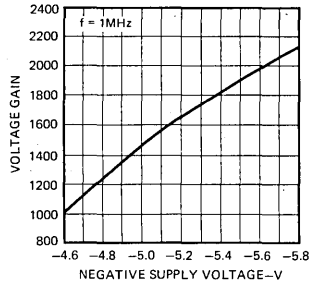
Response to 100MHz Sine Wave



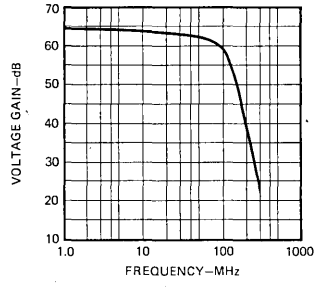
Voltage Gain as a Function of Temperature



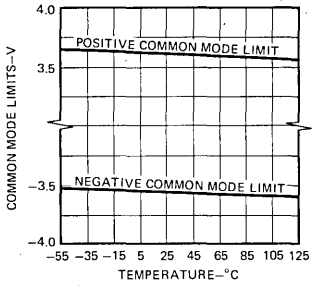
Voltage Gain as a Function of Negative Supply Voltage



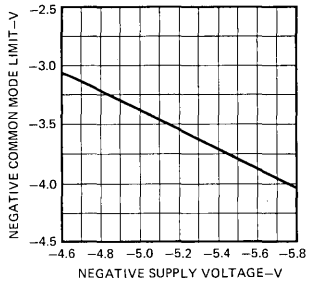
Voltage Gain as a Function of Frequency



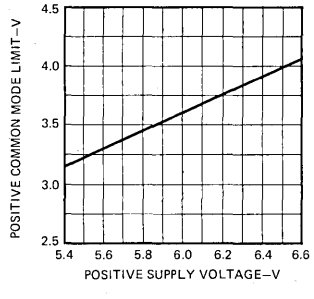
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



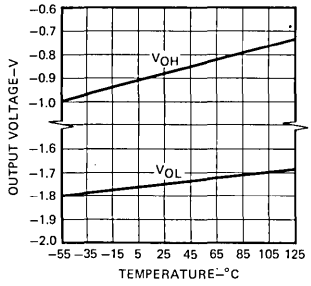
Positive Common Mode Limit as a Function of Positive Supply Voltage



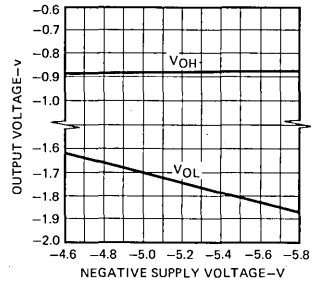
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

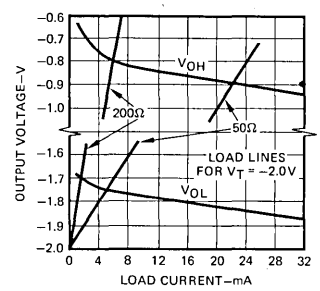
Output Levels as a Function of Temperature



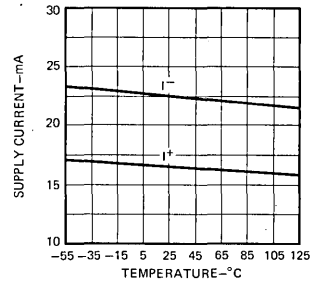
Output Levels As A Function Of Negative Supply Voltage



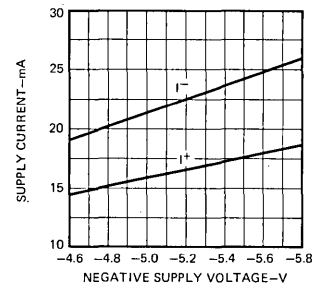
Output Levels As A Function Of DC Loading



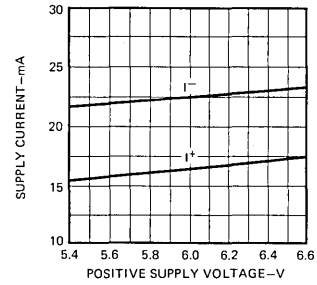
Supply Currents As A Function Of Temperature



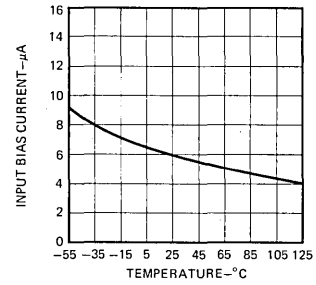
Supply Currents As A Function Of Negative Supply Voltage



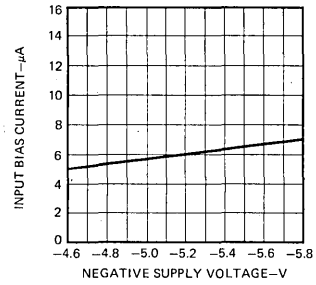
Supply Currents As A Function Of Positive Supply Voltage



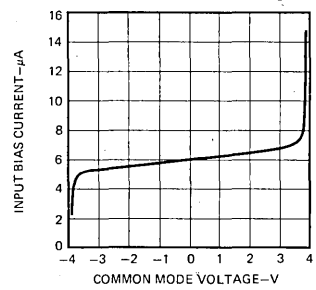
Input Bias Current As A Function Of Temperature



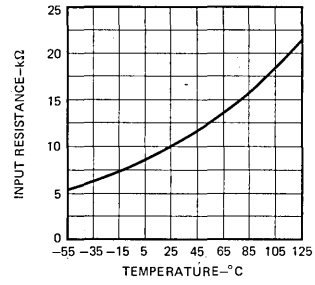
Input Bias Current As A Function Of Negative Supply Voltage



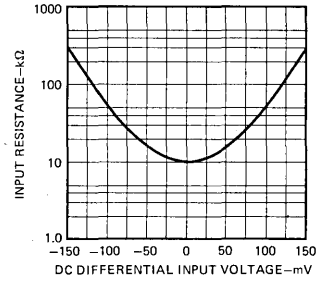
Input Bias Current As A Function Of Common Mode Voltage



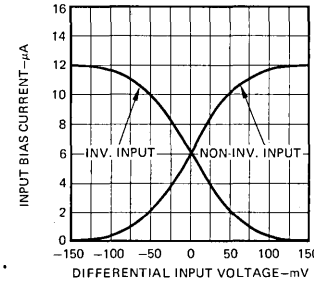
Input Resistance As A Function Of Temperature



Input Resistance As A Function Of DC Differential Input Voltage

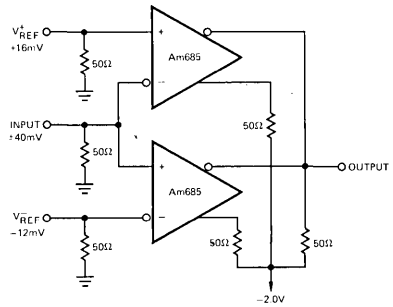


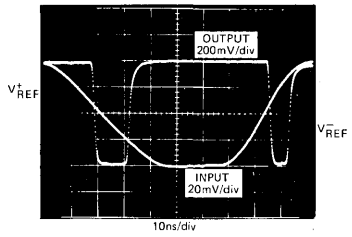
Input Current As A Function Of Differential Input Voltage



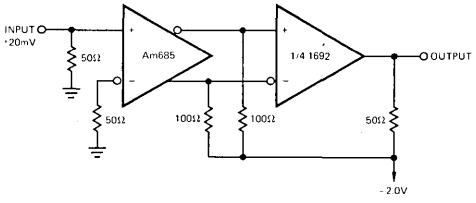
TYPICAL APPLICATIONS
(T_A = 25°C)

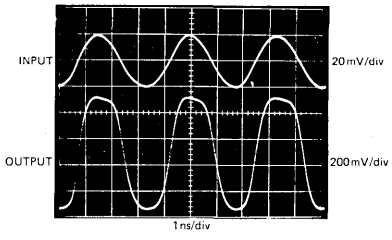
High-Speed Window Detector



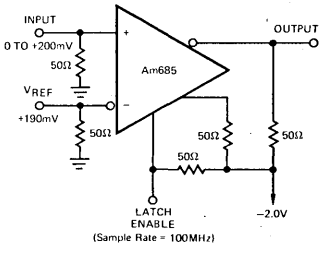


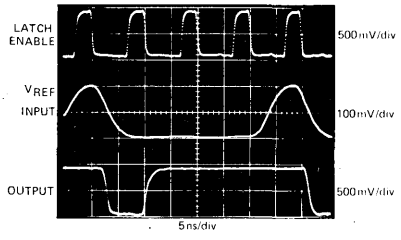
300MHz Line Receiver





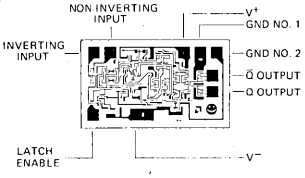
High-Speed Sampling





Metallization and Pad Layout

32 x 54 Mils



Am686
Voltage Comparator

Distinctive Characteristics

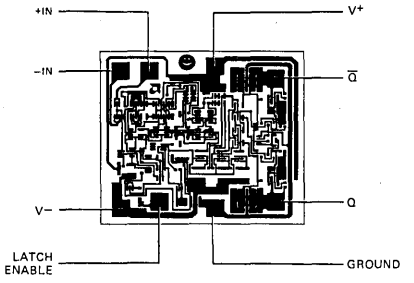
- 12ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary Schottky TTL outputs
- Fanout of 5
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in metal can and hermetic dual-in-line packages.

FUNCTIONAL DESCRIPTION

The Am686 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with Schottky TTL. The output current capability is adequate for driving 5 standard Schottky inputs. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

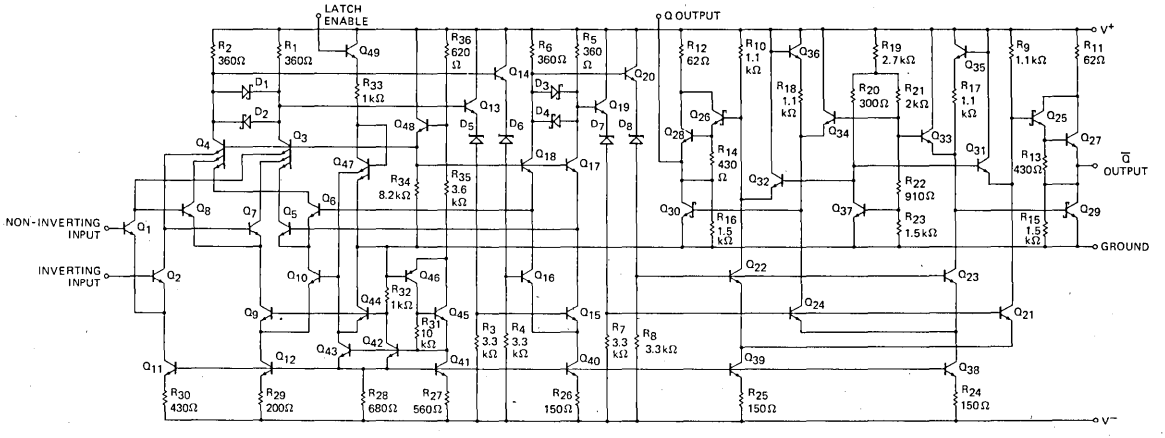
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is LOW, the comparator functions normally. When the Latch Enable is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable may be left open or connected to ground.

Metallization and Pad Layout



46 X 53 Mils

CIRCUIT DIAGRAM

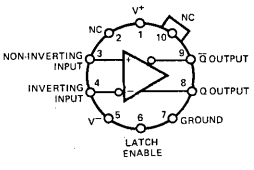


ORDERING INFORMATION

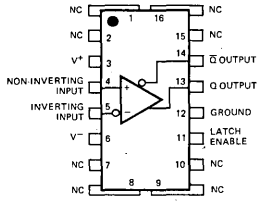
Part Number	Package Type	Temperature Range	Order Number
Am686	Metal Can	0°C to 70°C	Am686HC
	DIP	0°C to 70°C	Am686DC
Am686	Metal Can	−55°C to +125°C	Am686HM
	DIP	−55°C to +125°C	Am686DM
Am686	Dice	0°C to 70°C	Am686XC
	Dice	−55°C to +125°C	Am686XM

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case. On DIP, pin 6 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7V
Negative Supply Voltage	−7V
Input Voltage	±4V
Differential Input Voltage	±6V
Power Dissipation (Note 2)	600mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C

Operating Temperature Range	
Am686-C	0°C to +70°C
Am686-M	−55°C to +125°C
Operating Supply Voltage Range	
Am686-C	V^+ = +5.0V ±5%, V^- = −6.0V ±5%
Am686-M	V^+ = +5.0V ±10%, V^- = −6.0V ±10%
Minimum Operating Voltage (V^+ to V^-)	9.7V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$	3.0 3.5	2.0 3.0	mV MAX. mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	10	10	µV/°C MAX.
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_A$ (max.) $T_A = T_A$ (min.)	1.0 1.3	1.0 1.6	µA MAX. µA MAX.
I_B	Input Bias Current	$25°C \leq T_A \leq T_A$ (max.) $T_A = T_A$ (min.)	10 13	10 16	µA MAX. µA MAX.
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	V MIN.
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3V \leq V_{CM} \leq +2.7V$	80	80	dB MIN.
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$	70	70	dB MIN.
V_{OH}	Output HIGH voltage	$I_L = -1.0mA$, $V_S = V_S$ (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	$I_L = 10mA$, $V_S = V_S$ (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

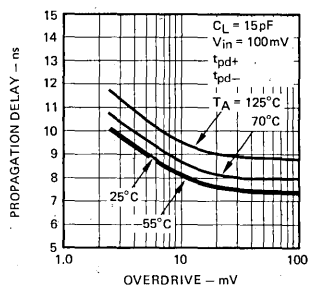
Switching Characteristics (V^+ = +5.0V, V^- = −6.0V, V_{in} = 100mV, V_{od} = 5.0mV, C_L = 15pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) $\leq T_A \leq 25°C$ $T_A = T_A$ (max.)	12 15	12 15	ns MAX. ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) $\leq T_A \leq 25°C$ $T_A = T_A$ (max.)	12 15	12 15	ns MAX. ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	$T_A = 25°C$	2.0	2.0	ns MAX.

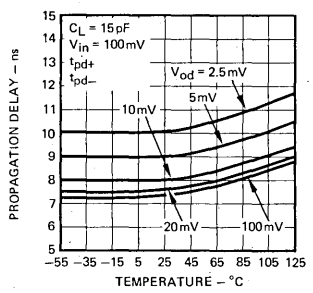
Notes:
2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.
3. Unless otherwise specified, V^+ = +5.0V, V^- = −6.0V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

PERFORMANCE CURVES

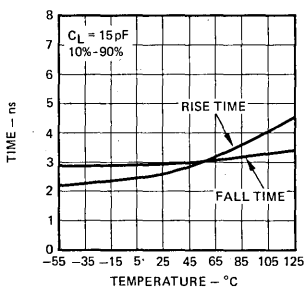
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



Am687·Am687A

Dual Voltage Comparators

Distinctive Characteristics

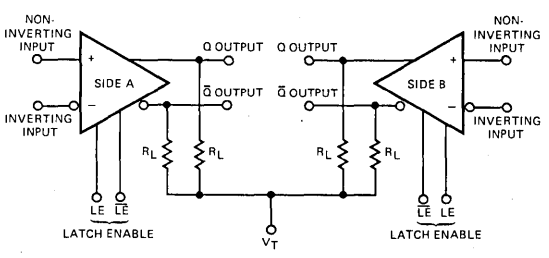
- **8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE**
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in the hermetic dual-in-line package.

FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

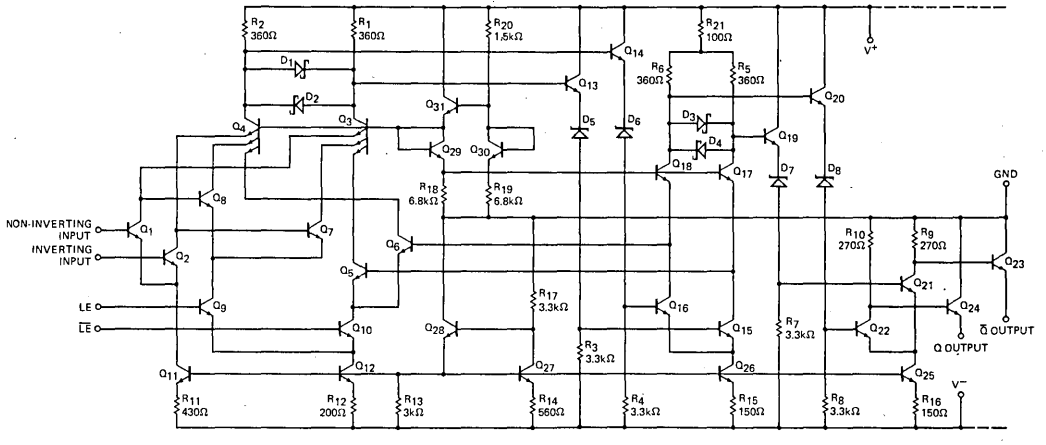
The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 6V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and $\overline{LE}$ is LOW, the comparator functions normally. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V, or 200–2000Ω connected to −5.2V.

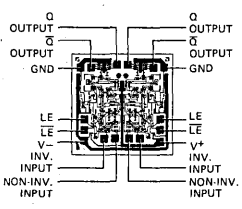
CIRCUIT DIAGRAM (Each Comparator)



ORDERING INFORMATION

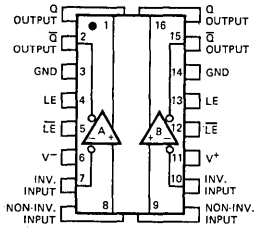
Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	−30°C to +85°C	AM687ADL
Am687A	DIP	−55°C to +125°C	AM687ADM
Am687	DIP	−30°C to +85°C	AM687DL
Am687	DIP	−55°C to +125°C	AM687DM
Am687	Dice	−30°C to +85°C	AM687XL
Am687	Dice	−55°C to +125°C	AM687XM

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.056"

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	600 mW

Operating Temperature Range	
Am687-L, Am687A-L	−30°C to +85°C
Am687-M, Am687A-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L / Am687-L Min.	Am687A-L / Am687-L Max.	Am687A-M / Am687-M Min.	Am687A-M / Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−3.5	+3.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$25°C \leq T_A \leq T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

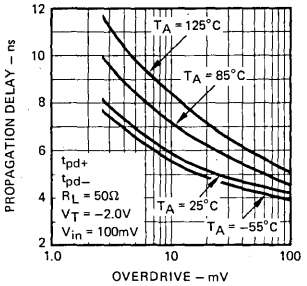
Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

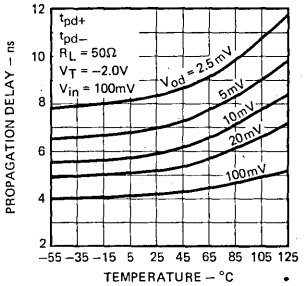
Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.
3. Unless otherwise specified $V^+ = +5.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

PERFORMANCE CURVES

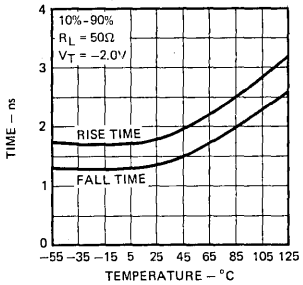
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



Am1500

Dual Precision Voltage Comparator

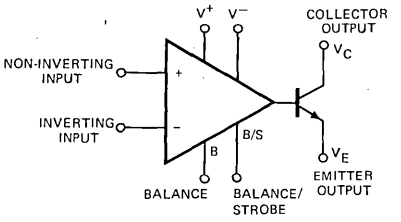
Distinctive Characteristics

- The Am1500 is functionally, electrically, and pin-for-pin equivalent to the National LH2111
- The Am1500 is a dual 111, but requires 25% less power than two 111 comparators
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage Range – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in Hermetic Dual-In-Line or Hermetic Flat Packages

FUNCTIONAL DESCRIPTION

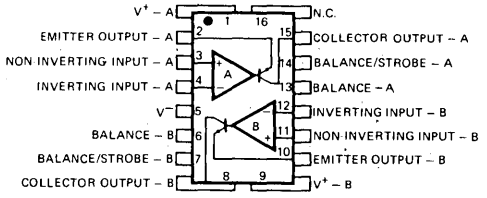
The Am1500 is a voltage comparator featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

FUNCTIONAL DIAGRAM
(each half)

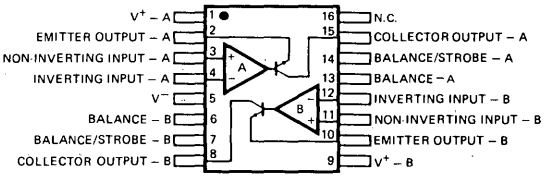


CONNECTION DIAGRAMS
Top Views

Dual In-Line



Flat Package



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1500C	TO-99	0°C to +70°C	AM1500DC
	Hermetic DIP	0°C to +70°C	AM1500FC
Am1500L	TO-99	–25°C to +85°C	AM1500DL
	Hermetic DIP	–25°C to +85°C	AM1500FL
Am1500M	Hermetic DIP	–55°C to +125°C	AM1500DM
	Flat Pak	–55°C to +125°C	AM1500FM

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
Am1500M, L	50V
Am1500C	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, −0V
Voltage from Inputs to V^+	−30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am1500M	−55°C to +125°C
Am1500L	−25°C to + 85°C
Am1500C	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

2

ELECTRICAL CHARACTERISTICS

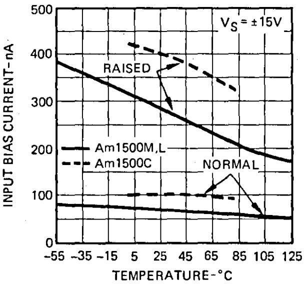
(T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am1500C Min.	Am1500C Typ.	Am1500C Max.	Am1500M Am1500L Min.	Am1500M Am1500L Typ.	Am1500M Am1500L Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current—Positive (Note 5)			3.9	7.5		7.0	9.5	mA
—Negative (Note 5)			2.6	5.0		4.8	7.5	
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{in} \leq -5.0mV$, I_C = 50mA					0.75	1.5	V
	$V_{in} \leq -10mV$, I_C = 50mA		0.75	1.5				
Output Leakage Current	$V_{in} \geq +5.0mV$, V_C to V_E = 50V					0.2	10.0	nA
	$V_{in} \geq +10mV$, V_C to V_E = 40V		0.2	50.0				
The Following Specifications Apply Over The Operating Temperature Range								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{in} \leq -6.0mV$, I_C = 8.0mA					0.23	0.40	V
	$V_{in} \leq -10mV$, I_C = 8.0mA		0.23	0.40				
Output Leakage Current	$V_{in} \geq +6.0mV$, V_C to V_E = 50V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current—Positive (Note 5)	T_A = +125°C					4.8	6.4	mA
—Negative (Note 5)						3.2	4.4	

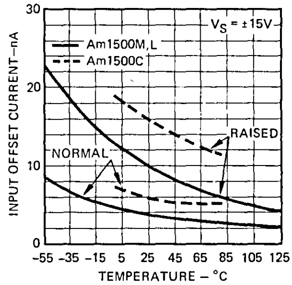
Notes:
1. For the Flat Package derate at 6.5mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = +15V, V^- = −15V, V_E = −15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5.0mV overdrive.
5. The Am1500 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

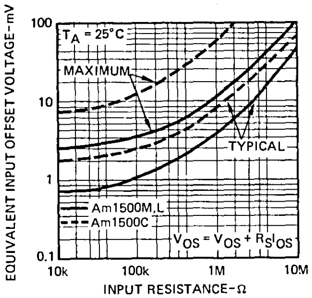
Input Bias Current



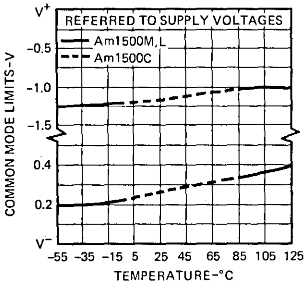
Input Offset Current



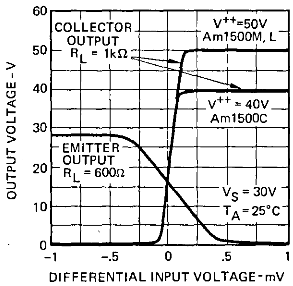
Offset Error



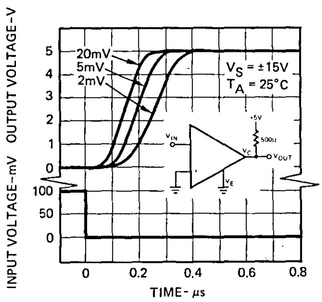
Common Mode Limits



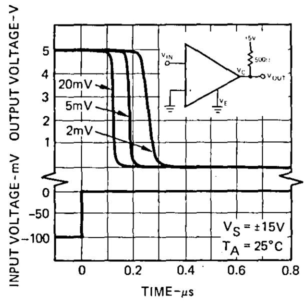
Transfer Function



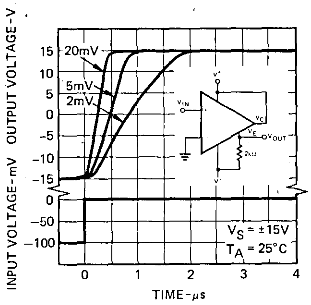
Response Time For Various Input Overdrives



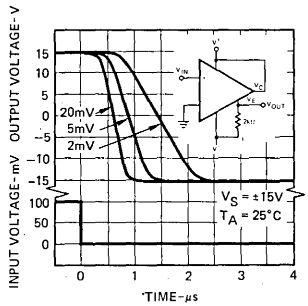
Response Time For Various Input Overdrives



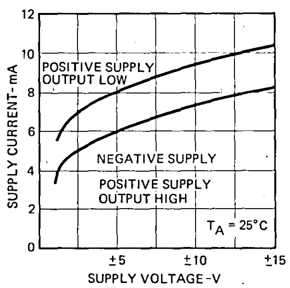
Response Time For Various Input Overdrives



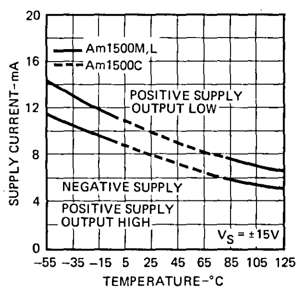
Response Time For Various Input Overdrives



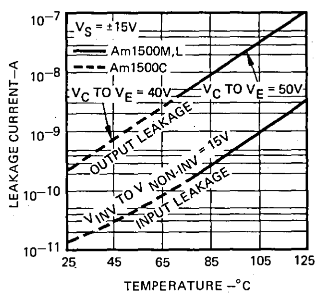
Supply Current



Supply Current

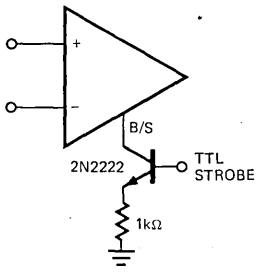


Leakage Current

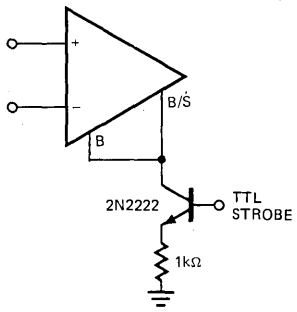


APPLICATIONS

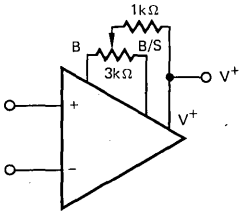
Strobing



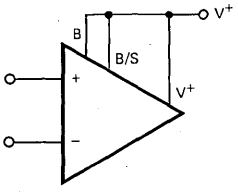
Strobing Off Both Input and Output Stages**



Offset Balancing



Increasing Input Stage Current*



*Increases input bias current and common-mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs storbed OFF.

LH2111/2211/2311

Dual Precision Voltage Comparator

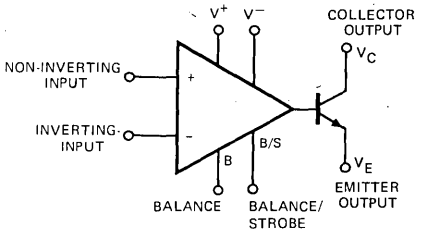
Distinctive Characteristics

- The LH2111/2211/2311 are functionally, electrically, and pin-for-pin equivalent to the National LH2111/2211/2311
- The LH2111 is a dual 111, but requires 25% less power than two 111 comparators
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in Hermetic Dual-In-Line or Hermetic Flat Packages

FUNCTIONAL DESCRIPTION

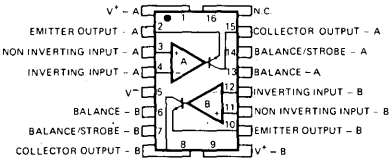
The LH2111/2211/2311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

FUNCTIONAL DIAGRAM
(Each Half)

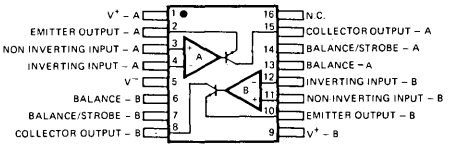


CONNECTION DIAGRAMS
Top Views

Dual-In-Line



Flat Package



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2311	DIP	0°C - +70°C	LH2311D
	Flat Pak	0°C - +70°C	LH2311F
LH2211	DIP	–25°C - +85°C	LH2211D
	Flat Pak	–25°C - +85°C	LH2211F
LH2111	DIP	–55°C - +125°C	LH2111D
	Flat Pak	–55°C - +125°C	LH2111F

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
LH2111/LH2211	50V
LH2311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, –0V
Voltage from Inputs to V^+	–30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LH2111	–55°C to +125°C
LH2211	–25°C to +85°C
LH2311	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

2

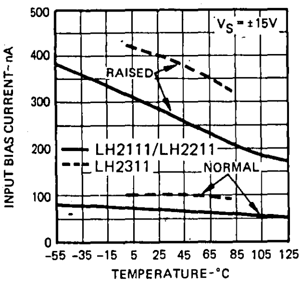
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	LH2311 Min.	LH2311 Typ.	LH2311 Max.	LH2111 LH2211 Min.	LH2111 LH2211 Typ.	LH2111 LH2211 Max.	Units
Input Offset Voltage (Note 3)			2	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current—Positive (Note 5)			3.9	7.5		7.0	9.5	mA
—Negative (Note 5)			2.6	5.0		4.8	7.5	
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{IN} \leq -5mV$, I_C = 50mA					0.75	1.5	V
	$V_{IN} \leq -10mV$, I_C = 50mA		0.75	1.5				
Output Leakage Current	$V_{IN} \geq +5mV$, V_C to V_E = 50V					0.2	10.0	nA
	$V_{IN} \geq +10mV$, V_C to V_E = 40V		0.2	50.0				
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{IN} \leq -6mV$, I_C = 8mA					0.23	0.40	V
	$V_{IN} \leq -10mV$, I_C = 8mA		0.23	0.40				
Output Leakage Current	$V_{IN} \geq +6mV$, V_C to V_E = 50V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current—Positive (Note 5)	T_A = 125°C					4.8	6.4	mA
—Negative (Note 5)						3.2	4.4	

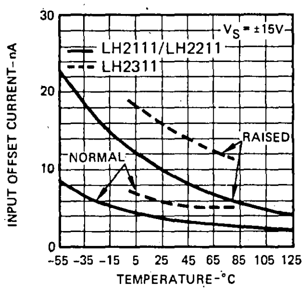
Notes:
1. For the Flat Package derate at 6.5 mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9 mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = 15V, V^- = –15V, V_E = –15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.
5. The LH2111 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

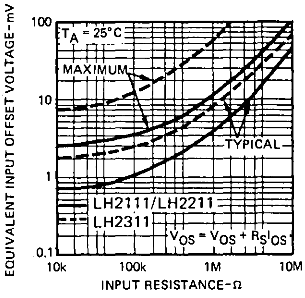
Input Bias Current



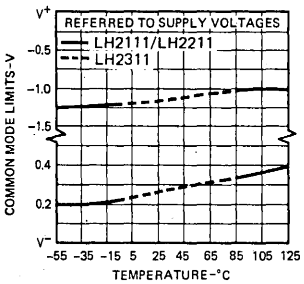
Input Offset Current



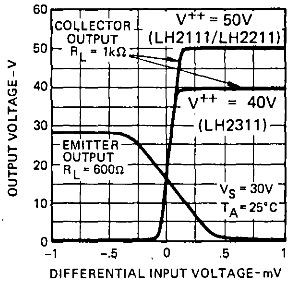
Offset Error



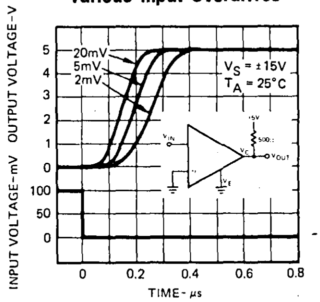
Common Mode Limits



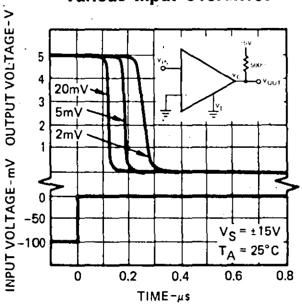
Transfer Function



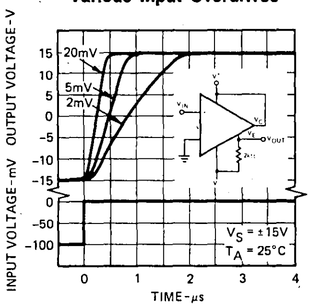
Response Time For Various Input Overdrives



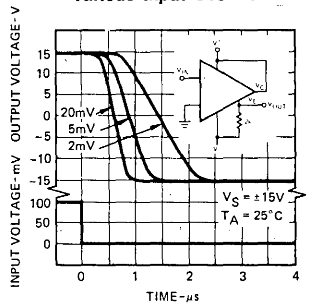
Response Time For Various Input Overdrives



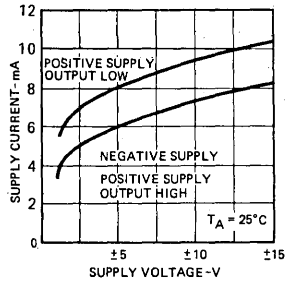
Response Time For Various Input Overdrives



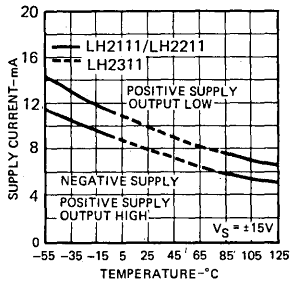
Response Time For Various Input Overdrives



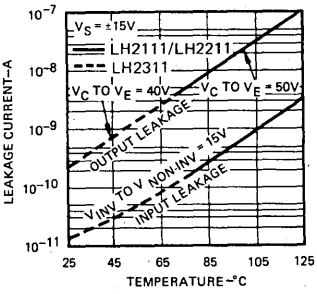
Supply Current



Supply Current

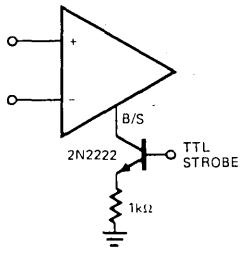


Leakage Current

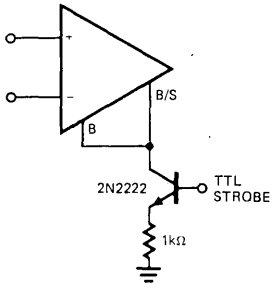


APPLICATIONS

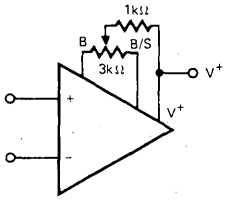
Strobing



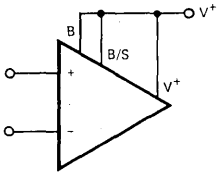
Strobing Off Both Input and Output Stages**



Offset Balancing



Increasing Input Stage Current*



*Increases input bias current and common-mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

A NEW HIGH-SPEED COMPARATOR THE Am685

By Jim Giles and Alan Seales

INTRODUCTION

Modern electronic systems require more and more that operations be performed in a few nanoseconds so that the delay of the complete system, which may be very complex, be held to a minimum. There are abundant logic circuit elements available that meet this criterion: gold-doped TTL, Schottky TTL, and emitter-coupled logic (ECL), listed in descending order of propagation delay. Where it is necessary to interface from the analog world to the input of a logic system, or to detect very low-level logic signals in the presence of heavy noise, a high-speed precision comparator is needed. If such a comparator had a propagation delay less than 10ns, it could replace costly and complex circuitry that designers are now forced to use in very high-speed analog-to-digital converters, data acquisition systems, and optical isolators, as well as make possible many applications hitherto considered unfeasible. It could also be used as a sensitive line receiver or sense amplifier, in 100MHz sample and hold circuits, and in very high-frequency voltage-controlled oscillators.

The basic requirements for a high-speed precision comparator are few and well-defined: good resolution (high gain), high common-mode and differential voltage ranges, outputs compatible with standard logic levels, and, above all, very fast response to signal levels ranging from a few millivolts to several volts. The industry workhorse, the 710, has come close to meeting these requirements, and except for the most demanding applications, its 40ns propagation delay is adequate. A survey of presently available monolithic IC comparators (Table I) shows that there is really none that meets the requirements of very high-speed systems. The newer TTL-output circuits offer only marginal improvement over the 710 when measured under identical conditions of large input pulse and small overdrive, and the ECL-output comparator, although faster, has such poor resolution that it can be used only for large input signals. Advanced Micro Devices felt there was a need for a family of linear devices to fill the needs of very high-speed systems, with the first circuit being a precision comparator with less than 10ns delay.

Type No.	Logic Family	Propagation Delay	Resolution
Am111	TTL	200ns	0.012mV
μA710	TTL	40ns	1.4mV
Am106	TTL	40ns	0.06mV
μA760	TTL	25ns	0.5mV
NE527/529	TTL	25ns	0.5mV
MC1650	ECL	12ns	30mV

Table I: Propagation Delays of Available Monolithic IC Comparators (100mV Input Step, 5mV Overdrive)

DESIGN OBJECTIVES

In order to achieve the ultimate in speed, it is clear that the comparator outputs must be compatible with ECL, even though at present the majority of systems use TTL. Designers striving for the highest possible speed will already be using ECL in the critical circuit areas of their systems to squeeze the last possible nanosecond out of the overall delay. Further, an ECL circuit requires only one-third the gain of an equivalent TTL circuit for the same resolution owing to its smaller output logic swing. This means that lower impedances can be used and consequently larger bandwidth realized for the same power dissipation. Also, there is no problem interfacing the linear input stages with the digital output gate since an ECL gate is basically a non-saturating overdriven differential amplifier. Properly driving a TTL gate from a linear amplifier is more difficult, however, because it requires a large voltage swing suitably biased to track the input logic threshold with temperature, plus a large peak negative current capability to turn off the gate with minimum delay.

The usefulness and versatility of a comparator can be enhanced by adding a strobe or latch function to the circuit. A strobe simply forces the output of the comparator to one fixed state, independent of input signal conditions, whereas a latch locks the output in the logical state it was in at the instant the latch was enabled. The latch can thus perform a sample and hold function, allowing short input signals to be detected and held for further processing. If the latch is designed to operate directly upon the input stage—so the signal does not suffer any additional delays through the comparator—signals only a few nanoseconds wide can be acquired and held. A latch, therefore, provides a more useful function than a strobe for very high-speed processing.

The most difficult input signal for a comparator to respond to is a large amplitude pulse that just barely exceeds the input threshold. This forces the input stage of the comparator to swing from a full off (or on) state to a point somewhere near the center of its linear range. This exercises both the large-and small-signal responses of the stage. If the comparator has less than 10ns delay under these stringent conditions, then it should be as fast or faster for any other circumstances (see Figure 1). The industry standard measurement is with a

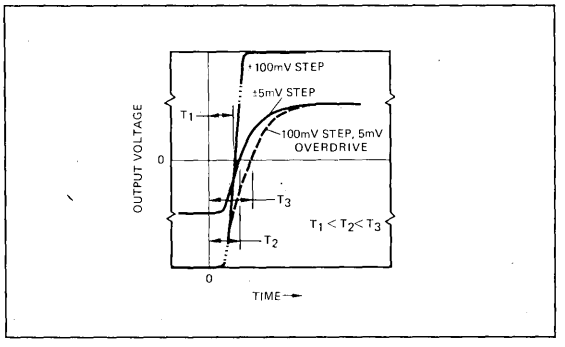


Figure 1. Response to step input signals at output of a differential amplifier

100mV input pulse and an overdrive 5mV above input threshold (this was used for the delays given in Table 1). Pulses larger than 100mV might be used, but this would multiply measurement difficulties, since only a few tenths of a percent aberration or ripple in the pulse generator waveform would be enough to seriously affect the accuracy of the small overdrive, and thus would give misleading results for the propagation delay.

To obtain satisfactory speed for all input signals and particularly for the worst case measurement conditions, the input stage of the comparator must have: 1) wide small-signal bandwidth, 2) high slew rate for large signals, 3) minimum voltage swings, and 4) high gain. The first requirement can be realized by using low-value load resistors, by making every effort in circuit design, device geometry and processing to minimize parasitic capacitances, and by using transistors with the highest f_T possible. The second item calls for high operating currents as well as minimum capacitance. The last two requirements are conflicting, since obtaining high gain normally requires a large voltage swing; therefore some means of clamping the swing must be used that does not degrade the propagation delay.

The overall gain of the complete comparator must also be high because, as illustrated in Figure 1, the propagation delay is less if each stage is well overdriven. To ensure that most of the input overdrive signal is actually used for overdriving, and not consumed in just moving the output from one state to the other, the gain error should be no more than about 10% of the input overdrive. Therefore, for a 5mV overdrive and an ECL output swing of 800mV, the minimum gain must be 1600. It is not practical to strive for much higher gain than this because the small-signal rise time begins to suffer as the stage gain increases. Addition of another stage is undesirable as this also adds delay and increases circuit complexity. It must be remembered that there is a maximum limit on power dissipation that a single integrated circuit package can handle adequately, and this consideration must influence the choice of operating currents and impedance levels throughout the design of the circuit.

With a figure for the total gain required, it is now possible to determine the number of stages and the gain per stage. Since the output stage must be ECL-compatible, its design is fixed, giving a differential-input to single-ended-output gain of about 6. This leaves a differential gain of 270 to be provided by the remainder of the comparator. This is most efficiently divided between two stages, each with a gain somewhat over 16. Both stages should be identical, since minimum overall delay time is obtained when identical stages are cascaded.

A factor not yet discussed that affects the accuracy of the comparator is its input offset voltage. Unless this is trimmed out initially, it must be added to the overdrive in determining the worse-case value of input signal for which the propagation delay specifications will be met. Even with trimming, the temperature drift of high-offset units is typically much greater than that of low-offset units. Therefore, it is desirable to have low initial offset so that trimming is not necessary, and so that the offset temperature coefficient will be good. Also affecting the offset voltage and its drift at higher source resistances are the input currents. To keep this contribution to the total offset low requires high current gains in the input transistors. Therefore, obtaining offsets in the 1–2mV range requires close attention to circuit design, mask layout, and very tight process control (equivalent to that needed for the high-performance, low-frequency operational amplifiers), but with the added kicker of f_Ts well above 1GHz.

As was mentioned, large common-mode and differential voltage ranges are desirable features of a comparator. The limits of the common-mode range in a well-designed circuit should be close to the supply voltages. Since a high-speed comparator will, of necessity, operate at fairly high current levels, the supply voltages must be low to stay within the package power dissipation limits. As a minimum, the common-mode range should be equal to or exceed the differential voltage range to take full advantage of the voltage breakdown characteristics of the input transistors. The basic differential amplifier input stage has a differential voltage breakdown in the range of 5 to 6 volts; the design goal for the common mode range should thus be at least ±3 volts.

In summary, the design objectives for a high-speed precision comparator are as follows:

1) propagation delay <10ns measured at 100mV input step, 5 mV overdrive
2) ECL-compatible outputs
3) latch capability
4) gain >1600
5) input offset voltage <±2mV
6) common -mode range >±3V

CIRCUIT DESIGN

The watchword in designing wideband circuits is simplicity – have the fewest possible active devices in the signal path, the lowest possible impedance levels, and the lowest possible capacitance. The simple, common-emitter differential amplifier can be designed to approach these ideals with one major exception: the deleterious shunting effect of the collector-to-base capacitance upon the driving source resistance is multiplied by the voltage gain of the stage (Miller effect). Even though the impedance levels will be only a few hundred ohms at most, this condition cannot be tolerated if maximum speed is to be achieved. The solution is to add an additional pair of common-base transistors to form a differential cascode amplifier (Figure 2). This circuit has all of the performance features of a common-emitter amplifier and no feedback capacitance.

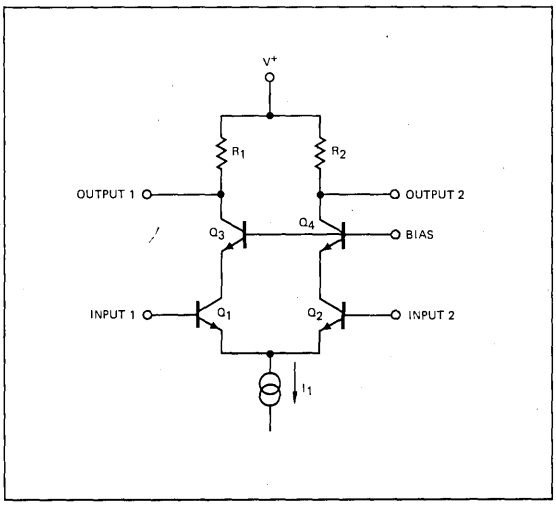


Figure 2. Differential cascode amplifier

Further advantages of the cascode will become apparent later when the latch design is discussed. The only drawback is that there are more devices in the signal path, the positive common-mode range is reduced, and circuitry has to be provided to bias the cascode transistors.

It is now necessary to provide a means of shifting the signal at the output of the cascode (which is very near the positive supply voltage) down to a lower voltage to drive the inputs of the second stage. The use of PNPs is definitely out because of their poor frequency response. This leaves three possibilities: a chain of forward-biased diodes, a programmed voltage drop across a resistor, or a zener diode. The diode chain is useful for level shifts of only a few volts at most, above that, the number of diodes gets too large, with a consequent increase in shunt capacitance and temperature coefficient. The use of a current-source/resistor combination is in the wrong direction for keeping impedance levels low. The resistors could be bypassed with capacitors, but this would offer only marginal improvement, since integrated capacitors have a large shunt component to the substrate. Besides, the addition of four capacitors (for both stages) would result in a large increase in chip area.

The zener diode is definitely superior for high-frequency applications because its shunt capacitance to ground is low, being equal to the collector-to-base capacitance of a transistor. It has no capacitance to the substrate, and its dynamic resistance is quite low. It does have the disadvantage that the level shift is limited to one voltage (6V), which restricts the range of power supply variation the circuit can tolerate. In addition it requires very tight control of the manufacturing process to maintain the matching required. For an input stage gain of 16 the zener voltages have to be matched to better than 0.25% to produce less than 1mV offset voltage at the input.

As shown in Figure 3, the zeners are buffered from the cascode collectors by emitter followers. The pulldown current through the zener-follower combination must be made large enough to discharge the node capacitance when the follower swings in the negative direction. The minimum value necessary is determined by the node capacitance, the signal swing, and the amount of delay that can be tolerated. The amount of signal swing can be reduced by adding clamping diodes across the collectors of the cascode. Regular diode-connected transistors could be used, but would add considerable collector-to-substrate capacitance across the load resistors as well as base-to-emitter capacitance between them. Schottky diodes, on the other hand, require little additional chip area, and are very fast. With clamping, some of the common-mode range lost when the cascode was added can be regained because the cascode transistors can be biased closer to the positive supply without fear of going into saturation at the extremes of the signal swing. The use of Schottky diodes, however, puts a few more gray hairs on the head of the process engineer since he has to control another set of characteristics without affecting the other parameters. The circuit values given in Figure 3 are designed for a minimum differential gain of 16, and a minimum negative-going slew rate at the output of the level-shifter of 1000V/μs.

As mentioned earlier the design of the output stage (Figure 4) can vary little from that of a standard ECL gate. The output emitter followers have to be large enough to handle loading by a 50Ω transmission line (25mA), yet small enough not to add a lot of capacitance that would slow down the response. Therefore, the transistor design must be as efficient as possible with regard to physical size and current-carrying

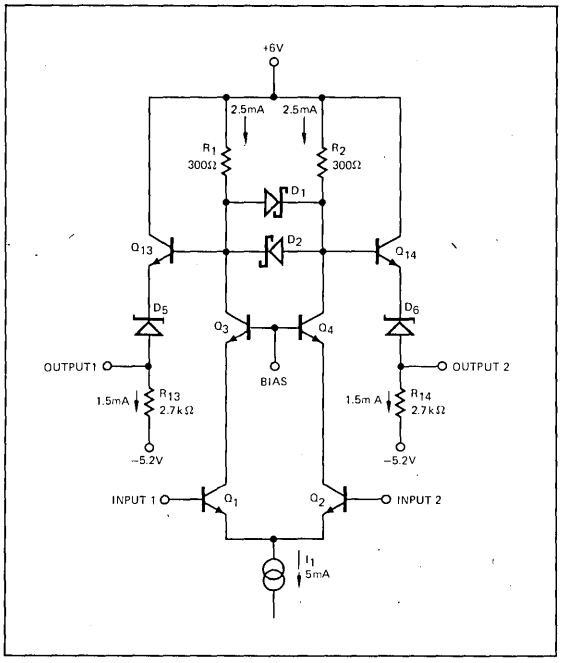


Figure 3. Basic cascode gain stage

capacity. Since the input common-mode level to the gate varies with changes in the power supplies and resistor tolerance, a current source is used to supply the emitters of the gate, rather than the usual resistor to the negative supply. The design of this current source must be such as to provide the correct logical "1" and "0" levels at the output and the proper variation with temperature and power supply changes. The propagation delays to either output of this gate will be equal, whereas they are slightly different in a standard ECL gate owing to the additional capacitive loading on the $\overline{Q}$ output caused by the multiple input transistors.

Implementation of the latch function must be accomplished without interfering with the normal comparator operation or degrading the speed in any way. It must be as close to the input as possible to permit short input signals to be acquired and held. One simple method of adding a latch to a differential

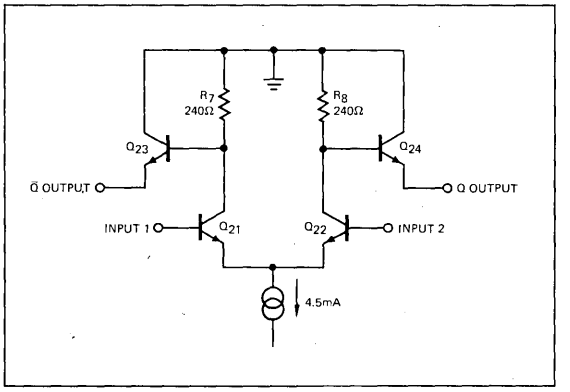


Figure 4. Output gate

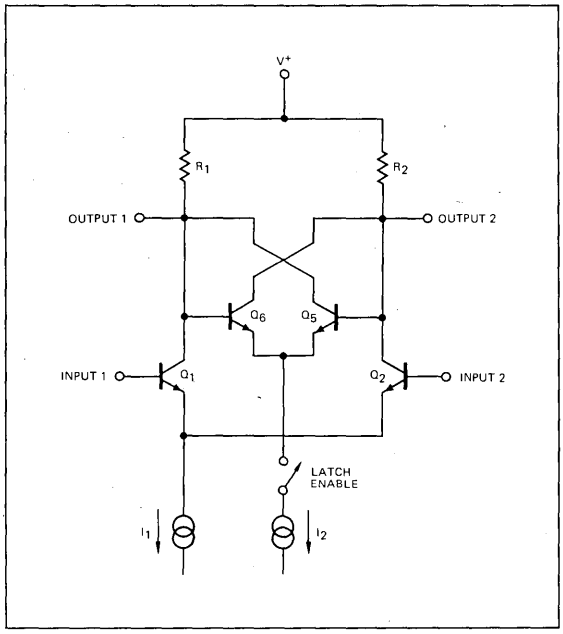


Figure 5. Simple latch circuit

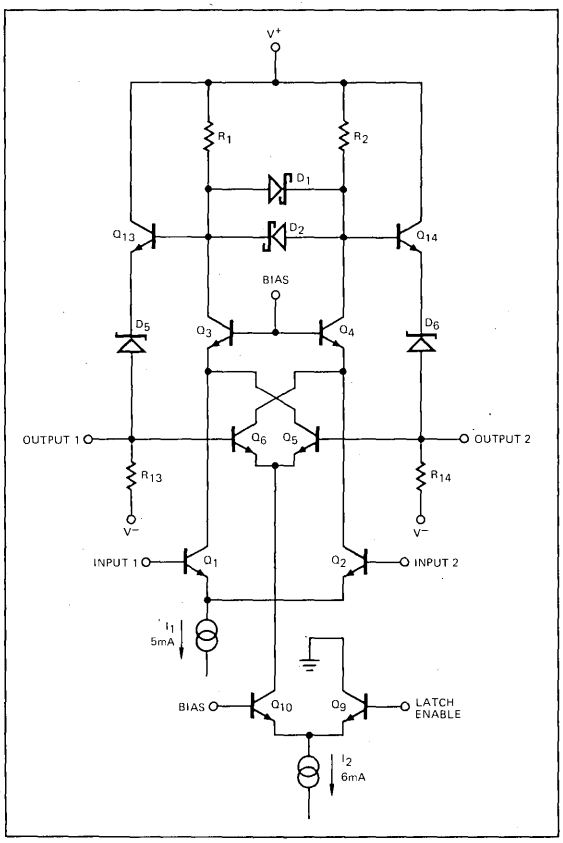


Figure 6. Cascode with latch

amplifier is shown in Figure 5. A pair of transistors, Q_5 and Q_6, are cross-coupled at the collectors of the input transistors, Q_1 and Q_2. The current source I_2 is switched on when it is desired to enable the latch. If I_2 is greater than I_1, the positive feedback via Q_5 and Q_6 will hold the circuit in whatever state it was in when the latch was turned on.

The simple circuit of Figure 5 is not the best for speed because of the added capacitance of Q_5 and Q_6 and the fact that they can saturate unless the signal swings are very small. However, it can be adapted to the cascode stage quite nicely as illustrated in Figure 6. Drive for the positive feedback transistors is taken from the level shifters, and the collectors go to the emitters of the cascode. With this arrangement there is no significant capacitive loading on the gain stage at all. The current source is switched by another differential amplifier, Q_9–Q_{10}, referenced to the ECL logic threshold voltage. This provides the correct input levels for the Latch Enable being driven from a standard ECL gate as well as being very fast, since only currents are being switched.

The latch current source (I_2) must be about 1mA greater than the input current source (I_1) to ensure positive latching for any condition of input signal. Thus, for 5mA in the input stage, at least 6mA must be used to power the latch. This amounts to a lot of power consumed for a function that some users may never even need. However, there is a way to cut the latch standby power down to zero; this is accomplished by the addition of Q_7 and Q_8, as shown in Figure 8.

To understand the function of these transistors, first refer to Figure 7. The differential voltage appearing across the emitters of the cascode transistors is equal to the input signal (for small input signals). This is because the currents through the lower pair of transistors in the cascode are equal to the corresponding currents through the upper pair, and the transistors are matched; therefore the differences in base-emitter voltages must be equal. Thus, Q_7 and Q_8 function as if they were

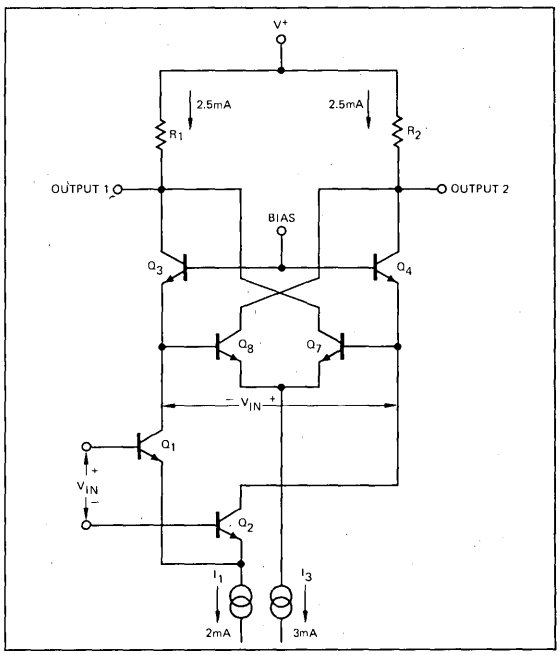


Figure 7. Cascode with "parallel" transistors

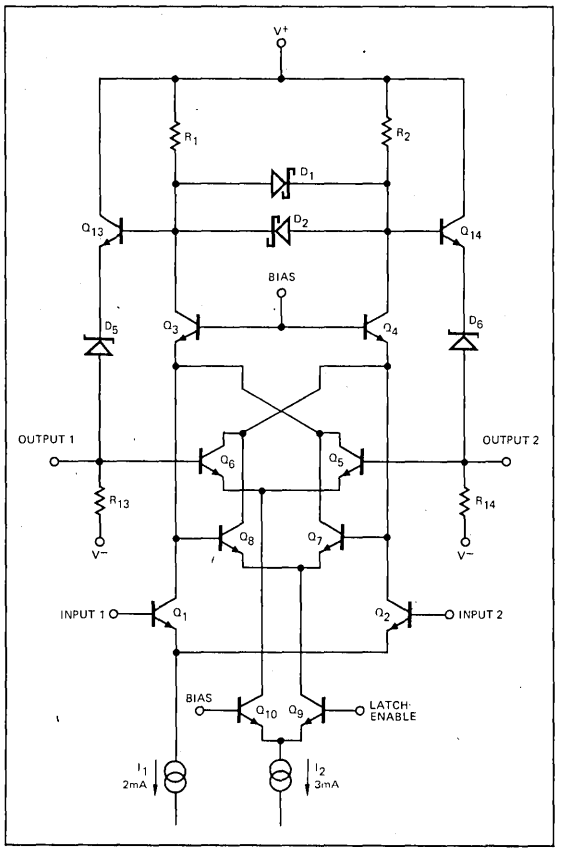


Figure 8. Complete input cascode stage with latch

simply connected in parallel with Q_1 and Q_2, as far as the net effect at the collector load resistors is concerned. To obtain the desired total stage gain, the current I_1 can be 2mA and I_3 can be 3mA.

Now refer to Figure 8. With the latch enable HIGH, Q_9 will be switched on and the 3mA current source will be supplied to the parallel transistors, Q_7–Q_8. The comparator functions normally, and no current is used up in the latch. When the latch enable goes LOW, I_2 will be switched through Q_{10} to the positive feedback transistors, robbing 3mA from the gain stage and giving it to the latch. The latch current is now 1mA greater than the input stage current, but the total current required is still only 5mA. As with the latch transistors, the collectors of the parallel transistors are connected to the emitters of the cascode, so no additional capacitance is added across the load resistors. This places the requirement on Q_7 and Q_8 that they maintain their high f_T at zero collector-to-base voltage.

The use of the parallel transistors has the added bonus that the input bias currents are decreased by more than a factor of two, thus reducing their influence on the offset voltage. The penalty paid is that all three pairs of junctions (Q_1–Q_2, Q_3–Q_4 and Q_7–Q_8) add equally to the input offset. Once again, the processing must be carefully controlled to keep the overall offset within the 2mV goal.

The complete circuit of the comparator is given in Figure 9. It includes some additional refinements as well as the DC biasing. The drive for the latching transistors is taken from the emitters of the second cascode rather than from the level-shifting zeners. This removes their input capacitance from the level shifter and also ensures that Q_{10} cannot saturate. A resistor (R_9) is included to center the common-mode voltage at the input to the gate within its dynamic range; this prevents saturation of the gate or its current source over the expected range of signal swing, temperature drift and supply voltage variations. A separate ground is used for the output emitter followers so that heavy loading at the output will not couple back into the remainder of the circuit. The DC bias chain for the current sources is referenced to ground and the negative supply, so the output logic levels will track those of other ECL circuits connected to the same negative supply. The current sources are designed to stay constant with temperature, which keeps the open-loop gain high at elevated temperatures (>1000 at +125°C), and thus helps to maintain good propagation delay.

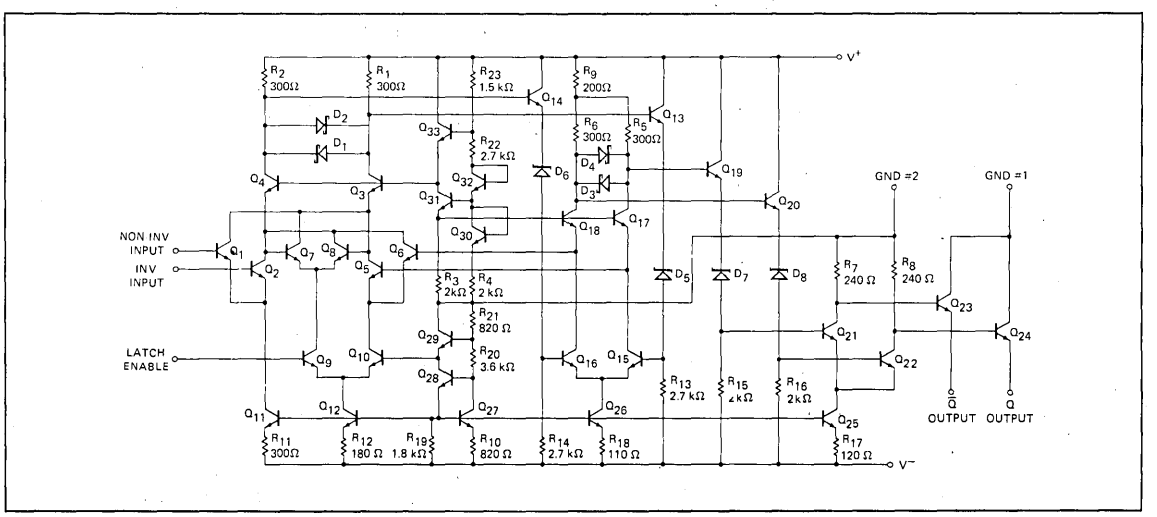


Figure 9. Complete schematic of the Am685 comparator

PROCESS TECHNOLOGY

Circuit design requirements for high speed and a latch function result in an input structure that has three pairs of transistors, the matching of which determines the offset voltage. This dictates that the matching of V_{BE} shall be extremely good between the transistors in each pair in order to meet the 2mV maximum offset voltage target. For the speeds necessary the transistor f_T has to be in the region above 1 GHz, so high-frequency performance can not be compromised. The slew rate of the input stage has to be very high for acceptable response with large input signals. This is achieved by high operating current and low stray capacitances. It is very desirable to keep both the input bias current and the input offset current very low so that the impedances in the source voltages do not introduce intolerable input voltage errors. It would be possible to use a Darlington-connected input stage to achieve these low currents, but the penalty exacted in offset voltage, offset voltage drift, and propagation delay is unacceptable, so high current-gain transistors that match extremely well are needed. The problems are thus centered on achieving very well-matched transistors with high beta and high f_T.

As previously mentioned, it is desirable in a comparator to have a wide common-mode voltage range and high power-supply rejection ratio. This is facilitated by using Schottky diodes to clamp the collector-to-collector swings in the first two stages. Schottky diodes can be fabricated simply by making a window in the oxide over the N-type epitaxial layer and using the same evaporated aluminum as is used for the interconnects (see Figure 10). The contact potential between silicon and aluminum causes a potential barrier to the flow of electrons. Making the metal positive lowers this barrier, allowing electrons to pass over it by virtue of their thermal energy. This process is essentially the same as thermionic emission. Since these electrons are majority carriers, Schottky diodes show extremely fast turn-off characteristics, desirable in this application. Why the Schottky diode is so attractive is that the forward voltage necessary to produce a given current may be several hundred millivolts less than that required to produce the same current in a p-n junction diode of about the same size. It can thus be used as a "clamp" to prevent a bipolar transistor from saturating, when connected from collector to base so as to prevent the forward voltage of the collector-base diode from rising to a level sufficient to cause appreciable current flow in the collector-base diode. This is the common application in Schottky TTL circuits.

In the ECL comparator the use is different. Here they are used back-to-back to limit the differential voltage swings between the collectors in both the first and the second stages. Connected in this way the reverse voltage seen by one Schottky diode is equal to the forward voltage drop of the other diode. Because this voltage is so small reverse leakage is not a great problem. In the simple Schottky diode structure, as described above, the reverse leakage is high. Most of this leakage current is generated at the perimeter of the metal, where there is an electric field concentration. In order to reduce this field the metal is extended all around the opening in the oxide, overlaying this oxide. Spacing the metal from the silicon in this way reduces the field and hence the leakage. In applications where low leakage is critical, the use of a P+ guard ring is called for, but this carries with it extra capacitance, so in view of the fact that the reverse voltage is so low the guard ring technique was discarded for this application. Even so, the diodes used in the comparator have low leakage characteristics with a breakdown at about 45V.

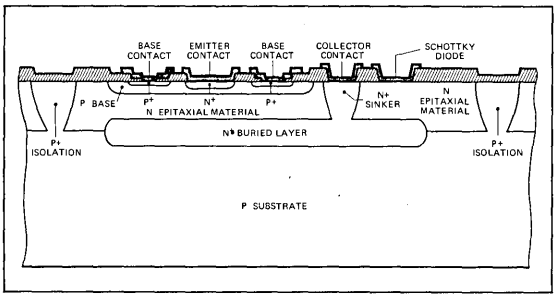


Figure 10. Cross section of transistor and Schottky diode showing sinker and P+ base contact enhancement

At the very high speeds being considered, much effort has to go into reducing capacitances and resistances. Thinning down the epitaxial layer to the minimum required to sustain the voltages encountered is of benefit in two ways: 1) the collector-isolation sidewall area is reduced, lowering the collector-to-substrate capacitance; 2) the collector-series resistance is reduced. The two major contributions to collector-series resistance are the resistance of the epitaxial material between the emitter and the buried N+ layer, and the resistance of the epitaxial layer between the collector contact and the buried layer. However, the first resistance is subject to reduction by conductivity modulation during operation of the device and thus is less important than the second term. The second term can be made very small by using a "sinker", which is a high concentration N-type diffusion from the surface, through the epitaxial layer, to the buried N+ layer. Contact to the collector is then made to the surface of the sinker. (see Figure 10)

Collector-to-base capacitance is held low by using very small dimensions and by using a relatively high epitaxial layer resistivity. The latter also serves to reduce the collector-to-substrate capacitance. A further reduction in collector-to-base capacitance results from using a shallow, high sheet-resistivity diffusion for the base. However, this raises the base resistance, both because the bulk resistance from the contact to the active base region is increased and because the specific contact resistance is increased. These resistances may be reduced by depositing P+ regions under the base contact areas after the main base diffusion.

A compromise has to be made in selecting emitter width. Large emitters are desirable for V_{BE} matching, but very small emitters are essential for high f_T. A stripe emitter, .25-mil wide and 1-mil long, was chosen as optimum. A difference in width, between two otherwise identical emitters, of .01-mil will be sufficient to cause an offset voltage of 1 mV. From this, it can be seen that the photolithography must be extremely carefully controlled, since the offset voltages of three pairs of transistors are summed to give the total offset of the comparator. Because the emitters are so narrow the normal procedure of making a contact cut inside of the emitter cannot be used. Instead, the emitter oxide is simply dissolved in hydrofluoric acid immediately before the aluminum evaporation in order to expose the emitter. As a consequence, the lateral distance between the metal and the emitter-base junction is very small, being equal to the lateral diffusion of the emitter. This means that the sintering process must be carried out at a temperature lower than is customary in linear circuit manufacture in order to avoid short-circuiting the

emitter-base junction by lateral migration of aluminum. An additional reason for lowering the sintering temperature is to avoid penetration of aluminum down through the emitter and base, causing emitter-to-collector shorts.

The requirement for high current gain, for low input bias currents, necessitates narrow base widths. Emitter-to-collector shorts can be a problem in these shallow, narrow-base structures. The probability of shorting can be minimized by careful cleaning procedures and by proper emitter doping levels. Keeping the emitter doping level low also reduces the magnitude of the "emitter dip" effect, whereby the diffusion coefficient of the boron in the region under the emitter is greatly increased by the lattice strain caused by the emitter, resulting in the running-on of the base under the emitter, making it very difficult to achieve a narrow base width.

An area that is neglected in digital circuit processing, because high beta is not necessary, but which is of major importance in linear processing, is the control of surface conditions. If high current gains are to be realized, both the surface area of the emitter-base-depletion region and the surface recombination velocity must be minimized. The former implies that ionic contamination, such as sodium ions, must be eliminated and that the surface state charge density, Qss, should be made as low as possible. The surface recombination velocity is proportional to the fast surface state density and so can be minimized by making this density very low. These three goals; low ionic contamination, low Qss and low fast surface state density are achieved by using the well known techniques of MOS and linear circuit processing, such as annealing in an inert atmosphere and proper choice of sintering cycle.

In the interests of minimum capacitance, the metal interconnects are designed to be narrower than is usual in linear circuits. Special etching techniques have to be employed in order to reproduce these narrow lines reliably. These lines can be seen in the photomicrograph of Figure 11.

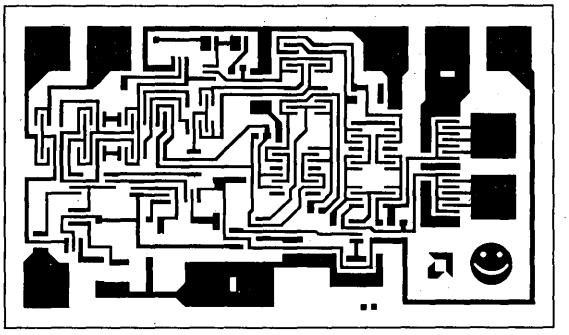


Figure 11. Photomicrograph of the Am685 comparator

PERFORMANCE

The primary design objective for the comparator was to obtain under 10ns propagation delay for large input signals with small overdrive. It should then be as fast or faster for any other input conditions. The performance of the Am685 comparator for a 100mV step input at various overdrives is shown in Figures 12 and 13. The propagation delay is measured from the time the input step crosses the input threshold voltage to the time the output crosses the logic threshold voltage. The input threshold voltage (i.e., the offset voltage) was adjusted for the figures so that the delay can be simply measured by

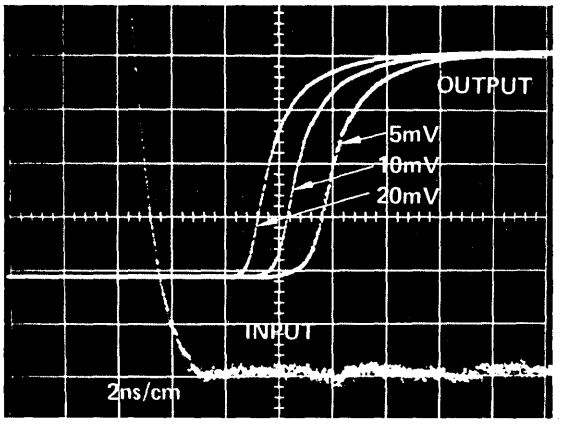


Figure 12. Tpd —"1" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

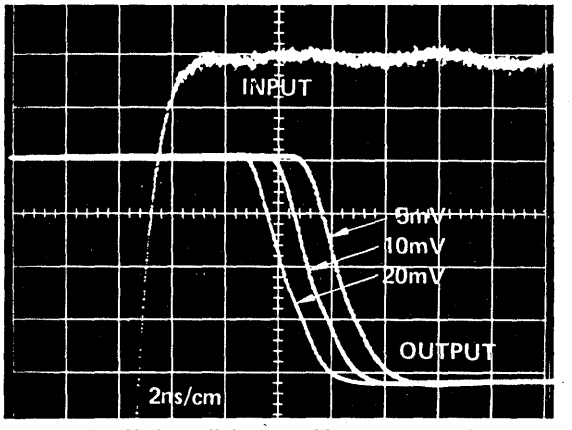


Figure 13. Tpd —"0" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

counting up 5, 10, or 20mV from the bottom of the input pulse. The input pulse, therefore, is displayed on a magnified scale to facilitate this measurement and also to illustrate the purity of input signal required to make accurate measurements at millivolt overdrives.

For a 100mV input step and 5mV overdrive, the propagation delay for a logical "0" is 6.3ns and for a logical "1" is about 300ps less. A graph of delay as a function of overdrive is given in Figure 14. It was previously stated that any other condition

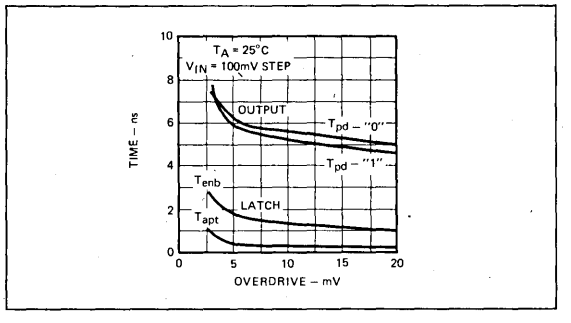


Figure 14. Delay times as a function of input overdrive

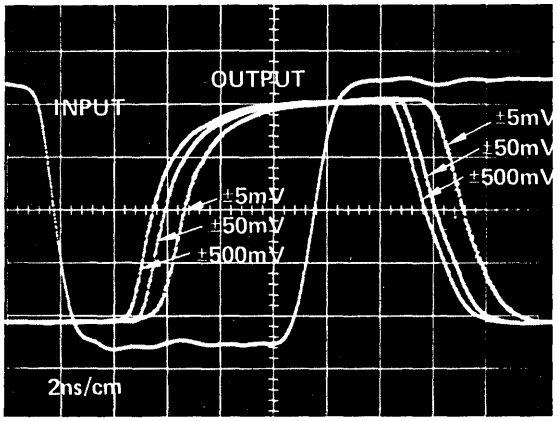


Figure 15. Response to symmetrical input signals

of input signal should give faster response (refer back to Figure 1). This is demonstrated by Figure 15, which illustrates the response of the comparator to symmetrical inputs ranging from ±5mV to ±500mV. The speeds are at least 1 to 2ns faster than for small overdrives.

Figure 16 shows how the delay time varies with temperature. The adverse effects of resistor and gain changes at elevated temperatures result in an increase in delay from 6.3ns at 25°C to 8.4 ns at 85°C and 10.4 ns at 125°C. All of the above data were taken with output loads of 50Ω connected to −2.0V. For lighter loading (such as 500Ω to −5.2V) the output rise and fall times and propagation delays are all slightly faster.

The usefulness of the latch is directly related to how quickly it can be enabled following a change in the input signal. The input signal must be present long enough to pass through the first stage of the comparator before the latching transistors can act upon it. The minimum time that the input must be present before the latch can be turned on is defined as the latch enable time. This is measured as the minimum time that must elapse

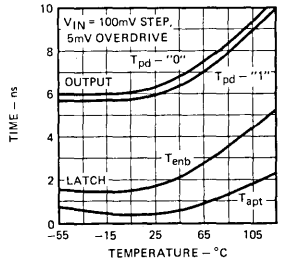


Figure 16. Delay times as a function of temperature

between the time the input step crosses the input threshold voltage and the time the latch enable input crosses the logic threshold voltage for which the comparator outputs will assume the correct states.

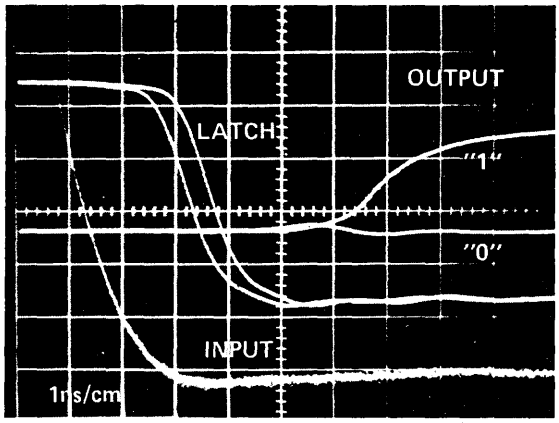


Figure 17. Latch enable time and latch aperature time for 100mV input step, 5mV overdrive (input = 5mV/cm, latch = 200mV/cm, output = 400mV/cm)

The performance of the latch function is illustrated by Figure 17. The input signal is the standard 100mV step with 5mV overdrive and is in the direction to cause the output to switch from a logical "0" to a logical "1". The delay of the latch signal relative to the input is adjusted until the output just switches to a "1"; this is the latch enable time and under these conditions is 1.8 ns. The difference between the latch timing for which the output just barely switches and when it does not switch is the latch aperture time; this is about 500ps for 5mV overdrive. The performance of the latch with input overdrive and temperature generally follows that of the propagation delays (Figure 14 and 16).

The overall performance of the Am685 is summarized in Table II. It is apparent from the table and the previous discussion that the device is ideally suited for applications where both precision and high speed are required, such as in analog-to-digital converters, data acquisition systems, and optical isolators. The device is the first in a family of new wideband linear integrated circuits designed to meet the requirements of very high-speed systems.

Propagation Delay (100mV step, 5mV overdrive)	6.5ns MAX
Input Offset Voltage	2.0mV MAX
Average Temperature Coefficient Of Input Offset Voltage	10μV/°C MAX
Input Offset Current	1.0μA MAX
Input Bias Current	10μA MAX
Common Mode Voltage Range	±3.3V MIN
Common Mode Rejection Ratio	80dB MIN
Supply Voltage Rejection Ratio	70dB MIN
Positive Supply Current	22mA MAX
Negative Supply Current	26mA MAX

Table II: Performance Characteristics of the Am685 Comparator (T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, R_L = 50Ω to −2.0V)

THE A-D APPLICATION

Very fast, precision, analog-to-digital conversion stands to benefit considerably from the availability of a fast comparator. As the block diagram of a fast 10-bit converter in Fig. 18 shows, a typical rapid conversion technique may resemble the use of feedforward compensation in an operational amplifier.

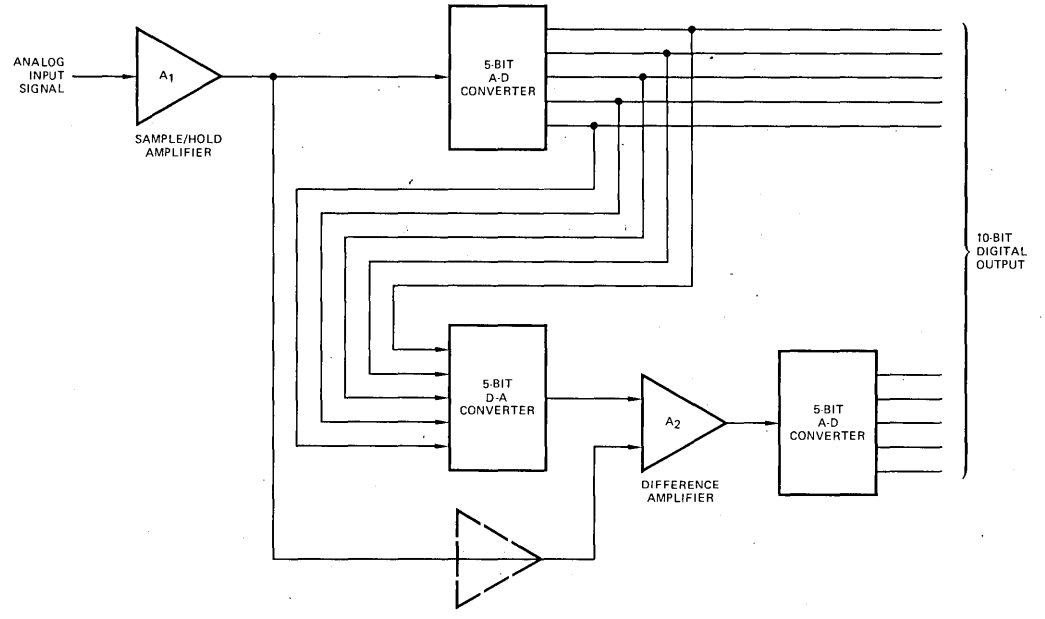
The analog input signal is sampled at the beginning of a conversion period and fed to a fast five-bit a-d converter, which provides the first five most significant bits of the output. These five bits also drive a companion d-a converter, which must be accurate to better than 10 bits. The output of the d-a converter is a replica of the input signal, quantized to five bits. This is compared with the actual input signal stored in the sample-and-hold amplifier. The difference between the two analog levels is the remaining part of the input signal that must be quantized. This difference is amplified and applied to another five-bit a-d converter to provide the five least-significant-bits of the final output.

Typical five-bit a-d converters may consist of 31 106-type comparators connected to the signal source and referenced to the full-scale input in steps of 1/32. The output of each comparator goes into a latch, and the latch outputs are decoded by three stages of TTL gages to develop the five-bit digital output.

Typical propagation delays are 40 ns for the comparators, 22 ns for the latches, and 10 ns for the decoding, resulting in a total delay of 80 ns. Average settling time for the five-bit d-a converter and the difference amplifier together comes to about 200 ns, and the settling time for the input sample-and-hold amplifier is 70 ns. Thus, the over-all conversion time for this 10-bit converter amounts to 430 ns.

Substitution of the high-speed ECL comparator for the 106 type in each of the five-bit converters leads to a significant improvement in propagation delay. The typical delay of the comparator is about 6.5 ns, and no external latch is required. With ECL it is possible to wire-OR outputs, so only one level of decoding gates is required. Allowing 1.5 ns for the gates, the total five-bit conversion time is only 8 ns – a tenfold improvement over the existing circuit.

If the latch function of the comparators is used as the sample-and-hold for the first five-bit converter, the sample-and-hold can be put in parallel with the first quantization step, as shown by the dotted lines in Fig. 18. This eliminates its settling time from the over-all delay of the system. With the new comparator, the total 10-bit conversion time drops to 216 ns, with over 90% of the delay attributable to the d-a converter and the difference amplifier. Moreover, the availability of an 8 ns five-bit converter should provide the impetus to improve the slower sections of the system. A 10-bit a-d converter with a delay under 100 ns is not an extravagant prediction.



If the standard 106-type comparator in this a-d converter is replaced by the 10 ns device, a tenfold improvement in speed is possible. What is more, the ECL makes possible both wired-OR outputs and a single level of decoding for gates.

Figure 18. Analog to digital.

Am685/Am686/Am687 DESIGNING WITH HIGH SPEED COMPARATORS

By Leonard Brown

INTRODUCTION

The Am685, Am686 and Am687 are a family of high-speed sampling comparators capable of detecting low-level signals of the order of 5-10mV in 12-15ns over the temperature range $-55^{\circ}C \leqslant T_A \leqslant 125^{\circ}C$. The Am686 is fully TTL-compatible and complementary outputs are available generated from a true differential output stage assuring a maximum output skew of under 2ns at 25°C. The Am685 and Am687 are single and dual ECL-compatible versions, respectively, and have output skews of less than 1ns. A high-speed latch is incorporated in the input stage permitting input signals to be acquired in 4.0ns maximum for the ECL versions and 6.0ns for the TTL device.

Applications of the devices are not limited to high-speed designs as the combination of the excellent DC input characteristics, availability of true differential outputs and the latch function permit unique solutions for slower speed applications where the response time of the comparators can be considered negligible.

THE SAMPLING COMPARATOR

The sampling comparator may be visualized as a conventional voltage comparator with the provision that the outputs may be latched into the logic states determined by the **input signal conditions existing at the time of application of the latch signal.** This is achieved by incorporating the latch circuitry in the input stage of the device. The minimum latch enable pulse width is necessarily less than the propagation delay of the device and, therefore, the comparator can be unlatched for a fraction of its propagation delay (4.0ns for the Am685). The outputs will then change in accordance with the input conditions existing at the time of the latch signal. Note: It is impossible for the comparator to oscillate under these conditions.

If the latch function is not used, the device operates as a conventional voltage comparator.

BACK TO BASICS

Comparators are designed to have both high gain and large bandwidth. This creates instability problems or oscillations when the device outputs are in the transition region. The tendency of a device to oscillate is a function of the layout, (poor layout increasing the amount of feedback caused by parasitic capacitance) and the source impedance of the circuit employed (The higher the source impedance the less parasitic coupling is necessary to cause oscillation.) It is mandatory with comparators of the gain and bandwidth of the Am685, Am686 and Am687 to ensure that power supplies are well decoupled, lead lengths are kept as short as possible, and wherever possible (especially in the case of the Am686), a ground plane should be employed.

In addition to reducing the effects of stray capacitance, a ground plane substantially reduces the possibility of the output current spike coupling back to the inputs through the ground lead when the TTL output stages switch.

The minimum slew rate at which the input signal must cross the threshold region to prevent oscillation, regardless of the particular layout parasitics, may be determined by applying a DC voltage to the input until the circuit just commences to oscillate and increasing this voltage until the oscillation ceases. The minimum necessary input slew rate is then given by $\Delta V/t_{pd}$ MIN, where ΔV is the input voltage required to prevent oscillation and t_{pd} MIN is the minimum propagation delay of the comparator.

The minimum slew rate will be found to be a function of source impedance and source impedance mismatch.

The curves of Figures 1 and 2 show the minimum slew rate for the Am686 as a function of source impedance and source impedance mismatch.

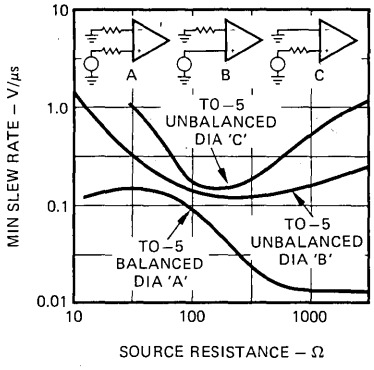


Figure 1. Minimum Slew Rate Versus Source Resistance (TO–5).

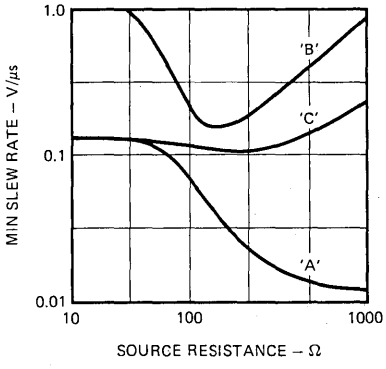


Figure 2. Minimum Slew Rate Versus Source Resistance (DIP).

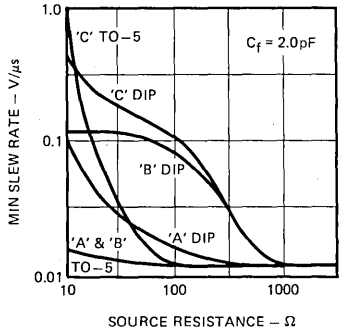


Figure 3. Minimum Slew Rate Versus Source Resistance (TO–5 & DIP).

It can be seen that unbalanced sources dramatically effect the minimum input slew rate required. Note that for optimum performance, the source impedance seen by the comparator should be both DC and AC balanced to reduce the differential feedback to a minimum.

The effect of an AC unbalanced source is seen especially on the Am686 as when the output switches, the output current spike is coupled back to the input. This can be eliminated by forcing the AC unbalance to result in positive feedback, which may be achieved by decoupling the inverting input or applying positive feedback via a 2-4pF capacitor from the Q output to the non-inverting input.

The curves of Figure 3 illustrate the improvement in minimum slew rate when a small amount of positive feedback is employed by virtue of a 2pF feedback capacitor.

OPTIMUM SOURCE CONDITIONS (C_f = 0pF)

With low source impedances (< 50Ω), the majority of the feedback between the output and the input occurs internal to the device. As the source impedance is raised, external feedback increases through the parasitic feedback capacitance until, at high source impedances, the external feedback dominates. This explains the anomolous characteristics of the minimum slew rate curves and suggests that the optimum source resistance for the device is between 300 and 500Ω for unbalanced sources and is approximately 1000Ω for a balanced source.

OPTIMUM SOURCE CONDITIONS (C_f = 2pF)

With a source impedance of 100Ω, the minimum slew rate is 0.15V/μs for the DIP configuration and 0.02V/μs for the TO-5. For balanced sources the minimum slew rate is 0.03V/μs for $R_S \geq 100\Omega$ and for a source impedance between 1kΩ and 3kΩ, the minimum slew rate is <0.02V/μs regardless of impedance, DC imbalance or package type.

The use of the feedback capacitor is recommended when:

1. The input slew rate is within a factor of 2 greater than the minimum theoretical slew rate.
2. System constraints do not permit optimisation of layout and lead lengths.
3. Unbalanced source impedances are used (it is not always possible to provide input conditions which are both DC and AC balanced).

A FAMILY AFFAIR

It must be stressed that the concepts discussed concerning source imbalance and minimum input slew rate apply to all devices in the family. The Am686 was highlighted as it is more sensitive to layout constraints and parasitic feedback because of its significantly higher voltage gain.

Similarly all of the applications which follow may be implemented with any device in the series provided due caution is exercised with regard to the different output logic levels.

THE RELAXATION OSCILLATOR

The principal problems in the design of a classical relaxation oscillator are:

1. The variation in potential to which the energy storage device (normally a capacitor) is charged.
2. The variation in the threshold level at which the capacitor is to be discharged.
3. The variation inherent in the sensor element (normally a comparator) in detecting equivalence between the threshold level and the capacitor's instantaneous potential.

The variations are all functions of both time and temperature and are the primary causes of frequency drift, symmetry error, and jitter.

By taking advantage of two unique properties of the Am686, a relaxation oscillator may be designed to eliminate the first two problems and reduce the third to a second-order effect for oscillation frequencies from 1MHz to 30MHz.

The true differential output stage of the comparator ensures that the Q and $\overline{Q}$ outputs change within 1-2ns of each other. This feature ensures that the outputs can never be in the same logic state instantaneously, either HIGH or LOW, and that the only time they are equal in voltage is when traversing the logic uncertainty levels. This property permits the design of a threshold setting circuit that varies in accordance with the charging voltage applied to the timing capacitor. Therefore, any change in charging potential is automatically compensated by a corresponding change in threshold level.

Second, the combination of the short propagation delay 7-10ns, the minimum difference in propagation delay between outputs and the stability of these delays with temperature assures square wave symmetry of better than 1% @ 1MHz and 5% @ 25MHz and a frequency stability of 1% @ 10MHz and 4% @ 25MHz.

The above statements are true from device to device and over the operating temperature range of –55°C to +125°C. Over the industrial temperature range, a factor of two improvement should be obtained.

CIRCUIT THEORY (Fig. 4)

Assuming the circuit is in an oscillating mode, the voltage appearing at the non-inverting terminal will alternate between V_X and V_Y where:

$$V_X = \frac{R_1}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL} \quad \text{and}$$

$$V_Y = \frac{R_2}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL}$$

When $V_{+IN} = V_X$, the timing capacitor C will be charging towards V_{OH}, and when $V_{+IN} = V_Y$, the timing capacitor will be discharging towards V_{OL}.

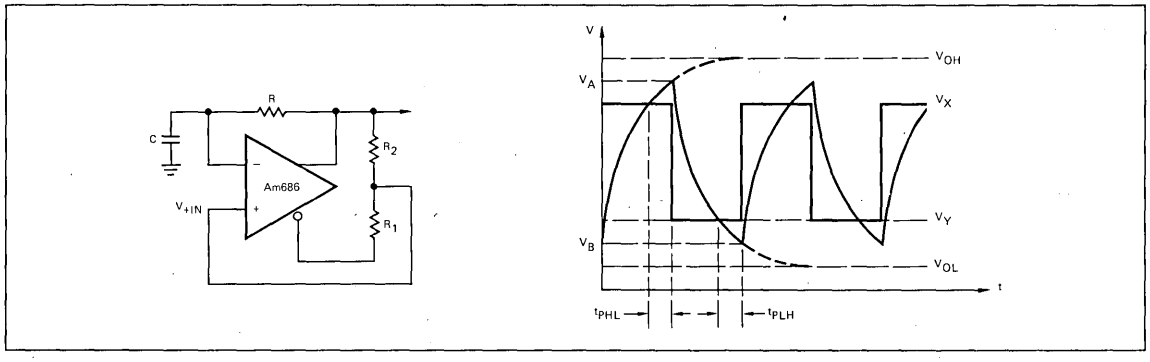


Figure 4. Circuit Design.

After the voltage on the capacitor equals the voltage on the non-inverting input, a finite time will elapse before the output of the circuit changes, during which time (the propagation delay of the Am686) the capacitor will continue to charge towards V_{OH}, or discharge towards V_{OL}.

Therefore, the capacitor will charge to a voltage

$$V_A = V_{OH} - e^{-t_{PHL}/CR} \cdot (V_{OH} - V_X)$$

and discharge to a voltage

$$V_B = V_{OL} + e^{-t_{PLH}/CR} \cdot (V_Y - V_{OL})$$

where t_{PHL} and t_{PLH} = propagation delay of the Am686 from the inputs to the output changing from HIGH – LOW and LOW – HIGH respectively.

The time to charge from V_B to V_A which is the positive half cycle is given by:

$$t^+ = CR\ 1n\ \frac{V_{OH} - V_B}{V_{OH} - V_A}$$

substituting for V_A and V_B

$$t^+ = CR\ 1n\ [(\frac{R_1}{R_2} + 1)\ e^{tPHL/CR} - 1]$$

Similarily the negative half cycle is given by:

$$t^- = CR\ 1n\ \frac{V_A - V_{OL}}{V_B - V_{OL}}$$

$$t^- = CR\ 1n[(\frac{R_1}{R_2} + 1)\ e^{tPLH/CR} - 1]$$

Note: The only assumptions are:

1. $(V_{OH} - V_{OL})$ of the Q output = $(V_{OH} - V_{OL})$ of the $\overline{Q}$ output.
2. Offset voltage and offset current errors are negligible.
3. $e^{t_{PLH}/CR} \times e^{-t_{PHL}/CR} = 1$

The only factor affecting pulse width variation is, therefore, t_{PHL} and t_{PLH}. As $t_{PHL} > t_{PLH}$ by 1-2ns, it is therefore anticipated that t^+ will be marginally greater than t^-.

MINIMUM OPERATING FREQUENCY

For the Am686, it is specified that the minimum slew rate at the input to insure that the device will not oscillate in the transition region is 1V/μs. This will determine the minimum operating frequency of the circuit.

The rate of change of voltage on the timing node is given by:

$$\rho = \frac{\partial v}{\partial t} = \frac{Vo}{CR} \times e^{-t/CR}$$

In the circuit,

a) $Vo = V_{OH} - V_B$ (assuming positive ramp)

and

b) $t = CR\ 1n\ [(\frac{R_1}{R_2} + 1)\ e^{tPHL/CR} - 1]$

As the slew rate is only critical in determining the lowest operating frequency, it may be assumed that $e^{tPHL/CR} = 1$ $(CR >>> t_{PHL})$; therefore, $Vo = V_{OH} - V_B \approx V_{OH} - V_Y$

$$Vo = (V_{OH} - V_{OL})\ \frac{R_1}{R_1 + R_2} \qquad \text{and, } t = CR\ 1n\ \frac{R_1}{R_2}$$

$$\therefore \rho = \frac{\partial v}{\partial t} = \frac{(V_{OH} - V_{OL})}{CR} \times \frac{R_1}{R_1 + R_2} \times \frac{R_2}{R_1}$$

$$= \frac{\Delta V}{CR} \times \frac{R_2}{R_1 + R_2}$$

where, $\Delta V = (V_{OH} - V_{OL})$

The minimum operating frequency

$$f_{MIN} = \frac{1}{2\ CR\ 1n\ \frac{R_1}{R_2}}$$

substituting

$$CR = \frac{\Delta V}{\rho}\ \frac{R_2}{R_1 + R_2} \qquad f_{MIN} = \frac{\rho}{2\Delta V} \times \frac{(R_1/R_2 + 1)}{1n\ R_1/R_2}$$

The expression for minimum frequency indicates that an optimum ratio of R_1/R_2 exists that is independent of any particular RC time constant which may have been chosen.

The ratio may be determined by differentiating f_{MIN} with respect to R_1/R_2.

$$\frac{\partial f_{MIN}}{\partial \frac{R_1}{R_2}} = \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - (\frac{R_1}{R_2} + 1)/\frac{R_1}{R_2})}{(1n\frac{R_1}{R_2})^2}$$

$$= \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1}}{(1n\frac{R_1}{R_2})^2}$$

Setting $\frac{\partial \frac{F}{R_1}}{\partial \frac{R_1}{R_2}} = 0$

$$1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1} = 0$$

$$\frac{R_1}{R_2} = \frac{1}{1n\frac{R_1}{R_2} - 1}$$

$$\therefore \frac{R_1}{R_2} = 3.59112$$

Therefore, the lowest frequency the oscillator will perform consistent with the 1V/μs constraint is:

$$f_{MIN} = \frac{1 \times 4.6}{2 \times 3.5\ 1n\ 3.6} = .513MHz$$

D.C. OFFSET ERRORS

The presence of DC errors resulting from the bias and offset currents and offset voltage of the Am686 will cause the V_Y and V_X thresholds to be both shifted either positive or negative by an equal amount δV where δV is the sum of all such errors.

The magnitude of these effects may be calculated as follows:

When the capacitor is discharging –

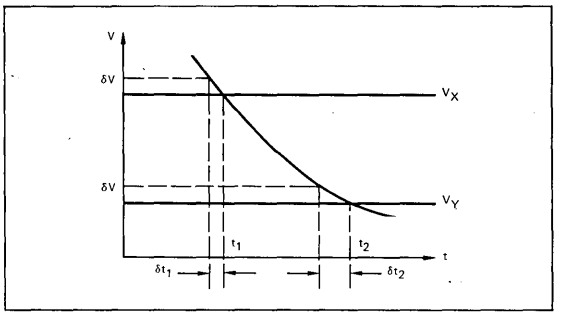


Figure 5.

$$V_{(t)} = V_o e^{-t/CR}$$

$$\frac{dv}{dt} = -\frac{1}{CR} Vo e^{-t/CR} = -\frac{1}{CR} V_{(t)}$$

$$\delta t_1 = -\frac{\delta V}{V_{(t_1)}} CR$$

$$\delta t_2 = \frac{-\delta V CR}{V_{(t_2)}}$$

Δt^- Negative Pulse Width Change =

$$\delta t_2 - \delta t_1 = \delta VCR \frac{V_{(t_2)} - V_{(t_1)}}{V_{(t_1)}\ V_{(t_2)}}$$

As $V_X = V_{t_1}, V_Y = V_{t_2}$

$$\Delta t^- = \frac{\delta VCR\ (V_Y - V_X)}{V_X V_Y}$$

Similarly for the positive pulse

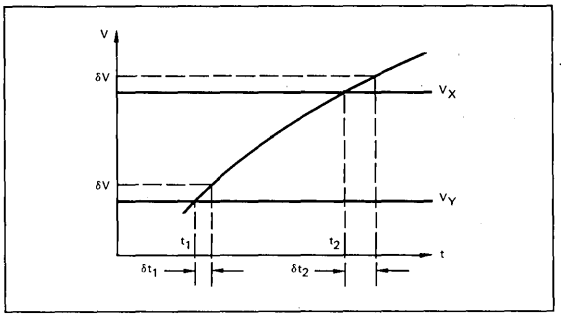


Figure 6.

$$V_{(t)} = Vo\ (1 - e^{-t/CR})$$

Whence, $dv/dt = \frac{1}{CR} (Vo - V_{(t)})$

$$\therefore \delta t_1 = \frac{\delta VCR}{Vo - V_{t_1}}$$

$$\delta t_2 = \frac{\delta VCR}{Vo - V_{t_2}}$$

Positive Pulse Width Change $\Delta t^+ = \delta t_2 - \delta t_1$

$$= \delta VCR \frac{1}{Vo - V_{(t_2)}} - \frac{1}{Vo - V_{(t_1)}}$$

In the circuit $V_{t_2} = V_X, V_{t_1} = V_Y, Vo - V_X = V_Y$

$$\Delta t^+ = \delta VCR \left(\frac{1}{V_Y} - \frac{1}{V_X}\right) = \delta VCR \frac{V_X - V_Y}{V_X V_Y} = -\Delta t^-$$

∴ Offset errors do not affect the frequency of oscillation, only the symmetry of the waveshape.

SYMMETRY ERROR

$$\text{Symmetry } S = \frac{\Delta t^+ - \Delta t^-}{2T} \times 100\% \text{ where } T = CR\ 1n\ \frac{V_Y}{V_X}$$

$$S = \frac{2\Delta t^+}{2T} \times 100\%$$

$$= \frac{\delta VCR\ (V_X - V_Y)}{V_X V_Y} \times \frac{1}{CR\ 1n\ V_Y/V_X}$$

Symmetry is worse for maximum value of $V_X - V_Y$. Maximum value of $V_X - V_Y$ occurs when R_1 and R_2 are arranged for minimum operating frequency, i.e., $R_1/R_2 = 3.6$

Substituing $\delta V = 5mV$

$$V_X/V_Y = 3.6$$

$$V_X V_Y = \frac{1}{4.6} V_{OH} \times \frac{3.6}{4.6} V_{OH}$$

$V_{OH} = 3.5V$ and neglecting V_{OL}

Symmetry is $< 0.38\%$

Note: 1. For any given ratio of $R_1 : R_2$ (i.e., V_X and V_Y), offset voltage Symmetry error is independent of frequency.

2. Symmetry improves to .33% @ $R_1 : R_2 = 2.5$

EXTENDING LOW FREQUENCY PERFORMANCE

If it is necessary to extend the lower limit of the oscillation frequency, a small amount of positive feedback may be introduced by connecting a 2-4pF capacitor between the Q output and the non-inverting input. This will decrease the minimum input slew rate required and enable oscillation frequencies of 1kHz to be achieved without spurious oscillations occuring on the rising or falling edges of the waveform. At frequencies below 1MHz, it is not necessary to take into account any potential frequency shift this additional feedback introduces. (Above 1MHz, it is not necessary to use this additional feedback.)

PERFORMANCE CHARACTERISTICS:

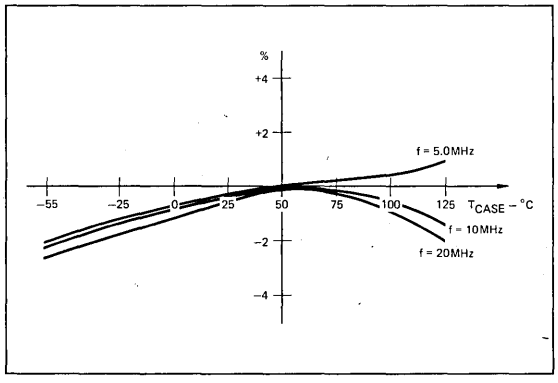


Figure 7. Percentage Change in Frequency Versus Case Temperature.

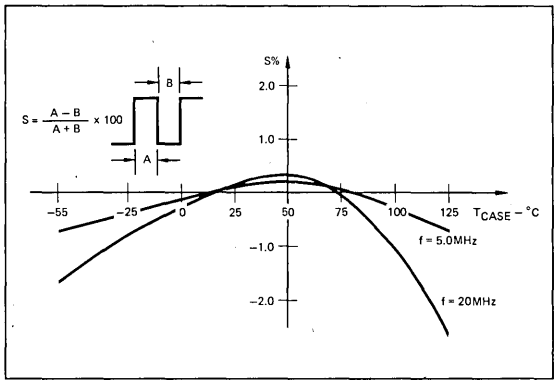


Figure 8. Change in Symmetry Versus Case Temperature.

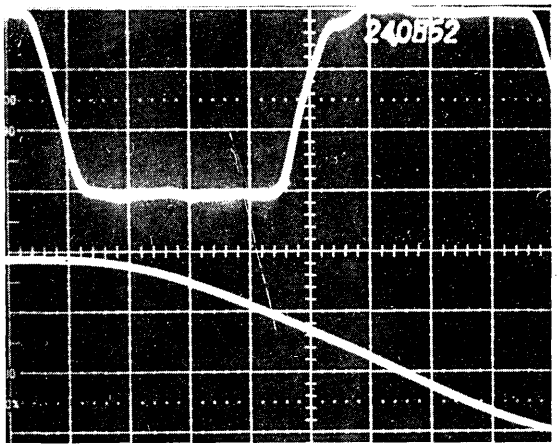


Figure 9. Output Waveform at 1.0MHz.

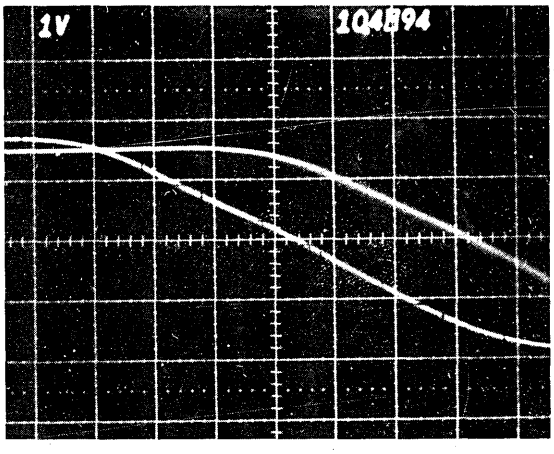


Figure 10. Output Waveform at 10MHz.

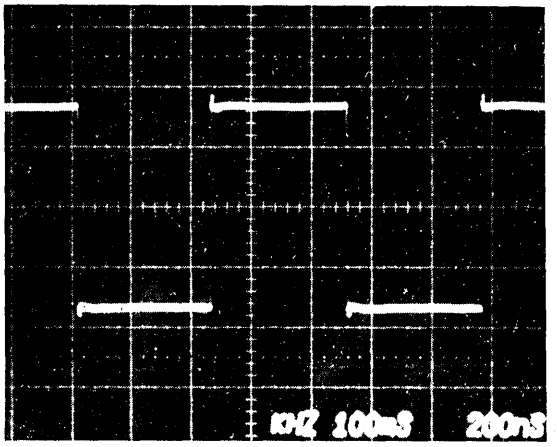


Figure 11. Output Waveform at 24MHz and Expanded Falling Edge Exhibiting <50ps Jitter.

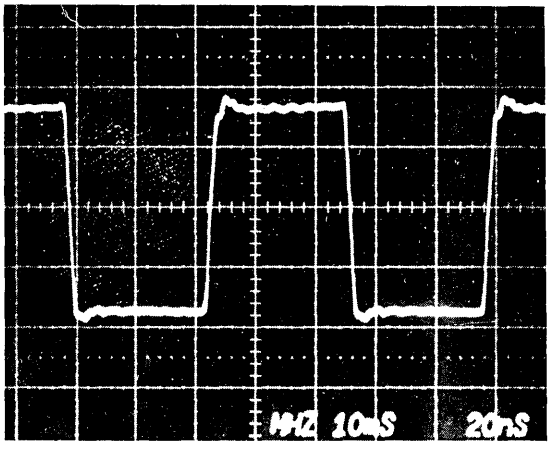


Figure 12. Change in Pulse Width and Jitter from 25°C to 125°C, f = 10MHz.

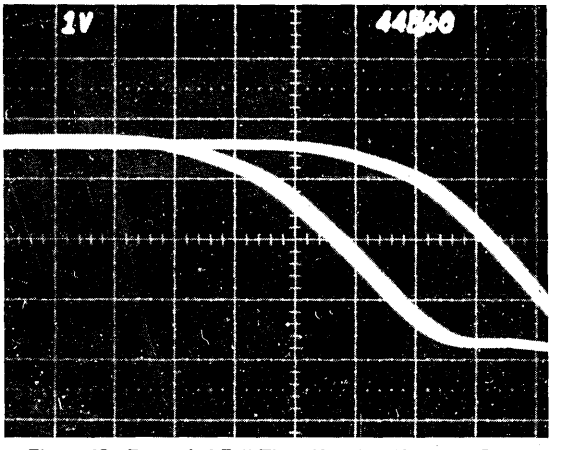


Figure 13. Expanded Fall Time Showing Change in Pulse Width from 25°C to 125°C, f = 1.0MHz, (Jitter ~ 300ps).

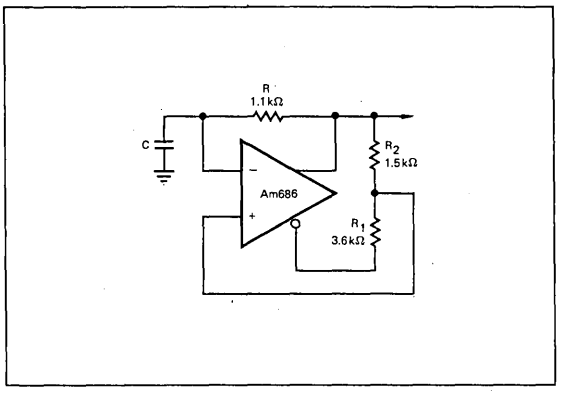


Figure 14. Circuit and Component Values used in Obtaining Performance Characteristics.

LOW LEVEL PULSE DETECTOR

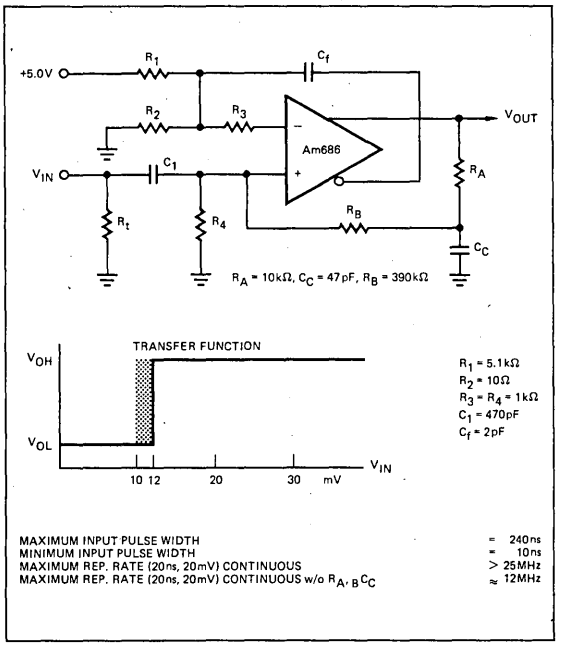


Figure 15.

CIRCUIT OPERATION

The input resistance is essentially determined by R_4 which was chosen to be 1kΩ on the basis that most sources would not be unduly loaded at this value and consequentially higher values would make the circuit excessively prone to oscillation. To minimize bias current errors, the inverting input is connected to the 10mV reference source (R_1 and R_2) through an equal-valued resistor (R_3).

Positive feedback is provided by C_f which provides a 50-60mV, 3-4ns pulse, significantly improving the switching time and narrowing the uncertainty region for pulses just in excess of the 10mV threshold.

Capacitor C_1 provides A-C coupling and thus isolates the circuit from slowly varying signals which may be superimposed on the signal to be detected. Such is the case for a detector sensing the output from a fibreoptic cable receiver. The A-C coupling imposes additional constraints; namely, the repetition rate and duty cycle of the input signal.

The signal which is seen by the non-inverting terminal and then compared to the reference is not simply the peak value of the input pulse but the peak value less the average D.C. value of the input signal.

Assuming a 20mV input pulse, 20ns wide and repeated every 20ns, the signal seen across R_4 will be as follows:

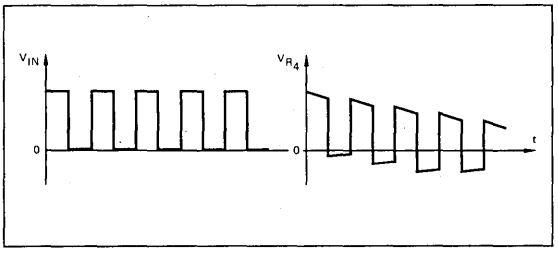


Figure 16.

By the ninth pulse, the peak signal will be 15.2mV dropping to 14.6mV by the end of the pulse; thus, after a pulse train of ~10 pulses, the detector will not detect the incoming signal.

Additionally, consider the case of a 20ns pulse repeated every 60 nanoseconds.

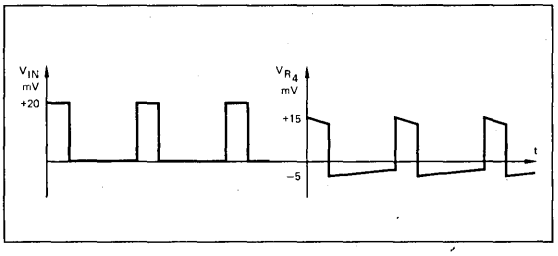


Figure 17.

The peak signal at the input will now be only 15mV; therefore, the maximum repetition rate consistent with providing a 5.0mV overdrive is 1/80ns or 12.5MHz.

Therefore, the circuit will only successfully detect 20mV, 20ns signals if: a) the pulse train is $\leq$ 10 pulses or b) the repetition rate $\leq$ 12MHz.

To compensate for these problems, a DC feedback signal is generated by R_A, R_B and C_C, which adjusts the reference level accordingly.

R_A and C_C form a low-pass filter that gives a maximum DC level of 1.7 volts at a 1:1 duty cycle. At this duty cycle, it is required to reduce the reference level by 5mV to maintain adequate overdrive. R_B and R_4 form an attenuator and the DC voltage level returned to the non-inverting input = 1.7V x $R_4/(R_4 + R_B)$ = 4.3mV. Using this network permits the circuit to work up to 25MHz, or better than a 1 : 1 duty cycle and removes the limitation imposed by the input A-C coupling.

Note: The response time of the feedback path must be the same as the input network; i.e., $R_AC_C = R_4C_1$ in order for the feedback to follow rapid changes in repetition rate or duty cycle.

PRECISION MONOSTABLE

Commercially available one-shots encounter problems in the generation of narrow (< 100ns) pulses. Namely, there is a significant delay between the input pulse and the output pulse of the order of 20ns and the resultant output pulse width is highly temperature dependent due to the variation in internal delays with temperature. Second, the input pulse must be of the logic level for the type of logic employed in the design — TTL, DTL, RTL, etc. Thus, the circuits are incapable of responding to low-level input signals in the millivolt range.

The Am685 series of sampling comparators can be employed in the design of a custom one-shot to overcome both of these problems.

Figure 18 shows the design of a monostable employing the Am686 to generate precision output pulses in the 20-100ns range and the values shown are for a 50ns pulse width.

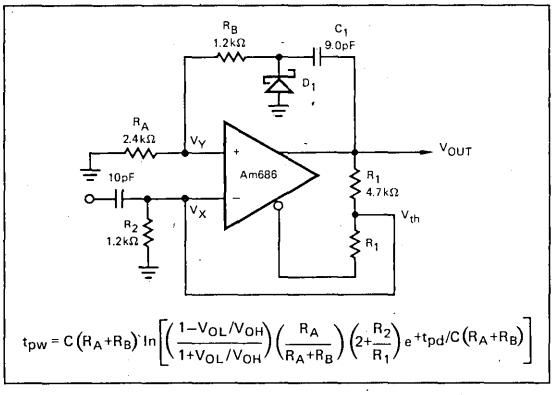


Figure 18.

The timing diagram illustrates the circuit operation.

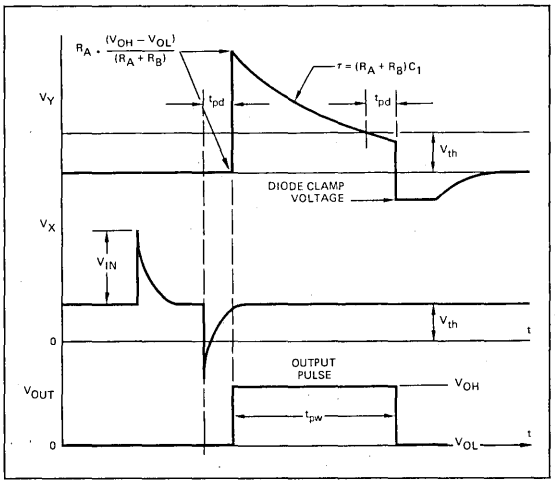


Figure 19.

The circuit triggers on the negative-going edge of the input pulse and the Q output switches high. The output signal is attenuated by R_A and R_B to keep the coupled pulse inside the common mode limits of the device. The output remains high until the voltage on the non-inverting input reaches the threshold set by R_1 and R_2. In order that the pulse width be independent of the input pulse amplitude, it is important to make the input time constant small compared to the desired output pulse width.

A unique feature of the circuit is the use of the differential outputs of the device to set the threshold, V_{th} thus providing temperature compensation and a reduction in pulse width variation from device to device.

Diode D_1 shortens the recovery time of the timing capacitor and permits retriggering 30ns after the end of the pulse with less than a 5% change in pulse width.

Complete isolation of the input signal and the timing network may be achieved by employing the latch function as shown below:

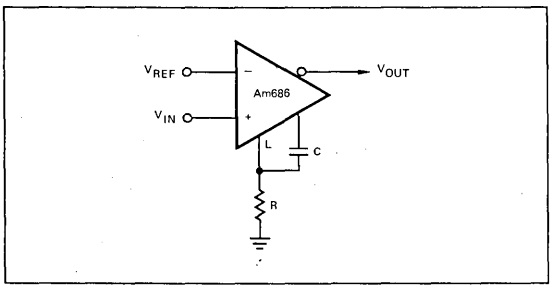


Figure 20.

When the input signal exceed V_{REF}, the output will switch and latch the comparator in the high state. When timing capacitor charges to the latch threshold, the latch will become disabled and the output will switch back to zero, providing the input is now below V_{REF}.

The advantages of this approach are:

1. No interaction between input signal and timing capacitor.
2. The input threshold set by V_{REF} is independent of the timing threshold.

Thus, the input threshold can be varied from millivolts to volts. A practical circuit is shown:

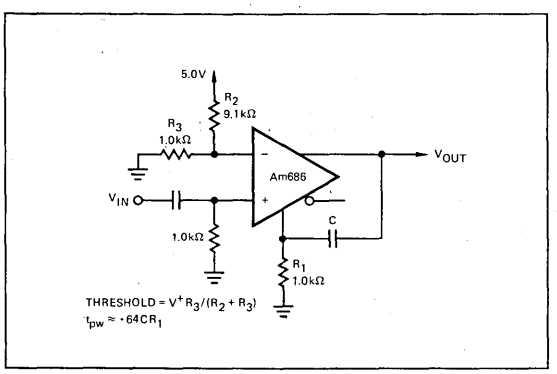


Figure 21.

The circuit is applicable for situations where accuracy of trigger threshold is important, a large variation in input signal level is expected or the input signal level is low. Timing accuracy (pulse width) is independent of the amplitude of the input pulse, but the output pulse width varies with temperature in accordance with the temperature dependence of the latch threshold (~ 3.0mV/°C for Am686).

APPLICATIONS REQUIRING INPUT HYSTERESIS

Comparators are frequently employed in systems where it is required that the transfer function contain a defined amount of hysteresis. Conventional comparators employing positive feedback can be used to generate hysteresis as shown below:

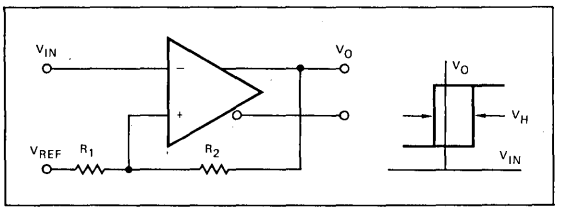


Figure 22.

Drawbacks of this technique include:

1. Response time of hysteresis loop ≥ comparator propagation delay
2. Hysteresis varies with V_{OH} and VOL changes
3. Hysteresis is not centered about zero unless an additional reference is used.

By utilizing the latch function on the Am685, Am686 and Am687, hysteresis can be inserted in a manner to overcome these drawbacks; namely:

1. **Response time of hysteresis loop << propagation delay**
2. Hysteresis not affected by V_{OH} and V_{OL} changes
3. Hysteresis is symmetrical about zero.
4. **Full input differential capability maintained over complete common mode range.**

The hysteresis is obtained by applying a slight bias to the latch inputs. The technique is illustrated in the test circuit shown for the Am687.

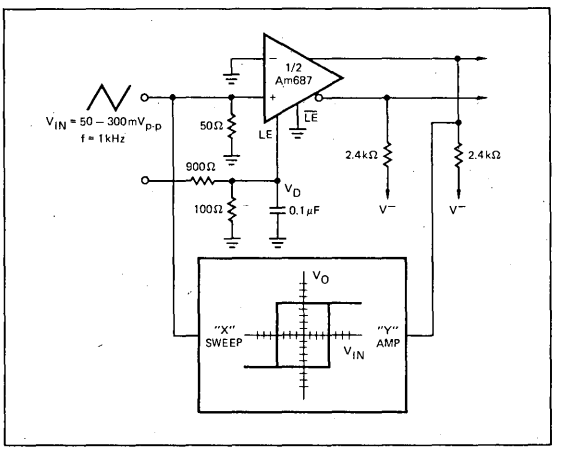


Figure 23.

The hysteresis is essentially symmetrical about zero and between ±5 and ±50mV of hysteresis can be generated before the relationship between the latch voltage and the thresholds become too sensitive.

The hysteresis is independent of changes in the positive supply voltage and the input common mode range and varies only with changes in temperature and negative supply voltage.

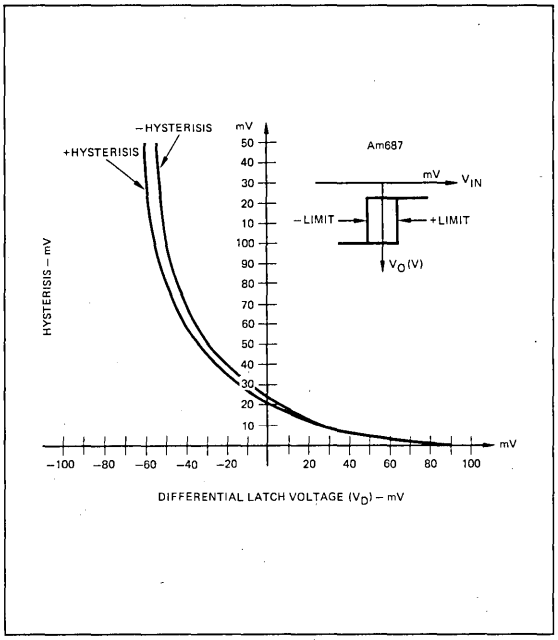


Figure 24. Input Hysteresis Versus Latch Voltage, $T_A = 25°C$.

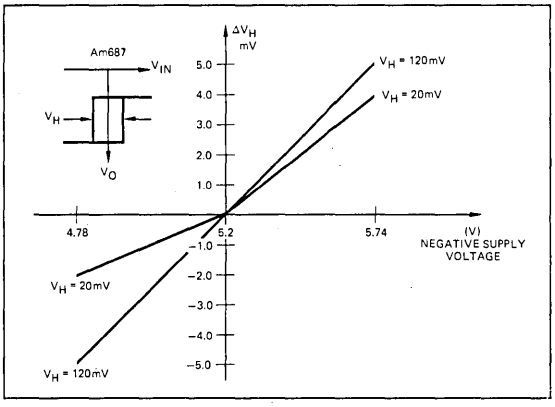


Figure 25. Change in Hysteresis Versus Change in Negative Supply Voltage.

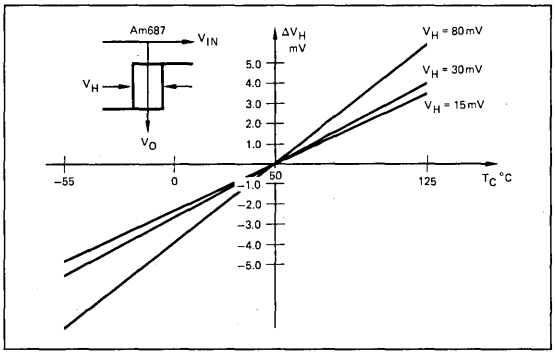
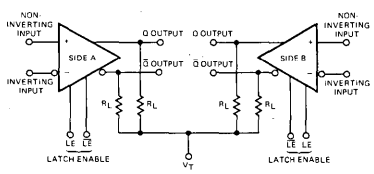


Figure 26. Change in Hysteresis Versus Case Temperature.

COMPARATOR PERFORMANCE SPECIFICATIONS

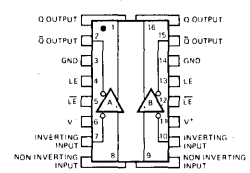
Am687

FUNCTIONAL DIAGRAM



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to −2.0V, or 200-2000Ω connected to −5.2V.

CONNECTION DIAGRAM
Top View



Note 1. Pin 6 is connected to bottom of case.

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics Symbol	Parameter	Conditions (Note 3)	Am687A-L Am687-L Min.	Am687A-L Am687-L Max.	Am687A-M Am687-M Min.	Am687A-M Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\Omega$	−3.5	+3.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$25°C \leq T_A \leq T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3 \leq V_{CM} \leq +2.7V$	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

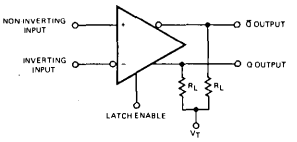
t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.
3. Unless otherwise specified $V^+ = +5.0V$, $V^- = -5.2V$, $V_T = -2.0V$, and $R_L = 50\Omega$; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

COMPARATOR PERFORMANCE SPECIFICATIONS (Cont.)

Am685

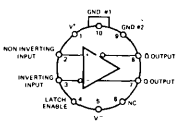
FUNCTIONAL DIAGRAM



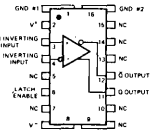
The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0 V, or 200–2000Ω connected to –5.2 V.

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 8 is connected to case.

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	–2.0	+2.0	–2.0	+2.0	mV
		$R_S \leq 100\Omega$	–2.5	+2.5	–3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	–10	+10	–10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	–1.0	+1.0	–1.0	+1.0	µA
			–1.3	+1.3	–1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		–3.3	+3.3	–3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3 \leq V_{CM} \leq +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	–0.960	–0.810	–0.960	–0.810	V
		$T_A = T_{A(min.)}$	–1.060	–0.890	–1.100	–0.920	V
		$T_A = T_{A(max.)}$	–0.890	–0.700	–0.850	–0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	–1.850	–1.650	–1.850	–1.650	V
		$T_A = T_{A(min.)}$	–1.890	–1.675	–1.910	–1.690	V
		$T_A = T_{A(max.)}$	–1.825	–1.625	–1.810	–1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

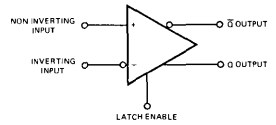
Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd+(E)}$	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd-(E)}$	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
$t_{pw(E)}$	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

NOTES:
2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.
3: Unless otherwise specified V^+ = 6.0V, V^- = –5.2V, V_T = –2.0V, and R_L = 50Ω; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

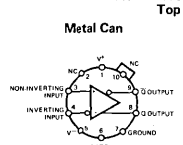
Am686

FUNCTIONAL DIAGRAM

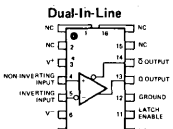


CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 6 is connected to case.

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	3.0	2.0	mV MAX.
		$R_S \leq 100\Omega$	3.5	3.0	mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	10	10	µV/°C MAX.
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_A$ (max.)	1.0	1.0	µA MAX.
		$T_A = T_A$ (min.)	1.3	1.6	µA MAX.
I_B	Input Bias Current	$25°C \leq T_A \leq T_A$ (max.)	10	10	µA MAX.
		$T_A = T_A$ (min.)	13	16	µA MAX.
V_{CM}	Input Voltage Range		+2.7, –3.3	+2.7, –3.3	V MIN.
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3V \leq V_{CM} \leq +2.7V$	80	80	dB MIN.
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$	70	70	dB MIN.
V_{OH}	Output HIGH voltage	$I_L = -1.0$mA, $V_S = V_S$ (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	$I_L = 10$mA, $V_S = V_S$ (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

Switching Characteristics ($V^+ = +5.0V$, $V^- = -6.0V$, $V_{in} = 100$mV, $V_{od} = 5.0$mV, $C_L = 15$pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) $\leq T_A \leq 25°C$	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) $\leq T_A \leq 25°C$	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	$T_A = 25°C$	2.0	2.0	ns MAX.

Notes: 2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.
3. Unless otherwise specified, $V^+ = +5.0V$, $V^- = -6.0V$ and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

Data Conversion Products — Section III

AmDAC-08

8-Bit High Speed Multiplying D/A Converter

Distinctive Characteristics

- Fast settling output current — 85nsec
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Nonlinearity to ±0.1% max over temperature range
- High output impedance and compliance
  −10V to +18V
- Differential current outputs
- Wide range multiplying capability
  1.0MHz bandwidth
- Low FS current drift — ±10ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33mW @ ±5V

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 nsec settling times with very low "glitch" and a low power consumption. Monotonic multiplying performance is attained over more than a 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

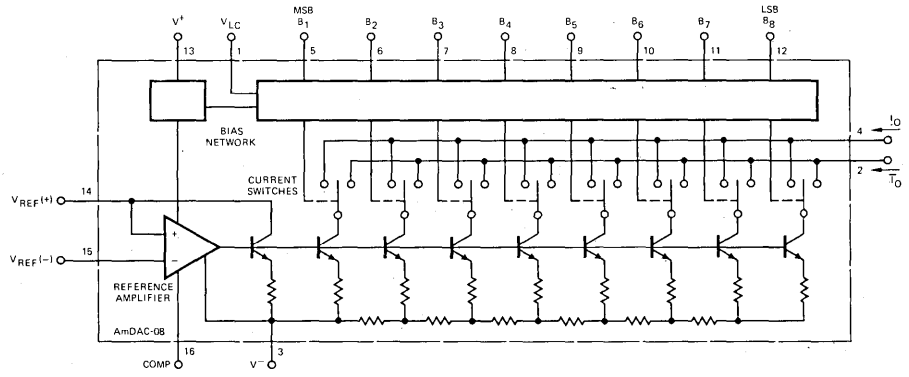
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. All devices are processed to MIL-STD-883.

DAC-08 applications include 8-bit, 1.0μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

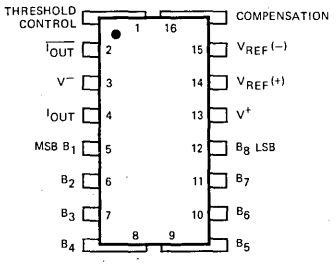
EQUIVALENT CIRCUIT



ORDERING INFORMATION

Order Number	Temperature Range	Nonlinearity
DAC-08AQ	−55°C to +125°C	±.1%
DAC-08Q	−55°C to +125°C	±.19%
DAC-08EQ	0°C to +70°C	±.19%
DAC-08CQ	0°C to +70°C	±.39%

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

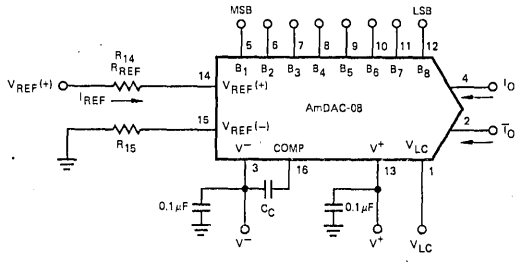
Operating Temperature	
DAC-08AQ, Q	–55°C to +125°C
DAC-08EQ, CQ	0°C to +70°C
Storage Temperature	–65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

V+ supply to V– Supply	36V
Logic Inputs	V– to V+ plus 36V
V_{LC}	V– to V+
Analog Current Outputs	See Fig. 12
Reference Inputs (V_{14}, V_{15})	V– to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS (V_S = ±15V, I_{REF} = 2.0mA)

Parameter	Description	Test Conditions	AmDAC-08A Min.	AmDAC-08A Typ.	AmDAC-08A Max.	AmDAC-08E Min.	AmDAC-08E Typ.	AmDAC-08E Max.	AmDAC-08C Min.	AmDAC-08C Typ.	AmDAC-08C Max.	Units
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity	T_A = MIN. to MAX.			±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±1/2 LSB, all bits switched ON or OFF, T_A = 25°C; DAC-08A, DAC-08		85	135		85	135				ns
		To ±1/2 LSB, all bits switched ON or OFF, T_A = 25°C; DAC-08E, DAC-08C					85	150		85	150	ns
t_{PLH}, t_{PHL}	Propagation Delay, Each Bit	T_A = 25°C		35	60		35	60		35	60	ns
	Propagation Delay, All Bits Switched	T_A = 25°C		35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < 1/2 LSB, R_{OUT} > 20MegΩ typ.	–10		+18	–10		+18	–10		+18	Volts
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R_{14}, R_{15} = 5.000kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1.0	±8.0		±2.0	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V⁻ = –5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V⁻ = –7.0V to –18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels, Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"	V_{LC} = 0V	2.0			2.0			2.0			Volts
I_{IL}	Logic Input Current, Logic "0"	V_{LC} = 0V, V_{IN} = –10V to +0.8V		–2.0	–10		–2.0	–10		–2.0	–10	μA
I_{IH}	Logic Input Current, Logic "1"	V_{LC} = 0V, V_{IN} = 2.0V to 18V		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V⁻ = –15V	–10		+18	–10		+18	–10		+18	Volts
V_{THR}	Logic Threshold Range	V_S = ±15V	–10		+13.5	–10		+13.5	–10		+13.5	Volts
I_{15}	Reference Bias Current			–1.0	–3.0		–1.0	–3.0		–1.0	–3.0	μA
dI/dt	Reference Input Slew Rate		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V^+ = 4.5V to 18V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
$PSSI_{FS-}$	Power Supply Sensitivity	V⁻ = –4.5V to –18V, I_{REF} = 1.0mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%/%
I^+	Power Supply Current	V_S = ±5.0V, I_{REF} = 1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-	Power Supply Current	V_S = ±5.0V, I_{REF} = 1.0mA		–4.3	–5.8		–4.3	–5.8		–4.3	–5.8	mA
I^+	Power Supply Current	V_S = +5.0V, –15V, I_{REF} = 2.0mA		2.4	3.8		2.4	3.8		2.4	3.8	mA
I^-	Power Supply Current	V_S = +5.0V, –15V, I_{REF} = 2.0mA		–6.4	–7.8		–6.4	–7.8		–6.4	–7.8	mA
I^+	Power Supply Current	V_S = ±15V, I_{REF} = 2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	mA
I^-	Power Supply Current	V_S = ±15V, I_{REF} = 2.0mA		–6.5	–7.8		–6.5	–7.8		–6.5	–7.8	mA
P_D	Power Dissipation	±5.0V, I_{REF} = 1.0mA		33	48		33	48		33	48	mW
P_D	Power Dissipation	+5.0V, –15V, I_{REF} = 2.0mA		108	136		108	136		108	136	mW
P_D	Power Dissipation	±15V, I_{REF} = 2.0mA		135	174		135	174		135	174	mW

BASIC CONNECTIONS



$$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000k$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
$V_{LC} = 0V$ (GROUND)

Figure 1. Basic Positive Reference Operation.

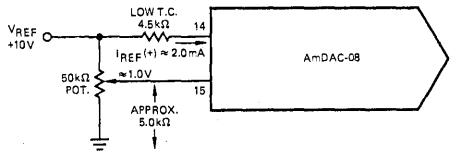
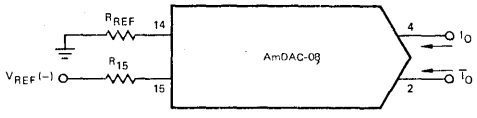


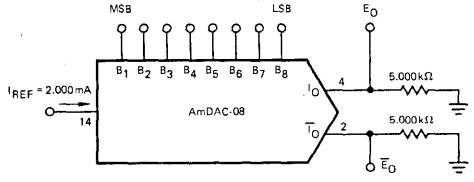
Figure 2. Recommended Full Scale Adjustment Circuit.



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

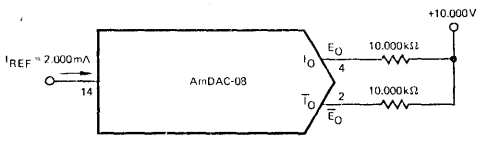
Note 1. R_{REF} Sets I_{FS}; R_{15} is for Bias Current Cancellation.

Figure 3. Basic Negative Reference Operation.



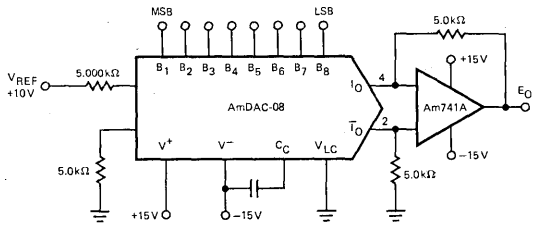
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	000	−9.960	000
FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	−.040
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	−.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Figure 4. Basic Unipolar Negative Operation.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	−9.940
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

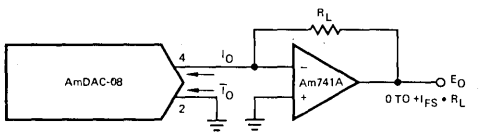
Figure 5. Basic Bipolar Output Operation.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	−9.940
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.920

Figure 6. Symmetrical Offset Binary Operation.

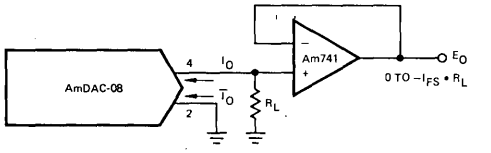
BASIC CONNECTIONS (Cont.)



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND

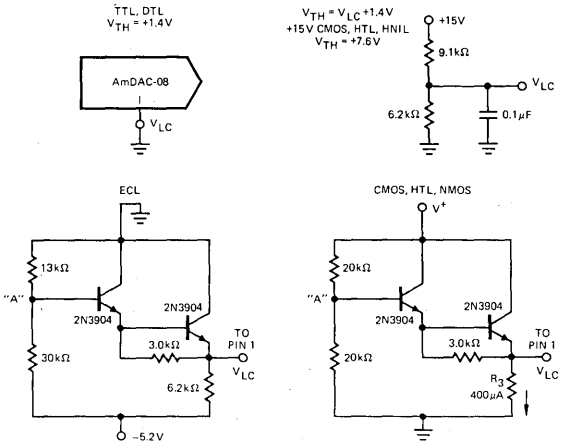
Figure 7. Positive Low Impedance Output Operation.



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

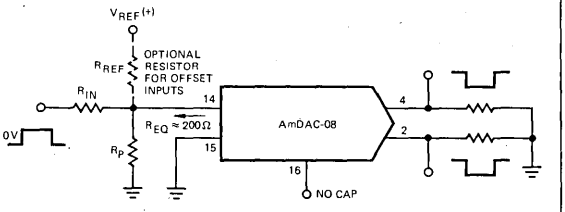
FOR COMPLEMENTARY (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 8. Negative Low Impedance Output Operation.



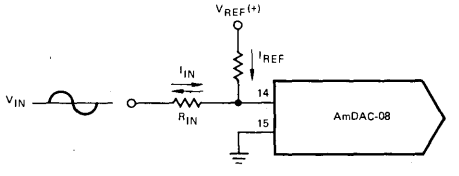
SET VOLTAGE AT NODE "A" EQUAL TO DESIRED LOGIC THRESHOLD.

Figure 9. Interfacing With Various Logic Families.

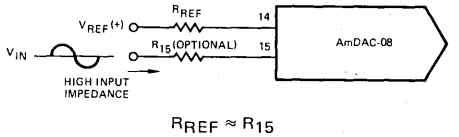


TYPICAL VALUES:
R_{IN} = 5k
$+V_{IN}$ = 10V

Figure 10. Pulsed Reference Operation.



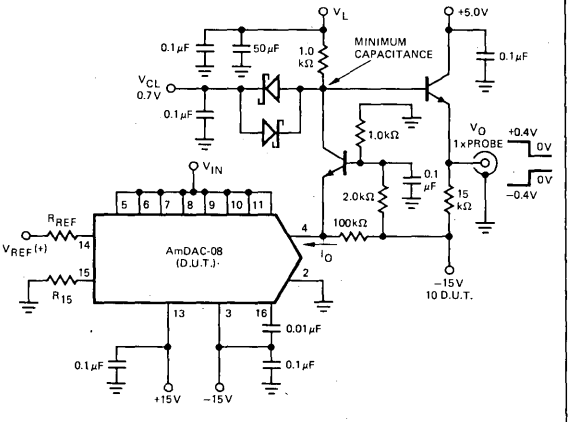
a) $I_{REF} \geq$ Peak Negative Swing of I_{IN}.



$R_{REF} \approx R_{15}$

b) $+V_{REF}$ Must Be Above Peak Positive Swing of V_{IN}.

Figure 11. Accomodating Bipolar References.



FOR TURN-ON, V_L = 2.7V
FOR TURN-OFF, V_L = 0.7V

Figure 12. Settling Time Measurement.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 1), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 3); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Fig. 11. The negative common mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus (I_{REF} X 1.0kΩ) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Fig. 2.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2.0mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Fig. 10. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus (I_{REF} X 1.0kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1.0mA is recommended. For interfacing other logic families, see Fig. 9. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, when $I_O + \overline{I}_O = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} • 1.0kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)\ (V+) + (I+)\ (V-) + (2\ I_{REF})\ (V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85nsec at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nsec, with each progressively larger bit taking successively longer. The MSB settles in 85nsec, thus determining the overall settling time of 85nsec. Settling to 6-bit accuracy requires about 65 to 70nsec. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 12 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients of "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

Am1508/1408
SSS1508A/1408A

8-Bit Multiplying D/A Converter

Distinctive Characteristics

- Improved direct replacement for MC1508/1408
- ±0.19% nonlinearity guaranteed over temperature range
- Improved settling time (SSS1508A/1408A) 250ns, typ.
- Improved power consumption (SSS1508A/1408A) 157mW, typ.
- Compatible with TTL, CMOS logic
- Standard supply voltage: +5.0V and −5.0V to −15V
- Output voltage swing: +0.5V to −5.0V
- High speed multiplying input: 4.0mA/μs

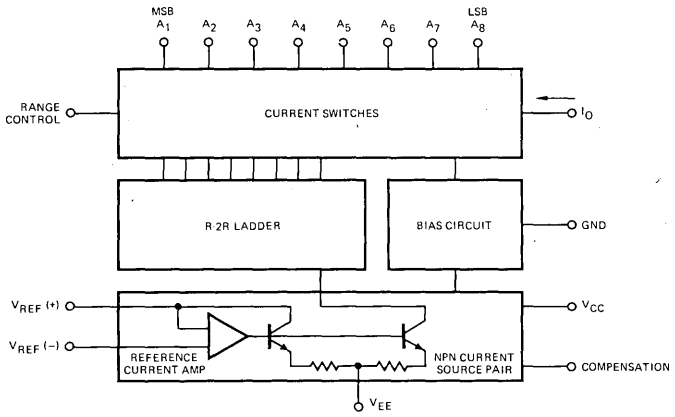
FUNCTIONAL DESCRIPTION

The SSS1508A/1408A, Am1508/1408 are 8-bit monolithic multiplying Digital-to-Analog Converters consisting of a reference current amplifier, an R-2R ladder, and eight high speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full scale output current of 1.992mA would result from a reference input current of 2.0mA.

The SSS1508A/1408A, Am1508/1408 is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building Tracking and Successive Approximation Analog-to-Digital Converters.

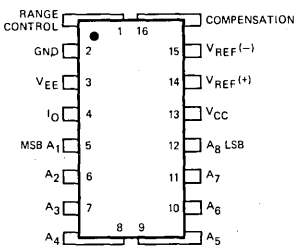
BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1408	Hermetic DIP	0°C to +70°C	AM1408L8
	Hermetic DIP	0°C to +70°C	AM1408L7
	Hermetic DIP	0°C to +70°C	AM1408L6
	Hermetic DIP	0°C to +70°C	SSS1408A-8Q
	Hermetic DIP	0°C to +70°C	SSS1408A-7Q
	Hermetic DIP	0°C to +70°C	SSS1408A-6Q
	Dice	0°C to +70°C	LD1408
Am1508	Hermetic DIP	−55°C to +125°C	AM1508L8
	Hermetic DIP	−55°C to +125°C	SSS1508A-8Q
	Dice	−55°C to +125°C	LD1508

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

(T_A = +25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	+5.5Vdc
V_{EE}	−16.5Vdc
Digital Input Voltage, V_5–V_{12}	+5.5, 0Vdc
Applied Output Voltage, V_O	−0.5, −5.2Vdc
Reference Current, I_{14}	5.0mA
Reference Amplifier Inputs, V_{14}, V_{15}	V_{CC}, V_{EE} Vdc

Power Dissipation (Package Limitation), P_D	
Ceramic Package	1000mW
Derate above T_A = +25°C	6.7mW/°C
Operating Temperature Range, T_A	
SSS1508A-8, Am1508	−55°C to +125°C
SSS1408A Series, Am1408 Series	0°C to +75°C
Storage Temperature, T_{stg}	−65°C to +150°C

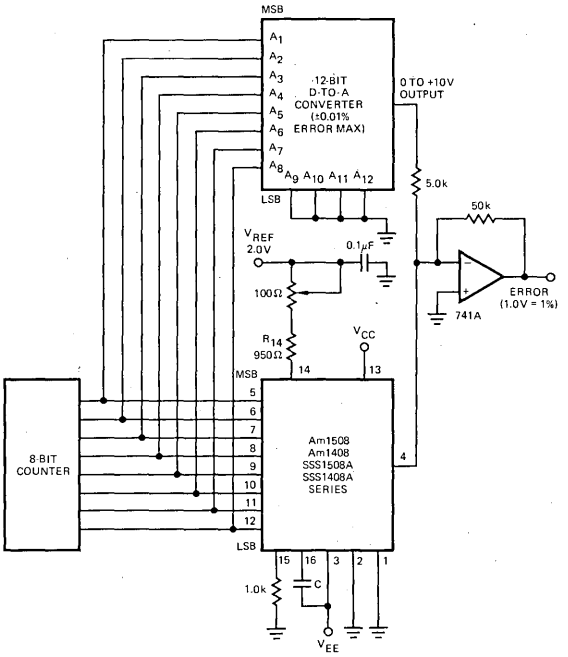
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(V_{CC} = 5.0Vdc, V_{EE} = −15Vdc, $\frac{V_{ref}}{R_{14}}$ = 2.0mA, SSS1508A-8/Am1508L8: T_A = −55°C to +125°C, SSS1408A/Am1408 Series: T_A = 0°C to +75°C unless otherwise noted. All digital inputs at high logic level.)

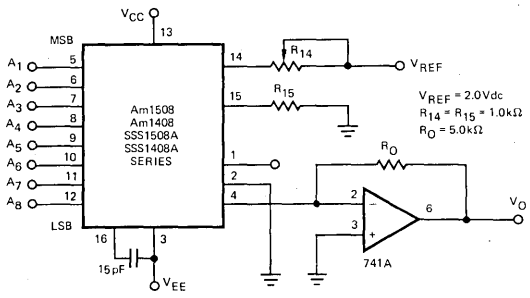
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
E_R	**Relative Accuracy**					
	SSS1508A-8, SSS1408A-8, Am1508L8, Am1408L8				±0.19	% IFS
	SSS1408A-7, Am1408L7				±0.39	
	SSS1408A-6, Am1408L6				±0.78	
t_S	**Settling Time to within 1/2 LSB (includes t_{PLH})**					
	SSS1508A/1408A	T_A = +25°C		250		ns
	Am1508/1408			300		
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = +25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		PPM/°C
	Digital Input Logic Levels (MSB)					
V_{IH}	High Level, Logic "1"		2.0			Vdc
V_{IL}	Low Level, Logic "0"				0.8	
I_{IH}	Digital Input Current (MSB)	High Level, V_{IH} = 5.0V		0	0.04	mA
I_{IL}		Low Level, V_{IL} = 0.8V		−0.002	−0.8	
	Reference Input Bias Current (Pin 15)					
I_{15}	SSS1508A/1408A			−1.0	−3.0	μA
	Am1508/1408			−1.0	−5.0	
I_{OR}	Output Current Range	V_{EE} = −5.0V	0	2.0	2.1	mA
		V_{EE} = −7.0V to −15V	0	2.0	4.2	
I_O	Output Current	V_{ref} = 2.000V, R_{14} = 1000Ω	1.9	1.99	2.1	mA
$I_{O\,(min.)}$	Output Current (All Bits Low)			0	4.0	μA
V_O	Output Voltage Compliance	V_{EE} = −5V			−0.6, +0.5	Vdc
	($E_r \leq 0.19\%$ at T_A = +25°C)	V_{EE} below −10V			−5.0, +0.5	
SRI_{ref}	Reference Current Slew Rate			4.0		mA/μs
$PSSI_O$	Output Current Power Supply Sensitivity			0.5	2.7	μA/V
	Power Supply Current					
I_{CC}	SSS1508A/1408A			2.5	14	mA
I_{EE}				−6.4	−13	
I_{CC}	Am1508/1408			2.5	22	
I_{EE}				−6.4	−13	
V_{CCR}	Power Supply Voltage Range	T_A = +25°C	4.5	5.0	5.5	Vdc
V_{EER}			−4.5	−15	−16.5	
P_d	**Power Dissipation**	All Bits Low				mW
	SSS1508A/1408A	V_{EE} = −5.0Vdc		34	136	
		V_{EE} = −15Vdc		108	265	
		All Bits High				
		V_{EE} = −5.0Vdc		34		
		V_{EE} = −15Vdc		108		
	Am1508/1408	All Bits Low				
		V_{EE} = −5.0Vdc		34	170	
		V_{EE} = −15Vdc		108	305	
		All Bits High				
		V_{EE} = −5.0Vdc		34		
		V_{EE} = −15Vdc		108		

TYPICAL APPLICATIONS

RELATIVE ACCURACY TEST CIRCUIT



USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

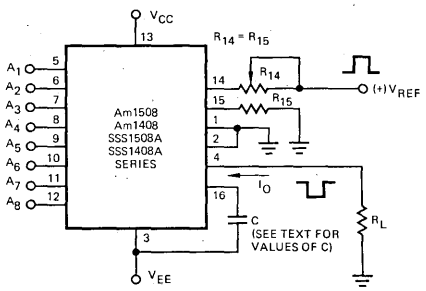
$$V_O = \frac{V_{REF}}{R_{14}}(R_O)\left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{126} + \frac{A_8}{256}\right]$$

ADJUST V_{REF}, R_{14} OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS

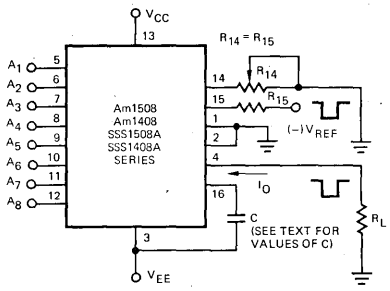
$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{126} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

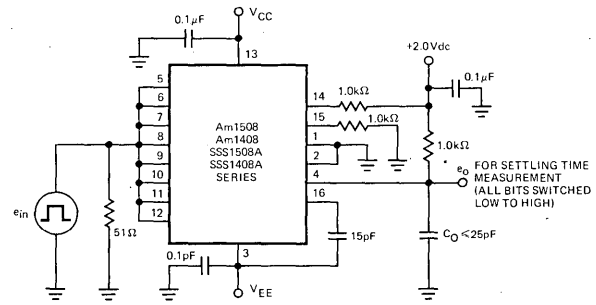
USE WITH POSITIVE V_{REF}



USE WITH NEGATIVE V_{REF}



TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive voltage are shown on page 3. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0 volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts when V_{EE} = −5.0V due to the current switching methods employed in the SSS1508A-8, Am1508.

The negative output voltage compliance of the SSS1508A-8, Am1508 is extended to −5.0V where the negative supply voltage is more negative than −10 volts. Using a full scale current of 1.992mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance but a 2.5-kilohm load increases "worst case" settling time to 1.2μS (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −7.0 volts, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the SSS1508A-8, Am1508 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the SSS1508A-8 has a very low full scale current drift with temperature.

The SSS1508A-8/Am1508 Series is guaranteed accurate to within ±1/2 LSB at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown on page 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the SSS1508A-8, Am1508 accuracy is essentially the same between 1.5 and 2.5mA. Then the SSS1508A-8, Am1508 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the SSS1508A-8, Am1508.

MULTIPLYING ACCURACY

The SSS1508A-8, Am1508 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the SSS1508A-8, Am1508 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a dc reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on," which coresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$pF.

The slowest single switch is the least significant bit. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Line Drivers/Receivers — Section IV

Am1603/3603

Dual Line Receivers

Distinctive Characteristics

- Three-state outputs for bus-organized systems
- Input sensitivity 3mV typical
- Common mode range of ±3V
- Common mode range of more than ±15V using external attenuator
- High common mode rejection ratio
- Blocking diodes provide high input impedance
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

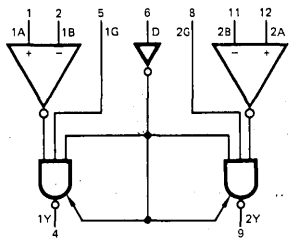
The Am1603 and Am3603 are high-speed dual line receivers designed for use as data receivers in balanced, unbalanced or party-line transmission systems. The two line receivers in each package share the common voltage and ground busses. All devices have a three-state output for bus organized systems.

Each receiver has a high impedance differential input for minimum transmission line loading. The differential inputs of the Am1603 and Am3603 are designed to detect input signals of 25mV or greater and provide TTL compatible outputs.

All devices contain block diodes in the input differential transistor pair collectors to provide high input impedance in the power-off condition.

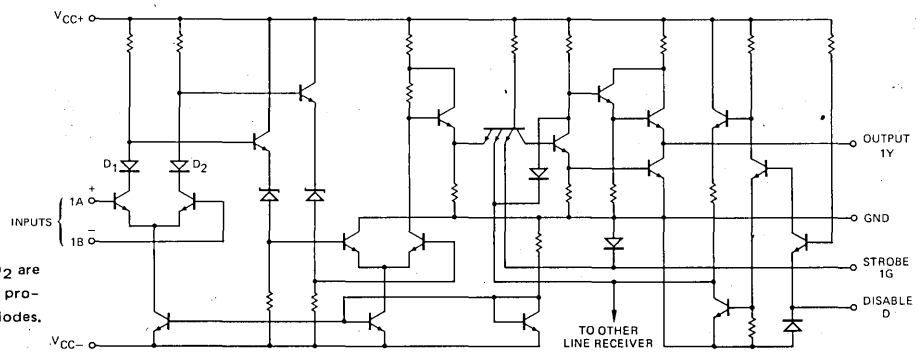
The device features a common three-state control, D. When the D input is HIGH, both outputs are in the high-impedance state regardless of all other inputs. Each receiver also has a separate gate input, G. When the gate input is LOW and the D input is also LOW, the receiver output is HIGH regardless of the A and B inputs.

LOGIC SYMBOL



V_{CC-} = Pin 13
V_{CC+} = Pin 14
GND = Pin 7

SCHEMATIC DIAGRAM
(One Receiver Shown)

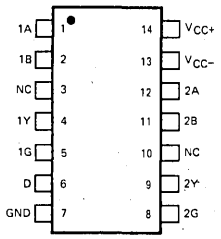


Note: D_1 and D_2 are the input protection diodes.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	DS3603N
Hermetic DIP	0°C to +70°C	DS3603J
Dice	0°C to +70°C	AM3603X
Hermetic DIP	-55°C to +125°C	DS1603J
Dice	-55°C to +125°C	AM1603X

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC+} max.
DC Input Voltage – Strobe	−0.5V to +5.5V
Differential Input Voltage	±6V
Common Mode Input Voltage (with Respect to GND Terminal)	±5V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Specified)

Am3603 $T_A = 0°C$ to $+70°C$ $V_{CC+} = 5.0V \pm 5\%$ $V_{CC-} = -5.0V \pm 5\%$ (COM'L)
Am1603 $T_A = -55°C$ to $+125°C$ $V_{CC+} = 5.0V \pm 10\%$ $V_{CC-} = -5.0V \pm 10\%$ (MIL)

Parameters	Description	Test Conditions (Notes 1, 4)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OH} = −2mA, V_{IC} = −3V to 3V V_{ID} = 25mV	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OL} = 16mA, V_{IC} = −3V to 3V V_{ID} = 25mV			0.4	Volts
V_{IH}	Disable or Gate Input HIGH Voltage	Guaranteed input logical HIGH voltage	2			Volts
V_{IL}	Disable or Gate Input LOW Voltage	Guaranteed input logical LOW voltage			0.8	Volts
V_{IDH}	Differential Input Voltage for Output HIGH		0.025		5.0	Volts
V_{IDL}	Differential Input Voltage for Output LOW		−5.0		−0.025	Volts
I_{IH}	Input HIGH Current into 1A,2A,1B or 2B	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75	μA
I_{IL}	Input LOW Current into 1A,2A,1B or 2B	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
I_{IH}	Input HIGH Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = 2.4V			40	μA
I_I	Input HIGH Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = V_{CC+} MAX.			1	mA
I_{IL}	Input LOW Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IL} = 0.4V			−1.6	mA
I_O	Output (off-state) Leakage	V_{CC+} = MIN., V_{CC-} = MIN., V_O = 2.4V			40	μA
		V_{CC+} = MIN., V_{CC-} = MIN., V_O = 0.4V			−40	μA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC+} = MAX., V_{CC-} = MAX.	−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, $T_A = 25°C$		28	40	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, $T_A = 25°C$		−8.4	−15	mA
V_I	Input Clamp Voltage, G or D	V_{CC+} = MIN., V_{CC-} = MIN. I_{IN} = −12mA, $T_A = 25°C$		−1	−1.5	Volts

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC+} = 5.0V$, $V_{CC-} = -5.0V$, $T_A = 25°C$ ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. V_{IC} = common mode voltage with respect to GND terminal.
V_{ID} = differential voltage ($V_A - V_B$).

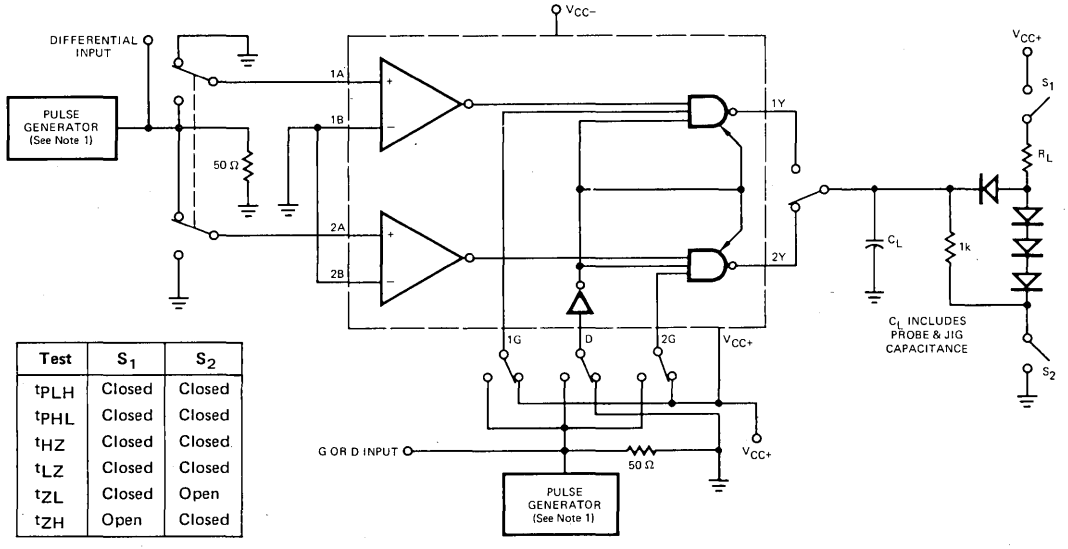
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC+} = 5.0V, V_{CC-} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} (Note 1)	A and B to Output	R_L = 390Ω, C_L = 50pF		17	25	ns
t_{PHL} (Note 1)	A and B to Output			17	25	ns
t_{PLH}	G to Output			10	15	ns
t_{PHL}	G to Output			8	15	ns
t_{HZ}	D to Output	R_L = 390Ω, C_L = 5pF			20	ns
t_{LZ}	D to Output	R_L = 390Ω, C_L = 5pF			30	ns
t_{ZH}	D to Output	R_L = 1kΩ to 0V, C_L = 50pF			25	ns
t_{ZL}	D to Output	R_L = 390Ω, C_L = 50pF			25	ns

Note: 1. Differential input is +100mV to −100mV pulse. Delays read from 0mV on input to 1.5V on output.

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



Test	S_1	S_2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{HZ}	Closed	Closed
t_{LZ}	Closed	Closed
t_{ZL}	Closed	Open
t_{ZH}	Open	Closed

Note: The pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_r = t_f$ = 10 ±5ns.

FUNCTION TABLE

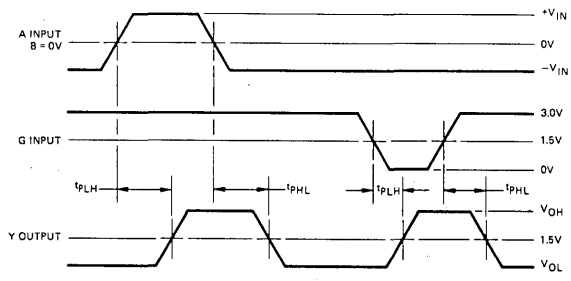
Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs		Output Y
	Gate G	Disable D	
$V_{ID} \geq +25mV$	X	L	H
$-25mV < V_{ID} < +25mV$	H	L	?
$V_{ID} \leq -25mV$	H	L	L
X	L	L	H
X	X	H	Z

H = HIGH
L = LOW
X = Don't Care
? = Don't Know

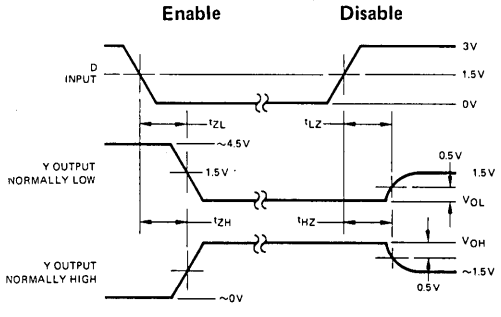
Z = High-Impedance State

VOLTAGE WAVEFORMS

PROPAGATION DELAY

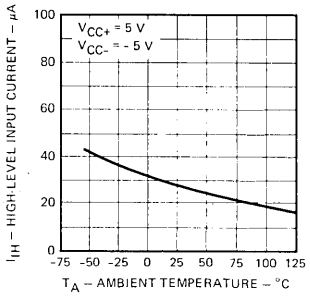


ENABLE AND DISABLE TIMES

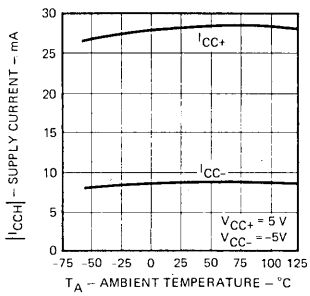


PERFORMANCE CURVES

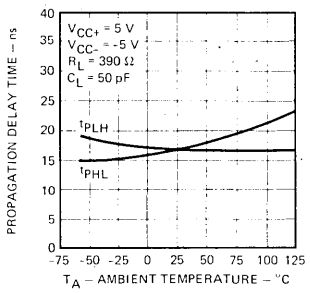
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



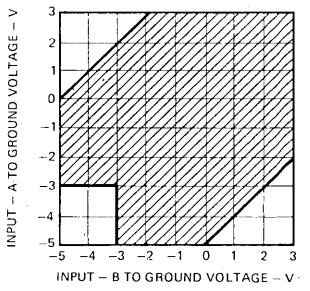
High-Logic-Level Supply Current Versus Ambient Temperature



Propagation Delay Time Differential Inputs Versus Ambient Temperature

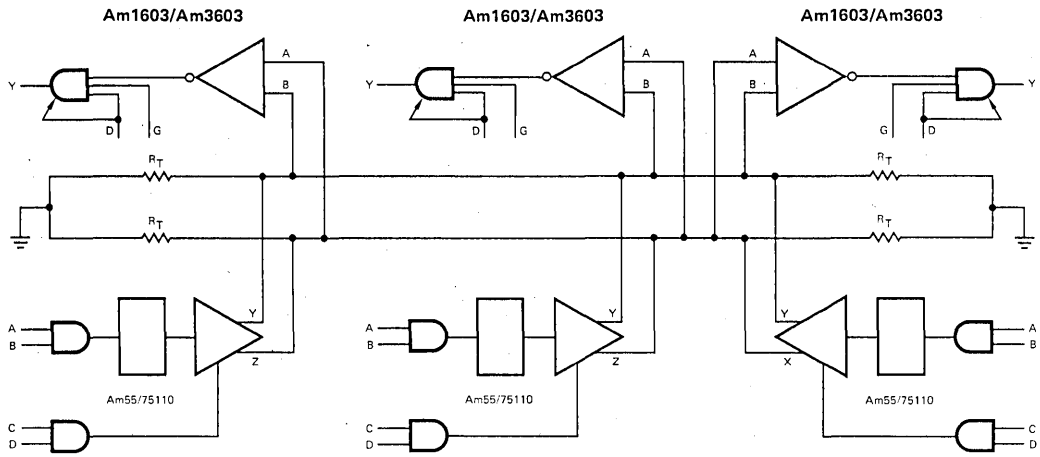


Recommended Combinations of Input Voltage for Line Receivers

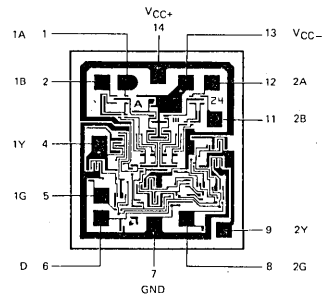


APPLICATIONS

BUS-ORGANIZED SYSTEM



Metallization and Pad Layout



DIE SIZE 0.049" X 0.056"

Am1488

Quad RS-232C Line Driver

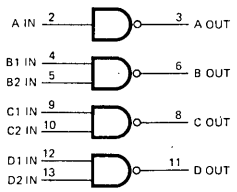
Distinctive Characteristics:

- Conforms to EIA specification RS-232C
- Short circuit protected output
- Simple slew rate control with external capacitor
- 100% reliability assurance testing in compliance with MIL STD 883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

The Am1488 is a quad line driver that conforms to EIA specification RS-232C. Each driver accepts one or two TTL/DTL inputs and produces a high-level logic signal on its output. The HIGH and LOW logic levels on the output are defined by the positive and negative power supplies to the drivers. For power supplies of plus and minus nine volts, the output levels are guaranteed to meet the ±6-volt specification with a 3kΩ load. There is an internal 300Ω resistor in series with the output to provide current limiting in both the HIGH and LOW logic levels. The Am1488 driver is intended for use with the Am1489 or Am1489A quad line receivers.

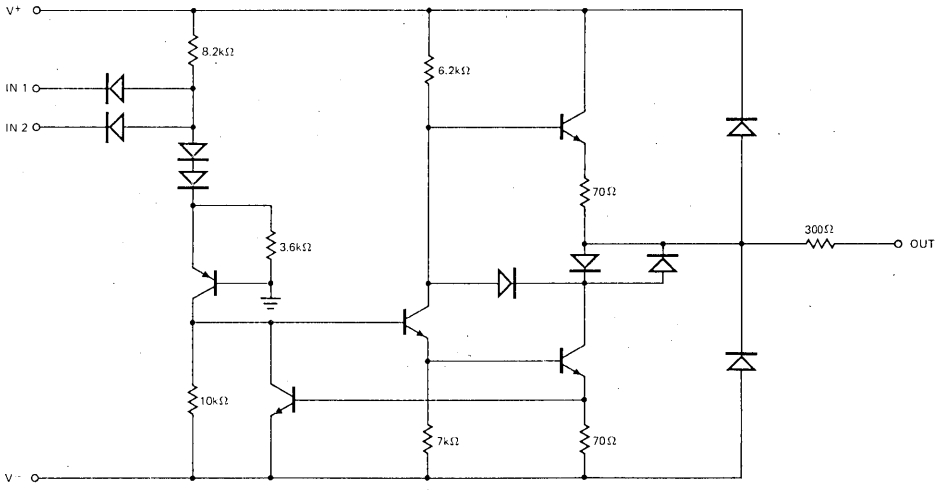
LOGIC SYMBOL



V⁻ = Pin 1
V⁺ = Pin 14
GND = Pin 7

4

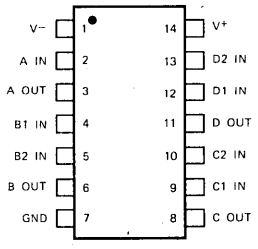
CIRCUIT DIAGRAM
(one driver shown)



Am1488 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	MC1488L
Molded DIP	0°C to +75°C	AM1488PC
Dice	0°C to +75°C	AM1488XC

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	V^+ +15V V^- −15V
DC Voltage Applied to Outputs for High Output State	$(V^+ +5.0V) \geq V_o \geq (V^- -5.0V)$
DC Input Voltage	±15V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The following conditions apply unless otherwise specified:
$T_A = 0°C$ to $+75°C$, $V^+ = +9.0V$, $V^- = -9.0V$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.6	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_L = 3.0k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$	6.0	7.0		Volts
			$V^+ = 13.2V$, $V^- = -13.2V$	9.0	10.5		Volts
V_{OL}	Low Level Output Voltage	$R_L = 3.0k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$	−6.0	−6.8		Volts
			$V^+ = 13.2V$, $V^- = -13.2V$	−9.0	−10.5		Volts
I_{SC}^+	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{SC}^-	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2.0V$		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V$, $V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V$, $V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = 9.0V$		4.5	6.0	mA
			$V^+ = 12V$, $V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V$, $V^- = -15V$		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V$, $V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V$, $V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		−1.0	−15	μA
			$V^+ = 12V$, $V^- = -12V$		−1.0	−15	μA
			$V^+ = 15V$, $V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V$, $V^- = -9.0V$			252	333	mW
		$V^+ = 12V$, $V^- = -12V$			444	576	mW

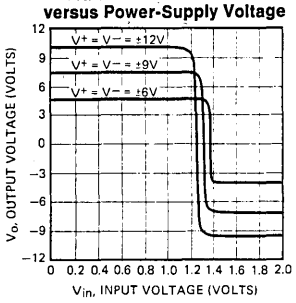
Switching Characteristics ($T_A = 25°C$, $V^+ = +9.0V$, $V^- = -9.0V$)

Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Delay from input LOW to output HIGH	$Z_L = 3.0\ k\Omega$ and 15 pF		150	200	ns
t_{PHL}	Delay from input HIGH to output LOW			65	120	ns
t_r	Output rise time			55	100	ns
t_f	Output fall time			45	75	ns

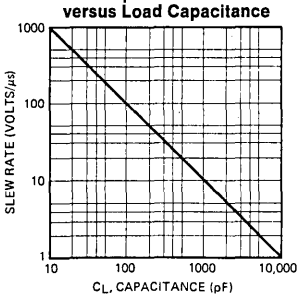
Note 1. Typical values are for $T_A = 25°C$.

TYPICAL CHARACTERISTICS

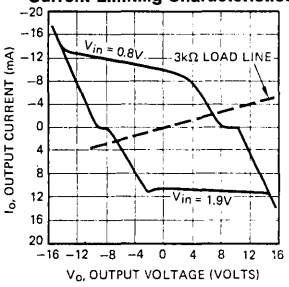
Transfer Characteristics versus Power-Supply Voltage

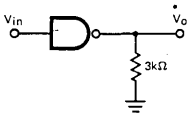


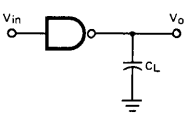
Output Slew Rate versus Load Capacitance

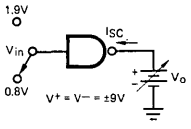


Output Voltage and Current-Limiting Characteristics

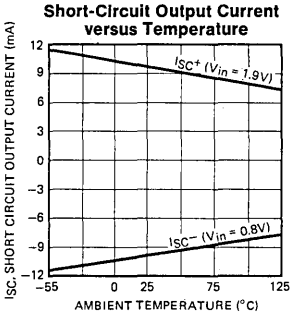




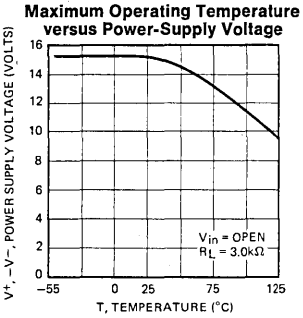




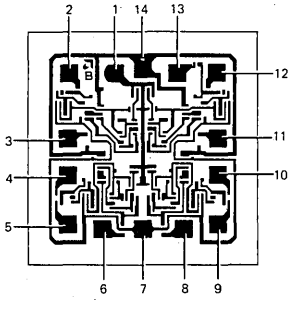
Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage



Metallization and Pad Layout



DIE SIZE 0.053" X 0.054"

Am1489•Am1489A

Quad RS-232C Line Receivers

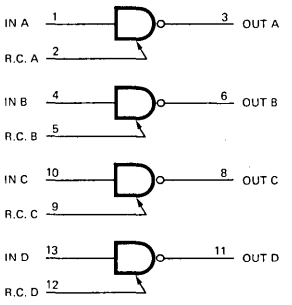
Distinctive Characteristics:

- Compatible with EIA specification RS-232C
- Input signal range ±30 volts
- 100% reliability assurance testing in compliance with MIL STD 883
- Includes response control input and built-in hysterisis

FUNCTIONAL DESCRIPTION:

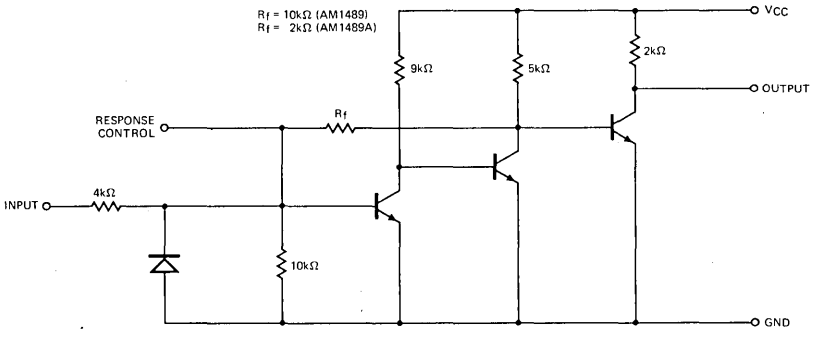
The Am1489 and Am1489A are quad line receivers whose electrical characteristics conform to EIA specification RS-232C. Each receiver has a single data input that can accept signal swings of up to ±30 V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. An internal feedback resistor causes the input to exhibit hysterisis so that AC noise immunity is maintained at a high level even near the switching thresholds. For both devices, when a receiver is in a LOW state on the output, the input may drop as LOW as 1.25 volts without affecting the output. Both devices are guaranteed to switch to the HIGH state when the input voltage is below 0.75 V. Once the output has switched to the HIGH state, the input may rise to 1.0 V for the Am1489 or 1.75 V for the Am1489A without causing a change in the output. The Am1489 is guaranteed to switch to a LOW output when its input reaches 1.5 V and, the Am1489A is guaranteed to switch to a LOW output when its input reaches 2.25 V. Because of this hysterisis in switching thresholds, the devices can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am1488.

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

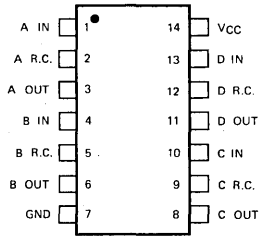
CIRCUIT DIAGRAM
(one receiver)



Am1489/Am1489A ORDERING INFORMATION

Package Type	Temperature Range	Am1489 Order Number	Am1489A Order Number
14-pin Molded DIP	0°C to +75°C	AM1489PC	AM1489APC
14-pin Hermetic DIP	0°C to +75°C	MC1489L	MC1489AL
Dice	0°C to +75°C	AM1489XC	AM1489AXC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +10 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am1489, Am1489A $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 1\%$ Response control pin open

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.5$ mA, $V_{IN} = +0.75$ V or open		2.6	4.0		Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 10$ mA, $V_{IN} = 1.5$ V			0.2	0.45	Volts
V_{IH}	Input HIGH Level Threshold	$T_A = 25°C$, $V_{OL} = 0.45$ V	Am1489	1.0	1.25	1.5	Volts
			Am1489A	1.75	1.95	2.25	
V_{IL}	Input LOW Level Threshold	$T_A = 25°C$, $V_{OH} = +2.5$ V		0.75		1.25	Volts
I_{IL}	Input LOW Current	$V_{IN} = -3.0$ V		−0.43			mA
		$V_{IN} = -25$ V		−3.6		−8.3	
I_{IH}	Input HIGH Current	$V_{IN} = +3.0$ V		0.43			mA
		$V_{IN} = +25$ V		3.6		8.3	
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.0$ V, $V_{OUT} = 0.0$ V			3.0		mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			20	26	mA

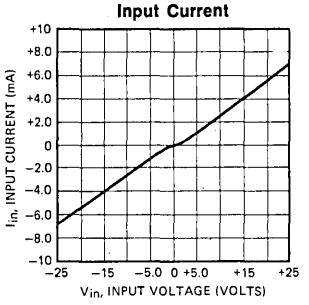
Note: 1) Typical Limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.

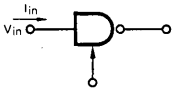
Switching Characteristics ($T_A = 25°C$, response control pin open, $C_L = 15$ pF)

Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Delay from Input LOW to Output HIGH	$R_L = 3.9$ kΩ		25	85	ns
t_{PHL}	Delay from Input HIGH to output LOW	$R_L = 390$ Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	$R_L = 3.9$ kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	$R_L = 390$ Ω		10	20	ns

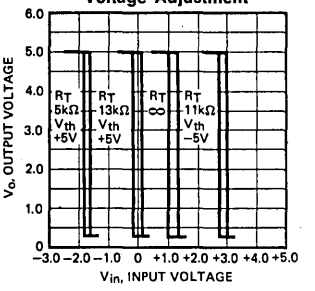
TYPICAL CHARACTERISTICS

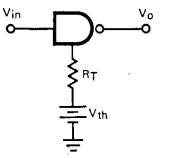
Input Current



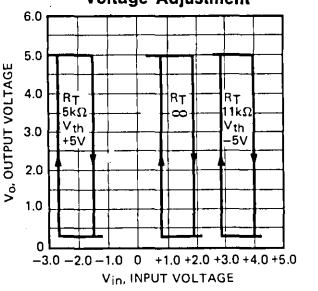


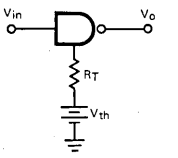
Am1489 Input Threshold Voltage Adjustment



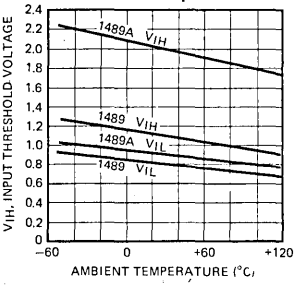


Am1489A Input Threshold Voltage Adjustment

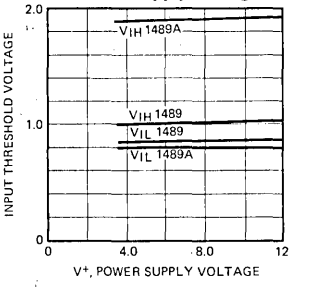




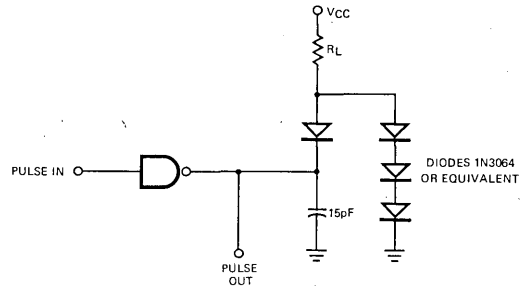
Input Threshold Voltage versus Temperature

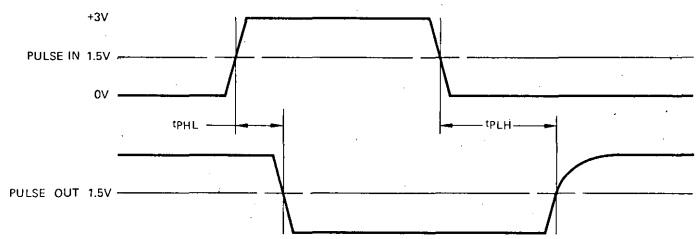


Input Threshold versus Power-Supply Voltage



SWITCHING TIME TEST CIRCUIT & WAVEFORMS





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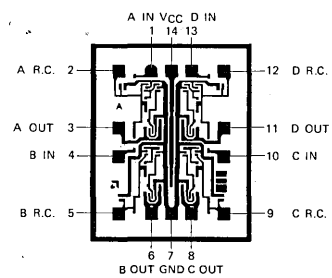
Metallization and Pad Layout



DIE SIZE 0.047" X 0.059"

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 50Ω transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

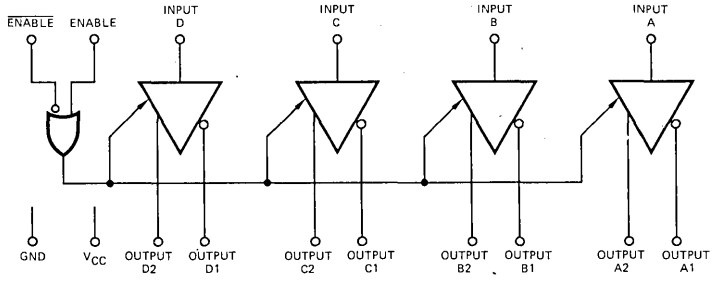
FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logically AND-ed complementary outputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

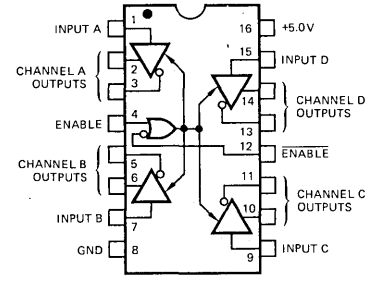
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM26LS31DM
Flat Pak	–55°C to +125°C	AM26LS31FM
Dice	–55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

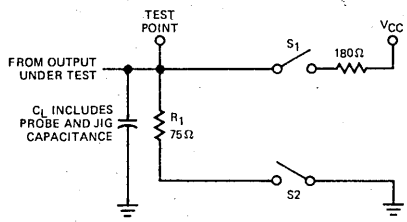
The following conditions apply unless otherwise specified:

Am26LS31XM (MIL) T_A = −55°C to +125°C V_{CC} = 5V ± 10%
Am26LS31XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5V ± 5%

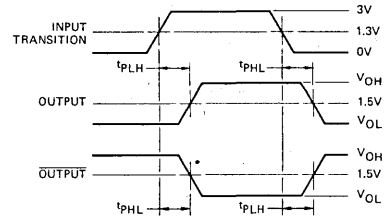
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −20mA		2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20mA				0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min.		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max.				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V				20	μA
I_I	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.5V			20	μA
			V_O = 0.5V			−20	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = 18mA				−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max.		−30		−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

Notes: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

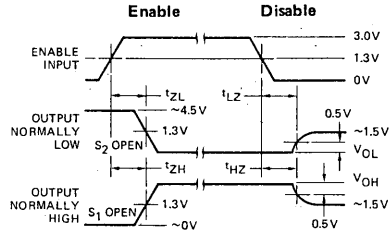
AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)

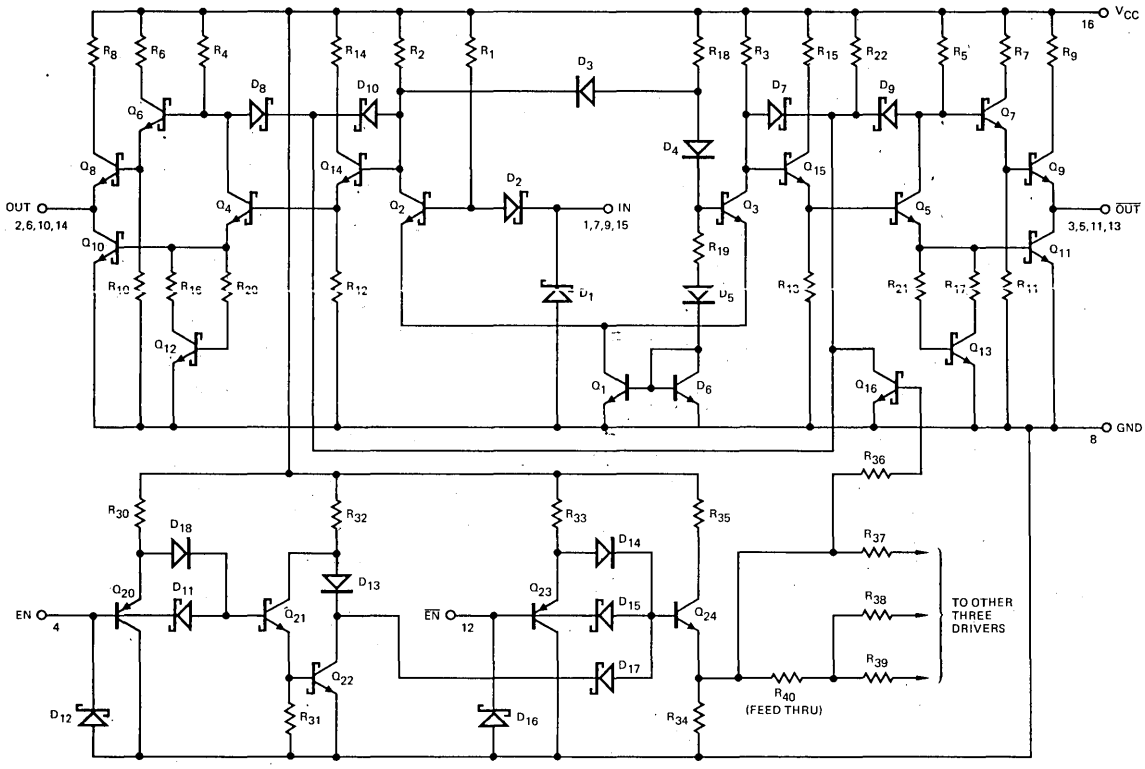


ENABLE AND DISABLE TIMES (Notes 2 and 3)

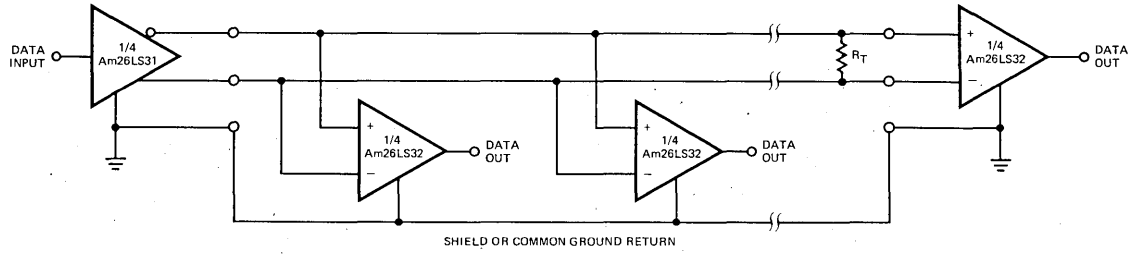


Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

EQUIVALENT CIRCUIT (1/4 Am26LS31)

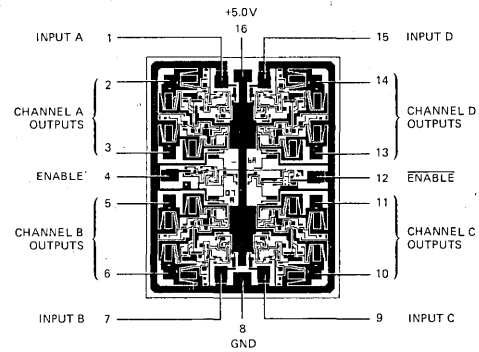


TYPICAL APPLICATION



4

Metallization and Pad Layout



DIE SIZE 0.067" X 0.084"

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

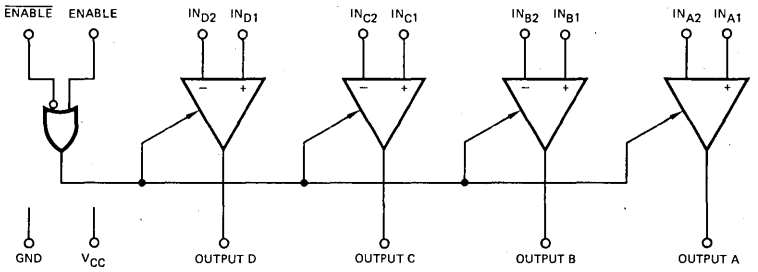
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

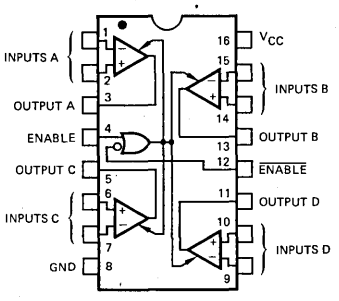
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	–55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	–55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	–55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

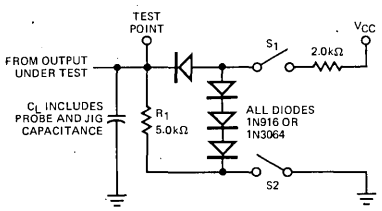
The following conditions apply unless otherwise specified:

Am26LS32XM, Am26LS33XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$
Am26LS32XC, Am26LS33XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

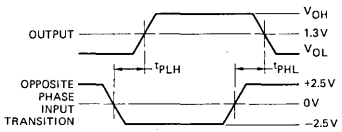
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, $-7V \leq V_{CM} \leq +7V$	0.2	0.06	0.2	Volts
			Am26LS33, $-15V \leq V_{CM} \leq +15V$	0.5	0.12	0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0k	8.5k		Ω
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0V$	COM'L	2.7	3.4		Volts
		$V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0V$	$I_{OL} = 4.0mA$			0.4	Volts
		$V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 2.4V$			20	mA
			$V_O = 0.4V$			−20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$				20	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max., $\Delta V_{IN} = +1.0V$		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
I_I	Input High Current	$V_{IN} = 5.5V$				100	μA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

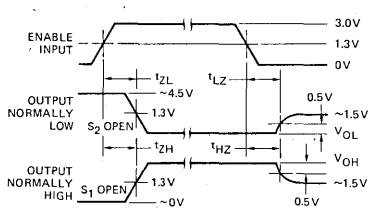
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)



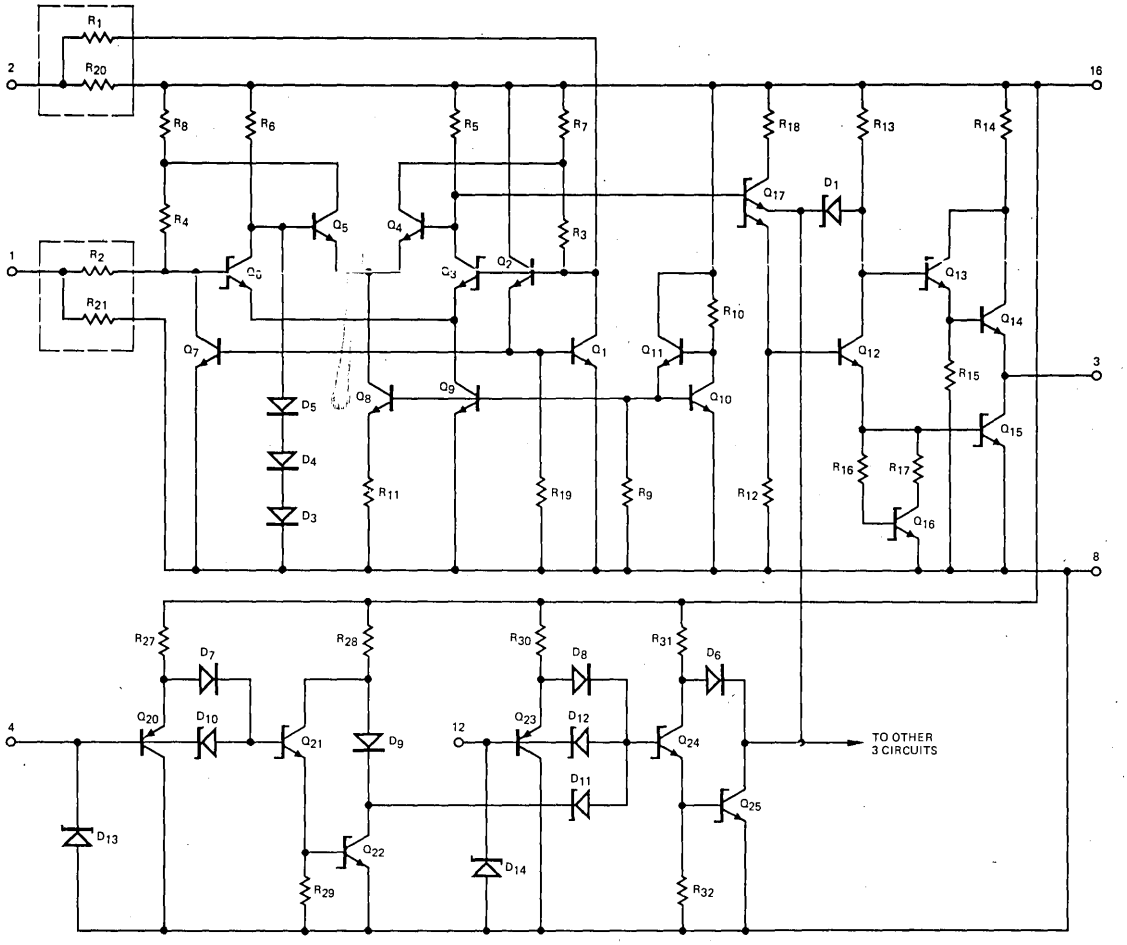
ENABLE AND DISABLE TIMES (Notes 2 and 3)



Notes:

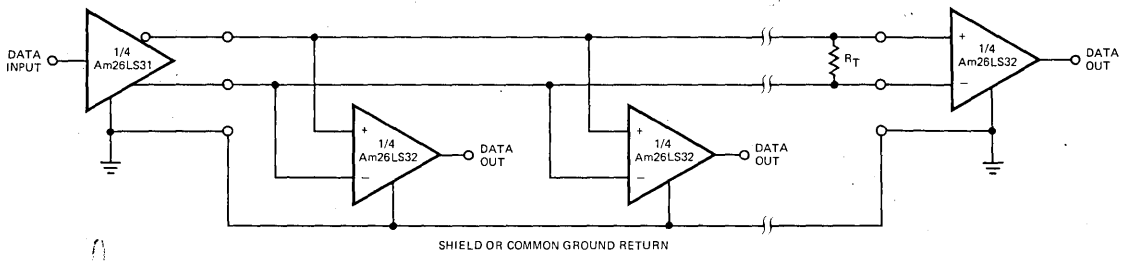
1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

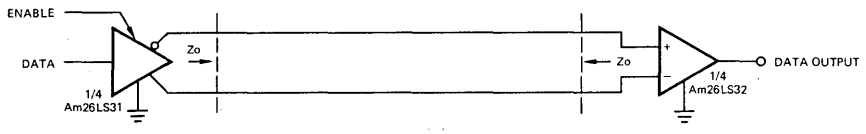
EQUIVALENT CIRCUIT (1/4 Am26LS32 OR Am26LS33)



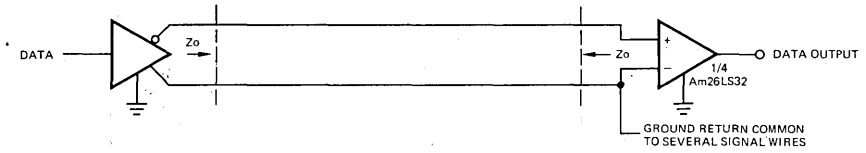
Note: R_4 value for Am26LS32 is 1/2 of Am26LS33 value.

TYPICAL APPLICATION





Two Wire Balanced System.



Single Wire With Common Ground Unbalanced System.

4

LINE TERMINATION

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of a reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

Various matching techniques that can be employed are shown in Figure 1. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V-I graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points — points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switched states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees one transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line sees at first a step to one half the final value and, two line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.

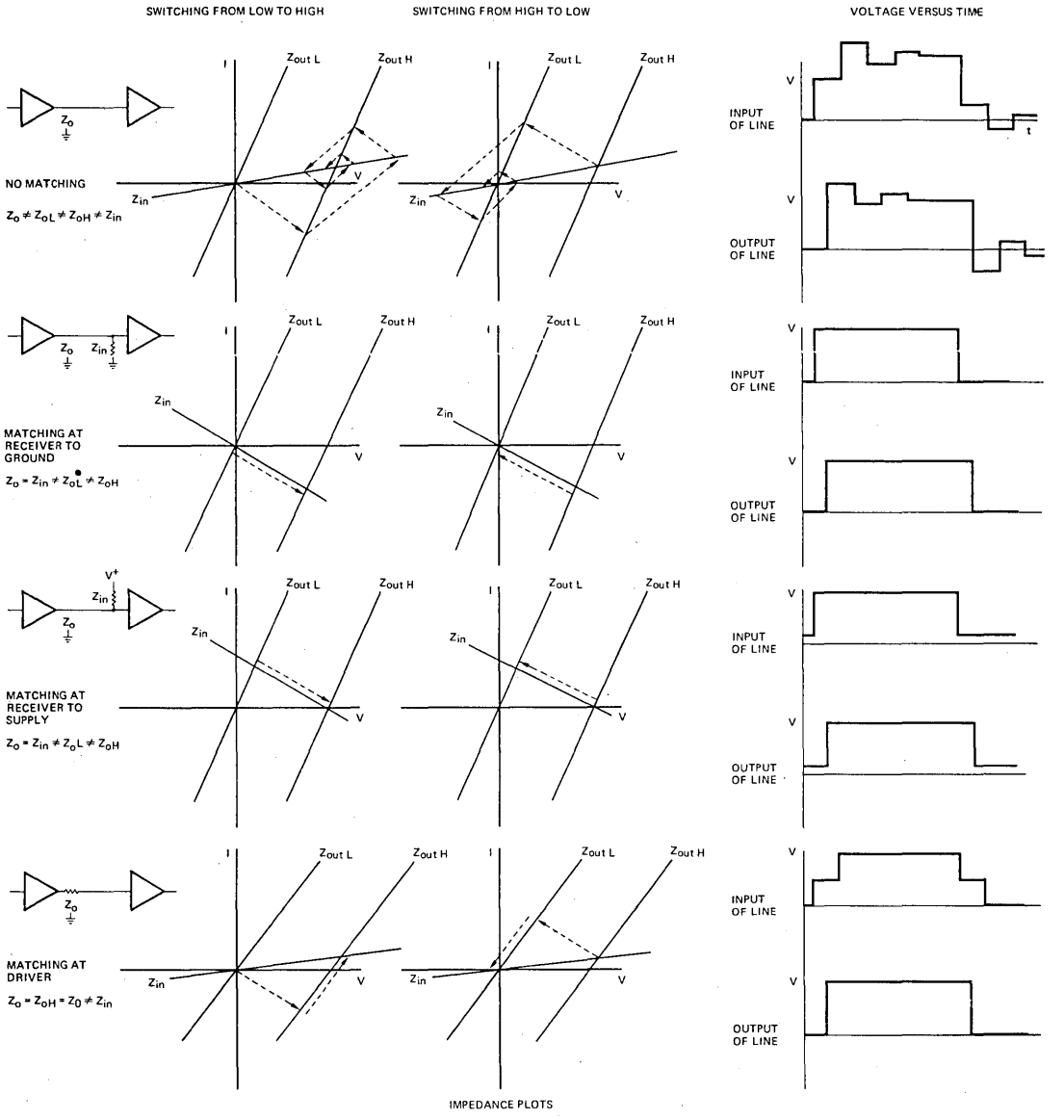
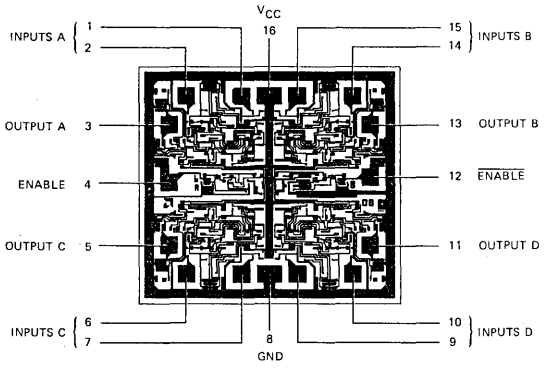


Figure 1. Line Matching Methods

Metallization and Pad Layout



DIE SIZE
0.063" X 0.069"

Am26S10 • Am26S11

Quad Bus Transceivers

Distinctive Characteristics

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

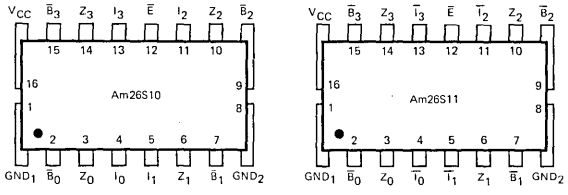
The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

ORDERING INFORMATION

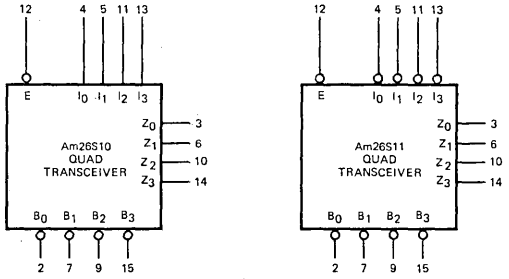
Package Type	Temperature Range	Am26S10 Order Number	Am26S11 Order Number
Molded DIP	0°C to +70°C	AM26S10PC	AM26S11PC
Hermetic DIP	0°C to +70°C	AM26S10DC	AM26S11DC
Dice	0°C to +70°C	AM26S10XC	AM26S11XC
Hermetic DIP	−55°C to +125°C	AM26S10DM	AM26S11DM
Hermetic Flat Pack	−55°C to +125°C	AM26S10FM	AM26S11FM
Dice	−55°C to +125°C	AM26S10XM	AM26S11XM

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

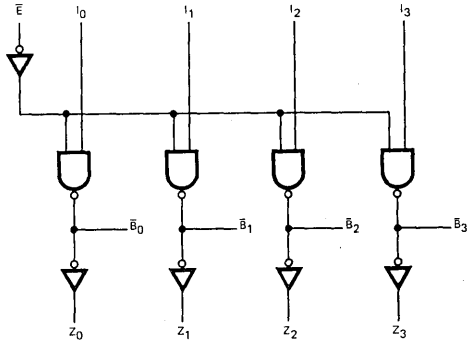
LOGIC SYMBOLS



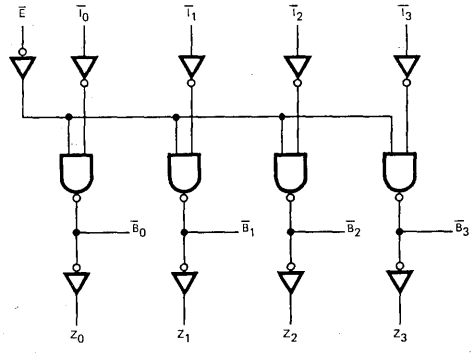
V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

LOGIC DIAGRAMS

Am26S10



Am26S11



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am26S10XC, Am26S11XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am26S10XM, Am26S11XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = −1.0mA, V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	µA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX., Enable = GND	Am26S10		45	70	mA
			Am26S11			80	

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			−50	µA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX	MIL		2.4	2.0		Volts
			COM'L		2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN	MIL			2.0	1.6	Volts
			COM'L			2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Bus	Am26S10	R_B = 50Ω C_B = 50pF (Note 1)		10	15	ns
t_{PHL}					10	15	
t_{PLH}		Am26S11			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	Am26S10			14	18	ns
t_{PHL}					13	18	
t_{PLH}		Am26S11			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out		R_B = 50Ω, R_L = 280Ω C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}					10	15	
t_r	Bus		R_B = 50Ω C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLES

Am26S10

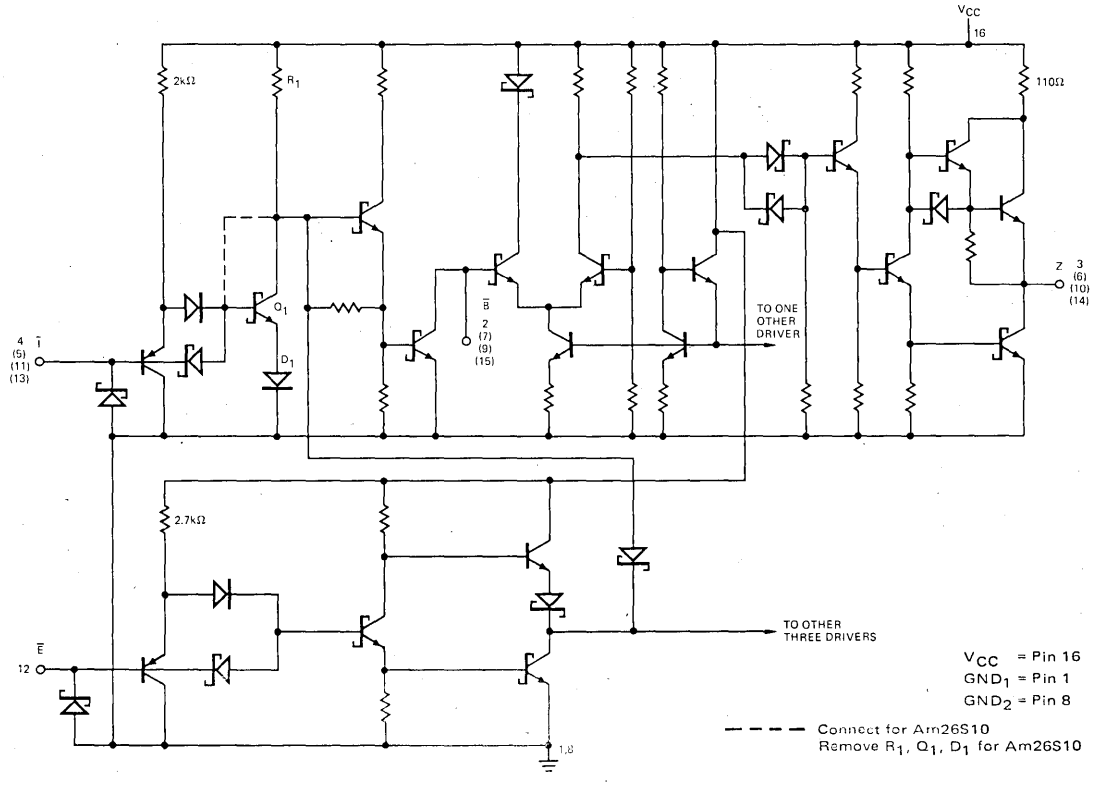
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

Am26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

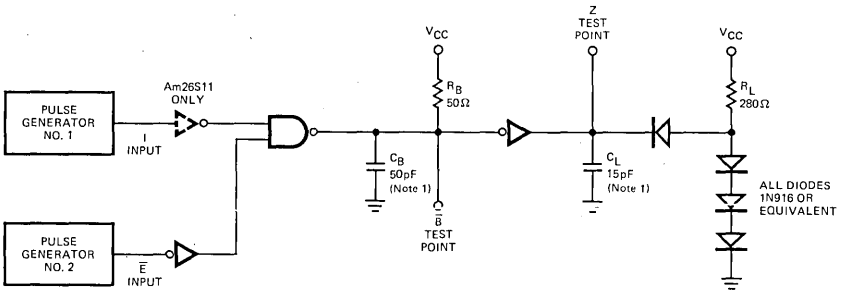
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

Am26S10/Am26S11 SCHEMATIC DIAGRAM



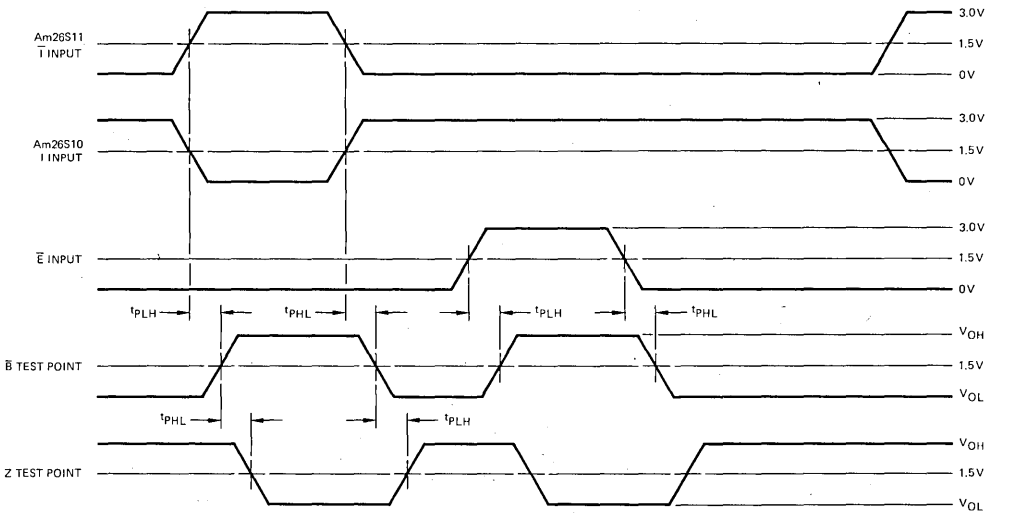
SWITCHING CHARACTERISTICS

TEST CIRCUIT



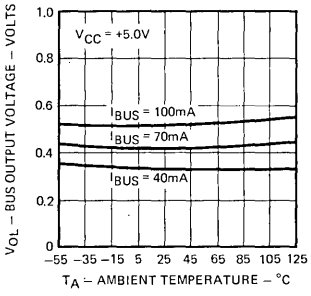
Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS

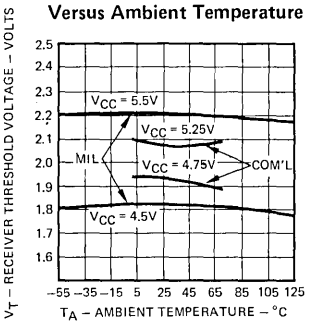


TYPICAL PERFORMANCE CURVES

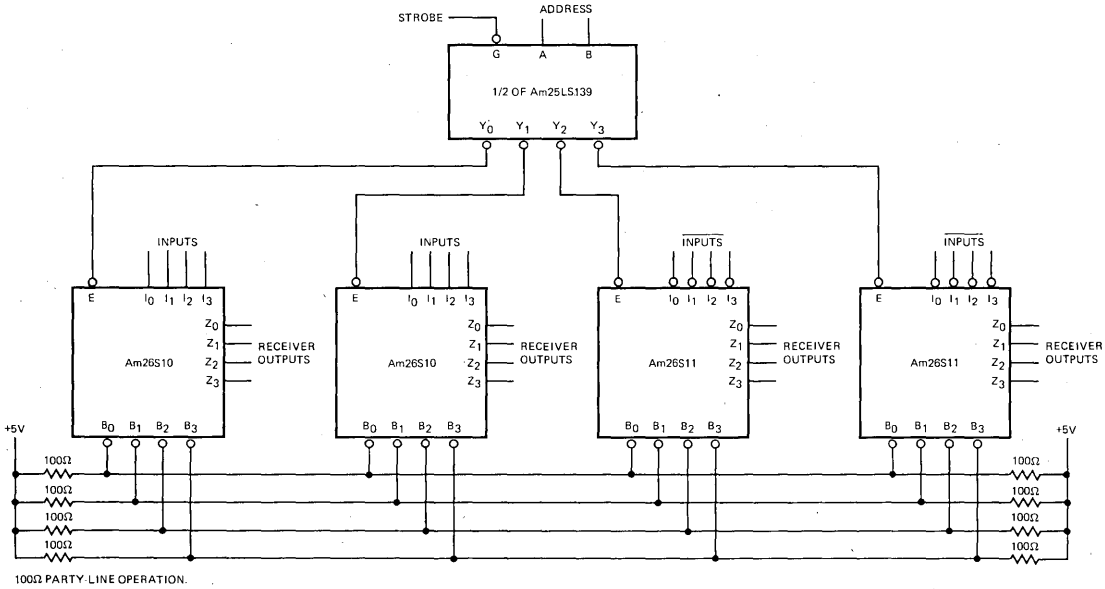
Typical Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



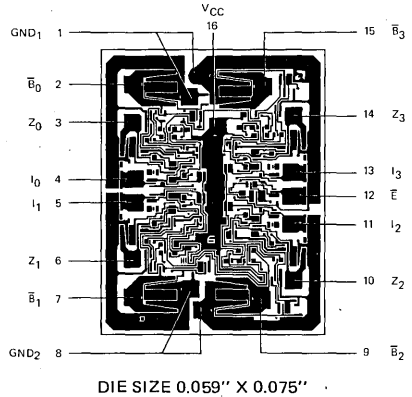
TYPICAL APPLICATION



100Ω PARTY-LINE OPERATION.

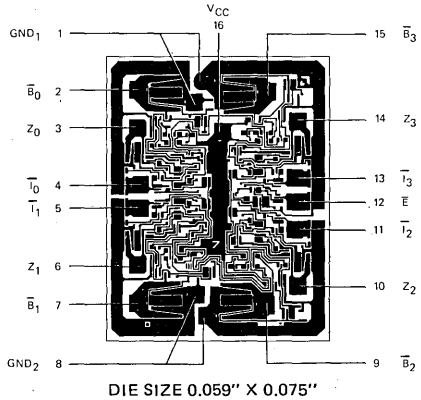
Metallization and Pad Layout

Am26S10



DIE SIZE 0.059" X 0.075"

Am26S11



DIE SIZE 0.059" X 0.075"

Am26S12•Am26S12A

Quad Bus Transceiver

Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- 100% reliability assurance testing in compliance with MIL-STD-883
- Choice of receiver hysteresis characteristics

FUNCTIONAL DESCRIPTION

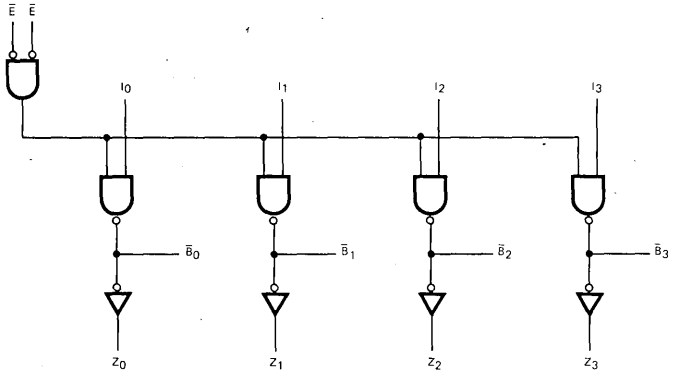
The Am26S12 • Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

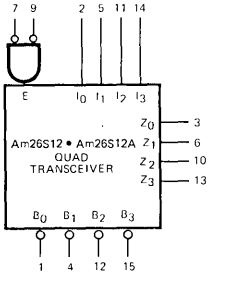
An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

LOGIC DIAGRAM/SYMBOL



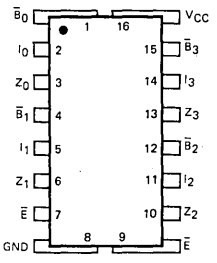


V_{CC} = PIN 16
GND = Pin 8

ORDERING INFORMATION

Package Type	Temperature Range	Am26S12 Order Number	Am26S12A Order Number
Molded DIP	0°C to +75°C	AM26S12PC	AM26S12APC
Hermetic DIP	0°C to +75°C	AM26S12DC	AM26S12ADC
Dice	0°C to +75°C	AM26S12XC	AM26S12AXC
Hermetic DIP	−55°C to +125°C	AM26S12DM	AM26S12ADM
Flat Pak	−55°C to +125°C	AM26S12FM	AM26S12AFM
Dice	−55°C to +125°C	AM26S12XM	AM26S12AXM

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs (BUS)	200mA
Output Current, Into Outputs (Receiver)	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S12XC-Am26S12AXC T_A = 0°C to +75°C V_{CC} = 5.0V ±5% (COM Range)
Am26S12XM-Am26S12AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL Range) Note 1

Parameters	Description	Test Conditions	Min.	Typ. (Note 2)	Max.	Units
I_{CC}	Power Supply Current	V_{CC} = MAX.		46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX. or 0V; V_{BUS} = 4.0V; Driver in OFF State			100	μA

Driver Characteristics

V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 100mA		0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_I = 2.4V				1.0	40	μA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_I = 0.4V				−0.4	−1.6	mA

Receiver Characteristics

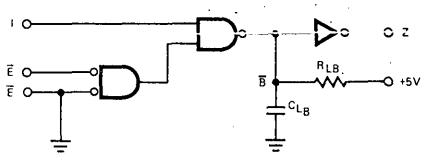
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA, V_{IN} = V_{IL} (Receiver)		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} (Receiver)			0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12	1.8	2.0	2.2	Volts
			Am26S12A	2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12	1.2	1.4	1.6	Volts
			Am26S12A	1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H		0.4			Volts
I_{OS}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20		−55	mA

Notes: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Turn Off Delay Input to Bus	C_{LB} = 15pF, R_{LB} = 100Ω		7	11	ns
t_{PHL}	Turn On Delay Input to Bus	C_{LB} = 300pF, R_{LB} = 50Ω		14	21	ns
t_{PLH}	Turn Off Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PHL}	Turn On Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PLH}	Turn Off Delay Bus to Output	C_L = 15pF		18	26	ns
t_{PHL}	Turn On Delay Bus to Output	C_L = 15pF		18	26	ns

SWITCHING CIRCUITS AND WAVEFORMS



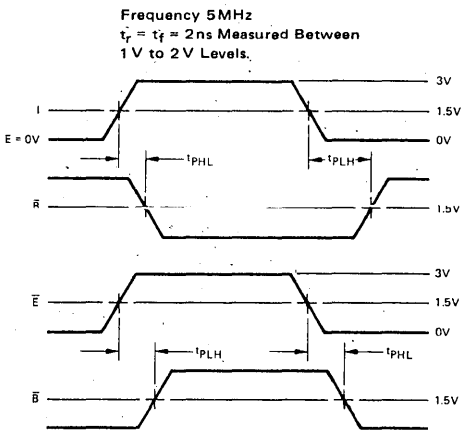
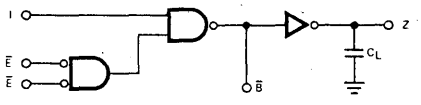


Figure 1. Bus Propagation Delays



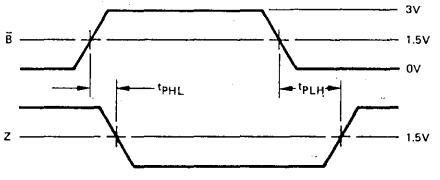


Figure 2. Receiver Propagation Delays

TRUTH TABLE
Am26S12/26S12A

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

PERFORMANCE CURVES

Am26S12 Typical Receiver Input Characteristic

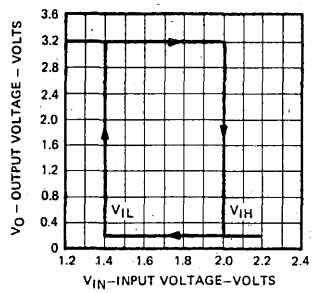


Figure 3

Am26S12A Typical Receiver Input Characteristic

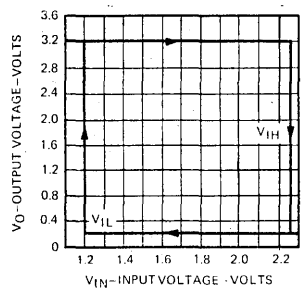


Figure 4

INPUT/OUTPUT CIRCUITRY

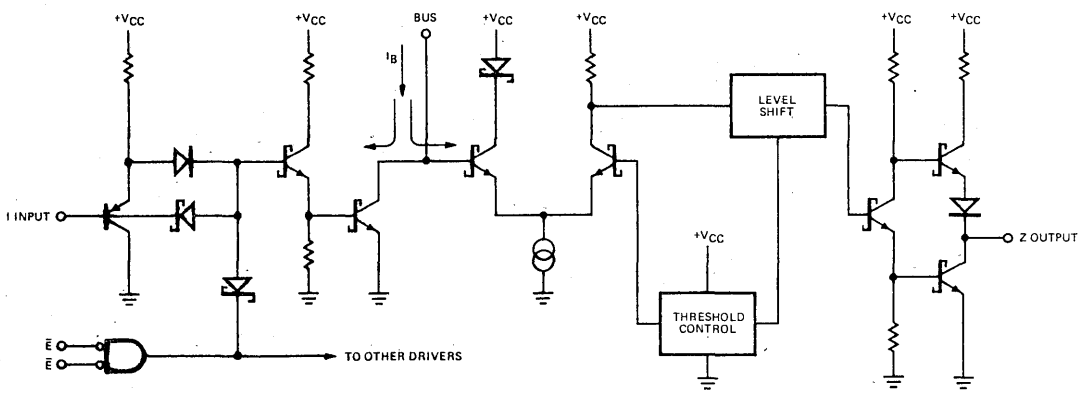


Figure 5

Am26S12/26S12A APPLICATION

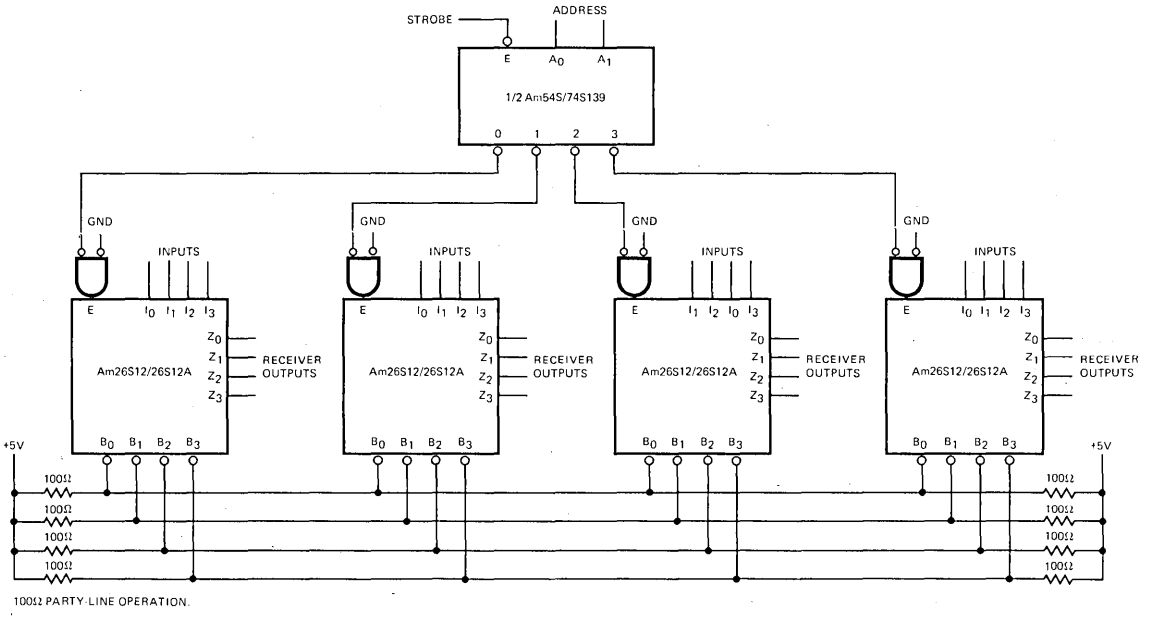
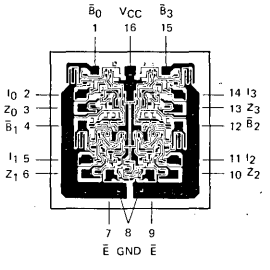


Figure 6

Metallization and Pad Layout



DIE SIZE: 0.071" x 0.072"

Am2614

Quad Single-Ended Line Driver

Distinctive Characteristics

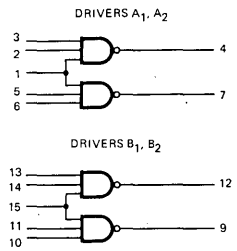
- Quad single-ended driver for multi-channel common ground operation
- Single 5V power supply
- DTL, TTL compatible
- Short-circuit protected outputs
- Capable of driving 50Ω terminated transmission lines
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2614 is a DTL, TTL compatible line driver operating off a single 5V supply. The Am2614 is a quad inverting driver with two separate inputs and one common-strobe input for each pair of drivers. The device has active pull-up outputs for high-speed and HIGH capacitance drive. The Am2614 is ideal for single-ended transmission line driving, or as a high-speed, high-fan-out driver for semiconductor memory decoding, buffering, clock driving and general logic use.

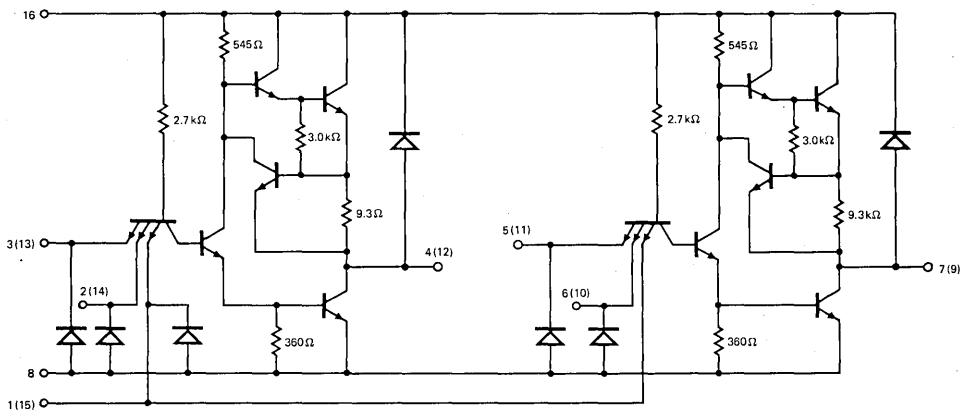
The Am2614 has short circuit protected active pull-ups, and incorporates input clamp diodes to reduce the effect of line transients, and also is capable of driving 50Ω terminated transmission lines.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

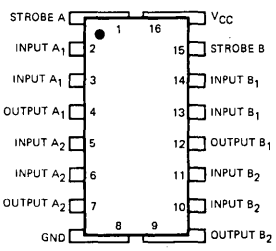
CIRCUIT DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM2614DM
Flat Pak	−55°C to +125°C	AM2614FM
Dice	−55°C to +125°C	AM2614XM
Hermetic DIP	0°C to +70°C	AM2614DC
Molded DIP	0°C to +70°C	AM2614PC
Dice	0°C to +70°C	AM2614XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2614XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V
Am2614XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

DC Characteristics (Note 2)

Parameters	Description	Test Conditions		LIMITS T_A MIN. Min.	T_A MIN. Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_AMAX. Min.	T_AMAX. Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA	MIL		0.4		0.2	0.4		0.4	Volts
			COM'L		0.45		0.2	0.45		0.45	
V_{IH}	Input HIGH Voltage	V_{CC} = MIN.	MIL	2.0		1.7	1.5		1.4		Volts
			COM'L	1.9		1.8	1.5		1.6		
V_{IL}	Input LOW Voltage	V_{CC} = MAX.	MIL		0.8		1.3	0.9		0.8	Volts
			COM'L		0.85		1.3	0.85		0.85	
I_F	Input Load Current	V_{CC} = MAX.	V_F = 0.4V, MIL		−2.4		−1.65	−2.4		−2.4	mA
			V_F = 0.45V, COM'L								
I_R	Reverse Input Current	V_{CC} = MAX. V_R = 4.5V			90			90		90	μA
I_{SC}	Short Circuit Current	V_{CC} = MAX., V_O = 0V				−40	−90	−120			mA
I_{PD}	Power Supply Current	V_{CC} = MAX., Inputs = 0V			48.7		33	48.7		48.7	
		V_{CC} = 7.0V, Inputs = 0V	COM'L				46	70			
			MIL				46	65.7			
I_{CEX}	Reverse Output Current	V_{CC} = MAX.	V_{CEX} = 5.5V, MIL		100		10	100		200	μA
			V_{CEX} = 5.25V, COM'L		100		10	100		200	
V_{OLC}	Output Low Clamp Voltage	V_{CC} = MAX., I_{OLC} = −40mA					−0.8	−1.5			Volts
V_{IC}	Input Clamp Voltage	V_{CC} = MIN., I_{IC} = −12mA					−1.0	−1.5			Volts

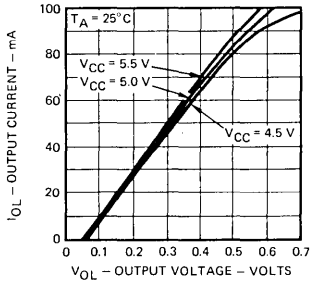
Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters	Description	Test Conditions	Am2614XM Min.	Am2614XM Typ.	Am2614XM Max.	Am2614XC Min.	Am2614XC Typ.	Am2614XC Max.	Units
t_{pd+}	Turn Off Delay	V_{CC} = 5.0V, C_L = 30pF, V_M = 1.5V, Refer to Fig. 92		8	12		8	15	ns
t_{pd-}	Turn On Delay			7	10		7	12	ns

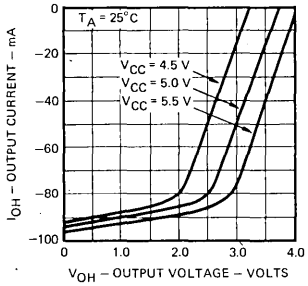
Notes: 1. Maximum current defined by DC input voltage.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type or grade.

TYPICAL ELECTRICAL CHARACTERISTICS

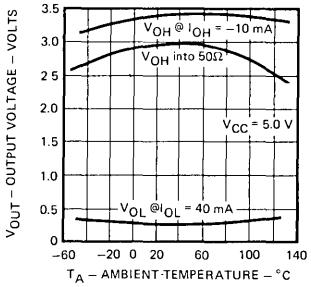
Output Low Current Versus Output Low Voltage



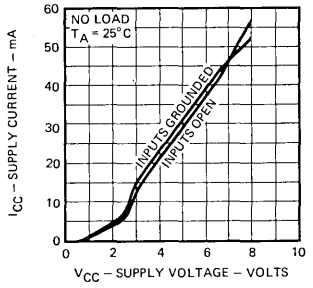
Output High Current Versus Output High Voltage



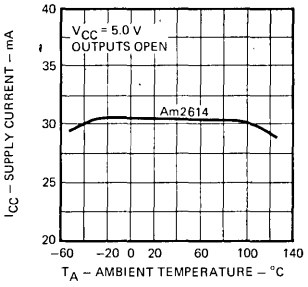
Logic Levels Versus Ambient Temperature



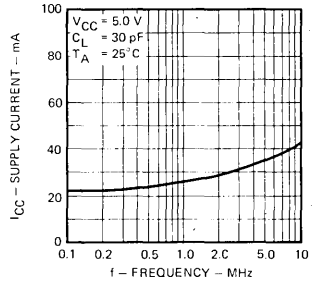
Supply Current Versus Supply Voltage



Supply Current Versus Temperature



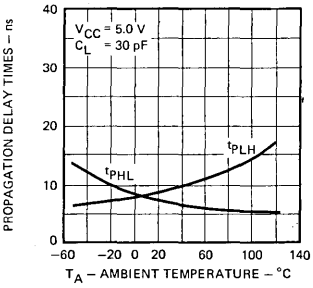
Supply Current Versus Operating Frequency



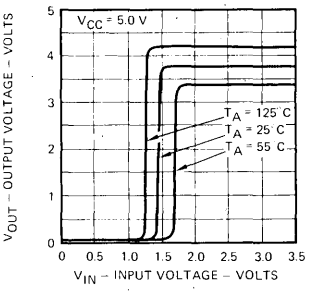
4

TYPICAL ELECTRICAL CHARACTERISTICS

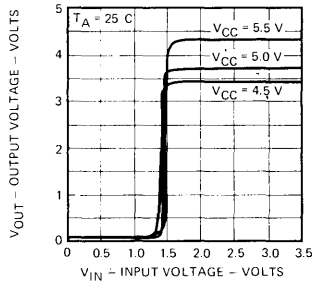
Propagation Delay Time Versus Temperature



Transfer Characteristics Versus Temperature



Transfer Characteristics Versus Supply Voltage



USER NOTES

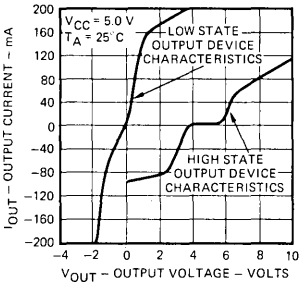
SINGLE ENDED LINES. The Am2614 quad line driver and the Am2615 dual differential amplifier allow data to be transmitted with only a single data wire per channel and a common ground for typically 8 data wires. This single-ended mode of interconnection offers considerable savings in integrated circuit packages required and effectively halves the number of interconnections as compared to a balanced differential system. The method still gives ±15V common mode rejection and DC noise margin of interconnected TTL logic. The common ground wire should be twisted in with the data wires so that any injected noise is common to all wires. If a multiwire cable with screen is used one of the wires is used as the common ground line, and the screen is tied to ground at the driving end only.

MATCHING. Transmission lines can be matched in a number of ways. The most widely used method is to terminate the line at the receiving end in its characteristic impedance. This impedance is connected across the input terminals of the receiver. A 130Ω resistor is included at the + input of each receiver for matching twisted pairs and this resistor, or if the characteristic impedance is not 130Ω, a discrete resistor is connected between the two receiver inputs. This method of matching causes a DC component in the signal. Power is dissipated in the resistor and the signal is attenuated. The DC component can be effectively removed by connecting a large capacitor in series with the terminating resistor.

The transmission line can also be terminated through the receiver power supply by placing equal value resistors from the + input of the receiver to V_{CC} and from the – input to ground. This method again has the disadvantage that a DC signal component exists, attenuation occurs, and power is dissipated in the terminating resistors but it does allow multiplexed operation in the balanced differential mode.

An alternate method of matching at the receiver is to back match at the driver. A resistor is placed in series with the line so that the signal from the driver which is reflected at the high input impedance of the receiver is absorbed at the driver. This method does not have a DC component and therefore no attenuation occurs and power is not dissipated in the resistor. For balanced differential driving a resistor is required in series with each line. The table below shows the value of each matching resistor required for lines of different characteristic impedance.

TYPICAL DC CHARACTERISTICS
FOR MATCHING TO TRANSMISSION LINE



BACK MATCHING TABLE

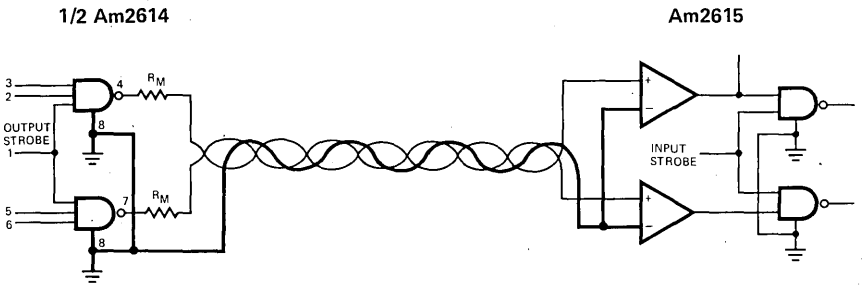
	R_M (ohms)
Z_O	SINGLE ENDED
50	24
75	51
92	68
100	75
130	110
300	280
600	580

LOADING RULES

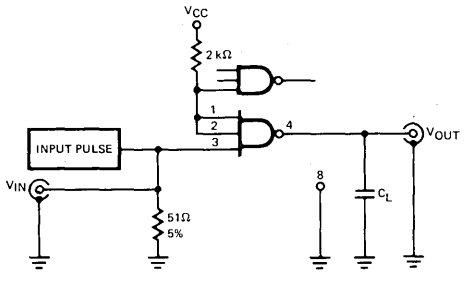
			Fanout	
Input/Output	Pin No.'s	Input Unit Load	Output HIGH	Output LOW
Strobe A	1	3	—	—
Input A_1	2	1.5	—	—
Input A_1	3	1.5	—	—
Output A_1	4	—	166	25
Input A_2	5	1.5	—	—
Input A_2	6	1.5	—	—
Output A_2	7	—	166	25
GND	8	—	—	—
Output B_2	9	—	166	25
Input B_2	10	1.5	—	—
Input B_2	11	1.5	—	—
Output B_2	12	—	166	25
Input B_1	13	1.5	—	—
Input B_1	14	1.5	—	—
Strobe B	15	3	—	—
V_{CC}	16	—	—	—

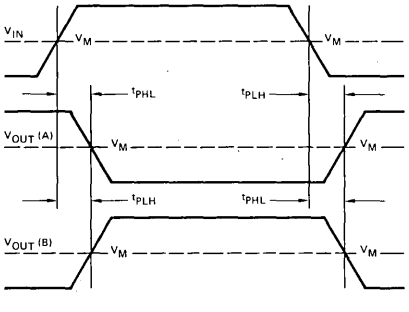
APPLICATIONS

Single-Ended Back-Matched Operation With Common Ground



SWITCHING CIRCUITS AND WAVEFORMS





INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

Am2615/9615

Dual Differential Line Receivers

Distinctive Characteristics:

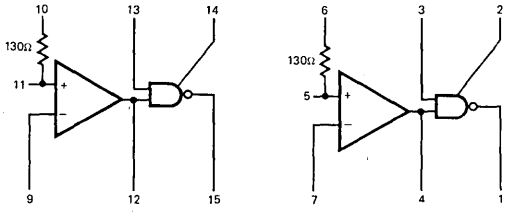
- Dual differential receiver (Am9615) pin-for-pin equivalent to the Fairchild 9615
- Dual differential receiver for single-ended data (Am2615)
- Single 5-volt supply
- High common-mode voltage range (±15 volts)
- Frequency response control, strobe, and internal terminating resistor
- Am2615 has fail safe capability
- Choice of uncommitted collector or active pull-up outputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2615 and Am9615 are dual differential line receivers designed to receive digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. The Am2615 can receive 3 volt single ended and the Am9615 ±500 mV differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed logic levels to the following DTL or TTL circuitry. The response time of each receiver and thereby immunity to AC noise can be controlled by an external capacitor. A strobe is provided for each receiver together with a 130Ω input terminating resistor. Each output has an uncommitted collector with an active pull-up network available on an adjacent pin.

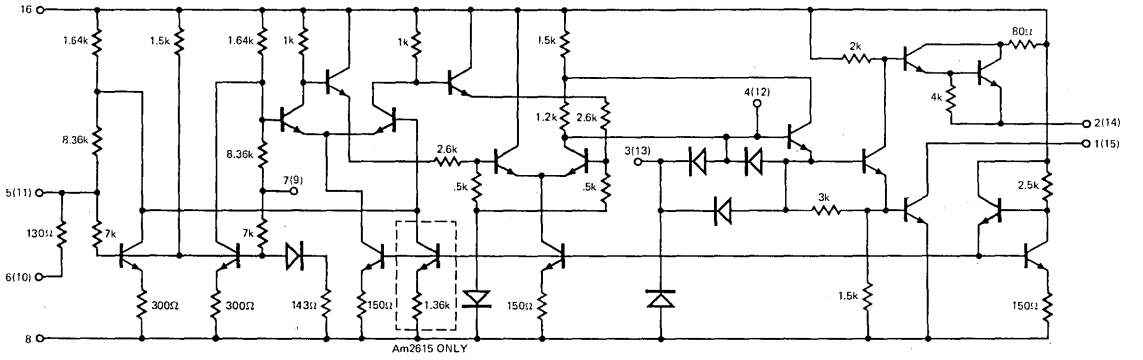
The Am2615 is identical to the Am9615 except for the input offset (threshold) voltage. The Am2615 has an input threshold of ~1.5 V compatible with DTL & TTL logic. The Am9615 has an input threshold of ~0 V. The Am2615 can directly replace the Am9615 and give fail safe protection in differential systems where the input difference is >2.0 V.

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

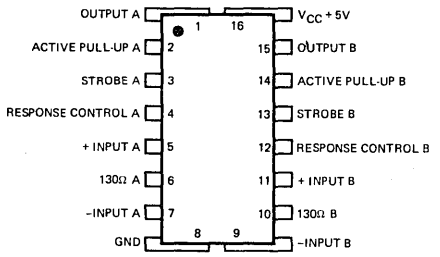
CIRCUIT DIAGRAM



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2615	Hermetic DIP	−55°C to +125°C	AM2615DM
	Flat Pak	−55°C to +125°C	AM2615FM
	Dice	−55°C to +125°C	AM2615XM
	Hermetic DIP	0°C to +75°C	AM2615DC
	Molded DIP	0°C to +75°C	AM2615PC
	Dice	0°C to +75°C	AM2615XC
Am9615	Hermetic DIP	−55°C to +125°C	9615DM
	Flat Pak	−55°C to +125°C	9615FM
	Dice	−55°C to +125°C	AM9615XM
	Hermetic DIP	0°C to +75°C	9615DC
	Molded DIP	0°C to +75°C	9615PC
	Dice	0°C to +75°C	AM9615XC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
DC Strobe Input Voltage	−0.5 V to +5.5 V
DC Data Input Voltage	−20 V to + 20 V
Output Current, Into Outputs	30 mA
DC Input Current	maximum current is defined by DC Input Voltage

Am2615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am2615XM V_{CC} = 4.5V to 5.5V T_A = −55°C to +125°C (MIL grade)
Am2615XC V_{CC} = 4.75V to 5.25V T_A = 0°C to +75°C (COM'L grade)

Parameters	Description	Test Conditions		LIMITS T_A = Min Min	Max	T_A = 25°C Min	Typ	Max	T_A = Max Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA V_{IN+} = +0.8 V, V_{IN-} = 0 V		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX I_{OH} = 15.0 mA V_{IN+} = +2.0 V, V_{IN-} = 0 V	MIL grade		0.40		.18	0.40		0.40	Volts
			COM'L grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN V_{IN+} = 0 V V_{IN-} = 4.5 V	V_{CEX} = 12 V V_{CEX} = 5.25 V	MIL grade COM'L grade	100			100		200	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX V_{OUT} = 0 V V_{IN+} = +0.8 V V_{IN-} = 0 V		MIL grade	−15 −80	−15	−39	−80	−15	−80	mA
				COM'L grade	−14 −100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}			−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{ST} = V_{OL} MAX V_{IN-} = 0 V			−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{RC} = V_{OL} MAX V_{IN-} = 0 V					−1.2	−3.4			mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V V_{IN+} - V_{IN-} = 0.4 or 2.4 V		−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN V_{ST} = 4.5 V V_{IN+} = +0.8 V V_{IN-} = 0 V	MIL grade					2.0		5.0	μA
			COM'L grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V V_{IN+} = 0 V V_{RES} = 1.0 V	MIL grade			77	130	167			Ω
			COM'L grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V		+0.8	+2.0	+0.8	+1.5	+2.0	+0.8	+2.0	V
I_{CC}	Power Supply Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{IN-} = 0 V	MIL grade		50		28.7	50		50	mA
			COM'L grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

Parameters	Test Conditions	Am2615XM Min	Typ	Max	Am2615XC Min	Typ	Max	Units
t_{pd+} Turn Off Delay R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-} Turn On Delay R_L = 390 Ω			30	50		30	75	
t_{pd+} Turn Off Delay Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-} Turn On Delay Strobe to Output	R_L = 390 Ω		10	15		10	20	

Am9615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9615XM V_{CC} = 4.5V to 5.5V T_A = −55°C to +125°C (MIL grade)
Am9615XC V_{CC} = 4.75V to 5.25V T_A = 0°C to +75°C (COM'L grade)

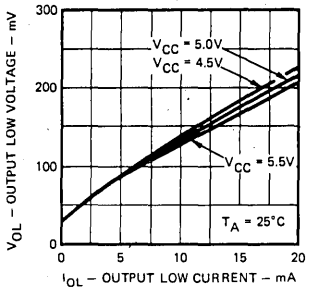
Parameters	Description	Test Conditions		LIMITS T_A = Min Min	Max	T_A = 25°C Min	Typ	Max	T_A = Max Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA V_{IN+} = −0.5 V, V_{IN-} = 0 V		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX I_{OH} = 15.0 mA V_{IN+} = +0.5 V, V_{IN-} = 0	MIL grade		0.40		.18	0.40		0.40	Volts
			COM'L grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN V_{IN+} = 0 V V_{IN-} = V_{CC}	V_{CEX} = 12 V, MIL grade V_{CEX} = 5.25 V, COM'L grade		100			100		200	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX V_{OUT} = 0 V V_{IN+} = −0.5 V V_{IN-} = 0 V	MIL grade	−15	−80	−15	−39	−80	−15	−80	mA
			COM'L grade	−14	−100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}			−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{ST} = $V_{OL\ MAX}$	V_{IN+} = +0.5 V V_{IN-} = 0 V		−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{RC} = $V_{OL\ MAX}$	V_{IN+} = +0.5 V V_{IN-} = 0 V				−1.2	−3.4			mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V	V_{IN+} - V_{IN-} = ±2.0 V	−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN V_{ST} = 4.5 V V_{IN+} = −0.5 V V_{IN-} = 0 V	MIL grade					2.0		5.0	μA
			COM'L grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V V_{IN+} = 0 V V_{RES} = 1.0 V	MIL grade			77	130	167			Ω
			COM'L grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V		−0.5	+0.5	−0.5	±0.02	+0.5	−0.5	+0.5	V
I_{CC}	Power Supply Current	V_{CC} = MAX V_{IN+} = +0.5 V V_{IN-} = 0 V	MIL grade		50		28.7	50		50	mA
			COM'L grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

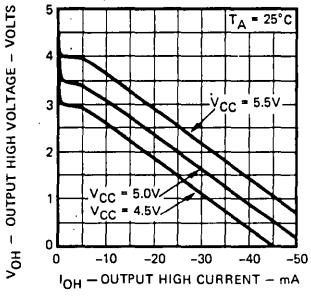
Parameters	Test Conditions	Am9615XM Min	Typ	Max	Am9615XC Min	Typ	Max	Units
t_{pd+} Turn Off Delay R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-} Turn On Delay R_L = 390 Ω			30	50		30	75	
t_{pd+} Turn Off Delay Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-} Turn On Delay Strobe to Output	R_L = 390 Ω		10	15		10	20	

D. C. CHARACTERISTICS

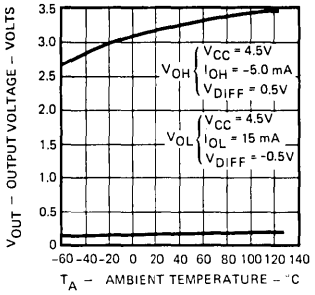
Output Low Voltage Versus Output Low Current



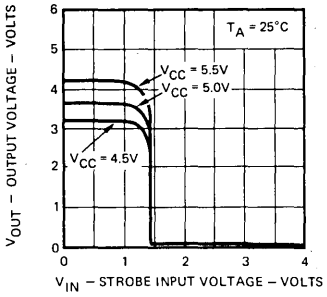
Output High Voltage Versus Output High Current



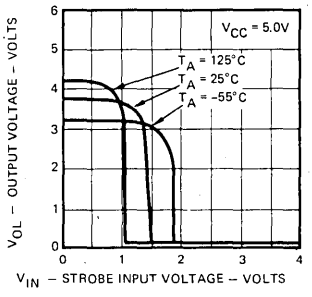
Output Voltage Versus Ambient Temperature



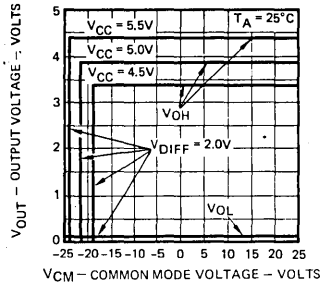
Strobe Input-Output Transfer Characteristic Versus V_{CC}



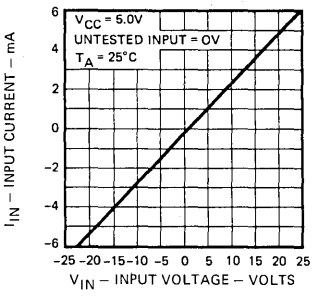
Strobe Input-Output Transfer Characteristic Versus Ambient Temperature



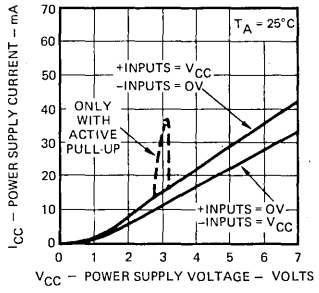
Output Voltage Versus Common Mode Voltage (Am9615)



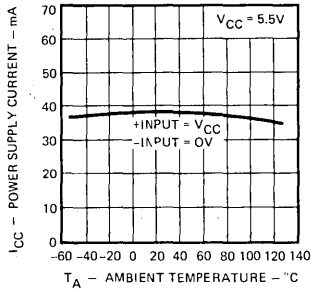
Input Current Versus Input Voltage



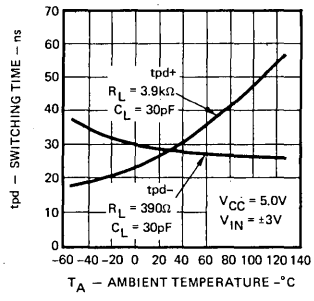
Power Supply Current Versus Power Supply Voltage



Power Supply Current Versus Ambient Temperature



Switching Time Versus Ambient Temperature

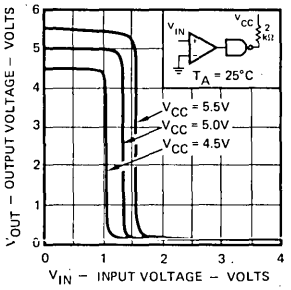


4

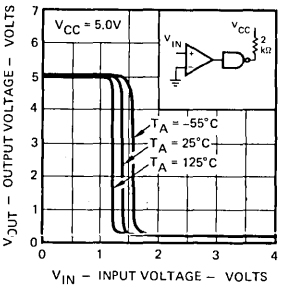
THRESHOLD CHARACTERISTICS

Am2615

Input-Output Transfer Characteristic Versus V_{CC}

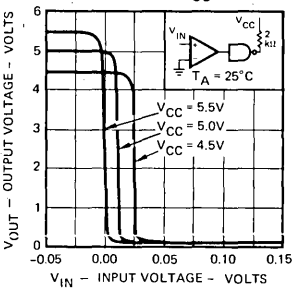


Input-Output Transfer Characteristic Versus Temperature

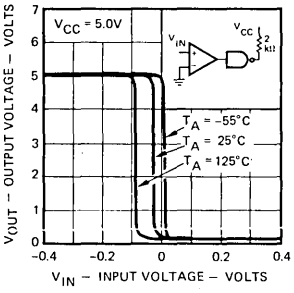


Am9615

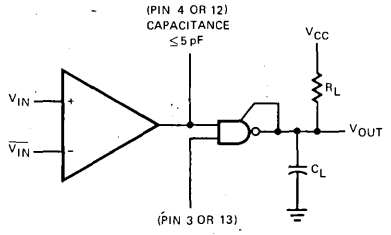
Input-Output Transfer Characteristic Versus V_{CC}



Input-Output Transfer Characteristic Versus Temperature



SWITCHING TIME TEST CIRCUIT & WAVEFORMS



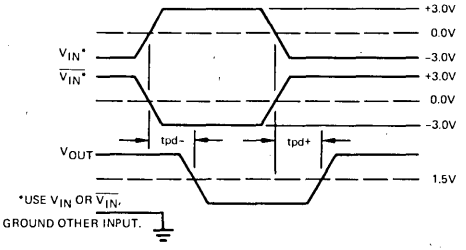
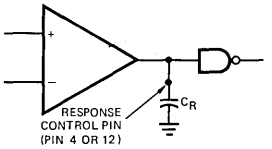
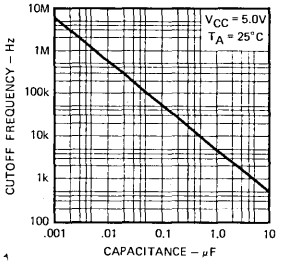


Figure 4

FREQUENCY RESPONSE CONTROL



Frequency Response Versus Capacitance

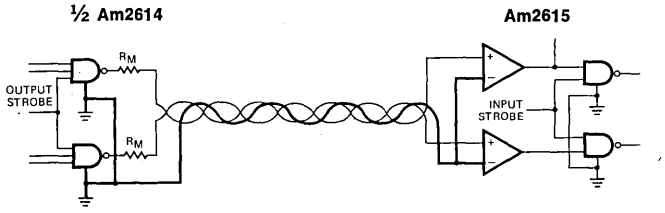


Am2615/9615 LOADING RULES

	Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Receiver A	Out	1	—	o/c	10
	Active Pull-Up	2	—	83	—
	Response Control	3	—	—	—
	Strobe	4	1.5	—	—
	+ In	5	0.5	—	—
	130 Ω	6	—	—	—
	– In	7	0.5	—	—
Receiver B	GND	8	—	—	—
	– In	9	0.5	—	—
	130 Ω	10	—	—	—
	+ In	11	0.5	—	—
	Response Control	12	—	—	—
	Strobe	13	1.5	—	—
	Active Pull-Up	14	—	83	—
	Out	15	—	o/c	10
	V_{CC}	16	—	—	—

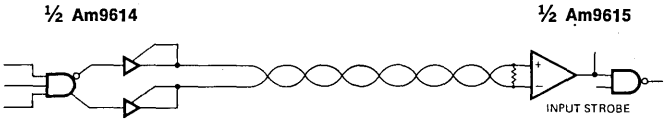
Am2615 STANDARD USAGE

Single-Ended-Back Matched Operation With Common Ground

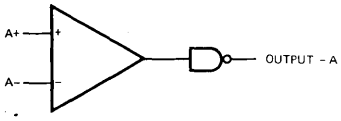


Am9615 STANDARD USAGE

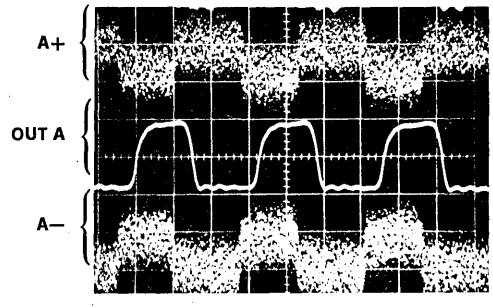
Differential Operation



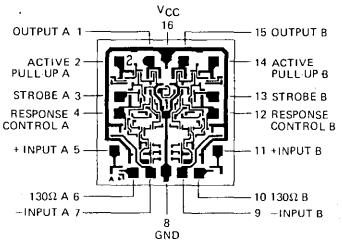
Photograph of an Am9615 switching differential data in the presence of high common mode noise.



Vertical = 2.0 V/Div. Horizontal = 50 ns/Div.



Metallization and Pad Layout



53 X 58 Mils

Am2616

Quad MIL-188C and RS-232C Line Driver

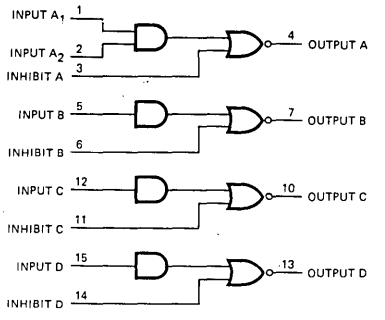
Distinctive Characteristics

- Conforms to EIA RS-232C, CCITT V.24 and MIL-188C specifications
- Short circuit protected output
- Internal slew rate limiting
- Supply independent output swing
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL/DTL compatible input

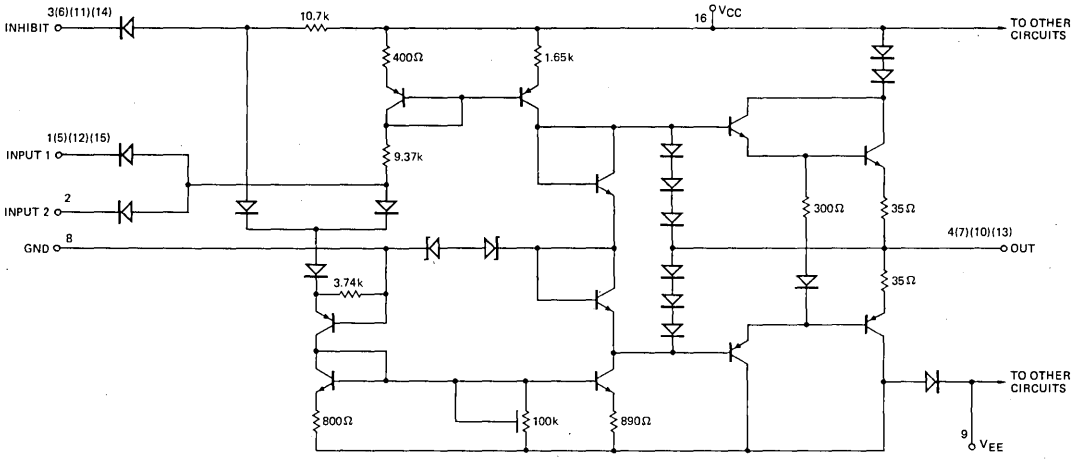
FUNCTIONAL DESCRIPTION

The Am2616 is a quad line driver specifically designed to meet the EIA RS-232C, CCITT V.24 and MIL-188C interface requirements. Each driver accepts DTL/TTL logic levels and converts them to the requisite levels for data transmission between equipment. The output slew rate of each driver is internally limited, but can be lowered by an external capacitor. All outputs are short circuit protected, and protected against fault conditions specified in RS-232C. A HIGH logic level on the inhibit input forces the driver output to V_{OL} or mark state. For 188C interface the output impedance is guaranteed to be less than 100 ohms and the positive and negative output voltage amplitudes are guaranteed to be within 10 percent of each other.

LOGIC SYMBOL



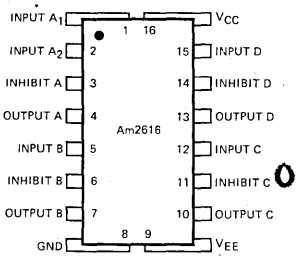
CIRCUIT DIAGRAM
(One Driver Shown)



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	AM2616DC
Molded DIP	0°C to +75°C	AM2616PC
Dice	0°C to +75°C	AM2616XC
Hermetic DIP	−55°C to +125°C	AM2616DM
Flat Pack	−55°C to +125°C	AM2616FM
Dice	−55°C to +125°C	AM2616XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	+15 V
V_{EE}	−15 V
DC Voltage Applied to Outputs	±15 V
DC Input Voltage	−1.5 V to +6 V
Lead Temperature (Soldering, 30 sec.)	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(COM'L) T_A = 0°C to +75°C
(MIL) T_A = −55°C to +125°C

V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, R_L = 3 kΩ unless otherwise noted

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Note 2)	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V	+5.0	+6.0	+7.0	Volts
V_{OL}	Output LOW Voltage (Note 2)	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V	−7.0	−6.0	−5.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage			0.8	Volts
I_{IL}	Input LOW Current	$V_{IN_1} = V_{IN_2}$ = 0.4 V or $V_{INHIBIT}$ = 0.4 V		−1.2	−1.6	mA
I_{IH}	Input HIGH Current	$V_{IN_1} = V_{IN_2}$ = 2.4 V or $V_{INHIBIT}$ = 2.4 V			40	μA
I_{SC}	Output Short Circuit Current (Positive) (Note 3)	R_L = 0 Ω V_{IN_1} or $V_{IN_2} = V_{INHIBIT}$ = 0.8 V	−10	−17	−30	mA
I_{SE}	Output Short Circuit Current (Negative) (Note 3)	R_L = 0 Ω V_{IN_1} or $V_{IN_2} = V_{INHIBIT}$ = 2.0 V	+10	+17	+30	mA
I_{CC}	Total Positive Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V		19	28	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V		9.5	17	
I_{EE}	Total Negative Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V		0	−2	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V		−20	−30	

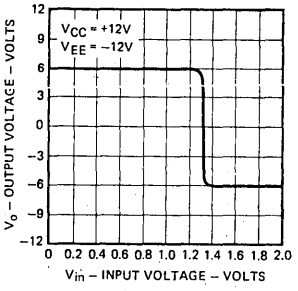
Notes: 1. Typical values are at V_{CC} = 12 V, V_{EE} = −12 V, T_A = 25°C.
2. V_{OH} and V_{OL} are guaranteed to be equal within ±10 percent of each other for MIL-188C operation. (i.e., V_{OH} = 6.0V then V_{OL} = −6.0V ±0.6V).
3. The I_{SC} and I_{SE} minimum limits guarantee the output impedance to be less than 100 ohms.

Switching Characteristics (T_A = 25°C, V_{CC} = +12.0 V, V_{EE} = −12.0 V)

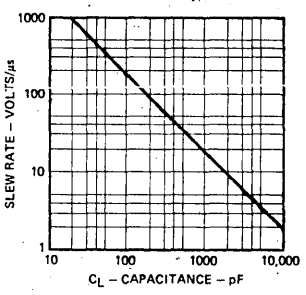
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	C_L = 15 pF, R_L = ∞		320	650	ns
t_{PHL}	Delay from Input HIGH to Output LOW			320	650	ns
dV/dt (+)	Positive Slew Rate	0 pF ≤ C_L ≤ 2500 pF, R_L ≥ 3 kΩ	4.0	15	30	V/μs
dV/dt(−)	Negative Slew Rate		−30	−15	−4.0	V/μs

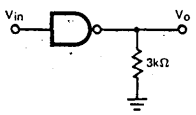
TYPICAL CHARACTERISTICS

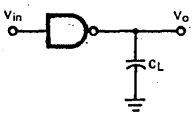
Transfer Characteristics



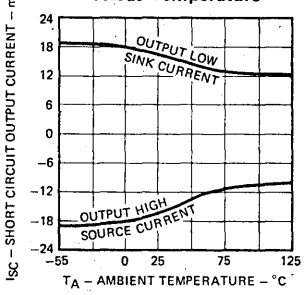
Output Slew Rate versus Load Capacitance



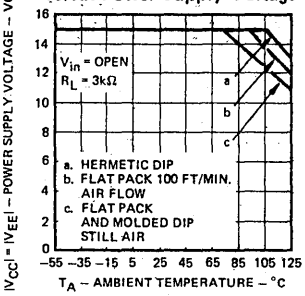




Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage



DEFINITION OF TERMS

FUNCTIONAL TERMS

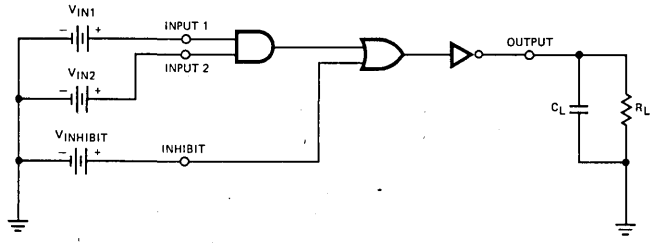
RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

R_L Load resistance. The DC resistance between the driver output and ground.

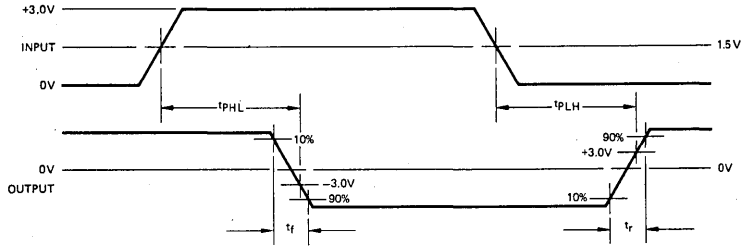
MIL-188C A Military specification that defines the electrical interface and characteristics of data signals transmitted between two pieces of digital equipment.

CCITT V.24 A European specification similar to the MIL-188C and RS-232 specifications.

SWITCHING TEST CIRCUIT & VOLTAGE WAVEFORMS

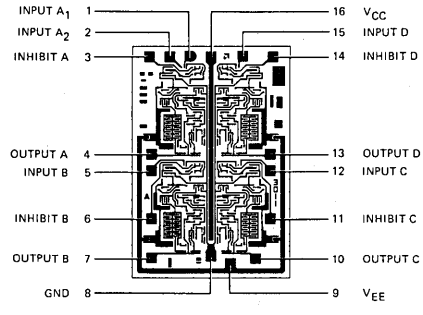


Note: Omit V_{IN2} for channels B, C and D.



Pulse Generator Rise Time = 10 ± 5ns.

Metallization and Pad Layout



DIE SIZE
0.069" X 0.103"

Am2617

Quad RS-232C Line Receiver

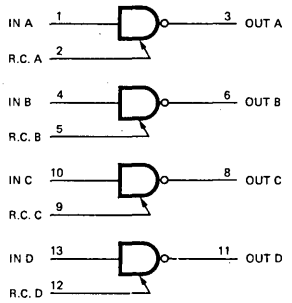
Distinctive Characteristics

- Full military temperature range
- Compatible with EIA specification RS-232C
- Input signal range ± 30 volts
- Guaranteed input thresholds over full military temperature range
- 100% reliability assurance testing in compliance with MIL-STD-883
- Includes response control input and built-in hysterisis

FUNCTIONAL DESCRIPTION

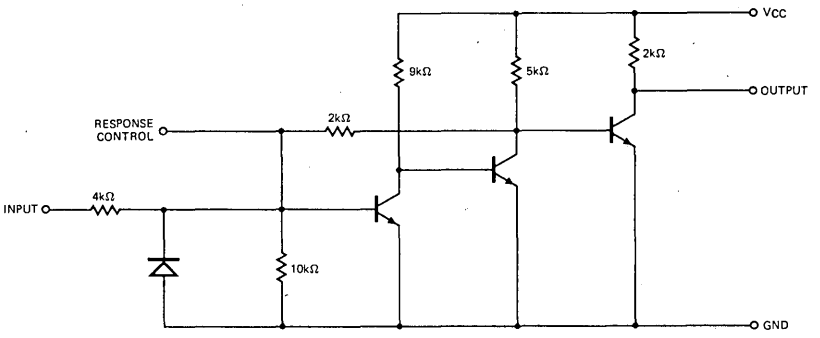
The Am2617 is a quad line receiver whose electrical characteristics conform to EIA specification RS-232C. Each receiver has a single data input that can accept signal swings of up to ±30V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. An internal feedback resistor causes the input to exhibit hysterisis so that AC noise immunity is maintained at a high level even near the switching thresholds. For example, at 25°C when a receiver is in a LOW state on the output, the input may drop as LOW as 1.25 volts without affecting the output. The device is guaranteed to switch to the HIGH state when the input voltage is below 0.75V. Once the output has switched to the HIGH state, the input may rise to 1.75V without causing a change in the output. The Am2617 is guaranteed to switch to a LOW output when its input reaches 2.25V. Because of this hysterisis in switching thresholds, the device can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am2616.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

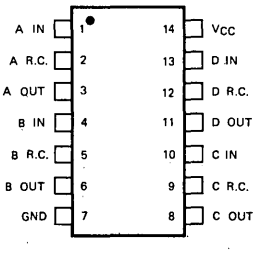
CIRCUIT DIAGRAM
(One Receiver)



ORDERING INFORMATION

	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM2617PC
Hermetic DIP	0°C to +75°C	AM2617DC
Dice	0°C to +75°C	AM2617XC
Hermetic DIP	−55°C to +125°C	AM2617DM
Hermetic Flat Pack	−55°C to +125°C	AM2617FM
Dice	−55°C to +125°C	AM2617XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +10 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%
T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%
} Response control pin open.

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5 mA, V_{IN} = 0.4 V or open	2.4	4.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA, V_{IN} = 3.0 V		0.2	0.45	Volts
I_{IL}	Input LOW Current	V_{IN} = −3.0 V	−0.43			mA
		V_{IN} = −25 V	−3.6		−8.3	
I_{IH}	Input HIGH Current	V_{IN} = +3.0 V	0.43			mA
		V_{IN} = +25 V	3.6		8.3	
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0 V, V_{OUT} = 0.0 V	1.9	2.5	3.8	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		20	26	mA

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

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Threshold Characteristics (Note 2)

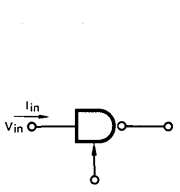
Parameters	Description	Test Conditions	T_A	Min.	Typ. (Note 1)	Max.	Units
V_{T+}	Positive-Going Threshold Voltage	V_{OL} = 0.45V, V_{CC} = 5.0V	−55°C	2.3		3.1	Volts
			0°C	1.9		2.5	
			25°C	1.75	2.0	2.25	
			75°C	1.45		1.90	
			125°C	1.20		1.65	
V_{T-}	Negative-Going Threshold Voltage	V_{OH} = 2.5V, V_{CC} = 5.0V	−55°C	0.85		1.65	Volts
			0°C	0.75		1.40	
			25°C	0.75	0.95	1.25	
			75°C	0.60		1.10	
			125°C	0.50		0.95	

Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. The input threshold margin for the device is greater than the voltage computed as the $V_{T+}-V_{T-}$ value. For the minimum value see the input threshold margin versus temperature graph.

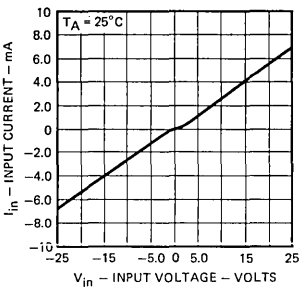
Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Delay from Input HIGH to Output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		10	20	ns

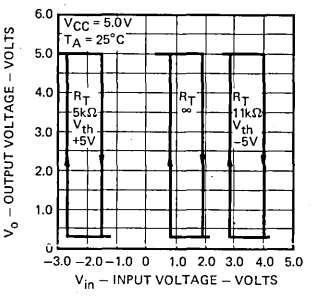
TYPICAL CHARACTERISTICS

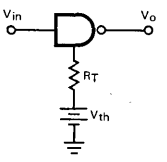


Input Current

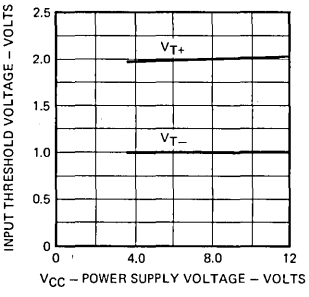


Input Threshold Voltage Adjustment

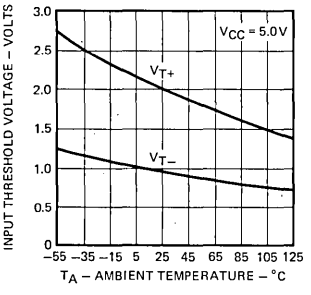




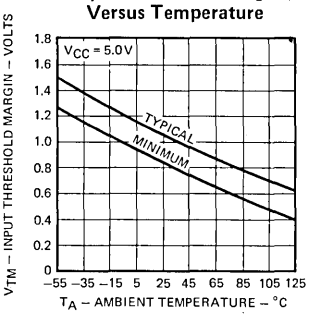
Input Threshold Versus Power-Supply Voltage



Input Threshold Voltage Versus Temperature



Input Threshold Margin Versus Temperature



DEFINITION OF TERMS

FUNCTIONAL TERMS

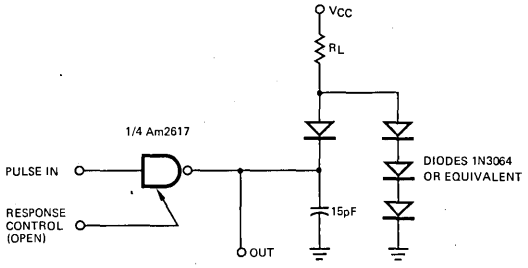
Response Control Pin A pin available on each receiver that allows the user to set the switching thresholds and frequency response of the receiver.

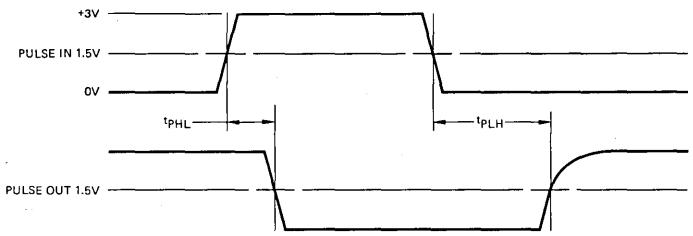
Threshold Voltage The voltage level on the input that will cause the output to change state. Because the device exhibits hysterisis, the LOW level input threshold is different from the HIGH level input threshold. Both thresholds can be moved by applying a bias to the response control pin.

RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

Input Signal Range The permitted range of DC voltages that can be applied to the receiver input without damage to the device.

SWITCHING TIME TEST CIRCUIT & WAVEFORMS





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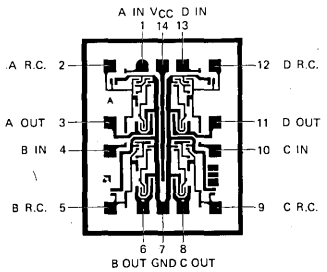
Metallization and Pad Layout



DIE SIZE 0.047" X 0.059"

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

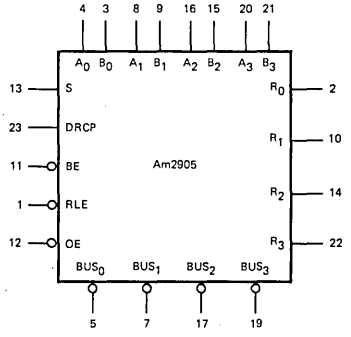
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

ORDERING INFORMATION

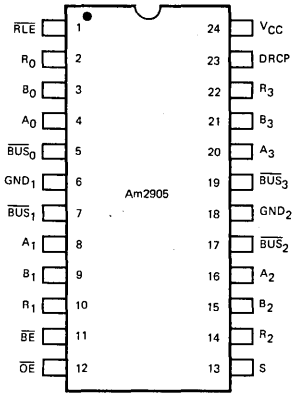
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2905PC
Hermetic DIP	0°C to +70°C	AM2905DC
Dice	0°C to +70°C	AM2905XC
Hermetic DIP	–55°C to +125°C	AM2905DM
Hermetic Flat Pak	–55°C to +125°C	AM2905FM
Dice	–55°C to +125°C	AM2905XM

LOGIC SYMBOL



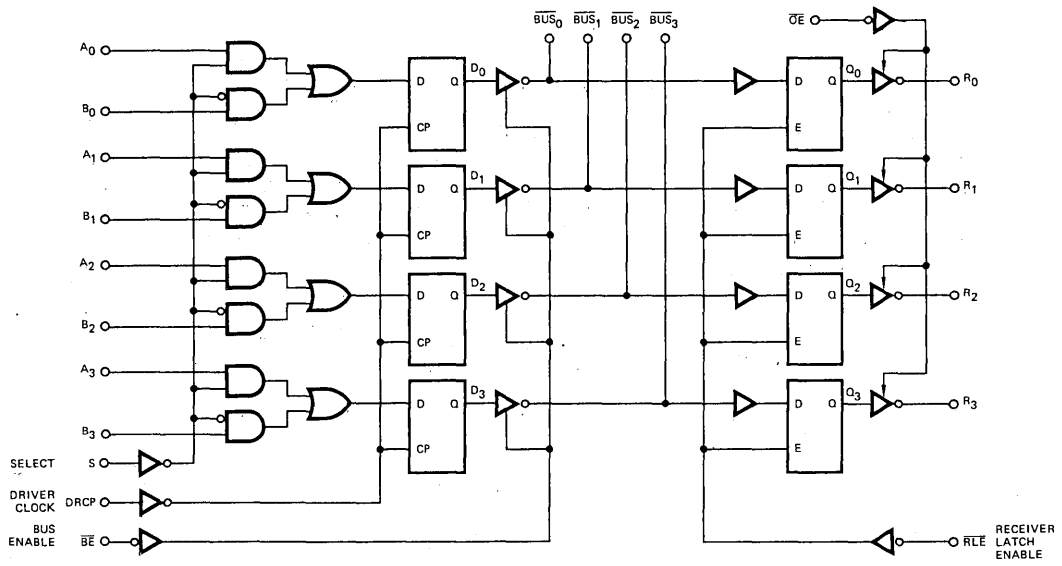
V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

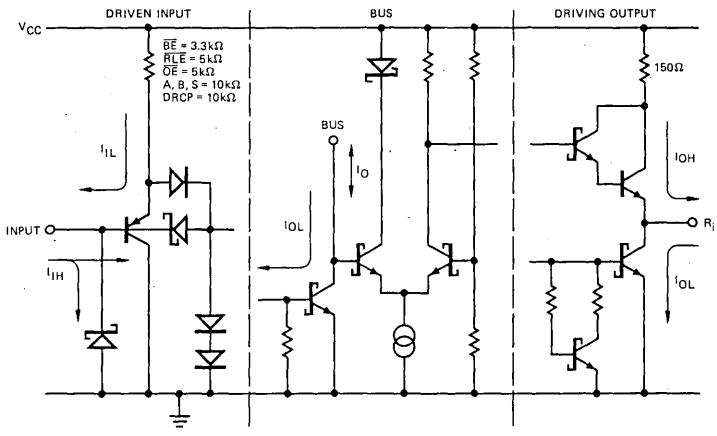
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA		2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA					−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V					20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V					100	µA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.		$V_O = 2.4$V			20	µA
				$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	$C_L = 15$pF, $R_L = 2.0$kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

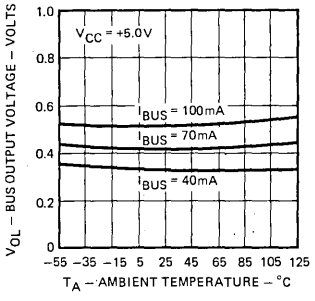
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



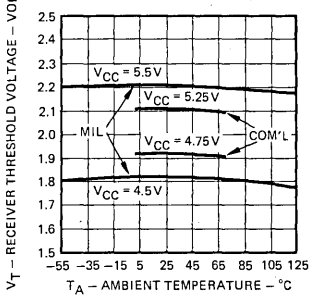
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

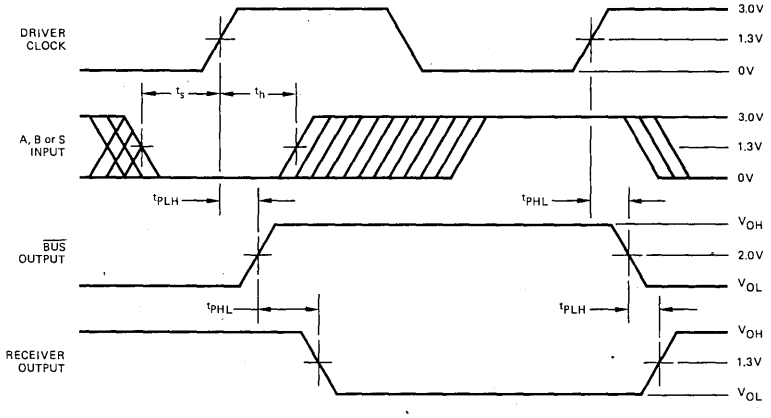
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 — The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 — The "B" word data input into the two input multiplexers of the driver register.

S — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

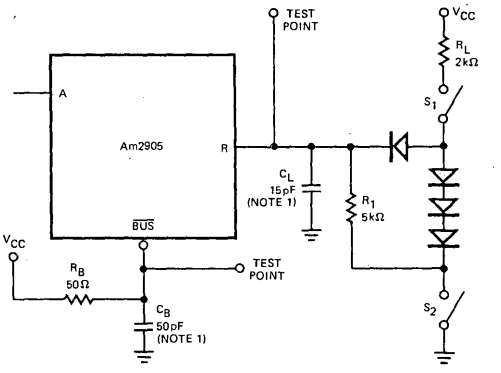
$\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$ — The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

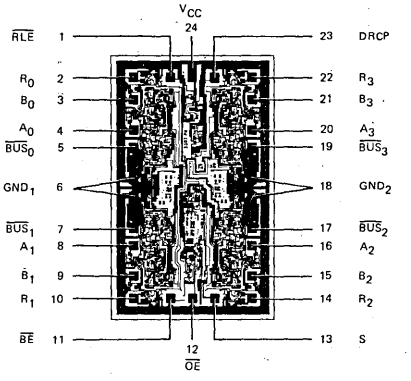
$\overline{RLE}$ — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

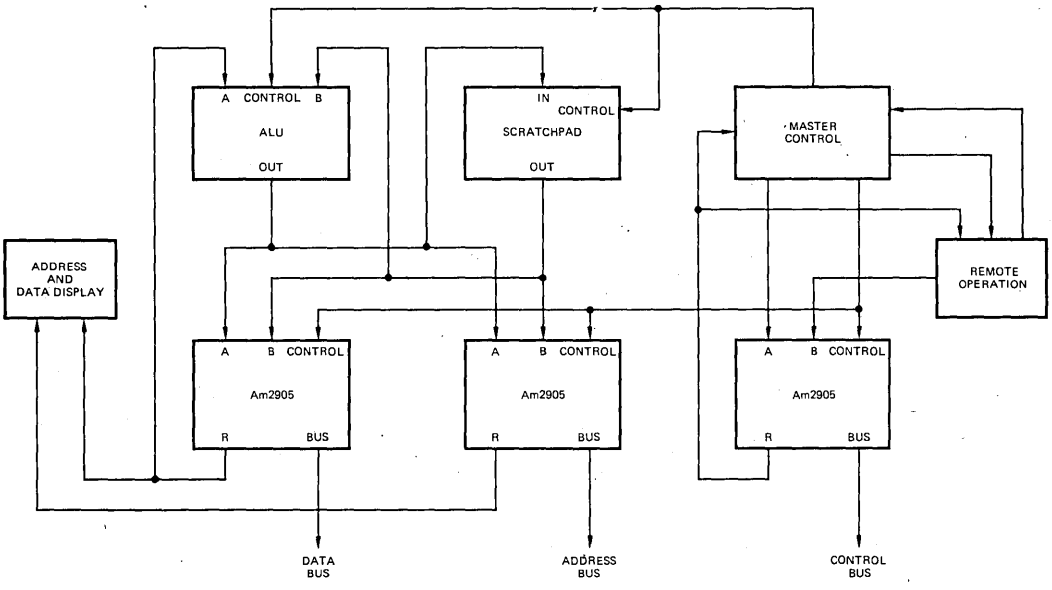


Metallization and Pad Layout

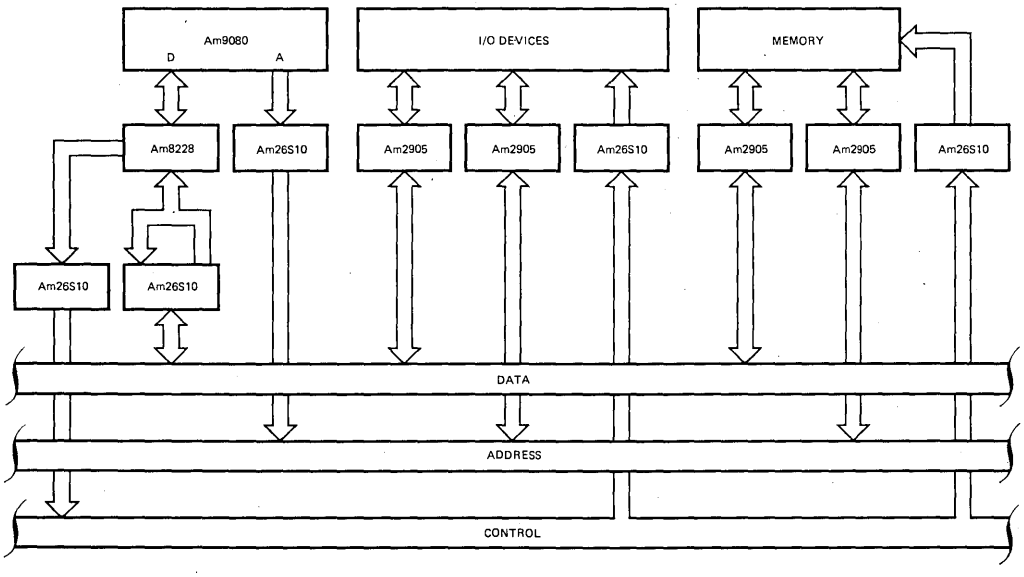


DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.



Using the Am2905 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
$\overline{BUS}_0$	5	–	OC	BUS
GND_1	6	–	–	–
$\overline{BUS}_1$	7	–	OC	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
$\overline{OE}$	12	1	–	–
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
$\overline{BUS}_2$	17	–	OC	BUS
GND_2	18	–	–	–
$\overline{BUS}_3$	19	–	OC	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

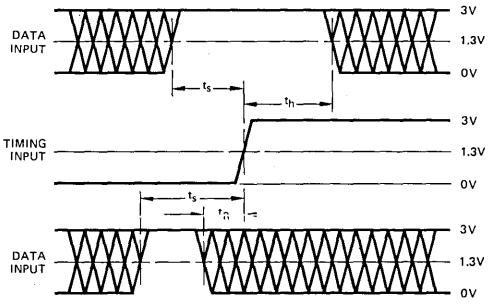
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

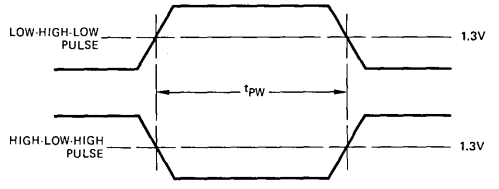
PARAMETERS MEASUREMENTS

SET-UP, HOLD, AND RELEASE TIMES

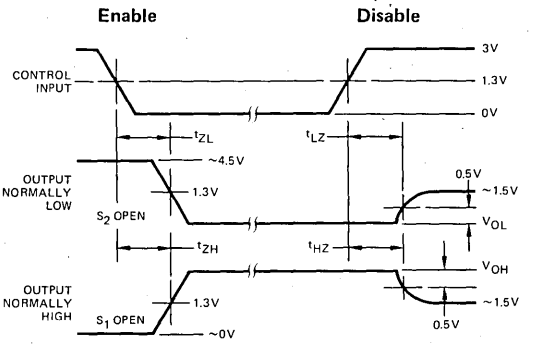


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 6.0ns; t_f ≤ 9.0ns.

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

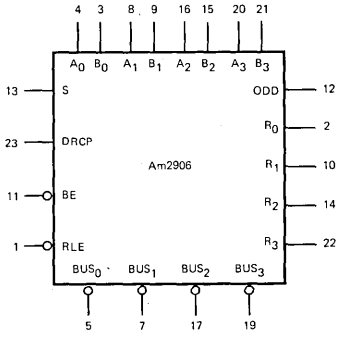
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

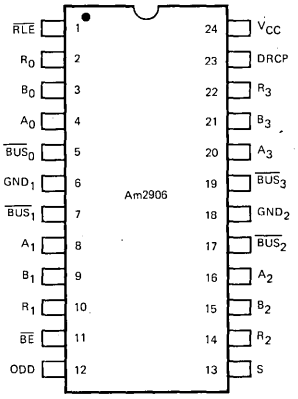
The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View

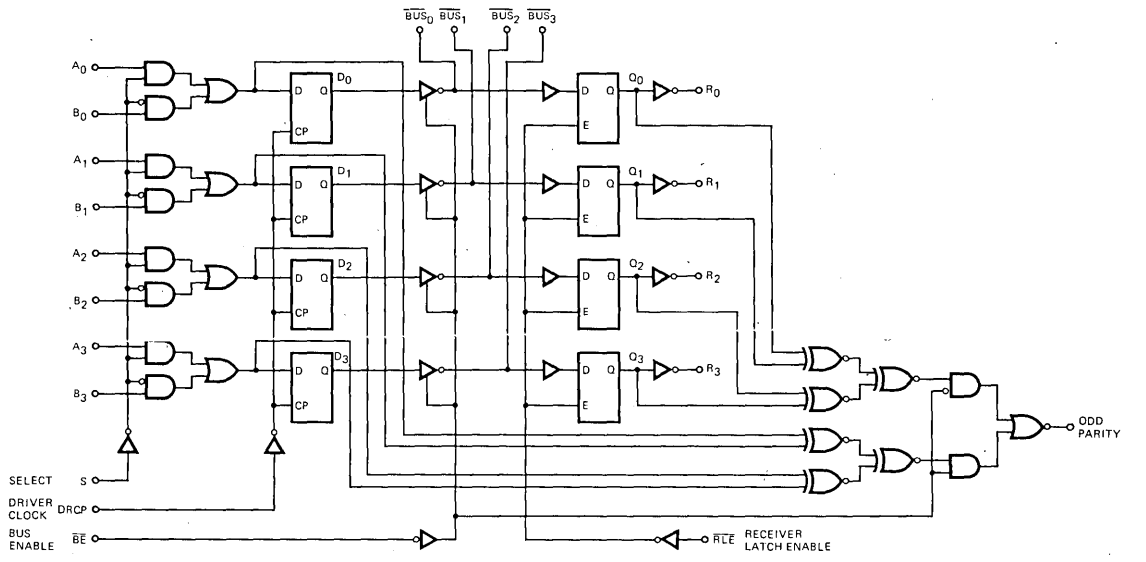


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2906PC
Hermetic DIP	0°C to +70°C	AM2906DC
Dice	0°C to +70°C	AM2906XC
Hermetic DIP	−55°C to +125°C	AM2906DM
Hermetic Flat Pak	−55°C to +125°C	AM2906FM
Dice	−55°C to +125°C	AM2906XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

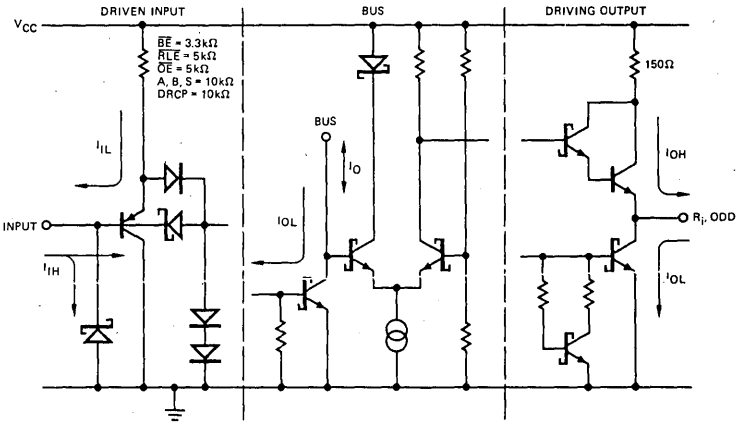
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.27	0.4	Volts
			$I_{OL} = 8mA$			0.32	0.45	
			$I_{OL} = 12mA$			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

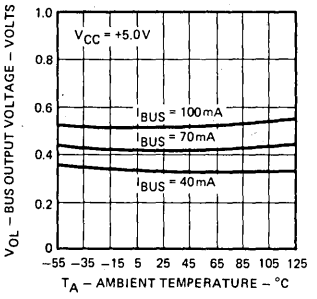
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



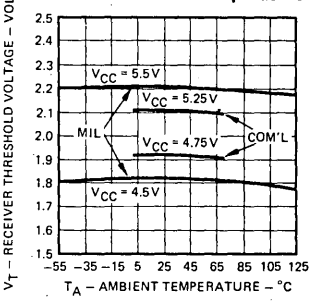
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

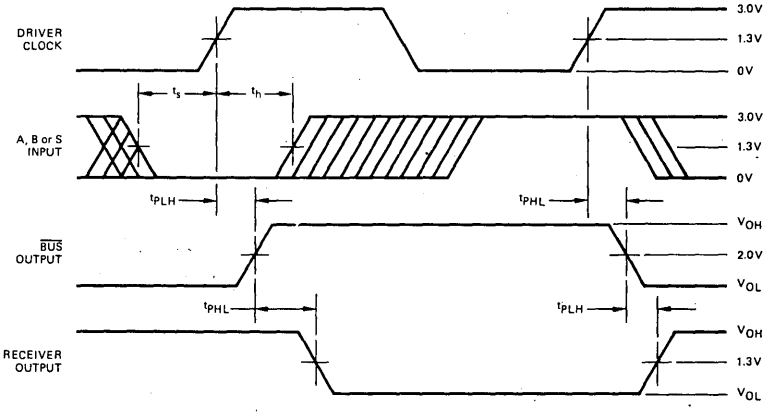
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

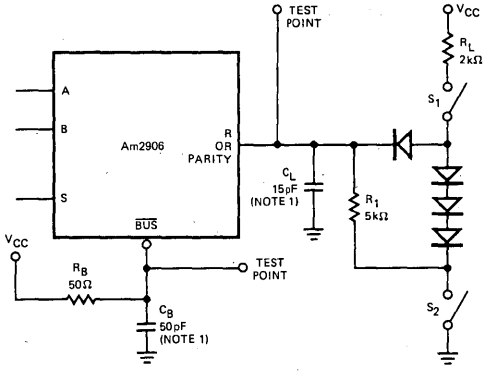
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

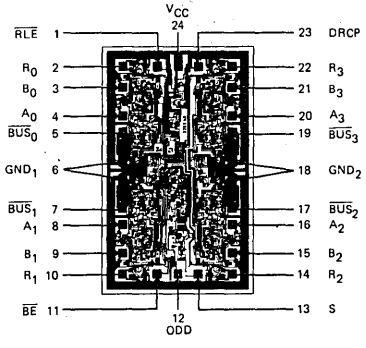
$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

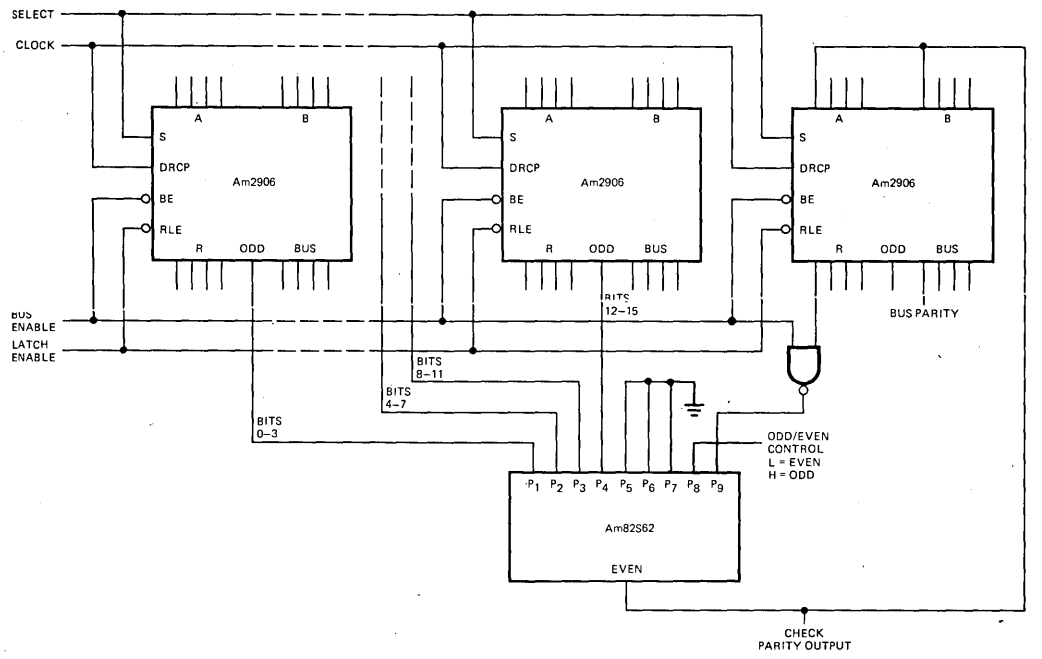


Metallization and Pad Layout

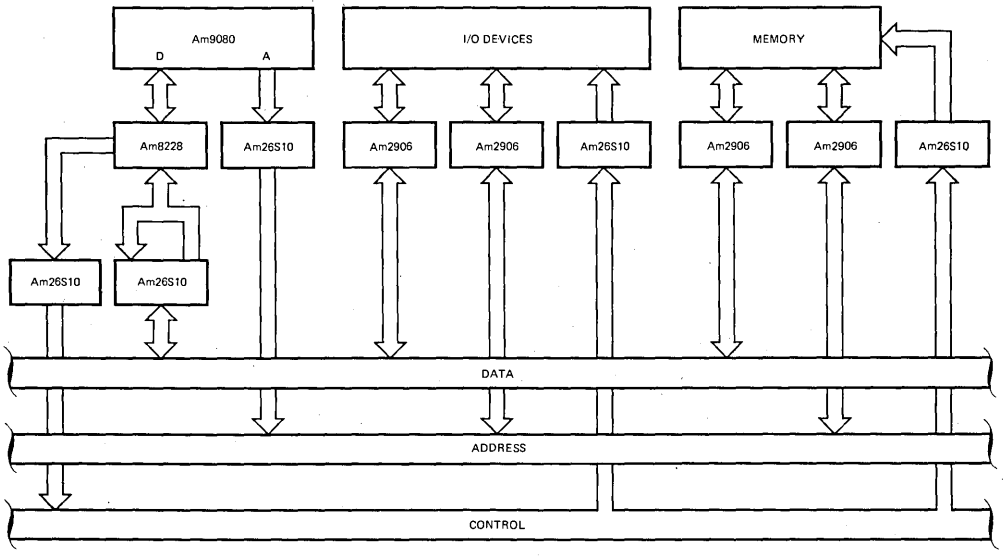


DIE SIZE 0.080" X 0.130"

APPLICATIONS



Generating or checking parity for 16 data bits.



Using the Am2906 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
$\overline{BUS}_0$	5	–	OC	BUS
GND_1	6	–	–	–
$\overline{BUS}_1$	7	–	OC	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
$\overline{OE}$	12	1	–	–
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
$\overline{BUS}_2$	17	–	OC	BUS
GND_2	18	–	–	–
$\overline{BUS}_3$	19	–	OC	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

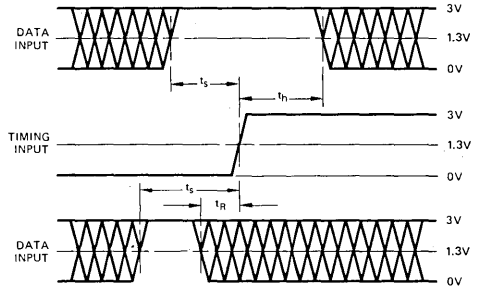
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

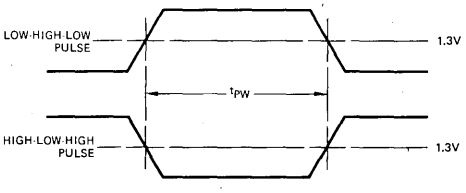
PARAMETER MEASUREMENTS

SET-UP, HOLD, AND RELEASE TIMES

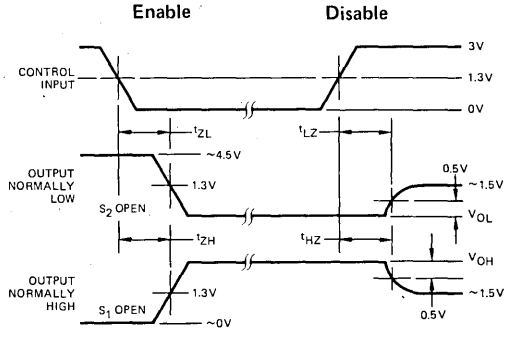


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross Hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6ns.

Am2907

Quad Bus Transceiver With Three-State Receiver And Parity

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

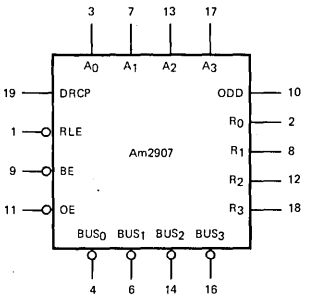
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

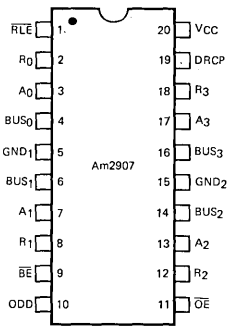
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

CONNECTION DIAGRAMS
Top Views

DIP



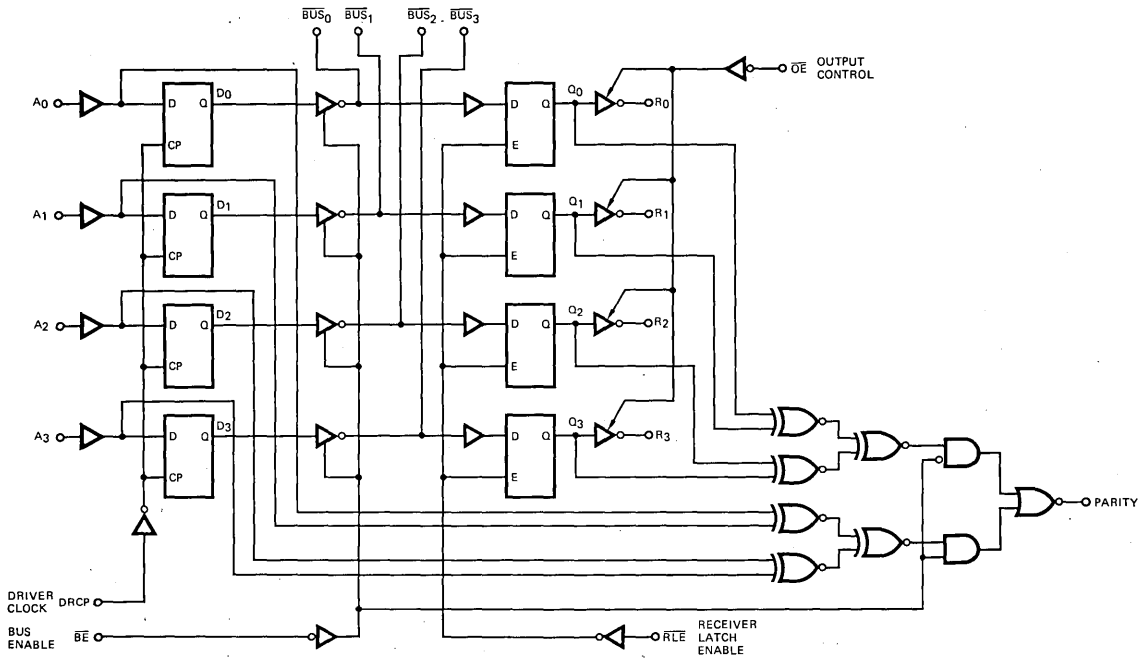
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2907PC
Hermetic DIP	0°C to +70°C	AM2907DC
Dice	0°C to +70°C	AM2907XC
Hermetic DIP	−55°C to +125°C	AM2907DM
* Hermetic Flat Pak	−55°C to +125°C	AM2907FM
Dice	−55°C to +125°C	AM2907XM

*Available on special order

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2907XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

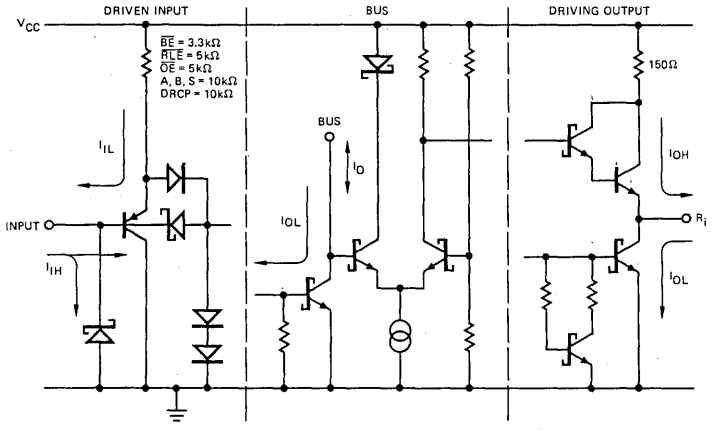
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1mA$		2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$ $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$ V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$ V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$ V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND				75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	A Data Inputs	C_L = 15pF R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

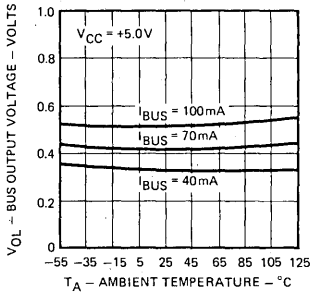


Note: Actual current flow direction shown.

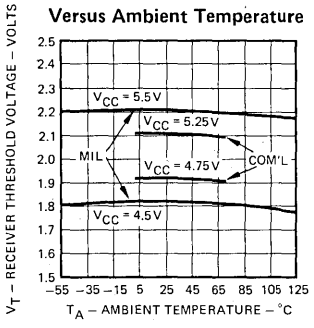
4

TYPICAL PERFORMANCE CURVES

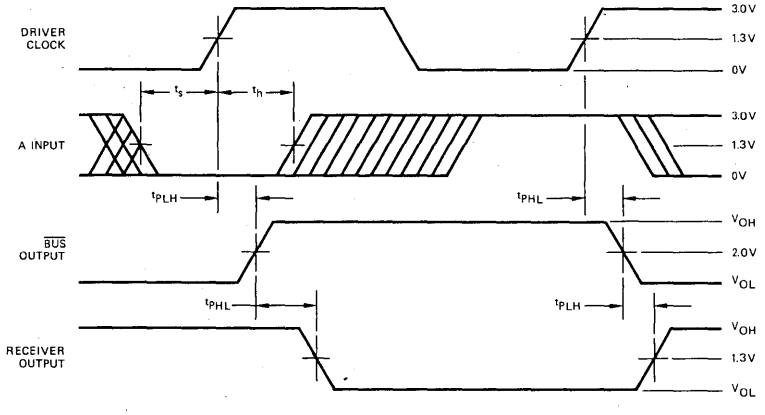
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Reciever output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

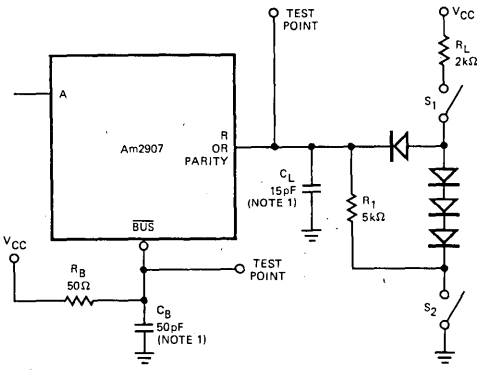
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

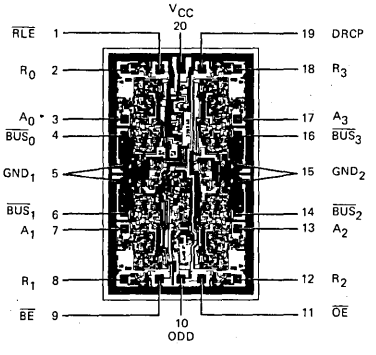
ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

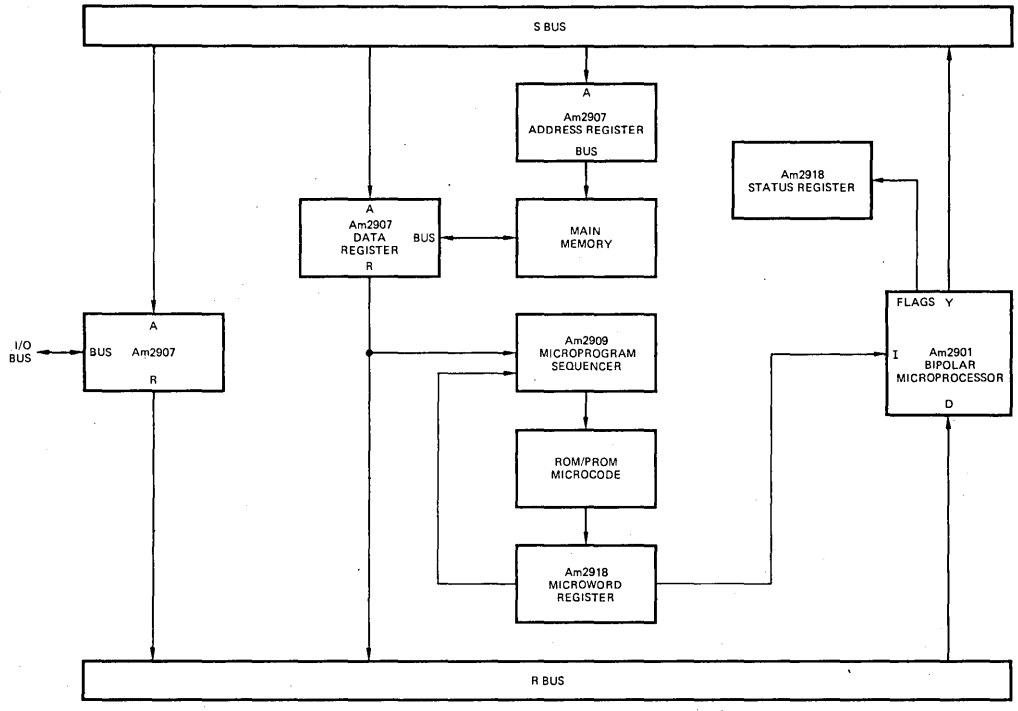


Metallization and Pad Layout

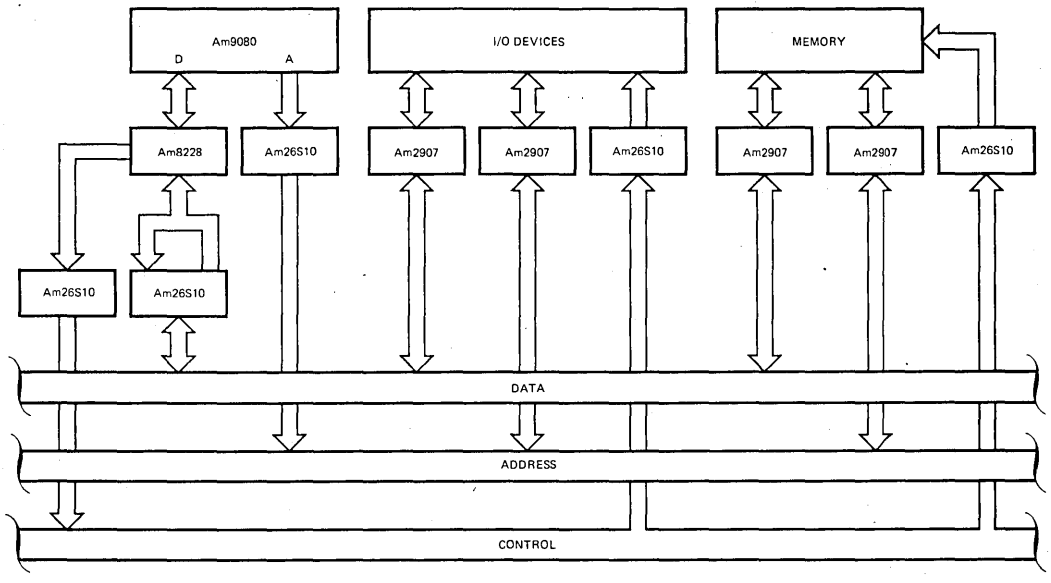


DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.



Using the Am2907 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No's	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
A_0	3	1	–	–
BUS_0	4	–	OC	BUS
GND_1	5	–	–	–
BUS_1	6	–	OC	BUS
A_1	7	1	–	–
R_1	8	–	50/130	33
$\overline{BE}$	9	1	–	–
ODD	10	–	33	33
$\overline{OE}$	11	1	–	–
R_2	12	–	50/130	33
A_2	13	1	–	–
BUS_2	14	–	OC	BUS
GND_2	15	–	–	–
BUS_3	16	–	OC	BUS
A_3	17	1	–	–
R_3	18	–	50/130	33
DRCP	19	1	–	–
V_{CC}	20	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

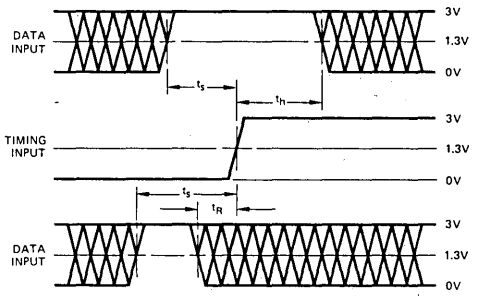
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

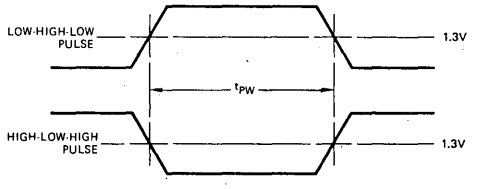
PARAMETER MEASUREMENTS

SET-UP, HOLD, AND RELEASE TIMES

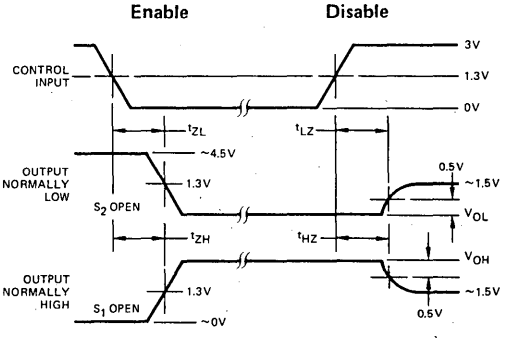


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross Hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15$ns; $t_f \leq 6$ns.

Am2915A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

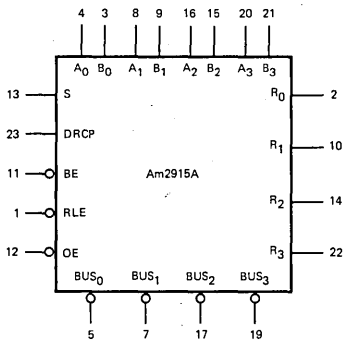
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

ORDERING INFORMATION

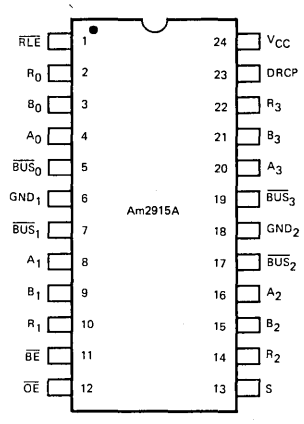
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2915APC
Hermetic DIP	0°C to +70°C	AM2915ADC
Dice	0°C to +70°C	AM2915AXC
Hermetic DIP	−55°C to +125°C	AM2915ADM
Hermetic Flat Pak	−55°C to +125°C	AM2915AFM
Dice	−55°C to +125°C	AM2915AXM

LOGIC SYMBOL

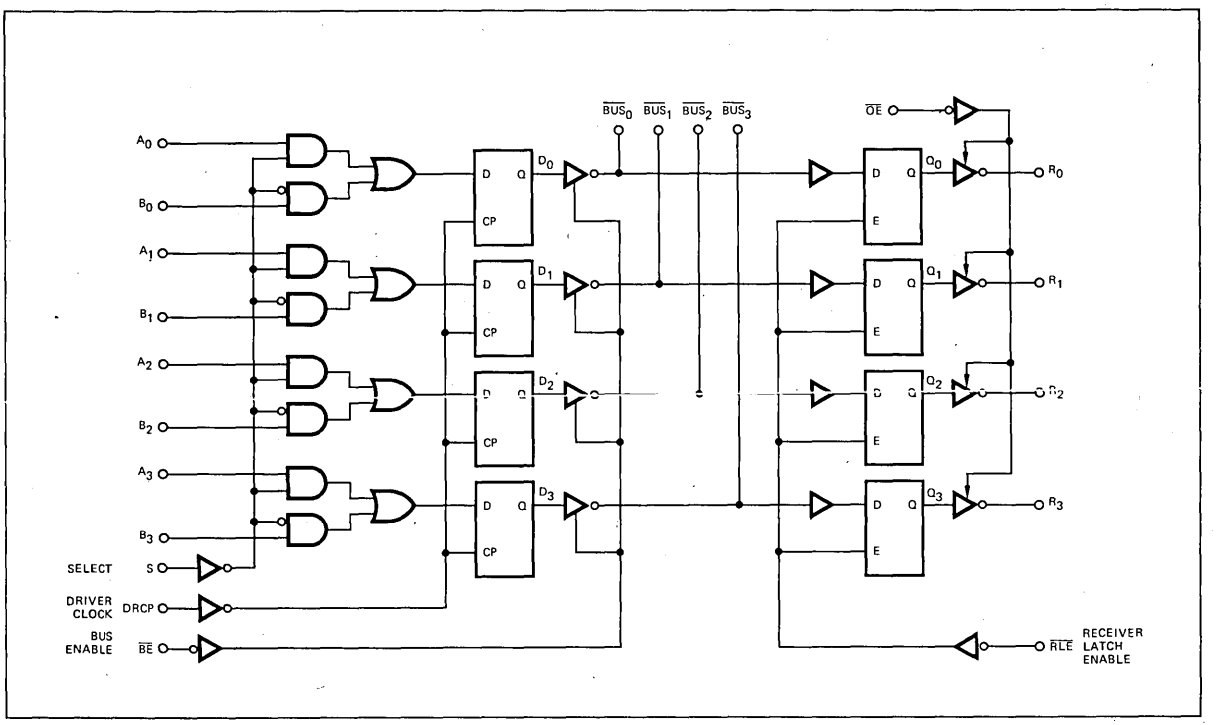


V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (Power OFF)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (High Impedance)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

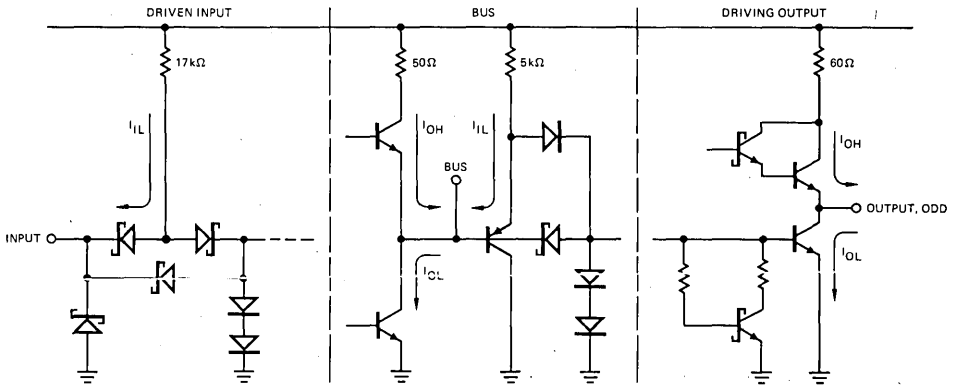
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			50	μA
			$V_O = 0.4$V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	$C_L = 15$pF, $R_L = 2.0$kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		$C_L = 5$pF, $R_L = 2.0$kΩ		14	26		14	23	

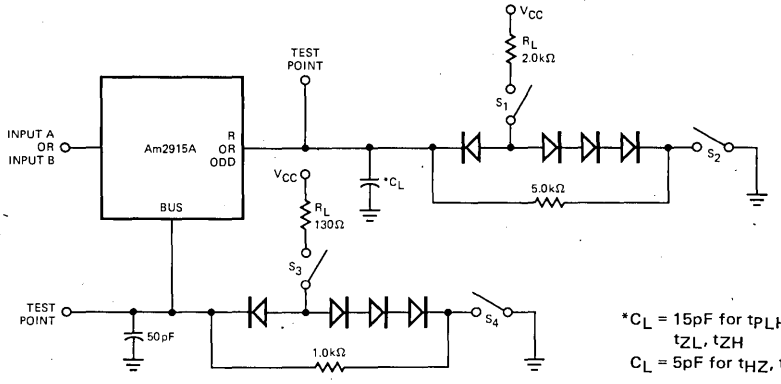
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



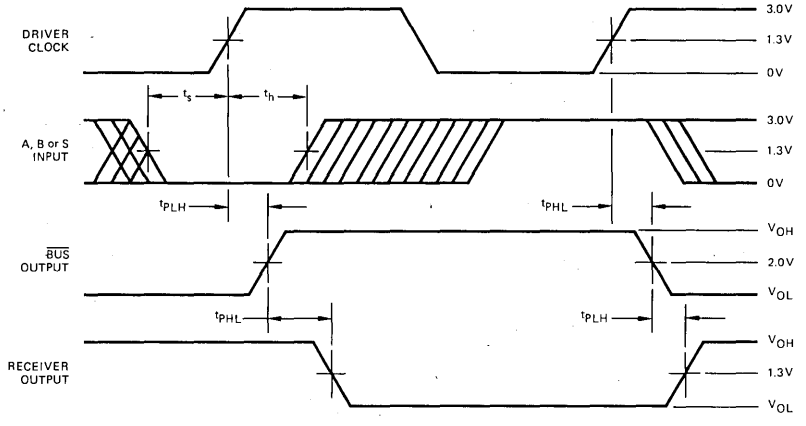
Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

SWITCHING WAVEFORMS



Note: Bus to Reciver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

4

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

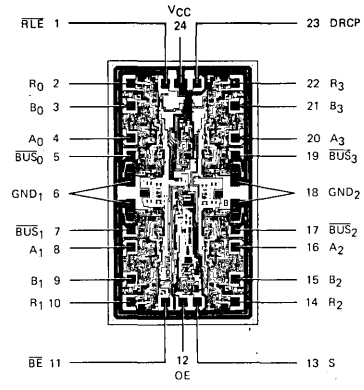
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

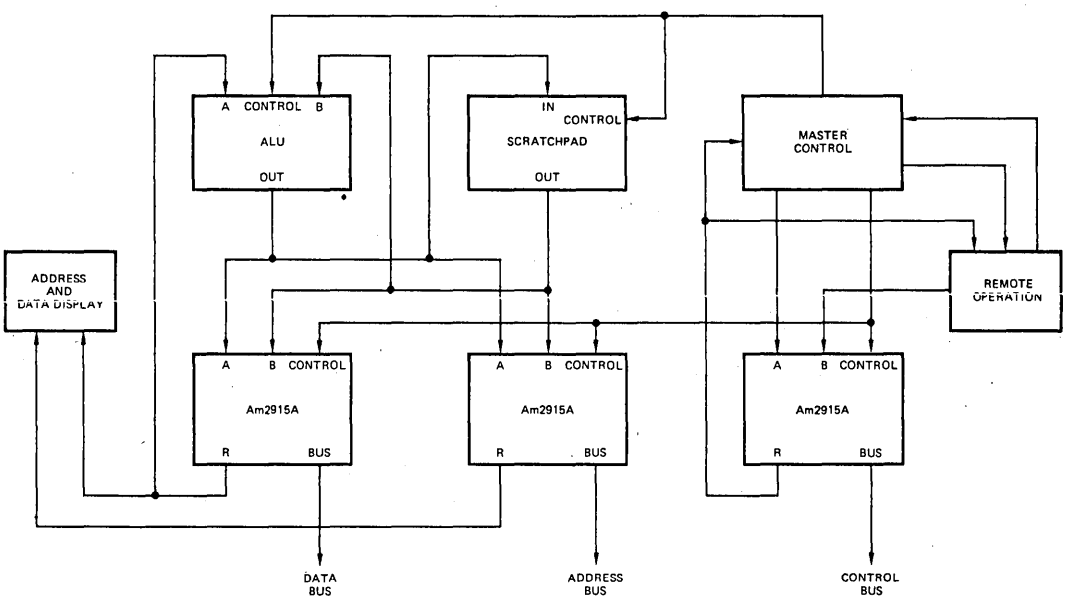
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

Metallization and Pad Layout

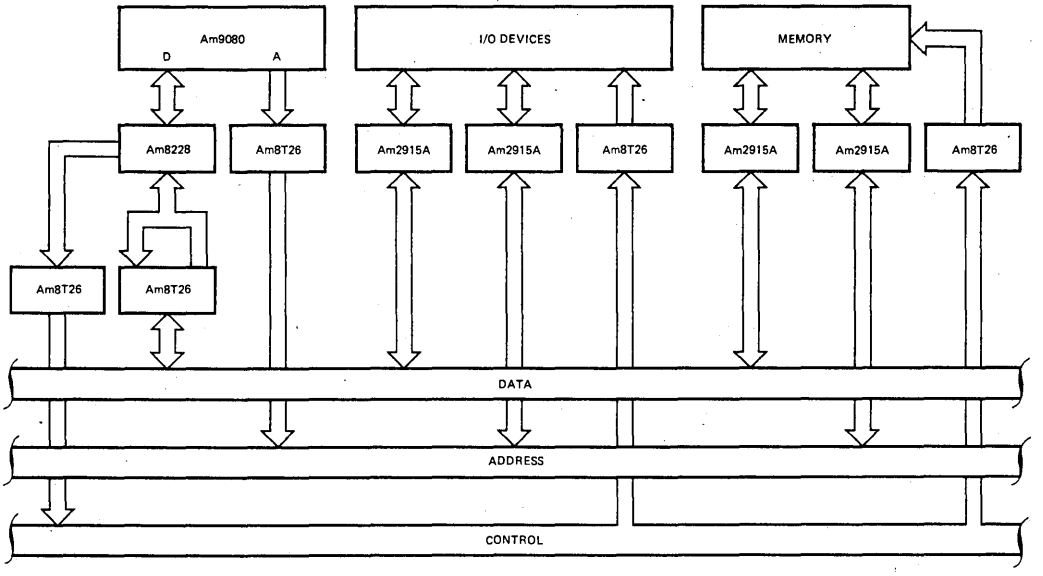


DIE SIZE .074" X .130"

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.



Using the Am2915A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
$\overline{BUS}_0$	5	–	BUS	BUS
GND_1	6	–	–	–
$\overline{BUS}_1$	7	–	BUS	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
$\overline{OE}$	12	1	–	–
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
$\overline{BUS}_2$	17	–	BUS	BUS
GND_2	18	–	–	–
$\overline{BUS}_3$	19	–	BUS	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

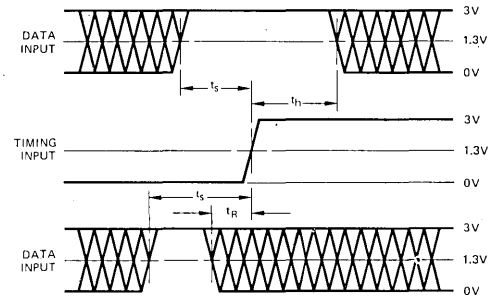
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

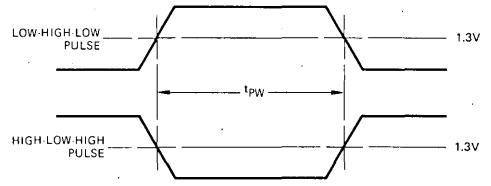
PARAMETER MEASUREMENT

SET-UP, HOLD, AND RELEASE TIMES

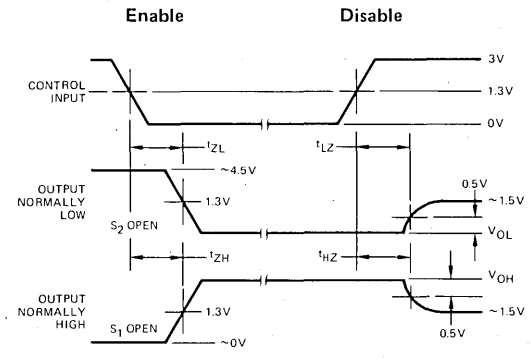


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6ns.

4

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

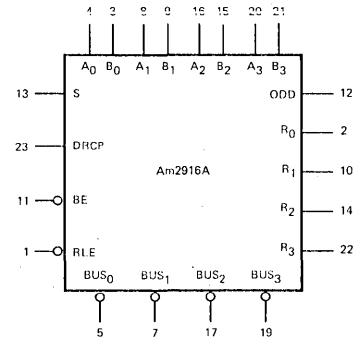
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

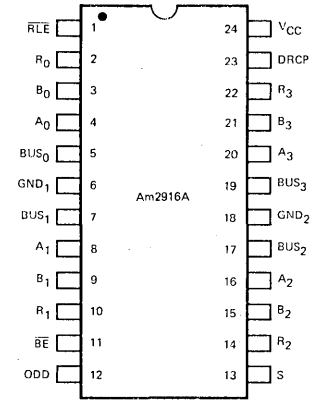
The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View

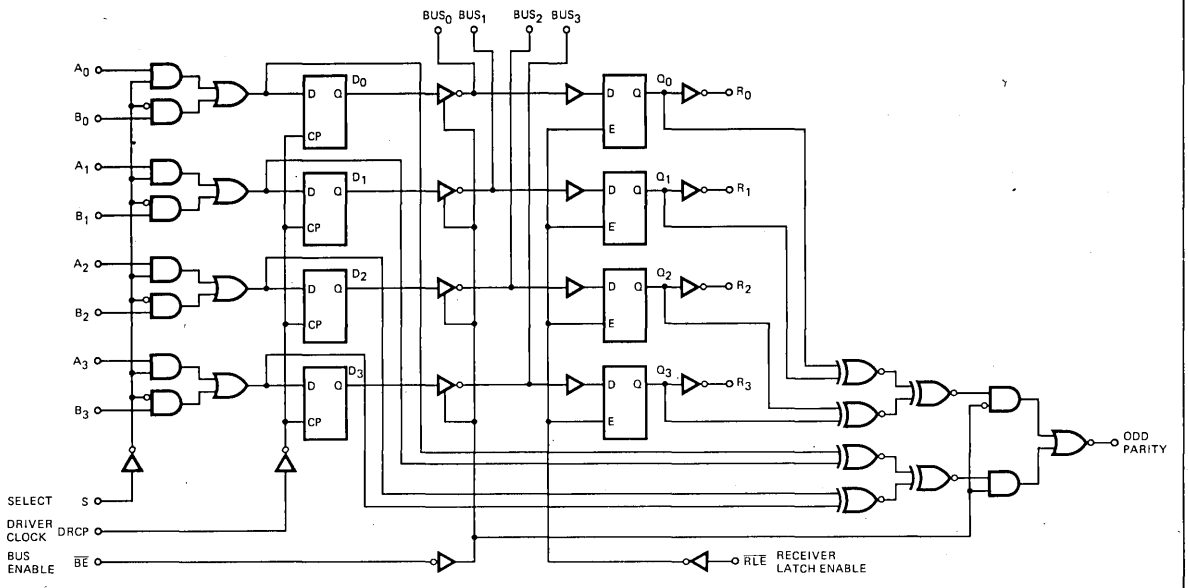


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2916APC
Hermetic DIP	0°C to +70°C	AM2916ADC
Dice	0°C to +70°C	AM2916AXC
Hermetic DIP	−55°C to +125°C	AM2916ADM
Hermetic Flat Pak	−55°C to +125°C	AM2916AFM
Dice	−55°C to +125°C	AM2916AXM

LOGIC DIAGRAM



4

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (Power OFF)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (High Impedance)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

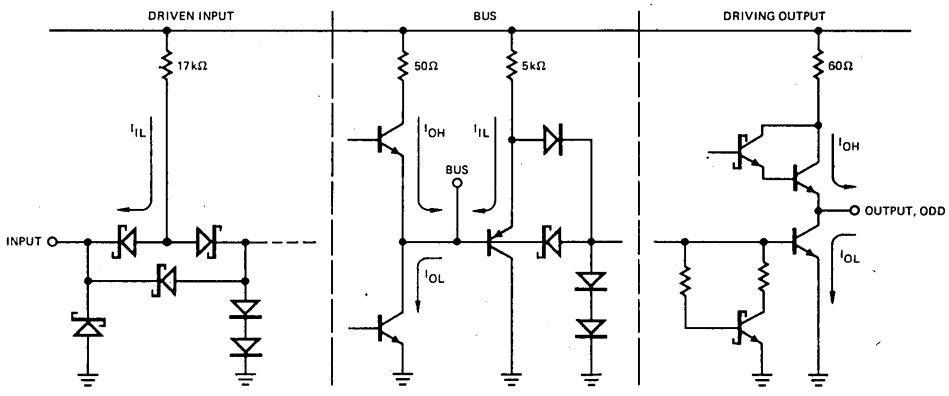
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)		15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 15pF R_L = 2.0kΩ		18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}		C_L = 5pF, R_L = 2.0kΩ		21	36		21	32	

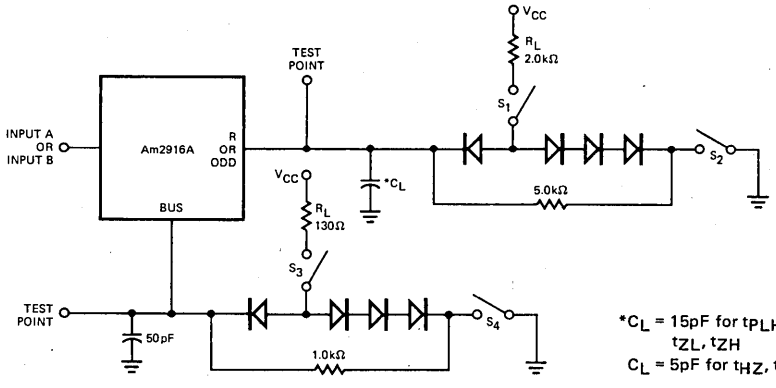
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



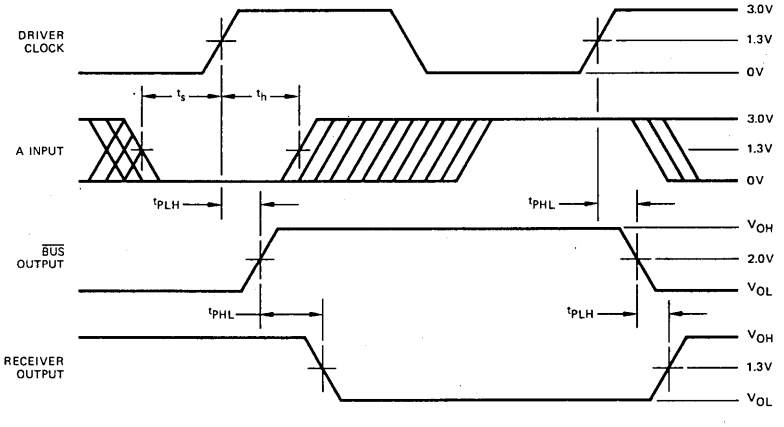
Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH
L = LOW
Z = HIGH Impedance
NC = No change
X = Don't care
↑ = LOW-to-HIGH transition
i = 0, 1, 2, 3

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

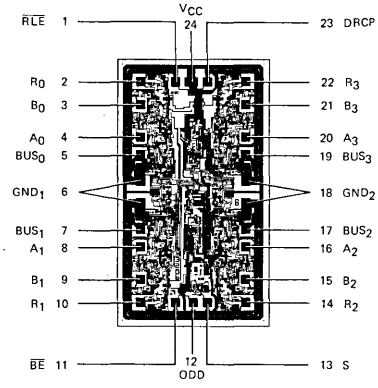
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

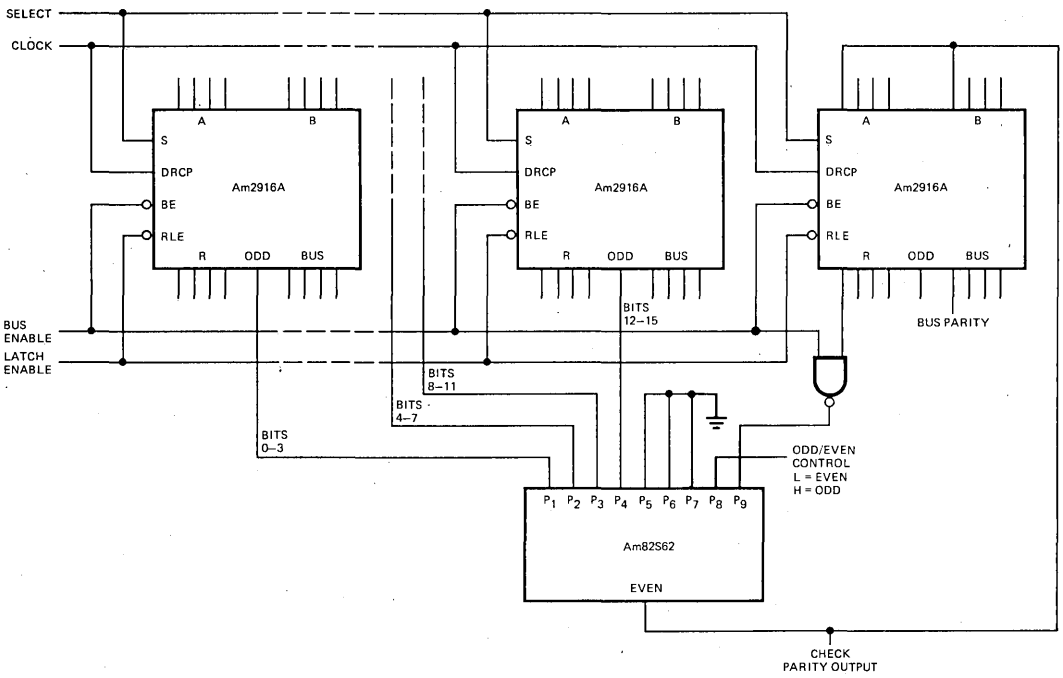
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

Metallization and Pad Layout

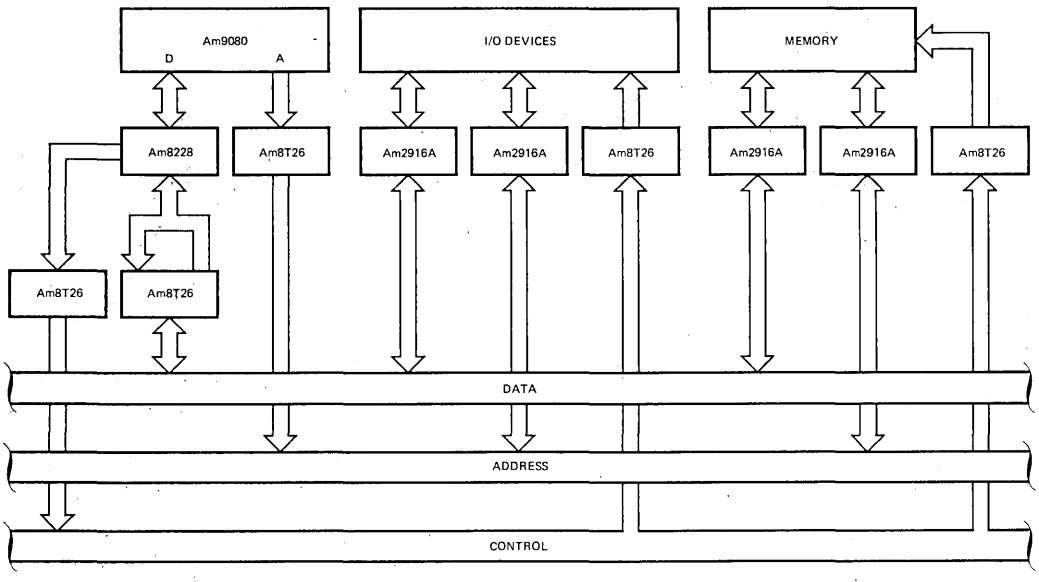


DIE SIZE .074" X .130"

APPLICATIONS



Generating or checking parity for 16 data bits.



Using the Am2916A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
$\overline{BUS}_0$	5	–	BUS	BUS
GND_1	6	–	–	–
$\overline{BUS}_1$	7	–	BUS	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
$\overline{OE}$	12	1	–	–
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
$\overline{BUS}_2$	17	–	BUS	BUS
GND_2	18	–	–	–
$\overline{BUS}_3$	19	–	BUS	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

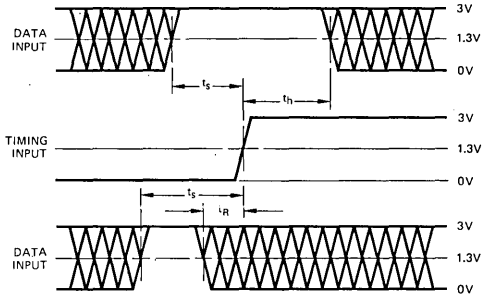
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

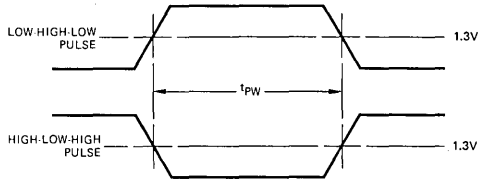
PARAMETER MEASUREMENT

SET-UP, HOLD, AND RELEASE TIMES

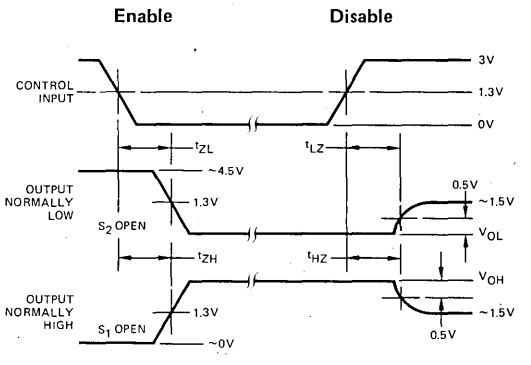


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6ns.

Am2917A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

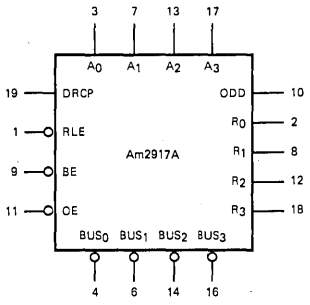
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

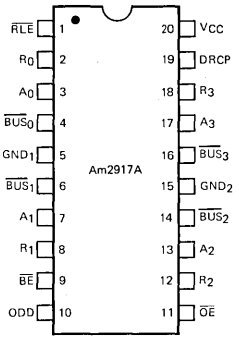
The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

CONNECTION DIAGRAM
Top View

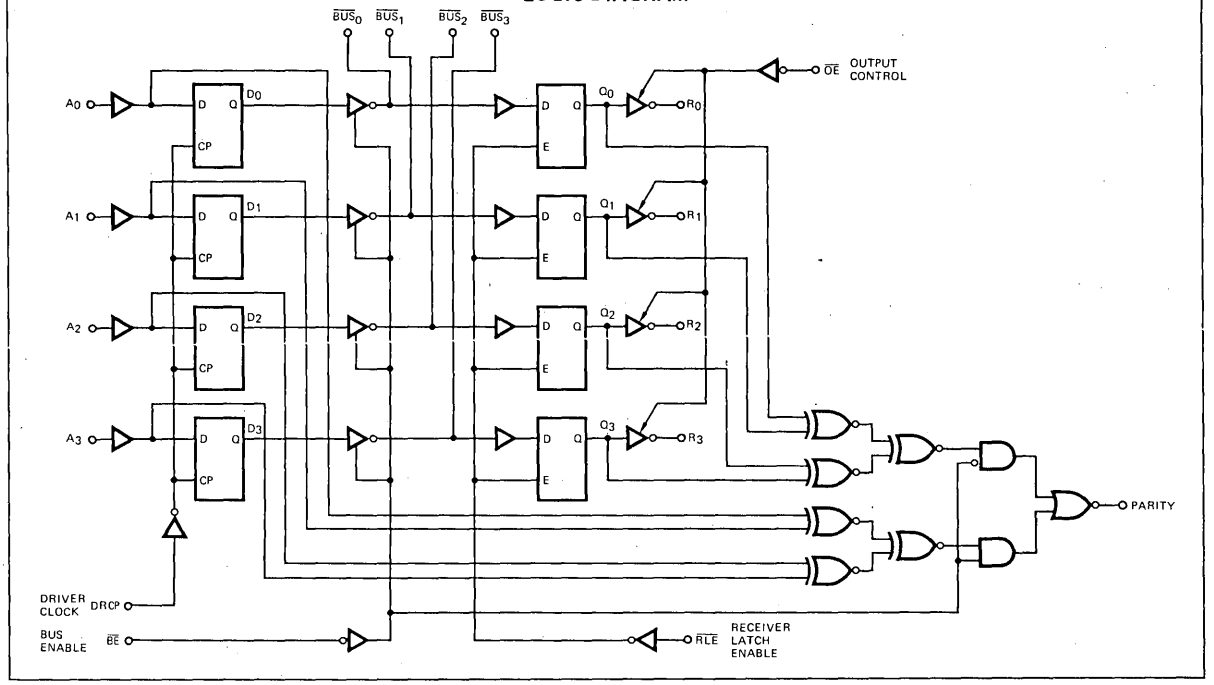


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2917APC
Hermetic DIP	0°C to +70°C	AM2917ADC
Dice	0°C to +70°C	AM2917AXC
Hermetic DIP	−55°C to +125°C	AM2917ADM
Hermetic Flat Pak	−55°C to +125°C	AM2917AFM
Dice	−55°C to +125°C	AM2917AXM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (Power OFF)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (High Impedance)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50			mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

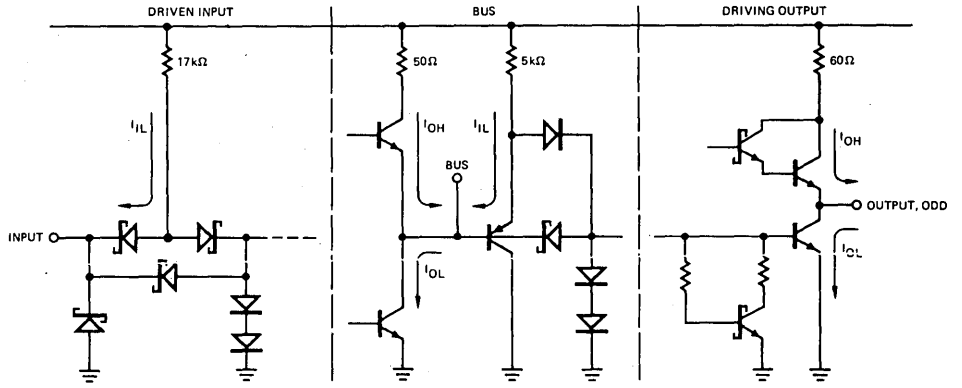
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs		15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)	C_L = 15 pF, R_L = 2.0 kΩ	15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5 pF, R_L = 2.0 kΩ		14	26		14	23	

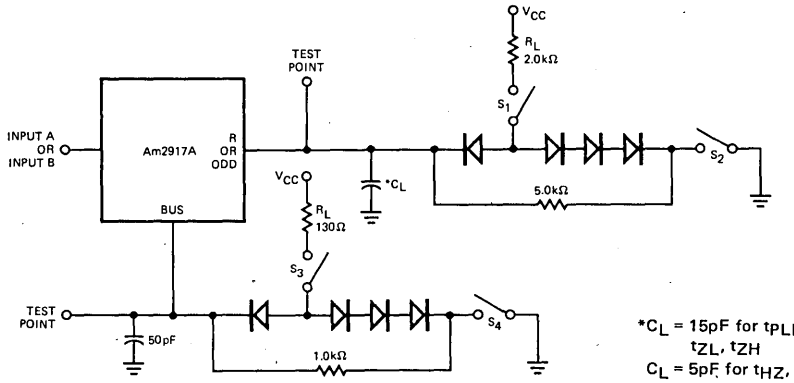
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



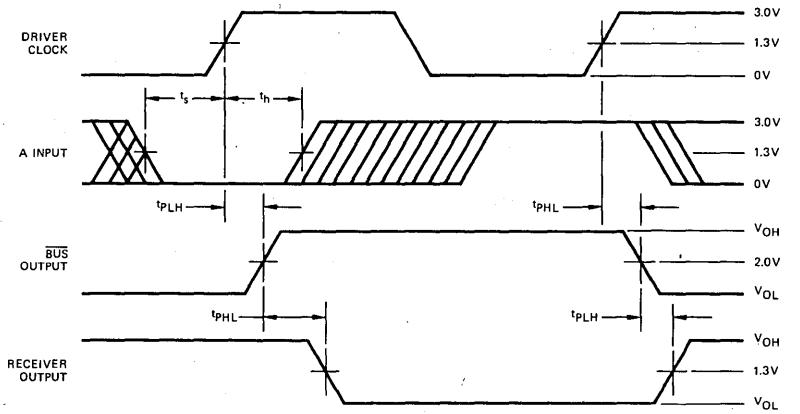
Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

FUNCTION TABLE

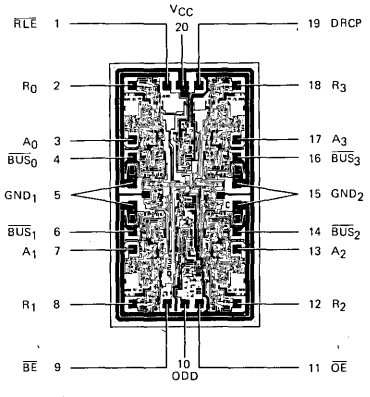
INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bús input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

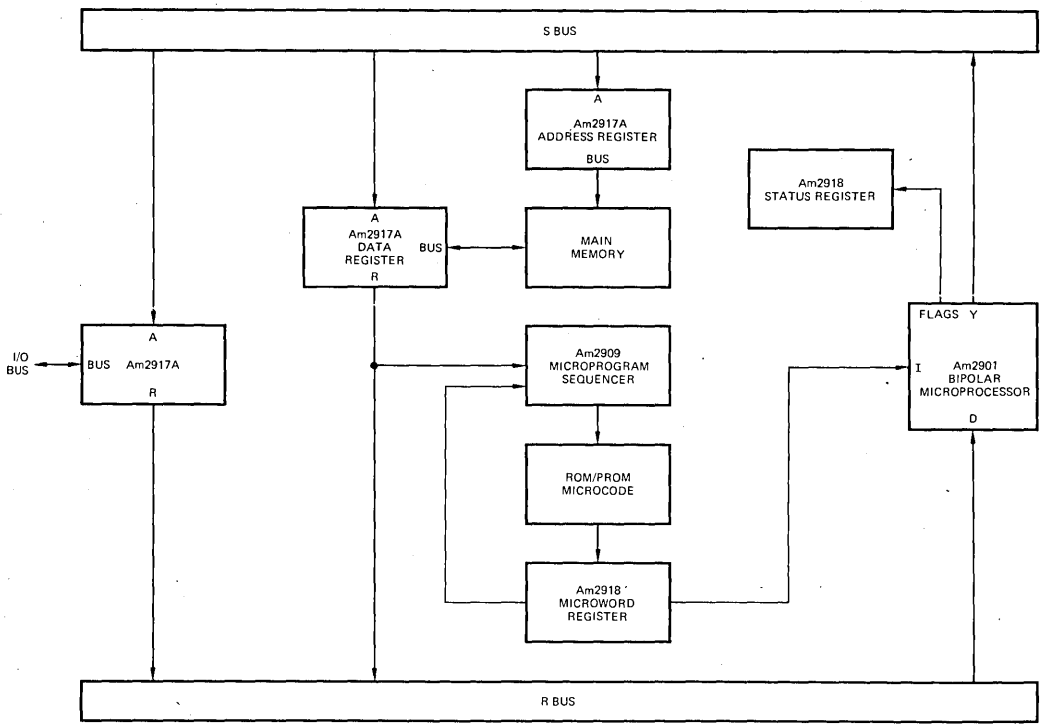
$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

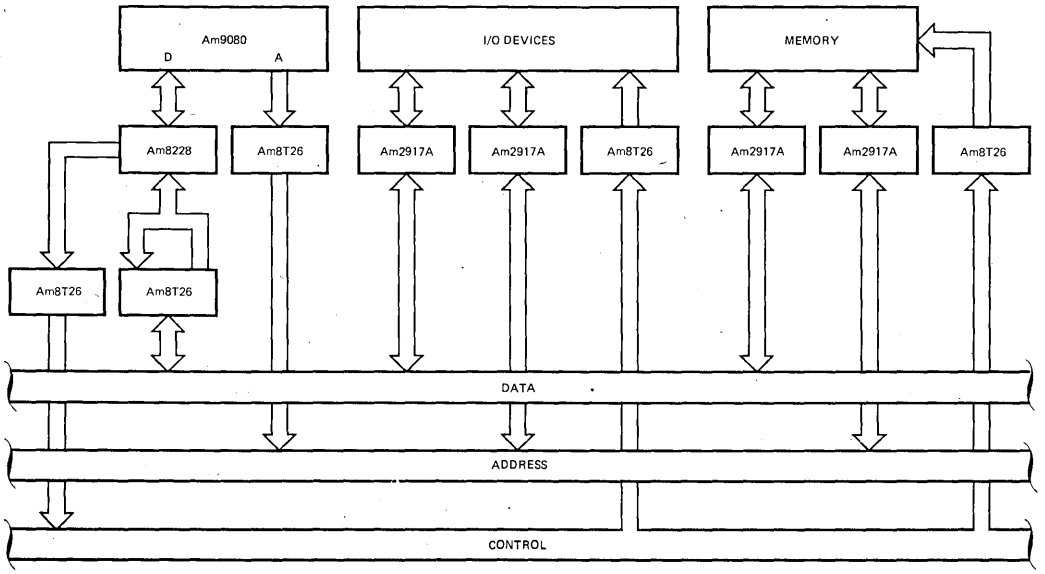
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

4

APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.



Using the Am2917A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

LOADING RULES (In Unit Loads)

Input/Output	Pin No's	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
A_0	3	1	–	–
BUS_0	4	–	BUS	BUS
GND_1	5	–	–	–
BUS_1	6	–	BUS	BUS
A_1	7	1	–	–
R_1	8	–	50/130	33
$\overline{BE}$	9	1	–	–
ODD	10	–	33	33
$\overline{OE}$	11	1	–	–
R_2	12	–	50/130	33
A_2	13	1	–	–
BUS_2	14	–	BUS	BUS
GND_2	15	–	–	–
BUS_3	16	–	BUS	BUS
A_3	17	1	–	–
R_3	18	–	50/130	33
DRCP	19	1	–	–
V_{CC}	20	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and –0.36mA measured at 0.4V LOW.

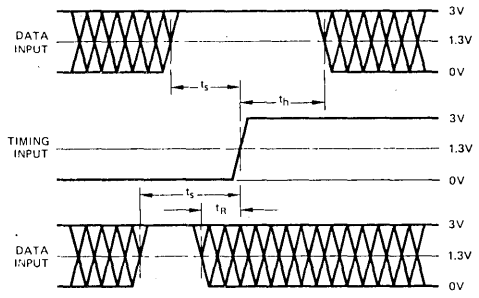
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	–1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	–2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	–0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	–0.36mA	0.4V
Am54/74	40μA	2.4V	–1.6mA	0.4V
54H/74H	50μA	2.4V	–2.0mA	0.4V
Am54S/74S	50μA	2.7V	–2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	–0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	–0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	–0.36mA	0.4V
Am9300	40μA	2.4V	–1.6mA	0.4V
Am93L00	20μA	2.4V	–0.4mA	0.3V
Am93S00	50μA	2.7V	–2.0 mA	0.5 V
Am75/85	40μA	2.4V	–1.6mA	0.4V
Am8200	40μA	4.5V	–1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

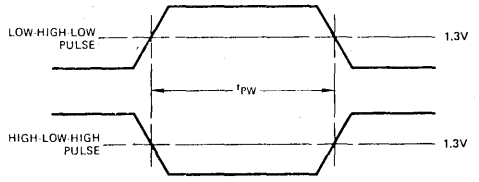
PARAMETER MEASUREMENTS

SET-UP, HOLD, AND RELEASE TIMES

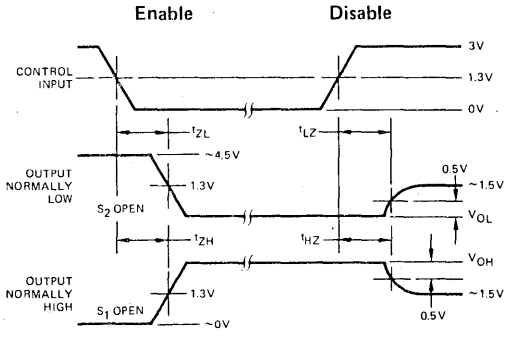


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross Hatched area is don't care condition.

PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6ns.

4

Am3212•Am8212

Eight-Bit Input/Output Port

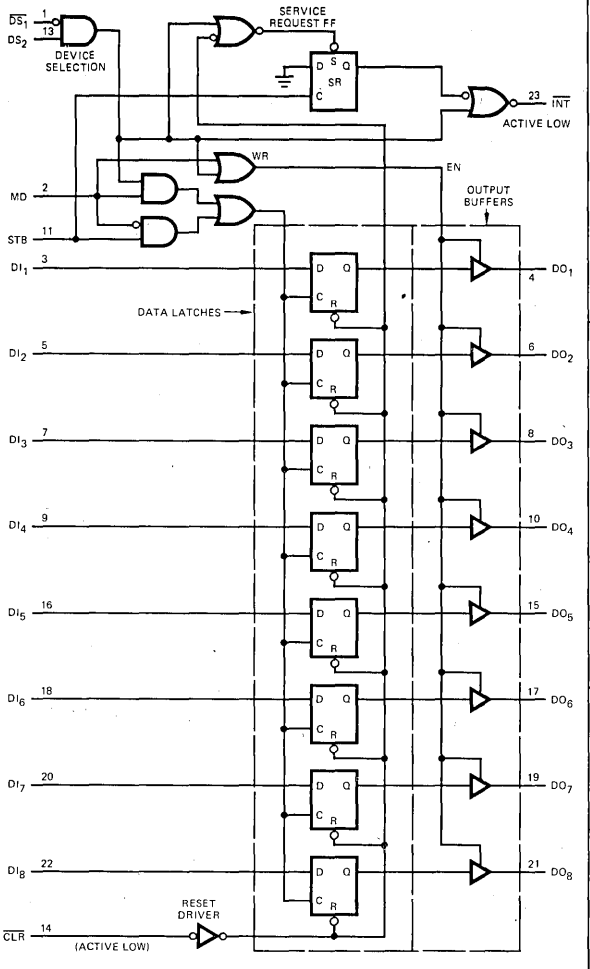
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

FUNCTIONAL DESCRIPTION

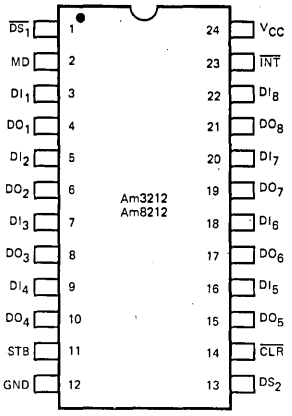
All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

LOGIC DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC
Hermetic DIP	0°C to +70°C	D3212
Hermetic DIP	–55°C to +125°C	MD3212
Molded DIP	0°C to +70°C	P3212

FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS_1}$, DS_2, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS_1}$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and DS_2 is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

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TRUTH TABLE

STB	MD	$\overline{DS_1} - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS_1} - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

$\overline{CLR}$ — Resets Data Latch
— Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage	−0.5V to +7.0V
Output Voltage	−0.5V to +7.0V
Input Voltages	−1.0V to +5.5V
Output Current (Each Output)	125mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212, P3212, D3212 (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%
Am8212DM, MD3212 (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%

DC CHARACTERISTICS

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, DI_1 – DI_8 Inputs	V_F = 0.45V				−0.25	mA
I_F	Input Load Current MD Input	V_F = 0.45V				−0.75	mA
I_F	Input Load Current DS_1 Input	V_F = 0.45V				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, DI_1 – DI_8 Inputs	V_R = 5.25V				10	µA
I_R	Input Leakage Current MO Input	V_R = 5.25V				30	µA
I_R	Input Leakage Current DS_1 Input	V_R = 5.25V				40	µA
V_C	Input Forward Voltage Clamp	I_C = −5.0mA	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 15mA				0.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0mA	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		I_{OH} = −0.5mA	MIL	3.5	4.0		
I_{SC}	Short Circuit Output Current	V_O = 0V		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	V_O = 0.45V/5.25V				20	µA
I_{CC}	Power Supply Current	Note 2			90	130	mA

AC CHARACTERISTICS (Note 3)

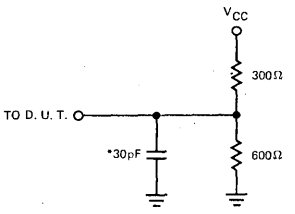
Parameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

CAPACITANCE (Note 4)

F = 1.0MHz, V_{BIAS} = 2.5V, V_{CC} = +5.0V, T_A = 25°C

Parameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, DI_1–DI_8 Input Capacitance	5.0	9.0	pF
C_{OUT}	DO_1–DO_8 Output Capacitance	8.0	12	pF

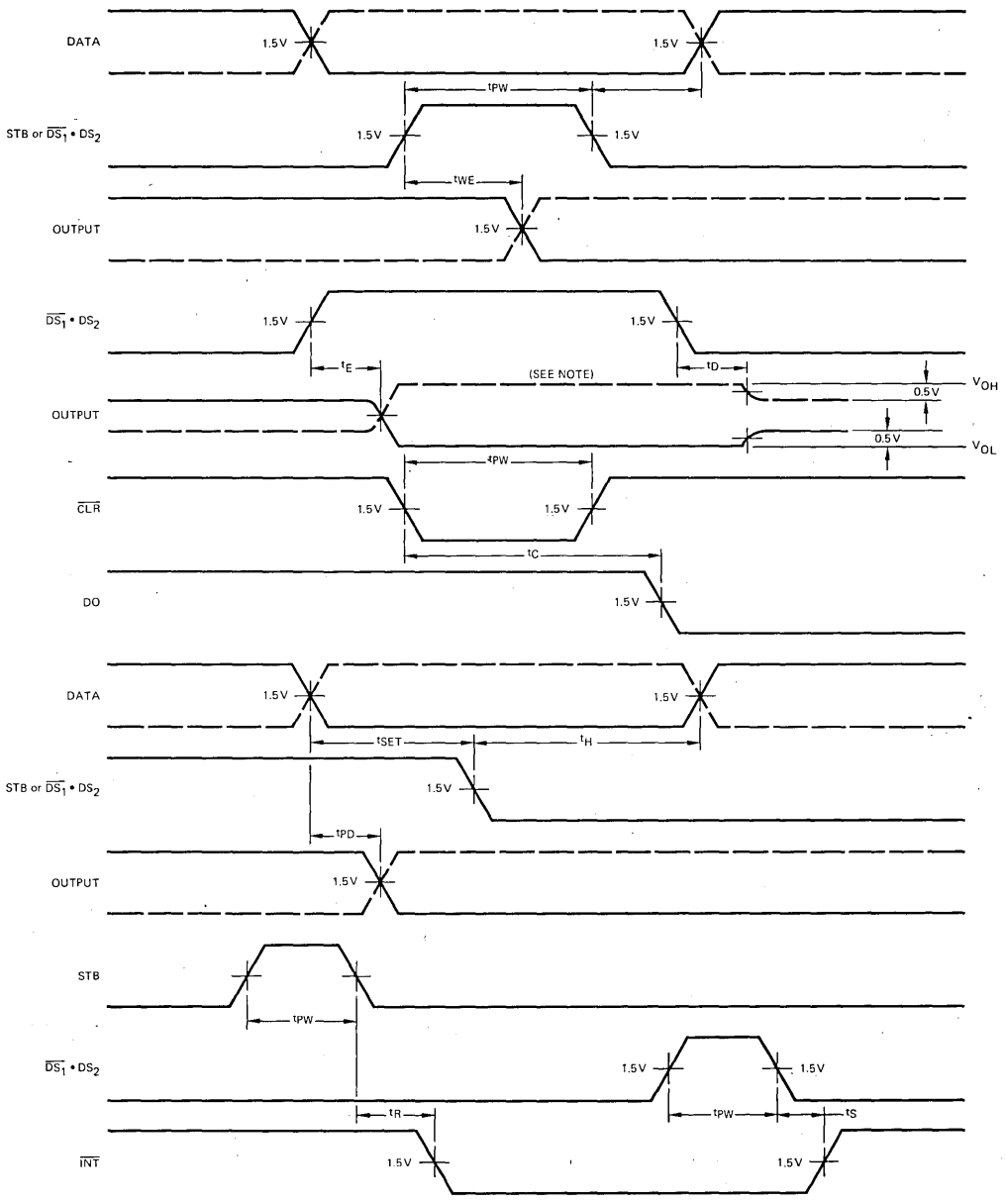
TEST LOAD (15mA and 30pF)



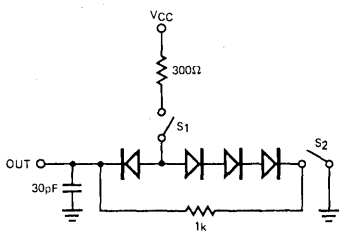
*Including Jig and Probe Capacitance.

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; DS_1 = DS_2 = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

TIMING DIAGRAM

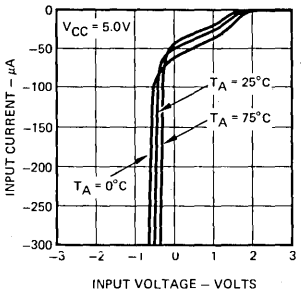


Note: Alternative Test Load.

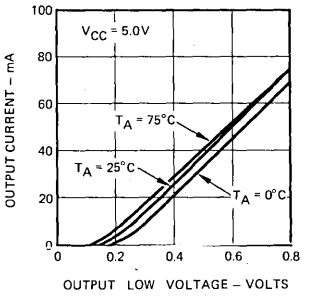


TYPICAL CHARACTERISTICS

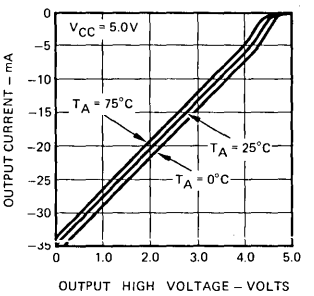
Input Current Versus Input Voltage



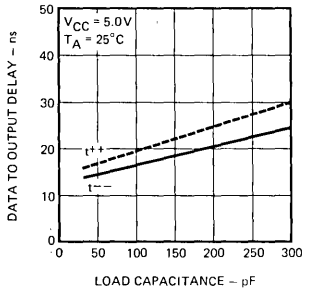
Output Current Versus Output LOW Voltage



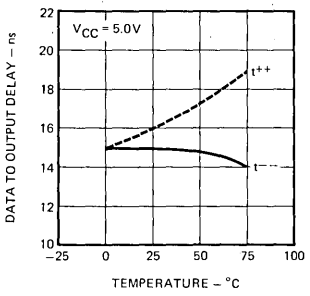
Output Current Versus Output HIGH Voltage



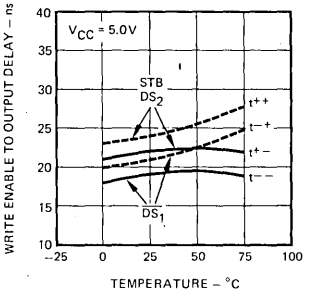
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature

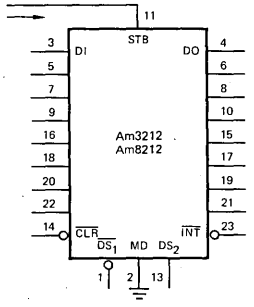


Write Enable to Output Delay Versus Temperature

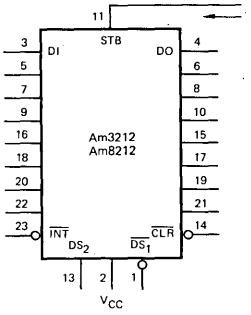


LOGIC SYMBOLS

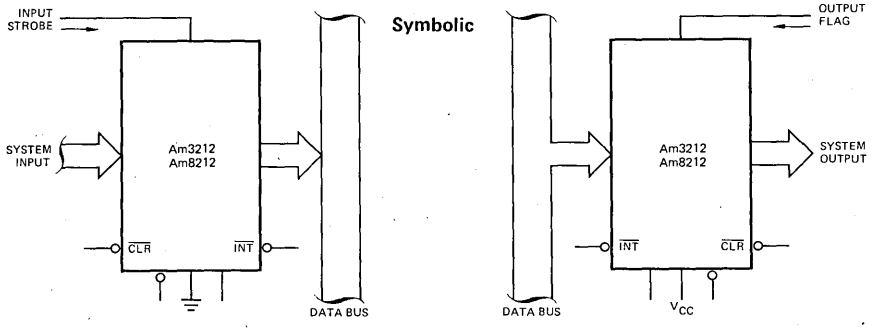
INPUT DEVICE



OUTPUT DEVICE



Detailed



Symbolic

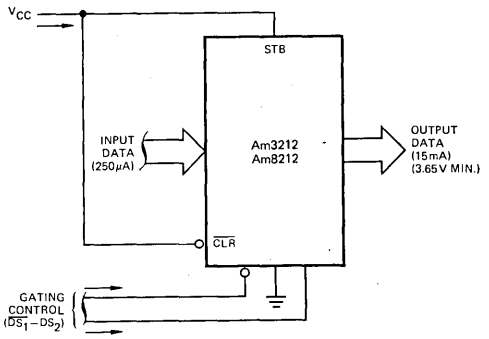
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

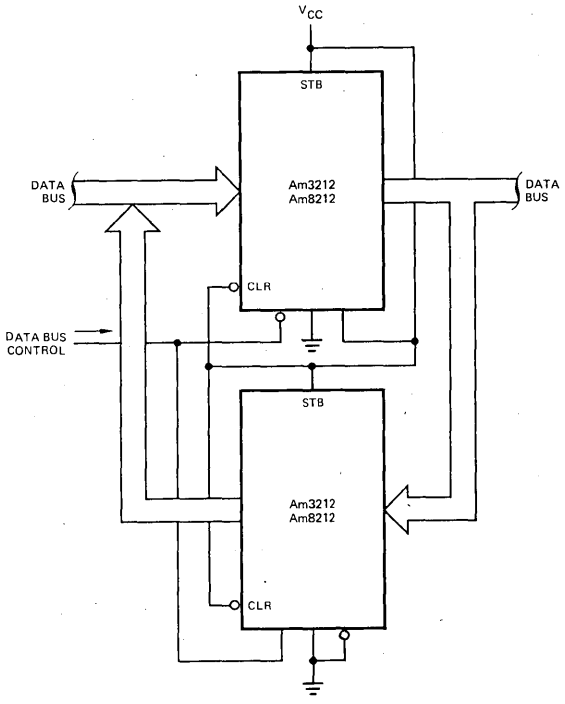
When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output.



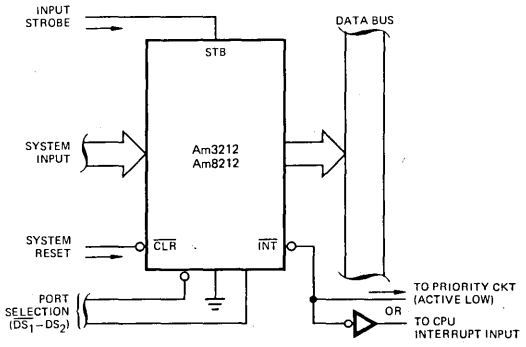
Bi-Directional Bus Driver

Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



Interrupting Input Port

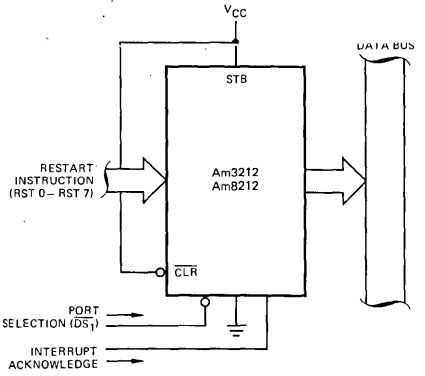
The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.



TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

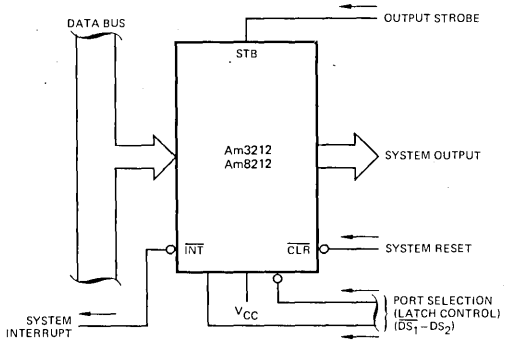
Interrupt Instruction Port

The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



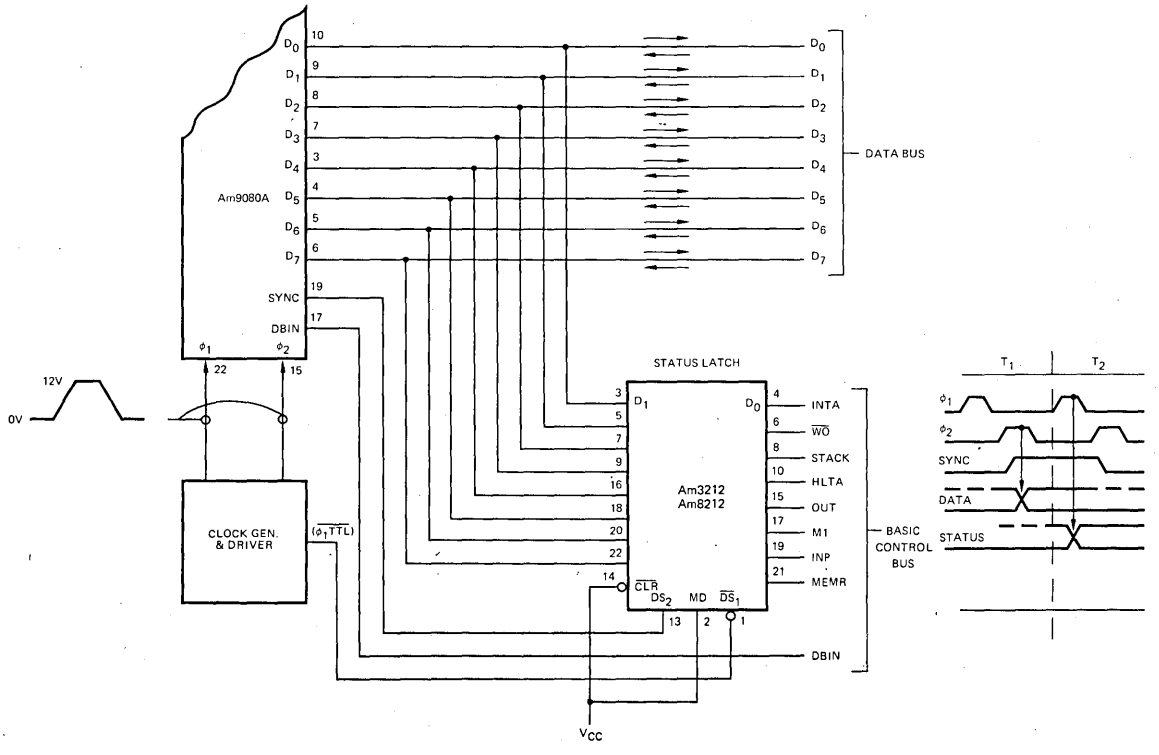
Output Port (With Hand-Shaking)

The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS_1} \cdot DS_2$).



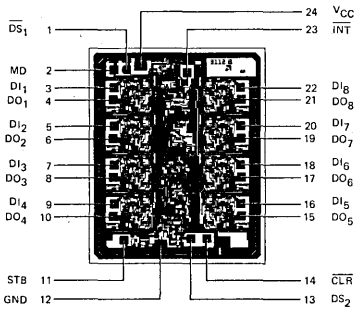
Am9080A Status Latch

The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



4

Metallization and Pad Layout



DIE SIZE
0.091" X 0.112"

Am3216 • Am3226 • Am8216 • Am8226

Four-Bit Parallel Bidirectional Bus Driver

Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am3216 and Am8216 have non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am3226 and Am8226 have inverting outputs

FUNCTIONAL DESCRIPTION

The Am3216, Am3226, Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am3216 and Am8216, and inverting Am3226 and Am8226 drivers are provided for flexibility in system design.

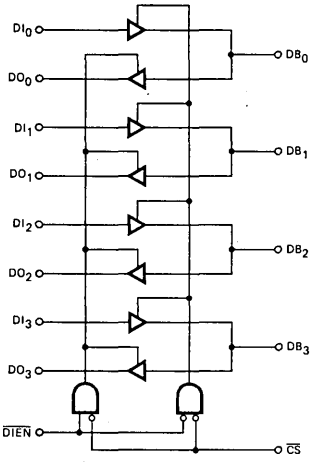
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

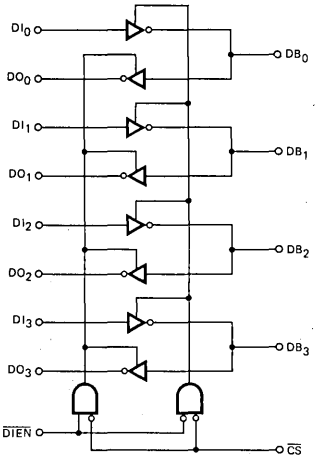
The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

LOGIC DIAGRAMS

Am3216 • Am8216



Am3226 • Am8226

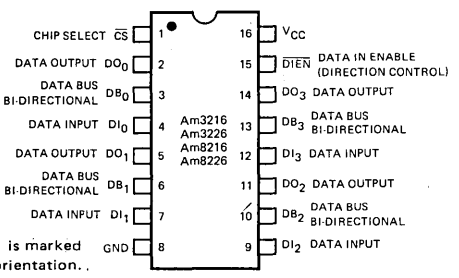


ORDERING INFORMATION

Package Type	Temperature Range	Am3216 Am8216 Order Number	Am3226 Am8226 Order Number
Hermetic DIP	–55°C to +125°C	MD3216	MD3226
Hermetic DIP	0°C to +70°C	D3216	D3226
Molded DIP	0°C to +70°C	P3216	P3226
Hermetic DIP	–55°C to +125°C	MD8216	MD8226
Hermetic DIP	0°C to +70°C	D8216	D8226
Molded DIP	0°C to +70°C	P8216	P8226
Dice	0°C to +70°C	AM8216XC	AM8226XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Temperature (Ambient) Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5 V to +7.0 V
All Input Voltages	−1.0 V to +5.5 V
Output Currents	125 mA

Am3216, Am3226, Am8216 AND Am8226 MILITARY ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

The following conditions apply unless otherwise specified:

MD3216, MD8216, MD3226, MD8226 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$			−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$			−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.5V$				80	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.5V$				40	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$				−1.2	Volts
V_{IL}	Input LOW Voltage	Am3216, Am8216					0.95	Volts
		Am3226, Am8226					0.9	
V_{IH}	Input HIGH Voltage				2.0			Volts
I_O	Output Leakage Current (Three-State)	DO	$V_O = 0.45V/5.5V$				20	μA
		DB					100	
I_{CC}	Power Supply Current	Am3216, Am8216				95	130	mA
		Am3226, Am8226				85	120	
V_{OL1}	Output LOW Voltage		DO Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$			0.3	0.45	Volts
V_{OL2}	Output LOW Voltage		DB Outputs $I_{OL} = 45mA$			0.5	0.6	Volts
V_{OH1}	Output HIGH Voltage		DO Outputs	$I_{OH} = -0.5mA$	3.4	4.0		Volts
				$I_{OH} = -2.0mA$	2.4			
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -5.0mA$		2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V, $V_{CC} = 5.0V$		−15	−35	−65	mA
			DB Outputs = 0V, $V_{CC} = 5.0V$		−30	−75	−120	

AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	33	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	75	ns
		Am8216	Note 2		45	75	
		Am3226, Am8226	Note 3		35	62	
t_D	Output Disable Time	Am3216, Am8216	Note 4		20	40	ns
		Am3226, Am8226			16	38	

Am3216, Am3226, Am8216 AND Am8226 COMMERCIAL ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D3216, D8216, D3226, D8226, P3216, P8216, P3226, P8226 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$		−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$		−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.25V$			20	µA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.25V$			10	µA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$			−1.0	Volts
V_{IL}	Input LOW Voltage					0.95	Volts
V_{IH}	Input HIGH Voltage			2.0			Volts
$\|I_{OL}\|$	Output Leakge Current (Three-State)	DO	$V_O = 0.45V/5.5V$			20	µA
		DB				100	
I_{CC}	Power Supply Current	Am3216, Am8216			95	130	mA
		Am3226, Am8226			85	120	
V_{OL1}	Output LOW Voltage		DB Outputs $I_{OL} = 15mA$ DB Outputs $IOL = 25mA$		0.3	0.45	Volts
V_{OL2}	Output LOW Voltage	Am3216, Am8216	DB Outputs $I_{OL} = 55mA$		0.5	0.6	Volts
		Am3226, Am8226	DB Outputs $I_{OL} = 50mA$		0.5	0.6	
V_{OH1}	Output HIGH Voltage		DO Outputs $I_{OH} = -1.0mA$ COM'L	3.65	4.0		Volts
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -10mA$	2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V	−15	−35	−65	mA
			DB Outputs $V_{CC} = 5.0V$	−30	−75	−120	

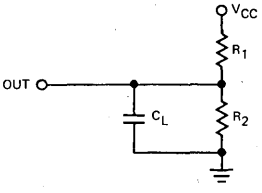
AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	30	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	65	ns
		Am8216	Note 2		45	65	
		Am3226, Am8226	Note 3		35	54	
t_D	Output Disable Time		Note 4		20	35	ns

TEST CONDITIONS

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

TEST LOAD CIRCUIT

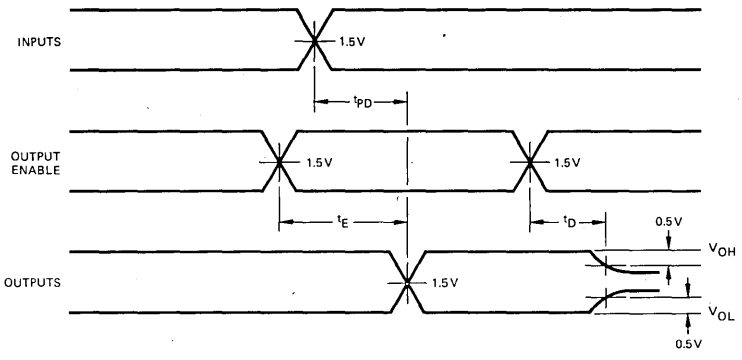


CAPACITANCE (Note 5)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		4.0	8.0	pF
C_{OUT1}	Output Capacitance			6.0	10	pF
C_{OUT2}	Output Capacitance			13	18	pF

Notes: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 180/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
3. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
4. DO outputs, C_L = 5.0pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 5.0pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
5. This parameter is periodically sampled and not 100% tested.

SWITCHING WAVEFORMS

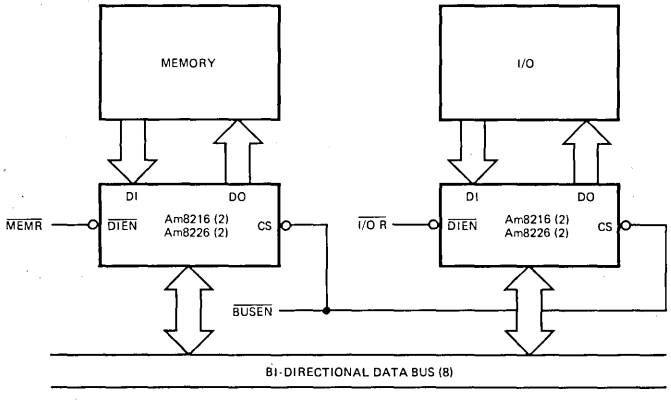


FUNCTION TABLE

$\overline{DIEN}$	$\overline{CS}$		8216 DB	8216 DO	8226 DB	8226 DO
L	L	DI ⇒ DB	DI	Z	$\overline{DI}$	Z
H	L	DB ⇒ DO	Z	DB	Z	$\overline{DB}$
L	H		Z	Z	Z	Z
H	H		Z	Z	Z	Z

H = HIGH
L = LOW

TYPICAL APPLICATION

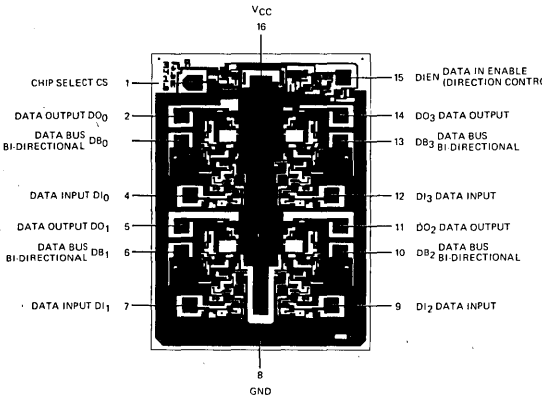


MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

4

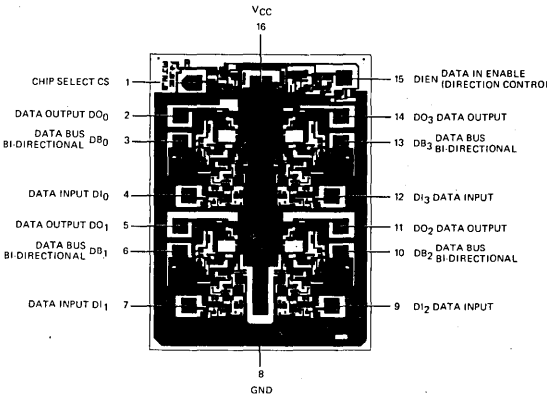
Metallization and Pad Layout

Am3216
Am8216



.DIE SIZE 0.066" X 0.090"

Am3226
Am8226



DIE SIZE 0.066" X 0.090"

Am54S/74S240 • Am54S/74S241
Am54S/74S242 • Am54S/74S243 • Am54S/74S244

Octal Buffers/Line Drivers/Line Receivers With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output propagation delay times:
  Inverting – 7.0ns MAX
  Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20 pin hermetic and molded DIP packages for Am54S/74S240, Am54S/74S241, and Am54S/74S244
- 14 pin hermetic and molded DIP packages for Am54S/74S242 and Am54S/74S243

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

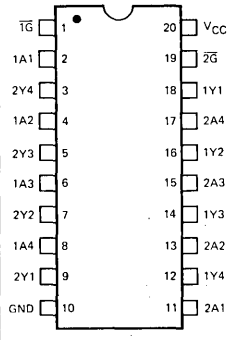
The Am54S/74S240, Am54S/74S241 and Am54S/74S244 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am54S/74S240 is inverting, while the Am54S/74S241 and Am54S/74S244 present true data at the outputs.

The Am54S/74S242 and Am54S/74S243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The Am54S/74S242 is inverting, while the Am54S/74S243 presents non-inverting data at the outputs.

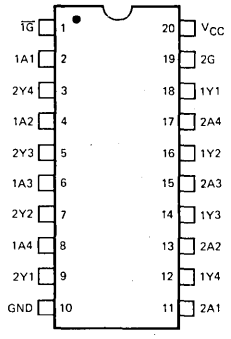
4

CONNECTION DIAGRAMS
Top Views

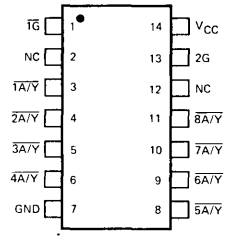
Am54S/74S240



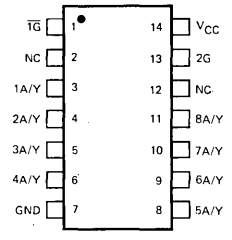
Am54S/74S241



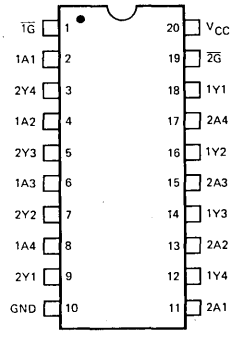
Am54S/74S242



Am54S/74S243



Am54S/74S244



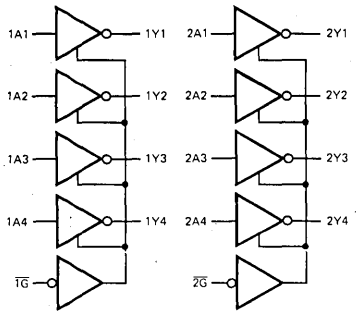
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

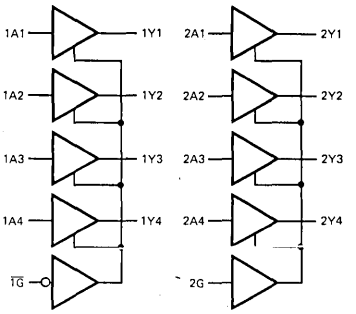
Package Type	Temperature Range	Order Number Am54S/74S240	Am54S/74S241	Am54S/74S242	Am54S/74S243	Am54S/74S244
Hermetic	–55°C to +125°C	SN54S240J	SN54S241J	SN54S242J	SN54S243J	SN54S244J
Dice	–55°C to +125°C	AM54S240X	AM54S241X	AM54S242X	AM54S243X	AM54S244X
Hermetic	0°C to +70°C	SN74S240J	SN74S241J	SN74S242J	SN74S243J	SN74S244J
Molded	0°C to +70°C	SN74S240N	SN74S241N	SN74S242N	SN74S243N	SN74S244N
Dice	0°C to +70°C	AM74S240X	AM74S241X	AM74S242X	AM74S243X	AM74S244X

LOGIC DIAGRAMS

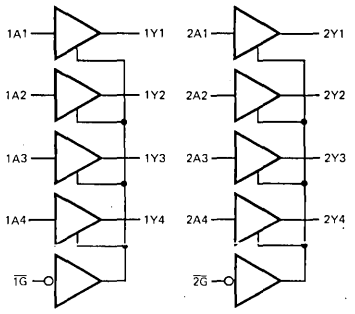
Am54S/74S240



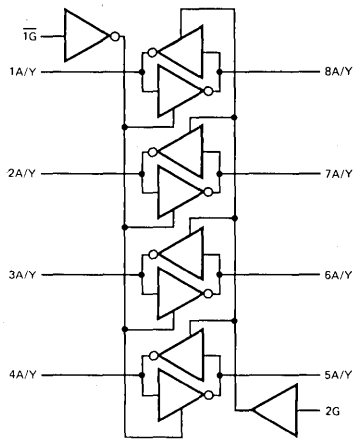
Am54S/74S241



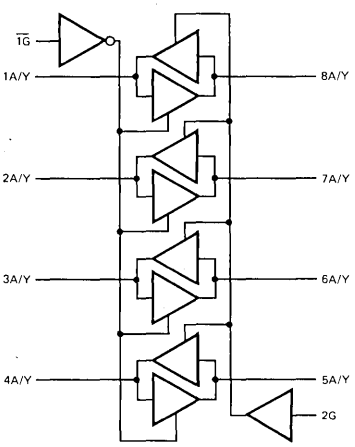
Am54S/74S244



Am54S/74S242



Am54S/74S243



Note: All gates have input hysteresis.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am54S240/S241/S242/S243/S244 (MIL) $T_A = -55°C$ to $+125°C$ V_{CC}(MIN.) = 4.50V V_{CC}(MAX.) = 5.50V
Am74S240/S241/S242/S243/S244(COM'L) $T_A = 0°C$ to $70°C$ V_{CC}(MIN.) = 4.75V V_{CC}(MAX.) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

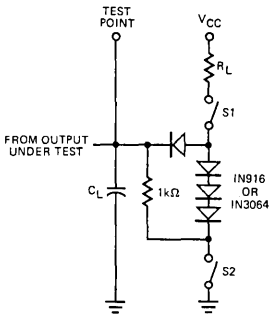
Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage				2.0			Volts
V_{IL}	Low-Level Input Voltage						0.8	Volts
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.2	Volts
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN.		0.2	0.4		Volts
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IL} = 0.8V, I_{OH} = −3.0mA		2.7	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	MIL, I_{OL} = 48mA			0.55	Volts
				COM'L, I_{OL} = 64mA			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = 0.8V	V_O = 2.4V			50	µA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.5V			−50	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 5.5V				1.0	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} = MAX., V_{IH} = 2.7V				50	µA
I_{IL}	Low-Level Input Current	Anny A	V_{CC} = MAX., V_{IL} = 0.5V				−400	µA
		Any G					−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)		V_{CC} = MAX.		−50		−225	mA
I_{CC}	Supply Current	Am54S/74S240 Am54S/74S242 — All Outputs High	V_{CC} = MAX. Outputs open	MIL		80	123	mA
				COM'L		80	135	
		Am54S/74S240 Am54S/74S242 — All Outputs High		MIL		100	145	
				COM'L		100	150	
		Am54S/74S240 Am54S/74S242 — Outputs at Hi-Z		MIL		100	145	
				COM'L		100	150	
		Am54S/74S241 Am54S/74S243 Am54S/74S244 — All Outputs High		MIL		95	147	mA
				COM'L		95	160	
		Am54S/74S241 Am54S/74S243 Am54S/74S244 — All Outputs High		MIL		120	170	
				COM'L		120	180	
		Am54S/74S241 Am54S/74S243 Am54S/74S244 — Outputs at Hi-Z		MIL		120	170	
				COM'L		120	180	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

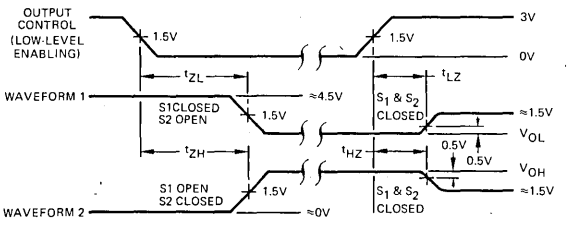
SWITCHING CHARACTERISTICS (V_{CC} = 5V, $T_A = 25°C$)

Parameter	Description	Test Conditions	Am54S/74S240 Am54S/74S242 Min.	Typ.	Max.	Am54S/74S241 Am54S/74S243 Am54S/74S244 Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 50pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

FUNCTION TABLES

Am54S/74S242

INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	L	H
L	H	H	L

Am54S/74240

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am54S/74S241
Am54S/74S243

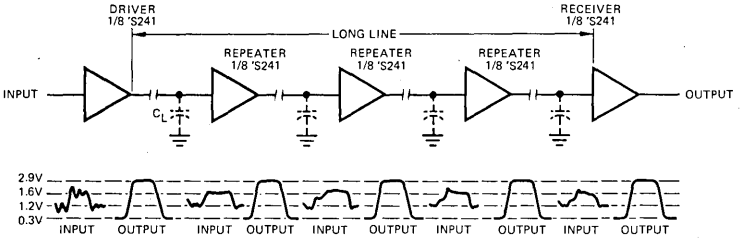
INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

Am54S/74S244

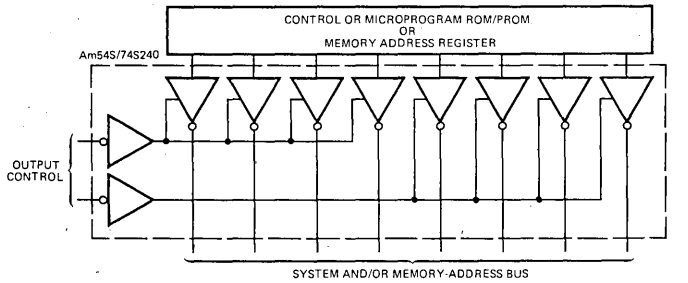
INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

APPLICATIONS

Am54/74S241'S USED AS REPEATER/LEVEL RESTORER

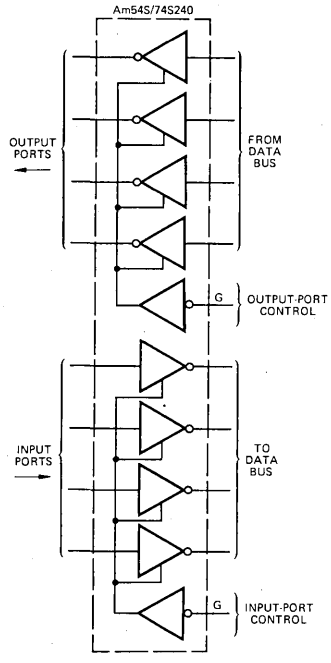


'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER— 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

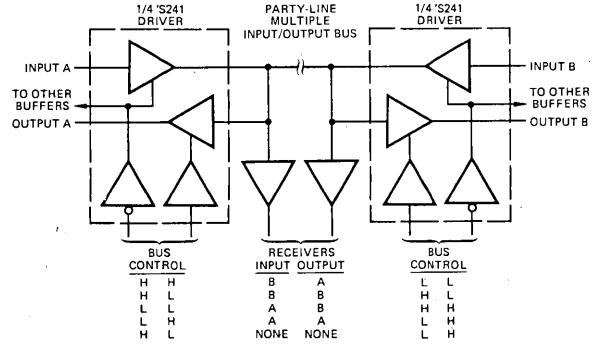


APPLICATIONS (Cont.)

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS



4

Am55/75107B • Am55/75108B

Dual Line Receivers

Distinctive Characteristics

- Input sensitivity 3mV typical
- Common mode range of ±3V
- Common mode range of more than ±15V using external attenuator
- TTL compatible output
- High common mode rejection ratio
- Blocking diodes provide high input impedance
- Strobe and gate inputs for flexibility
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am55/75107B and Am55/75108B are high speed dual line receivers designed for use as data receivers in balanced, unbalanced or party-line transmission systems. The two line receivers in each package share the common voltage and ground busses. The Am55/75107B has a standard active pull-up totem-pole output while the Am55/75108B has an open collector output for bus organized systems.

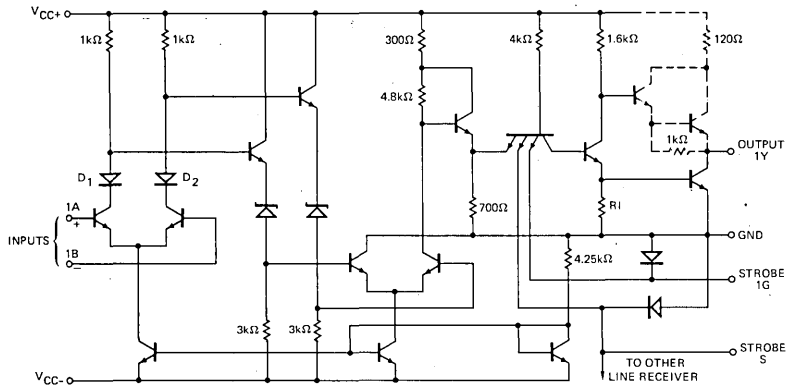
Each receiver has a high impedance differential input for minimum transmission line loading. The differential inputs of the Am55/75107B and Am55/75108B are designed to detect input signals of 25mV or greater and provide TTL compatible outputs.

All devices contain blocking diodes in the input differential transistor pair collectors to provide high input impedance in the power-off condition. The SN55/75107A and SN55/75108A are identical devices except for these input protection diodes.

Each receiver has a separate gate input, G. When the gate is LOW, the output is HIGH regardless of the other inputs. The device also has a common strobe, S, which can be used to gate both receivers simultaneously. When the strobe is LOW, the output is HIGH regardless of the other inputs.

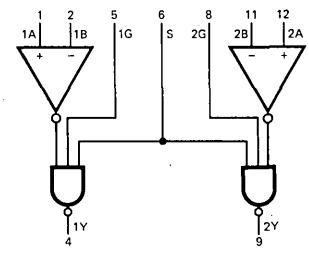
Note: Output HIGH on the Am55/75108B is high impedance condition.

SCHEMATIC DIAGRAM
(One Receiver Shown)



Notes: 1. Components shown with dashed lines are applicable to the Am55/75107B
2. RI = 1kΩ for Am55/75107B and 750Ω for Am55/75108B
3. D1 and D2 are the input protection diodes.

LOGIC SYMBOL

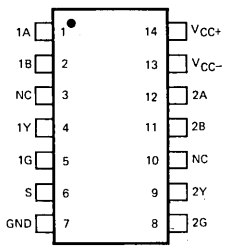


VCC- = Pin 13
VCC+ = Pin 14
GND = Pin 7

ORDERING INFORMATION

Package Type	Temperature Range	Am55/75107B Order Number	Am55/75108B Order Number
Molded DIP	0°C to +70°C	SN75107BN	SN75108BN
Hermetic DIP	0°C to +70°C	SN75107BJ	SN75108BJ
Dice	0°C to +70°C	AM75107BX	AM75108BX
Hermetic DIP	-55°C to +125°C	SN55107BJ	SN55108BJ
Dice	-55°C to +125°C	AM55107BX	AM55107BX

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7.0V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC+} max.
DC Input Voltage — Strobe	−0.5V to +5.5V
Differential Input Voltage	±6.0V
Common Mode Input Voltage (with Respect to GND Terminal)	±5.0V
Any Differential Input to Ground	−5.0V to +3.0V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am75107B, Am75108B (COM'L) $T_A = 0°C$ to $70°C$ $V_{CC+} = 5.0\ V \pm 5\%$ $V_{CC-} = -5.0\ V \pm 5\%$ (COM'L)

Am55107B, Am55108B (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC+} = 5.0\ V \pm 10\%$ $V_{CC-} = -5.0\ V \pm 5\%$ (MIL)

Parameters	Description	Test Conditions (Notes 1, 4, & 5)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Am55/75107B Only)	V_{CC+} = MIN., V_{CC-} = MIN. $I_{OH} = -400\mu A$, $V_{IC} = -3V$ to 3V		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OL} = 16mA, $V_{IC} = -3V$ to 3V				0.4	Volts
V_{IH}	Strobe or gate input HIGH Voltage	See Test Table		2.0			Volts
V_{IL}	Strobe or Gate Input LOW Voltage	See Test Table				0.8	Volts
V_{IDH}	Differential Input Voltage for Output HIGH	See Test Table		0.025		5.0	Volts
V_{IDL}	Differential Input Voltage for Output LOW	See Test Table		−5.0		−0.025	Volts
I_{IH}	Input HIGH Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. $V_{ID} = 0.5V$, $V_{IC} = -3V$ to 3V			30	75	μA
I_{IL}	Input LOW Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. $V_{ID} = -2V$, $V_{IC} = -3V$ to 3V				−10	μA
I_{IH}	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. $V_{IH} = 2.4V$	S			80	μA
			G			40	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. $V_{IH} = V_{CC+}$ MAX.	S			2	mA
			G			1	
I_{IL}	Input LOW Current	V_{CC+} = MAX., V_{CC-} = MAX. $V_{IL} = 0.4V$	S			−3.2	mA
			G			−1.6	
I_{OH}	HIGH Level Output Leakage (Am55/75108B Only)	V_{CC+} = MIN., V_{CC-} = MIN. $V_{OH} = V_{CC+}$ MAX.				250	μA
I_{SC}	Output Short Circuit Current (Note 3) (Am55/75107B Only)	V_{CC+} = MAX., V_{CC-} = MAX.		−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, $T_A = 25°C$			18	30	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, $T_A = 25°C$			−8.4	−15	mA
V_I	Input Clamp Voltage, S or G	V_{CC+} = MIN., V_{CC-} = MIN. $I_{IN} = -12mA$, $T_A = 25°C$			−1	−1.5	Volts

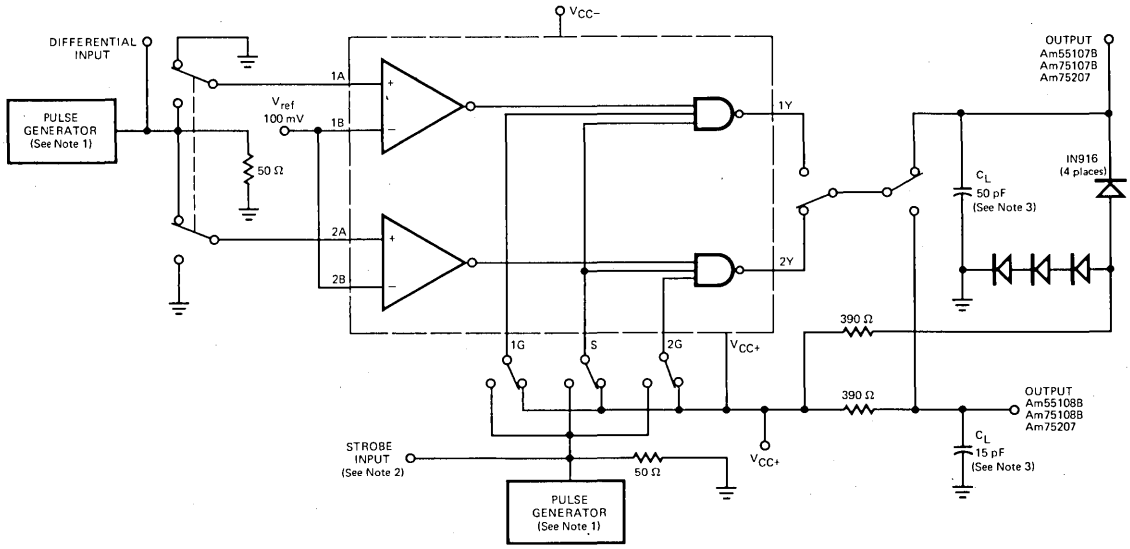
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC+} = 5.0V$, $V_{CC-} = -5.0V$, $T_A = 25°C$ ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. V_{IC} = common mode voltage with respect to GND terminal.
V_{ID} = differential voltage ($V_A - V_B$).

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC}+ = 5V, V_{CC}– = –5V)

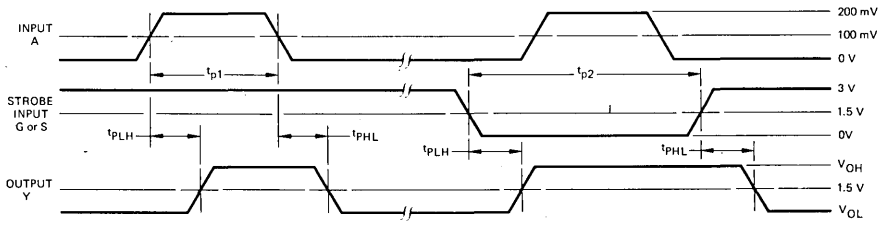
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
Am55/75107B Only						
t_{PLH}	A and B to Output	R_L = 390Ω, C_L = 50 pF		17	25	ns
t_{PHL}	A and B to Output			17	25	ns
t_{PLH}	G or S to Output			10	15	ns
t_{PHL}	G or S to Output			8	15	ns
Am55/75108B Only						
t_{PLH}	A and B to Output	R_L = 390Ω, C_L = 15 pF		19	25	ns
t_{PHL}	A and B to Output			19	25	ns
t_{PLH}	G or S to Output			13	20	ns
t_{PHL}	G or S to Output			13	20	ns

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



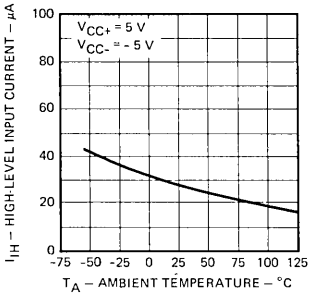
VOLTAGE WAVEFORMS



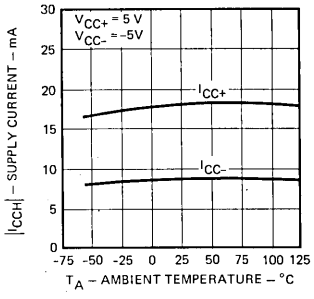
Notes:
1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = t_f = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A – 1B are being tested, to Strobe S when inputs 1A – 1B or 2A – 2B are being tested, and to Strobe 2G when inputs 2A – 2B are being tested.
3. C_L includes probe and jig capacitance.

PERFORMANCE CURVES

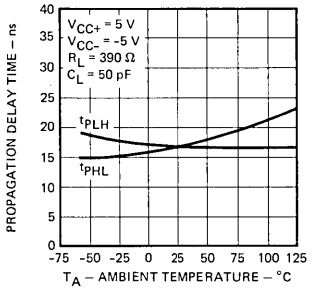
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



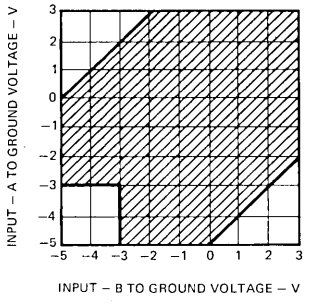
High-Logic-Level Supply Current Versus Ambient Temperature



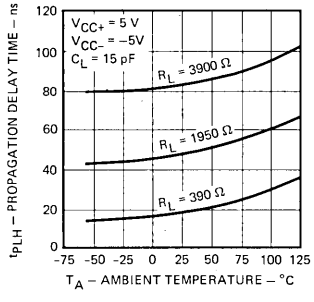
Am55107B, Am75107B Propagation Delay Time Differential Inputs Versus Ambient Temperature



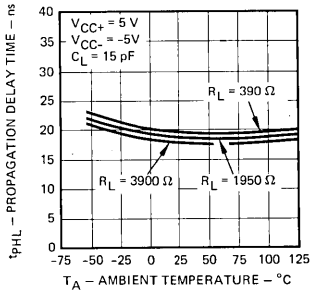
Recommended Combinations of Input Voltage for Line Receivers



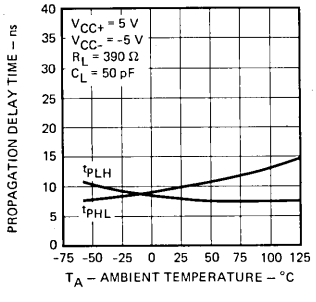
Am55108B, Am75108B Propagation Delay Time Low-to-High Level Differential Inputs Versus Ambient Temperature



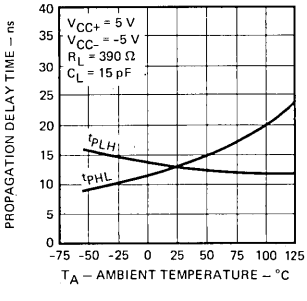
Am55108B, Am75108B Propagation Delay Time High-to-Low Level Differential Inputs Versus Ambient Temperature



Am55107B, Am75107B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Am55108B, Am75108B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Note: Use 0°C to +70°C temperature range only for commercial (Am75 Series) devices.

FUNCTION TABLE

Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs		Output
	Gate	Strobe	
	G	S	Y
$V_{ID} \geq +25mV$	X	X	H
$-25mV < V_{ID} < +25mV$	H	H	?
$V_{ID} \leq -25mV$	H	H	L
X	L	X	H
X	X	L	H

H = HIGH
L = LOW
X = Don't Care
? = Don't Know

Note: For Am75207 and Am75208 substitute 10mV for 25mV.

DEFINITION OF FUNCTIONAL TERMS

1A, 2A The non-inverting input of the line receivers.

1B, 2B The inverting input of the line receivers.

1Y, 2Y The output of each line receiver.

1G, 2G The gate input of each line receiver. A LOW on the gate input forces the output HIGH.

S The strobe input that is common to both line receivers. A LOW on the strobe forces both (1Y and 2Y) outputs HIGH.

V_{IC} Input Common Mode voltage with respect to ground terminal.

V_{ID} Differential Input voltage ($V_A - V_B$).

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

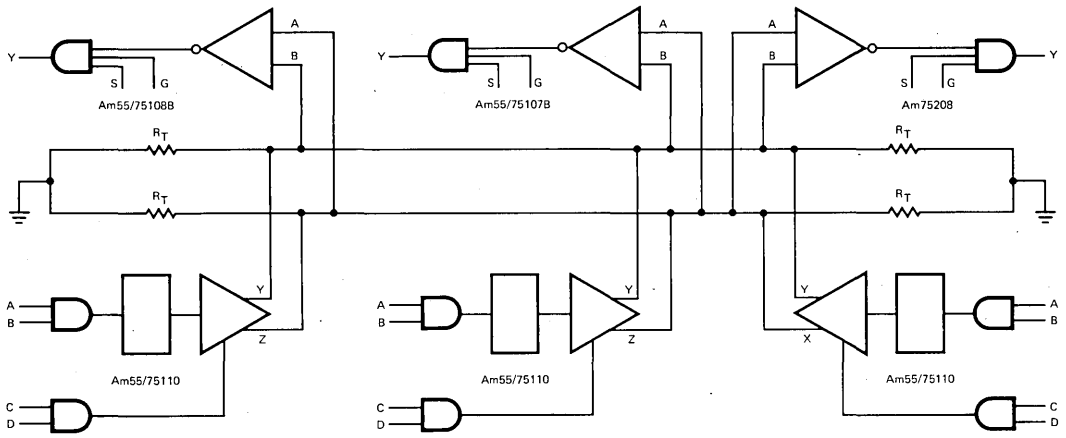
DC TEST TABLE

Parameter	1A	2A	1B 2B	V_{IC} (Common Mode)	V_{ID} (Differential)	1Y 2Y	1G	2G	S	Note
V_{IDH}	–		–	−3V to 3V	Test	−400μA (Note 2)	+5V		+5V	1
V_{IDL}	–		–	−3V to 3V	Test	16mA	+5V		+5V	1
I_{IH} @ A	–		–	−3V to 3V	+0.5V	Open	Open		Open	1
I_{IL} @ A	–		–	−3V to 3V	−2V	Open	Open		Open	1
V_{OL} @ Y	–		–	−3V to 3V	−25mV	16mA	V_{IH}		V_{IH}	1
V_{OH} @ Y	–		–	−3V to 3V	+25mV	−400μA	V_{IH}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	−3V to 3V	−25mV	−400μA	V_{IL}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	−3V to 3V	−25mV	−400μA	V_{IH}		V_{IL}	1 & 2
I_{OH} @ Y	–		–	−3V to 3V	+25mV	V_{CC+}MAX.	V_{IH}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	−3V to 3V	−25mV	V_{CC+}MAX.	V_{IL}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	−3V to 3V	−25mV	V_{CC+}MAX.	V_{IH}		V_{IL}	1 & 3
I_{IH} @ 1G	+25mV	GND	GND	–	–	Open	V_{IH}	GND	GND	–
I_{IH} @ 2G	GND	+25mV	GND	–	–	Open	GND	V_{IH}	GND	–
I_{IH} @ S	+25mV	+25mV	GND	–	–	Open	GND	GND	V_{IH}	–
I_{IL} @ 1G	−25mV	GND	GND	–	–	Open	V_{IL}	GND	4.5V	–
I_{IL} @ 2G	GND	−25mV	GND	–	–	Open	GND	V_{IL}	4.5V	–
I_{IL} @ S	−25mV	−25mV	GND	–	–	Open	4.5V	4.5V	V_{IL}	–
I_{OS} @ Y	+25mV		GND	–	–	GND	GND		GND	–
I_{CC+}	+25mV		GND	–	–	Open	+5V		+5V	–
I_{CC-}	+25mV		GND	–	–	Open	+5V		+5V	–

Notes: 1. When testing one channel, the inputs of the other channels are grounded.
2. Am55/75107B only.
3. Am55/75108B only.

APPLICATIONS

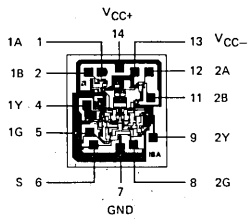
BUS-ORGANIZED SYSTEM



4

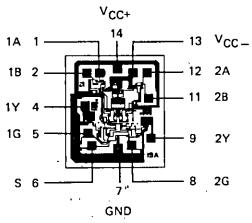
Metallization and Pad Layouts

Am55/75107B



DIE SIZE: 0.049" X 0.056"

Am55/75108B



DIE SIZE: 0.049" X 0.056"

Am55/75109 • Am55/75110

Dual Line Drivers

Distinctive Characteristics

- Input is TTL compatible.
- High common-mode output range of −3V to +10V.
- Separate and common output inhibits.
- Open-collector differential outputs for bus-organized systems.
- 100% reliability assurance testing in compliance with MIL-STD-883.

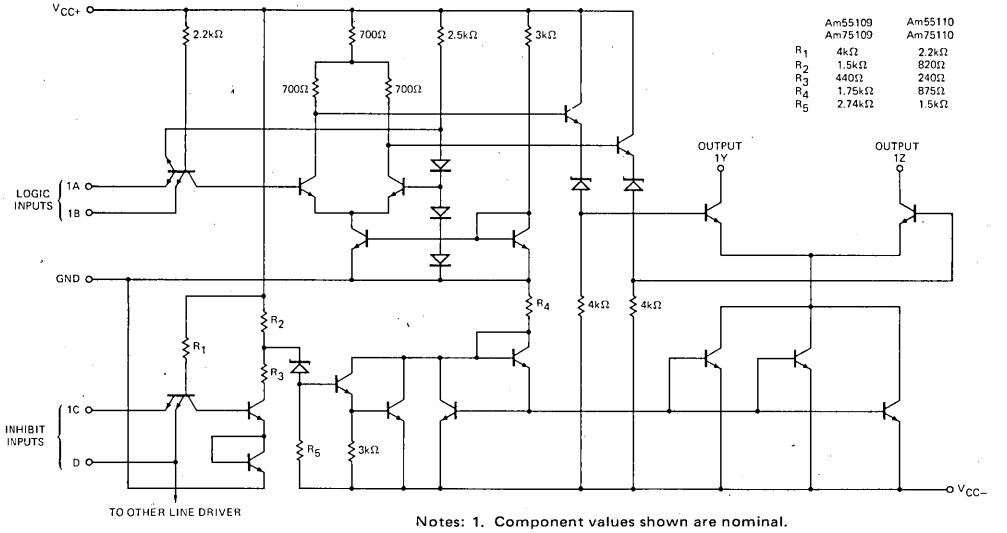
FUNCTIONAL DESCRIPTION

The Am55/75109 and Am55/75110 are dual line drivers characterized for applications in balanced, unbalanced, and party-line systems. The drivers provide a constant current output that is switched to either of the two differential output terminals under the control of the A and B inputs. When A and B are HIGH, the Y output is HIGH and Z output is LOW

These drivers feature a separate inhibit input, C, that is used to switch off the constant current output. This leaves the driver differential output in the high impedance state for use in bus organized systems. A LOW on the C input forces the driver to the OFF state by switching off the current source of the differential output transistor pair. Likewise, the two drivers have a common inhibit input, D, that forces both drivers to the OFF state. A LOW on the D inputs turns off the output current sources of both drivers such that both differential outputs are in the high impedance state.

The driver outputs have a common mode voltage range of −3V to +10V. The Am55/75109 output current is typically 6mA while the Am55/75110 output current is typically 12mA.

SCHEMATIC DIAGRAM
(One Driver Shown)

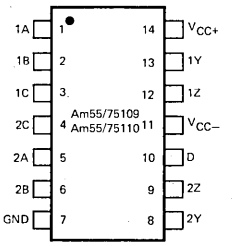


Notes: 1. Component values shown are nominal.
2. Resistance values are in ohms.

ORDERING INFORMATION

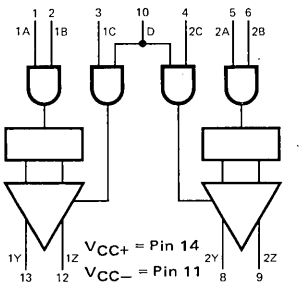
Package Type	Temperature Range	Am55/75109 Order Number	Am55/75110 Order Number
Molded DIP	0°C to +70°C	SN75109N	SN75110N
Hermetic DIP	0°C to +70°C	SN75109J	SN75110J
Dice	0°C to +70°C	AM75109X	AM75110X
Hermetic DIP	−55°C to +125°C	SN55109J	SN55110J
Dice	−55°C to +125°C	AM55109X	AM55110X

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC+} Supply Voltage to Ground Potential	+7V
V_{CC-} Supply Voltage to Ground Potential	−7V
Common Mode DC Voltage Applied to Outputs	−5V to +12V
DC Input Voltage	−0.5V to +V_{CC+}max.
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am75109, Am75110 V_{CC+} MIN. = 4.75V V_{CC+} MAX. = 5.25V, V_{CC-} MIN. = −4.75V V_{CC-} MAX. = −5.25V; T_A = 0°C to +70°C
Am55109, Am55110 V_{CC+} MIN. = 4.5V V_{CC+} MAX. = 5.5V, V_{CC-} MIN. = −4.5V V_{CC-} MAX. = −5.5V; T_A = −55°C to +125°C

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		5.5	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		0		0.8	Volts
I_{IL} (Note 3)	Input Low Current Am55/75109	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B			−3	mA
			C			−1.6	
			D			−3	
I_{IL} (Note 3)	Input LOW Current Am55/75110	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B, C			−3	mA
			D			−6	
I_{IH} (Note 3)	Input HIGH Current	V_{CC+} = MAX., V_{IN} = 2.4 V, V_{CC-} = MAX.	A, B, C			40	µA
			D			80	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{IN} = MAX., V_{CC-} = MAX.	A, B, C			1	mA
			D			2	
$I_{O(on)}$	Output Current On-State	V_{CC+} = MAX., V_{CC-} = MAX.	109			7	mA
			110			15	
$I_{O(on)}$	Output Current On-State	V_{CC+} = MIN., V_{CC-} = MAX.	109	3.5			mA
			110	6.5			
$I_{O(off)}$	Output Current Off-State	V_{CC+} = MIN., V_{CC-} = MIN.				100	µA
$I_{CC+(on)}$	Positive Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		18	30	mA
			110		23	35	
$I_{CC-(on)}$	Negative Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		−18	−30	mA
			110		−34	−50	
$I_{CC+(off)}$	Positive Supply Current; Driver Disabled	All Inputs = 0.4V	109		18		mA
			110		21		
$I_{CC-(off)}$	Negative Supply Current; Driver Disabled	All Inputs = 0.4V	109		−10		mA
			110		−17		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A or B to Y or Z	V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, R_L = 50Ω, C_L = 40 pF		9	15	ns
t_{PHL}	A or B to Y or Z			9	15	ns
t_{PLH}	C or D to Y or Z			16	25	ns
t_{PHL}	C or D to Y or Z			13	25	ns

FUNCTION TABLE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH
L = LOW
ON = I_O(on) Current
OFF = I_O(off) Current
X = Don't Care

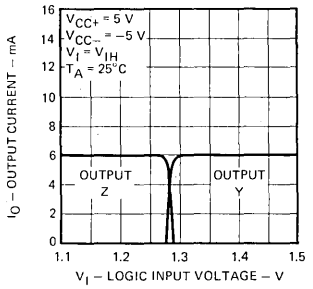
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load Am55/75109	Input Unit Load Am55/75110	Fan-out Output HIGH	Fan-out Output LOW
1A	1	1-7/8	1-7/8	–	–
1B	2	1-7/8	1-7/8	–	–
1C	3	1	1-7/8	–	–
2C	4	1	1-7/8	–	–
2A	5	1-7/8	1-7/8	–	–
2B	6	1-7/8	1-7/8	–	–
GND	7	–	–	–	–
2Y	8	–	–	(Diff output)	
2Z	9	–	–		
D	10	1-7/8	3-3/4	–	–
V_{CC-}	11	–	–	–	–
1Z	12	–	–	(Diff output)	
1Y	13	–	–		
V_{CC+}	14	–	–	–	–

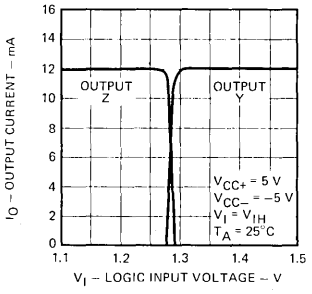
A TTL Unit Load is defined as 40 μA measured at 2.4 V HIGH and −1.6mA measured at 0.4 V LOW.

PERFORMANCE CURVES
(Typical)

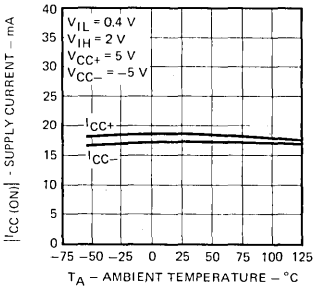
Am55109, Am75109
Output Current
Versus
Logic Input Voltage



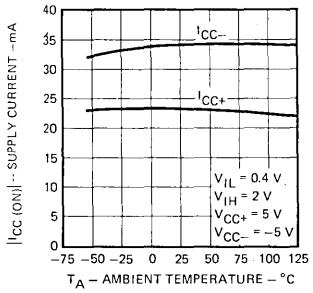
Am55110, Am75110
Output Current
Versus
Logic Input Voltage



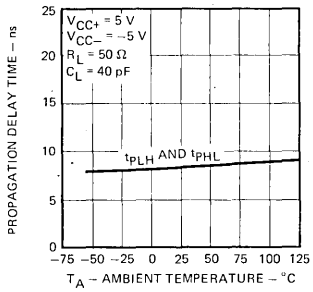
Am55109, Am75109
Supply Current With Driver Enabled
Versus
Ambient Temperature



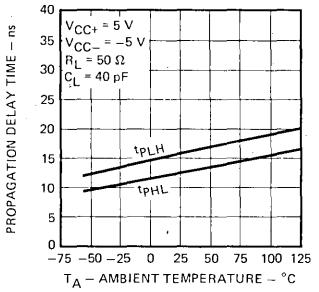
Am55110, Am75110
Supply Current With Driver Enabled
Versus
Ambient Temperature



Propagation Delay Time
Logic Inputs
Versus
Ambient Temperature



Propagation Delay Time
Inhibit Inputs
Versus
Ambient Temperature



Note: For Am75 Series use 0°C to +70°C temperature range only.

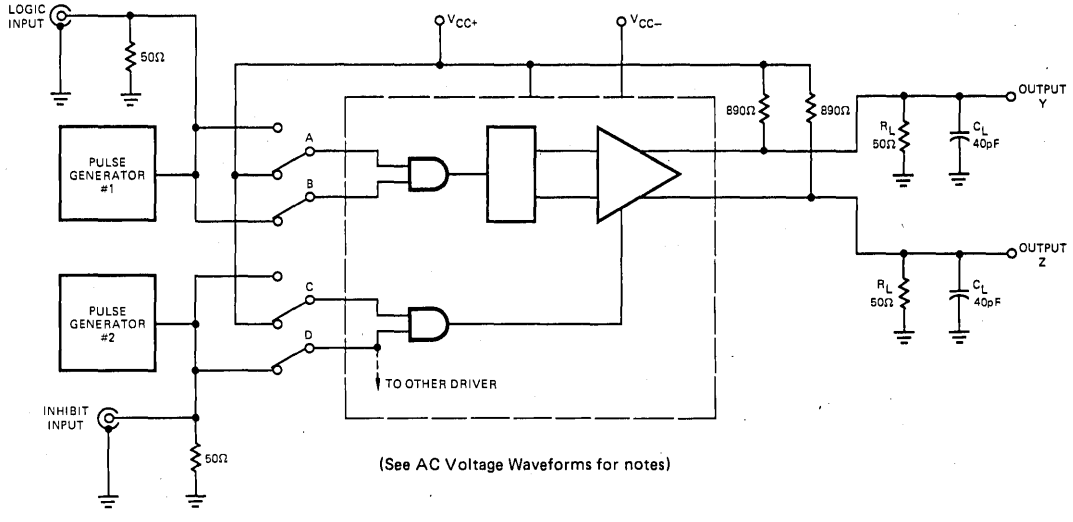
DC TEST TABLE

Parameter	INPUTS A	B	C	D	OUTPUTS Y	Z
V_{IH}	Test	Open	V_{IH}	V_{IH}	OFF	ON
V_{IH}	Open	Test	V_{IH}	V_{IH}	OFF	ON
V_{IL}	Test	V_{CC+}	V_{IH}	V_{IH}	ON	OFF
V_{IL}	V_{CC+}	Test	V_{IH}	V_{IH}	ON	OFF
I_{IH}	Test	GND	V_{IH}	V_{IH}	GND	GND
I_{IH}	GND	Test	V_{IH}	V_{IH}	GND	GND
I_{IL}	Test	4.5V	V_{IH}	V_{IH}	GND	GND
I_{IL}	4.5V	Test	V_{IH}	V_{IH}	GND	GND
V_{IH}	V_{IH}	V_{IH}	Test	Open	OFF	ON
V_{IH}	V_{IH}	V_{IH}	Open	Test	OFF	ON
V_{IH}	V_{IL}	V_{IL}	Test	Open	ON	OFF
V_{IH}	V_{IL}	V_{IL}	Open	Test	ON	OFF
V_{IL}	V_{IH}	V_{IH}	Test	Open	OFF	OFF
V_{IL}	V_{IH}	V_{IH}	Open	Test	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	Test	V_{CC+}	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	V_{CC+}	Test	OFF	OFF
I_{IH}	GND	GND	Test	GND	GND	GND
I_{IH}	GND	GND	GND	Test	GND	GND
I_{IL}	GND	GND	Test	4.5V	GND	GND
I_{IL}	GND	GND	4.5V	Test	GND	GND
$I_{O(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(off)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IL}	Test	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IH}	Test	Test
$I_{O(off)}$	X	X	V_{IH}	V_{IL}	Test	Test
$I_{CC+(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC-(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC+(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND
$I_{CC-(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND

X = Don't Care; Note 1: Output not under test must have a low impedance (<50Ω) termination to GND.

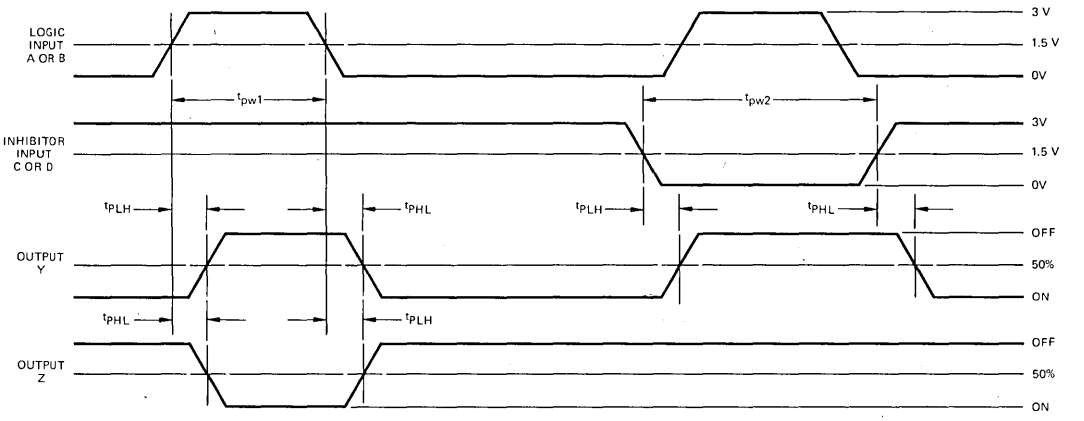
AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



(See AC Voltage Waveforms for notes)

AC VOLTAGE WAVEFORMS



Notes: 1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5$ns; $t_{pw1} = 500$ns, PRR = 1 MHz; $t_{pw2} = 1\mu$s, PRR = 500kHz.

2. C_L includes probe and jig capacitance.

3. For simplicity, only one channel and the inhibitor connections are shown.

UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

DEFINITION OF FUNCTIONAL TERMS

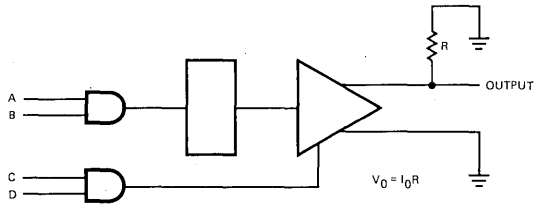
1A, 2A, 1B, 2B The TTL data inputs to each driver.

1C, 2C The TTL inhibit inputs to each driver. A LOW input forces both outputs to the off-state.

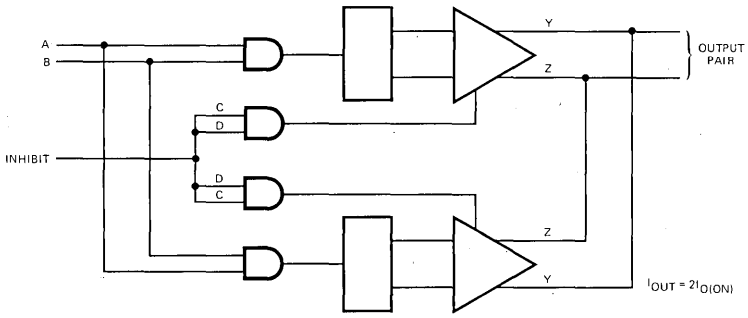
D The common TTL inhibit input to both drivers. A LOW input forces all four outputs to the off-state.

1Y, 2Y, 1Z, 2Z The differential output of each driver.

APPLICATIONS



Am55/75109 or Am55/75110 in a unbalanced or single-ended connection.

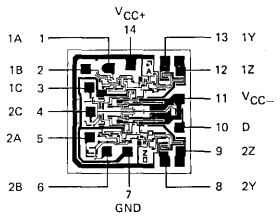


Two line drivers connected in parallel for higher current.

4

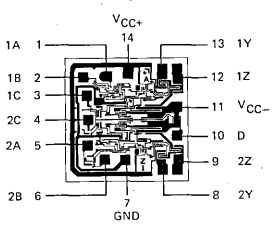
Metallization and Pad Layouts

Am55/75109



DIE SIZE 0.056" X 0.056"

Am55/75110



DIE SIZE 0.056" X 0.056"

Am78/8820·Am78/8820A

Dual Differential Line Receivers

Distinctive Characteristics:

- Dual differential receiver pin-for-pin equivalent to the National 78/8820 and 78/8820A
- 500mV sensitivity at ±3V common mode
  1V sensitivity at ±15V common mode
- Single 5-volt supply
- Frequency response control, strobe and internal terminating resistor
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

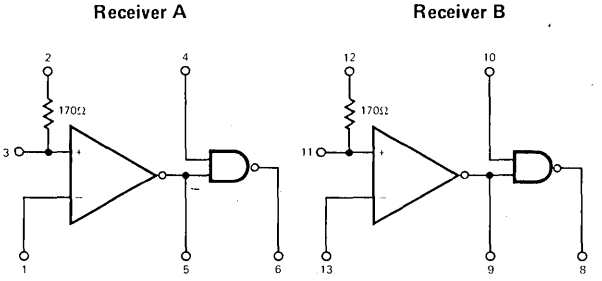
The Am78/8820 and Am78/8820A are dual differential line receivers designed to receive digital data from transmission lines and provide up to 15 volts of common mode rejection with a single 5-volt supply.

The device would normally be used in systems using twisted pair lines for connection, with each receiver having a terminating resistor included. The receivers respond to small differential signals and reject considerable amounts of common mode noise.

Each receiver has a strobe that enables the output and a response control that allows the time constant of the output circuit to be controlled by an external capacitor and give noise rejection of high frequency noise and short logic spikes.

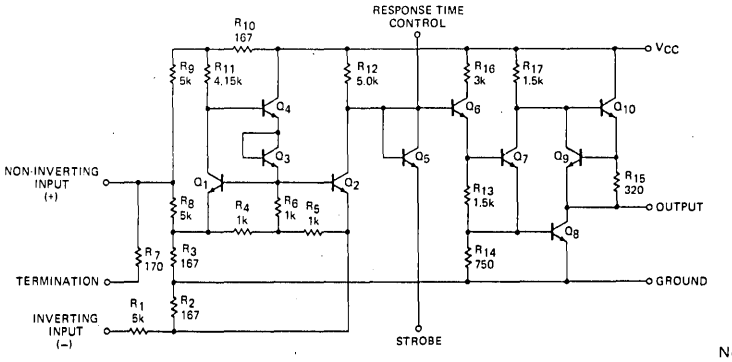
Companion differential line drivers are the Am78/8830, Am78/8831 and Am78/8832.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

CIRCUIT DIAGRAM

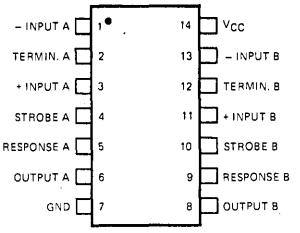


Note: Only one receiver shown.

ORDERING INFORMATION

Package Type	Temperature Range	Am78/8820 Order Number	Am78/8820A Order Number
Molded DIP	0°C to +75°C	DM8820N	DM8820AN
Hermetic DIP	0°C to +75°C	DM8820J	DM8820AJ
Dice	0°C to +75°C	AM8820X	AM8820AX
Hermetic DIP	–55°C to +125°C	DM7820J	DM7820AJ
Hermetic Flat Pak	–55°C to +125°C	DM7820W	DM7820AW
Dice	–55°C to +125°C	AM7820X	AM7820AX

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am7820 • Am8820

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8820A	$T_A = 0°C$ to $+75°C$	$V_{CC} = 5.0V \pm 5\%$	$V_{CM} = -15V$ to $+15V$
Am7820A	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	$V_{CM} = -15V$ to $+15V$

Parameters	Description	Test Conditions	Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} \leq 0.2mA$	2.5	4.0	5.5	Volts
V_{OL}	Output LOW Voltage	$I_{OL} \leq 3.5mA$	0		0.4	Volts
V_{TH}	Differential Threshold Voltage	$V_{CM} = 0V$		+0.06	+0.5	Volts
		$-15V \leq V_{CM} \leq +15V$		+0.06	+1.0	
		$V_{CM} = 0V$	−0.5	−0.08		
		$-15V \leq V_{CM} \leq +15V$	−1.0	−0.08		
I_{IH}	Strobe Input HIGH Current	$V_{STROBE} = 5.5V$		0.01	5.0	μA
I_{IL}	Strobe Input LOW Current	$V_{STROBE} = 0.4V$	−1.4	−1.0		mA
$I_{IN\ INV}$	Inverting Input Current	$V_{CM} = +15V$		+3.0	+4.2	mA
		$V_{CM} = 0V$	−0.5	0		
		$V_{CM} = -15V$	−4.2	−3.0		
$I_{IN\ NINV}$	Non-Inverting Input Current	$V_{CM} = +15V$		+5.0	+7.0	mA
		$V_{CM} = 0V$	−1.6	−1.0		
		$V_{CM} = -15V$	−9.8	−7.0		
I_{CC}	Power Supply Current (Each Receiver)	$V_{CM} = +15V$		+3.9	+7.0	mA
		$V_{CM} = 0V$		+6.5	+10.2	
		$V_{CM} = -15V$		+8.3	+15.0	
$R_{IN\ INV}$	Inverting Input Resistance		3.6	5.0		kΩ
$R_{IN\ NINV}$	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_{TERM}	Input Terminating Resistor	$T_A = 25°C$	120	170	250	Ω

Notes: 1. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the AM7820, or 150°C/W and 115°C maximum junction temperature for the AM8820.
2. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{RESP}	Response Time	$C_{delay} = 0$		40		ns
t_{RESP}	Response Time	$C_{delay} = 100\ pF$		150		ns

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		−65°C to +150°C
Temperature (Ambient) Under Bias		−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous		−0.5 V to +8.0 V
DC Common Mode Voltage		−20 V to +20 V
DC Strobe Input Voltage		−0.5 V to +8.0 V
DC Data Input Voltage		−20 V to +20 V
Output Current, Into Outputs:	Am78/8820	25 mA
	Am78/8820A	50 mA
Power Dissipation (Note 1)		600 mW

Am7820A • Am8820A

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8820A $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0V \pm 5\%$ $V_{CM} = -15V$ to $+15V$
Am7820A $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ $V_{CM} = -15V$ to $+15V$

Parameters	Description	Test Conditions	Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{DIFF} = +1V$, $I_{OH} = -400\mu A$	2.5	4.0	5.5	Volts
V_{OL}	Output LOW Voltage	$V_{DIFF} = -1V$				Volts
V_{IH}	Strobe Input HIGH Level Voltage	$V_{DIFF} = -3V$ $V_{OUT} \leq 0.4V$, $I_{OUT} = 16mA$	2.1			Volts
V_{IL}	Strobe Input LOW Level Voltage	$V_{DIFF} = -3V$ $V_{OUT} \geq 2.5V$, $I_{OUT} = -400\mu A$			0.9	Volts
V_{TH}	Differential Threshold Voltage	$-3V \leq V_{CM} \leq +3V$, $I_{OUT} = -400\mu A$		+0.06	+0.5	Volts
		$-15V \leq V_{CM} \leq +15V$, $I_{OUT} = -400\mu A$		+0.06	+1.0	
		$-3V \leq V_{CM} \leq +3V$, $I_{OUT} = 16mA$	−0.5	−0.08		
		$-15V \leq V_{CM} \leq +15V$, $I_{OUT} = 16mA$	−1.0	−0.08		
I_{IH}	Strobe Input HIGH Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = +3V$		0.01	5.0	μA
I_{IL}	Strobe Input LOW Current	$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$	−1.4	−1.0		mA
$I_{IN\ INV}$	Inverting Input Current	$V_{CM} = +15V$		+3.0	+4.2	mA
		$V_{CM} = 0V$	−0.5	0		
		$V_{CM} = -15V$	−4.2	−3.0		
$I_{IN\ NINV}$	Non-Inverting Input Current	$V_{CM} = +15V$		+5.0	+7.0	mA
		$V_{CM} = 0V$	−1.6	−1.0		
		$V_{CM} = -15V$	−9.8	−7.0		
I_{SC}	Output Short Circuit Current	$V_{OUT} = 0V$, $V_{STROBE} = 0V$, $V_{CC} = 5.5V$	−6.7	−4.5	−2.8	mA
I_{CC}	Power Supply Current (Each Receiver)	$V_{CM} = +15V$, $V_{DIFF} = -1V$		+3.9	+6.0	mA
		$V_{CM} = 0V$, $V_{DIFF} = -0.5V$		+6.5	+10.2	
		$V_{CM} = -15V$, $V_{DIFF} = -1V$		+9.2	+14.0	
$R_{IN\ INV}$	Inverting Input Resistance		3.6	5.0		kΩ
$R_{IN\ NINV}$	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_{TERM}	Input Terminating Resistor	$T_A = 25°C$	120	170	250	Ω

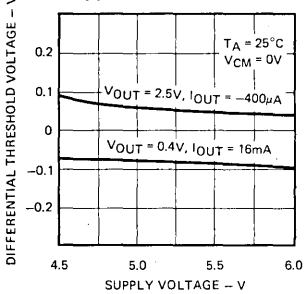
Notes: 1. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the AM7820A, or 150°C/W and 115°C maximum junction temperature for the AM8820A.
2. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

Switching Characteristics ($T_A = 25°C$)

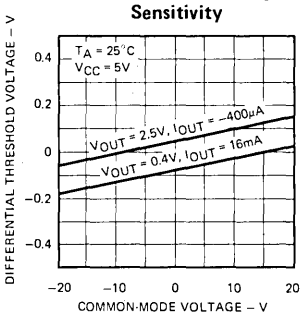
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Differential Input to Output LOW	$V_{CC} = 5.0$ V See Switching Waveforms		25	45	ns
t_{PLH}	Differential Input to Output HIGH			22	40	ns
t_{PHL}	Strobe Input to Output LOW			16	25	ns
t_{PLH}	Strobe Input to Output HIGH			15	30	ns

TYPICAL PERFORMANCE CHARACTERISTICS

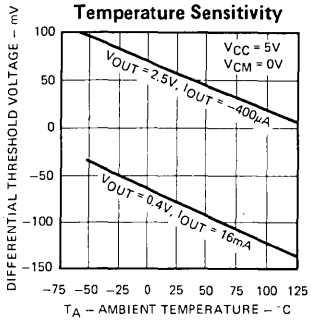
Supply Voltage Sensitivity



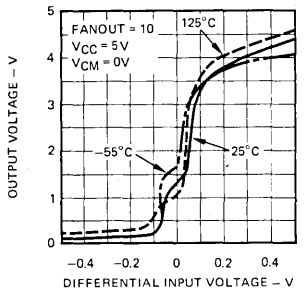
Common-Mode Voltage Sensitivity



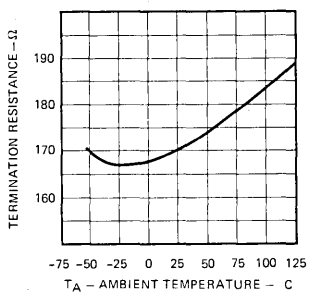
Temperature Sensitivity



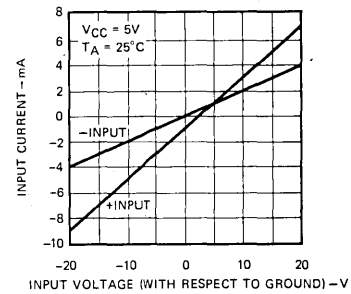
Transfer Function



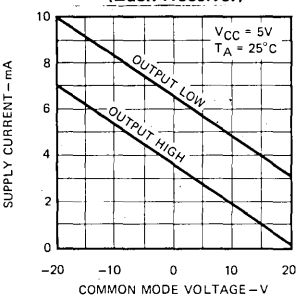
Termination Resistance



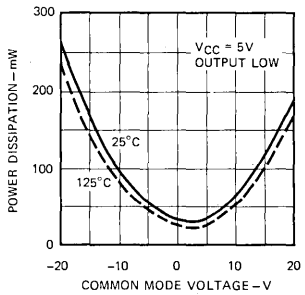
Input Characteristics



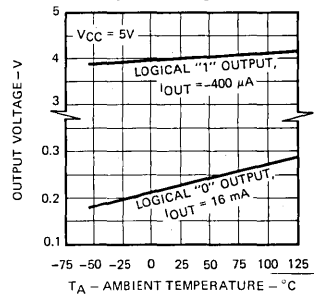
Power Supply Current (Each Receiver)



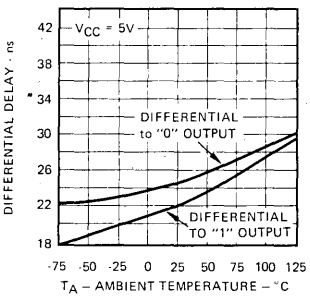
Internal Power Dissipation (Each Receiver)



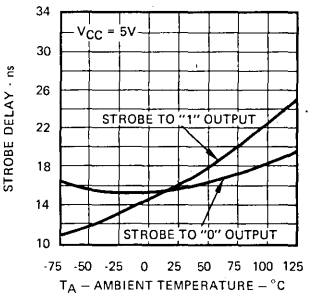
Output Voltage Levels



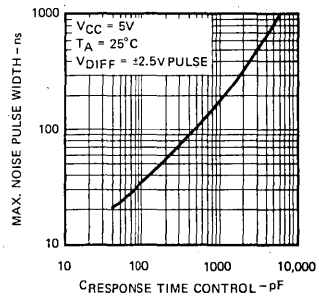
Differential Input Delays



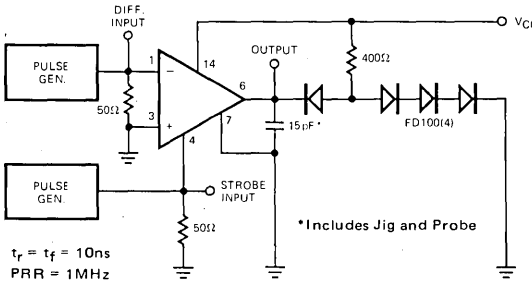
Strobe Delays

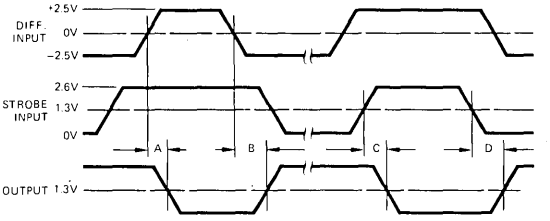


Noise Rejection



AC TEST CIRCUIT AND WAVEFORMS

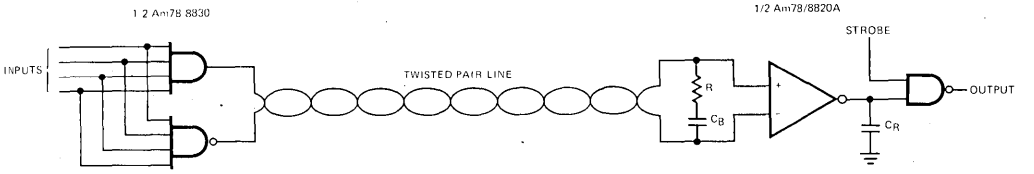




A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

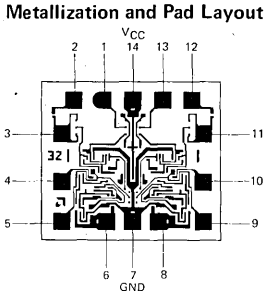
TYPICAL APPLICATION

TYPICAL TWISTED PAIR DIFFERENTIAL COMMUNICATION SYSTEM



The Am78/8830 drives a twisted pair line which is terminated at the receiving end by an RC network. The R is approximately equal to the line impedance (170Ω) and is part of the Am78/8820A differential receiver. The C_B is a blocking capacitor which stops DC current flow, and for low duty cycles reduces power consumption. The value of this capacitor depends upon the data rate, C_B must be large compared to $\frac{1}{fd \cdot R}$ where fd is the data rate. The capacitor C_R is used to control the response time of the receiver and limit high frequency noise. $C_R \sim 4 \times 10^3 \frac{1}{fn}$ where C is in pF and fn is the lowest noise frequency expected in MHz.

Metallization and Pad Layout



DIE SIZE 0.045" X 0.050"

Am78/8830

Dual Differential Line Driver

Distinctive Characteristics

- Single 5-volt power supply
- Input diodes for prevention of line ringing
- Low output skew between NAND and AND propagation delays
- Clamped outputs for reduction in positive and negative voltage transients.
- 100% reliability assurance testing in compliance with MIL-STD-883.

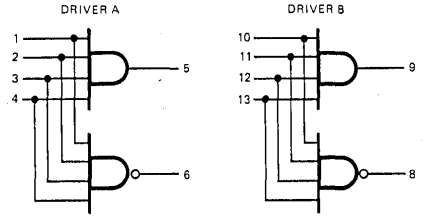
FUNCTIONAL DESCRIPTION

The Am78/8830 is a dual differential line driver suitable for driving differential lines with characteristic impedances in the range 50Ω to 500Ω.

Each driver consists of a 4-input AND gate in parallel with a 4-input NAND gate. The inputs to the gates are clamped to reduce the effect of line transients. The differential outputs are balanced and have approximately the same delay so as to minimize skew problems, and have high drive capability at both the LOW and HIGH logic levels.

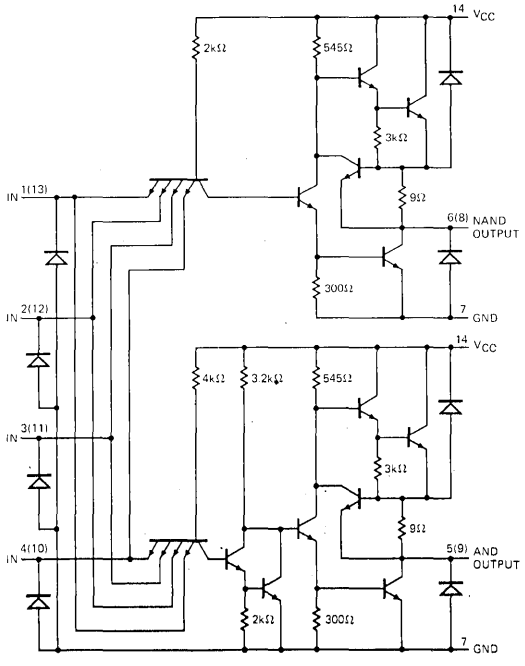
The device is ideal for driving differential transmission lines, and forms a very noise insensitive balanced digital communication system with excellent common mode noise rejection when used in conjunction with the Am78/8820A dual differential receiver.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

CIRCUIT DIAGRAM

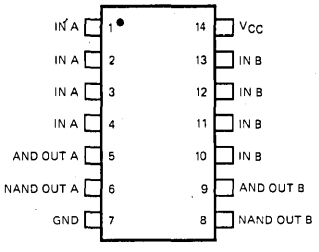


Note: Only one driver shown

Am78/8830 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	DM8830N
Ceramic DIP	0°C to +75°C	DM8830J
Hermetic DIP	–55°C to +125°C	DM7830J
Hermetic Flat Pak	–55°C to +125°C	DM7830W
Dice	0°C to +75°C	AM8830X
Dice	–55°C to +125°C	AM7830X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA
Output Short Circuit Duration at 125°C	1 sec

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8830 T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am7830 T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = 0.8V	I_{OH} = −40mA	1.8	2.9		Volts
			I_{OH} = −0.8mA	2.4	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = 0.8V	I_{OL} = 40mA		0.22	0.5	Volts
			I_{OL} = 32mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			−3.0	−4.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				120	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				2.0	mA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = 5.0V, V_{OUT} = 0.0V		−40	−100	−120	mA
I_{CC}	Power Supply Current*	V_{CC} = MAX. (Each Driver)			11	18	mA

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 2. Limits for T_A = +125°C only.

Switching Characteristics (T_A = 25°C)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs to Output of AND Gate	V_{CC} = 5.0V, C_L = 15pF See Figure 1		8	12	ns
t_{PHL}				11	18	ns
t_{PLH}	Delay from Inputs to Output of NAND gate			8	12	ns
t_{PHL}				5	8	ns
t_1	Differential Delay	V_{CC} = 5.0V, C_L = 5000pF R_L = 100Ω, See Figure 2		12	16	ns
t_2				12	16	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT

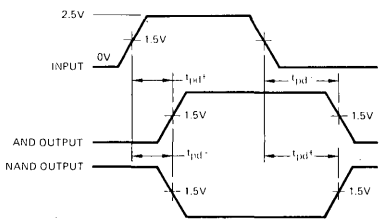


Figure 1.

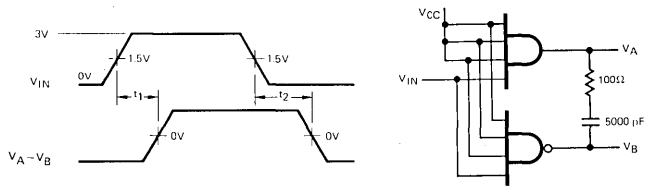
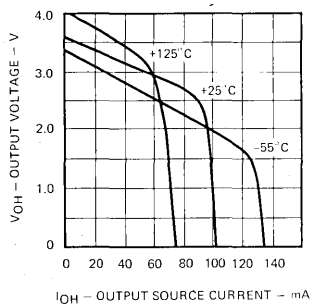


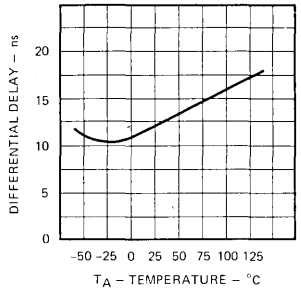
Figure 2.

TYPICAL ELECTRICAL CHARACTERISTICS

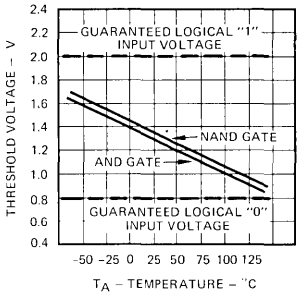
Output High Voltage Versus Output Current



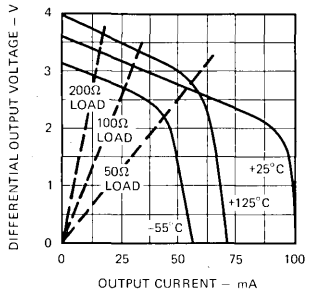
Differential Delay Versus Temperature



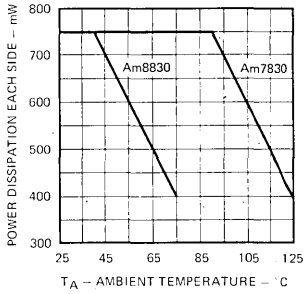
Threshold Voltage Versus Temperature



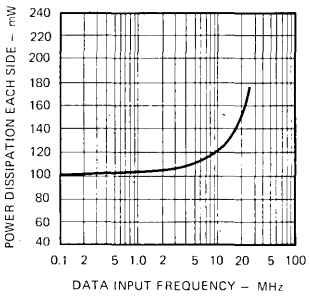
Differential Output Voltage $V_{AND} - V_{NAND}$ Versus Differential Output Current



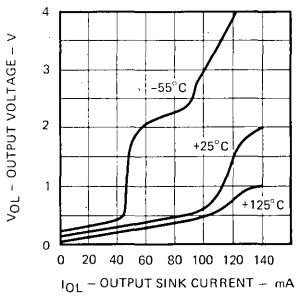
Maximum Power Dissipation



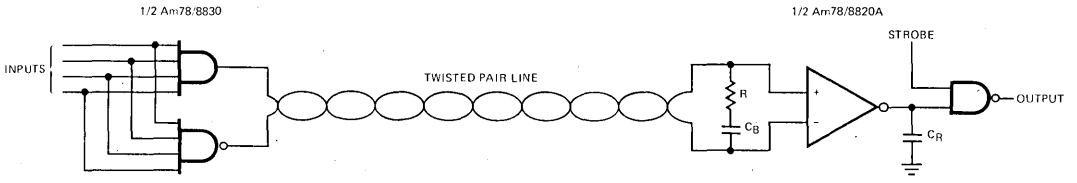
Power Dissipation (No Load) Versus Data Input Frequency



Output Low Voltage Versus Output Current



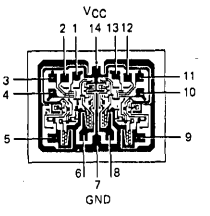
APPLICATIONS



TYPICAL TWISTED PAIR DIFFERENTIAL COMMUNICATION SYSTEM

The Am78/8830 drives a twisted pair line which is terminated at the receiving end by an RC network. The R is approximately equal to the line impedance (170Ω) and is part of the Am78/8820A differential receiver. The C_B is a blocking capacitor which stops DC current flow, and for low duty cycles reduces power consumption. The value of this capacitor depends upon the data rate, C_B must be large compared to $\frac{1}{fd \cdot R}$ where fd is the data rate. The capacitor C_R is used to control the response time of the receiver and limit high frequency noise. $C_R \sim 4 \times 10^3 \frac{1}{fn}$ where C is in pF and fn is the lowest noise frequency expected in MHz.

Metallization and Pad Layout



DIE SIZE 0.050" x 0.063"

Am78/8831•Am78/8832

Three-State Line Driver

Distinctive Characteristics

- Three-State Line Drivers pin-for-pin equivalent to the DM78/8831 and DM78/8832
- Mode control for quad single-ended or dual differential operation
- Common bus operation
- High-drive capability
- 40mA sink and source current
- Series 54/74 compatible
- 13ns typical propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

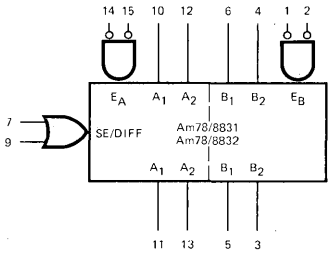
The Am78/8831 and Am78/8832 line drivers can be used either as a quad single-ended driver or as a dual differential driver. Each driver has a three-state output making the device particularly suitable for party-line operation where several drivers are directly connected to the same bus. The Am78/8832 does not have the V_{CC} clamp diodes found on the Am74/8831.

When used for single-ended operation the two differential/single-ended control inputs are held LOW. The device then operates as four independent non-inverting drivers. For differential working at least one differential/single-ended control input is held HIGH. The A-channel inputs are connected together and the B-channel inputs are connected together. Signal inputs will then pass non-inverted to the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

For party-line operation outputs of different channels are tied together, and outputs of all channels except one are forced into the third high impedance state by having at least one of the channel disable inputs HIGH. The channel that is enabled has both channel disable inputs LOW, and the low-output impedance of this output at both logic levels controls the level of the bus, provides good capacitance drive and insures good waveform integrity.

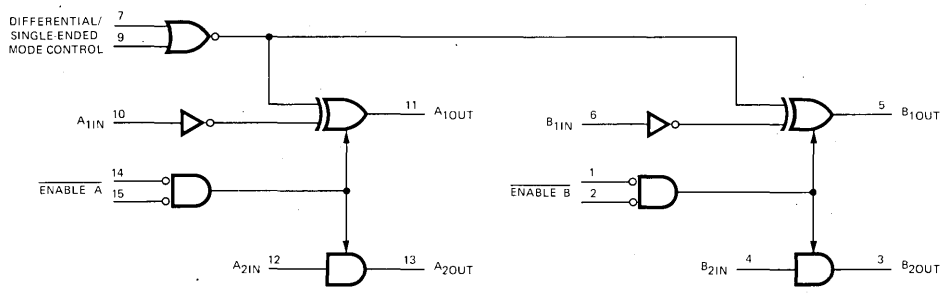
The channel which is enabled can conveniently be selected by a decoding matrix using Am9301 1-of-10 or Am9311 1-of-16 active LOW output decoders. The high drive capability at both logic levels enables drivers to drive a low impedance line and still supply the inverse leakage current of several disabled drivers.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

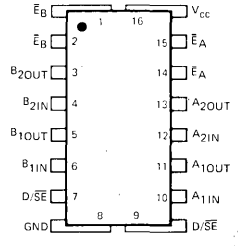
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am78/8831 Order Number	Am78/8832 Order Number
Molded DIP	0°C to +75°C	DM8831N	DM8832N
Hermetic DIP	0°C to +75°C	DM8831J	DM8832J
Dice	0°C to +75°C	AM8831X	AM8832X
Hermetic DIP	–55°C to +125°C	DM7831J	DM7832J
Hermetic Flat Pak	–55°C to +125°C	DM7831W	DM7832W
Dice	–55°C to +125°C	AM7831X	AM8832X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA
Time that 2 Bus-Connected Devices May Be in Opposite Low Impedance States Simultaneously	∞

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8831, Am8832	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V	
Am7831, Am7832	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V	

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −40 mA	1.8	2.8		Volts
			Am7831, 32 I_{OH} = −2 mA	2.4	3.1		
			Am8831, 32 I_{OH} = −5.2 mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 40 mA		0.29	0.5	Volts
			I_{OL} = 32 mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_L	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 2.4 V			5	40	μA
		V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 0.4 V			−5	−40	
V_I	Input Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
V_O	Output Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = 12 mA, T_A = 25°C Am78/8831 Only				V_{CC} + 1.5V	Volts
V_O	Output Substrate Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V, T_A = MAX.		−40		−120	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			57	90	mA

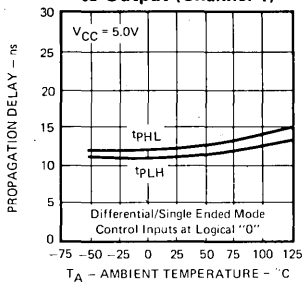
Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Only one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°)

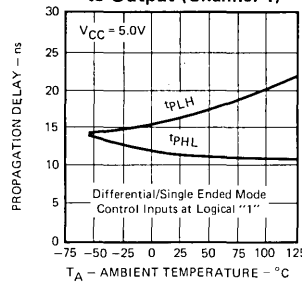
Parameters	Description	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs A_1, A_2, B_1, B_2 and Single-Ended/ Diff. Control to Output		13	25	ns
t_{PHL}			13	25	ns
t_{HZ}	Delay from Output Enable to Output		6	12	ns
t_{LZ}			14	22	ns
t_{ZH}	Delay from Output Enable to Output		14	22	ns
t_{ZL}			18	27	ns

TYPICAL PERFORMANCE CHARACTERISTICS

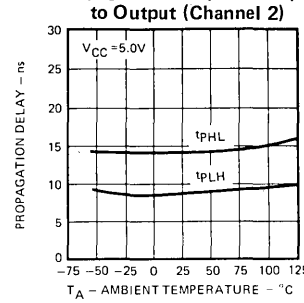
Propagation Delay from Input to Output (Channel 1)



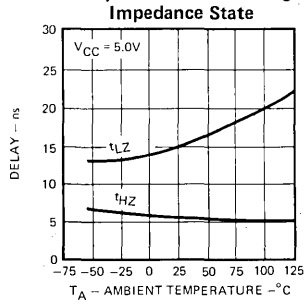
Propagation Delay from Input to Output (Channel 1)



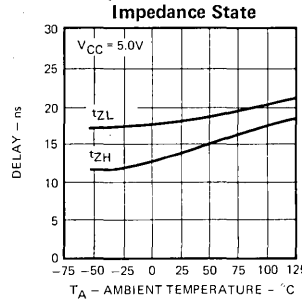
Propagation Delay from Input to Output (Channel 2)



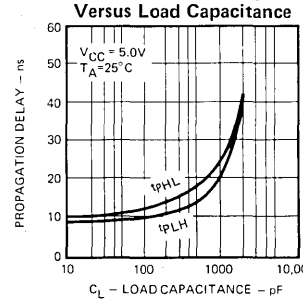
Delay from Disable to High Impedance State



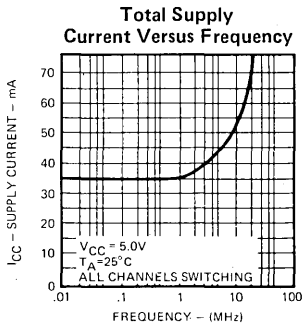
Delay from Disable to Low Impedance State



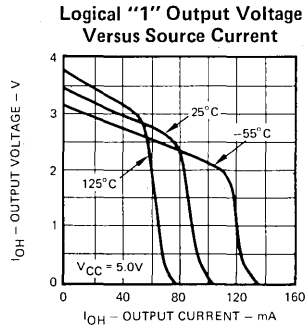
Propagation Delay Versus Load Capacitance



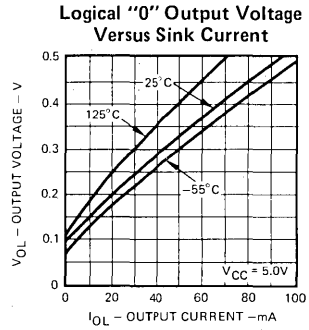
Total Supply Current Versus Frequency



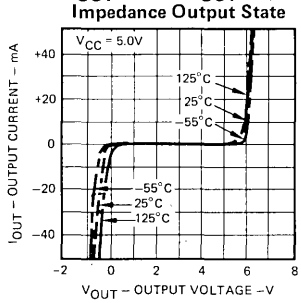
Logical "1" Output Voltage Versus Source Current



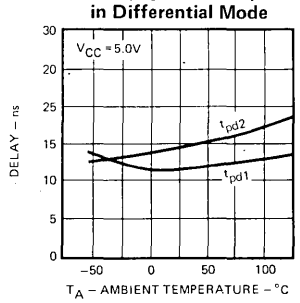
Logical "0" Output Voltage Versus Sink Current

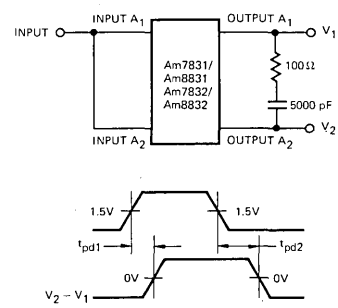


I_{OUT} Versus V_{OUT} High Impedance Output State



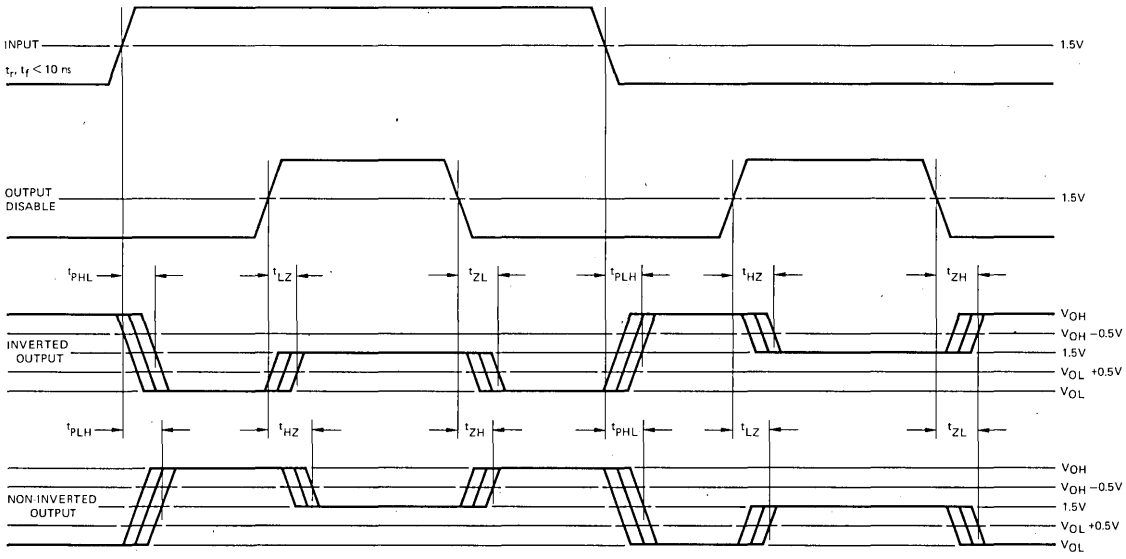
Propagation Delay in Differential Mode





4

SWITCHING TIME WAVEFORMS AND TEST CIRCUIT

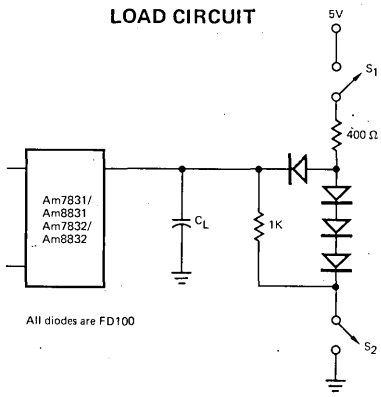


NOTE: V_{OL} and V_{OH} refer to actual voltages on output LOW and HIGH states.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY	▒▒▒	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
▒▒▒	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L	><><	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
▒▒▒	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

LOAD CIRCUIT



	Switch S_1	Switch S_2	C_L
t_{PLH}	closed	closed	50 pF
t_{PHL}	closed	closed	50 pF
t_{HZ}	closed	closed	* 5 pF
t_{LZ}	closed	closed	* 5 pF
t_{ZL}	closed	open	50 pF
t_{ZH}	open	closed	50 pF

*Jig Capacitance

TRUTH TABLE
(Shown for A Channels Only)

SINGLE-ENDED/ DIFF CONTROL		A ENABLE		IN A_1	OUT A_1	IN A_2	OUT A_2
L	L	L	L	A_1	A_1	A_2	A_2
H	X	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	H	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	X	H	X	X	F	X	F
X	X	X	H	X	F	X	F

H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
F = Floating Output

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

LOADING RULES (In Unit Loads)

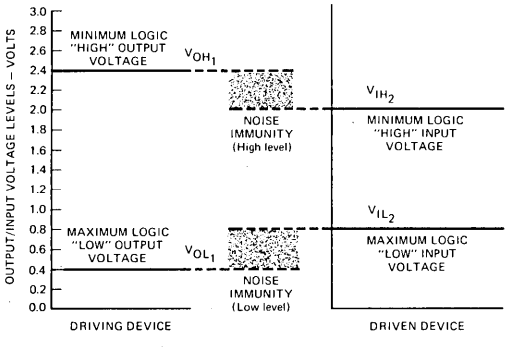
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{\text{Enable B}}$	1	1	–	–
$\overline{\text{Enable B}}$	2	1	–	–
B_2 Out	3	–	1000	25
B_2 In	4	1	–	–
B_1 Out	5	–	1000	25
B_1 In	6	1	–	–
$\overline{\text{SE}}$/Diff	7	1	–	–
GND	8	–	–	–
$\overline{\text{SE}}$/Diff	9	1	–	–
A_1 In	10	1	–	–
A_1 Out	11	–	1000	25
A_2 In	12	1	–	–
A_2 Out	13	–	1000	25
$\overline{\text{Enable A}}$	14	1	–	–
$\overline{\text{Enable A}}$	15	1	–	–
V_{CC}	16	–	–	–

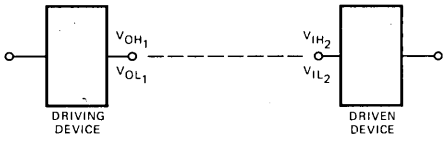
TABLE II

4

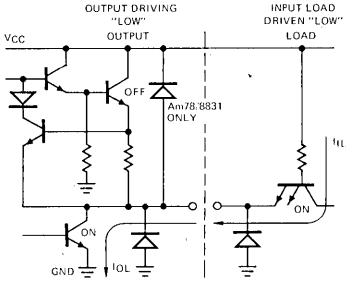
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions – LOW & HIGH

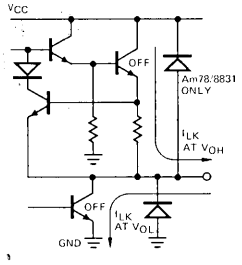




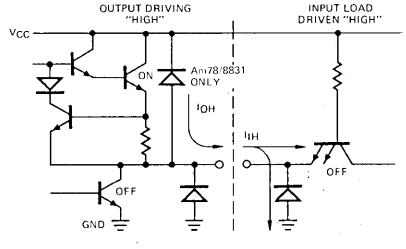
Current Interface Conditions – LOW



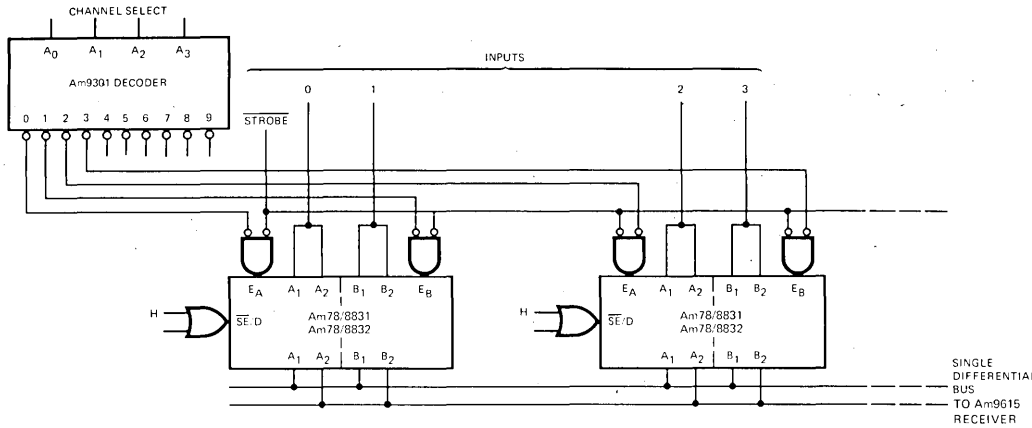
Current Interface Conditions – FLOATING



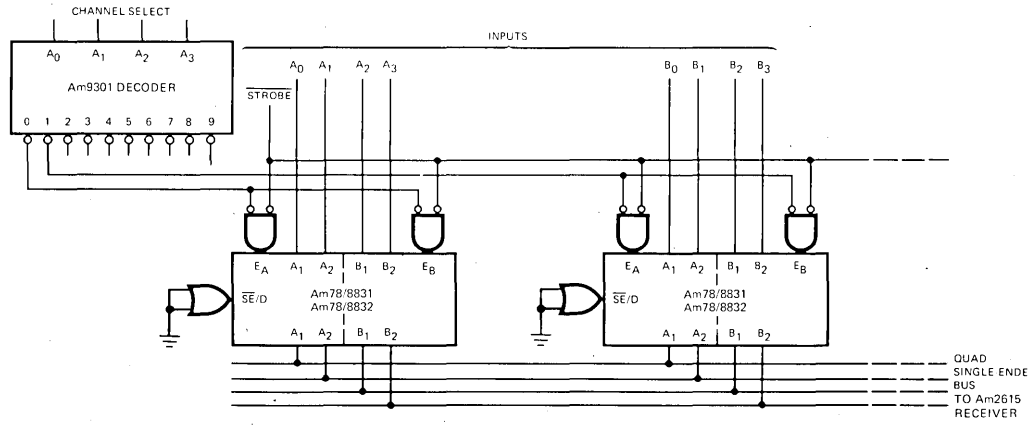
Current Interface Conditions – HIGH



APPLICATIONS

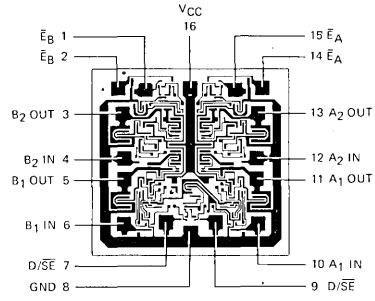


PARTY LINE DIFFERENTIAL OPERATION



PARTY LINE SINGLE-ENDED OPERATION

Metallization and Pad Layout



DIE SIZE 0.057" X 0.058"

Am7838 • Am8838

Quad Unified Bus Transceiver

DISTINCTIVE CHARACTERISTICS

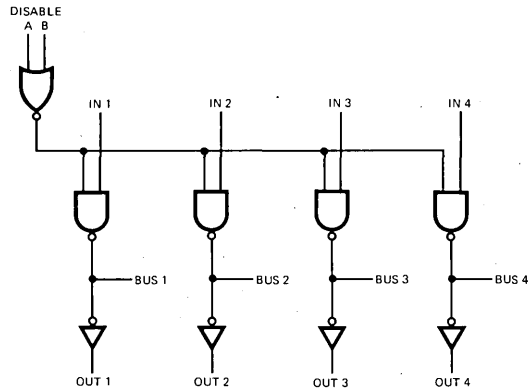
- 4 totally separate driver/receiver pairs per package.
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High-Speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs
- Advanced Schottky processing

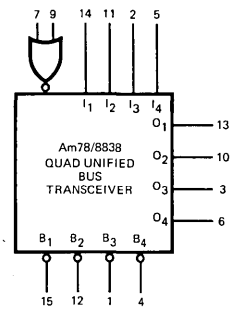
FUNCTIONAL DESCRIPTION

The Am7838 • Am8838 are quad high-speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ≤ 1.0μs/V.

4

LOGIC DIAGRAM AND LOGIC SYMBOL



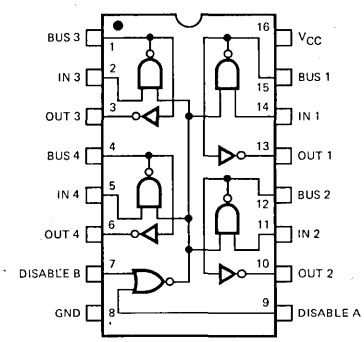


V_{CC} = PIN 16
GND = PIN 8

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DS7838J
Hermetic DIP	0°C to +70°C	DS8838J
Molded DIP	0°C to +70°C	DS8838N

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input and Output Voltage	5.5V
Power Dissipation	600mW
Operating Temperature Range	
Am7838	−55°C to +125°C
Am8838	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

Am7838 (MIL)	T_A = −55°C to +125°C	V_{CC}MIN = 4.50V	V_{CC}MAX = 5.50V
Am8838 (COM'L)	T_A = 0°C to +70°C	V_{CC}MIN = 4.75V	V_{CC}MAX = 5.25V

Driver and Disable Inputs

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage					0.8	Volts
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1.0	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12mA, I_{IN} = −12mA, I_{BUS} = −12mA, T_A = 25°C			−1.0	−1.5	Volts

Driver Output/Receiver Input

V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2.0V, I_{BUS} = 50mA			0.4	0.7	Volts
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4.0V, V_{CC} = $V_{MAX.}$			20	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4.0V, V_{CC} = 0V			2.0	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16mA	Am7838	1.65	2.25	2.65	Volts
			Am8838	1.80	2.25	2.50	
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	Am7838	0.97	1.30	1.63	Volts
			Am8838	1.05	1.30	1.55	

Receiver Output

V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA	2.4			Volts
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4.0V, I_{OL} = 16mA		0.25	0.4	Volts
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = $V_{MAX.}$ (Note 3)	−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2.0V, (Per Package)		50	70	mA

AC CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C unless otherwise specified)

t_{pd}	Propagation Delays	Disable to Bus "1"	(Note 4)		19	30	ns
		Disable to Bus "0"	(Note 4)		15	23	ns
		Driver Input to Bus "1"	(Note 4)		17	25	ns
		Driver Input to Bus "0"	(Note 4)		9.0	15	ns
		Bus to Logical "1" Receiver Output	(Note 5)		20	30	ns
		Bus to Logical "0" Receiver Output	(Note 6)		18	30	ns

Notes:
1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max. or min. on absolute value basis.
3. Only one output at a time should be shorted.
4. 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, C_{LOAD} = 15pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3.0V pulse.
5. Fan-out of 10 load, C_{LOAD} = 15pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.
6. Fan-out of 10 load, C_{LOAD} = 15pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Am8T26

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 40mA driver sink current
- Three-state outputs on driver and receiver
- PNP inputs
- 20ns max. driver propagation delay
- 18ns max. receiver propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

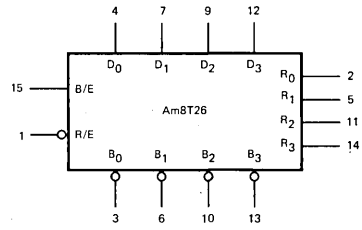
FUNCTIONAL DESCRIPTION

The Am8T26 is a high speed bus transceiver consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

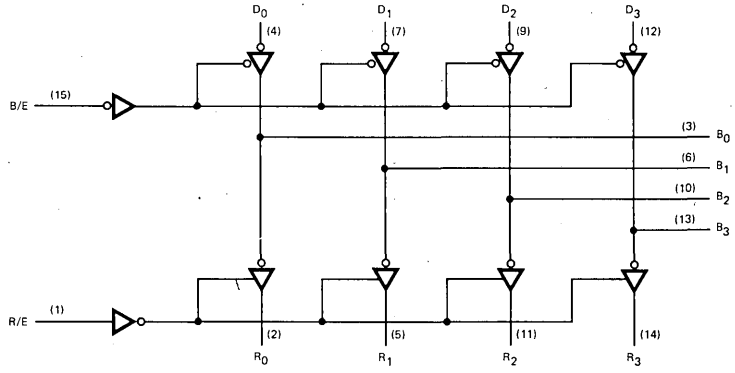
A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

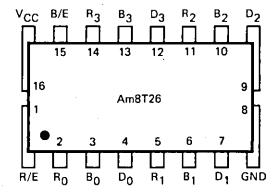
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N8T26B
Hermetic DIP	0°C to +75°C	N8T26F
Dice	0°C to +75°C	AM8T26XC
Hermetic DIP	−55°C to +125°C	S8T26F
Dice	−55°C to +125°C	AM8T26XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

N8T26 T_A = 0°C to +75°C
S8T26 T_A = −55°C to +125°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Driver Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA V_{IN} = V_{IH} or V_{IL}		2.6	3.1		Volts
V_{OL}	Driver Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}		2.6	3.1		Volts
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., I_{OL} = −16mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.85	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −5mA				−1.0	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.25V				25	µA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Driver	−50		−150	mA
			Receiver	−30		−75	
I_{CC}	Power Supply Current	V_{CC} = MAX.				87	mA
I_O	Bus Leakage Current with Driver Off	V_{CC} = MAX., V_{BUS} = 2.6V V_{IN} = V_{IH} or V_{IL}				100	µA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		16	20	ns
t_{PHL}				16	20	
t_{PLH}	Bus to Receiver Output	Figure 2		13	18	ns
t_{PHL}				6	10	
t_{ZL}	Driver Enable to Bus	Figure 3		29	38	ns
t_{LZ}				35	43	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		20	30	ns
t_{LZ}				10	17	

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

B_0, B_1, B_2, B_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

R/E Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
R/E	1	1/8	–	–
R_0	2	–	50	10
B_0	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
B_1	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
B_2	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
B_3	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

4

DRIVER FUNCTION TABLE

INPUTS		OUTPUT
B/E	D_i	B_i
L	X	Z
H	L	H
H	H	L

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

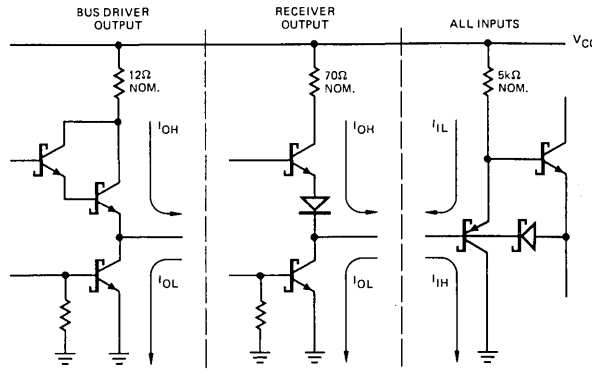
RECEIVER FUNCTION TABLE

INPUTS		OUTPUT
R/E	B_i	R_i
H	X	Z
L	L	H
L	H	L

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

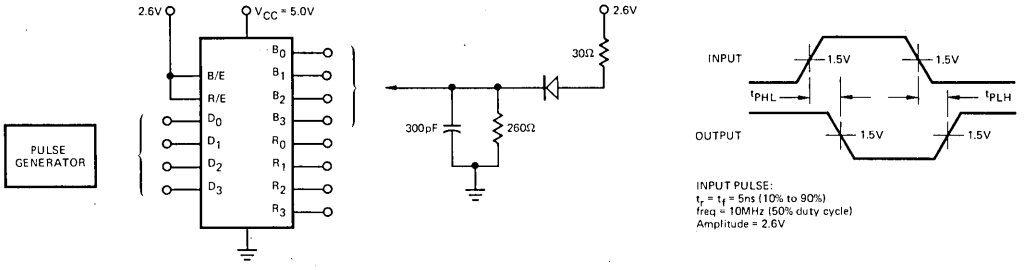


Figure 1

PROPAGATION DELAY (Bus to Receiver Out)

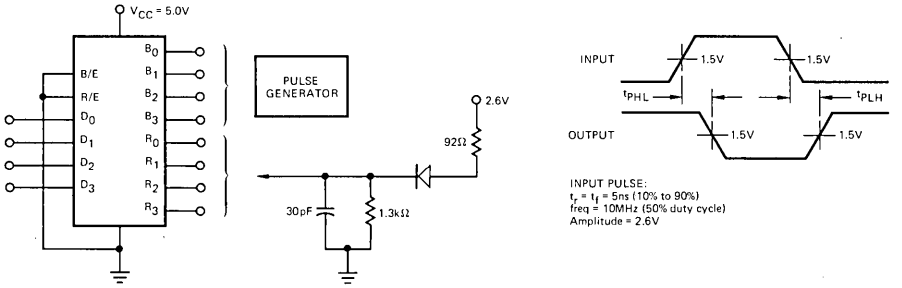


Figure 2

PROPAGATION DELAY (Bus Enable to Bus Output)

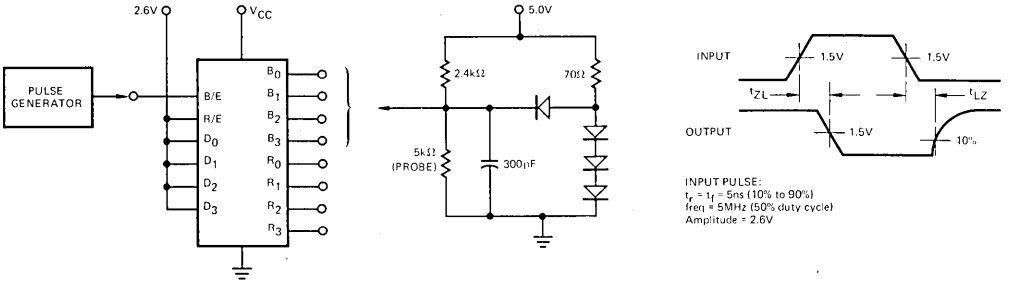


Figure 3

PROPAGATION DELAY (Receive Enable to Receive Output)

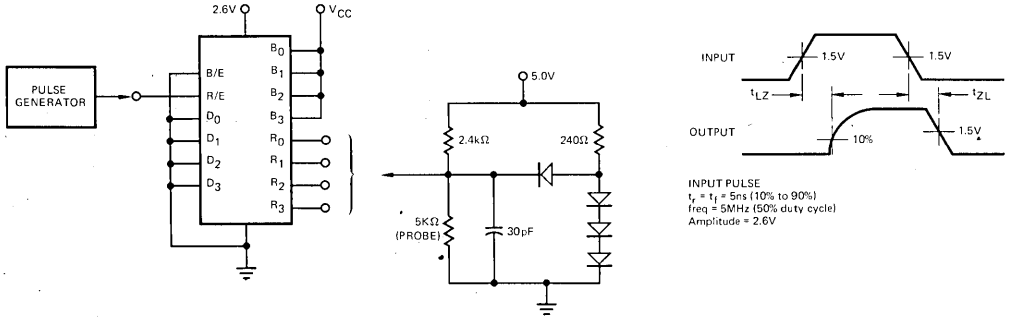
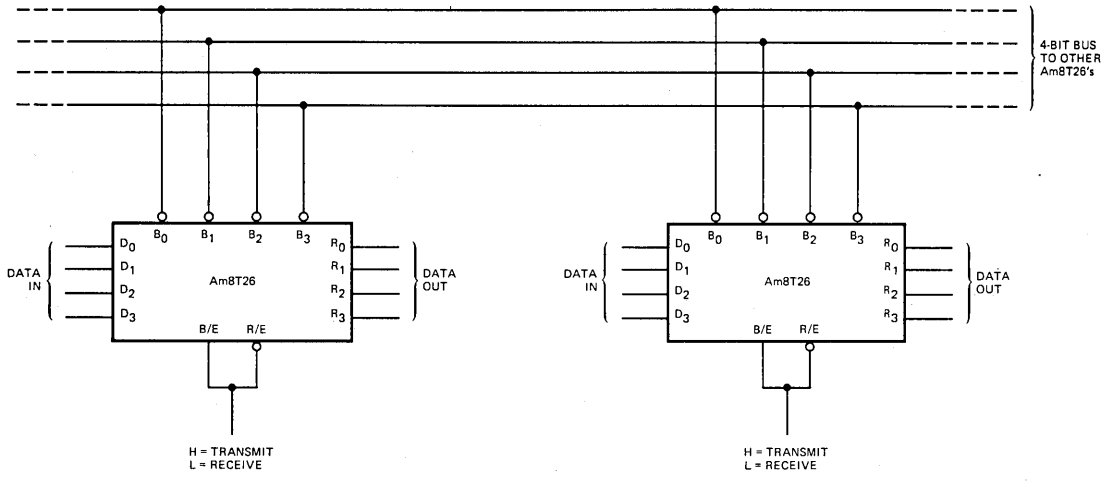


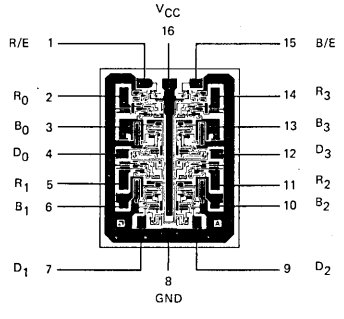
Figure 4

APPLICATION



4

Metallization and Pad Layout



DIE SIZE 0.063" X 0.082"

Am8T26A•Am8T28

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- Three-state outputs on driver and reciever
- PNP inputs
- Am8T26A has inverting outputs
- Am8T28 has non-inverting outputs
- Driver propagation delay — 14ns max. for 8T26A; 17ns max. for 8T28
- Receiver propagation delay — 14ns max. for 8T26A; 17ns max. for 8T28
- 100% reliability assurance testing in compliance with MIL-STD-883

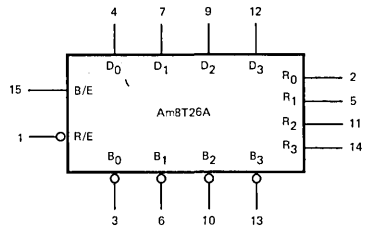
FUNCTIONAL DESCRIPTION

The Am8T26A/Am8T28 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

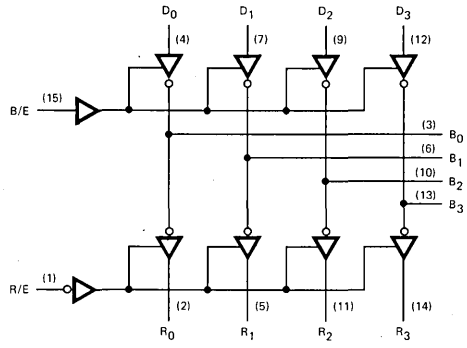
LOGIC SYMBOL



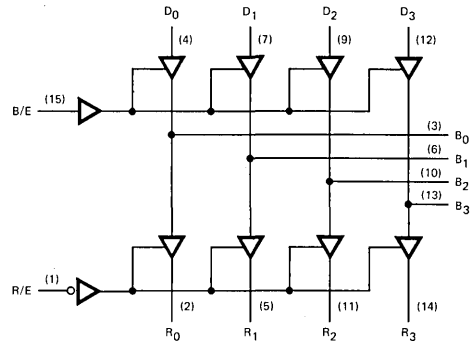
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am8T26A
Inverting Output (Three-State)



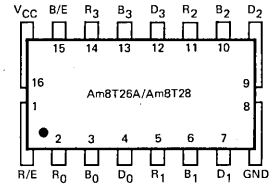
Am8T28
Non-Inverting Output (Three-State)



ORDERING INFORMATION

Package Type	Temperature Range	Am8T26A Order Number	Am8T28 Order Number
Molded DIP	0°C to +75°C	N8T26AB	N8T28B
Hermetic DIP	0°C to +75°C	N8T26AF	N8T28F
Dice	0°C to +75°C	AM8T26AXC	AM8T28XC
Hermetic DIP	−55°C to +125°C	S8T26AF	S8T28F
Dice	−55°C to +125°C	AM8T26AXM	AM8T28XM

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

N8T26A, N8T28 T_A = 0°C to +75°C (COM'L) MIN. = 4.75 V MAX. = 5.25 V

S8T26A, S8T28 T_A = −55°C to +125°C (MIL) MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4 V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 48 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −10 mA, V_{CC} = V_{CC} MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX. (Note 4)	−50		−150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −100 μA, V_{CC} = 5.0 V	3.5			Volts
		I_{OUT} = −2.0 mA (Note 6)	2.4			
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX.	−30		−75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			Volts
V_{TH}	High Level Input Threshold Voltage				2.0	Volts
I_O	Low Level Output Off Leakage Current	V_{OUT} = 0.5 V			−100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4 V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	Volts
P_{WR}/ I_{CC}	Power/Current Consumption (Am8T26A)	V_{CC} = V_{CC} MAX.			457/87	mW/mA
	Power/Current Consumption (Am8T28)	V_{CC} = V_{CC} MAX.			578/110	mW/mA

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Am8T26A Min.	Am8T26A Typ.	Am8T26A Max.	Am8T28 Min.	Am8T28 Typ.	Am8T28 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

B_0, B_1, B_2, B_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

R/E Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
R/E	1	1/8	–	–
R_0	2	–	50	10
B_0	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
B_1	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
B_2	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
B_3	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

DRIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
B/E	D_i	B_i	B_i
L	X	Z	Z
H	L	H	L
H	H	L	H

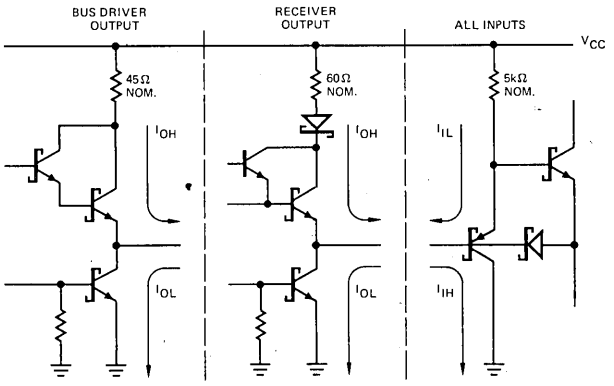
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
R/E	B_i	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

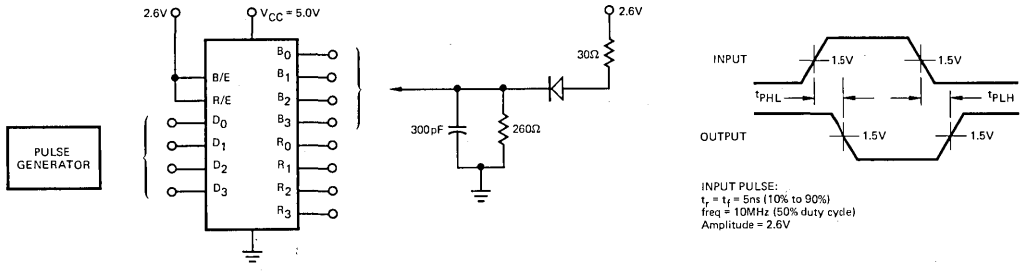


Figure 1

PROPAGATION DELAY (Bus to Receiver Out)

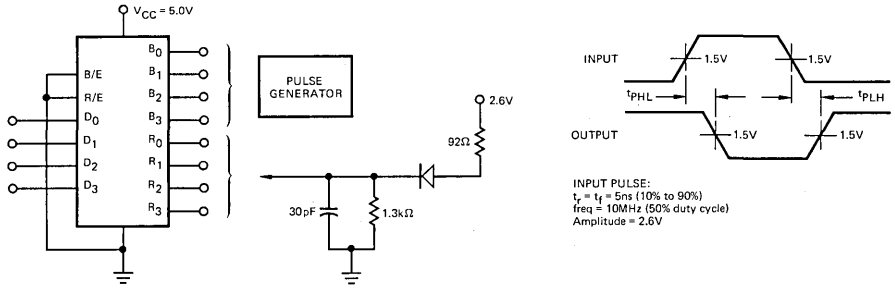


Figure 2

PROPAGATION DELAY (Bus Enable to Bus Output)

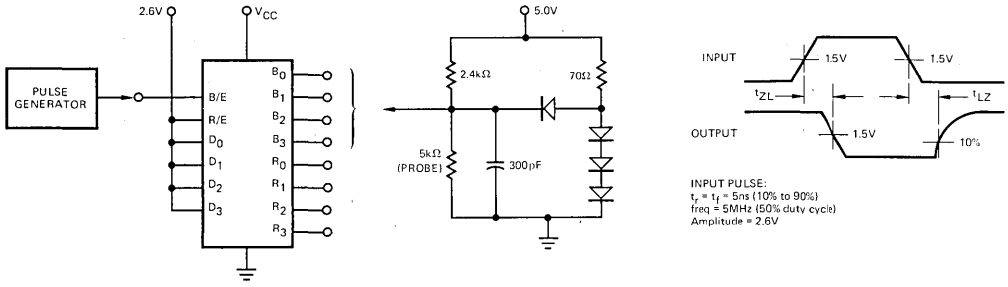


Figure 3

PROPAGATION DELAY (Receive Enable to Receive Output)

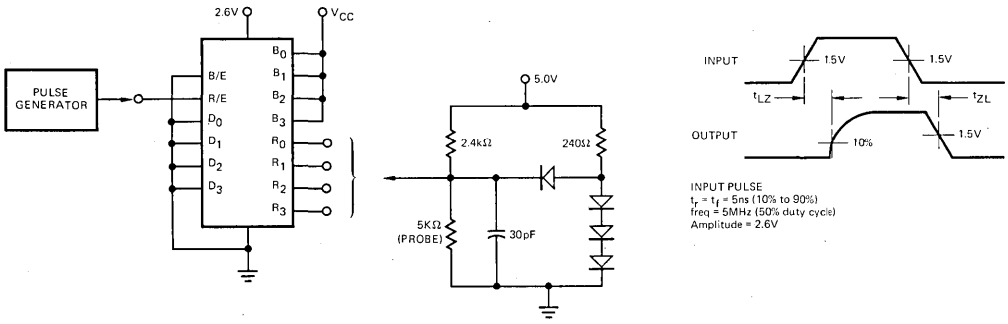


Figure 4

4

Am9614

Dual Differential Line Driver

Distinctive Characteristics

- Dual differential line driver with complementary outputs
- Single 5-volt supply
- DTL, TTL compatible
- Short-circuit protected outputs
- Able to drive 50Ω terminated transmission lines
- 100% reliability assurance testing in compliance with MIL-STD-883

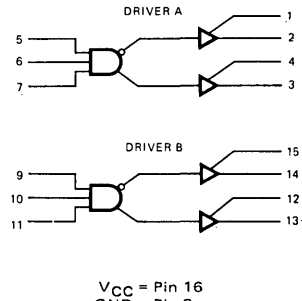
FUNCTIONAL DESCRIPTION

The Am9614 is a DTL, TTL compatible line driver operating off a single 5V supply.

The Am9614 is designed to drive either differential or single-ended, back-matched or terminated transmission lines. The device has the active pull-down and active pull-up circuits split and brought out to adjacent pins. This allows multiplex operation (wire-AND) at the driving end in either the single-ended mode via the uncommitted collector or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other. The complementary outputs of the Am9614 give great application flexibility.

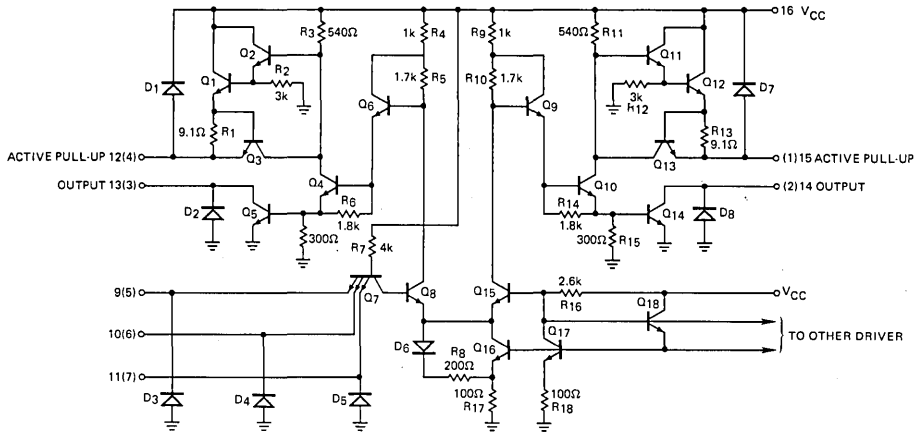
The Am9614 has short-circuit protected active pull-ups, and incorporates input clamp diodes to reduce the effect of line transients, and can drive into 50Ω terminated transmission lines.

LOGIC DIAGRAMS



V_{CC} = Pin 16
GND = Pin 8

CIRCUIT DIAGRAM (1/2 Am9614)

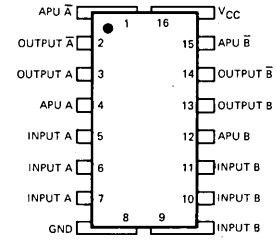


Notes: 1. Circuit shown for one driver only.
2. Pin numbers in parenthesis refer to the other driver.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	-55°C to +125°C	9614DM
Flat Pak	-55°C to +125°C	9614FM
Dice	-55°C to +125°C	AM9614XM
Hermetic DIP	0°C to +70°C	9614DC
Molded DIP	0°C to +70°C	9614PC
Dice	0°C to +70°C	AM9614XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Ouputs	200mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

9614XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V
9614XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

DC Characteristics (Note 2)

Parameters	Description	Test Conditions		T_A MIN. Min.	T_A MIN. Max.	LIMITS +25°C Min.	LIMITS +25°C Typ.	LIMITS +25°C Max.	T_A MAX. Min.	T_A MAX. Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA	MIL		0.4		0.2	0.4		0.4	Volts
			COM'L		0.45		0.2	0.45		0.45	
V_{IH}	Input HIGH Voltage	V_{CC} = MIN.	MIL	2.0		1.7	1.5		1.4		Volts
			COM'L	1.9		1.8	1.5		1.6		
V_{IL}	Input LOW Voltage	V_{CC} = MAX.	MIL		0.8		1.3	0.9		0.8	Volts
			COM'L		0.85		1.3	0.85		0.85	
I_F	Input Load Current	V_{CC} = MAX.	V_F = 0.4V, MIL		−1.6		−1.1	−1.1		−1.6	mA
			V_F = 0.45V, COM'L		−1.6		−1.0	−1.6		−1.6	
I_R	Reverse Input Current	V_{CC} = MAX. V_R = 4.5V			60			60		60	µA
I_{SC}	Short Circuit Current	V_{CC} = MAX., V_O = 0V				−40	−90	−120			mA
I_{PD}	Power Supply Current	V_{CC} = MAX., Inputs = 0V			48.7		33	48.7		48.7	mA
		V_{CC} = 7.0V, Inputs = 0V	COM'L				46	70			
			MIL				46	65.7			
I_{CEX}	Reverse Output Current	V_{CC} = MAX	V_{CEX} = 12V, MIL		100		10	100		200	µA
			V_{CEX} = 5.25V, COM'L		100		10	100		200	
V_{OLC}	Output Low Clamp Voltage	V_{CC} = MAX., I_{OLC} = −40mA					−0.8	−1.5			Volts
V_{IC}	Input Clamp Voltage	V_{CC} = MIN., I_{IC} = −12mA					−1.0	−1.5			Volts

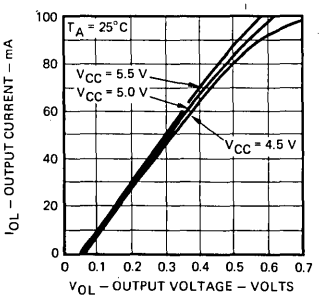
Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters	Description	Test Conditions	9614XM Min.	9614XM Typ.	9614XM Max.	9614XC Min.	9614XC Typ.	9614XC Max.	Units
t_{pd+}	Turn Off Delay	V_{CC} = 5.0V, C_L = 30pF, V_M = 1.5V, Refer to Fig. 1		14	20		14	30	ns
t_{pd-}	Turn On Delay			18	20		18	30	ns

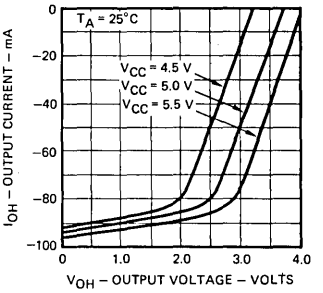
Notes: 1. Maximum current defined by DC input voltage.
2. For conditions shown as MIN. or MAX. use the appropriate value specified under electrical characteristics for the applicable device type or grade.

TYPICAL ELECTRICAL CHARACTERISTICS

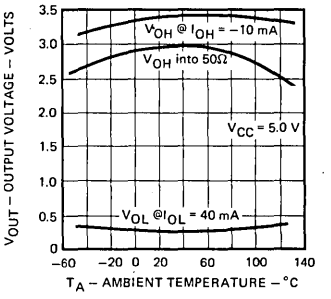
Output Low Current Versus Output Low Voltage



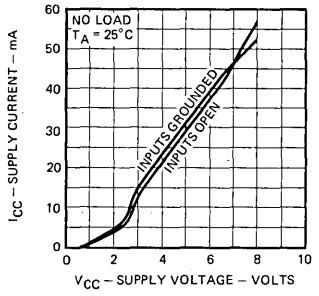
Output High Current Versus Output High Voltage



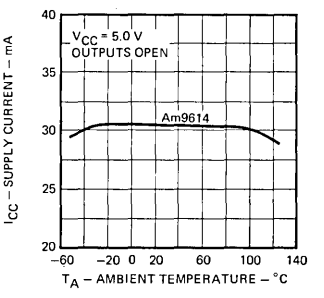
Logic Levels Versus Ambient Temperature



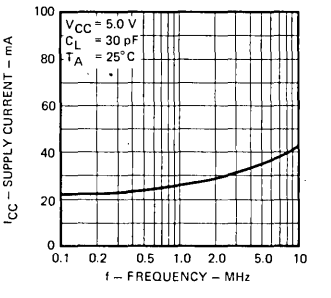
Supply Current Versus Supply Voltage



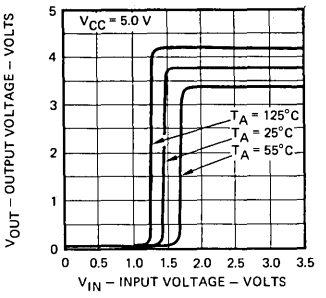
Supply Current Versus Temperature



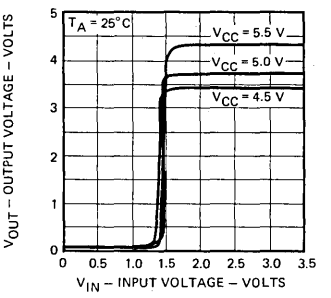
Supply Current Versus Operating Frequency



Transfer Characteristics Versus Temperature



Transfer Characteristics Versus Supply Voltage



USERS NOTES

DIFFERENTIAL LINES. The Am9614 dual differential line driver can be used with the Am9615 dual differential line receiver to form an interconnection system which can tolerate extremely noisy environments and interconnect equipments where there is a ±15V difference in voltage level of the equipment grounds. Two wires are used for each channel to form a balanced transmission line. This method of sending data between equipments offers extremely high protection from common mode noise and also gives excellent DC noise margins.

MATCHING. Transmission lines can be matched in a number of ways. The most widely used method is to terminate the line at the receiving end in its characteristic impedance. This impedance is connected across the input terminals of the receiver. A 130Ω resistor is included at the + input of each receiver for matching twisted pairs and this resistor, or if the characteristic impedance is not 130Ω, a discrete resistor, is connected between the two receiver inputs. This method of matching causes a DC component in the signal. Power is dissipated in the resistor and the signal is attenuated. The DC component can be effectively removed by connecting a large capacitor in series with the terminating resistor.

The transmission line can also be terminated through the receiver power supply by placing equal value resistors from the + input of the receiver to V_{CC} and from the – input to ground. This method again has the disadvantage that a DC signal component exists, attenuation occurs, and power is dissipated in the terminating resistors but it does allow multiplexed operation in the balanced differential mode.

An alternate method to matching at the receiver is to back match at the driver. A resistor is placed in series with the line so that the signal from the driver which is reflected at the high input impedance of the receiver is absorbed at the driver. This method does not have a DC component and therefore no attenuation occurs and power is not dissipated in the resistor. For balanced differential driving a resistor is required in series with each line. The table below shows the value of each matching resistor required for lines of different characteristic impedance.

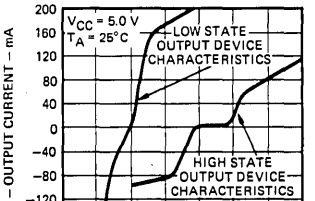
MULTIPLEXING. When operating in the balanced differential mode the Am9614 driver can be OR tied with other devices to allow multiplexed operation. The open collector NAND outputs are connected together and the active pull-up AND outputs are connected together. Selection of the active driver can be made by two of the three logic inputs on the driver. Multiplexed operation can only be performed with the lines terminated to the appropriate voltage level at the driver so that this method has a DC component and power is dissipated in the terminating resistors.

4

TYPICAL DC CHARACTERISTICS
FOR MATCHING TO TRANSMISSION LINE

BACK MATCHING TABLE

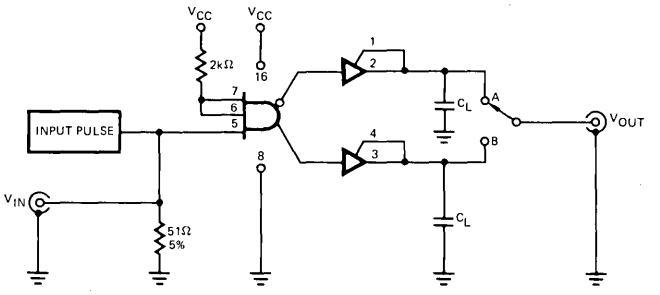
Z_O	R_M (ohms) Differential
50	12
75	24
92	33
100	36
130	54
300	140
600	290

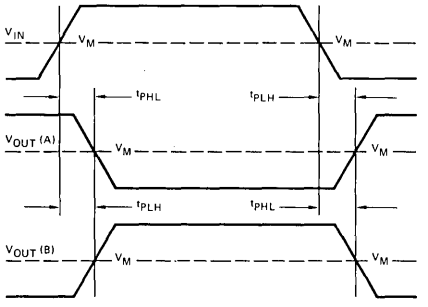


LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
APU A	1	—	166	—
Output A	2	—	—	25
Output A	3	—	—	25
APU A	4	—	166	—
Input A	5	1	—	—
Input A	6	1	—	—
Input A	7	1	—	—
GND	8	—	—	—
Input B	9	1	—	—
Input B	10	1	—	—
Input B	11	1	—	—
APU B	12	—	166	—
Output B	13	—	—	25
Output B	14	—	—	25
APU B	15	—	166	—
V_{CC}	16	—	—	—

SWITCHING CIRCUITS AND WAVEFORMS

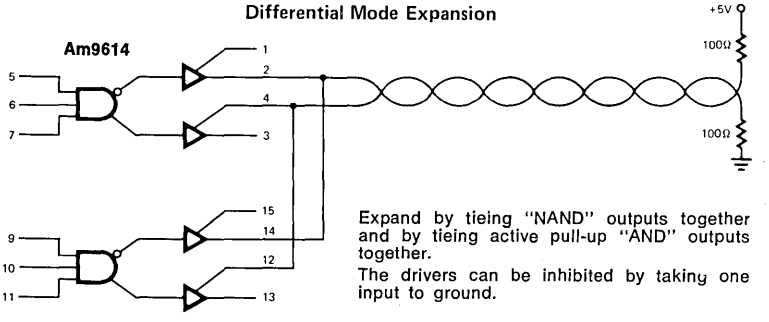




INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

APPLICATION

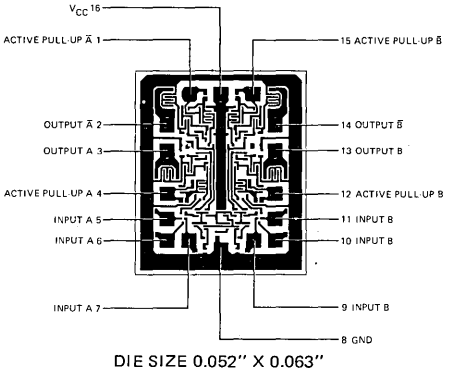
Differential Mode Expansion



Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together.

The drivers can be inhibited by taking one input to ground.

Metallization and Pad Layout



DIE SIZE 0.052" X 0.063"

Am9616

Triple EIA RS-232C/MIL-STD-188C Line Driver

Distinctive Characteristics

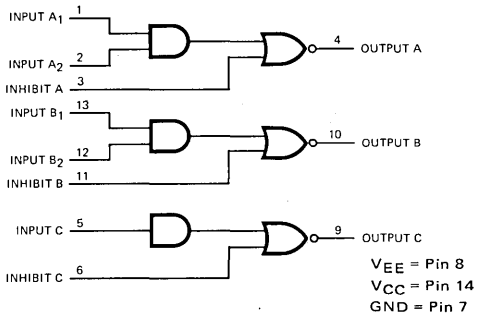
- Conforms to EIA RS-232C and CCITT V.24 specifications and/or MIL-STD-188C
- Short circuit protected output
- Internal slew rate limiting
- Supply independent output swing
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

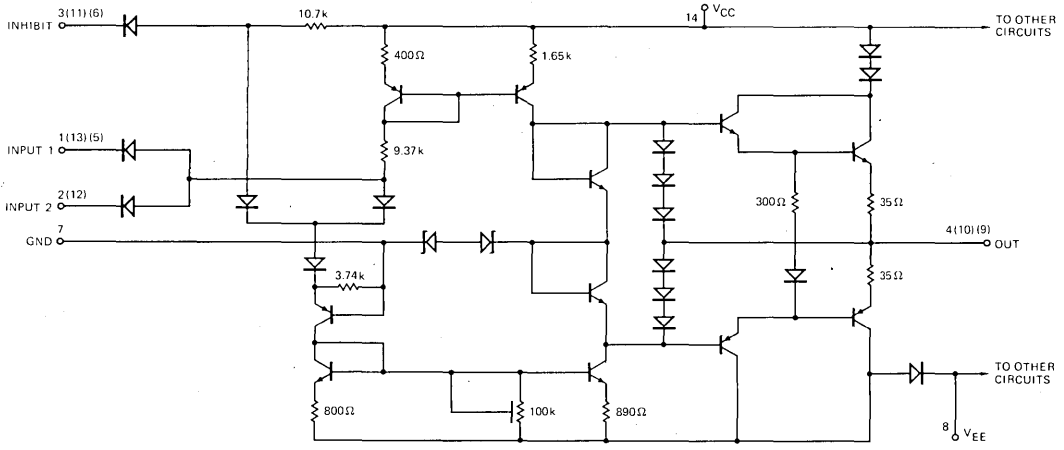
The Am9616 is a triple line driver specifically designed to meet the EIA RS-232C and CCITT V.24 and/or MIL-STD-188C electrical interface requirements. Each driver accepts DTL/TTL logic levels and converts them to EIA/CCITT levels for data transmission between equipment. The output slew rate of each driver is internally limited, but can be lowered by an external capacitor. All outputs are short circuit protected, and protected against fault conditions specified in RS-232C. A HIGH logic level on the inhibit input forces the driver output to V_{OL} or mark state.

The Am9616EXC and Am9616XM meets the requirements of MIL-STD-188C and EIA RS-232C. The Am9616XC conforms to the requirements of EIA RS-232C.

LOGIC SYMBOL



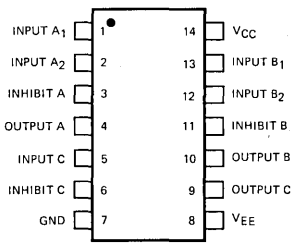
CIRCUIT DIAGRAM
(One Driver Shown)



Am9616 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	9616DM
Dice	−55°C to +125°C	AM9616XM
Hermetic DIP	0°C to +75°C	9616EDC
Hermetic DIP	0°C to +75°C	9616DC
Molded DIP	0°C to +75°C	9616EPC
Molded DIP	0°C to +75°C	9616PC
Dice	0°C to +75°C	AM9616XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	
V_{CC}	+15 V
V_{EE}	−15 V
DC Voltage Applied to Outputs	±15 V
DG Input Voltage	−1.5 V to +6 V
Lead Temperature (Soldering, 30 sec.)	300°C

Am9616XM AND Am9616EXC
RS232-C AND MIL-STD-188C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:
Am9616XM (MIL) $T_A = -55°C$ to $+125°C$
Am9616EXC (COM'L) $T_A = 0°C$ to $+70°C$
$V_{CC} = +12V \pm 10\%$, $V_{EE} = -12V \pm 10\%$, $R_L = 3k\Omega$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage			5.0	6.0	7.0	Volts
V_{OL}	Output LOW Voltage			−7.0	−6.0	−5.0	Volts
	Ripple Rejection	Power Supply Ripple = $2.4V_{p\text{-}p}$, f = 400Hz			0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage, Magnitude Matching Error					±10	%
R_{OUT}	Output Resistance, Power On	$R_L = 6k\Omega$, $\Delta I_L = 10mA$			75		Ω
I_{SC+}	Positive Output Short Circuit Current				22	100	mA
I_{SC-}	Negative Output Short Circuit Current			−100	−22		mA
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{IL}	Input LOW Voltage					0.8	Volts
I_{IH}	Input HIGH Current	$V_{IN} = 2.4V$				40	μA
		$V_{IN} = 5.5V$				1.0	mA
I_{IL}	Input LOW Current	$V_{IN} = 0.4V$		−1.6			mA
R_{OUT}	Output Resistance, Power Off	$-2.0V \leq V_{OUT} \leq +2.0V$ All Inputs and Supply Pins Grounded		300			Ω
I_+	Positive Supply Current	$T_A = +25°C$	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8V$		15	22	mA
			$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0V$		7.5	13	
I_-	Negative Supply Current	$T_A = +25°C$	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8V$		0	−1	mA
			$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0V$		−15	−22	

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE OF $T_A = 0°C$ TO $70°C$ (Note 2)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
	Positive Slew Rate	$0pF \leq C_L \leq 2500pF$ $R_L \geq 3k\Omega$	4.0	15	30	V/μs
	Negative Slew Rate	$0pF \leq C_L \leq 2500pF$ $R_L \geq 3k\Omega$	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

Notes: 1. Typical values are at $V_{CC} = 12V$, $V_{EE} = -12V$, $T_A = 25°C$.
2. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate.

Am9616XC
EIA RS-232-C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:
$T_A = 0°C$ to $+75°C$, $V_{CC} = +12V \pm 10\%$, $V_{EE} = -12V \pm 10\%$, $R_L = 3k\Omega$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

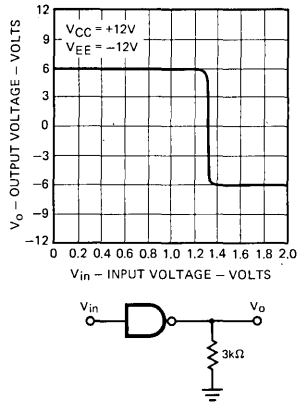
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{IN_1} or $V_{IN_2} = V_{INHIBIT} = 0.8\ V$	+5.0	+6.0	+7.0	Volts
V_{OL}	Output LOW Voltage	$V_{IN_1} = V_{IN_2} = V_{INHIBIT} = 2.0\ V$	−7.0	−6.0	−5.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage			0.8	Volts
I_{IL}	Input LOW Current	$V_{IN_1} = V_{IN_2} = 0.4\ V$ or $V_{INHIBIT} = 0.4\ V$		−1.2	−1.6	mA
I_{IH}	Input HIGH Current	$V_{IN_1} = V_{IN_2} = 2.4\ V$ or $V_{INHIBIT} = 2.4\ V$			40	μA
I_{SC}	Output Short Circuit Current (Positive)	$R_L = 0\ \Omega$ V_{IN_1} or $V_{IN_2} = V_{INHIBIT} = 0.8\ V$	−8	−17	−30	mA
I_{SE}	Output Short Circuit Current (Negative)	$R_L = 0\ \Omega$ V_{IN_1} or $V_{IN_2} = V_{INHIBIT} = 2.0\ V$	+8	+17	+30	mA
I_{CC}	Total Positive Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT} = 0.8\ V$		15	22	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT} = 2.0\ V$		7.5	13	
I_{EE}	Total Negative Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT} = 0.8\ V$		0	−1	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT} = 2.0\ V$		−15	−22	

AC CHARACTERISTICS

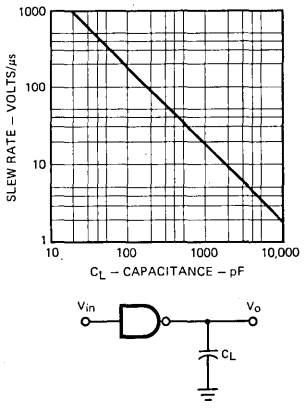
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	$C_L = 15\ pF$, $R_L = \infty$		320	650	ns
t_{PHL}	Delay from Input HIGH to Output LOW			320	650	ns
	Positive Slew Rate	$0\ pF \leq C_L \leq 2500\ pF$, $R_L \geq 3\ k\Omega$	4.0	15	30	V/μs
	Negative Slew Rate		−30	−15	−4.0	V/μs

TYPICAL CHARACTERISTICS

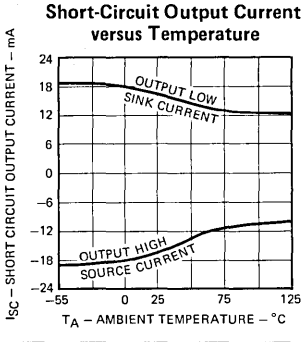
Transfer Characteristics



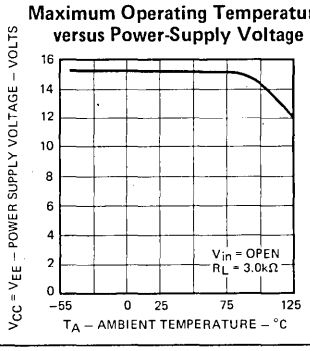
Output Slew Rate versus Load Capacitance



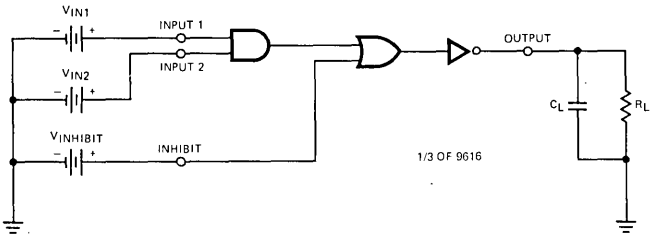
Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage

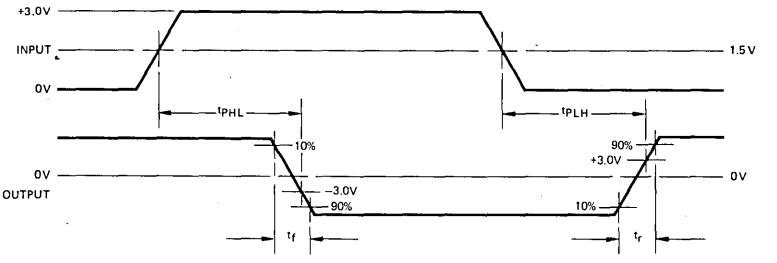


SWITCHING TEST CIRCUIT



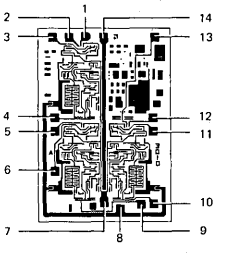
Note: Omit V_{IN2} for channel "C".

VOLTAGE WAVEFORMS



Pulse Generator Rise Time = 10 ± 5ns.

Metallization and Pad Layout



DIE SIZE 0.069" X 0.103"

Am9617

RS-232C Line Receiver

Distinctive Characteristics

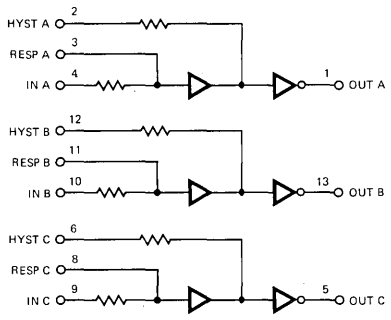
- Compatible with EIA RS-232C and CCITT V24 specifications.
- Input signal range ±30 volts
- Available in commercial and military temperature range
- Variable hysteresis
- 100% reliability assurance testing in compliance with MIL-STD-883
- Includes response control input and built-in hysteresis.

FUNCTIONAL DESCRIPTION

The Am9617 is a triple line receiver that meets both the CCITT TV24 and EIA RS-232C specifications. Each receiver has single data input that can accept signal swings of up to ±30V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. Each receiver has a hysteresis input so that the hysteresis can be controlled by means of a series resistor between the HYST input and a response control input RESP.

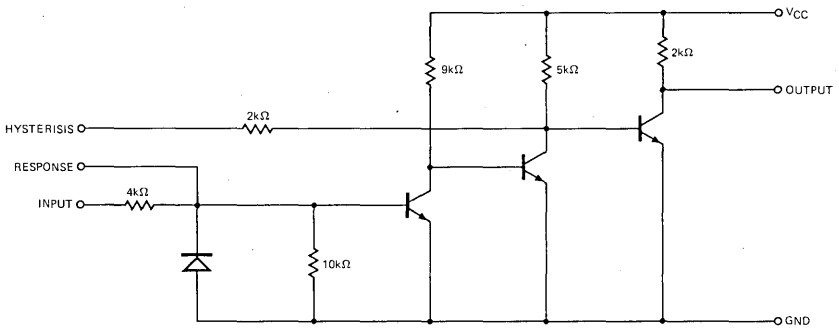
Because of this hysteresis in switching thresholds, the device can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am9616.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

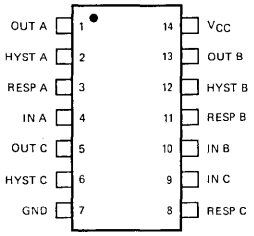
CIRCUIT DIAGRAM
(One Receiver)



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	-55°C to +125°C	9617DM
Hermetic DIP	0°C to +75°C	9617DC
Molded DIP	0°C to +75°C	9617PC
Dice	-55°C to +125°C	AM9617XM
Dice	0°C to +75°C	AM9617XC

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:
Am9617XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V
Am9617XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Response Control Pin Open Unless Otherwise Specified

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

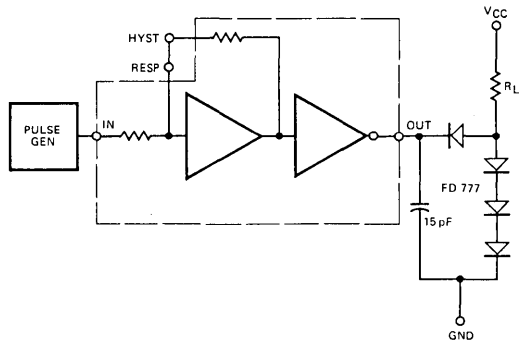
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
R_{IN}	Input Resistance	V_{IN} = ± 25V		3.0	4.0	7.0	kΩ
V_{IN}	Open Circuit Input Voltage				0.2	2.0	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −0.2mA, V_{CC} = Min. V_{IN} = −3.0V, 0V or Open Circuit		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{CC} = Min. V_{IN} = +3.0V			0.3	0.4	Volts
V_{IH}	Input HIGH Level Threshold	V_{OL} = 0.45V, V_{CC} = 5.0V Resp-Hyst Connected	−55°C	2.3		3.1	Volts
			0°C	1.9		2.5	
			25°C	1.75	2.0	2.25	
			75°C	1.45		1.90	
			125°C	1.20		1.65	
V_{IL}	Input LOW Level Threshold	V_{OH} = 2.5V, V_{CC} = 5.0V Resp-Hyst Connected	−55°C	0.85		1.65	Volts
			0°C	0.75		1.40	
			25°C	0.75	0.95	1.25	
			75°C	0.60		1.10	
			125°C	0.50		0.95	
V_{IO}	Open Loop Input Threshold		25°C	0.4	1.0	1.2	Volts
				0.4		1.4	
I_{IL}	Input LOW Current	V_{IN} = −25V	25°C	−3.6		−8.0	mA
						−8.3	
I_{IH}	Input HIGH Current	V_{IN} = +25V	25°C	3.6		8.0	mA
						8.3	
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0V, V_{OUT} = 0.0V			2.5		mA
I_{CC}	Power Supply Current	V_{IN} = 5.0V, V_{CC} = Max.			12	18	mA

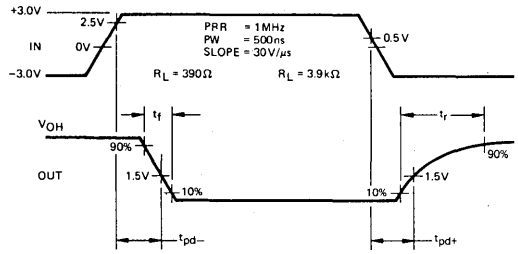
Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. The input threshold margin for the device is greater than the voltage computed as the $V_{T+}-V_{T-}$ value. For the minimum value see the input threshold margin versus temperature graph.

Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

Parameters	Definition	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{pd-}	Delay from Input HIGH to Output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		15	40	ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

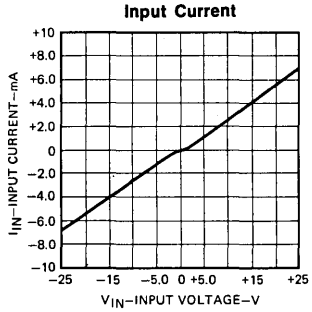


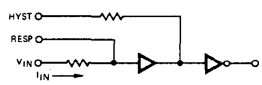


Note: Wiring capacitance should be minimized between Outputs, Hysterisis and Response Pins.

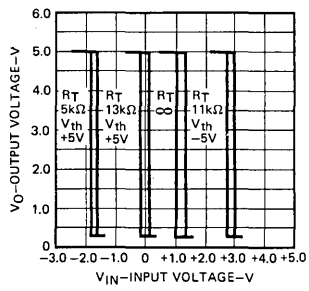
TYPICAL CHARACTERISTICS

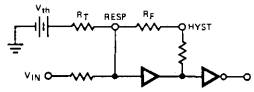
Input Current



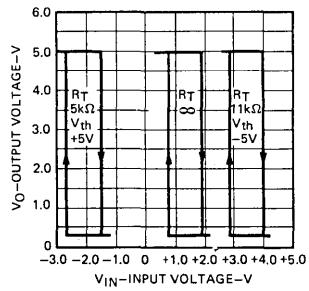


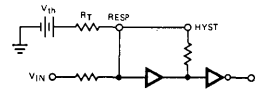
R_F = 8k Input Threshold Voltage Adjustment



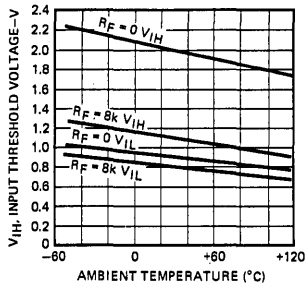


R_F = 0 Input Threshold Voltage Adjustment

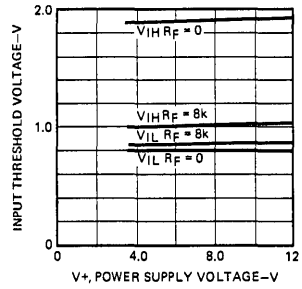




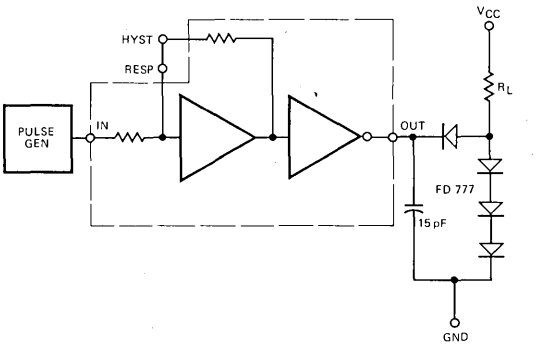
Input Threshold Voltage Versus Temperature

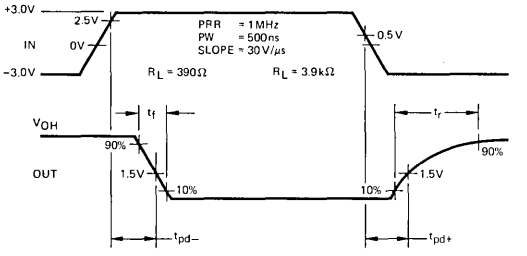


Input Threshold Versus Power-Supply Voltage



SWITCHING TIME TEST CIRCUIT & WAVEFORMS

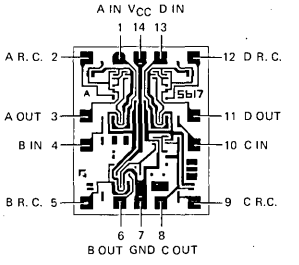




NOTE: Wiring capacitance should be minimized between Outputs, Hysterisis and Response Pins.

Metallization and Pad Layout

DIE SIZE 0.047" x 0.059"



Am9620

Dual Differential Line Receiver

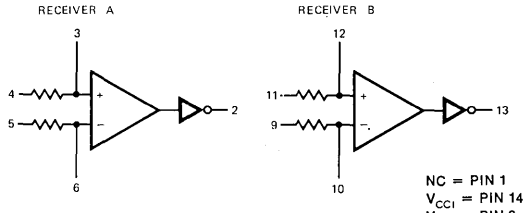
Distinctive Characteristics

- Dual Differential Receiver
- DTL, TTL compatible
- High common-mode voltage range (±15 volts)
- Wire AND capability
- 100% reliability assurance testing in compliance with MIL-STD-883

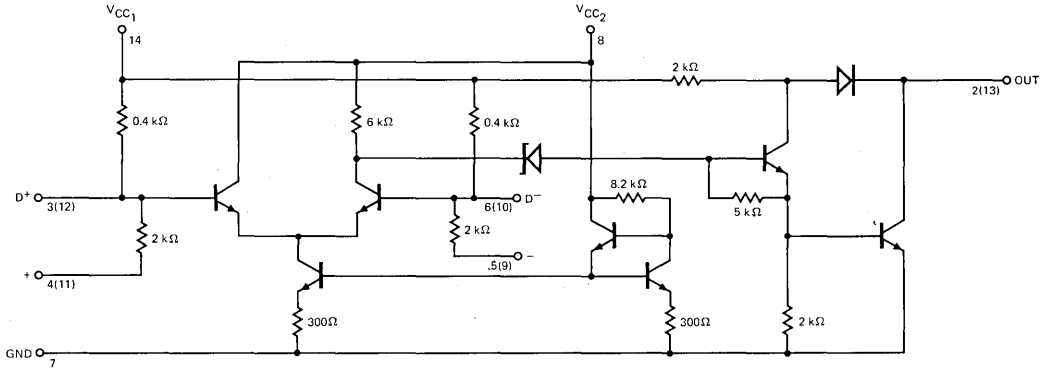
FUNCTIONAL DESCRIPTION

The Am9620 is a dual differential line receiver designed to receive digital data from transmission lines. The receiver produces an undisturbed output for ±500mV of differential data on the inputs in the presence of up to ±15V of common mode noise voltages. The device has a DTL, TTL compatible output which can be AND tied with other receiver outputs. In addition to attenuated inputs which are normally used, the receiver has direct inputs which allow the input attenuation and response time to be changed by use of external components.

LOGIC DIAGRAM



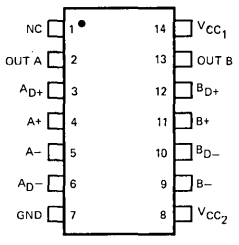
CIRCUIT DIAGRAM



Am9620 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	9620DM
Flat Pak	−55°C to +125°C	9620FM
Dice	−55°C to +125°C	AM9620XM
Hermetic DIP	0°C to +70°C	9620DC
Molded DIP	0°C to +70°C	9620PC
Dice	0°C to +70°C	AM9620XC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
DC Data Input Voltage	−20 V to +20 V
Output Current, Into Outputs	30 mA
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V

ELECTRICAL CHARACTERISTICS

Am9620XM $T_A = -55°C$ to $+125°C$ $V_{CC1} = 5.0\ V \pm 10\%$ $V_{CC2} = 12\ V \pm 10\%$
Am9620XC $T_A = 0°C$ to $+75°C$ $V_{CC1} = 5.0\ V \pm 5\%$ $V_{CC2} = 12\ V \pm 5\%$

DC Characteristics (Notes 1, 2)

Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am9620XM	$V_{CC1} = 4.5\ V$, $V_{DIFF} = -0.5\ V$, $I_{OH} = -0.2\ mA$, $V_{CC2} = 10.8\ V$	2.80				3.00	3.3				2.90		Volts
	Am9620XC	$V_{CC1} = 4.75\ V$, $V_{DIFF} = -0.5\ V$, $I_{OH} = -0.2\ mA$, $V_{CC2} = 11.4V$			2.80		3.00	3.3		2.90				
V_{OL} Output LOW Voltage	Am9620XM	$V_{CC1} = 4.5\ V$, $V_{DIFF} = +0.5\ V$, $I_{OL} = 15.0\ mA$		0.40				0.25	0.40				0.45	Volts
	Am9620XC	$V_{CC1} = 4.75\ V$, $I_{OL} = 15.0\ mA$				0.45		0.25	0.45		0.50			
I_{CEX} Output Leakage Current	Am9620XM	$V_{CC1} = 4.5\ V$, $V_{DIFF} = -4.5\ V$, $V_{CEX} = 12\ V$		50					100				200	μA
	Am9620XC	$V_{CC1} = 4.75\ V$, $V_{CEX} = 5.25\ V$				50			100		200			
I_{SC} Output Short Circuit Current	Am9620XM	$V_{CC1} = 5.0\ V$, $V_{SC} = 0\ V$						−1.4	−2.15 −3.1					mA
	Am9620XC	$V_{CC1} = 5.0\ V$, $V_{SC} = 0\ V$						−1.4	−2.15 −3.1					
I_F Input Load Current	Am9620XM	$V_{CC1} = 5.0\ V$, $V_{CC2} = 12\ V$		−3.1					−2.1 −3.0				−3.0	mA
	Am9620XC	$V_{CC1} = 5.0\ V$, $V_{CC2} = 12\ V$				−3.1			−2.1 −3.0		−3.0			
V_{CM} Common Mode Voltage	Am9620XM	$V_{CC1} = 5.0\ V$, $V_{DIFF} = 2.0\ V$, $V_{CC2} = 12\ V$	−15	+15				−15	±17.5 +15			−15	+15	Volts
	Am9620XC	$V_{CC1} = 5.0\ V$, $V_{DIFF} = 2.0\ V$, $V_{CC2} = 12\ V$			−12	+12		−12	±17.5 +12	−12	+12			
V_{TH} Differential Input Threshold Voltage	Am9620XM	$V_{CC1} = 5.0\ V$, $V_{CM} = 0\ V$, $V_{CC2} = 12\ V$		500					120 500				500	mV
	Am9620XC	$V_{CC1} = 5.0\ V$, $V_{CM} = 0\ V$, $V_{CC2} = 12\ V$				500			120 500		500			mV
I_{CC1} Power Supply Current	Am9620XM	$V_{CC1} = 5.5\ V$, + Input = 5.5 V, $V_{CC2} = 13.2\ V$, − Input = 0 V		13					8.2 13				13	mA
	Am9620XC	$V_{CC1} = 5.25\ V$, + Input = 5.25 V, $V_{CC2} = 12.6\ V$, − Input = 0 V				13.5			8.2 13.5		13.5			
I_{CC2} Power Supply Current	Am9620XM	$V_{CC1} = 5.5\ V$, + Input = 5.5 V, $V_{CC2} = 13.2\ V$, − Input = 0 V		8.0					5.6 8.0				8.0	mA
	Am9620XC	$V_{CC1} = 5.25\ V$, + Input = 5.25 V, $V_{CC2} = 12.6V$, − Input = 0 V					8.5	5.6	8.5		8.5			

Switching Characteristics

Parameters			Am9620XM +25°C Min	Typ	Max	Am9620XC +25°C Min	Typ	Max	Units
t_{pd+}	Turn Off Delay $R_L = 3.9\ k$	$V_{CC} = 5.0\ V$, $C_L = 30\ pF$ Refer to figure 1		35	50		35	75	ns
t_{pd-}	Turn On Delay $R_L = 390\ \Omega$			20	50		20	75	

Note: 1. Pulse tested.
2. V_{DIFF} is the differential voltage referred from A+ to A− and from B+ to B−.

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

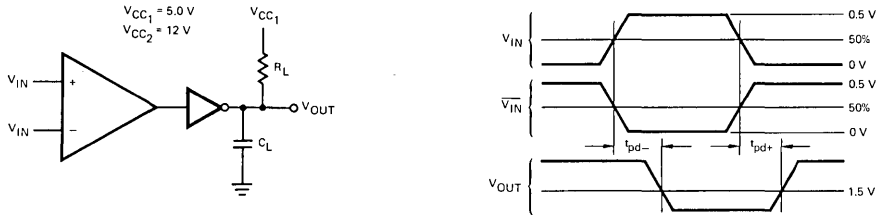
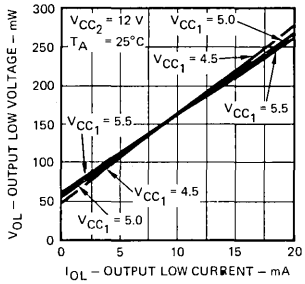


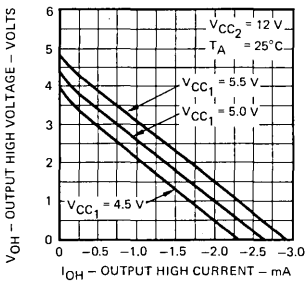
Figure 1.

TYPICAL ELECTRICAL CHARACTERISTICS

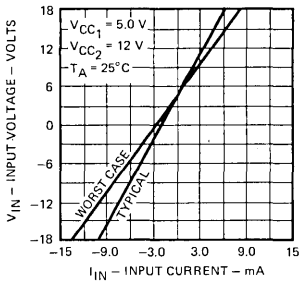
Output Low Voltage Versus Output Low Current



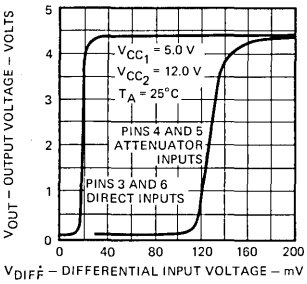
Output High Voltage Versus Output High Current



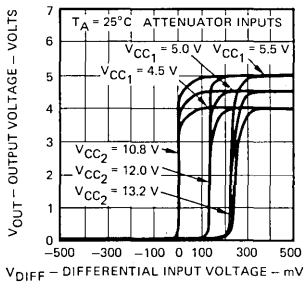
Input Voltage Versus Input Current



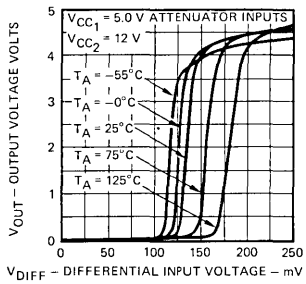
V_{out} Versus V_{DIFF} Transfer Characteristic



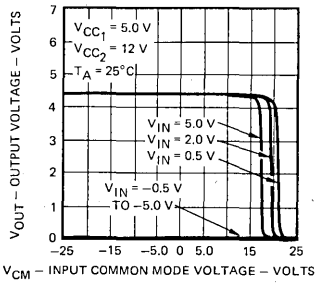
V_{out} Versus V_{DIFF} Transfer Characteristic



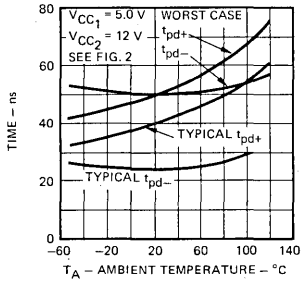
V_{out} Versus V_{DIFF} Transfer Characteristic



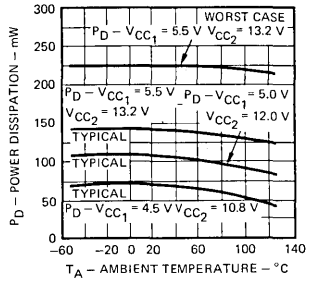
V_{out} Versus V_{CM} Characteristics



Switching Time Versus Ambient Temperature

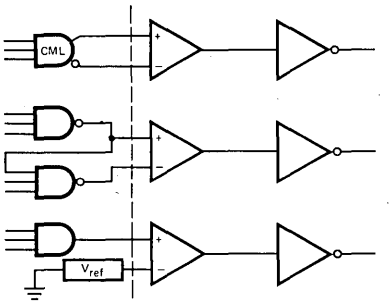


Power Dissipation Versus Ambient Temperature

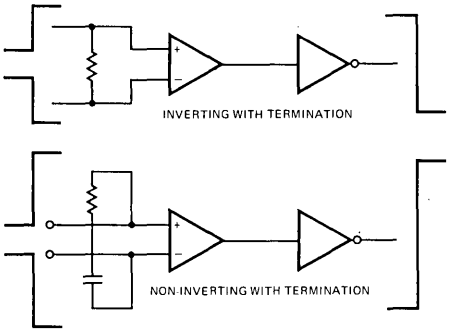


APPLICATIONS

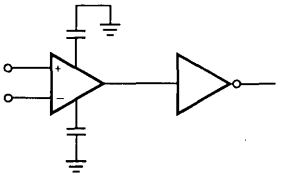
Interfacing Methods



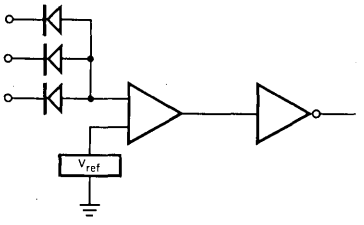
Digital Differential Amplifier (Line Receiver) Expanded Interface



Digital Differential Line Receiver With Inputs Rolled Off

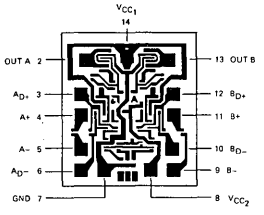


V_{ref} = Resistor, Diodes, or Supply



Metallization and Pad Layout

42 x 48 Mils



Am9621
Dual Line Driver

Distinctive Characteristics

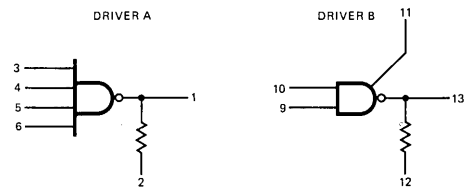
- Dual differential driver
- Transmission line back-matching
- No supply current surges during power-on sequence
- DTL, TTL compatible
- Clamped outputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am9621 is a dual line driver designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair lines are included. The device has the capability of driving high-capacitance loads being able to switch more than 200mA typically during transients.

The Am9621 is designed so that power supplies can be switched on in any sequence without supply current surges.

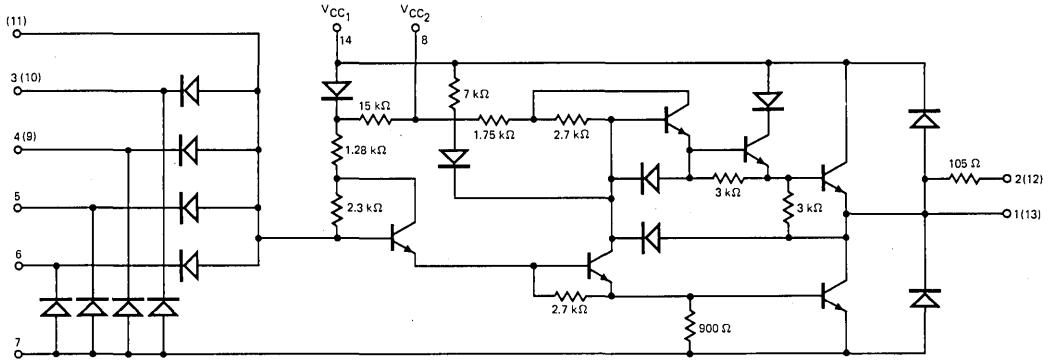
LOGIC DIAGRAM



V_{CC1} = PIN 14
V_{CC2} = PIN 8
GND = PIN 7

4

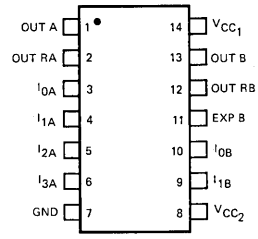
CIRCUIT DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	9621DM
Flat Pak	−55°C to +125°C	9621FM
Dice	−55°C to +125°C	AM9621XM
Hermetic DIP	0°C to +70°C	9621DC
Molded DIP	0°C to +70°C	9621PC
Dice	0°C to +70°C	AM9621XC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
DC Input Voltage	−0.5 V to +15 V
Voltage Applied to Outputs	−2.0 V to +V_{CC1} +1.0 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ELECTRICAL CHARACTERISTICS

Am9621XM - T_A = −55°C to +125°C V_{CC1} = 5.0 V ±10%, V_{CC2} = 12.0 V ±10%
Am9621XC - T_A = 0°C to +75°C V_{CC1} = 5.0 V ±5%, V_{CC2} = 12.0 V ±5%

DC Characteristics (Note 2)

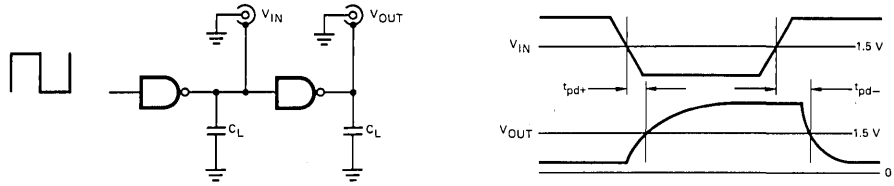
Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am9621XM	V_{CC1} = 4.5 V, I_{OH} = −20 mA	4.00				4.00	4.3				4.00		Volts
	Am9621XC	V_{CC1} = 4.75 V, I_{OH} = −20 mA			4.20		4.20	4.4		4.20				
V_{OL} Output LOW Voltage	Am9621XM	V_{CC1} = 4.5 V, I_{OL} = 20 mA		0.35				0.2	0.35				0.40	Volts
	Am9621XC	V_{CC1} = 4.75 V, I_{OL} = 20 mA				0.40		0.2	0.40		0.45			
V_{OLR} (Note 2) Resistive Output LOW Voltage	Am9621XM	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OL} = 2.8 mA						380	500					mV
	Am9621XC	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OL} = 2.8 mA						380	500					
V_{OHR} (Note 2) Resistive Output HIGH Voltage	Am9621XM	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OH} = −2.3 mA					4.00	4.2						Volts
	Am9621XC	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OH} = −2.3 mA					4.00	4.2						
I_{OL} (Note 1) Output LOW Current	Am9621XM	V_{CC1} = 4.5 V, V_{CC2} = 10.8 V V_O = 5.0 V					150	200						mA
	Am9621XC	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V V_O = 5.0 V					75	200						
V_{IH} Input HIGH Voltage	Am9621XM	V_{CC1} = 4.5 V, V_{CC2} = 13.2 V	2.20				2.00	1.7				1.80		Volts
	Am9621XC	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V			2.20		2.00	1.7		1.80				
V_{IL} Input LOW Voltage	Am9621XM	V_{CC1} = 5.5 V, V_{CC2} = 10.8 V		1.30				1.5	1.00				0.70	Volts
	Am9621XC	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V				1.30		1.5	1.00		0.70			
I_F Input Load Current	Am9621XM	V_{CC1} = 5.5 V, V_F = 0 V V_{CC2} = 13.2 V		1.8				1.15	1.8				1.8	mA
	Am9621XC	V_{CC1} = 5.25 V, V_F = 0 V V_{CC2} = 12.6 V				1.8		1.15			1.8			
I_R Reverse Input Current	Am9621XM	V_{CC1} = 5.5 V, V_R = 5.5 V V_{CC2} = 13.2 V		2.0				<1.0	2.0				5.0	μA
	Am9621XC	V_{CC1} = 5.25 V, V_R = 5.25 V V_{CC2} = 12.6 V				5.0		<1.0	5.0		10.0			
I_{SC} (Note 1) Short Circuit Current	Am9621XM	V_{CC1} = 4.5 V, V_{CC2} = 10.8 V V_O = 0 V					−180	−300						mA
	Am9621XC	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V V_O = 0 V					−100	−300						
I_{CC1} Power Supply Current	AM9621XM	V_{CC1} = 5.5 V, V_{CC2} = 13.2 V Inputs Open		7.0				4.7	7.0				7.3	mA
	Am9621XC	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V Inputs Open				7.0		4.7	7.0		7.3			
I_{CC2} Power Supply Current	AM9621XM	V_{CC1} = 5.5 V, V_{CC2} = 13.2 V Inputs Open		9.8				6.5	9.8				9.8	
	Am9621XC	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V Inputs Open				9.8		6.5	9.8		9.8			
V_{OLC} (Note 3) Output LOW Clamp Voltage	Am9621XM	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OLC} = −20 mA						−1.0	−2.0					Volts
	Am9621XC	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OLC} = −20 mA												
V_{OHC} (Note 3) Output HIGH Clamp Voltage	Am9621XM	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OHC} = 20 mA						6.0	7.0					Volts
	Am9621XC	V_{CC1} = 5.0 V, V_{CC2} = 12 V I_{OHC} = 20 mA						6.0	7.0					

Note 1. Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
2. Test output resistance including 105Ω output resistor.
3. Tests output clamp diodes.
4. For Am9621XM with both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for dual-in-line package (θ_{JA} = 95°C/W) or 300 kHz for ceramic lat Pak (θ_{JA} = 165°C/W).
5. For Am9621XC with both sides loaded at T_A = +75°C, maximum frequency = 500 kHz for both dual-in-line package and ceramic flat pak.

Switching Characteristics

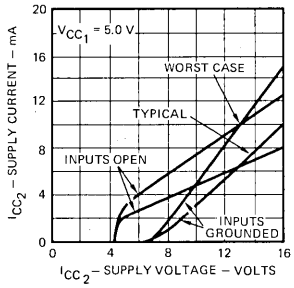
Parameters		Test Conditions	Am9621XM +25°C Min	Typ	Max	Am9621XC +25°C Min	Typ	Max	Units
t_{pd+}	Turn Off Delay	V_{CC1} = 5.0 V, C_L = 30 pF		13	25		13	40	ns
t_{pd-}	Turn On Delay	V_{CC2} = 12 V		9	25		9	40	ns
t_{pd+}	Turn Off Delay	V_{CC1} = 5.0 V, C_L = 5000 pF	(Note 4)	30	150	(Note 5)	30	200	ns
t_{pd-}	Turn On Delay	V_{CC2} = 12 V	(Note 4)	80	150	(Note 5)	80	200	ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

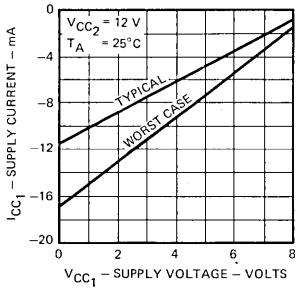


TYPICAL ELECTRICAL CHARACTERISTICS

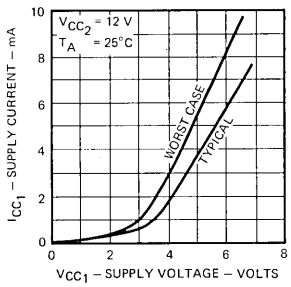
Supply Current Versus Supply Voltage



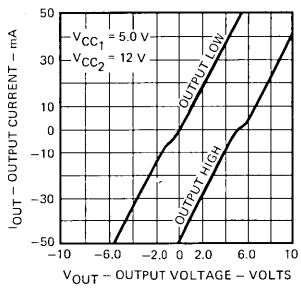
Supply Current Versus Supply Voltage Inputs Grounded



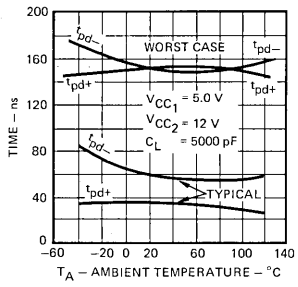
Supply Current Versus Supply Voltage Inputs Open



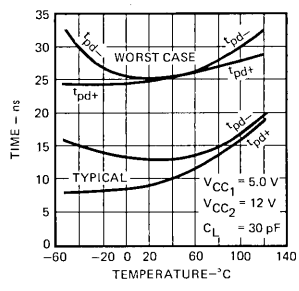
Typical Output Impedance With Back Matching Resistors



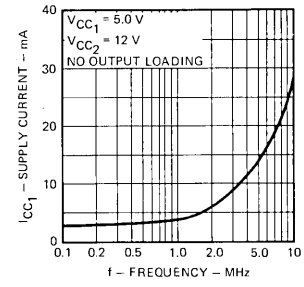
Switching Time Versus Temperature



Switching Time Versus Temperature

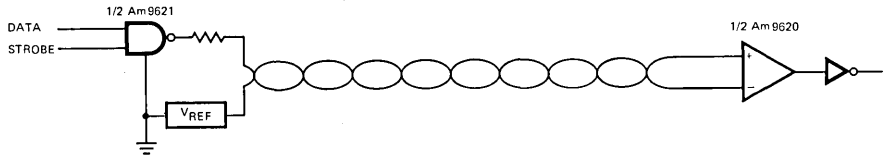


Typical Supply Current Versus Frequency

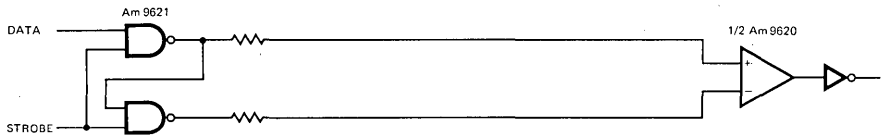


APPLICATIONS

SINGLE-ENDED DRIVING



DIFFERENTIAL DRIVING

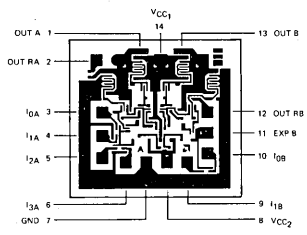


BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

Metallization and Pad Layout

54 x 52 Mils



Magnetic Memory Interface — Section V

Am55/7520 • Am55/7521

Dual Sense Amplifiers

Distinctive Characteristics

- High speed and fast recovery
- High DC noise margin
- ±4mV threshold on Am55/7520
- ±7mV threshold on Am55/7521
- Narrow region of threshold voltage uncertainty
- 100% reliability assurance testing in compliance with MIL-STD-883
- Standard logic supply voltages

FUNCTIONAL DESCRIPTION

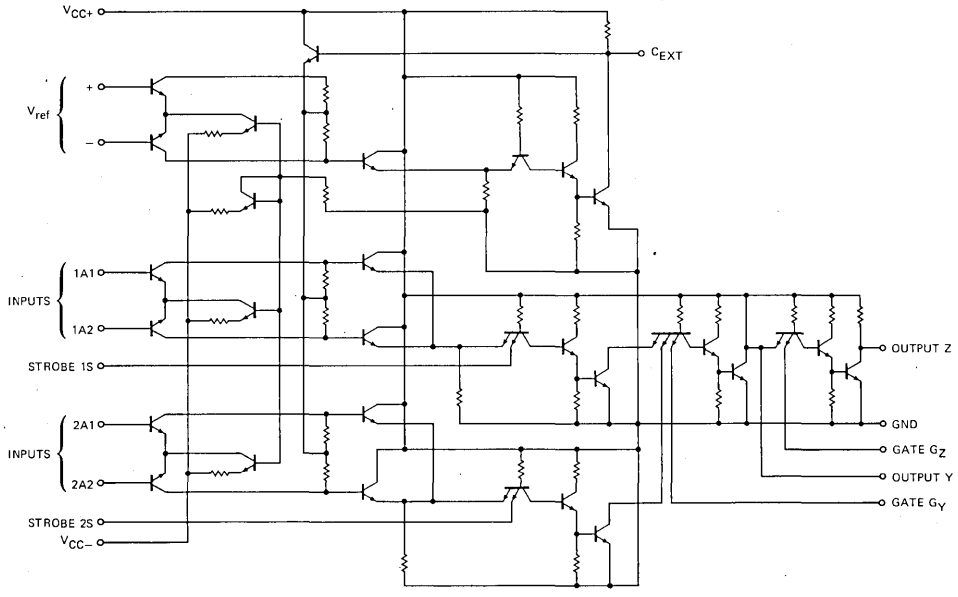
The Am55/7520 and Am55/7521 monolithic sense amplifiers are intended for use in high-speed memory systems. These devices detect bipolar differential-input signals from the memory and provide the required interface with the digital logic.

The Am7520 and Am7521 circuits may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The circuit design provides high stability of the input threshold voltage over a wide range of power supply voltage and temperature variation.

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40mV.

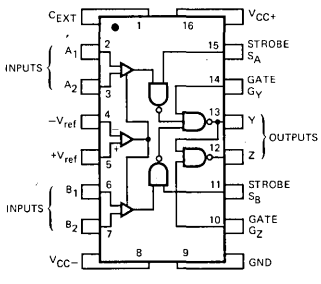
SCHEMATIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am55/7520 Order Number	Am55/7521 Order Number
Molded DIP	0° to +70°C	SN7520N	SN7521N
Hermetic DIP	0° to +70°C	SN7520J	SN7521J
Dice	0° to +70°C	AM7520X	AM7521X
Hermetic DIP	−55° to +125°C	SN5520J	SN5521J
Hermetic Flat Pak	−55° to +125°C	SN5520W	SN5521W
Dice	−55° to +125°C	AM5520X	AM5521X

LOGIC SYMBOL AND CONNECTION DIAGRAM
Top View



Notes:
Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		−65°C to +150°C
Operating Temperature (Ambient) Range		−55°C to +125°C
Supply Voltages	V_{CC+}	+7.0V
	V_{CC-}	−7.0V
Differential Input Voltage, V_{ID} or V_{ref}		±5.0V
Voltage from any Input to Ground		+5.0V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am7520, Am7521 T_A = 0°C to +70°C MIN. = 4.75V MAX. = 5.25V
Am5520, Am5521 T_A = −55°C to +125°C MIN. = −4.75V MAX. = −5.25V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_T	Differential-Input Threshold Voltage (Fig. 1, Note 3)	V_{ref} = 15mV	Am55/7521		8.0	15	22	mV
			Am55/7520	0°C to +70°C	11	15	19	
				−55°C to 0°C	10	15	20	
				+70°C to +125°C				
		V_{ref} = 40mV	Am55/7521		33	40	47	mV
			Am55/7520	0°C to +70°C	36	40	44	
				−55°C to 0°C	35	40	45	
				+70°C to +125°C				
V_{ICF}	Common-Mode Input Firing Voltage (Note 4)	V_{ref} = 40mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse = $t_r \leq 15ns$, $t_f \leq 15ns$, $t_w = 50ns$				±2.5		Volts
I_{IB}	Differential-Input Bias Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0		0°C to T_A max.		30	75	µA
				−55°C to 0°C			100	
I_{IO}	Differential-Input Offset Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0				0.5		µA
V_{IH}	High-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic HIGH			2.0			Volts
V_{IL}	Low-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic LOW					0.8	Volts
V_{OH}	High-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OH} = −400µA			2.4	4.0		Volts
V_{OL}	Low-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OL} = 16mA				0.25	0.4	Volts
I_{IH}	High-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 2.4V					40	µA
I_{IL}	Low-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IL} = 0.4V				−1.0	−1.6	mA
$I_{OS(Y)}$	Short-Circuit Output Current Into Y (Fig. 5)	V_{CC+} = 5.25V, V_{CC-} = −5.25V			−3.0		−5.0	mA
$I_{OS(Z)}$	Short-Circuit Output Current Into Z (Fig. 5)	V_{CC+} = 5.25V, V_{CC-} = −5.25V			−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				28	40	mA
I_{CC-}	Supply Current from V_{CC-} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C					−20	mA

Notes:
1. Electrical characteristics unless otherwise noted V_{CC+} = 0V, V_{CC-} = −5.0V, T_A = operating temperature range.
2. Typical values are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, 25°C ambient and maximum loading.
3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

Typical Recovery and Cycle Times (V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C, $C_{ext} \geq 100pF$)

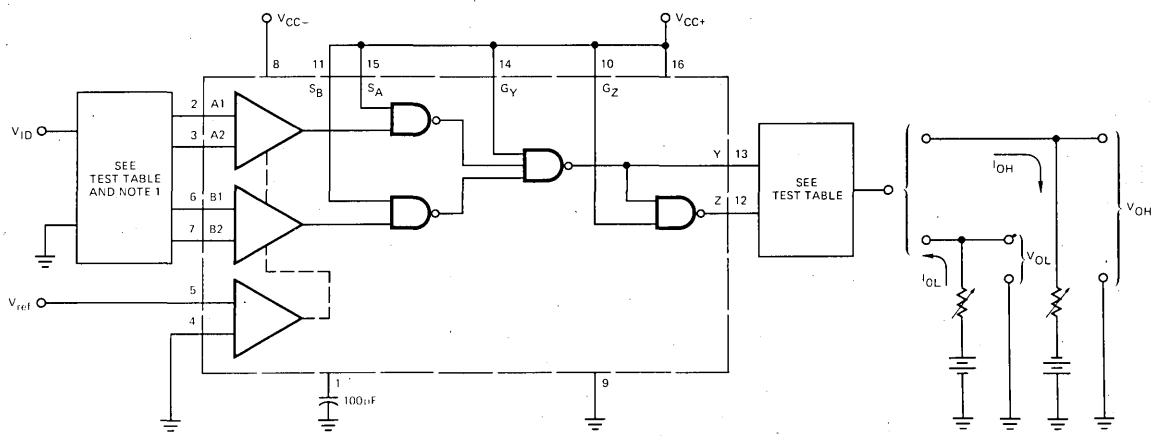
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{or\ D}$	Differential-Input Overload Recovery Time (Note 1)	Differential-Input Pulse V_{ID} = 2.0V, $t_r = t_f$ = 20ns		20		ns
$t_{or\ C}$	Common-Mode-Input Overload Recovery Time (Note 2)	Common-Mode Input Pulse V_{IC} = ±2.0V, $t_r = t_f$ = 20ns		20		ns
$t_{cyc(min.)}$	Minimum Cycle Time			200		ns

Notes:
1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
2. Common-mode-input overload recovery time is the time necessary for the device to recover from, the specified common-mode-input overload signal prior to the strobe-enable signal.

Switching Characteristics (V_{CC+} = 5.0V, V_{CC-} = 5.0V, $C_{EXT} \geq 100$ pF, $T_A = 25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{PLH(DR)}$	Propagation Delay Times From Input A1-A2 or B1-B2 to Output Y (Fig. 7)	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DR)}$				20		
$t_{PLH(DZ)}$	Propagation Delay Times From Input A1-A2 or B1-B2 to Output Z (Fig. 7)	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$				35	55	
$t_{PLH(SY)}$	From Input Strobe A or B to Output Y (Fig. 7)	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$				20		
$t_{PLH(SZ)}$	From Input Strobe A or B to Output Z (Fig. 7)	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$				35	55	
$t_{PLH(GY, Y)}$	From Input Gate G_Y to Output Y (Fig. 8)	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$				10		
$t_{PLH(GY, Z)}$	From Input Gate G_Y to Output Z (Fig. 8)	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$				20	30	
$t_{PLH(GZ, Z)}$	From Input Gate G_Z to Output Z (Fig. 9)	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$				10	20	

DC PARAMETER MEASUREMENT INFORMATION



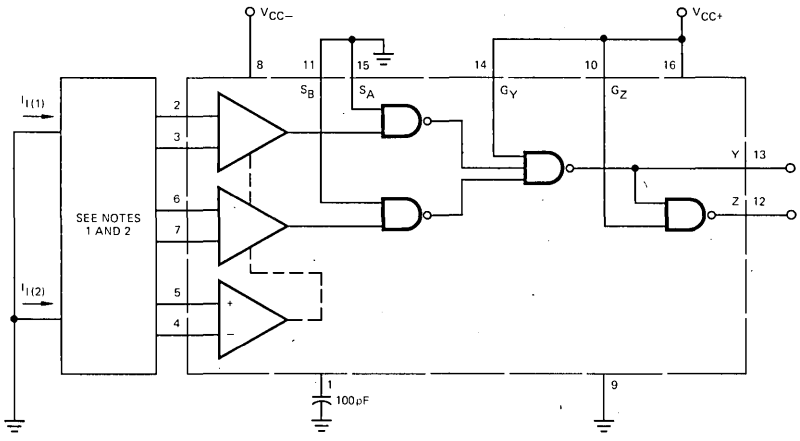
Note 1. Each pair of differential inputs is tested separately with the other pair grounded.

TEST TABLE

INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
			V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
A1-A2 or B1-B2	15mV	≤11mV	≤0.4V		16mA	≥2.4V	−400μA	
A1-A2 or B1-B2	15mV	≥19mV	≥2.4V	−400μA		≤0.4V		16mA
A1-A2 or B1-B2	40mV	≤26mV	≤0.4V		16mA	≥2.4V	−400μA	
A1-A2 or B1-B2	40mV	≥44mV	≥2.4V	−400μA		≤0.4V		16mA
A1-A2 or B1-B2	15mV	≤ 8mV	≤0.4V		16mA	≥2.4V	−400μA	
A1-A2 or B1-B2	15mV	≥22mV	≥2.4V	−400μA		≤0.4V		16mA
A1-A2 or B1-B2	40mV	≤33mV	≤0.4V		16mA	≥2.4V	−400μA	
A1-A2 or B1-B2	40mV	≥47mV	≥2.4V	−400μA		≤0.4V		16mA

Figure 1. V_T

DC PARAMETER MEASUREMENT INFORMATION (Cont.)



Notes: 1. Each preamplifier is tested separately. Inputs not under test are grounded.
2. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

Figure 2. I_{IB} and I_{IO}

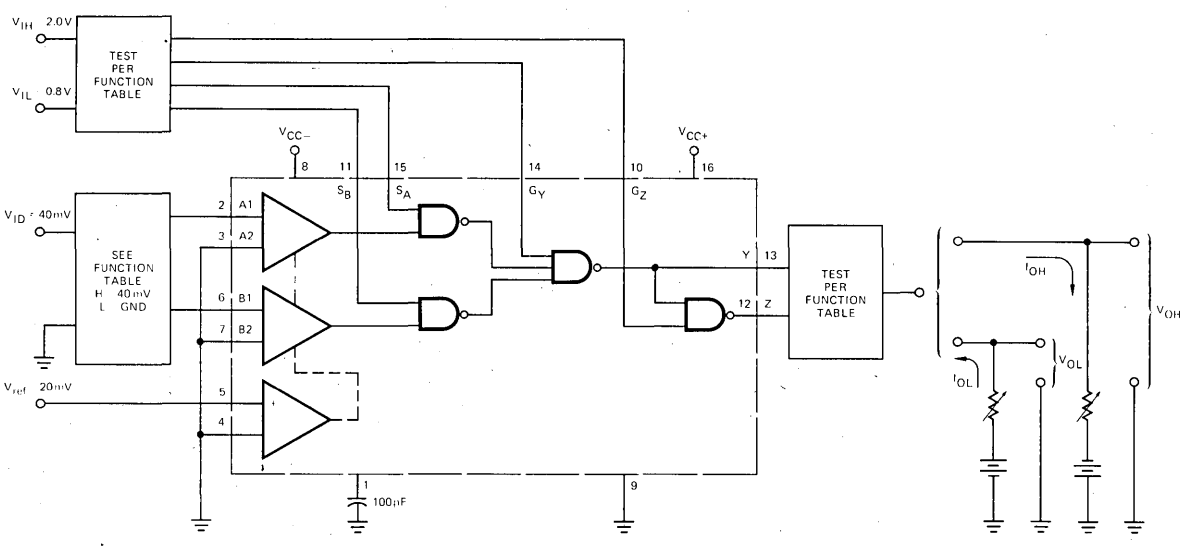
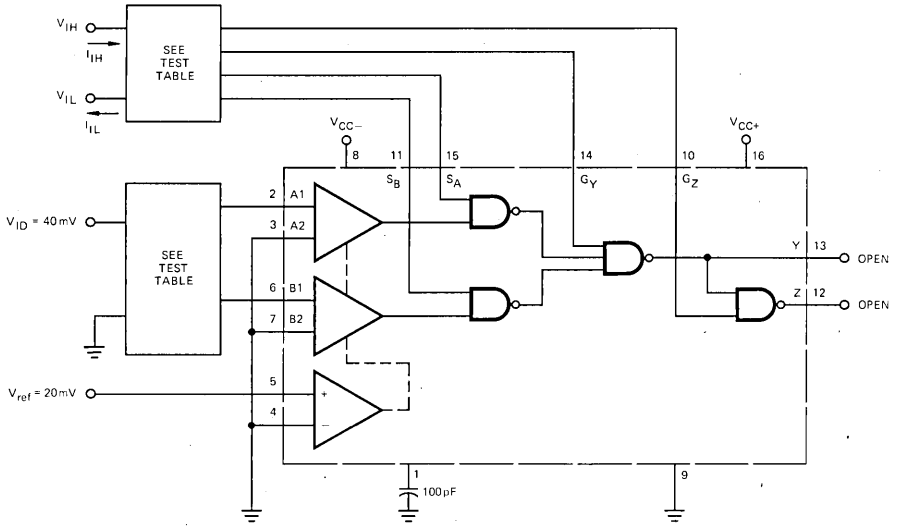


Figure 3. V_{IH}, V_{IL}, V_{OH}, V_{OL}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)

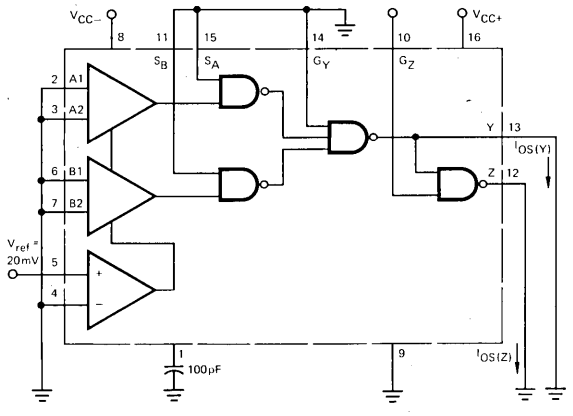


Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

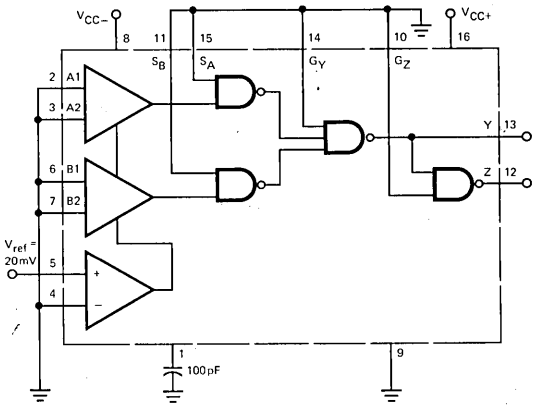
Figure 4. I_{IH}, I_{IL}



Note 1. When testing $I_{OS(Y)}$, pin 10 is open; when testing $I_{OS(Z)}$, pin 10 is grounded.

Figure 5. I_{OS}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)



Note 1. When testing $I_{OS(Y)}$, pin 10 is open; when testing $I_{OS(Z)}$, pin 10 is grounded.

Figure 6. I_{CC+} and I_{CC-}

FUNCTION TABLE

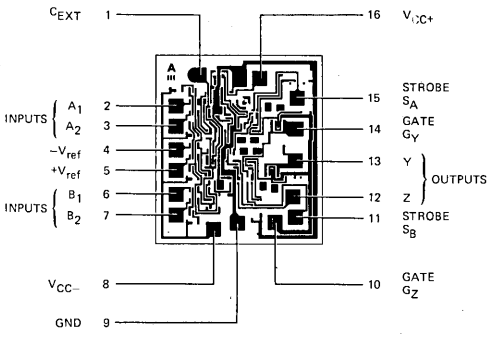
INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\bar{G}_Z$
H	X	X	X	H	X	H	$\bar{G}_Z$
X	H	X	X	X	H	H	$\bar{G}_Z$
L	L	H	X	X	H	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

DEFINITION OF ABOVE LOGIC LEVELS

INPUT	H	L	X
A	$V_{ID} \geq V_T$ max.	$V_{ID} \leq V_T$ min.	IRRELEVANT
S	$V_I \geq V_{IH}$ min.	$V_I \leq V_{IL}$ max.	IRRELEVANT

Note: A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

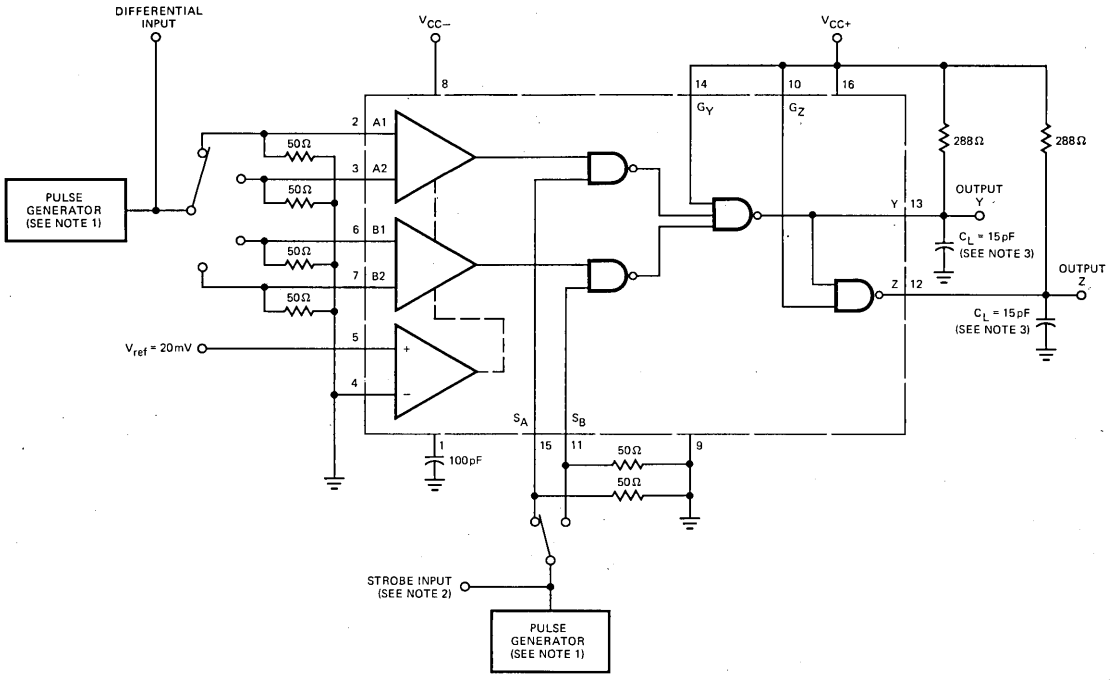
Metallization and Pad Layout



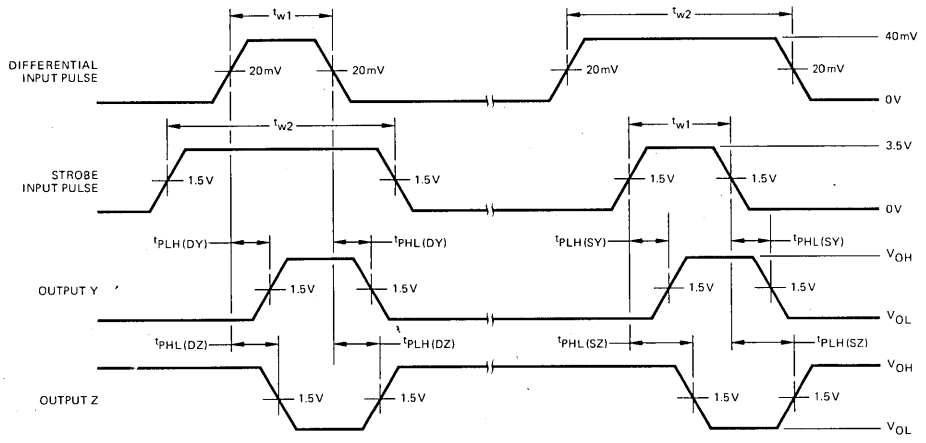
DIE SIZE 0.061" X 0.063"

SWITCHING PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS

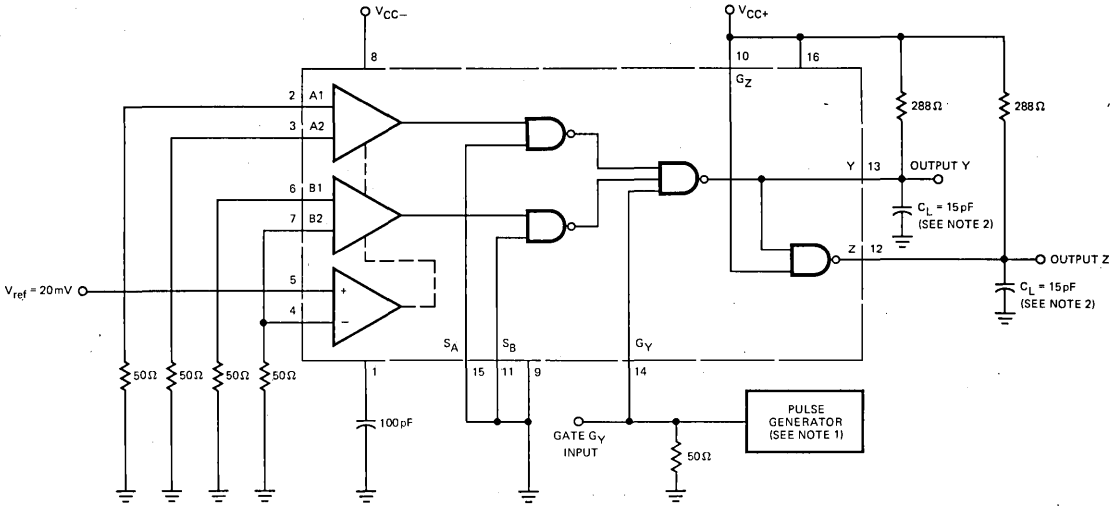


Notes: 1. The pulse generators have the following characteristics: $Z_O = 50\Omega$, $t_r = 15 \pm 5$ns, $t_f = 15 \pm 5$ns, $t_{w1} = 100$ns, $t_{w2} = 300$ns, and PRR = 1MHz.
2. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.
3. C_L includes probe and jig capacitance.

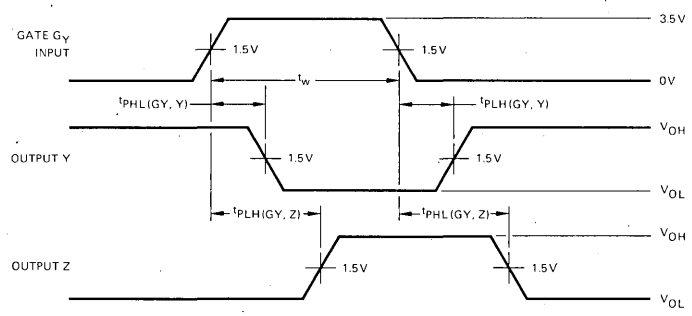
Figure 7. Propagation Delay Times from Differential and Strobe Inputs.

SWITCHING PARAMETER MEASUREMENT INFORMATION (Cont.)

TEST CIRCUIT



VOLTAGE WAVEFORMS

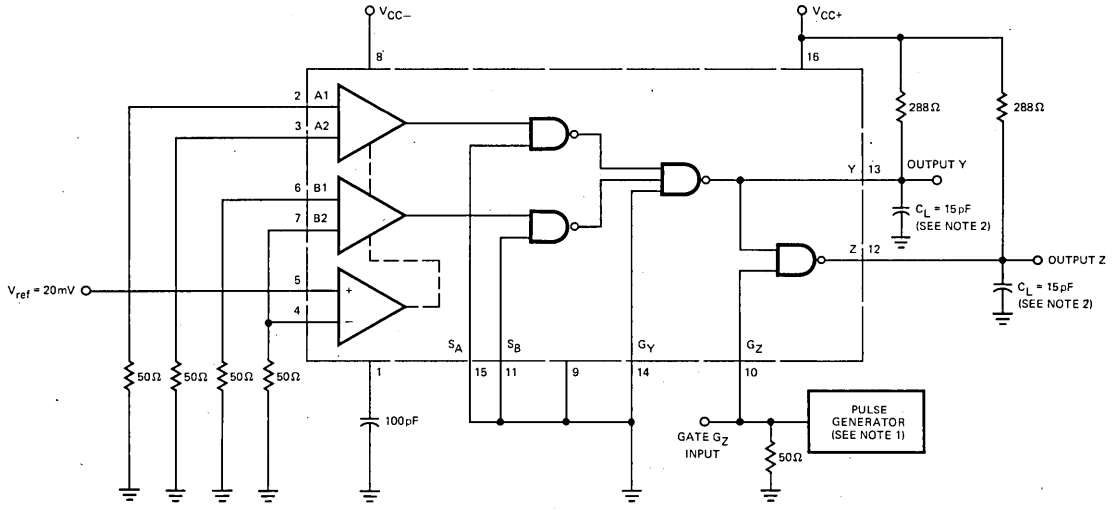


Notes: 1. The pulse generator has the following characteristics: $Z_O = 50\Omega$, $t_r = 15 \pm 5$ns, $t_f = 15 \pm 5$ns, $t_w = 100$ns, and PRR = 1MHz.
2. C_L includes probe and jig capacitance.

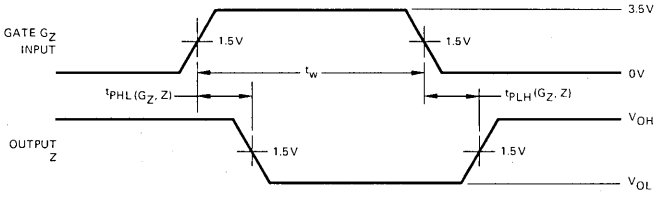
Figure 8. Propagation Delay Times from Gate GY.

SWITCHING PARAMETER MEASUREMENT INFORMATION (Cont.)

TEST CIRCUIT



VOLTAGE WAVEFORMS

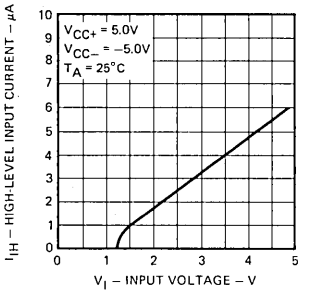


Notes: 1. The pulse generator has the following characteristics: $Z_O = 50\Omega$, $t_r = 15 \pm 5$ns, $t_f = 15 \pm 5$ns, $t_w = 100$ns, and PRR = 1MHz.
2. C_L includes probe and jig capacitance.

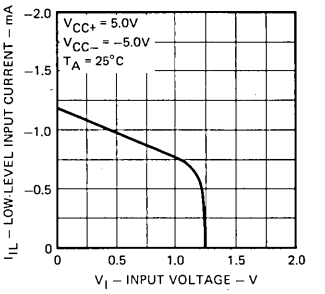
Figure 9. Propagation Delay Times from Gate G_Z.

TYPICAL CHARACTERISTICS

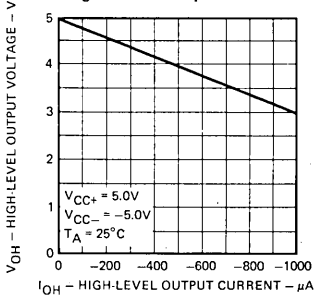
High-Level Input Current Versus Input Voltage



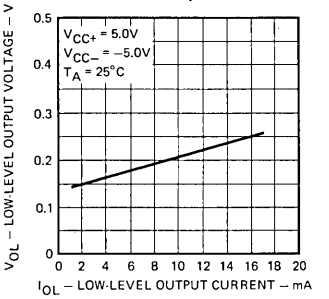
Low-Level Input Current Versus Input Voltage



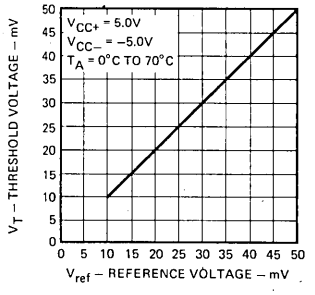
High-Level Output Voltage Versus High-Level Output Current



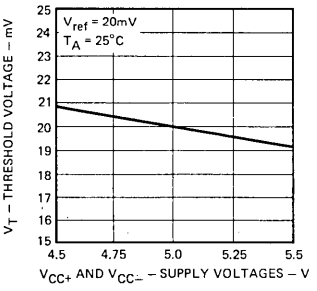
Low-Level Output Voltage Versus Low-Level Output Current



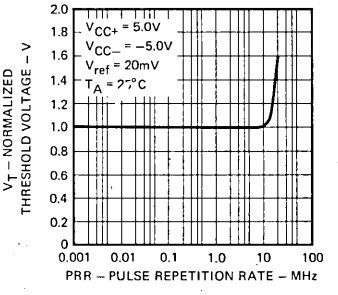
Threshold Voltage Versus Reference Voltage



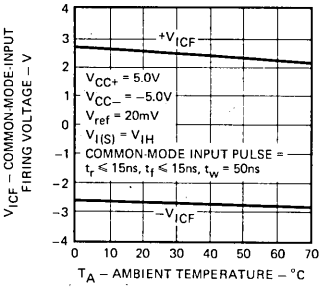
Threshold Voltage Versus Supply Voltage



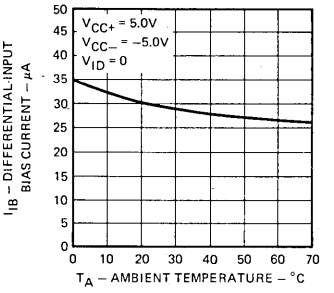
Normalized Threshold Voltage Versus Pulse Repetition Rate



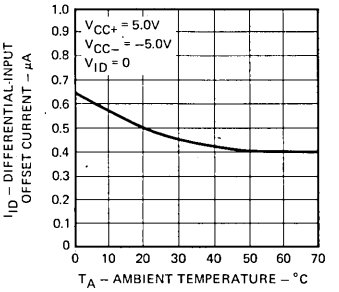
Common-Mode Firing Voltage Versus Ambient Temperature



Differential-Input Bias Current Versus Ambient Temperature



Differential-Input Offset Current Versus Ambient Temperature



Am55/75234 • Am55/75235

Dual Sense Amplifiers

Distinctive Characteristics

- High speed and fast recovery time
- High DC noise margin
- ±4mV threshold on Am55/75234
- ±7mV threshold on Am55/75235
- Narrow region of threshold voltage uncertainty
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCITONAL DESCRIPTION

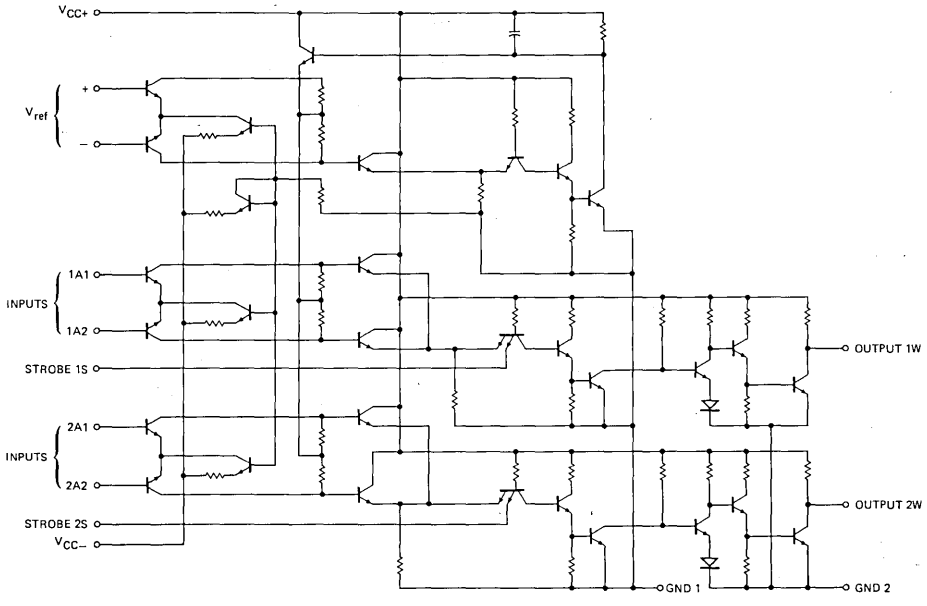
The Am55/75234 and Am55/75235 monolithic sense amplifiers are intended for use in high-speed memory systems. These devices detect bipolar differential-input signals from the memory and provide the required interface with the digital logic.

Each device contains two differential input preamplifiers and an output driver that has a separate strobe input. Both sense amplifiers have inverted outputs and are internally compensated.

The circuit design provides high stability of the input threshold voltage over a wide range of power supply voltage and temperature variation.

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40mV.

SCHEMATIC DIAGRAM

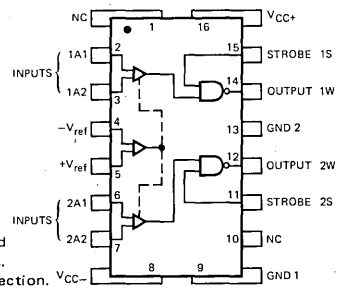


ORDERING INFORMATION

Package Type	Temperature Range	Am55/75234 Order Number	Am55/75235 Order Number
Molded Dip	0°C to +70°C	SN75234N	SN75235N
Hermetic DIP	0°C to +70°C	SN75234J	SN75235J
Dice	0°C to +70°C	AM75234X	AM75235X
Hermetic DIP	–55°C to +125°C	SN55234J	SN55235J
Hermetic Flat Pak	–55°C to +125°C	SN55234W	SN55235W
Dice	–55°C to +125°C	AM55234X	AM55235X

LOGIC SYMBOL AND CONNECTION DIAGRAM

Top View



Notes:
Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		−65°C to +150°C
Operating Temperature (Ambient) Range		−55°C to +125°C
Supply Voltages	V_{CC+}	+7.0V
	V_{CC-}	−7.0V
Differential Input Voltage, V_{ID} or V_{ref}		±5.0V
Voltage from any Input to Ground		+5.5V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am75234, Am75235 T_A = 0°C to +70°C
Am55234, Am55235 T_A = −55°C to +125°C
V_{CC+} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V
V_{CC-} = −5.0V ±5% MIN. = −4.75V MAX. = −5.25V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_T	Differential-Input Threshold Voltage (Fig. 1, Note 3)	V_{ref} = 15mV	Am55/75235		8.0	15	22	mV
			Am55/75234	0°C to +70°C	11	15	19	
				−55°C to 0°C	10	15	20	
				+70°C to +125°C				
		V_{ref} = 40mV	Am55/75235		33	40	47	mV
			Am55/75234	0°C to +70°C	36	40	44	
				−55°C to 0°C	35	40	45	
				+70°C to +125°C				
V_{ICF}	Common-Mode Input Firing Voltage (Note 4)	V_{ref} = 40mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse = $t_r \leq 15ns$, $t_f \leq 15ns$, $t_w = 50ns$				±2.5		Volts
I_{IB}	Differential-Input Bias Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0		0°C to T_A max.		30	75	µA
				−55°C to 0°C			100	
I_{IO}	Differential-Input Offset Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0				0.5		µA
V_{IH}	High-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic HIGH			2.0			Volts
V_{IL}	Low-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic LOW					0.8	Volts
V_{OH}	High-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OH} = −400µA			2.4	4.0		Volts
V_{OL}	Low-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OL} = 16mA				0.25	0.4	Volts
I_{IH}	High-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 2.4V					40	µA
		V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 5.25V					1.0	mA
I_{IL}	Low-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IL} = 0.4V				−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current (Fig. 5)	V_{CC+} = 5.25V, V_{CC-} = −5.25V			−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				25	40	mA
I_{CC-}	Supply Current from V_{CC-} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				−15	−20	mA

Notes:
1. Electrical characteristics unless otherwise noted V_{CC+} = 5V, V_{CC-} = −5V, T_A = operating temperature range.
2. Typical values are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, 25°C ambient and maximum loading.
3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

Switching Characteristics (V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C)

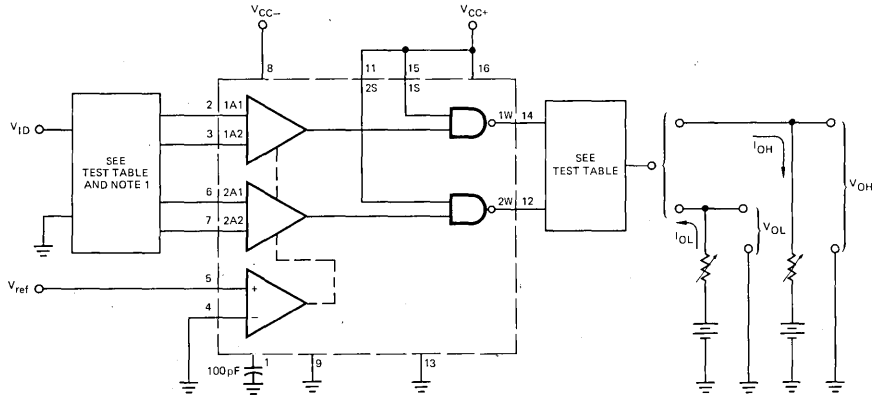
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Times From Input A1-A2 to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		25		ns
t_{PHL}				25	40	
t_{PLH}	Propagation Delay Times From Input Strobe to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		25		ns
t_{PHL}				15	30	

Typical Recovery and Cycle Times (V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C, C_{ext} ⩾ 100pF)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{or} D	Differential-Input Overload Recovery Time (Note 1)	Differential-Input Pulse V_{ID} = 2.0V, $t_r = t_f$ = 20ns		20		ns
t_{or} C	Common-Mode-Input Overload Recovery Time (Note 2)	Common-Mode Input Pulse V_{IC} = ±2.0V, $t_r = t_f$ = 20ns		20		ns
$t_{cyc(min.)}$	Minimum Cycle Time			200		ns

Notes: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
2. Common-mode-input overload recovery time is the time necessary for the device to recover from, the specified common-mode-input overload signal prior to the strobe-enable signal.

DC PARAMETER MEASUREMENT INFORMATION

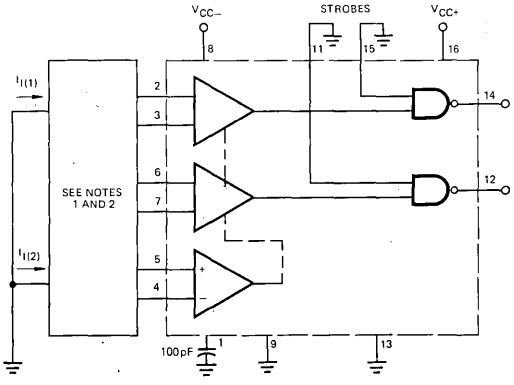


TEST TABLE

INPUTS	V_{ref}	V_{ID}			OUTPUTS		
		Am75234	Am55234	Am55/75235	V_O	I_{OH}	I_{OL}
A1-A2	15mV	⩽11mV	⩽10mV	⩽8mV	⩾2.4mV	−400μA	
A1-A2	15mV	⩾19mV	⩾20mV	⩾22mV	⩽0.4V		16mA
A1-A2	40mV	⩽36mV	⩽35mV	⩽33mV	⩾2.4V	−400μA	
A1-A2	40mV	⩾44mV	⩾45mV	⩾47mV	⩽0.4V		16mA

Note 1. Each pair of inputs is tested separately with its corresponding output.

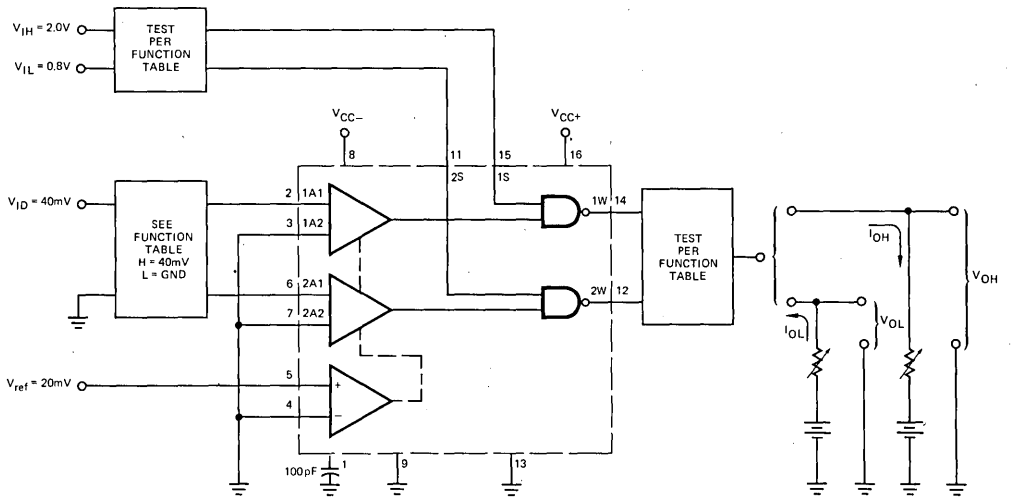
Figure 1. V_T



Notes: 1. Each preamplifier is tested separately. Inputs not under test are grounded.
2. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

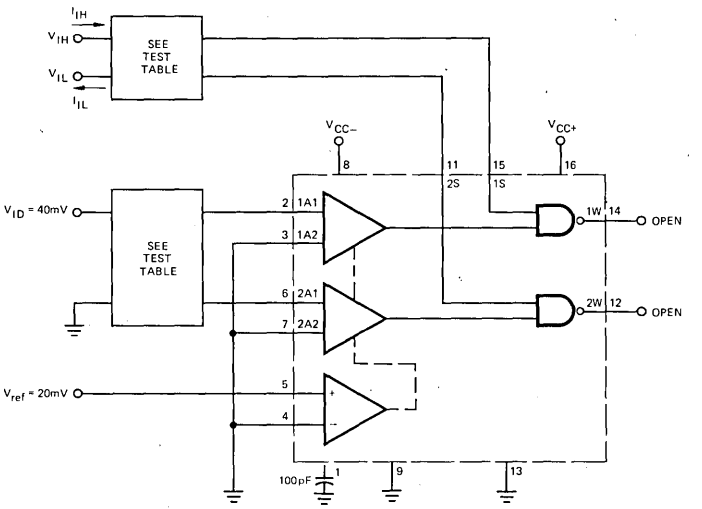
Figure 2. I_{IB} and I_{IO}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)



Note 1. Arrows indicate actual direction of current flow. Current into terminal is a positive value.

Figure 3. V_{IH}, V_{IL}, V_{OH} and V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} AT STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} AT STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} AT STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} AT STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Figure 4. I_{IH} and I_{IL}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)

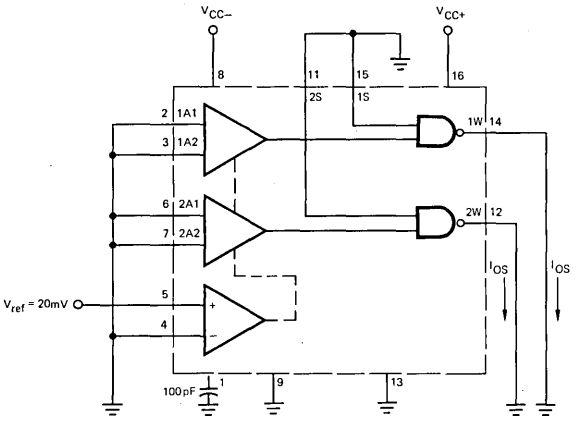


Figure 5. I_{OS}

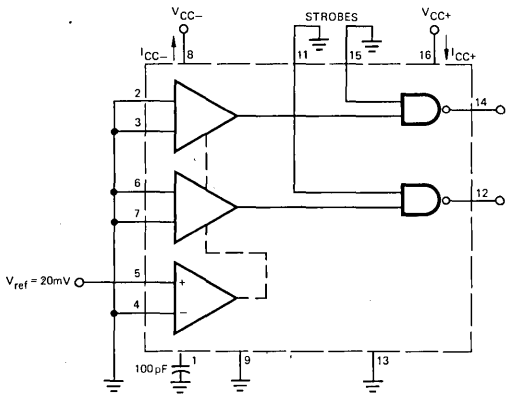


Figure 6. I_{CC+} and I_{CC-}

FUNCTION TABLE

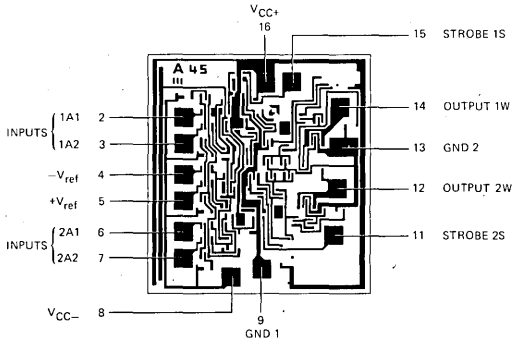
INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

DEFINITION OF ABOVE LOGIC LEVELS

INPUT	H	L	X
A	$V_{ID} \geq V_T$ max.	$V_{ID} \leq V_T$ min.	IRRELEVANT
S	$V_I \geq V_{IH}$ min.	$V_I \leq V_{IL}$ max.	IRRELEVANT

Note: A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

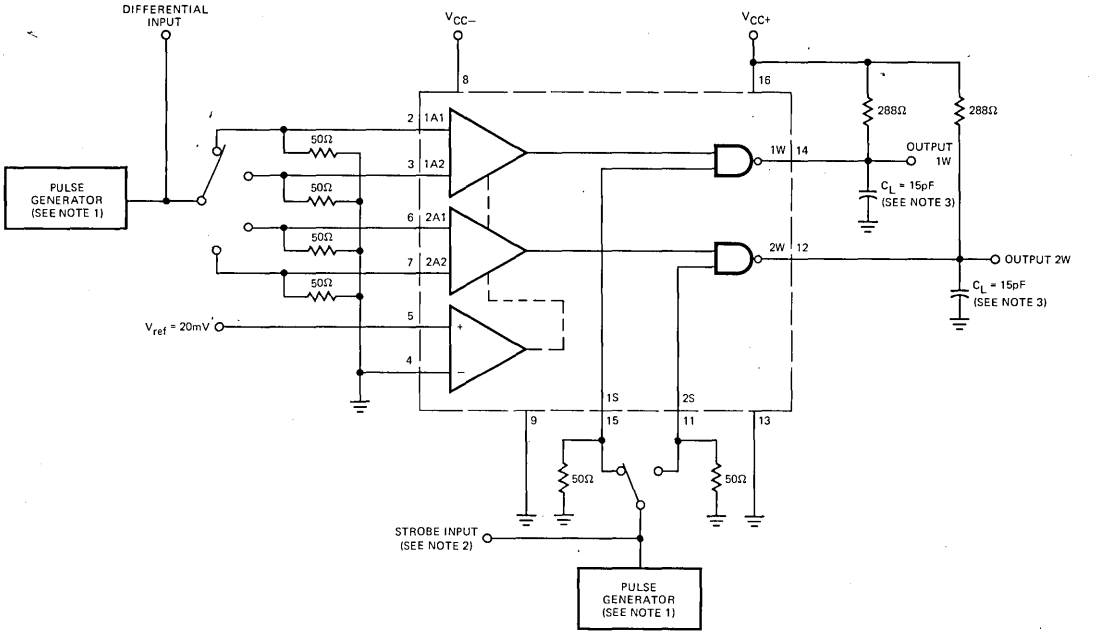
Pad Layout



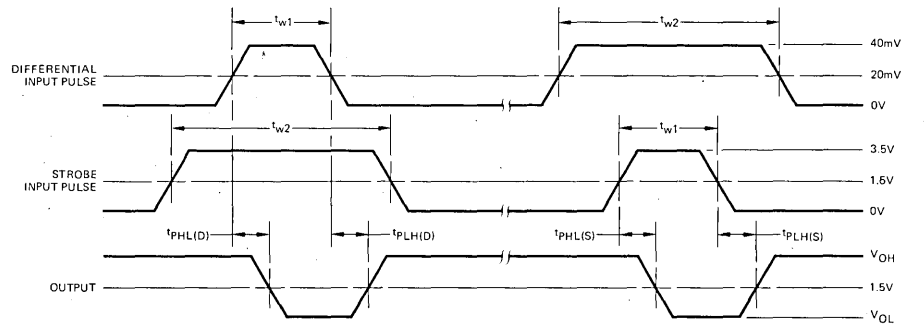
DIE SIZE 0.061" X 0.063"

SWITCHING PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS

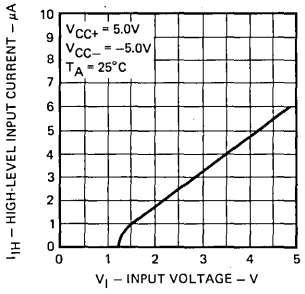


Notes: 1. The pulse generators have the following characteristics: Z_O = 50Ω, t_r = 15 ± 5ns, t_f = 15 ± 5ns, t_{w1} = 100ns, t_{w2} = 300ns, and PRR = 1 MHz.
2. The strobe input pulse is applied to Strobe 1S when inputs 1A1–1A2 are being tested and to Strobe 2S when inputs 2A1–2A2 are being tested.
3. C_L includes probe and jig capacitance.

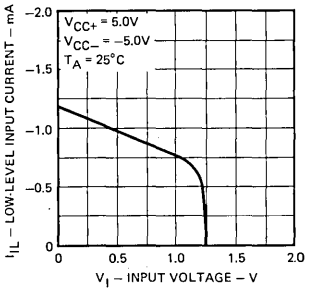
Figure 7. Propagation Delay Times.

TYPICAL CHARACTERISTICS

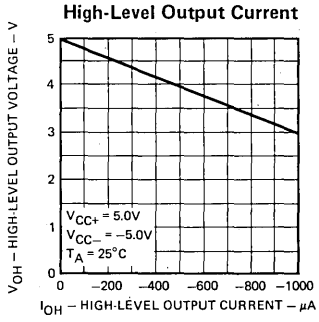
High-Level Input Current Versus Input Voltage



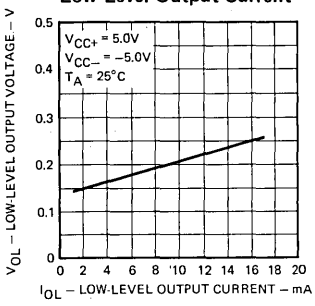
Low-Level Input Current Versus Input Voltage



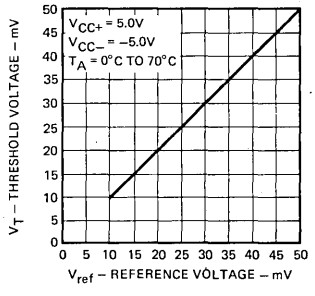
High-Level Output Voltage Versus High-Level Output Current



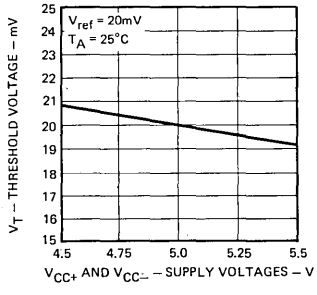
Low-Level Output Voltage Versus Low-Level Output Current



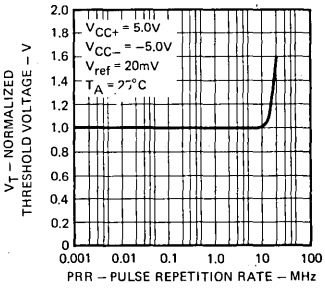
Threshold Voltage Versus Reference Voltage



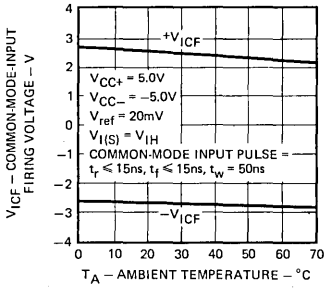
Threshold Voltage Versus Supply Voltage



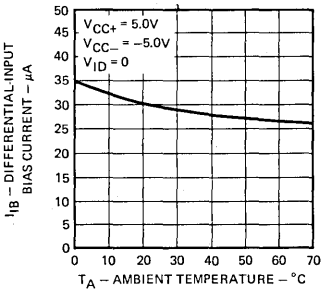
Normalized Threshold Voltage Versus Pulse Repetition Rate



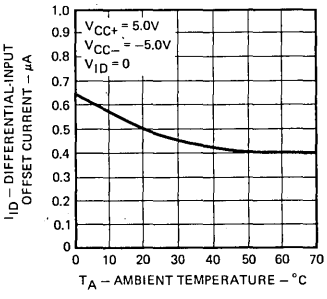
Common-Mode Firing Voltage Versus Ambient Temperature



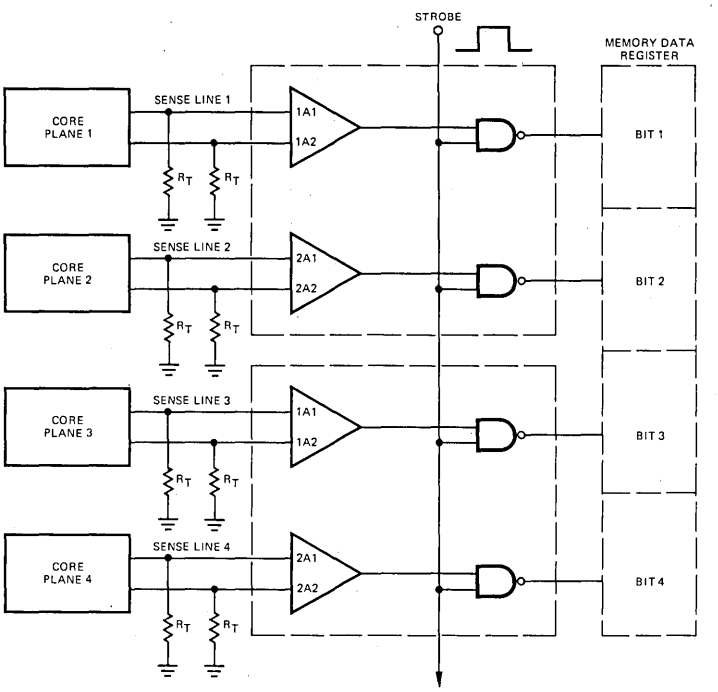
Differential-Input Bias Current Versus Ambient Temperature



Differential-Input Offset Current Versus Ambient Temperature



TYPICAL APPLICATIONS



SMALL MEMORY SYSTEM SENSE LINES

Am55/75238 • Am55/75239

Dual Sense Amplifiers with Preamplifier Test Point

Distinctive Characteristics

- Test point on each sense preamplifier
- ±4mV threshold on Am55/75238
- ±7mV threshold on Am55/75239
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTION DESCRIPTION

The Am55/75238 and Am55/75239 monolithic sense amplifiers are intended for use in high-speed memory systems. These devices detect bipolar differential-input signals from the memory and provide the required interface with the digital logic.

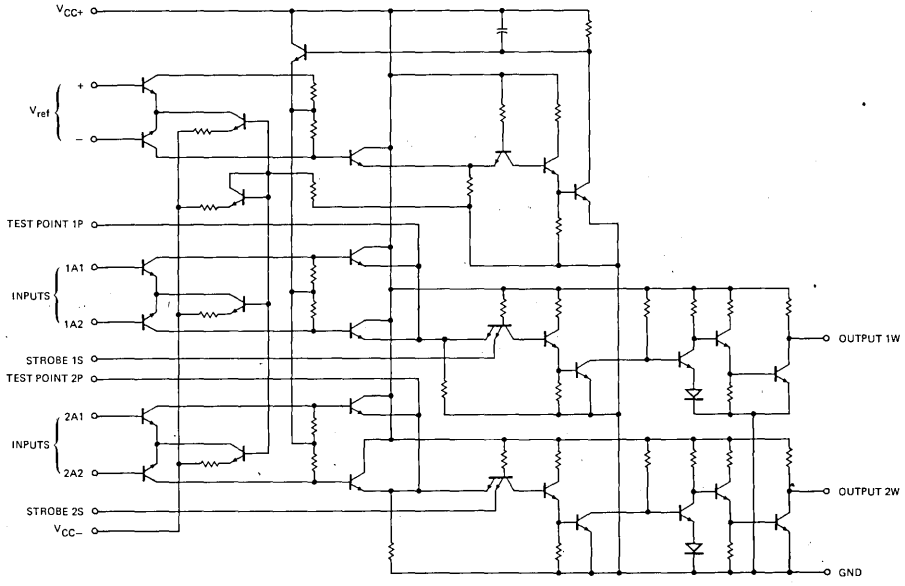
Each device contains two differential input preamplifiers and an output driver that has a separate strobe input. Both sense amplifiers have inverted outputs and are internally compensated.

The circuit design provides high stability of the input threshold voltage over a wide range of power supply voltage and temperature variation.

The Am55/75238 and Am55/75239 sense amplifiers contain test points at the output of each sense preamplifier. The test point data is inverted with respect to the normal sense amplifier output.

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40mV.

SCHEMATIC DIAGRAM

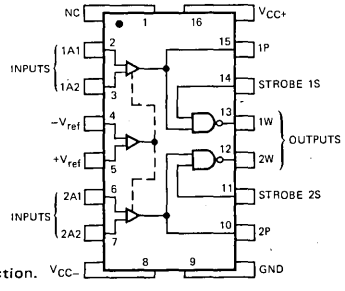


ORDERING INFORMATION

Package Type	Temperature Range	Am55/75238 Order Number	Am55/75239 Order Number
Molded DIP	0°C to +70°C	SN75238N	SN75239N
Hermetic DIP	0°C to +70°C	SN75238J	SN75239J
Dice	0°C to +70°C	AM75238X	AM75239X
Hermetic DIP	−55°C to +125°C	SN55238J	SN55239J
Hermetic Flat Pak	−55°C to +125°C	SN55238W	SN55239W
Dice	−55°C to +125°C	AM55238X	AM55239X

LOGIC SYMBOL AND CONNECTION DIAGRAM

Top View



Notes:
Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature (Ambient) Range	−55°C to +125°C
Supply Voltages V_{CC+}	+7.0V
V_{CC-}	−7.0V
Differential Input Voltage, V_{ID} or V_{ref}	±5.0V
Voltage from any Input to Ground	+5.5V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am75238, Am75239 T_A = 0°C to +70°C
Am55238, Am55239 T_A = −55°C to +125°C
V_{CC+} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V
V_{CC-} = −5.0V ±5% MIN. = −4.75V MAX. = −5.25V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_T	Differential-Input Threshold Voltage (Fig. 1, Note 3)	V_{ref} = 15mV	Am55/75239		8.0	15	22	mV
			Am55/75238	0°C to +70°C	11	15	19	
				−55°C to 0°C	10	15	20	
				+70°C to +125°C				
		V_{ref} = 40mV	Am55/75239		33	40	47	mV
			Am55/75238	0°C to +70°C	36	40	44	
				−55°C to 0°C	35	40	45	
				+70°C to +125°C				
V_{ICF}	Common-Mode Input Firing Voltage (Note 4)	V_{ref} = 40mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse = $t_r \leq 15ns$, $t_f \leq 15ns$, $t_w = 50ns$				±2.5		Volts
I_{IB}	Differential-Input Bias Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0		0°C to T_A max.		30	75	μA
				−55°C to 0°C			100	
I_{IO}	Differential-Input Offset Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0				0.5		μA
V_{IH}	High-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic HIGH			2.0			Volts
V_{IL}	Low-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic LOW					0.8	Volts
V_{OH}	High-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OH} = −400μA			2.4	4.0		Volts
V_{OL}	Low-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OL} = 16mA				0.25	0.4	Volts
I_{IH}	High-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 2.4V					40	μA
		V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 5.25V					1.0	mA
I_{IL}	Low-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IL} = 0.4V				−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current (Fig. 5)	V_{CC+} = 5.25V, V_{CC-} = −5.25V			−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				25	40	mA
I_{CC-}	Supply Current from V_{CC-} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				−15	−20	mA

Notes:
1. Electrical characteristics unless otherwise noted V_{CC+} = 5V, V_{CC-} = −5V, T_A = operating temperature range.
2. Typical values are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, 25°C ambient and maximum loading.
3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

Switching Characteristics (V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C)

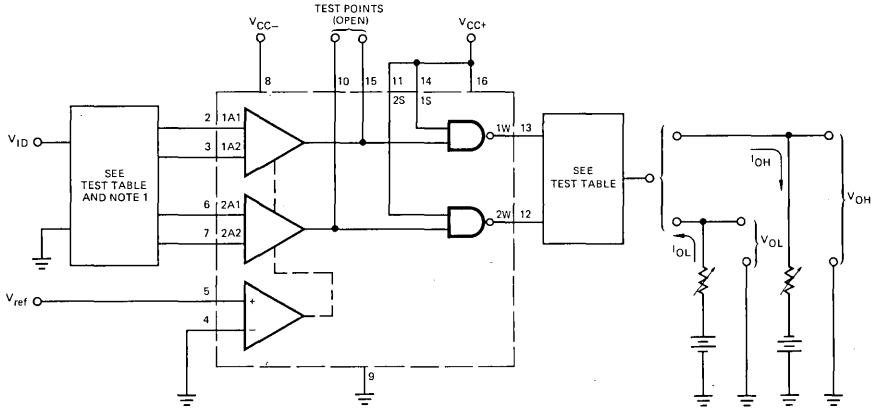
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Times From Input A1-A2 to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		25		ns
t_{PHL}				25	40	
t_{PLH}	Propagation Delay Times From Input Strobe to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		25		ns
t_{PHL}				15	30	

Typical Recovery and Cycle Times (V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C, $C_{ext} \geq$ 100pF)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{or} D	Differential-Input Overload Recovery Time (Note 1)	Differential-Input Pulse V_{ID} = 2.0V, $t_r = t_f$ = 20ns		20		ns
t_{or} C	Common-Mode-Input Overload Recovery Time (Note 2)	Common-Mode Input Pulse V_{IC} = ±2.0V, $t_r = t_f$ = 20ns		20		ns
$t_{cyc(min.)}$	Minimum Cycle Time			200		ns

Notes: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
2. Common-mode-input overload recovery time is the time necessary for the device to recover from, the specified common-mode-input overload signal prior to the strobe-enable signal.

DC PARAMETER MEASUREMENT INFORMATION

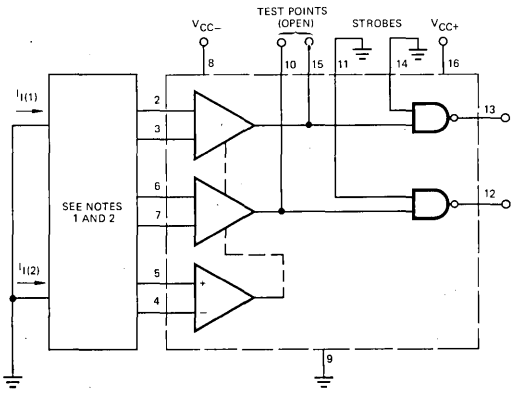


TEST TABLE

INPUTS	V_{ref}	V_{ID}			OUTPUTS		
		Am75238	Am55238	Am55/75239	V_O	I_{OH}	I_{OL}
A1-A2	15mV	≤11mV	≤10mV	≤8mV	≥2.4mV	−400μA	
A1-A2	15mV	≥19mV	≥20mV	≥22mV	≤0.4V		16mA
A1-A2	40mV	≤36mV	≤35mV	≤33mV	≥2.4V	−400μA	
A1-A2	40mV	≥44mV	≥45mV	≥47mV	≤0.4V		16mA

Note 1. Each pair of inputs is tested separately with its corresponding output.

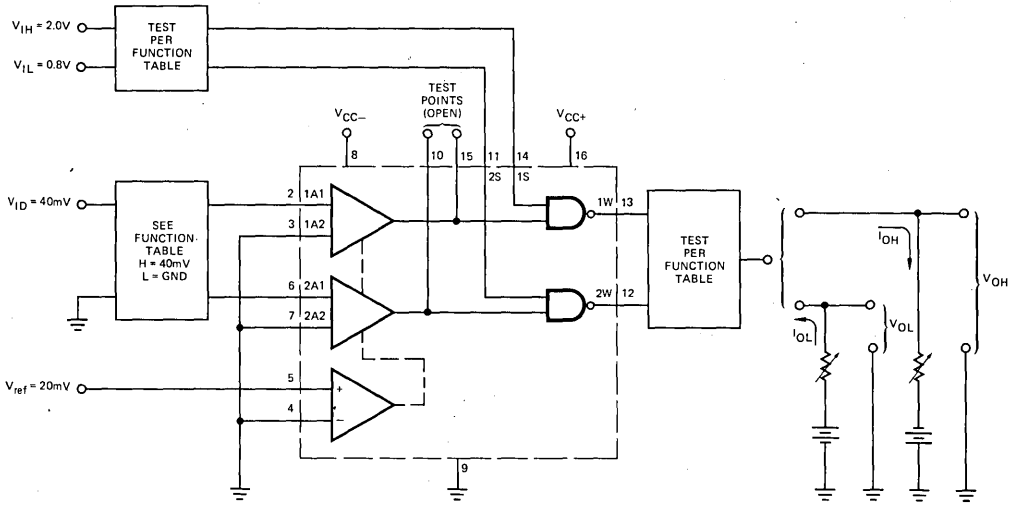
Figure 1. V_T



Notes: 1. Each preamplifier is tested separately. Inputs not under test are grounded.
2. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

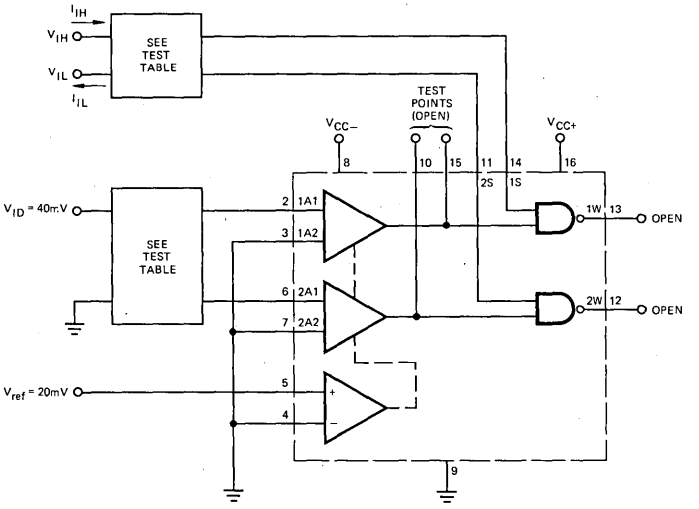
Figure 2. I_{IB} and I_{IO}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)



Note: 1. Arrows indicate actual direction of current flow. Current into terminal is a positive value.

Figure 3. V_{IH}, V_{IL}, V_{OH} and V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} AT STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} AT STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} AT STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} AT STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Figure 4. I_{IH} and I_{IL}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)

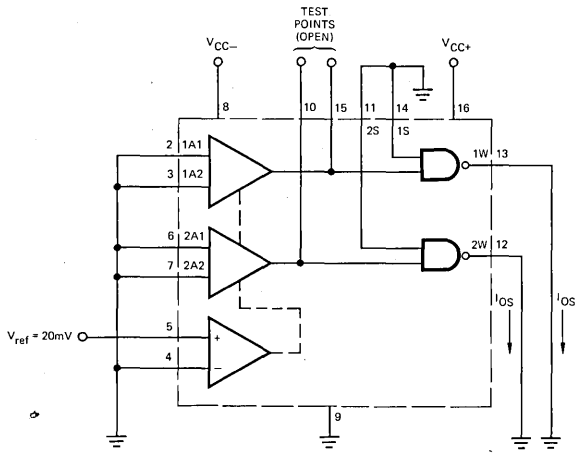


Figure 5. I_{OS}

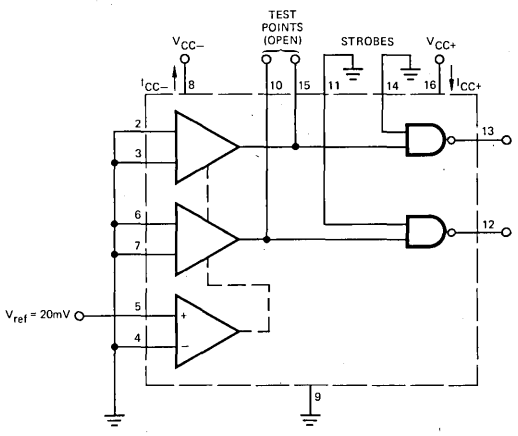


Figure 6. I_{CC+} and I_{CC-}

FUNCTION TABLE

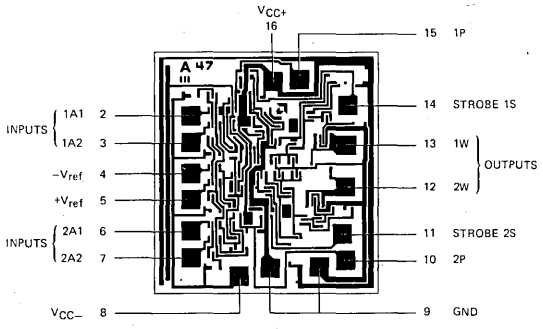
INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

DEFINITION OF ABOVE LOGIC LEVELS

INPUT	H	L	X
A	$V_{ID} \geq V_T$ max.	$V_{ID} \leq V_T$ min.	IRRELEVANT
S	$V_I \geq V_{IH}$ min.	$V_I \leq V_{IL}$ max.	IRRELEVANT

Note: A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

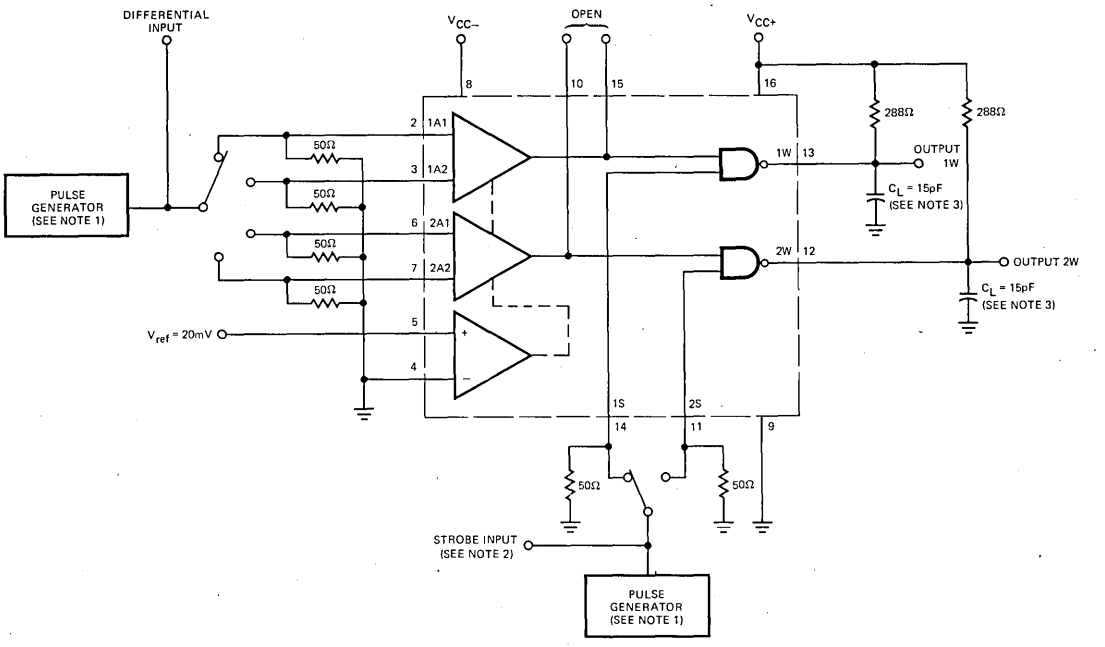
Metallization and Pad Layout



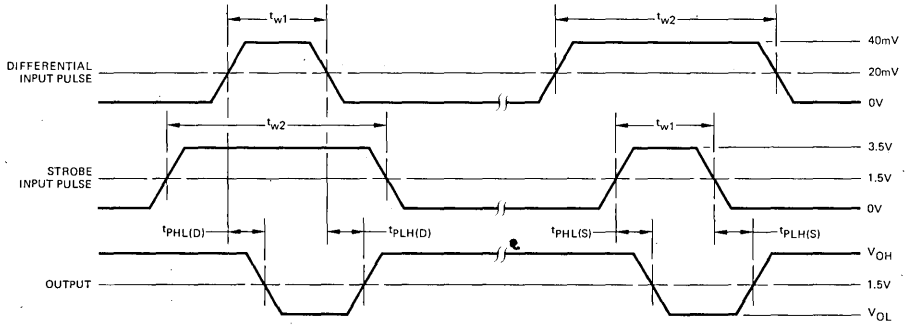
DIE SIZE 0.061" X 0.063"

SWITCHING PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS

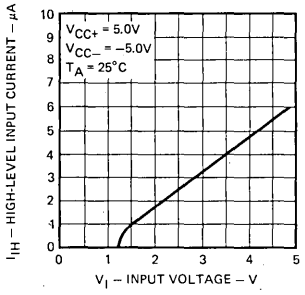


Notes: 1. The pulse generators have the following characteristics: $Z_O = 50\Omega$, $t_r = 15 \pm 5$ns, $t_f = 15 \pm 5$ns, $t_{w1} = 100$ns, $t_{w2} = 300$ns, and PRR = 1 MHz.
2. The strobe input pulse is applied to Strobe 1S when inputs 1A1–1A2 are being tested and to Strobe 2S when inputs 2A1–2A2 are being tested.
3. C_L includes probe and jig capacitance.

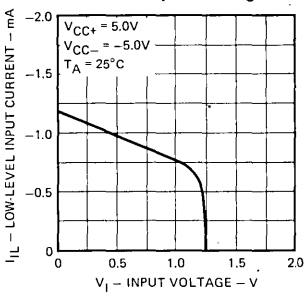
Figure 7. Propagation Delay Times.

TYPICAL CHARACTERISTICS

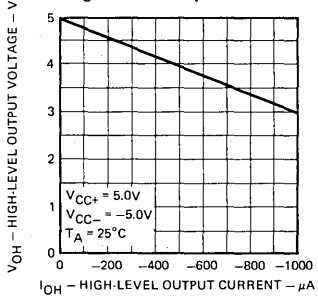
High-Level Input Current Versus Input Voltage



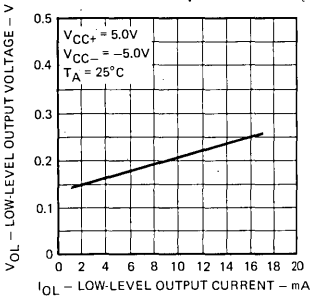
Low-Level Input Current Versus Input Voltage



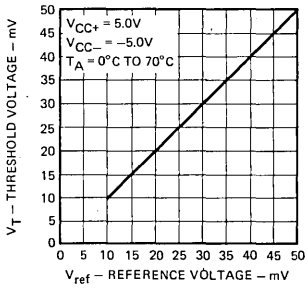
High-Level Output Voltage Versus High-Level Output Current



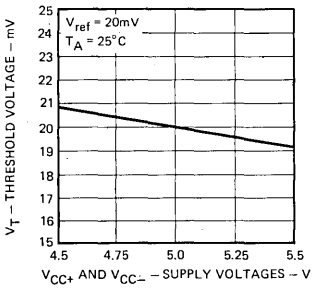
Low-Level Output Voltage Versus Low-Level Output Current



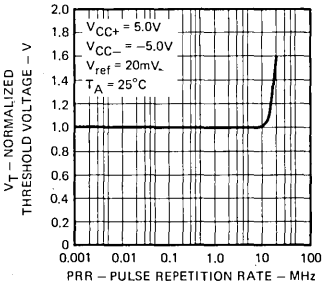
Threshold Voltage Versus Reference Voltage



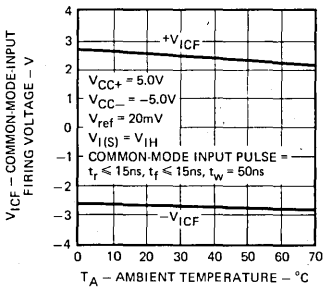
Threshold Voltage Versus Supply Voltage



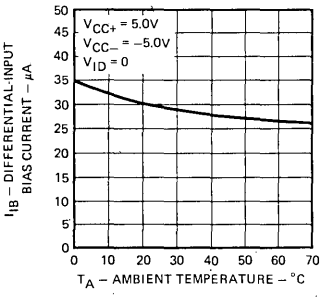
Normalized Threshold Voltage Versus Pulse Repetition Rate



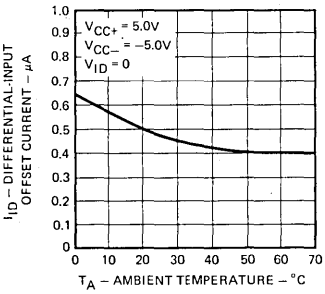
Common-Mode Firing Voltage Versus Ambient Temperature



Differential-Input Bias Current Versus Ambient Temperature

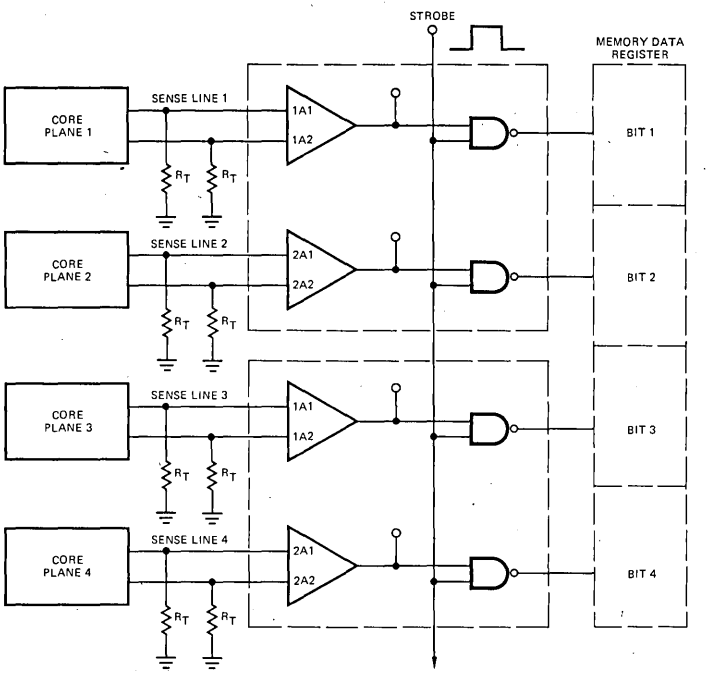


Differential-Input Offset Current Versus Ambient Temperature



5

TYPICAL APPLICATIONS



SMALL MEMORY SYSTEM SENSE LINES

Am55/7524 • Am55/7525

Dual Sense Amplifiers

Distinctive Characteristics

- High speed and fast recovery time
- High DC noise margin
- ±4 mV threshold on Am55/7524
- Good fan-out capability
- ±7 mV threshold on Am55/7525
- Narrow region of threshold voltage uncertainty
- 100% reliability assurance testing in compliance with MIL-STD-883
- Standard logic supply voltage

FUNCITONAL DESCRIPTION

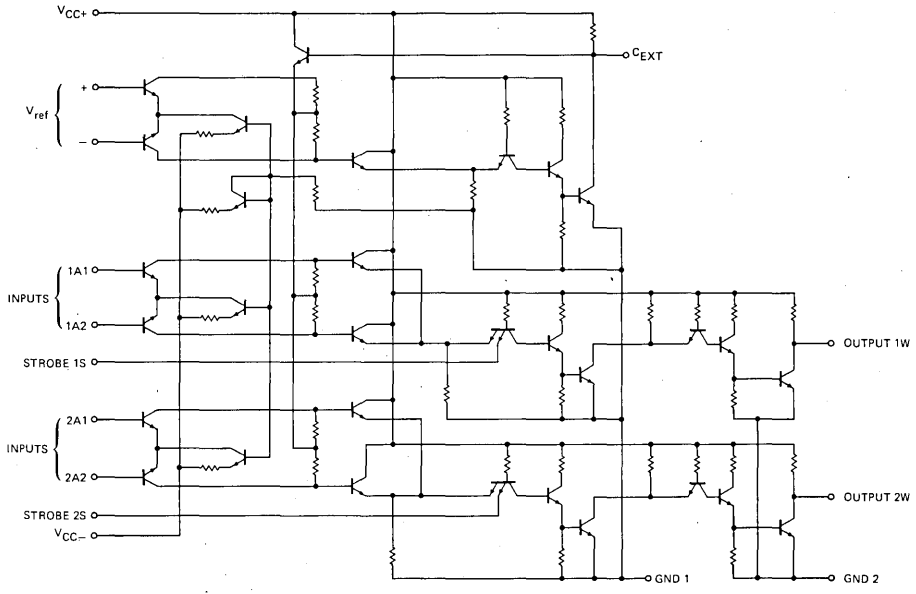
The Am55/7524 and Am55/7525 monolithic sense amplifiers are intended for use in high-speed memory systems. These devices detect bipolar differential-input signals from the memory and provide the required interface with the digital logic.

Each device contains two differential input preamplifiers and an output driver that has a separate strobe input. Both sense amplifiers have non-inverted outputs.

The circuit design provides high stability of the input threshold voltage over a wide range of power supply voltage and temperature variation.

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40mV.

SCHEMATIC DIAGRAM

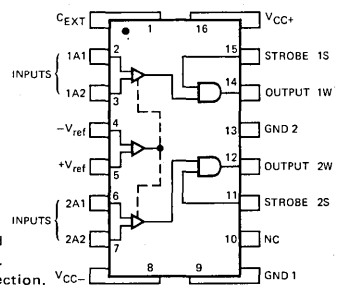


ORDERING INFORMATION

Package Type	Temperature Range	Am55/7524 Order Number	Am55/7525 Order Number
Molded DIP	0°C to +70°C	SN7524N	SN7525N
Hermetic DIP	0°C to +70°C	SN7524J	SN7525J
Dice	0°C to +70°C	AM7524X	AM7525X
Hermetic DIP	−55°C to +125°C	SN5524J	SN5525J
Hermetic Flat Pak	−55°C to +125°C	SN5524W	SN5525W
Dice	−55°C to +125°C	AM5524X	AM5525X

LOGIC SYMBOL AND CONNECTION DIAGRAM

Top View



Notes:
Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature (Ambient) Range	−55°C to +125°C
Supply Voltages V_{CC+}	+7.0V
V_{CC-}	−7.0V
Differential Input Voltage, V_{ID} or V_{ref}	±5.0V
Voltage from any Input to Ground	+5.5V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am7524, Am7525 T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am5524, Am5525 T_A = −55°C to +125°C V_{CC} MIN. = −4.75 V V_{CC} MAX. = −5.25 V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_T	Differential-Input Threshold Voltage (Fig. 1, Note 3)	V_{ref} = 15mV	Am55/7525		8.0	15	22	mV
			Am55/7524	0°C to +70°C	11	15	19	
				−55°C to 0°C	10	15	20	
				+70°C to +125°C				
		V_{ref} = 40mV	Am55/7525		33	40	47	mV
			Am55/7524	0°C to +70°C	36	40	44	
				−55°C to 0°C	35	40	45	
				+70°C to +125°C				
V_{ICF}	Common-Mode Input Firing Voltage (Note 4)	V_{ref} = 40mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse = $t_r \leq 15$ns, $t_f \leq 15$ns, t_W = 50ns				±2.5		Volts
I_{IB}	Differential-Input Bias Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0		0°C to T_A max.		30	75	µA
				−55°C to 0°C			100	
I_{IO}	Differential-Input Offset Current (Fig. 2)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{ID} = 0				0.5		µA
V_{IH}	High-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic HIGH			2.0			Volts
V_{IL}	Low-Level Input Voltage (Strobe Inputs) (Fig. 3)	Guaranteed input logic LOW					0.8	Volts
V_{OH}	High-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OH} = −400µA			2.4	4.0		Volts
V_{OL}	Low-Level Output Voltage (Fig. 3)	V_{CC+} = 4.75V, V_{CC-} = −4.75V, I_{OL} = 16mA				0.25	0.4	Volts
I_{IH}	High-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 2.4V					40	µA
		V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IH} = 5.25V					1.0	mA
I_{IL}	Low-Level Input Current (Strobe Inputs) (Fig. 4)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, V_{IL} = 0.4V				−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current (Fig. 5)	V_{CC+} = 5.25V, V_{CC-} = −5.25V			−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				25	40	mA
I_{CC-}	Supply Current from V_{CC-} (Fig. 6)	V_{CC+} = 5.25V, V_{CC-} = −5.25V, T_A = 25°C				−15	−20	mA

Notes: 1. Electrical characteristics unless otherwise noted V_{CC+} = 5V, V_{CC-} = −5V, T_A = operating temperature range.
2. Typical values are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, 25°C ambient and maximum loading.
3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

Switching Characteristics (V_{CC+} = 5.0V, V_{CC-} = −5.0V, $C_{ext} \geq$ 100pF, T_A = 25°C)

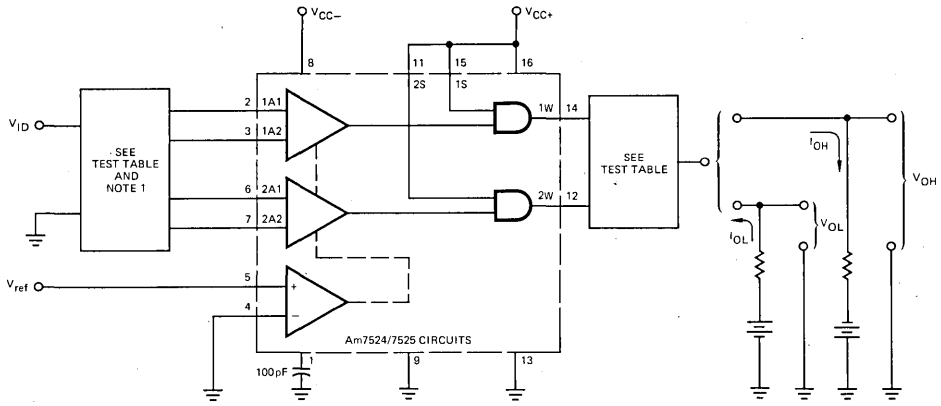
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Times From Input A1-A2 to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		25	40	ns
t_{PHL}				20		
t_{PLH}	Propagation Delay Times From Input Strobe to Output W (Fig. 7)	C_L = 15pF, R_L = 288Ω		15	30	ns
t_{PHL}				20		

Typical Recovery and Cycle Times (V_{CC+} = 5.0V, V_{CC-} = −5.0V, $C_{ext} \geq$ 100pF, T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{or} D	Differential-Input Overload Recovery Time (Note 1)	Differential-Input Pulse V_{ID} = 2.0V, $t_r = t_f$ = 20ns		20		ns
t_{or} C	Common-Mode-Input Overload Recovery Time (Note 2)	Common-Mode Input Pulse V_{IC} = ±2.0V, $t_r = t_f$ = 20ns		20		ns
$t_{cyc(min.)}$	Minimum Cycle Time			200		ns

Notes: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
2. Common-mode-input overload recovery time is the time necessary for the device to recover from, the specified common-mode-input overload signal prior to the strobe-enable signal.

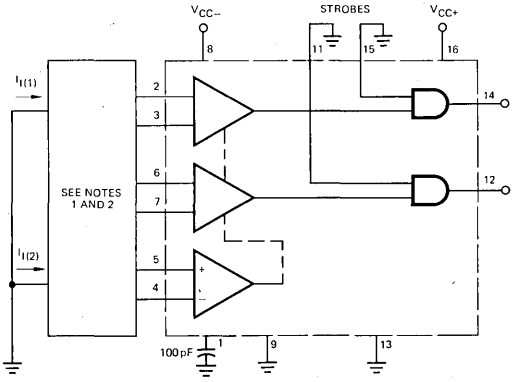
DC PARAMETER MEASUREMENT INFORMATION



INPUTS	V_{ref}	V_{ID}	OUTPUT		
			V_O	I_{OH}	I_{OL}
A1-A2	15mV	≤11mV	≤0.4V		16mA
A1-A2	15mV	≥19mV	≥2.4V	−400μA	
A1-A2	40mV	≤36mV	≤0.4V		16mA
A1-A2	40mV	≥44mV	≥2.4V	−400μA	
A1-A2	15mV	≤ 8mV	≤0.4V		16mA
A1-A2	15mV	≥22mV	≥2.4V	−400μA	
A1-A2	40mV	≤33mV	≤0.4V		16mA
A1-A2	40mV	≥47mV	≥2.4V	−400μA	

Note 1. Each pair of differential inputs is tested separately with its corresponding output.

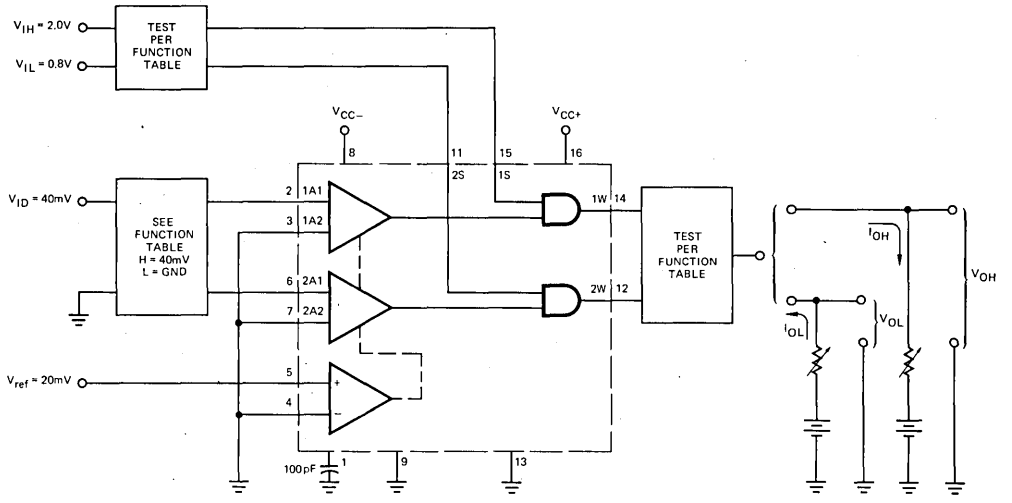
Figure 1. V_T



Notes: 1. Each preamplifier is tested separately. Inputs not under test are grounded.
2. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

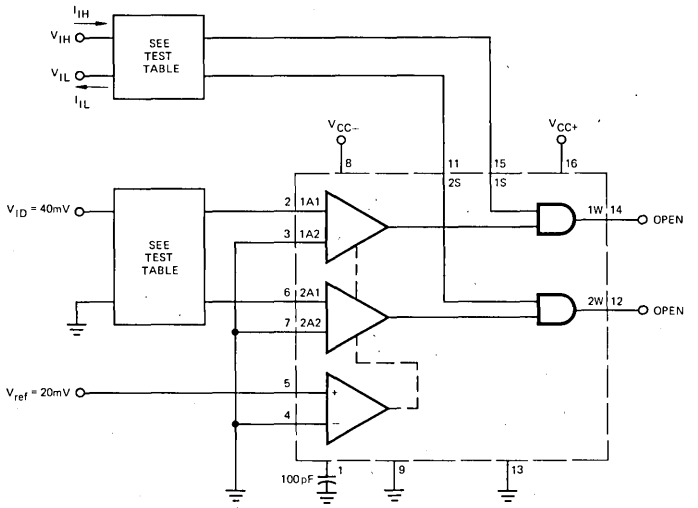
Figure 2. I_{IB} and I_{IO}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)



Note 1. Arrows indicate actual direction of current flow. Current into terminal is a positive value.

Figure 3. V_{IH}, V_{IL}, V_{OH} and V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} AT STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} AT STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} AT STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} AT STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Figure 4. I_{IH} and I_{IL}

DC PARAMETER MEASUREMENT INFORMATION (Cont.)

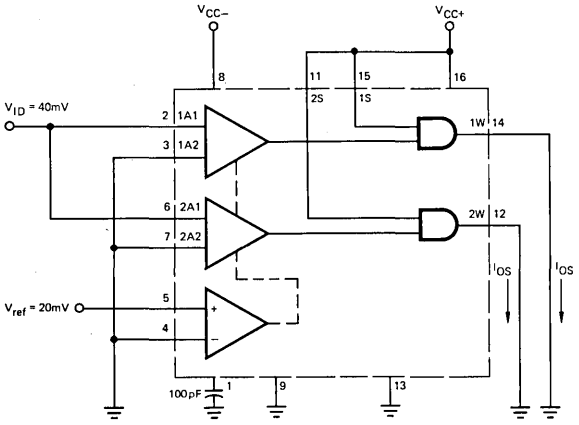


Figure 5. I_{OS}

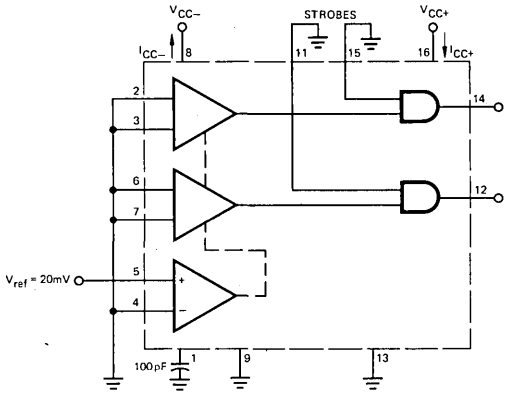


Figure 6. I_{CC+} and I_{CC-}

FUNCTION TABLE

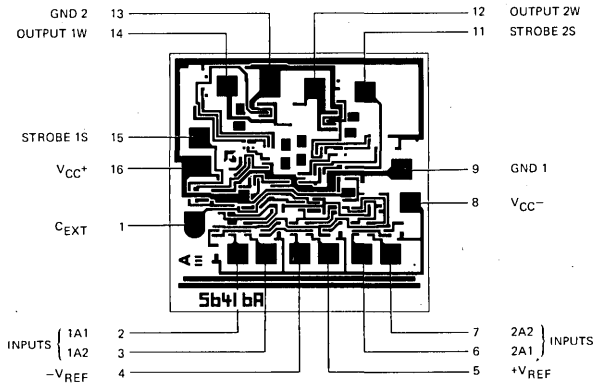
INPUTS A	INPUTS S	OUTPUT W
H	H	H
L	H	L
X	L	L

DEFINITION OF ABOVE LOGIC LEVELS

INPUT	H	L	X
A	$V_{ID} \geq V_T$ max.	$V_{ID} \leq V_T$ min.	IRRELEVANT
S	$V_I \geq V_{IH}$ min.	$V_I \leq V_{IL}$ max.	IRRELEVANT

Note: A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

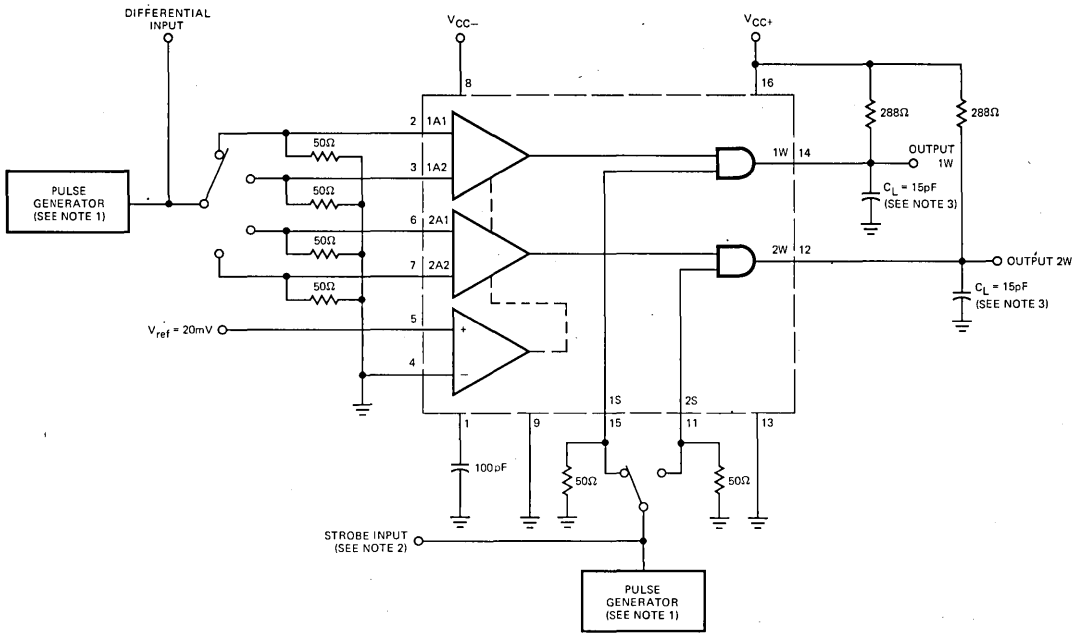
Pad Layout



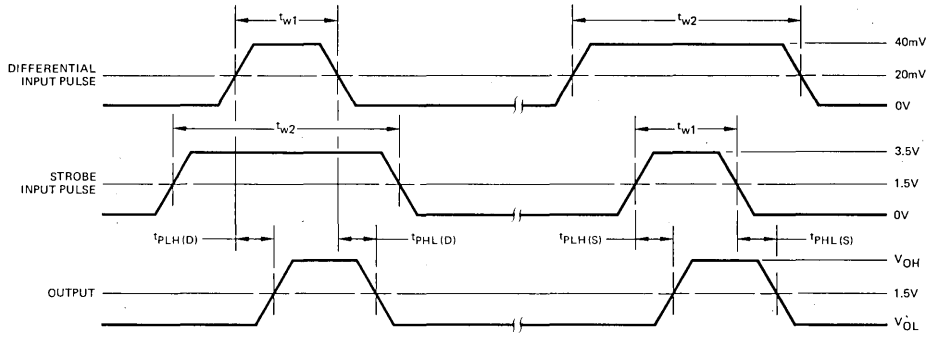
DIE SIZE 0.061" X 0.063"

SWITCHING PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS

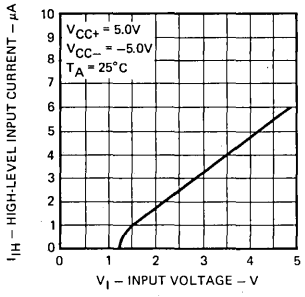


Notes: 1. The pulse generators have the following characteristics: $Z_O = 50\Omega$, $t_r = 15 \pm 5$ns, $t_f = 15 \pm 5$ns, $t_{w1} = 100$ns, $t_{w2} = 300$ns, and PRR = 1 MHz.
2. The strobe input pulse is applied to Strobe 1S when inputs 1A1–1A2 are being tested and to Strobe 2S when inputs 2A1–2A2 are being tested.
3. C_L includes probe and jig capacitance.

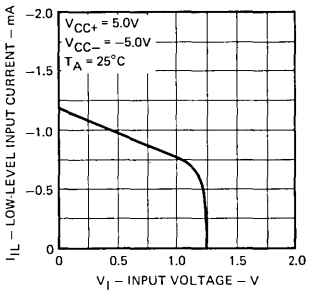
Figure 7. Propagation Delay Times.

TYPICAL CHARACTERISTICS

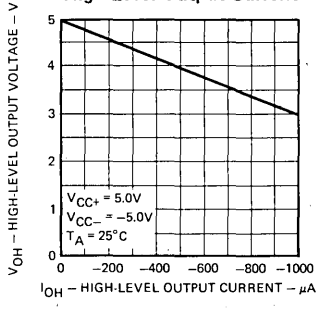
High-Level Input Current Versus Input Voltage



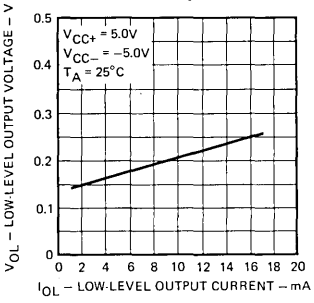
Low-Level Input Current Versus Input Voltage



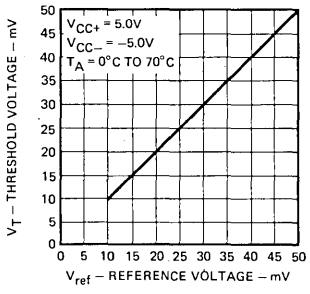
High-Level Output Voltage Versus High-Level Output Current



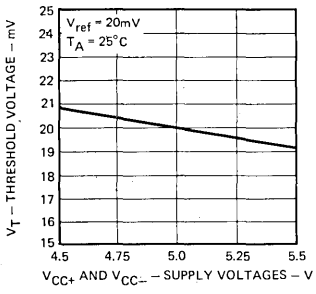
Low-Level Output Voltage Versus Low-Level Output Current



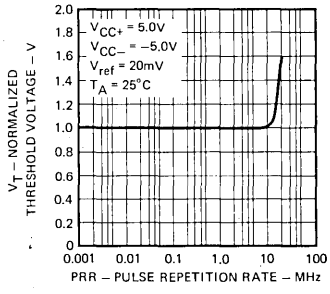
Threshold Voltage Versus Reference Voltage



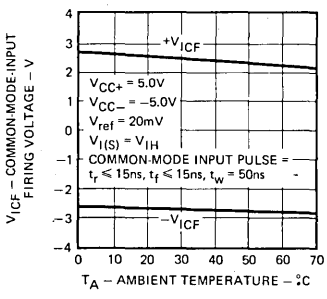
Threshold Voltage Versus Supply Voltage



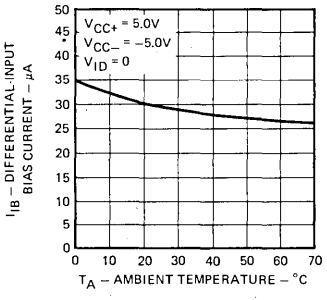
Normalized Threshold Voltage Versus Pulse Repetition Rate



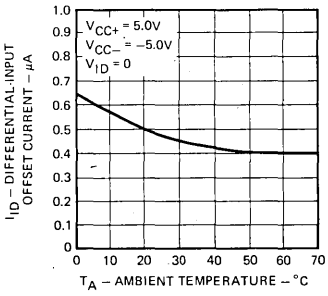
Common-Mode Firing Voltage Versus Ambient Temperature



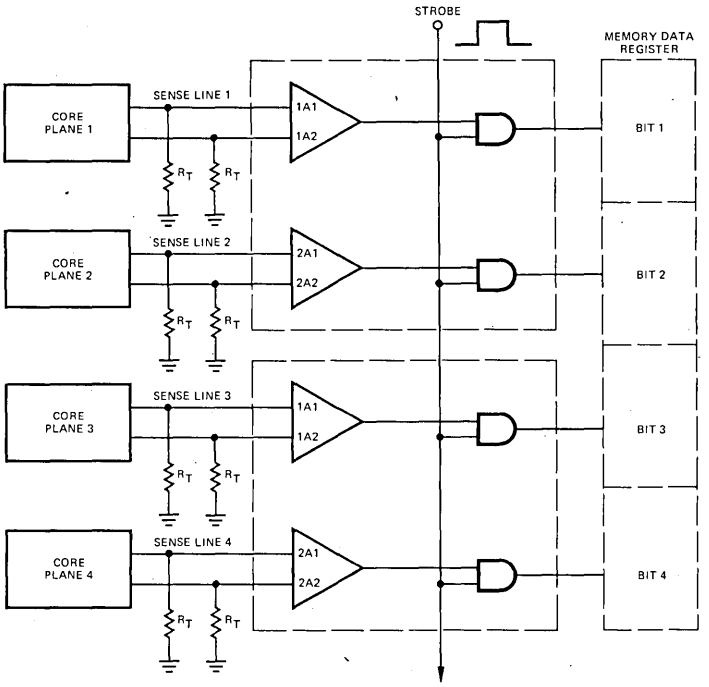
Differential-Input Bias Current Versus Ambient Temperature



Differential-Input Offset Current Versus Ambient Temperature



TYPICAL APPLICATIONS



Am55/75325

Memory Drivers

Distinctive Characteristics

- 600mA output source/sink capability
- Output short circuit protection
- Two source outputs and two sink outputs
- Source strobe input and sink strobe input
- 24 volt output range
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am55/75325 is a high-speed driver for use in magnetic memory systems. The device contains two 600mA NPN source transistor switch pairs and two 600mA NPN sink transistor switch pairs.

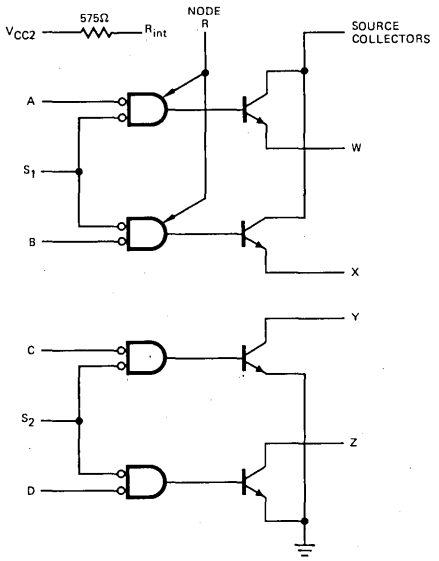
The W source output is enabled when the A input is LOW. The X source output is enabled when the B input is LOW. When the S1 source strobe input goes LOW, the selected source output will turn on. The Y sink output is enabled when the C input is LOW. The Z sink output is enabled when the D input is LOW. When the S2 sink strobe input is LOW, the selected sink output will turn on. Thus, an output can be enabled and turned on with minimum skew time.

When R_{int} and node R are connected together, the base drive for the source output transistors is set by a 575Ω internal resistor. This method provides the required base drive for source currents up to 375mA with V_{CC2} at 15V or 600mA with V_{CC2} at 24V.

When source currents greater than 375mA are used, an external resistor should be connected from V_{CC2} to node R and R_{int} should be left unconnected. This allows the base drive of the source transistors to be regulated within ±5%.

Each output sink transistor has an internal pull-up resistor in parallel with a clamp diode connected to V_{CC2}. This provides protection from voltage surges associated with switching inductive loads.

LOGIC DIAGRAM

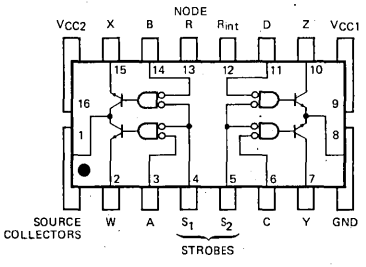


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	SN75325N
Hermetic DIP	0°C to +70°C	SN75325J
Dice	0°C to +70°C	AM75325X
Hermetic DIP	−55°C to +125°C	SN55325J
Hermetic Flat Pak	−55°C to +125°C	SN55325W
Dice	−55°C to +125°C	AM55325X

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential V_{CC1}	0 V to +7.0 V
Supply Voltage to Ground Potential V_{CC2}	0 V to +25 V
DC Input Voltage	−0.5 V to +5.5 V
Continuous Total Dissipation at (or Below) 100°C Case Temperature (Note 1)	1 W

Note: 1. For operation above 100°C case temperature, see derating curves.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am75325 $T_A = 0°C$ to $+70°C$
Am55325 $T_A = -55°C$ to $+125°C$

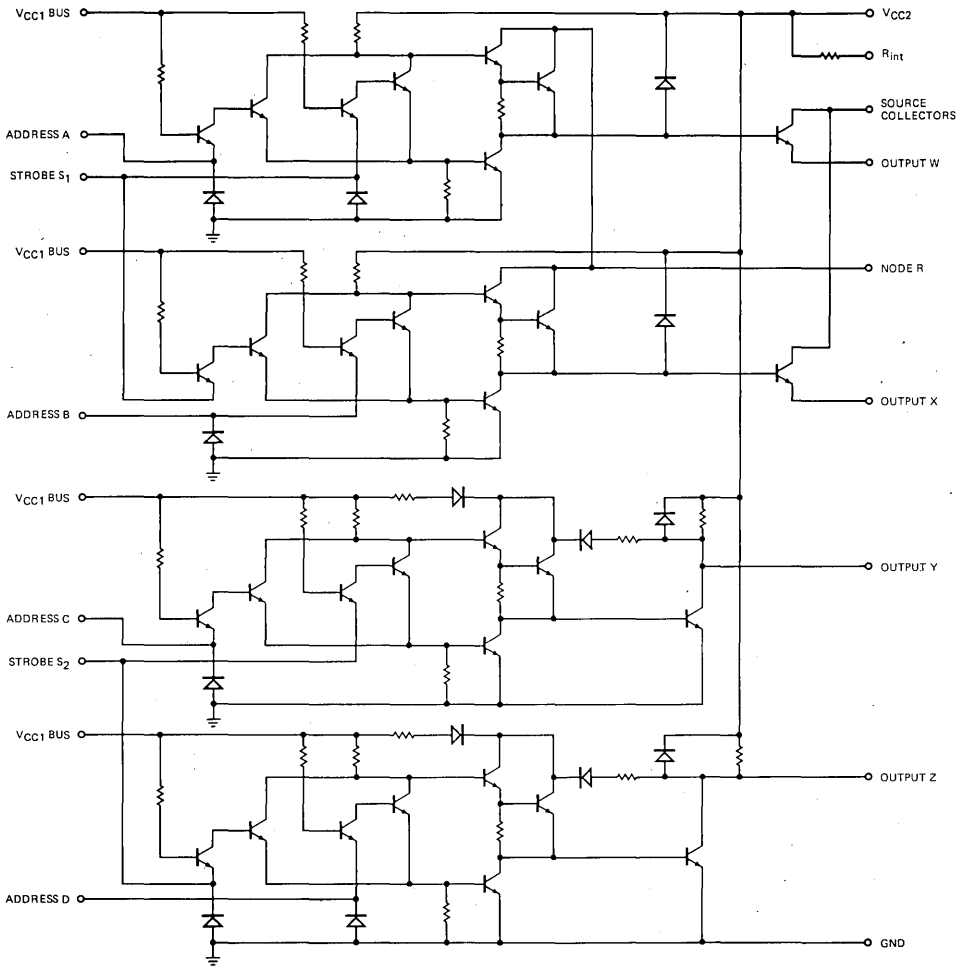
Parameters	Description		Test Figure	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{IH}	High-Level Input Voltage		1 & 2				2.0			Volts
V_{IL}	Low-Level Input Voltage		3 & 4						0.8	Volts
V_I	Input Clamp Voltage		5	V_{CC1} = 4.5V, V_{CC2} = 24V I_I = −10mA, T_A = 25°C				−1.3	−1.7	Volts
$I_{(off)}$	Source-Collector Terminal Off-State Current		1	V_{CC1} = 4.5V V_{CC2} = 24V	Am55, −55°C to +125°C				500	µA
					Am55, T_A = 25°C			3.0	150	
					Am75, 0°C to +70°C				200	
					Am75, T_A = 25°C			3.0	200	
V_{OH}	High-Level Sink Output Voltage		2	V_{CC1} = 4.5V, V_{CC2} = 24V I_O = 0			19	23		Volts
$V_{(sat)}$	Saturation Voltage (Note 2)	Source Outputs	3	V_{CC1} = 4.5V V_{CC2} = 15V R_L = 24Ω $I_{(source)} \approx$ −600mA (Note 4)	Full Range (Note 3)				0.9	Volts
					T_A = 25°C	Am55		0.43	0.7	
						Am75		0.43	0.75	
		Sink Outputs	4	V_{CC1} = 4.5V V_{CC2} = 15V R_L = 24Ω $I_{(sink)} \approx$ 600mA (Note 4)	Full Range (Note 3)				0.9	Volts
					T_A = 25°C	Am55		0.43	0.7	
						Am75		0.43	0.75	
I_I	Input Current at Maximum Input Voltage	Address Inputs	5	V_{CC1} = 5.5V, V_{CC2} = 24V V_{IN} = 5.5V					1.0	mA
		Strobe Inputs							2.0	
I_{IH}	High Level Input Current	Address Inputs	5	V_{CC1} = 5.5V, V_{CC2} = 24V V_{IN} = 2.4V				3.0	40	µA
		Strobe Inputs						6.0	80	
I_{IL}	Low-Level Input Current	Address Inputs	5	V_{CC1} = 5.5V, V_{CC2} = 24V V_{IN} = 0.4V				−1.0	−1.6	mA
		Strobe Inputs						−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	6	V_{CC1} = 5.5V, V_{CC2} = 24V T_A = 25°C				14	22	mA
		From V_{CC2}						7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		7	V_{CC1} = 5.5V, V_{CC2} = 24V $I_{(sink)}$ = 50mA, T_A = 25°C				55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		8	V_{CC1} = 5.5V, V_{CC2} = 24V $I_{(source)}$ = −50mA, T_A = 25°C (Note 4)				32	50	mA

Notes: 1. All typical values are at T_A = 25°C.
2. Not more than one output is to be on at any one time.
3. Full range for Am55325 is −55°C to 125°C and for Am75325 is 0°C to 70°C.
4. These parameters must be measured using pulse techniques. t_w = 200µs, duty cycle ≤ 2%.

Switching Characteristics (V_{CC1} = 5V, T_A = 25°C)

Parameters	To (Output)	Test Figure	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Source Collectors	9	V_{CC2} = 15V, R_L = 24Ω C_L = 25pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source Outputs	10	V_{CC2} = 20V, R_L = 1kΩ C_L = 25pF		7.0		ns
t_{THL}					55		
t_{PLH}	Sink Outputs	9	V_{CC2} = 15V, R_L = 24Ω C_L = 25pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink Outputs	9	V_{CC2} = 15V, R_L = 24Ω C_L = 25pF		7.0	15	ns
t_{THL}					9.0	20	
t_s	Sink Outputs	9	V_{CC2} = 15V, R_L = 24Ω C_L = 25pF		15	30	ns

SCHEMATIC DIAGRAM



FUNCTION TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = HIGH
L = LOW
X = Don't Care

Note: Not more than one output is to be on at any one time.

DEFINITION OF FUNCTIONAL TERMS

A The enable input for the W source output. When the A input is LOW, the W output is enabled.

B The enable input for the X source output. When the B input is LOW, the X output is enabled.

C The enable input for the Y sink output. When the C input is LOW, the Y output is enabled.

D The enable input for the Z sink output. When the D input is LOW, the Z output is enabled.

S1 The strobe input for the source drivers. When the S1 input is LOW, the enabled source driver is on.

S2 The strobe input for the sink drivers. When the S2 input is LOW, the enabled sink driver is on.

W, X The two source driver outputs.

Y, Z The two sink driver outputs.

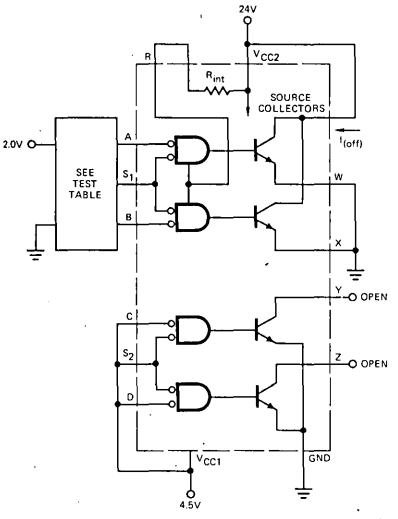
Source Collectors The common node of the driver transistors of the source outputs.

R_{int} The node for a 575Ω internal resistor. The other terminal of the resistor is connected internally to V_{CC2}.

R The base drive node of the output source transistor drivers.

DC PARAMETER MEASUREMENT INFORMATION

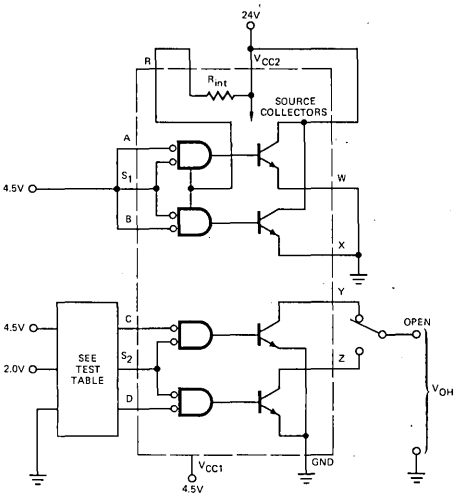
DC TEST CIRCUITS



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

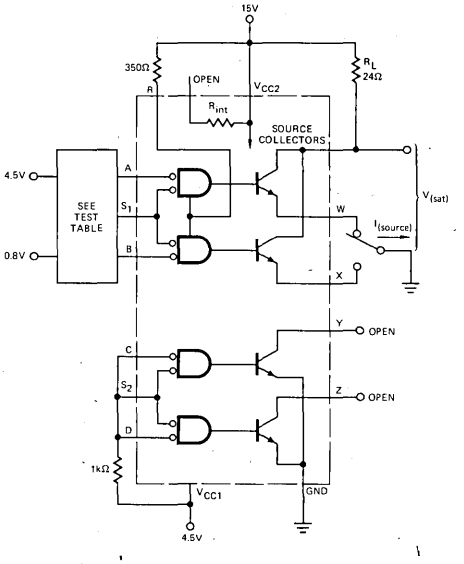
Figure 1. V_{IH} and $I_{(Off)}$



TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

Figure 2. V_{IH} and V_{OH}

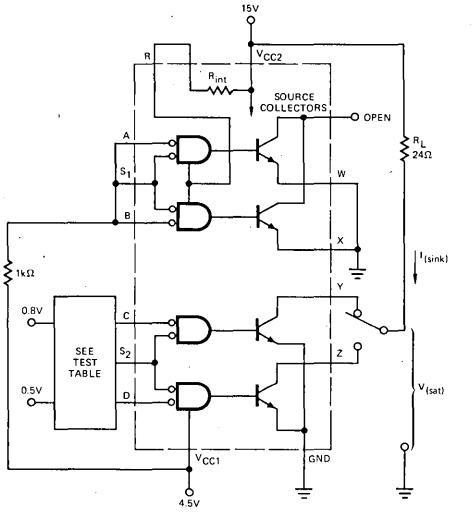


Note:
These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ⩽ 2%.

TEST TABLE

A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

Figure 3. V_{IL} and Source $V_{(sat)}$



Note:
These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ⩽ 2%.

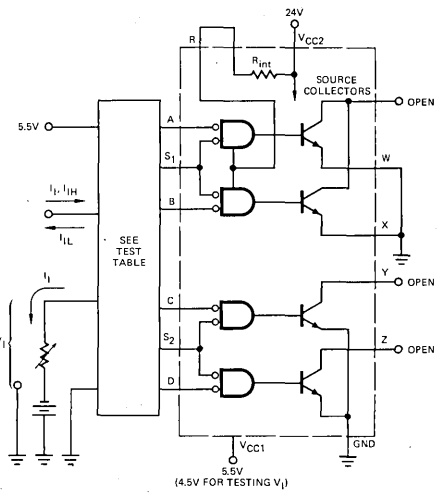
TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

Figure 4. V_{IL} and Sink $V_{(sat)}$

DC PARAMETER MEASUREMENT INFORMATION (Cont.)

DC TEST CIRCUITS



I_I, I_{IH}

Apply V_I = 5.5V, Measure I_I / Apply V_I = 2.4V, Measure I_{IH}	Ground	Apply 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

Apply V_I = 0.4V Measure I_{IL} / Apply I_I = −10mA Measure V_I	Apply 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

Figure 5. V_I, I_I, I_{IH}, and I_{IL}

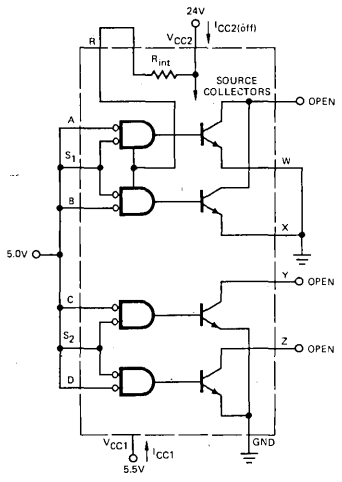
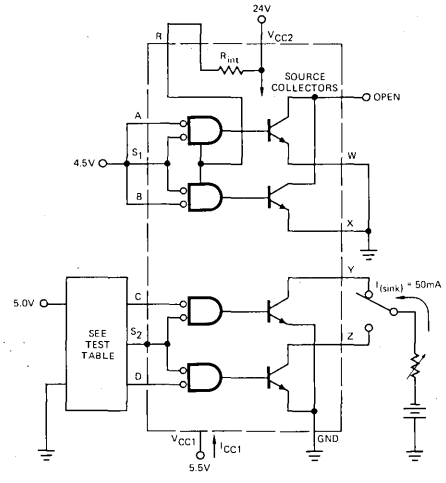


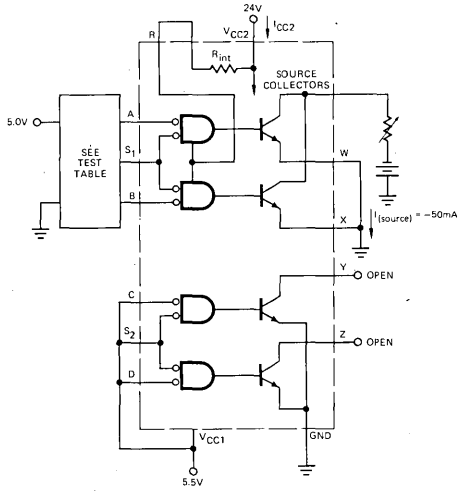
Figure 6. $I_{CC1(off)}$ and $I_{CC2(off)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(sink)}$	OPEN
5V	GND	GND	OPEN	$I_{(sink)}$

Figure 7. I_{CC1}, Either Sink On



TEST TABLE

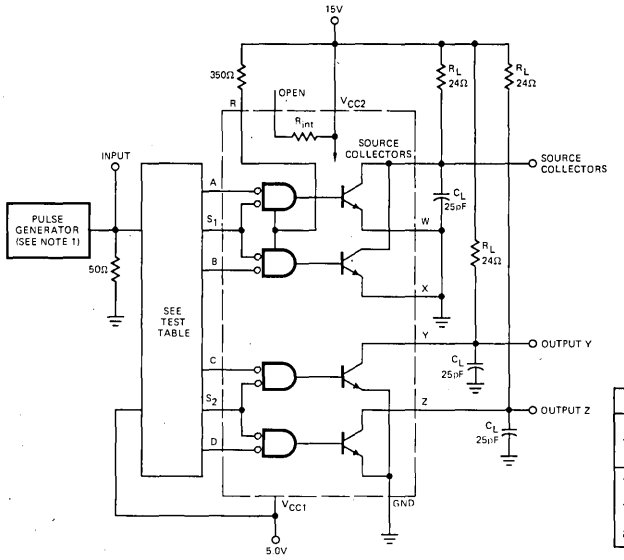
A	B	S1
GND	5V	GND
5V	GND	GND

Figure 8. I_{CC2}, Either Source On

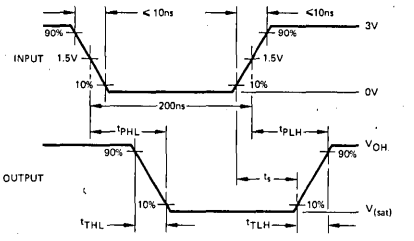
AC PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS

TEST CIRCUIT



VOLTAGE WAVEFORMS



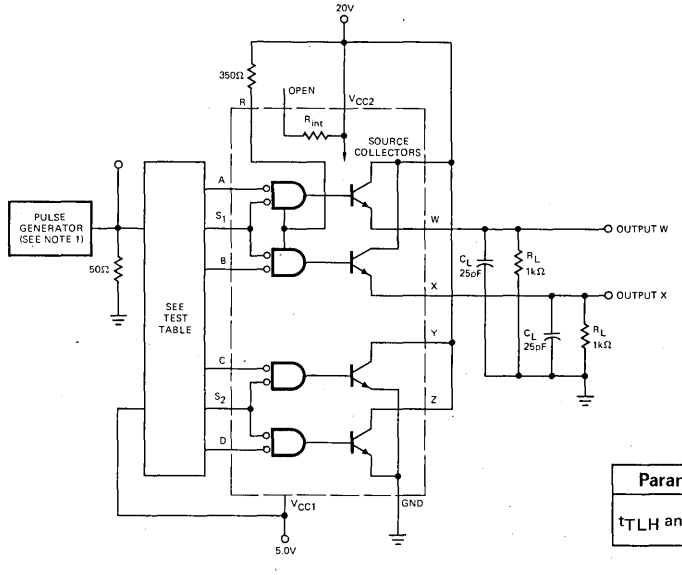
TEST TABLE

Parameter	Output Under Test	Input	Connect to 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

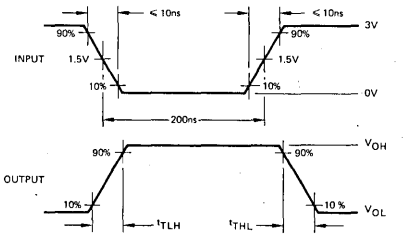
Notes: 1. The pulse generator has the following characteristics: Z_{out} = 50Ω, duty cycle ≤ 1%
2. C_L includes probe and jig capacitance.

Figure 9. Switching Times

TEST CIRCUIT



VOLTAGE WAVEFORMS



TEST TABLE

Parameter	Output Under Test	Input	Connect to 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

Notes: 1. The pulse generator has the following characteristics: Z_{out} = 50Ω, duty cycle ≤ 1%.
2. C_L includes probe and jig capacitance.

Figure 10. Transition Times of Source Outputs

TYPICAL CHARACTERISTICS

Off-State Current Into Source Collectors Versus Ambient Temperature

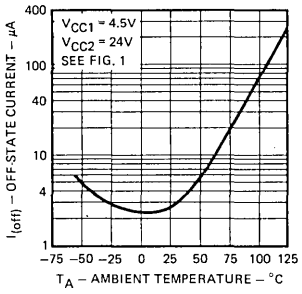


Figure 11

High-Level Sink Output Voltage Versus Ambient Temperature

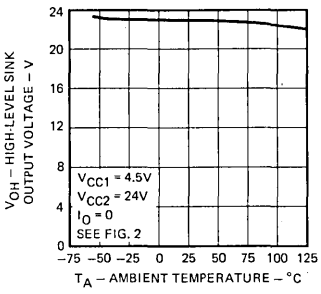


Figure 12

Source or Sink Saturation Voltage Versus Source Current or Sink Current

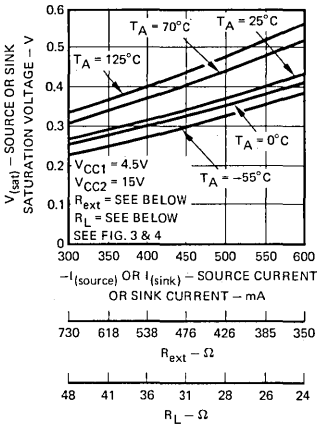


Figure 13

Source or Sink Saturation Voltage Versus Ambient Temperature

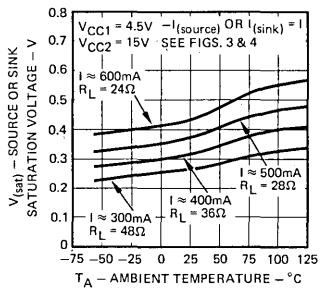


Figure 14

Supply Current, All Sources and Sinks Off Versus Ambient Temperature

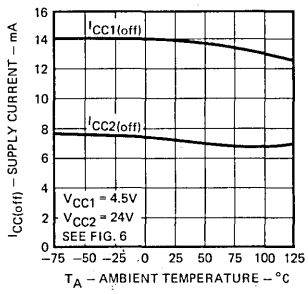
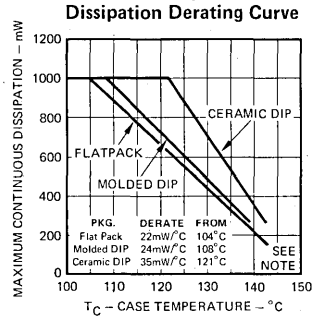


Figure 15

Case Temperature Dissipation Derating Curve



Note: Rated operating ambient temperature ranges must be observed regardless of heat-sinking.

Figure 16

Ambient Temperature Dissipation Derating Curve

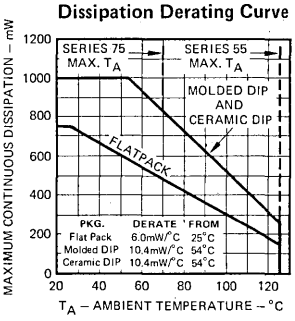


Figure 17

APPLICATIONS

External Resistor Calculation

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined as:

$$R_{ext} = \frac{16\,[V_{CC2(min.)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min.)} - V_S - 2.9]}$$

where R_{ext} is in kΩ,

$V_{CC2(min.)}$ is the lowest expected value of V_{CC2} in volts,

V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated as:

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min.)} - V_S - 2]$$

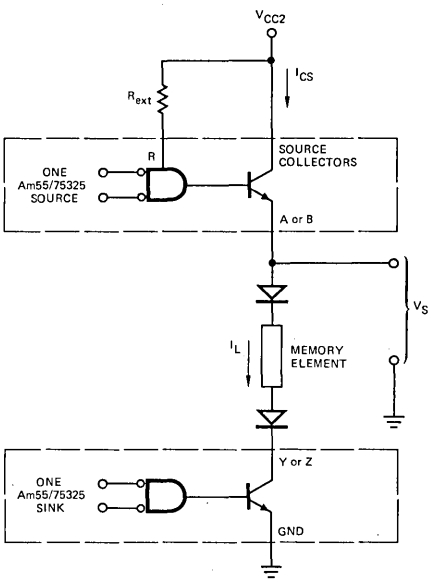
where P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from:

$$I_{CS} \approx 0.94\, I_L$$

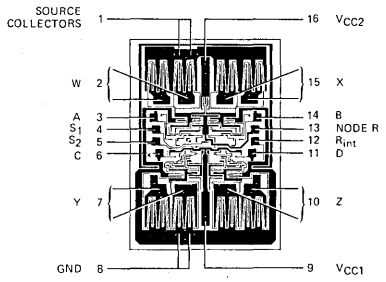
where I_{CS} is in mA.

The regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate and I_{CS} comprise I_L.



Notes: 1. For clarity, partial logic diagrams of two Am75325's are shown.
2. Source and sink shown are in different packages.

Metallization and Pad Layout



DIZE SIZE 0.077" X 0.112"

MOS Memory and Microprocessor Interface – Section VI

Am0026/Am0026C

5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20 ns rise and fall times with 1000 pF load
- 20 V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10 MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883

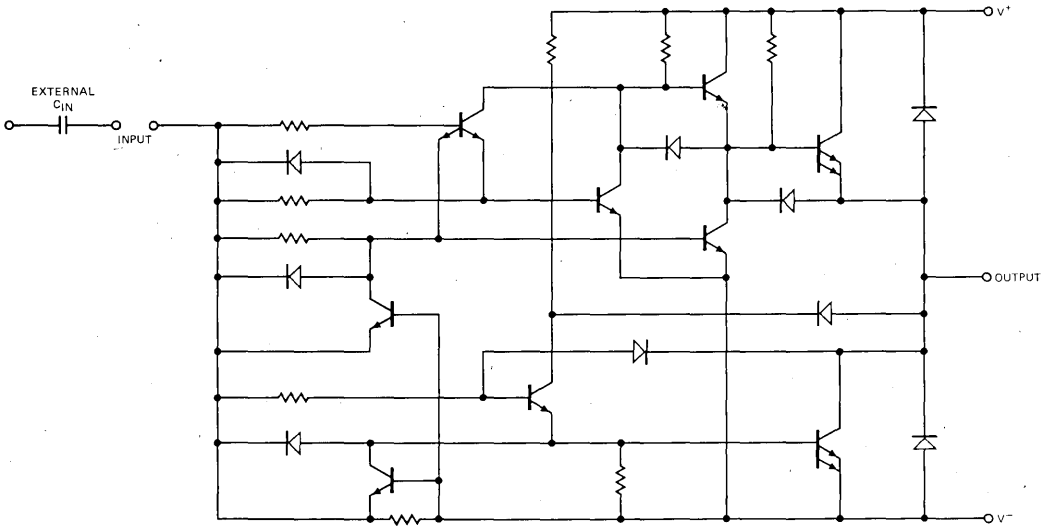
FUNCTIONAL DESCRIPTION

The Am0026 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0026 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in an 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a 14-pin ceramic package.

SCHEMATIC DIAGRAM
(One Driver Shown)

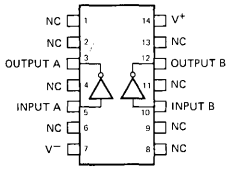


ORDERING INFORMATION

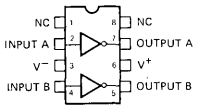
Package Type	Temperature Range	Order Number
TO-99	0°C to 70°C	MH0026CH
Mini-DIP	0°C to 70°C	MH0026CN
TO-8	0°C to 70°C	MH0026CG
Ceramic DIP	0°C to 70°C	MMH0026CL
Dice	0°C to 70°C	AM0026XC
TO-99	−55°C to +125°C	MH0026H
TO-8	−55°C to +125°C	MH0026G
Ceramic DIP	−55°C to +125°C	MMH0026L
Dice	−55°C to +125°C	AM0026XM

CONNECTION DIAGRAMS
Top Views

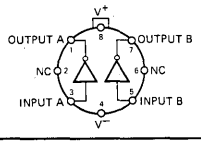
Ceramic DIP



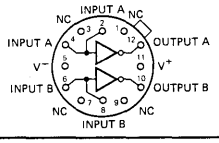
Mini DIP



TO-99



TO-8



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22 V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5 V
Peak Output Current	1.5 A
Power Dissipation	See curves

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am0026C T_A = 0°C to 85°C (COM Range) $V^+ - V^-$ = 10 V to 20 V
Am0026 T_A = −55°C to +125°C (MIL Range) Unless Otherwise Specified

Parameter	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Logical "0")	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −11.6 V	4.0	4.3		Volts
		$V_{IN} - V^-$ = 0.4 V	V^+ −1.0	V^+ −0.7		
V_{OL}	Output LOW Voltage (Logical "1")	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −9.5 V		−11.5	−11.0	Volts
		$V_{IN} - V^-$ = 2.5 V		V^- +0.5	V^- +1.0	
V_{IH}	Input HIGH Level	$V_{OUT} = V^-$ +1.0 V	2.5	1.5		Volts
V_{IL}	Input LOW Level	$V_{OUT} = V^+$ −1.0 V		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^-$ = 0 V, $V_{OUT} = V^+$ −1.0 V		−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^-$ = 2.5 V, $V_{OUT} = V^-$ +1.0 V		10	15	mA
$I_{CC\,ON}$	"ON" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 2.5 V		30	40	mA
$I_{CC\,OFF}$	"OFF" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 0.0 V	COM'L	10	100	μA
			MIL	50	500	

Notes: 1. These specifications apply for $V^+ - V^-$ = 10 V to 20 V, C_L = 1000 pF, over the temperature range −55°C to +125°C for the Am0026 and 0°C to +85°C for the Am0026C.
2. All typical values for T_A = 25°C.

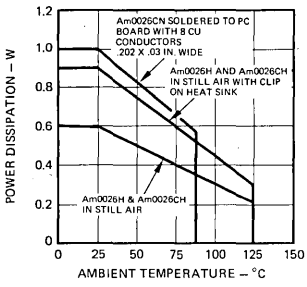
Switching Characteristics (Notes 1 and 2 Above)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Turn On Delay		5.0	7.5	12	ns
t_{PLH}	Turn Off Delay		5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		12		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		15	18	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		10		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		12	16	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		17	25	

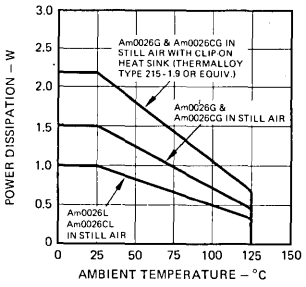
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CHARACTERISTICS

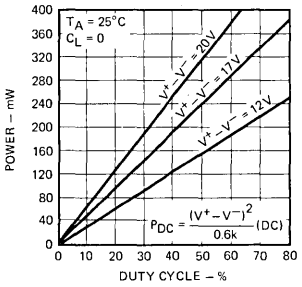
Power Ratings TO-5 & 8-Pin DIP



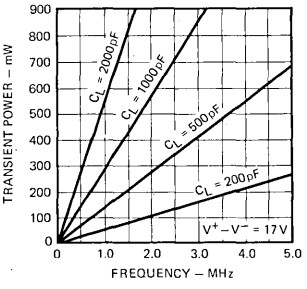
Power Rating TO-8 & 14-Pin DIP



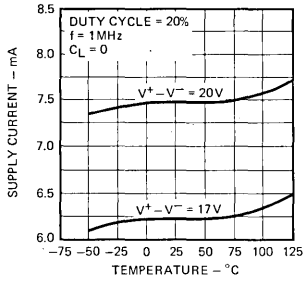
DC Power (P_{DC}) Versus Duty Cycle



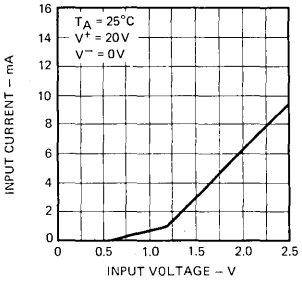
Transient Power (P_{AC}) Versus Frequency



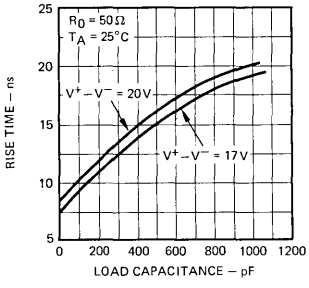
Supply Current Versus Temperature



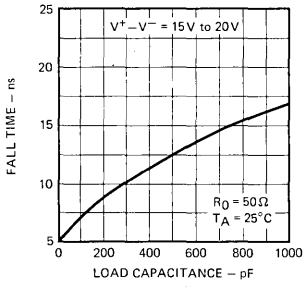
Input Current Versus Input Voltage



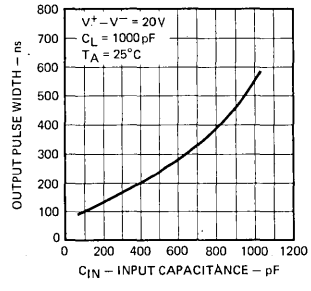
Rise Time Versus Load Capacitance



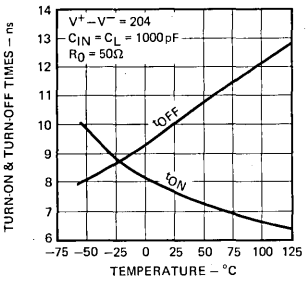
Fall Time Versus Load Capacitance



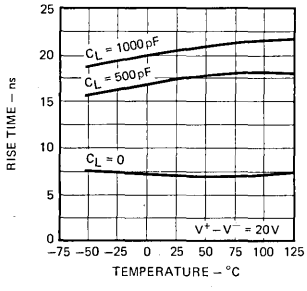
Optimum Input Capacitance Versus Output Pulse Width



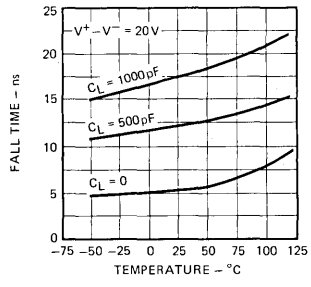
Turn-On & Turn-Off Time Versus Temperature



Rise Time Versus Temperature

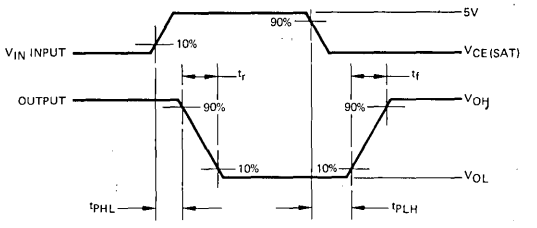


Fall Time Versus Temperature

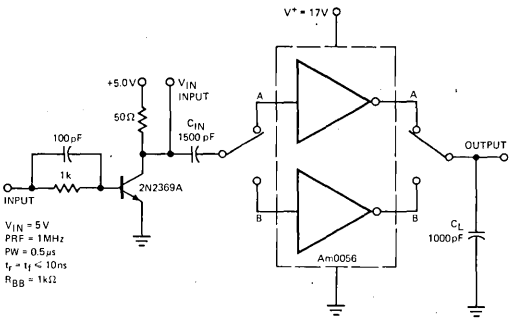


6

SWITCHING TIME WAVEFORMS



AC TEST CIRCUIT



APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0026 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leqslant P_{MAX.}$$

With the device dissipating only 2 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per driver:

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S\,(LOW)} \times \text{Duty Cycle}$$

where $I_{S\,(LOW)}$ is $I_{SUPPLY\,(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY\,(ON)} \text{ is } 40\,\text{mA} \times \frac{(V^+ - V^-)}{20\,\text{V}} \text{ worst case}$$

$$\text{or } 30\,\text{mA} \times \frac{(V^+ - V^-)}{20\,\text{V}} \text{ typically}$$

AC transient power per driver:

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-5 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

$$C_L\,(\text{max.}) = \frac{10^3}{n} \frac{(P_{max.}\ \text{Req} - 10^3 n\,(V^+ - V^-)^2\ \text{Duty Cycle})}{\text{Req}\,(V^+ - V^-)^2 \times f}$$

where n is the number of drivers used in the package.

$P_{max.}$ is the package power rating in milliwatts for given package, heat sink, and maximum ambient temperature.

Req is the equivalent resistance $(V^+ - V^-)/I_{S\,(LOW)} = 500\,\Omega$ (worst case over temperature or 600 Ω (typically).

Duty cycle is the fraction of the time that the output signal is in the LOW state.

f is the input signal frequency in MHz.

$C_{L\,(max.)}$ is the maximum load capacitance per driver in picofarads which can be driven without exceeding device power limits.

When used as a non-overlapping two phase driver with each side operating at the same frequency and duty cycle, and with $(V^+ - V^-) = 17\,\text{V}$, the above equation simplifies to

$$C_L = \frac{10^3}{f}\left[\frac{P_{max.}}{578} - \text{Duty Cycle}\right]$$

Table I gives maximum drive capability for various system conditions using the above equation.

PULSE WIDTH CONTROL

The Am0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} \simeq (PW)_{IN} + t_f = PW_{IN} + 25\,\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0026 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\,\text{pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0026's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5\ A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)\ \ (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20\,V$, $C_L = 1000\,pF$, t_r is:

$$t_r \cong (20\ V)\ \ (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\ ns$$

For small values of C_L, the equation above predicts optimistic values for t_r. The graph in the performance curves shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2\ R\left(C_S + \frac{C_L}{h_{FE}+1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0026. The critical valve for $R_S = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_r \cong 2.2 R_S\ C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least $2\,V_{BE}$ before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2 k and 10 kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

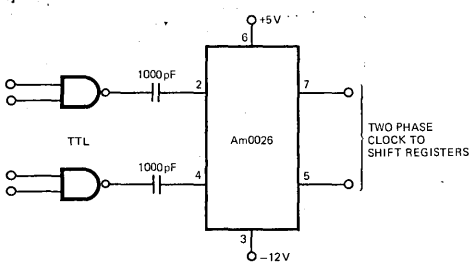
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0026*

Package Type		TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle \ Max. Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100 kHz	5%	30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500 kHz	10%	6.5k	5.1k	4.1k	3.2k	2.5k	1.9k	1.4k	1.1k	2k
1 MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2 MHz	25%	1.4k	1.1k	850	650	540	400	280	190	390
5 MHz	25%	620	470	380	290	220	160	110	75	165
10 MHz	25%	280	220	170	130	110	79	55	37	90

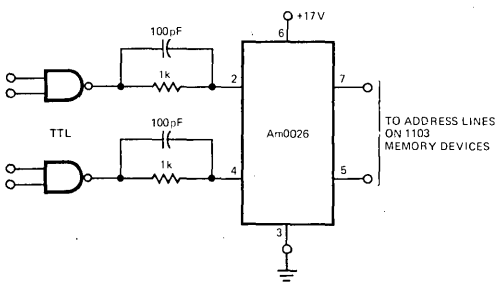
*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\,V$.

TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver

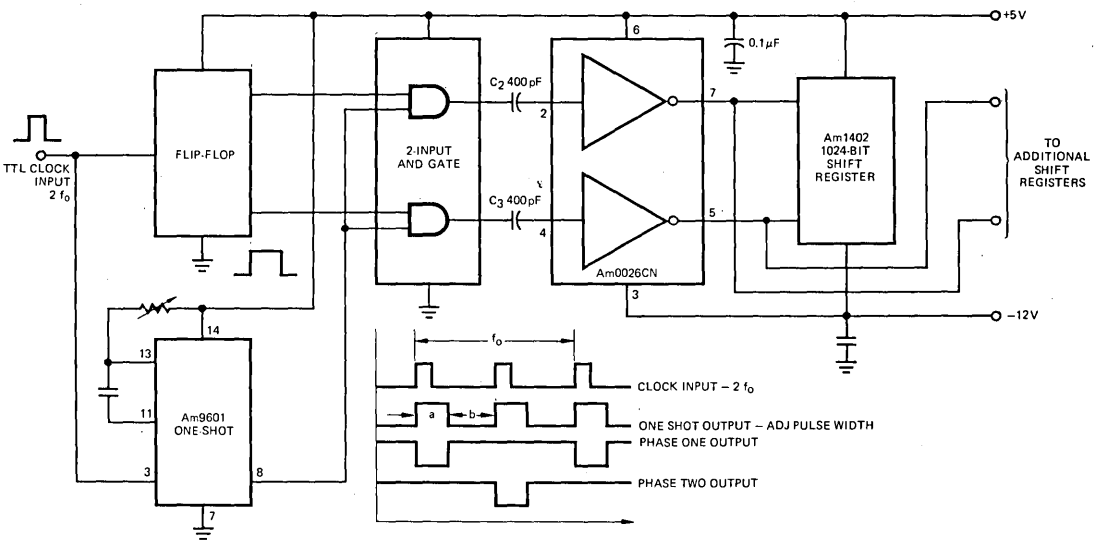


DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

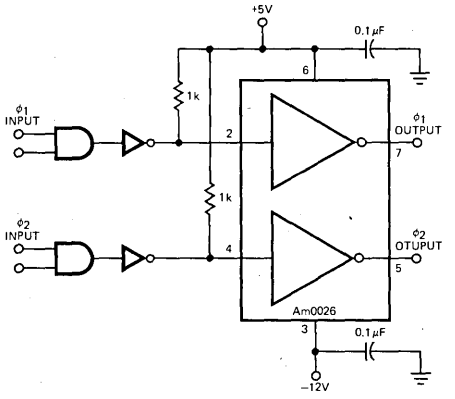


TYPICAL APPLICATIONS (Cont.)

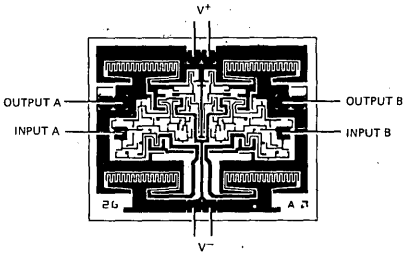
Logically Controlled AC Coupled Clock Driver



DC Coupled MOS Clock Driver



Metallization and Pad Layout



DIE SIZE 0.063" X 0.078"

Am0056•Am0056C

5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20ns rise and fall times with 1000pF load
- 20V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883
- Improved V_{OH} compared with Am0026

FUNCTIONAL DESCRIPTION

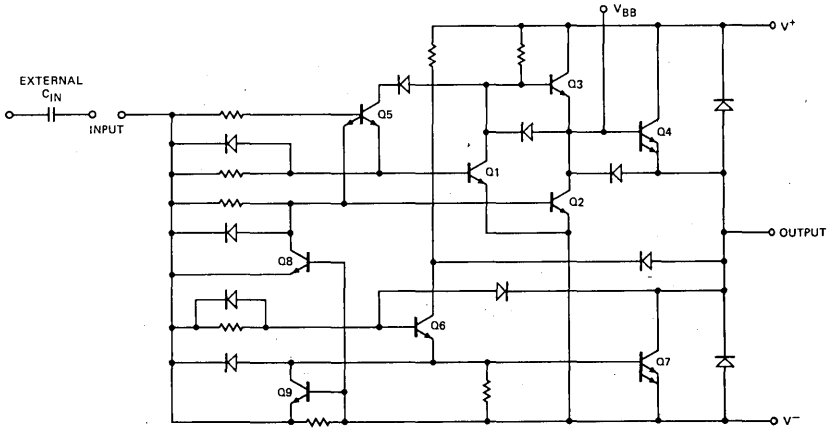
The Am0056 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0056 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in a TO-99, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a ceramic DIP.

The V_{BB} terminal is intended to be connected through a series resistor to a supply higher than V^+. This connection will enable the output to pull-up to V^+–0.1V. Under no conditions should the V_{BB} terminal be connected directly to a positive supply as the device will be damaged when the driver switches LOW.

SCHEMATIC DIAGRAM (One Driver Shown)



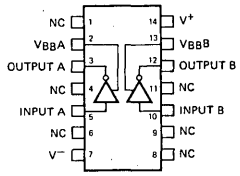
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
TO-99	0°C to 70°C	DS0056CH
Mini-DIP	0°C to 70°C	DS0056CN
TO-8	0°C to 70°C	DS0056CG
Ceramic DIP	0°C to 70°C	DS0056CJ
Dice	0°C to 70°C	AM0056XC
TO-99	–55°C to +125°C	DS0056H
TO-8	–55°C to +125°C	DS0056G
Ceramic DIP	–55°C to +125°C	DS0056J
Dice	–55°C to +125°C	AM0056XM

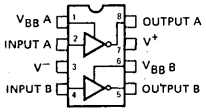
CONNECTION DIAGRAMS

Top Views

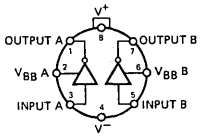
Ceramic DIP



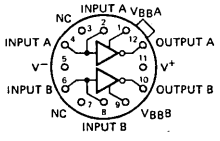
Mini DIP



TO-99



TO-8



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22V
Input Current	100mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Power Dissipation	See curves
V_{BB} Voltage	V^+ +5.0V
Current Into V_{BB}	50mA
Operating Temperature—Am0056	−55°C to +125°C
Am0056C	0°C to 70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Logical "0" Output Voltage)	$V_{IN} - V^- = 0.4V$, V_{BB} Open Circuit ($R_{BB} = \infty$)	$V^+ - 2.5$	$V^+ - 1.4$		Volts
		$V_{IN} - V^- = 0.4V$, $R_{BB} = 1k\Omega$; V_{BB} $V_B \geq V^+ + 1.0V$	$V^+ - 0.3$	$V^+ - 0.1$		
V_{OL}	Output LOW Voltage (Logical "1" Output Voltage)	$V_{IN} - V^- = 2.4V$		$V^- + 0.7$	$V^- + 1.0$	Volts
V_{IH}	Input HIGH Level	$V_{OUT} = V^- + 1.0V$	2.0	1.5		Volts
V_{IL}	Input LOW Level	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^- = 2.4V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
$I_{CC\,ON}$	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$		15	30	mA
$I_{CC\,OFF}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$ COM'L		10	100	μA
		MIL		50	500	
I_{BB}	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_{BB} = V^+ + 3.0V$, $R_{BB} = 1k\Omega$		22		mA

Notes: 1. These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000pF$, over the temperature range −55°C to +125°C for the Am0056 and 0°C to +70°C for the Am0056C.
2. All typical values for $T_A = 25°C$.

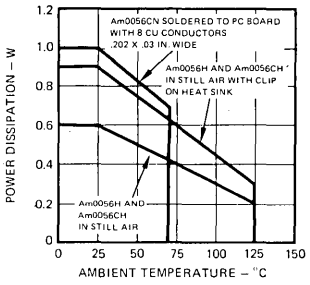
SWITCHING CHARACTERISTICS (Notes 1 and 2 Above)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
t_{PHL}	Turn ON Delay			5.0	8.0	12	ns
t_{PLH}	Turn OFF Delay			5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		15	18	ns
			$C_L = 1000pF$		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		12	16	ns
			$C_L = 1000pF$		17	25	

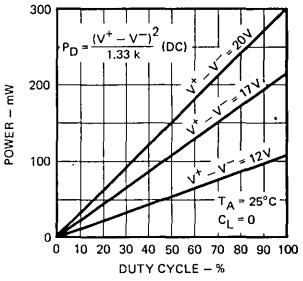
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CURVES

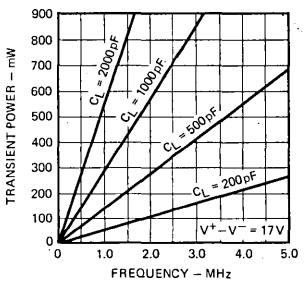
Power Ratings TO-5 & 8-Pin DIP



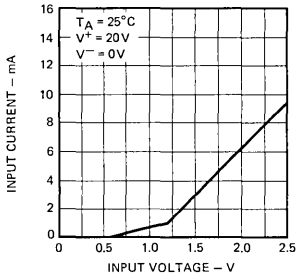
DC Power (P_{DC}) Versus Duty Cycle (DC)



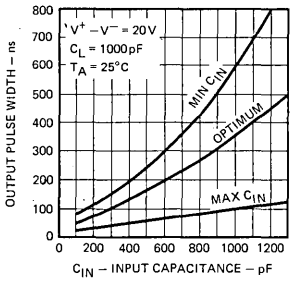
Transient Power (P_{AC}) Versus Frequency



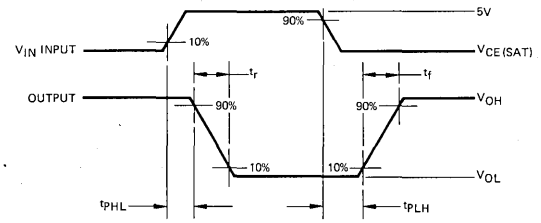
Input Current Versus Input Voltage



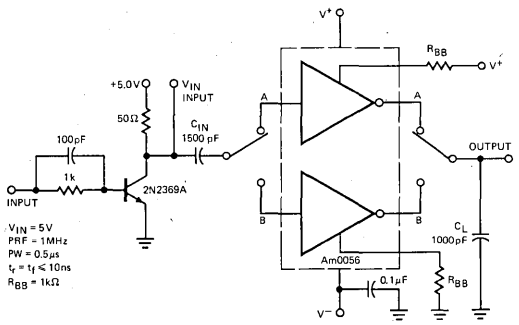
Optimum Input Capacitance Versus Output Pulse Width



SWITCHING TIME WAVEFORMS



AC TEST CIRCUIT



APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0056 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX.}$$

With the device dissipating only 10 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per Driver

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S\,(LOW)} \times \text{Duty Cycle}$$

where $I_{S\,(LOW)}$ is $I_{SUPPLY\,(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY\,(ON)} \text{ is } 30\text{mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ worst case}$$

$$\text{or } 15\text{mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ typically}$$

AC Transient Power per Driver

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-99 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent – derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

MAXIMUM LOAD CONSIDERATIONS

The maximum capacitive load that the Am0056 can drive is determined by:

The AC power consumed = $nVs^2\ C_L f \times 10^{-3}$ mW

The DC power consumed = $\frac{nVs^2}{Req}\ \rho \times 10^3$ mW

The package power rating for a given package, heatsink, and maximum ambient temperature = Pmax mW

Combining these expressions:

$$Pmax = \frac{nVs^2\ \rho \times 10^3}{Req} + nVs^2\ C_L f \times 10^{-3}$$

from which the maximum capacitive load:

$$C_{L(max)} = \frac{10^3}{n} \cdot \frac{(Pmax\ Req - nVs^2 \rho \times 10^3)}{Vs^2 f\ Req}$$

Where n = number of drivers employed in the package
Vs = total supply voltage $(V^+ - V^-)$ across device
ρ = duty cycle = time in output LOW state/time in output LOW + time in output HIGH

Req = $(V^+ - V^-)/I_{CC}$ ON = 1000 Ω worst case or 1300 Ω TYP

C_L = load capacitance per driver in pF

f = input signal frequency in MHz

When used as a non-overlapping, two-phase driver with each side operating at the same frequency and duty cycle and with V_s = 17 V, the above equation reduces to:

$$C_{L(max)} = \frac{10^3}{f}\left(\frac{Pmax}{578} - \rho\right)$$

Table 1 gives maximum drive capability using above equation.

PULSE WIDTH CONTROL

The Am0056 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_f = PW_{IN} + 17\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0056 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN}\ (3 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (3 \times 10^{-3})\ (500 \times 10^{-9}) = 1500\text{pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0056's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leq 1.5\text{ A}$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V) \quad (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20\,V) \quad (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\ ns$$

For small values of C_L, the equation above predicts optimistic values for t_r.

The output fall time may be predicted by:

$$t_f \cong 2.2\,R\left(C_S + \frac{C_L}{h_{FE}+1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0056 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0056. The critical value for $R_S = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2 R_S\, C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0056 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output will drop until Q_4 becomes active. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0056 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ and V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0056 is strongly recommended. This decoupling is necessary because of the 1.5 ampere currents which flow during logic transition when charging clock lines.

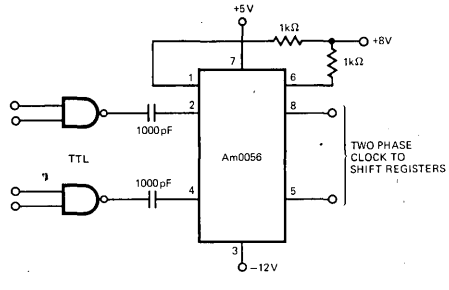
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0056*

Package Type			TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle	P_{Max}mW	1775	1400	1150	900	769	604	460	360	665
		Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100kHz	5%		30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500kHz	10%		6.0k	4.6k	3.8k	2.9k	2.5k	1.9k	1.4k	1.0k	2k
1MHz	20%		2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2MHz	25%		1.4k	1.1k	870	650	540	400	270	190	390
5MHz	25%		560	440	350	260	220	160	110	75	165
10MHz	25%		280	220	170	130	110	80	55	37	90

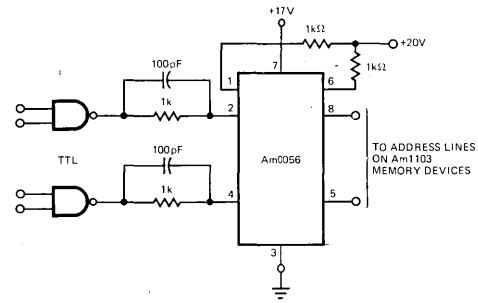
*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\,V$.

TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver

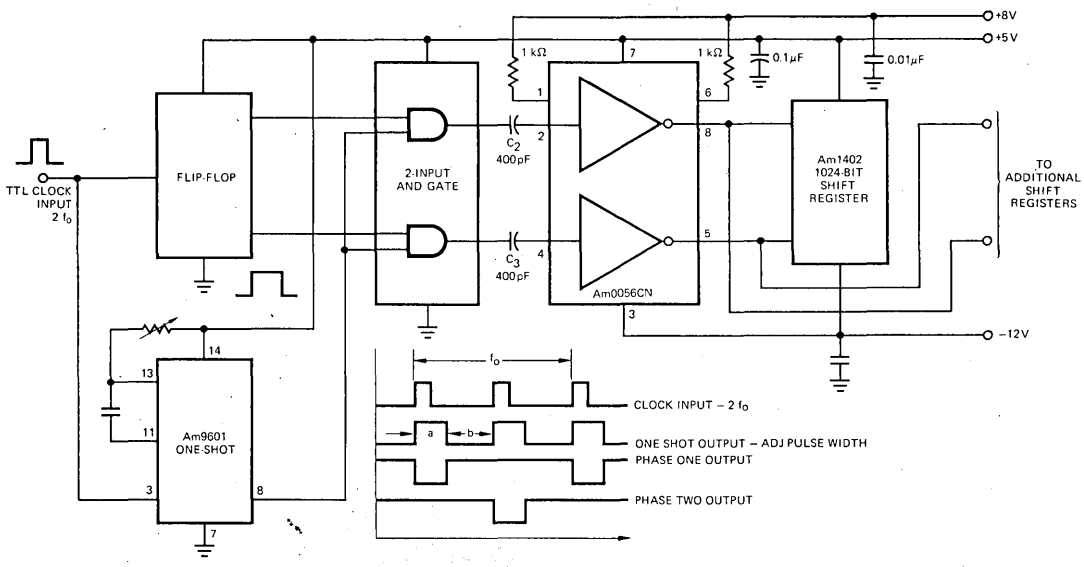


DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

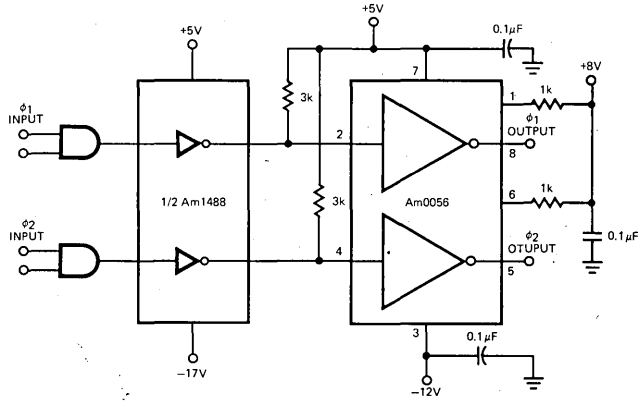


TYPICAL APPLICATIONS (Cont.)

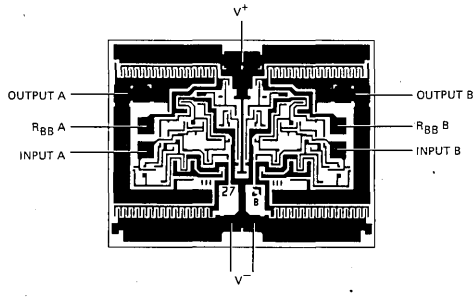
Logically Controlled AC Coupled Clock Driver



DC Coupled MOS Clock Driver



Metallization and Pad Layout



DIE SIZE 0.056" X 0.074"

Am3604

Dual Sense Amplifier for MOS Memories

Distinctive Characteristics

- Three-state outputs
- Input sensitivity 10mV max.
- Common mode range of ±3V
- Common mode range of more than ±15V using external attenuator
- High common rejection ratio
- Blocking diodes provide high input impedance
- 100% reliability assurance testing in compliance with MIL-STD-883

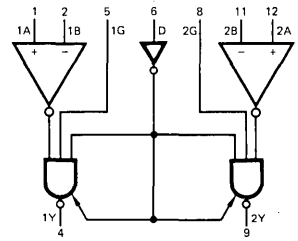
FUNCTIONAL DESCRIPTION

The Am3604 is a pin-for-pin replacement for the Am3603. The improved input sensitivity makes it more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes the Am3604 more useful in line receiver applications by allowing use of longer transmission line lengths. The Am3604 features a three-state output.

All devices contain blocking diodes in the input differential transistor pair collectors to provide high input impedance in the power-off condition.

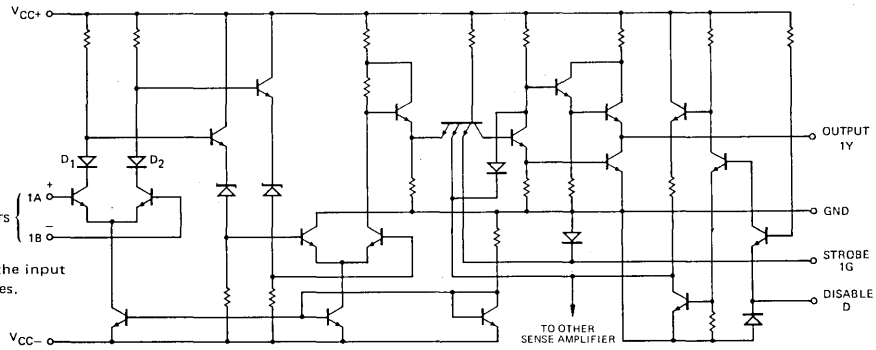
The device features a common three-state control, D. When the D input is HIGH, both outputs are in the high-impedance state regardless of all other inputs. Each sense amplifier also has a separate gate input, G. When the gate input is LOW and the D input is also LOW, the sense amplifier output is HIGH regardless of the A and B inputs.

LOGIC SYMBOL



V_{CC-} = Pin 13
V_{CC+} = Pin 14
GND = Pin 7

SCHEMATIC DIAGRAM
(One Sense Amplifier Shown)

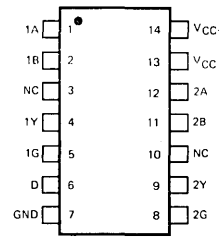


Note: D_1 and D_2 are the input protection diodes.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	DS3604N
Hermetic DIP	0°C to +70°C	DS3604J
Dice	0°C to +70°C	AM3604C

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC+} max.
DC Input Voltage – Strobe	−0.5V to +5.5V
Differential Input Voltage	±6V
Common Mode Input Voltage (with Respect to GND Terminal)	±5V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am3604 $T_A = 0°C$ to $+70°C$ $V_{CC+} = 5.0V \pm 5\%$ $V_{CC-} = -5.0V \pm 5\%$

Parameters	Description	Test Conditions (Notes 1 and 4)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OH} = −2mA, V_{IC} = −3V to 3V V_{ID} = 10mV		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OL} = 16mA, V_{IC} = −3V to 3V V_{ID} = 10mV				0.4	Volts
V_{IH}	Disable or Gate Input HIGH Voltage	Guaranteed input logical HIGH voltage		2			Volts
V_{IL}	Disable or Gate Input LOW Voltage	Guaranteed input logical LOW voltage				0.8	Volts
V_{IDH}	Differential Input Voltage for Output HIGH			0.010		5.0	Volts
V_{IDL}	Differential Input Voltage for Output LOW			−5.0		−0.010	Volts
I_{IH}	Input HIGH Current into 1A,2A,1B or 2B	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	µA
I_{IL}	Input LOW Current into 1A,2A,1B or 2B	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = −2V, V_{IC} = −3V to 3V				−10	µA
I_{IH}	Input HIGH Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = 2.4V				40	µA
I_I	Input HIGH Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = V_{CC+} MAX.				1.0	mA
I_{IL}	Input LOW Current into G or D	V_{CC+} = MAX., V_{CC-} = MAX. V_{IL} = 0.4V				−1.6	mA
I_O	Output (off-state) Leakage	V_{CC+} = MIN. V_{CC-} = MIN.	V_O = 2.4V			40	µA
			V_O = 0.4V			−40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC+} = MAX., V_{CC-} = MAX.		−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 10mV, $T_A = 25°C$			28	40	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 10mV, $T_A = 25°C$			−8.4	−15	mA
V_I	Input Clamp Voltage, G or D	V_{CC+} = MIN., V_{CC-} = MIN. I_{IN} = −12mA, $T_A = 25°C$			−1	−1.5	Volts

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC+} = 5.0V$, $V_{CC-} = -5.0V$, $T_A = 25°C$ ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. V_{CC} = common mode voltage with respect to GND terminal.
   V_{ID} = differential voltage ($V_A - V_B$).

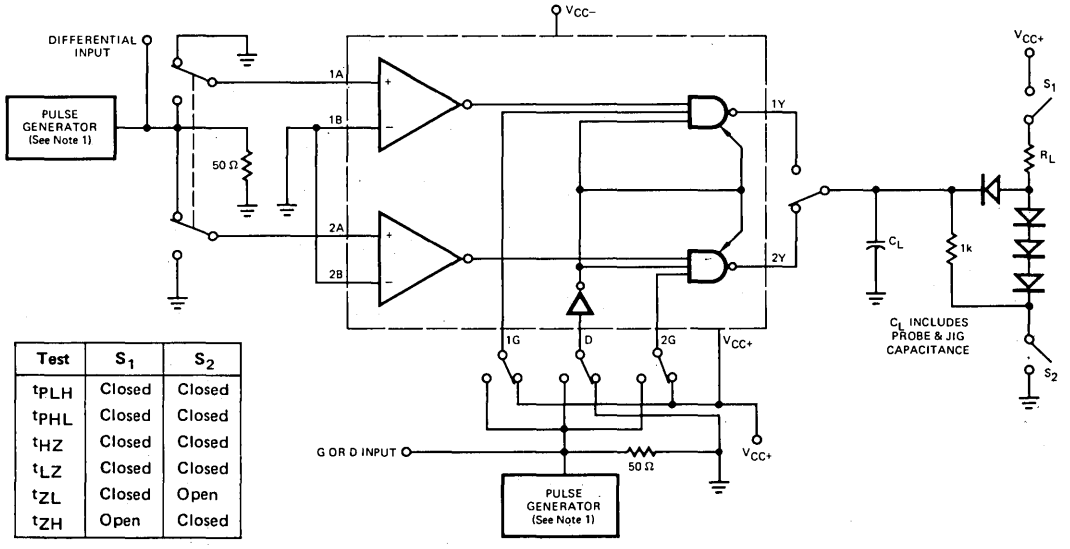
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC+} = 5.0V, V_{CC-} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} (Note 2)	A and B to Output	R_L = 470Ω, C_L = 15pF			35	ns
t_{PHL} (Note 2)	A and B to Output				20	ns
t_{PLH}	G to Output				17	ns
t_{PHL}	G to Output				17	ns
t_{HZ}	D to Output	R_L = 470Ω, C_L = 5pF			20	ns
t_{LZ}	D to Output	R_L = 470Ω, C_L = 5pF			30	ns
t_{ZH}	D to Output	R_L = 1kΩ to 0V, C_L = 15pF			25	ns
t_{ZL}	D to Output	R_L = 470Ω, C_L = 15pF			25	ns

Notes: 1. Differential input is +100mV to −100mV pulse. Delays read from 0mV on input to 1.5V on output.
2. Differential input is +10mV to −30mV pulse. Delays read from 0mV on input to 1.5V on outputs.

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



Test	S_1	S_2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{HZ}	Closed	Closed
t_{LZ}	Closed	Closed
t_{ZL}	Closed	Open
t_{ZH}	Open	Closed

Note: The pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_r = t_f$ = 10 ±5ns.

FUNCTION TABLE

Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs		Output Y
	Gate G	Disable D	
$V_{ID} \geq +10mV$	X	L	H
$-10mV < V_{ID} < +10mV$	H	L	?
$V_{ID} \leq -10mV$	H	L	L
X	L	L	H
X	X	H	Z

H = HIGH
L = LOW
X = Don't Care
? = Don't Know
Z = High-Impedance State

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted).

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_{HZ} The delay time from a control input change to the three-state output HIGH-level to high-impedance transition.

t_{LZ} The delay time from a control input change to the three-state output LOW-level to high-impedance transition.

t_{ZH} The delay time from a control input change to the three-state output high impedance to HIGH-level transition.

t_{ZL} The delay time from a control input change to the three-state output high impedance to LOW-level transition.

DEFINITION OF FUNCTIONAL TERMS

1A, 2A The non-inverting input of the line receivers.

1B, 2B The inverting input of the line receivers.

1Y, 2Y The output of each line receiver.

1G, 2G The gate input of each line receiver. A LOW on the gate input forces the output HIGH.

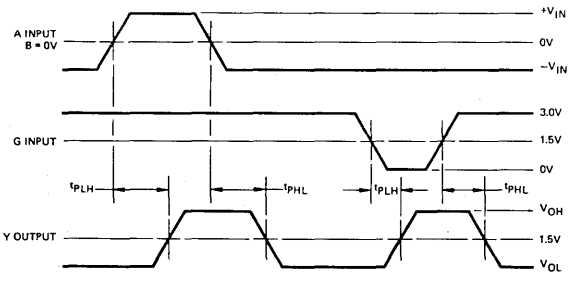
V_{IC} Input Common Mode voltage with respec to ground terminal.

V_{ID} Differential Input voltage $(V_A - V_B)$.

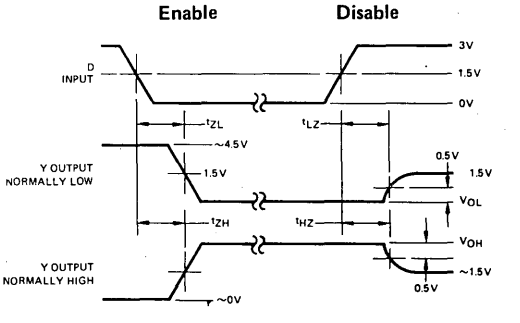
D The disable input that is common to both line receivers. A HIGH on the D input forces both line receivers to the high-impedance state.

VOLTAGE WAVEFORMS

PROPAGATION DELAY

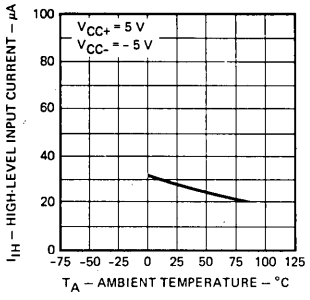


ENABLE AND DISABLE TIMES

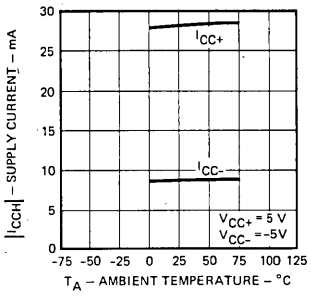


PERFORMANCE CURVES

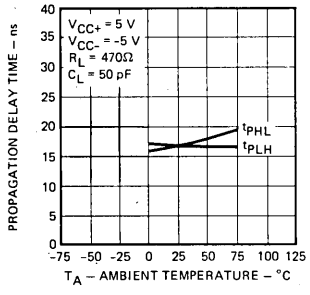
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



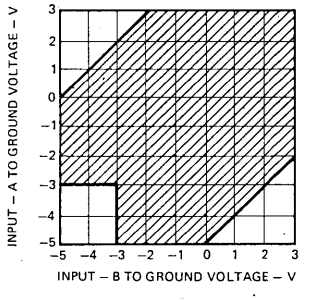
High-Logic-Level Supply Current Versus Ambient Temperature



Propagation Delay Time Differential Inputs Versus Ambient Temperature



Recommended Combinations of Input Voltage for Line Receivers



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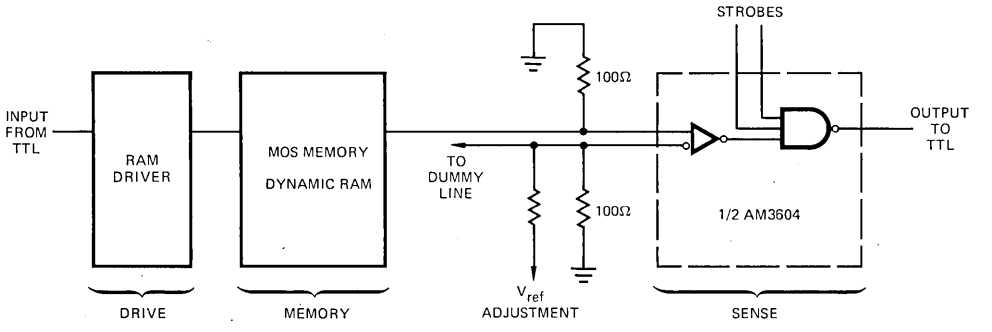
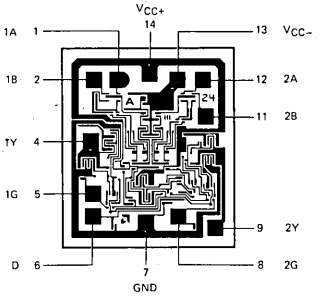
APPLICATION



MOS MEMORY SENSE AMPLIFIER

Metallization and Pad Layout



DIE SIZE 0.049" X 0.056"

Am75207 • Am75208

Dual Sense Amplifiers for MOS Memories

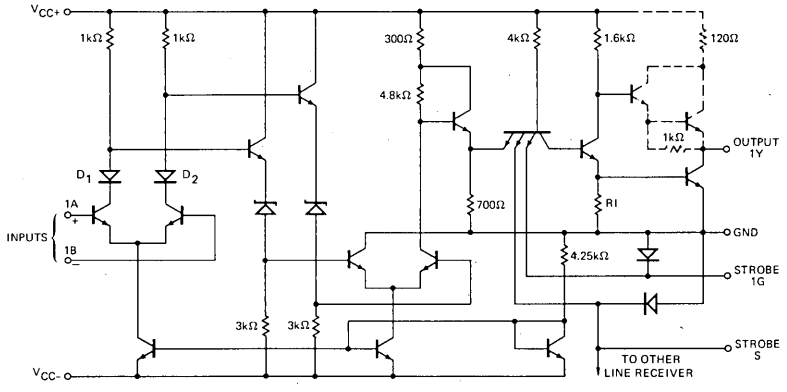
Distinctive Characteristics

- ±10mV guaranteed input sensitivity
- Common mode range of ±3.0V
- Common mode range of more than ±15V using external attenuator
- TTL compatible output
- High common mode rejection ratio
- Blocking diodes provide high input impedance
- Strobe and gate inputs for flexibility
- 100% reliability assurance testing in compliance with MIL-STD-883
- Standard supply voltages of ±5.0V

FUNCTIONAL DESCRIPTION

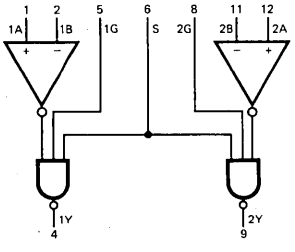
The Am75207 and Am75208 are pin-for-pin replacements for the Am75107A and Am75108A, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The Am75207 features a TTL-compatible active-pull-up output. The Am75208 features an open-collector output that permits wired-AND logic connections with similar output configurations.

SCHEMATIC DIAGRAM
(One Receiver Shown)



Notes: 1. Components shown with dashed lines are applicable to the Am75207 only.
2. R_1 = 1.0kΩ for Am75207, 750Ω for Am75208.
3. D_1 and D_2 are the input protection diodes.

LOGIC SYMBOL

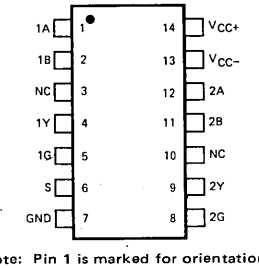


V_{CC-} = Pin 13
V_{CC+} = Pin 14
GND = Pin 7

ORDERING INFORMATION

Package Type	Temperature Range	Am75207 Order Number	Am75208 Order Number
Molded DIP	0°C to +70°C	SN75207N	SN75208N
Hermetic DIP	0°C to +70°C	SN75207J	SN75208J
Dice	0°C to +70°C	AM75207X	AM75208X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7.0V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC+} max.
DC Input Voltage — Strobe	−0.5V to +5.5V
Differential Input Voltage	±6.0V
Common Mode Input Voltage (with Respect to GND Terminal)	±5.0V
Any Differential Input to Ground	−5.0V to +3.0V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The following conditions apply unless otherwise noted: $T_A = 0°C$ to $+70°C$, $V_{CC+} = 5.0V \pm 5\%$, $V_{CC-} = -5.0V \pm 5\%$

Parameters	Description	Test Conditions (Notes 1, 4, & 5)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC+} = MIN., V_{CC-} = MIN., I_{OH} = −400μA, V_{IC} = −3.0V to +3.0V		2.4			V
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN., I_{OL} = 16mA, V_{IC} = −3.0V to +3.0V				0.4	V
V_{IDH}	Differential Input Voltage for Output HIGH	See Test Table		0.010		5.0	V
V_{IDL}	Differential Input Voltage for Output LOW	See Test Table		−0.5		−0.010	V
I_{IH}	Input HIGH Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX., V_{ID} = 0.5V, V_{IC} = −3.0V to +3.0V			30	75	μA
I_{IL}	Input LOW Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX., V_{ID} = −2.0V, V_{IC} = −3.0V to +3.0V				−10	μA
I_{IH}	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX., V_{IH} = 2.4V	S			80	μA
			G			40	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX., V_{IH} = V_{CC+}MAX.	S			2.0	mA
			G			1.0	
I_{IL}	Input LOW Current	V_{CC+} = MAX., V_{CC-} = MAX., V_{IL} = 0.4V	S			−3.2	mA
			G			−1.6	
I_{OH}	HIGH Level Output (Am75208 Only)	V_{CC+} = MIN., V_{CC-} = MIN., V_{OH} = V_{CC+}MAX.				250	μA
I_{SC}	Output Short Circuit Current (Note 3) (Am75207 Only)	V_{CC+} = MAX., V_{CC-} = MAX.		−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX., V_{ID} = 10mV, T_A = 25°C			18	30	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX., V_{ID} = 10mV, T_A = 25°C			−8.4	−15	mA

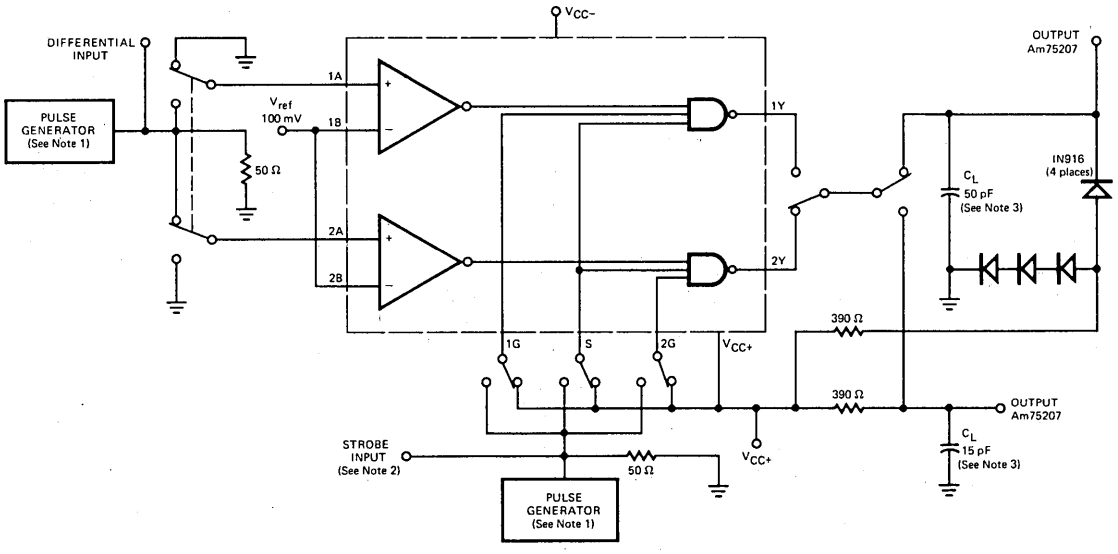
Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC+} = 5.0V, V_{CC-} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. V_{IC} = common mode voltage with respect to GND terminal.
   V_{ID} = differential voltage ($V_A - V_B$).

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC}+ = +5V, V_{CC}– = –5V)

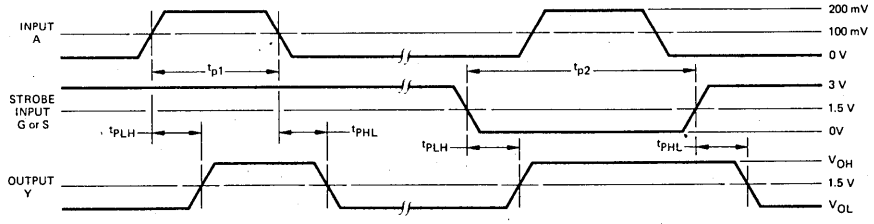
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A and B to Output	R_L = 470 Ω C_L = 15 pF			35	ns
t_{PHL}	A and B to Output				20	ns
t_{PLH}	G or S to Output				17	ns
t_{PHL}	G or S to Output				17	ns

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS



Notes:
1. The pulse generators have the following characteristics: Z_{out} = 50Ω, t_r = t_f = 10 ± 5.0ns, t_{p1} = 500ns, PRR = 1.0MHz, t_{p2} = 1.0ns, PRR = 500kHz.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A–1B are being tested, to Strobe S when inputs 1A–1B or 2A–2B are being tested, and to strobe 2G when inputs 2A–2B are being tested.
3. C_L includes probe and jig capacitance.

FUNCTION TABLE

Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs		Output
	Gate	Strobe	
	G	S	Y
$V_{ID} \geq +10mV$	X	X	H
$-10mV < V_{ID} < 10mV$	H	H	?
$V_{ID} \leq -25mV$	H	H	L
X	L	X	H
X	X	L	H

H = HIGH
L = LOW
X = Don't Care
? = Don't Know

DEFINITION OF FUNCTIONAL TERMS

1A, 2A The non-inverting input of the line receivers.

1B, 2B The inverting input of the line receivers.

1Y, 2Y The output of each line receiver.

1G, 2G The gate input of each line receiver. A LOW on the gate input forces the output HIGH.

S The strobe input that is common to both line receivers. A LOW on the strobe forces both (1Y and 2Y) outputs HIGH.

V_{IC} Input Common Mode voltage with respect to ground terminal.

V_{ID} Differential Input voltage ($V_A - V_B$).

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

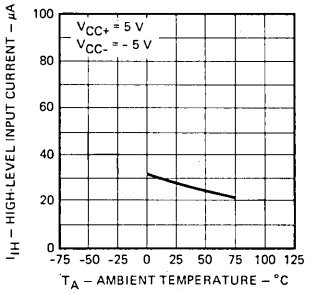
DC TEST TABLE

Parameter	1A	2A	1B 2B	V_{IC} (Common Mode)	V_{ID} (Differential)	1Y 2Y	1G	2G	S	Note
V_{IDH}	–		–	−3V to 3V	Test	−400μA (Note 2)	+5V		+5V	1
V_{IDL}	–		–	−3V to 3V	Test	16mA	+5V		+5V	1
I_{IH} @ A	–		–	−3V to 3V	+0.5V	Open	Open		Open	1
I_{IL} @ A	–		–	−3V to 3V	−2V	Open	Open		Open	1
V_{OL} @ Y	–		–	−3V to 3V	−10mV	16mA	V_{IH}		V_{IH}	1
V_{OH} @ Y	–		–	−3V to 3V	+10mV	−400μA	V_{IH}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	−3V to 3V	−10mV	−400μA	V_{IL}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	−3V to 3V	−10mV	−400μA	V_{IH}		V_{IL}	1 & 2
I_{OH} @ Y	–		–	−3V to 3V	+10mV	V_{CC}+MAX.	V_{IH}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	−3V to 3V	−10mV	V_{CC}+MAX.	V_{IL}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	−3V to 3V	−10mV	V_{CC}+MAX.	V_{IH}		V_{IL}	1 & 3
I_{IH} @ 1G	+10mV	GND	GND	–	–	Open	V_{IH}	GND	GND	–
I_{IH} @ 2G	GND	+10mV	GND	–	–	Open	GND	V_{IH}	GND	–
I_{IH} @ S	+10mV	+10mV	GND	–	–	Open	GND	GND	V_{IH}	–
I_{IL} @ 1G	−10mV	GND	GND	–	–	Open	V_{IL}	GND	4.5V	–
I_{IL} @ 2G	GND	−10mV	GND	–	–	Open	GND	V_{IL}	4.5V	–
I_{IL} @ S	−10mV	−10mV	GND	–	–	Open	4.5V	4.5V	V_{IL}	–
I_{OS} @ Y	+10mV		GND	–	–	GND	GND		GND	–
I_{CC+}	+10mV		GND	–	–	Open	+5V		+5V	–
I_{CC-}	+10mV		GND	–	–	Open	+5V		+5V	–

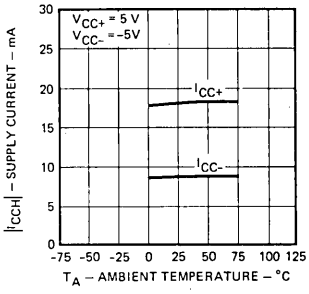
Notes: 1. When testing one channel, the inputs of the other channels are grounded.
2. Am25207 only.
3. Am75208 only.

PERFORMANCE CURVES

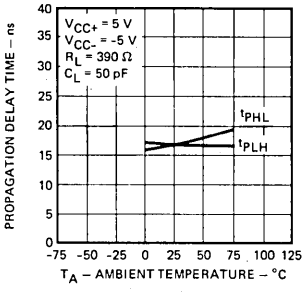
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



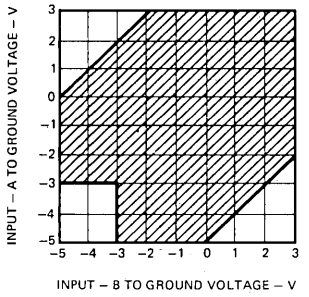
High-Logic-Level Supply Current Versus Ambient Temperature



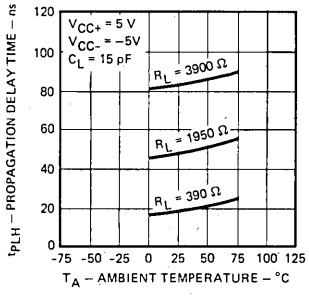
Am207 Propagation Delay Time Differential Inputs Versus Ambient Temperature



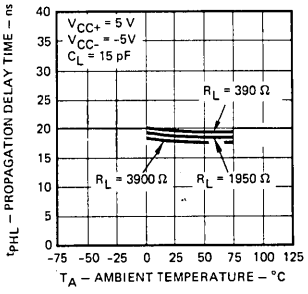
Recommended Combinations of Input Voltage for Line Receivers



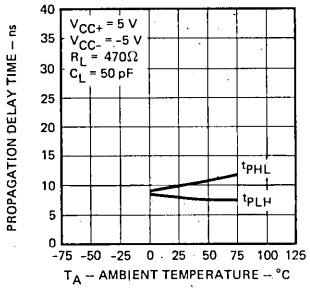
Am75208 Propagation Delay Time Low-to-High Level Differential Inputs Versus Ambient Temperature



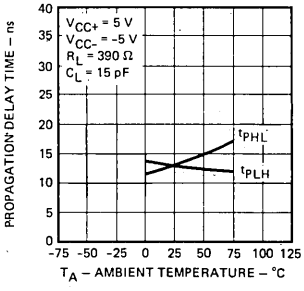
Am75208 Propagation Delay Time High-to-Low Level Differential Inputs Versus Ambient Temperature



Am75207 Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Am75208 Propagation Delay Time Strobe Inputs Versus Ambient Temperature



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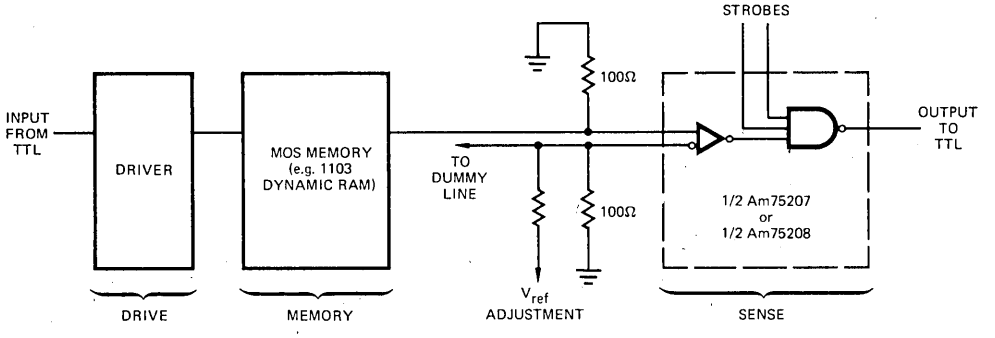
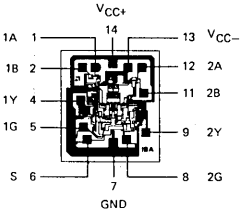
APPLICATION



MOS Memory Sense Amplifier

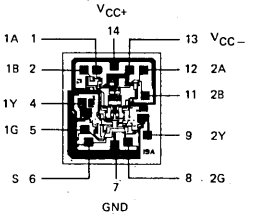
Metallization and Pad Layouts

Am75207



DIE SIZE: 0.049" X 0.056"

Am75208



DIE SIZE: 0.049" X 0.056"

Am8224

Clock Generator and Driver

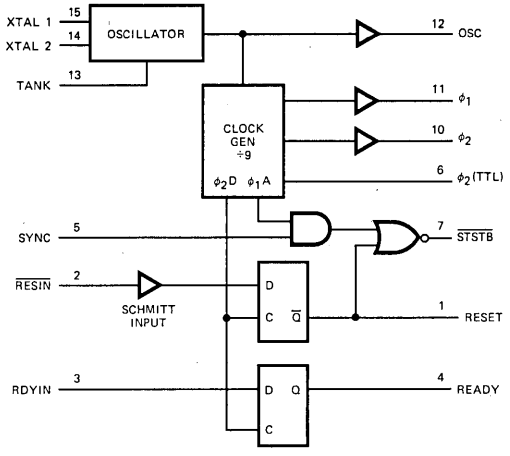
Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and $\phi 2$ outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications.

LOGIC DIAGRAM



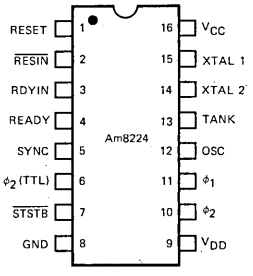
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM8224DM
Hermetic DIP	0°C to +70°C	AM8224DC
Molded DIP	0°C to +70°C	AM8224PC
Dice	0°C to +70°C	AM8224XC

PIN DEFINITION

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
$\phi 2$(TTL)	$\phi 2$ CLK (TTL LEVEL)
V_{CC}	+5.0V
V_{DD}	+12V
GND	0V
$\overline{RESIN}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{STSTB}$	STATUS STB (ACTIVE LOW)
$\phi 1$	Am9080A/8080A CLOCKS
$\phi 2$	

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	7.5V
V_{DD}	15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% V_{DD} = 12 V ±5%
Am8224XM (MIL) T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% V_{DD} = 12 V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 2)	Max.	Units
I_F	Input Current Loading	V_F = 0.45 V				−0.25	mA
I_R	Input Leakage Current	V_R = 5.25 V				10	μA
V_C	Input Forward Clamp Voltage	I_C = −5.0 mA	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage	V_{CC} = 5.0 V				0.8	Volts
V_{IH}	Input HIGH Voltage	Reset input	COM'L	2.6	2.2		Volts
			MIL	2.8	2.2		
		All other inputs		2.0			
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5.0 V		0.25	0.5		Volts
V_{OL}	Output LOW Voltage	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA				0.45	Volts
		All other inputs I_{OL} = 15 mA				0.45	
V_{OH}	Output HIGH Voltage	ϕ_1, ϕ_2; I_{OH} = −100μA	COM'L	9.4	11		Volts
			MIL	V_{DD} −1.6V	V_{DD} −1.0V		
		READY, RESET; I_{OH} = −100μA	COM'L	3.6	4.0		
			MIL	3.35	4.0		
		All other outputs; I_{OH} = −1.0 mA		2.4	3.0		
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)	V_O = 0 V V_{CC} = 5.0 V		−10		−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 3)			70	115	mA
I_{DD}	Power Supply Current	V_{DD} = MAX.			5.0	12	mA

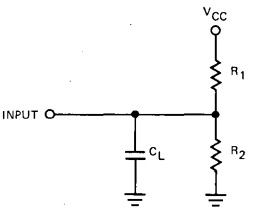
Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.
2. Typical limits are at V_{CC} = 5.0 V, V_{DD} = 12 V, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

TEST CIRCUIT



AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8224XM Min.	Am8224XM Typ.	Am8224XM Max.	Am8224XC Min.	Am8224XC Typ.	Am8224XC Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	C_L = 20pF to 50pF	$\frac{2t_{CY}}{9}$ - 23ns			$\frac{2t_{CY}}{9}$ - 20ns			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		$\frac{5t_{CY}}{9}$ - 35ns			$\frac{5t_{CY}}{9}$ - 35ns			
t_{D1}	ϕ_1 to ϕ_2 Delay		0			0			
t_{D2}	ϕ_2 to ϕ_1 Delay		$\frac{2t_{CY}}{9}$ - 17ns			$\frac{2t_{CY}}{9}$ - 14ns			
t_{D3}	ϕ_1 to ϕ_2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ + 22ns	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ + 20ns	
t_r	ϕ_1 and ϕ_2 Rise Time				20			20	
t_f	ϕ_1 and ϕ_2 Fall Time				20			20	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	ϕ_2 (TTL), C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω	−5.0		15	−5.0		15	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{6t_{CY}}{9}$ - 33ns		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}$ - 30ns		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9}$ - 18ns			$\frac{t_{CY}}{9}$ - 15ns			
t_{DRS}	RDYIN Set-up Time to Status Strobe		50ns - $\frac{4t_{CY}}{9}$			50ns - $\frac{4t_{CY}}{9}$			
t_{DRH}	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			$\frac{4t_{CY}}{9}$			
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset, C_L = 10pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{4t_{CY}}{9}$ - 25ns			$\frac{4t_{CY}}{9}$ - 25ns			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$			$\frac{t_{CY}}{9}$		
f_{max}	Maximum Oscillating Frequency		27			28.12			MHz
C_{in}	Input Capacitance	V_{CC} = 5.0V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1.0MHz			8.0			8.0	pF

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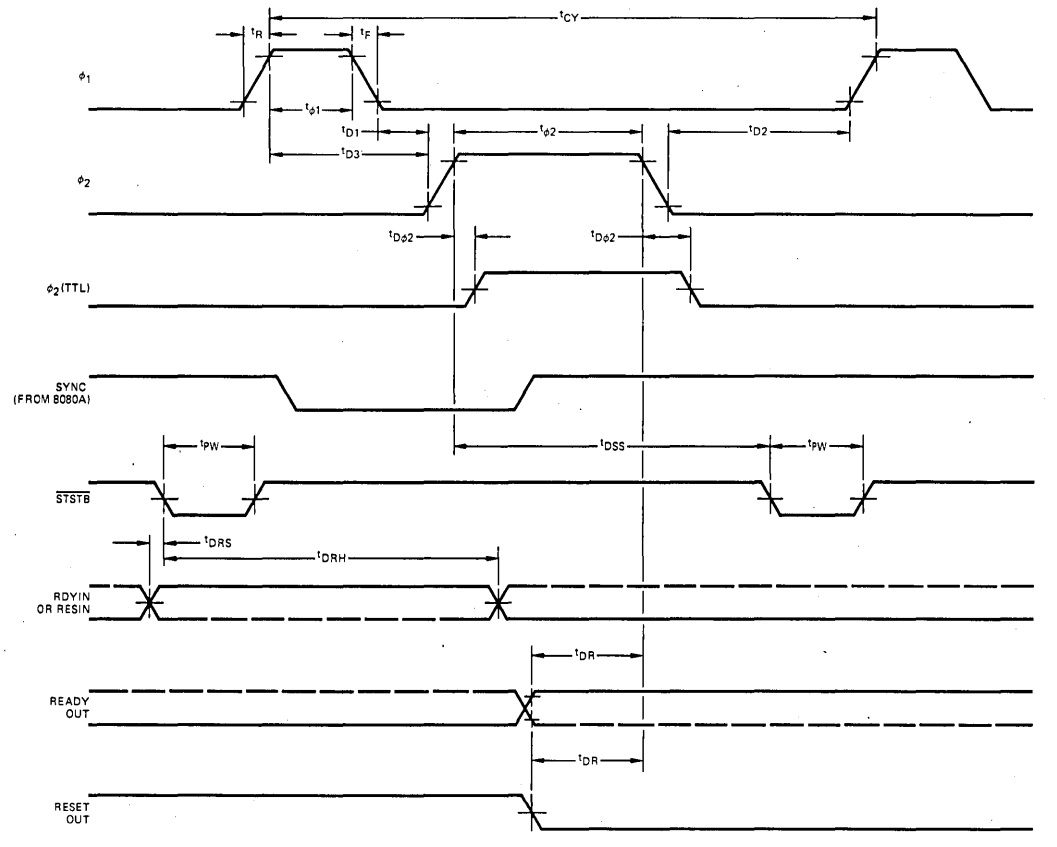
AC CHARACTERISTICS (For t_{CY} = 488.28ns)

T_A = 0°C to +70°C V_{CC} = +5.0V ±5% V_{DD} = +12V ±5%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	ϕ_1 and ϕ_2 Loaded to C_L = 20 to 50pF	89			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		236			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		95			ns
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay		−5.0		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-up Time to $\overline{STSTB}$	Ready and Reset Loaded to 2.0mA/10pF	−167			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		217			ns
t_{DR}	Ready or Reset to ϕ_2 Delay		192			ns
FREQ	Oscillator Frequency				18.432	MHz

Note: 1. All measurements referenced to 1.5V unless specified otherwise.

SWITCHING WAVEFORMS



Voltage measurement points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to guide the crystal selection is:

$$\text{Crystal Frequency} = \frac{1}{t_{CY}} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" may be necessary to produce the desired frequency. The addition of a small selected capacitance (3pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has much lower "gain" than the fundamental type so an external LC network is necessary to provide the additional "gain" for proper oscillator operation. The external LC network is connected to the TANK input and is AC coupled to ground. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; phase 1 and phase 2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator fre-

quency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{STSTB}$) is achieved.

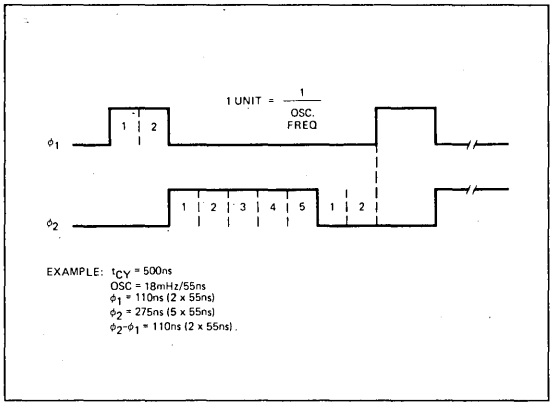


Figure 1. Clock Generator Waveforms.

$\overline{STSTB}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ1A), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{STSTB}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{STSTB}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{RESIN}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ2D (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ2D, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

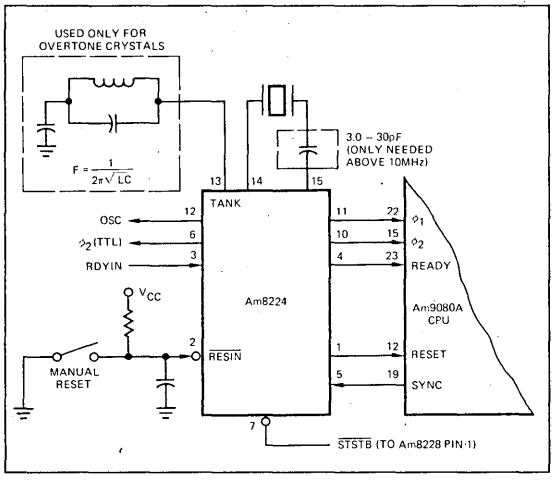
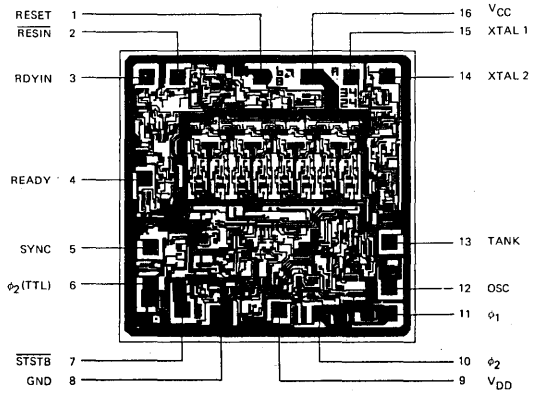


Figure 2. Typical Application with Am8224 and Am9080A.

Metallization and Pad Layout



DIE SIZE
0.085" X 0.084"

Am8228 • Am8238

System Controller and Bus Driver

Distinctive Characteristics

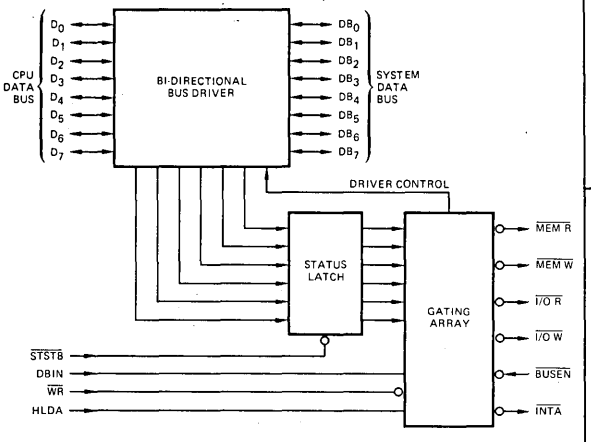
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080A/8080A systems
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}$/$\overline{MEMW}$ pulse width

FUNCTIONAL DESCRIPTION

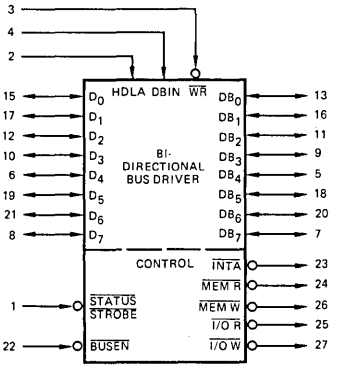
The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A single byte and multiple byte interrupt operation.

LOGIC DIAGRAM

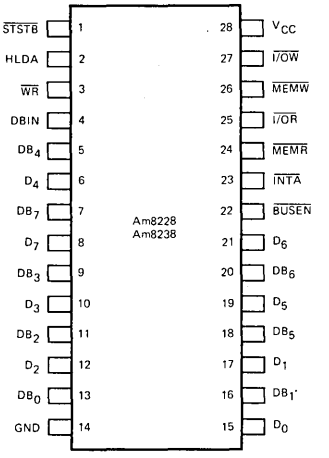


LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−1.5V to +7.0V
DC Output Current, Into Outputs	50mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228DM, Am8238DM T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V
Am8228PC, Am8228XC, D8228, Am8238PC, Am8238XC, D8238 T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −10μA	D_0-D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			I_{OH} = −1.0mA	All other outputs		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0-D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., I_C = −5.0mA					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				500	μA
				D_2 and D_6				750	
				All other inputs				250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0-DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Off State Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Ouputs)	V_{CC} = 5.0V				15		90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8228XM/Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/Am8238XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe		22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7		12			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7		5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	C_L = 100pF	20	30	60	20	30	60	ns
t_{RR}	Delay from DBIN to Control Outputs			15	35		15	30	ns
t_{RE}	Delay from DBIN to Enable/Disable 8080A Bus	C_L = 25pF		25	45		25	45	ns
t_{RD}	Delay from System Bus to 8080A Bus During Read			15	30		15	30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	C_L = 100pF	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$			25	36		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write		5.0	20	40	5.0	20	40	ns
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7			25	35		25	30	ns
t_{HD}	HLDA to Read Status Outputs			15	28		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA		10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20			20			ns

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

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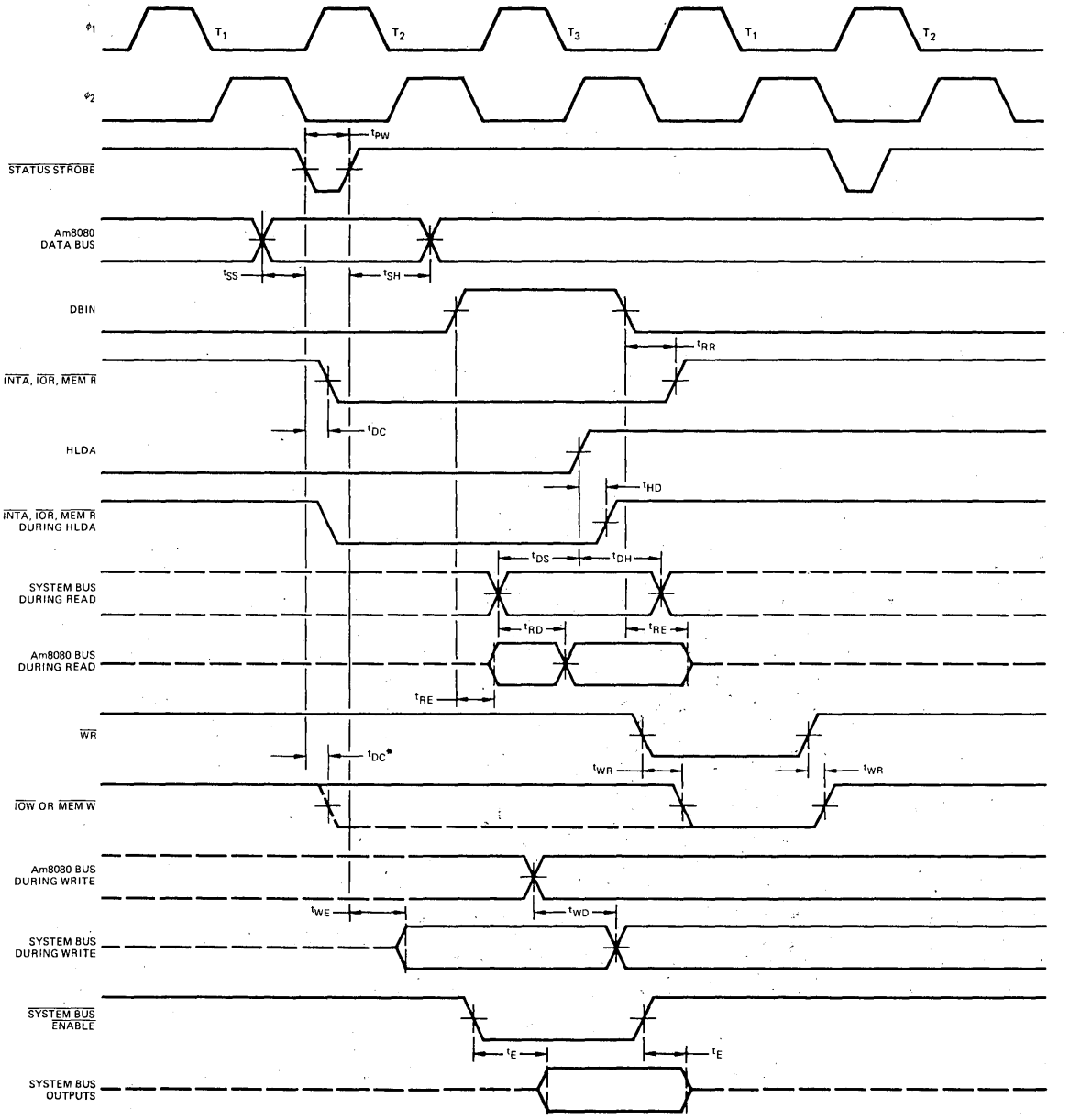
CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

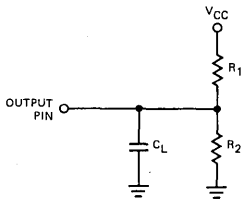
SWITCHING WAVEFORMS



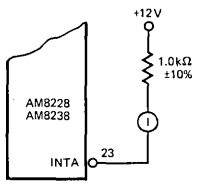
Voltage measurements points: $D_0 - D_7$ (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

TEST CIRCUITS



Note 1. For D_0-D_7: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.



INTA (for RST 7)

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

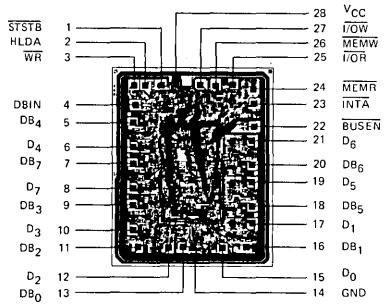
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{I/OR}$	Input/output read strobe output active LOW
$\overline{I/OW}$	Input/output write strobe output active LOW
$\overline{MEM\ R}$	Memory read strobe, output, active LOW
$\overline{MEM\ W}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{INTA}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{WR}$	Write input strobe, active HIGH
$\overline{BUSEN}$	BUSS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{STSTB}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

Metallization and Pad Layout



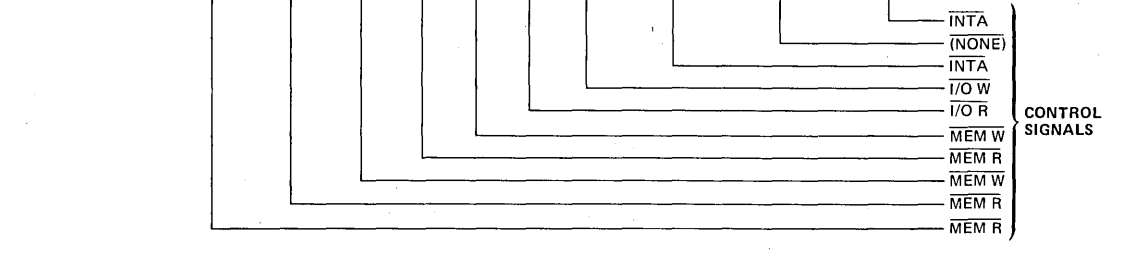
DIE SIZE 0.110" X 0.136"

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{STSTB}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{WR}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{MEM\ R}$	24	–	10mA	−1mA
$\overline{MEM\ W}$	26	–	10mA	−1mA
$\overline{I/OR}$	25	–	10mA	−1mA
$\overline{IOW}$	27	–	10mA	−1mA
$\overline{BUSEN}$	22	250μA	–	–
$\overline{INTA}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

STATUS WORD CHART

		TYPE OF MACHINE CYCLE										
Data Bus Bit	Status Information	Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEM R	1	1	0	1	0	0	0	0	1	0	



Operational Amplifiers — Section VII

Am101/201/301

Operational Amplifiers

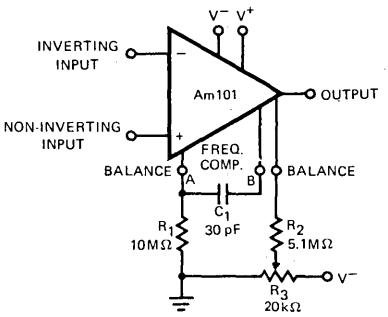
Description: The Am101/201/301 monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101, and LM201. They are available in the hermetic TO-99 metal can, dual-in-line packages, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883 Class B.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

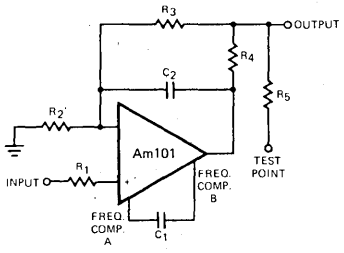
FUNCTIONAL DESCRIPTION

The Am101/201/301 are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor.

FUNCTIONAL DIAGRAM



APPLICATIONS



INPUT/OUTPUT OVERLOAD PROTECTION

If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

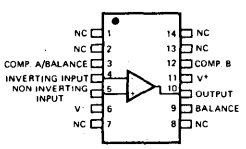
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am301	DIP	0°C to +70°C	LM301D
	Metal Can	0°C to +70°C	LM301H
	Dice	0°C to +70°C	LD301
Am201	DIP	−25°C to +80°C	LM201D
	Metal Can	−25°C to +80°C	LM201H
Am101	DIP	−55°C to +125°C	LM101D
	Metal Can	−55°C to +125°C	LM101H
	Dice	−55°C to +125°C	LD101

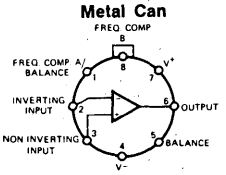
CONNECTION DIAGRAMS

Top Views

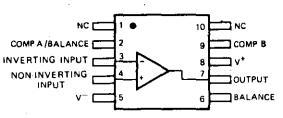
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am101	−55°C to +125°C
Am201	−25°C to +85°C
Am301	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

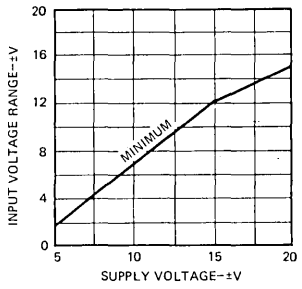
Parameter (see definitions)	Conditions	Am301 Min	Am301 Typ	Am301 Max	Am101 Am201 Min	Am101 Am201 Typ	Am101 Am201 Max	Units
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	7.5		1.0	5.0	mV
Input Offset Current			100	500		40	200	nA
Input Bias Current			250	1500		120	500	nA
Input Resistance		0.1	0.4		0.3	0.8		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$	20	150		50	160		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			10			6.0	mV
Input Offset Current	$T_A = T_{A\ (min)}$ $T_A = T_{A\ (max)}$		150 50	750 400		100 10	500 200	nA nA
Input Bias Current	$T_A = T_{A\ (min)}$		0.32	2		0.28	1.5	μA
Large Signal Voltage Gain	$V_S = \pm 15\ V, V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	15			25			V/mV
Input Voltage Range	$V_S = \pm 15\ V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	65	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Output Voltage Swing	$V_S = \pm 15\ V, R_L = 10\ k\Omega$, $R_L = 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C\ V_S = \pm 20\ V$					1.2	2.5	mA

Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V and C_l = 30 pF.

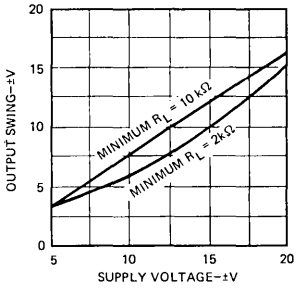
GUARANTEED PERFORMANCE CURVES

(Curves apply over the Operating Temperature Ranges)

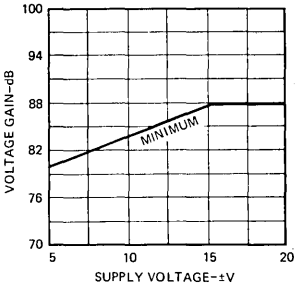
Input Voltage Range



Output Swing

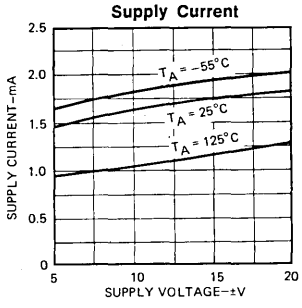


Voltage Gain

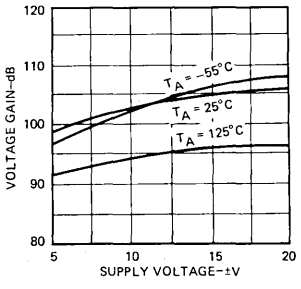


PERFORMANCE CURVES

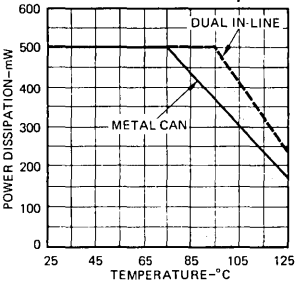
Supply Current



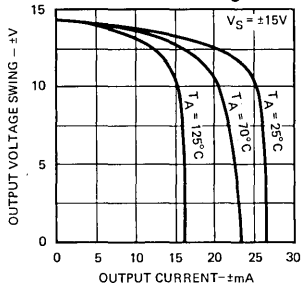
Voltage Gain



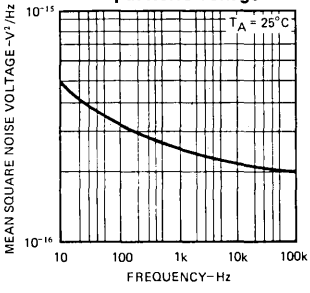
Maximum Power Dissipation



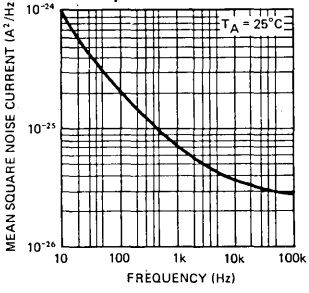
Current Limiting



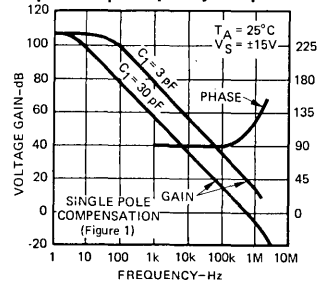
Input Noise Voltage



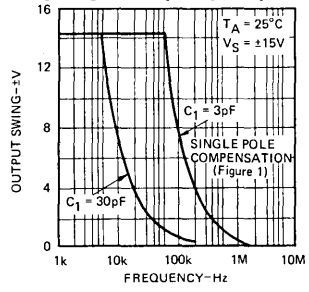
Input Noise Current



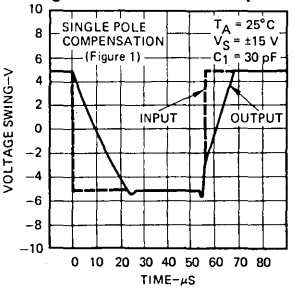
Open Loop Frequency Response



Large Signal Frequency Response



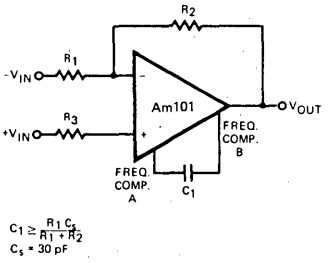
Voltage Follower Pulse Response



7

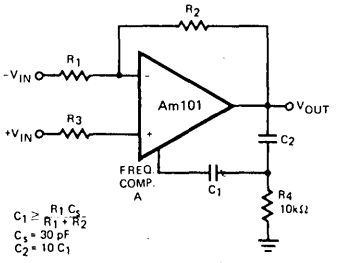
FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation



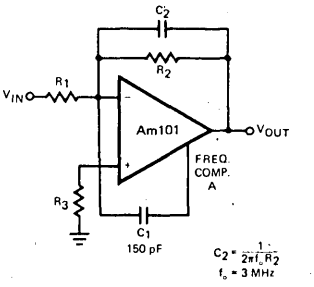
$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$
$C_S = 30\ pF$

Two Pole Compensation



$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$
$C_S = 30\ pF$
$C_2 = 10\ C_1$

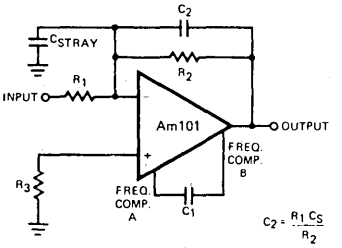
Feedforward Compensation



$C_2 = \frac{1}{2\pi f_o R_2}$
$f_o = 3\ MHz$

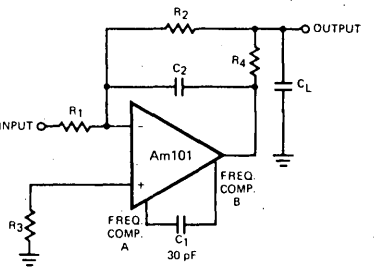
Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance



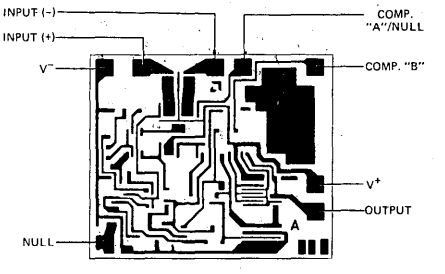
$C_2 = \frac{R_1 C_S}{R_2}$

Isolating Large Capacitive Loads



The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

Metallization and Pad Layout



49 x 56 Mils

Am101A/201A/301A

Operational Amplifiers

Description: The Am101A, Am201A and Am301A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101A, LM201A, and LM301A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

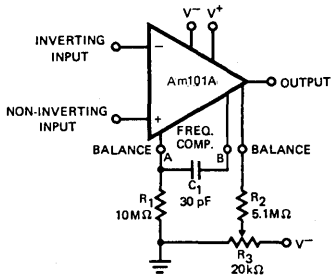
Distinctive Characteristics: 100% reliability ssurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

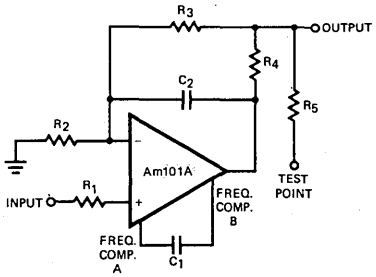
The Am101A/Am201A/Am301A are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the Am101A/Am201A/Am301A amplifiers for low level and general purpose applications.

FUNCTIONAL DIAGRAM



APPLICATIONS

INPUT/OUTPUT OVERLOAD PROTECTION



If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1 μF) is equivalent to a low-source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

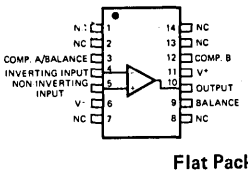
The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

ORDERING INFORMATION

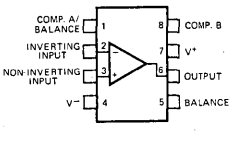
Part Number	Package Type	Temperature Range	Order Number
Am301A	DIP	0°C to +70°C	LM301AD
	Metal Can	0°C to +70°C	LM301AH
	Molded DIP	0°C to +70°C	LM301AN
	Dice	0°C to +70°C	LD301A
Am201A	DIP	−25°C to +85°C	LM201AD
	Metal Can	−25°C to +85°C	LM201AH
	Flat Pak	−25°C to +85°C	Lm201AF
Am101A	DIP	−55°C to +125°C	LM101AD
	Metal Can	−55°C to +125°C	LM101AH
	Flat Pak	−55°C to +125°C	LM101AF
	Dice	−55°C to +125°C	LD101A

CONNECTION DIAGRAM
Top Views

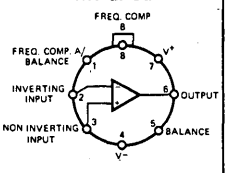
Dual-In-Line



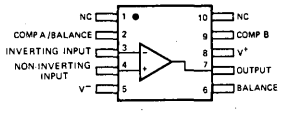
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

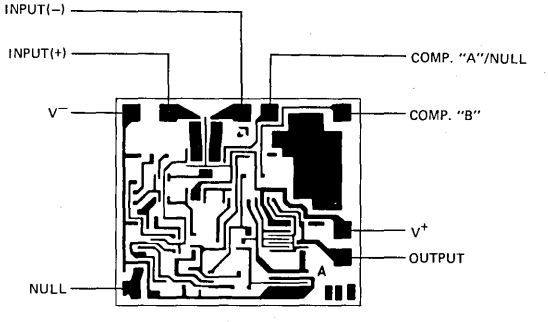
Supply Voltage Am101A, 201A Am301A	 ±22V ±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am101A Am201A Am301A	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am301A Min	Am301A Typ	Am301A Max	Am101A Am201A Min	Am101A Am201A Typ	Am101A Am201A Max	Units
Input Offset Voltage	$R_S \leq 50\ k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$ $V_S = \pm 15V$		1.8	3.0		1.8	3.0	mA mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	25	160		50	160		V/mV
Slew Rate	$V_S = \pm 20V$, $A_V = +1$		0.5			0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50\ k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{A\ (max)}$ $T_{A\ (min)} \leq T_A \leq$ 25°C		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	25			25			V/mV
Input Voltage Range	$V_S = \pm 20\ V$ $V_S = \pm 15\ V$	+15, −12			±15			V V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $R_L = 2\ k\Omega$,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	T_A = +125°C $V_S = \pm 20\ V$					1.2	2.5	mA

Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the 101A and 201A, and from ±5 V to ±15 V for the 301A.

Metallization and Pad Layout



49 X 56 Mils

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

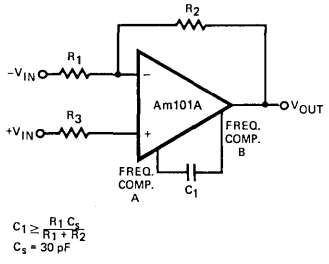


Figure 1

Two Pole Compensation

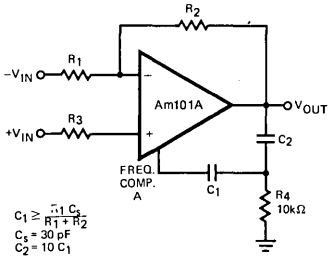


Figure 2

Feedforward Compensation

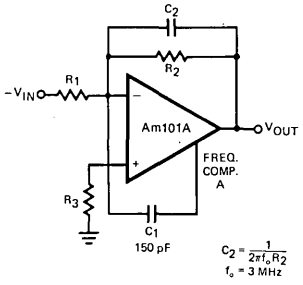


Figure 3

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance

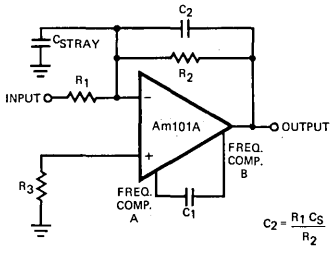


Figure 4

Isolating Large Capacitive Loads

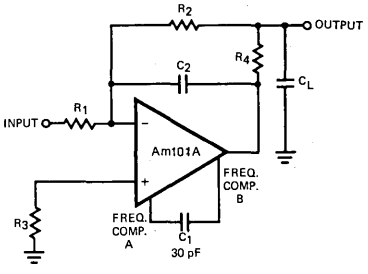


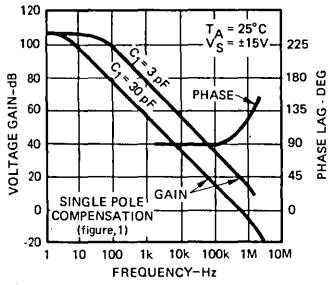
Figure 5

The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

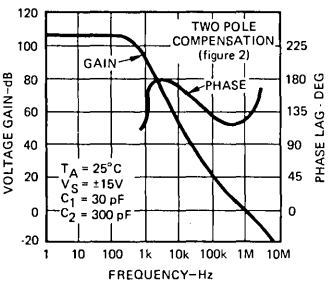
7

PERFORMANCE CURVES (Note 3)

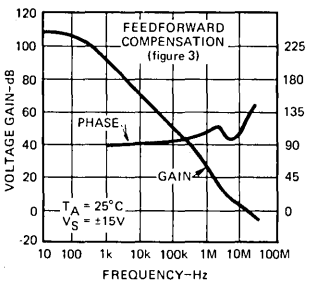
Open Loop Frequency Response



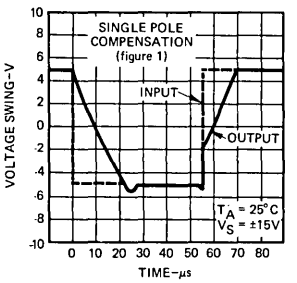
Open Loop Frequency Response



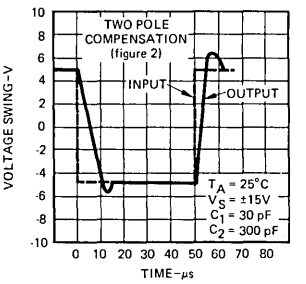
Open Loop Frequency Response



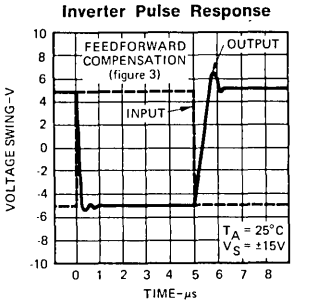
Voltage Follower Pulse Response



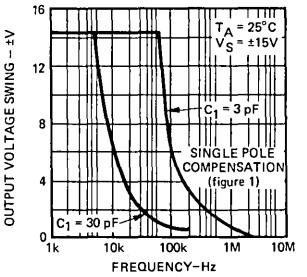
Voltage Follower Pulse Response



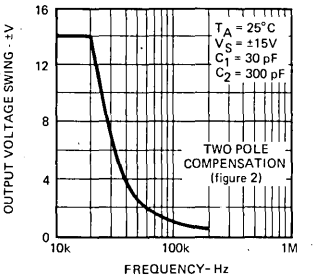
Inverter Pulse Response



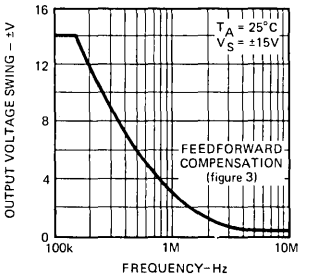
Large Signal Frequency Response



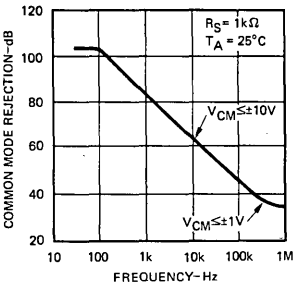
Large Signal Frequency Response



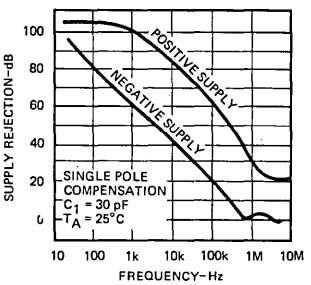
Large Signal Frequency Response



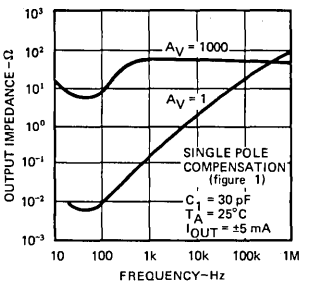
Common Mode Rejection



Power Supply Rejection



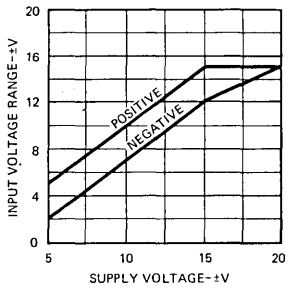
Closed Loop Output Impedance



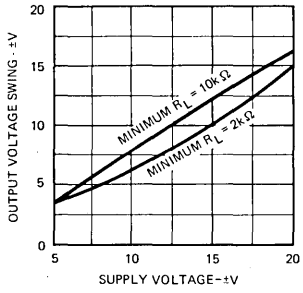
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

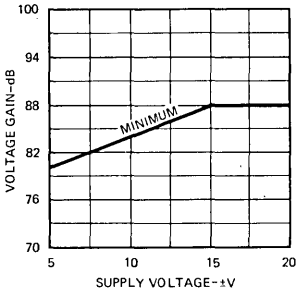
Input Voltage Range



Output Swing

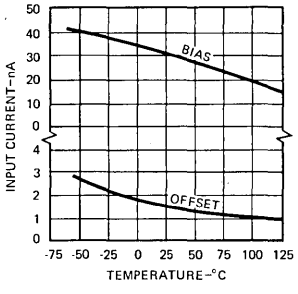


Voltage Gain

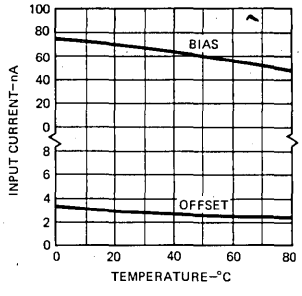


PERFORMANCE CURVES (Note 3)

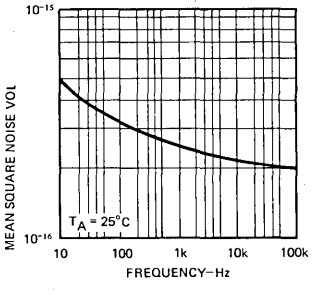
Input Current—101A, 201A



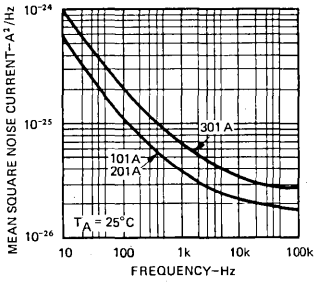
Input Current—301A



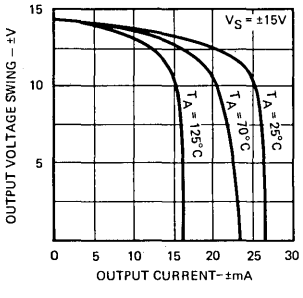
Input Noise Voltage



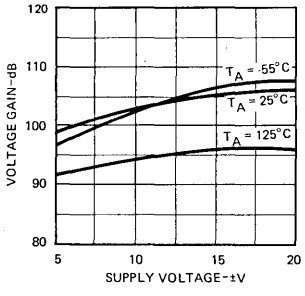
Input Noise Current



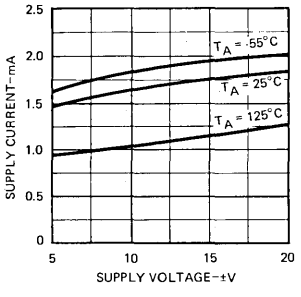
Current Limiting



Voltage Gain



Supply Current



7

Am102/202/302

Voltage Follower

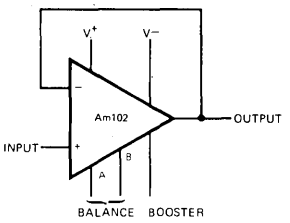
Distinctive Characteristics

- The Am102/202/302 are functionally, electrically, and pin-for-pin equivalent to the National LM102/202/302
- Slew rate: 20V/μs
- Small signal bandwidth: 20MHz
- Input current: 100nA max. over temperature
- Supply voltage range: ±5.0V to ±18V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected dice for hybrid manufacturers
- Available in metal can, hermetic dual-in-line or hermetic flat packages

FUNCTIONAL DESCRIPTION

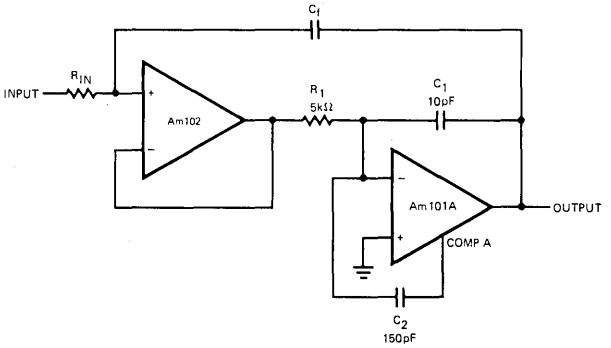
The Am102/202/302 is a monolithic Operational Amplifier internally connected as a unity gain non-inverting amplifier. This circuit is ideal for such applications as fast sample and hold circuits, active filters, or as a general purpose buffer. Super-beta transistors are used allowing the devices to operate at very low input currents without sacrificing speed. It may be used to replace conventional op amps such as 101 and the 741 in voltage follower applications, where lower offset voltage, drift, bias current, noise, plus higher speed and a wider operating voltage range is desirable.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION

Fast Integrator With Low-Input Current



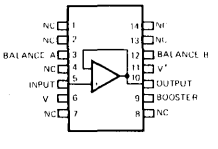
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am302	TO-99	0°C to +70°C	LM302H
	Hermetic DIP	0°C to +70°C	LM302D
	Dice	0°C to +70°C	LD302
Am202	TO-99	−25°C to +85°C	LM202H
	Hermetic DIP	−25°C to +85°C	LM202D
Am102	TO-99	−55°C to +125°C	LM102H
	Hermetic DIP	−55°C to +125°C	LM102D
	Flat Pak	−55°C to +125°C	LM102F
	Dice	−55°C to +125°C	LD102

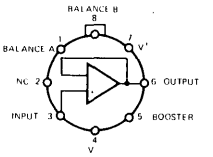
CONNECTION DIAGRAMS

Top Views

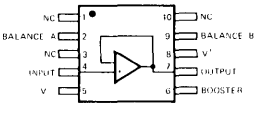
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am102	−55°C to +125°C
Am202	−25°C to + 85°C
Am302	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

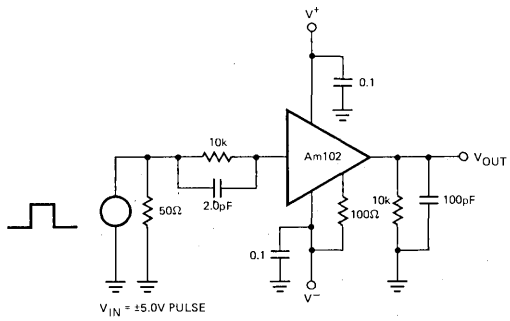
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am302 Min.	Am302 Typ.	Am302 Max.	Am102 Am202 Min.	Am102 Am202 Typ.	Am102 Am202 Max.	Units
Input Offset Voltage			2.5	15		2.0	5.0	mV
Input Bias Current			2.0	30		3.0	10	nA
Input Resistance		10^3	10^6		10^4	10^6		MΩ
Input Capacitance			1.5			1.5		pF
Large-Signal Voltage Gain	R_L = 8.0kΩ, V_{OUT} = ±10V, V_S = ±15V	0.9985	0.9995		0.999	0.9996		V/V
Output Resistance			0.75	2.5		0.8	2.5	Ω
Supply Current			3.9	5.5		3.9	5.5	mA
Slew Rate	V_S = ±15V, V_{IN} = ±10V, R_L = 10kΩ		20			20		V/μs
The Following Specifications Apply Over The Operating Temperature Range								
Input Offset Voltage				10.0			7.5	mV
Input Bias Current				10.0		30	100	nA
Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V, V_S = ±15V	0.9985			0.999			V/V
Output Voltage Swing (Note 5)	R_L = 10kΩ, V_S = ±15V	±10			±10			V
Supply Current	T_A = +125°C					2.0	4.0	mA
Supply Voltage Rejection Ratio	±5.0V ≤ V_S ≤ ±18V	60			70			dB
Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C		20					μV/°C
	−55°C ≤ T_A ≤ +85°C					6.0		μV/°C
	+85°C ≤ T_A ≤ +125°C					12		μV/°C

Notes:
1. Derate Metal Can package 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line at 9.0mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. To prevent damage when the output is shorted, it is necessary to insert a resistor larger than 2.0kΩ in series with the input. Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C for the 102/202. For 302, the corresponding temperatures are +70°C and +55°C respectively.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5.0V to ±18V.
5. Greater output voltage swing can be obtained by connecting a resistor from booster terminal to V−.

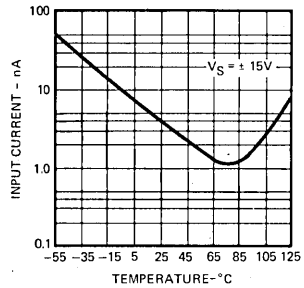
7

AC TEST CIRCUIT

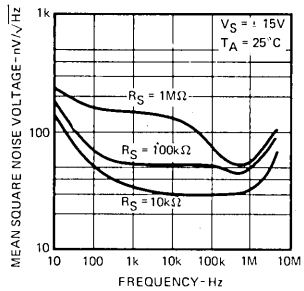


TYPICAL PERFORMANCE CURVES

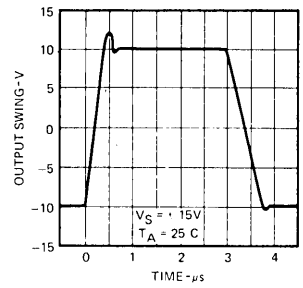
Input Current



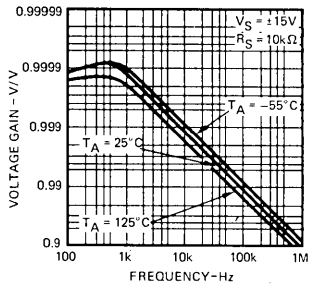
Output Noise Voltage



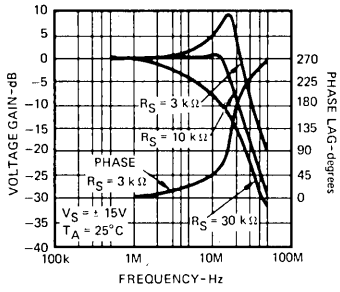
Large Signal Pulse Response



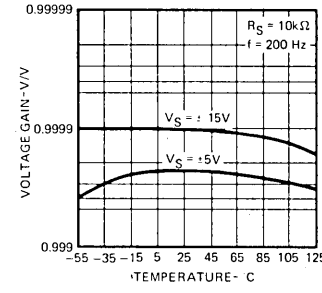
Voltage Gain



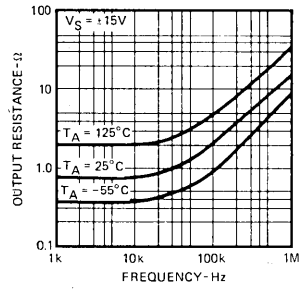
Voltage Gain



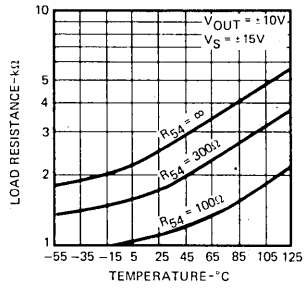
Voltage Gain



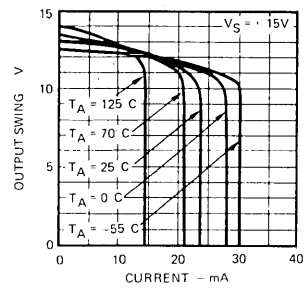
Output Resistance



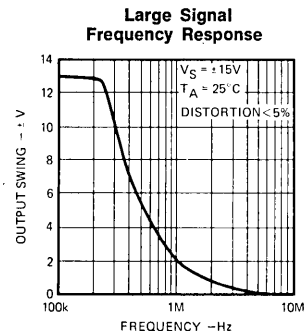
Symmetrical Output Swing



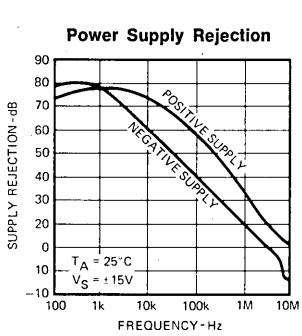
Positive Output Swing



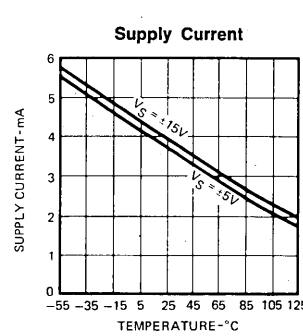
Large Signal Frequency Response



Power Supply Rejection

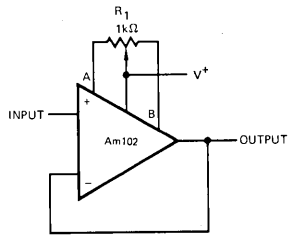


Supply Current

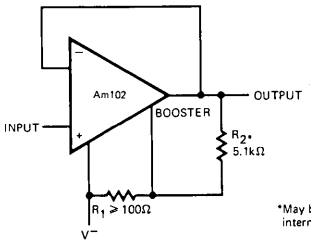


APPLICATIONS

Offset Nulling Circuit

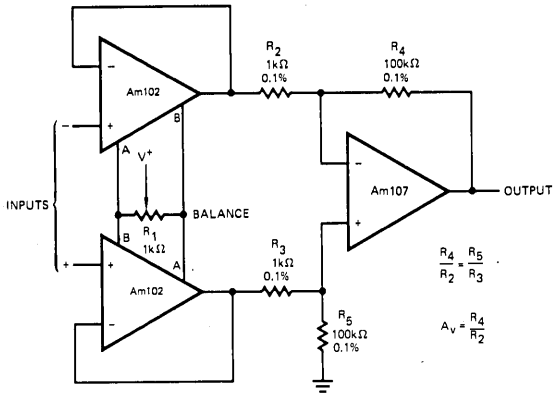


Increasing Negative Swing Under Load

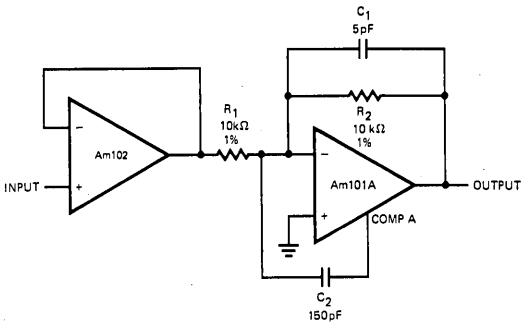


*May be added to reduce internal dissapation.

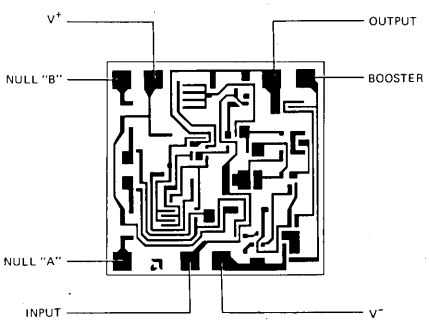
Differential Input Instrumentation Amplifier



Fast Inverting Amplifier With High Input Impedance



Metallization and Pad Layout



40 x 40 Mils

Am107/207/307

Frequency Compensated Operational Amplifier

Description: The Am107/207/307 Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the National LM107/207/307. They are available in the hermetic metal can, flat package, and dual-in-line packages.

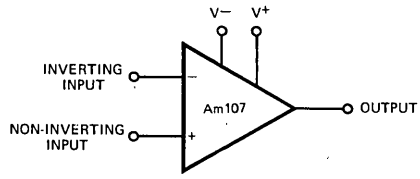
Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

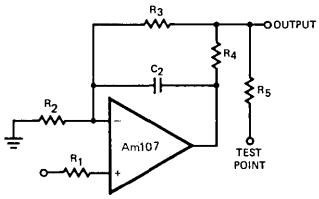
The Am107/207/307 monolithic operational amplifiers are internally frequency compensated and input/output overload protected. These differential input, class AB output amplifiers are intended to provide high accuracy and lower noise in high impedance applications. The Am107/207/307 provide improved electrical parameters and are pin-for-pin replacements for the 709, 101, 101A and 741 in most applications.

FUNCTIONAL DIAGRAM



APPLICATIONS

Input/Output Protection



If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor ($>0.1\mu F$) is equivalent to a low source impedance and should be protected against by an isolation resistor .

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

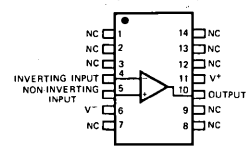
The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high-peak current rating connected to the device supply lines.

ORDERING INFORMATION

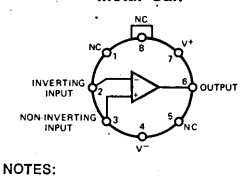
Part Number	Package Type	Temperature Range	Order Number
Am307	DIP	0°C to +70°C	LM307D
	Metal Can	0°C to +70°C	LM307H
	Dice	0°C to +70°C	LD307
Am207	DIP	−25°C to +85°C	LM207D
	Metal Can	−25°C to +85°C	LM207H
	Flat Package	−25°C to +85°C	LM207F
Am107	DIP	−55°C to +125°C	LM107D
	Metal Can	−55°C to +125°C	LM107H
	Flat Package	−55°C to +125°C	LM107F
	Dice	−55°C to +125°C	LD107

CONNECTION DIAGRAMS
Top View

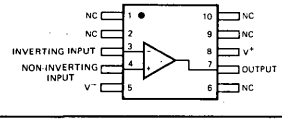
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage Am107, Am207, Am307	 ±22V ±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am107 Am207 Am307	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am307 Min	Am307 Typ	Am307 Max	Am107 Am207 Min	Am107 Am207 Typ	Am107 Am207 Max	Units
Input Offset Voltage	$R_S \leq 50\ k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$ $V_S = \pm 15V$		1.8	3.0		1.8	3.0	mA mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	25	160		50	160		V/mV
Slew Rate	$R_L \geq 2\ k\Omega$	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50\ k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A\ (max)}$ $T_{A\ (min)} \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	25			25			V/mV
Input Voltage Range	$V_S = \pm 20\ V$ $V_S = \pm 15\ V$	 +15, −12			±15			V V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $R_L = 2\ k\Omega$,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C$ $V_S = \pm 20\ V$					1.2	2.5	mA

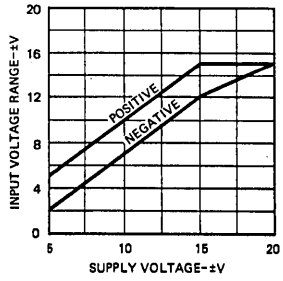
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the Am107 and Am207 and from ±5 V to ±15 V for the Am307.

7

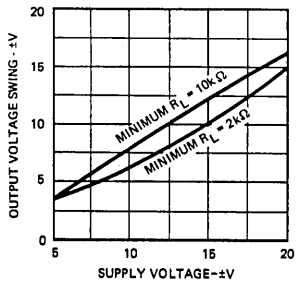
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

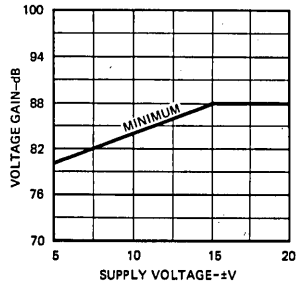
Input Voltage Range



Output Swing

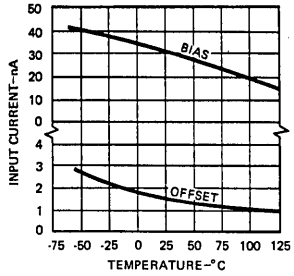


Voltage Gain

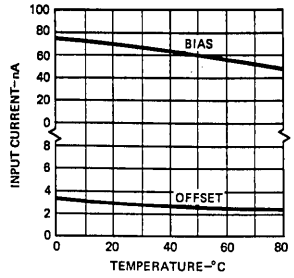


PERFORMANCE CURVES (Note 3)

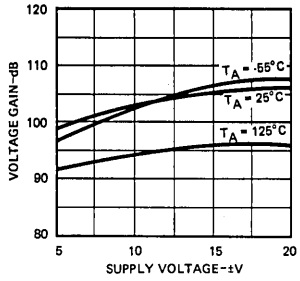
Input Current—Am107, Am207



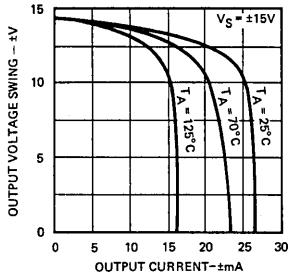
Input Current—Am307



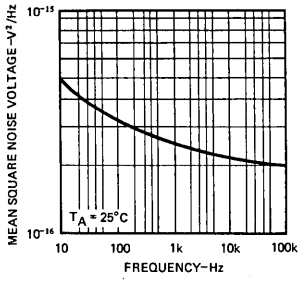
Voltage Gain



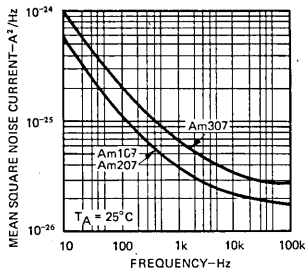
Current Limiting



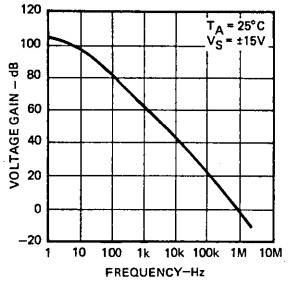
Input Noise Voltage



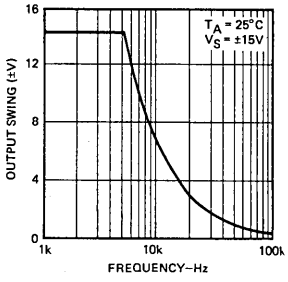
Input Noise Current



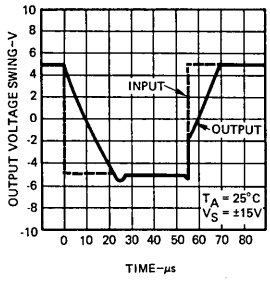
Open Loop Frequency Response



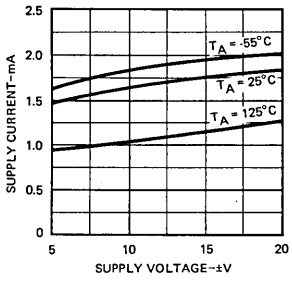
Large Signal Frequency Response



Voltage Follower Pulse Response

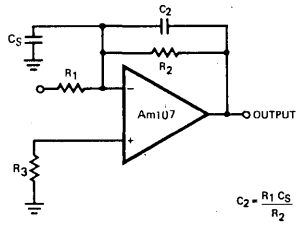


Supply Current

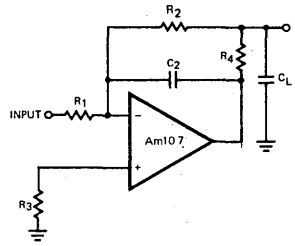


ADDITIONAL APPLICATION INFORMATION

Stray Input Capacitance/Large Feedback Resistance

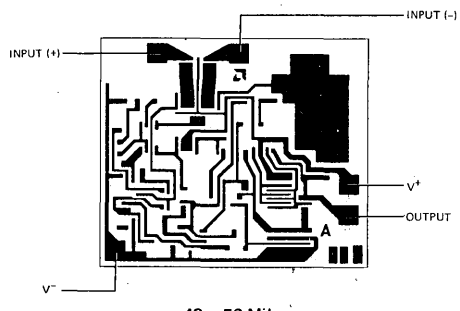


Large Capacitive Loads



Stability is guaranteed for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF, and capacitive loads smaller than 100 pF. If any of these conditions is not met, lead capacitors may be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads. Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card.

Metallization and Pad Layout



49 x 56 Mils

Am108/208/308•Am108A/208A/308A

Operational Amplifiers

Description: The 108, 208, 308, 108A, 208A and 308A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalents to the National LM108, LM208, LM308, LM108A, LM208A and LM308A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

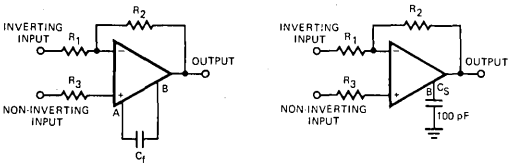
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

These differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor and are pin-for-pin interchangeable with the 101A/201A/301A. The 108A, 208A, and 308A are high performance selections from the 108/208/308 amplifier family.

FUNCTIONAL DIAGRAM

Frequency Compensation Circuits

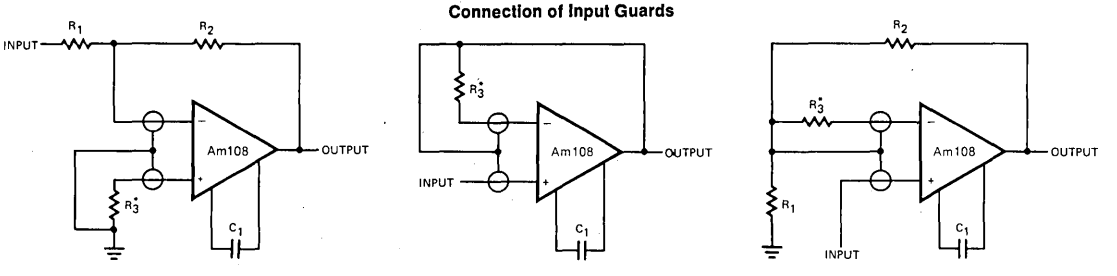


$$C_f \geq C_o\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

C_o = 30 pF

APPLICATIONS

Connection of Input Guards



* Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

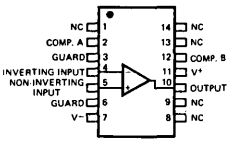
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am308	Hermetic DIP	0°C to +70°C	LM308D
	TO-99	0°C to +70°C	LM308H
	Molded DIP	0°C to +70°C	LM308N
	Dice	0°C to +70°C	LD308
Am308A	Hermetic DIP	0°C to +70°C	LM308AD
	TO-99	0°C to +70°C	LM308AH
	Molded DIP	0°C to +70°C	LM308AN
	Dice	0°C to +70°C	LD308A
Am208	Hermetic DIP	-25°C to +85°C	LM208D
	TO-99	-25°C to +85°C	LM208H
Am208A	Hermetic DIP	-25°C to +85°C	LM208AD
	TO-99	-25°C to +85°C	LM208AH
Am108	Hermetic DIP	-55°C to +125°C	LM108D
	TO-99	-55°C to +125°C	LM108H
	Dice	-55°C to +125°C	LD108
Am108A	Hermetic DIP	-55°C to +125°C	LM108AD
	TO-99	-55°C to +125°C	LM108AH
	Dice	-55°C to +125°C	LD108A

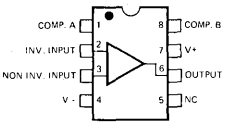
CONNECTION DIAGRAMS

Top Views

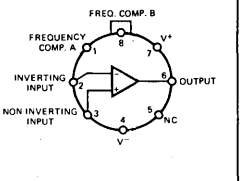
Dual-In-Line



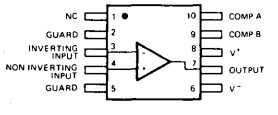
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 7 is connected to bottom of package.

(3) On Flat Package, pin 6 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage Am108, 208, 108A, 208A, Am308, 308A	 ±20 V ±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am108, 108A Am208, 208A Am308, 308A	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

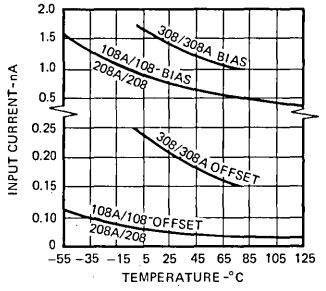
Parameter (see definitions)	Conditions	Am308 Min.	Am308 Typ.	Am308 Max.	Am308A Min.	Am308A Typ.	Am308A Max.	Am108 Am208 Min.	Am108 Am208 Typ.	Am108 Am208 Max.	Am108A Am208A Min.	Am108A Am208A Typ.	Am108A Am208A Max.	Units
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20 V V_S = ±15 V		0.3	0.8		0.3	0.8		0.3	0.6		0.3	0.6	mA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq 10$ kΩ	25	300		80	300		50	300		80	300		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq 10$ kΩ	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15 V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ,	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	V_S = ±20 V V_S = ±15 V		0.6	1.0		0.6	0.8		0.15	0.4		0.15	0.4	mA

Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the 108, 208, 108A and 208A and from ±5 V to ±15 V for the 308 and 308A.

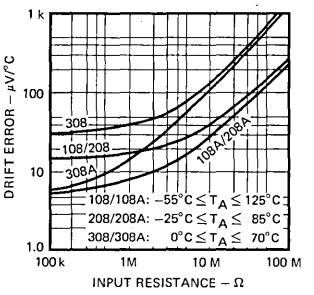
7

TYPICAL PERFORMANCE CURVES

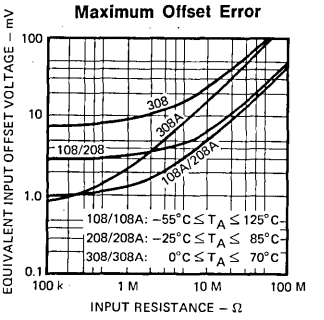
Input Currents



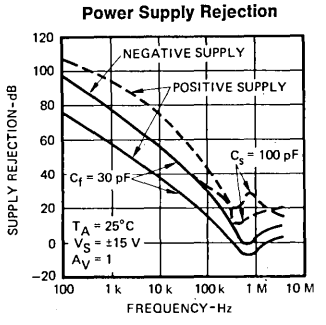
Maximum Drift Error



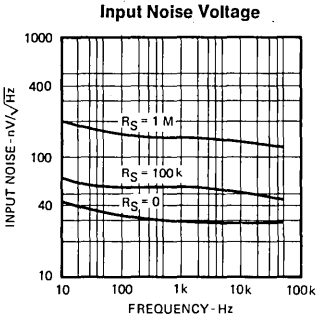
Maximum Offset Error



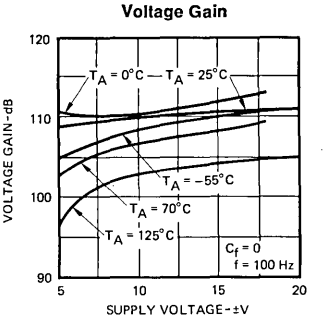
Power Supply Rejection



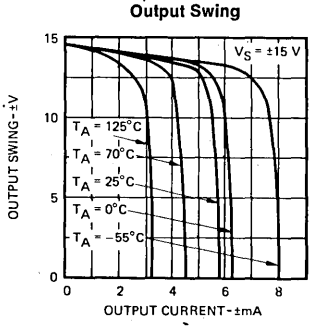
Input Noise Voltage



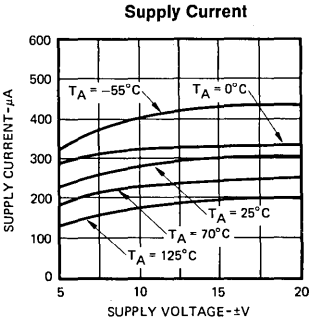
Voltage Gain



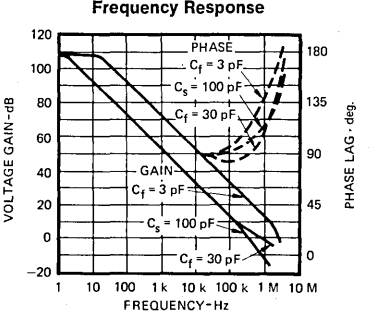
Output Swing



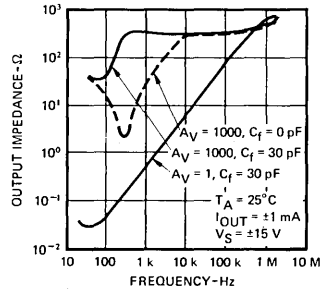
Supply Current



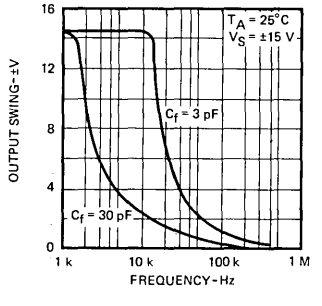
Open Loop Frequency Response



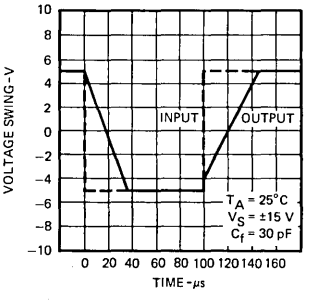
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



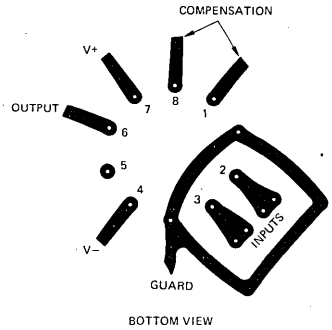
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

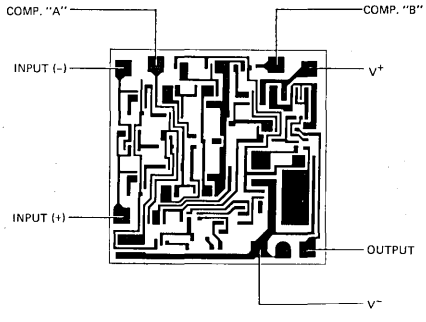
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



Board layout for Input Guarding with TO-99 package.

7

Metallization and Pad Layout



56 x 56 Mils

Am110/210/310

Voltage Follower

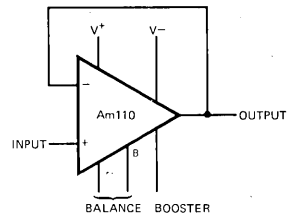
Distinctive Characteristics

- The Am110/210/310 are functionally, electrically, and pin-for-pin equivalent to the National LM 110/210/310
- Slew rate: 30V/μs
- Small signal bandwidth: 20 MHz
- Input current: 10 nA max. over temperature
- Supply voltage range: ±5V to ±18V
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

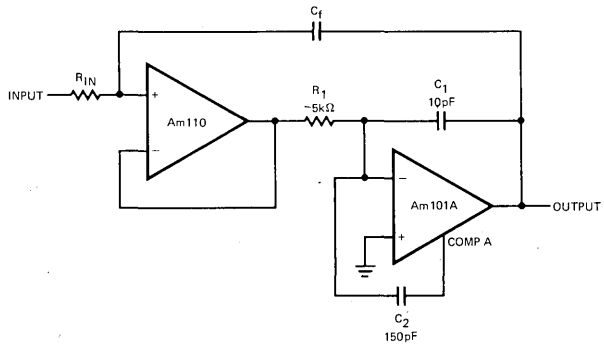
The Am110/210/310 are voltage followers featuring high-speed, low-input currents and large input voltage range. They are internally compensated with provision for external offset adjustment. Operation over wide supply voltages and temperature is possible.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION

Fast Integrator With Low-Input Current



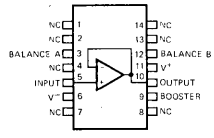
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am310	TO-99	0°C to +70°C	LM310H
	DIP	0°C to +70°C	LM310D
	Flat Package	0°C to +70°C	LM310F
	Molded DIP	0°C to +70°C	LM310N
	Dice	0°C to +70°C	LD310
Am210	TO-99	−25°C to +85°C	LM210H
	DIP	−25°C to +85°C	LM210D
	Flat Pak	−25°C to +85°C	LM210F
Am110	TO-99	−55°C to +125°C	LM110H
	DIP	−55°C to +125°C	LM110D
	Flat Package	−55°C to +125°C	LM110F
	Dice	−55°C to +125°C	LD110

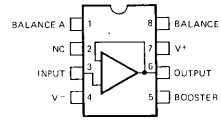
CONNECTION DIAGRAMS

Top Views

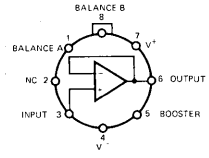
Dual-In-Line



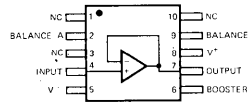
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage		±18 V
Internal Power Dissipation (Note 1)		500 mW
Input Voltage (Note 2)		±15 V
Output Short-Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	Am110	−55°C to +125°C
	Am210	−25°C to +85°C
	Am310	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 60 sec)		300°C

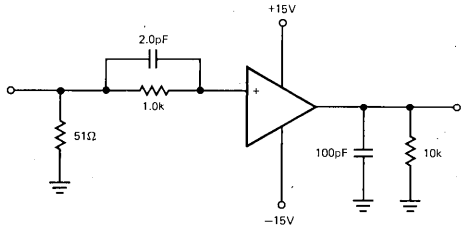
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am310 Min	Am310 Typ	Am310 Max	Am110 Am210 Min	Am110 Am210 Typ	Am110 Am210 Max	Units
Input Offset Voltage			2.5	7.5		1.5	4.0	mV
Input Bias Current			2.0	7.0		1.0	3.0	nA
Input Resistance		10^4	10^6		10^4	10^6		MΩ
Input Capacitance			1.5			1.5		pF
Large-Signal Voltage Gain	$R_L = 8\ k\Omega$, $V_{out} = \pm 10\ V$, $V_S = \pm 15\ V$	0.999	0.9999		0.999	0.9999		V/V
Output Resistance			0.75	2.5		0.75	2.5	Ω
Supply Current			3.9	5.5		3.9	5.5	mA
Slew Rate	$V_S = \pm 15\ V$, $V_{IN} = \pm 10\ V$, $R_L = 10\ k\Omega$		30		20	30		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage				10.0			6.0	mV
Input Bias Current				10.0			10.0	nA
Large-Signal Voltage Gain	$R_L = 10\ k\Omega$, $V_{out} = \pm 10\ V$, $V_S = \pm 15\ V$	0.999			0.999			V/V
Output Voltage Swing (Note 5)	$R_L = 10\ k\Omega$, $V_S = \pm 15\ V$	±10			±10			V
Supply Current	$T_A = +125°C$					2.0	4.0	mA
Supply Voltage Rejection Ratio	$\pm 5\ V \leq V_S \leq \pm 18\ V$	70			70			dB
Average Temperature Coefficient of Input Offset Voltage	$0° \leq T_A \leq 70°C$		10					μV/°C
	$-55°C \leq T_A \leq 85°C$ $+85°C \leq T_A \leq 125°C$					6 12		μV/°C

Notes:
1. Derate Metal Can package 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. To prevent damage when the output is shorted, it is necessary to insert a resistor larger than 2 kΩ in series with the input. Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C for the 110/210. For 310, the corresponding temperatures are 70°C and 55°C respectively.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 to ±18 V.
5. Greater output voltage swing can be obtained by connecting a resistor from booster terminal to V−.

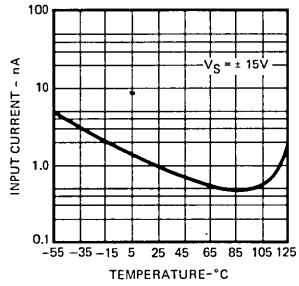
7

AC TEST CIRCUIT

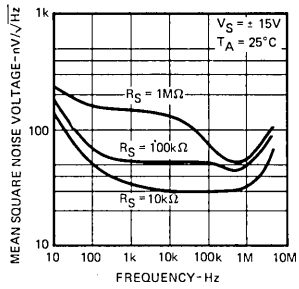


PERFORMANCE CURVES

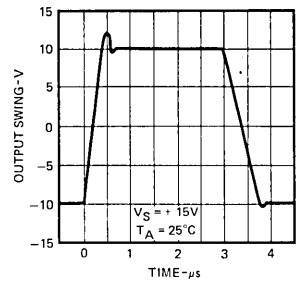
Input Current



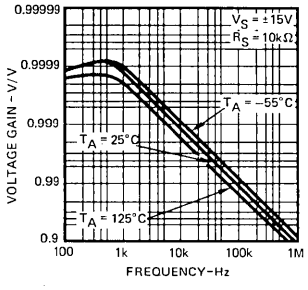
Output Noise Voltage



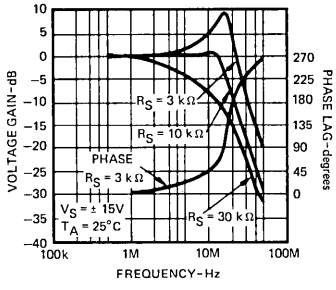
Large Signal Pulse Response



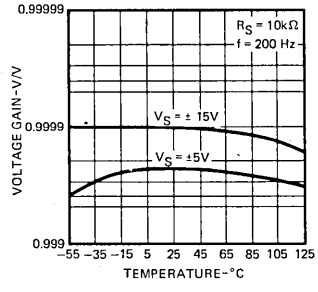
Voltage Gain



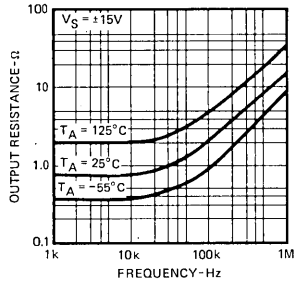
Voltage Gain



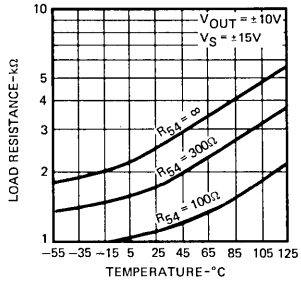
Voltage Gain



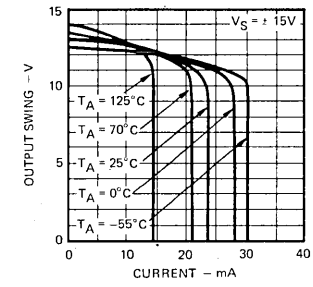
Output Resistance



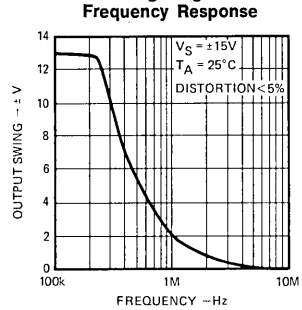
Symmetrical Output Swing



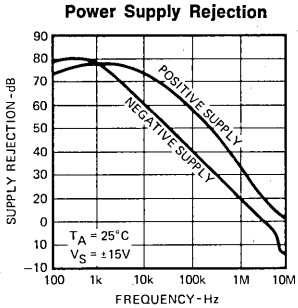
Positive Output Swing



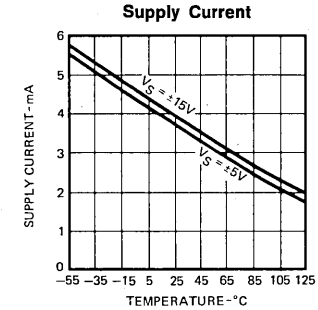
Large Signal Frequency Response



Power Supply Rejection

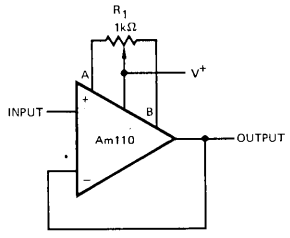


Supply Current

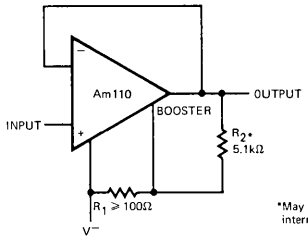


APPLICATIONS

Offset Nulling Circuit

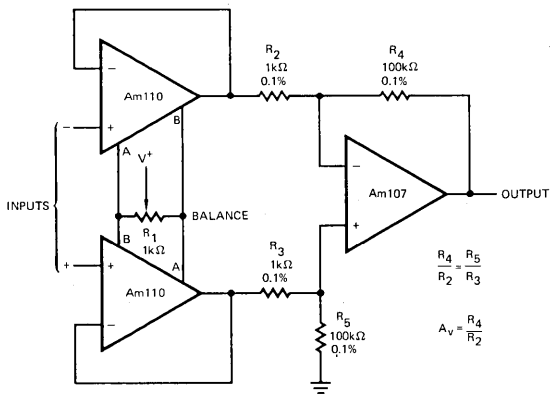


Increasing Negative Swing Under Load

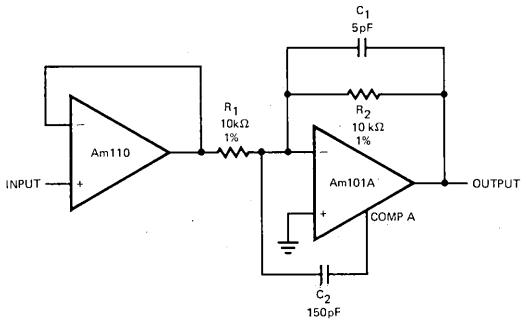


*May be added to reduce internal dissapation.

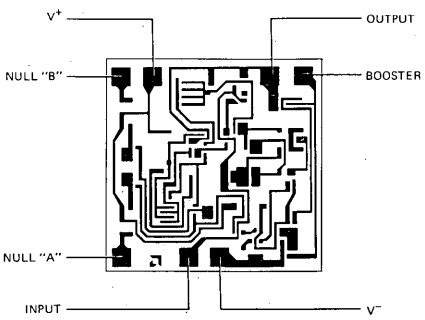
Differential Input Instrumentation Amplifier



Fast Inverting Amplifier With High Input Impedance



Metallization and Pad Layout



40 x 40 Mils

Am112/212/312

Compensated, High-Performance Operational Amplifier

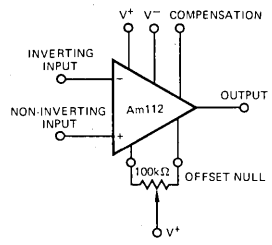
Distinctive Characteristics

- The Am112/212/312 are functionally, electrically, and pin-for-pin equivalents to the National LM112/212/312.
- Low input bias currents: 800pA
- Low input offset currents: 50pA
- Low power consumption: 3mW
- Internal frequency compensation.
- Offset nulling provisions.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

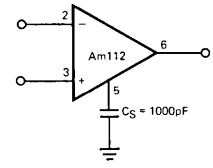
FUNCTIONAL DESCRIPTION

The Am112/212/312 are compensated high-performance operational amplifiers featuring very low offset voltage and input current errors competitive with FET and chopper-stabilized amplifiers. The devices will operate over a supply voltage range of ±2V to ±20V, drawing a typical quiescent current of only 300μA. The Am112/212/312 are internally frequency compensated and provision is made for offset adjustment with a single potentiometer. Overcompensation providing a greater stability margin is possible and the internal protection of the MOS capacitor makes it immune to overvoltage transients.

FUNCTIONAL DIAGRAM

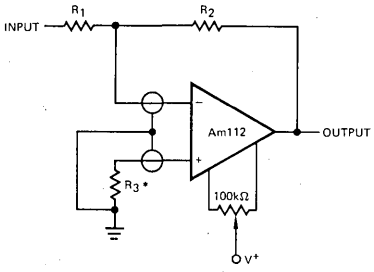


Overcompensation for Greater Stability Margin

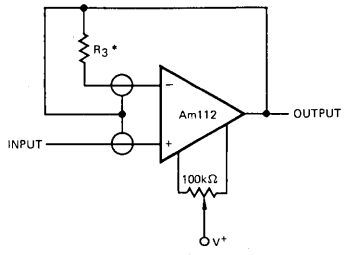


TYPICAL APPLICATIONS

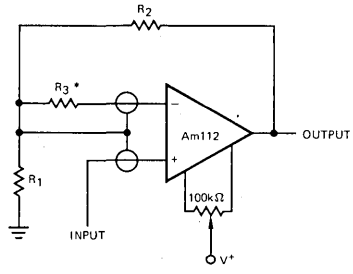
Connection of input guards and offset null



INVERTING AMPLIFIER



FOLLOWER



NON-INVERTING AMPLIFIER

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

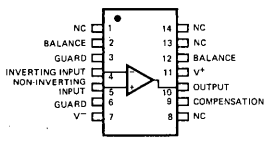
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am312	DIP	0°C to +70°C	LM312D
	Metal Can	0°C to +70°C	LM312H
	Dice	0°C to +70°C	LD312
Am212	DIP	−25°C to +85°C	LM212D
	Metal Can	−25°C to +85°C	LM212
	Flat Pak	−25°C to +85°C	LM212F
AM112	DIP	−55°C to +125°C	LM112D
	Metal Can	−55°C to +125°C	LM112
	Flat Pak	−55°C to +125°C	LM112F
	Dice	−55°C to +125°C	LD112

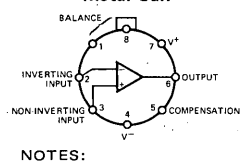
CONNECTION DIAGRAMS

Top Views

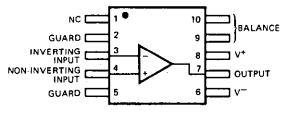
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On metal can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On flat package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

MAXIMUM RATINGS

Supply Voltage	
Am112, 212	±20V
Am312	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am112	−55°C to +125°C
Am212	−25°C to +85°C
Am312	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

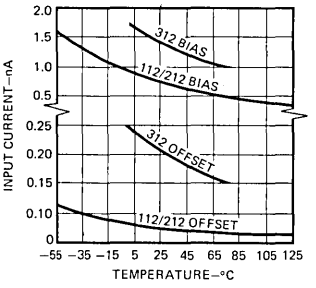
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am312 Min.	Am312 Max.	Am112 Am212 Min.	Am112 Am212 Max.	Units
Input Offset Voltage			7.5		2.0	mV
Input Offset Current			1		0.2	nA
Input Bias Current			7		2.0	nA
Input Resistance		10		30		MΩ
Supply Current			0.8		0.6	mA
Large Signal Voltage Gain	V_{OUT} = ±10V, V_S = ±15V R_L > 10kΩ	25		50		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges						
Input Offset Voltage			10		3.0	mV
Average Temperature Coefficient of Input Offset Voltage			30		15	μV/°C
Input Offset Current			1.5		0.4	nA
Average Temperature Coefficient of Input Offset Current			10		2.5	pA/°C
Input Bias Current			10		3.0	nA
Supply Current	T_A = +125°C				0.4	mA
Large Signal Voltage Gain	V_{OUT} = ±10V, V_S = ±15V R_L > 10kΩ	15		25		V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13		±13		V
Input Voltage Range	V_S = ±15V	±13.5		±13.5		V
Common Mode Rejection Ratio		80		85		dB
Supply Voltage Rejection Ratio		80		80		dB

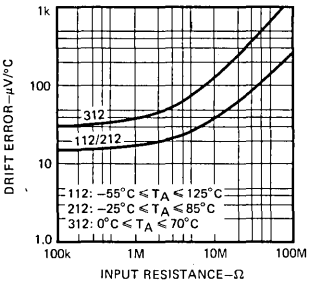
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the Am112, Am212 and from ±5 V to ±15 V for the Am312.

TYPICAL PERFORMANCE CURVES

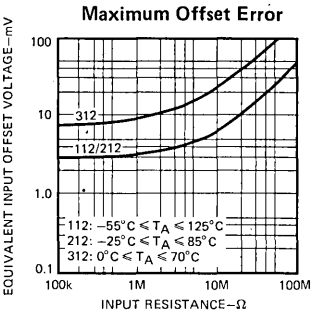
Input Currents



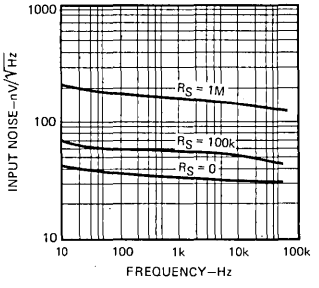
Maximum Drift Error



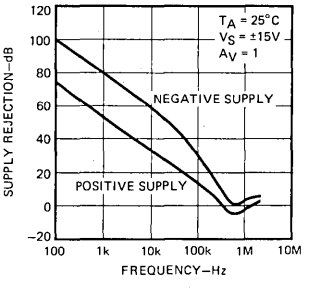
Maximum Offset Error



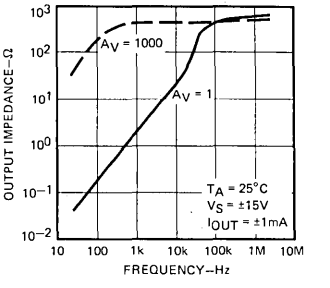
Input Noise Voltage



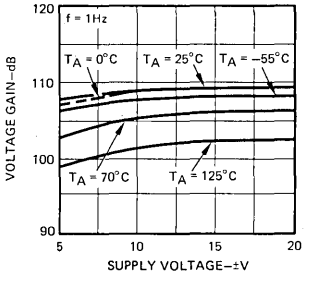
Power Supply Rejection



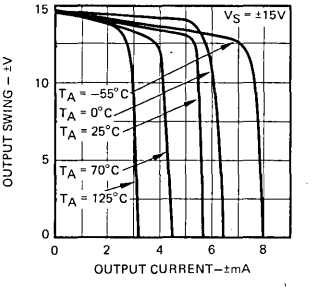
Closed Loop Output Impedance



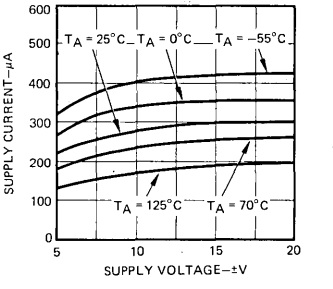
Voltage Gain



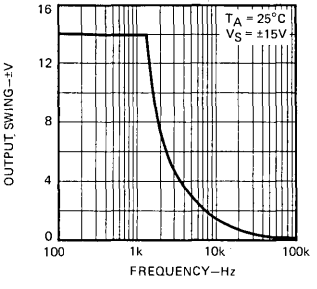
Output Swing



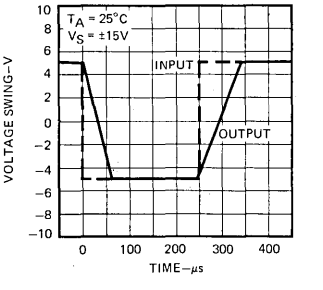
Supply Current



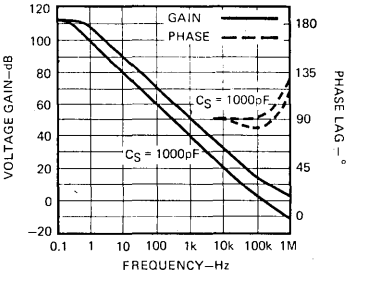
Large Signal Frequency Response



Voltage Follower Pulse Response



Open Loop Frequency Response



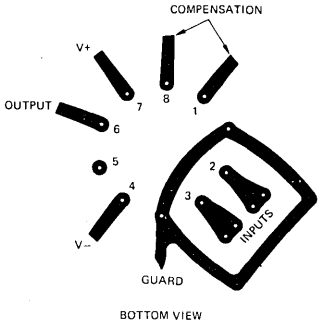
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 112 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

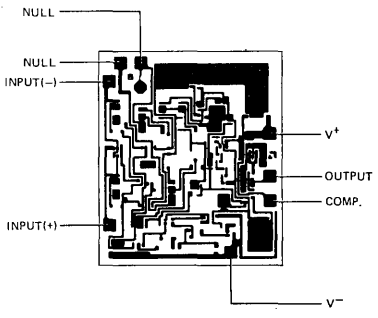
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard Am741 and Am101A pin configuration.)



Note: Board layout for input Guarding with TO-99 package.

7

Metallization and Pad Layout



62 x 72 Mils

Am118/218/318

High-Speed Operational Amplifier

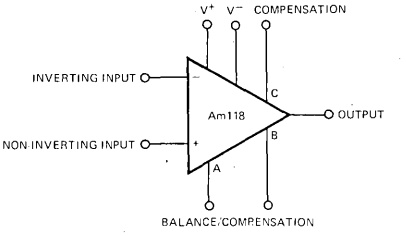
Distinctive Characteristics

- The Am118/218/318 are functionally, electrically, and pin-for-pin equivalent to the National LM118/218/318
- Slew rate: 70V/μs
- Small signal bandwidth: 15MHz
- Internal frequency compensation
- Supply voltage range: ±5V to ±20V
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line, hermetic flat package or plastic minidip.

FUNCTIONAL DESCRIPTION

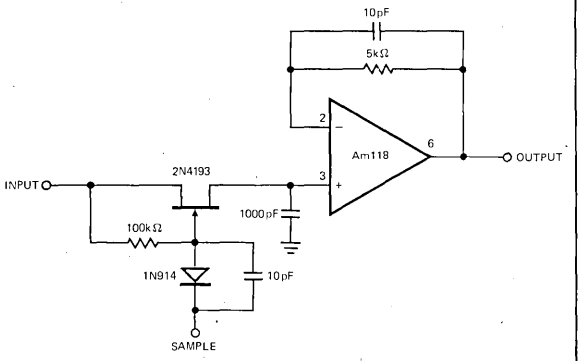
The Am118/218/318 are internally compensated high-speed operational amplifiers featuring minimum slew rate of 50V/μs, low input bias currents, large input voltage range and excellent performance over a wide range of supply voltages and temperature. They have provision for increased speeds when operating in the inverting mode.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS

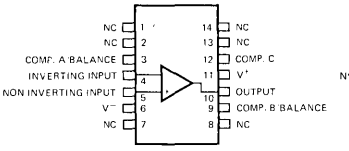
Fast Sample and Hold



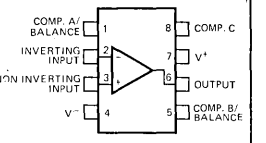
CONNECTION DIAGRAMS

Top Views

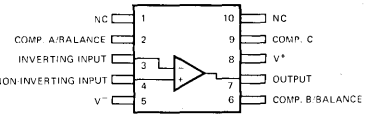
Dual-In-Line



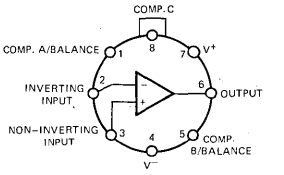
Dual-In-Line



Flat Package



Metal Can



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am318	Metal Can	0°C to +70°C	LM318H
	DIP	0°C to +70°C	LM318D
	Flat Package	0°C to +70°C	LM318F
	Molded DIP	0°C to +70°C	LM318N
	Dice	0°C to +70°C	LD318
Am218	Metal Can	−25°C to +85°C	LM218H
	DIP	−25°C to +85°C	LM218D
	Flat Pak	−25°C to +85°C	LM218F
Am118	Metal Can	−55°C to +125°C	LM118H
	DIP	−55°C to +125°C	LM118D
	Flat Package	−55°C to +125°C	LM118F
	Dice	−55°C to +125°C	LD118

Notes: 1. On Metal Can, pin 4 is connected to case.
2. On DIP, pin 6 is connected to bottom of package.
3. On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage (Note 2)	±5V
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am118	−55°C to +125°C
Am218	−25°C to +85°C
Am318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

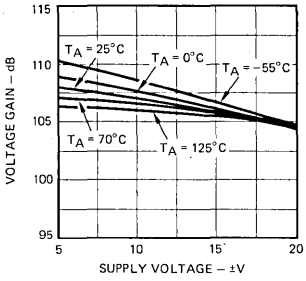
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am318 Min.	Am318 Typ.	Am318 Max.	Am118 Am218 Min.	Am118 Am218 Typ.	Am118 Am218 Max.	Units
Input Offset Voltage	$R_S \leq 5k\Omega$		4	10		2	4	mV
Input Offset Current			30	200		6	50	nA
Input Bias Current			150	500		120	250	nA
Input Resistance		0.5	3		1.0	3		MΩ
Supply Current	V_S = ±20V		5	10		5	8	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	25	200		50	200		V/mV
Slew Rate	A_V = +1, V_S = ±15V (Fig.1) R_L = 2kΩ, C_L = 30pF	50	70		50	70		V/μs
Small Signal Bandwidth	V_S = ±15V		15			15		MHz
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 5k\Omega$			15			6	mV
Input Offset Current				300			100	nA
Input Bias Current				750			500	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	20			25			V/mV
Input Voltage Range	V_S = ±15V	±11.5			±11.5			V
Common Mode Rejection Ratio	$R_S \leq 5k\Omega$	70			80			dB
Supply Voltage Rejection Ratio	$R_S \leq 5k\Omega$	65			70			dB
Output Voltage Swing	V_S = ±15V, R_L = 2kΩ	±12	±13		±12	±13		V
Supply Current	V_S = ±20V, T_A = 125°C						7	mA

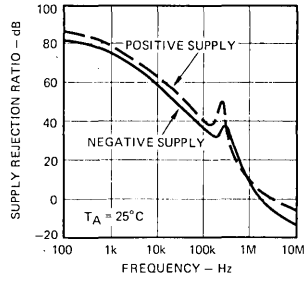
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with diodes for overvoltage protection. To limit the current in the protection diodes, resistances of 2 kΩ or greater should be inserted in series with the input leads for differential input voltages greater than ±5 V.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V.

PERFORMANCE CURVES

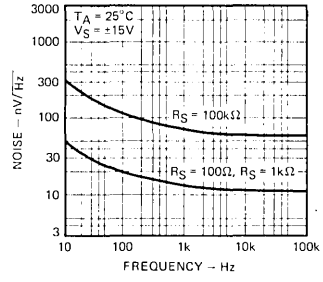
Voltage Gain



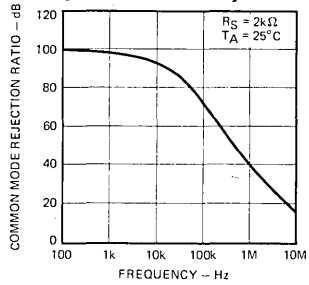
Power Supply Rejection



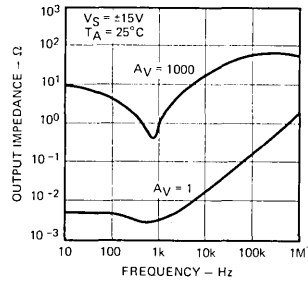
Input Noise Voltage



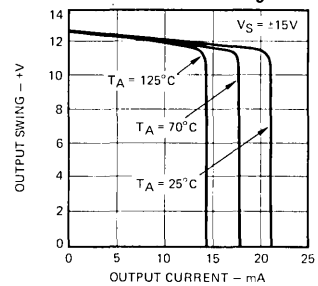
Common Mode Rejection



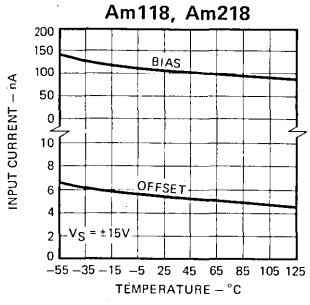
Closed Loop Output Impedance



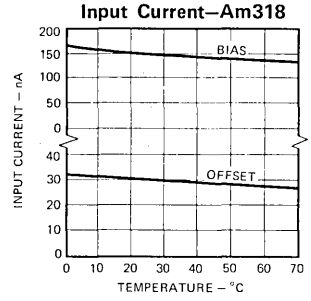
Current Limiting



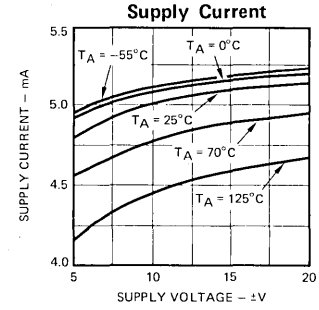
Input Current Am118, Am218



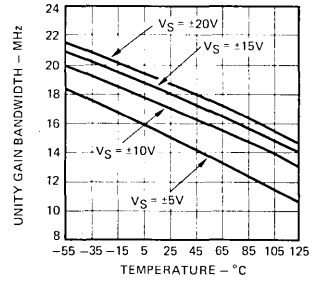
Input Current–Am318



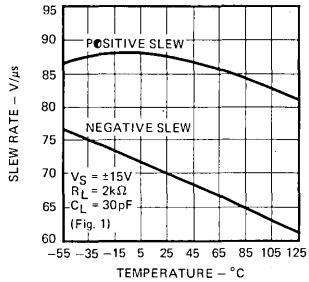
Supply Current



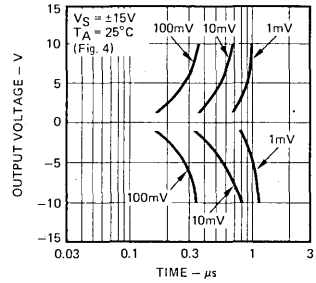
Unity Gain Bandwidth



Voltage Follower Slew Rate

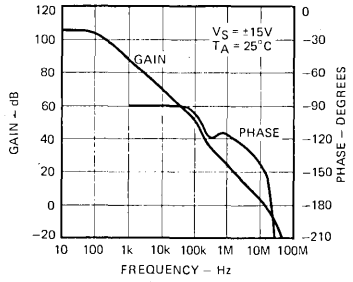


Inverter Settling Time

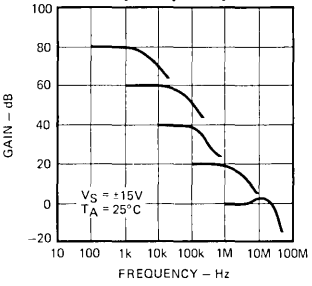


PERFORMANCE CURVES

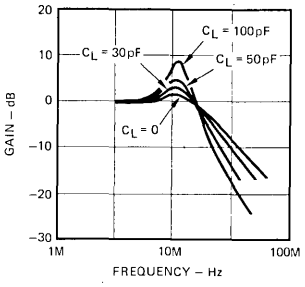
Open Loop Frequency Response



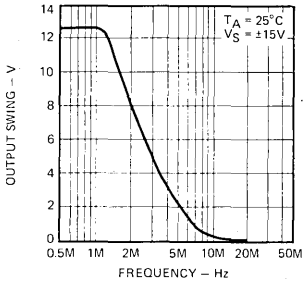
Closed Loop Frequency Response



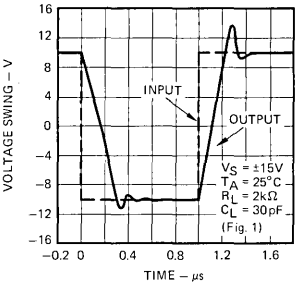
Effect of Capacitive Loading on Closed Loop Frequency Response



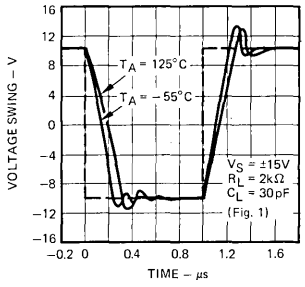
Large Signal Frequency Response



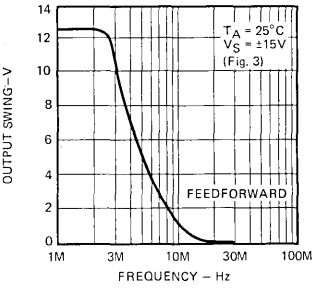
Voltage Follower Pulse Response



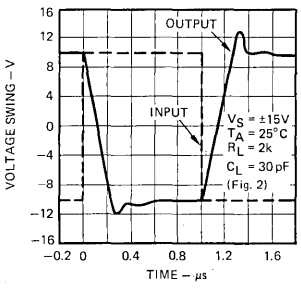
Voltage Follower Pulse Response Over Temperature



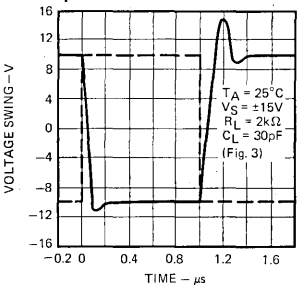
Large Signal Frequency Response with Feedforward



Inverter Pulse Response without Feedforward



Inverter Pulse Response with Feedforward



The high gain and large bandwidth of the Am118 make it mandatory to observe the following precautions in using the device, as is the case with any high-frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to minimum, or the amplifier must be isolated as shown in the applications.

APPLICATIONS

Voltage Follower (Slew Rate Test Circuit)

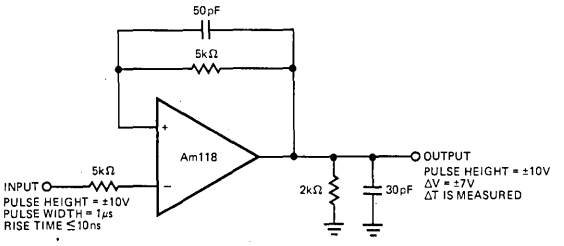


Figure 1

Inverter

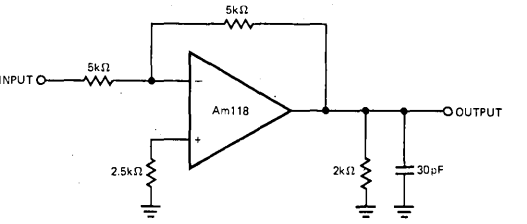


Figure 2

Inverter with Feedforward Compensation for Higher Slew Rate

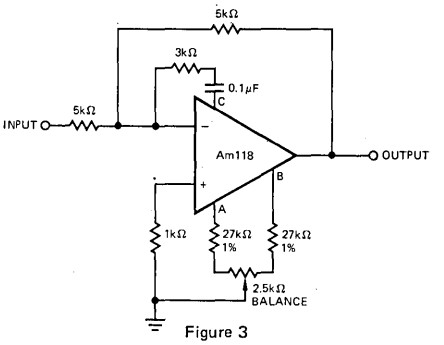


Figure 3

Compensation for Minimum Settling Time

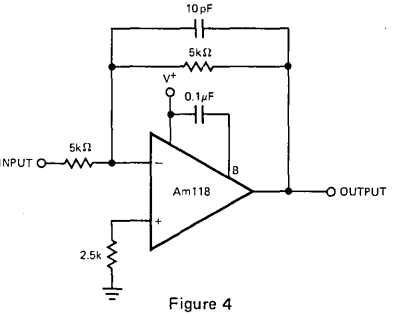


Figure 4

Offset Nulling

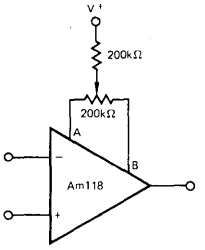


Figure 5

Isolating Large Capacitive Loads

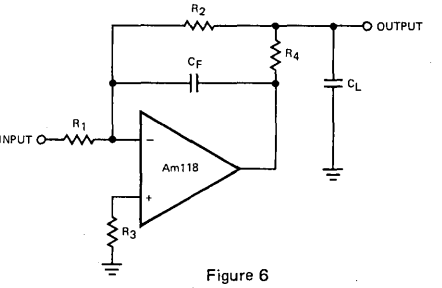


Figure 6

Over Compensation

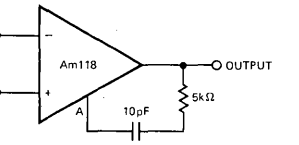


Figure 7

D/A Converter with Ladder Network

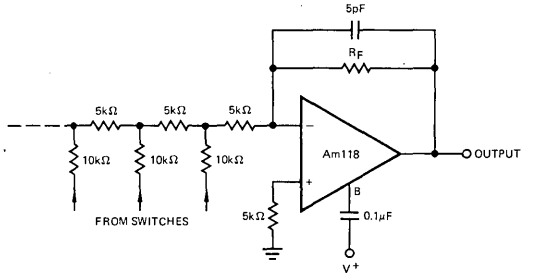


Figure 8

D/A Converter with Binary Network

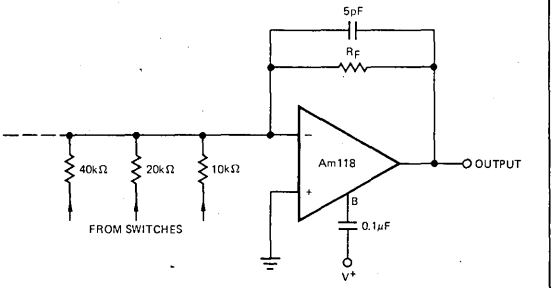


Figure 9

ADDITIONAL APPLICATIONS

High Speed Summing Amplifier with Low Input Bias Currents

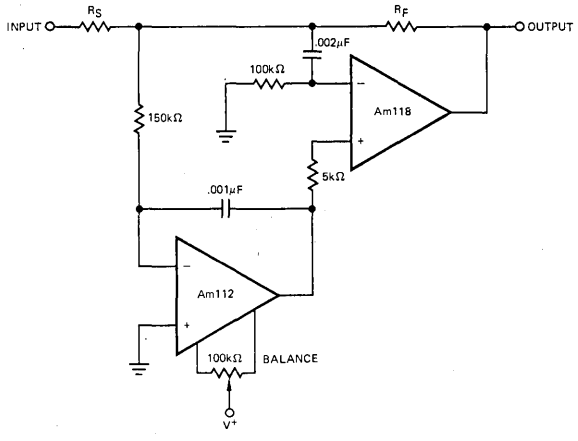
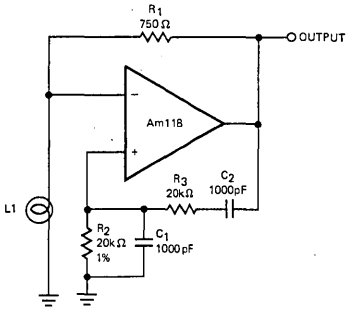


Figure 10

Wien Bridge Oscillator

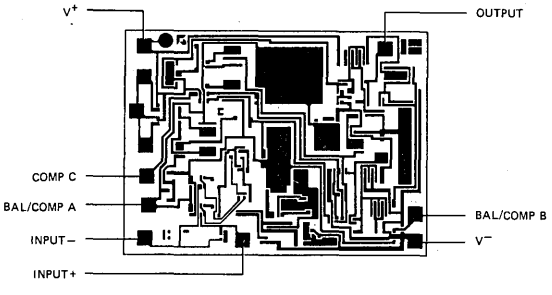


L1–10V–14mA
bulb ELDEMA 1869
$R1 = R_2$
$C_1 = C_2$

$$f = \frac{1}{2\pi R1C1}$$

Figure 11

Metallization and Pad Layout



64 X 86 Mils

Am124/224/324
Am124A/224A/324A

Quad Op Amps

Distinctive Characteristics

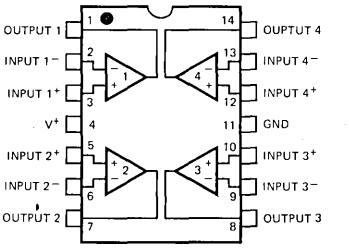
- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated
- Internally frequency compensated for unity gain
- Large dc voltage gain – 100dB
- Wide bandwidth (unity gain) – 1MHz (temperature compensated)
- Wide power supply range:
  Single supply – 3V to 30V
  Dual supplies – ±1.5V to ±15V
- Very low supply current drain (800μA) – essentially independent of supply voltage (1mW/op amp at +5V)
- Low input biasing current – 45nA (temperature compensated)
- Low input offset voltage – 2mV and offset current – 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing – 0V to V^+ –1.5V

FUNCTIONAL DESCRIPTION

The Am124 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed primarily to operate from a single power supply over a wide range of voltages. These devices can also operate from split power supplies and the low power supply current drain is independent of the magnitude of the power supply voltage.

Functional applications consist of all the conventional op amp circuits which can now be more easily implemented in single power supply systems along with transducer amplifiers and dc gain blocks.

CONNECTION DIAGRAM
Top View

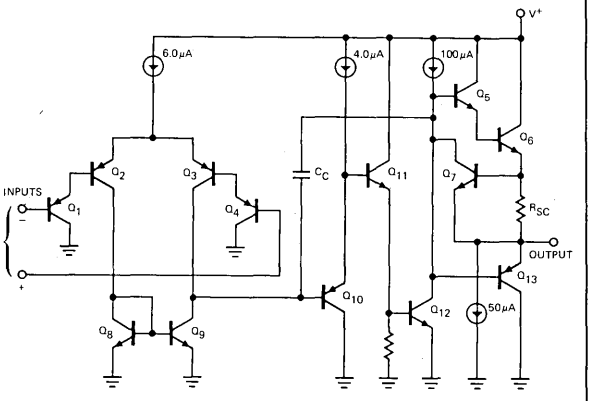


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am324	Hermetic DIP	0°C to +70°C	LM324D
	Molded DIP	0°C to +70°C	LM324N
	Dice	0°C to +70°C	LD324
Am224	Hermetic DIP	–25°C to +85°C	LM224D
Am124	Hermetic DIP	–55°C to +125°C	LM124D
	Flat Pack	–55°C to +125°C	LM124F
	Dice	–55°C to +125°C	LM124
Am324A	Hermetic DIP	0°C to +70°C	LM324AD
	Molded DIP	0°C to +70°C	LM324AN
	Dice	0°C to +70°C	LM324A
Am224A	Hermetic DIP	–25°C to +85°C	LM224AD
Am124A	Hermetic DIP	–55°C to +125°C	LM124AD
	Flat Pack	–55°C to +125°C	LM124AF
	Dice	–55°C to +125°C	LD124A

SCHEMATIC DIAGRAM (Each Amplifier)



ELECTRICAL CHARACTERISTICS ($V^+ = +5.0\,V_{DC}$, Note 4)

Parameter		Conditions	Am124A			Am224A			Am324A			Am124/Am224			Am324			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage		$T_A = 25°C$ (Note 5)		1.0	2.0		1.0	3.0		2.0	3.0		±2.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current (Note 6)		$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250	nA_{DC}
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2.0	10		2.0	15		5.0	30		±3.0	±30		±5.0	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)		$V^+ = 30\,V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current		$R_L = \infty$, $V_{CC} = 30\,V$		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0	mA_{DC}
		$R_L = \infty$		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain		$V^+ = 15\,V_{DC}$ (For large V_O swing) $R_L \geq 2.0k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		V/mV
Output Voltage Swing		$R_L = 2.0k\Omega$, $T_A = 25°C$										0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio		DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		dB
Power Supply Rejection Ratio		DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		dB
Amplifier to Amplifier Coupling (Note 8)		f = 1.0kHz to 20kHz, $T_A = 25°C$ (Input referred)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN+} = 1.0\,V_{DC}$, $V_{IN-} = 0\,V_{DC}$, $V^+ = 15\,V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA_{DC}
	Sink	$V_{IN-} = 1.0\,V_{DC}$, $V_{IN+} = 0\,V_{DC}$, $V^+ = 15\,V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		
		$V_{IN-} = 1.0\,V_{DC}$, $V_{IN+} = 0\,V_{DC}$, $T_A = 25°C$, $V_O = 200\,mV_{DC}$	12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground		$T_A = 25°C$ (Note 2)		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage		Note 5			4.0			4.0			5.0			±7.0			±9.0	mV_{DC}
Input Offset Voltage Drift		$R_S = 0\Omega$		7.0	20		7.0	20		7.0	30		7.0		7.0			$\mu V/°C$
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150	nA_{DC}
Input Offset Current Drift				10	200		10	200		10	300		10			10		$pA_{DC}/°C$
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)		$V^+ = 30\,V_{DC}$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Large Signal Voltage Gain		$V^+ = +15\,V_{DC}$ (For large V_O swing) $R_L \geq 2.0k\Omega$	25			25			15			25			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30\,V_{DC}$, $R_L = 2.0k\Omega$	26			26			26			26			26			V_{DC}
		$R_L \geq 10k\Omega$	27	28		27	28		27	28		27	28		27	28		
	V_{OL}	$V^+ = 5.0\,V_{DC}$, $R_L \leq 10k\Omega$		5.0	20		5.0	20		5.0	20		5.0	20		5.0	20	mV_{DC}
Output Current	Source	$V_{IN+} = 1.0\,V_{DC}$, $V_{IN-} = 0\,V_{DC}$, $V^+ = 15\,V_{DC}$	10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN-} = 1.0\,V_{DC}$, $V_{IN+} = 0\,V_{DC}$, $V^+ = 15\,V_{DC}$	10	15		5.0	8.0		5.0	8.0		5.0	8.0		5.0	8.0		
Differential Input Voltage		Note 7			V^+			V^+			V^+			V^+			V^+	V_{DC}

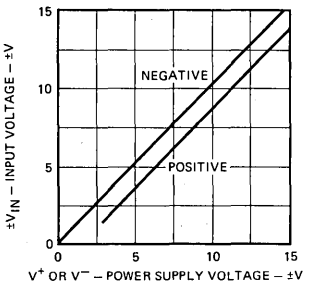
Notes:
1. For operating at high temperatures, the Am324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am224 and Am124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers — use external resistors, where possible to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.
4. These specifications apply for $V^+ = +5V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the Am224, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the Am324 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
5. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).
6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
7. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32V without damage.
8. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

MAXIMUM RATINGS (Above which the useful life may be impaired)

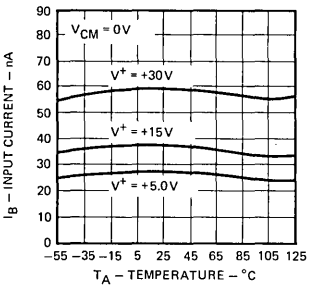
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	570mW
Cavity DIP	900mW
Flat Pak (Am124F)	800mW
Output Short Circuit to GND (Note 2)	
(One Amplifier) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous
Input Current ($V_{IN} < -0.3V_{OL}$) (Note 3)	50mA
Operating Temperature Range	
Am324/Am324A	0°C to +70°C
Am224/Am224A	−25°C to +85°C
Am124/Am124A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL PERFORMANCE CURVES

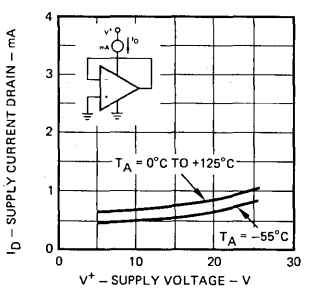
Input Voltage Range



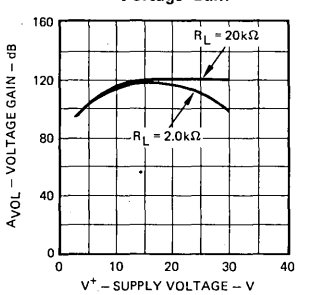
Input Current



Supply Current

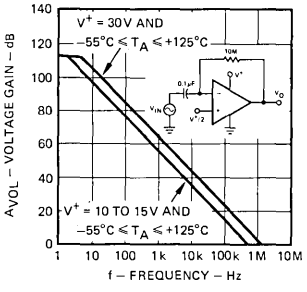


Voltage Gain

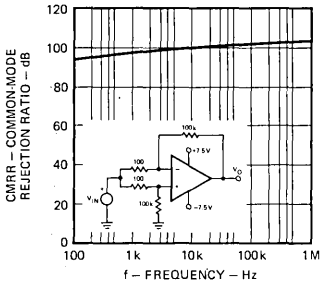


TYPICAL PERFORMANCE CURVES (Cont.)

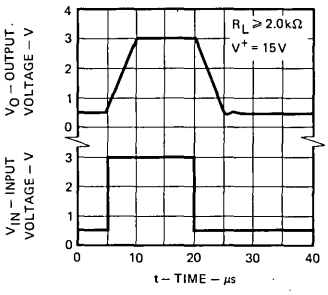
Open Loop Frequency Response



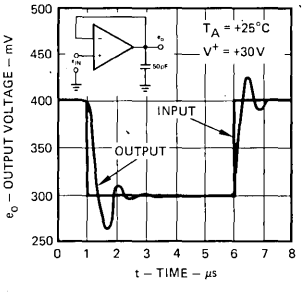
Common-Mode Rejection Ratio



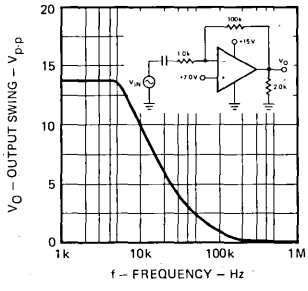
Voltage Follower Pulse Response



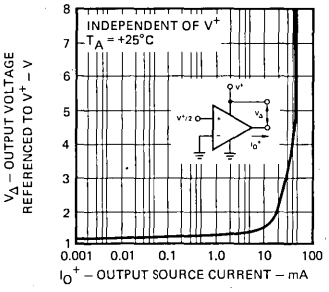
Voltage Follower Pulse Response (Small Signal)



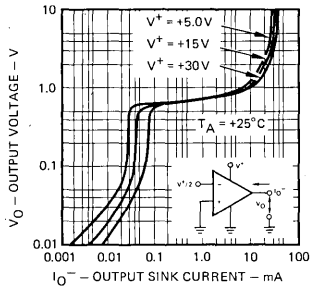
Large Signal Frequency Response



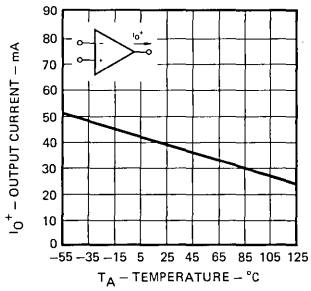
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



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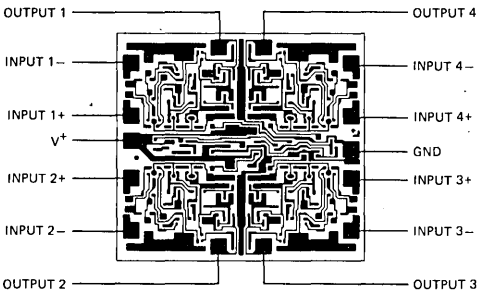
Metallization and Pad Layout



58 x 63 MILS

APPLICATION INFORMATION

The Am124 series are op amps primarily operating from a single power supply voltage and have true-differential inputs remaining in the linear mode with an input common-mode voltage of 0V. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. The bias network of the amplifier establishes a drain current independent of the magnitude of the power supply voltage over the range of from 3V to 30V.

The pin configuration is designed to simplify PC board layouts. Since the amplifier outputs are placed at the corners of the package (pins 1, 7, 8, and 14) and are adjacent to the inverting inputs.

Extra care should be taken to insure that the power for the circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket. This prevents a possible fusing of the internal conductors and becoming a destroyed unit which could occur from the unlimited current surge through the resulting forward diode within the IC.

The use of input differential voltage protection diodes is not needed since large differential voltages can be readily applied resulting in no large input currents. The differential input voltage may be larger than V^+ without damaging the device. Protection, such as an input clamp diode with a resistor to the IC input terminal, should be provided to prevent the input voltages from going negative more than –0.3V (at 25°C).

The amplifiers contain a class A output stage for small signal levels which converts to class B in a large signal mode, to reduce the power supply current drain. Since this allows the amplifiers to both source and sink large output currents, both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to rise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC coupled applications crossover distortion can be minimized by utilizing a resistor from the output of the amplifier to ground. However, in DC applications, where the load is directly coupled, there is no crossover distortion.

To maintain resistance to destruction, output short circuits either to ground or to the positive power supply should be restricted to short time durations. The possibility of destruction exists, not as a result of the short circuit current metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short circuits on more than one amplifier at a time increases the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see section on typical performance characteristics) than a standard IC op amp.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accomodated using the worst case noninverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The series, as presented in the section on typical applications, emphasize operations on only a single power supply voltage. Yet, if complementary power supplies are available, all of the standard op amp circuits can be implemented. A unique feature in introducing a pseudo-ground (a bias voltage reference of $V^+/2$) is allowing operation above and below this value in single power supply systems. In most cases, input biasing is not required and input voltages which range to ground can be easily accomodated.

Am148 • Am149

PRELIMINARY DATA

Quad 741 Op Amps

Distinctive Characteristics

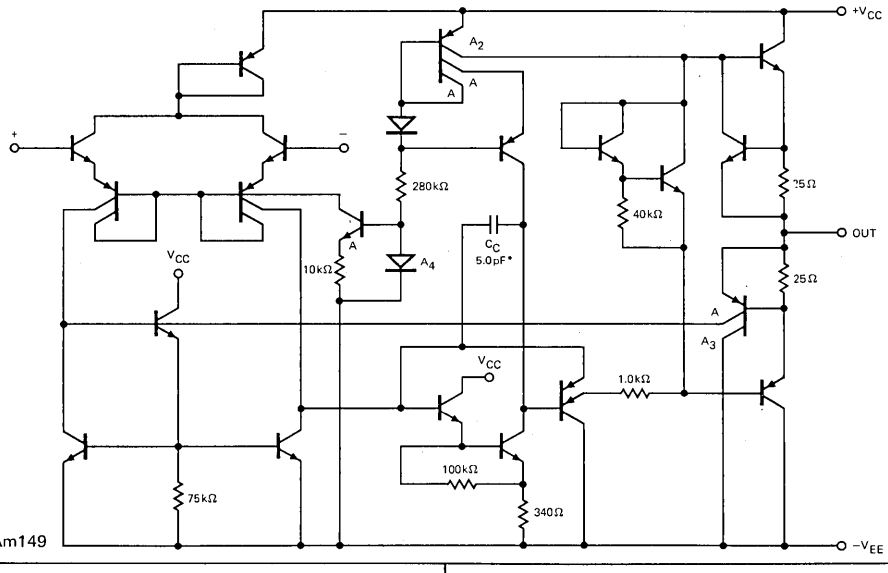
- 741 op amp operating characteristics
- Low supply current drain — 0.6mA/amplifier
- Class AB output state — no crossover distortion
- Pin compatible with the Am124
- Low input offset voltage — 1.0mV
- Low input offset current — 4.0nA
- Low input bias current — 30nA
- Gain bandwidth product
  Am148 (unity gain) — 1.0MHz
  Am149 ($A_V \geq 5$) — 4.0MHz
- High degree of isolation between amplifiers — 120dB
- Overload protection for inputs and outputs

FUNCTIONAL DESCRIPTION

The Am148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The Am149 series has the same features as the Am148 plus a gain bandwidth product of 4.0MHz at a gain of 5.0 or greater.

The Am148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

SCHEMATIC DIAGRAM (Each Amplifier)

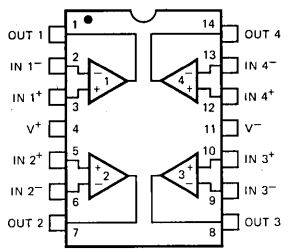


*1.0pF on the Am149

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am348	Hermetic DIP	0°C to +70°C	LM348D
	Molded DIP	0°C to +70°C	LM348N
	Dice	0°C to +70°C	LD348
Am248	Hermetic DIP	−25°C to +85°C	LM248D
Am148	Hermetic DIP	−55°C to +125°C	LM148D
	Dice	−55°C to +125°C	LD148
Am349	Hermetic DIP	0°C to +70°C	LM349D
	Molded DIP	0°C to +70°C	LM349N
	Dice	0°C to +70°C	LD349
Am249	Hermetic DIP	−25°C to +85°C	LM249D
Am149	Hermetic DIP	−55°C to +125°C	LM149D
	Dice	−55°C to +125°C	LD149

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS

	Am148/Am149	Am248/Am249	Am348/Am349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage	±22V	±18V	±18V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) – P_d		570mW	500mW
– θ_{jA}		150°C/W	150°C/W
Cavity DIP (D) (J) – P_d	900mW	900mW	900mW
– θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature ($T_{jmax.}$)	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

See Am741 for Typical Performance Characteristics.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameters	Conditions		Am148/Am149 Min.	Am148/Am149 Typ.	Am148/Am149 Max.	Am248/Am249 Min.	Am248/Am249 Typ.	Am248/Am249 Max.	Am348/Am349 Min.	Am348/Am349 Typ.	Am348/Am349 Max.	Units
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10k\Omega$			1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$			4.0	25		4.0	50		4.0	50	nA
Input Bias Current	$T_A = 25°C$			30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm15V$			2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 2.0k\Omega$		50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1.0Hz to 20kHz (Input Referred)			–120			–120			–120		dB
Small Signal Bandwidth	$T_A = 25°C$	Am148 Series		1.0			1.0			1.0		MHz
		Am149 Series		4.0			4.0			4.0		
Phase Margin	$T_A = 25°C$	Am148 Series ($A_V = 1$)		60			60			60		degrees
		Am149 Series ($A_V = 5$)		60			60			60		
Slew Rate	$T_A = 25°C$	Am148 Series ($A_V = 1$)		0.5			0.5			0.5		V/μs
		Am149 Series ($A_V = 5$)		2.0			2.0			2.0		
Output Short Circuit Current	$T_A = 25°C$			25			25			25		mA
Input Offset Voltage	$R_S \leq 10k\Omega$				6.0			7.5			7.5	mV
Input Offset Current					75			125			100	nA
Input Bias Current					325			500			400	nA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L > 2.0k\Omega$		25			15			15			V/mV
Output Voltage Swing	$V_S = \pm15V$	$R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		V
		$R_L = 2.0k\Omega$	±10	±12		±10	±12		±10	±12		
Input Voltage Range	$V_S = \pm15V$		±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$		70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10k\Omega$		77	96		77	96		77	96		dB

Notes:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{jmax.}$, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jmax.} - T_A)/\theta_{jA}$ or the 25°C $P_{dmax.}$, whichever is less. Derate Dual In-Line package at 9mW/°C for operation at ambient temperatures above 95°C.
3. These specifications apply for $V_S = \pm15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.
4. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

LF155/LF156/LF157

Monolithic JFET Input Operational Amplifiers

DISTINCTIVE CHARACTERISTICS

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000pF) without stability problems
- Internal compensation and large differential input voltage capability

GENERAL DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

The LF155, LF156, LF157 series are direct replacements for National LF155, LF156, LF157 series.

COMMON FEATURES
(LF155A, LF156A, LF157A)

Low input bias current	30pA
Low input offset current	3.0pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1.0mV
Low input offset voltage temperature drift	3.0μV/°C
Low input noise current	0.01pA/√Hz
High common-mode rejection ratio	100dB
Large dc voltage gain	106dB

APPLICATIONS

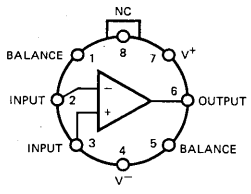
- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

UNCOMMON FEATURES

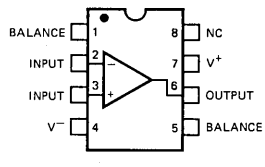
	LF155A	LF156A	LF157A (A_V = 5)	Units
Extremely fast settling time to 0.01%	4.0	1.5	1.5	μs
Fast slew rate	5.0	12	50	V/μs
Wide gain bandwidth	2.5	5.0	20	MHz
Low input noise voltage	20	12	12	nV/√Hz

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line

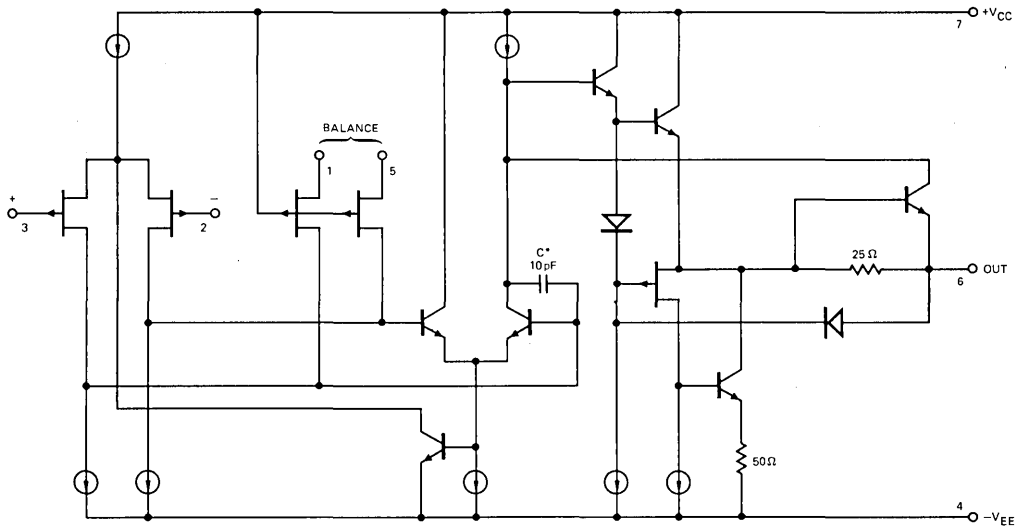


Notes: 1. On Dual-In-Line Pin 1 is marked for orientation.
2. On Metal Can Pin 4 is connected to case.

ORDERING INFORMATION

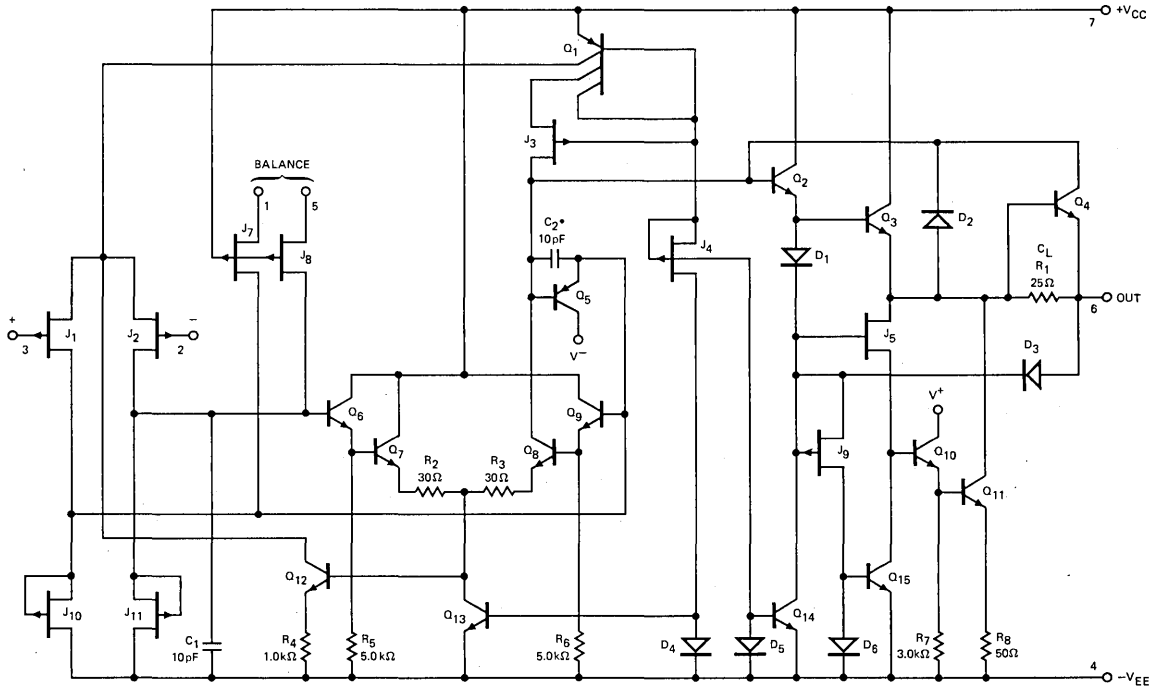
Part Number	Package Type	Temperature Range	Order Number
LF355	Metal Can	0°C to +70°C	LF355H
	Molded DIP	0°C to +70°C	LF355N
	Dice	0°C to +70°C	LD355
LF255	Metal Can	−25°C to +85°C	LF255H
LF155	Metal Can	−55°C to +125°C	LF155H
	Dice	−55°C to +125°C	LD155
LF355A	Metal Can	0°C to +70°C	LF355AH
	Dice	0°C to +70°C	LD355A
LF155A	Metal Can	−55°C to +125°C	LF155AH
	Dice	−55°C to +125°C	LD155A
LF356	Metal Can	0°C to +70°C	LF356H
	Molded DIP	0°C to +70°C	LF356N
	Dice	0°C to +70°C	LD356
LF256	Metal Can	−25°C to +85°C	LF256H
LF156	Metal Can	−55°C to +125°C	LF156H
	Dice	−55°C to +125°C	LD156
LF356A	Metal Can	0°C to +70°C	LF356AH
	Dice	0°C to +70°C	LD356A
LF156A	Metal Can	−55°C to +125°C	LF156AH
	Dice	−55°C to +125°C	LD156A
LF357	Metal Can	0°C to +70°C	LF357H
	Molded DIP	0°C to +70°C	LF357N
	Dice	0°C to +70°C	LD357
LF257	Metal Can	−25°C to +85°C	LF257H
LF157	Metal Can	−55°C to +125°C	LF157H
	Dice	−55°C to +125°C	LD157
LF357A	Metal Can	0°C to +70°C	LF357AH
	Dice	0°C to +70°C	LD357A
LF157A	Metal Can	−55°C to +125°C	LF157AH
	Dice	−55°C to +125°C	LD157A

SIMPLIFIED SCHEMATIC



*C = 2pF on LF157

DETAILED SCHEMATIC



*C = 2pF on LF157

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF155/6/7	LF255/6/7	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H Package)	670mW	670mW	570mW	500mW
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
$T_{J(Max.)}$	150°C	150°C	115°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Note 3)

DC CHARACTERISTICS

Parameters	Description	Test Conditions	LF155A/6A/7A Min.	LF155A/6A/7A Typ.	LF155A/6A/7A Max.	LF355A/6A/7A Min.	LF355A/6A/7A Typ.	LF355A/6A/7A Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1.0	2.0		1.0	2.0	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3.0	5.0		3.0	5.0	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Note 3, 5)		3.0	10		3.0	10	pA
		$T_J \leq T_{HIGH}$			10			1.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J < T_{HIGH}$			25			5.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = ±15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = ±10V$, $R_L = 2k\Omega$ Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = ±15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		Volts
		$V_S = ±15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = ±15V$	±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

AC CHARACTERISTICS ($T_A = 25°C$, $V_S = ±15V$)

Parameters	Description	Test Conditions	LF155A/355A Min.	LF155A/355A Typ.	LF155A/355A Max.	LF156A/356A Min.	LF156A/356A Typ.	LF156A/356A Max.	LF157A/357A Min.	LF157A/357A Typ.	LF157A/357A Max.	Units
SR	Slew Rate	LF155A/6A: $A_V = 1$	3.0	5.0		10	12					V/µs
		LF157A: $A_V = 5$							40	50		V/µs
GBW	Gain-Bandwidth Product			2.5		4.0	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4.0			1.5			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000Hz		20			12			12		
i_n	Equivalent Input Noise Current	f = 100Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000Hz		0.01			0.01			0.01		
C_{IN}	Input Capacitance			3.0			3.0			3.0		pF

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ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

DC CHARACTERISTICS (Note 3)

Parameters	Description	Test Conditions	LF155/6/7 Min.	LF155/6/7 Typ.	LF155/6/7 Max.	LF255/6/7 Min.	LF255/6/7 Typ.	LF255/6/7 Max.	LF355/6/7 Min.	LF355/6/7 Typ.	LF355/6/7 Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3.0	5.0		3.0	5.0		3.0	10	mV
		Over Temperature			7.0			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5.0			5.0			5.0		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Notes 3, 5)		3.0	20		3.0	20		3.0	50	pA
		$T_J \leq T_{HIGH}$			20			1.0			2.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5.0			8.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		25	200		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$ Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		Volts
		$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12			+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$)

Parameters	LF155A/355A LF155/255 Typ.	LF155A/355A LF155/255 Max.	LF355 Typ.	LF355 Max.	LF156A LF156/256 Typ.	LF156A LF156/256 Max.	LF356A/356 Typ.	LF356A/356 Max.	LF157A LF157/257 Typ.	LF157A LF157/257 Max.	LF357A/357 Typ.	LF357A/357 Max.	Units
Supply Current	2.0	4.0	2.0	4.0	5.0	7.0	5.0	10	5.0	7.0	5.0	10	mA

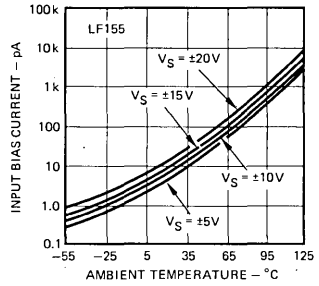
AC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$)

Parameters	Description	Test Conditions	LF155/255/ LF355 Typ.	LF156/256 Min.	LF156/256/ LF356 Typ.	LF157/257 Min.	LF157/257 LF357 Typ.	Units
SR	Slew Rate	LF155/6: $A_V = 1$,	5.0	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain-Bandwidth Product		2.5		5.0		20	MHz
t_s	Settling Time fo 0.01%	(Note 7)	4.0		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000Hz	20		12		12	
i_n	Equivalent Input Noise Current	f = 100Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000Hz	0.01		0.01		0.01	
C_{IN}	Input Capacitance		3.0		3.0		3.0	pF

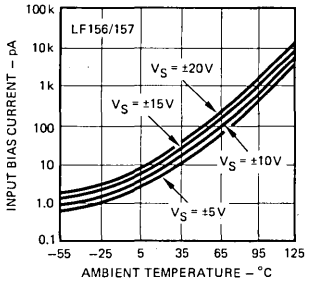
Notes:
1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
4. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C) typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
5. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}Pd$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
6. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
7. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

TYPICAL DC PERFORMANCE CHARACTERISTICS

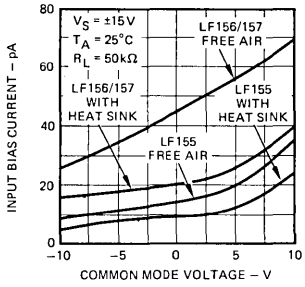
Input Bias Current



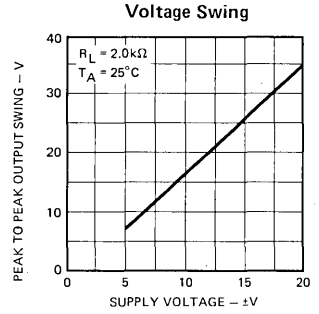
Input Bias Current



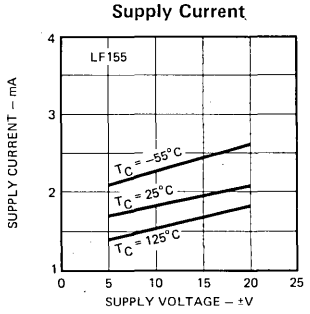
Input Bias Current



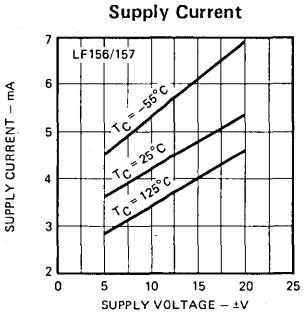
Voltage Swing



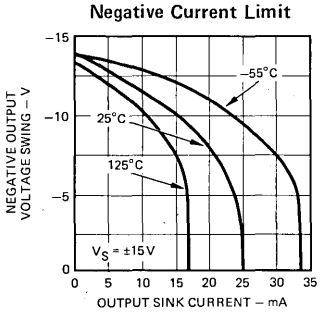
Supply Current



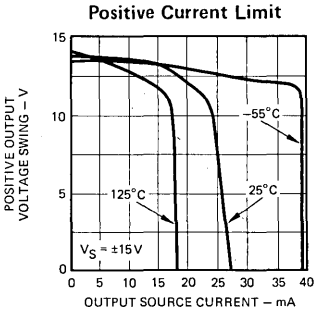
Supply Current



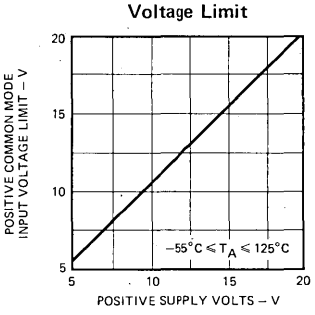
Negative Current Limit



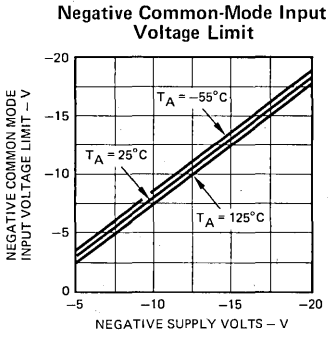
Positive Current Limit



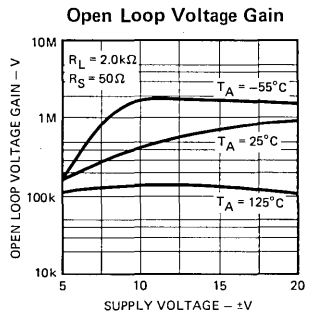
Positive Common-Mode Input Voltage Limit



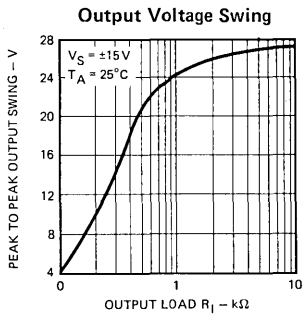
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



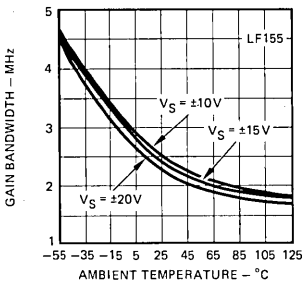
Output Voltage Swing

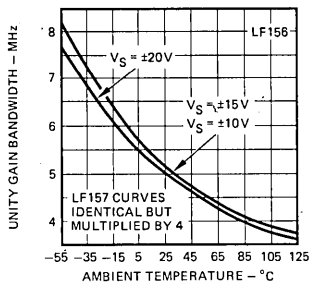


7

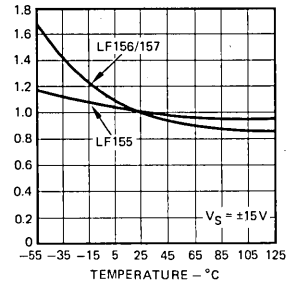
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

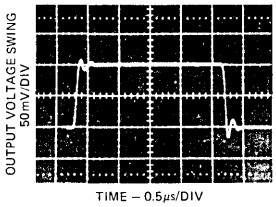




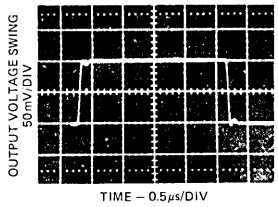
Normalized Slew Rate



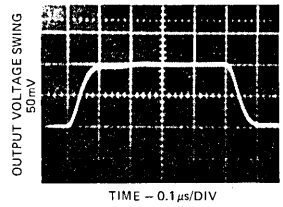
LF155 Small Signal Pulse Response, A_V = +1



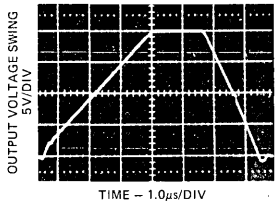
LF156 Small Signal Pulse Response, A_V = +1



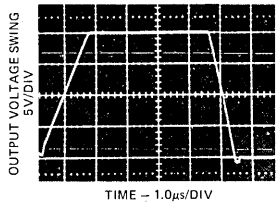
LF157 Small Signal Pulse Response, A_V = +5



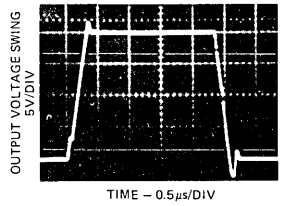
LF155 Large Signal Pulse Response, A_V = +1



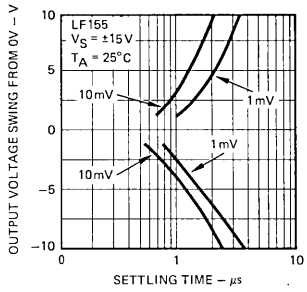
LF156 Large Signal Pulse Response, A_V = +1



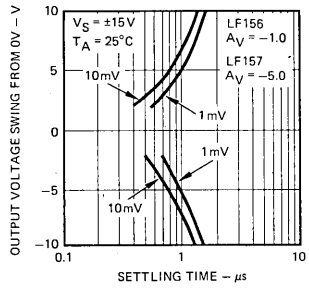
LF157 Large Signal Pulse Response, A_V = +5



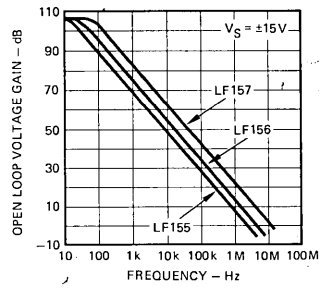
Inverter Settling Time



Inverter Settling Time

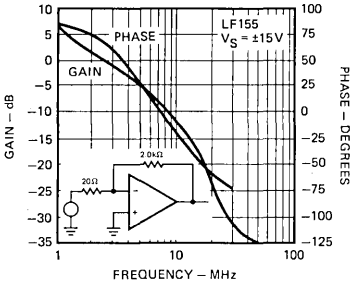


Open Loop Frequency Response

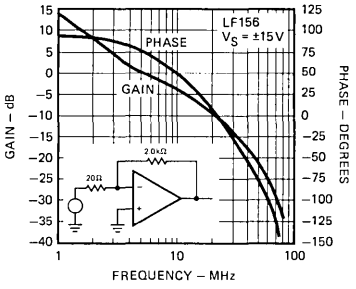


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont.)

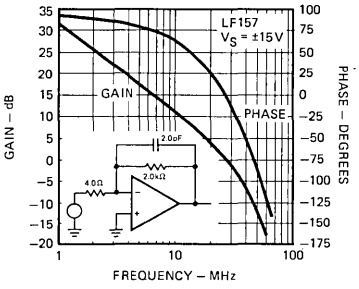
Bode Plot



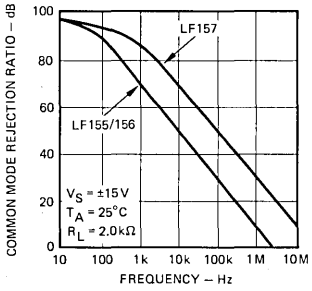
Bode Plot



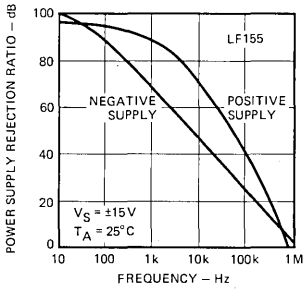
Bode Plot



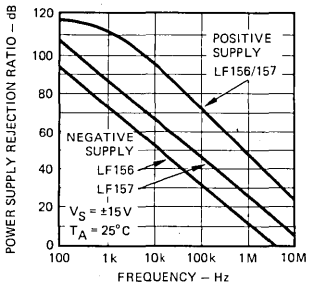
Common-Mode Rejection Ratio



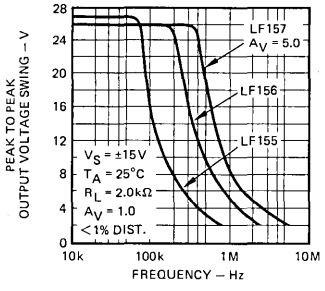
Power Supply Rejection Ratio



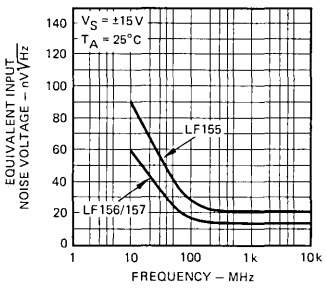
Power Supply Rejection Ratio



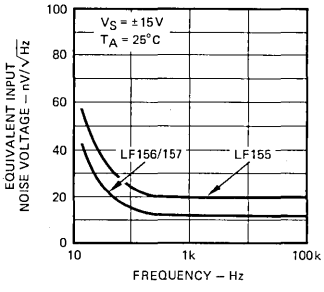
Undistorted Output Voltage Swing



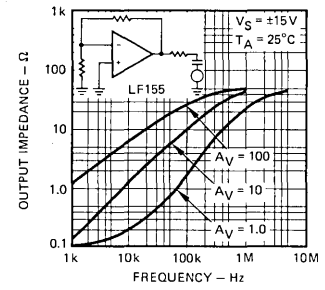
Equivalent Input Noise Voltage



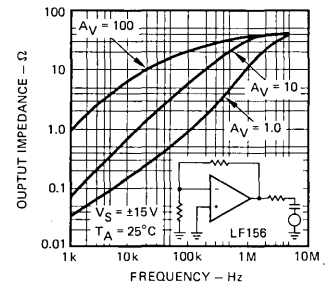
Equivalent Input Noise Voltage (Expanded Scale)



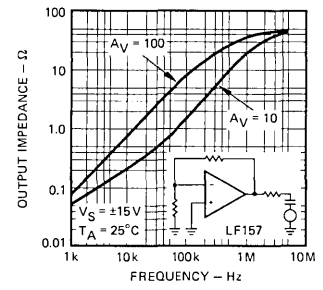
Output Impedance



Output Impedance



Output Impedance



7

APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

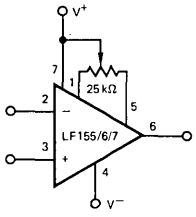
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

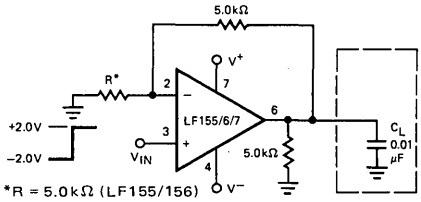
TYPICAL CIRCUIT CONNECTIONS AND PAD LAYOUT

V_{OS} Adjustment



V_{OS} is adjusted with a 25 k potentiometer.
The potentiometer wiper is connected to V^+.

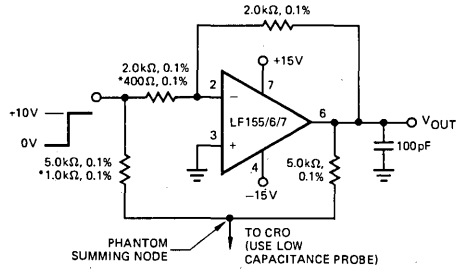
Driving Capacitive Loads



*R = 5.0 kΩ (LF155/156)
*R = 1.25 kΩ (LF157)

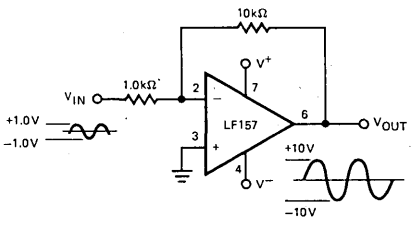
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
C_L Max. ⩾ 0.01 μF
Overshoot ⩽ 20%
Settling time (t_s) ⩾ 5.0μs

Settling Time Test Circuit



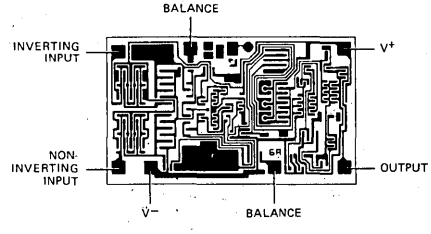
Settling time is tested with the LF155/156 connected as unity gain converter and LF157 connected for A_V = −5.0
Output = 10V step
*A_V = −5.0 for LF157

A Large Power BW Amplifier (LF157)



For distortion ⩽ 1% and a 20Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Metallization and Pad Layout



75 x 45 Mils

Am216/316•Am216A/316A

Compensated, High-Performance Operational Amplifier

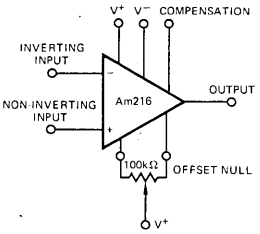
Distinctive Characteristics

- The Am216/Am216A/Am316/Am316A are functionally, electrically, and pin-for-pin equivalent to the National LM216/LM216A/LM316/LM316A.
- Low input bias currents: 50pA
- Low input offset currents: 15pA
- Low power consumption: 3mW
- Internal frequency compensation
- Offset nulling provisions
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in metal can, hermetic dual-in-line and flat packages.

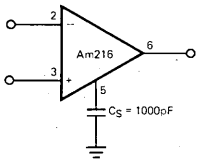
FUNCTIONAL DESCRIPTION

The Am216/Am216A/Am316/Am316A are compensated high performance operational amplifiers featuring extremely low input-current errors. High input impedance achieved using supergain transistors in a Darlington input stage produces input bias currents that are equal to high quality FET amplifiers. These devices are internally frequency compensated and provision is made for offset adjustment with a single potentiometer.

FUNCTIONAL DIAGRAM

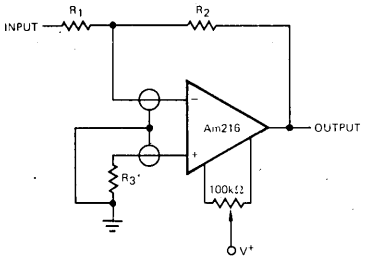


Overcompensation for Greater Stability Margin

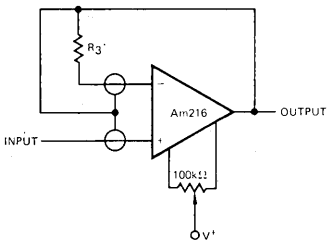


TYPICAL APPLICATIONS

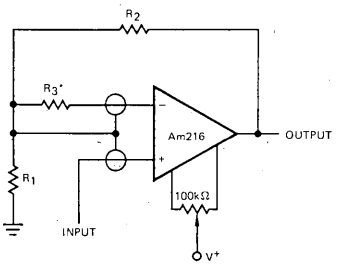
Connection of Input Guards and Offset Null



Inverting Amplifier



Follower



Non-Inverting Amplifier

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1+R_2}$ Must be LOW impedance

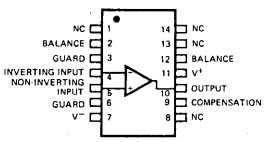
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am316	DIP	0°C to +70°C	LM316D
	Metal Can	0°C to +70°C	LM316H
	Flat Pak	0°C to +70°C	LM316F
	Dice	0°C to +70°C	LD316
Am361A	DIP	0°C to +70°C	LM316AD
	Metal Can	0°C to +70°C	LM316AH
	Flat Pak	0°C to +70°C	LM316AF
	Dice	0°C to +70°C	LD316A
Am216	DIP	−25°C to +85°C	LM216D
	Metal Can	−25°C to +85°C	LM216H
	Flat Pak	−25°C to +85°C	LM216F
	Dice	−25°C to +85°C	LD216
Am216A	DIP	−25°C to +85°C	LM216AD
	Metal Can	−25°C to +85°C	LM216AH
	Flat Pak	−25°C to +85°C	LM216AF
	Dice	−25°C to +85°C	LD216A

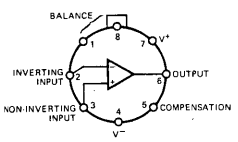
CONNECTION DIAGRAMS

Top Views

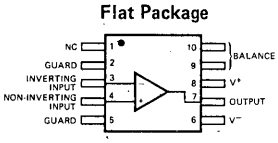
Dual-In-Line



Metal Can



Flat Package



Notes:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On Flat Package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

7

MAXIMUM RATINGS

Supply Voltage	±20 V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am216/Am216A	−25°C to 85°C
Am316/Am316A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

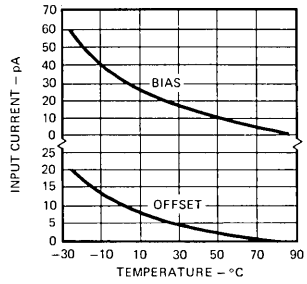
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am216	Am216A	Am316	Am316A	Units
Input Offset Voltage		10	3	10	3	mV
Input Offset Current		50	15	50	15	pA
Input Bias Current		150	50	150	50	pA
Input Resistance		1	5	1	5	GΩ
Supply Current		0.8	0.6	0.8	0.6	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq$ 10kΩ	20	40	20	40	V/mV
The Following Specifications Apply Over The Operating Temperature Ranges						
Input Offset Voltage		15	6	15	6	mV
Input Offset Current		100	30	100	30	pA
Input Bias Current		250	100	250	100	pA
Supply Current	$T_A = T_{MAX.}$		0.5		0.5	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq$ 10kΩ	10	20	15	30	V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±13	±13	±13	V
Input Voltage Range	V_S = ±15V	±13	±13	±13	±13	V
Common Mode Rejection Ratio		80	80	80	80	dB
Supply Voltage Rejection Ratio		80	80	80	80	dB

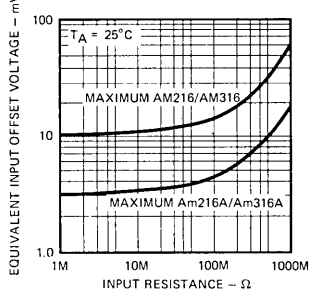
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V.

TYPICAL PERFORMANCE CHARACTERISTICS

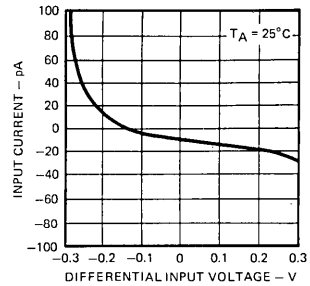
Input Currents



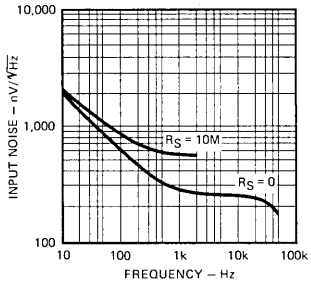
Offset Error



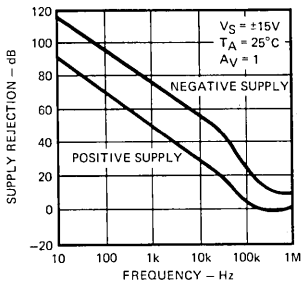
Input Current



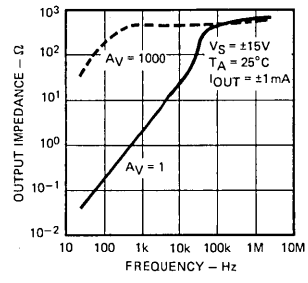
Input Noise Voltage



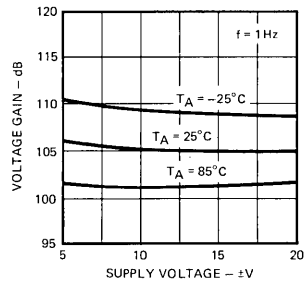
Power Supply Rejection



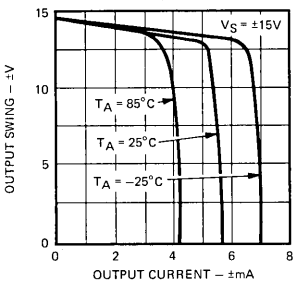
Closed Loop Output Impedance



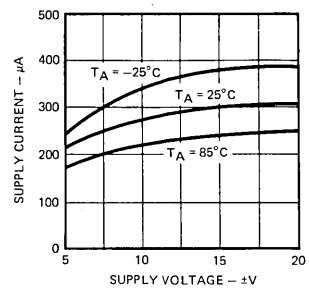
Voltage Gain



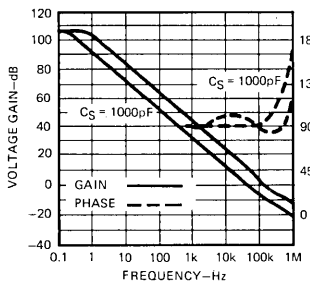
Output Swing



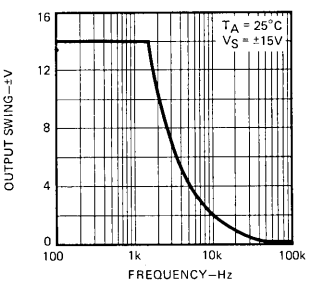
Supply Current



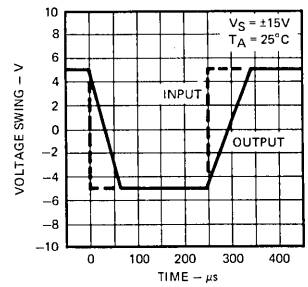
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



7

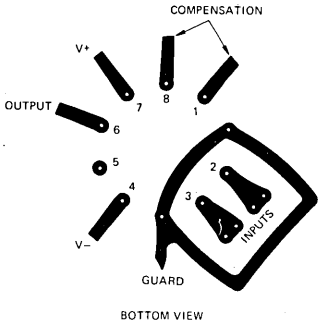
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the Am216 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

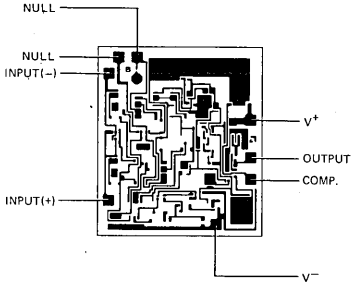
Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



Note: Board layout for input Guarding with TO-99 package.

Metallization and Pad Layout



62 x 72 Mils

Am715/715C

High-Speed Operational Amplifier

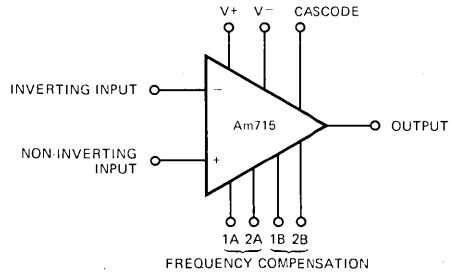
Description: The Am715 and Am715C high-speed operational amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA715 and μA715C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

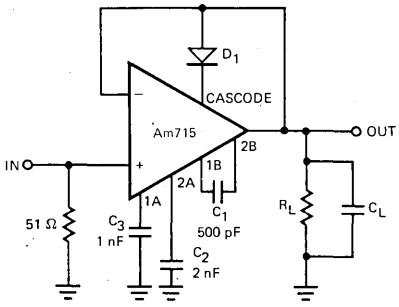
The Am715 is a differential input, single-ended output operational amplifier having wide bandwidth and high slew rate. It has internal lead compensation and four points for external lag compensation networks, providing many possible combinations of frequency compensation. In addition, a point is brought out for use with an external diode to prevent latch-up in voltage follower applications.

FUNCTIONAL DIAGRAM

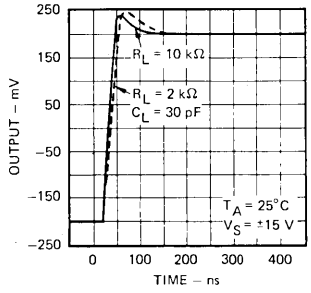


APPLICATIONS

Voltage Follower



Voltage Follower Small-Signal Pulse Response



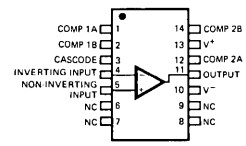
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am715C	Metal Can	0°C to +70°C	715HC
	DIP	0°C to +70°C	715DC
	Dice	0°C to +70°C	715XC
Am715	Metal Can	−55°C to +125°C	715HM
	DIP	−55°C to +125°C	715DM
	Flat Pak	−55°C to +125°C	715FM
	Dice	−55°C to +125°C	715XM

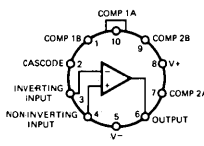
CONNECTION DIAGRAMS

Top Views

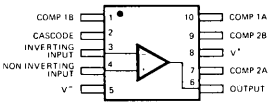
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 10 is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

7

MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±6 V
Input Voltage (Note 2)	±15 V
Operating Temperature Range	
Am715C	0°C to +70°C
Am715	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am715C Min	Am715C Typ	Am715C Max	Am715 Min	Am715 Typ	Am715 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5		2.0	5.0	mV
Input Offset Current			70	250		70	250	nA
Input Bias Current			0.4	1.5		0.4	0.75	μA
Input Resistance			1.0			1.0		MΩ
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74	92		74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		70	400		70	300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10	30		15	30		V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Output Resistance			75			75		Ω
Supply Current			5.5	10		5.5	7.0	mA
Power Consumption			165	300		165	210	mW
Transient Response (Voltage Follower) Risetime	$V_{out} = \pm 200$ mV, $R_L = 2$ kΩ, $C_L = 30$ pF		30	75		30	60	ns
Overshoot			30	50		30	40	%
Slew Rate	Av = 100 (Fig. 8) $V_{out} = 0$ to +10 V,		65			65		V/μs
	Av = 10 (Fig. 7) $R_L = 2$ kΩ,		40			40		V/μs
	Av = 1 (Figs. 1 & 2) $C_L = 30$ pF	10	20		15	20		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			10			7.5	mV
Input Offset Current	$T_A = T_{A\,max}$			250			250	nA
	$T_A = T_{A\,min}$			750			800	nA
Input Bias Current	$T_A = T_{A\,max}$			1.5			0.75	μA
	$T_A = T_{A\,min}$			7.5			4.0	μA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74			74			dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ			400			300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	8.0			10			V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			±10			V

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

PERFORMANCE CURVES

Voltage Follower

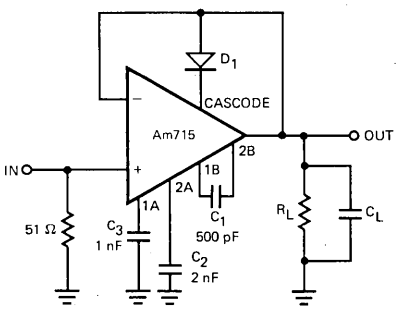


Figure 1

X1 Inverting Amplifier

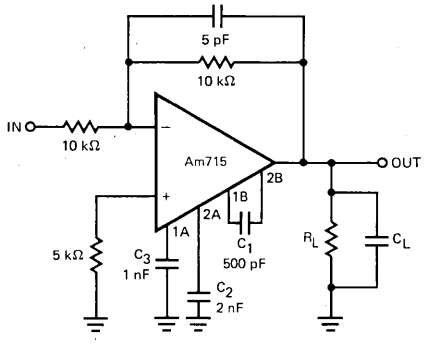
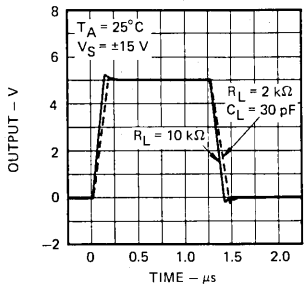


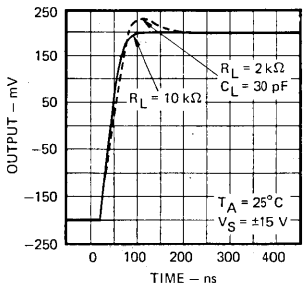
Figure 2

The high gain and large bandwidth of the Am715 make it mandatory to observe the following precautions in using the device, as is the case with any high frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs and frequency compensation pins. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance of the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to an absolute minimum, since the amplifier cannot tolerate more than 30 pF directly at its output with full feedback.

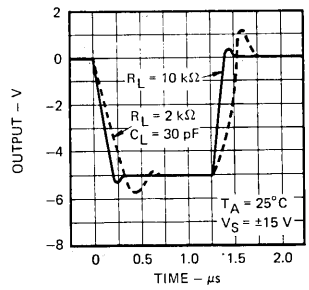
Follower & X1 Inverter Positive Large-Signal Pulse Response



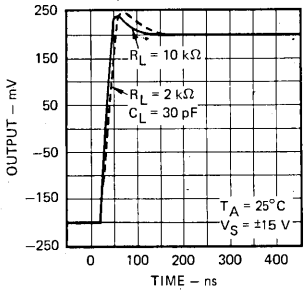
X1 Inverter Small-Signal Pulse Response



Follower & X1 Inverter Negative Large-Signal Pulse Response



Voltage Follower Small-Signal Pulse Response



7

X10 Amplifier

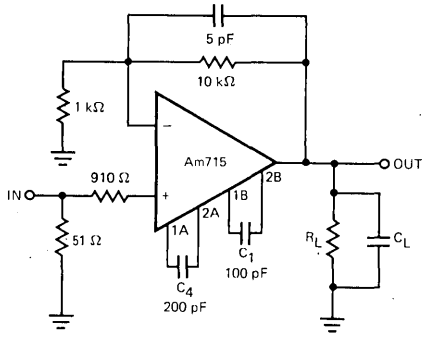


Figure 3

X100 Amplifier

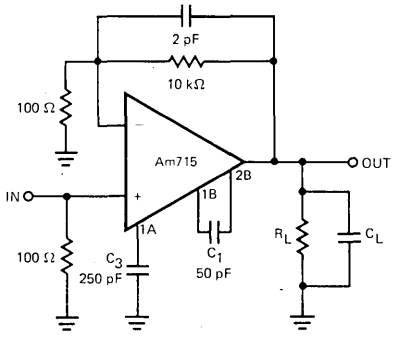
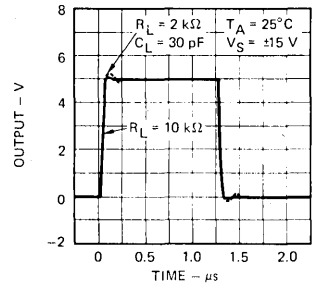


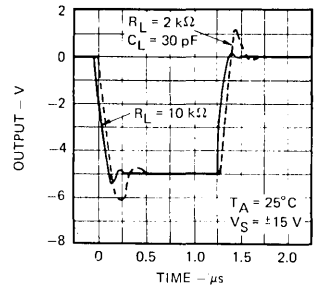
Figure 4

PERFORMANCE CURVES

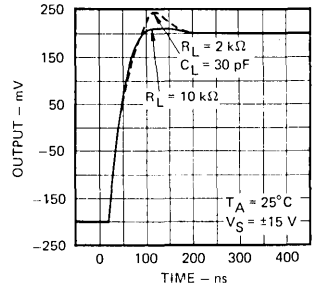
X10 Amplifier Positive Large-Signal Pulse Response



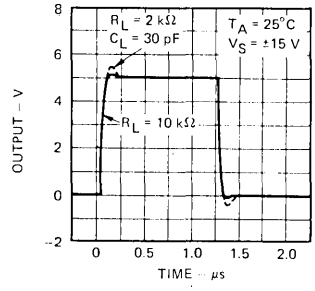
X10 Amplifier Negative Large-Signal Pulse Response



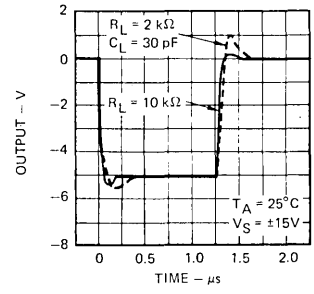
X10 Amplifier Small-Signal Pulse Response



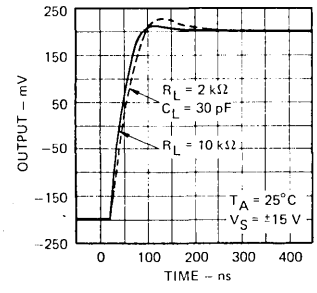
X100 Amplifier Positive Large-Signal Pulse Response



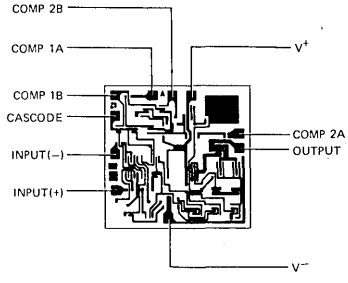
X100 Amplifier Negative Large-Signal Pulse Response



X100 Amplifier Small-Signal Pulse Response



Metallization and Pad Layout



62 x 62 Mils

Am725/725C

Instrumentation Operational Amplifiers

Description:

The Am725 and Am725C monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild 725 and 725C. They are available in the hermetic metal can and DIP packages.

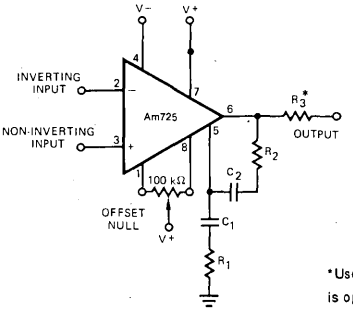
Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The 725/725C are instrumentation operational amplifiers. Device design has been optimized to provide low noise voltage, low offset voltage, low offset voltage drift and high common mode rejection. The 725 is offset voltage adjustable and is pin-for-pin compatible with the 108 and 101A amplifiers. However, additional frequency compensation components are required and should be determined by the desired closed loop gain.

FUNCTIONAL DIAGRAM



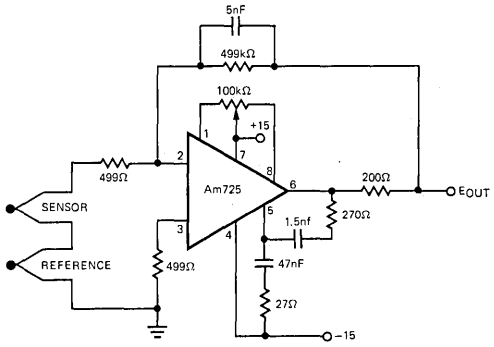
Compensation Component Values

A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	—	—
100	47	10	—	—
10	27	50	270	1.5
1	10	50	39	20

*Use R_3 = 51Ω when the amplifier is operated with capacitive loads.

APPLICATION

Thermocouple Amplifier



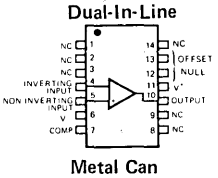
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am725C	TO-99	0°C to +70°C	725HC
	DIP	0°C to +70°C	725DC
	Molded DIP	0°C to +70°C	725CN
	Dice	0°C to +70°C	725XC
Am725	TO-99	−55°C to +125°C	725HM
	DIP	−55°C to +125°C	725DM
	Dice	−55°C to +125°C	725XM

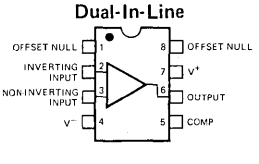
CONNECTION DIAGRAMS

Top Views

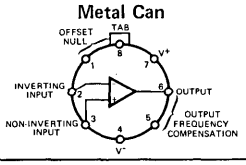
Dual-In-Line



Dual-In-Line



Metal Can



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Operating Temperature Range	
Am725	−55°C to +125°C
Am725C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

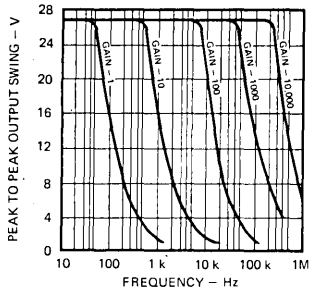
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Am725C Min	Am725C Typ	Am725C Max	Am725 Min	Am725 Typ	Am725 Max	Units
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5		0.5	1.0	mV
Input Offset Current			3.0	35		2.0	20	nA
Input Bias Current			50	125		42	100	nA
Input Noise Voltage	f_o = 10Hz f_o = 100Hz f_o = 1kHz		15 12 8.0			15 9.0 8.0		nV/√Hz nV/√Hz nV/√Hz
Input Noise Current	f_o = 10Hz f_o = 100Hz f_o = 1kHz		1.0 0.8 0.6			1.0 0.3 0.15		pA/√Hz pA/√Hz pA/√Hz
Input Resistance			3.0			1.5		MΩ
Input Voltage Range		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} = ±10V	0.25	3.0		1.0	3.0		V/μV
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	96	120		110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$		2.0	35		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±13 ±13		±12 ±12	±13.5 ±13.5		V V
Output Resistance			150			150		Ω
Power Consumption			80	150		80	105	mW
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Without external trim)	$R_S \leq 10k\Omega$		0.8	3.5			1.5	mV
Average Temperature Coefficient of Input Offset Voltage (Without external trim)	R_S = 50Ω		1.2			2.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Voltage (With external trim)	R_S = 50Ω		0.5			0.6		μV/°C
Input Offset Current	$T_{A(max)}$ $T_{A(min)}$		25 100	125 250		20 80	100 200	nA nA
Average Temperature Coefficient of Input Offset Current			25			25	150	pA/°C
Input Bias Current	$T_{A(max)}$ $T_{A(min)}$		25 100	125 250		20 80	100 200	nA nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $T_{A(max)}$ $R_L \geq 2k\Omega$, $T_{A(min)}$	0.125 0.125			1.0 0.25			V/μV
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$		115		100			dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$		20				20	μV/V
Output Voltage Swing	$R_L \geq 2k\Omega$	±10	±13		±10			V

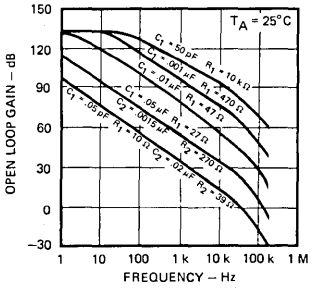
Notes: 1. Derate at 6.8 mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

PERFORMANCE CURVES

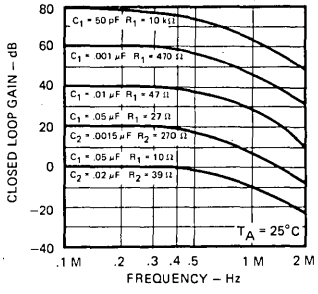
Maximum Undistorted Sinusoidal Output Versus Frequency



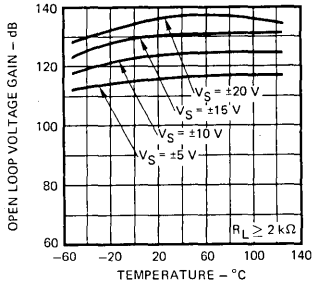
Open Loop Response For Various Values Of Compensation



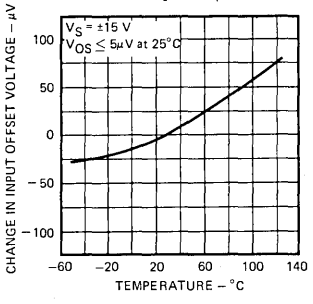
Frequency Response For Various Closed Loop Gains



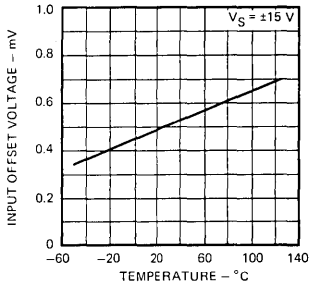
Open Loop Voltage Gain As A Function Of Temperature For Various Supply Voltages



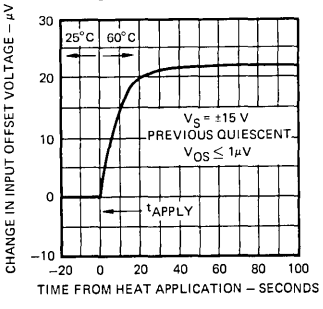
Nulled Input Offset Voltage As A Function Of Temperature



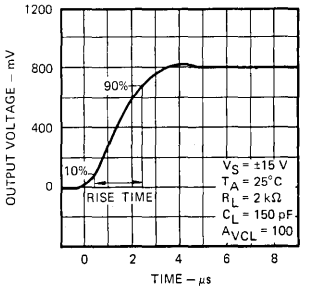
Unnulled Input Offset Voltage As A Function Of Temperature



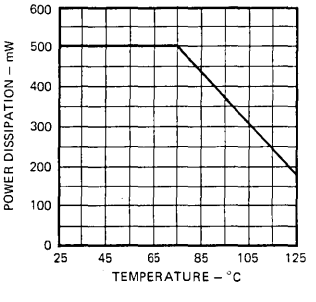
Change In Input Offset Voltage Due To Thermal Shock As A Function Of Time



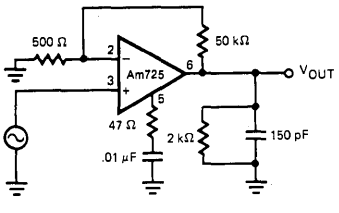
Transient Response



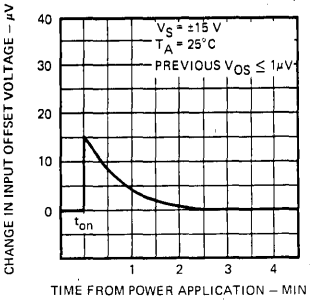
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



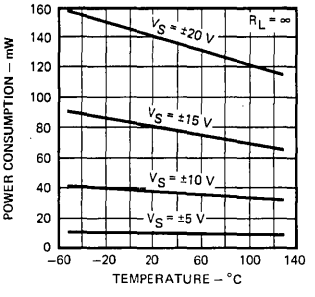
Transient Response Test Circuit



Stabilization Time Of Input Offset Voltage From Power Turn-On



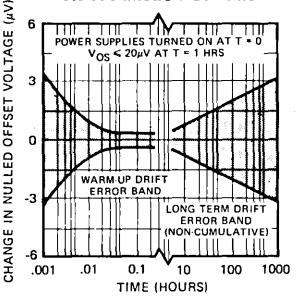
Power Consumption As A Function Of Temperature



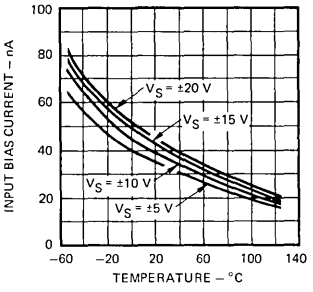
7

PERFORMANCE CURVES

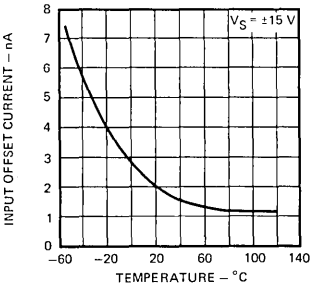
Input Offset Voltage Drift As A Function Of Time



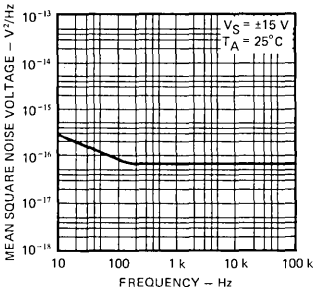
Input Bias Current As A Function Of Temperature



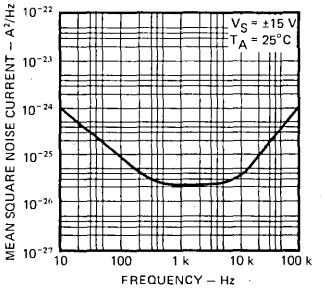
Input Offset Current As A Function Of Temperature



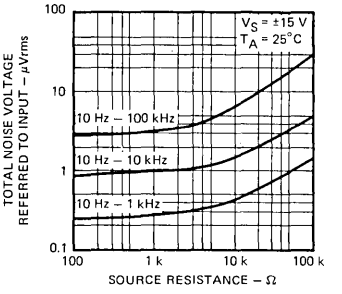
Input Noise Voltage As A Function Of Frequency



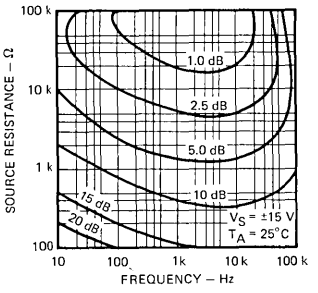
Input Noise Current As A Function Of Frequency



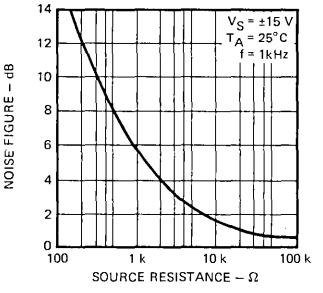
Broadband Noise For Various Bandwidths



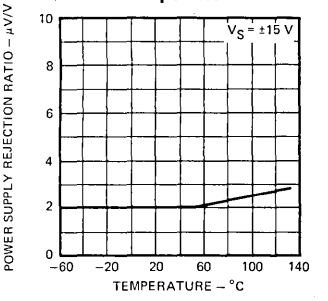
Narrow Band Spot Noise Figure Contours



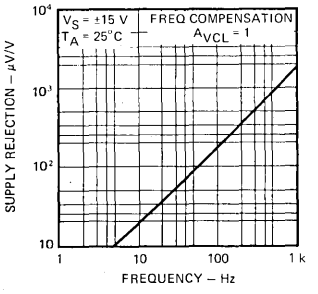
Noise Figure As A Function Of Source Resistance



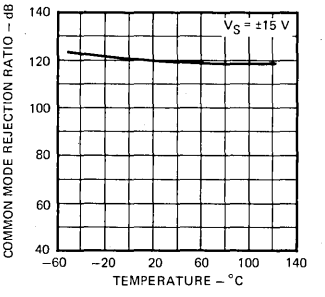
Supply Voltage Rejection Ratio As A Function Of Temperature



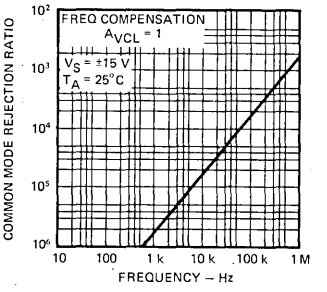
Supply Rejection As A Function Of Frequency



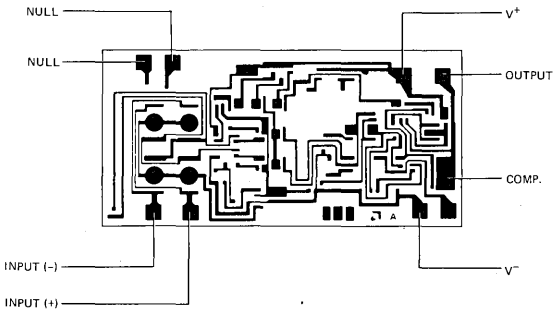
Common Mode Rejection Ratio As A Function Of Temperature



Common Mode Rejection Ratio As A Function Of Frequency



Metallization and Pad Layout



50 x 95 Mils

Am741/741C/741A/741E

Frequency-Compensated Operational Amplifier

Description:

The Am741 Series Frequency Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μ741 series. The are available in the hermetic metal can, flat package, and dual-in-line packages as well as plastic dual-in-line.

The Am741A and Am741E are tested to the electrical characteristics of the current revision of MIL-M-38510/10101.

Distinctive Characteristics:

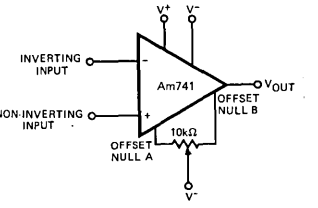
100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

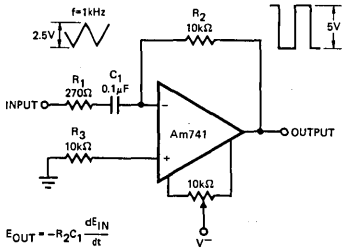
The Am741 series are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM

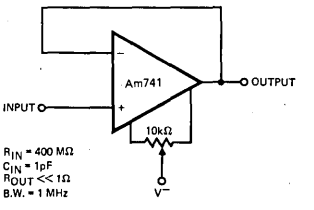


APPLICATIONS

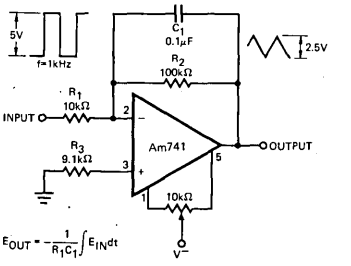
DIFFERENTIATOR



UNITY GAIN VOLTAGE FOLLOWER



INTEGRATOR

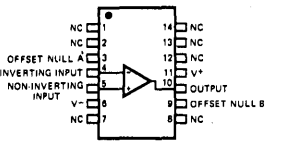


ORDERING INFORMATION

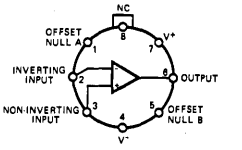
Part Number	Package Type	Temperature Range	Order Number
Am741C	Metal Can	0°C to +70°C	741HC
	Hermetic DIP	0°C to +70°C	741DC
	Dice	0°C to +70°C	741XC
Am741	Metal Can	−55°C to +125°C	741HM
	Hermetic DIP	−55°C to +125°C	741DM
	Flat Pack	−55°C to +125°C	741FM
	Dice	−55°C to +125°C	741XM
Am741E	Metal Can	0°C to +70°C	741EHC
	Hermetic DIP	0°C to +70°C	741EDC
Am741A	Metal Can	−55°C to +125°C	741AHM
	Hermetic DIP	−55°C to +125°C	741ADM
	Flat Pack	−55°C to +125°C	741AFM

CONNECTION DIAGRAMS
Top Views

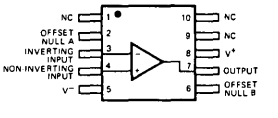
Dual-In-Line



Metal Can



Flat Package



Notes:
1. On DIP, pin 6 is connected to bottom of package.
2. On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	
Am741/741A/741E	±22 V
Am741C	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V^-	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am741/741A	−55°C to +125°C
Am741C/741E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am741C Min.	Am741C Typ.	Am741C Max.	Am741 Min.	Am741 Typ.	Am741 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.4		0.3	0.4		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

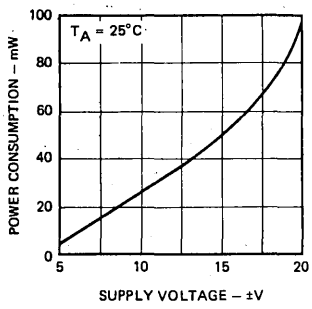
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified) Am741A/741E

Parameters (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Input Offset Current			3.0	30	nA
Input Bias Current (Note 5)			30	110	nA
Power Supply Rejection Ratio (Note 6)	V_S = +10, –20; V_S = +20, –10V, R_S = 50Ω		15	50	μV/V
Common Mode Rejection	V_{CM} = ±15V	80			dB
Output Short Circuit Current	±V_{CC} = ±15V, V_O = ±15V Short to Other Supply	9		40	mA
Power Dissipation		10		150	mW
Large Signal Voltage Gain	±V_{CC} = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	50			V/mV
	±V_{CC} = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV
Transient Response (unity gain) Rise Time			0.30	0.8	μs
Overshoot			5.0	20	%
Adjustment for Input Offset Voltage	(Note 7)	7.5			mV
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Slew Rate (unity gain)	V_{IN} = ±10V	0.3	0.42		V/μs
Noise	Bandwidth = 5kHz			15	μV RMS
	Bandwidth = 5kHz			40	μV Peak
The Following Specifications Apply for Min ≤ T_A ≤ Max					
Input Offset Voltage				4.0	mV
Average Input Offset Voltage Drift				15	μV/°C
Input Offset Current	$T_{A(max)}$			30	nA
	$T_{A(min)}$			70	nA
Average Input Offset Current Drift	25°C ≤ T_A ≤ Max			200	pA/°C
	Min ≤ T_A ≤ 25°C			500	pA/°C
Input Bias Current (Note 5)	$T_{A(max)}$	1.0		110	nA
	$T_{A(min)}$	1.0		265	nA
Output Short Circuit Current	$T_{A(max)}$	9.0		40	mA
	$T_{A(min)}$	9.0		55	mA
Power Dissipation	$T_{A(max)}$			135	mW
	$T_{A(min)}$			165	mW
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Large Signal Voltage Gain	±V_{CC} = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	32			V/mV
	±V_{CC} = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV

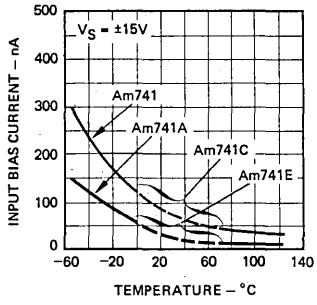
Notes:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. $T_{A(min)}$ for 741A is –55°C and for 741E is 0°C. $T_{A(max)}$ for 741A is +125°C and for 741E is +70°C.
5. Input bias currents are measured individually to specified limits.
6. PSRR measured separately for positive and negative supply to specified limits.
7. V_{OS} adjust is measured in both positive and negative direction to the specified limit.

PERFORMANCE CURVES

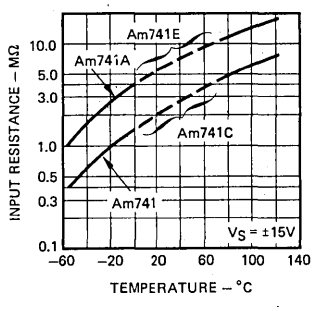
Power Consumption As A Function Of Supply Voltage



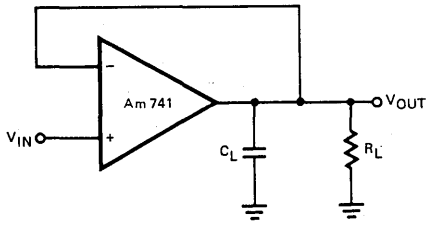
Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature



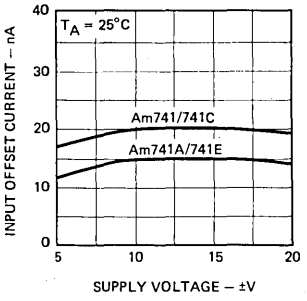
Slew Rate & Transient Response Test Circuit



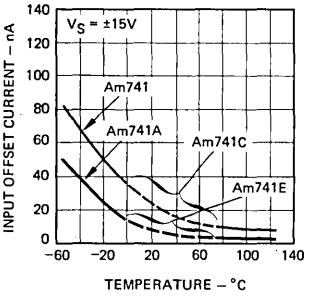
$C_L \leq 100$ pF
$R_L = 2$ kΩ

PERFORMANCE CURVES (Cont.)

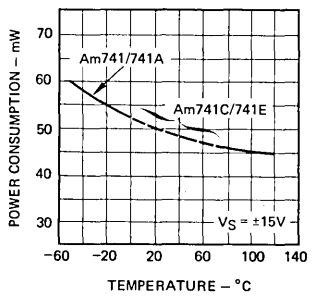
Input Offset Current As A Function Of Supply Voltage



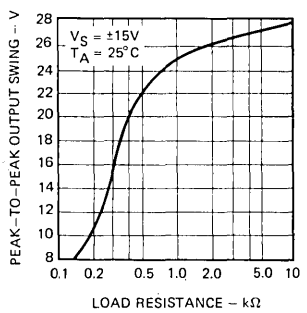
Input Offset Current As A Function Of Ambient Temperature



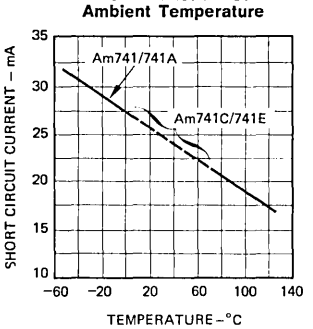
Power Consumption As A Function Of Ambient Temperature



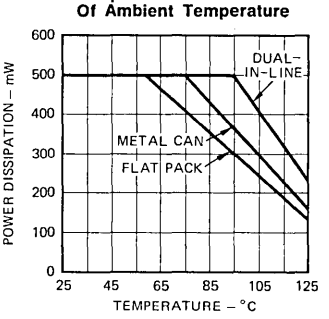
Output Voltage Swing As A Function Of Load Resistance



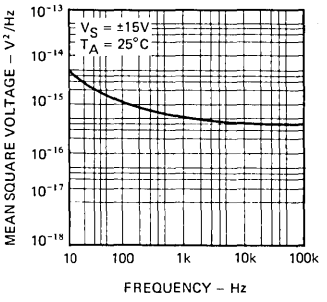
Output Short-Circuit Current As A Function Of Ambient Temperature



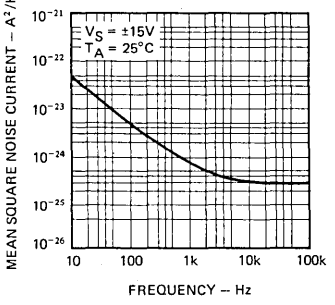
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



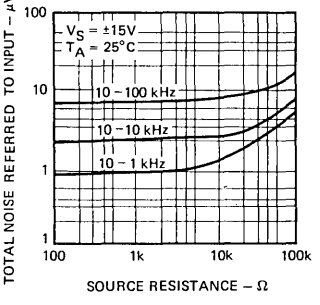
Input Noise Voltage As A Function Of Frequency



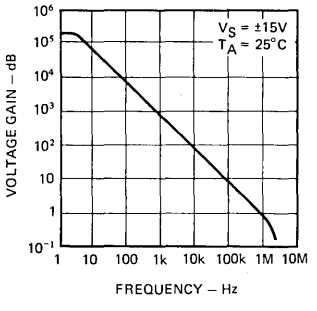
Input Noise Current As A Function Of Frequency



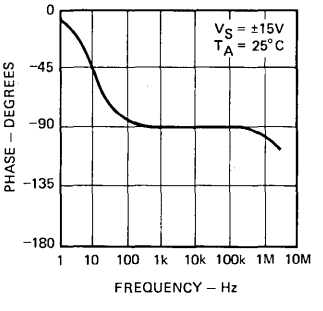
Broadband Noise For Various Bandwidths



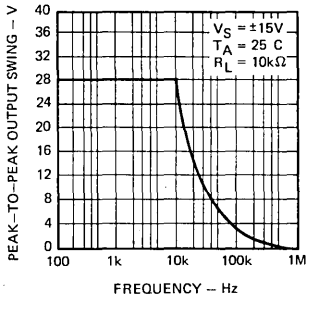
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency

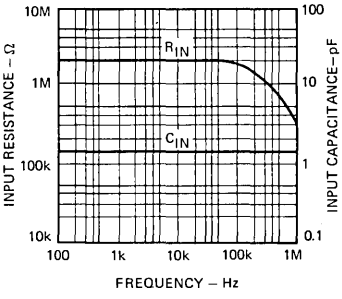


Output Voltage Swing As A Function Of Frequency

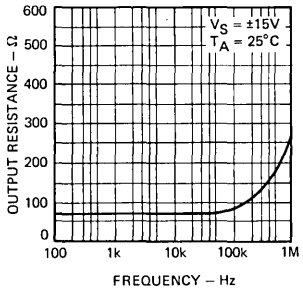


PERFORMANCE CURVES (Cont.)

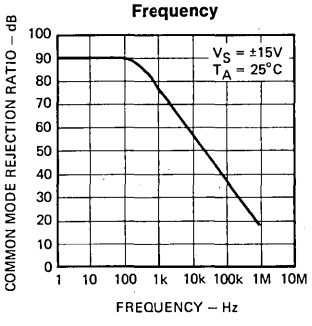
Input Resistance And Input Capacitance As A Function Of Frequency



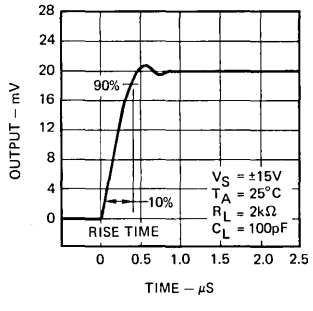
Output Resistance As A Function Of Frequency



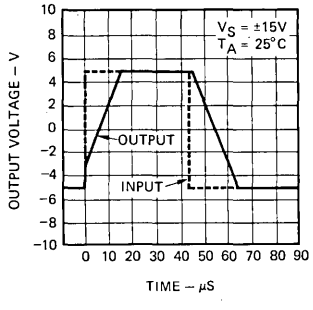
Common Mode Rejection Ratio As A Function Of Frequency



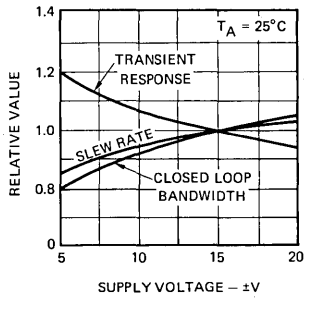
Transient Response



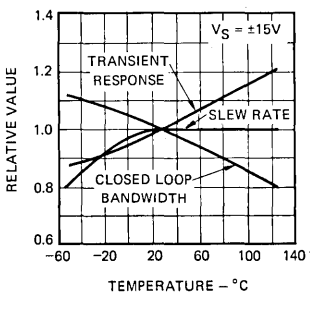
Voltage Follower Large-Signal Pulse Response



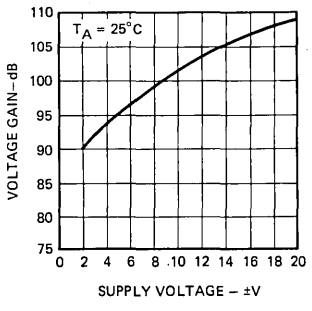
Frequency Characteristics As A Function Of Supply Voltage



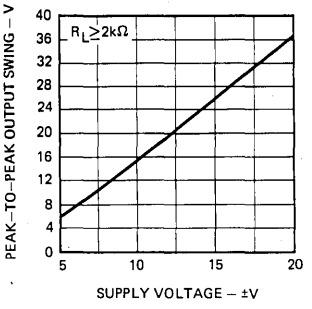
Frequency Characteristics As A Function Of Ambient Temperature



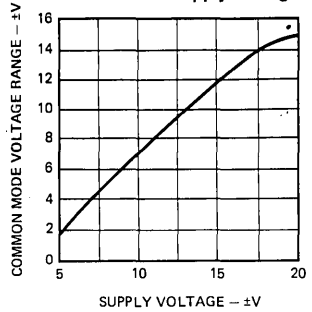
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage

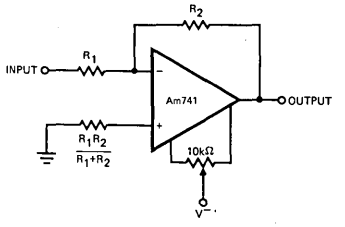


Input Common Mode Voltage Range As A Function Of Supply Voltage



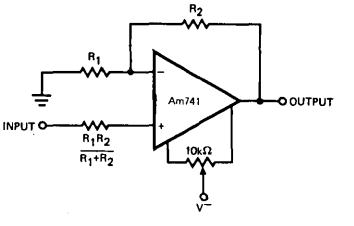
7

INVERTING AMPLIFIER



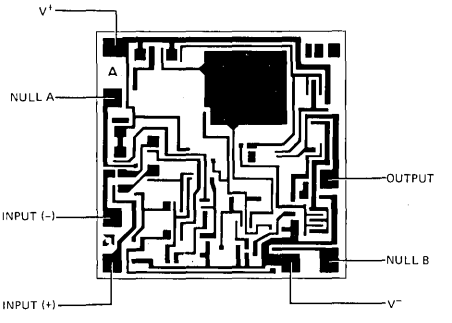
GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

NON-INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

Metallization and Pad Layout



56 X 56 Mils

Am747/747C/747A/747E

Dual Frequency-Compensated Operational Amplifiers

Description:

The Am747 Series Dual Frequency-Compensated Operational Amplifiers are functionally, electrically, and pin-for pin equivalent to the Fairchild μA747 series. They are available in the hermetic metal can, dual-in-line and flat packages as well as plastic dual-in-line.

The Am747A and Am747E are tested to the electrical characteristics of the current revision of MIL-M-38510/10102.

Distinctive Characteristics:

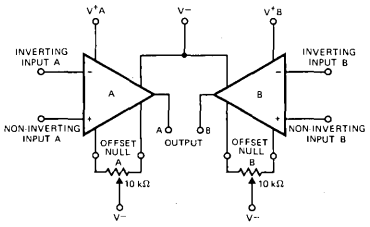
100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

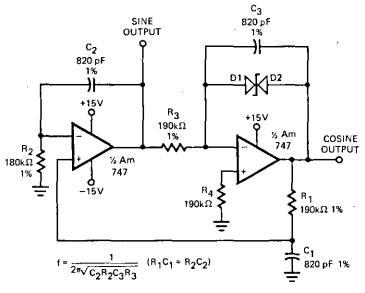
The Am747 is a dual Am741 internally compensated operational amplifier. The Am747 Series are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM

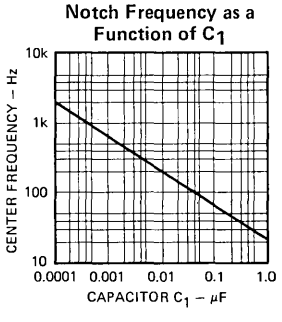


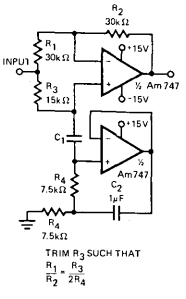
APPLICATIONS

QUADRATURE OSCILLATOR



NOTCH FILTER USING THE Am747 AS A GYRATOR



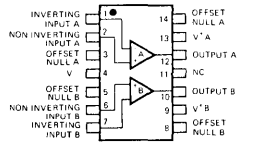


ORDERING INFORMATION

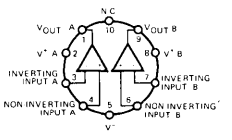
Part Number	Package Type	Temperature Range	Order Number
Am747C	Hermetic DIP	0°C to +70°C	747DC
	Metal Can	0°C to +70°C	747HC
	Molded DIP	0°C to +70°C	747PC
	Dice	0°C to +70°C	747XC
Am747	Hermetic DIP	−55°C to +125°C	747DM
	Metal Can	−55°C to +125°C	747HM
	Flat Pak	−55°C to +125°C	747FM
	Dice	−55°C to +125°C	747XM
Am747E	Hermetic DIP	0°C to +70°C	747EDC
	Metal Can	0°C to +70°C	747EHC
Am747A	Hermetic DIP	−55°C to +125°C	747ADM
	Metal Can	−55°C to +125°C	747AHM
	Flat Pak	−55°C to +125°C	747AFM

CONNECTION DIAGRAMS
Top Views

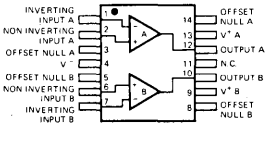
Dual-In-Line



Metal Can



Flat Package



Notes:
1. On Metal Can, pin 5 is connected to case.
2. On DIP, pin 4 is connected to bottom of package.
3. On Flat Package, pin 4 is connected to bottom of package.
4. V^+A and V^+B are connected internally.

MAXIMUM RATINGS

Supply Voltage	
Am747, Am747A, Am747E	±22 V
Am747C	±18 V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800 mW
Flat Package	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V^-	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am747, Am747A	−55°C to +125°C
Am747C, Am747E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS—Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am747C Min.	Am747C Typ.	Am747C Max.	Am747 Min.	Am747 Typ.	Am747 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.4		0.3	0.4		V/μs
Channel Separation	$R_S = 50$ Ω, $R_L \geq 10$ kΩ		120			120		dB
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

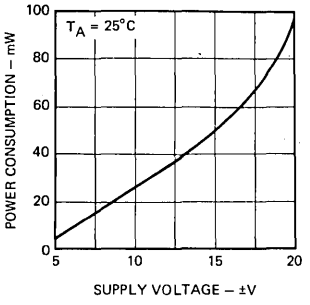
Parameters (see definitions)	Conditions	Am747A/747E Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Input Offset Current			3.0	30	nA
Input Bias Current (Note 5)			30	110	nA
Power Supply Rejection Ratio (Note 6)	V_S = +10, −20; V_S = +20, −10V, R_S = 50Ω		15	50	μV/V
Common Mode Rejection	V_{CM} = ±15V	80			dB
Output Short Circuit Current	$\pm V_{CC}$ = ±15V, V_O = ±15V Short to Other Supply	9		40	mA
Power Dissipation		10		150	mW
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ 10kΩ; V_O = ±15V	50			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ 10kΩ; V_O = ±2V	10			V/mV
Transient Response (unity gain)					
Rise Time			0.30	0.8	μs
Overshoot			5.0	20	%
Adjustment for Input Offset Voltage	(Note 7)	7.5			mV
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Slew Rate (unity gain)	V_{IN} = ±10V	0.3	0.42		V/μs
Noise	Bandwidth = 5kHz			15	μV RMS
	Bandwidth = 5kHz			40	μV Peak
The Following Specifications Apply for Min $\leq T_A \leq$ Max					
Input Offset Voltage				4.0	mV
Average Input Offset Voltage Drift				15	μV/°C
Input Offset Current	$T_{A(max)}$			30	nA
	$T_{A(min)}$			70	nA
Average Input Offset Current Drift	25°C $\leq T_A \leq$ Max			200	pA/°C
	Min $\leq T_A \leq$ 25°C			500	pA/°C
Input Bias Current (Note 5)	$T_{A(max)}$	1.0		110	nA
	$T_{A(min)}$	1.0		265	nA
Output Short Circuit Current	$T_{A(max)}$	9.0		40	mA
	$T_{A(min)}$	9.0		55	mA
Power Dissipation	$T_{A(max)}$			135	mW
	$T_{A(min)}$			165	mW
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	32			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV

Notes:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. $T_{A(min)}$ for 741A is −55°C and for 741E is 0°C. $T_{A(max)}$ for 741A is +125°C and for 741E is +70°C.
5. Input bias currents are measured individually to specified limits.
6. PSRR measured separately for positive and negative supply to specified limits.
7. V_{OS} adjust is measured in both positive and negative direction to the specified limit.

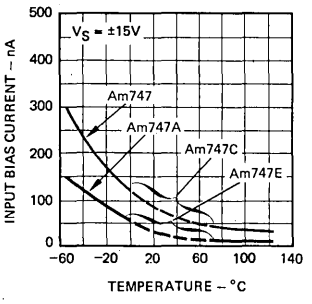
PERFORMANCE CURVES

(Each Amplifier)

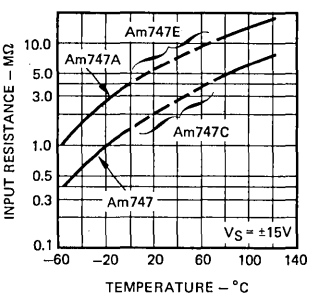
Power Consumption As A Function Of Supply Voltage



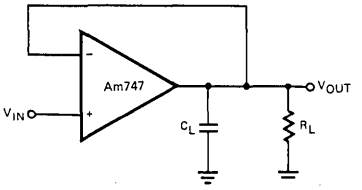
Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature



Transient Response Test Circuit

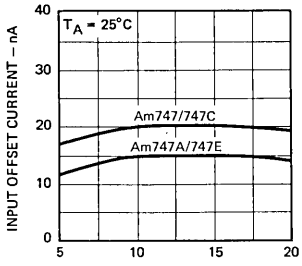


$C_L \leq 100$ pF
$R_L = 2$ kΩ

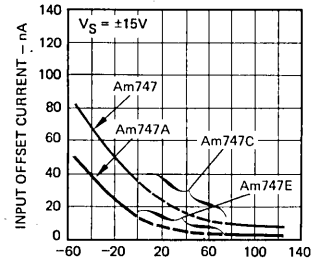
PERFORMANCE CURVES (Cont.)

(Each Amplifier)

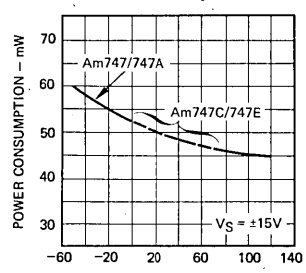
Input Offset Current As A Function Of Supply Voltage



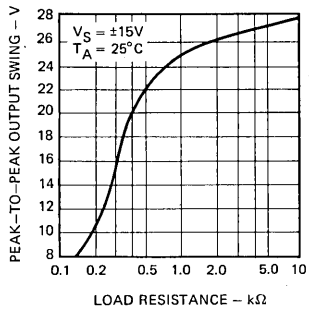
Input Offset Current As A Function Of Ambient Temperature



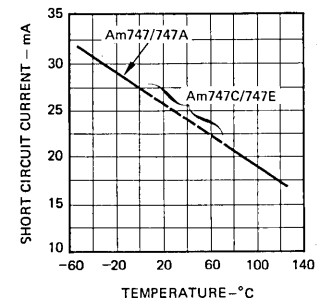
Power Consumption As A Function Of Ambient Temperature



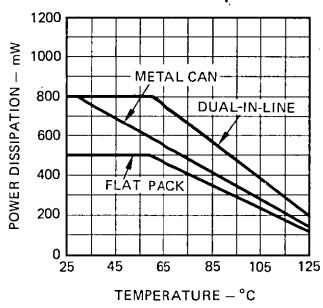
Output Voltage Swing As A Function Of Load Resistance



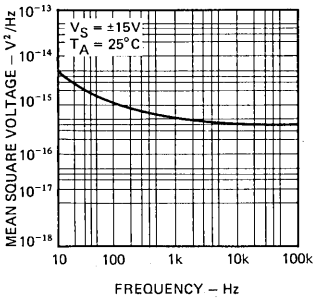
Output Short-Circuit Current As A Function Of Ambient Temperature



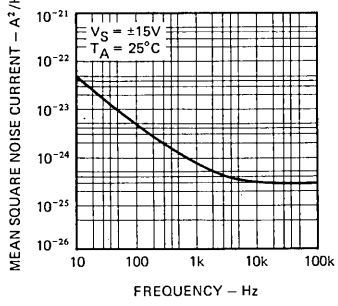
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



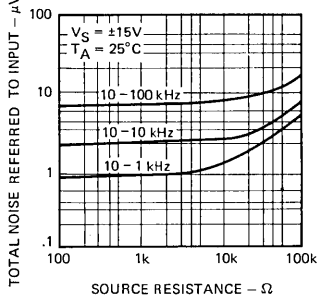
Input Noise Voltage As A Function Of Frequency



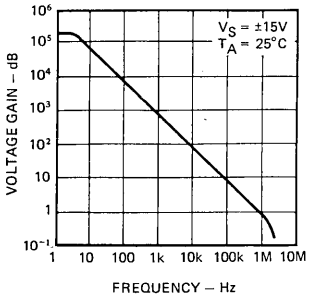
Input Noise Current As A Function Of Frequency



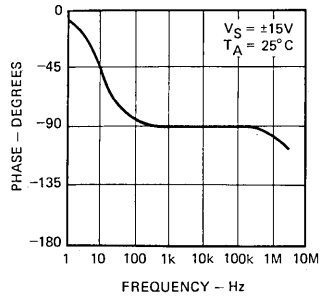
Broadband Noise For Various Bandwidths



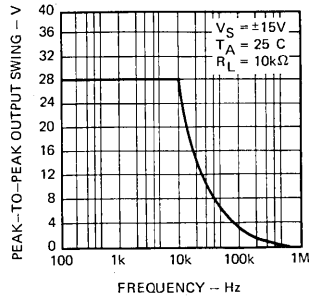
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



Output Voltage Swing As A Function Of Frequency

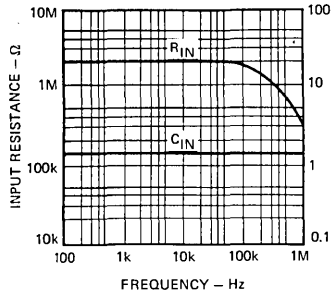


7

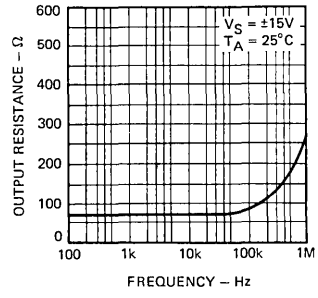
PERFORMANCE CURVES (Cont.)

(Each Amplifier)

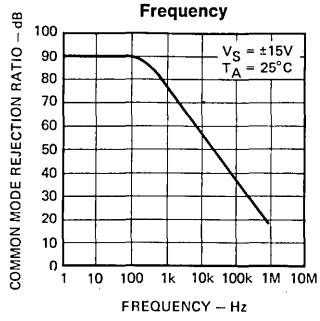
Input Resistance And Input Capacitance As A Function Of Frequency



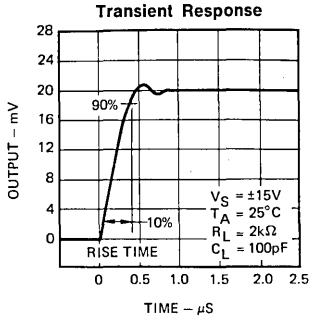
Output Resistance As A Function Of Frequency



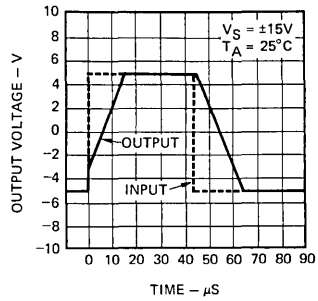
Common Mode Rejection Ratio As A Function Of Frequency



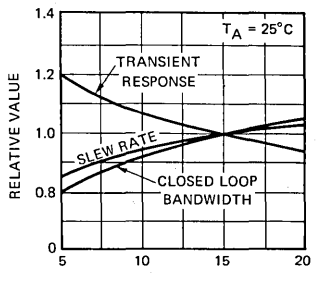
Transient Response



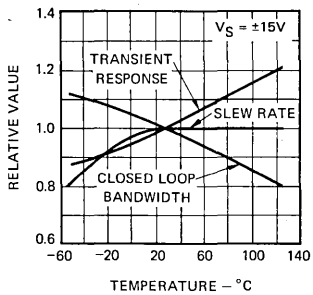
Voltage Follower Large-Signal Pulse Response



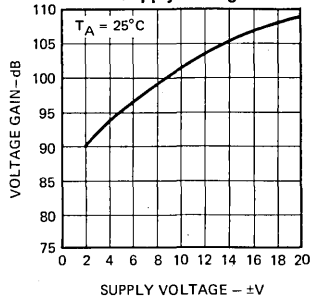
Frequency Characteristics As A Function Of Supply Voltage



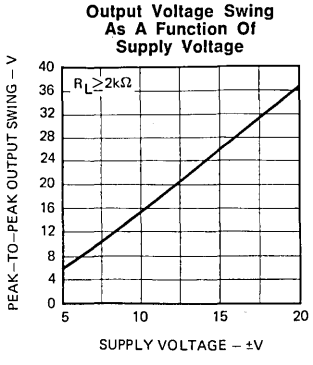
Frequency Characteristics As A Function Of Ambient Temperature



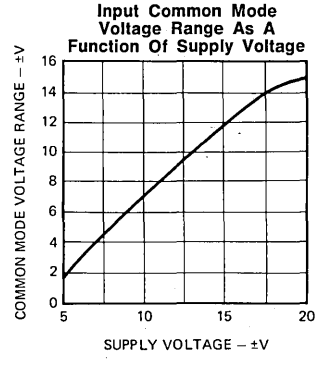
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage

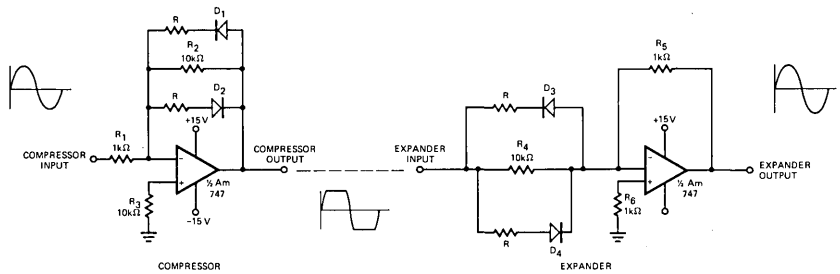


Input Common Mode Voltage Range As A Function Of Supply Voltage



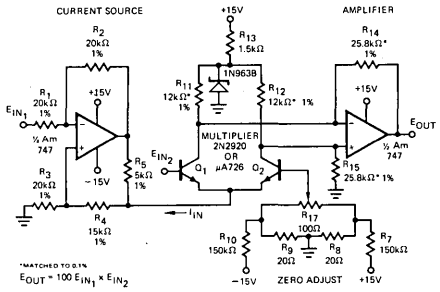
ADDITIONAL APPLICATIONS

COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION/EXPANSION RATIO = R_1/R (10 kΩ ≥ R ≥ 0)
DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

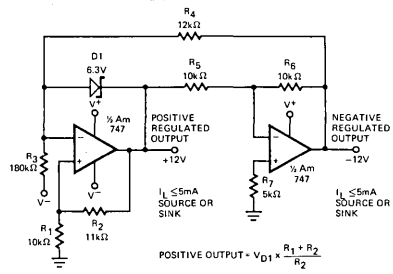
ANALOG MULTIPLIER



*MATCHED TO 0.1%

$E_{OUT} = 100\, E_{IN_1} \times E_{IN_2}$

TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES

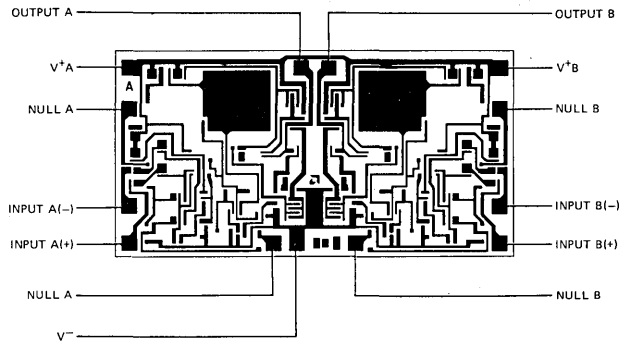


POSITIVE OUTPUT = $V_{D1} \times \frac{R_1 + R_2}{R_2}$

NEGATIVE OUTPUT = −POSITIVE OUTPUT × $\frac{R_6}{R_5}$

7

Metallization and Pad Layout



56 x 106 Mils

SSS725•SSS741•SSS747

High-Performance Operational Amplifiers

Functional Description

The SSS series are high-performance operational amplifiers designed for systems demanding extremely high accuracy. Superior DC and AC characteristics of low input offset voltage, low input offset current, low input bias current and high large signal voltage gain provide performance comparable to discrete or hybrid modules. The SSS series are functionally, electrically and pin-for-pin equivalent to the PMI SSS series.

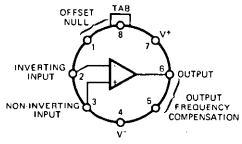
Distinctive Characteristics

- Superior DC and AC characteristics V_{OS}, I_{OS}, A_{VO}, I_B, CMRR, PSRR
- 100% reliability assurance testing in compliance with MIL-STD-883

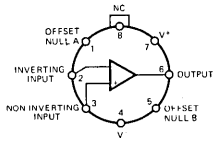
CONNECTION DIAGRAMS

Top View

SSS725 — Metal Cans

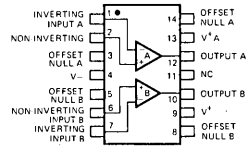


SSS741 — Metal Cans

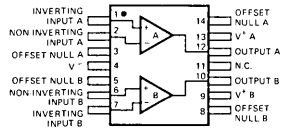


Notes:
(1) All leads through. No pins connected to case on SSS725.
(2) Pin 4 connected to case on SSS741.

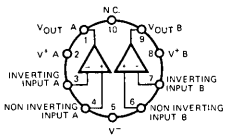
SSS747 — Dual-In-Line



SSS747 — Flat Package



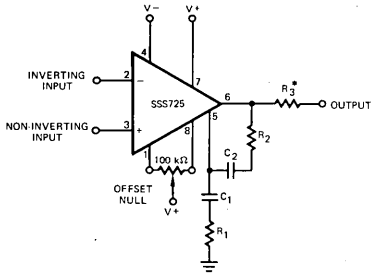
SSS747 — Metal Can



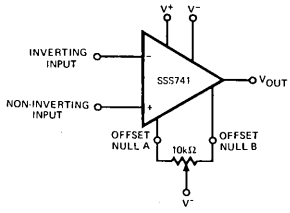
Notes:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 4 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

FUNCTIONAL DIAGRAMS

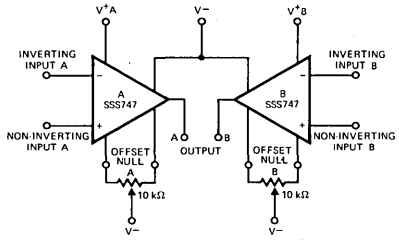
SSS725



SSS741



SSS747



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SSS725J	Metal Can	−55°C - +125°C
SSS725BJ	Metal Can	−25°C - +85°C
SSS725EJ	Metal Can	0°C - +70°C
SSS741J	Metal Can	−55°C - +125°C
SSS741CJ	Metal Can	0°C - +70°C
SSS747K	Metal Can	−55°C - +125°C
SSS747P	Hermetic DIP	−55°C - +125°C
SSS747M	Flat Pak	−55°C - +125°C
SSS747CK	Metal Can	0°C - +70°C
SSS747CP	Hermetic DIP	0°C - +70°C

SSS725 FREQUENCY

Compensation Component Values

A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	–	–
100	47	10	–	–
10	27	50	270	1.5
1	10	50	39	20

* Use $R_3 = 51\,\Omega$ when the amplifier is operated with capacitive loads.

MAXIMUM RATINGS — HIGH-PERFORMANCE INSTRUMENTATION OP AMP — SSS725

Supply Voltage	±22V
Internal Power Dissipation (Note 1) Metal Can (TO-99)	500mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
SSS725	−55°C to +125°C
SSS725B	−25°C to +85°C
SSS725E	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Condition	SSS725/725E Min.	SSS725/725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.5		0.75	mV
I_{os}	Input Offset Current			5.0		5.0	nA
I_B	Input Bias Current			80		80	nA
e_n	Input Noise Voltage (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		15.0 9.0 7.5		15.0 9.0 7.5	nV/√Hz nV/√Hz nV/√Hz
i_n	Input Noise Current (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		1.2 0.6 0.25		1.2 0.6 0.25	pA/√Hz pA/√Hz pA/√Hz
R_{in}	Input Resistance		0.7		0.7		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_o = ±10V	1,000,000		1,000,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0		±12.5 ±12.0 ±11.0		V V V
CMVR	Input Voltage Range		±13.5		±13.5		V
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	120		110		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		5.0		5.0	µV/V
P_d	Power Consumption			120		120	mW
A_{vo}	Large Signal Voltage Gain	$R_L \geq 500\Omega$ V_o = ±0.5V V_s = ±3V	100,000		100,000		
P_d	Power Consumption	V_s = ±3V		6		6	mW

The Following Specifications Apply Over The Operating Temperature Range

Symbol	Parameter	Condition	SSS725 Min.	SSS725 Max.	SSS725E Min.	SSS725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.7		0.6		1.0	mV
	Average Input Offset Voltage Drift (Without external trim) (Note 4)	R_s = 50Ω		2.0		2.0 (Note 3)		2.8 (Note 3)	µV/°C
	Average Input Offset Voltage Drift (With external trim) (Note 4)	R_s = 50Ω		1.0		0.6		1.0 (Note 3)	µV/°C
I_{os}	Input Offset Current	T_A MAX. T_A MIN.		4.0 18.0		5.0 7.0		5.0 14.0	nA nA
	Average Input Offset Current Drift			90		40 (Note 3)		90 (Note 3)	pA/°C
I_B	Input Bias Current	T_A MAX. T_A MIN.		70 180		80 100		80 150	nA nA
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	110		115		106		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		8.0		7.0		8.0	µV/V
A_{vo}	Large Signal Voltage Gain	V_o = ±10V; T_A MAX. $R_L \geq 2k\Omega$; T_A MIN.	1,000,000 500,000		1,000,000 800,000		1,000,000 500,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±12.0		±12.0		±12.0		V

Notes 1. Derate at 6.8mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested. 90% of all units meet these specifications.
4. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

MAXIMUM RATINGS HIGH-PERFORMANCE FREQUENCY COMPENSATED OP AMP SSS741/741C

Supply Voltage	
SSS741	±22V
SSS741C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V^-	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS741	−55°C to +125°C
SSS741C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

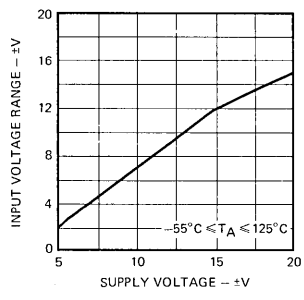
ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions	SSS741 Min.	SSS741 Max.	SSS741C Min.	SSS741C Max.	Units
V_{os}	Input Offset Voltage	$R_s \leq 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L \geq 2k\Omega$ $V_{out} = \pm10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm15V$ $V_s = \pm20V$	±12 ±15		±12		V
CMRR	Common Mode Rejection Ratio	$R_s \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 50k\Omega$		100		150	μV/V
P_d	Power Consumption	$V_s \leq \pm15V$		85		85	mW
The Following Specifications Apply Over the Operating Temperature Range							
V_{os}	Input Offset Voltage	$R_s \leq 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		200	nA
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L \geq 2k\Omega$ $V_{out} = \pm10V$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_s \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 50k\Omega$		100		150	μV/V

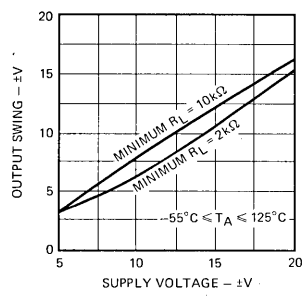
Notes 1. Derate metal can package at 6.8mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. The SSS741 specifications apply for $\pm5V \leq V_s \leq \pm20V$. The SSS741C specifications apply for $V_s = \pm15V$.

GUARANTEED PERFORMANCE

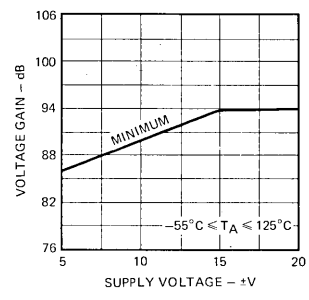
Input Voltage Range



Output Swing



Voltage Gain



MAXIMUM RATINGS HIGH-PERFORMANCE DUAL FREQUENCY COMPENSATED OP AMP SSS747/747C

Supply Voltage	
SSS747	±22V
SSS747C	±18V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800mW
Flat Package	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V^-	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS747	−55°C to +125°C
SSS747C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

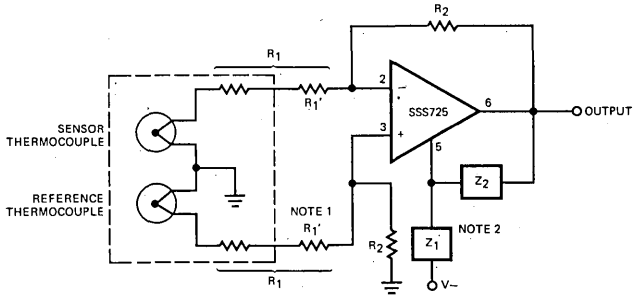
Symbol	Parameter	Conditions	SSS747 Min.	SSS747 Max.	SSS747C Min.	SSS747C Max.	Units
V_{os}	Input Offset Voltage	$R_S \leq 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_S = \pm 15V$, $V_{out} = \pm 10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_S = \pm 15V$ $V_S = \pm 20V$	 ±15		±12		V V
CMRR	Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50k\Omega$		100		150	μV/V
P_d	Power Dissipation	$V_S \leq \pm 15V$		85		85	mW
CS	Channel Separation		100				dB
The Following Specifications Apply Over The Operating Temperature Ranges							
V_{os}	Input Offset Voltage	$R_S \leq 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		150	nA
A_{vo}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_S = \pm 20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50k\Omega$		100		150	μV/V

Notes 1. Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the dual-in-line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.
4. The SSS747 specifications apply for $\pm 5V \leq V_S \leq \pm 20V$, unless otherwise noted. The SSS747C specifications apply for $\pm 5V \leq V_S \leq \pm 15V$, unless otherwise noted.

TYPICAL APPLICATIONS

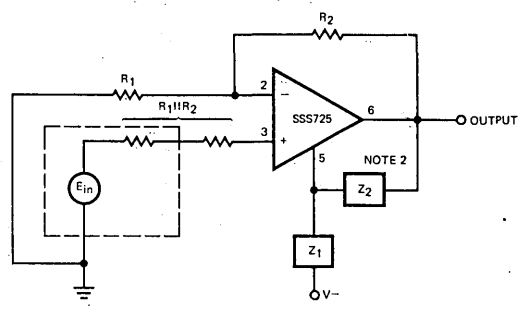
SSS725

Thermocouple Amplifier



$$A_V = \frac{-R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

High Gain Non-Inverting Amplifier



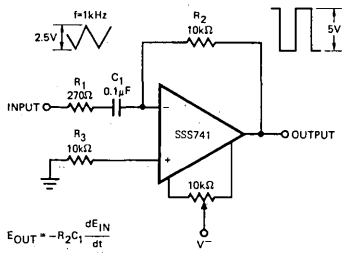
$$A_V = \frac{R_1 + R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

Notes:
(1) R_1' is adjusted so that the sum of R_1' and the thermocouple circuit resistance equals the correct value for R_1.
(2) See Frequency Compensation Circuit.

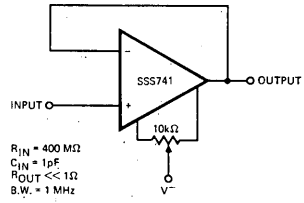
For ideal resistors and open loop gain greater than 10^6, in a +1000 gain configuration, the gain error will be less than 0.1% and input impedance will be greater than 700MΩ.

SSS741

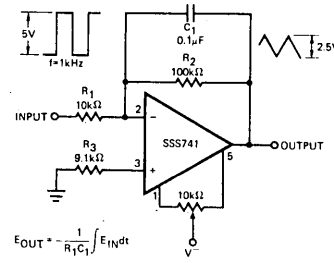
Differentiator



Unity Gain Voltage Follower

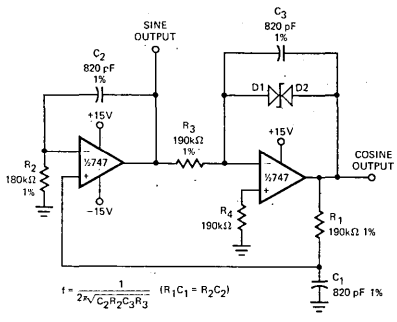


Integrator

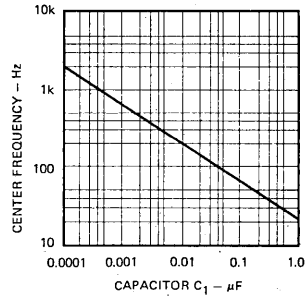


SSS747

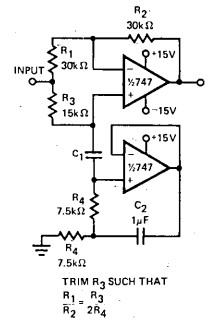
Quadrature Oscillator



Notch Frequency as a Function of C_1

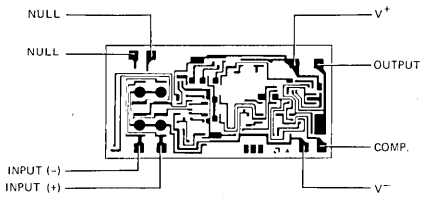


Notch Filter Using the 747 as a Gyrator

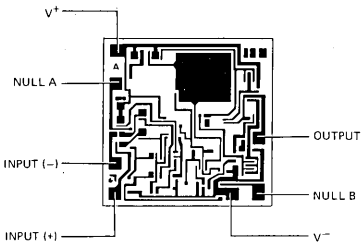


Metallization and Pad Layouts

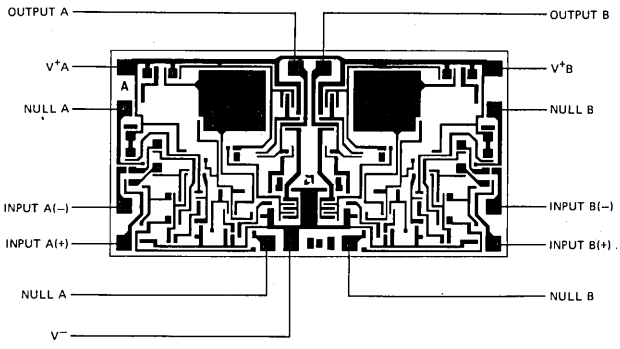
SSS725



SSS741



SSS747



7

Am748/748C

Operational Amplifier

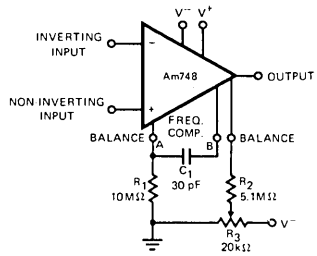
Description: The Am748/748C Monolithic Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA748 and μA748C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD 883 Class B.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION:

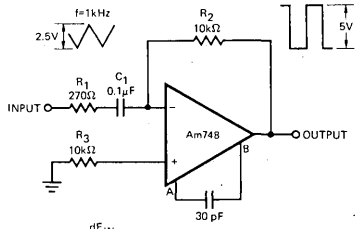
The Am748 and Am748C are differential input class AB output amplifiers intended for general-purpose application. They are protected against faults at input and output, and may be frequency compensated with an external 30 pF capacitor.

FUNCTIONAL DIAGRAM



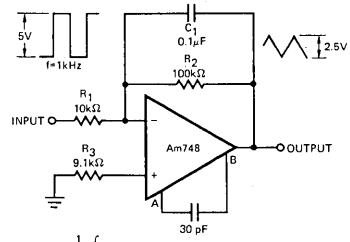
APPLICATIONS

DIFFERENTIATOR



$$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$$

INTEGRATOR



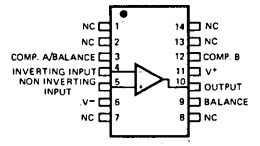
$$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$$

ORDERING INFORMATION

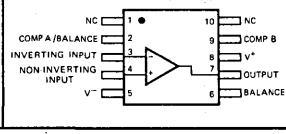
Part Number	Package Type	Temperature Range	Order Number
Am748C	Metal Can	0°C to +70°C	748HC
	Hermetic DIP	0°C to +70°C	748DC
	Dice	0°C to +70°C	748XC
Am748	Metal Can	−55°C to +125°C	748HM
	Hermetic DIP	−55°C to +125°C	748DM
	Dice	−55°C to +125°C	748XM

CONNECTION DIAGRAMS
Top Views

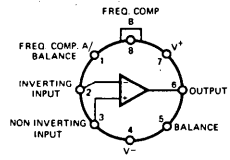
Dual-In-Line



Flat Package



Metal Can



NOTES:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 6 is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	
Am748	±22 V
Am748C	±18 V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am748	−55°C to +125°C
Am748C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

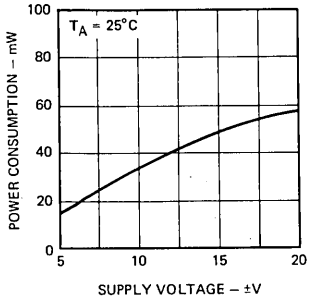
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am748C Min.	Am748C Typ.	Am748C Max.	Am748 Min.	Am748 Typ.	Am748 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

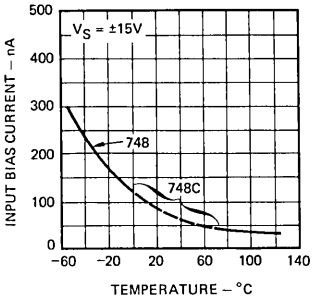
Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PERFORMANCE CURVES

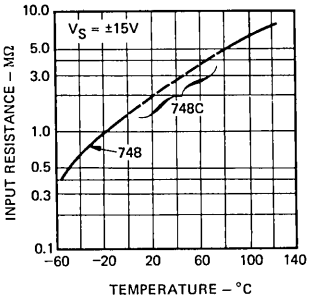
Power Consumption As A Function Of Supply Voltage



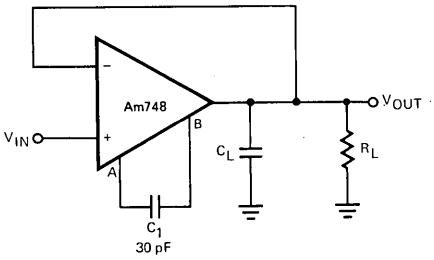
Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature

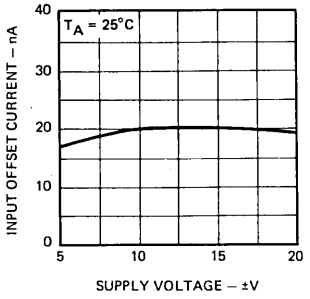


TRANSIENT RESPONSE TEST CIRCUIT

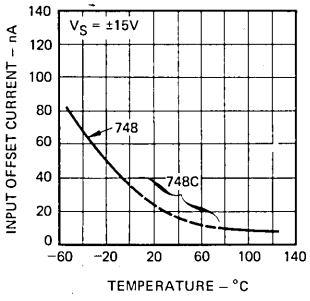


PERFORMANCE CURVES

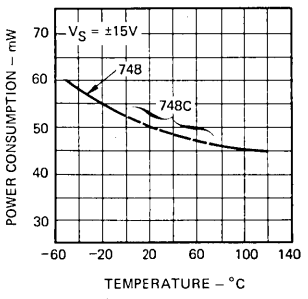
Input Offset Current As A Function Of Supply Voltage



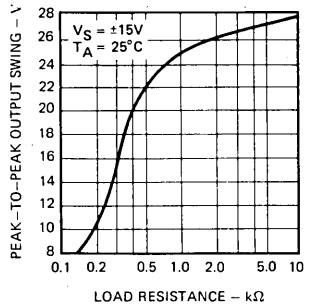
Input Offset Current As A Function Of Ambient Temperature



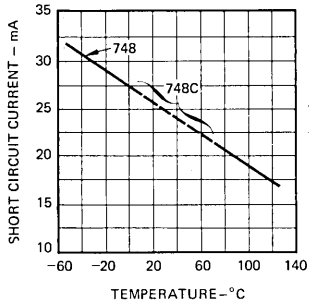
Power Consumption As A Function Of Ambient Temperature



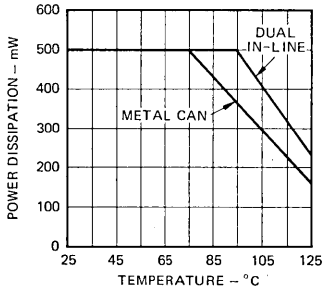
Output Voltage Swing As A Function Of Load Resistance



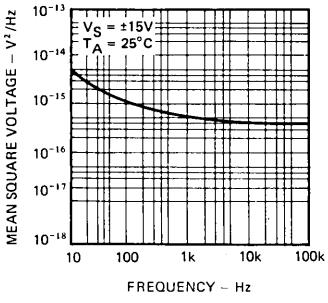
Output Short-Circuit Current As A Function Of Ambient Temperature



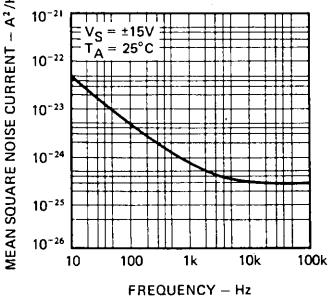
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



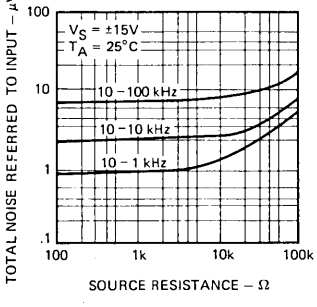
Input Noise Voltage As A Function Of Frequency



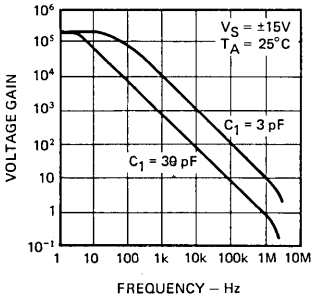
Input Noise Current As A Function Of Frequency



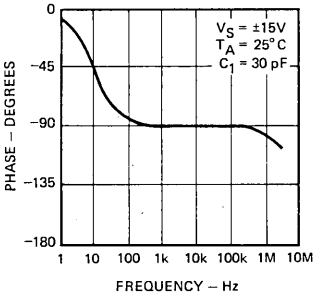
Broadband Noise For Various Bandwidths



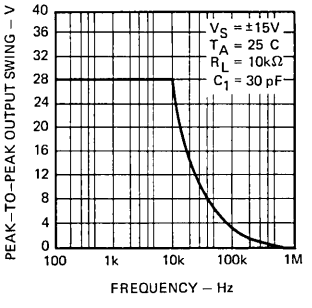
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



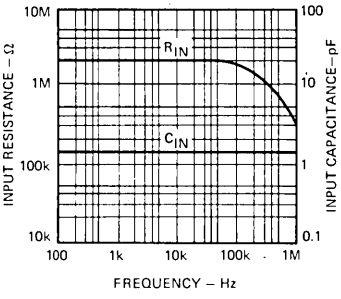
Output Voltage Swing As A Function Of Frequency



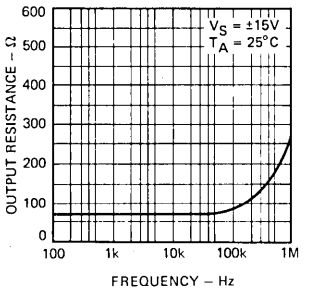
7

PERFORMANCE CURVES

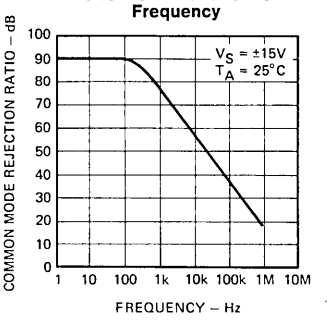
Input Resistance And Input Capacitance As A Function Of Frequency



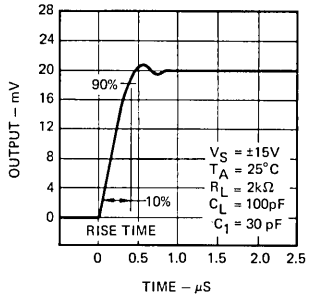
Output Resistance As A Function Of Frequency



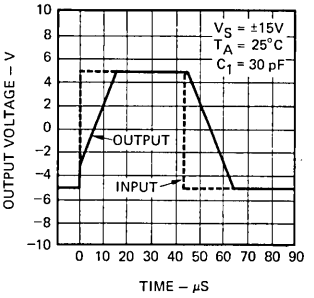
Common Mode Rejection Ratio As A Function Of Frequency



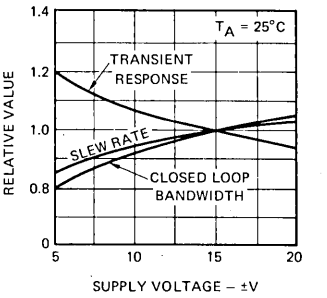
Transient Response



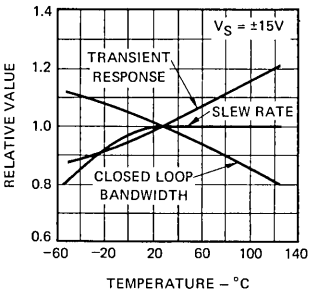
Voltage Follower Large-Signal Pulse Response



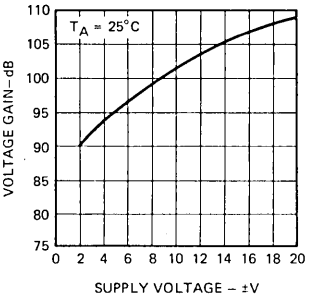
Frequency Characteristics As A Function Of Supply Voltage



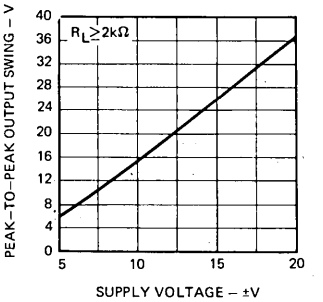
Frequency Characteristics As A Function Of Ambient Temperature



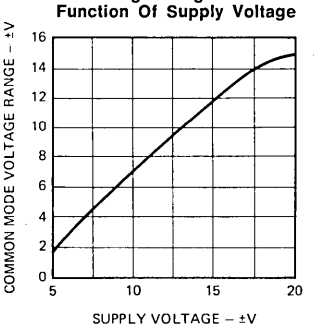
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage

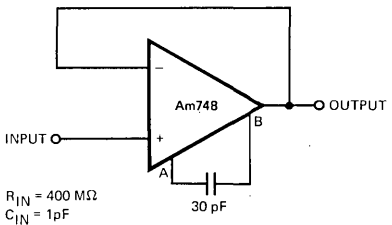


Input Common Mode Voltage Range As A Function Of Supply Voltage



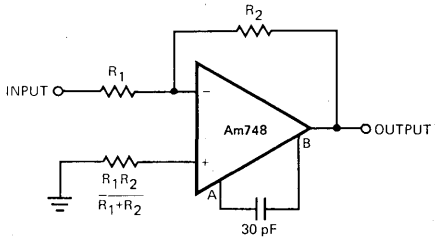
BASIC Am748 AMPLIFIER APPLICATIONS

UNITY GAIN VOLTAGE FOLLOWER



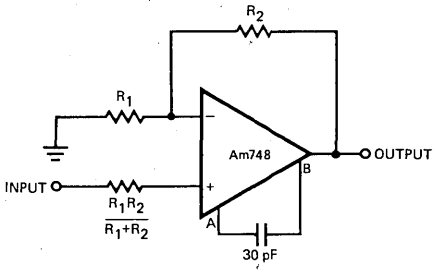
R_{IN} = 400 MΩ
C_{IN} = 1pF
$R_{OUT} << 1Ω$
B.W. = 1 MHz

INVERTING AMPLIFIER



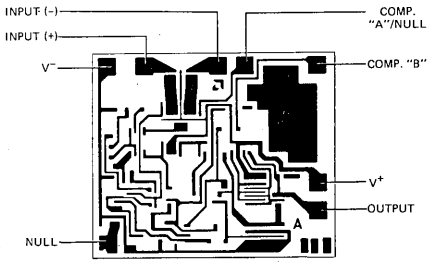
GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

NON-INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

Metallization and Pad Layout



49 x 56 Mils

Am1501

Dual Operational Amplifiers

Distinctive Characteristics

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

FUNCTIONAL DESCRIPTION

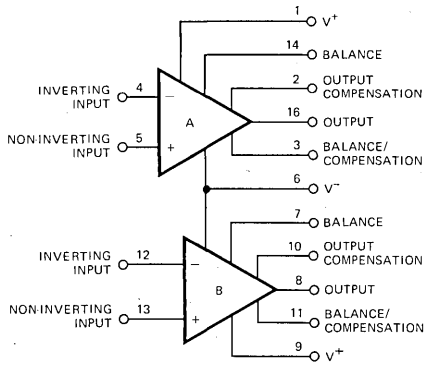
The Am1501 series are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the Am1501 series amplifiers for low level and general purpose applications.

DESCRIPTION

The Am1501 series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. They are functionally, electrically and pin-for-pin equivalent to the National LH2101A series. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles.

The Am1501M is specified for operation over the −55°C to +125°C military temperature range. The Am1501L is specified for operation over the −25°C to +85°C temperature range. The Am1501C is specified for operation over the 0°C to +70°C temperature range.

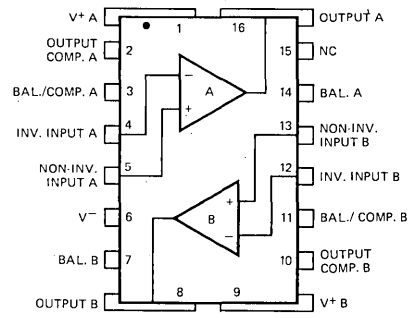
FUNCTIONAL DIAGRAM



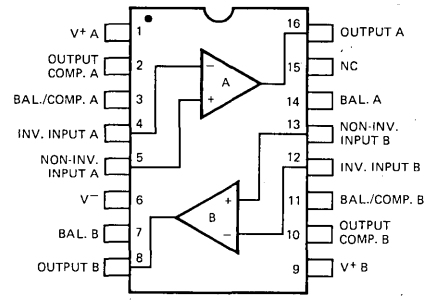
CONNECTION DIAGRAMS

Top Views

Dual-In-Line



Flat Package



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1501C	Hermetic Dip	0°C to +70°C	AM1501DC
	Flat Pak	0°C to +70°C	AM1501FC
Am1501L	Hermetic Dip	−25°C to +85°C	AM1501DL
	Flat Pak	−25°C to +85°C	AM1501FL
Am1501M	Hermetic Dip	−55°C to +125°C	AM1501DM
	Flat Pak	−55°C to +125°C	AM1501FM

MAXIMUM RATINGS

Supply Voltage	
Am1501M, Am1501L	±22V
Am1501C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am1501M	−55°C to +125°C
Am1501L	−25°C to + 85°C
Am1501C	0°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)
(EACH AMPLIFIER)

Parameter (see definitions)	Conditions	Am1501C Min.	Am1501C Typ.	Am1501C Max.	Am1501M Am1501L Min.	Am1501M Am1501L Typ.	Am1501M Am1501L Max.	Units
Input Offset Voltage	$R_S \leq 50k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3.0	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2.0		1.5	4.0		MΩ
Supply Current (Total Both Amplifiers)	V_S = ±20V					3.6	6.0	mA
	V_S = ±15V		3.6	6.0				
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L > 2.0k\Omega$	25	160		50	160		V/mV
Slew Rate	V_S = ±20V, A_V = +1.0	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min.)} \leq T_A \leq T_{A(max.)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{A(max.)}$		0.01	0.3		0.01	0.1	nA/°C
	$T_{A(min.)} \leq T_A \leq$ 25°C		0.02	0.6		0.02	0.2	
Input Bias Current				300			100	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L > 2.0k\Omega$	25			25			V/mV
Input Voltage Range	V_S = ±20V				±15			V
	V_S = ±15V	+15,−12						
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		80	96		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2.0kΩ	±10	±13		±10	±13		
Supply Current (Total Both Amplifiers)	T_A = +125°C, V_S = ±20V					2.4	5.0	mA

Notes:
1. The maximum junction temperature of the Am1501M is 150°C, while that of the Am1501L and Am1501C is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C, unless otherwise specified. With the Am1501L, however, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C. For the Am1501C these specifications apply for 0°C ≤ T_A ≤ +70°C, ±5V and ≤ V_S ≤ ±15V. Supply current and input voltage range are specified as V_S = ±15V for the Am1501C. C_1 = 30pF unless otherwise specified.

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

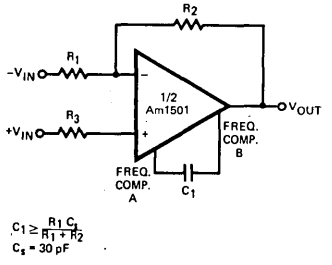


Figure 1

Two Pole Compensation

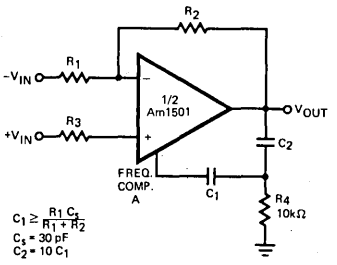


Figure 2

Feedforward Compensation

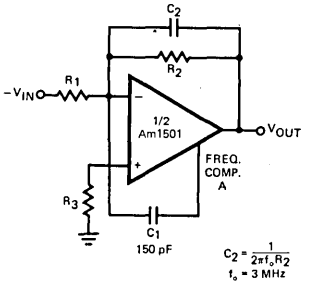


Figure 3

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance

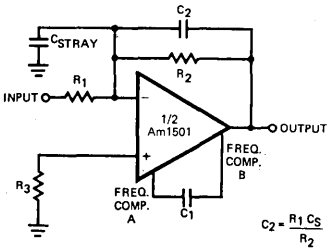


Figure 4

Isolating Large Capacitive Loads

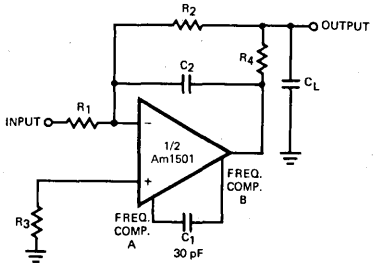
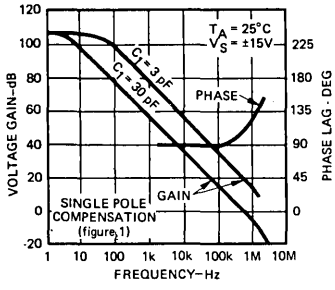


Figure 5

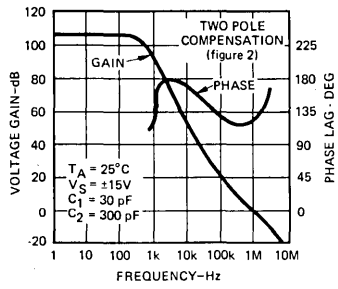
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PERFORMANCE CURVES (Note 3)

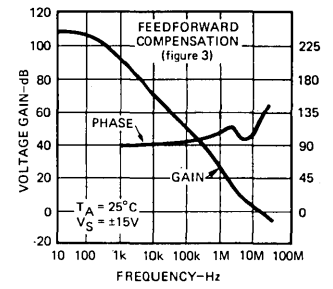
Open Loop Frequency Response



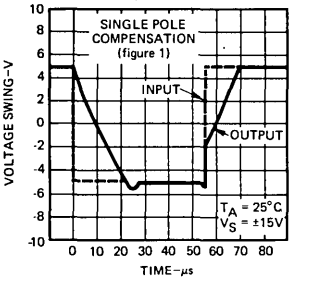
Open Loop Frequency Response



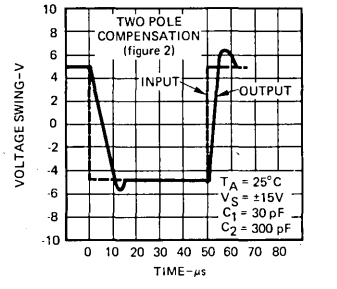
Open Loop Frequency Response



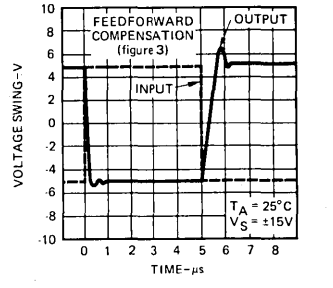
Voltage Follower Pulse Response



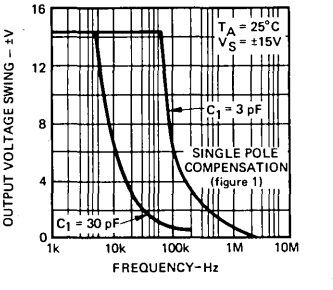
Voltage Follower Pulse Response



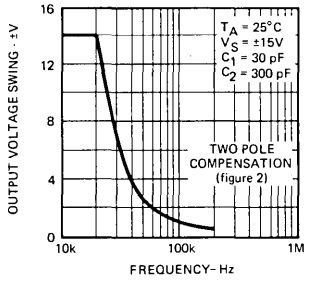
Inverter Pulse Response



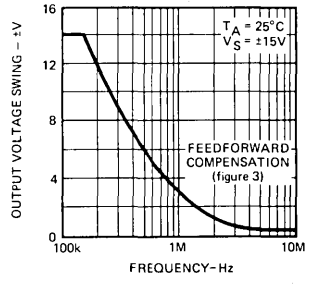
Large Signal Frequency Response



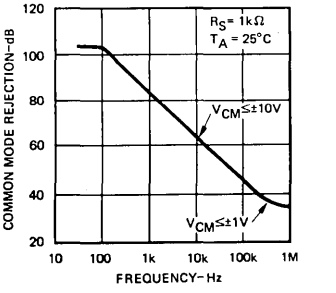
Large Signal Frequency Response



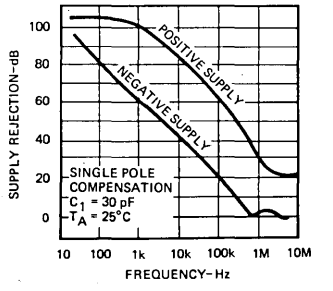
Large Signal Frequency Response



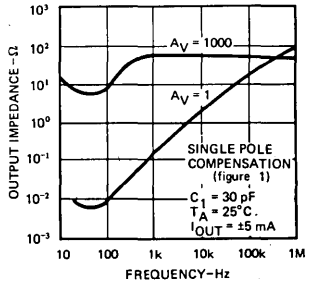
Common Mode Rejection



Power Supply Rejection



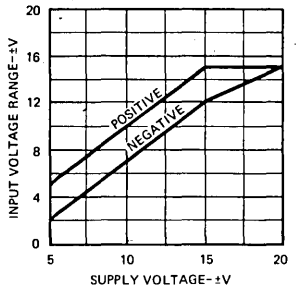
Closed Loop Output Impedance



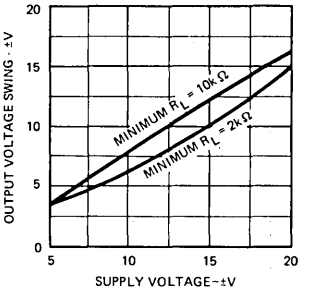
7

GUARANTEED PERFORMANCE CURVES (Note 3)
(Curves apply over the Operating Temperature Ranges)

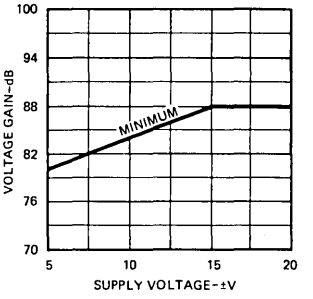
Input Voltage Range



Output Swing

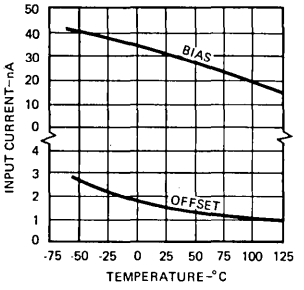


Voltage Gain

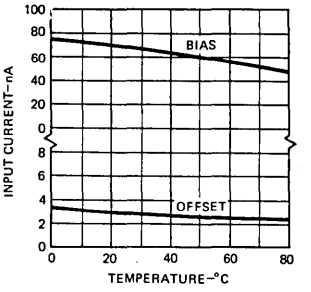


PERFORMANCE CURVES (Note 3)

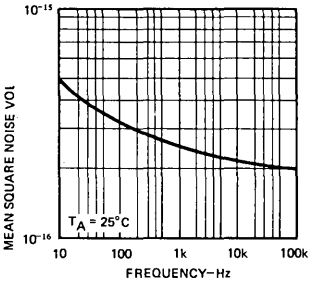
Input Current – Am1501M, L



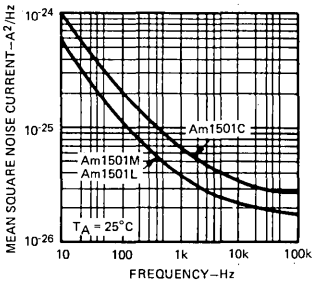
Input Current – Am1501C



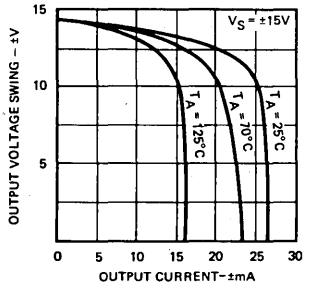
Input Noise Voltage



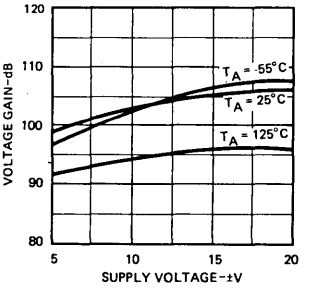
Input Noise Current



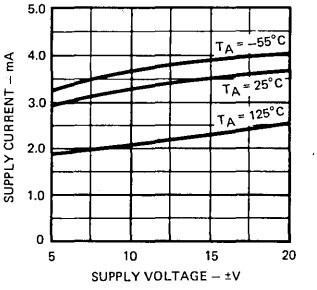
Current Limiting



Voltage Gain



Supply Current



Am1558/1458

Dual Frequency Compensated Operational Amplifiers

Description

The Am1558 and Am1458 Dual Frequency Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Motorola MC1558 and MC1438. Both are available in the hermetic metal can package.

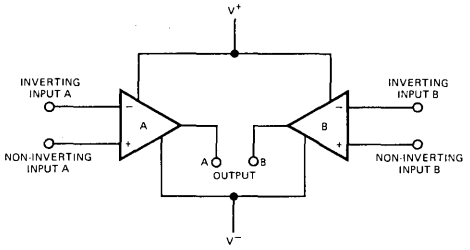
Distinctive Characteristics

- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883
- Electrically tested and optically inspected dice for the assemblers of hybrid circuits

FUNCTIONAL DESCRIPTION

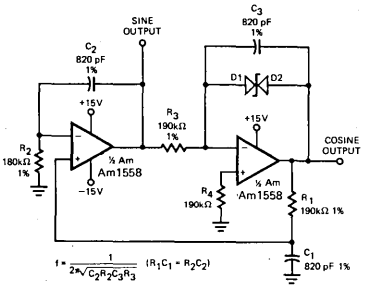
The Am1558 is a dual 741 internally compensated operational amplifier. The Am1558 and Am1458 are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM

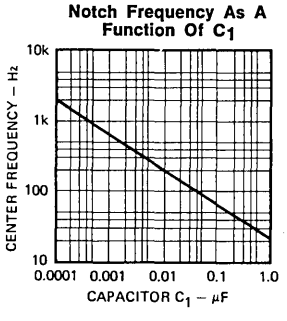


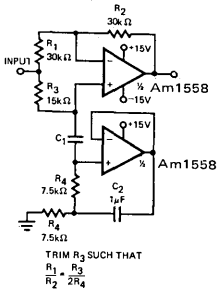
APPLICATIONS

QUADRATURE OSCILLATOR



NOTCH FILTER USING THE 1558 AS A GYRATOR



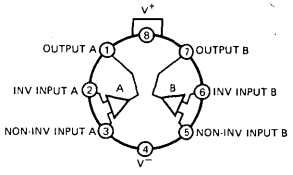


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1458	Metal Can	0°C to +70°C	AM1458H
	Dice	0°C to +70°C	LD1458
Am1558	Metal Can	−55°C to +125°C	AM1558H
	Dice	−55°C to +125°C	LD1558

See Am747 for dice layout

CONNECTION DIAGRAM
Top View

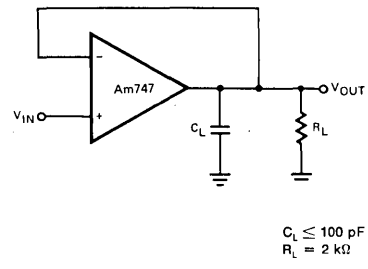


Note: Pin 4 Connected to Case.

MAXIMUM RATINGS

Supply Voltage	
Am1558	±22V
Am1458	±18V
Internal Power Dissipation (Note 1)	
Metal Can	800mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am1558	-55°C to +125°C
Am1458	0°C to + 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Transient Response Test Circuit



$C_L \leq 100$ pF
$R_L = 2$ kΩ

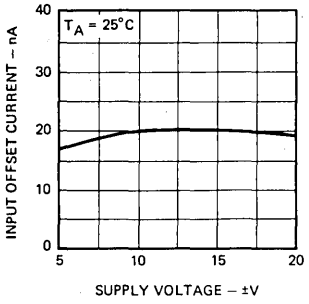
ELECTRICAL CHARACTERISTICS—Each Amplifier (V_S = ±15V, T_A = 25°C unless otherwise specified)

Parameter (see definitions)	Conditions	Am1458 Min.	Am1458 Typ.	Am1458 Max.	Am1558 Min.	Am1558 Typ.	Am1558 Max.	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_{OUT} = ±10V	20	100		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Current (Both Amplifiers)			3.4	5.6		3.4	5.6	mA
Power Consumption (Both Amplifiers)			100	170		100	170	mW
Transient Response (Unity Gain) Risetime Overshoot	V_{IN} = 20mV, R_L = 2.0kΩ, $C_L \leq$ 100pF		 0.3 5.0			 0.3 5.0		 μs %
Slew Rate	$R_L \geq 2.0k\Omega$	0.3	0.5		0.3	0.5		V/μs
Channel Separation	R_S = 50Ω, $R_L \geq 10k\Omega$		120			120		dB
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			6.0	mV
Input Offset Current	T_A MAX. T_A MIN.		9.0 35	300 300		7.0 85	200 500	nA
Input Bias Current	T_A MAX. T_A MIN.		0.04 0.13	0.8 0.8		0.03 0.3	0.5 1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_{OUT} = ±10V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2.0k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
Supply Current (Both Amplifiers)	T_A MAX. T_A MIN.		1.6 1.8	3.3 3.3		3.0 4.0	5.0 6.6	mA
Power Consumption (Both Amplifiers)	T_A MAX. T_A MIN.		100 110	170 200		90 120	150 200	mW

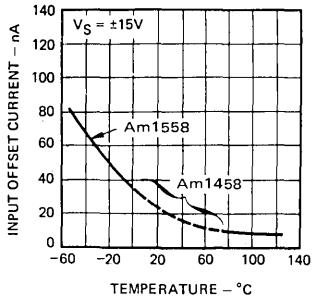
Notes: 1. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 30°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to +125°C case temperature or +60°C ambient temperature for each side.

PERFORMANCE CURVES
(Each Amplifier)

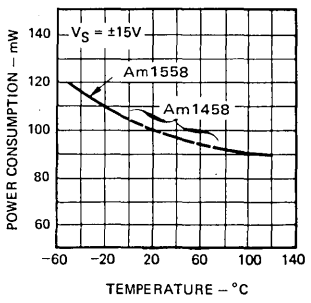
Input Offset Current As A Function Of Supply Voltage



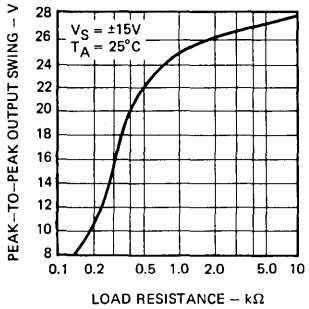
Input Offset Current As A Function Of Ambient Temperature



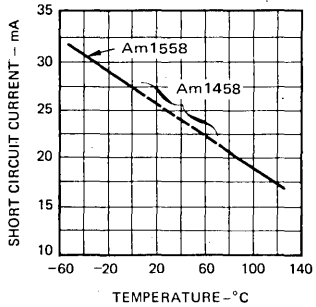
Power Consumption As A Function Of Ambient Temperature



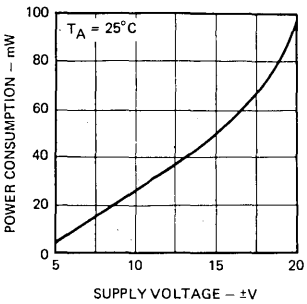
Output Voltage Swing As A Function Of Load Resistance



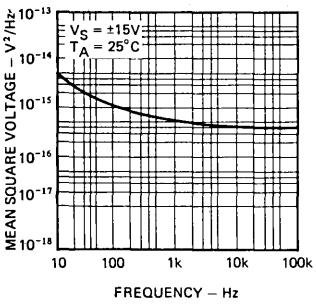
Output Short-Circuit Current As A Function Of Ambient Temperature



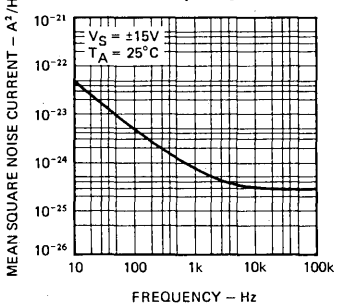
Power Consumption As A Function Of Supply Voltage



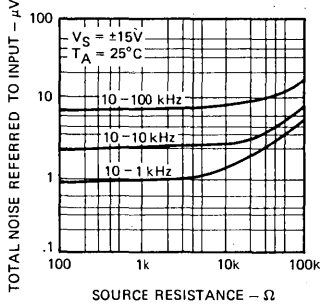
Input Noise Voltage As A Function Of Frequency



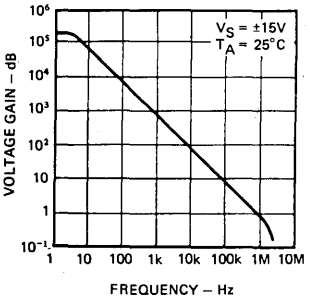
Input Noise Current As A Function Of Frequency



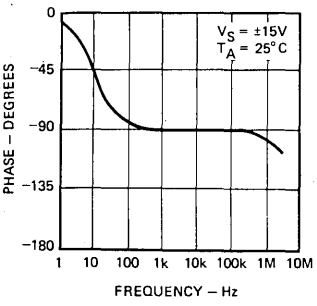
Broadband Noise For Various Bandwidths



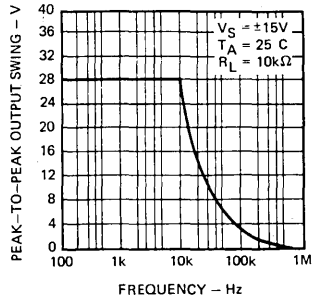
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



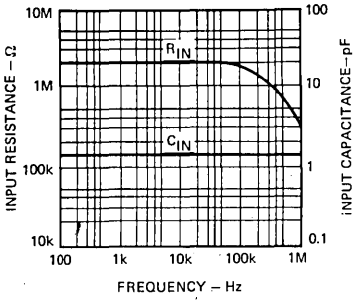
Output Voltage Swing As A Function Of Frequency



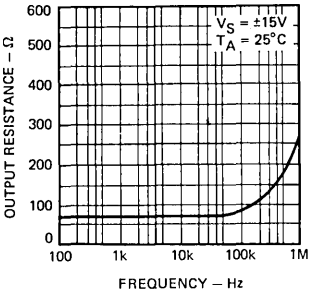
7

PERFORMANCE CURVES
(Each Amplifier)

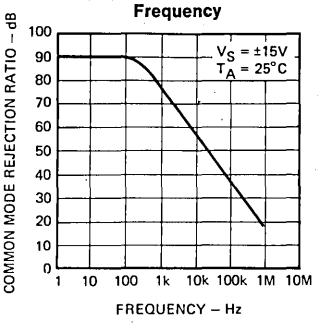
Input Resistance And Input Capacitance As A Function Of Frequency



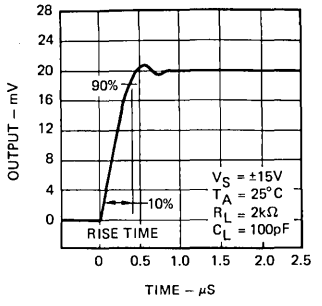
Output Resistance As A Function Of Frequency



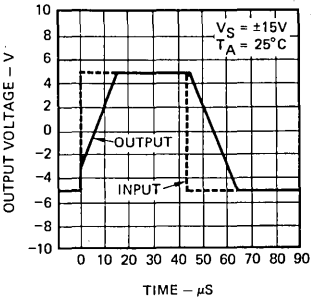
Common Mode Rejection Ratio As A Function Of Frequency



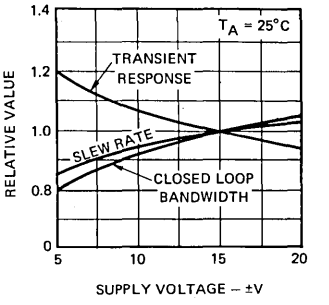
Transient Response



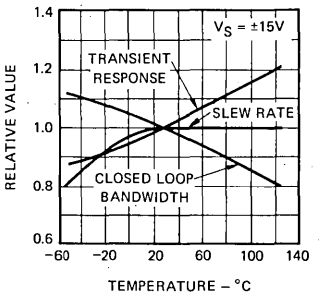
Voltage Follower Large-Signal Pulse Response



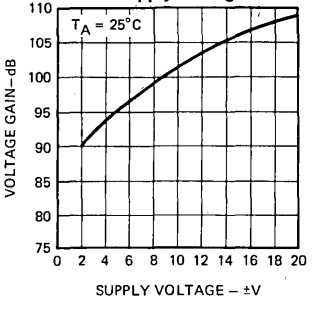
Frequency Characteristics As A Function Of Supply Voltage



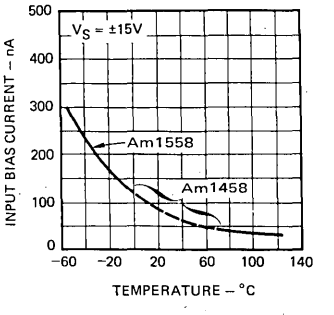
Frequency Characteristics As A Function Of Ambient Temperature



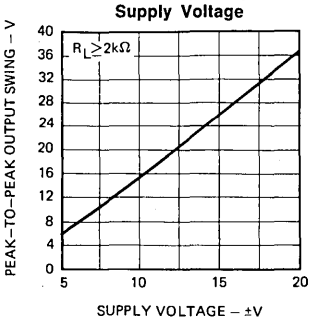
Open Loop Voltage Gain As A Function Of Supply Voltage



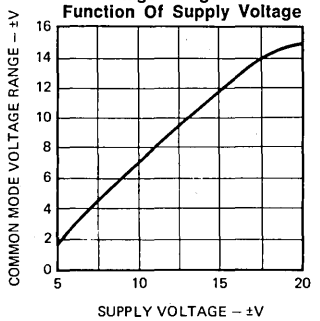
Input Bias Current As A Function Of Ambient Temperature



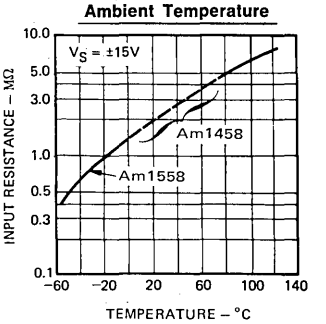
Output Voltage Swing As A Function Of Supply Voltage



Input Common Mode Voltage Range As A Function Of Supply Voltage



Input Resistance As A Function Of Ambient Temperature



LH2101A/LH2201A/LH2301A

Dual Operational Amplifiers

Distinctive Characteristics

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

FUNCTIONAL DESCRIPTION

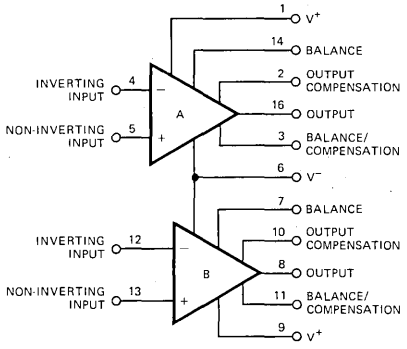
The LH2101A series are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the LH2101A series amplifiers for low level and general purpose applications.

DESCRIPTION

The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. They are functionally electrically and pin for pin equivalent to the National LH2101A series. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles.

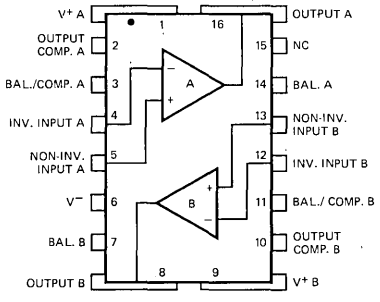
The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

FUNCTIONAL DIAGRAM



CONNECTION DIAGRAMS
Top Views

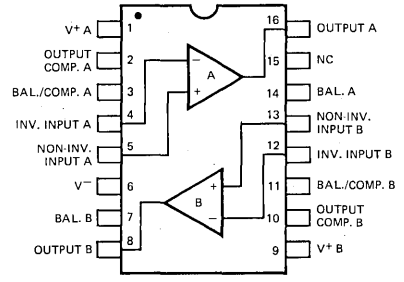
Dual-In-Line



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2301A	DIP	0°C to +70°C	LH2301AD
	Flat Pak	0°C to +70°C	LH2301AF
LH2201A	DIP	-25°C to +85°C	LH2201AD
	Flat Pak	-25°C to +85°C	LH2201AF
LH2101A	DIP	−55°C to +125°C	LH2101AD
	Flat Pak	−55°C to +125°C	LH2101AF

Flat Package



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS

Supply Voltage	
LH2101A, LH2201A	±22V
LH2301A	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LH2101A	−55°C to +125°C
LH2201A	−25°C to +85°C
LH2301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)
(Each Amplifier)

Parameter (see definitions)	Conditions	LH2301A Min.	LH2301A Typ.	LH2301A Max.	LH2101A LH2201A Min.	LH2101A LH2201A Typ.	LH2101A LH2201A Max.	Units
Input Offset Voltage	$R_S \leq 50k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3.0	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2.0		1.5	4.0		MΩ
Supply Current (Total Both Amplifiers)	V_S = ±20V					3.6	6.0	mA
	V_S = ±15V		3.6	6.0				
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L > 2k\Omega$	25	160		50	160		V/mV
Slew Rate	V_S = ±20V, A_V = +1	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(MIN)} \leq T_A \leq T_{A(MAX)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{A(MAX)}$		0.01	0.3		0.01	0.1	nA/°C
	$T_{A(MIN)} \leq T_A \leq$ 25°C		0.02	0.6		0.02	0.2	
Input Bias Current				300			100	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L > 2k\Omega$	25			25			V/mV
Input Voltage Range	V_S = ±20V				±15			Volts
	V_S = ±15V	+15,−12						
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		80	96		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		Volts
	R_L = 2kΩ	±10	±13		±10	±13		
Supply Current (Total Both Amplifiers)	T_A = +125°C, V_S = ±20V					2.4	5.0	mA

Notes: 1. The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A and LH2301A is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3. These specifications apply for ±5V ≤ $V_S \leq$ +20V and −55°C ≤ $T_A \leq$ 125°C, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to −25°C ≤ $T_A \leq$ 85°C. For the LH2301A these specifications apply for 0°C ≤ $T_A \leq$ 70°C, ±5V and ≤ $V_S \leq$ ±15V. Supply current and input voltage range are specified as V_S = ±5V for the LH2301A. C_1 = 30pF unless otherwise specified.

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

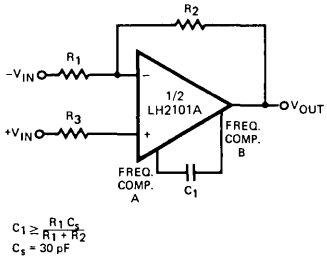


Figure 1

Two Pole Compensation

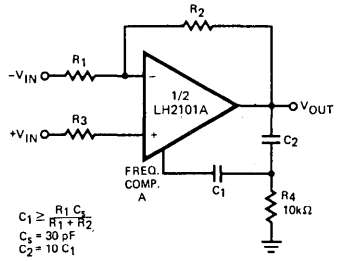


Figure 2

Feedforward Compensation

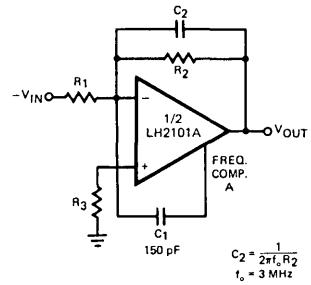


Figure 3

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance

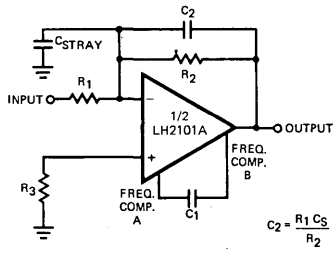


Figure 4

Isolating Large Capacitive Loads

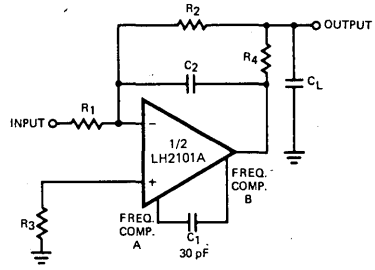
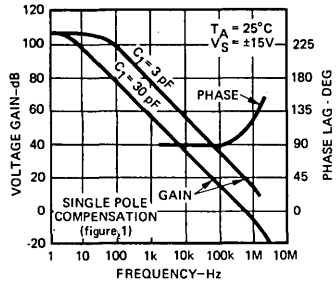


Figure 5

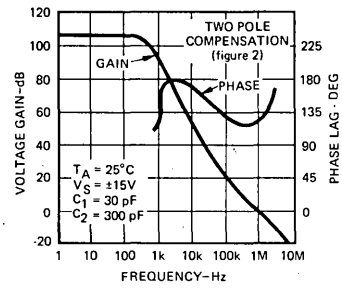
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PERFORMANCE CURVES (Note 3)

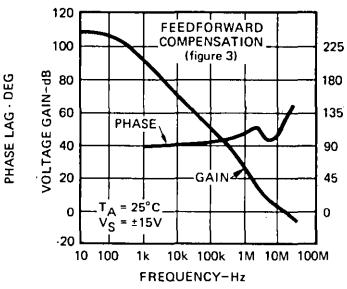
Open Loop Frequency Response



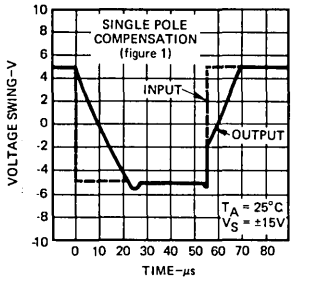
Open Loop Frequency Response



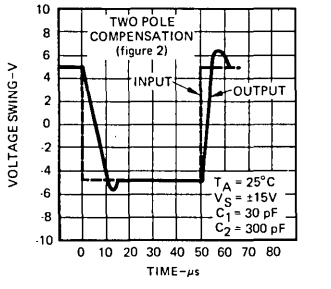
Open Loop Frequency Response



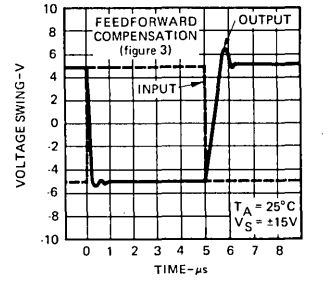
Voltage Follower Pulse Response



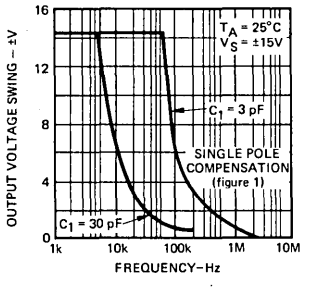
Voltage Follower Pulse Response



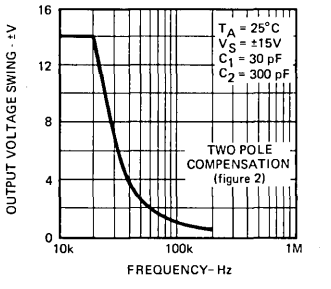
Inverter Pulse Response



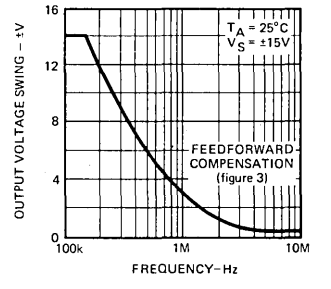
Large Signal Frequency Response



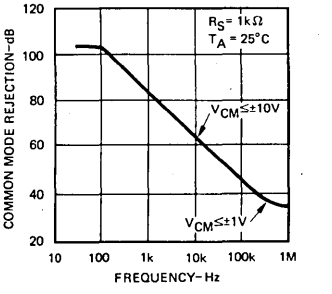
Large Signal Frequency Response



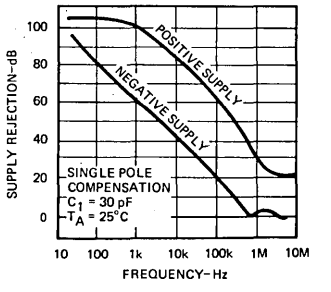
Large Signal Frequency Response



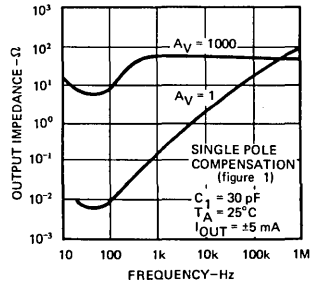
Common Mode Rejection



Power Supply Rejection



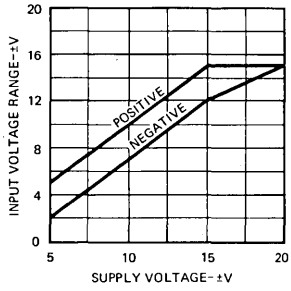
Closed Loop Output Impedance



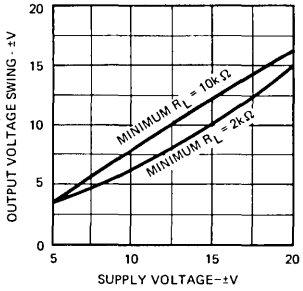
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

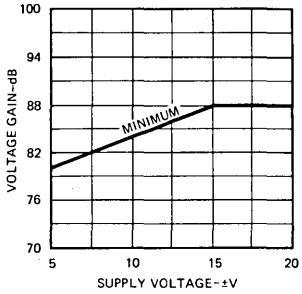
Input Voltage Range



Output Swing

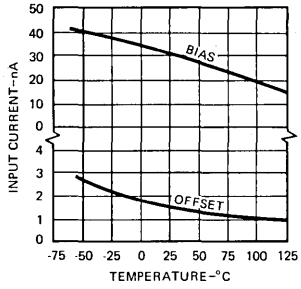


Voltage Gain

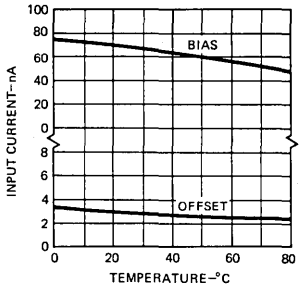


PERFORMANCE CURVES (Note 3)

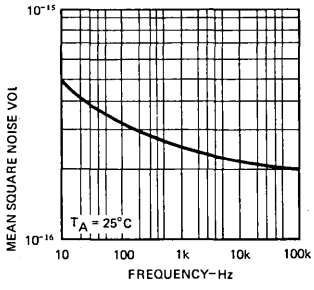
Input Current – LH2101A, LH2201A



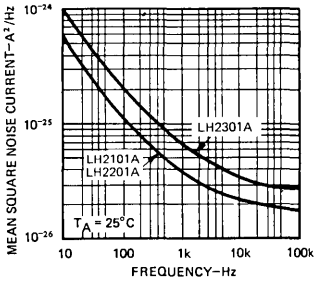
Input Current – LH2301A



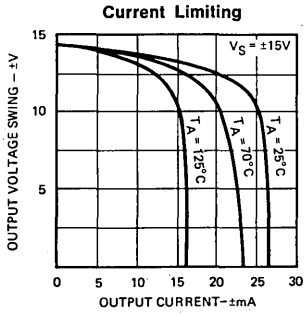
Input Noise Voltage



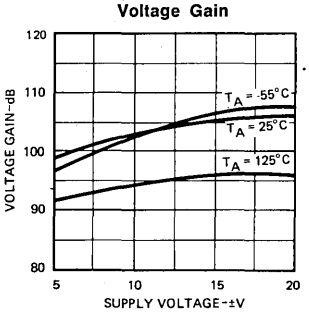
Input Noise Current



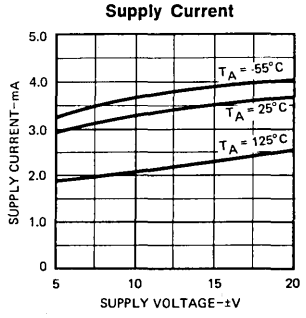
Current Limiting



Voltage Gain



Supply Current



7

Special Functions — Section VIII

Am555

Precision Timer

Distinctive Characteristics

- Timing from microseconds through hours
- 200mA output sink current
- Variable duty cycle
- TTL output compatibility
- Temperature stability of 0.005%/°C
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am555 is a highly stable timing device used to provide accurate time delays or to build precision oscillators. When the device is used as a monostable, the time is precisely controlled using one external resistor and one external capacitor. When the device is used as a precision oscillator, the frequency and duty cycle are controlled by two external resistors and one external capacitor.

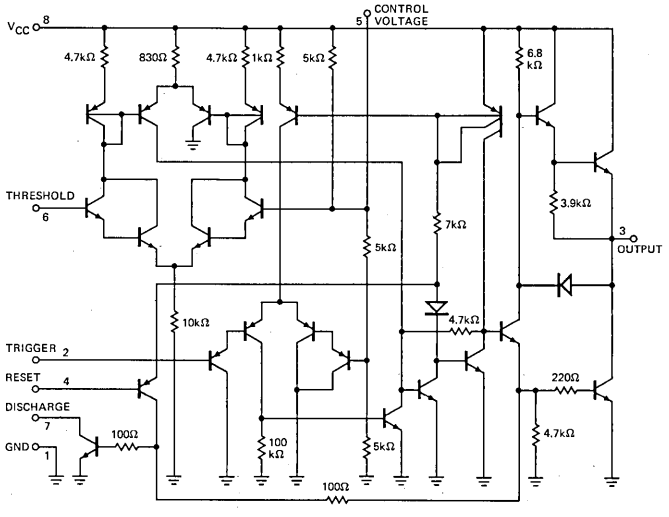
For monostable operation, a HIGH-to-LOW transition is applied to the trigger input. The device is triggered when the input trigger voltage reaches 1/3 V_{CC}.

Once the circuit is triggered, it will remain in the triggered state until the set time has elapsed, even if it is triggered again. The output pulse width is equal to 1.1 $R_A C$.

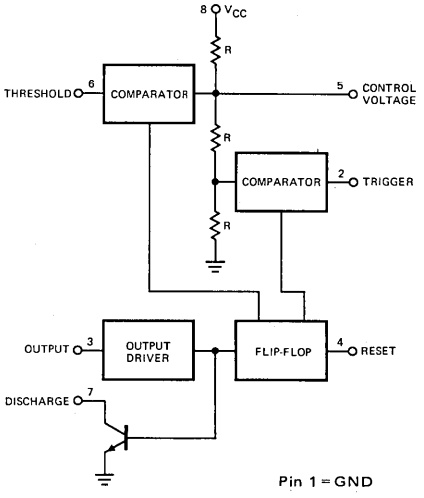
For continuous oscillation, two external resistors are used such that the external capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time is given by $t_{charge} = 0.693 (R_A + R_B)C$ while the discharge time is $t_{discharge} = 0.693 R_B C$.

The device also features a direct reset that overrides all other inputs. When the reset is LOW the output is LOW regardless of the other inputs.

SCHEMATIC DIAGRAM



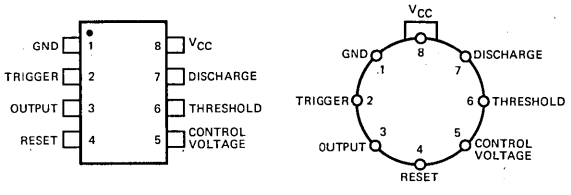
LOGIC SYMBOL



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Mini-DIP	0°C to +70°C	NE555V
TO-5	0°C to +70°C	NE555T
Dice	0°C to +70°C	AM555XC
TO-5	–55°C to +125°C	SE555T
Dice	–55°C to +125°C	AM555XM

CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

8

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	
Military Grade	−55°C to +125°C
Commercial Grade	0°C to +70°C
Supply Voltage to Ground Potential	+18V
Power Dissipation	600mW
Lead Temperature (Soldering, 60 seconds)	+300°C

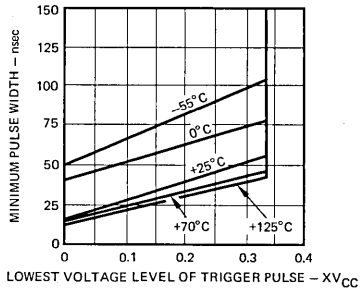
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15V Unless Otherwise Noted)

Parameter	Test Conditions		Military Min.	Military Typ.	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
Supply Voltage			4.5		18	4.5		16	V
Supply Current (LOW State)	V_{CC} = 5V, R_L = ∞			3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Note 1)			10	12		10	15	
Threshold Voltage				2/3			2/3		XV_{CC}
Trigger Voltage	V_{CC} = 15V		4.8	5	5.2		5		V
	V_{CC} = 5V		1.45	1.67	1.9		1.67		
Trigger Current				0.5			0.5		μA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current				0.1			0.1		mA
Threshold Current	(Note 3)			0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V		9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V		2.9	3.33	3.8	2.6	3.33	4	
Output Voltage (LOW)	V_{CC} = 15V	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
		I_{SINK} = 50mA		0.4	0.5		0.4	.75	
		I_{SINK} = 100mA		2.0	2.2		2.0	2.5	
		I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V	I_{SINK} = 8mA		0.1	0.25				V
		I_{SINK} = 5mA					.25	.35	
Output Voltage (HIGH)	V_{CC} = 15V	I_{SOURCE} = −200mA		12.5			12.5		V
	V_{CC} = 15V	I_{SOURCE} = − 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V		3.0	3.3		2.75	3.3		
Timing Error (Monostable)									
Initial Accuracy	R_A = 1kΩ to 100kΩ			0.5	2		1		%
Drift with Temp.	C = 0.1μF (Note 2)			30	100		50		ppm/°C
Drift with Sup. Volt.				0.05	0.2		0.1		%/Volt
Rise Time of Output				100			100		nsec.
Fall Time of Output				100			100		

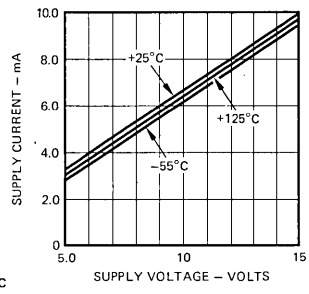
Notes: 1. Supply current when output HIGH typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. Determines the maximum value of $R_A + R_B$. For 15V operation, the max. total R = 20mΩ.

TYPICAL CHARACTERISTICS

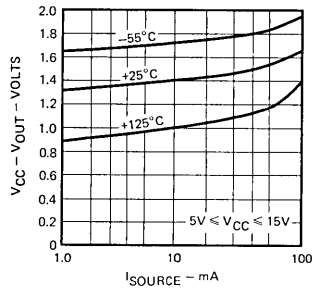
Minimum Pulse Width Required for Triggering



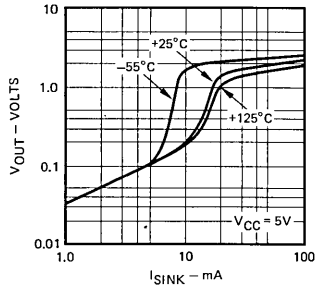
Supply Current Versus Supply Voltage



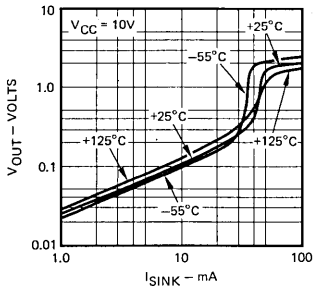
High Output Voltage Versus Output Source Current



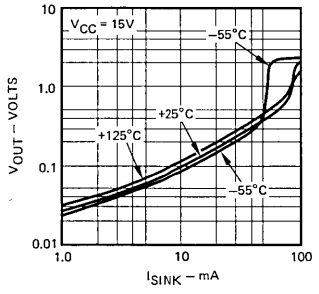
Low Output Voltage Versus Output Sink Current



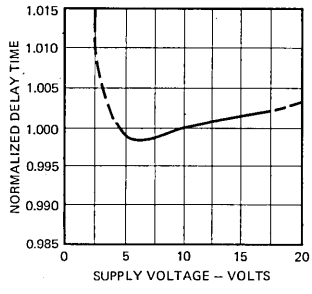
Low Output Voltage Versus Output Sink Current



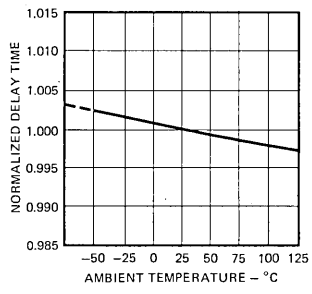
Low Output Voltage Versus Output Sink Current



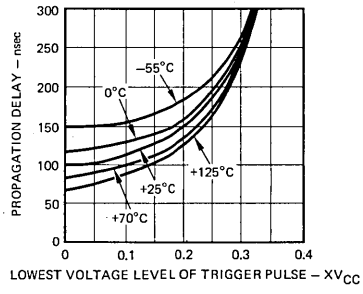
Delay Time Versus Supply Voltage



Delay Time Versus Temperature



Propagation Delay Versus Voltage Level of Trigger Pulse



8

APPLICATIONS

MONOSTABLE OPERATION

When the timer is operated as a monostable multivibrator, one external capacitor, C, and one external resistor, R_A, are used as shown in Figure 1. When the trigger input is reduced below 1/3 V_{CC}, the timer internal flip-flop is set. This releases the short circuit across the external capacitor and the Q output goes HIGH. The voltage across the capacitor begins to rise exponentially with the time constant R_AC. When the capacitor voltage reaches 2/3 V_{CC}, the internal comparator resets the flip-flop and the external capacitor, C, is rapidly discharged provided the trigger voltage is returned above 1/3 V_{CC}. The output is now in LOW state and a new timing cycle may be initiated. The time that the output is in the HIGH state is given by 1.1 R_AC or can be taken directly from Figure 2. Both the charge rate and internal threshold are directly proportional to the V_{CC} supply voltage. Thus, the timer output pulse width is independent of the power supply voltage. If a LOW is applied to the reset input, the output is forced LOW and the external capacitor discharged regardless of the other inputs.

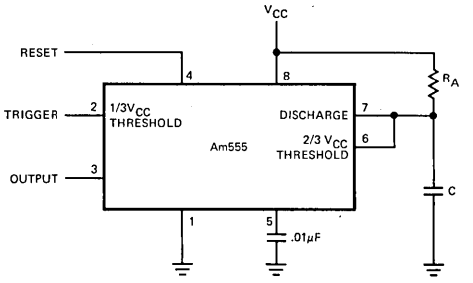


Fig. 1. Monostable Operation of the Am555.

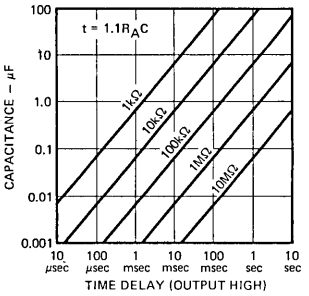


Fig. 2. Monostable Pulse Width.

ASTABLE OPERATION

When the timer is operated in the astable mode, two external resistors, R_A and R_B, and one external capacitor, C, are used as shown in Figure 3. With this connection scheme, the external capacitor, C, charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time (output HIGH) is

$$t_{AB} = 0.693\ (R_A + R_B)\ C$$

The discharge time (output LOW) is

$$t_B = 0.693\ R_BC$$

The total period for one cycle of output HIGH and output LOW is

$$T = t_{AB} + t_B = 0.693\ (R_A + 2R_B)\ C$$

The frequency for this period, T, is

$$f = \frac{1}{T} = \frac{1}{0.693\ (R_A + 2R_B)\ C}$$

The astable free running frequency can also be found from the graph shown in Figure 4. The duty cycle, time the output is LOW divided by the period, is given by

$$D = \frac{t_B}{t_{AB} + t_B} = \frac{R_B}{R_A + 2R_B}$$

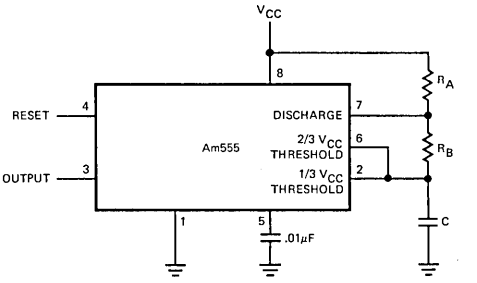


Fig. 3. Astable Operation of the Am555.

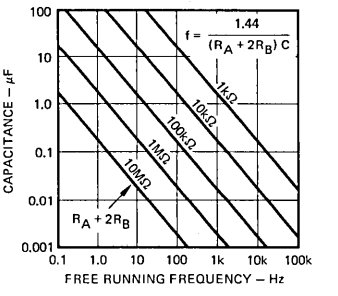
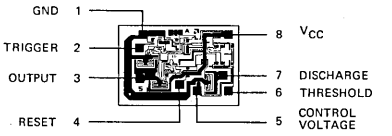


Fig. 4. Astable Free Running Frequency.

Metallization and Pad Layout



DIE SIZE: 0.040" X 0.060"

Am556

Dual Precision Timer

Distinctive Characteristics

- Timing from microseconds through hours
- 200mA output sink current
- Variable duty cycle
- TTL output compatibility
- Temperature stability of 0.005%/°C
- Replaces two Am555's
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

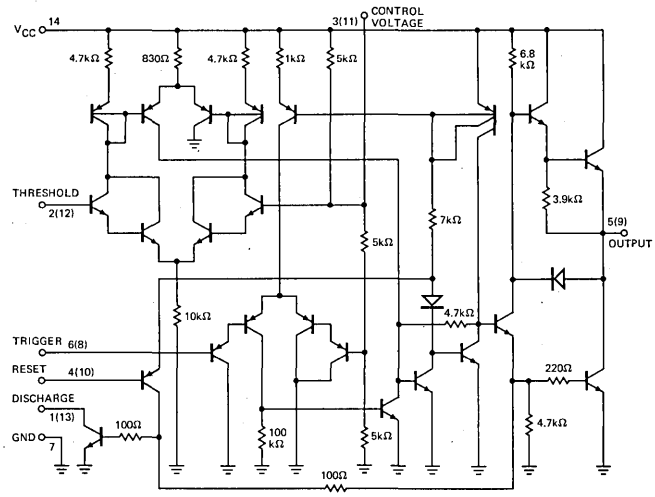
The Am556 is a dual highly stable timing device used to provide accurate time delays or to build precision oscillators. The Am556 is a dual Am555, where the two timers operate independently of each other sharing only V_{CC} and GND. When either timer is used as a monostable, the time is precisely controlled using one external resistor and one external capacitor. When the timer is used as a precision oscillator, the frequency and duty cycle are controlled by two external resistors and one external capacitor.

For monostable operation, a HIGH-to-LOW transition is applied to the trigger input. The device is triggered when the input trigger voltage reaches 1/3 V_{CC}. Once the circuit is triggered, it will remain in the triggered state until the set time has elapsed, even if it is triggered again. The output pulse width is equal to 1.1 $R_A C$.

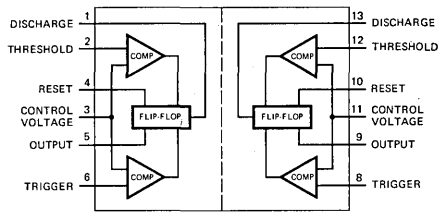
For continuous oscillation, two external resistors are used such that the external capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time is given by $t_{charge} = 0.693\ (R_A + R_B)C$ while the discharge time is $t_{discharge} = 0.693\ R_B C$. (See Fig. 3)

Each timer also features a direct reset that overrides all other inputs. When the reset is LOW the output is LOW regardless of the other inputs.

SCHEMATIC DIAGRAM
(One Timer Shown)



LOGIC SYMBOL

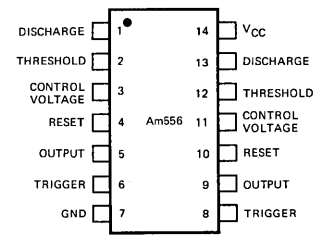


V_{CC} = Pin 14
GND = Pin 7

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	NE556A
Hermetic DIP	0°C to +70°C	NE556F
Dice	0°C to +70°C	AM556XC
Hermetic DIP	−55°C to +125°C	SE556F
Dice	−55°C to +125°C	AM556XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	
Military Grade	−55°C to +125°C
Commercial Grade	0°C to +70°C
Supply Voltage to Ground Potential	+18V
Power Dissipation	600mW
Lead Temperature (Soldering, 60 Seconds)	+300°C

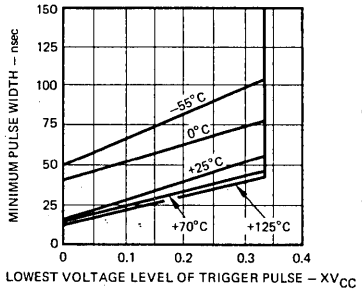
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5V to 15V Unless Otherwise Specified)

Parameter	Test Conditions		Military Min.	Military Typ.	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
Supply Voltage			4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞			3	5		3	6	mA
LOW State (Per Timer)	V_{CC} = 15V, R_L = ∞			10	11		10	14	mA
Threshold Voltage				2/3			2/3		XV_{CC}
Threshold Current	Note 3			30	100		30	100	nA
Trigger Voltage	V_{CC} = 15V		4.8	5	5.2		5		V
	V_{CC} = 5V		1.45	1.67	1.9		1.67		V
Trigger Current				0.5			0.5		μA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current				0.1			0.1		mA
Control Voltage Level	V_{CC} = 15V		9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V		2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage (LOW)	V_{CC} = 15V	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
		I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
		I_{SINK} = 100mA		2.0	2.25		2.0	2.75	V
		I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V	I_{SINK} = 8mA		0.1	0.25				V
		I_{SINK} = 5mA					0.25	0.35	V
Output Voltage (HIGH)	V_{CC} = 15V	I_{SOURCE} = −200mA		12.5			12.5		V
	V_{CC} = 15V	I_{SOURCE} = −100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V		3.0	3.3		2.75	3.3		V
Rise Time of Output				100			100		ns
Fall Time of Output				100			100		ns
Timing Error (Monostable)									
Initial Accuracy	R_A = 2K to 100K			0.5	1.5		0.75		%
Drift with Temperature	C = 0.1μF (Note 2)			30	100		50		ppm/°C
Drift with Supply Voltage				0.05	0.2		0.1		%/Volt
Timing Error (Astable)									
Initial Accuracy	R_A, R_B = 2K to 100K			1.5			2.25		%
Drift with Temperature	C = 0.1μF (Note 2)			90			150		ppm/°C
Drift with Supply Voltage				0.15			0.3		%/Volt
Discharge Leakage Current				20	100		20	100	nA
Matching Characteristics (Note 4)									
Initial Timing Accuracy				0.05	0.1		0.1	0.2	%
Timing Drift with Temperature				+10			+10		ppm/°C
Drift with Supply Voltage				0.1	0.2		0.2	0.5	%/Volt

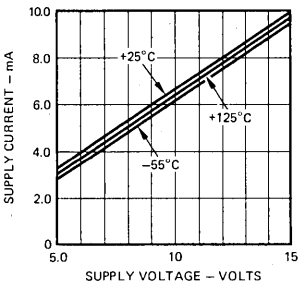
Notes: 1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine maximum value of $R_A + R_B$ for 15V operation. The max. total R = 20 Meg Ω.
4. Matching characteristics refer to the differences between performance characteristics of each timer section.

TYPICAL CHARACTERISTICS

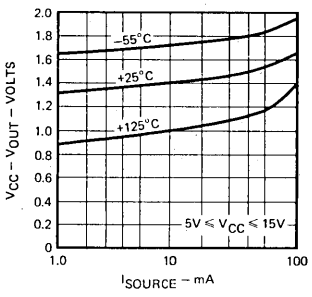
Minimum Pulse Width Required for Triggering



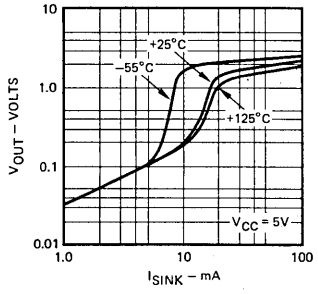
Supply Current Versus Supply Voltage



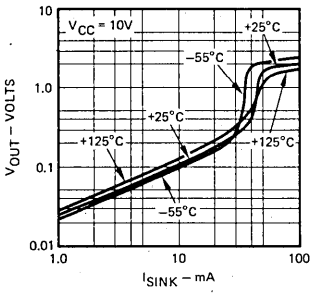
High Output Voltage Versus Output Source Current



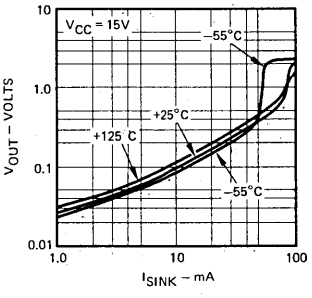
Low Output Voltage Versus Output Sink Current



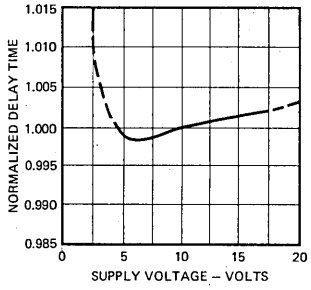
Low Output Voltage Versus Output Sink Current



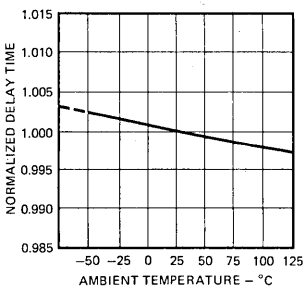
Low Output Voltage Versus Output Sink Current



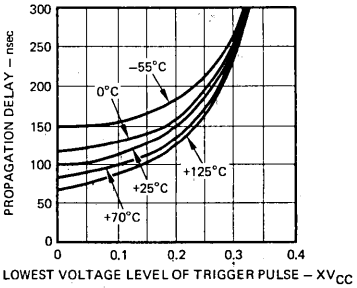
Delay Time Versus Supply Voltage



Delay Time Versus Temperature



Propagation Delay Versus Voltage Level of Trigger Pulse



8

APPLICATIONS

MONOSTABLE OPERATION

When the timer is operated as a monostable multivibrator, one external capacitor, C, and one external resistor, R_A, are used as shown in Figure 1. When the trigger input is reduced below 1/3 V_{CC}, the timer internal flip-flop is set. This releases the short circuit across the external capacitor as the Q output goes HIGH. The voltage across the capacitor begins to rise exponentially with the time constant R_AC. When the capacitor voltage reaches 2/3 V_{CC}, the internal comparator resets the internal flip-flop and discharges the external capacitor, C, very rapidly. The output is now in LOW state and a new timing state may be initiated. The time that the output is in the HIGH state is given by 1.1 R_AC or can be taken directly from Figure 2. Both the charge rate and internal threshold are directly proportional to the V_{CC} supply voltage. Thus, the timer output pulse width is independent of the power supply voltage. If a LOW is applied to the reset input, the output is forced LOW and the external capacitor discharged regardless of the other inputs.

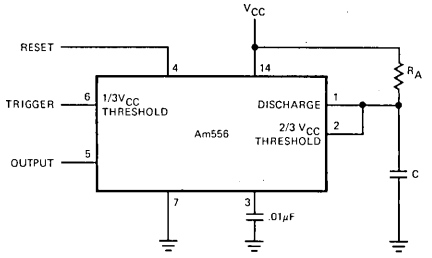


Fig. 1. Monostable Operation of the Am556.

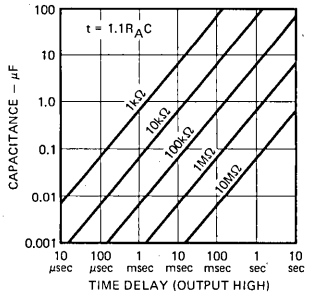


Fig. 2. Monostable Pulse Width Graph.

ASTABLE OPERATION

When the timer is operated in the astable mode, two external resistors, R_A and R_B, and one external capacitor, C, are used as shown in Figure 3. With this connection scheme, the external capacitor, C, charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time (output HIGH) is

$$t_{AB} = 0.693 (R_A + R_B) C$$

The discharge time (output LOW) is

$$t_B = 0.693 R_B C$$

The total period for one cycle of output HIGH and output LOW is

$$T = t_{AB} + t_B = 0.693 (R_A + 2R_B) C$$

The frequency for this period, T, is

$$f = \frac{1}{T} = \frac{1}{0.693 (R_A + 2R_B) C}$$

The astable free running frequency can also be found from the graph shown in Figure 4. The duty cycle, time the output is LOW divided by the period, is given by

$$D = \frac{t_B}{t_{AB} + t_B} = \frac{R_B}{R_A + 2R_B}$$

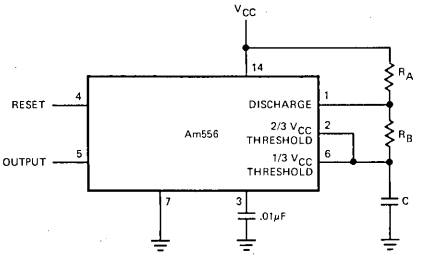


Fig. 3. Astable Operation of the Am556.

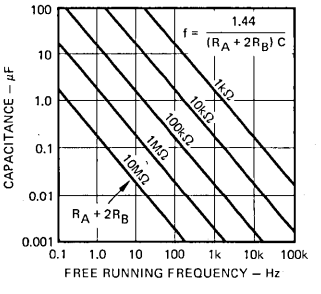
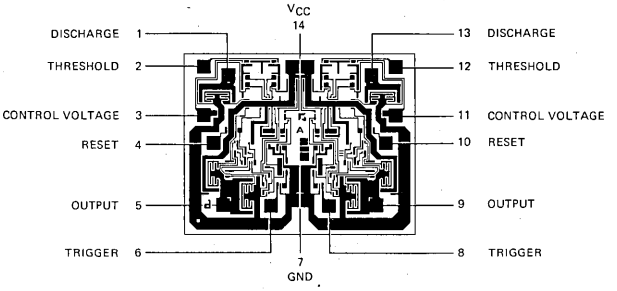


Fig. 4. Astable Free Running Frequency.

Metallization and Pad Layout



DIE SIZE 0.060" X 0.074"

Am592

Differential Video Amplifier

PRELIMINARY DATA

Distinctive Characteristics

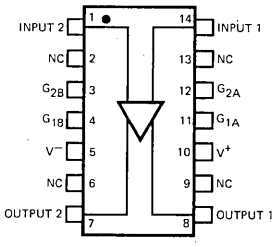
- The Am592 and Am592C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Signetics SE592 and NE592.
- Bandwidths: 40 to 120 MHz
- Rise times: 2.5 to 10 ns
- Propagation delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL-STD-883A
- Electrically tested and optically inspected dice for hybrid manufacturers
- 120 MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Available in metal can, hermetic dual-in-line or plastic dual-in-line packages

FUNCTIONAL DESCRIPTION

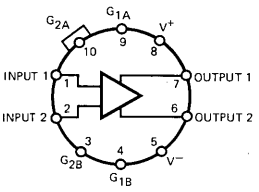
The Am592/Am592C is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

CONNECTION DIAGRAMS
Top Views

Dual-In-Line



Metal Can

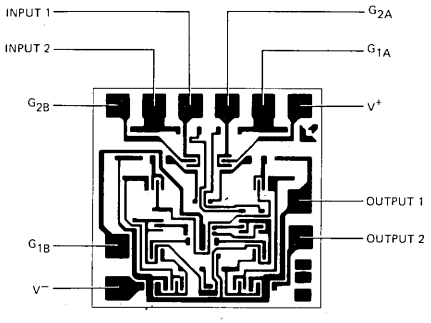


Note: On Metal Can, pin 5 is conneted to case.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am592C	TO-100	0°C to +70°C	AM592HC
	DIP	0°C to +70°C	AM592DC
	Molded DIP	0°C to +70°C	AM592PC
	Dice	0°C to +70°C	LD592C
Am592	TO-100	−55°C to +125°C	AM592HM
	DIP	−55°C to +125°C	AM592DM
	Dice	−55°C to +125°C	LD592

Metallization and Pad Layout



DIE SIZE 41 X 41 mils

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range	
Am592	−55°C to +125°C
Am592C	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS Standard Conditions (T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified)

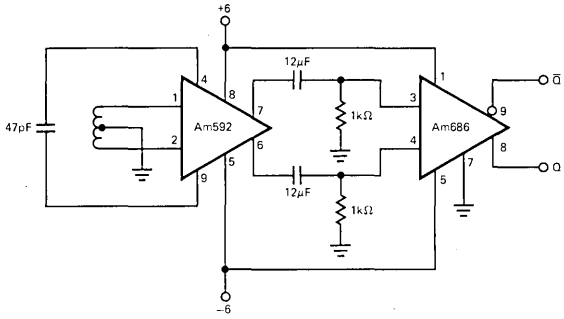
Parameter		Conditions		Am592C Min.	Am592C Typ.	Am592C Max.	Am592 Min.	Am592 Typ.	Am592 Max.	Units
Differential Voltage Gain	Gain 1	Note 1	R_L = 2kΩ, V_{OUT} = 3V p-p	250	400	600	300	400	500	
	Gain 2	Note 2		80	100	120	90	100	110	
Bandwidth	Gain 1	Note 1			40			40		MHz
	Gain 2	Note 2			90			90		
Rise Time	Gain 1	Note 1	V_{OUT} = 1V p-p		11			11		ns
	Gain 2	Note 2			6.0	12		6.0	10	
Propagation Delay	Gain 1	Note 1	V_{OUT} = 1V p-p		7.5			7.5		ns
	Gain 2	Note 2			6.0	10		6.0	10	
Input Resistance	Gain 1	Note 1			4.0			4.0		kΩ
	Gain 2	Note 2		10	30		20	30		
Input Capacitance	Gain 2	Note 2			2.0			2.0		pF
Input Offset Current					0.4	5.0		0.4	3.0	μA
Input Bias Current					9.0	30		9.0	20	μA
Input Noise Voltage		BW 1kHz to 10kHz			12			12		μV rms
Input Voltage Range						±1.0			±1.0	Volts
Common Mode Rejection Ratio	Gain 2	VCM ± 1V, F <100kHz		60	86		60	86		dB
	Gain 2	VCM ± 1V, F = 5MHz			60			60		
Supply Voltage Rejection Ratio	Gain 2	ΔVS = ±0.5V		50	80		50	80		dB
Output Offset Voltage	Gain 3	Note 3	R_L = ∞		0.2	0.75		0.2	0.75	Volts
Output Common Mode Voltage		R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	Volts
Output Voltage Swing		R_L = 2kΩ, Single Ended		3.0	3.9		3.0	3.9		Volts
Output Resistance					20			20		Ω
Power Supply Current		R_L = ∞			16	24		16	24	mA

Recommended Operating Supply Voltage (V_S = ±6.0V)

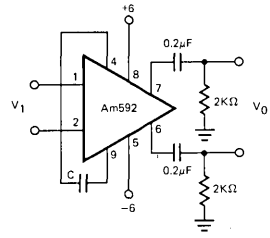
Notes: 1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL APPLICATIONS

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



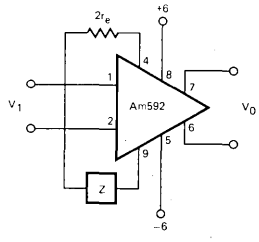
DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



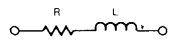
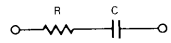
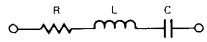
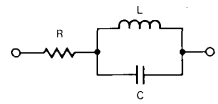
FOR FREQUENCY $F_1 \ll 1/2\,\pi\,(32)\,C$

$$v_0 \geq 1.4 \times 10^4 C \frac{dvi}{dT}$$

FILTER NETWORKS



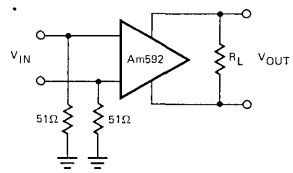
$$\frac{v_0(s)}{v_1(s)} \geq \frac{1.4 \times 10^4}{Z(s) + 2r_e} \geq \frac{1.4 \times 10^4}{Z(s) + 32}$$

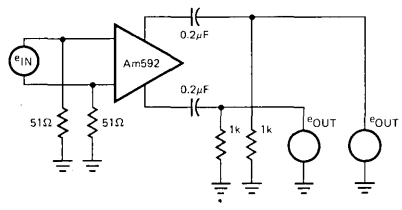
Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the value used is assumed to include $2r_e$, or approximately 32 ohms.

TEST CIRCUITS

($T_A = 25°C$ Unless Otherwise Noted)





Am733/733C

Differential Video Amplifier

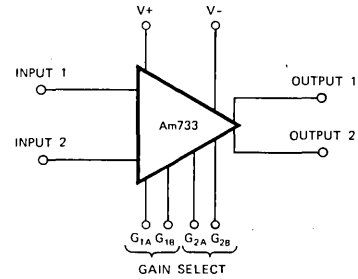
Distinctive Characteristics

- The Am733 and Am733C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild μA733 and 733C.
- Bandwidths: 40 to 120 MHz
- Rise Times: 2.5 to 10 ns
- Propagation Delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

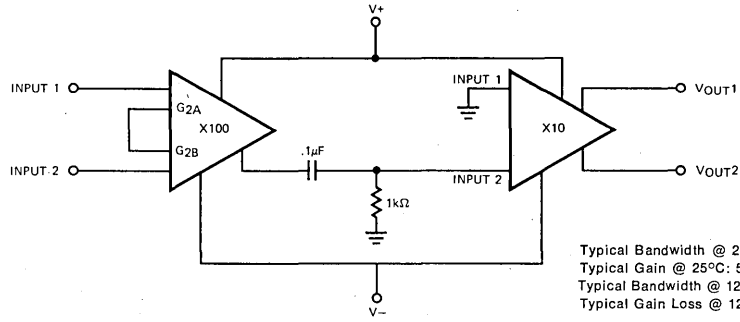
The Am733 is a monolithic two-stage differential input, emitter follower differential output video amplifier. Internal series-shunt feedback is used to obtain fixed gains of 10, 100 or 400, and adjustable gains from 10 to 400 by the use of an external resistor.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION

HIGH-GAIN WIDEBAND AMPLIFIER



Typical Bandwidth @ 25°C: 65 MHz
Typical Gain @ 25°C: 54 dB
Typical Bandwidth @ 125°C: 57 MHz
Typical Gain Loss @ 125°C: 1 dB

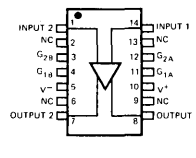
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am733C	TO-99	0°C to +70°C	733HC
	DIP	0°C to +70°C	733DC
	Dice	0°C to +70°C	733XC
Am733	TO-99	−55°C to +125°C	733HM
	DIP	−55°C to +125°C	733DM
	Flat Pak	−55°C to +125°C	733FM
	Dice	−55°C to +125°C	733XM

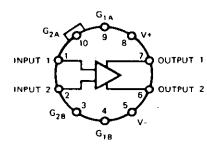
CONNECTION DIAGRAMS

Top Views

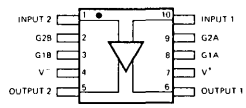
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 5 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Am733C	0°C to +70°C
Am733	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	300	400	500	
Gain 2 (Note 3)		80	100	120	90	100	110	
Gain 3 (Note 4)		8.0	10	12	9.0	10	11	
Bandwidth	$R_S = 50\,\Omega$							
Gain 1			40			40		MHz
Gain 2			90			90		MHz
Gain 3			120			120		MHz
Risetime	$R_S = 50\,\Omega$, $V_{out} = 1$ Vpp							
Gain 1			10.5			10.5		ns
Gain 2			4.5	12		4.5	10	ns
Gain 3			2.5			2.5		ns
Propagation Delay	$R_S = 50\,\Omega$, $V_{out} = 1$ Vpp							
Gain 1			7.5			7.5		ns
Gain 2			6.0	10		6.0	10	ns
Gain 3			3.6			3.6		ns
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		10	30		20	30		kΩ
Gain 3			250			250		kΩ
Input Capacitance	Gain 2		2.0			2.0		pF
Input Offset Current			0.4	5.0		0.4	3.0	μA
Input Bias Current			9.0	30		9.0	20	μA
Input Noise Voltage	$R_S = 50\,\Omega$, BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio								
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage								
Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5		0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	Single Ended	3.0	4.0		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		2.5	3.6		mA
Output Resistance			20			20		Ω
Power Supply Current			18	24		18	24	mA
The Following Specifications Apply Over The Operating Temperature Ranges								
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	200	400	600	
Gain 2 (Note 3)		80	100	120	80	100	120	
Gain 3 (Note 4)		8.0	10	12	8.0	10	12	
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		8.0	30		8.0	30		kΩ
Gain 3			250			250		kΩ
Input Offset Current			0.4	6.0		0.4	5.0	μA
Input Bias Current			9.0	40		9.0	40	μA
Input Voltage Range		±1.0			±1.0			V

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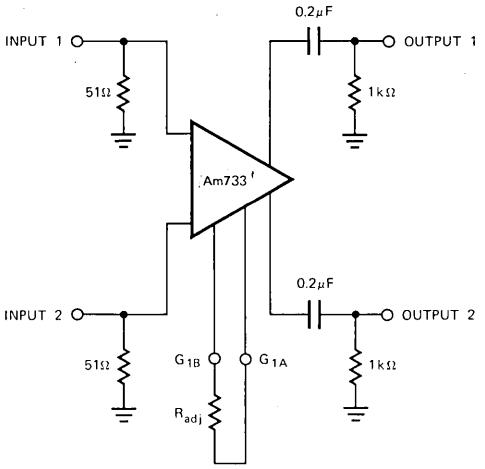
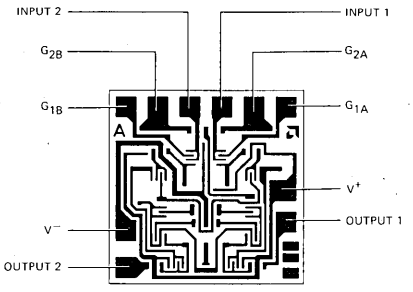
Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
The Following Specifications Apply Over The Operating Temperature Ranges								
Common Mode Rejection Ratio Gain 2	$V_{cm} = \pm 1$ V, f $\leq$ 100 kHz	50	86		50	86		dB
Supply Voltage Rejection Ratio Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5		0.35	1.2	V
Output Voltage Swing	Single Ended	2.8	4.0		2.5	4.0		Vpp
Output Sink Current		2.5	3.6		2.2	3.6		mA
Power Supply Current				27			27	mA

Notes:
1. Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 85°C and Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 100°C.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

VOLTAGE GAIN ADJUST CIRCUIT



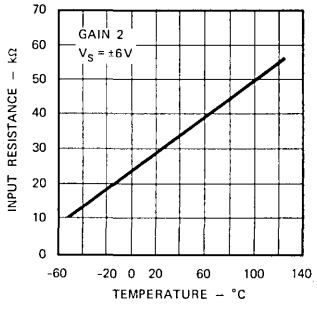
Metallization and Pad Layout



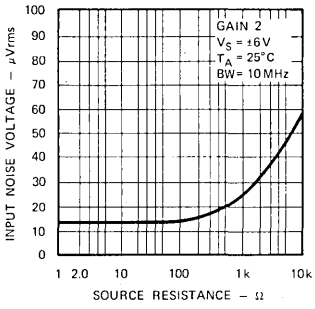
41 X 41 Mils

PERFORMANCE CURVES

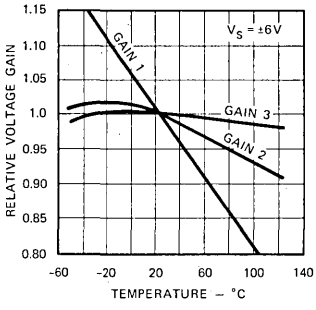
Input Resistance Vs. Temperature



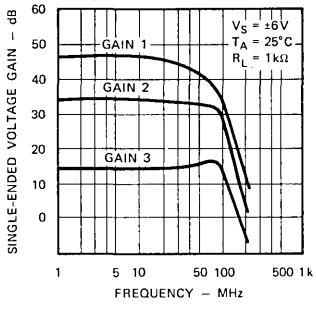
Input Noise Voltage



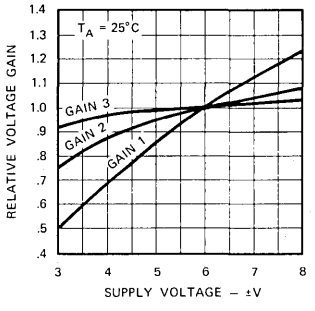
Gain Vs. Temperature



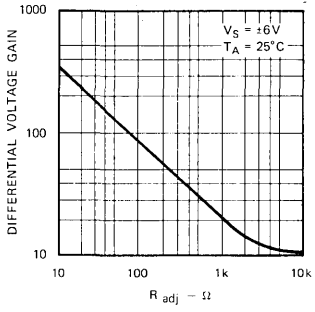
Gain Vs. Frequency



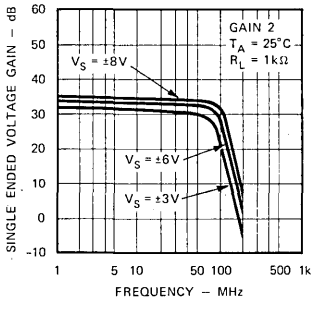
Gain Vs. Supply Voltage



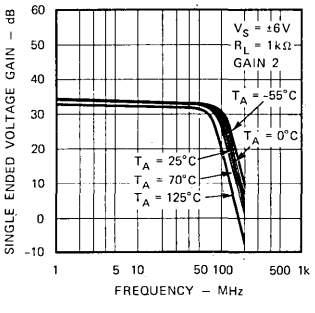
Gain Vs. R_{Adjust}



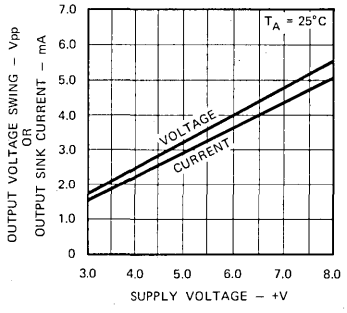
Gain Vs. Frequency and Supply Voltage



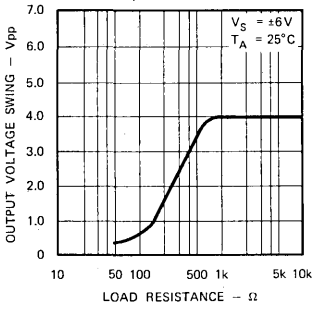
Gain Vs. Frequency and Temperature



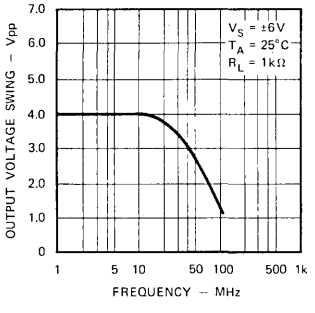
Output Voltage Swing And Sink Current Vs. Supply Voltage



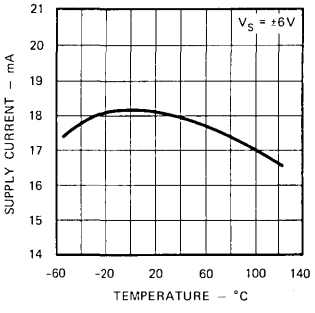
Output Voltage Swing Vs. Load Resistance



Output Voltage Swing Vs. Frequency



Supply Current Vs. Temperature



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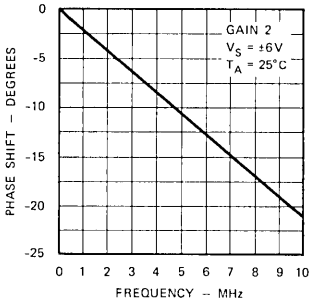
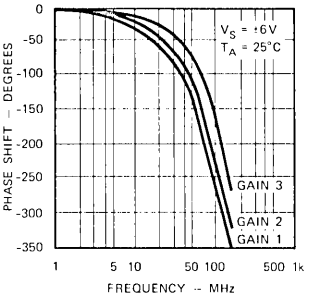
PERFORMANCE CURVES

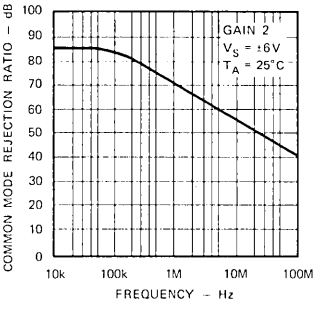
Phase Shift Vs. Frequency



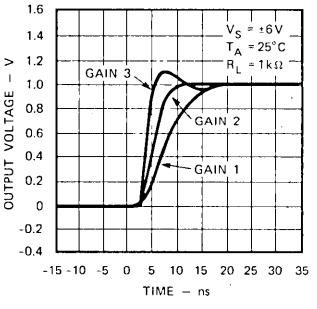
Phase Shift Vs. Frequency



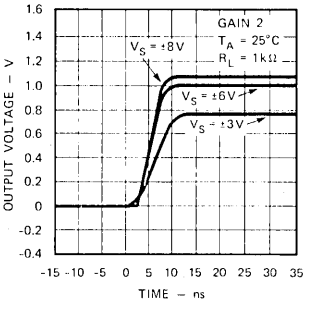
Common Mode Rejection Ratio



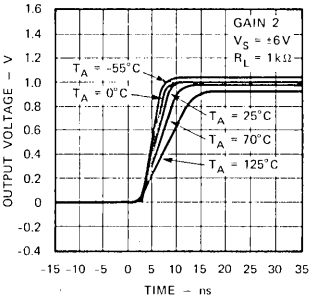
Pulse Response Vs. Gain



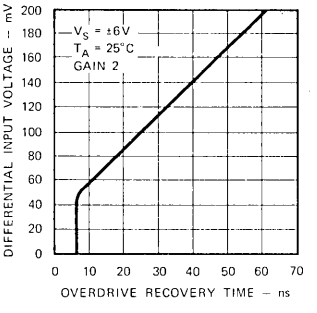
Pulse Response Vs. Supply Voltage



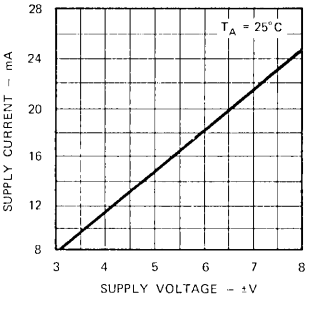
Pulse Response Vs. Temperature



Differential Overdrive Recovery Time



Supply Current Vs. Supply Voltage



Voltage Regulators – Section IX

Am105/205/305/305A

Voltage Regulator

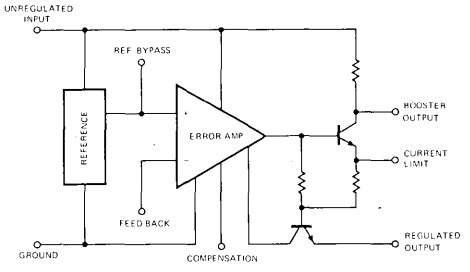
Distinctive Characteristics

- The Am105/205/305/305A are functionally, electrically, and pin-for-pin equivalent to the National LM 105/205/305/305A.
- Output voltage adjustable from 4.5V to 40V.
- Output currents in excess of 10A possible by adding external transistors.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

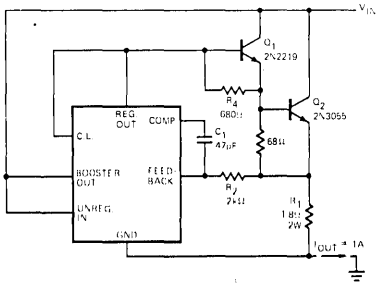
The Am105/205/305/305A is a positive voltage regulator which can be used in the series, shunt, linear or switching modes of operation. The circuits feature low stand-by current drain, operation under minimum load conditions and an output current capability of up to 20 mA.

FUNCTIONAL DIAGRAM

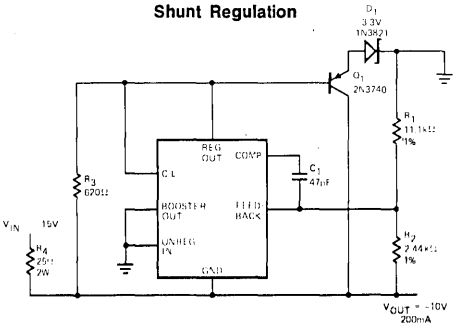


TYPICAL APPLICATIONS

Current Regulator



Shunt Regulation



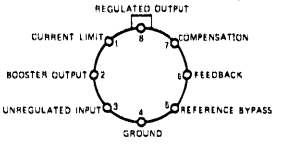
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am305A	TO-99	0°C to +70°C	LM305AH
Am305	TO-99	0°C to +70°C	LM305H
	Dice	0°C to +70°C	LD305
Am205	TO-99	–25°C to +85°C	LM205H
Am105	TO-99	–55°C to +125°C	LM105H
	Dice	–55°C to +125°C	LD105

CONNECTION DIAGRAM

Top View

Metal Can



NOTES: (1) On Metal Can, pin 4 is connected to case.

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MAXIMUM RATINGS

Input Voltage Range	Am105/205/305A	50 V
	Am305	40 V
Input-Output Voltage Differential		40 V
Internal Power Dissipation (Note 1)		
Metal Can (Similar to TO-99)		500 mW
		800 mW
Operating Temperature Range		
Am105		−55°C to +125°C
Am205		−25°C to +85°C
Am305/305A		0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

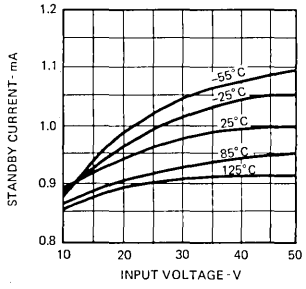
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am305 Min	Am305 Typ	Am305 Max	Am305A Min	Am305A Typ	Am305A Max	Am105 Am205 Min	Am105 Am205 Typ	Am105 Am205 Max	Units
Input Voltage Range		8.5		40	8.5		50	8.5		50	V
Output Voltage Range		4.5		30	4.5		40	4.5		40	V
Input-Output Voltage Differential		3.0		30	3.0		30	3.0		30	V
Line Regulation (Note 3)	$V_{in} - V_{out} \leq 5$ V		0.025	0.06		0.025	0.06		0.025	0.06	%/V
	$V_{in} - V_{out} \geq 5$ V		0.015	0.03		0.015	0.03		0.015	0.03	%/V
Load Regulation (Note 3)	$0 \leq I_O \leq 12$ mA										
	$R_{SC} = 18\ \Omega$, $T_A = 25°C$		0.02	0.05					0.02	0.05	%
	$R_{SC} = 15\ \Omega$, $T_A = T_A$(max)		0.03	0.1							%
	$R_{SC} = 10\ \Omega$, $T_A = T_A$(max)								0.03	0.01	%
	$R_{SC} = 18\ \Omega$, $T_A = T_A$(min)		0.03	0.1					0.03	0.1	%
	$0 \leq I_O \leq 45$ mA										
	$R_{SC} = 0\ \Omega$, $T_A = 25°C$					0.02	0.2				%
	$R_{SC} = 0\ \Omega$, $T_A = T_A$ (max)					0.03	0.4				%
	$R_{SC} = 0\ \Omega$, $T_A = T_A$ (min)					0.03	0.4				%
Feedback Sense Voltage		1.63	1.70	1.81	1.55	1.70	1.85	1.63	1.70	1.81	V
Ripple Rejection	$C_{REF} = 10\ \mu$f, f = 120 Hz		0.003	0.01		0.003			0.003	0.01	%/V
Output Noise Voltage	10 Hz $\leq$ f $\leq$ 10 kHz										
	$C_{REF} = 0$		0.005			0.005			0.005		%
	$C_{REF} > 0.1\ \mu$f		0.002			0.002			0.002		%
Standby Current Drain	$V_{in} = 40$ V		0.8	2.0							
	$V_{in} = 50$ V					0.8	2.0		0.8	2.0	mA
Long Term Stability			0.1	1.0		0.1	1.0		0.1	1.0	%
Temperature Stability			0.3	1.0		0.3	1.0		0.3	1.0	%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\ \Omega$, $T_A = 25°C$ $V_{out} = 0$ V	225	300	375	225	300	375	225	300	375	mV

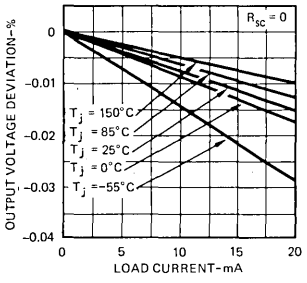
Notes:
1. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 25°C.
2. These specifications apply over the operating temperature range, for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.
5. Connect booster output to unregulated input when no external pass transistor is used.

PERFORMANCE CURVES

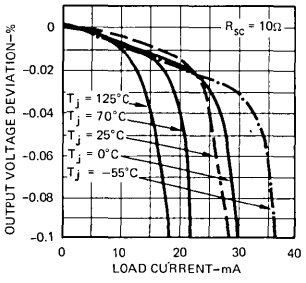
Standby Current Drain As A Function Of Input Voltage



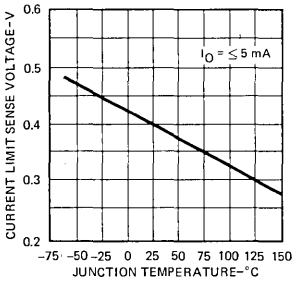
Load Regulation



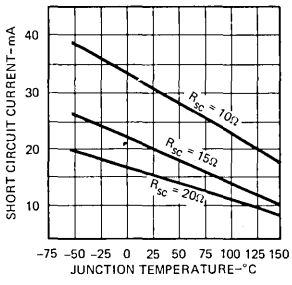
Load Regulation Characteristics With Current Limiting



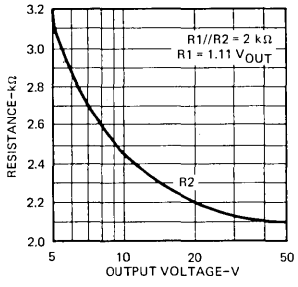
Current Limiting Sense Voltage As A Function of Junction Temperature



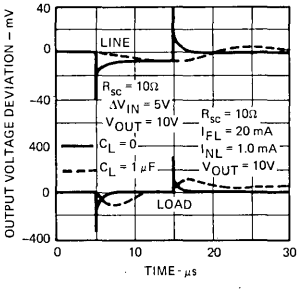
Short Circuit Current



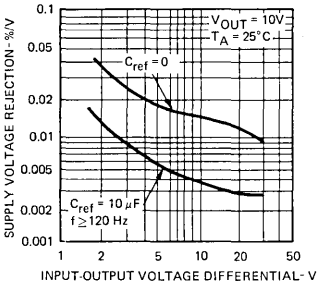
Optimum Divider Resistance Values



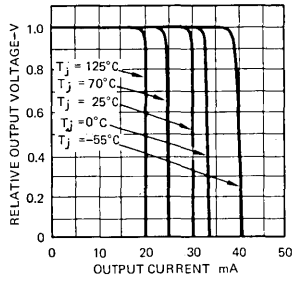
Transient Response



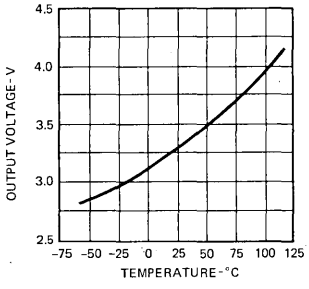
Supply Voltage Rejection



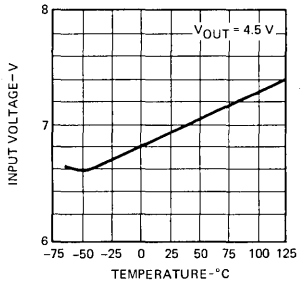
Current Limiting Characteristics



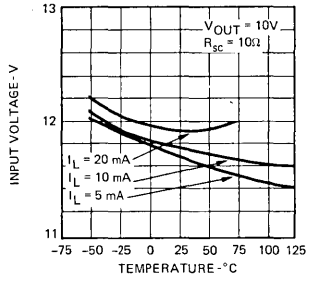
Minimum Output Voltage



Minimum Input Voltage



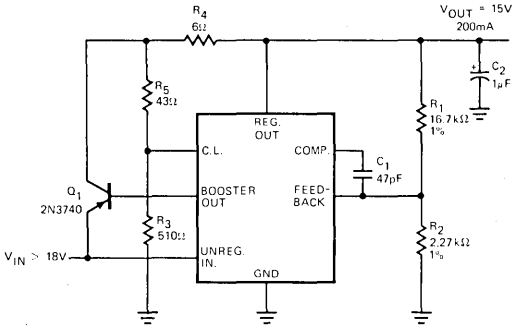
Regulator Dropout Voltage



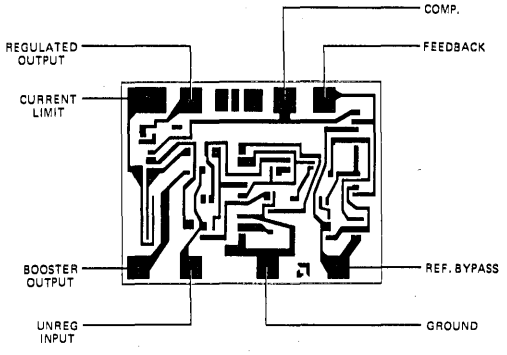
9

ADDITIONAL APPLICATIONS

Linear Regulator with Foldback Current Limiting



Metallization and Pad Layout



38 x 48 Mils

Am723/723C

Voltage Regulator

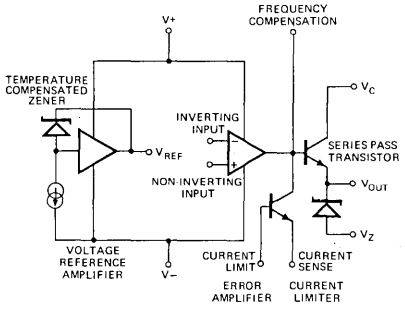
Description: The Am723 and Am723C monolithic voltage regulators are functionally and electrically equivalent to the Fairchild μA723 and μA723C. Both are available in the hermetic dual-in-line and metal can packages and are pin for pin replacements for the Fairchild μA723 and μA723C.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

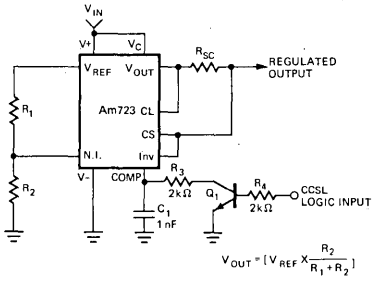
The Am723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. It is applicable to remote shutdown and current limiting operations and will accept either PNP or NPN external pass elements to increase output current capability.

FUNCTIONAL DIAGRAM



APPLICATIONS

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)

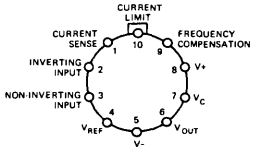


ORDERING INFORMATION

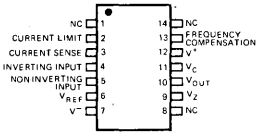
Part Number	Package Type	Temperature Range	Order Number
Am723C	DIP	0°C to +70°C	723DC
	Metal Can	0°C to +70°C	723HC
	Molded DIP	0°C to +70°C	723PC
	Dice	0°C to +70°C	723XC
Am723	DIP	–55°C to +125°C	723DM
	Metal Can	–55°C to +125°C	723HM
	Dice	–55°C to +125°C	723XM

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



NOTES: (1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 7 is connected to case.

9

MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 msec)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	850 mW
DIP	900 mW
Operating Temperature Range	
Am723C	0°C to +70°C
Am723	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

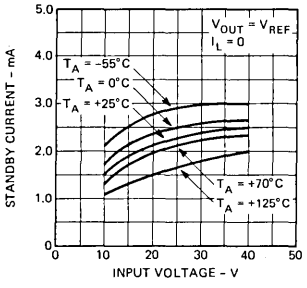
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am723C Min	Am723C Typ	Am723C Max	Am723 Min	Am723 Typ	Am723 Max	Units
Line Regulation (Note 3)	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1		0.01	0.1	% V_{OUT}
	V_{IN} = 12 V to V_{IN} = 40 V		0.1	0.5		0.02	0.2	% V_{OUT}
Load Regulation (Note 3)	I_L = 1 mA to I_L = 50 mA		0.03	0.2		0.03	0.15	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.80	7.15	7.50	6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30 V		2.3	4.0		2.3	3.5	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V
The Following Specifications Apply Over The Operating Temperature Ranges								
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V			0.3			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA			0.6			0.6	% V_{OUT}
Average Temperature Coefficient of Output Voltage			0.003	0.015		0.002	0.015	%/°C

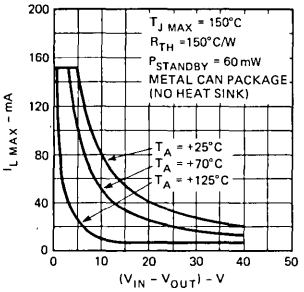
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 25°C and Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 50°C.
2. Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12 V, V− = 0 V, V_{out} = 5 V, I_L = 1 mA, R_{SC} = 0, C_I = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤10 kΩ when connected as shown in Fig. 3.
3. The load & line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

PERFORMANCE CURVES

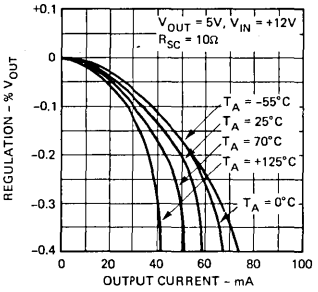
Standby Current Drain As A Function Of Input Voltage



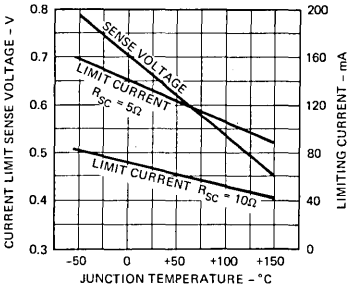
Maximum Load Current As A Function Of Input-Output Voltage Differential



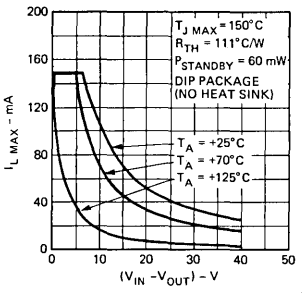
Load Regulation Characteristics With Current Limiting



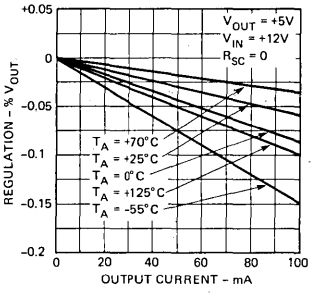
Current Limiting Characteristics As A Function of Junction Temperature



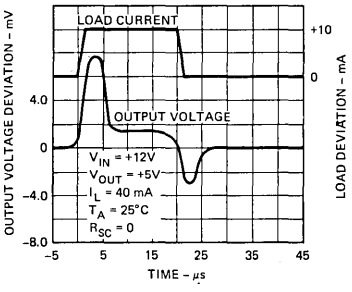
Maximum Load Current As A Function Of Input-Output Voltage Differential



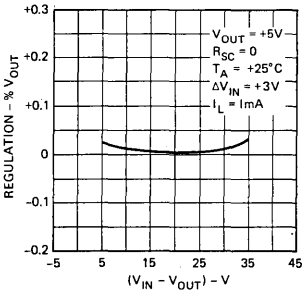
Load Regulation Characteristics Without Current Limiting



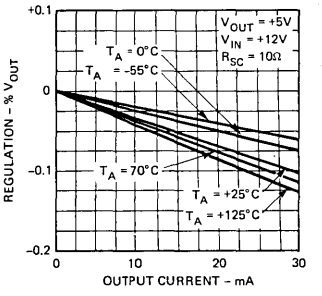
Load Transient Response



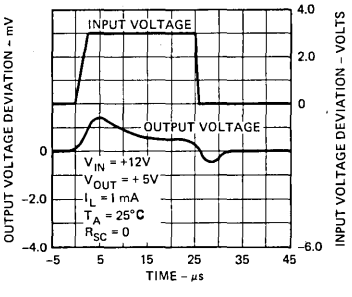
Line Regulation As A Function Of Input-Output Voltage Differential



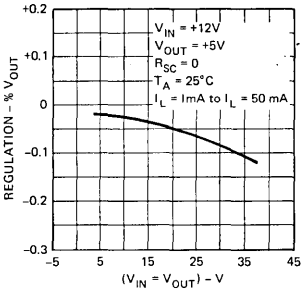
Load Regulation Characteristics With Current Limiting



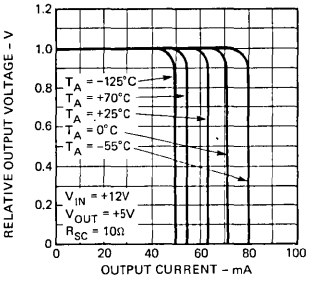
Line Transient Response



Load Regulation As A Function Of Input-Output Voltage Differential



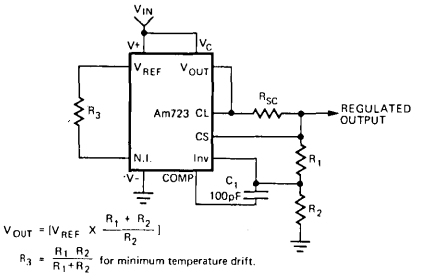
Current Limiting Characteristics



9

APPLICATIONS

HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



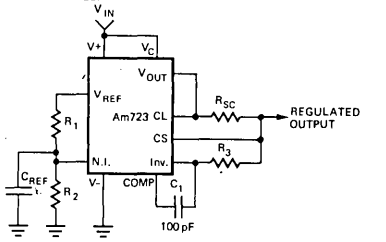
$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 1

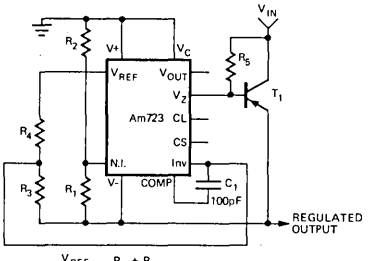
LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$; $R_3 = \frac{R_1 R_2}{R_2 + R_2}$ for minimum temperature drift.

Figure 3

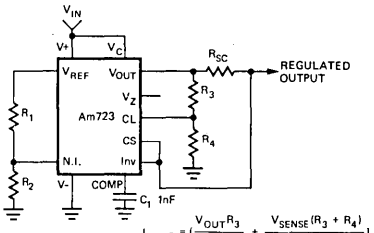
NEGATIVE VOLTAGE REGULATOR



$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$

Figure 2

FOLDBACK CURRENT LIMITING REGULATOR

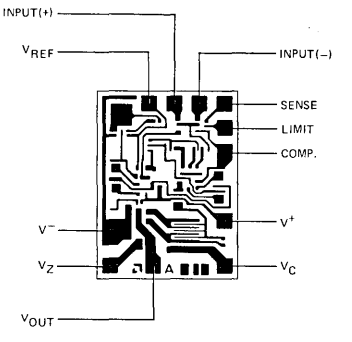


$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{SC} R_4}]$

$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$; $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$

Figure 4

Metallization and Pad Layout

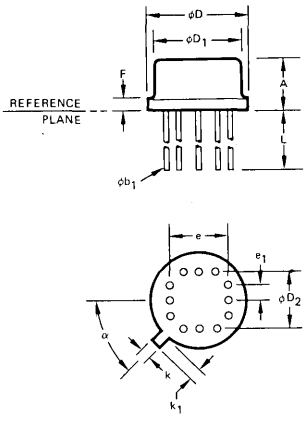


51 x 39 Mils

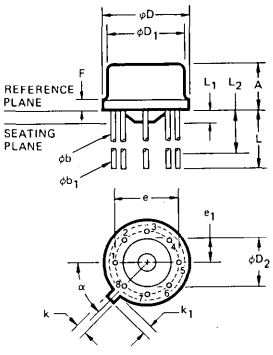
Section X

PACKAGE OUTLINES

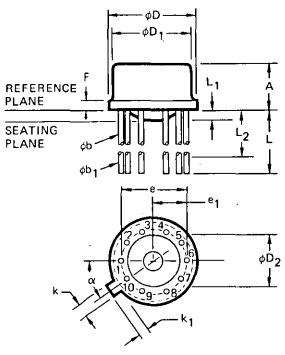
G-12-1
12-LEAD METAL CAN
(TO-8)



H-8-1
8-LEAD METAL CAN
(TO-99)



H-10-1
10-LEAD METAL CAN
(TO-100)

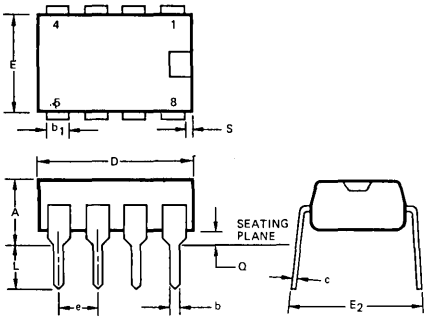


DIMENSIONS (inches)

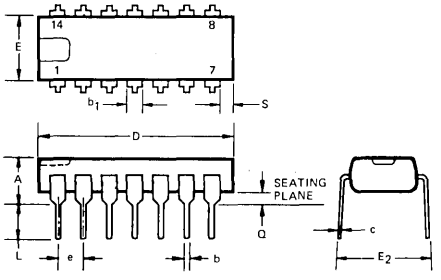
Parameters	G-12-1		H-10-1		H-8-1	
	Min.	Max.	Min.	Max.	Min.	Max.
A	.155	.180	.165	.185	.165	.185
e	.390	.410	.215	.245	.185	.215
e_1	.090	.110	.105	.125	.090	.110
F	.020	.030	.013	.033	.013	.033
k	.024	.034	.027	.034	.027	.034
k_1	.024	.038	.027	.045	.027	.045
L	.500	.600	.500	.610	.500	.570
L_1				.050		.050
L_2			.250		.250	
α	45°		36° BSC		45° BSC	
ϕb			.016	.019	.016	.019
ϕb_1	.016	.021	.016	.021	.016	.021
ϕD	.590	.610	.350	.370	.350	.370
ϕD_1	.540	.560	.305	.335	.305	.335
ϕD_2	.390	.410	.120	.160	.120	.160

PACKAGE OUTLINES (Cont.)

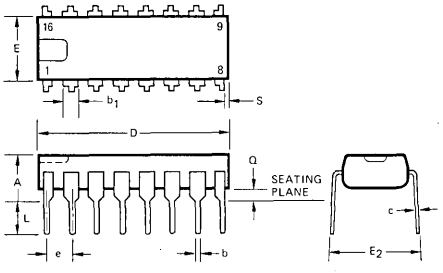
P-8-1
8-LEAD MOLDED DUAL-IN-LINE



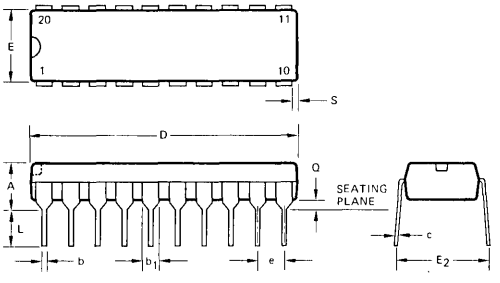
P-14-1
14-LEAD MOLDED DUAL-IN-LINE
(TO-116)



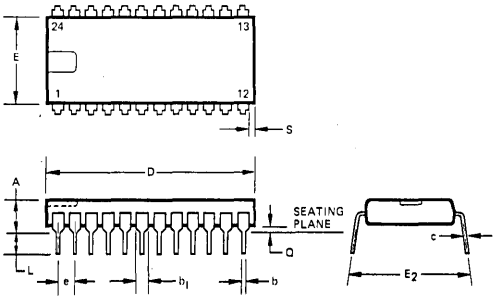
P-16-1
16-LEAD MOLDED DUAL-IN-LINE



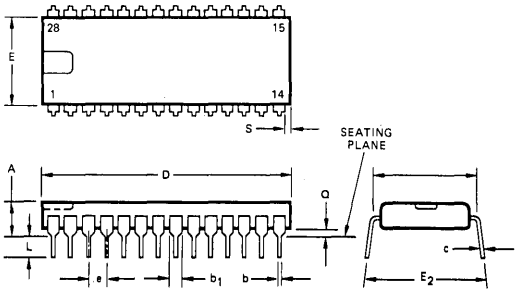
P-20-1
20-LEAD MOLDED DUAL-IN-LINE



P-24-1
24-LEAD MOLDED DUAL-IN-LINE



P-28-1
28-LEAD MOLDED DUAL-IN-LINE

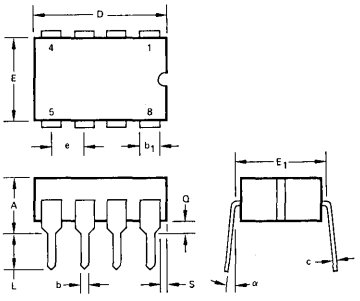


DIMENSIONS (inches)

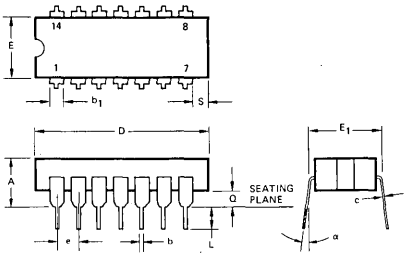
Parameters	P-8-1		P-14-1		P-16-1		P-20-1		P-24-1		P-28-1	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200
b	.015	.022	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.370	.390	.735	.765	.735	.765	1.000	1.040	1.235	1.265	1.440	1.460
E	.240	.260	.240	.260	.240	.260	.250	.290	.515	.540	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.310	.385	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S	.010	.020	.035	.055	.010	.020	.025	.035	.035	.055	.035	.055

PACKAGE OUTLINES (Cont.)

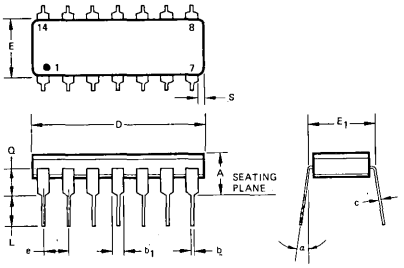
D-8-1
8-LEAD HERMETIC DUAL-IN-LINE



D-14-1
14-LEAD HERMETIC DUAL-IN-LINE

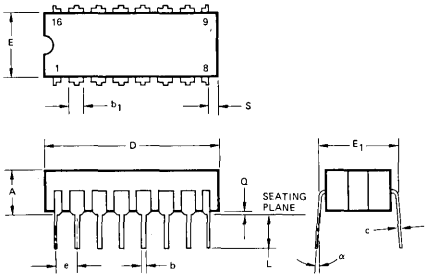


†D-14-3
14-LEAD METAL HERMETIC
DUAL-IN-LINE

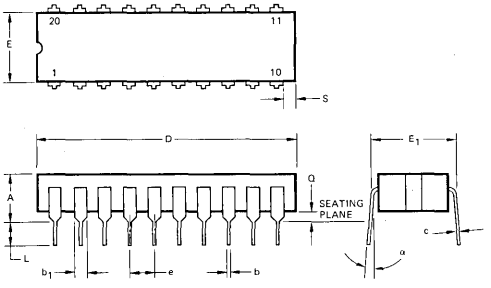


†This package is used only for LM108/LM108A series of product.

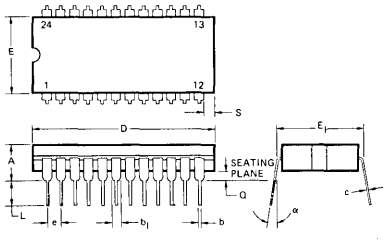
D-16-1
16-LEAD HERMETIC DUAL-IN-LINE



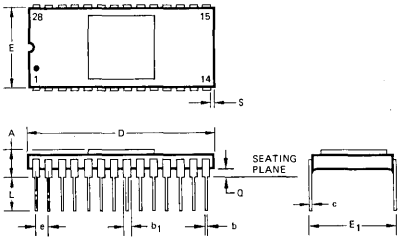
D-20-1
20-LEAD HERMETIC DUAL-IN-LINE



D-24-1
24-LEAD HERMETIC DUAL-IN-LINE



D-28-2
28-LEAD HERMETIC DUAL-IN-LINE



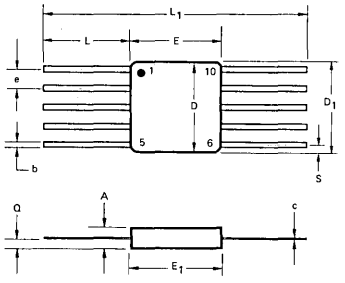
DIMENSIONS (inches)

Parameters	D-8-1		D-14-1		D-14-3		D-16-1		D-20-1		D-24-1		D-28-2	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.130	.200	.100	.200	.130	.200	.140	.220	.150	.225	.100	.200
b	.016	.020	.016	.020	.015	.023	.016	.020	.016	.020	.016	.020	.015	.022
b_1	.050	.070	.050	.070	.030	.070	.050	.070	.050	.070	.045	.065	.030	.060
c	.009	.011	.009	.011	.008	.011	.009	.011	.009	.011	.009	.011	.008	.012
D	.370	.400	.745	.785	.660	.785	.745	.785	.935	.970	1.230	1.285	1.380	1.420
E	.240	.285	.245	.285	.230	.265	.245	.285	.245	.285	.510	.545	.560	.600
E_1	.300	.320	.290	.320	.290	.310	.290	.320	.290	.320	.600	.620	.590	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.100	.150	.125	.150	.125	.150	.120	.150	.120	.150
Q	.015	.045	.015	.045	.020	.080	.015	.045	.015	.045	.015	.045	.020	.060
S*	.004		.020				.005		.005		.010		.005	
α	3°	13°	3°	13°			3°	13°	3°	13°	3°	13°	0	

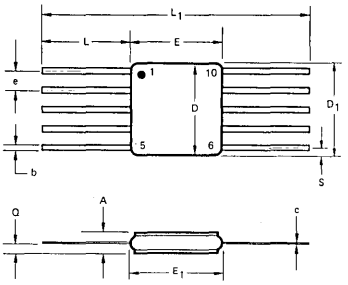
*From edge of end lead.

PACKAGE OUTLINES (Cont.)

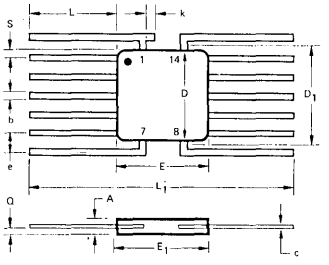
F-10-1
10-LEAD CERPAK



†F-10-2
10-LEAD FLAT PACKAGE

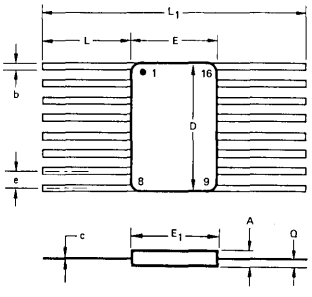


F-14-1
14-LEAD CERPAK

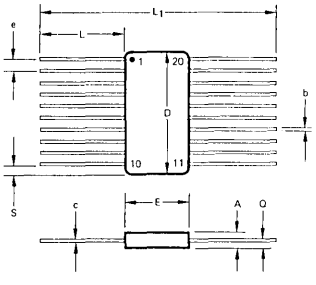


†This package is used only for LM108/LM108A series of product.

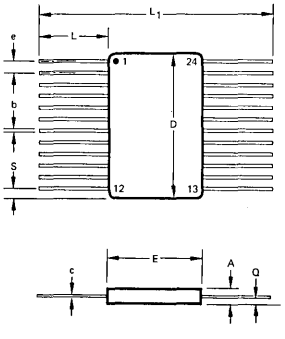
F-16-1
16-LEAD CERPAK



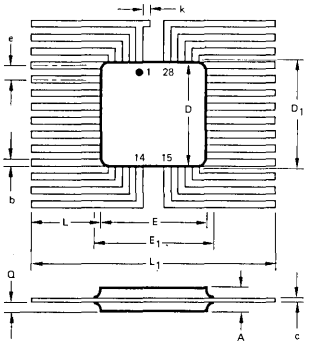
F-20-1
20-LEAD CERPAK



F-24-1
24-LEAD CERPAK



F-28-2
28-LEAD FLAT PACKAGE



DIMENSIONS (inches)

Parameters	F-10-1		F-10-2		F-14-1		F-16-1		F-20-1		F-24-1		F-28-1	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.080	.045	.080	.045	.085	.045	.085	.050	.090	.045	.080
b	.015	.019	.012	.019	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
c	.004	.006	.003	.006	.004	.006	.004	.006	.004	.006	.004	.006	.003	.006
D	.230	.255	.235	.275	.230	.255	.370	.425	.490	.520	.580	.620	.360	.410
D_1				.275										.410
E	.240	.260	.240	.260	.240	.260	.245	.285	.245	.285	.360	.385	.360	.410
E_1		.275		.280		.275		.290		.290		.410		.410
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.335	.370	.335	.370	.335	.370	.335	.370	.335	.370	.270	.320	.270	.320
L_1	.920	.995	.920	.980	.920	.995	.925	.995	.925	.995	.955	1.000	.955	1.000
Q	.010	.040	.010	.040	.010	.040	.020	.040	.020	.040	.020	.040	.010	.040
S*	.005		.005		.005		.005		.005		.005		.005	

*From edge of end lead.

GLOSSARY

$\Delta I_{OS}/\Delta T_A$	**Average Temperature Coefficient of Input Offset Current** – The ratio of the change in input offset current, over the operating temperature range, to the operating temperature range. (pA/°C)
$\Delta V_{OS}/\Delta T_A$	**Average Temperature Coefficient of Input Offset Voltage** – The ratio of the change in input offset voltage, over the operating temperature range, to the operating temperature range. (μV/°C)
BW	**Bandwidth** – The frequency at which the gain of the device is 3 dB below its low frequency value.
CS	**Channel Separation** – The log of the ratio of the input of an undriven amplifier to the output of an adjacent driven amplifier. (dB)
V_{OHC}	**Clamped Output High Voltage** – The voltage potential necessary to turn on (forward bias) the clamping diode on the output pin. (V)
V_{OLC}	**Clamped Output Low Voltage** – The voltage potential necessary to turn off (reverse bias) the clamping diode on the output pin. (V)
f_{clock}	**Clock Frequency** – The reciprocal of the clock period; the clock repetition rate.
	Clock Input, Amplitude – The peak amplitude of the clock signal.
t_{PW}	**Clock Input, Width** – The time duration of the clock pulse.
	Common Mode Gain – The ratio of the output voltage change to the input common mode voltage producing that change.
	Common Mode Input Overload Recovery Time – The time delay between removal of an input common mode voltage outside the input common mode range, and resumption of normal device operation. (ns)
	Common Mode Input Resistance – The value of resistance with respect to a common mode signal, seen when looking into both inputs. (Ω)
	Common Mode Input Voltage Swing – The peak value of the common mode input voltage at which the device will operate in a linear fashion. (V)
	Common Mode Output Voltage – The output voltage resulting from the application of a voltage common to both inputs and the average of the two output voltages of a differential output amplifier. (V)
CMRR	**Common Mode Rejection Ratio** – The ratio of the change in input offset voltage to the total change in common mode voltage producing it. (dB)
V_{CM}	**Common Mode Voltage** – The arithmetic mean of the voltage present at the differential inputs with respect to the device ground reference. (V)
t_d	**Delay Time** – See Propagation Delay. (ns)
	Differential Input Bias Current – The current required in the differential input stage to bias the stage into operation.
	Differential Input Capacitance – The effective capacitance between the two inputs, operating open loop.
	Differential Input Impedance – The impedance seen looking between the input terminals.
	Differential Input Offset Current – The difference in currents required by the transistors in the input stage to bias the input stage to its quiescent operation point.
	Differential Input Overload Recovery Time – The time delay between removal of a differential input voltage that exceeds the differential input voltage operating range, and resumption of normal device operation.
	Differential Input Resistance – The effective resistance between the two inputs, operating open loop.
	Differential Input Threshold Voltage – The voltage difference between the + and – inputs required to guarantee the output logic state.
	Differential Input Voltage Range – The range of voltage applied between the input terminals for which operation remains within specifications.
	Differential Load Rejection – The ratio of the change in input offset voltage to the change in differential load current.
	Differential Output Resistance – The resistance measured between the two output terminals.
	Differential Output Voltage Swing – The peak differential output voltage that can be obtained without clipping the output voltage waveform.
	Differential Voltage Gain – The ratio of the change in differential output voltage to the change in differential input voltage.
V_{DO}	**Dropout Voltage** – The input-output voltage differential that causes the output voltage to decrease by 5% of its initial value. (V)

GLOSSARY (Cont.)

t_{ZH}	**Enable HIGH** – The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.
t_{ZL}	**Enable LOW** – The delay time from a control input change to the three-state output high-impedance to LOW-level transition.
i_n	**Equivalent Input Noise Current** – The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance. (pA/$\sqrt{Hz}$)
e_n	**Equivalent Input Noise Voltage** – The input noise voltage that would reproduce the noise seen at the output if all amplifier noise sources and the source resistances were set to zero. (nV/$\sqrt{Hz}$)
t_f	**Fall Time** – The time required for the signal to fall from 90% to 10% of its output value into a specified load network. (ns)
	Feedback Capacitance – The effective value of the capacitive coupling from output to input.
V_{sense}	**Feedback Sense Voltage** – The voltage measured on the feedback terminal of the regulator, with respect to ground, when the device is operating in regulation. (V)
	Frequency Response – The frequency at which the output drops to 0.707 of its low frequency value.
f_t	**Gain Bandwidth Product** – The frequency at which the small signal ac gain of the device reduces to unity. (MHz)
H	**HIGH** – Applying to a HIGH voltage level.
h_{fe}	**High Frequency Current Gain** – The small signal ac current gain at a specified frequency.
t_{HZ}	**HIGH to Disable** – The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).
t_h	**Hold Time** – The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.
ΔV_{TH}	**Hysteresis** – The voltage difference between the switching points of the device. See Lower Input Threshold Voltage and Upper Input Threshold Voltage.
I	**Input.**
I_{BIAS}	**Input Bias Current** – The average of the two input currents with no signal applied. (nA or pA) **Input Bias Current Drift** – The change in input bias current with temperature supply voltage, or time. ($\Delta I_{BIAS}/\Delta T, \Delta V_S, \Delta t$)
C_{IN}	**Input Capacitance** – The equivalent capacitance of either input with the other input grounded. (pF)
V_{IH}	**Input HIGH Voltage** – The range of input voltages that represents a logic HIGH in the system.
V_C	**Input Clamp Diode Voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.
CMVR	**Input Common Mode Voltage Range** – The range of common mode input voltage over which the device will operate within specifications. (V)
I_{IN}	**Input Current** – The current flowing into the input with a specified voltage applied to the input.
	Input Current at Maximum Input Voltage – The current into a TTL or DTL input with the absolute maximum allowed input voltage applied to the input.
I_F	**Input Forward Current** – See Input LOW Current.
I_{IH}	**Input HIGH Current** – The current flowing out of an input when a specified LOW voltage is applied.
V_{IH}	**Input HIGH Voltage** – The range of input voltages that represents a logic HIGH in the system.
	Input Latch Voltage – See Input Clamp Diode Voltage.
I_{IL}	**Input LOW Current** – The current flowing out of an input when a specified LOW voltage is applied.
V_{IL}	**Input LOW Voltage** – The range of input voltages that represents a logic LOW in the system.
	Input Noise Voltage – The rms noise voltage present at the amplifier output divided by the gain of the amplifier, measured with the inputs connected to ground through a low resistance.(e_n)
I_{OS}	**Input Offset Current** – The difference in current into the two input terminals with the output voltage at zero. In a comparator, it is the difference between the two input currents with the output at the logic threshold voltage. Also, it is defined as the difference in input currents required to give equal output currents from a matched pair of devices. (nA or pA)
$\Delta I_{OS}/\Delta T$ $\Delta V, \Delta t$	**Input Offset Current Drift** – The change in input offset current produced with time, voltage or temperature. $\Delta V, \Delta t$ (pA/°C, V, s)
V_{OS}	**Input Offset Voltage** – The voltage applied between the input terminals to obtain zero output voltage. In Compar-

ators, it is the voltage applied to the input terminals to give the logic threshold voltage at the output. It is also defined as the input voltage differential required to give equal output currents from a matched pair of devices. (mV)

$\Delta V_{OS}/\Delta T$, ΔV, Δt — **Input Offset Voltage Drift** — The change in input offset voltage with time, voltage or temperature. ($\mu V/^{\circ}C$, V, s)

Input-Output Voltage Differential — The voltage range between the unregulated input voltage and the regulated output voltage in which a regulator operates within specifications.

R_{IN} — **Input Resistance** — The equivalent resistance seen looking into either input terminal with the other terminal grounded. ($M\Omega$)

I_R — **Input Reverse Current** — See Input HIGH Current. (μA)

Input to Output Delay — See Propagation Delay.

V_{IN} — **Input Voltage** — The voltage potential between the input terminal and the device ground reference. (V)

$V_{IN(MIN)}$ — **Input Voltage (Min)** — The minimum voltage required to bias the reference to specification limits. (V)

V_{IN} — **Input Voltage Range** — The range of voltage on an input terminal over which the device operates as specified. (V)

Large Signal Voltage Gain — The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

$\Delta V_{OUT}/\Delta V_{IN}$ — **Line Regulation** — The change in output voltage for a specified change in input voltage. (mV or %)

Linearity — The deviation of the characteristic from a straight line.

$\Delta V_{OUT}/\Delta I_L$ — **Load Regulation** — The change in output voltage for a specified change in load current. (mV or %)

L — **LOW** — Applying to a LOW voltage level.

t_{LZ} — **LOW to Disable** — The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

V_{ILMAX} — **Maximum input LOW voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

V_{IHMIN} — **Minimum input HIGH Voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{T-} — **Negative-going Threshold Voltage** — The input voltage of a variable threshold device that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$

Negative Current — Current flowing out of the device.

NF — **Noise Figure** — The ratio of the input signal-to-noise ratio to the output signal-to-noise ratio. Usually expressed as common log. (dB)

1/F Noise — The noise measured at a specified low frequency below the frequency range where the device noise spectrum is essentially flat. (nV)

A_{VOL} — **Open Loop Voltage Gain** — The ratio of the output signal voltage to the differential input signal voltage, with no feedback applied. (dB or V/mV)

Oscillator Control Sensitivity — The ratio of the change in oscillator frequency to the change in control voltage causing it.
Oscillator Pull-In Range — The range of free-running frequency over which the oscillator is locked to the incoming signal.

O — **Output.**

Output Common Mode Voltage — The arithmetic mean of the two output voltages for devices with differential outputs.

I_{OH} — **Output High Current** — The current flowing out of an output which is in the HIGH state.

V_{OH} — **Output HIGH Voltage** — The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

V_{OL} — **Output Low Voltage** — The maximum voltage at an output terminal sinking the maximum specified load current I_{OL} and at the minimum value of V_{CC}.

Z_O — **Output Impedance** — The equivalent impedance seen looking into the output terminal. (Ω)

I_{CEX} — **Output Leakage Current** — The leakage current into the output transistor at the specified output voltage potential for uncommitted or open-collector outputs. (μA)

I_{OL} — **Output LOW Current** — The current flowing into an output which is in the LOW state.

GLOSSARY (Cont.)

e_{no}	**Output Noise Voltage** – The rms value of the noise voltage measured at the output with constant load current and no input ripple. (μV)
I_{OZH}	**Output Off Current HIGH** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	**Output Off Current LOW** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.
	Output Offset Voltage – The voltage difference between the two outputs with both inputs grounded.
R_O	**Output Resistance** – The small signal ac resistance seen looking into the output with no feedback applied and the output dc voltage near zero. For comparators, it is the resistance seen looking into the output with the dc output level at the logic threshold. (Ω)
	Output Saturation Voltage – The dc voltage between output and ground in the saturated condition.
I_{SC}	**Output Short Circuit Current** – The current flowing out of an output which is in the HIGH state when that output is short circuited to ground (or other specified potential).
I_{SINK}	**Output Sink Current** – The maximum current into the collector of an open-collector device. (mA)
V_{OUT}	**Output Voltage** – The voltage present at the output terminal referred to ground. (V)
ΔV_{OUT}	**Output Voltage Range** – The range of output voltages over which the specifications apply. (V)
$\pm V_{OUT}$	**Output Voltage Swing** – The peak output voltage swing, referred to zero, that can be obtained wihtout clipping the output voltage waveform. (V)
	Overshoot – The difference between the peak amplitude of the output and the final value of the output divided by the output times 100%. (%)
$I_{OUT(Pk)}$	**Peak Output Current** – The maximum current delivered by the device for a period too short for thermal protection to be activated. (A)
	Phase Margin – The difference between 180° and the phase shift at the frequency where the open loop gain equals unity.
V_{T+}	**Positive-going Threshold Voltage** – The input voltage of a variable threshold device that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.
t_{PW}	**Pulse Width** – The time between the leading and trailing edges of a pulse.
	Power Bandwidth The maximum frequency at which the maximum output can be maintained without significant distortion.
	Power Consumption – The dc power required to operate the device under no load conditions.
$P_{D(MAX)}$	**Power Dissipation (Max)** – The maximum power that can be dissipated in the device with a given heat sink beyond which the device may not perform to specification. (mW)
I_{SS}	**Power Supply Current** – The current required from the power supply to operate the amplifier with no load and no signal applied. (mA)
PSRR	**Power Supply Rejection Ratio** – The ratio of the change in input offset voltage to the change in power supply voltage producing it. (μV/V)
	Power Supply Sensitivity – The ratio of the change of a specified parameter to the change in supply voltage.
t_{pd}	**Propagation Delay** – The time interval between application of an input voltage step and its arrival at the output.
I_Q	**Quiescent Current** – That part of a regulator input current that is not delivered to the load. (mA)
	Quiescent Output Current – The output current with no signal applied to the input.
I_{REF}	**Reference (Control) Current** – The current drawn or supplied by the reference (control) terminal. (μA)
V_{REF}	**Reference Voltage** – The output of the reference amplifier measured with respect to the negative supply. (V)
I_{RIN}	**Response Control Input Current** – The current flowing out of the response control pin that is available to charge the response control capacitor.
t_{resp}	**Response Time** – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level. (ns)
t_{rr}	**Reverse Recovery Time** – The time taken for the reverse recovery current to fall to a specified value after removal of the reverse bias under specified conditions. (ns)
t_R	**Release Time** – The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

GLOSSARY (Cont.)

Ripple Rejection – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage. (dB)

t_r **Rise Time** – The time interval required for a signal to rise from 10% to 90% of its final amplitude. (ns or μs)

Settling Time – The time from a step change of input to the time the corresponding output settles to within a specified percentage of the final value. (ns)

t_s **Set-up Time** – The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

Short-Circuit Current Limit – The output current of a regulator with the output shorted to common (ground). (mA)

Short-Circuit Load Current – The maximum output current which the device will provide into a short-circuit.

SR **Slew Rate** – The maximum rate of change of output under large signal conditions. (V/μs)

Standby Current Drain – The supply current drawn by a regulator with no output load and no reference voltage load (see Quiescent Current).

t_s **Storage Time** – The propagation delay due to stored charge in the transistor. (ns)

Strobe Activation Voltage – The voltage applied to the strobe terminal beyond which the device does not respond to the conditions at the input terminals. (V)

I_{Strobe} **Strobe Current** – The maximum current taken by the strobe terminal during activation. (μA)

Strobe Release Time – The time required for the outputs to rise to the logic threshold voltage after the strobe terminal has been activated.

Strobed Output Level – The dc output voltage, independant of input voltage, with the voltage on the strobe terminal in excess of the strobe activation voltage. (V)

I_{CC} **Supply Current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

Supply Regulation – The change in internal device supply voltage for a specified change in external power supply voltage.

V_{CC} **Supply Voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

Supply Voltage Rejection Ratio – See Power Supply Rejection Ratio.

Switching Speed – See Propagation Delay.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

Temperature Coefficient – See Average Temperature Coefficient of specific parameter.

$\Delta V_{OUT}/\Delta T_A$ **Temperature Stability** – The percentage change in output voltage over a specified ambient temperature range (V/°C)

Terminating Resistance – The resistance normally used to provide a termination to a transmission line.

V_{TH} **Threshold Voltage** – The input voltage at which the output logic level changes state. (V)

f_{MAX} **Toggle Frequency/Operating Frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

THD **Total Harmonic Distortion** – The rms value of the harmonic content of a signal expressed as a percentage of the rms value of its fundamental.

Transient Response – The closed loop step function response of the circuit under small signal conditions.

Transition Time, HIGH to LOW Output – See Fall Time.
Transition Time, LOW to HIGH Output – See Rise Time.

t_{PHL} **Turn-on Time** – See Propagation Delay Time, HIGH to LOW Output. (ns)

f_t **Unity Gain Bandwidth** – The frequency at which the open loop gain is reduced to unity. (MHz)

V_{TH+} **Upper Threshold Voltage** – The input voltage that causes the output to change logic stage, when the input voltage is increasing in a device with hysteresis.

A_V **Voltage Gain** – The ratio of the output voltage to the input voltage under small signal conditions. For comparators, it is the ratio of the change in output voltage to the change in voltage between the input terminals, with the dc output in the vicinity of the logic threshold. (dB or V/mV)

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