AMD Geode™ GX Processors Silicon Revision 2.1 Specification Update

Scope

This document discusses known issues of silicon revision 2.1 of the AMD Geode™ GX processors (i.e., Geode GX 533@1.1W processor*, Geode GX 500@1.0W processor*, and Geode GX 466@0.9W processor*). The table below provides a summary of the issues. A detailed description of each issue, its impact and a recommended resolution/fix follow.

The silicon revision number, 2.1, is printed on the top-side of the package following the Geode GX processor's marking.

Software Readable IDs for Rev 2.1

- Geode GX Processor Silicon Revision:
  — MSR 4C000017h[7:0] = 21h
- Device (Module) Revisions:
  — CPU Core: MSR 00002000h[7:0] = 02h
  — GLIU0: MSR 10002000h[7:0] = 01h
  — GLMC: MSR 20002000h[7:0] = 01h
  — GLIU1: MSR 40002000h[7:0] = 01h
  — GLCP: MSR 4C002000h[7:0] = 01h
  — GLPCI: MSR 50002000h[7:0] = 01h
  — GIO: MSR 54002000h[7:0] = 00h
  — DC: MSR 80002000h[7:0] = 01h
  — GP: MSR A0002000h[7:0] = 00h
  — VP: MSR C0002000h[7:0] = 01h

Note: This is revision E of this document. The change from revision D (dated October 2004) is added issue 1.1 and made the document non confidential.

Issue Summary

Issue #[1]	Description
1.0 Common Issues	
1.1	Changing VGA resolution on-the-fly can hang the display controller
1.4	Branch prediction circuit requires special configuration
1.5	GLPCI fails to detect bad data parity on the last data phase of outbound read
1.6	Clock gating causes JTAG read data errors
1.7	VGA Enable configuration bit does not stop VGA CRTC
1.9	Graphics hang can occur during VGA mode change
1.12	Cursor, icon, and border colors do not display correctly in 32-bit alpha mode
1.14	Unpacked monochrome expansion BLTs with width less than 8 pixels fail
1.15	Limit fault during exception in SMM with unreal code segment
1.18	VGA Input Status Register 1 non-functional during VESA, DC modes
1.19	GLPCI write combining can break ordering rules
1.20	VGA memory accesses can hang after a mode switch
1.21	General protection faults (GPFs) may be missed if a jump instruction straddles the CS limit boundary
1.22	GLPCI reread of prefetched read data
1.23	CR4 not reset correctly
1.24	Strange horizontal lines during vertical vectors and BLTs
1.25	Some VGA modes do not display full screen correctly on larger resolution panels

*The AMD Geode GX 533@1.1W processor operates at 400 MHz, the AMD Geode GX 500@1.0W processor operates at 366 MHz, and the AMD Geode GX 466@0.9W processor operates at 333 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodegxbenchmark.

Issue Summary (Continued)

Issue #[1]	Description
1.26	YUV to RGB Color Space Converter is inaccurate
1.27	Maskable interrupt immediately after STI instruction failure
1.28	GLCP CPU throttling does not match ACPI specification
1.29	Main GLIU clock domain does not awaken when statistics counter generates an ASMI
1.30	Video DAC Palette Mask register (Address 3C6h) always reads 00h
1.31	Minimum spaced consecutive reads fail on PCI bus
1.32	HSYNC, VSYNC, and REQ1# fail ESD rating
1.33	Write allocate causes failure
1.34	Register in Display Controller is write only
1.35	I/O's internally tied to V_{MEM}
1.36	Segment register misuse in AC stage of CPU execution pipeline
1.37	Screen corruption occurs with heavy PCI activity
1.38	Writes to the gamma RAM sometimes fail
1.39	PLL may not restart from S1
1.40	Access to unimplemented memory address space causes hang
1.41	Two DIMMs do not work reliably at a memory speed of 266 MHz
1.42	Possible character corruption in VGA text modes
2.0 CRT Issues (No issues.)	
3.0 FP Issues (No issues.)	

1. Issue numbers may not be sequential since issues are omitted once they are resolved.

Issues

1.0 Common Issues

1.1 Changing VGA resolution on-the-fly can hang the display controller

Description: When running on a flat-panel display, if the CRTC settings are modified while the display is active, an internal state machine can hang. There are some applications (Including the Red-Hat installation program and Quake) that do this.

Implications: If an application changes the CRTC settings as described above, the display controller will hang. Only the display controller is hung, all other operations of the Geode™ GX processor are still active.

Resolution: None. Avoid modifying the CRTC settings while the CRTC is running. The CPU has not crashed due to this issue, and a subsequent sequencer reset (or mode switch) rectifies the problem.

1.4 Branch prediction circuit requires special configuration

Description: The branch prediction circuit predicts whether or not a branch is taken and stores a small cache of targets for those predicted branches. This circuit does not work correctly.

Implications: A correctly working branch prediction circuit increases CPU performance. With the branch prediction not working, the performance gain is not realized.

Resolution: A workaround has been implemented that utilizes some of the internal diagnostics capabilities of the Geode GX processor. The workaround has a performance impact of less than 1% overall. The MSR writes to GLIU0 and the GLCP must occur before the branch prediction circuit is enabled. Clock throttling and SYSENTER/SYSEXIT must also be disabled for correct operation.

MSR 4C000016h	00000000_00000000h
MSR 4C000016h	00000000_00000001h
MSR 10002005h	00000000_80330000h
MSR 4C000045h	5AD68000_00000000h
MSR 4C000044h	00000000_00000140h
MSR 4C00004Dh	00002000_00000000h
MSR 4C000075h	00000000_00400000h
MSR 4C000073h	00000000_00030000h
MSR 4C00006Dh	00000000_00430000h
MSR 4C00005Fh	00000000_80004000h
MSR 00003003h	0080A13D_00000000h

1.5 GLPCI fails to detect bad data parity on the last data phase of outbound read

Description: During an outbound memory read transaction, with the target returning bad parity (wrong value of PAR) on the last data phase, the GLPCI does not detect a parity error.

Implications: PCI spec violation. Exception will not occur if parity error occurs in this case.

Resolution: None. PCI parity generation and detection are normally not used.

1.6 Clock gating causes JTAG read data errors

Description: When attempting to read GLCP MSRs through the JTAG interface with clock gating enabled, the reads may return incorrect values.

Implications: Reading MSRs through the JTAG interface with GLCP clock gating enabled is unreliable.

Resolution: Turn GLCP clock gating off via GLD_MSR_PM (MSR 4C002004h[1:0] = 00) before attempting MSR reads through the JTAG interface. Only GLCP clock gating is affected by this issue

1.7 VGA Enable configuration bit does not stop VGA CRTC

Description: The VGA Enable configuration bit (DC Memory Offset 004h[7]) masks off the VGA memory requests and color data from the DC pipeline, but does not shut down the VGA CRTC/sequencer.

Implications: VGA power management will not work properly and the VGA VSYNC generates an SMI if the appropriate mask is not set (MSR 80002002h[3]).

Resolution: Follow this procedure.

1. Set the SCREEN_OFF bit in the VGA Sequencer Register (SQ Index 01h[5] = 1).

2. Wait at least 50 µs for the VGA to stop fetching data.

3. Clear the Sequencer Reset Register (SQ Index 00h[1:0] = 00).

4. Clear the VGA Enable bit. (DC Memory Offset 004h[7] = 0).

1.9 Graphics hang can occur during VGA mode change

Description: If a write sequence occurs to the VGA hardware that causes a display mode change, the Display Controller can hang and ultimately cause the system to hang.

Implications: VGA mode changes can cause a graphics hang.

Resolution: Disable the Display Controller clock gating. Write a 0 to MSR 80002011h (undocumented register in data book, publication #31505). Just before a mode switch, turn off Timing Generator Enable (TGEN, DC Memory Offset 08h[0]) and wait 20 µS before deactivating Data Fifo Load Enable (DFLE, DC Memory Offset 04h[0]). This has been shown to completely avoid the problem. Power consumption is not measurably affected.

1.12 Cursor, icon, and border colors do not display correctly in 32-bit alpha mode

Description: In 32-bit graphics modes where per-pixel alpha is sent via the Display Controller to the external digital RGB interface, the 24-bit color value is dithered and reduced to 16 or 19 bits. The per-pixel alpha value is placed on the remaining 8 or 5 bits of the output. Because dithering and muxing occur early in the DC pipeline, the cursor, icon, and border colors (added near the end of the DC pipeline, via the palette RAM) are not modified appropriately.

Implications: Curser, icon, and border colors cannot be used in the normal way when performing per-pixel alpha blending.

Resolution: Program the palette RAM entries for cursor, icon, and border with entries that are already in the 8:5:6:5 or 5:6:7:6 (ARGB) format.

1.14 Unpacked monochrome expansion BLTs with width less than 8 pixels fail

Description: Unpacked monochrome expansion BLTs with a width of less than 8 pixels do not work correctly.

Implications: Cannot perform unpacked monochrome expansion BLTs with a width of less than 8 pixels.

Resolution: None.

1.15 Limit fault during exception in SMM with unreal code segment

Description: When an exception or other intersegment change of flow (COF) occurs inside an SMI handler and the target offset is higher than the SMI handler's code segment (CS) limit, a spurious general protection fault for a segment limit violation may occur. The CS limit, normally FFFFh in real mode, can be set to a smaller value inside SMM with RSM or with an MSR write. When fetching the first instruction of an exception handler, or the target of a far jump, the CPU mistakenly uses that shortened CS limit instead of the implicit limit of FFFFh that would normally apply to a real mode code segment. This leads to an erroneous general protection exception.

Implications: Exceptions may generate a limit fault when a COF occurs while in SMM.

Resolution: Leave the SMM's code segment limit at FFFFh, or put any SMM exception handlers and intersegment COF targets lower in their segment, at offsets that are less than the SMM CS limit.

1.18 VGA Input Status Register 1 non-functional during VESA, DC modes

Description: The VGA's Input Status Register 1 (I/O Address 3BAh or 3DAh) includes status bits to indicate the state of vertical sync and display enable. When the DC is driving the timings directly and the VGA hardware is disabled, the state of this register is not updated by the DC logic. This occurs in some VESA modes.

Implications: Any software that reads the status bits when in VESA, where the VGA hardware is disabled, will not work correctly.

Resolution: None. No software other then internal test software has exposed this issue, and none is expected.

1.19 GLPCI write combining can break ordering rules

Description: During a PCI write cycle, where the Geode GX processor is the target, the write combining logic in the GLPCI can cause incorrect ordering of data on the GLIU.

Implications: The write combining feature in the GLPCI can not be used.

Resolution: Disable GLPCI write combining by programming the IWC bit in the GLPCI Global Control register to 0 (MSR 50002010h[3]).

1.20 VGA memory accesses can hang after a mode switch

Description: If the Data FIFO Load Enable bit (DFLE) (DC Memory Offset 04h[0]) is turned off while the DC is actively fetching data, a counter may get out of sync. This counter is used to determine when to switch between data fetches for display refresh and data fetches for host accesses to the VGA frame buffer. Subsequent reads or writes to VGA frame buffer space will be held off forever, resulting in a system hang.

Implications: The system will hang.

Resolution: Turn off the Timing Generator Enable (TGEN) bit (DC Memory Offset 08h[0] = 0) and wait about 20 µs before deactivating DFLE.

1.21 General protection faults (GPFs) may be missed if a jump instruction straddles the CS limit boundary

Description: A GPF may be missed when a conditional jump instruction spans the CS limit and is predicted not-taken by PF, but is determined to be taken by EX.

Implications: This condition should produce a GPF, but does not. However, GPFs are not part of properly functioning programs.

Resolution: None.

1.22 GLPCI reread of prefetched read data

Description: Out-bound transactions always force a flush of the prefetched read data.

Implications: Some system performance is lost (much less then 1%).

Resolution: None.

1.23 CR4 not reset correctly

Description: INIT does not reset CR4.

Implications: CR4 is in an unknown state at reset.

Resolution: Startup software can not assume that CR4 begins with a value of zero. The following instructions must be used to clear CR4: XOR EAX, EAX MOV CR4, EAX.

1.24 Strange horizontal lines during vertical vectors and BLTs

Description: Vertical vectors rendered using BLTs with a width of 1 pixel and no source data cause wide horizontal stripes to be painted across the screen during the BLTs.

Implications: This type of BLT can fail.

Resolution: Set the Source Mode bits in GP_BLT_MODE as unpacked monochrome (GP Memory Offset 40h[7:6] = 01) when initiating a BLT that does not require source data. This action provides source data to the hardware that is not used. This avoids the failure.

1.25 Some VGA modes do not display full screen correctly on larger resolution panels

Description: The fixed timing controller in the VGA module prevents it from displaying images full screen that are less than half of the panel height. For example, with a panel of 1024x768, VGA modes of less than 384 lines are affected. This includes VGA modes 10h and 0Fh. With a panel larger than 960 lines, 1280x1024 for example, all VGA modes are affected.

Implications: For the larger panel resolution, many VGA modes cannot be viewed full screen, and for panels with greater than 960 lines, no VGA modes can be viewed full screen.

Resolution: These modes can be displayed as centered images (with a large border). Use AMD graphics drivers instead of standard VGA modes whenever possible.

1.26 YUV to RGB Color Space Converter is inaccurate

Description: The YUV to RGB Color Space Converter (CSC) has rounding errors that produce errors as large as +/-5 points. See the document titled AMD *Geode™ GX Processors YUV to RGB CSC Correction* (publication #31536) for more details.

Implications: The YUV to RGB CSC's conversions are inaccurate. This affects the video frame buffer's quality when rendered on either a CRT monitor or FP display.

Resolution: The gamma RAM in the Video Processor can be used to improve but not completely correct the accuracy of the conversion. See the document titled AMD *Geode GX Processors YUV to RGB CSC Correction* (publication #31536) for more details.

1.27 Maskable interrupt immediately after STI instruction failure

Description: According to the x86 rules; when an STI instruction is followed immediately by a RET or SYSEXIT instruction, maskable interrupts are not to be allowed until after the RET or SYSEXIT instruction completes. The CPU core can violate this rule if an external stall occurs just after the STI command. In rare cases, this can allow an interrupt to get processed at a higher priority than usual.

Implications: In normal operation this issue has not been shown to cause any failures when the next instruction is a RET. If the next instruction is a SYSEXIT, failures have been observed.

Resolution: SYSENTER/SYSEXIT is an advanced feature that is identified in the feature flags of CPUID. BIOS must disable the SYSENTER/SYSEXIT feature by writing to the CPUID3 register, MSR 00003003h [43] = 0.

1.28 GLCP CPU throttling does not match ACPI specification

Description: A duty cycle setting of 15 in the CPU clock throttling implementation results in no throttling. The ACPI specification expects the CPU to be active 15/16ths of the time with this setting. Note that all other settings are slightly off. A setting of 14 results in 14/15ths in the Geode GX processor instead of the ACPI specified 14/16ths.

Implications: The result of this deviation is the CPU P State test in Microsoft® HCT (Hardware Compatibility Test) fails. The test expects minimal throttling to occur when it programs a duty cycle of 15, however, the Geode GX processor runs full speed with this setting.

Resolution: None.

1.29 Main GLIU clock domain does not awaken when statistics counter generates an ASMI

Description: When the GLIU statistics counters are in use, they generate ASMIs under certain conditions. These counter functions work correctly. The primary GLIU logic and these counters operate on different clock domains and hence have separate controls in GLD_MSR_PM (GLIU0 MSR 10002004h and GLIU1 40002004h). There are domains zero and one respectively. If hardware clock gating is enabled for domain zero and a statistics counter generates an ASMI, the domain zero clock should wakeup to pass on the ASMI. However, it does not.

Implications: If the statistics counters are used in a mode that generates an ASMI, then any given ASMI could be lost if hardware clock gating is enabled for domain zero.

Resolution: If the statistics counters are used in a mode that generates an ASMI, then leave hardware clock gating off for domain zero.

1.30 Video DAC Palette Mask register (Address 3C6h) always reads 00h

Description: The Video DAC Palette Mask register (Address 3C6h) always reads back 00h. When written it behaves properly by accepting a non-zero value.

Implications: Although no specific VGA applications have been identified, those that change the palettes or access them often and expect to read back a non-zero mask value will have problems. An additional issue may arise if the system goes into Save-to-RAM with a mask of something other than 0FFh (all colors enabled) because the Save-to-RAM code always saves the mask as 0FFh and restores it to that value. Under that scenario, the display will have unexpected colors.

Resolution: None.

1.31 Minimum spaced consecutive reads fail on PCI bus

Description: If two reads occur on the PCI bus that are spaced with 0 or 1 clock, the address of the second read will not be correctly interpreted and the second read may fail.

Implications: Consecutive reads that are spaced by 0 or 1 clock can not be done

Resolution: Disable fast back-to-back reads in the Virtual PCI Header. This will further reduce the already low probability of the failing condition.

Most PCI devices do not perform fast back-to-back reads. Any devices that do, can not be used.

1.32 HSYNC, VSYNC, and REQ1# fail ESD rating

Description: HSYNC, VSYNC, and REQ1# do not meet the ESD Machine Model immunity rating of 200V as indicated in Table 6-1 “Absolute Maximum Ratings” of the *AMD Geode™ GX Processors Data Book*. HSYNC, VSYNC, and REQ1# pass at 150V.

Implications: Special care may be required when handling the parts.

Resolution: None.

1.33 Write allocate causes failure

Description: When a write allocate request to the data cache and an instruction request from the prefetch queue to the instruction cache occur simultaneously, the instruction request sometimes gets the data from the write allocate request.

Implication: Write allocate function is not reliable.

Resolution: Disable write allocate. Bit 1 in all the Region Configuration Registers, MSR 00001808h through 00001817h, must be written to 0.

1.34 Register in Display Controller is write only

Description: The ExtendedStartAddress register (CRTC Index 44h) is write only.

Implication: Read/Modify/Write operations will fail. Save-to-RAM implementation cannot read this register during save and write the saved contents during restore.

Resolution: Do not use the ExtendedStartAddress register. This register is also accessible via the VGA Extended Start Offset register (DC Memory Offset 108h). Always use the VGA Extended Start Offset register since it is a read/write register.

1.35 I/O's internally tied to V_{MEM}

Description: JTAG signals TCLK and TDI are internally connected to V_{MEM}.

Implication: For DDR SDRAM systems, V_{MEM} is 2.5V. There will be a higher input current through the pull-up resistors that are connected to these signals. The extra current is not damaging. A JTAG tester may drive the signals to 3.3V and if the current is sufficient, damage to the I/Os may result.

Resolution: Connect the pull-up to V_{MEM} to prevent excessive current. If a JTAG tester is connected, ensure that the voltage does not exceed 2.5V. Use level-shifting if necessary.

1.36 Segment register misuse in AC stage of CPU execution pipeline

Description: When a specific instruction sequence is executed (example shown below), the AC stage of the CPU execution pipeline puts the wrong data into the segment register. The “movsb” instructions that are speculatively executed and the two loads of the segment register following the “jz” are required for the failure to manifest.

```
jz MISSY: ;Conditional jmp will be taken
   movsb ;This code is not executed but the branch
   movsb ;prediction logic will cause speculative
   movsb ;execution until jump is resolved
   hlt
MISSY:
   mov es,bx ;First mov to ES is correct
   mov es,cx ;Second mov to ES is incorrect
```

Implications: Code sequences as described above cause the CPU's execution pipeline to incorrectly execute. This faulty execution was discovered in random simulation testing. This type of code sequence is extremely unlikely in real code. Back to back loads to the same segment register is considered abnormal code and has not been observed in any runtime operation.

Resolution: None. Avoid the abnormal code sequence.

1.37 Screen corruption occurs with heavy PCI activity

Description: This issue on occurs when operating the PCI bus at 66 MHz. If PCI traffic is heavy, sometimes the Display Controller cannot gain timely access to the graphics frame buffer memory and its FIFO underruns causing intermittent screen corruption. The Geode GX processor has a unified memory architecture (UMA), meaning that the CPU and the graphics subsystem use the same physical memory space. Most PCI memory activity causes cache snoops. These snoops can create a significant amount of memory management activity to make sure the memory remains coherent. This activity delays other requests, specifically the Display Controller to the memory controller. Gig ethernet controllers and USB v2.0 controllers have been observed to create this issue.

Implication: Temporary screen tearing can occur if the PCI bus is operating at 66 MHz with high PCI traffic and a screen resolution at or above 1280x1024@85 Hz.

Resolution: A workaround has been implemented in the BIOS using some of the internal debug capabilities of the Geode GX processor. This workaround throttles PCI traffic by inserting dummy requests into the same GLIU that the PCI bus is connected to. This throttling reduces the available PCI bandwidth up to 25% at the higher graphics resolutions, but prevents the screen tearing. PCI available bandwidth goes from a measured 193 MB/sec to 143 MB/sec. This workaround can be disabled if not needed. This workaround should only be implemented in systems that operate the PCI bus at 66 MHz and have high PCI traffic.

1.38 Writes to the gamma RAM sometimes fail

Description: CPU writes to the gamma RAM in the Video Processor randomly fail. This is caused due to a synchronization problem between the GLIU clock and graphics clock domains. Varying the GLIU and graphics clock frequencies can increase or decrease the failure rate.

Implications: Video or graphics image corruption can occur if the gamma RAM is used.

Resolution: Enabling the gamma RAM before changing the contents prevents the synchronization problem. Write GAM_EN = 0 in the Video Processor, (VP Memory Offset 050h[0]) and wait one vertical sync time. The GAM_EN bit is latched by VSYNC before taking effect.

1.39 PLL may not restart from S1

Description: The PLL post-divide logic that feeds the CPU can get into an illegal state if the PLL is powered down and then powered up without a hard or soft chip reset active. In S1, PCI clocks are shut off to produce a low power state for the system.

Implications: The PLLs and PCI clock must remain powered and running when the ACPI state S1 is entered or S1 cannot be used. S3 or S5 can be used normally since these states use a chip reset to restart the system.

Resolution: The PLLs must be left on when in S1.

1.40 Access to unimplemented memory address space causes hang

Description: A portion of the assigned memory range in the Video Processor, VP Base+C00h through VP Base+FFFh, is not used by the Video Processor. Accessing this space should simply result in invalid data, but instead results in a hang. The decode of this address range is programmed in one of the GLIU decode descriptor MSRs.

Implications: Performing a memory access (read or write) with an address between VP Base+C00h through VP Base+FFFh will result in a system hang.

Resolution: None. Avoid this address range.

1.41 Two DIMMs do not work reliably at a memory speed of 266 MHz

Description: Parallel termination is required when this memory configuration is used. The DQS output pre-amble from the CPU appears to be in spec, but not sufficiently to function properly when two DIMMs are installed. The maximum loading on the DQS outputs when two DIMMs are installed reduces the timing margin.

Implications: Two DIMMs are not supported, when using the AMD Geode GX 533@1.1W (400 MHz) SKU with a memory speed of 266 MHz.

Resolution: Limited testing has shown that 75 ohm terminations on the DQS signals may result in a stable memory subsystem. Contact you local AMD sales office for more information on this possible workaround.

1.42 Possible character corruption in VGA text modes

Description: Some devices exhibit corruption of the first two columns of characters in VGA text modes. The corruption can appear as shimmering dots or as horizontal dashes that appear on the left side of the screen (first two columns of characters). It can also appear as character pixels that are the wrong color. The corruption typically appears on alternating scan lines in VGA Mode 3 (the most common text mode), although in other text modes with VGA line doubling enabled, it may occur on fewer lines. Enabling the VGA fixed-timings stretch mode (used for TFT displays) will also affect the appearance of the corruption. This is a VGA text mode issue only.

Implications: Systems that have a BIOS summary screen and/or setup screens, use DOS as the operating system, full screen DOS box in Windows® XP/XPe or Linux console without frame buffer driver can experience this issue. VGA text modes are often used to support development efforts but are not used in the final product. Applications that use graphics drivers or VGA graphics modes will not experience this problem.

Resolution: Avoid the use of VGA text modes whenever possible. For BIOS summary and setup screens use a VGA graphics mode. For DOS, Windows XP/XPe DOS box and Linux console, there is no workaround.

2.0 CRT Issues

None.

3.0 FP Issues

None.

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